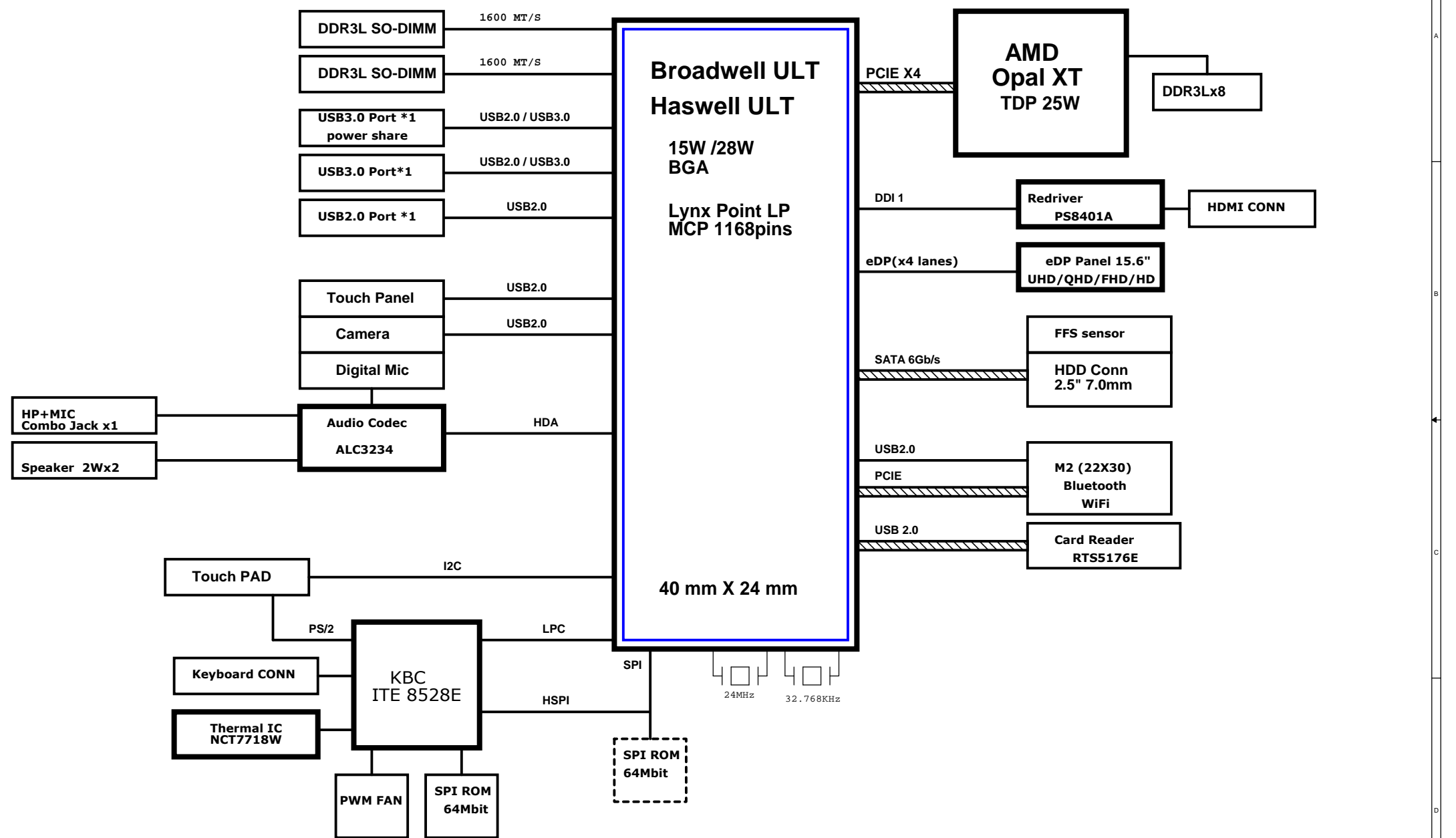


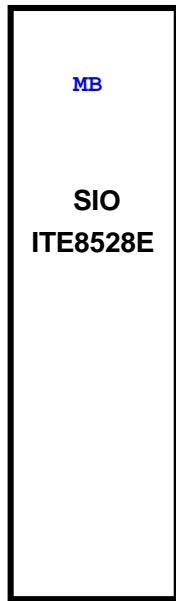
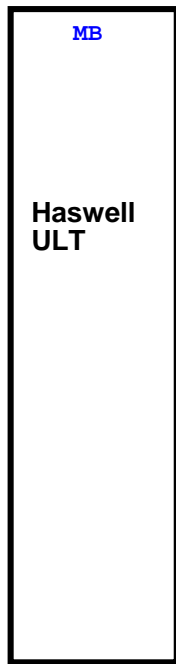
AM6 BLOCK DIAGRAM



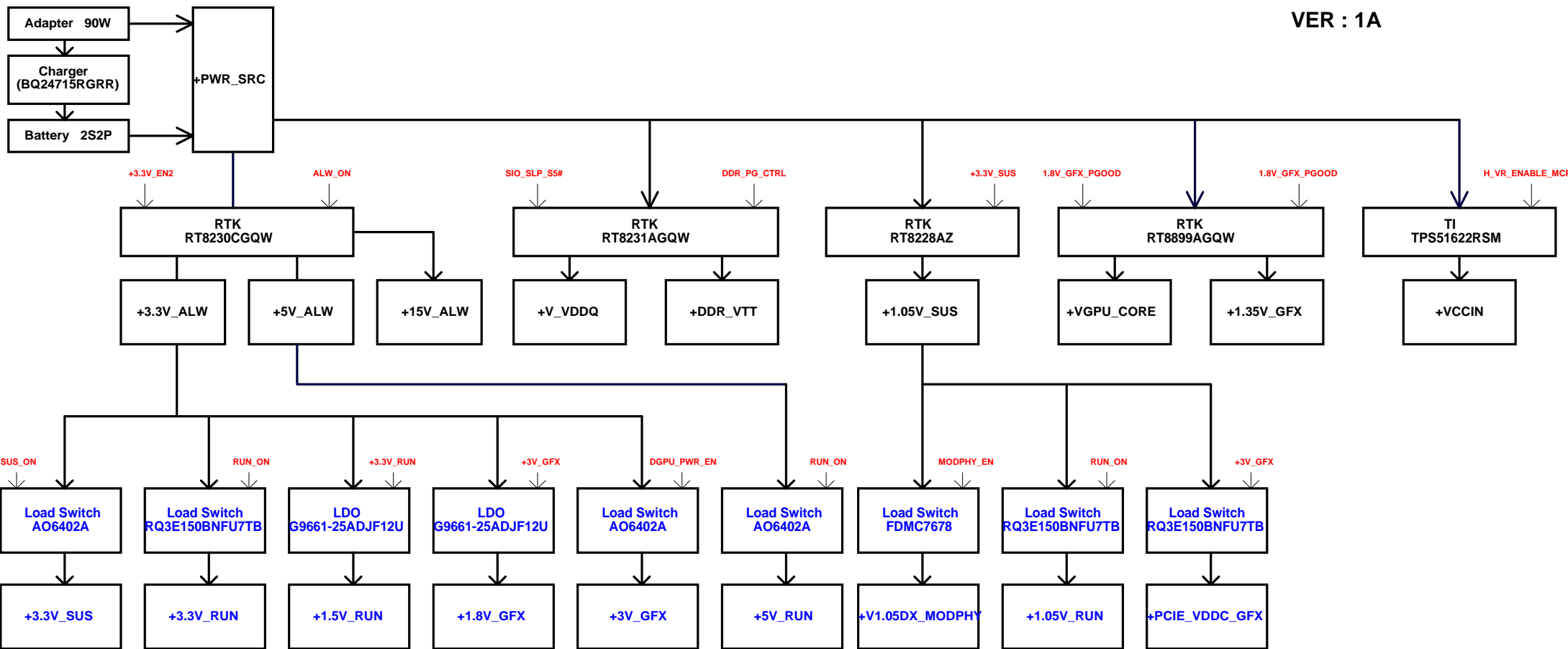
HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 Left Power Share		
2	USB3.0_2 Right		
3	USB3.0_3 X	PCIE1 X	
4	USB3.0_4 X	PCIE2 X	
5		PCIE3 X	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 X
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 X
CLK2 X
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

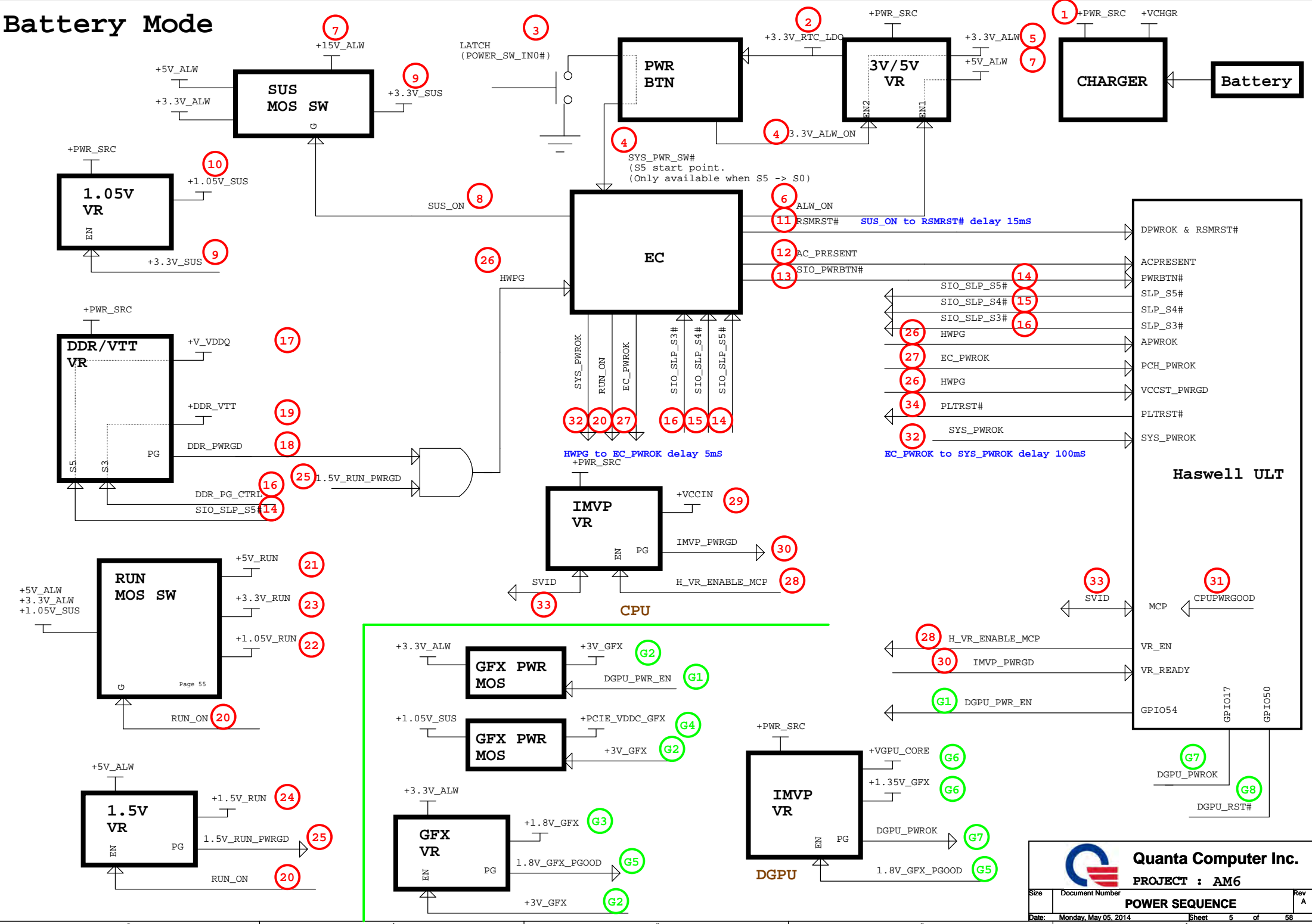
USB2.0
USB2.0_0 Left Power Share
USB2.0_1 Right /w 3.0
USB2.0_2 Right
USB2.0_3 Card Reader
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 X



	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	BQ24715RGRR	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	DIMM A	SPD	(A0h)
	DIMM B	SPD	(A4h)
	Free-fall sensor	LNG3DMTR	(50h)
I2C	Touch Pad		(2Ch)

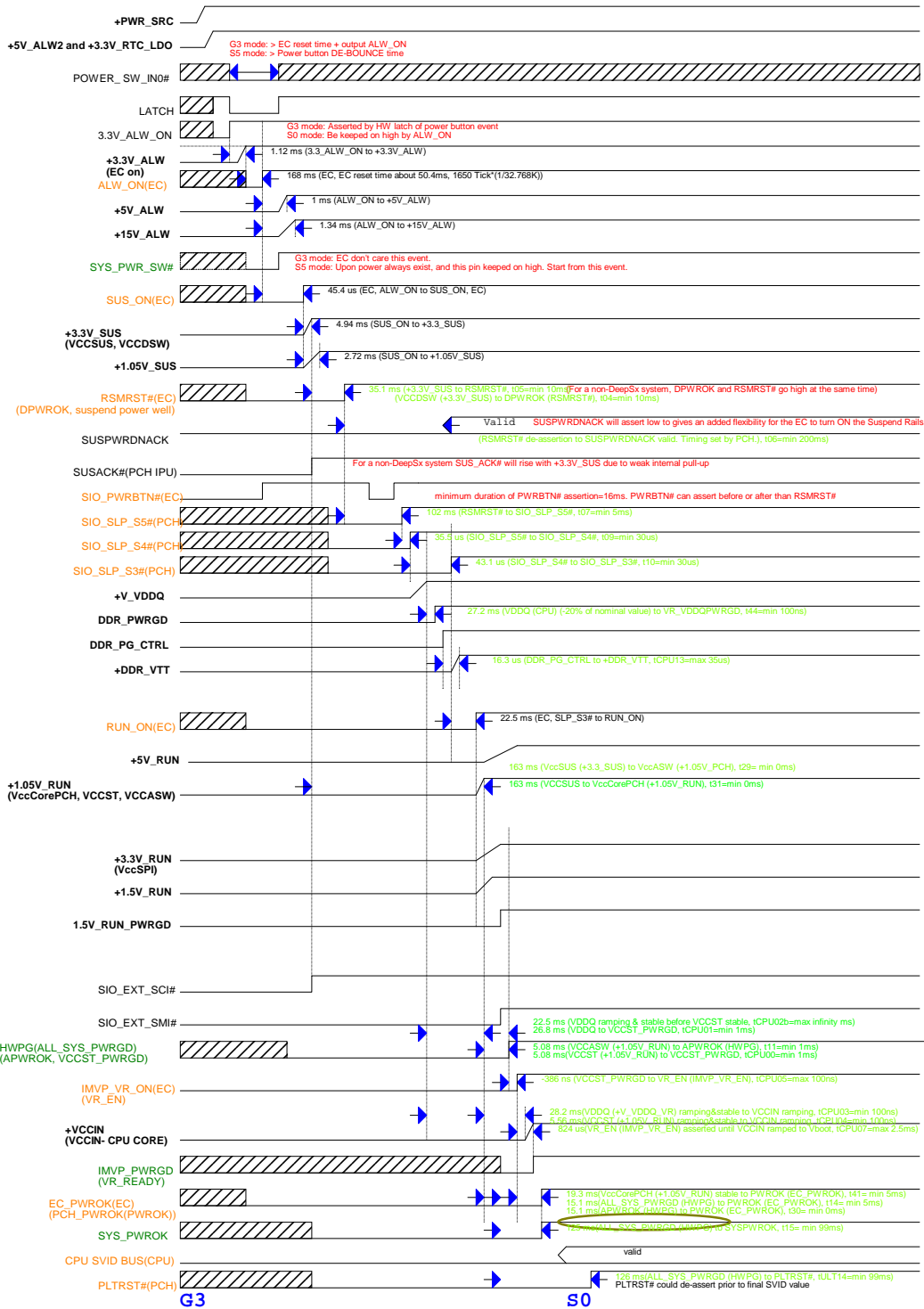


Battery Mode

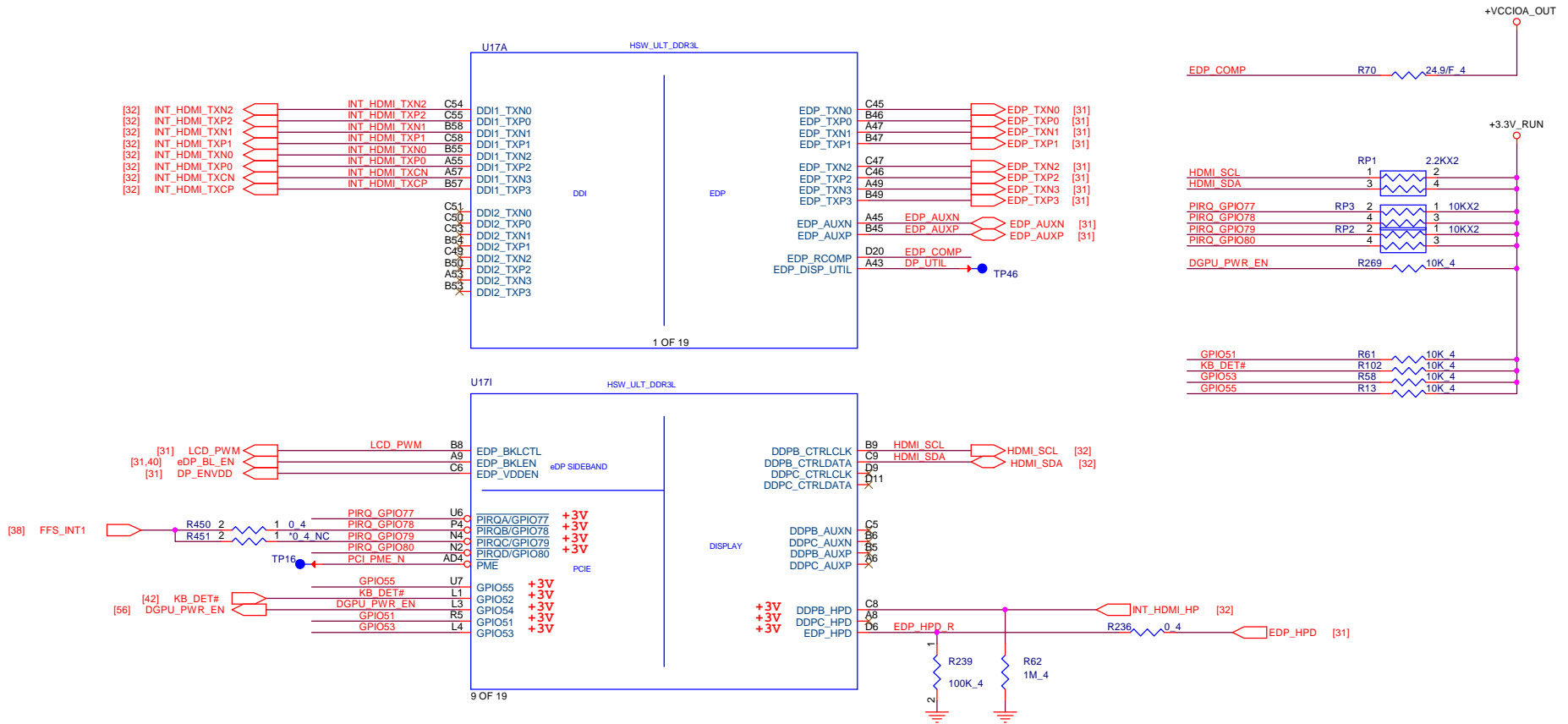


Power Sequence (G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1



Haswell ULT (DISPLAY)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DDPB_CTRLDATA	Port B Detected	PCH_PWROK	0 = Port B is not detected. 1 = Port B is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. PU 2.2K to +3.3V_RUN
DDPC_CTRLDATA	Port C Detected	PCH_PWROK	0 = Port C is not detected. 1 = Port C is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. NC

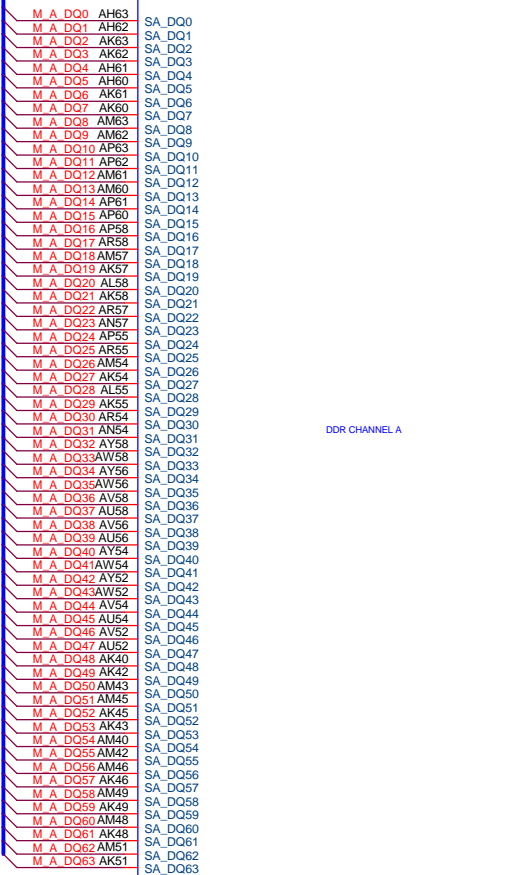
Haswell ULT (DDR3L)

[19] M_A_DQ[63..0]

[20] M_B_DQ[63..0]

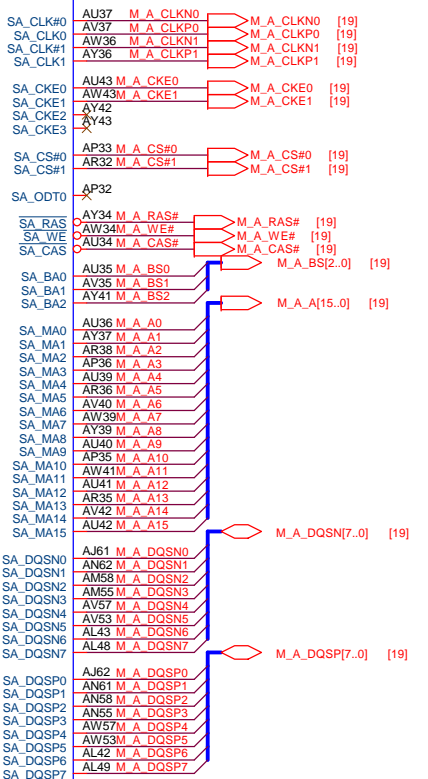
U17C

HSW_ULT_DDR3L



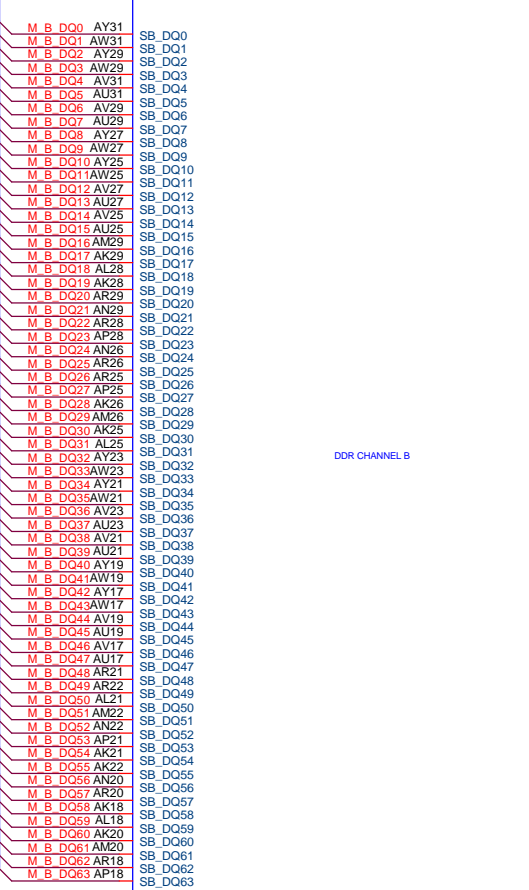
DDR CHANNEL A

3 OF 19



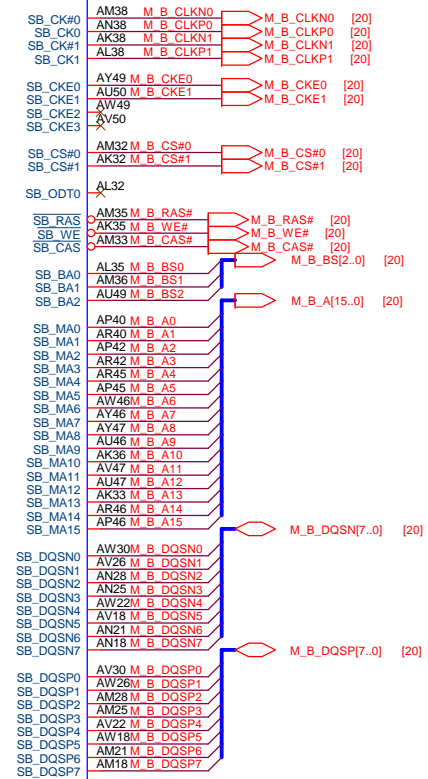
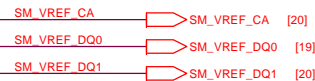
U17D

HSW_ULT_DDR3L



DDR CHANNEL B

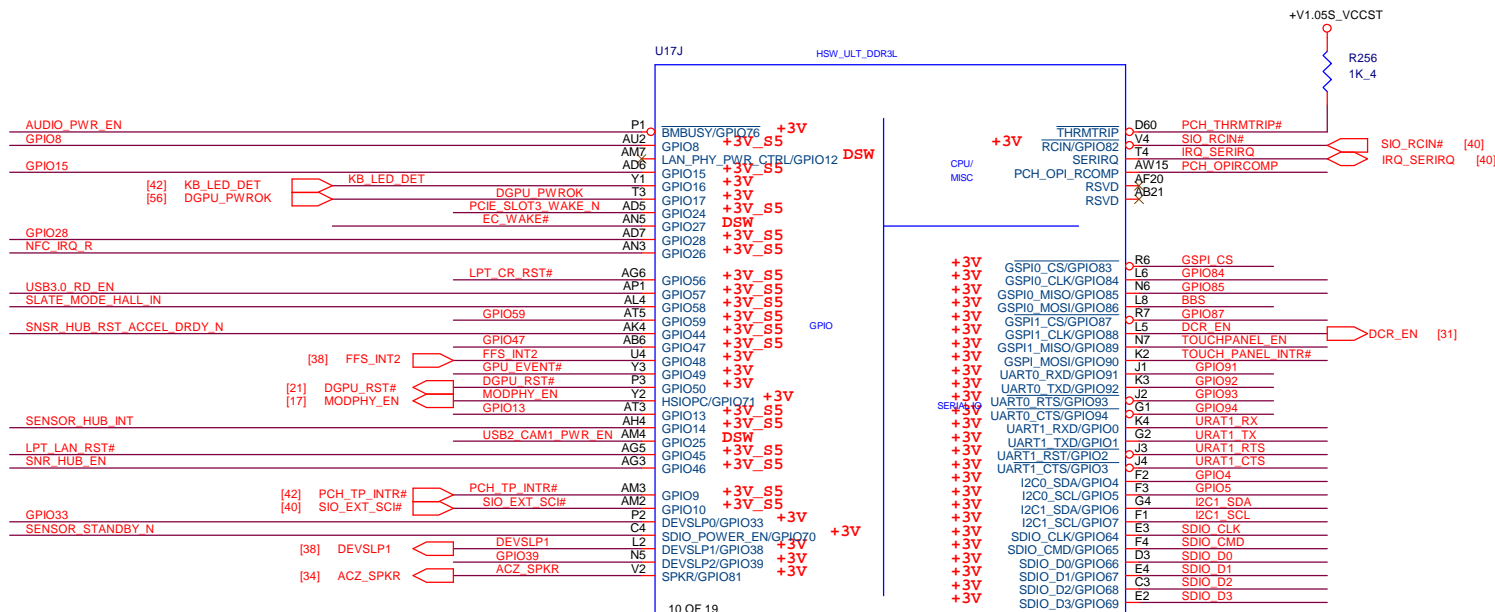
4 OF 19



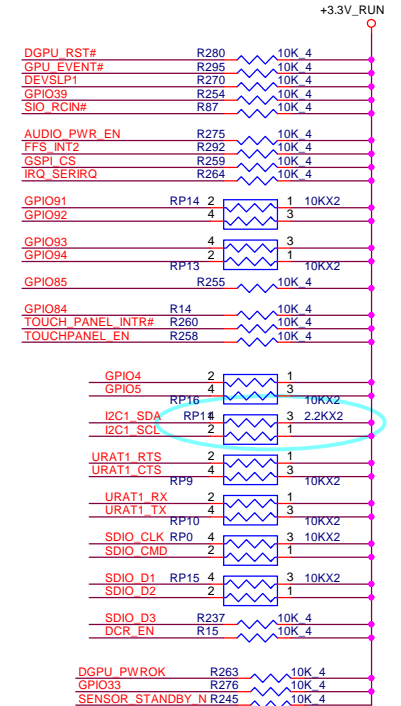
Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Haswell ULT 2/12	A
Date:	Monday, May 05, 2014	Sheet 8 of 58

Hasswell ULT (GPIO, LPIO, MISC)

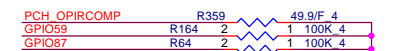
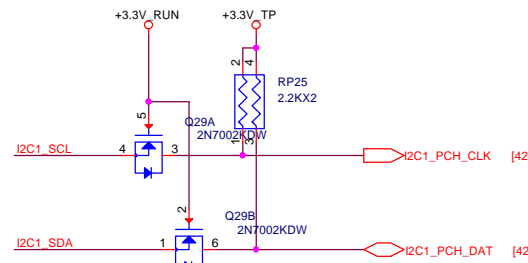
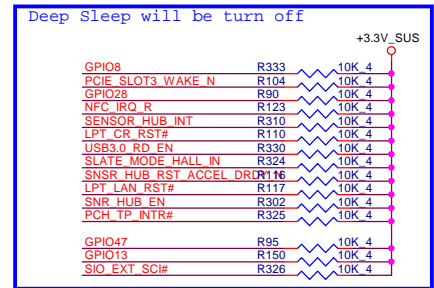
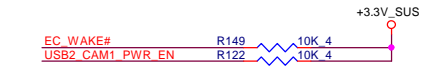


GPIO Pull-up/Pull-down (CLG)

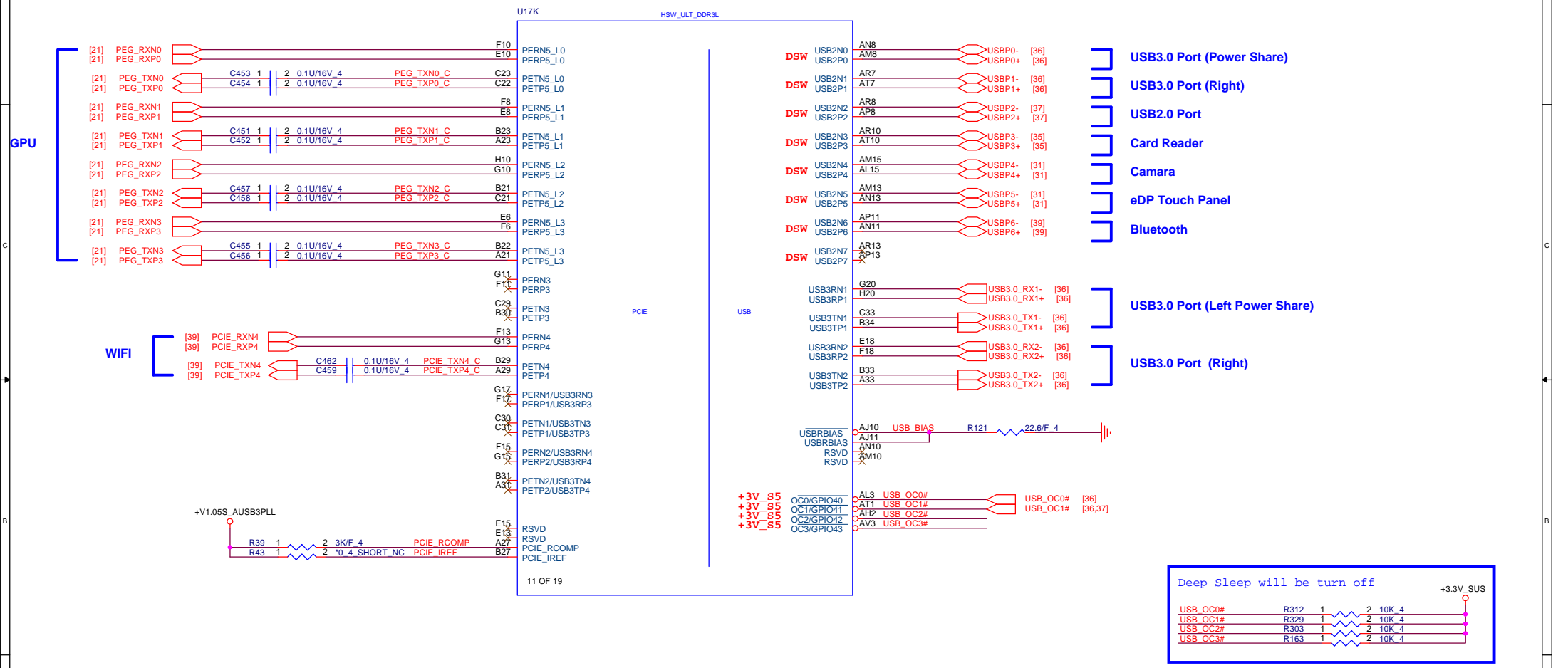


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable 1 = Enable	This signal has a weak internal pull-down. Deep Sleep will be turn off. +3.3V_SUS ○ R103 10K_4_NC GPIO15
SPKR/GPIO81	No Reboot mode	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down. NA
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = SPI 1 = LPC	This signal has a weak internal pull-down. +3.3V_RUN ○ R265 1K_4_NC BBS
SDIO_D0/GPIO66	Top Swap Override	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down. +V3.3S_1.8S_LPSS_SDIO ○ R21 1K_4_NCSIO_D0

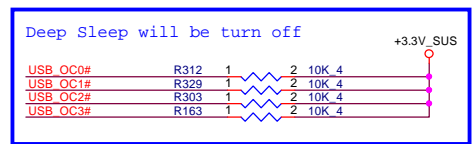


Haswell ULT (PCIE,USB)

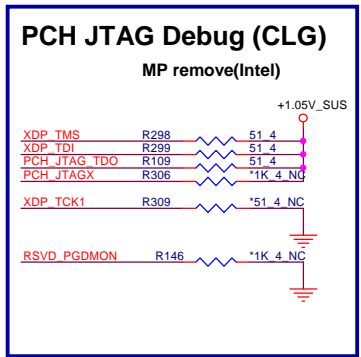
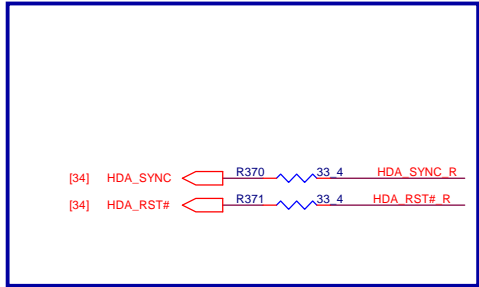
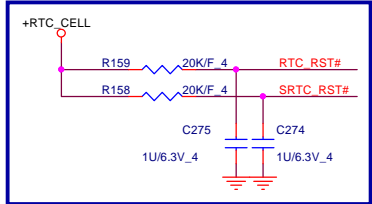
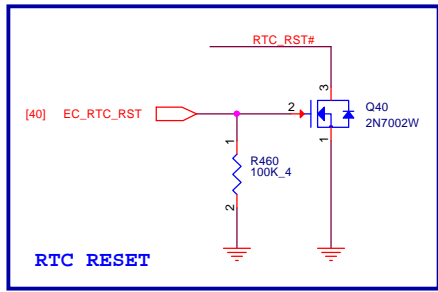
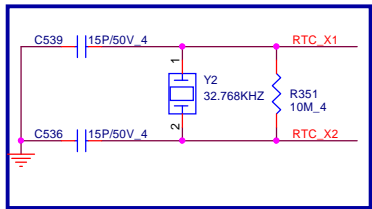


Overcurrent Pin Setting

Pin	Default Port Mapping	AM6 setting
OC0#	Port 0, Port 1	Port 0
OC1#	Port 2, Port 3	Port 1, Port 2
OC2#	Port 4, Port 5	no use
OC3#	Port 6, Port 7	no use



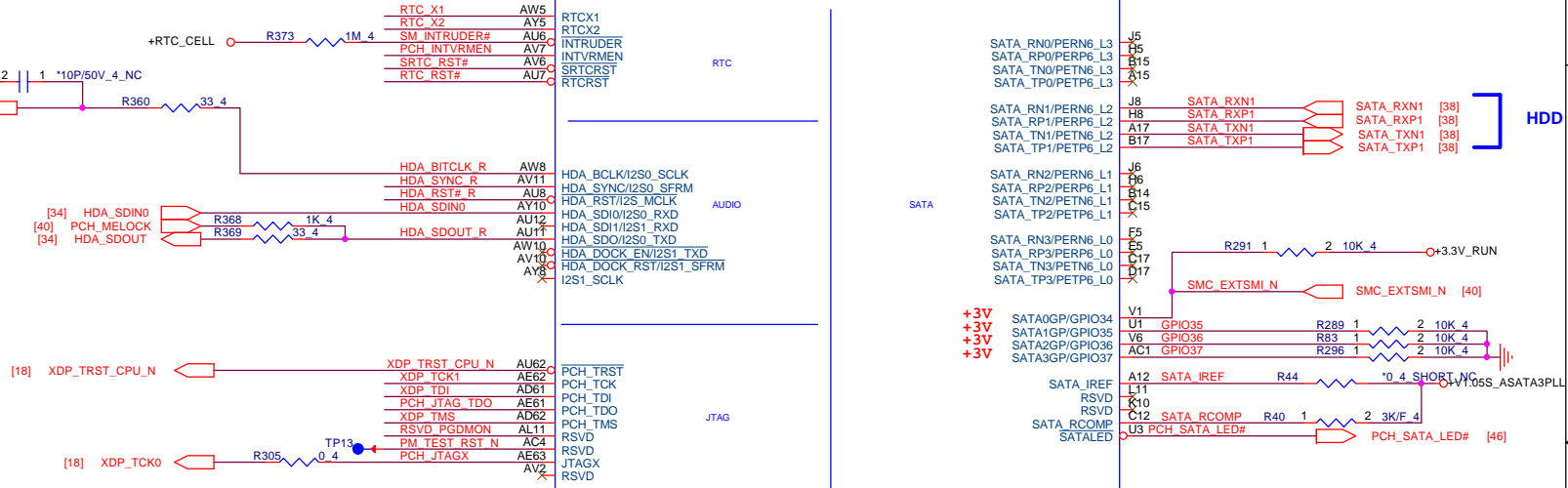
Haswell ULT (RTC, HDA, JTAG, SATA)



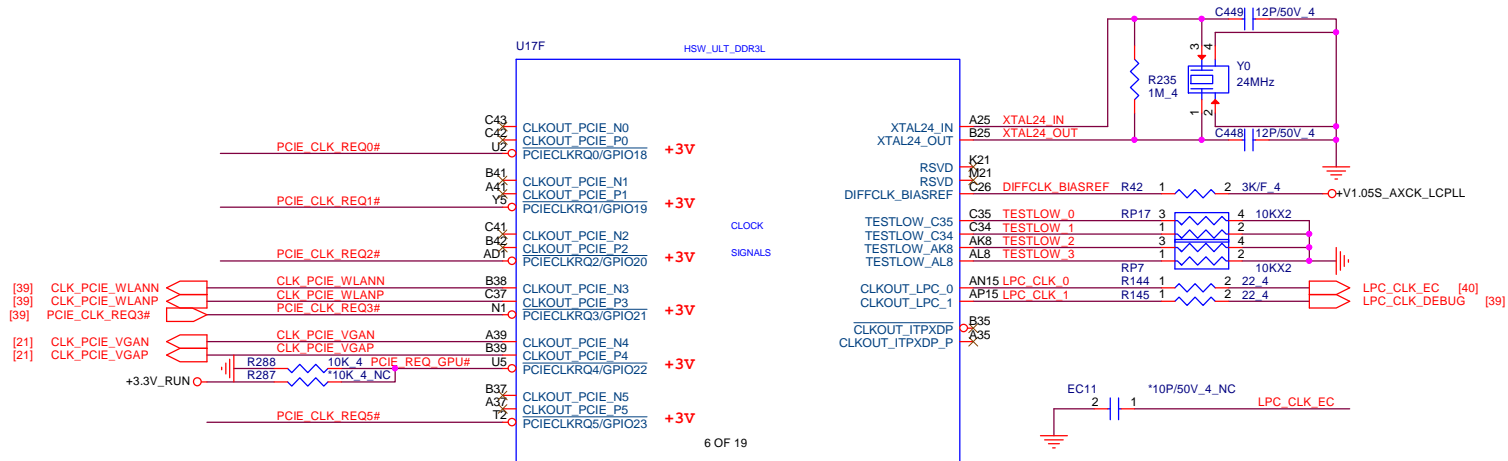
DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = Security Effect (Int PD) 1 = Can be Override	This signal has a weak internal pull-down. The internal pull-down is disabled after PLTRST# deasserts
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Integrated VRMs disabled. 1 = Integrated VRMs enabled.	+RTC_CELL - R157 - *330K 4 NC - PCH_INTVRMEN - R147 - 330K 4 -

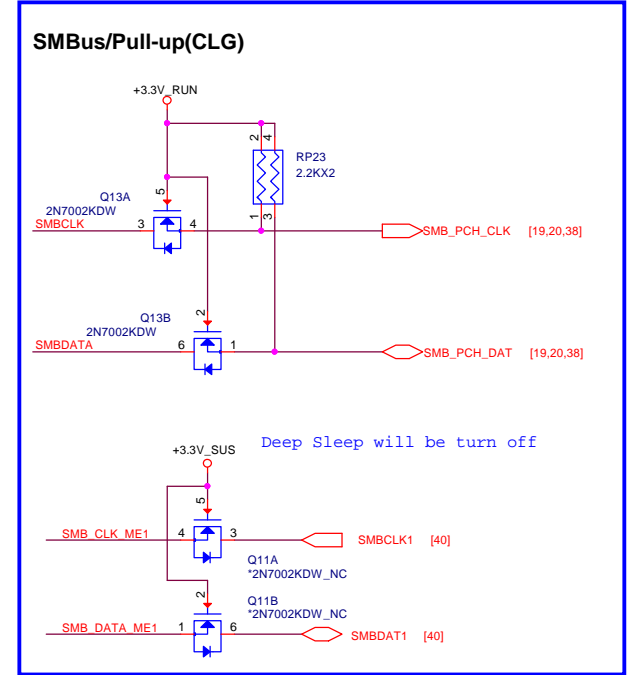
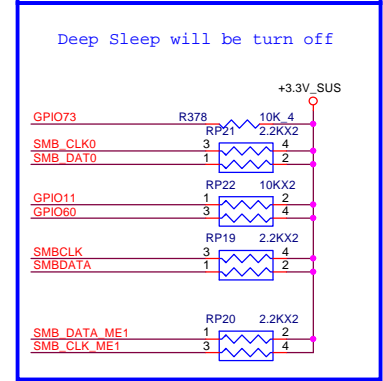
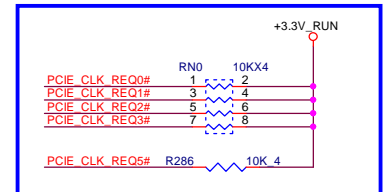
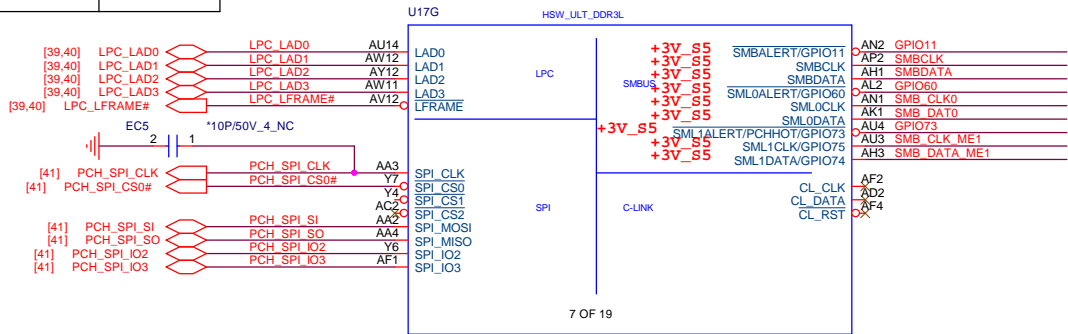


Haswell ULT (CLK)

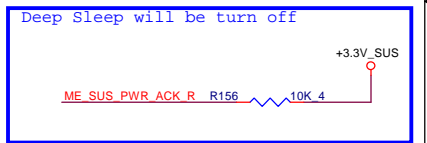
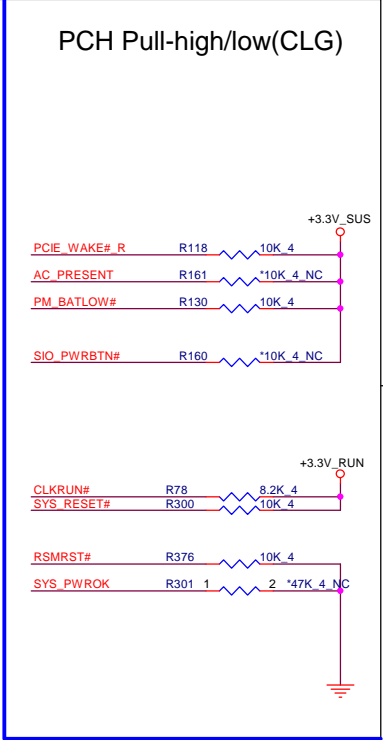
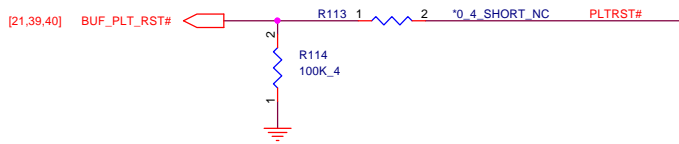
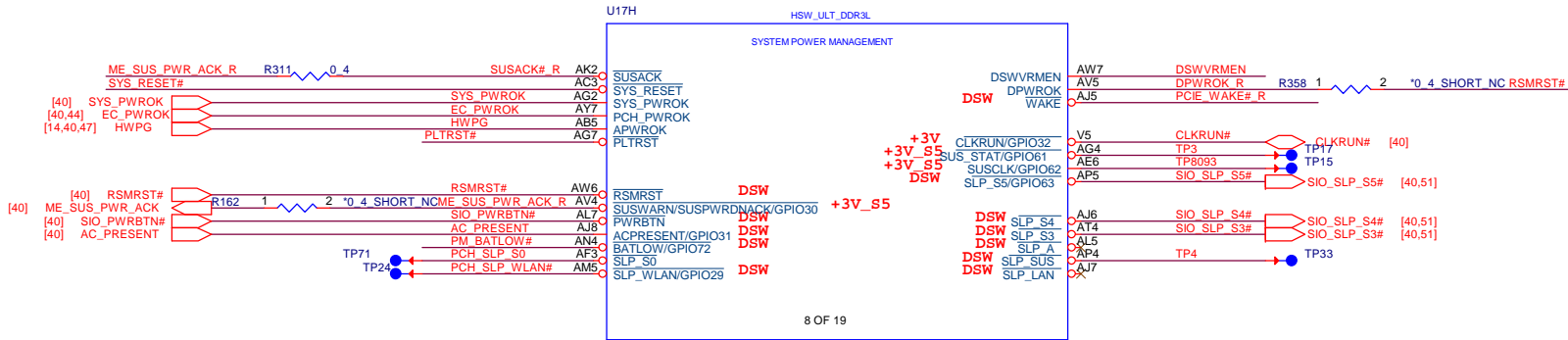


	UMA	Discrete
R288	*10K_4_NC	10K_4
R287	10K_4	*10K_4_NC

Haswell ULT (LPC/SPI/SMB/CLINK)



Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	1. This signal is always sampled. 2. This signal is in the RTC well. +RTC_CELL - 330K_4 - R372 - DSWVRMEN

Haswell ULT MCP (POWER)

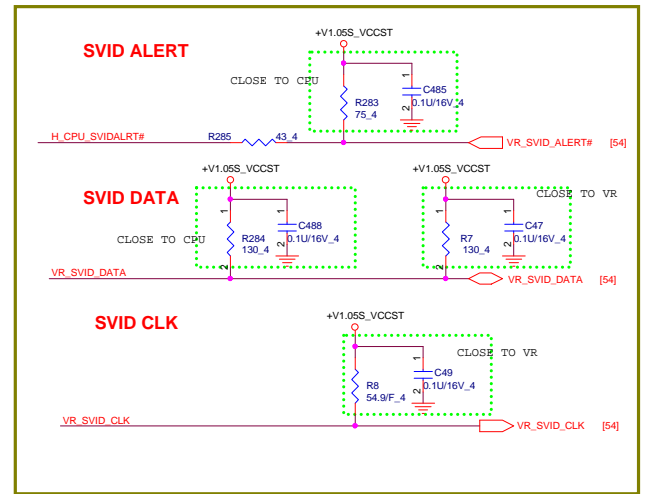
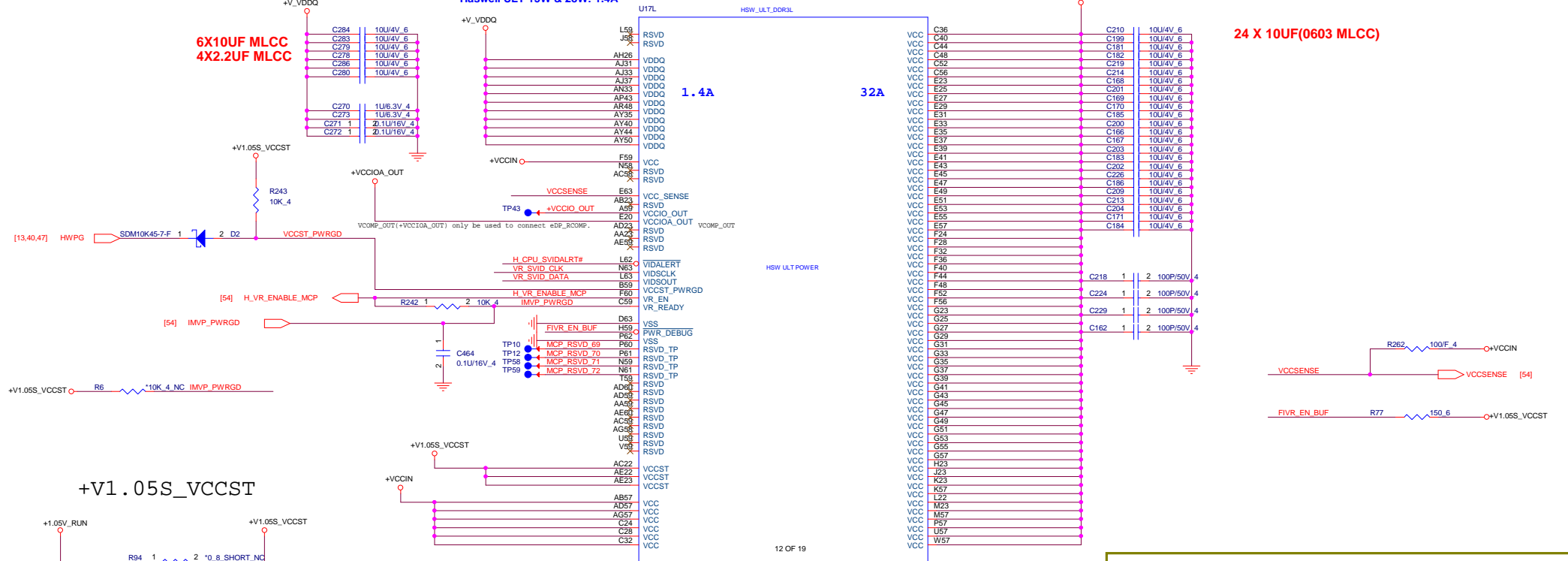
CPU VDDQ
Haswell ULT 15W & 28W: 1.4A

CPU VCC

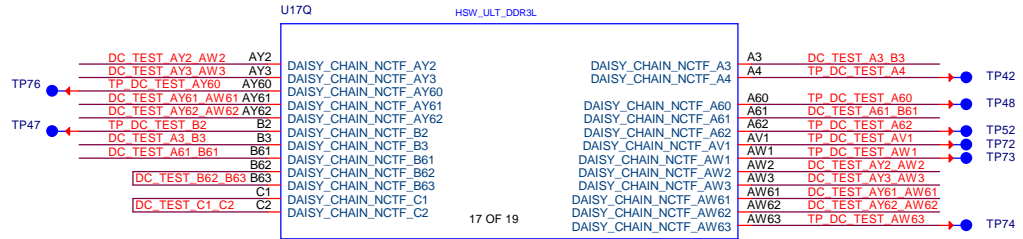
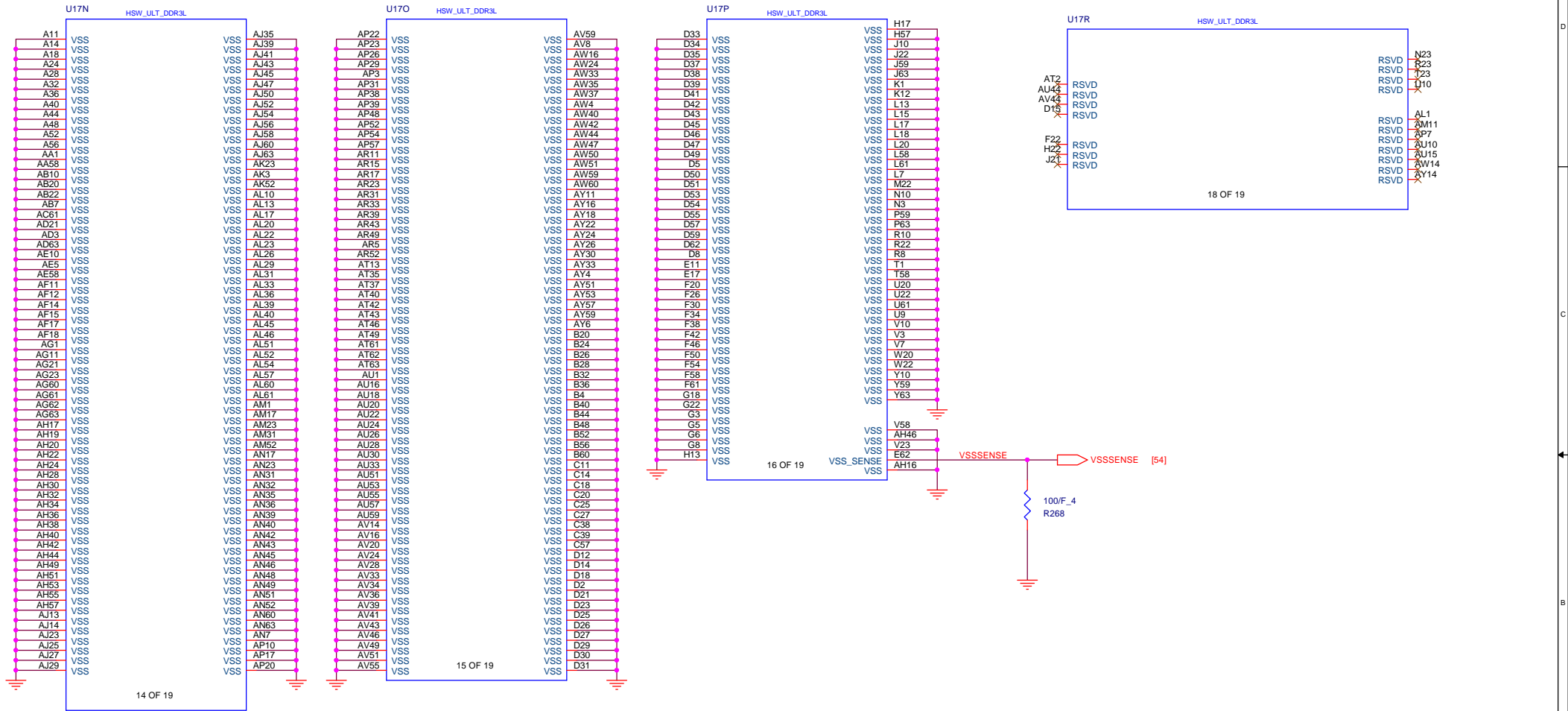
Haswell ULT 15W : 32A
28W : 40A

6X10UF MLCC
4X2.2UF MLCC

24 X 10UF(0603 MLCC)

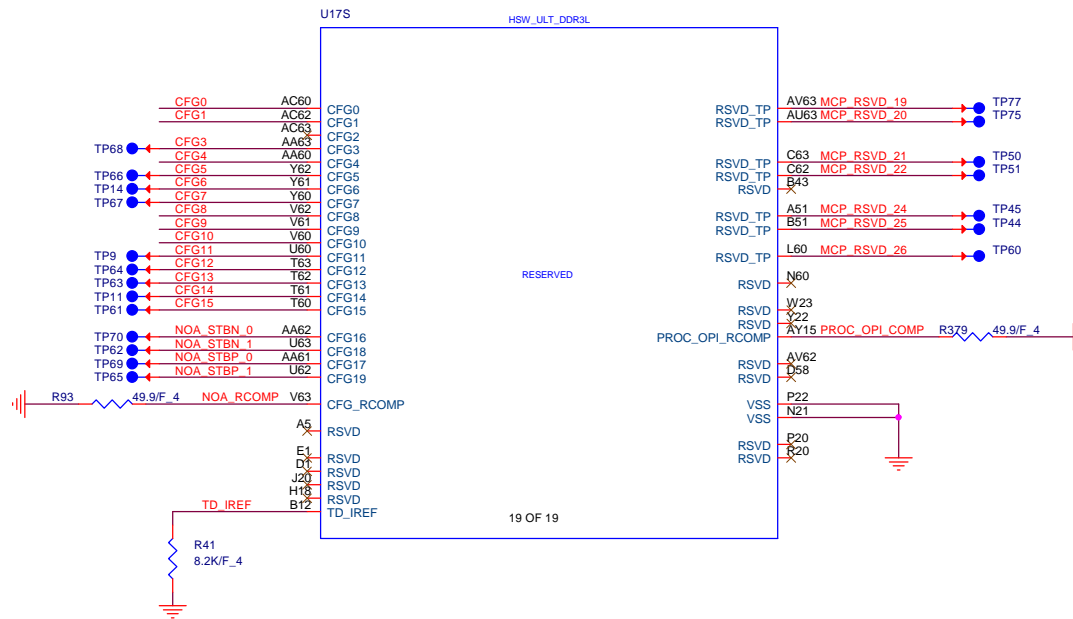


Haswell ULT (GND)



Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Haswell ULT 9/12	A
Date:	Monday, May 05, 2014	Sheet 15 of 58

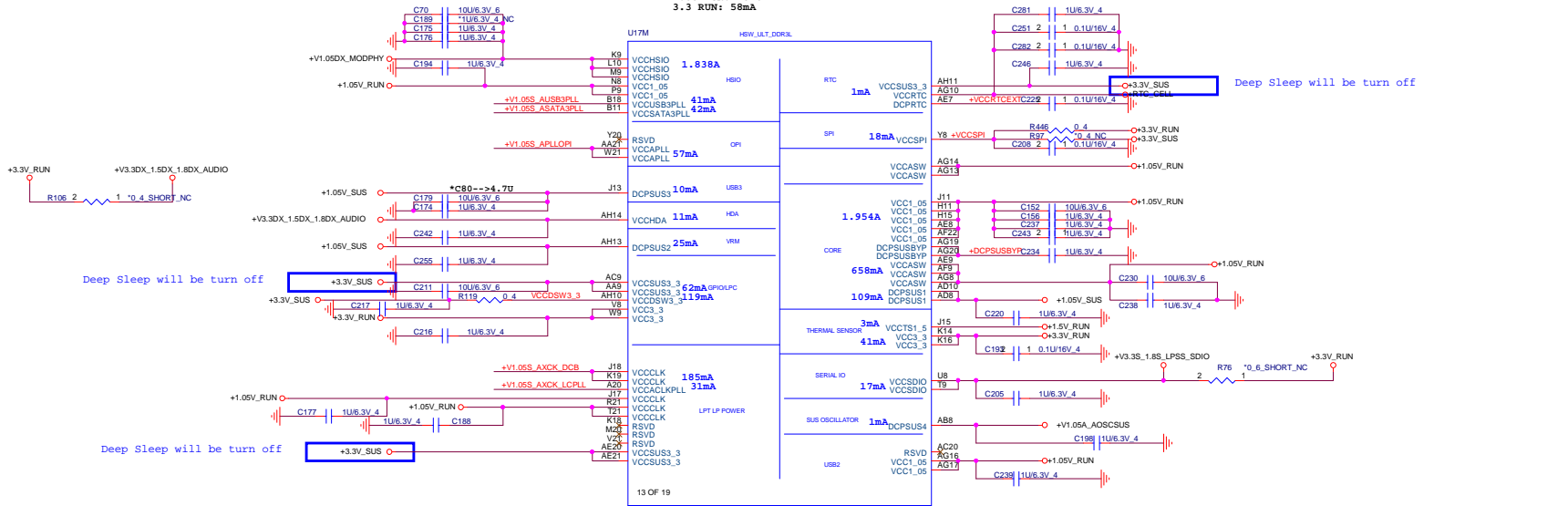


Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

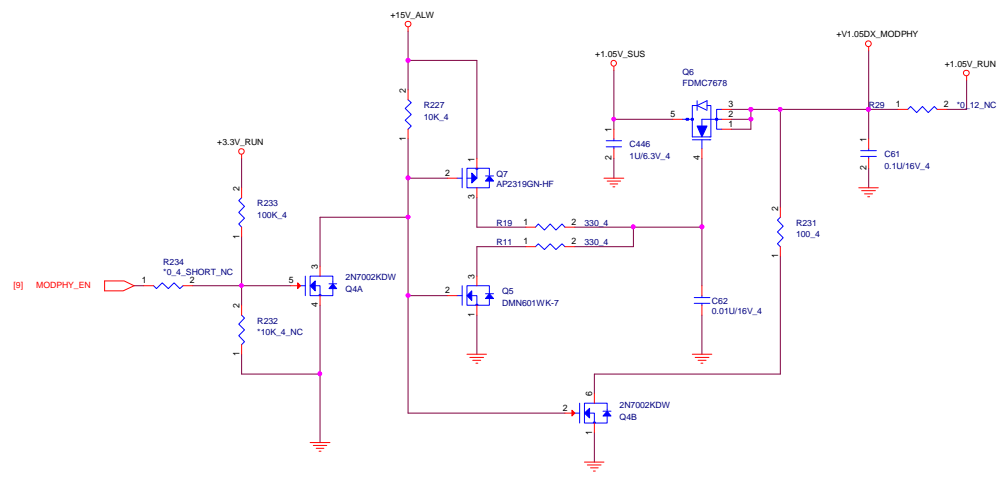
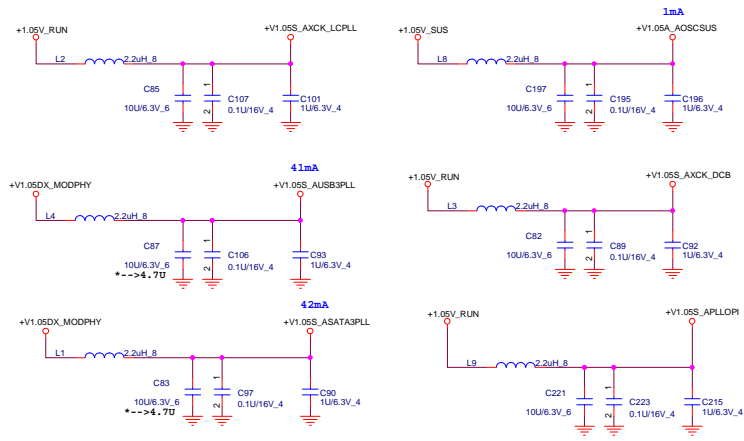
	1	0	
CFG0 Reserved	(DEFAULT) NORMAL OPERATION		
CFG1 Reserved	(DEFAULT) NORMAL OPERATION		
CFG2 Reserved	(DEFAULT) NORMAL OPERATION		
CFG3 MSR Privacy Bit Feature	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	
CFG4 eDP enable	Disabled	Enabled	
CFG[19:5] Reserved	(DEFAULT) NORMAL OPERATION		

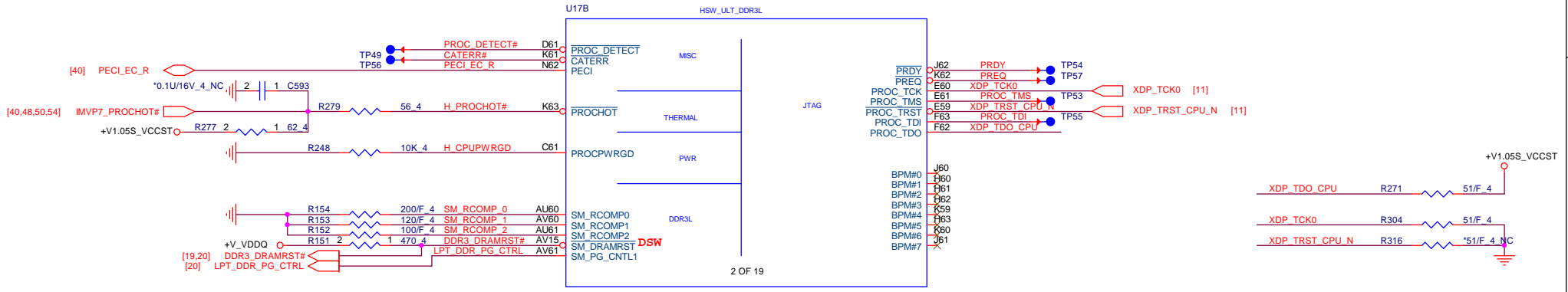
Haswell ULT PCH(POWER)

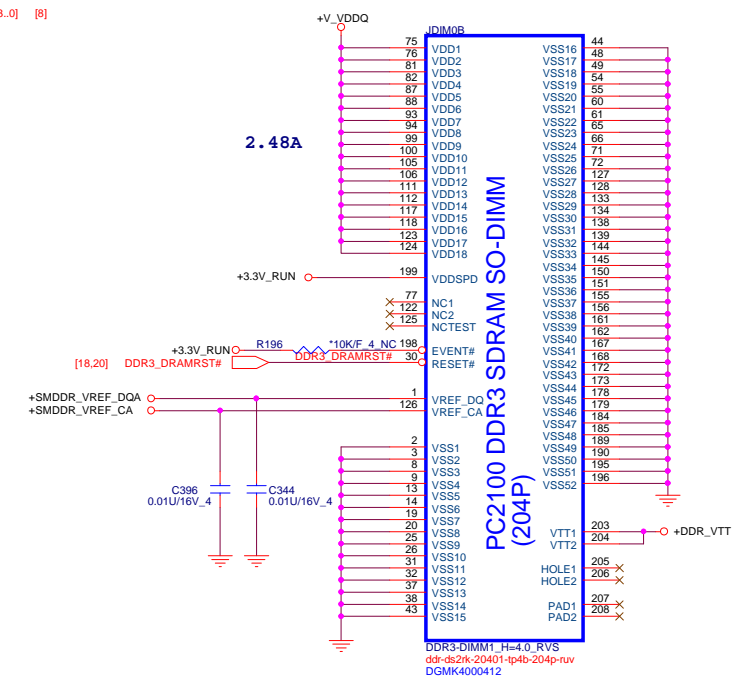
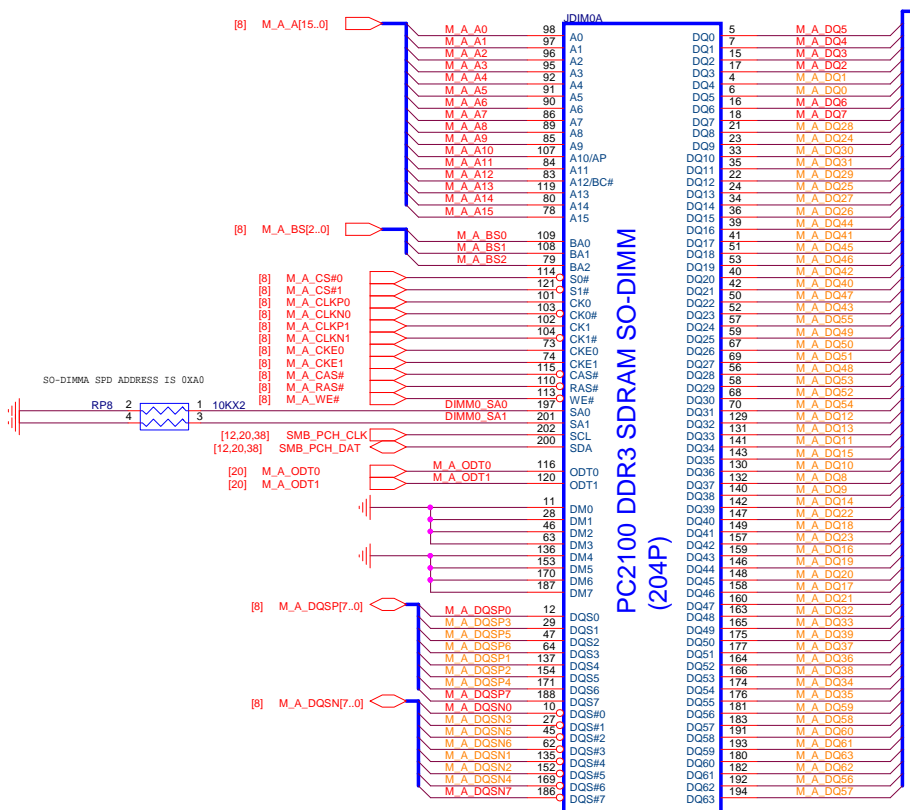
3.3 SUB: 205mA
 1.05 SUB: 206mA
 1.05 RUN: 2578mA
 3.3 RUN: 58mA



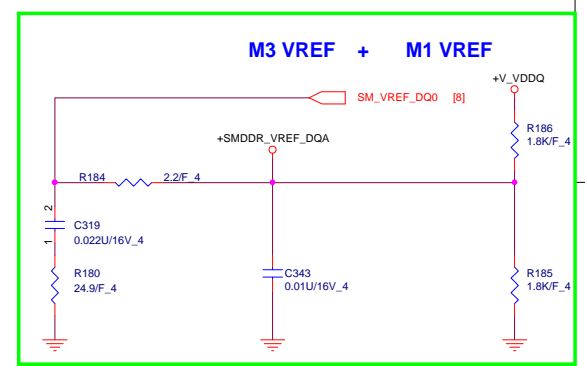
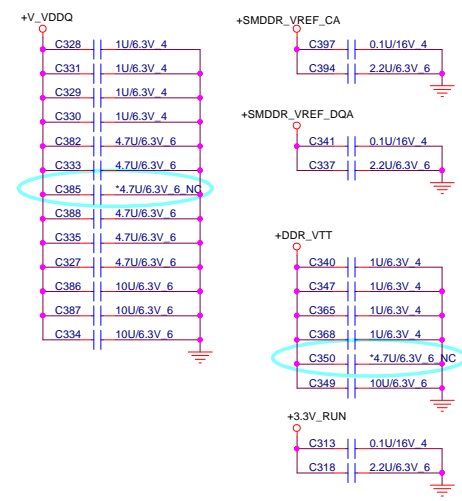
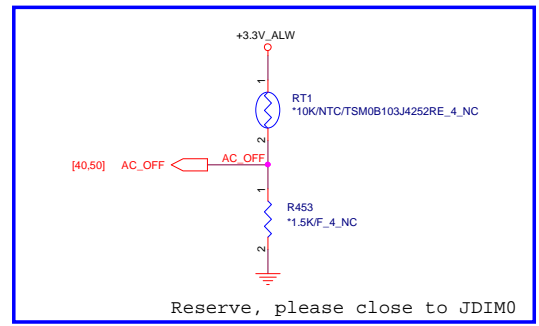
boot strap capacitor	VCCDSW3_3	C233	0.47uF	10u6.3V.4	DCPSUSBYP
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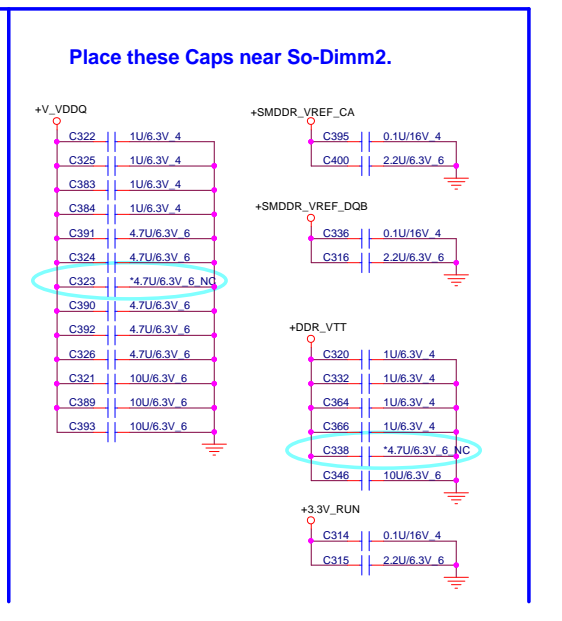
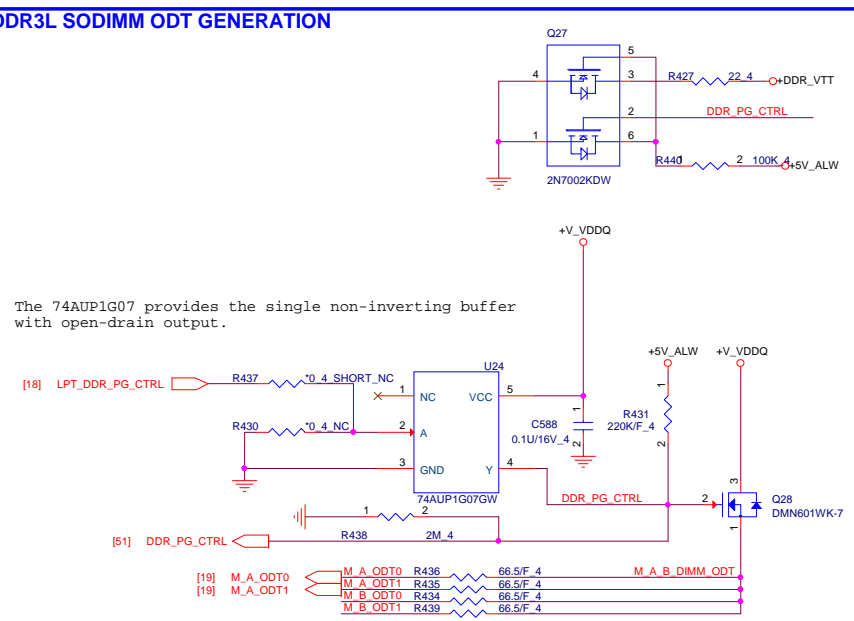
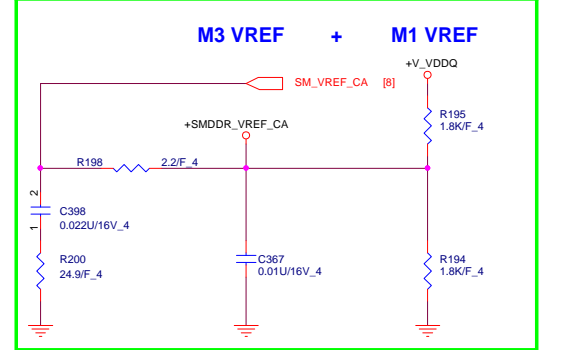
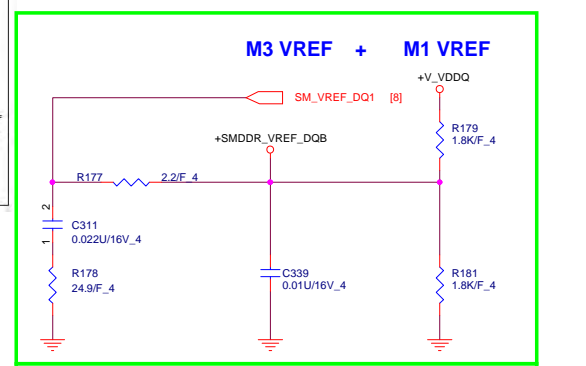
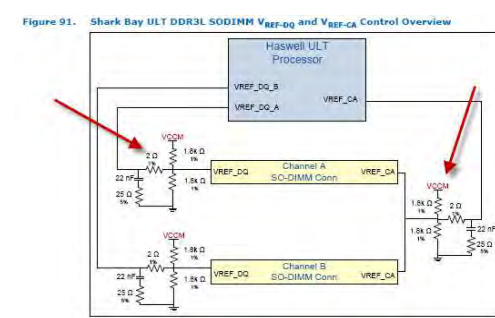
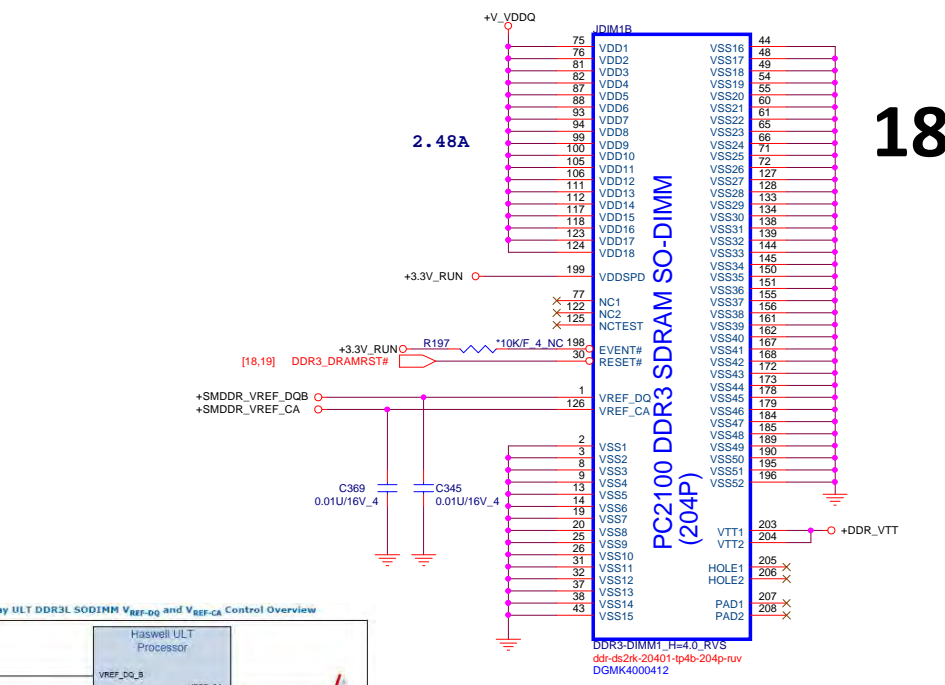
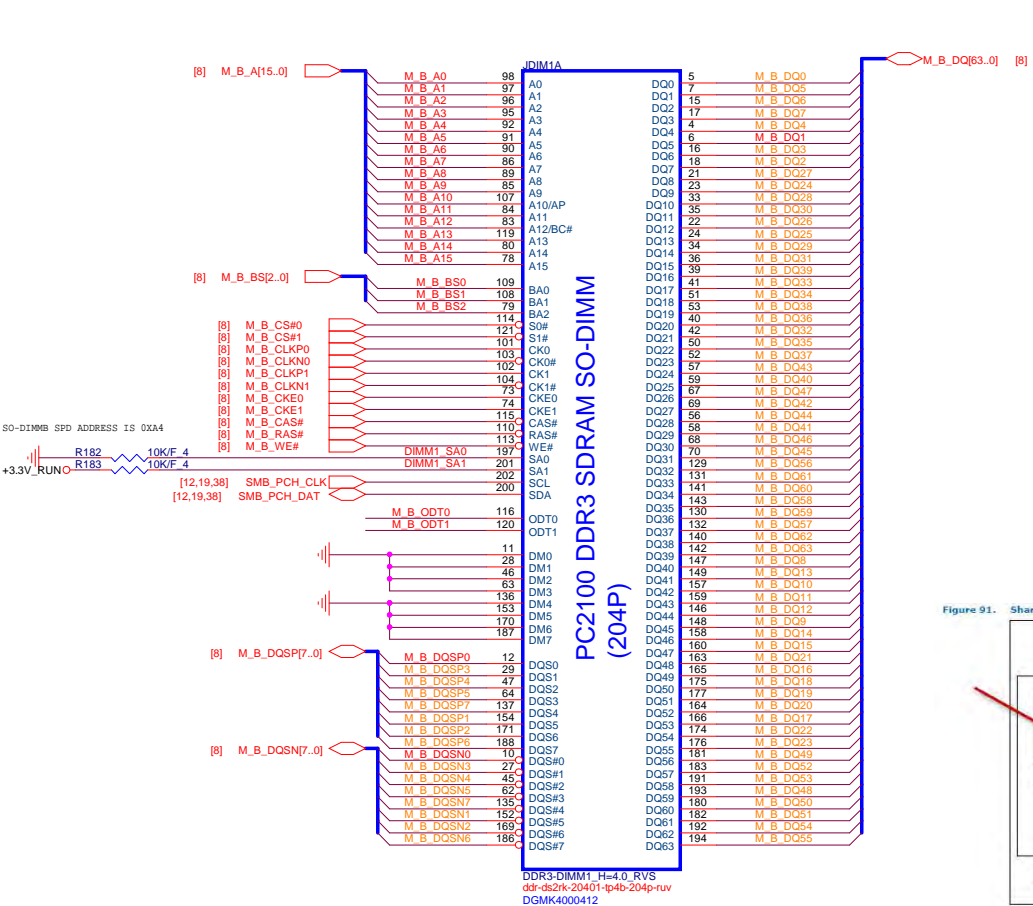


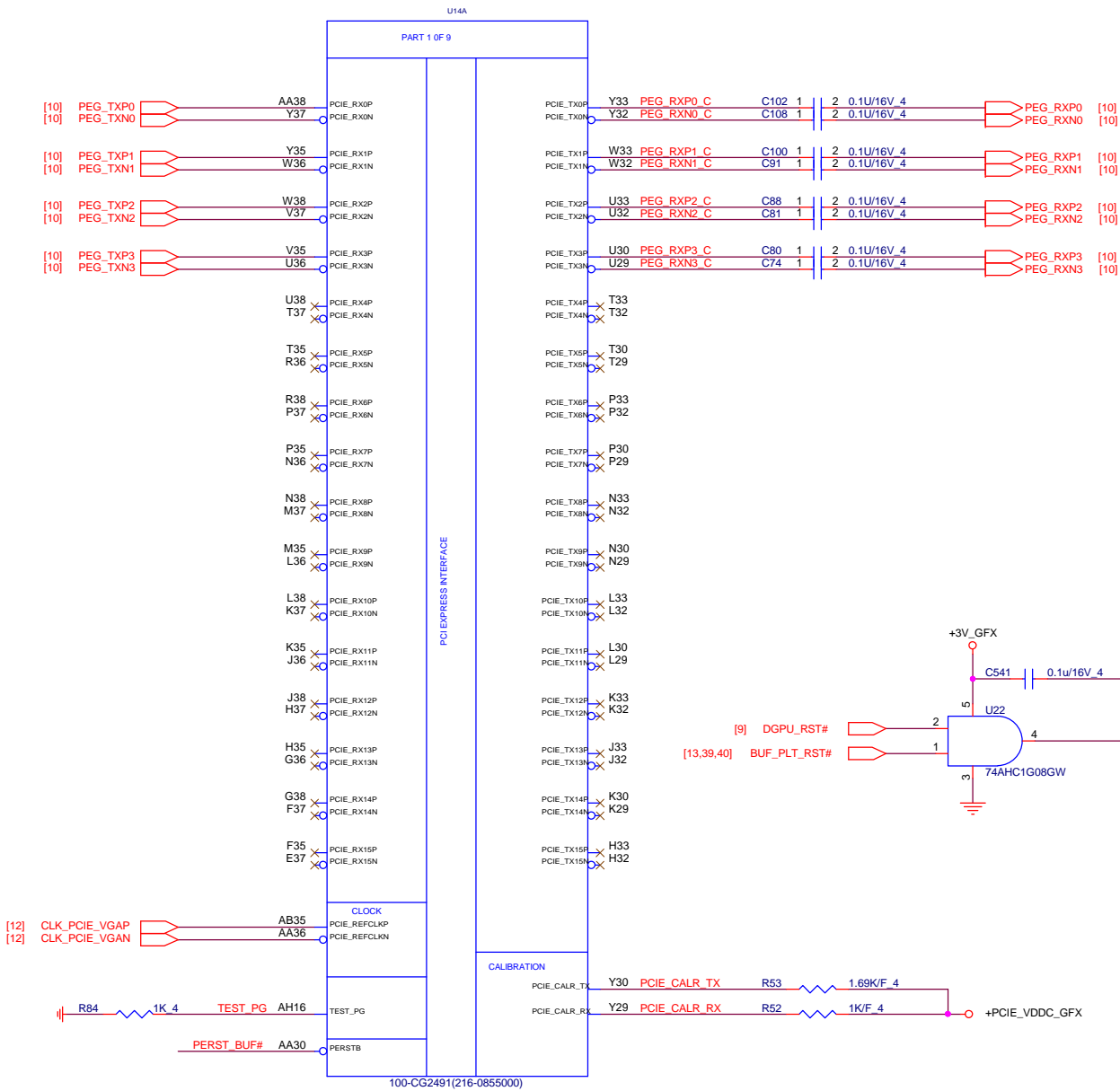




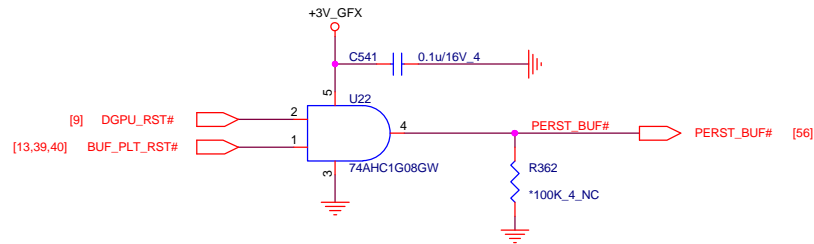
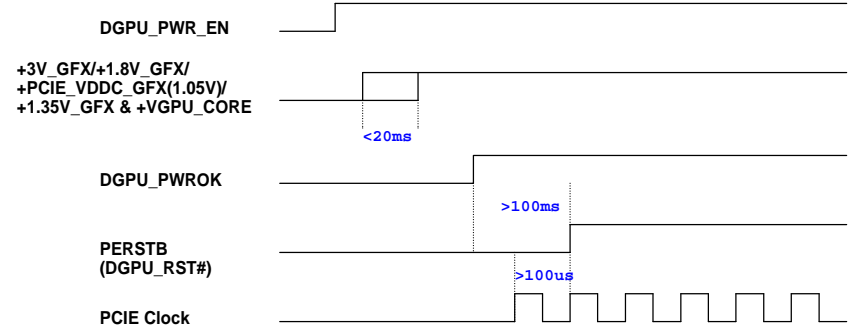
Place these Caps near So-Dimm1.







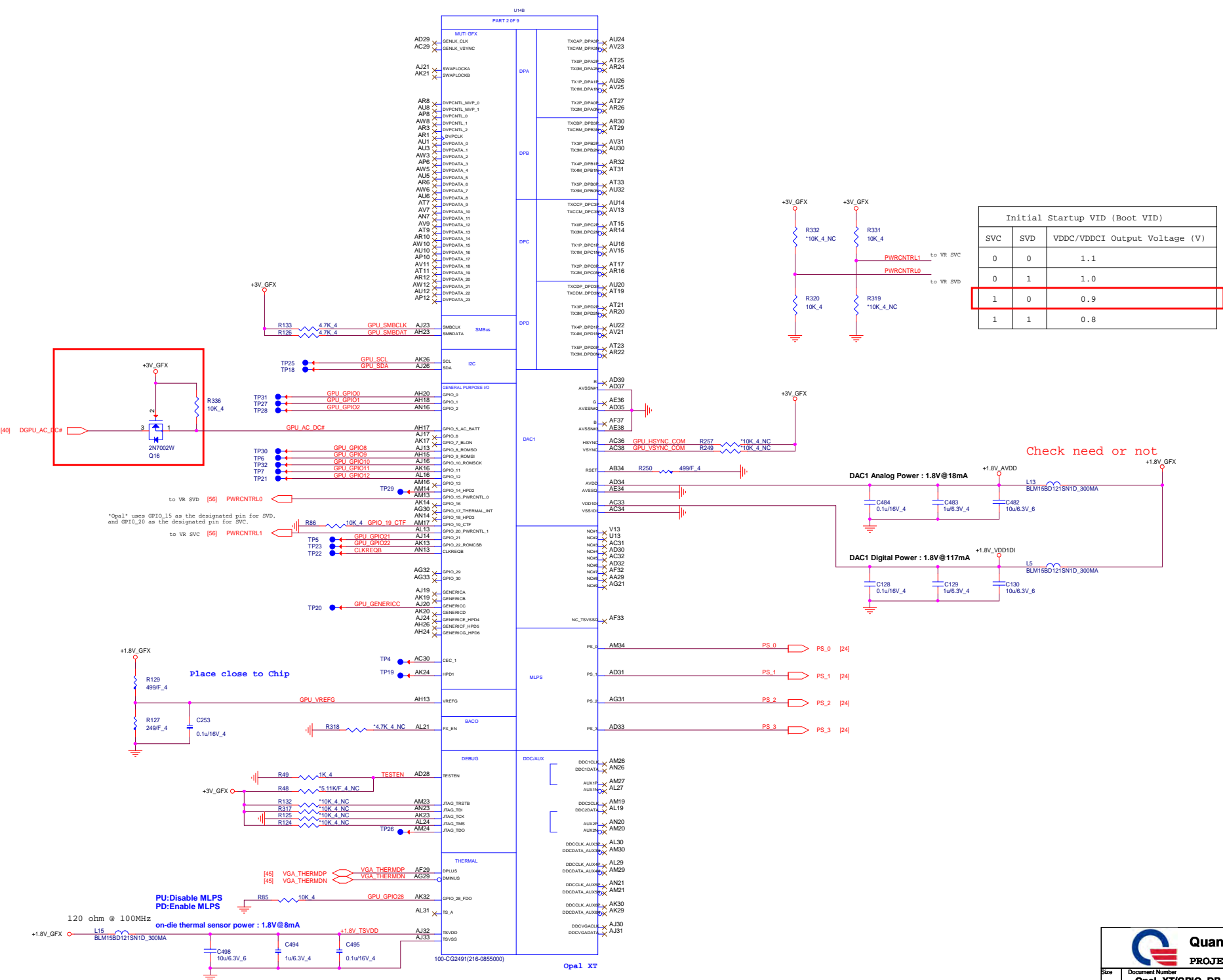
Opal XT Power-on sequence

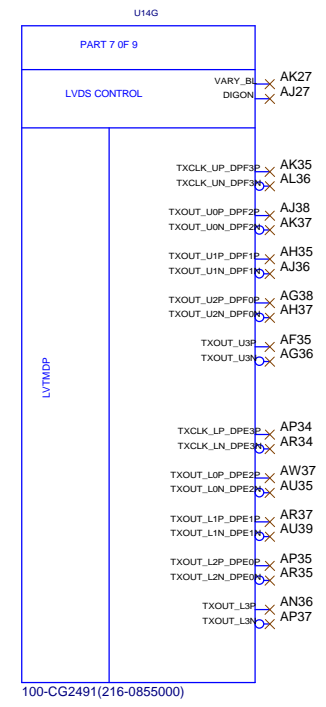
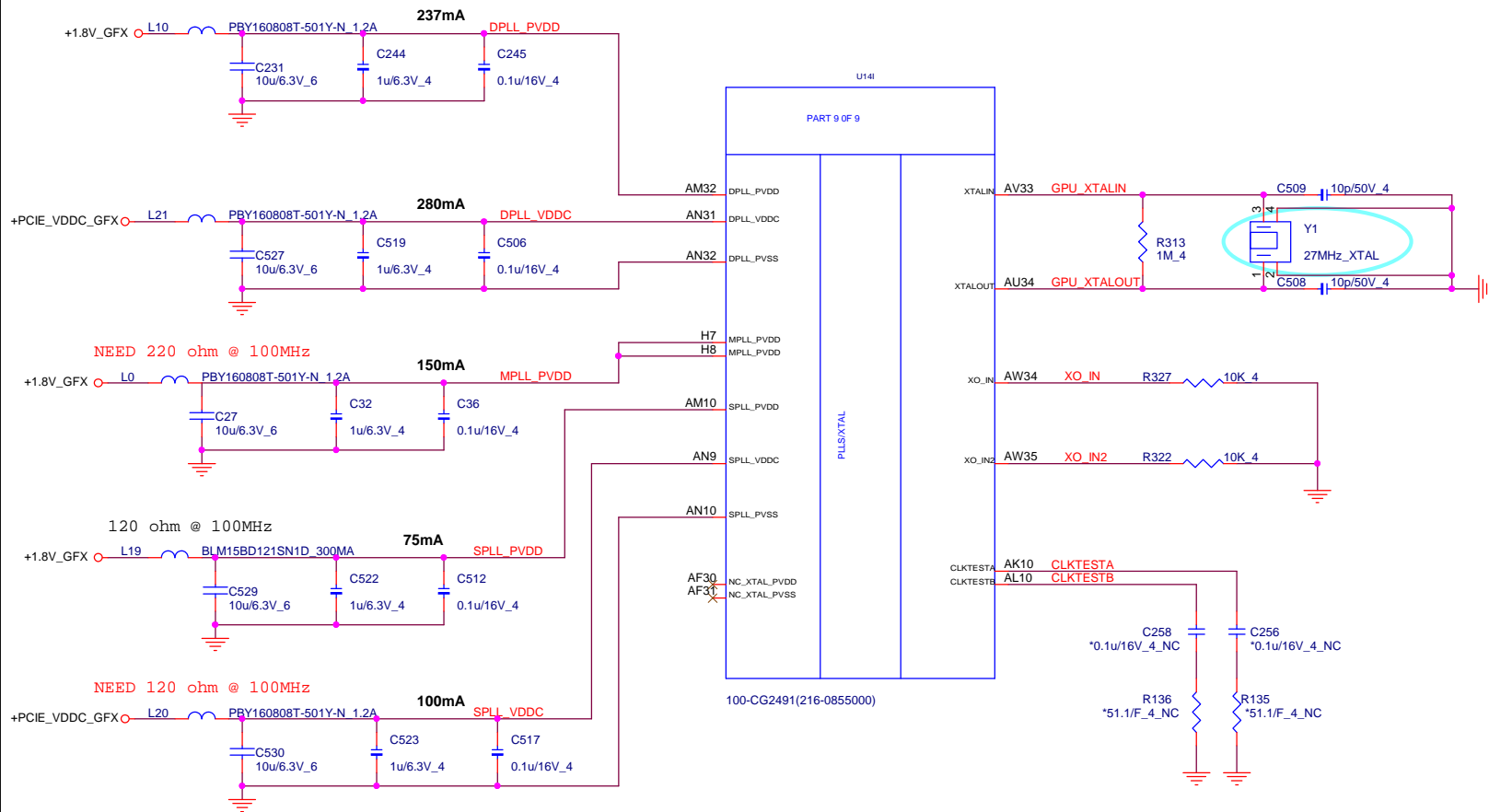


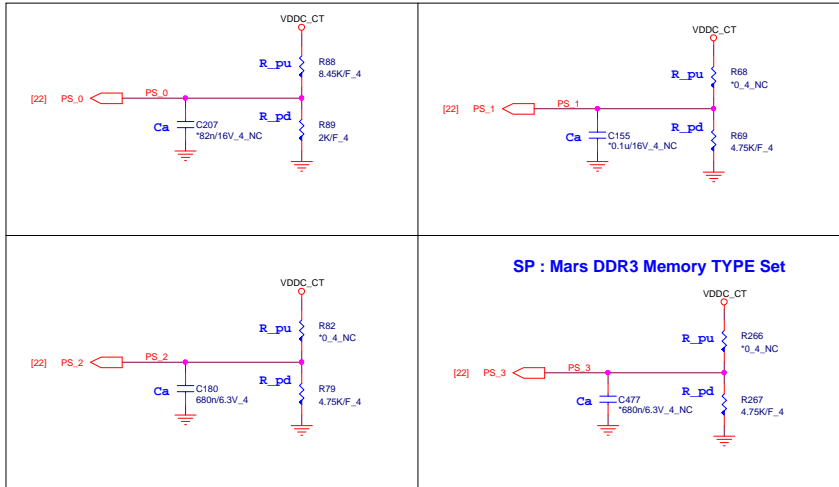
Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Opal_XT/PEG*16	A
Date:	Monday, May 05, 2014	Sheet 21 of 58







SP : Mars DDR3 Memory TYPE Set

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	00000
PS_3	11XXXX

MLPS

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	NA

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

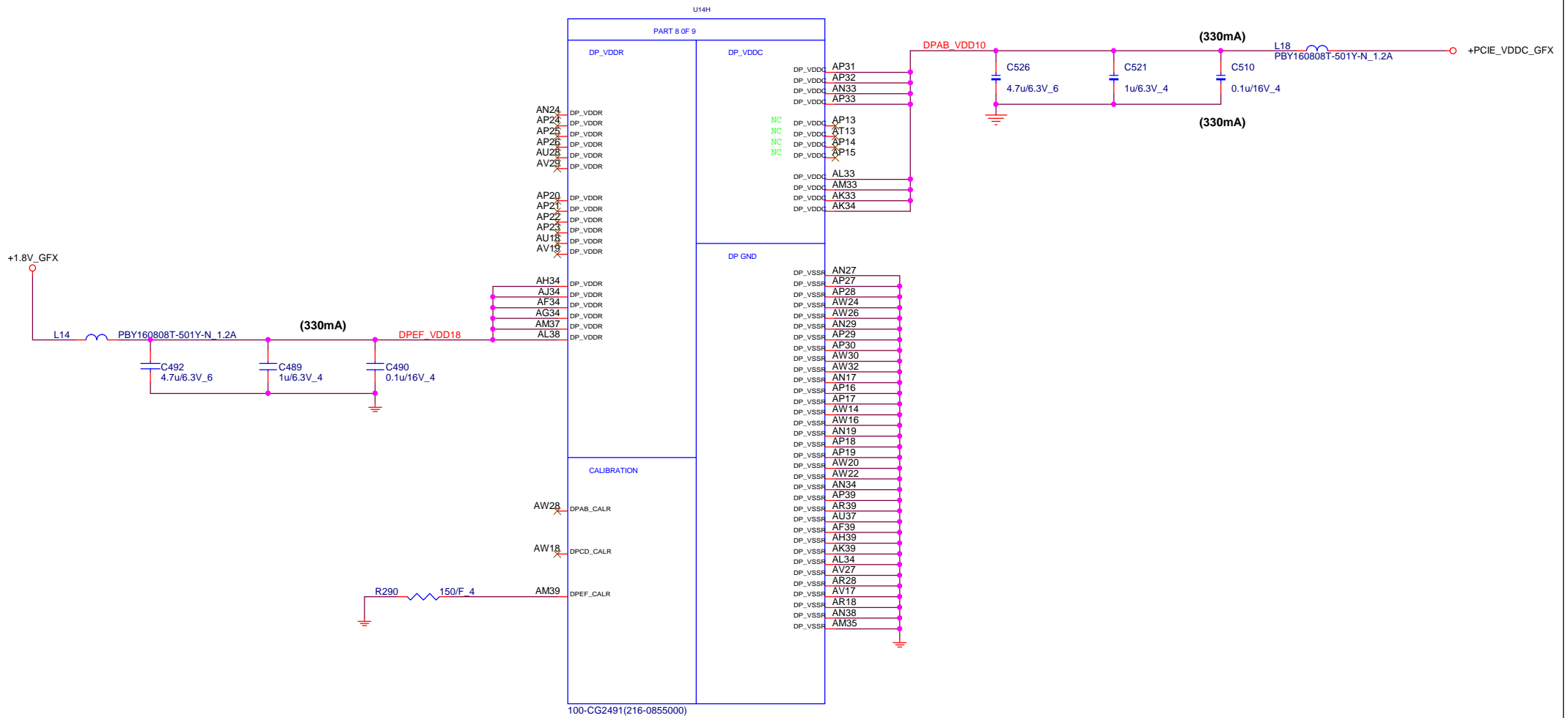
R_pu/R_pd	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

MLPS Bit	Strap Name	AM6 Settings	AM6 Settings	Description	AMD Recommended Settings
PS_0[1]	ROM_CONFIG[0]	1	Memory Aperture Size Select : 256MB	Serial ROM type or Memory Aperture Size Select # STRAP BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. # STRAP BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size.	Design dependent, SIZE ROM_CONFIG[2:0] 128MB 000 256MB 001 64MB 010 Reserved 011
PS_0[2]	ROM_CONFIG[1]	0			
PS_0[3]	ROM_CONFIG[2]	0			
PS_0[4]	N/A	1	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	1	All endpoints are usable.	the strap option indicates the number of audio-capable display outputs.	Design dependent
PS_1[1]	STRAP_BIF_GEN3_EN_A	0	PCIe GEN3 is not supported. (use GEN2)	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent
PS_1[2]	STRAP_BIF_CLK_PM_EN	0	The CLKREQ power management capability is disabled	Determines whether or not the PCIe reference clock power management capability 0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.	0
PS_1[3]	N/A	0	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1	The transmitter full-swing is enabled	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	1	Tx deemphasis enabled.	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent
PS_2[1]	N/A	0	Reserved.	Reserved.	N/A
PS_2[2]	N/A	0	Reserved.	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	0	Disable the external BIOS ROM device.	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent
PS_2[4]	STRAP_BIF_VGA_DIS	0	Standalone dGPU design	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	Standalone dGPU design = 0 AMD PowerXpress design = 1
PS_2[5]	N/A	0	Reserved.	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	X	VRAM vendor BOARD_CONFIG[2:0] Hynix 000 default Micron 001 Samsung 010	Board configuration related strapping, such as for memory ID	Design dependent
PS_3[2]	BOARD_CONFIG[1]	X			
PS_3[3]	BOARD_CONFIG[2]	X			
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	1	No usable endpoints.	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	1			

System Memory Aperture size

GPIO9 BIOSROM	SIZE	GPIO13 ROM_CONFIG2	GPIO12 ROM_CONFIG1	GPIO11 ROM_CONFIG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1

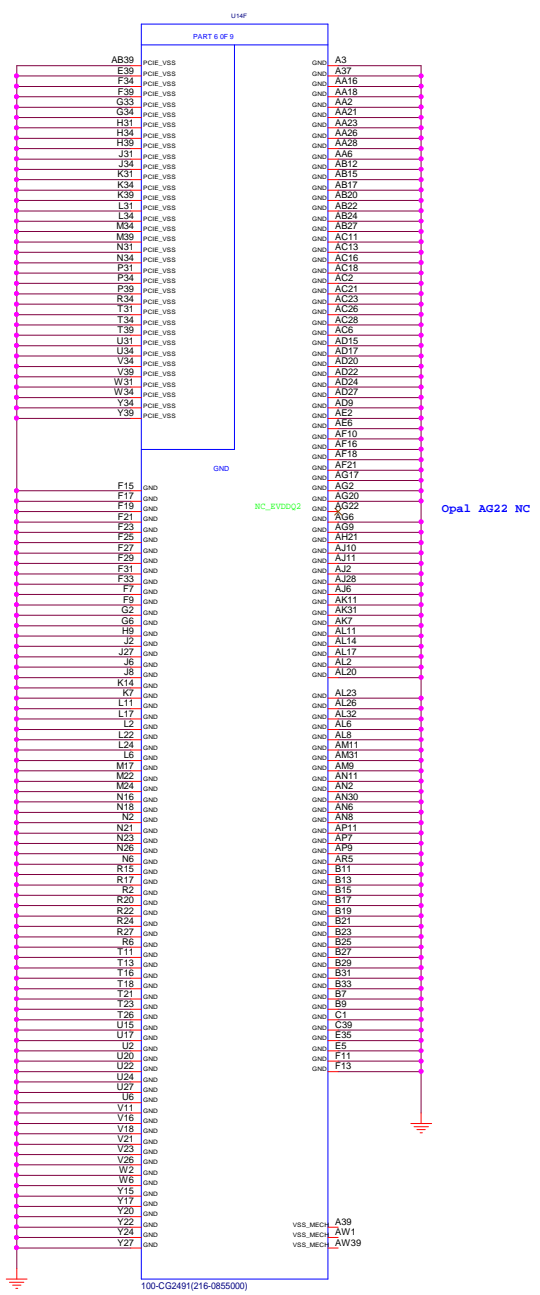
Vendor	Vendor P/N	STN B/S P/N	Size	MLPS
Hynix	H5TC4G63AFR-11C (256M*16)	AKD5PGWWT11 * 8	4GB	000
Micron	MT41J256M16HA-093G:E (256M*16)	AKD5PZSTL02 * 8	4GB	001
Samsung	K4W4G1646D-BC1A (256M*16)	AKD5PGWT500 * 8	4GB	010



Quanta Computer Inc.

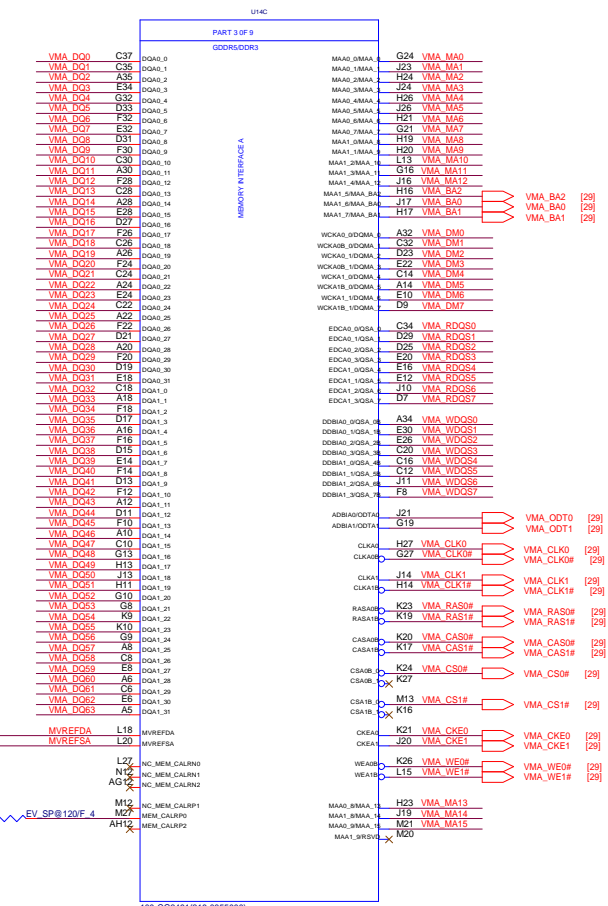
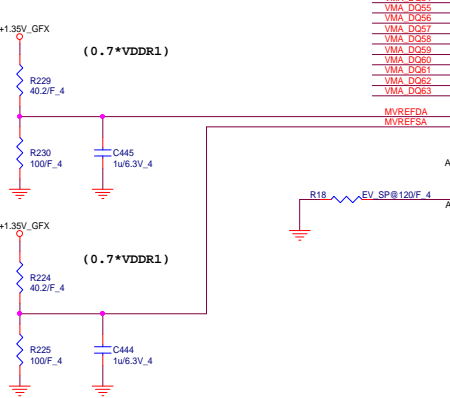
PROJECT : AM6

Size	Document Number	Rev
	Opal_XT/DP_Powers	A
Date:	Monday, May 05, 2014	Sheet 26 of 58

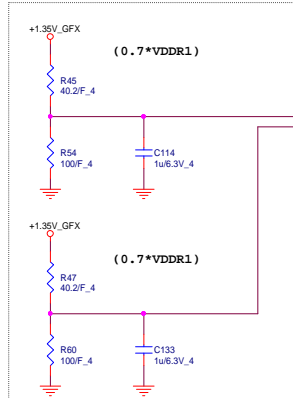


- [29] VMA_DQ[63..0] <-> VMA_DQ[63..0]
- [29] VMA_RDQS[7..0] <-> VMA_RDQS[7..0]
- [29] VMA_WDQS[7..0] <-> VMA_WDQS[7..0]
- [29] VMA_MA[15..0] <-> VMA_MA[15..0]
- [29] VMA_DM[7..0] <-> VMA_DM[7..0]

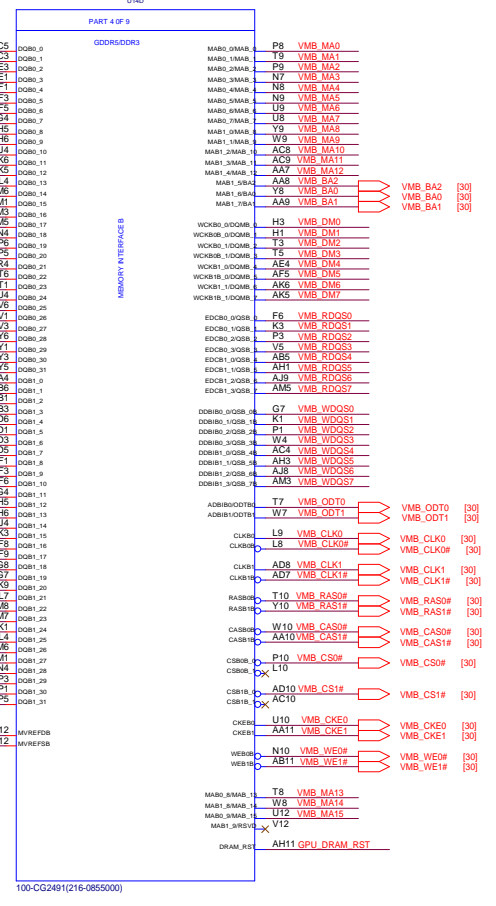
Place MVREF dividers and Caps close to ASIC



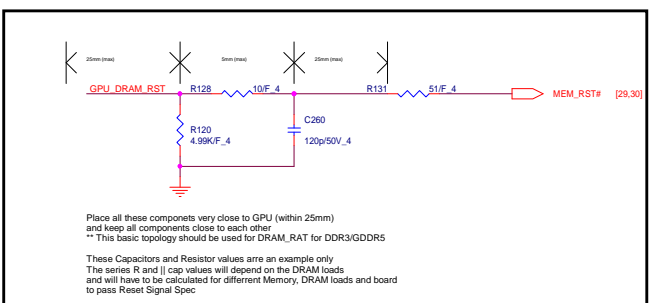
- [30] VMB_DQ[63..0] <-> VMB_DQ[63..0]
- [30] VMB_RDQS[7..0] <-> VMB_RDQS[7..0]
- [30] VMB_WDQS[7..0] <-> VMB_WDQS[7..0]
- [30] VMB_MA[15..0] <-> VMB_MA[15..0]
- [30] VMB_DM[7..0] <-> VMB_DM[7..0]



Place MVREF dividers and Caps close to ASIC

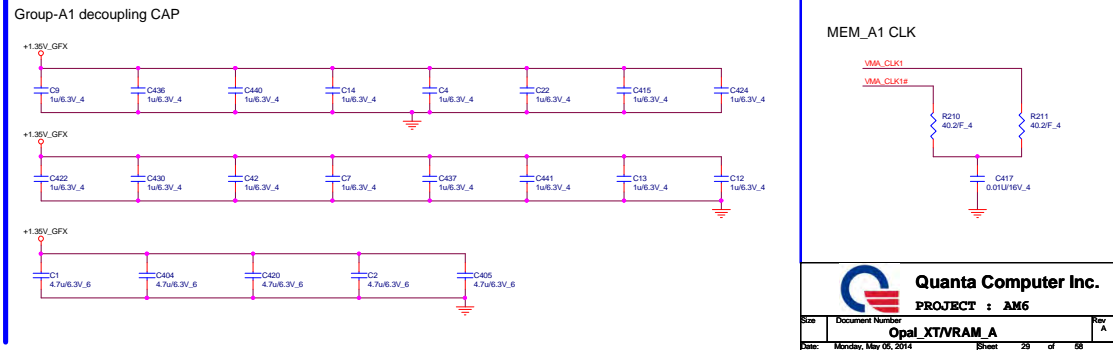
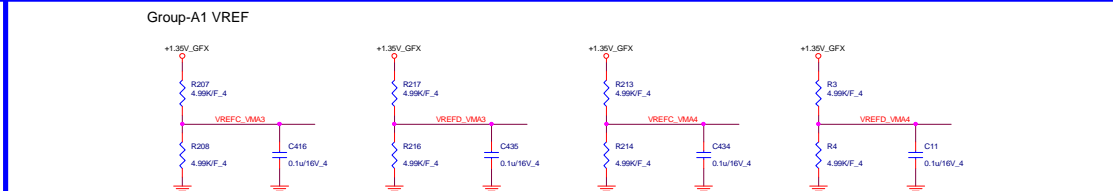
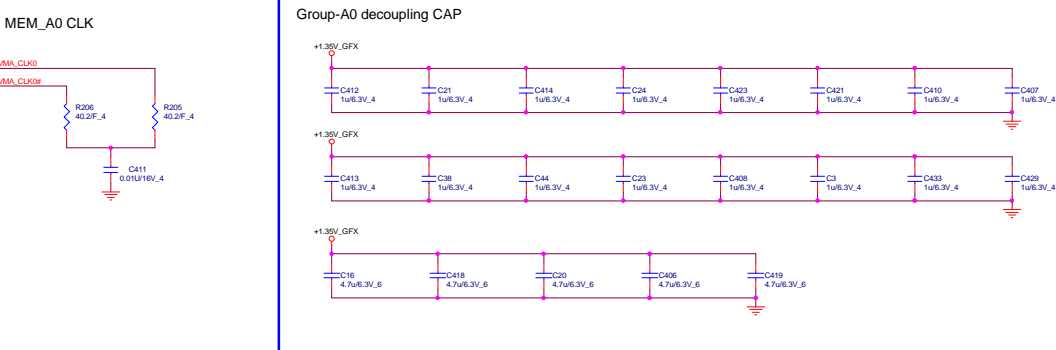
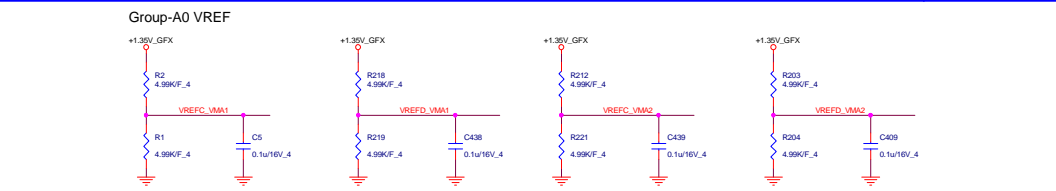
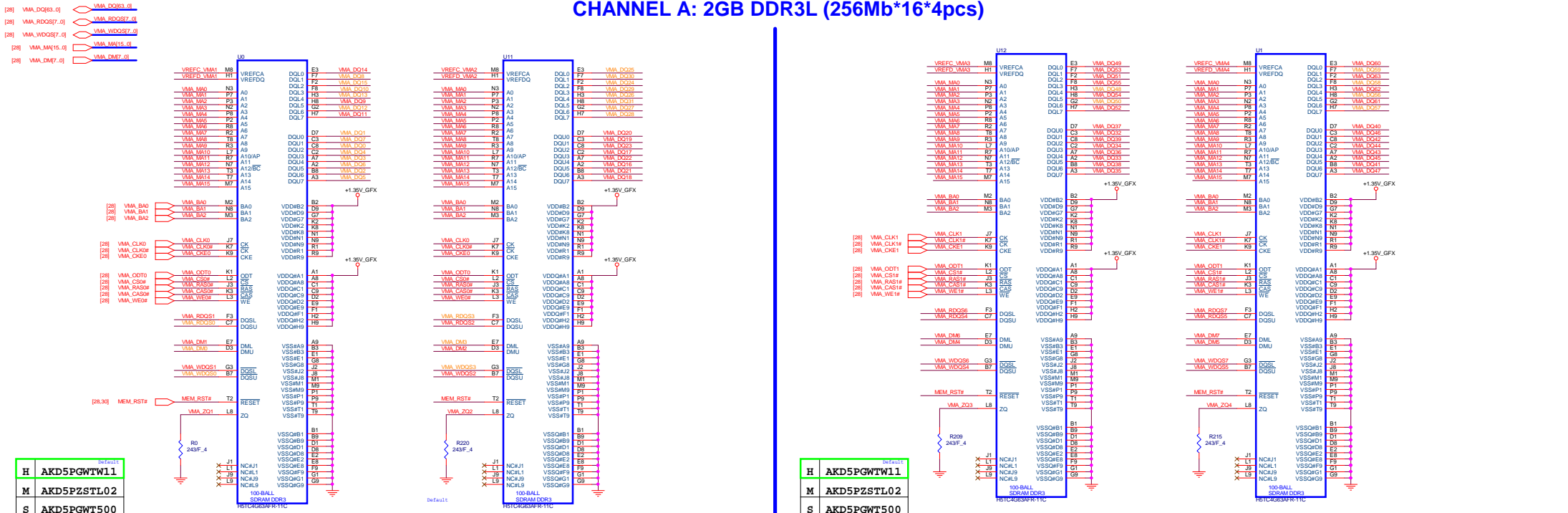


- [30] VMB_ODT0 <-> VMB_ODT0
- [30] VMB_ODT1 <-> VMB_ODT1
- [30] VMB_CLK0 <-> VMB_CLK0
- [30] VMB_CLK#0 <-> VMB_CLK#0
- [30] VMB_CLK1 <-> VMB_CLK1
- [30] VMB_CLK#1 <-> VMB_CLK#1
- [30] VMB_RAS0# <-> VMB_RAS0#
- [30] VMB_RAS1# <-> VMB_RAS1#
- [30] VMB_CAS0# <-> VMB_CAS0#
- [30] VMB_CAS1# <-> VMB_CAS1#
- [30] VMB_CS0# <-> VMB_CS0#
- [30] VMB_CS1# <-> VMB_CS1#
- [30] VMB_CKE0 <-> VMB_CKE0
- [30] VMB_CKE1 <-> VMB_CKE1
- [30] VMB_WE0# <-> VMB_WE0#
- [30] VMB_WE1# <-> VMB_WE1#



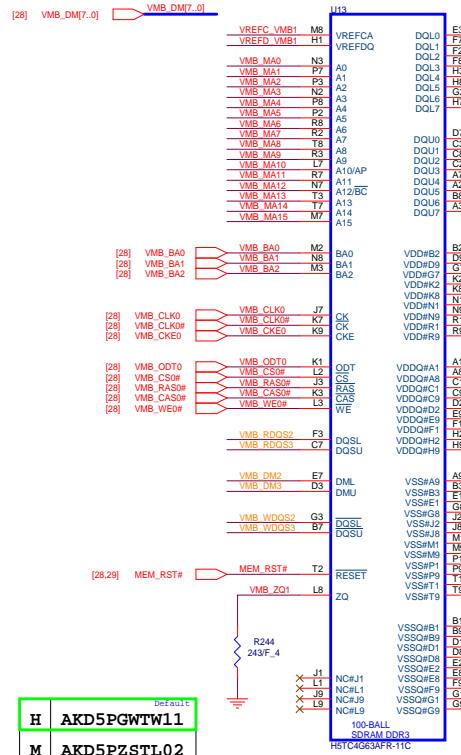
Place all these components very close to GPU (within 25mm) and keep all components close to each other
 ** This basic topology should be used for DRAM_RST for DDR3/GDDR5
 These Capacitors and Resistor values are an example only
 The series R and || cap values will depend on the DRAM loads and will have to be calculated for different Memory, DRAM loads and board to pass Reset Signal Spec

CHANNEL A: 2GB DDR3L (256Mb*16*4pcs)

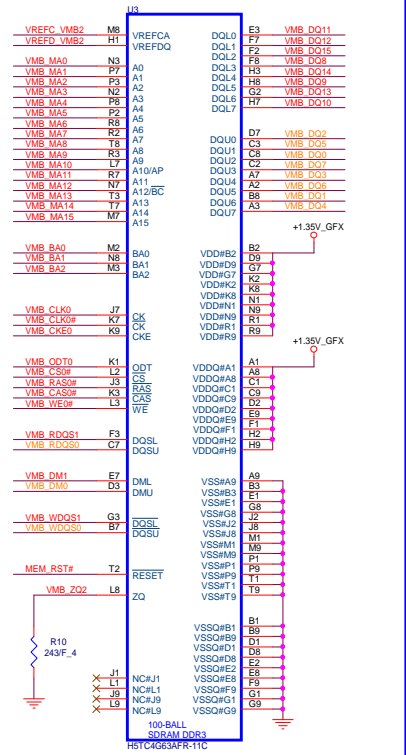


CHANNEL B: 2GB DDR3L (256Mb*16*4pcs)

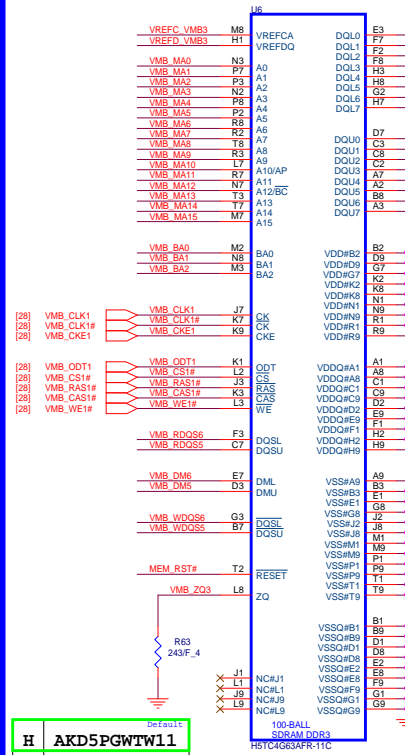
- [28] VMB_DQ[63..0] VMB_DQ[63..0]
- [28] VMB_RDQS[7..0] VMB_RDQS[7..0]
- [28] VMB_WDQS[7..0] VMB_WDQS[7..0]
- [28] VMB_MA[15..0] VMB_MA[15..0]
- [28] VMB_DM[7..0] VMB_DM[7..0]



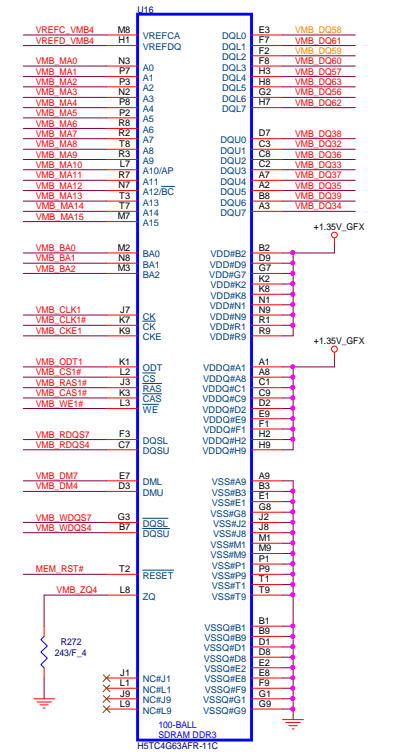
BOT Down



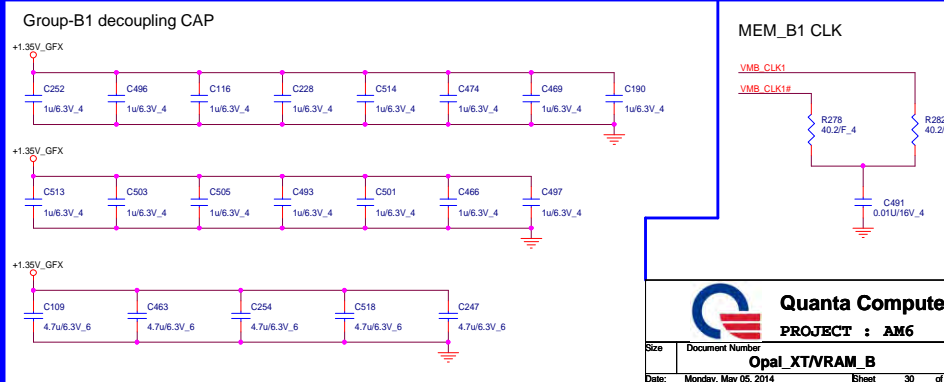
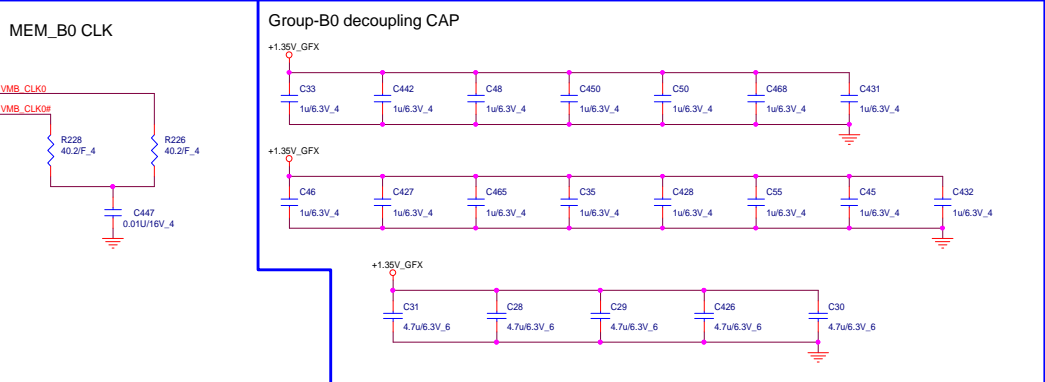
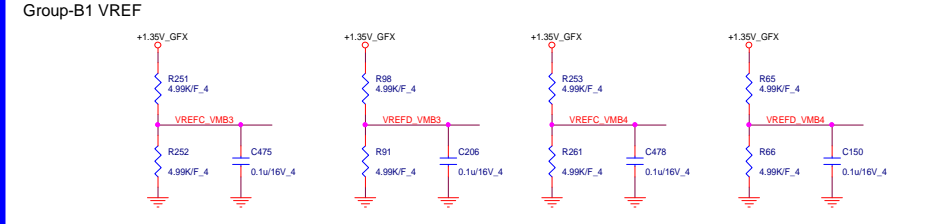
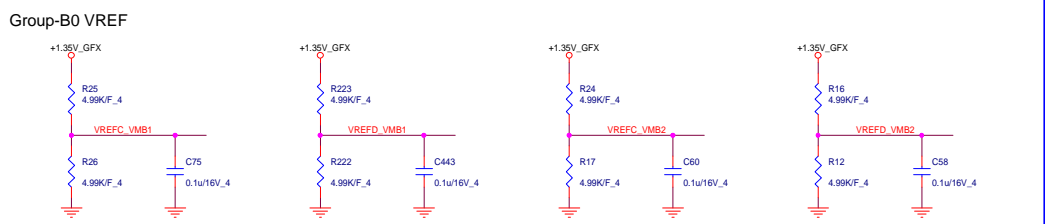
TOP Down

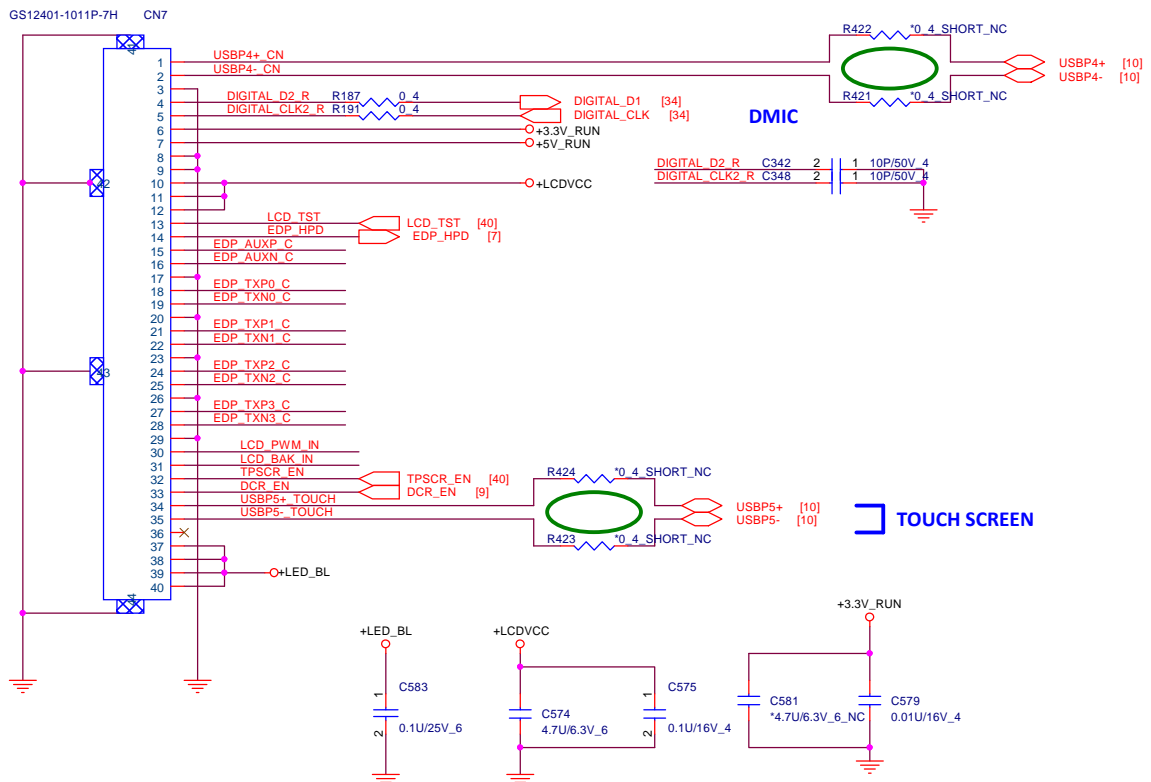


TOP Up

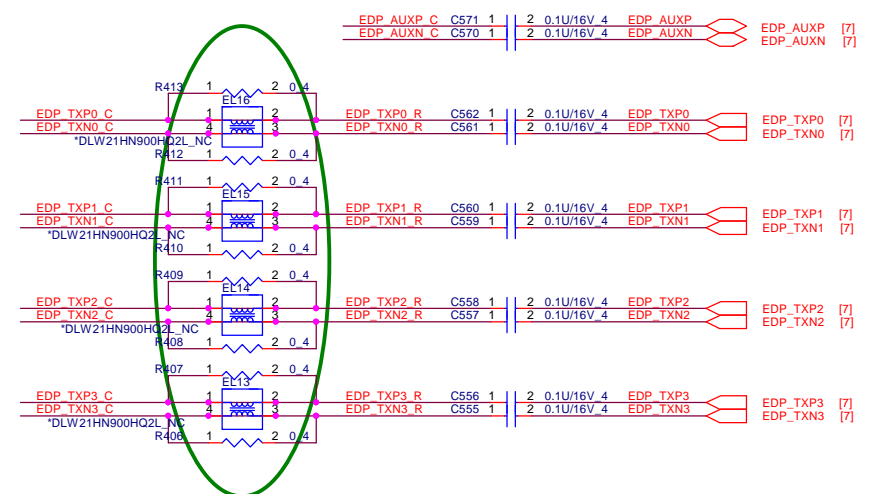


BOT Up

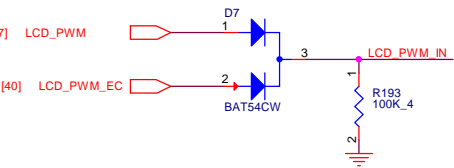




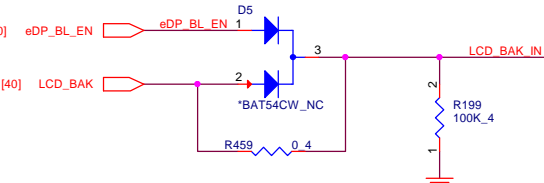
CAMERA



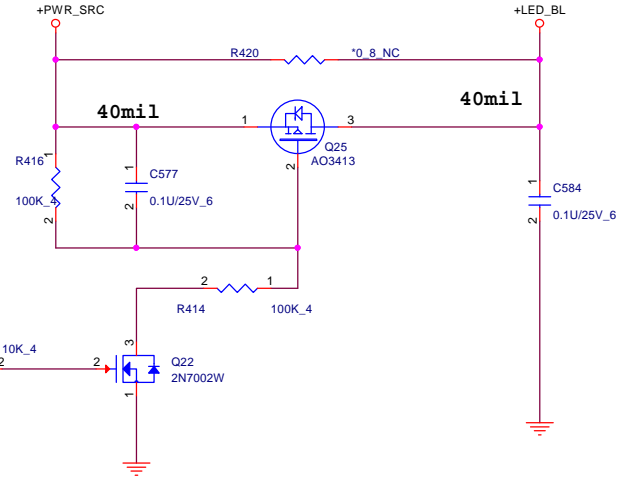
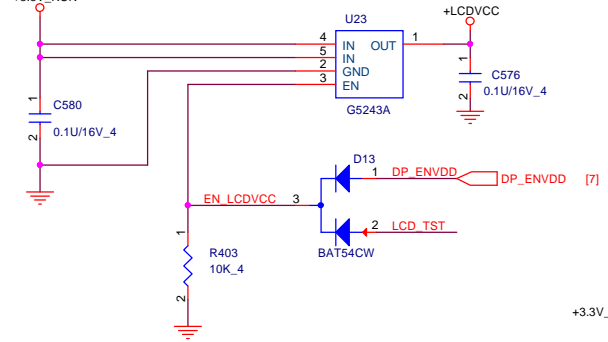
Brightness Control

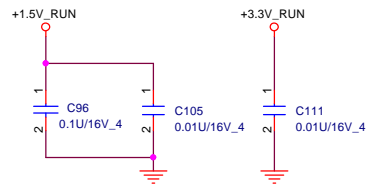


BAK_EN



LCD_VCC Imax(rating)=2.8A

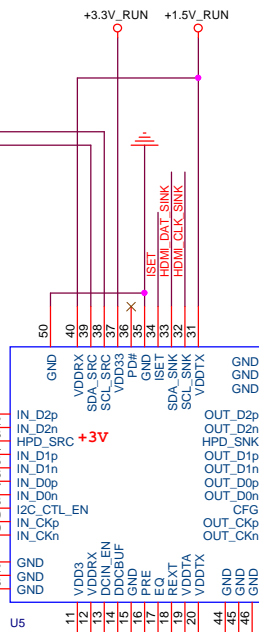




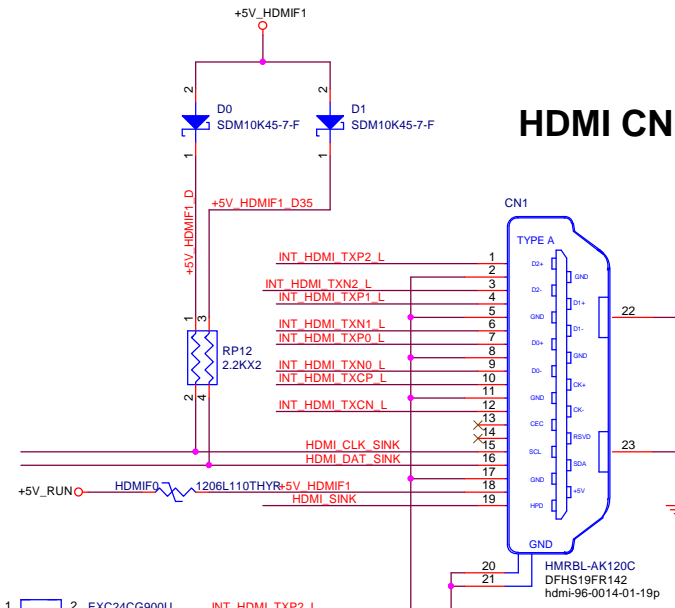
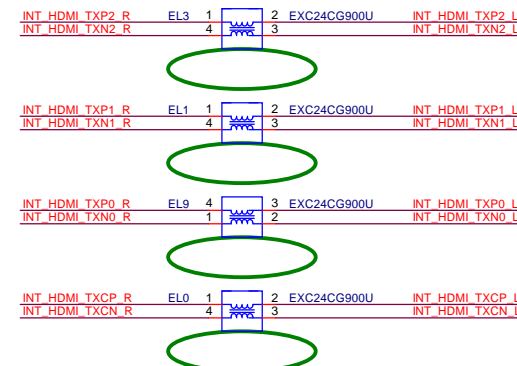
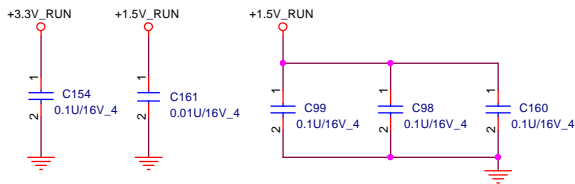
[7] HDMI_SCL
[7] HDMI_SDA

[7] INT_HDMI_TXP2
[7] INT_HDMI_TXN2
[7] INT_HDMI_HP
[7] INT_HDMI_TXP1
[7] INT_HDMI_TXN1
[7] INT_HDMI_TXP0
[7] INT_HDMI_TXN0
[7] INT_HDMI_TXCP
[7] INT_HDMI_TXCN

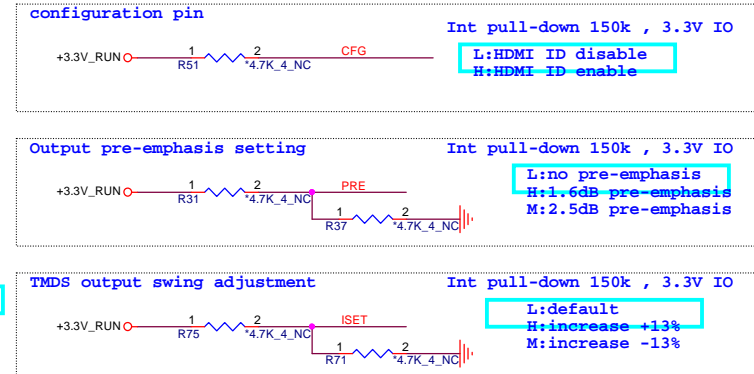
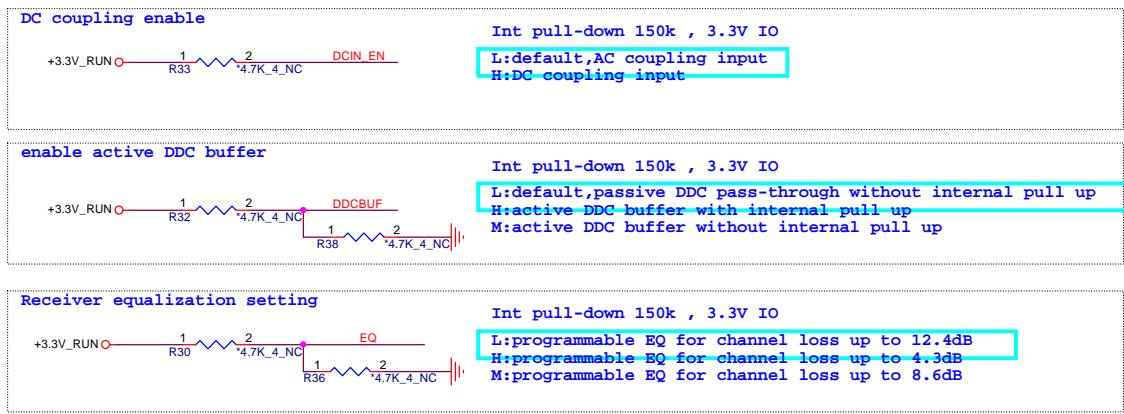
C157	1	2	0.1U/16V_4	INT_HDMI_TXP2_C	1
C147	1	2	0.1U/16V_4	INT_HDMI_TXN2_C	2
C141	1	2	0.1U/16V_4	INT_HDMI_TXP1_C	4
C136	1	2	0.1U/16V_4	INT_HDMI_TXN1_C	5
C127	1	2	0.1U/16V_4	INT_HDMI_TXP0_C	6
C117	1	2	0.1U/16V_4	INT_HDMI_TXN0_C	7
C115	1	2	0.1U/16V_4	INT_HDMI_TXCP_C	8
C112	1	2	0.1U/16V_4	INT_HDMI_TXCN_C	10



PS8401A



3 Level Input:
L:LOW, internal pull down
H:HIGH, external pull up
M:(VDD3)/2, both external pill-up and pull-down



Quanta Computer Inc.
PROJECT : AM6
HDMI

Size	Document Number	Rev
Date	Monday, May 05, 2014	A

Sheet 32 of 58

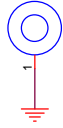
H8
*H-C158D158N_NC



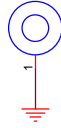
H20
*h-o114x98d114x98n_NC



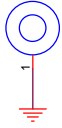
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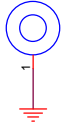
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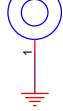
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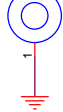
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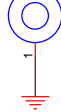
H9
*O-AM6-2_NC



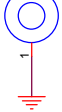
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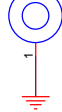
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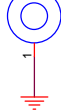
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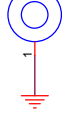
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H2
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H13
*O-AM6-1_NC



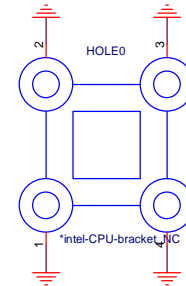
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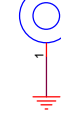
H5
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Bracket



H17
H-TC217BC141D141PT



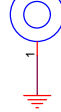
NGFF NUT

NUT

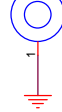
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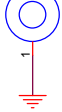
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H-TC217BC141D141PT




H18
H-TC217BC141D141PT

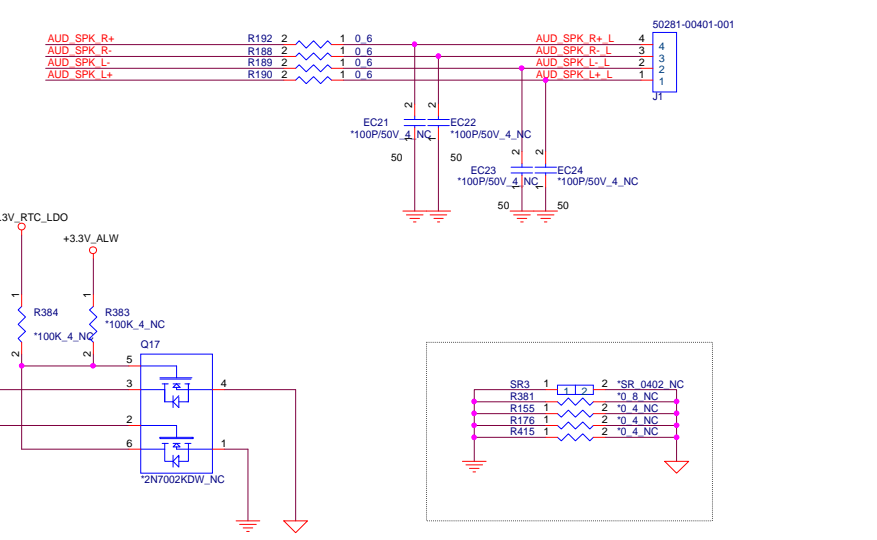
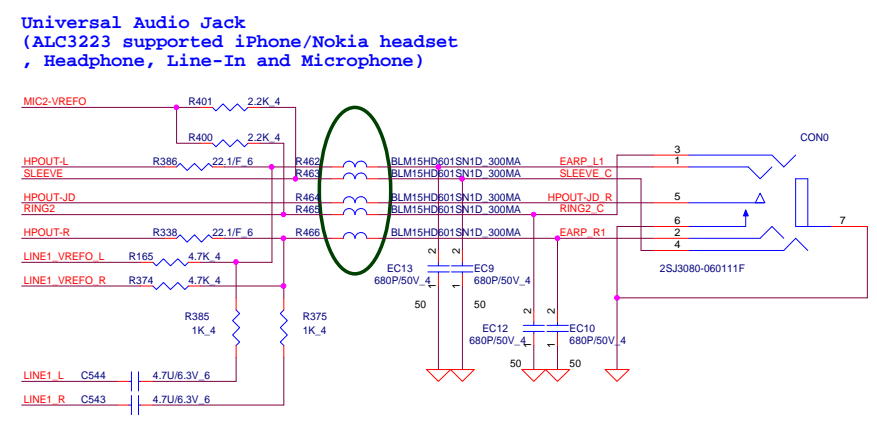
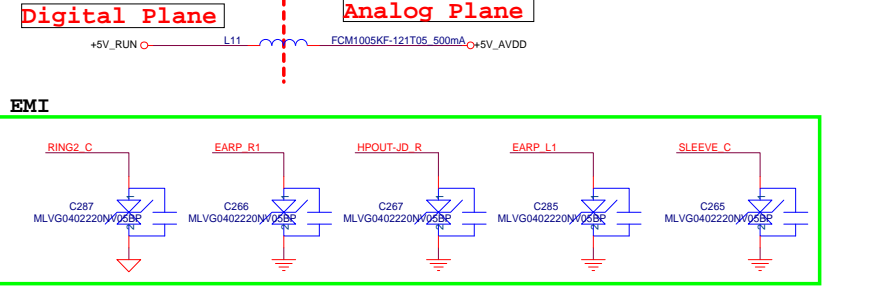
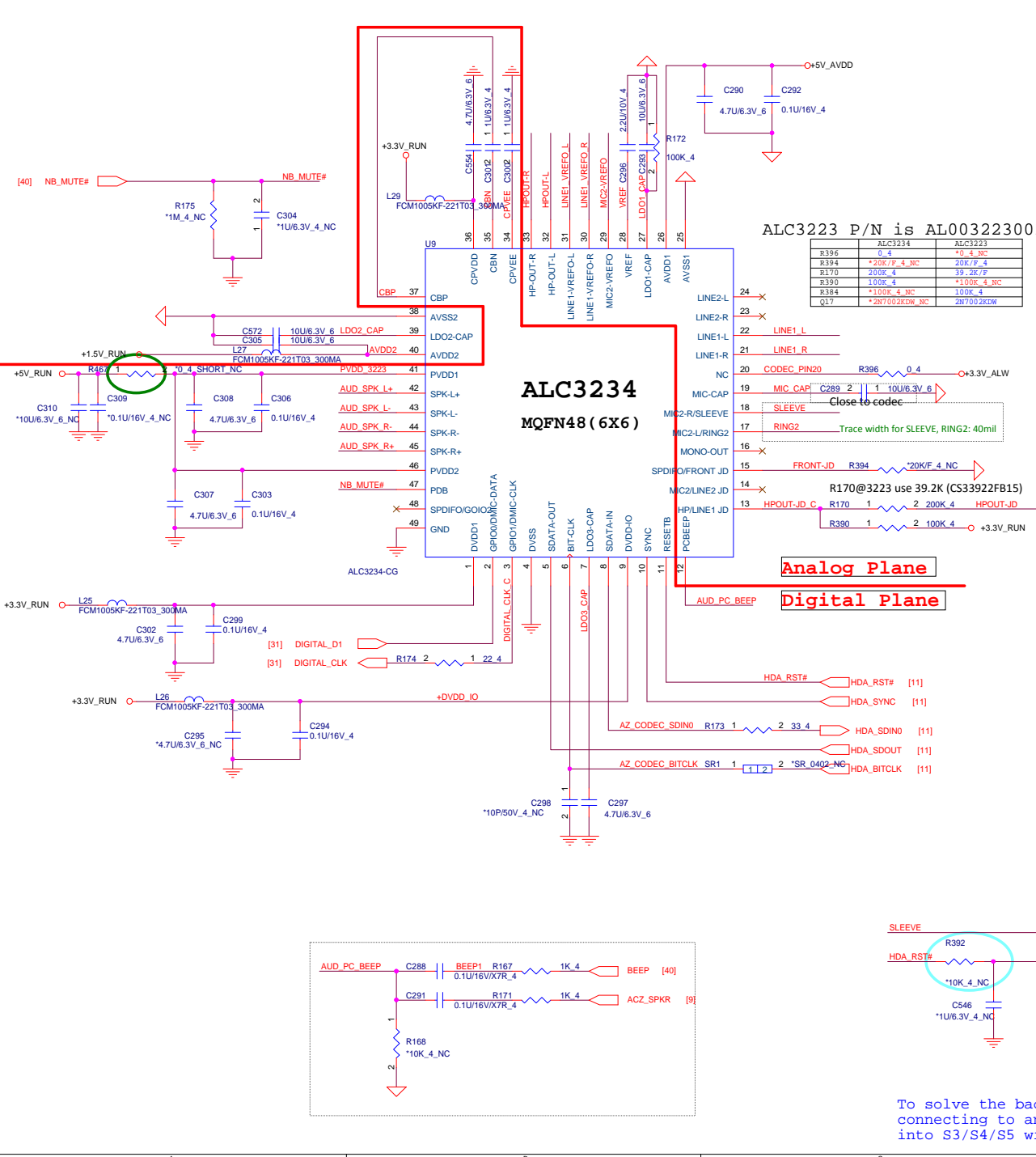


H19
H-TC217BC141D141PT



 **Quanta Computer Inc.**
PROJECT : AM6

Size	Document Number	Rev
		A
Hole		
Date:	Monday, May 05, 2014	Sheet 33 of 58



To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power

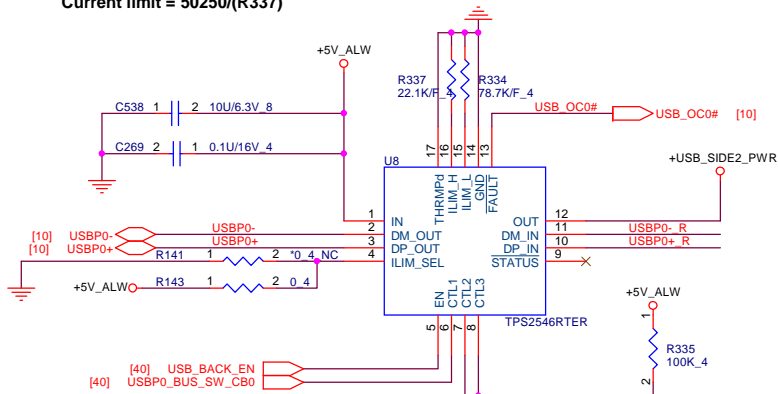
USB3.0 Power Share

USB Power share

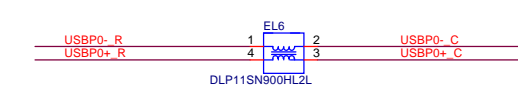
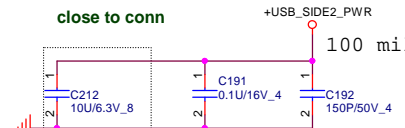
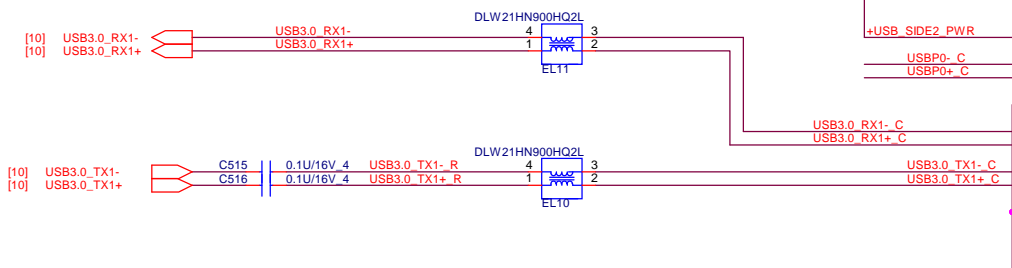
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.2

	R337	mA
OC limitation	100k ohm	504
	22.1k ohm	2274 Applied Now

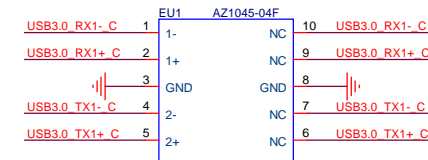
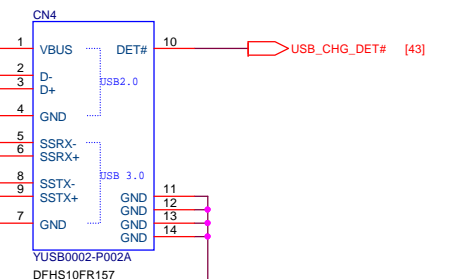
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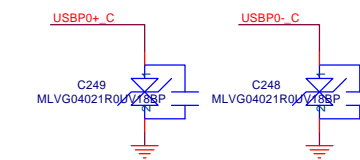
USB3.0/2.0 COMBO X 1



USB 3.0

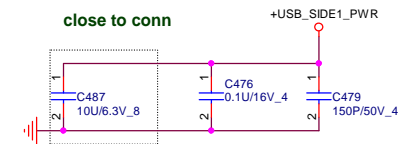
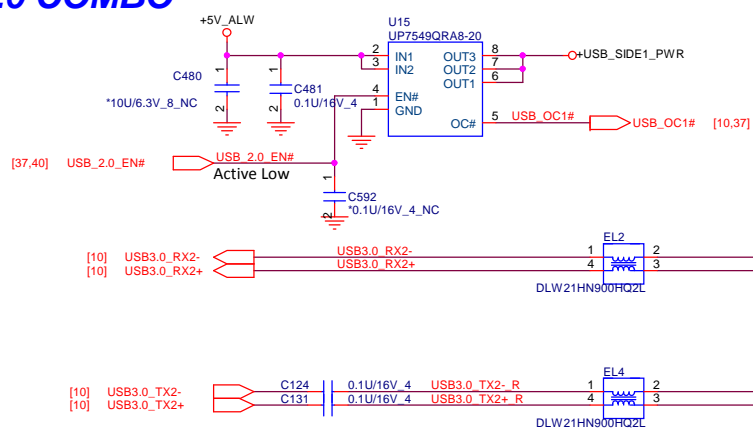


ESD Function
Place ESD diodes as close as USB connector.

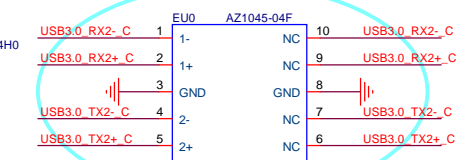
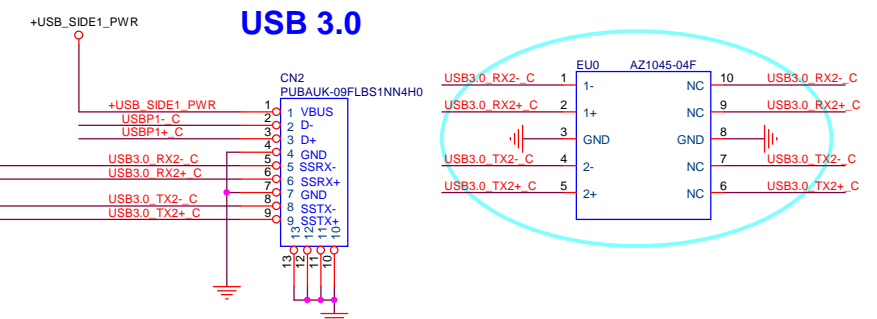


USB3.0/2.0 COMBO

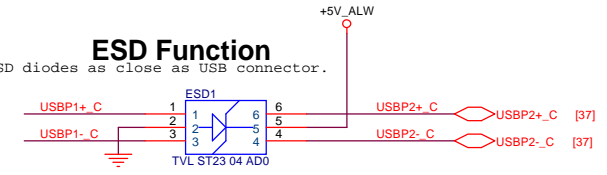
M15 Design Requirement:
I continuous 1.5A ; OC 2.0A



USB 3.0



ESD Function
Place ESD diodes as close as USB connector.

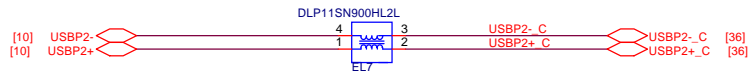
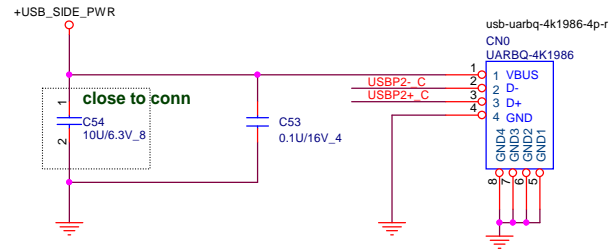
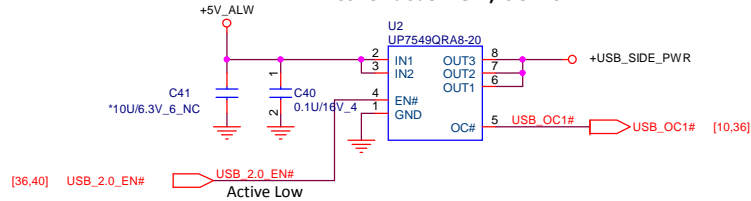


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PROJECT : AM6

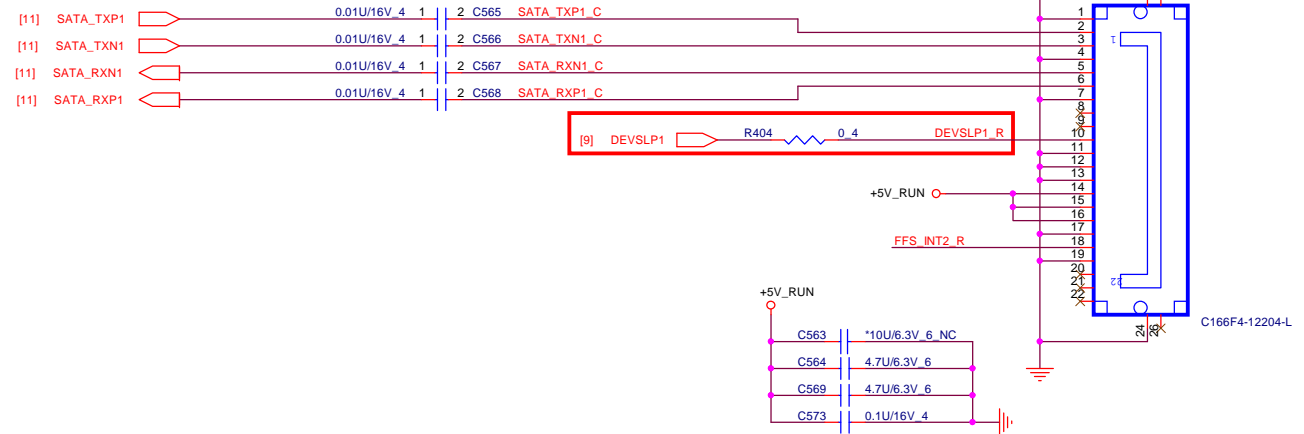
Size	Document Number	Rev
	USB3/USB Charger	A
Date:	Monday, May 05, 2014	Sheet 36 of 58

USB2.0 X1

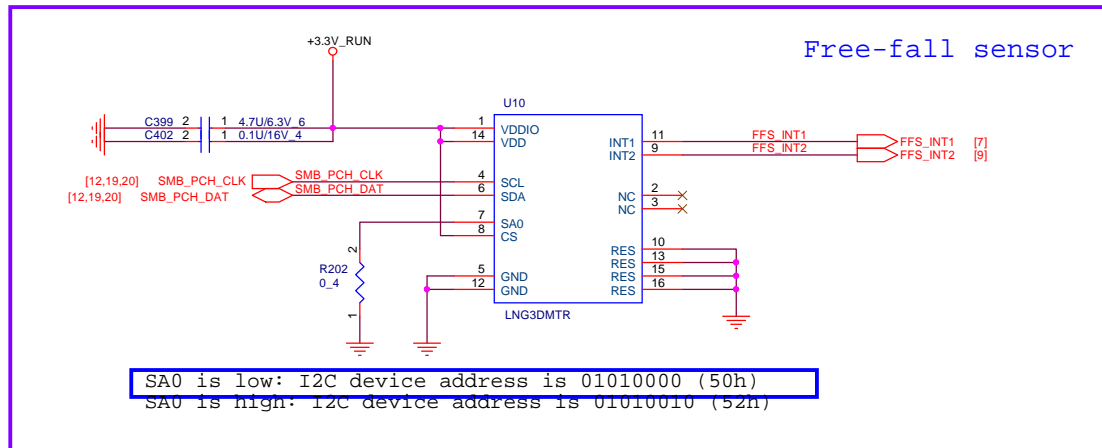
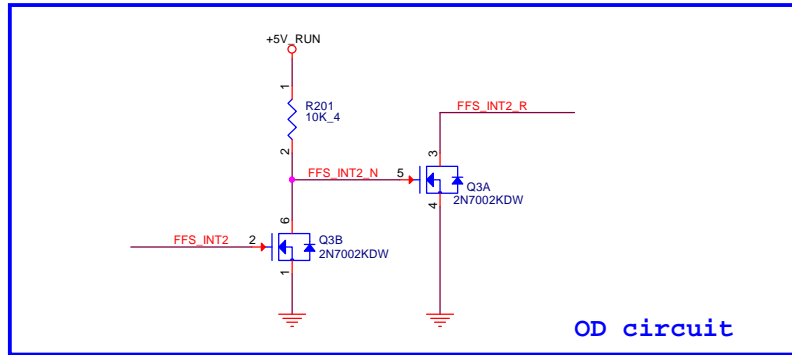
**M15 Design Requirement:
I continuous 1.5A ; OC 2.0A**



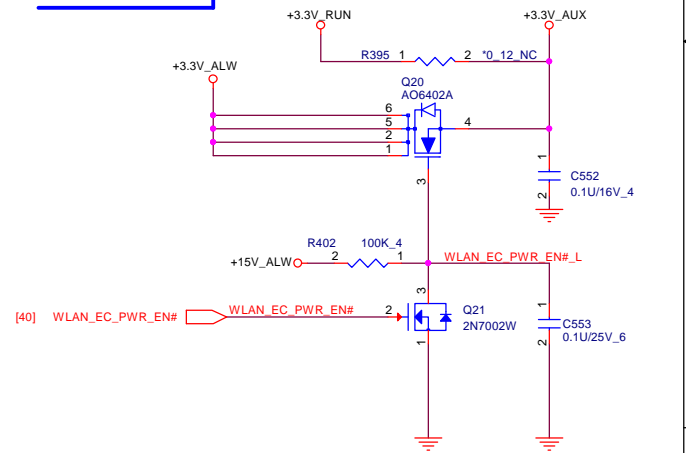
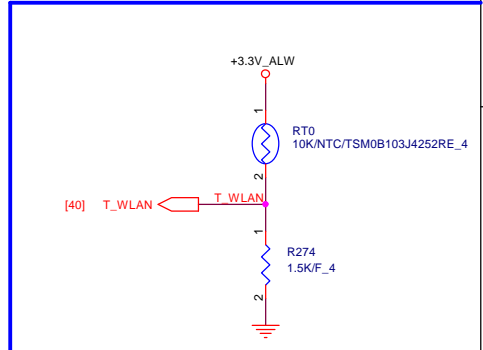
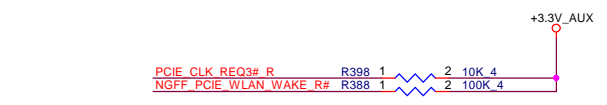
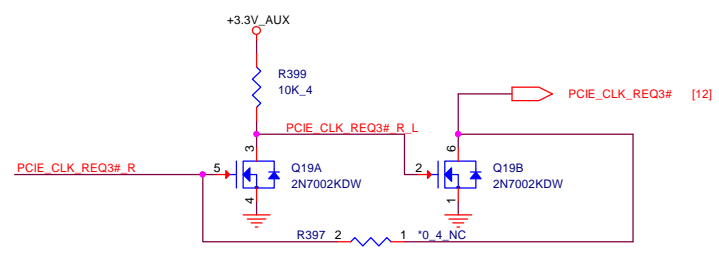
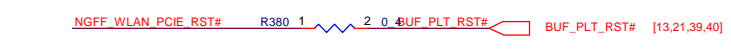
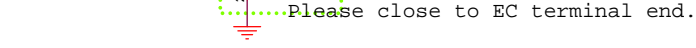
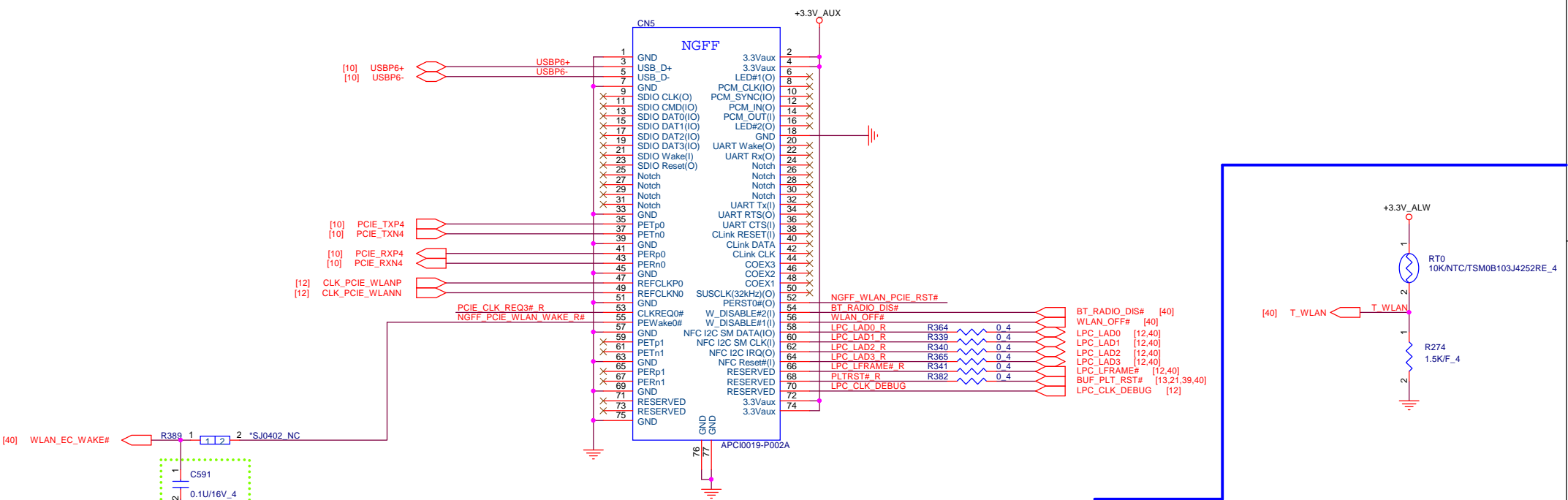
SATA HDD Connector



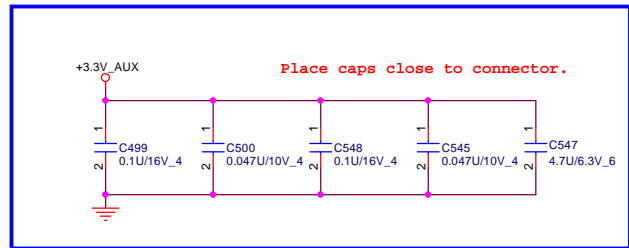
If you have two HDD, need add two OD circuit for Fall sensor interrupt circuit

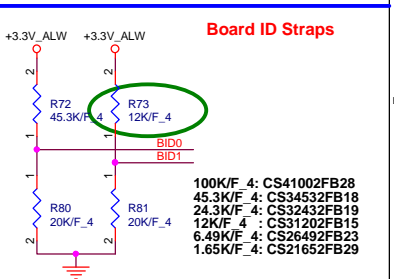
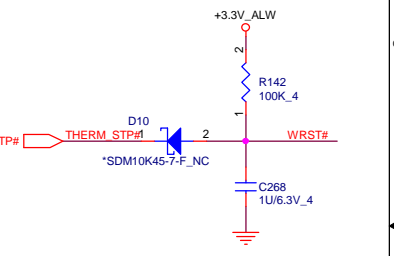
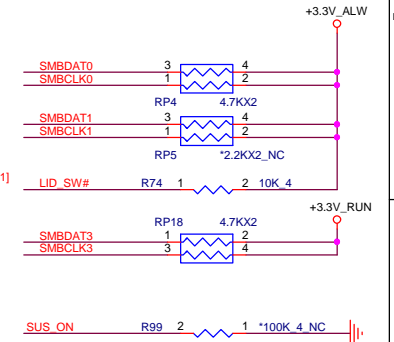
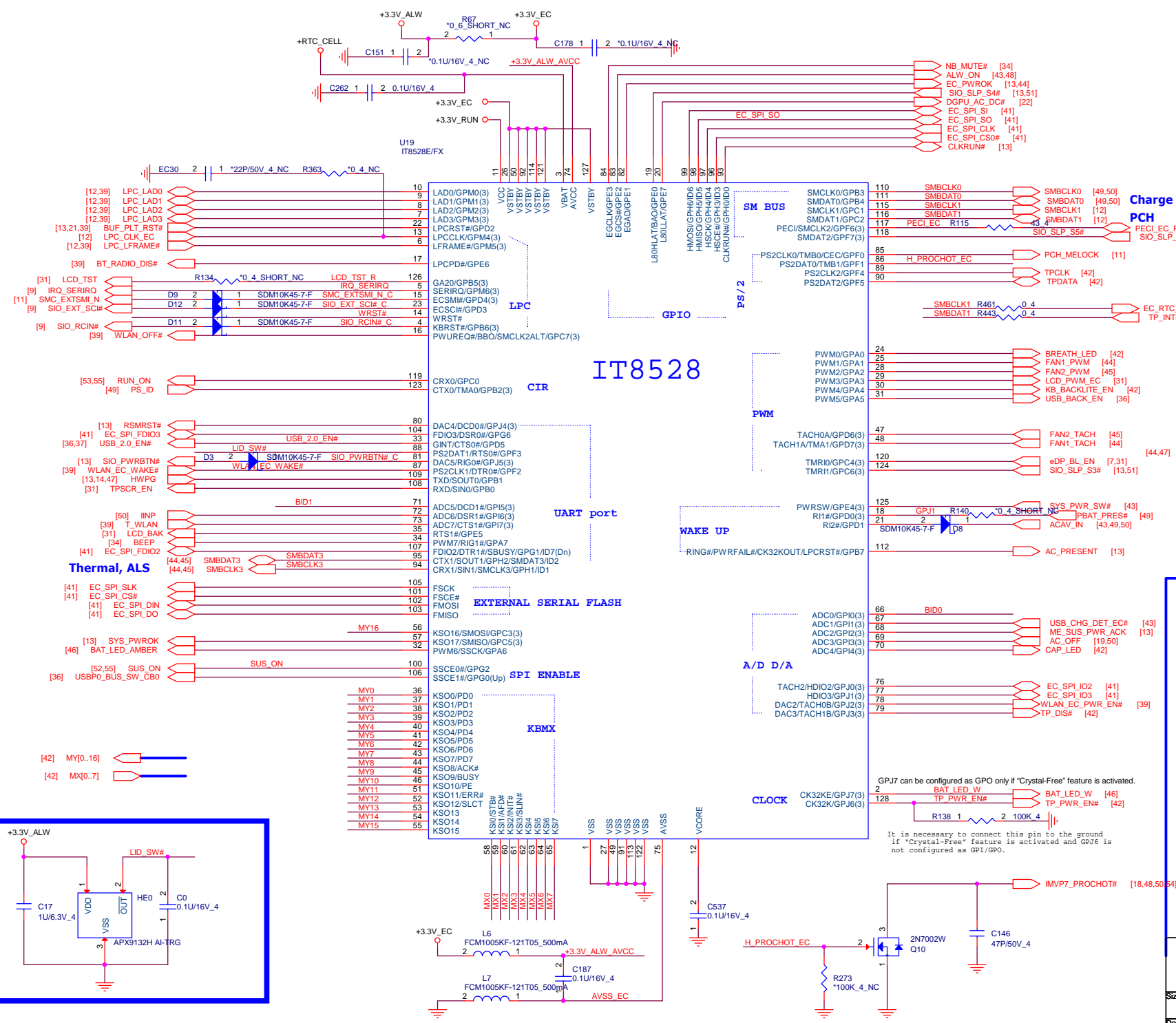
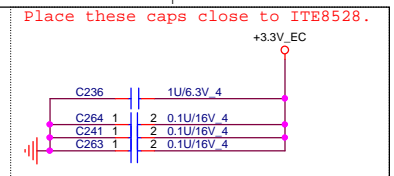


NGFF Wifi/BT connector



Support AOAC on WLAN





BD0	000	0.5V	PU 100K	HSW UMA
	001	1.0V	PU 45.3K	HSW DIS
	010	1.5V	PU 24.3K	BSW UMA
	100	2.0V	PU 12K	BDW DIS
	101	2.5V	PU 6.49K	
	110	3.0V	PU 1.65K	
	111	0V	NO PU	

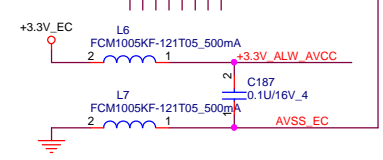
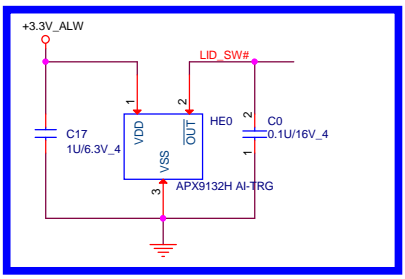
BD1	000	0.5V <th>PU 100K</th> <th>EVT (X00)</th>	PU 100K	EVT (X00)
	001	1.0V	PU 45.3K	DVT1 (X01)
	010	1.5V	PU 24.3K	DVT2 (X02)
	100	2.0V	PU 12K	Pilot Build (A00)
	101	2.5V	PU 6.49K	
	110	3.0V	PU 1.65K	
	111	0V	NO PU	

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PROJECT : AM6

SIO (ITE528H)

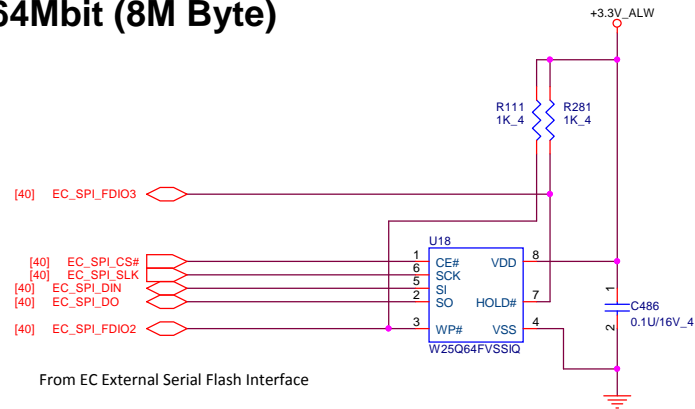
Date: Monday, May 05, 2014 Sheet 40 of 58



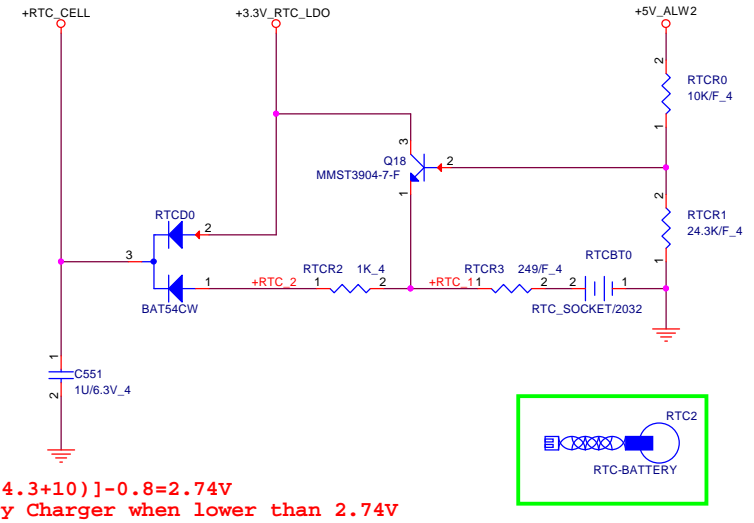
GPJ7 can be configured as GPO only if "Crystal-Free" feature is activated.

It is necessary to connect this pin to the ground if "Crystal-Free" feature is activated and GPJ6 is not configured as GPI/GPO.

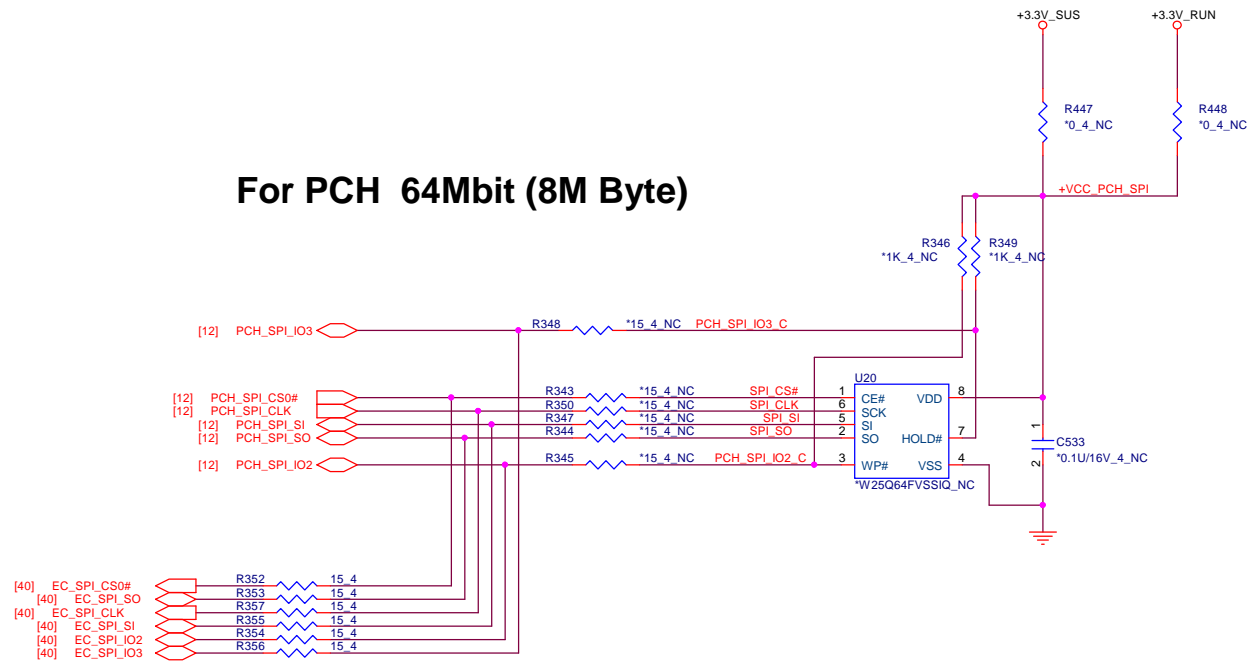
For EC 64Mbit (8M Byte)



RTC BATTERY



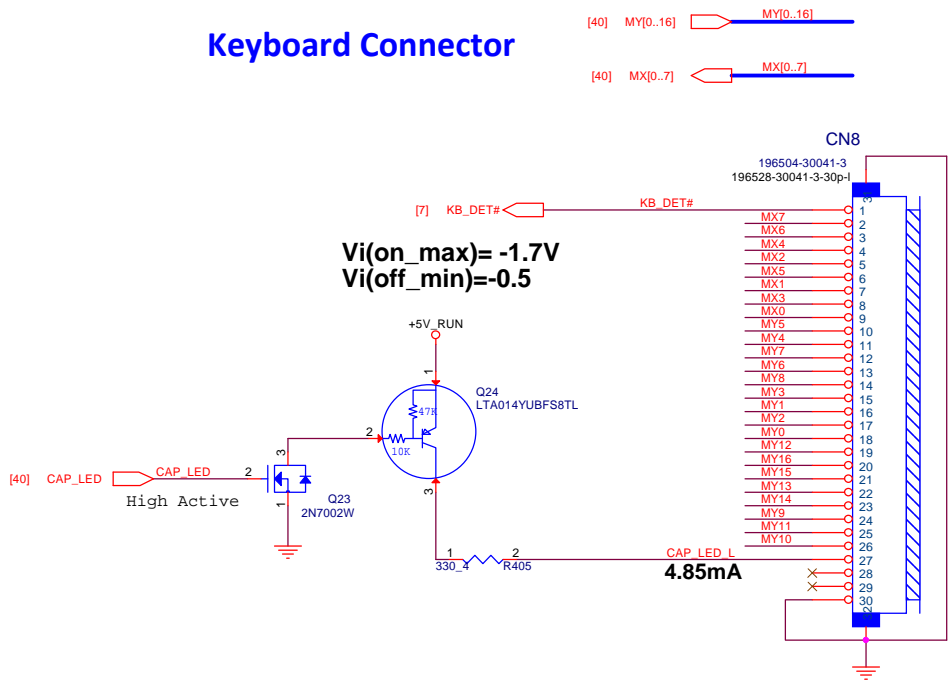
For PCH 64Mbit (8M Byte)



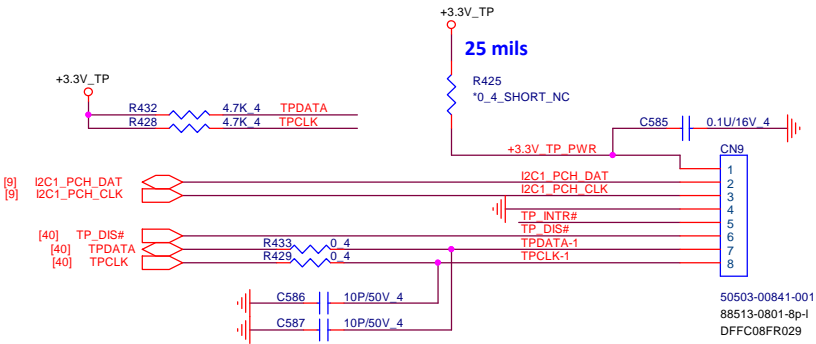
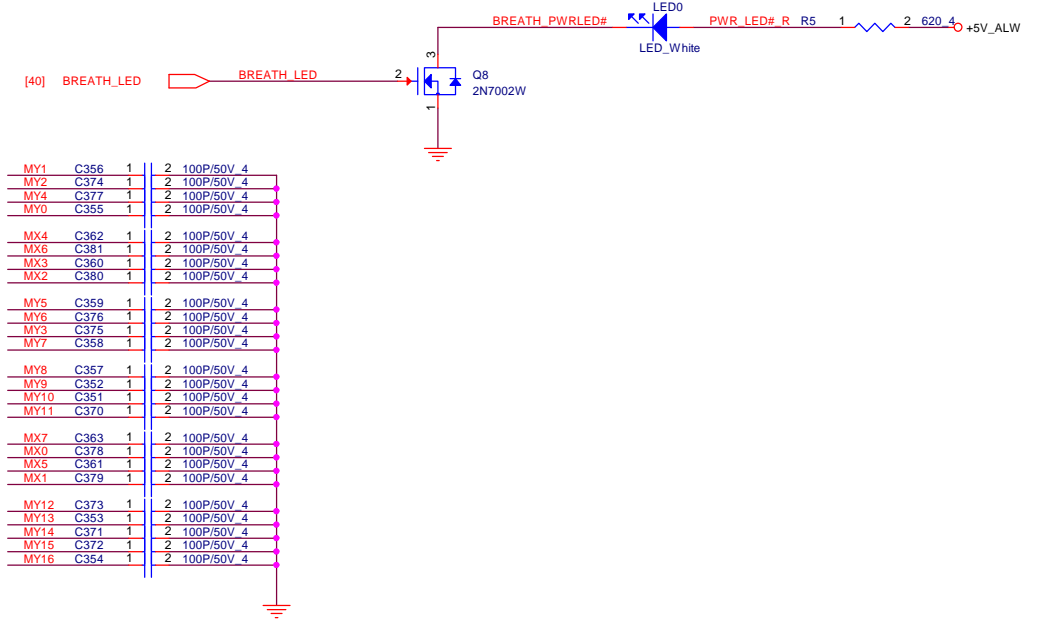
Quanta Computer Inc.

PROJECT : AM6

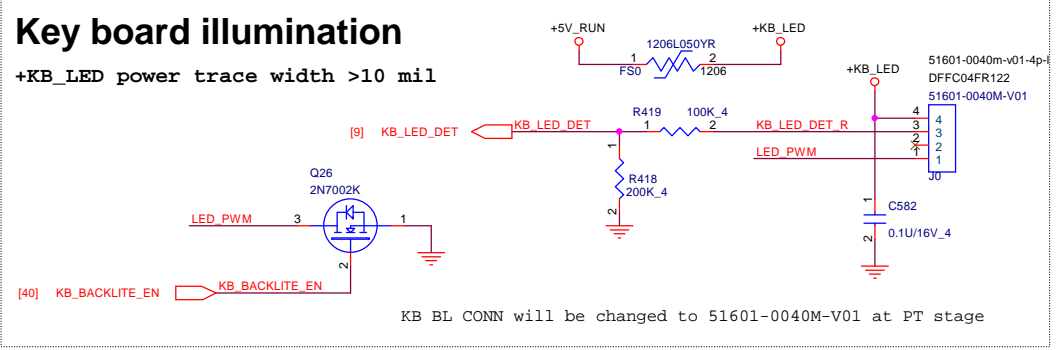
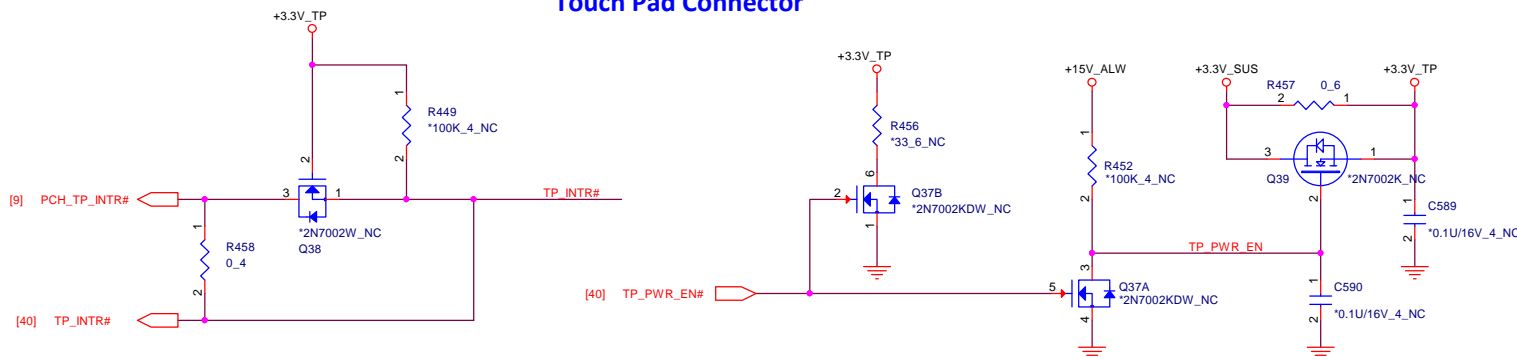
Keyboard Connector



BREATH_LED

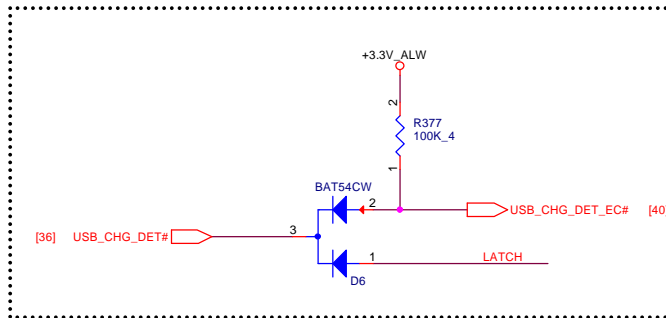
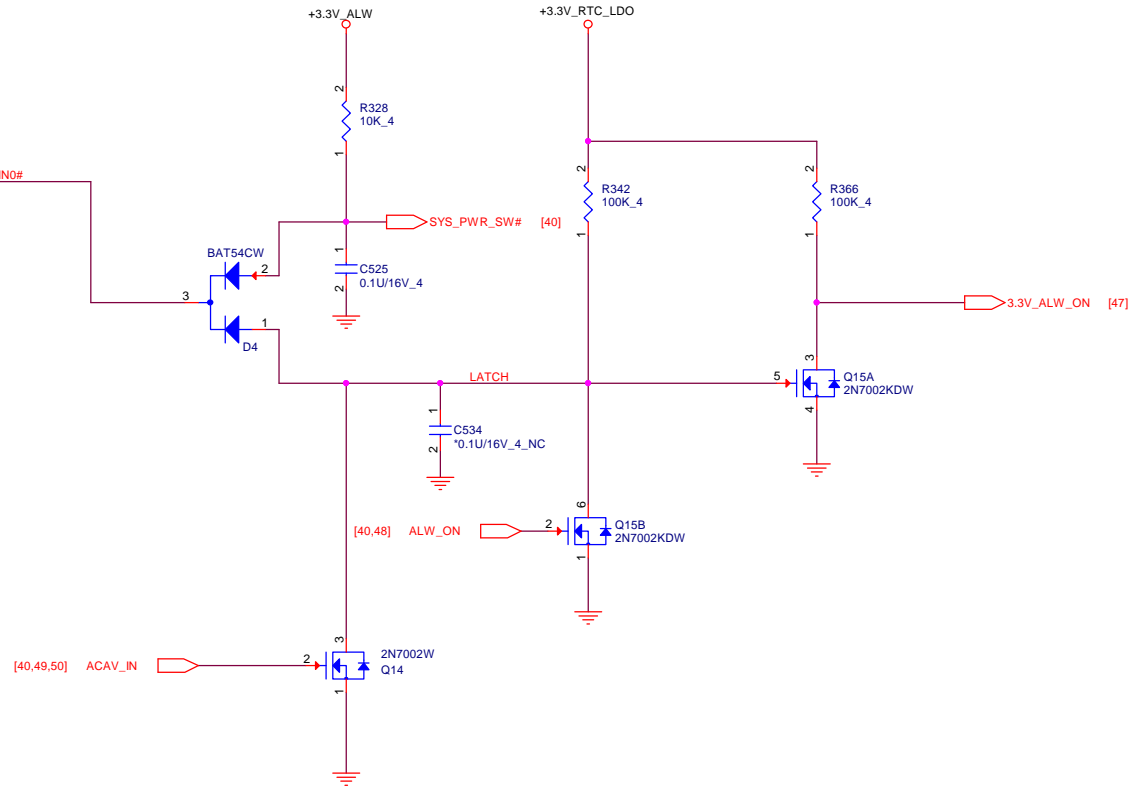
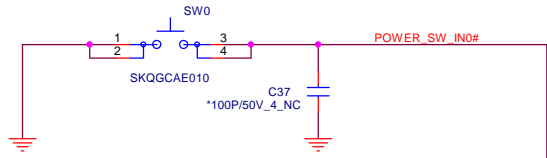


Touch Pad Connector

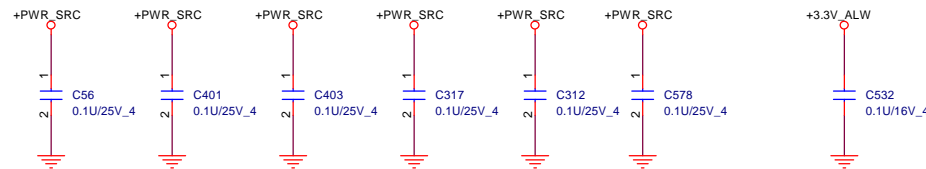


3VALW ON POWER LOGIC

POWER BUTTON



Stitching Capacitors

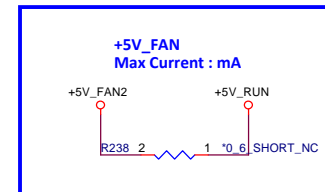
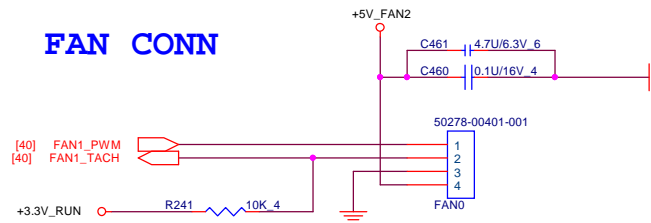


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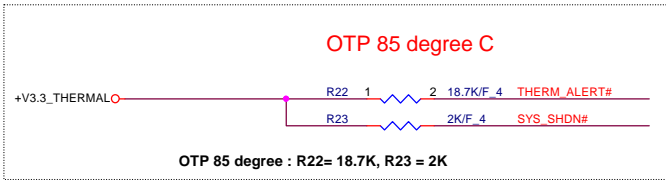
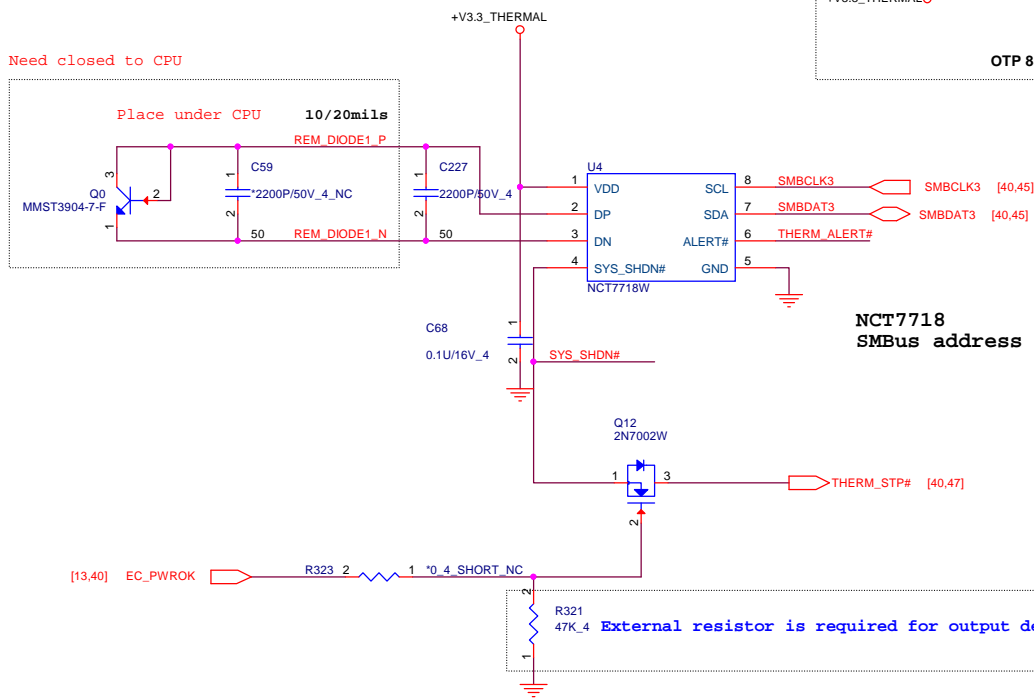
PROJECT : AM6

3VALW ON POWER LOGIC

FAN CONN

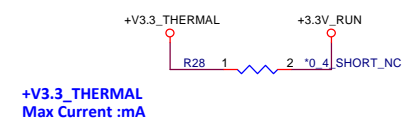


THERMAL IC



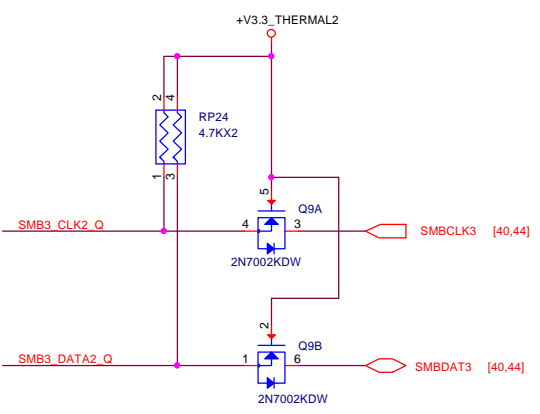
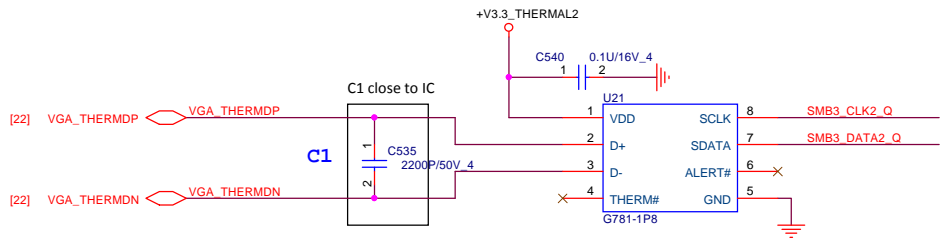
SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77°C	87°C	97°C	107°C	117°C
7.5K	79°C	89°C	99°C	109°C	119°C
10.5K	81°C	91°C	101°C	111°C	121°C
14K	83°C	93°C	103°C	113°C	123°C
18.7K	85°C	95°C	105°C	115°C	125°C

NCT7718
SMBus address is 1001100xb (98h) (x is R/W bit).

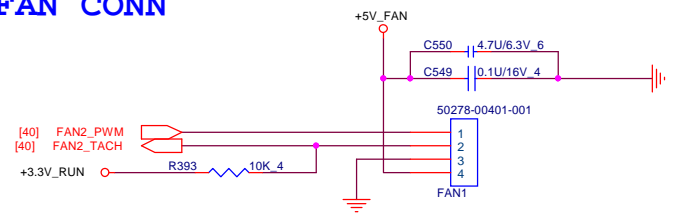


For GPU use

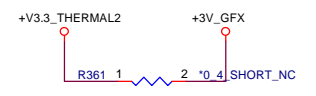
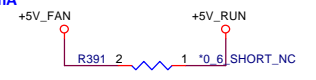
G781-1P8
 SMBus address is 1001101xb (9Ah) (x is R/W bit).



FAN CONN



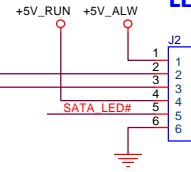
+5V_FAN
 Max Current : mA



+V3.3_THERMAL
 Max Current :mA

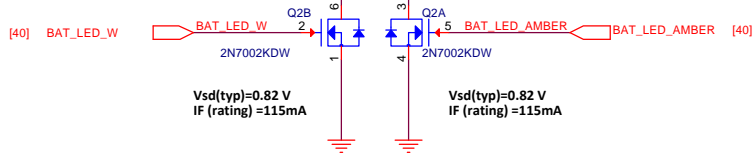
LED Status

LED Board

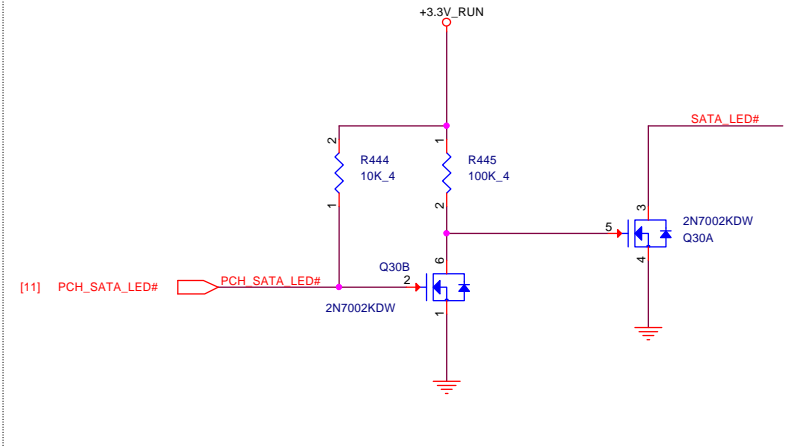


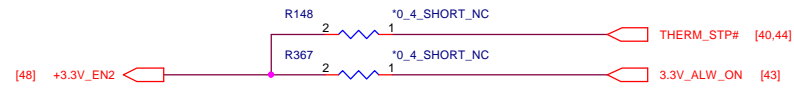
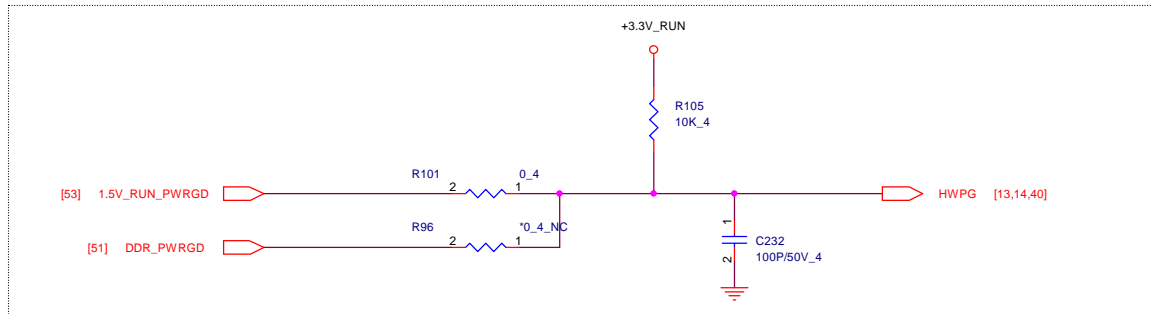
50501-00601-001
 DFFC06FR065
 88501-0601-6p-l-smt

Battrey charger LED



HDD activity LED.





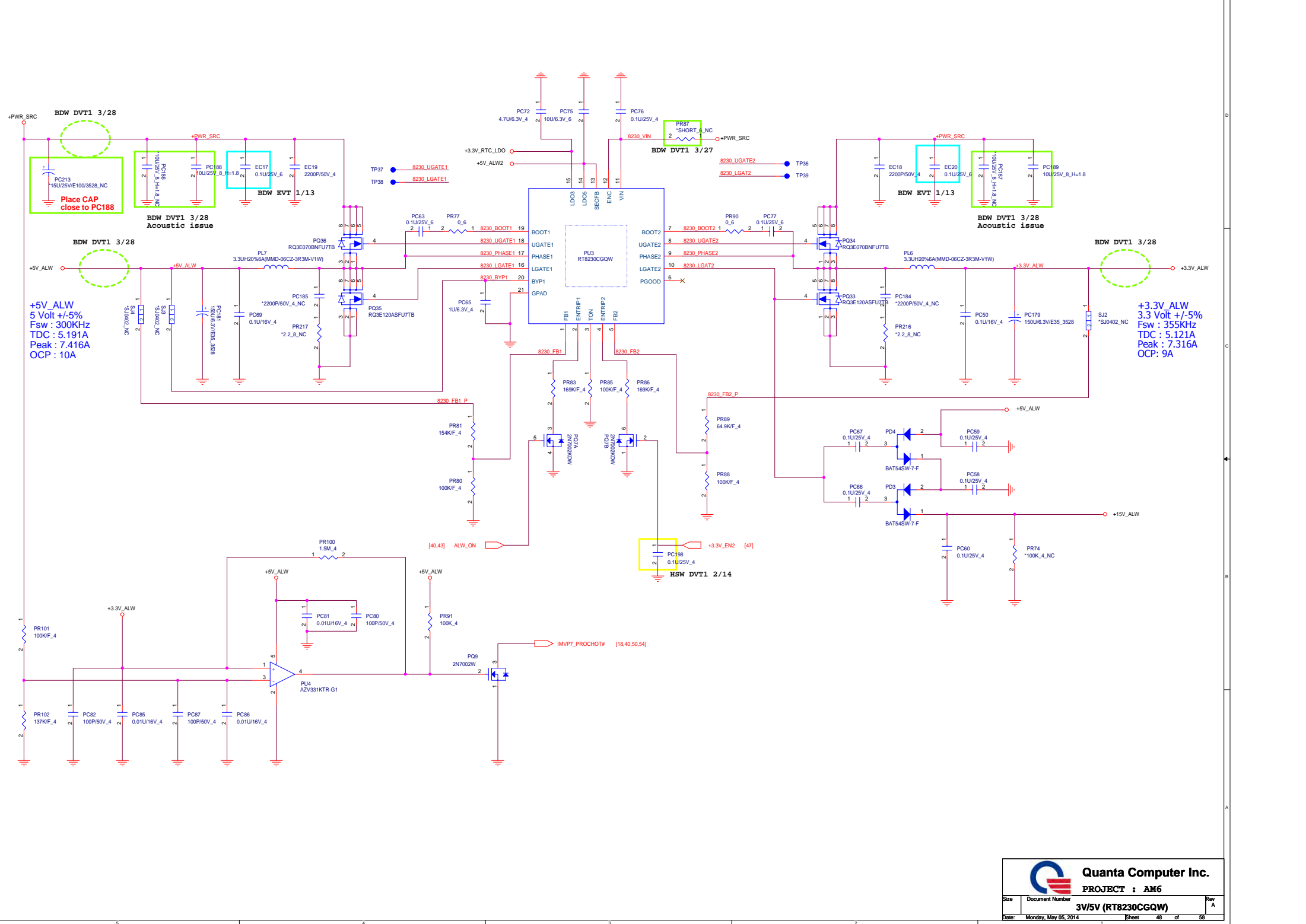
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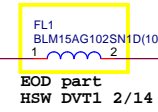
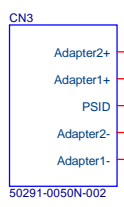
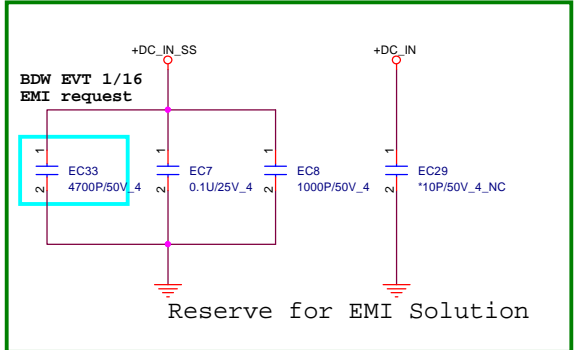
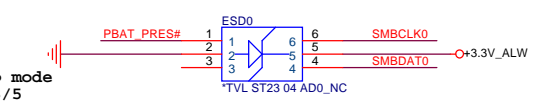
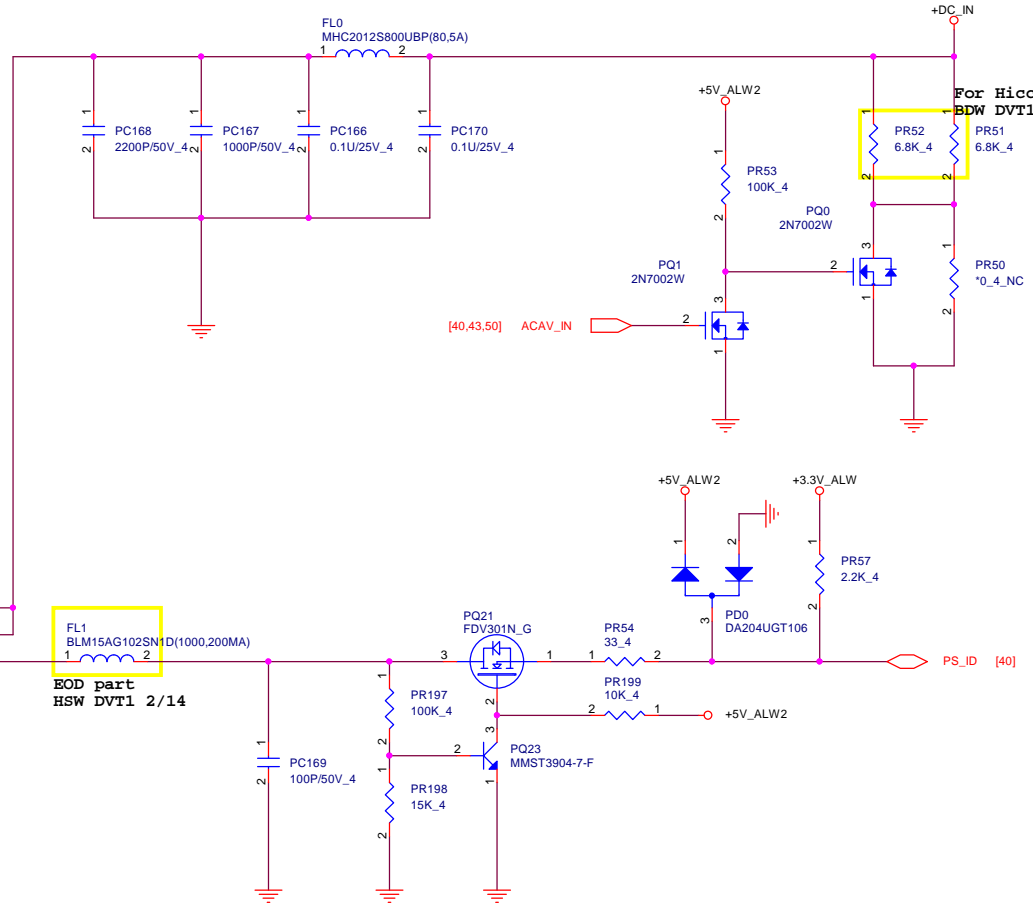
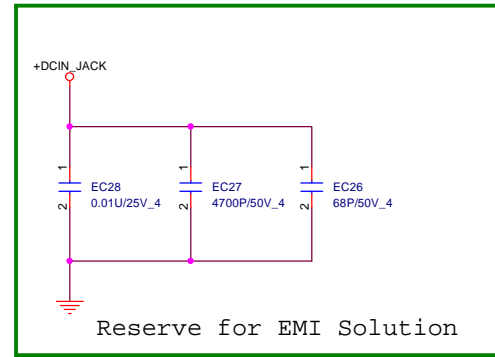
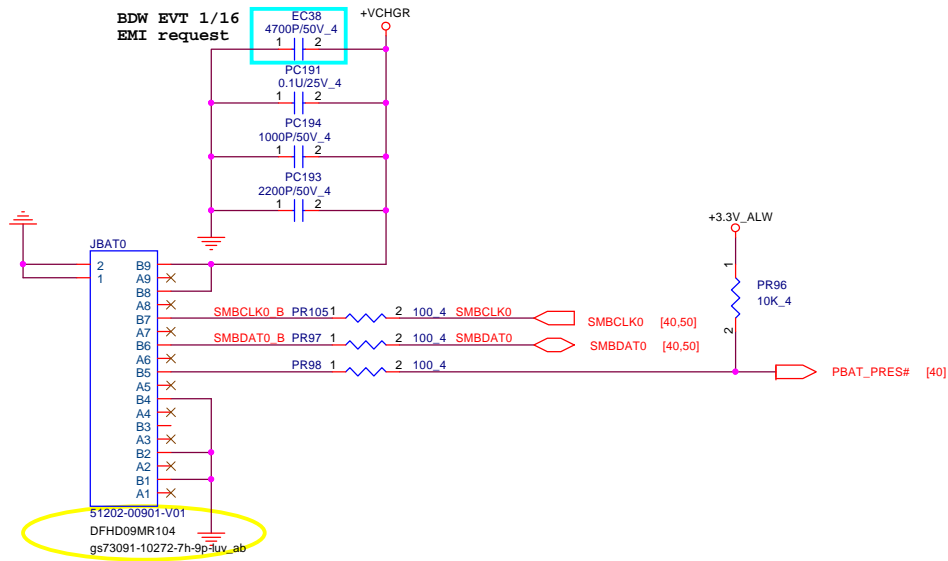
PROJECT : AM6

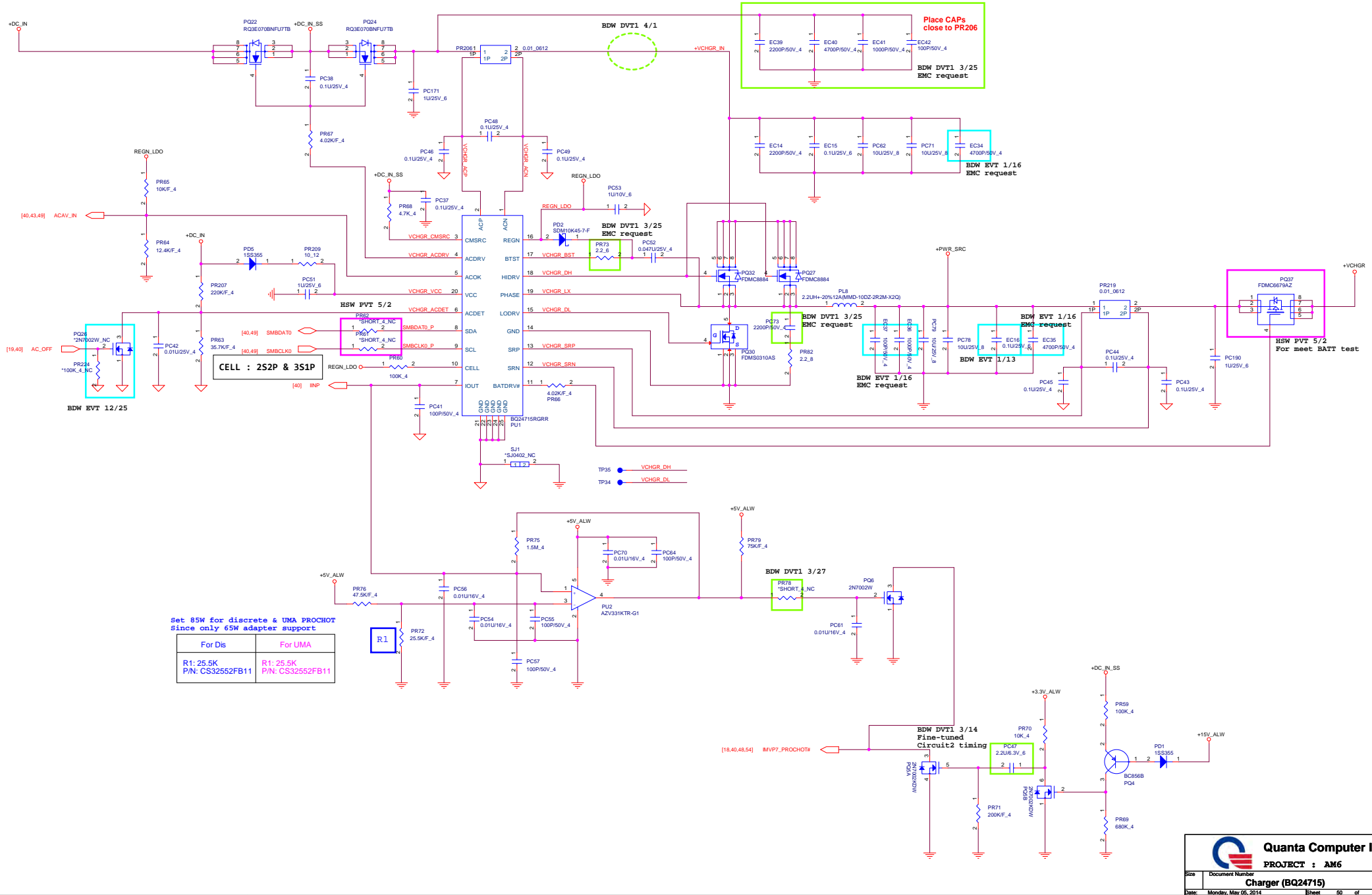
Size	Document Number	Rev
		A

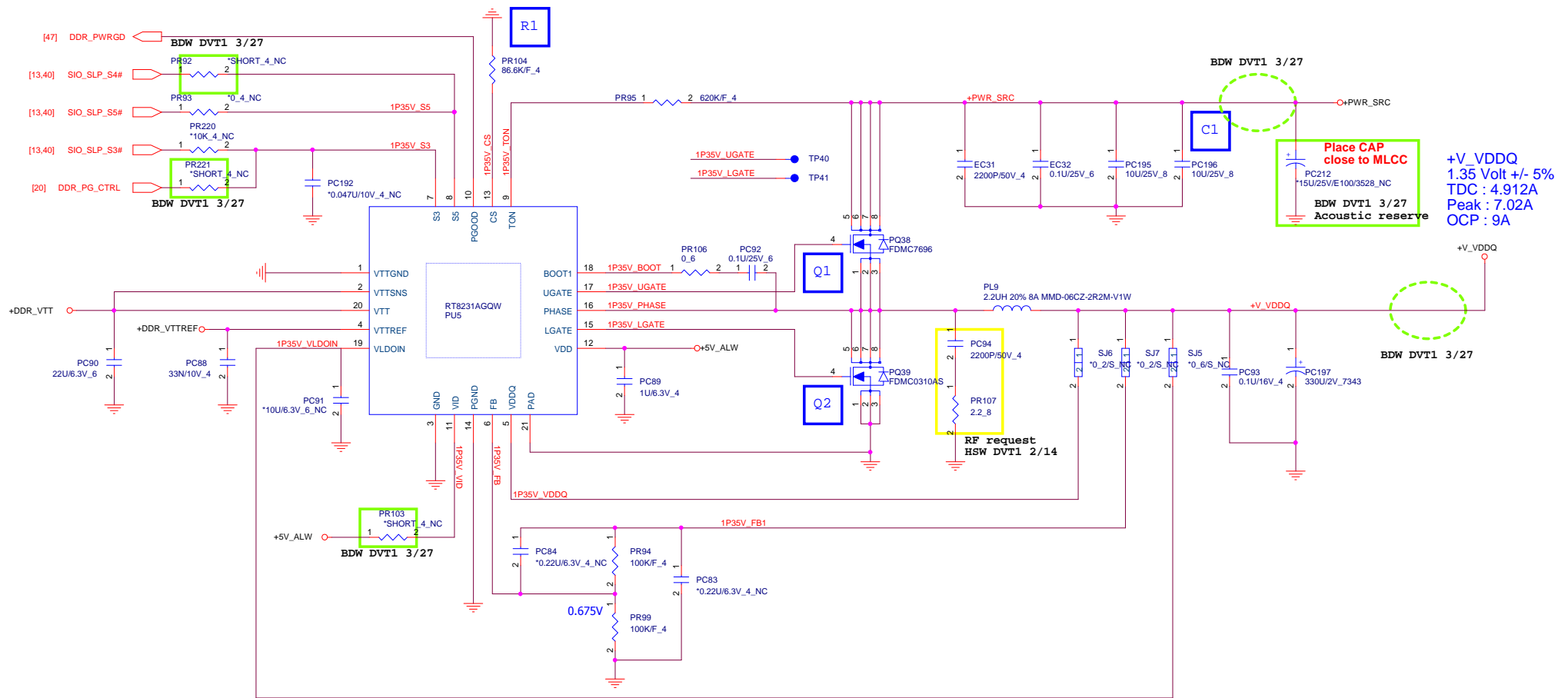
System Reset Circuit

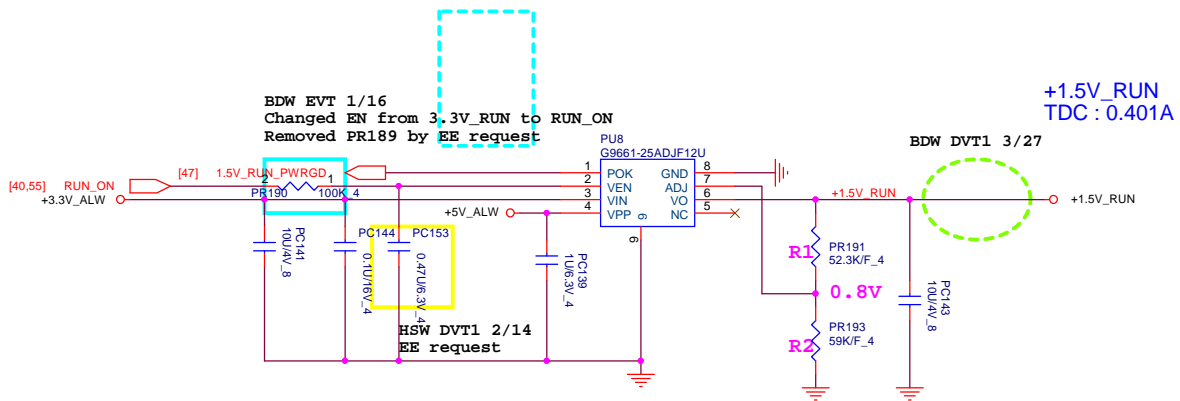
Date: Monday, May 05, 2014	Sheet 47 of 58
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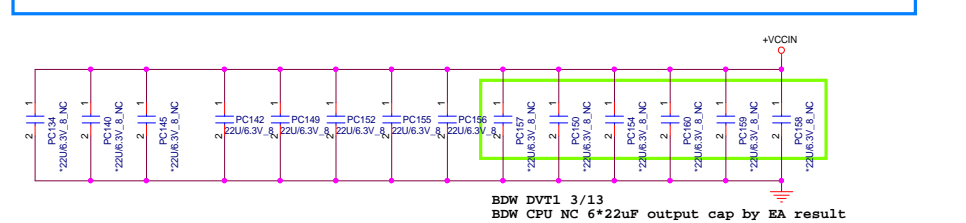
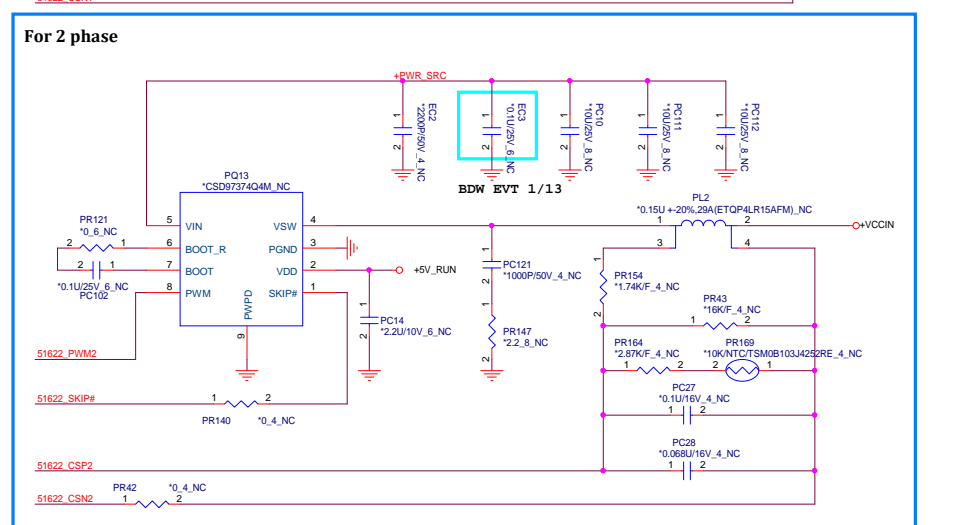
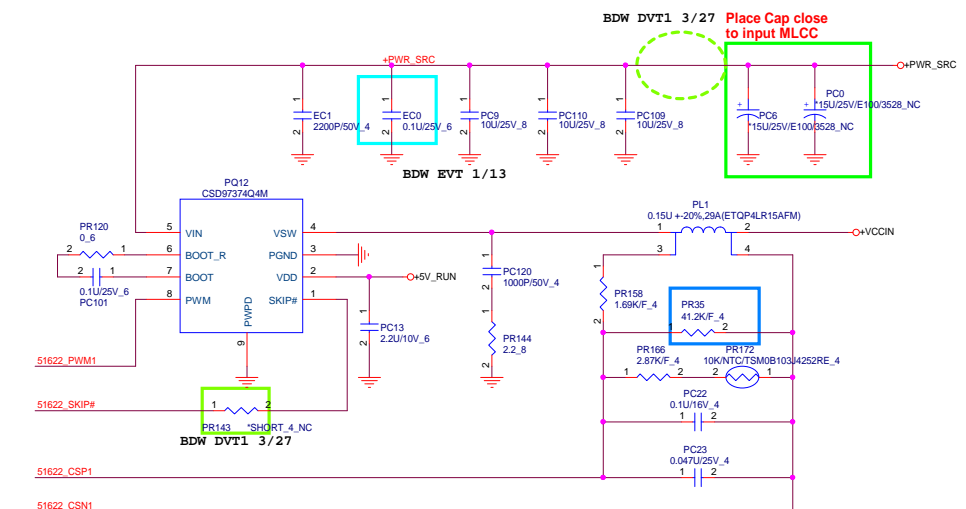
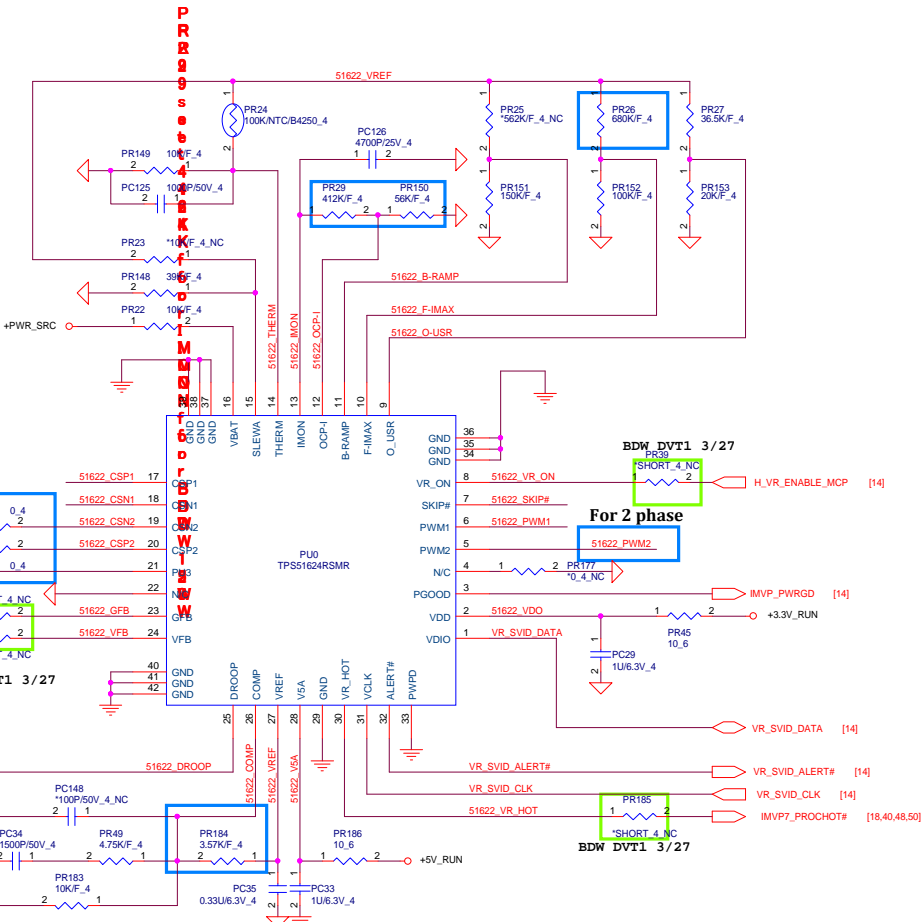


For BDW 15W change item
 PR26 680k → CS46802FB00
 PR29 412k → CS44122FB00
 PR150 56k → CS35602FB11
 PR35 41.2k → CS34122FB19
 PR184 3.57k → CS23572FB11

For BDW 28W change item
 PR26 523k → CS45232FB00
 PR29 464k → CS44642FB00
 PR150 75k → CS37502FB12
 PR35 22.6k → CS32262FB15
 PR184 3.65k → CS23652FB08

For HS	For BDW
IC1: TPS51622RSMR PN: AL051622001	IC1: TPS51624RSMR PN: AL051624000

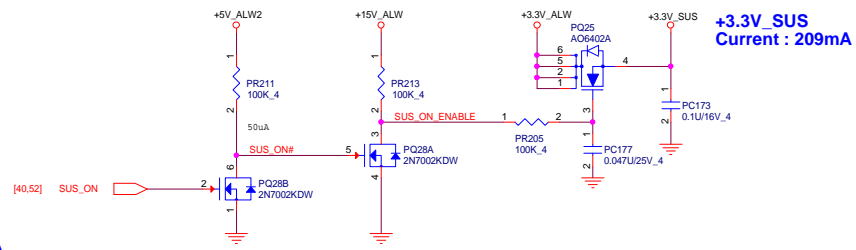
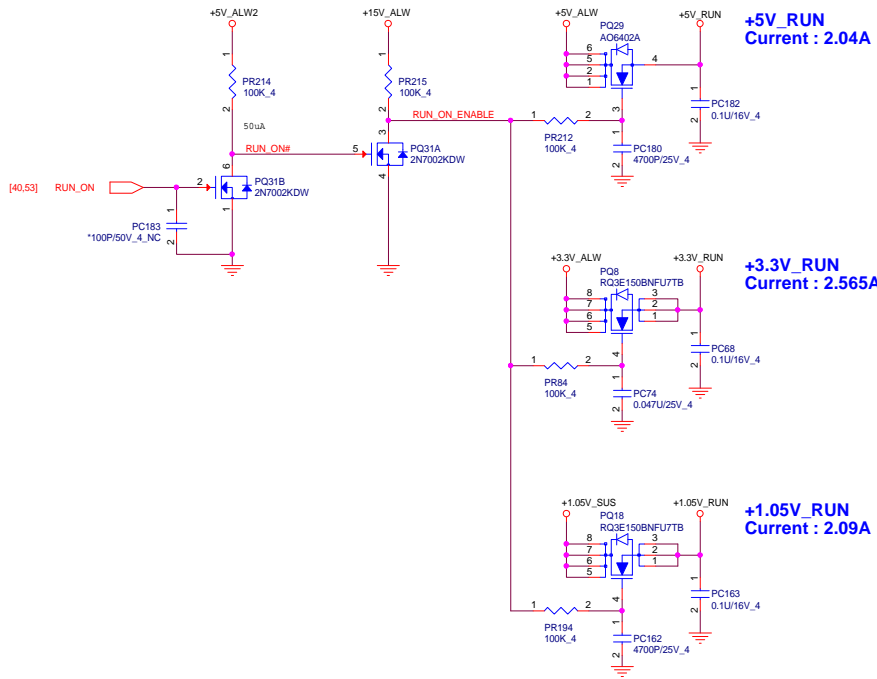
C O S T S
P I N N O



BDW DVT1 3/13
 BDW CPU NC 6*22uF output cap by EA result

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PROJECT : AM6

Size	Document Number	Rev
	CPU Core (TPS51624RSMR)	A
Date:	Monday, May 05, 2014	Sheet 54 of 58



+1.35V_GFX Volt +/- 5%
TDC: 2.585A
Peak: 4A
OCP: 6A

Boot VID voltage is 0.9V
 Set OFSA to 1.65V
 $+1.35V_GFX = (1.65 - 1.2) + 0.9 = 1.35V$

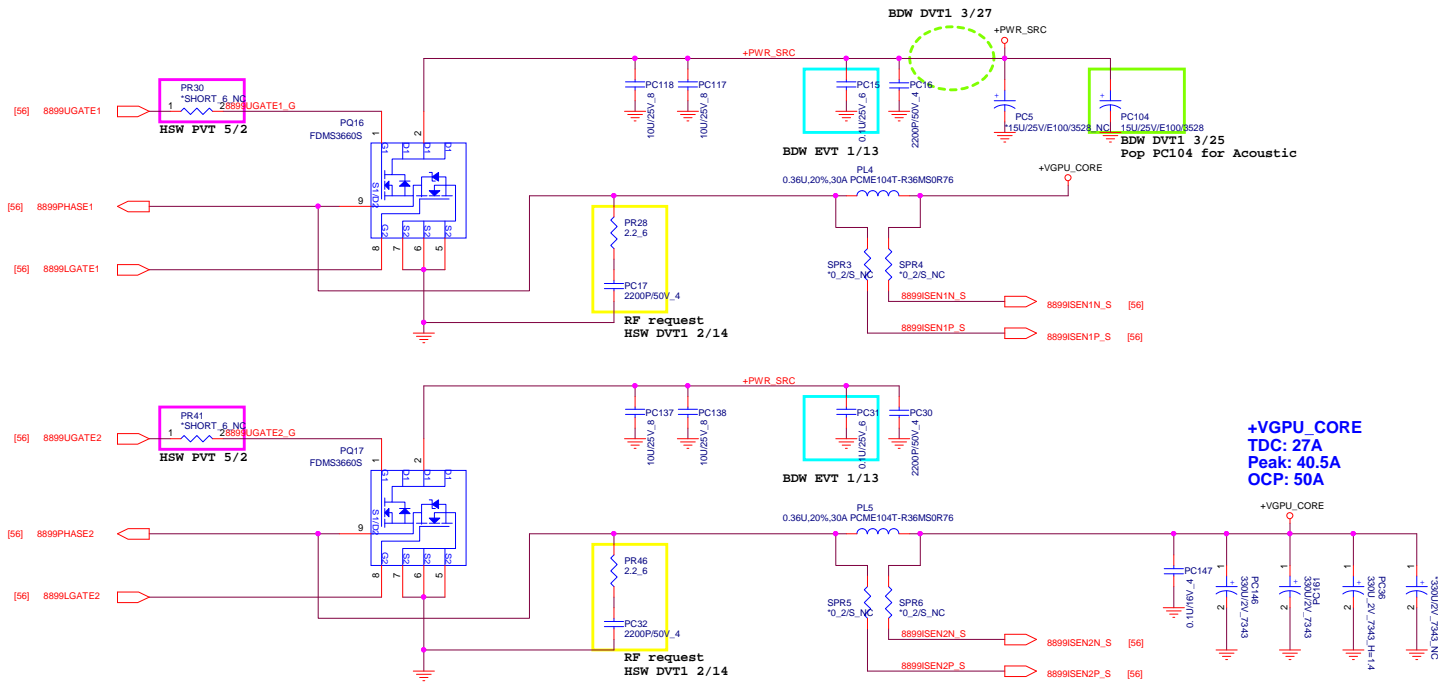
+1.05V_GFX
Current : 1.33A

+3V_GFX
Current : 22mA

BDW DVTT1 3/31, confirmed with EE
 Add +1.8V_GFX discharge circuit

BDW EVT 1/13, confirmed with EE
 Add +3V_GFX discharge circuit

Title	<Title>		Rev	A
Size	Document Number	Customer-Doc		
Date:	Monday, May 05, 2014	Sheet	56	of 58



BDW DVT1 3/27

BDW EVT 1/13

BDW DVT1 3/25

Pop PC104 for Acoustic

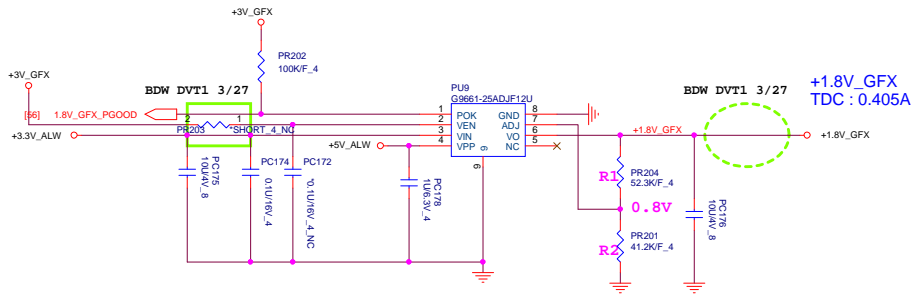
RF request
HSW DVT1 2/14

BDW EVT 1/13

+VGPU_CORE
TDC: 27A
Peak: 40.5A
OCP: 50A

RF request
HSW DVT1 2/14

Title	<Title>	Rev	A
Size	Document Number		
	Custom-Doc>		
Date:	Monday, May 05, 2014	Sheet	57 of 58



Title		<Title>
Size	Document Number	Rev A
Date: Monday, May 05, 2014		Sheet 58 of 58