

**MODEL NAME : VBW00**  
**PROJECT CODE : ANRVBW0100**  
**PCB NO : DA8000WK000 LA-9981P M/B**  
**DA40001FO00 LS-9101P POWER BUTTON/B**  
**DA40001FP00 LS-9102P USB/B**  
**DA40001FQ00 LS-9103P TP BUTTON/B**

# Dell / Compal Confidential

## Schematic Document

**Intel Shark Bay ULT**  
**OAK Value2**  
**UMA/DIS AMD Sun XT**

2013-03-09

Rev: 0.2

**X76@ : 76 level**  
**46@ : 46 level**  
**@ : Nopop component**  
**CONN@ : Connector component**  
**XDP@ : XDP function**  
**UMA@ : Only for UMA**  
**DIS@ : Only for Discrete**  
**SUN@ : SUN XT**  
**EMI@ : EMI parts**  
**@EMI@ : Reserve EMI parts**  
**ESD@ : ESD parts**  
**RF@ : RF parts**

BOM config

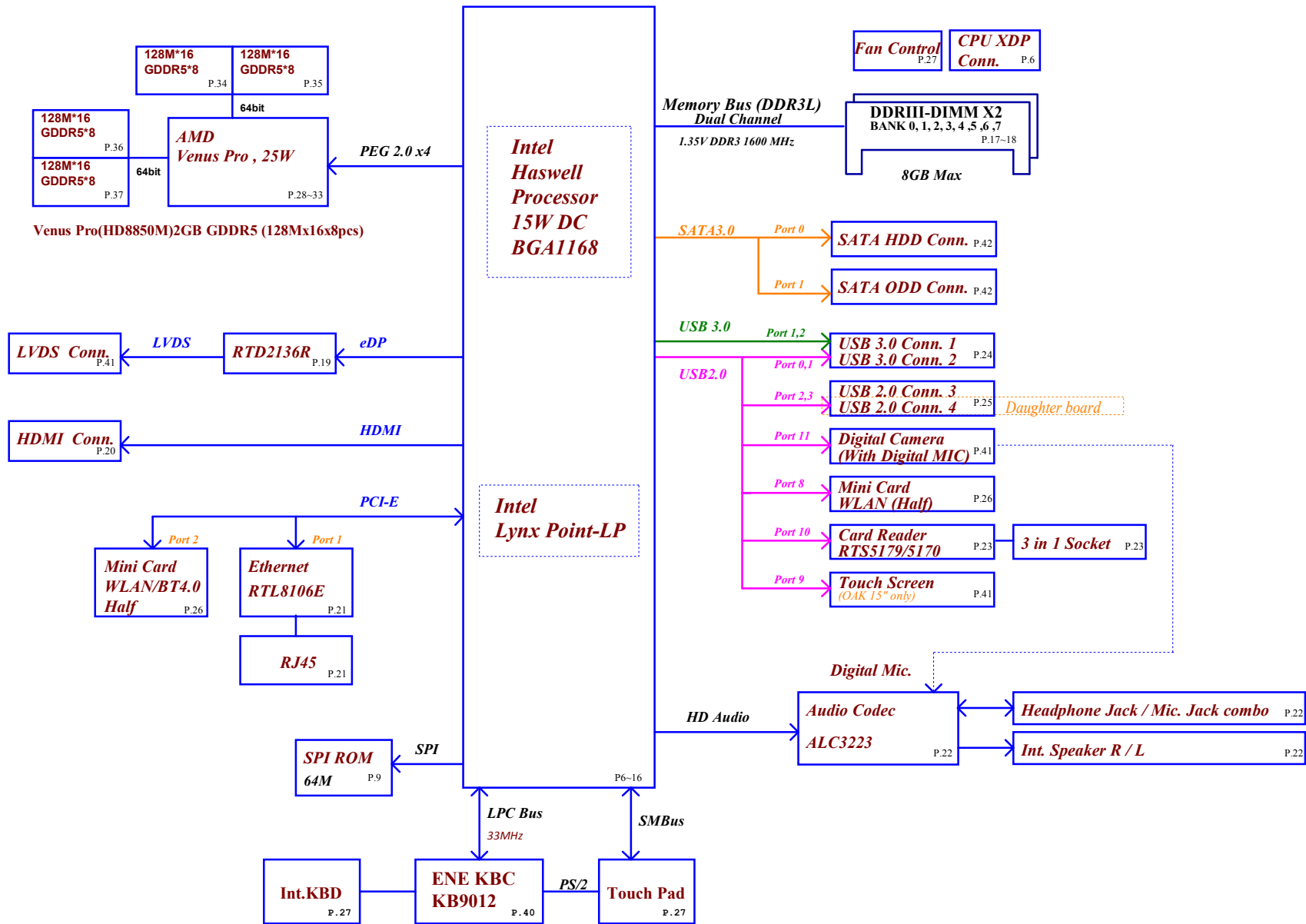
UMA : UMA@,EMI@,ESD@,RF@,XDP@

DIS SUN : SUN@,DIS@,EMI@,ESD@,RF@,XDP@



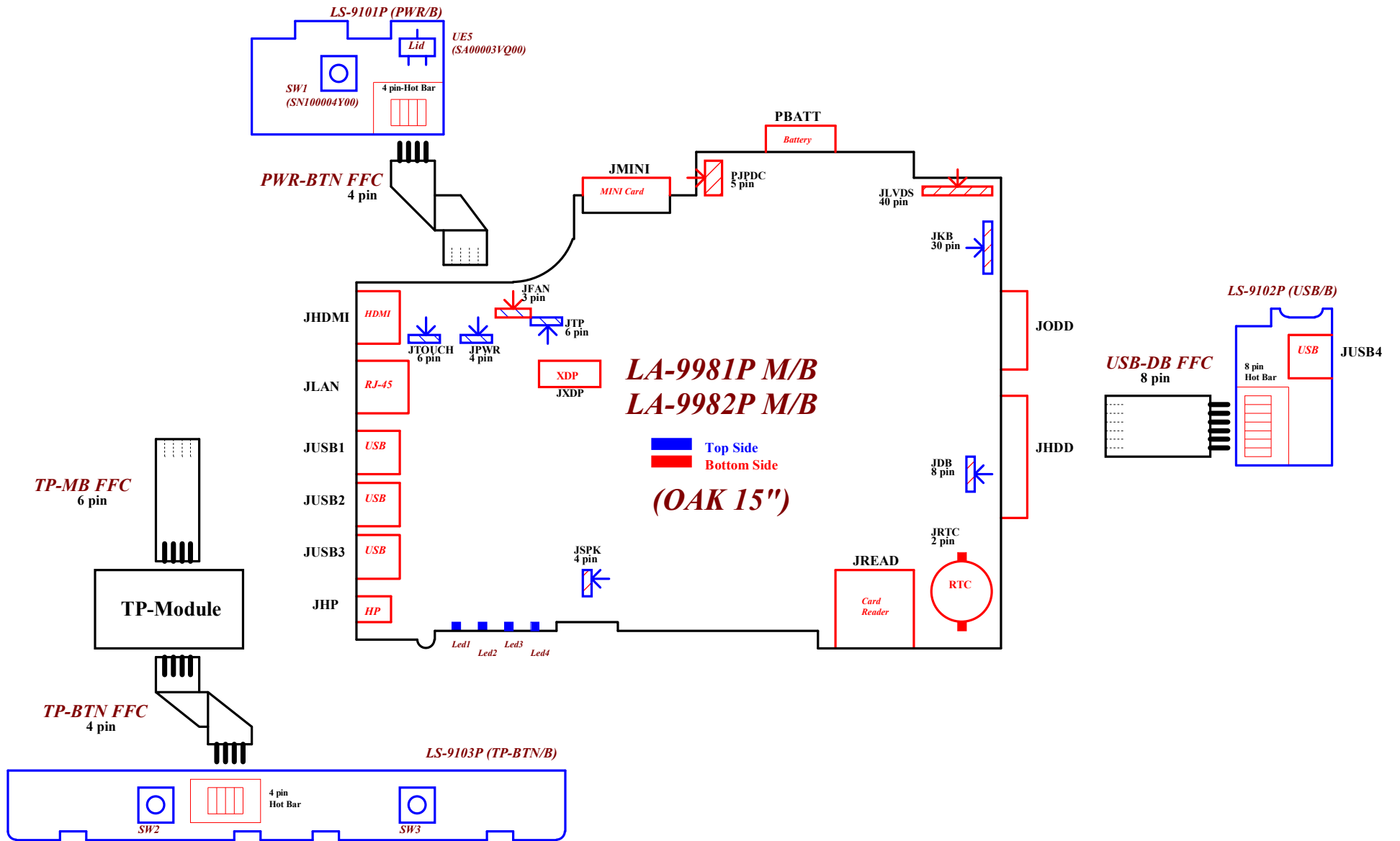
PCB VBW01 LA9981P/LS9101P/LS9102P/LS9103P  
DA8000WK000

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			Sheet 1 of 55	



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Size	Document Number	Rev	0.2	
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**Project Code : VAW00 / VAW01**  
**File Name : LA-9981P / LA-9982P**



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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title <b>DB block diagram</b>		
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**Board ID Table for AD channel**

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

**SMBUS Control Table**

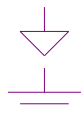
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

**BOARD ID Table**

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0

Symbol Note :



: means Digital Ground



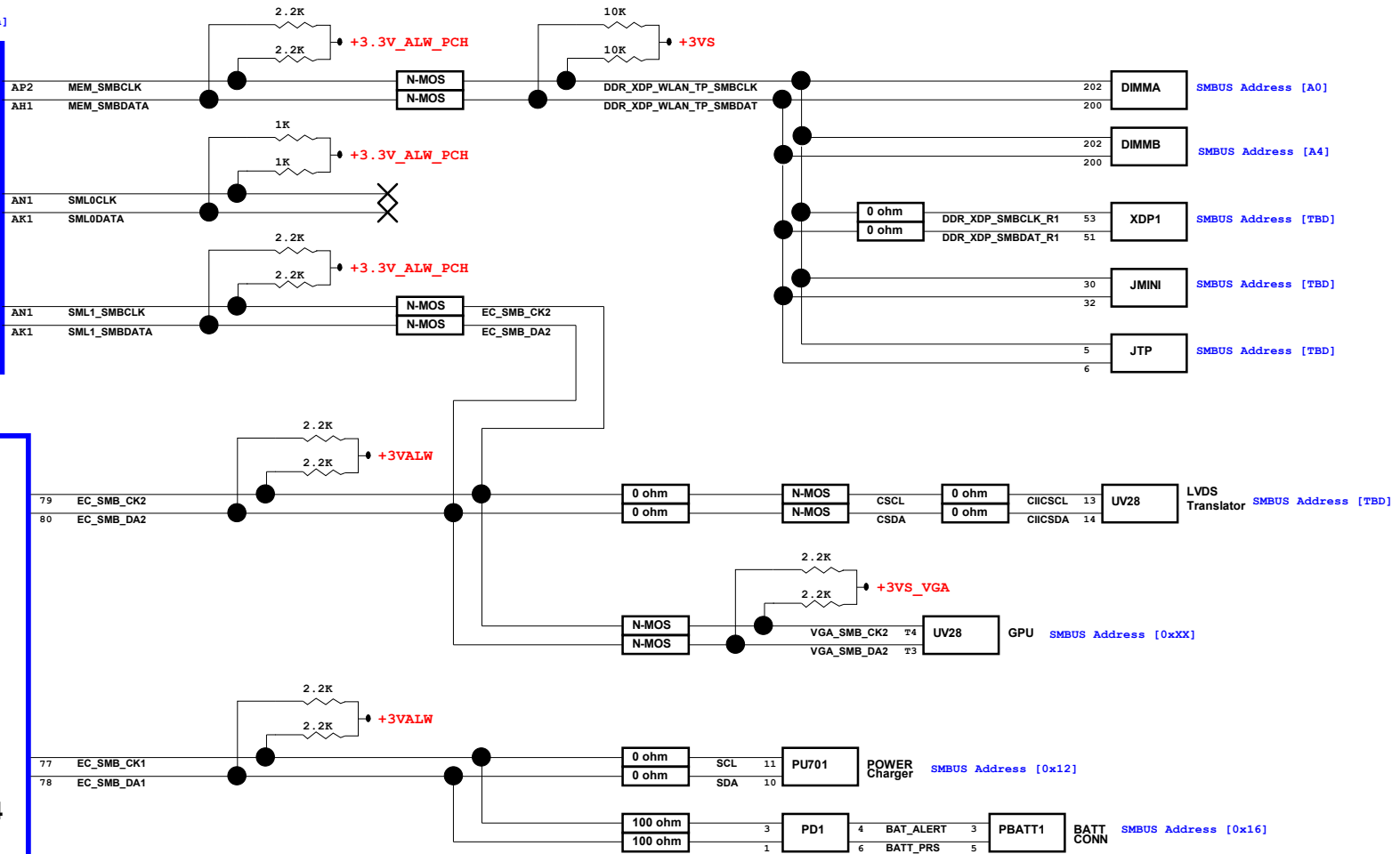
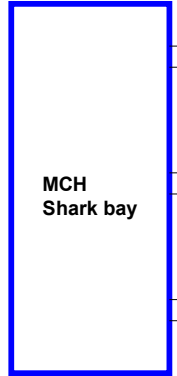
: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU (N14P)
CLKOUT_PCIE5	

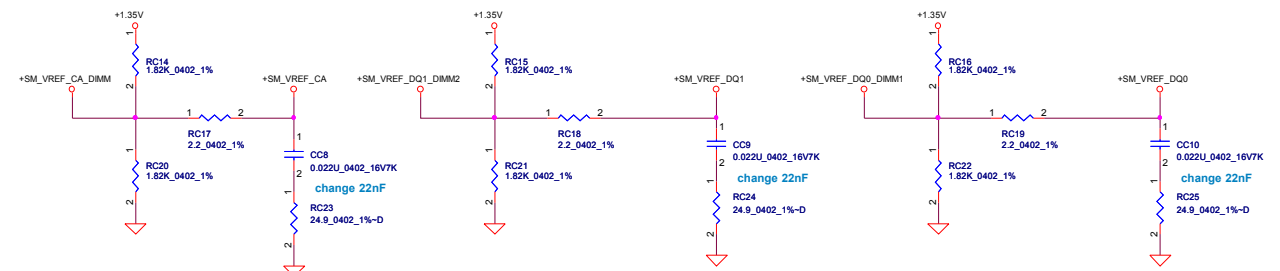
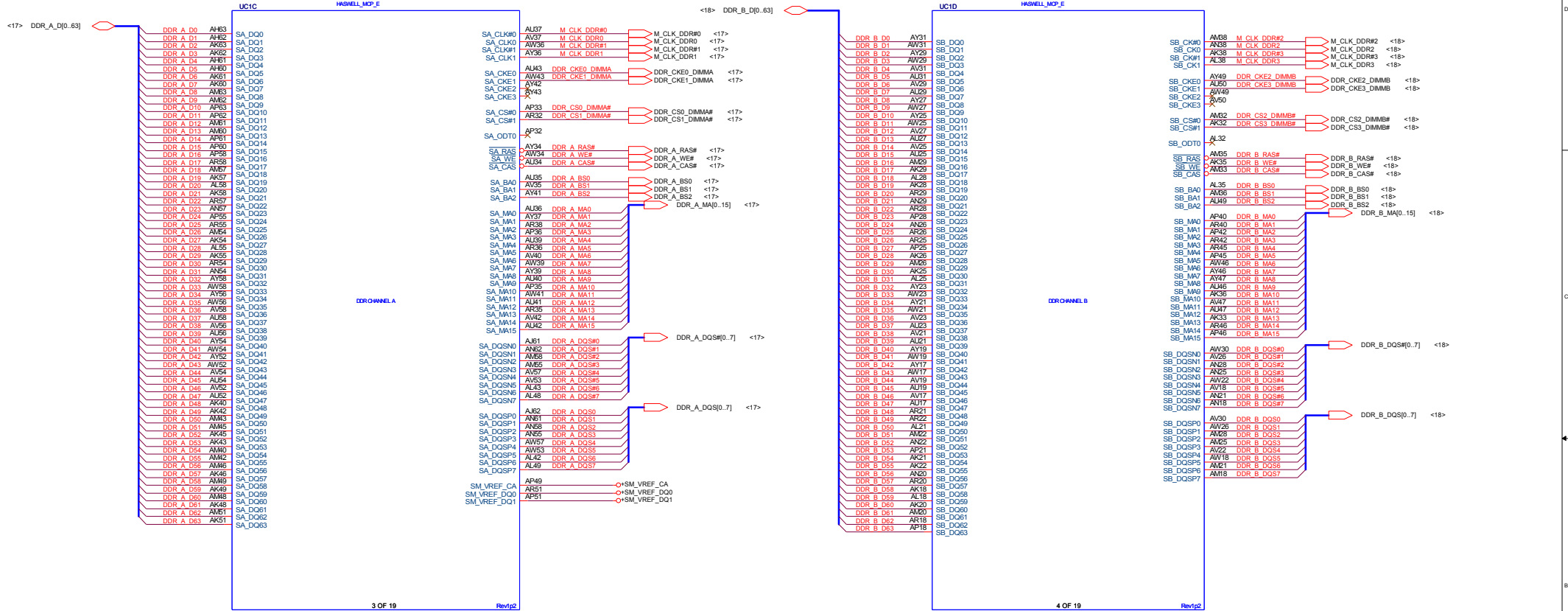
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

ULT

SMBUS Address [0x9a]

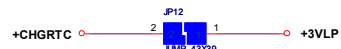
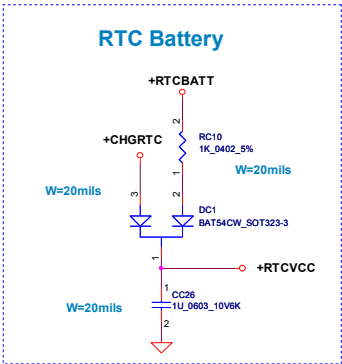




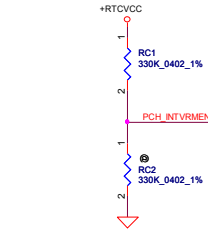


confirm by intel request PDG P141

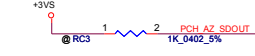
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	<b>MCP(3,4/19) DDR3</b>
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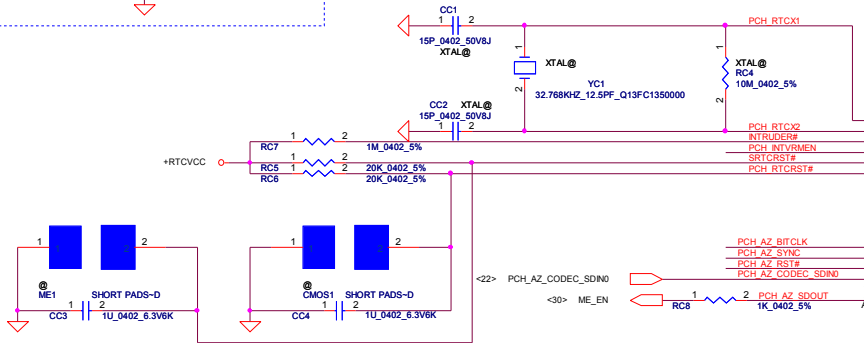
### For GCLK



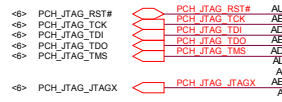
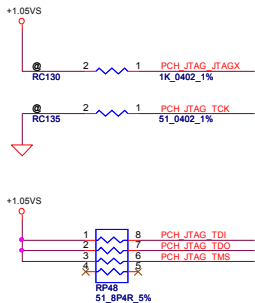
**INTVRMEN - INTEGRATED SUS 1.05V VRM**  
**ENABLE**  
 High - Enable Internal VRs  
 Low - Enable External VRs



**FLASH DESCRIPTOR SECURITY OVERRIDE**  
**LOW = DISABLED (DEFAULT)**  
**HIGH = ENABLED**

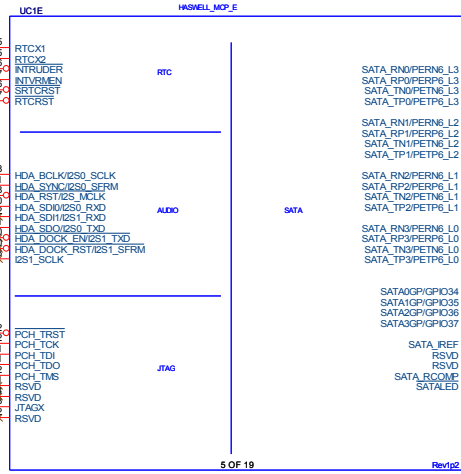


### CMOS place near DIMM



CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

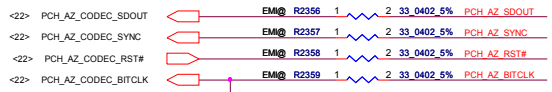
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



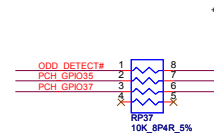
PCH Rx side need use strap pin to update PCIE +/-

**SATA Impedance Compensation**  
 within 500 mils  
 CAD note:  
 Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins. reference FFRD sch 0.5

### HDA for Codec



**EMI depop location**

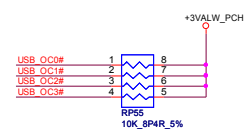
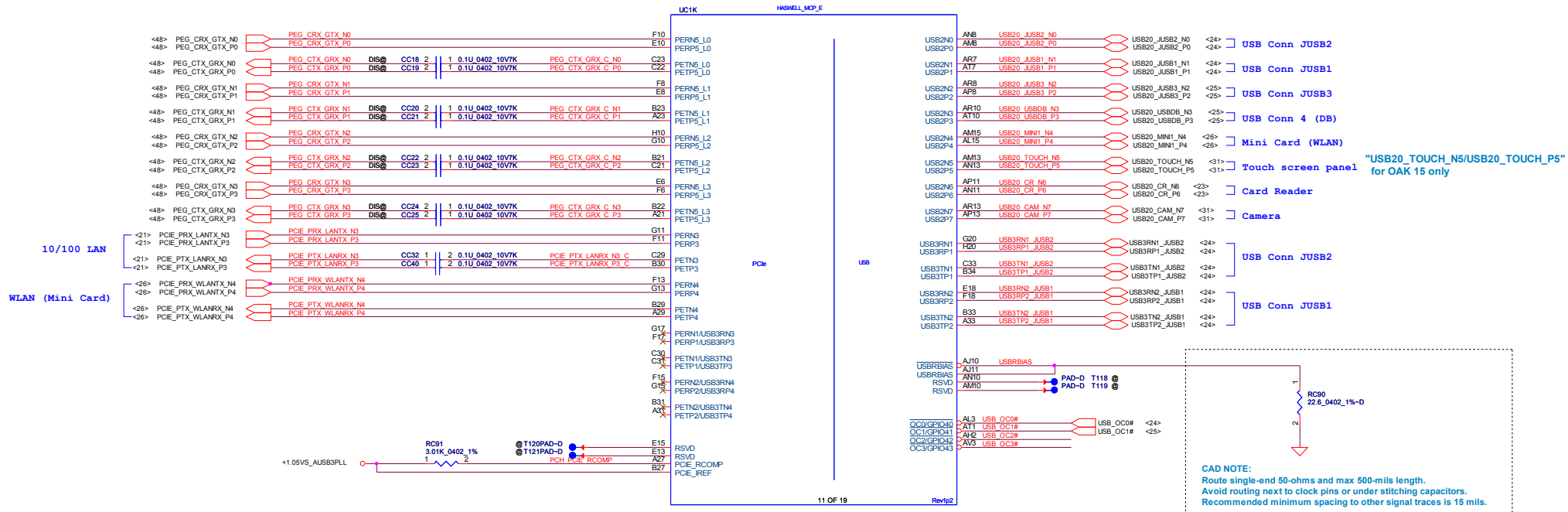




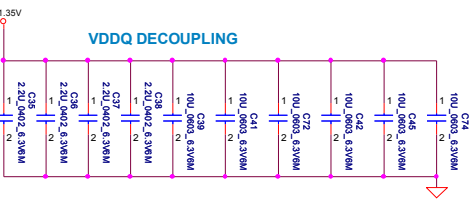
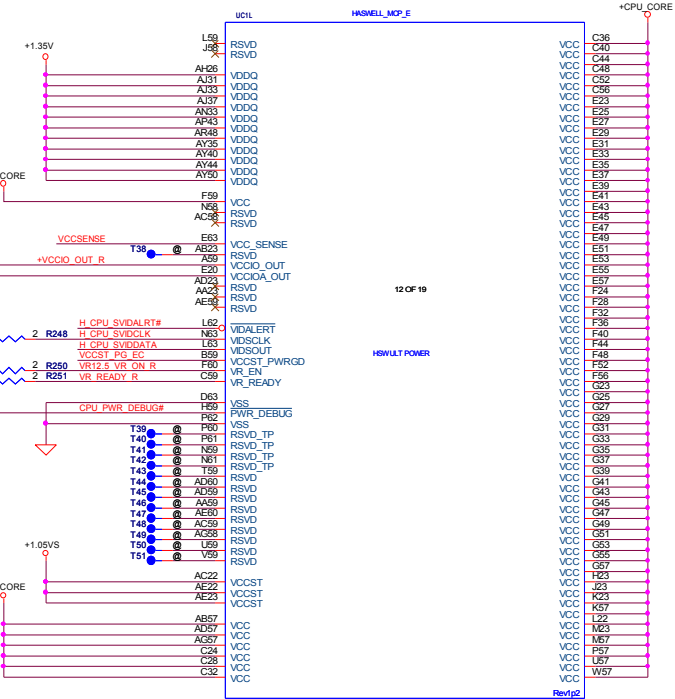
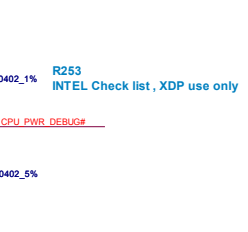
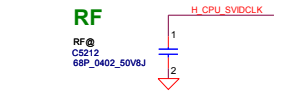
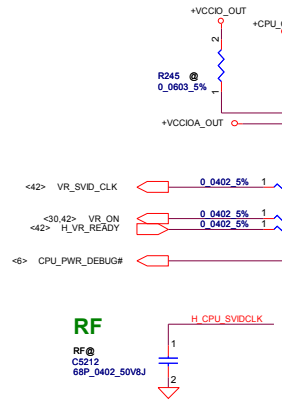
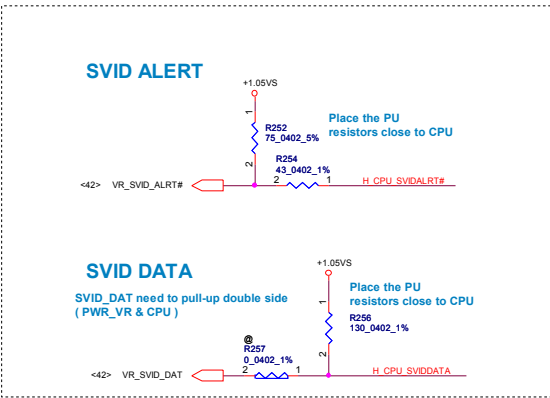
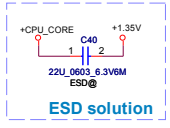
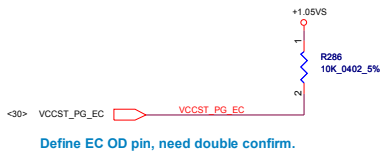




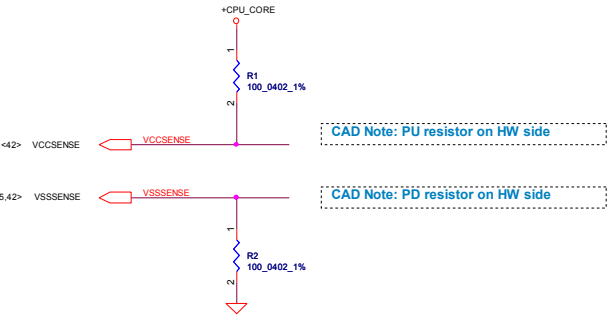




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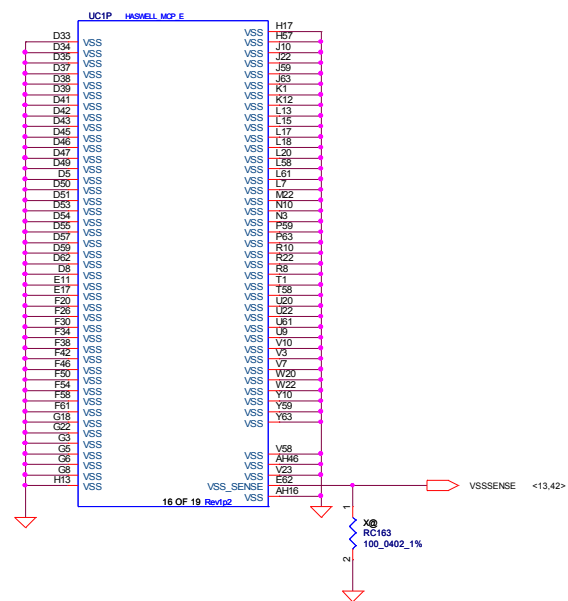
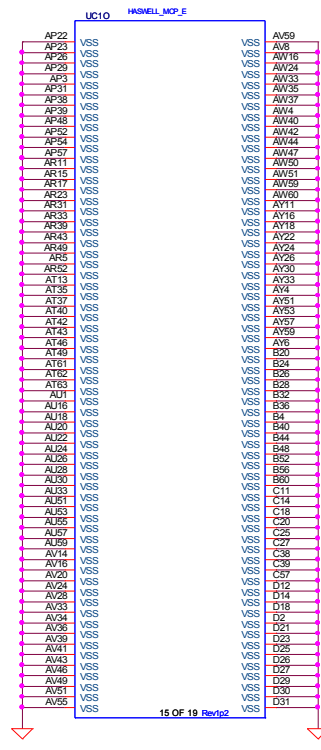
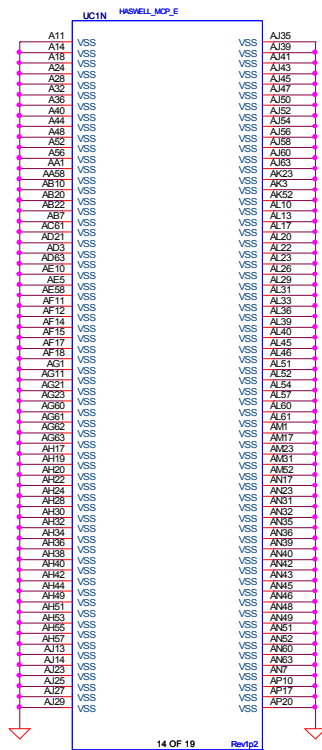


+1.35V : 470UF/2V/7343 \*2 (PWR)  
 10UF/6.3V/0603 \* 6  
 2.2UF/6.3V/0402 \* 4



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CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

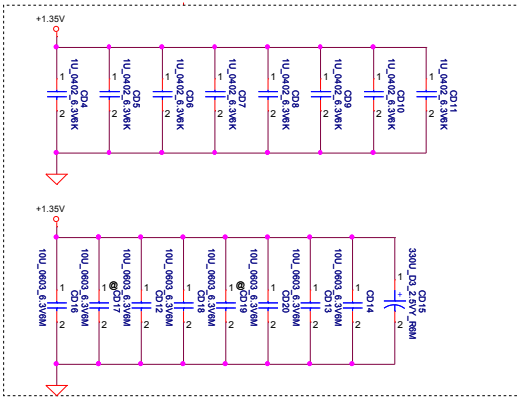
<7> DDR\_A\_DQS[0..7]   
<7> DDR\_A\_DQ[0..63]   
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<7> DDR\_MA[0..15] 

All VREF traces should have 10 mil trace width

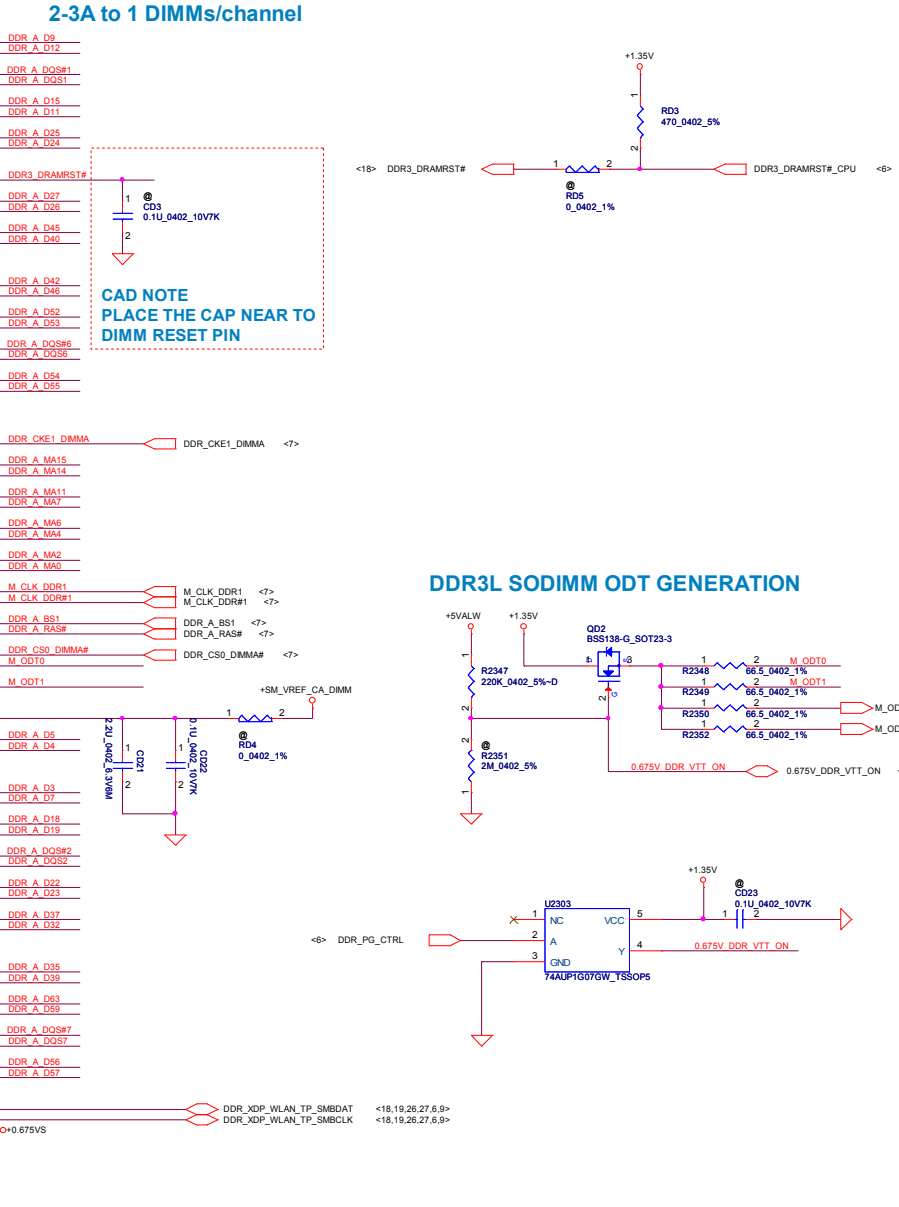
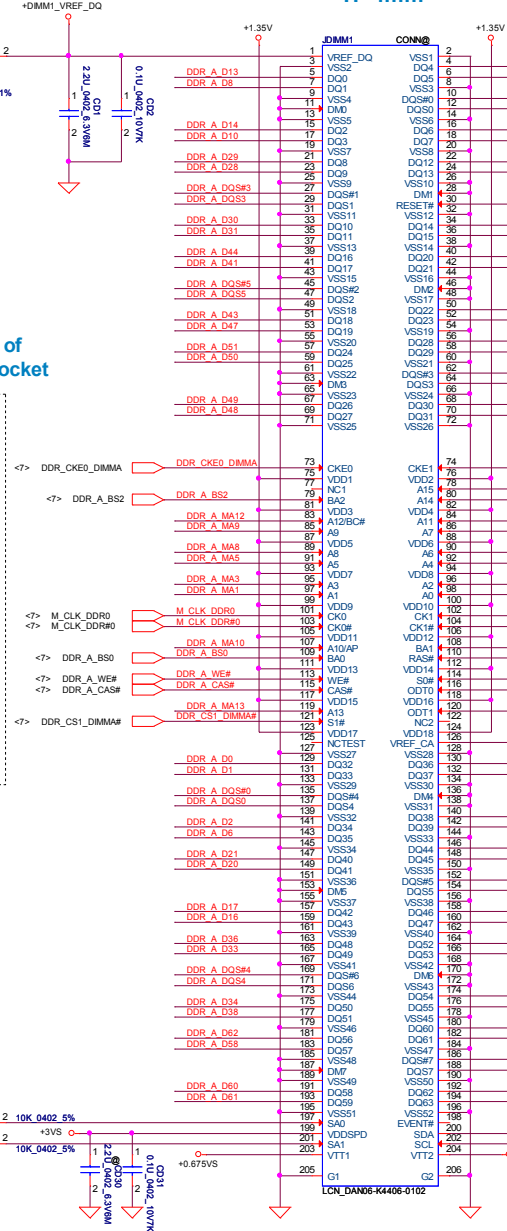
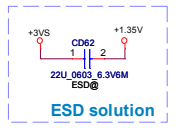
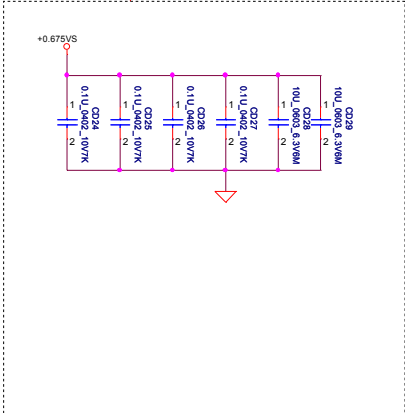
Layout Note:  
Place near JDIMM1

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket

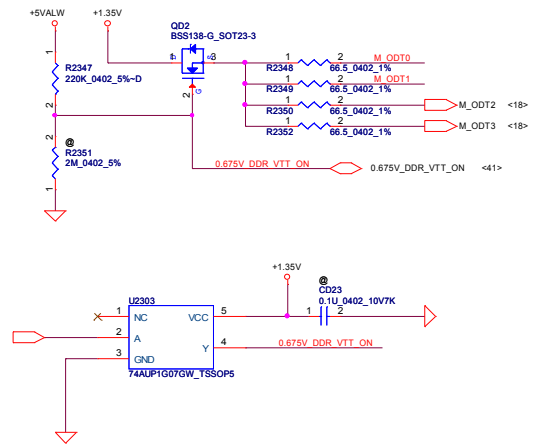
CAD NOTE  
PLACE THE CAP NEAR TO DIMM RESET PIN



Layout Note:  
Place near JDIMM1.203,204

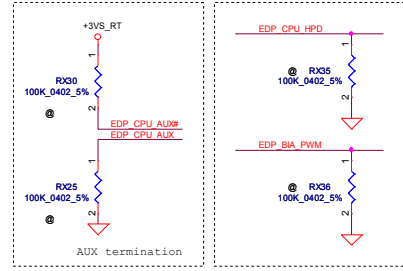
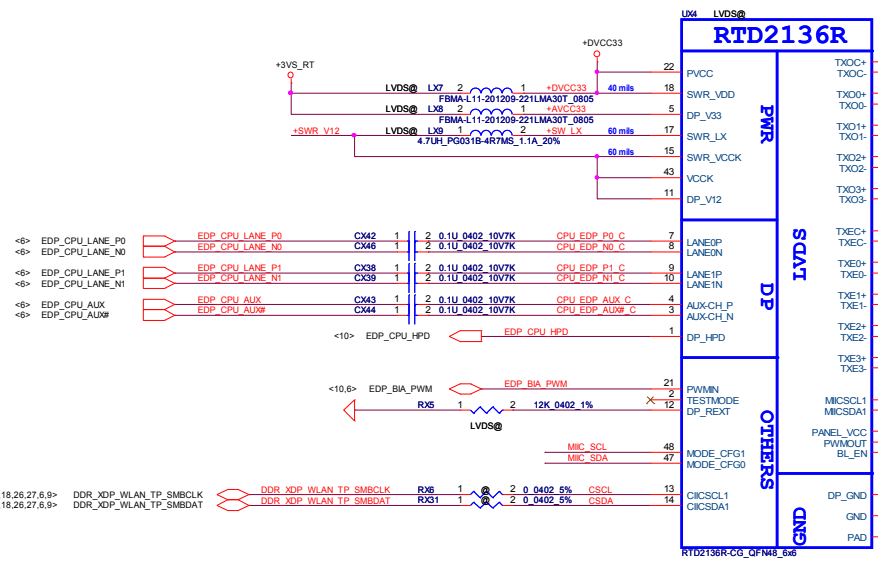
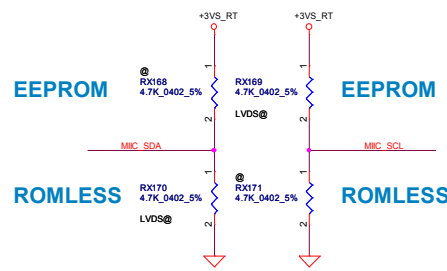
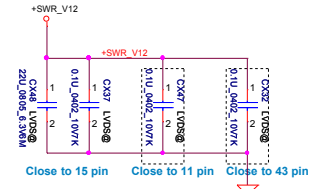
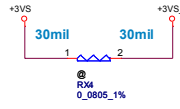
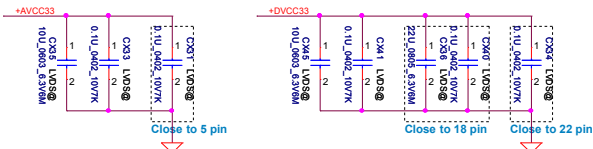


DDR3L SODIMM ODT GENERATION



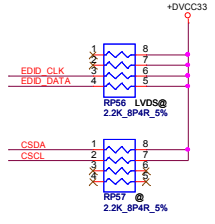
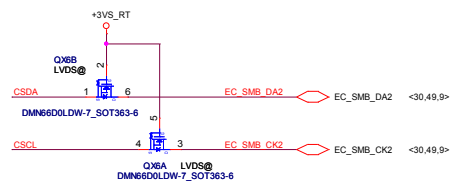
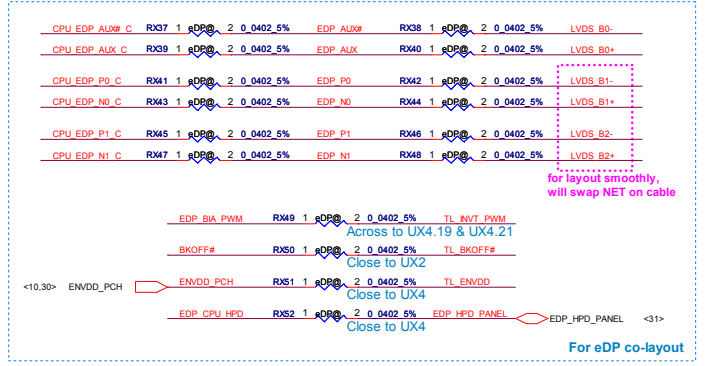
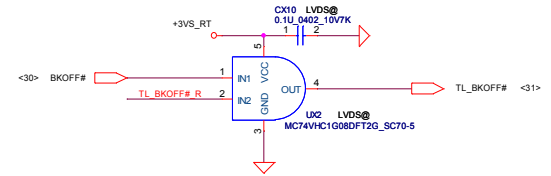
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Document Number				LA-9981P	
Date:				San Jose, March 05, 2013	
Sheet				17 of 55	



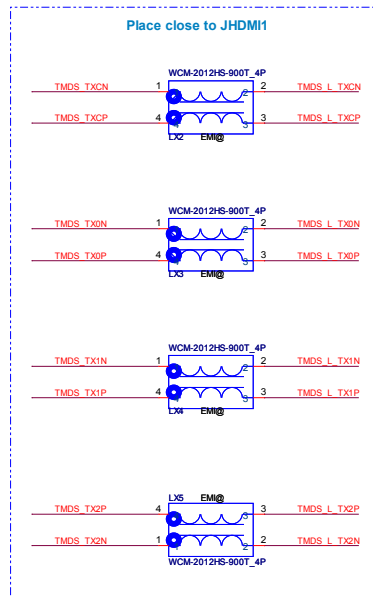
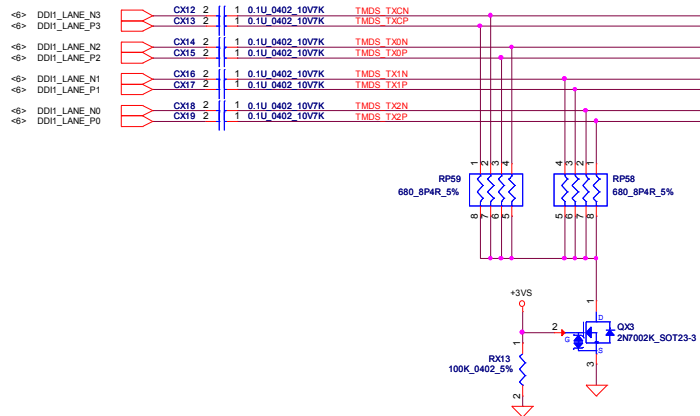


**RTD2136S : SA00004NW10**  
**RTD2136R : SA000067100**

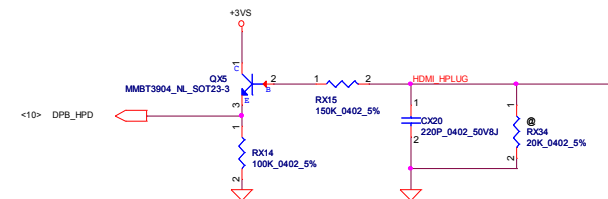
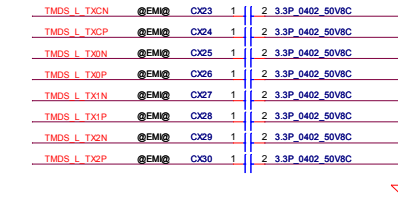
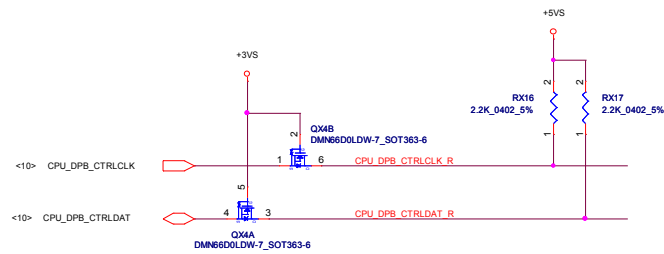
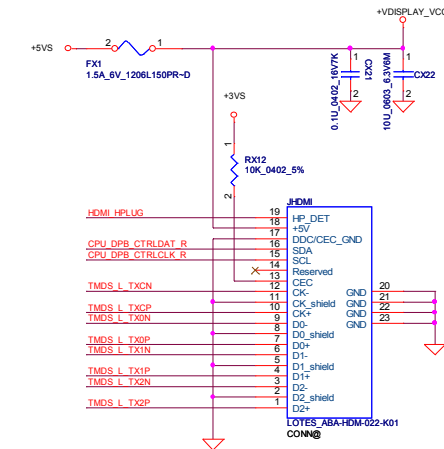
Vendor advise reserve it



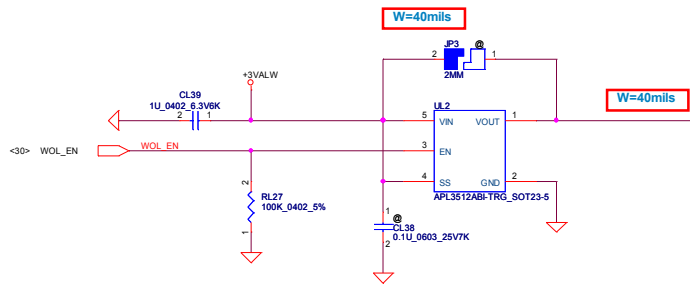
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Issued Date		Deciphered Date		8DP to LVDS converter	
2013/03/09		2014/04/01		8DP to LVDS converter	
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Size	Document Number	Date:		Sheet	Rev
1A.9981P	LA.9981P	San Jose, March 09, 2013		19	0.2
				of	55



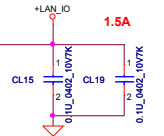
W=40mils



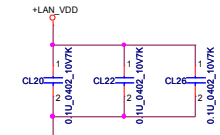
Security Classification	Compal Secret Data		Title			
Issued Date	2013/03/09	Deciphered Date	2014/04/01	HDMI		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
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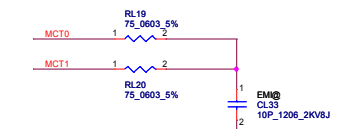
W=40mils +LAN\_IO rising time : >1ms and <100ms



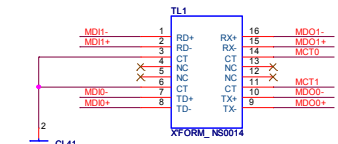
These caps close to Pin 23,32 For 8106E pop the capacitor close pin 23,32



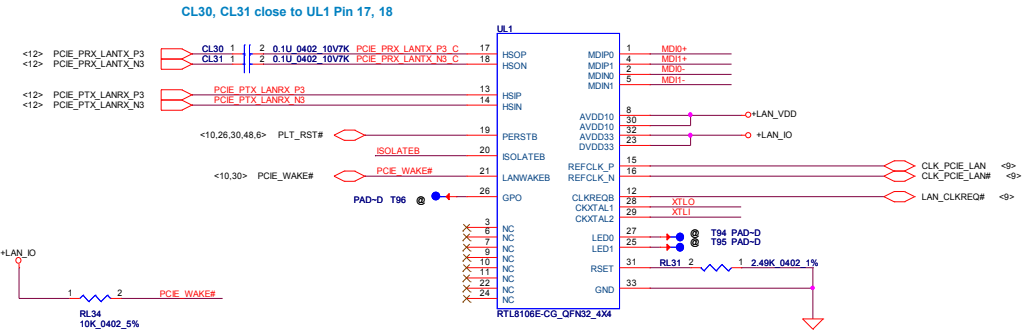
These caps close to Pin 8,30 For 8106E pop capacitor close to pin 8,30



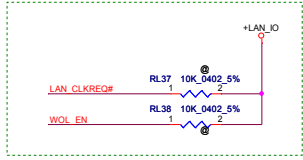
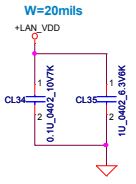
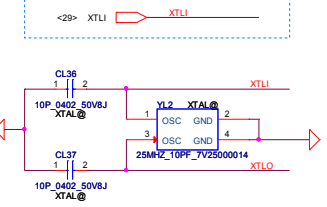
Place close to TCT pin



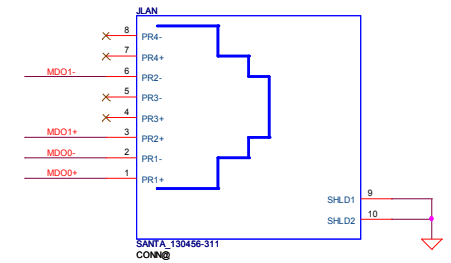
Change CPN to SP050007J00 only Need CIS symbol



For GCLK



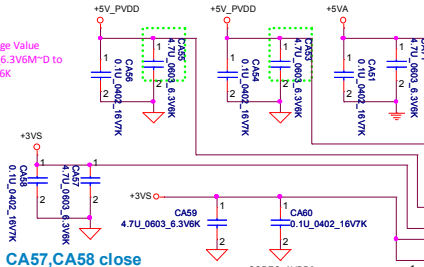
Reserve 10K pull LAN\_IO



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				10P_0402_50V8J	LA-9981P	0.2
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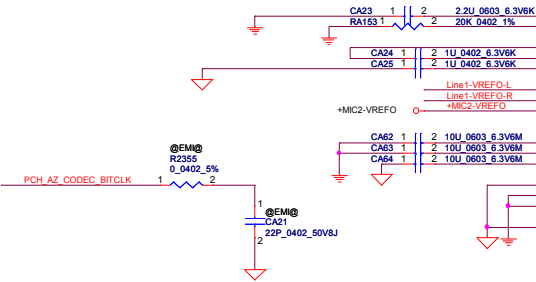
**CA71, CA51 place close to Pin 26**

CA53, CA55 change Value from 10U\_0603\_6.3V6K to 4.7U\_0603\_6.3V6K

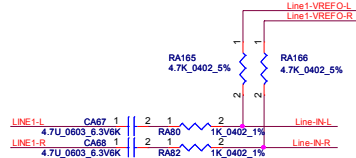
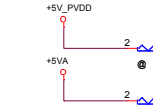


**CA57, CA58 close to UA1 pin1**

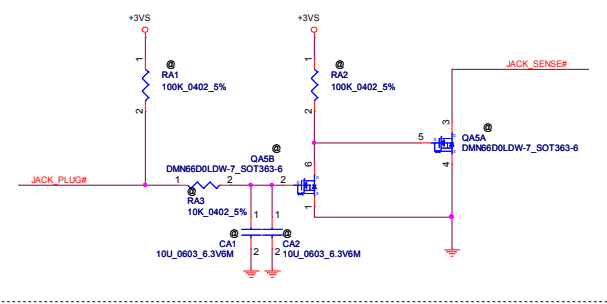
- <8> PCH\_AZ\_CODEC\_SDIND
- <8> PCH\_AZ\_CODEC\_SDOOUT
- <8> PCH\_AZ\_CODEC\_BITCLK
- <8> PCH\_AZ\_CODEC\_SYNC
- <8> PCH\_AZ\_CODEC\_RST#



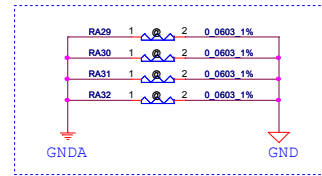
**Reserve for HDA issue**



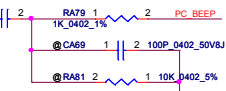
**JACK\_PLUG Delay circuitis**



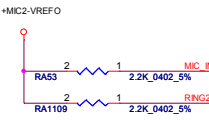
**Reserve for cancel Delay circuitis**



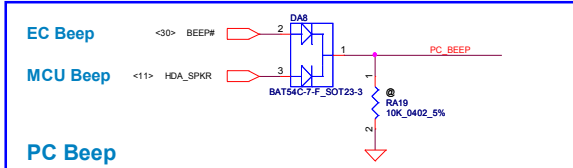
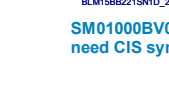
Place on the moat between GND & GNDA.



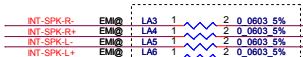
**RA51, RA33 place close to UA1**



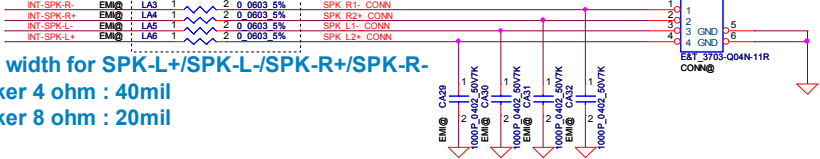
**SM1000BV00 need CIS symbol**



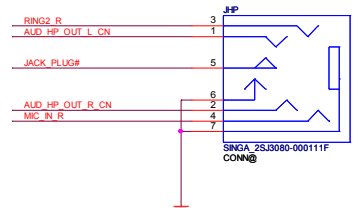
**Close to UA1 Pin11,13,14,16**



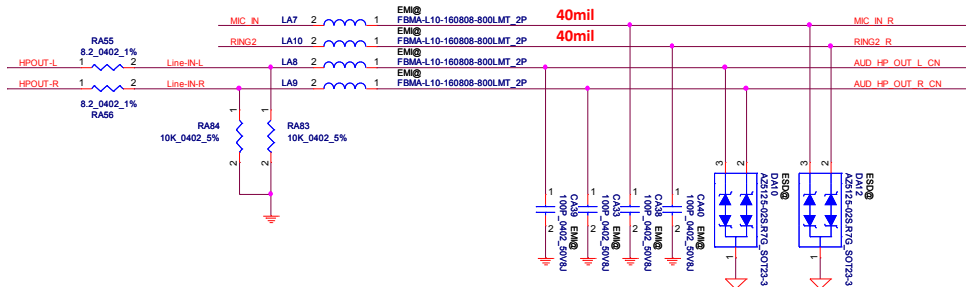
**close to Codec**



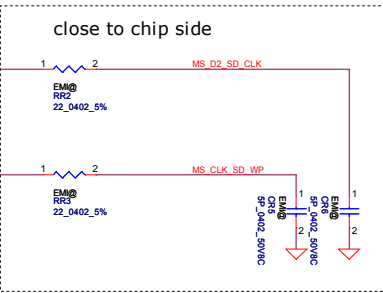
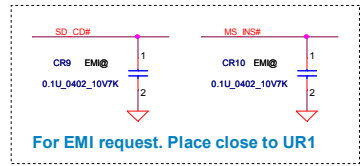
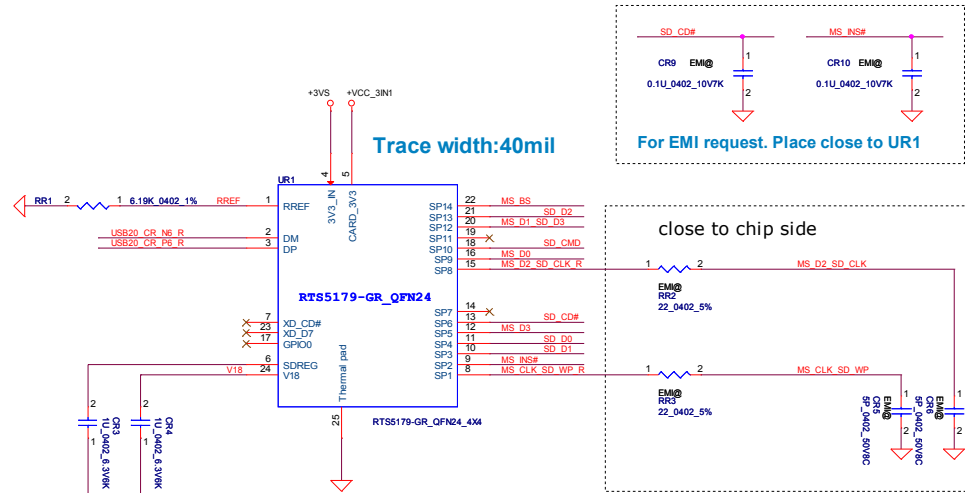
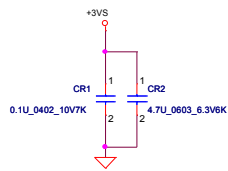
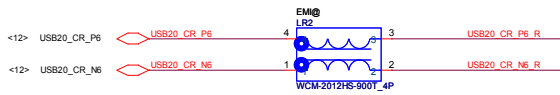
**Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R- Speaker 4 ohm : 40mil Speaker 8 ohm : 20mil**



**iPhone and Nokia type Combo Jack**

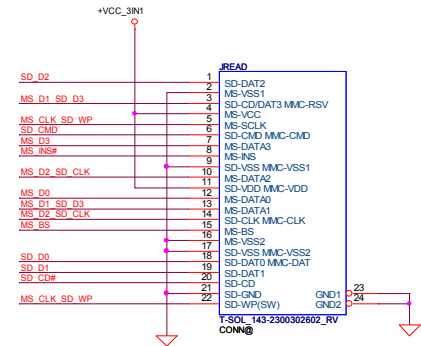
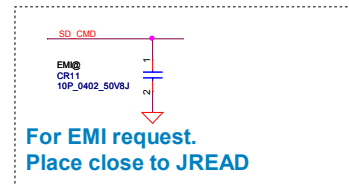
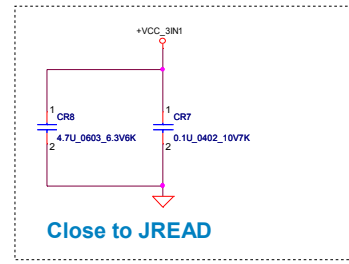


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				Date:	Sheet 22 of 55

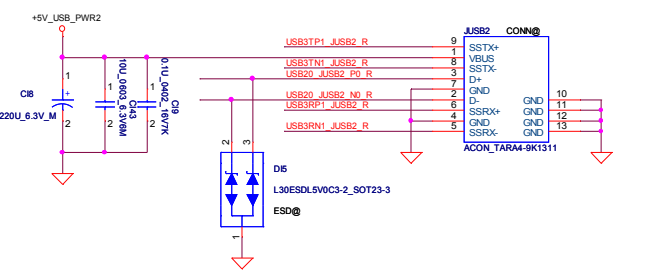
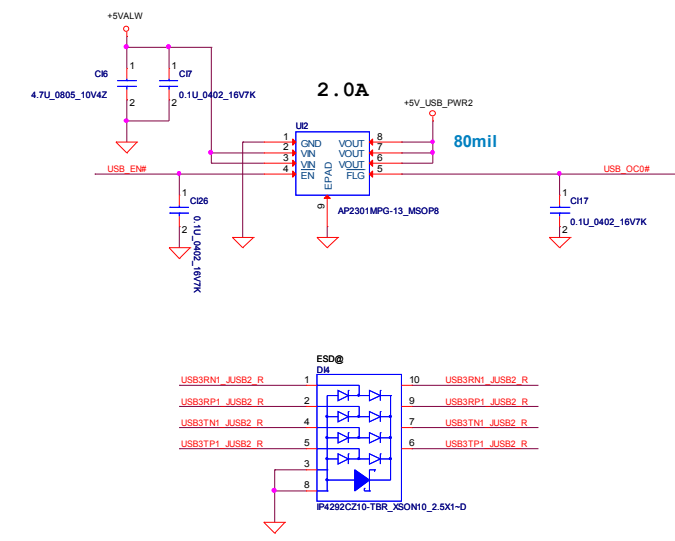
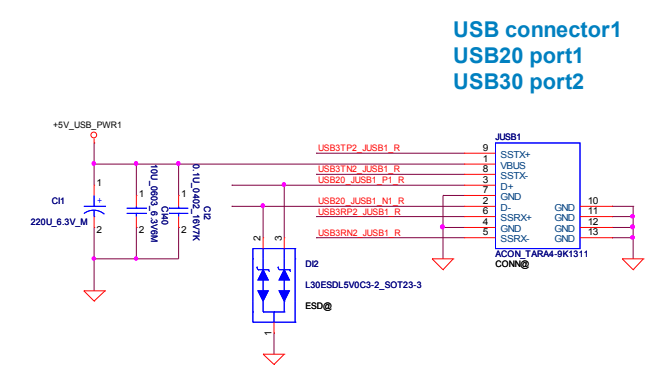
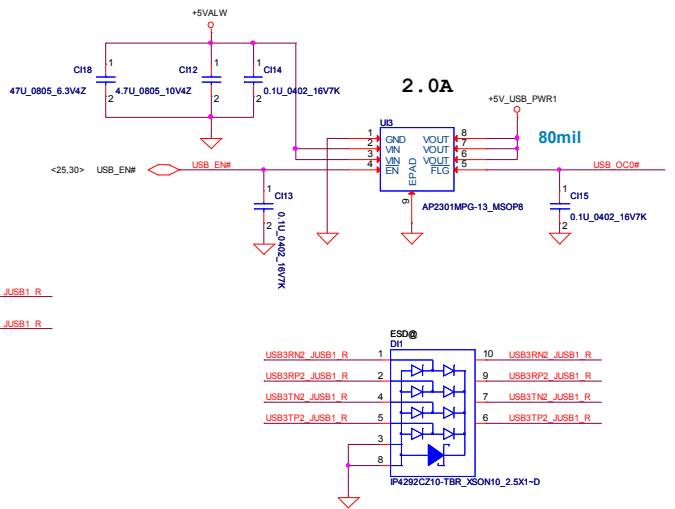


拉MS\_D2\_SD\_CLK到Conn pin 13 SD\_CLK  
再打Via拉到pin 10 MS\_D2

拉MS\_CLK\_SD\_WP到Conn pin 5 MS\_CLK  
再打Via拉到pin 20 SD\_W

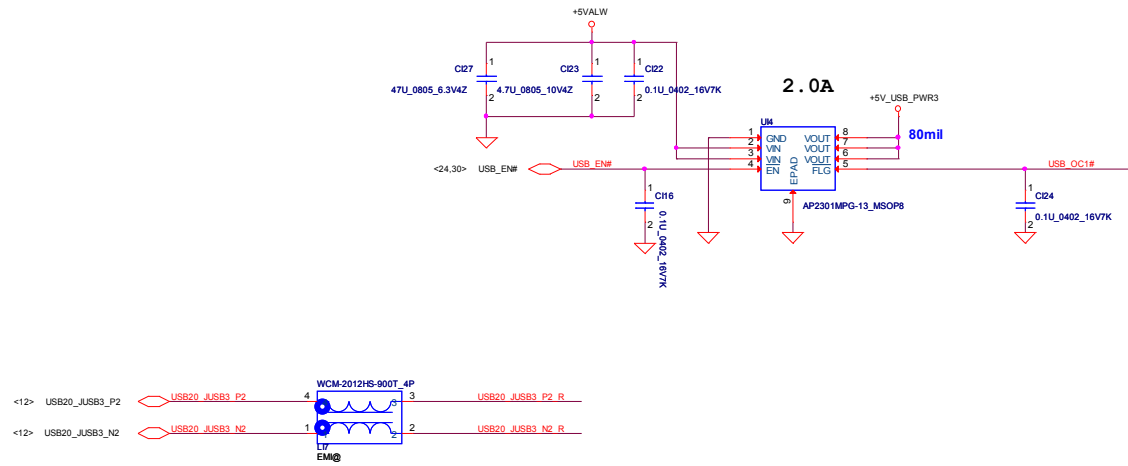


Security Classification	Compal Secret Data		Title	
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Date: Saturday, March 09, 2013				Sheet 23 of 55

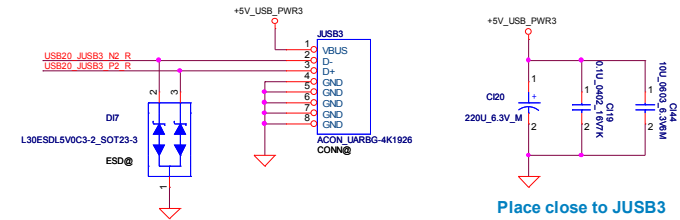


Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	USB3.0	
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				LA9981P	Rev 0.2
				Date: Saturday, March 09, 2013	Sheet 24 of 55

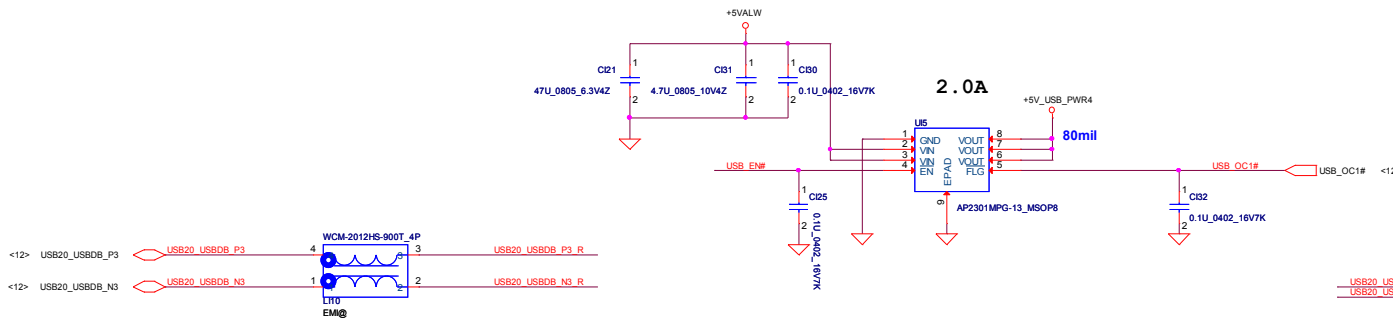




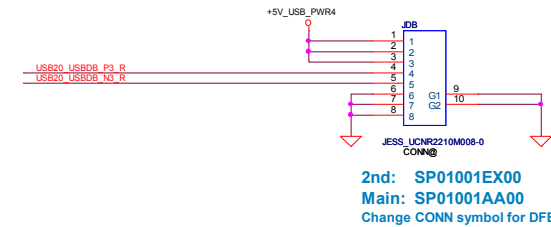
USB connector3  
USB20 port2



Place close to JUSB3



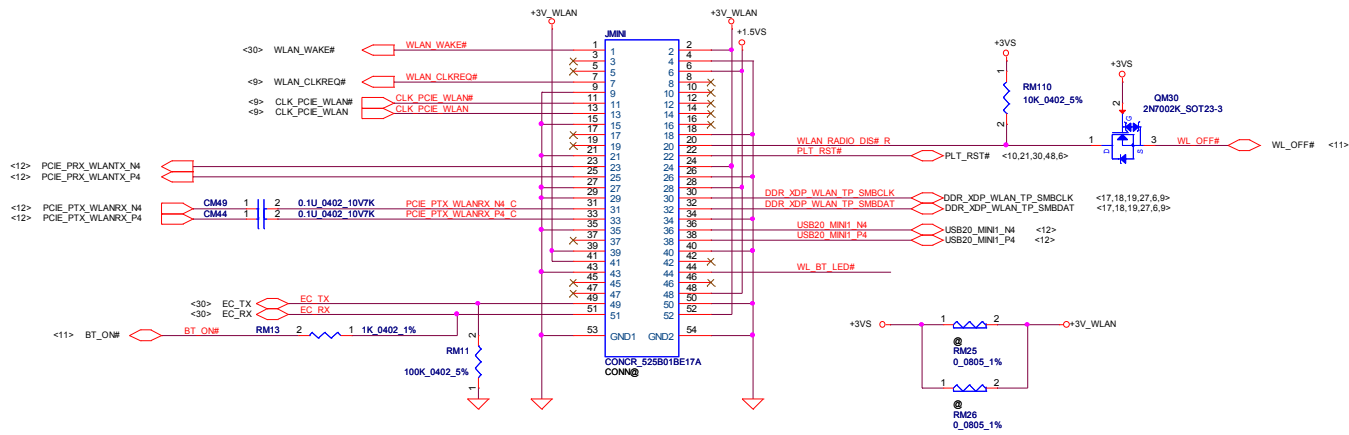
USB connector4  
USB20 port3



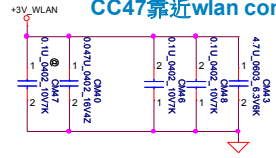
2nd: SP01001EX00  
Main: SP01001AA00  
Change CONN symbol for DFB

Security Classification	Compal Secret Data		Title		<b>Compal Electronics, Inc.</b>	
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					<b>LA-9981P</b>	0.2
				Date:	Saratov, March 09, 2013	Sheet 25 of 55

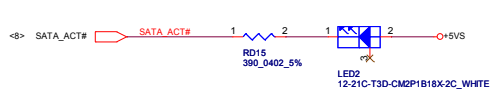
### Mini WLAN/WIMAX H=6.7



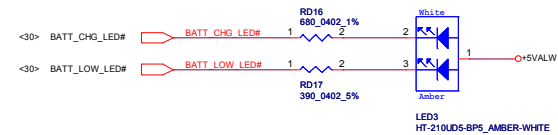
### CC47靠近wlan connector



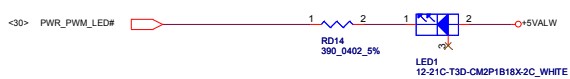
### HDD LED



### Battery LED

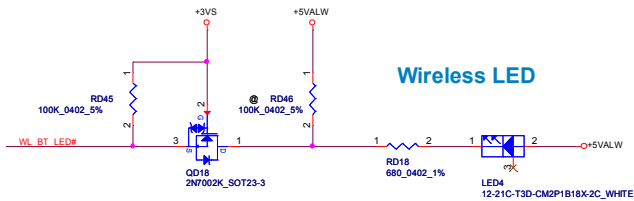


### Power LED



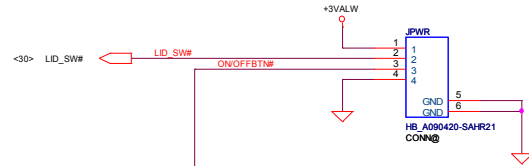
### 10mils, All pins

### Wireless LED



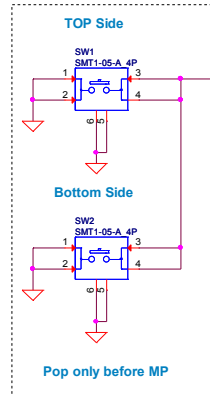
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2014/04/01	
2013/03/09		2014/04/01		Mini Card/LED	
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Size	Document Number	Date:		Rev	0.2
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### POWER/B

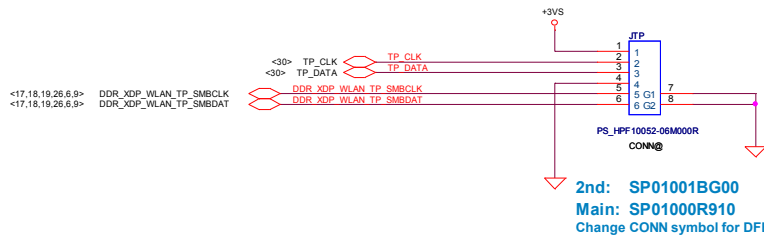


### Power ON Circuit

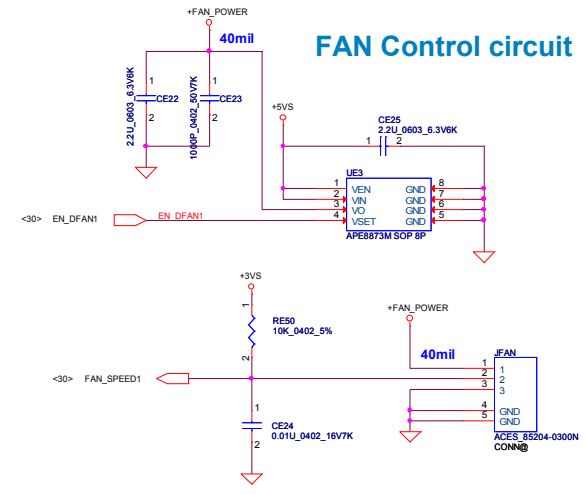
#### ON/OFF switch



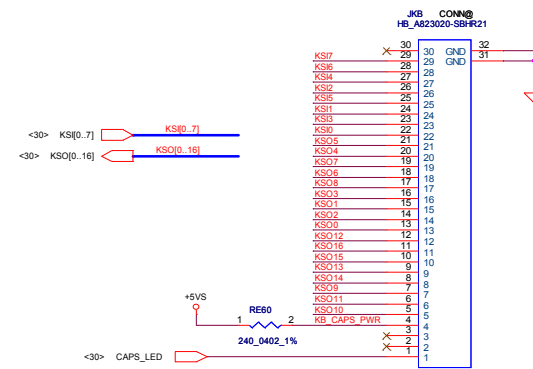
### Touch pad



### FAN Control circuit

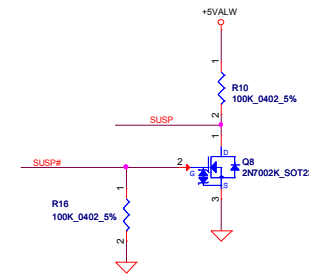
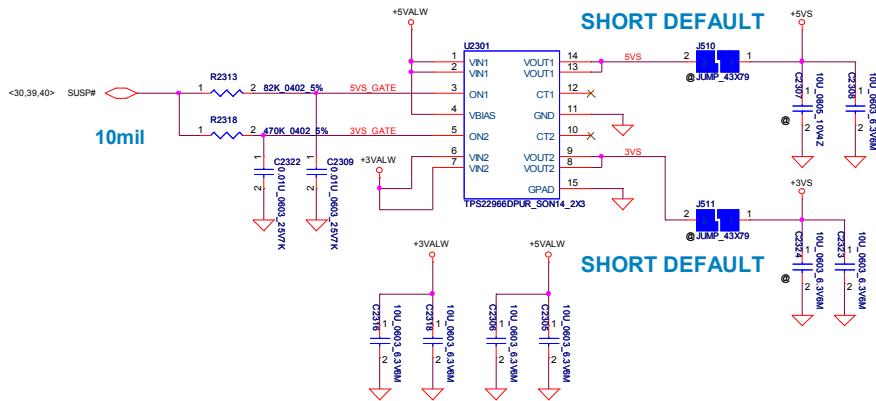


### INT\_KBD Connector

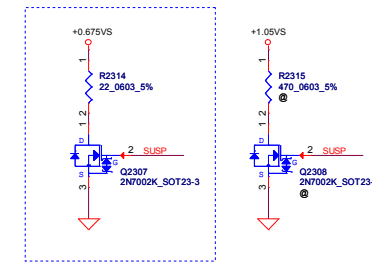
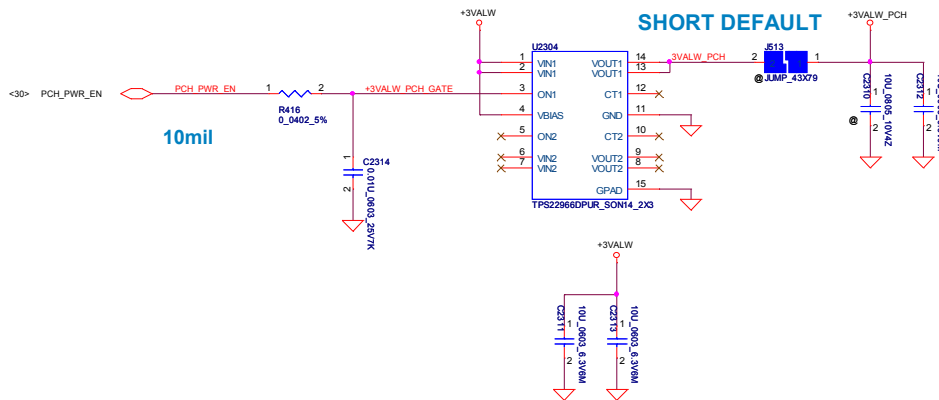


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## +5VS and +3VS switch

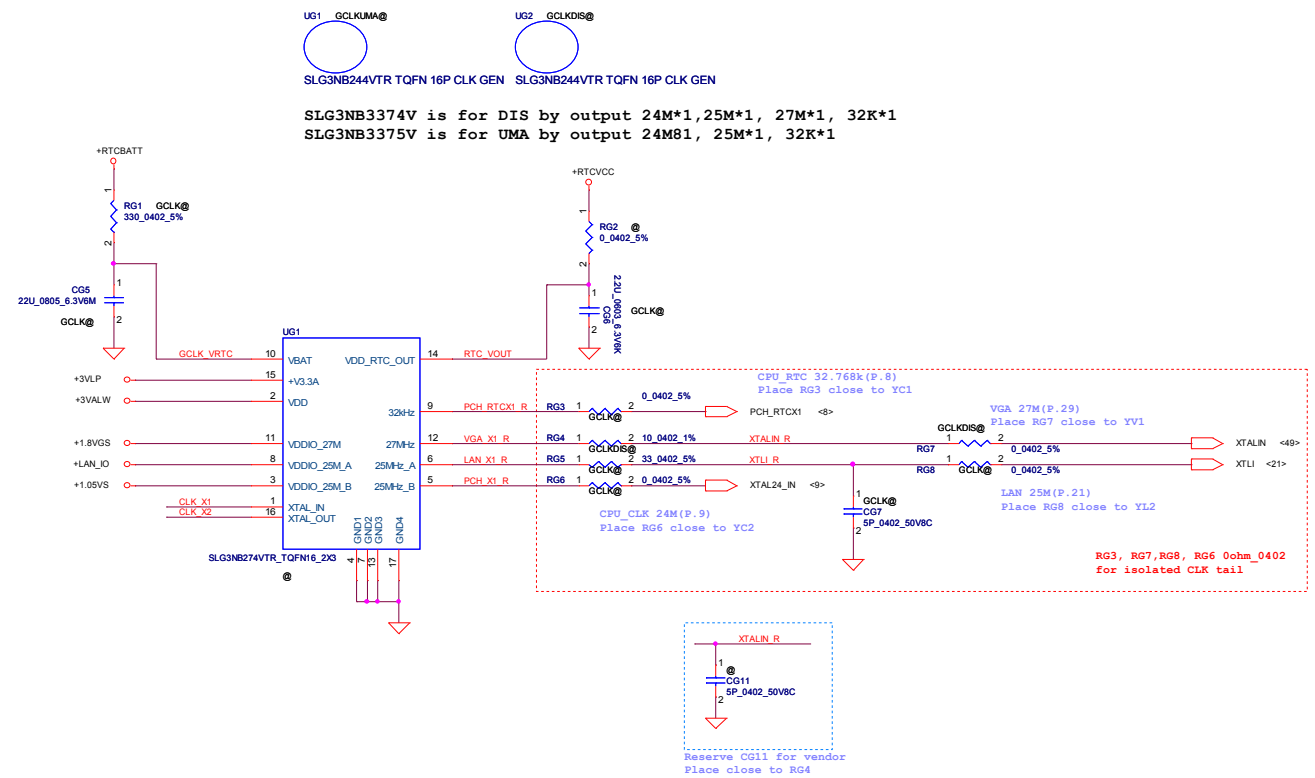
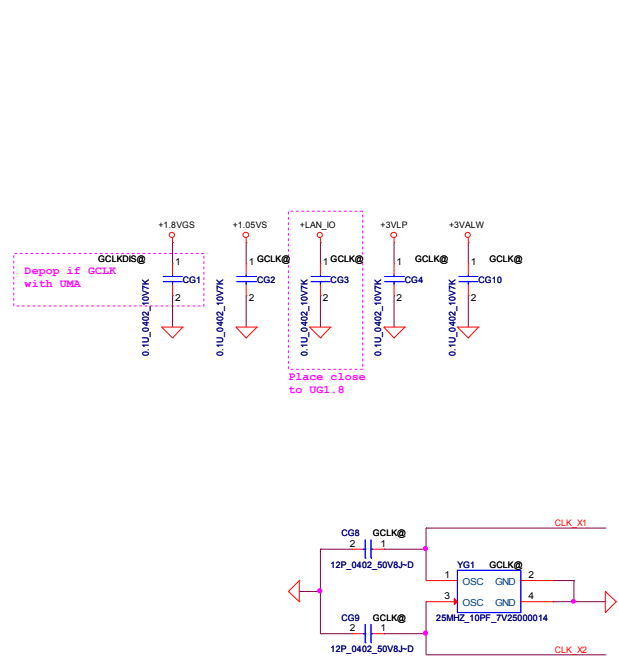


## +3VALW\_PCH switch



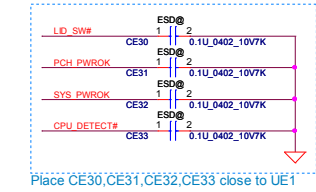
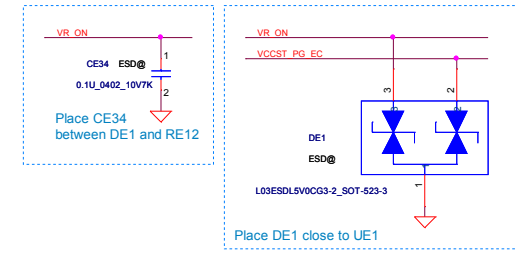
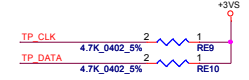
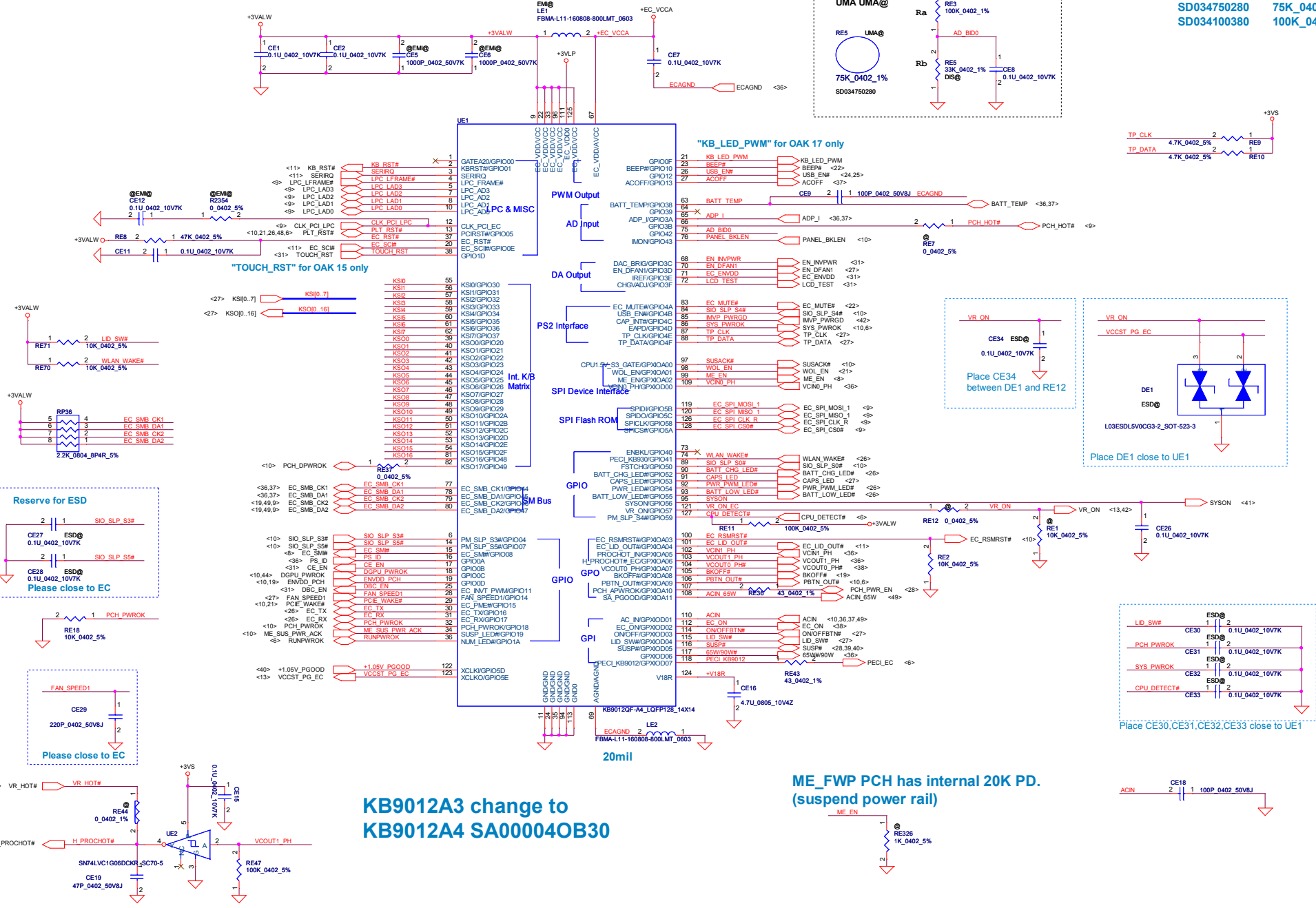
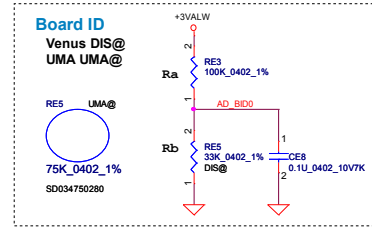
For Intel S3 Power Reduction

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Issued Date	2013/03/09	Deciphered Date	2014/04/01	GCLK	
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				LA-9981P	Rev 0.2
				Date: Saturday, March 09, 2013	Sheet 23 of 55

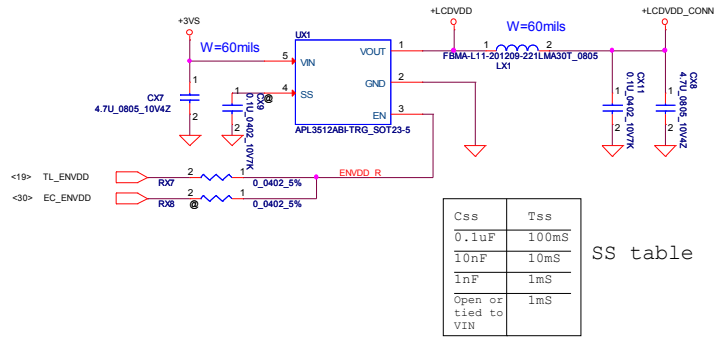
- SD034120280 12K\_0402\_1%
- SD034100300 27K\_0402\_1%
- SD034430280 33K\_0402\_1%
- SD034430280 43K\_0402\_1%
- SD034560280 56K\_0402\_1%
- SD034750280 75K\_0402\_1%
- SD034100380 100K\_0402\_1%



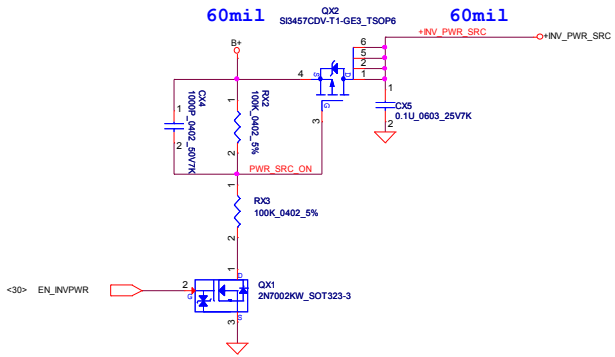
**ME\_FWP PCH has internal 20K PD. (suspend power rail)**

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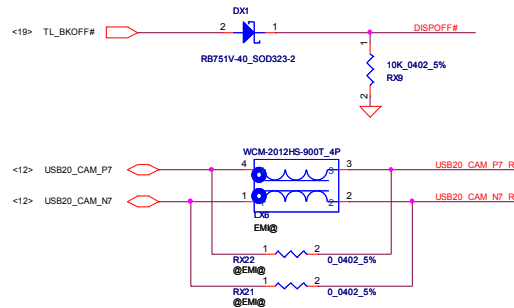
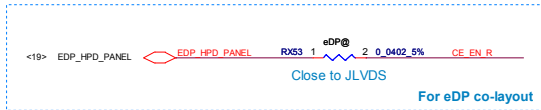
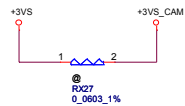
### LCD PWR CTRL



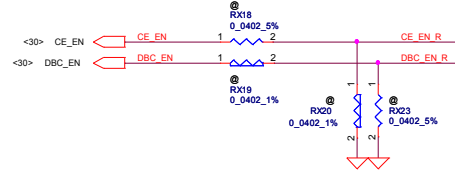
### LCD backlight PWR CTRL



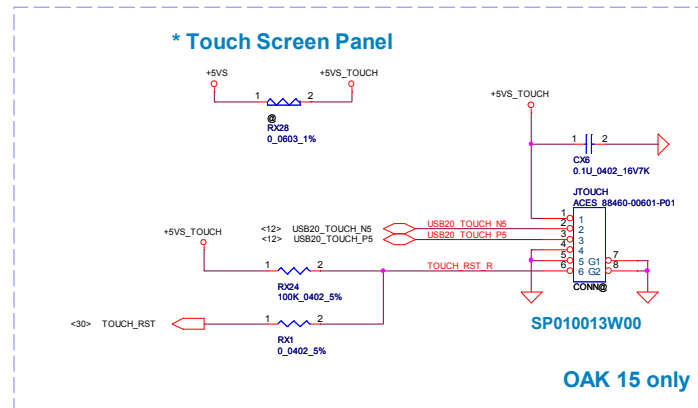
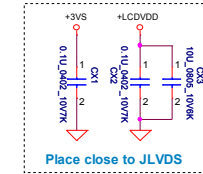
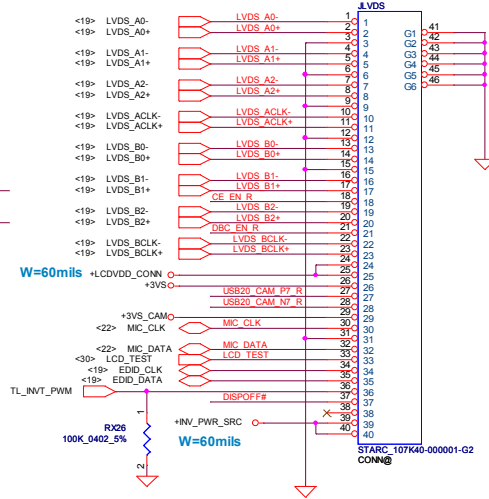
### Webcam PWR CTRL



CE\_EN\_R only for reserve.

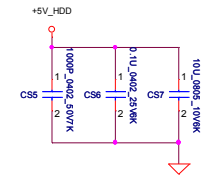
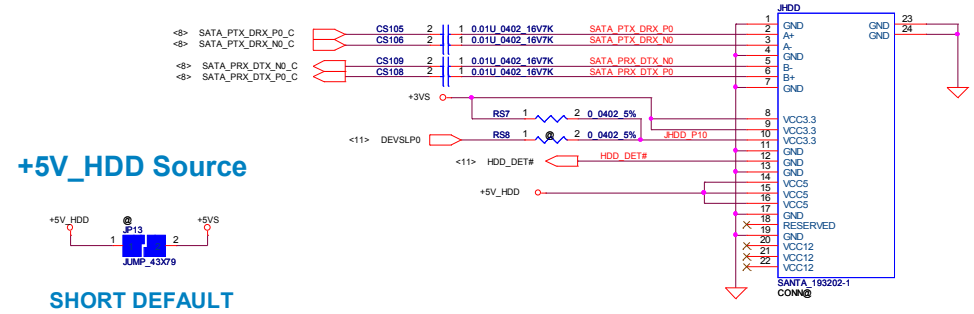


### LVDS Connector

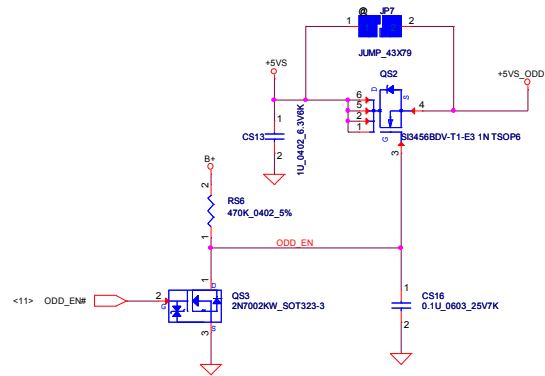


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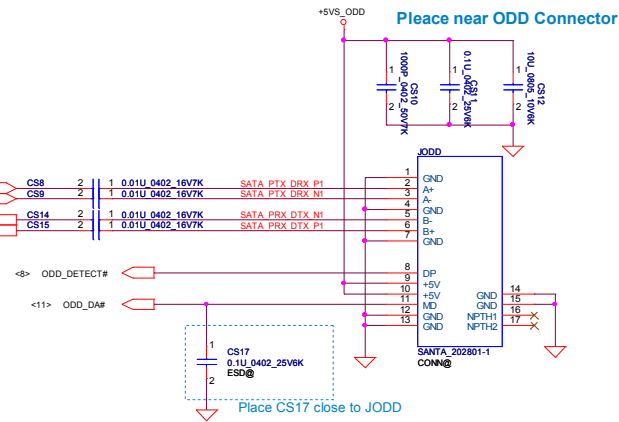
## SATA HDD Connector



## ODD Power Control



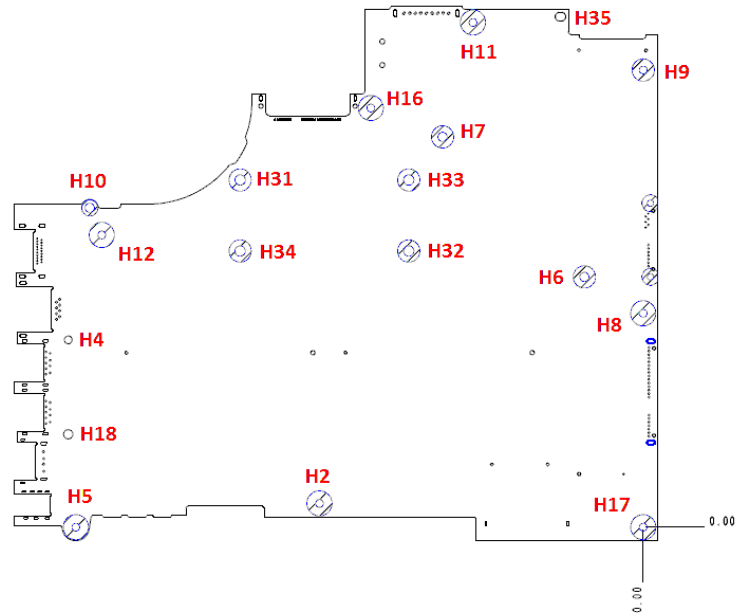
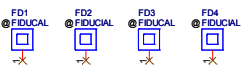
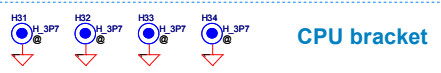
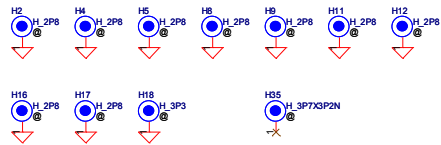
## SATA ODD Connector



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## Screw Hole

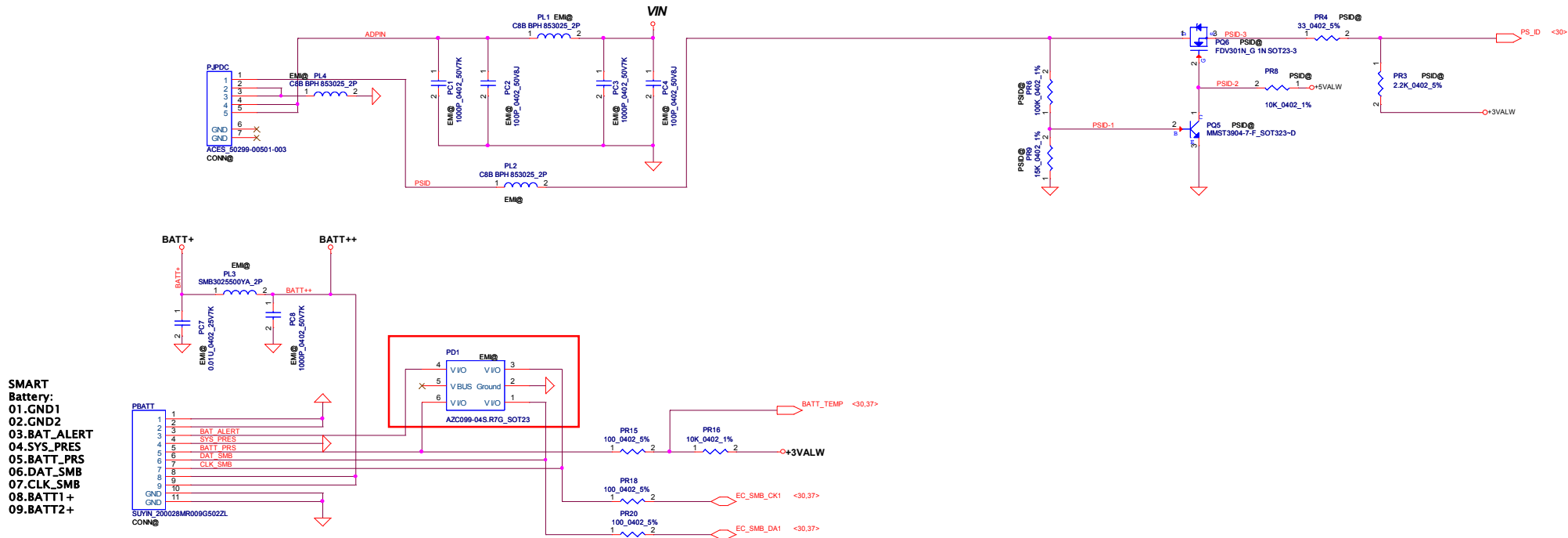


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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title
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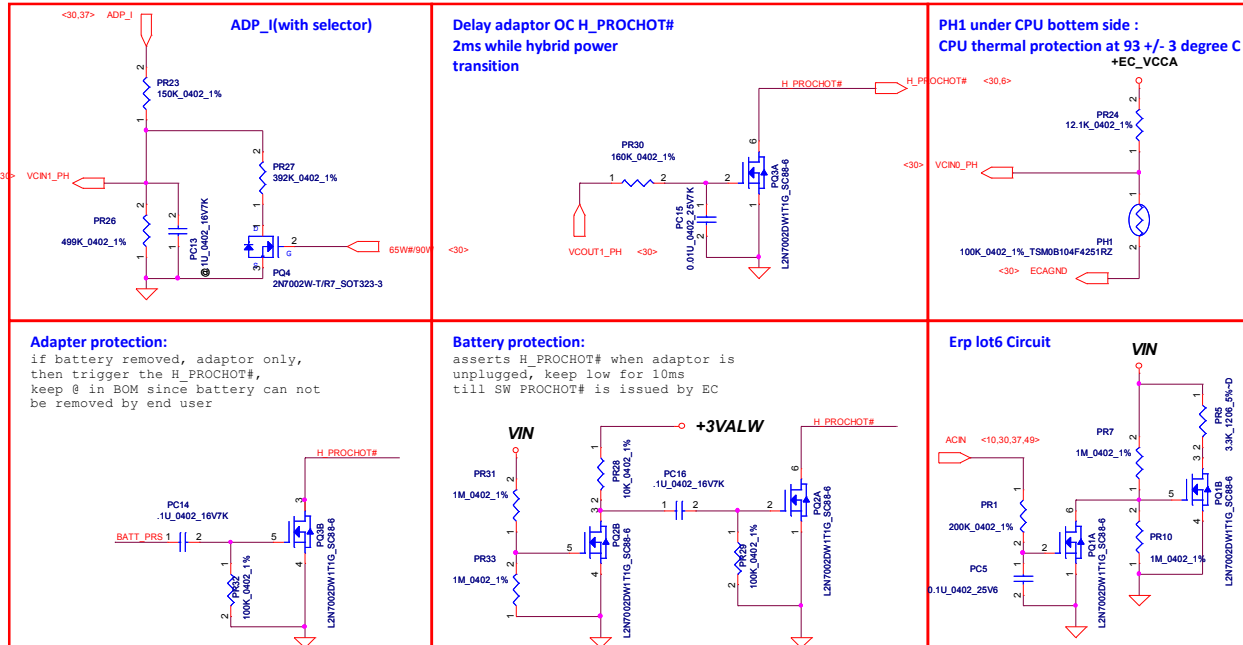
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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Security Classification	Compal Secret Data		Title		<b>Compal Electronics, Inc.</b>	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title		<b>HW-PIR Page.2</b>
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					<b>LA-9981P</b>	0.2
				Date:	Saturday, March 09, 2013	Sheet 35 of 55



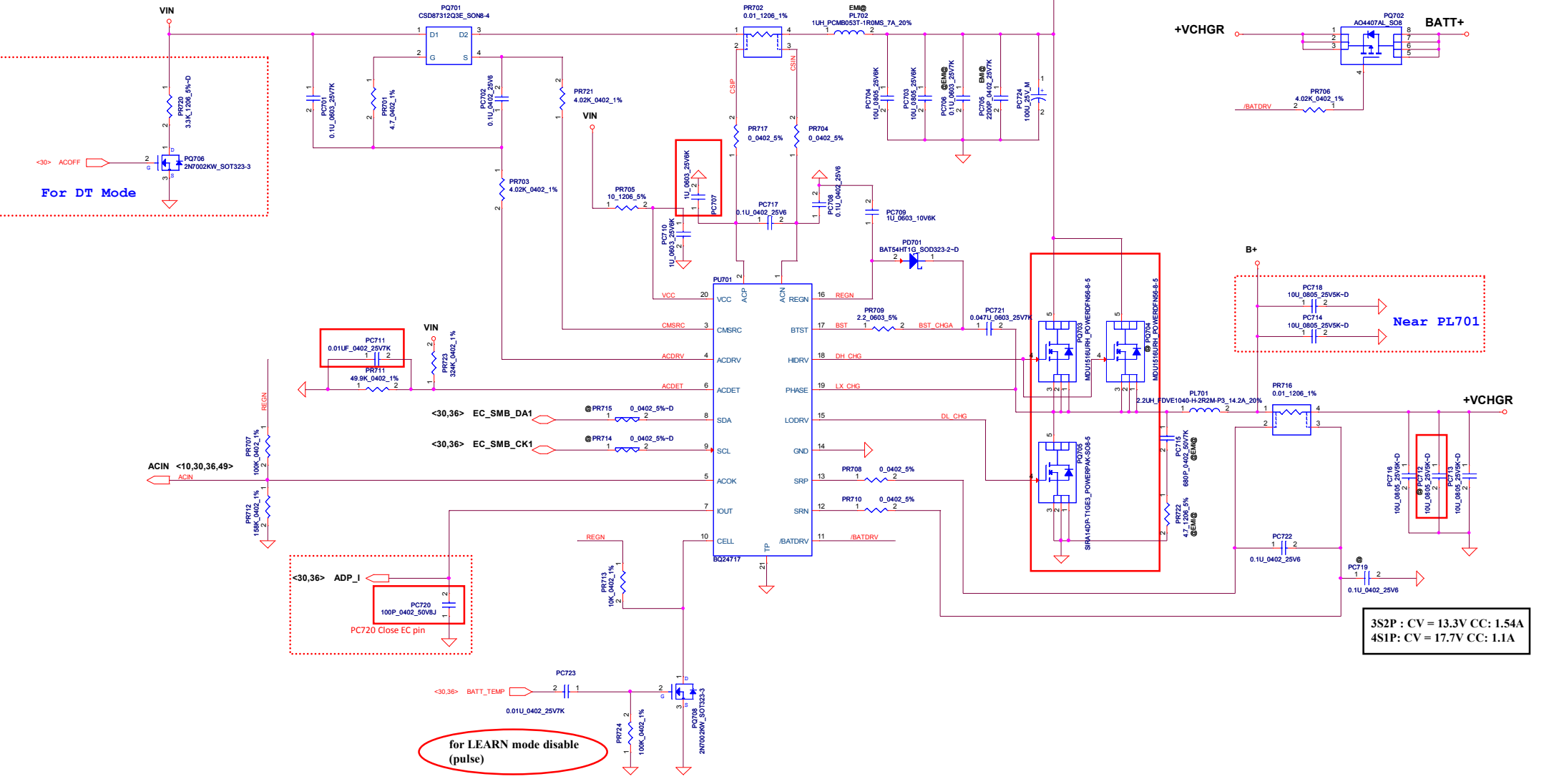
Other component (37.1)



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Date:	Saturday, March 09, 2013	Sheet	36	of	55

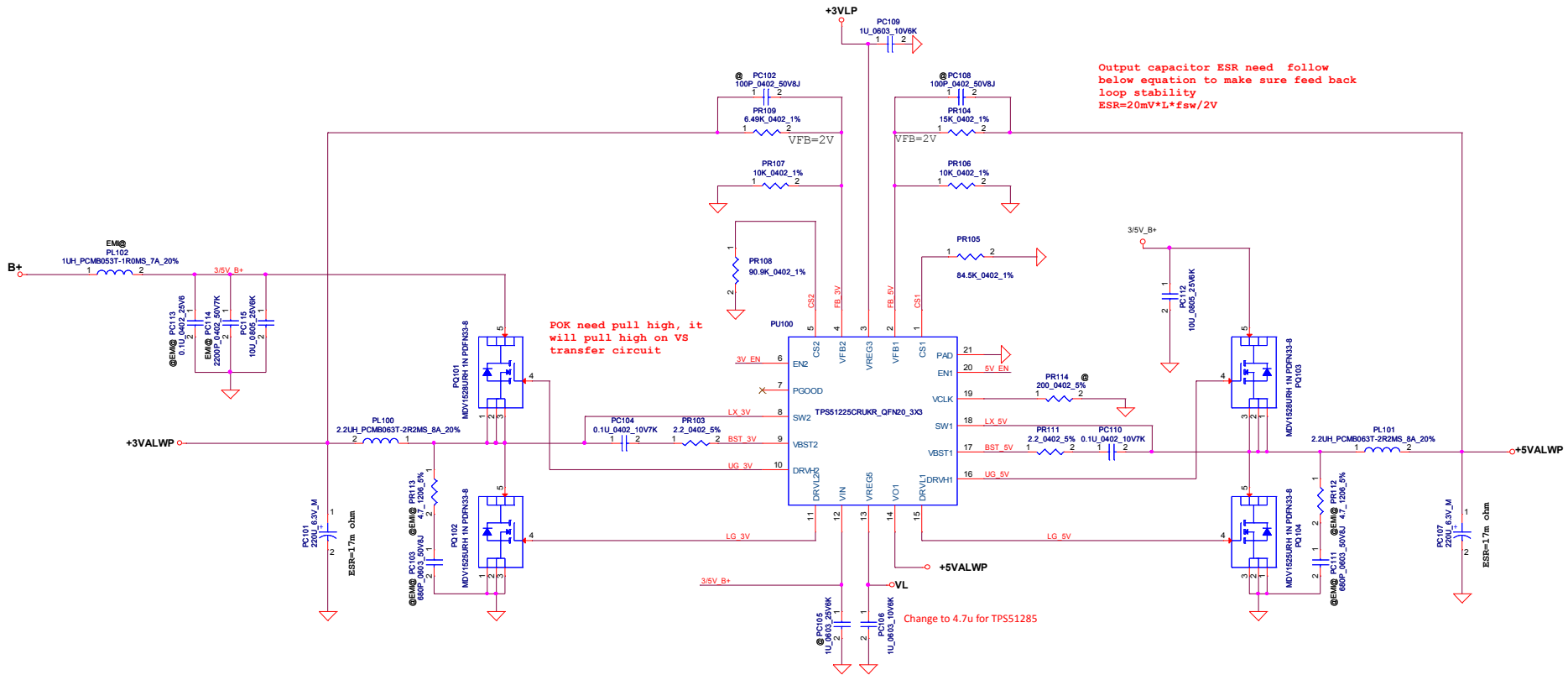
I<sub>ada</sub>=0~3.33A (65W)  
 I<sub>ada</sub>=0~4.62A (90W)

$$ADP\_I = 40 * I_{adapter} * R_{sense}$$

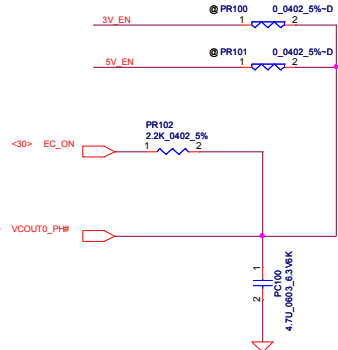
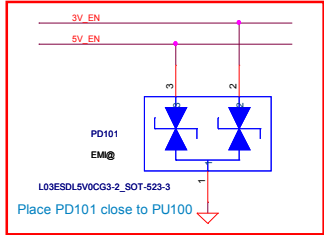


3S2P : CV = 13.3V CC: 1.54A  
 4S1P: CV = 17.7V CC: 1.1A

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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	
				PWR CHARGER	
				Rev	
				0.2	
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				Sheet	37 of 55

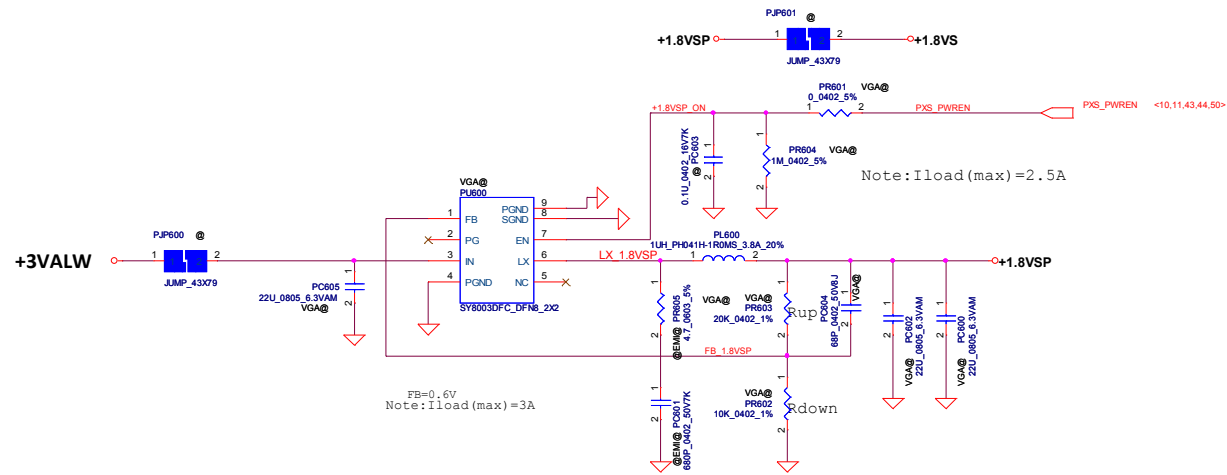
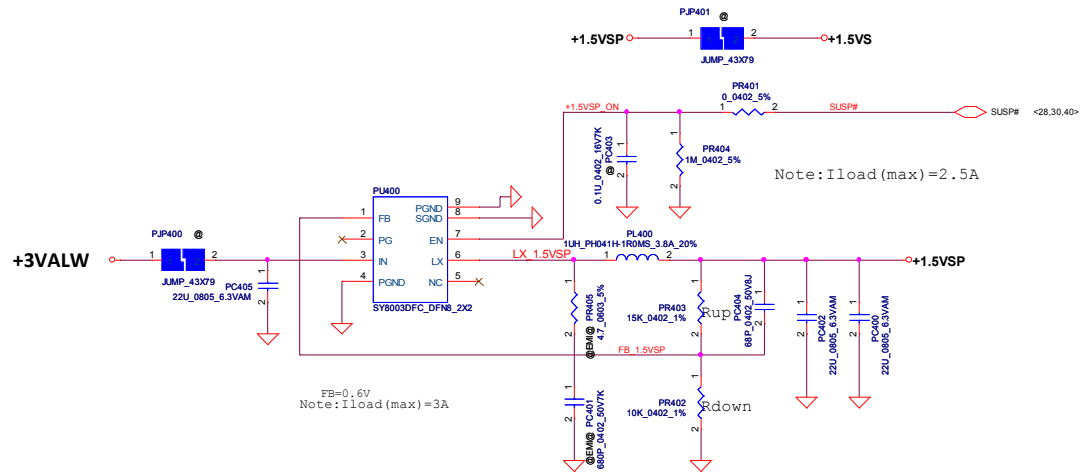


**3VALWP**  
 TDC 5.95A  
 Peak Current 8.5A  
 OCP current 10.2A  
 TYP MAX  
 H/S Rds (on) : 22mohm , 30mohm  
 L/S Rds (on) : 10.8mohm , 13.6mohm

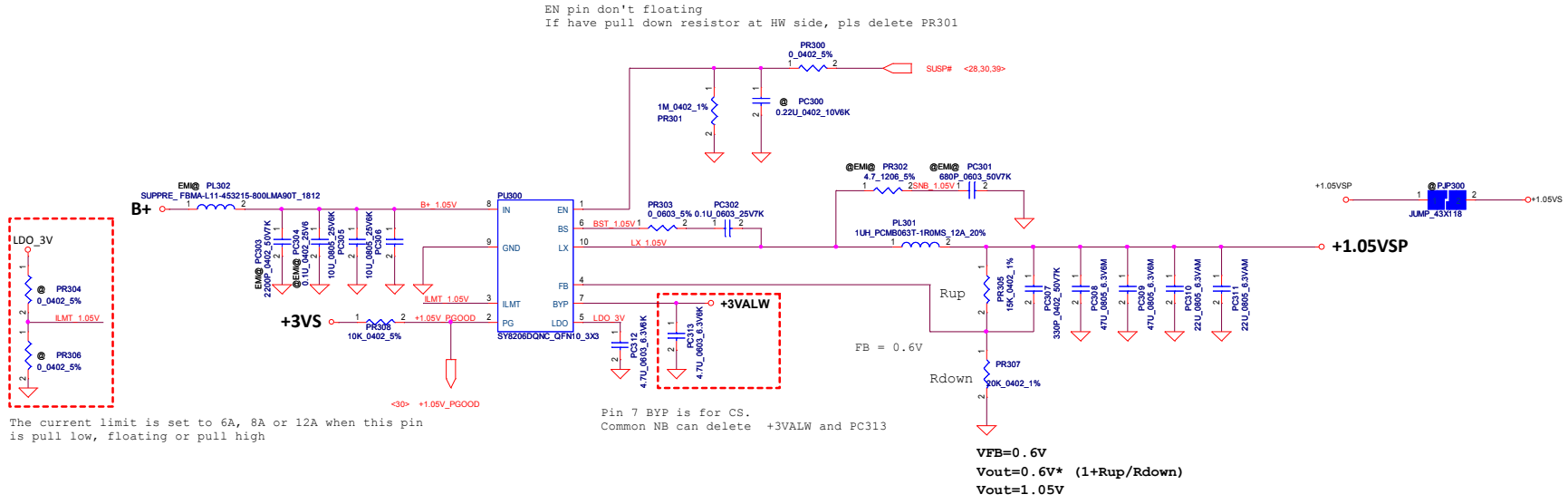


**5VALWP**  
 TDC 5.96A  
 Peak Current 8.51A  
 OCP current 10.2A  
 TYP MAX  
 H/S Rds (on) : 22mohm , 30mohm  
 L/S Rds (on) : 10.8mohm , 13.6mohm

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Issued Date	2013/03/09	Deciphered Date	2014/04/01	PWR 3.3VALWP/5VALWP	
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title <b>PWR 1.5VSP / 1.8VSP</b>	
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EN pin don't floating  
 If have pull down resistor at HW side, pls delete PR301

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

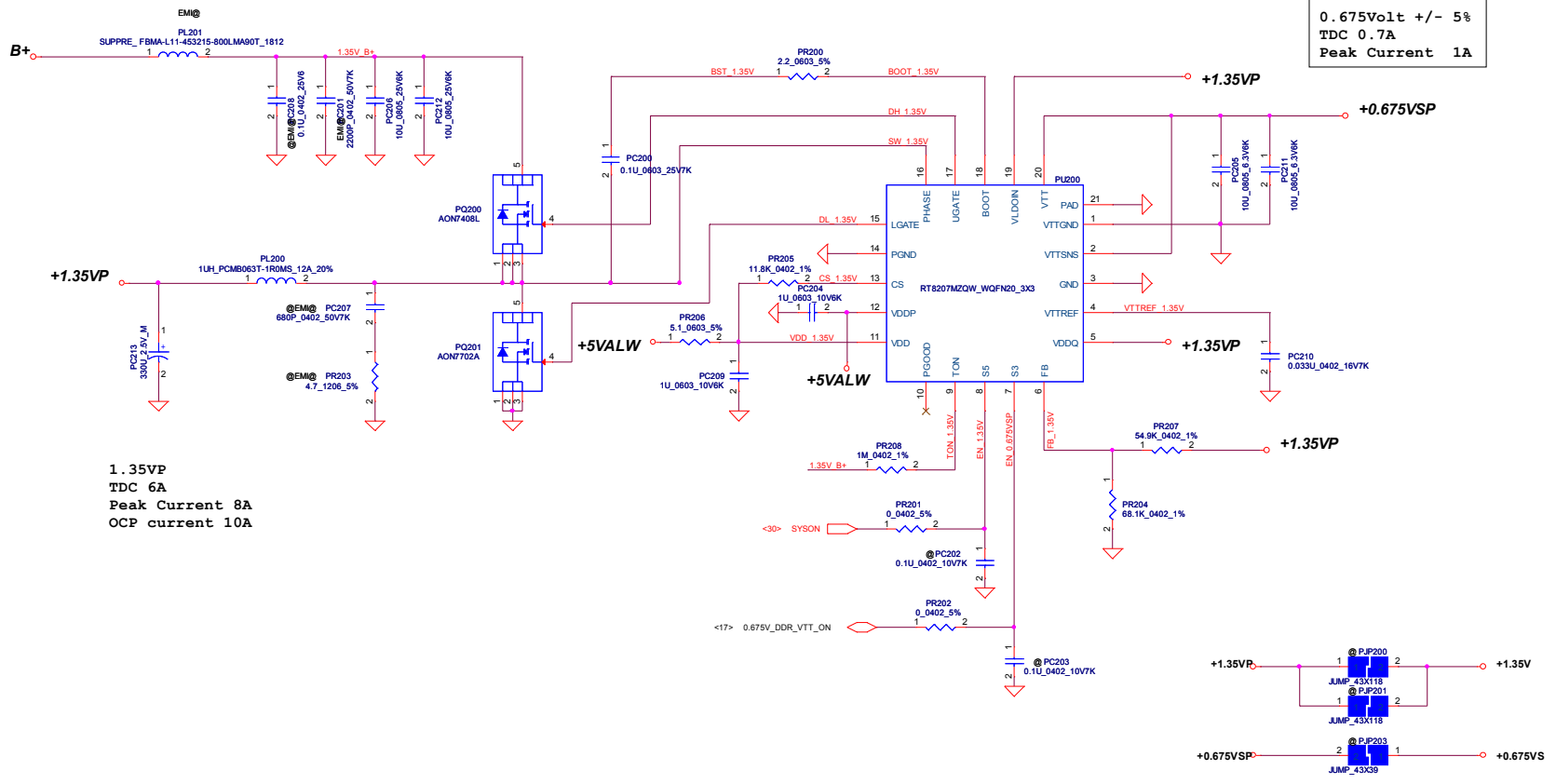
Pin 7 BYP is for CS.  
 Common NB can delete +3VALW and PC313

$V_{FB} = 0.6V$   
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$   
 $V_{out} = 1.05V$

+1.05VSP  
 TDC 5A  
 Peak Current 6.6A  
 OCP current 8A

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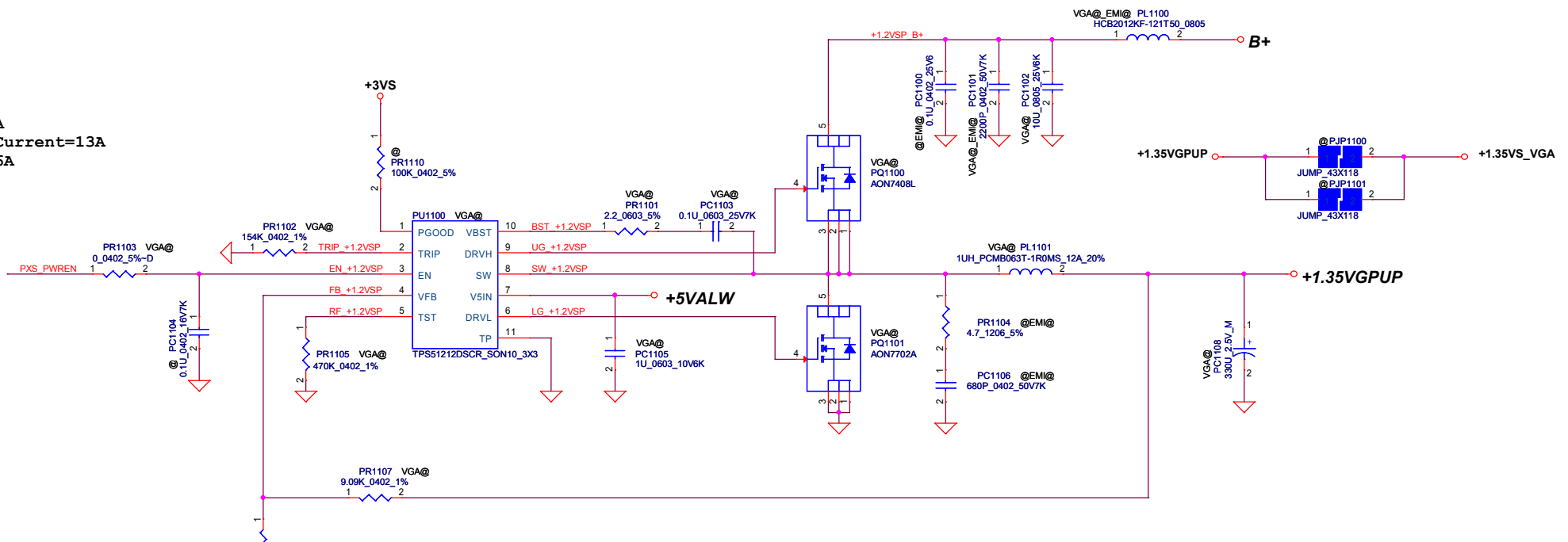




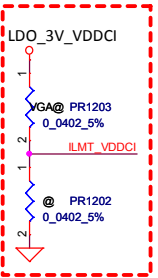
Security Classification	Compal Secret Data		Title	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	<b>Compal Electronics, Inc.</b>
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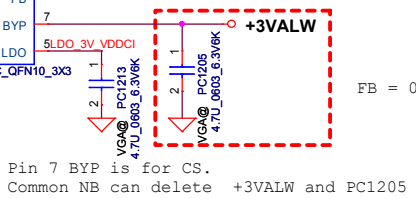
TDC=9A  
Peak Current=13A  
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

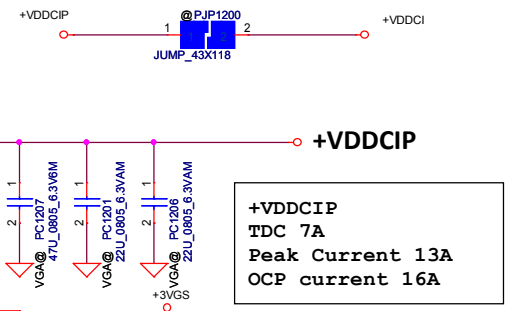


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC1205

VFB=0.6V  
 $V_{out}=0.6V * (1+R_{up}/R_{down})$   
 $V_{out}=0.9V$



+VDDCIP  
TDC 7A  
Peak Current 13A  
OCP current 16A

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				LA-9981P	
				Date:	Saturday, March 09, 2013
				Sheet	43 of 55

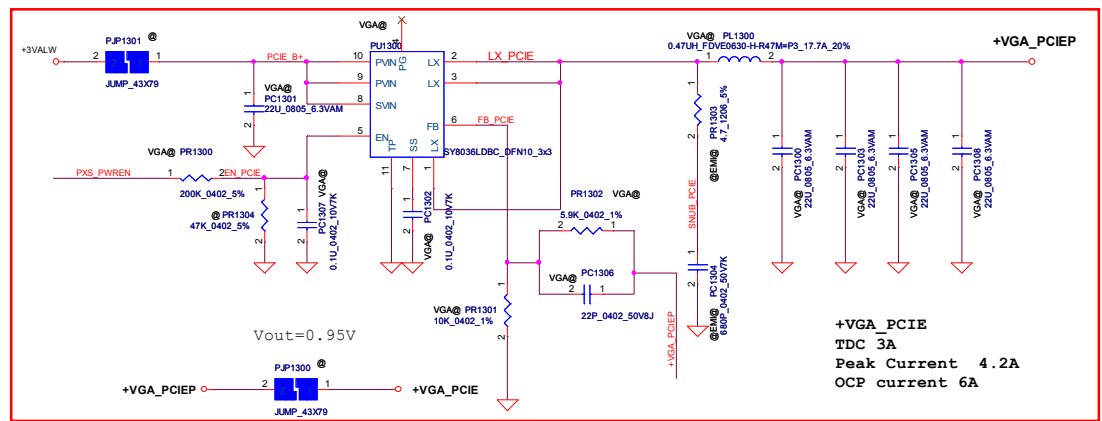
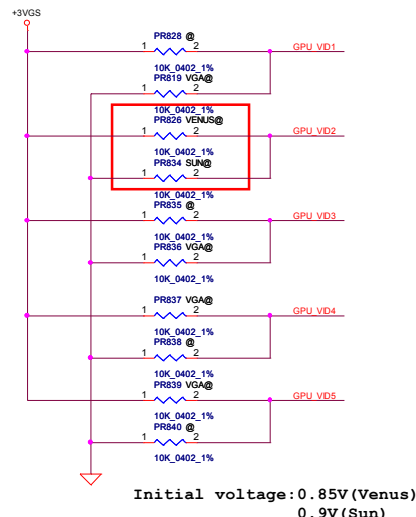
	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

**VGA\_CORE**  
Frequency 300kHz  
TDC 23A (25W) / 33A (32W)  
Peak Current 30A (25W) / 47A (32W)  
OCP current 36A (25W) / 56A (32W)  
TYP MAX  
H/S Rds (on) : 12.2mohm , 15mohm  
L/S Rds (on) : 2.75mohm , 3.5mohm  
Choke DCR 1.1mohm (Typ) / 1.3mohm (Max)  
Load line : -1.5mV/A

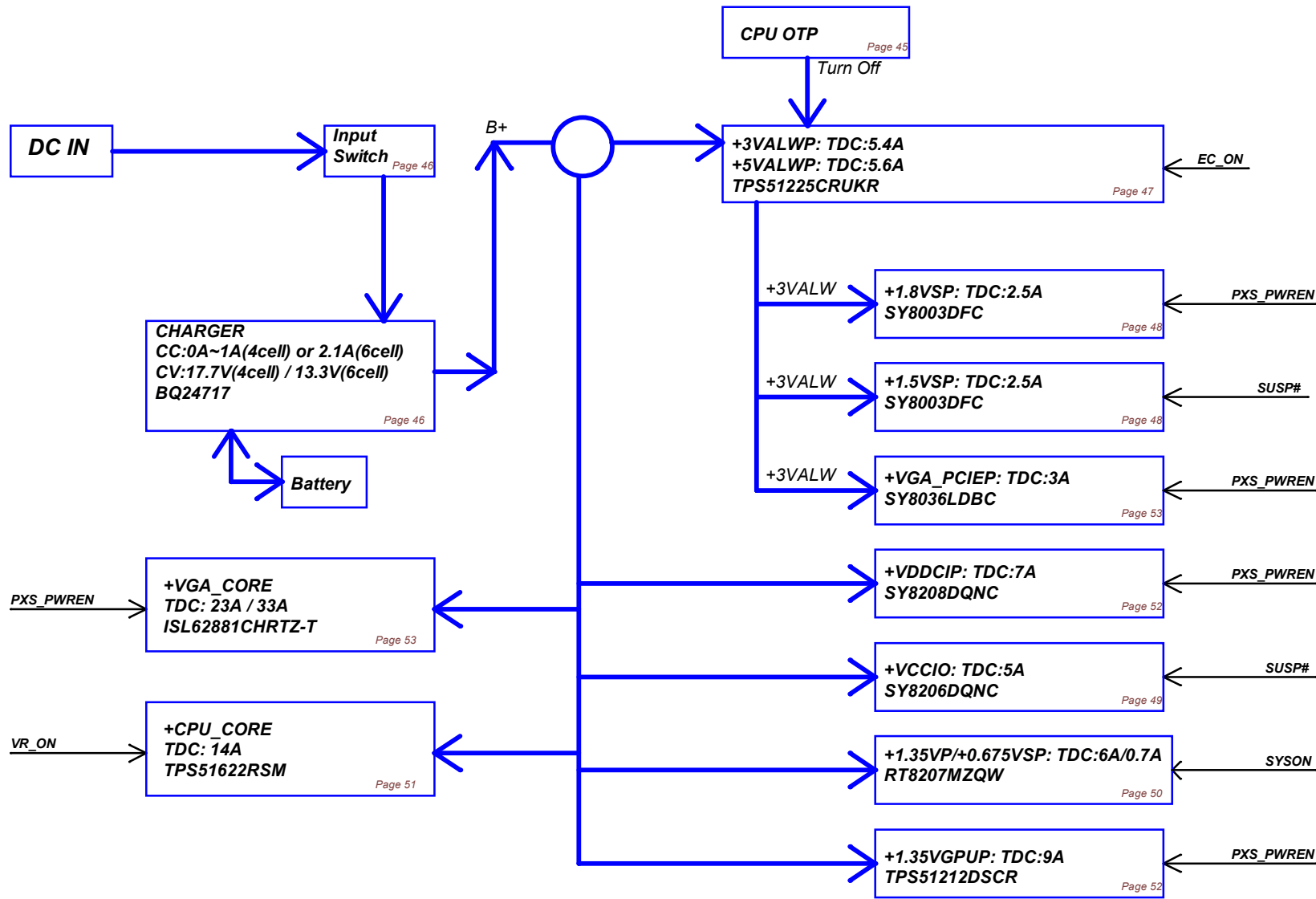


SPU_VID5 (GPIO_10)	SPU_VID4 (GPIO_14)	SPU_VID3 (GPIO_15)	SPU_VID2 (GPIO_16)	SPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V





# Power block



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*Version Change List (P. I. R. List)*

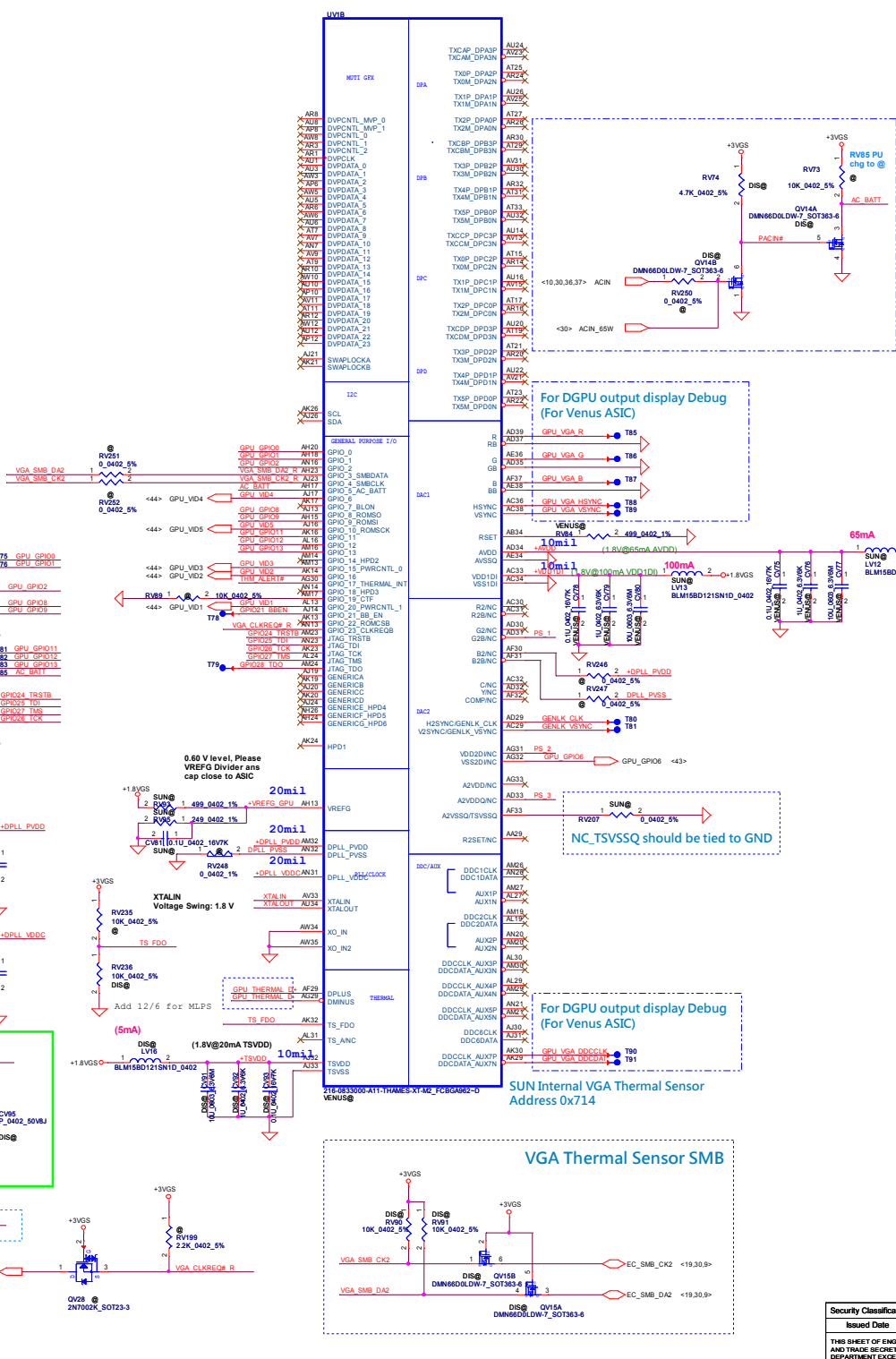
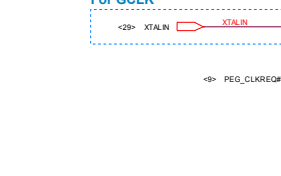
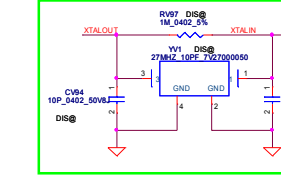
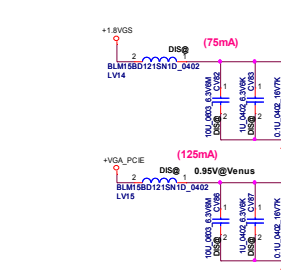
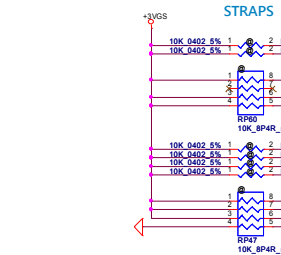
<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	45	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.2
2	50	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.2
3	44	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.2
4	46	3.3VALWP/SVALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101 (SCA00002A00)	0.2
5	50	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.2
6	52	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.2
7	52	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.2





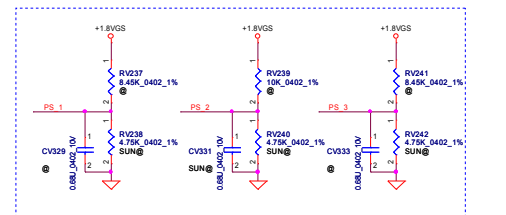
SUN GPIO N.C. PIN

- GPIO1 GPU\_GPIO1
- GPIO2 GPU\_GPIO2
- GPIO7 N.C
- GPIO11 GPU\_GPIO11
- GPIO12 GPU\_GPIO12
- GPIO13 GPU\_GPIO13
- GPIO14 N.C
- GPIO18 N.C



CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	RECOMMENDED SETTINGS
TX_PWRs_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	0: 50% swing 1: full swing	X
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BF_VGA_DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMDCFG(2:0)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
WP_DEVICE_STRAP_ENA	V25VNC	IGNORE WP DEVICE STRAPS		0
RSVD	H25VNC			0
RSVD	GENERIC			0
AUD[1]	HSYNC	AUD[1]AUD[0]	0: 0 No audio function 1: 1 Auto for DisplayPort and HDMI if dongle is detected 2: 1 Auto for DisplayPort only	11
AUD[0]	VSYNC			

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET		
GPIO21	H25VNC	GENERIC
GPIO2	GPIO8	

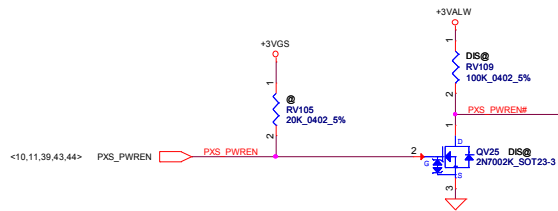


Vendor	RV241	RV242	Bits [3:1]
1280x16 (1GB) DDR3	Hynix 2Gb SA0006H40L(R1) SA0006H41L(R3)	NC	4.75K 000
1280x16 (1GB) DDR3	Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3)	8.45K 2K	001
1280x16 (1GB) DDR3	Micron 2Gb SA00005XB0L(R1) SA00005XB1L(R3)	4.75K NC	111



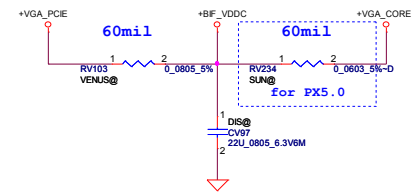
PX\_MODE=1 for Normal Operation  
 PX\_MODE=0 for BACO mode to shut down power rails except VDDR3,PCIE\_VDDC and 1.8V rail

**Note:**  
 PX4.0 +VGA\_CORE,VDDCI,+1.5VGS ON  
 PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF  
 PX5.0 +3VGS,+VGA\_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

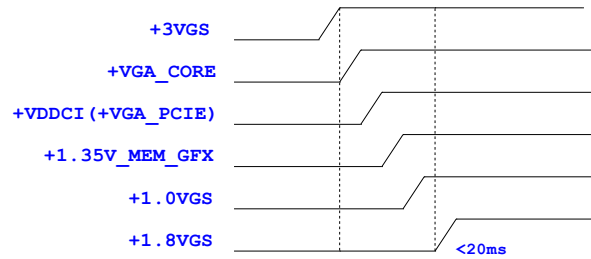


for PX4.0 and PX5.0

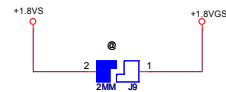
## Switch circuits in BACO desings for Thames/Seymour only 55mA@1.0V, in BACO mode



### Power sequence of Sun XT, Venus Pro, Venus XT

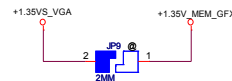


### +1.8VS TO +1.8VGS



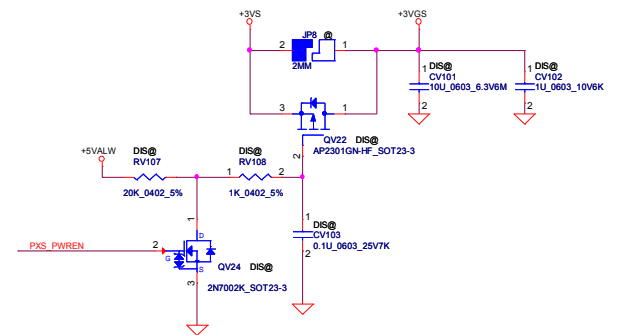
SHORT DEFAULT

### +1.35VS\_VGA TO +1.35V\_MEM\_GFX

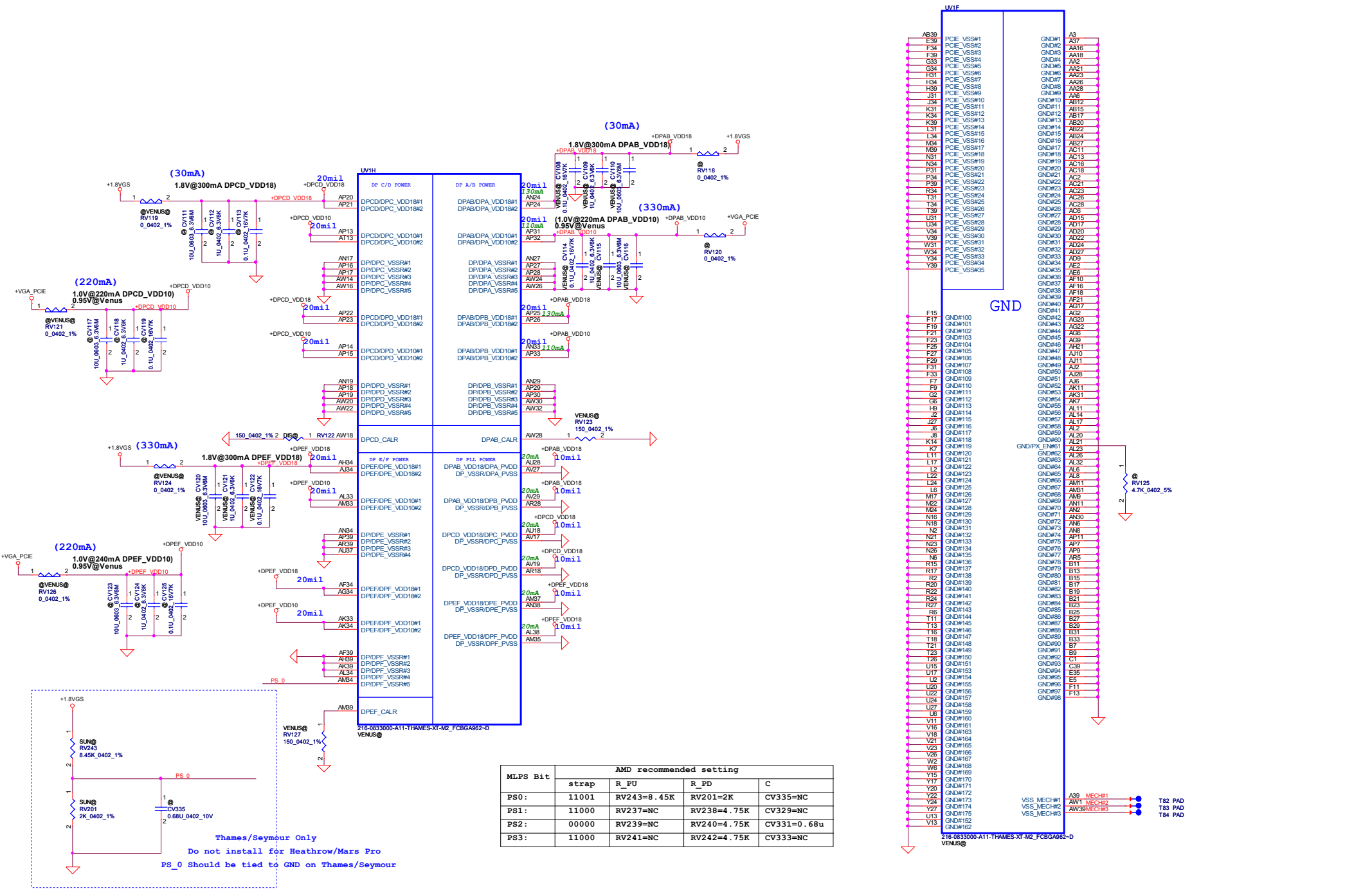


SHORT DEFAULT

### +3VS TO +3VGS

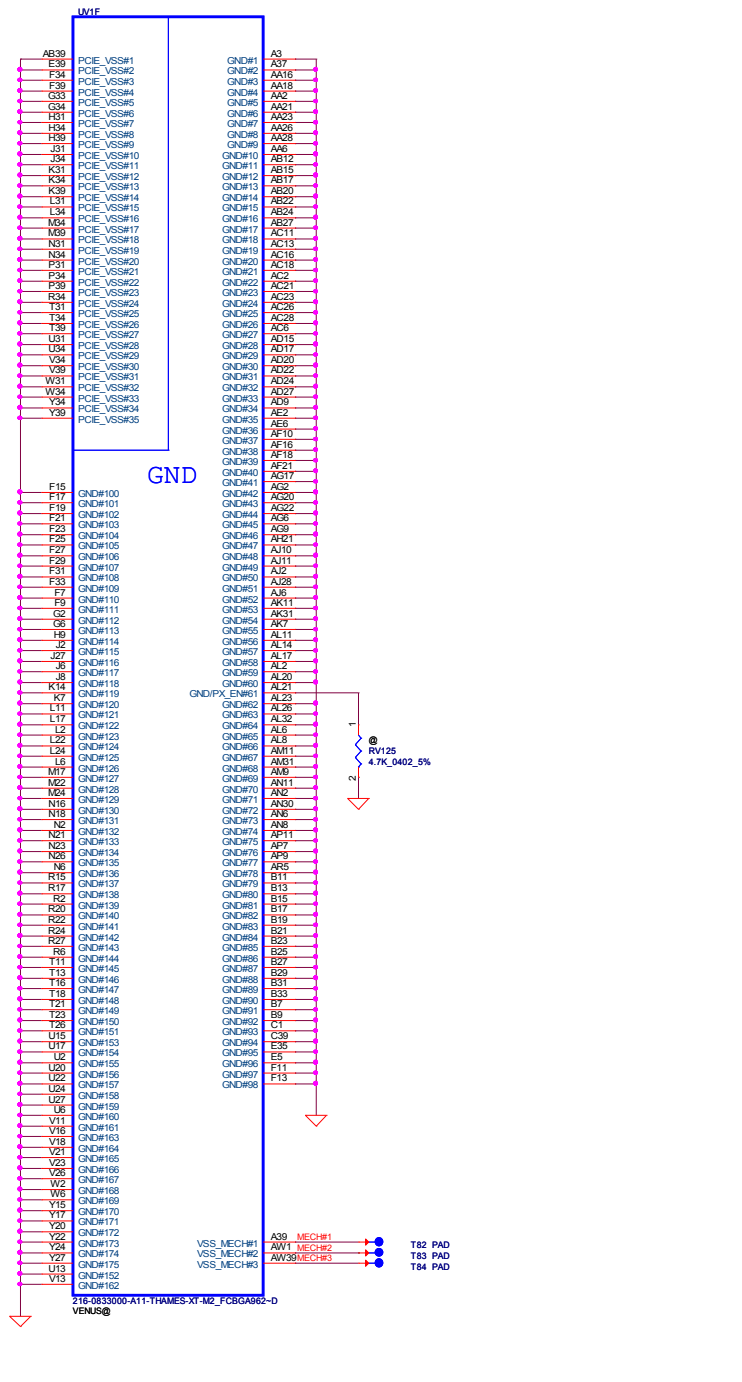


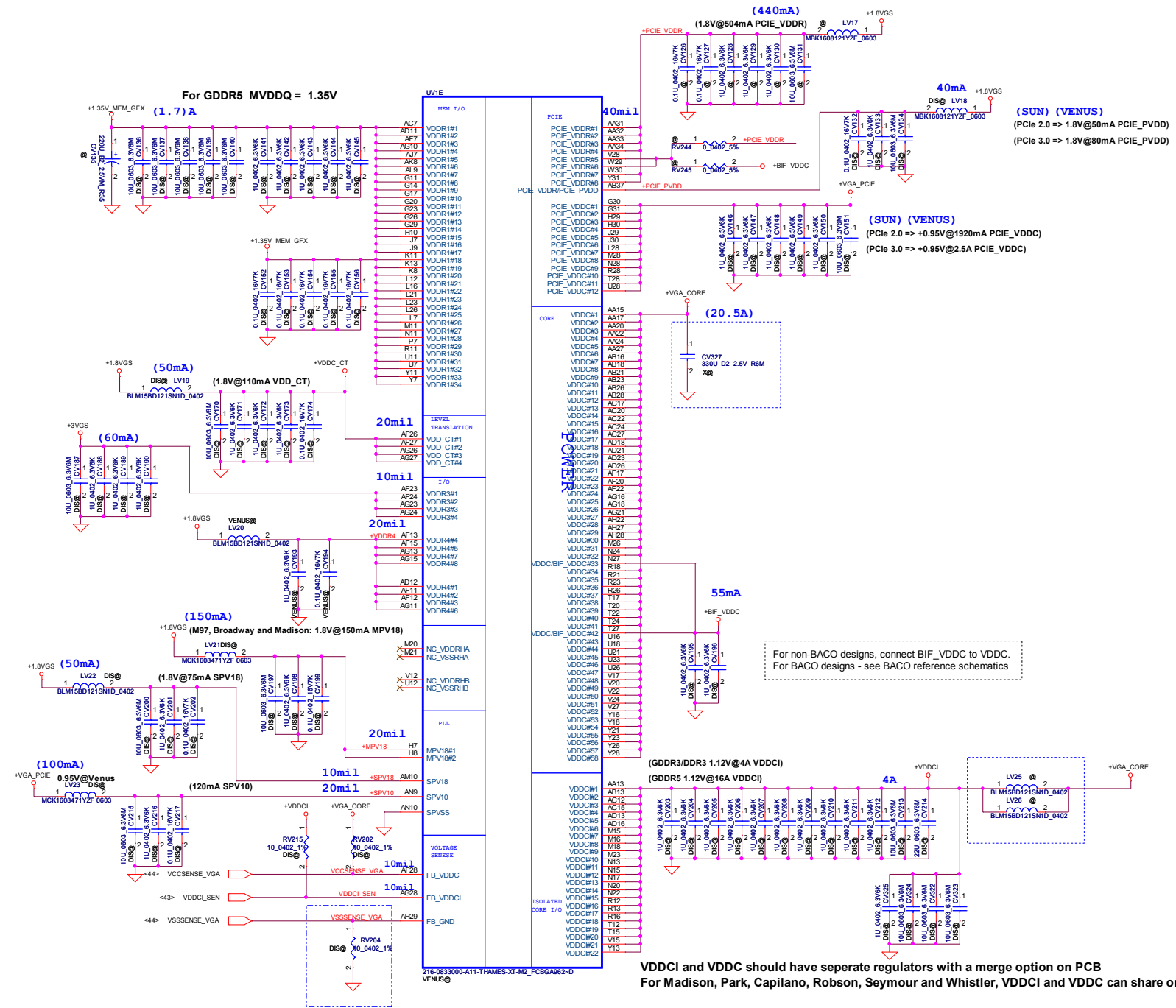
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MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

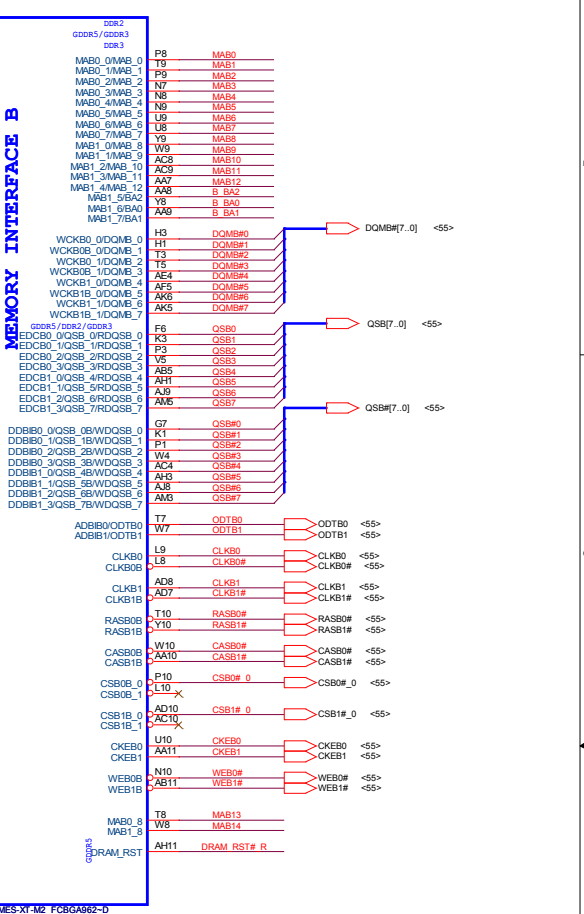
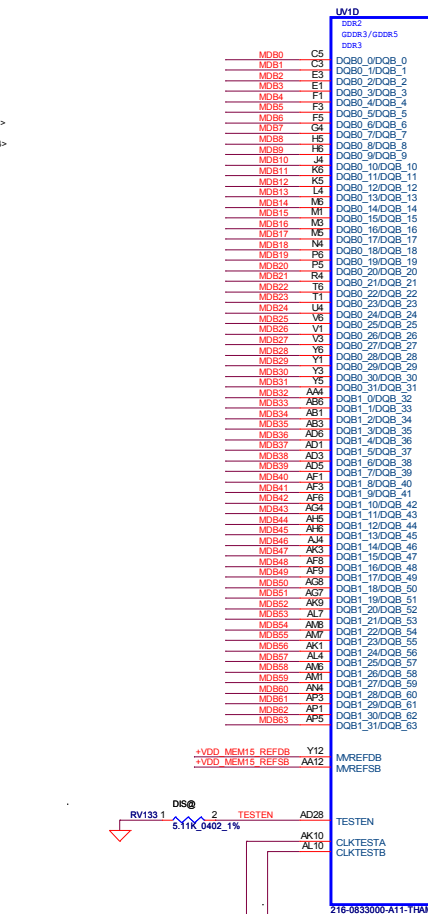
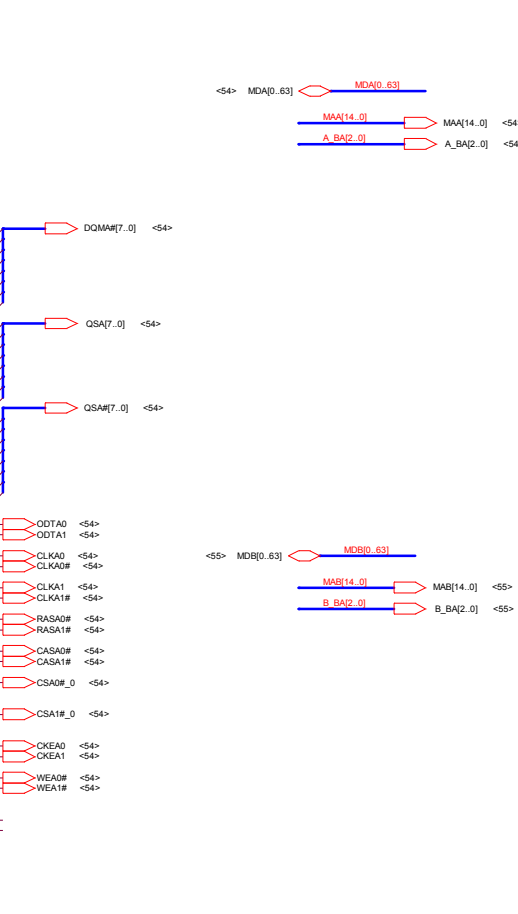
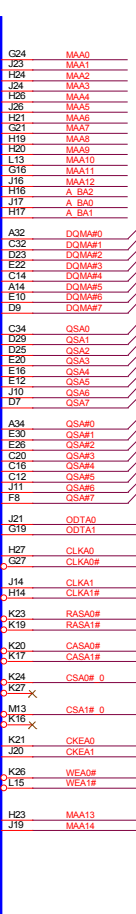
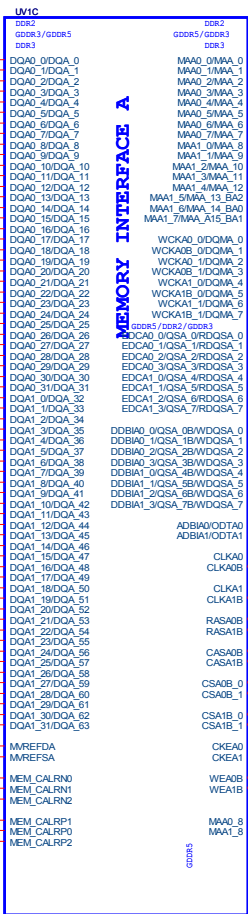
Thames/Seymour Only  
Do not install for Heathrow/Mars Pro  
PS\_0 Should be tied to GND on Thames/Seymour



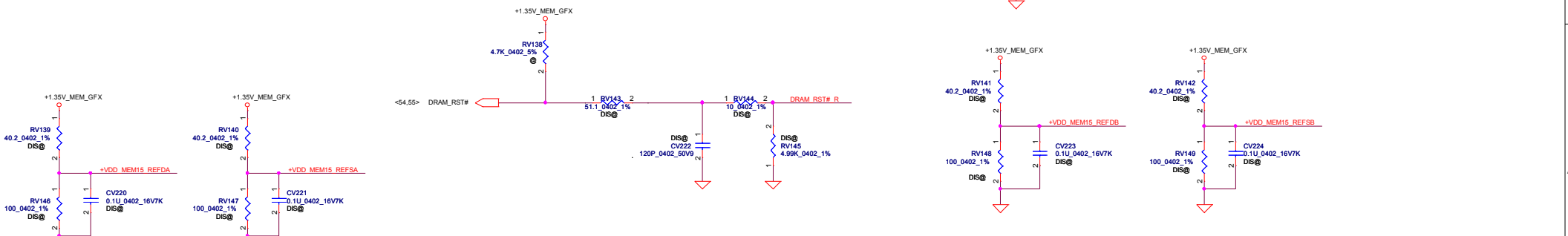
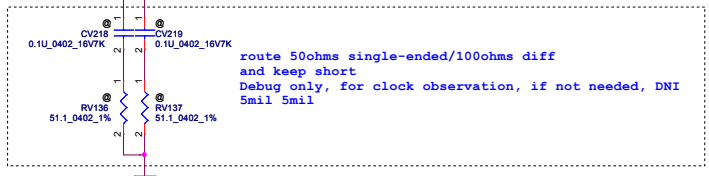


VDDCI and VDDC should have separate regulators with a merge option on PCB  
 For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

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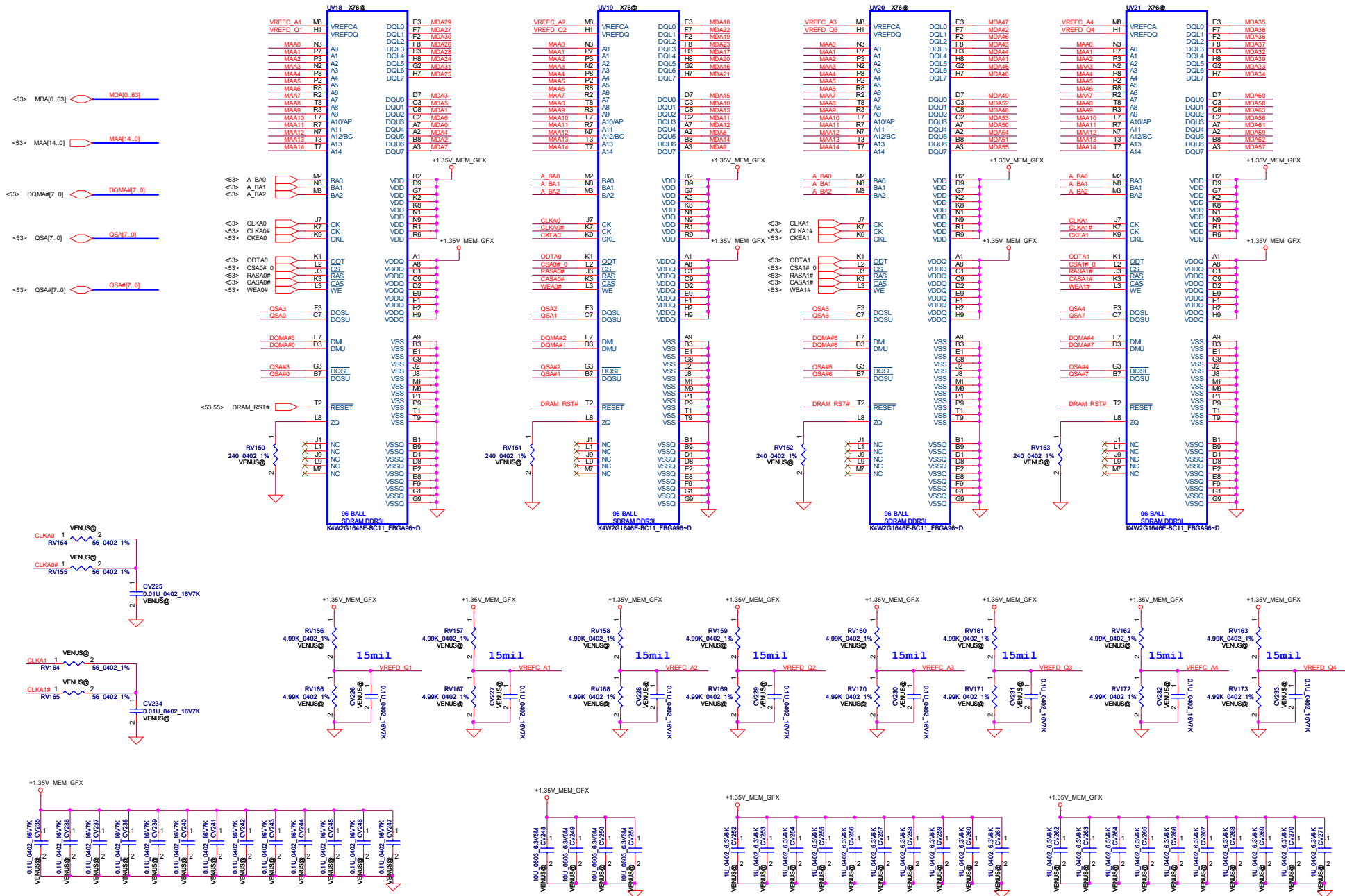


This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2



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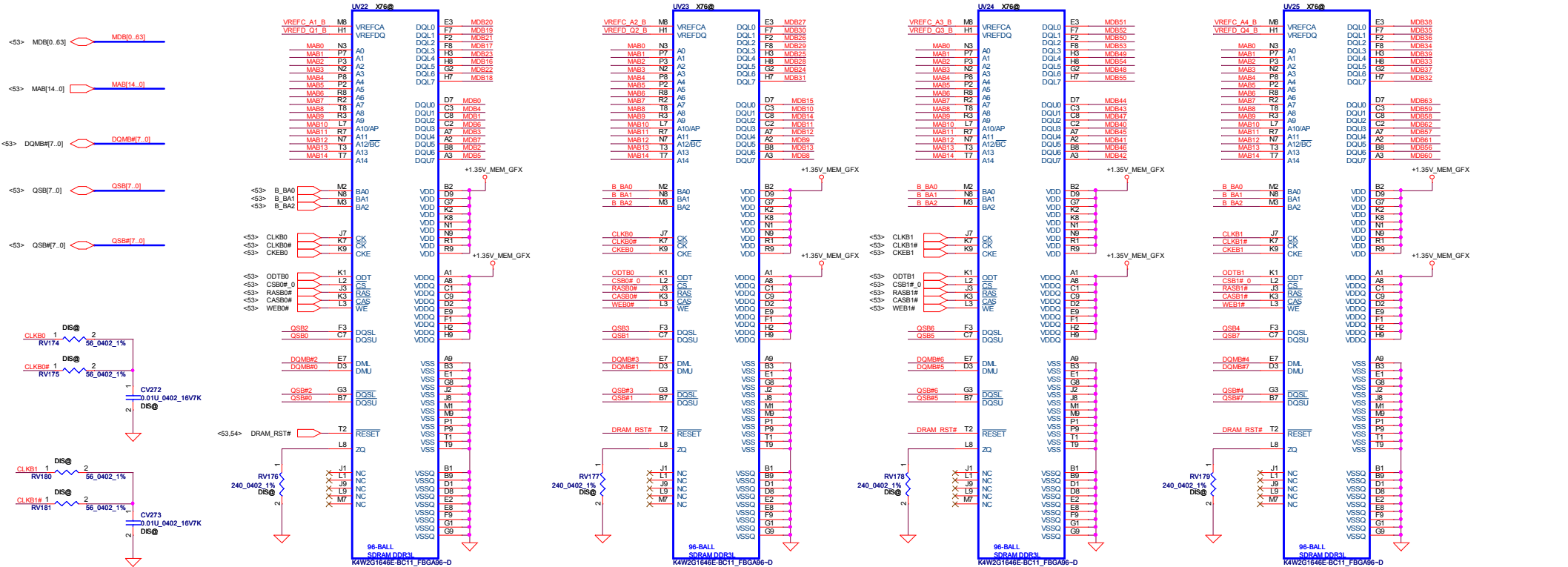
# CHANNEL A: 256MB DDR3



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# CHANNEL B : 256MB DDR3



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