Iris HSW/BDW Schematics
Broadwell-ULT

2015-01-20
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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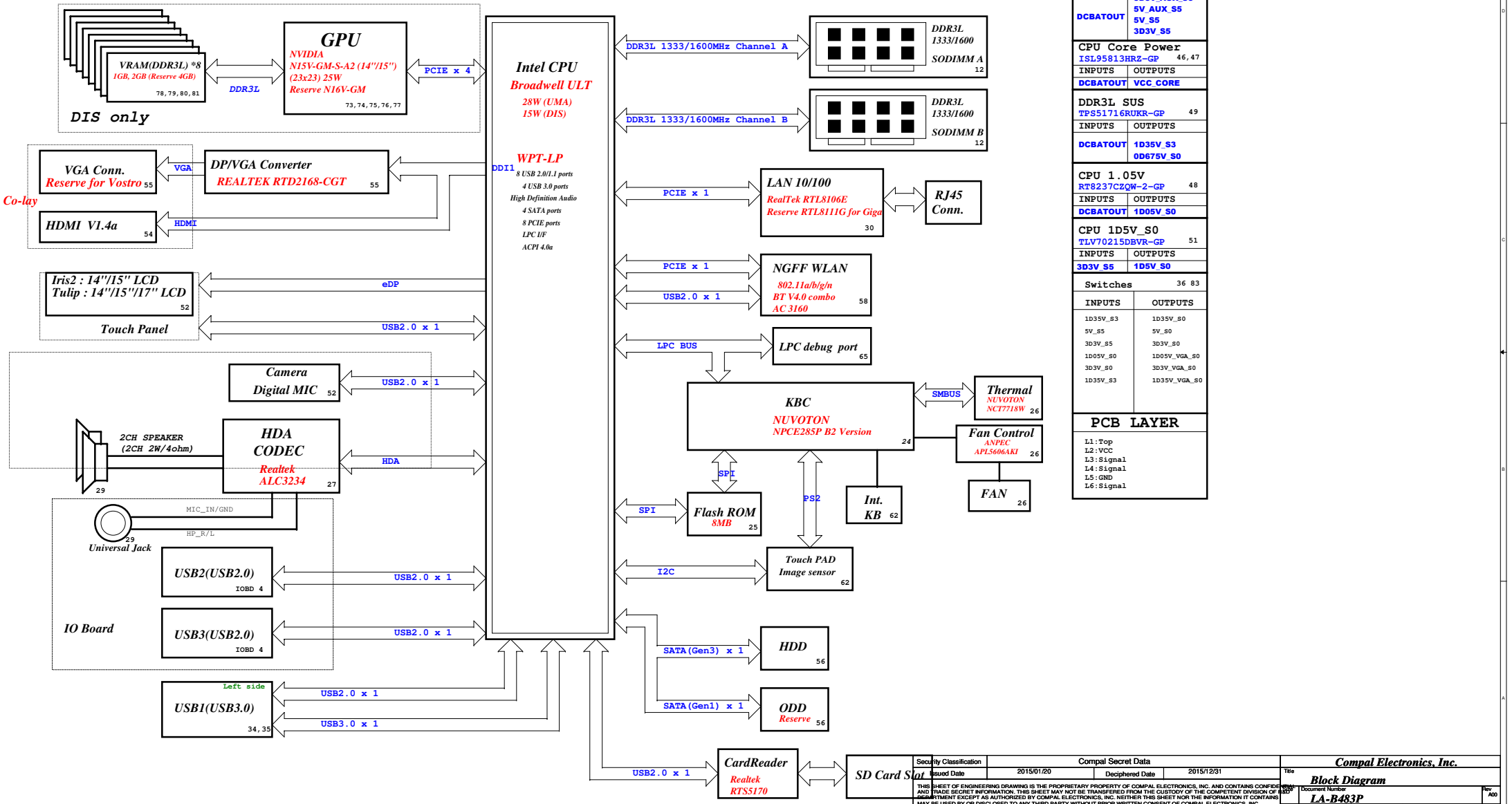
Title: *Cover Page*

Size | Document Number: *LA-B483P* | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 1 of 102

Project code:
Iris-2 14 --> 4PD031010001
Iris-2 15 --> 4PD032010001
PCB P/N: 14216
Revision: X01

Iris2/Tulip/VanGogh Block Diagram



CHARGER		
HPA02224RGRR-1-GP		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95813HRZ-GP	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

CPU 1.05V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU 1D5V_S0	
TLV70215DBVR-GP	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

Switches 36 83

INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

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Title: Block Diagram			
Document Number: LA-B483P			Rev: A00
Date: Wednesday, January 21, 2015	Sheet 2 of 102		

(Blanking)

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Compal Electronics, Inc.

Title: **Reserved**

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 3 of 102

Main Func = CPU

For EMI Reserved

H_CPUPWRGD — EC4011 2 SCD1U16V2KX-3GP @EMI@

XDP_TRST# — EC4021 2 SCD1U16V2KX-3GP @EMI@

1D05S_VCCST

RN401
XDP_TMS 1 8
XDP_TDI 2 7
3 6
XDP_TDO 4 5
SRN51J-1-GP @

@
XDP_TRST# R402 1 2 51R2J-2-GP
XDP_TCLK R406 1 2 51R2J-2-GP

1D05S_VCCST

Remove TP401 for TP604 spacing.

R401 62R2J-GP

Layout Note:
Impedance control:50 ohm

<24,42,43,48> H_PROHOT#

<24> H_PECI

H_CATERR# — TP402 TPAD14-OP-GP

H_PROHOT# R — R403 56R2J-4-GP

DY
<36> H_THERMTRIP_EN — R411 0R2J-2-GP

Layout Note: Close to CPU

H_CPUPWRGD — TP403 TPAD14-OP-GP — R405 10KR2J-3-GP

SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
SM_DRAMRST#
DDR_PG_CTRL
<12> DDR_PG_CTRL

CPU1B — HSW_ULT_DDR3L — 2 OF 19

PROC_DETECT#	D61	MISC
CATERR#	K61	
PECI	N62	
PROCHOT#	K63	THERMAL
PROCPWRGD	C61	PWR
SM_RCOMP0	AU60	DDR3L
SM_RCOMP1	AV60	
SM_RCOMP2	AU61	
SM_DRAMRST#	AV15	
SM_PG_CNTL1	AV61	

JTAG

PRDY#	J62	XDP_PRDY#
PREQ#	K62	XDP_PREQ#
PROC_TCK	E60	XDP_TCLK
PROC_TMS	E61	XDP_TMS
PROC_TRST#	E59	XDP_TRST#
PROC_TDI	F63	XDP_TDI
PROC_TDO	F62	XDP_TDO

XDP_PRDY# <96>
XDP_PREQ# <96>
XDP_TCLK <96>
XDP_TMS <96>
XDP_TRST# <96>
XDP_TDI <96>
XDP_TDO <96>

XDP_BPM[7:0] — XDP_BPM[7:0] <96>

BPM#0	J60	XDP_BPM0
BPM#1	H60	XDP_BPM1
BPM#2	H61	XDP_BPM2
BPM#3	H62	XDP_BPM3
BPM#4	K59	XDP_BPM4
BPM#5	H63	XDP_BPM5
BPM#6	K60	XDP_BPM6
BPM#7	J61	XDP_BPM7

GP

HASWELL-6-GP-U

@

R407 1 2 200R2F-L-GP SM_RCOMP_0
R408 1 121R2F-GP SM_RCOMP_1
R409 1 2 100R2F-L1-GP-U SM_RCOMP_2

Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

1D35V_S3

R410 470R2J-2-GP

SM_DRAMRST# — R404 1 @ 2 0_0402_1% — DDR3_DRAMRST# <12,13>
Short Pad

Layout Note:
Place close to DIMM

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Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

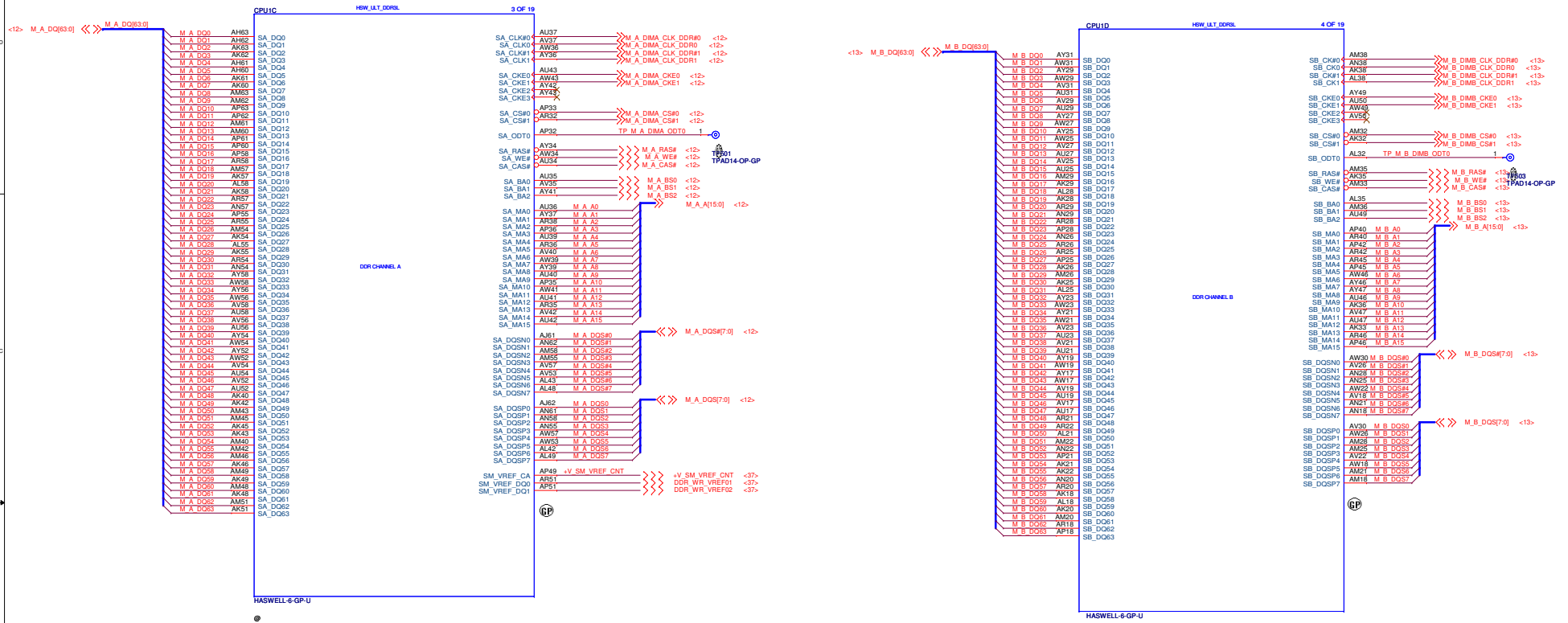
Title: CPU (THERMAL/MISC/PM)

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 4 of 102

Main Func = CPU

DDR3L ball type: Non-Interleaved Type



HSW

CPU1 4030@

CL8064701552900 SR1EN D0 1.9G A31!

SA00007TA1L

CPU1 4005@

CL8064701478404 SR1EK D0 1.7G BGA

SA000072Q2L

Broadwell

CPU1 BDW_PQS@

FH8065801620003 QH15 E0 2.2G

SA000083A0L

CPU1 3805@

FH8065801620702 SR210 E0 1.9G FCBGA

SA000083F2L

CPU1 3205@

FH8065801882800 SR215 E0 1.5G FCBGA

SA000083H1L

CPU1 5010@

FH8065801620406 SR23Z F0 2.1G FCBGA

SA00008982L

CPU1 5200@

FH8065801620204 SR23Y F0 2.2G FCBGA

SA00008992L

CPU1 5005@

FH8065801884006 SR244 F0 2G FCBGA

SA000083E3L

CPU1 5500@

FH8065801620004 SR23W F0 2.4G FCBGA

SA000089A2L

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Issued Date	2015/01/20	Deciphered Date	2015/12/31

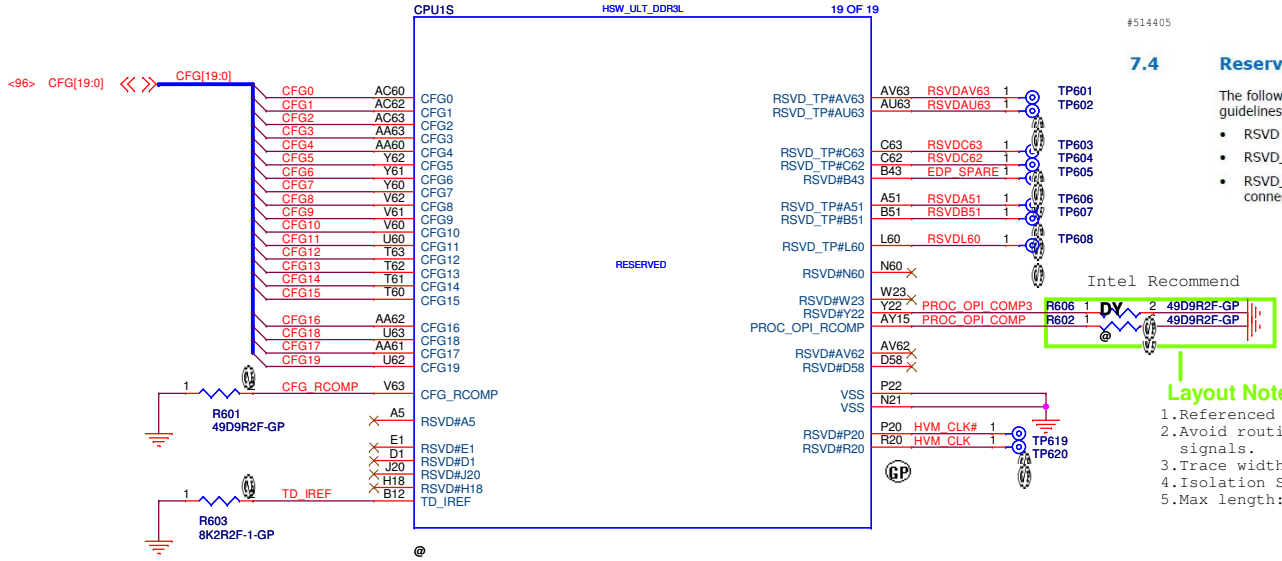
Compal Electronics, Inc.

Title: *CPU (DDR)*

Size | Document Number: *LA-B483P* | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 5 of 102

Main Func = CPU



#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Intel Recommend

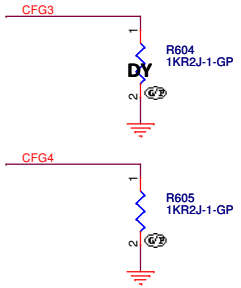
Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405

PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. • **CFG[2:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[3]: MSR Privacy Bit Feature** – 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting – 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • **CFG[4]: eDP enable** – 1 = Disabled – 0 = Enabled • **CFG[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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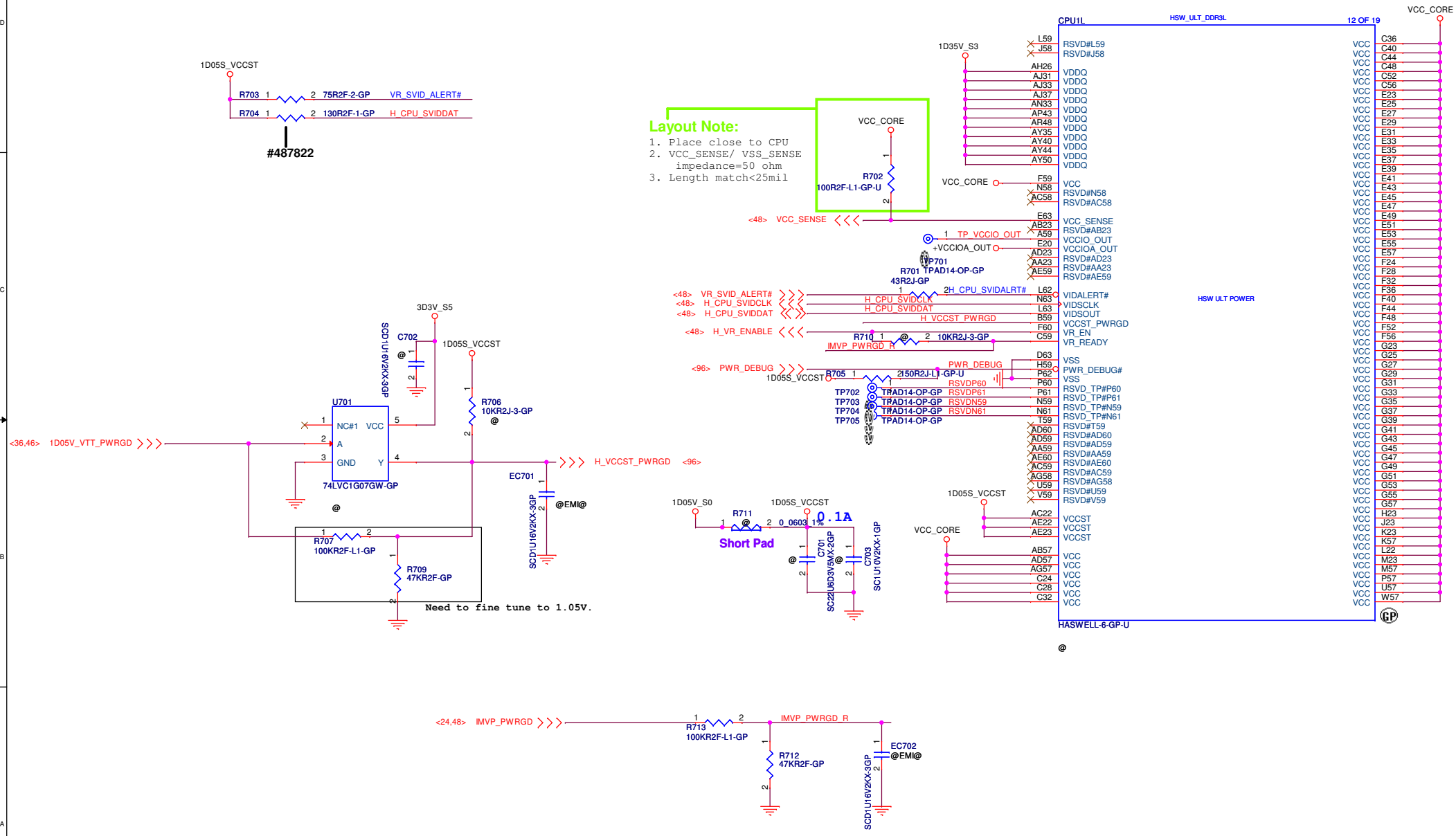
Title	CPU (RESERVED)		
Size	Document Number		Rev
	LA-B483P		A00
Date:	Wednesday, January 21, 2015	Sheet	6 of 102

Main Func = CPU



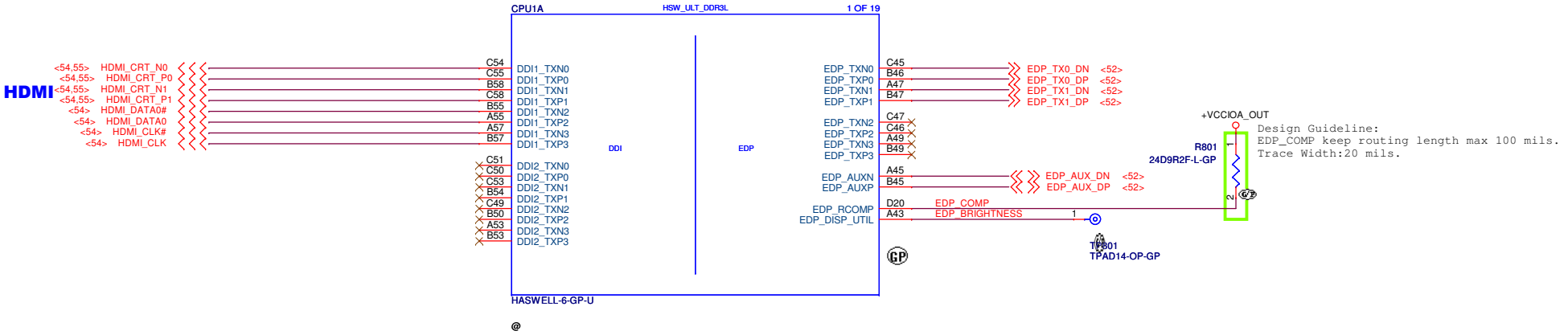
Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **CPU (VCC Core)**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 7 of 102



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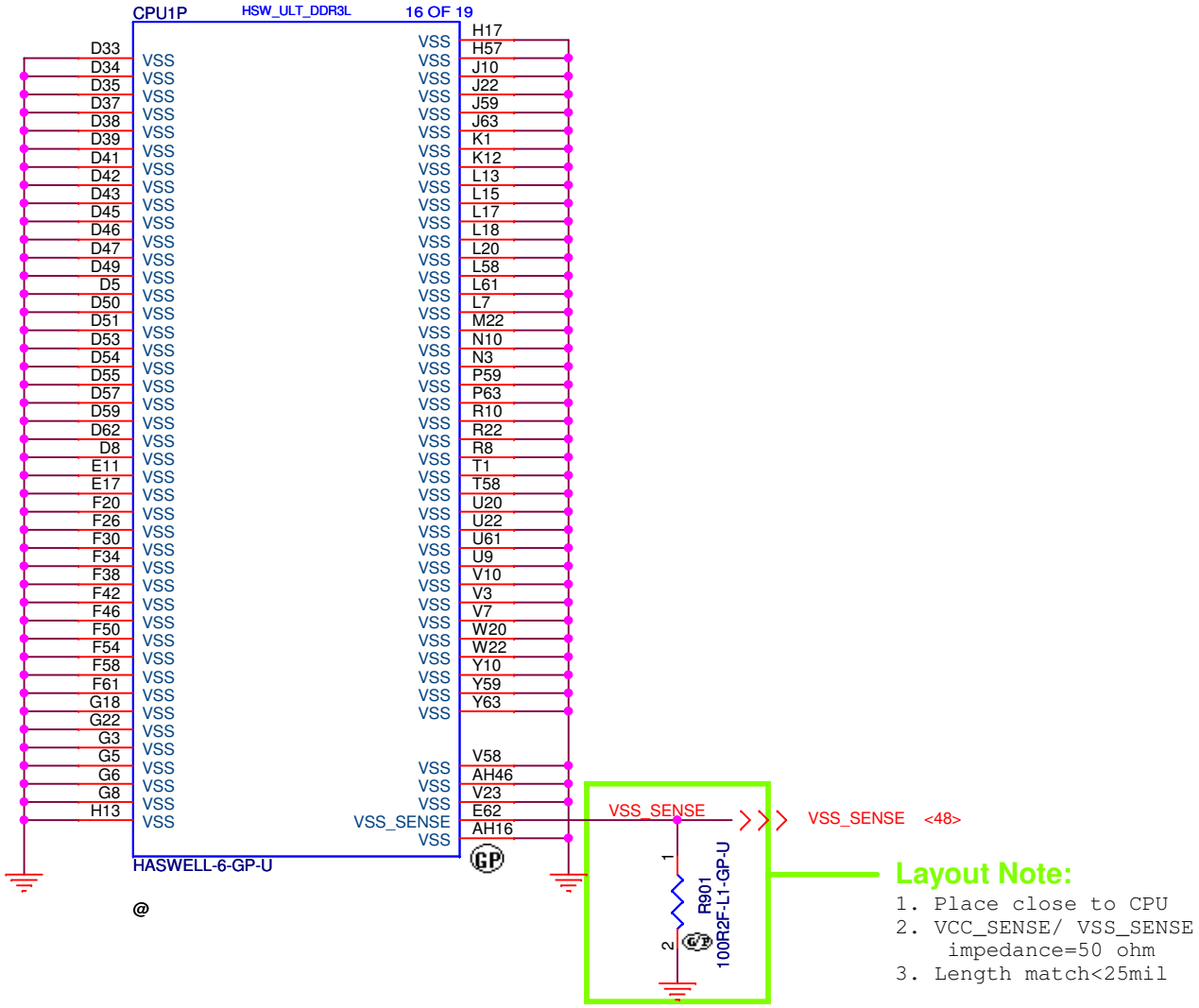
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: CPU (DDI/EDP)			
Size	Document Number: LA-B483P		Rev: A00
Date: Wednesday, January 21, 2015	Sheet 8 of 102		

Main Func = CPU



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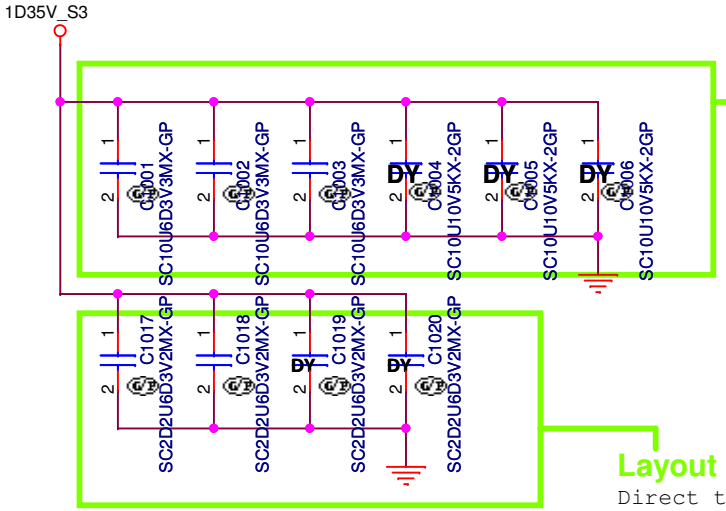
Compal Electronics, Inc.

Title: **CPU (VSS)**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 9 of 102

Main Func = CPU



Layout Note:
As close to CPU as possible

Layout Note:
Direct tie to CPU VccIn/Vss balls

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Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **CPU (Power CAP1)**

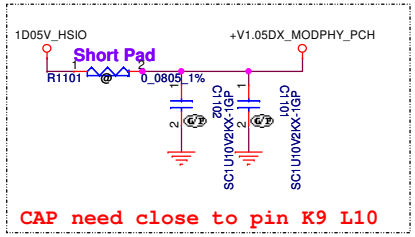
Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 10 of 102

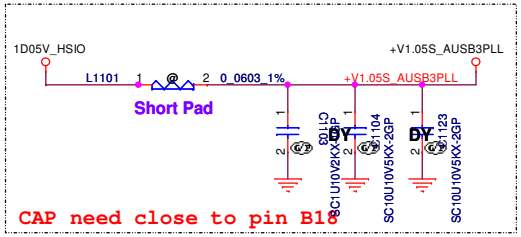
Main Func = CPU

MAX: 1.92A

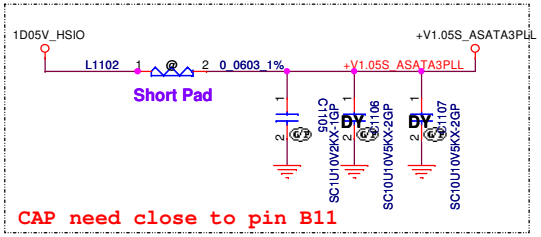
1.838A



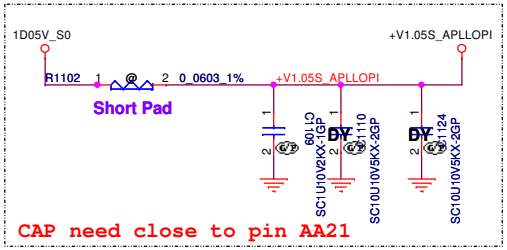
41mA



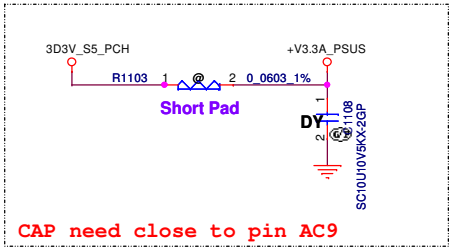
42mA



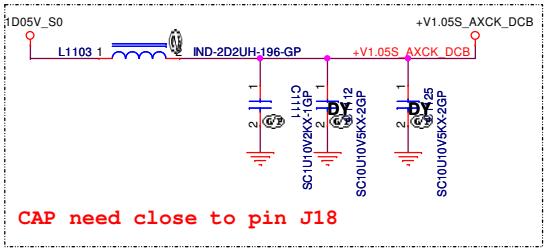
57mA



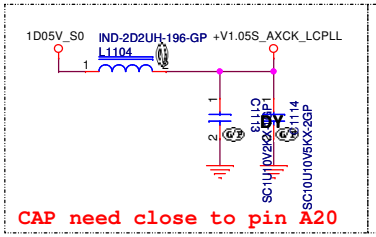
62mA



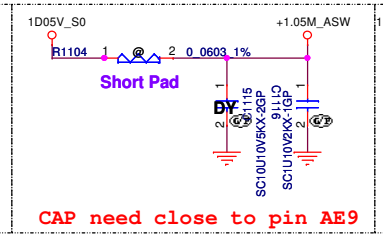
185mA



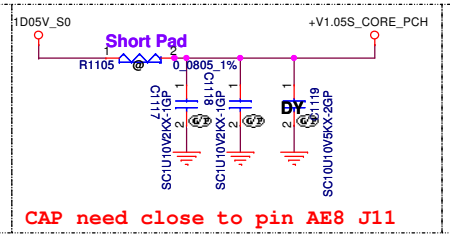
31mA



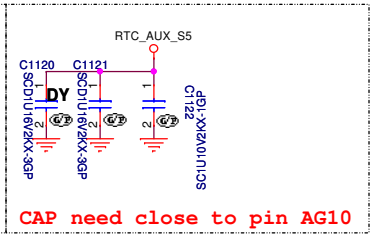
658mA



1.632A



1mA



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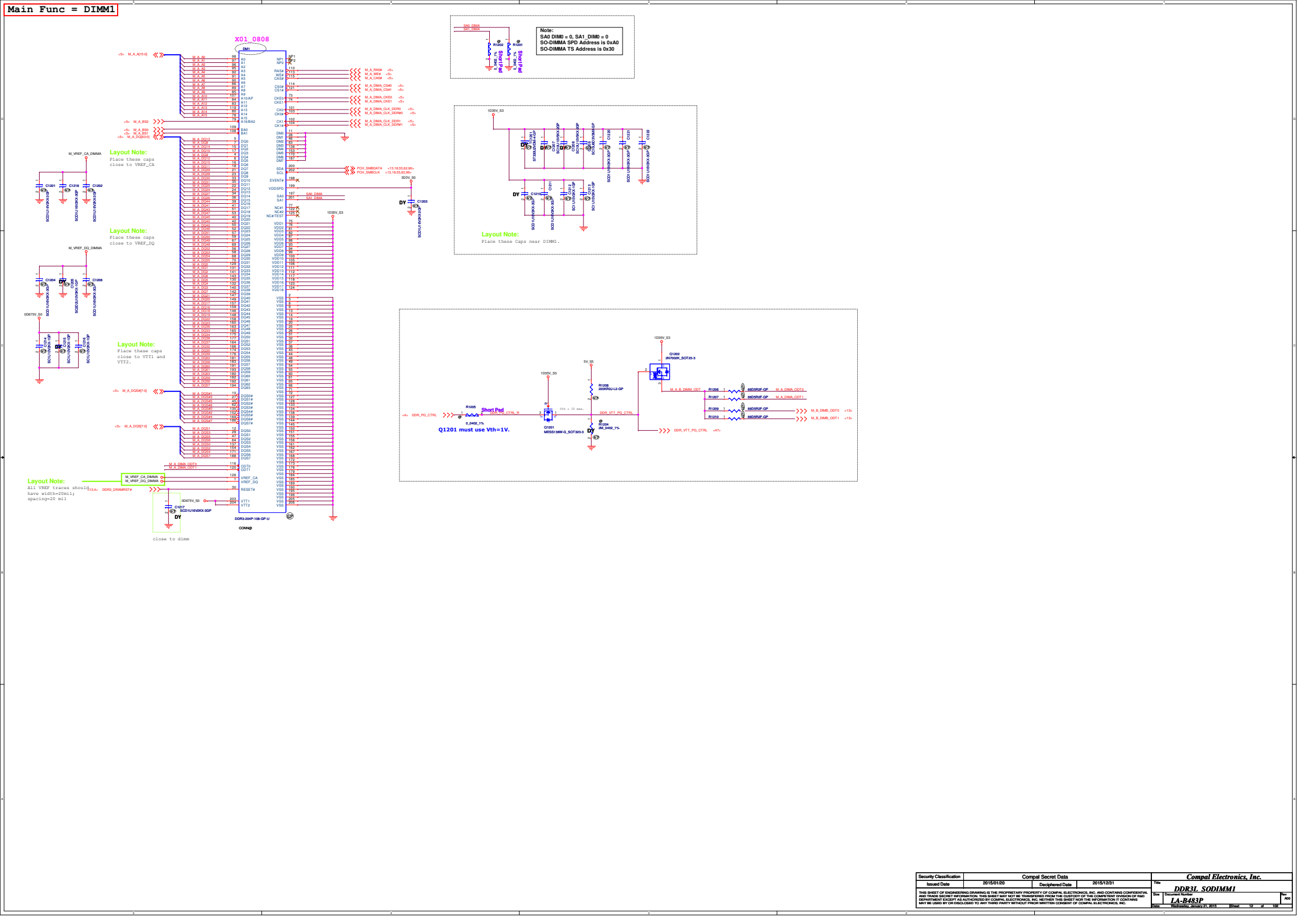
Compal Electronics, Inc.

Title: CPU (Power CAP2)

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 11 of 102

Main Func = DIMM1



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

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Compal Electronics, Inc.

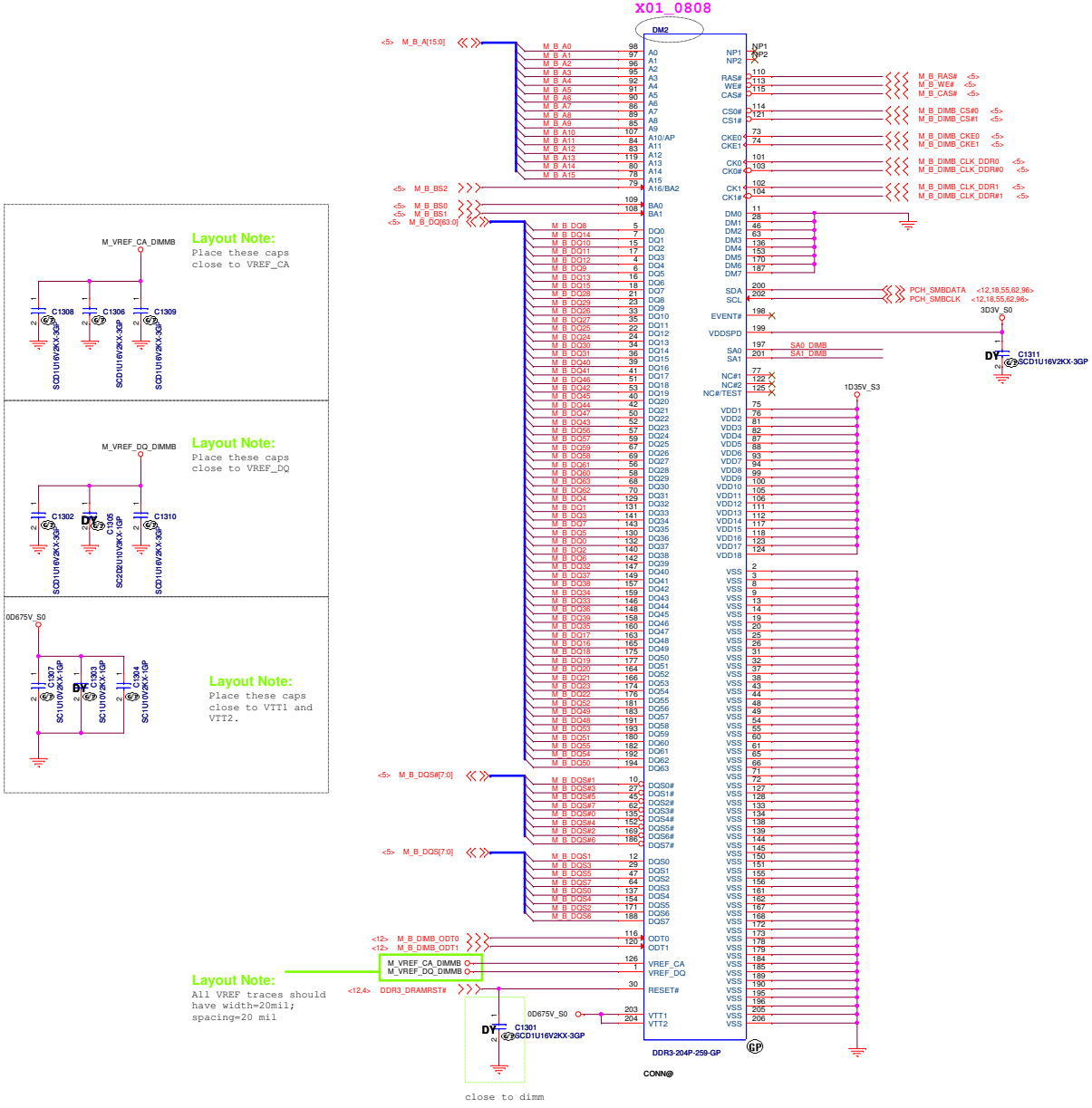
Title: DDR3L SODIMM1

Size: | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 12 of 102

Main Func = DIMM2

X01_0808

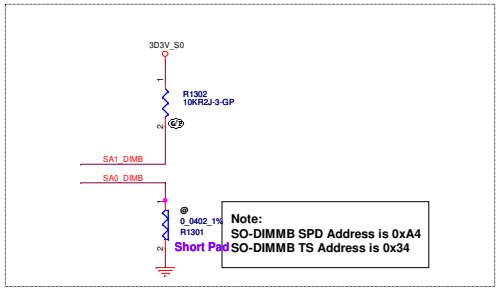


Layout Note:
Place these caps close to VREF_CA

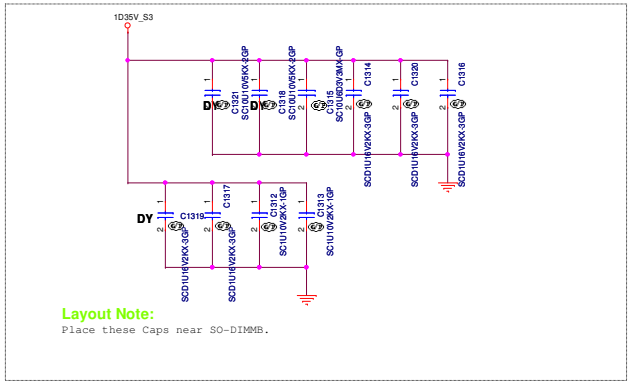
Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



Layout Note:
Place these Caps near SO-DIMMB.

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DDR3L_SODIMM2

Size: | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 13 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: (Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
	LA-B483P	A00

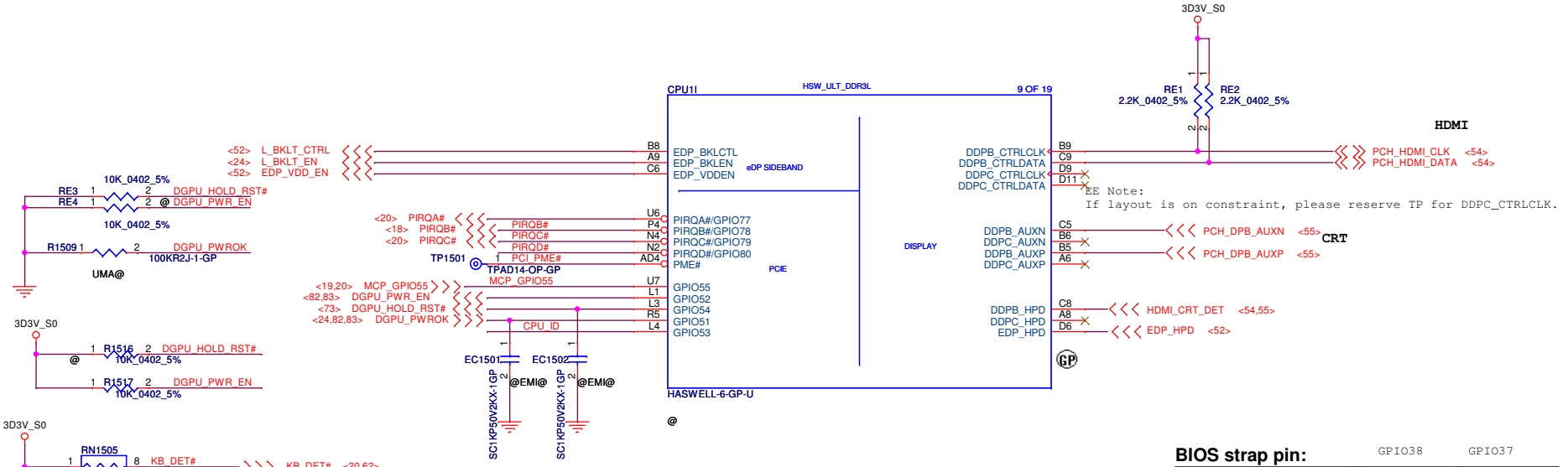
Date: Wednesday, January 21, 2015 | Sheet 14 of 102

Main Func = PCH

PCH strap pin:

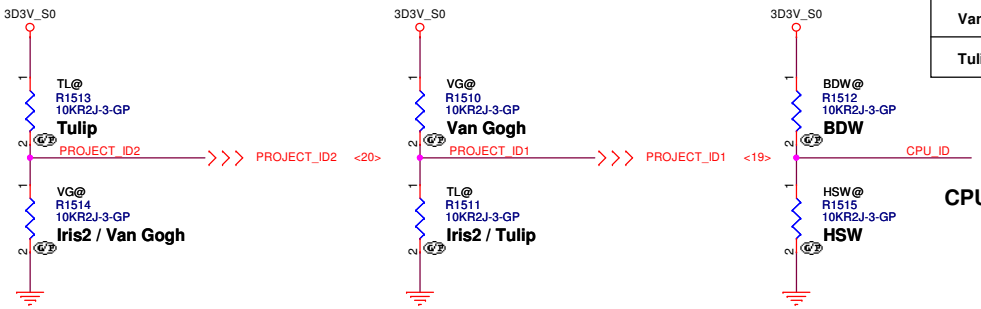
Port B Detected	
DDPB_CTRLDATA	Low = Disable Port B (default) * High = Enable Port B
DDPC_CTRLDATA	* Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts



BIOS strap pin:

BIOS VRAM Size Strap pin	GPIO38 (PROJECT_ID2)	GPIO37 (PROJECT_ID1)
Iris2	0	0
Van Gogh	0	1
Tulip	1	0



CPU detect pin

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

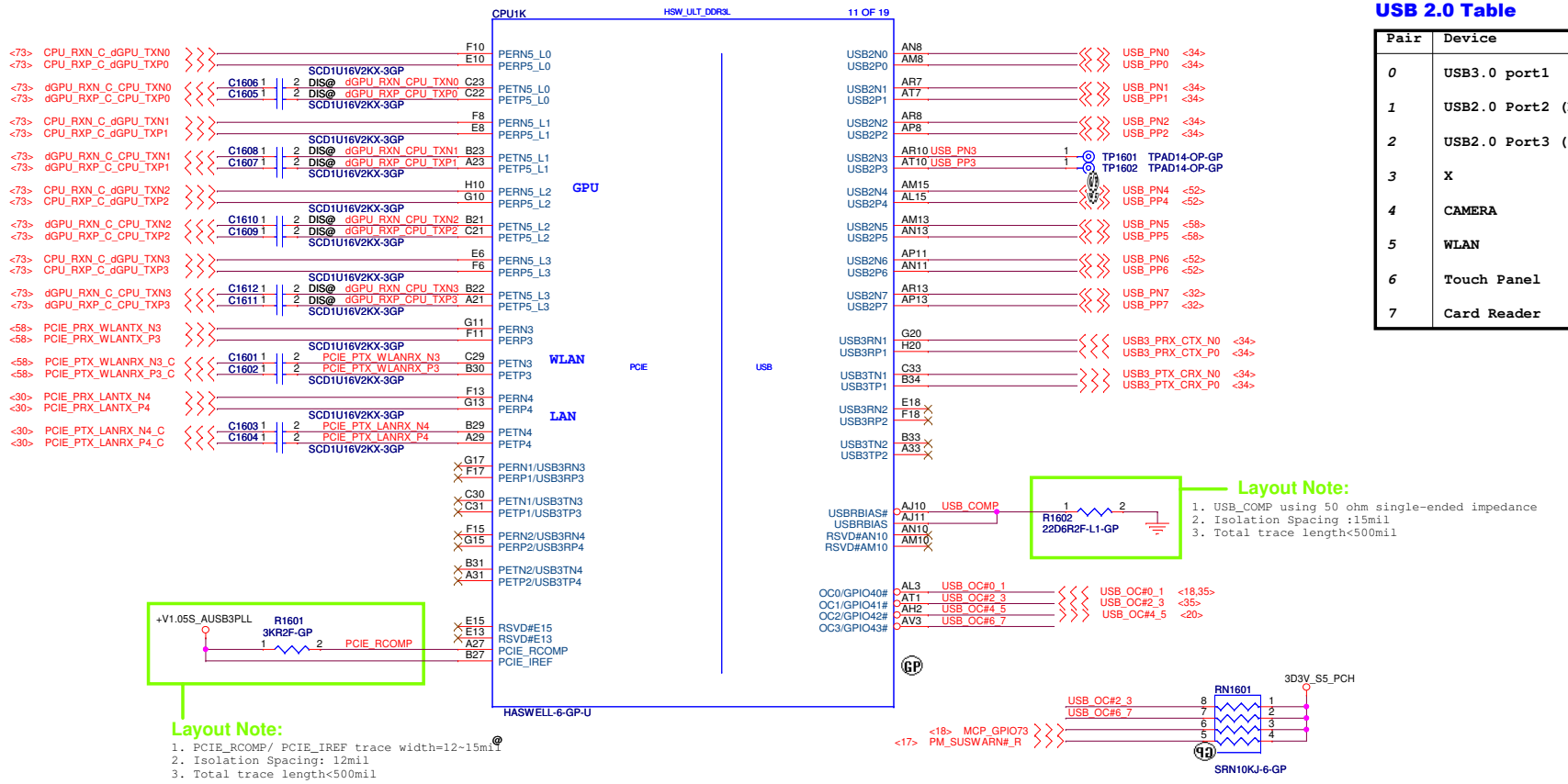
Compal Electronics, Inc.

Title: CPU (PCI/CRT/DDI)

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 15 of 102

Main Func = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0~L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3 / PCIe* Port 1 SSD	USB 3.0 Port4 / PCIe* Port 2 SSD	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	SATA 6Gb/s Port 3 / PCIe* Port 6 Lane 0 SSD	SATA 6Gb/s Port 2 / PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1 / PCIe* Port 6 Lane 2	SATA 6Gb/s Port 0 / PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3 / PCIe* Port 1 SSD	USB 3.0 Port4 / PCIe* Port 2 SSD	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/20	Deciphered Date	2015/12/31

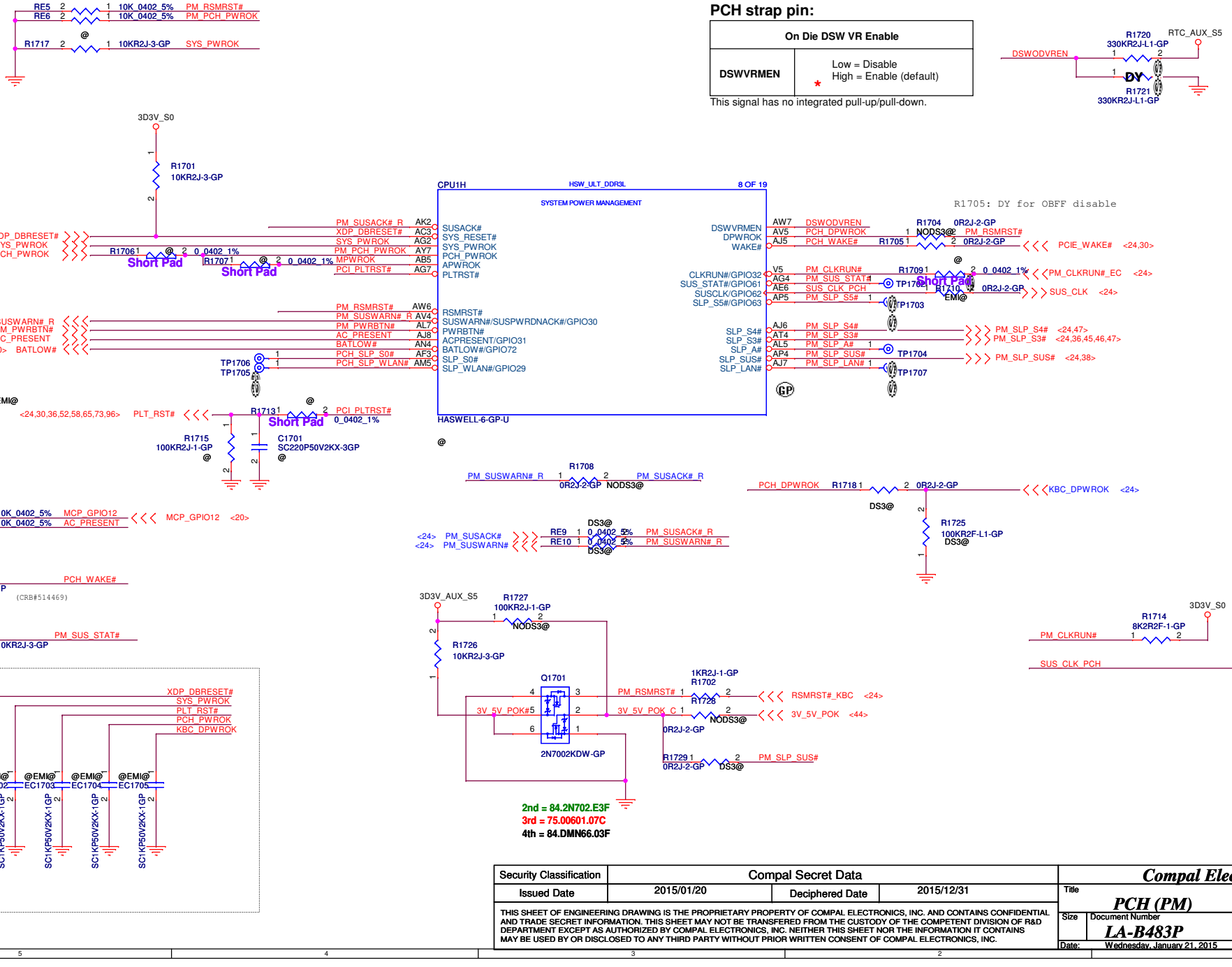
Title	PCH (PCIE/USB)		
Size	Document Number: LA-B483P		Rev: A00
Date: Wednesday, January 21, 2015	Sheet 16 of 102		

Main Func = PCH

PCH strap pin:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable High = Enable (default) *

This signal has no integrated pull-up/pull-down.



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

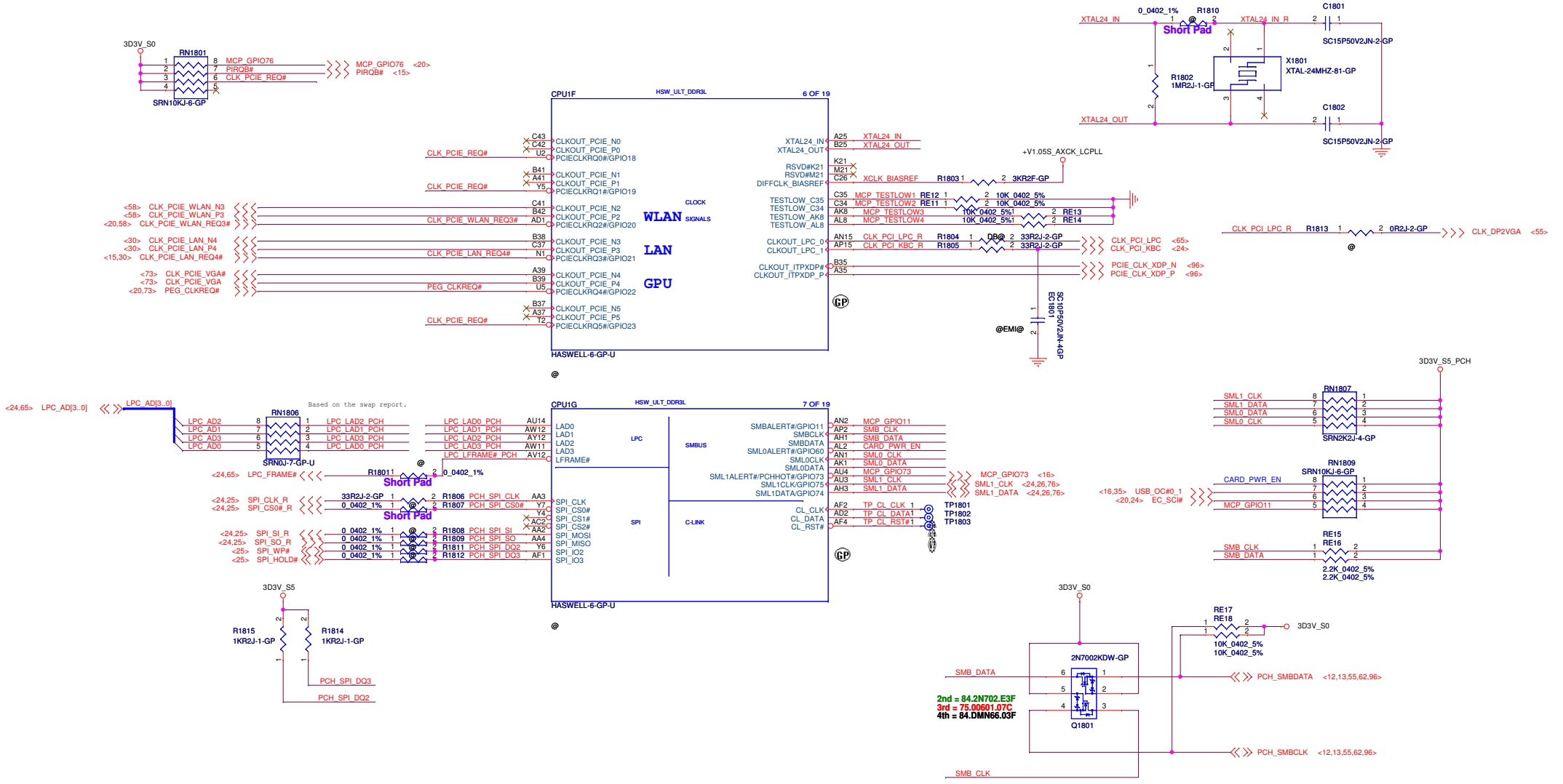
Compal Electronics, Inc.

Title: **PCH (PM)**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 17 of 102

Main Func = PCH



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 Sheet 18 of 102

Main Func = PCH

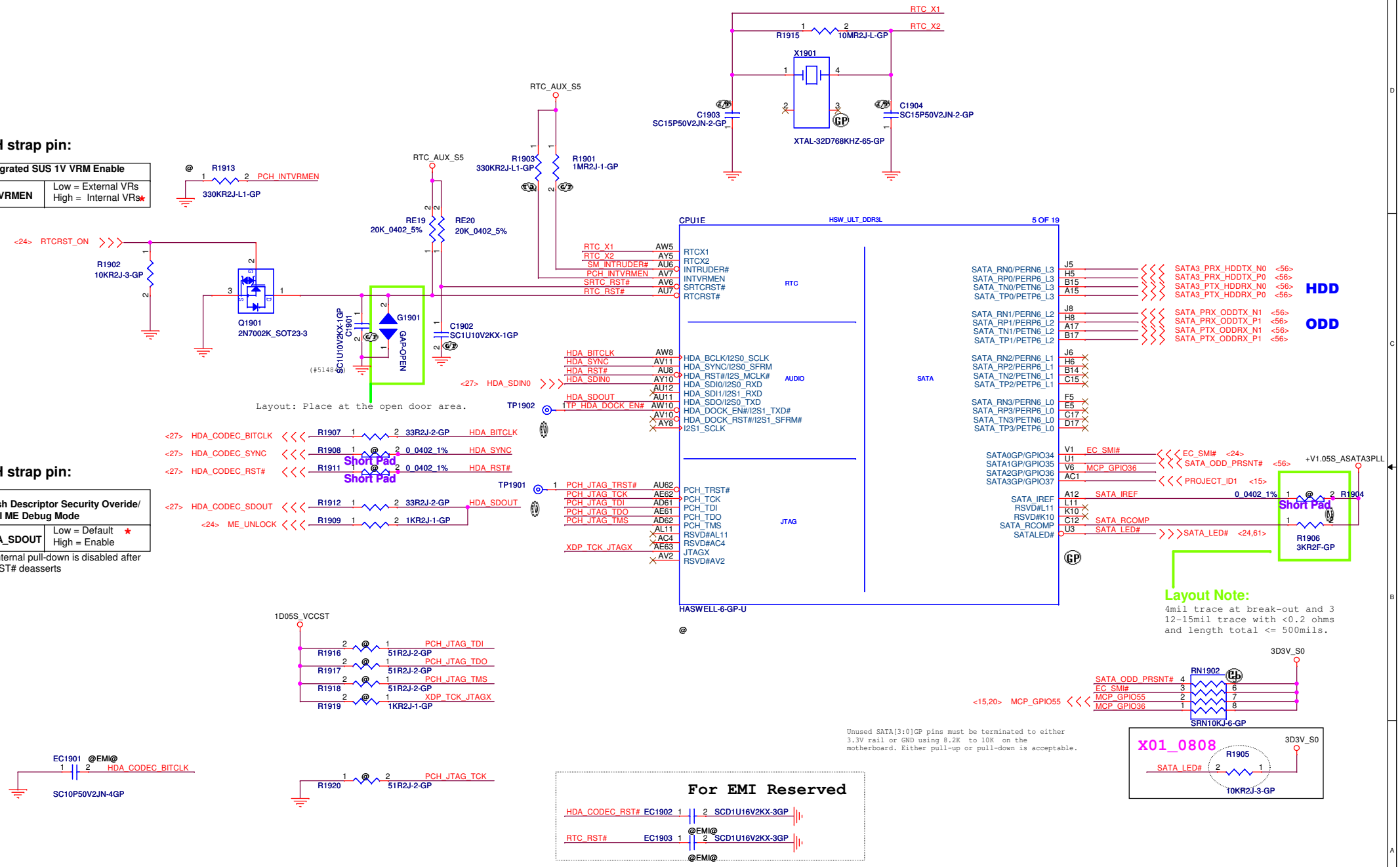
PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs★

PCH strap pin:

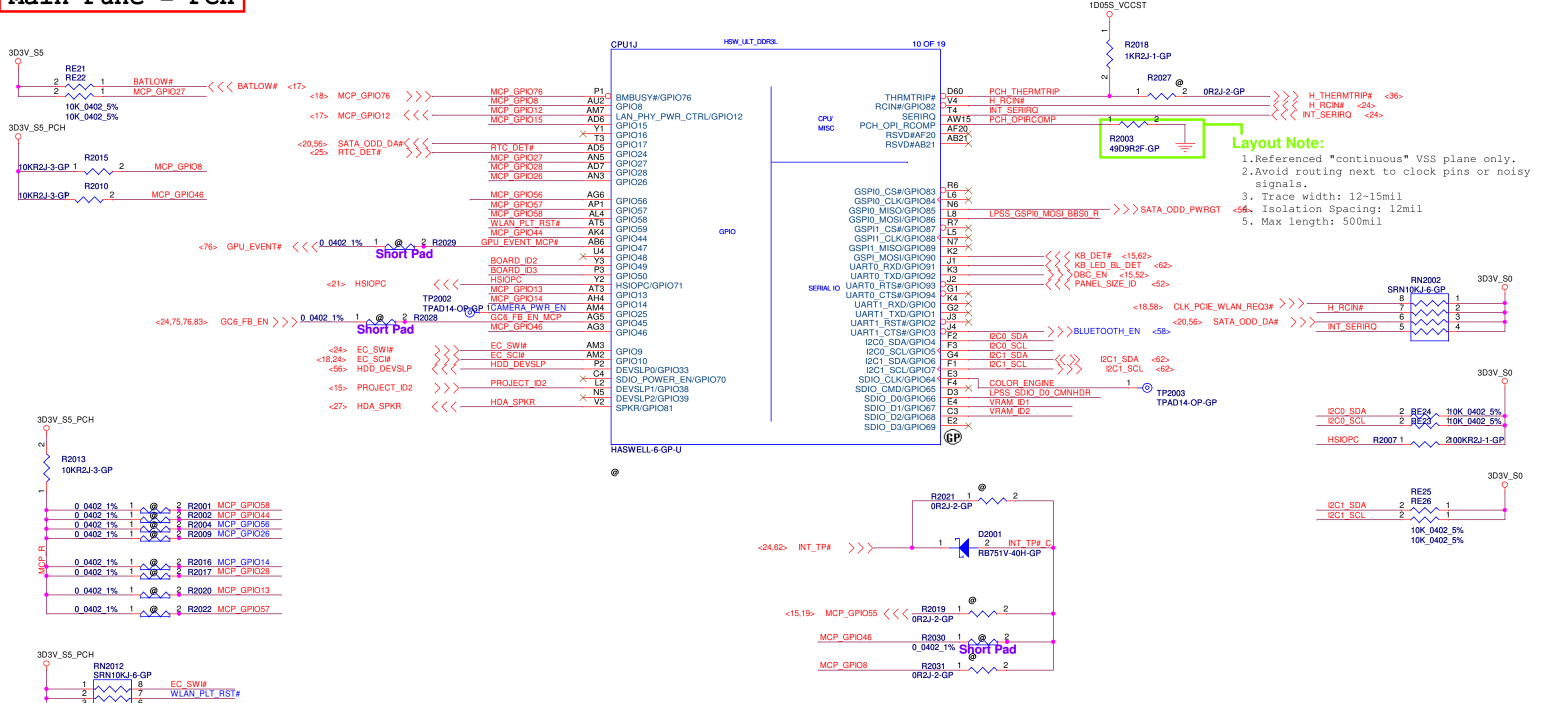
Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

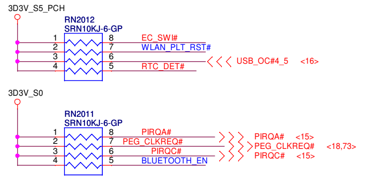
The internal pull-down is disabled after PLTRST# deasserts



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: CPU (RTC/SATA/IHDA/JTAG)			
Size	Document Number: LA-B483P		Rev: A00
Date: Wednesday, January 21, 2015	Sheet 19 of 102		

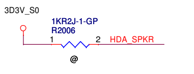




PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

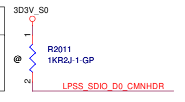
The internal pull-down is disabled after PLTRST# deasserts



PCH strap pin:

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode ★ Low = Disable "Top-Block swap" mode (Default)

The internal pull-down is disabled after PLTRST# deasserts

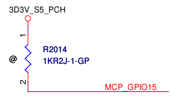


Need SW double confirm if that's needed Top-Block swap

PCH strap pin:

TLS Confidentiality	
GPIO15	★ Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

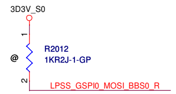
The internal pull-down is disabled after RSMRST# deasserts.



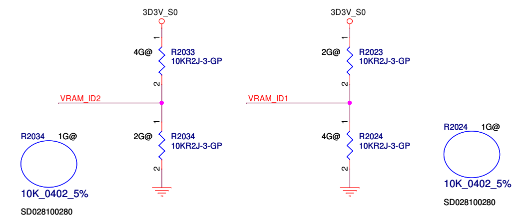
PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

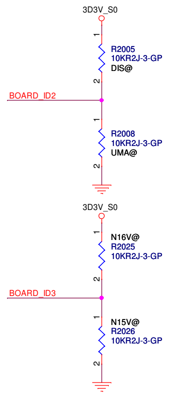


Need double confirm, GPIO table set to GPI if that's needed PH or PL



BIOS strap pin:

BIOS VRAM Size Strap pin	VRAM_ID2 (GPIO68)	VRAM_ID1 (GPIO67)
1G	0	0
2G	0	1
4G	1	0



BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM	0
N16V-GM	1

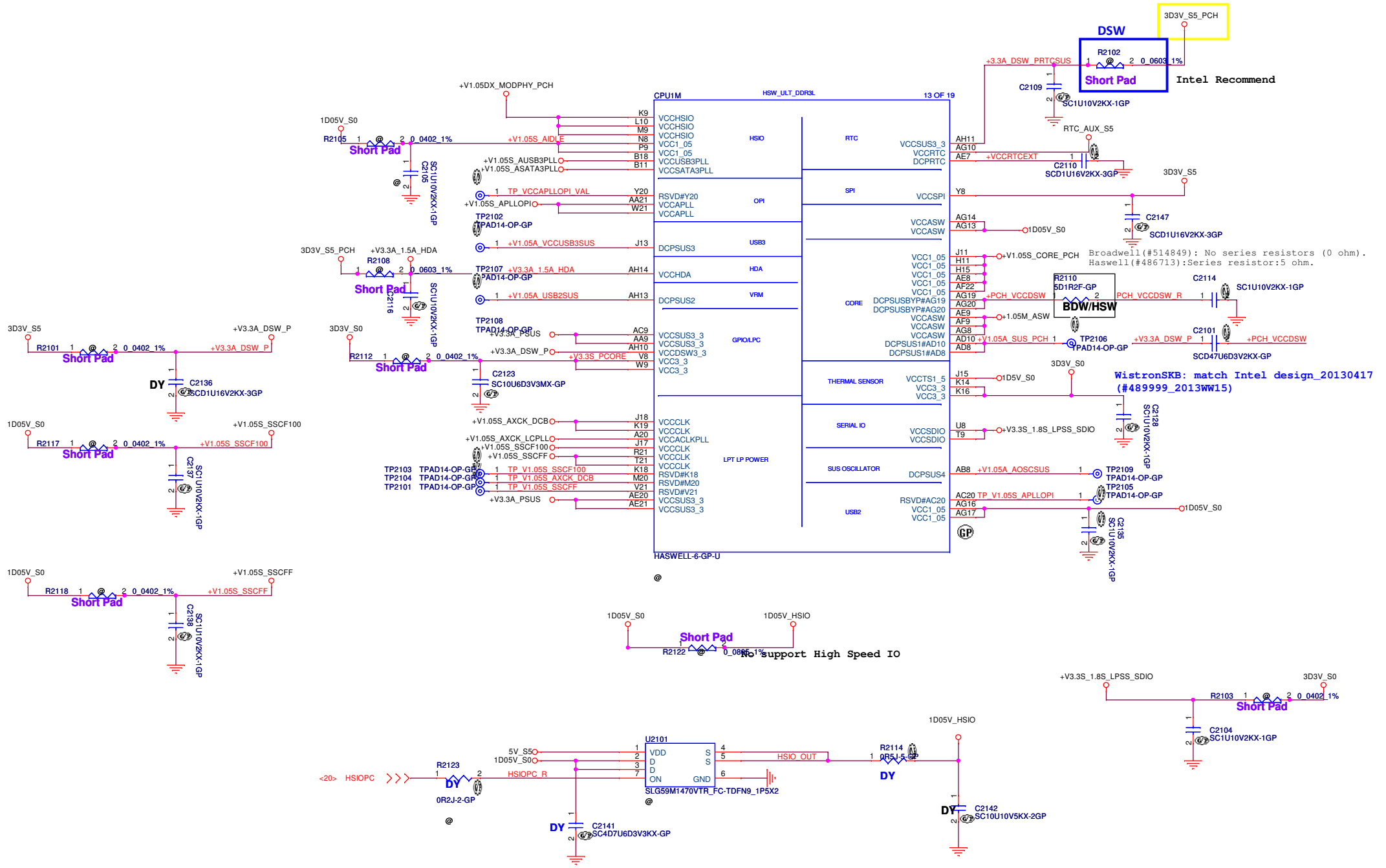
Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: CPU (GPIO/CPU)

Size | Document Number: LA-B483P | Rev: A00

Main Func = PCH



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

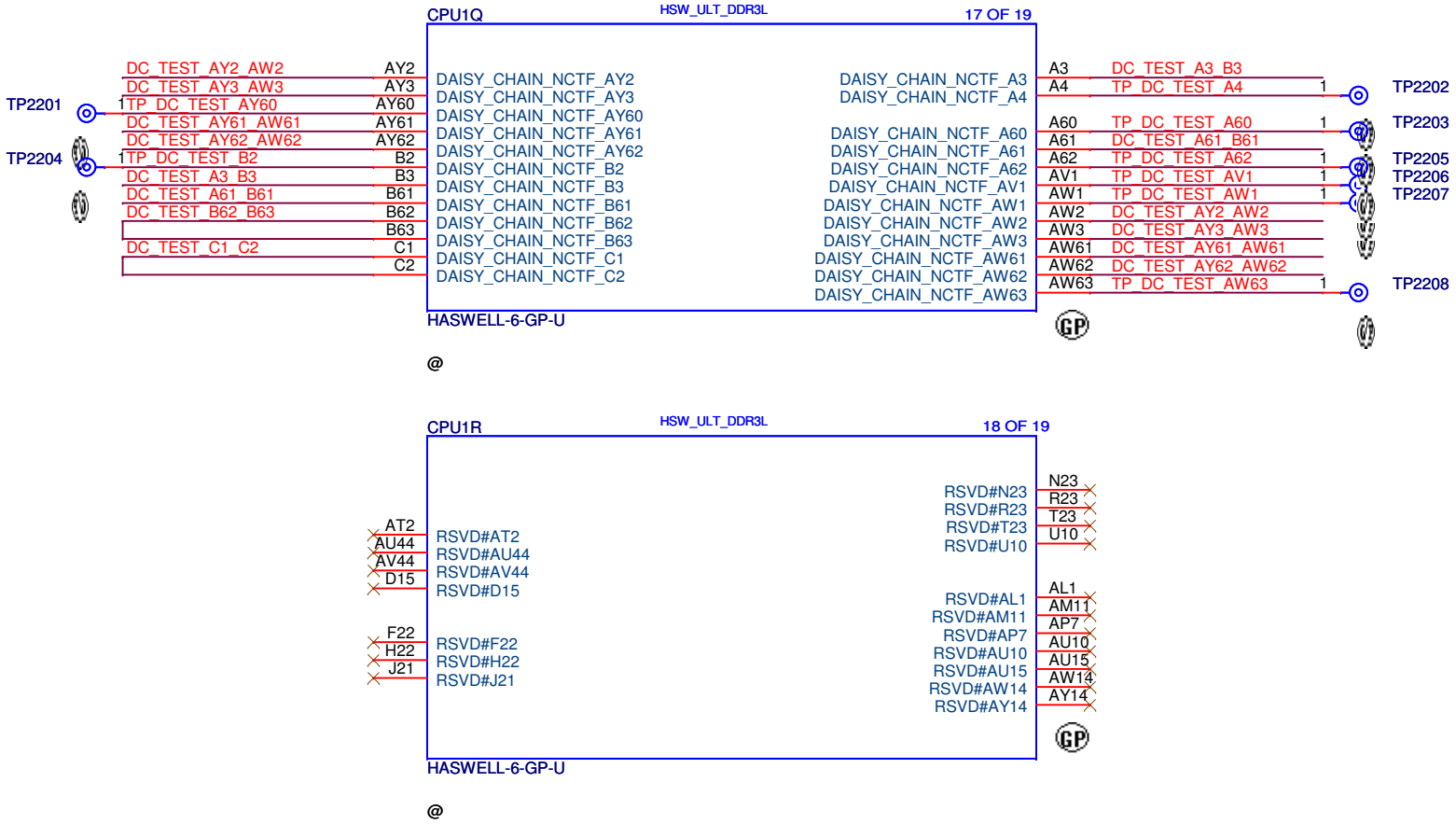
Compal Electronics, Inc.

Title: **CPU (POWER1)**

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 21 of 102

Main Func = PCH



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

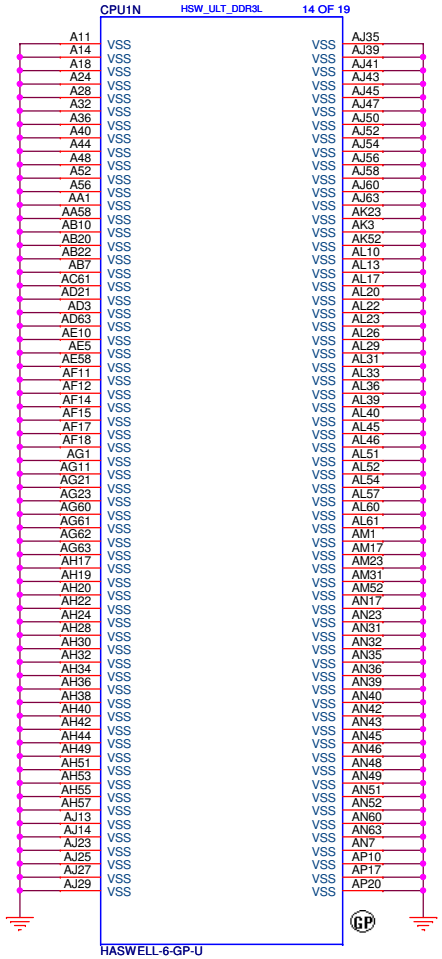
Compal Electronics, Inc.

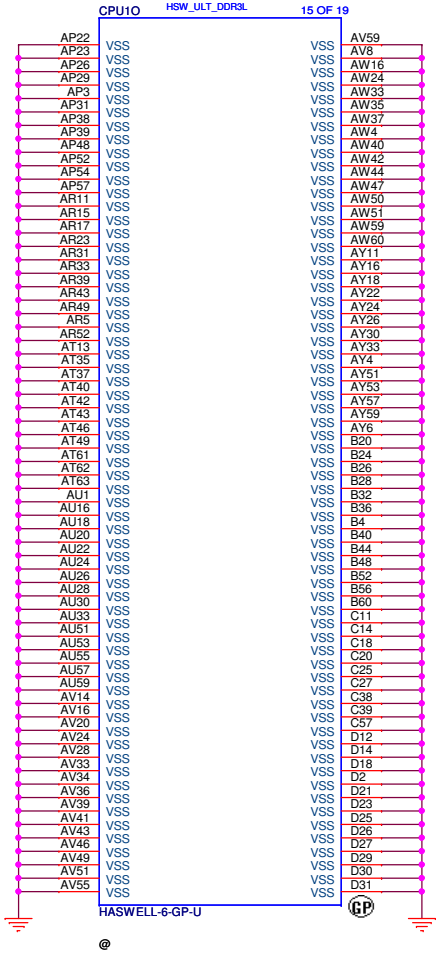
Title: **CPU (RSVD)**

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 Sheet 22 of 102

Main Func = PCH





Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **CPU(VSS)**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 23 of 102

Main Func = KBC

PCB VERSION AD(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K	3.0V
X00 (SB)	100.0K	20.0K	2.75V
X01 (SC)	100.0K	33.0K	2.48V
X02 (SD)	100.0K	47.0K	2.24V
A00 (E)	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.35SV
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Yan Gosh-HSW-OPS	100.0K	10.0K(64.10025.6D1)	3.0V
Yan Gosh-HSW-UMA	100.0K	13.7K(64.13725.6D1)	2.902V
Yan Gosh-BDW-OPS	100.0K	17.8K(64.17825.6D1)	2.801V
Yan Gosh-BDW-UMA	100.0K	23.1K(64.23125.6D1)	2.702V
TBD	100.0K	27.0K(64.27025.6D1)	2.598V
TBD	100.0K	32.4K(64.32425.6D1)	2.492V
TBD	100.0K	37.4K(64.37425.6D1)	2.402V
TBD	100.0K	43.2K(64.43225.6D1)	2.304V
TBD	100.0K	49.9K(64.49925.6D1)	2.201V
Tela-3-HSW-OPS	100.0K	57.6K(64.57625.6D1)	2.053V
Tela-3-HSW-UMA	100.0K	64.9K(64.64925.6D1)	2.001V
Tela-3-BDW-OPS	100.0K	73.2K(64.73225.6D1)	1.902V
Tela-3-BDW-UMA	100.0K	82.5K(64.82525.6D1)	1.808V
TBD	100.0K	93.1K(64.93125.6D1)	1.700V
TBD	100.0K	107K(64.10725.6D1)	1.594V
TBD	100.0K	130K(64.12035.6D1)	1.499V
Tulip-HSW-OPS	100.0K	137K(64.13735.6D1)	1.392V
Tulip-HSW-UMA	100.0K	154K(64.15435.6D1)	1.298V
Tulip-BDW-OPS	100.0K	200K(64.20035.6D1)	1.099V
Tulip-BDW-UMA	100.0K	232K(64.23236.6D1)	0.994V

Layout Note:
Need very close to EC

ALL_SYS_PWRGD assert, delay 10ms; PCH_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from PCH

KBC24 change to B2 version : 071.00285.0A0G

EC_GPIO47 High Active

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

Power Switch Logic(PSL)

Layout Note:
Need very close to EC

Security Classification	Compal Secret Data
Issued Date	2015/01/20
Deciphered Date	2015/12/31

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Compal Electronics, Inc.

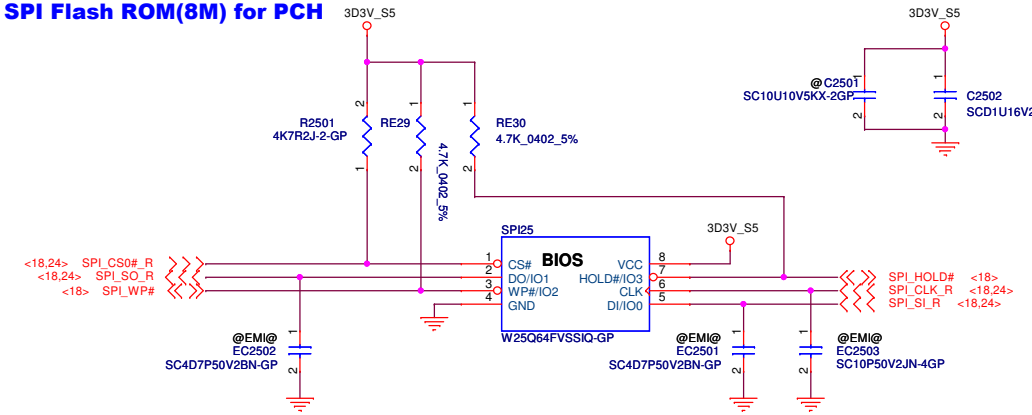
Title: KBC Nuvoton NPCE285PA0DX

Size: Document Number: LA-B483P Rev: A00

Date: Wednesday, January 21, 2015 Sheet 24 of 102

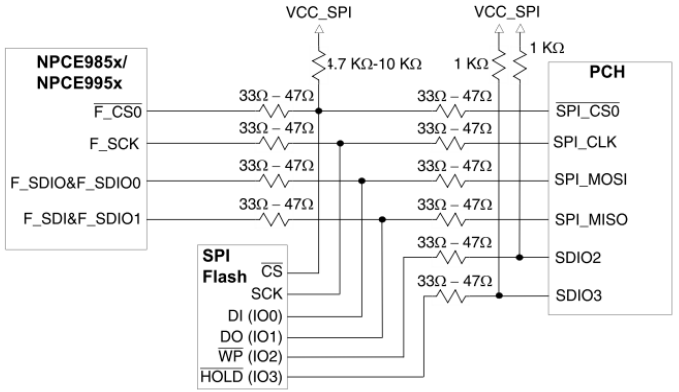
Main Func = SPI Flash

SPI Flash ROM(8M) for PCH



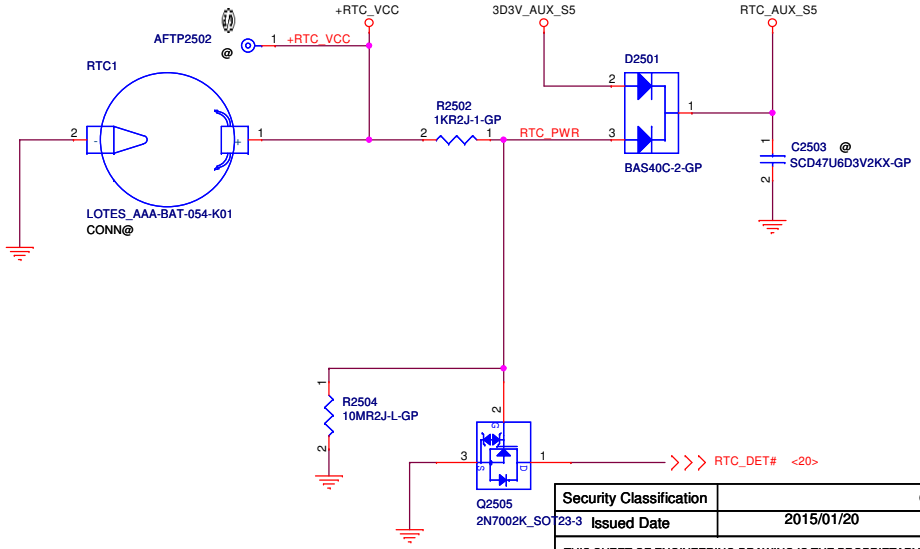
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O
072.25B64.0001	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

Main Func = RTC



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

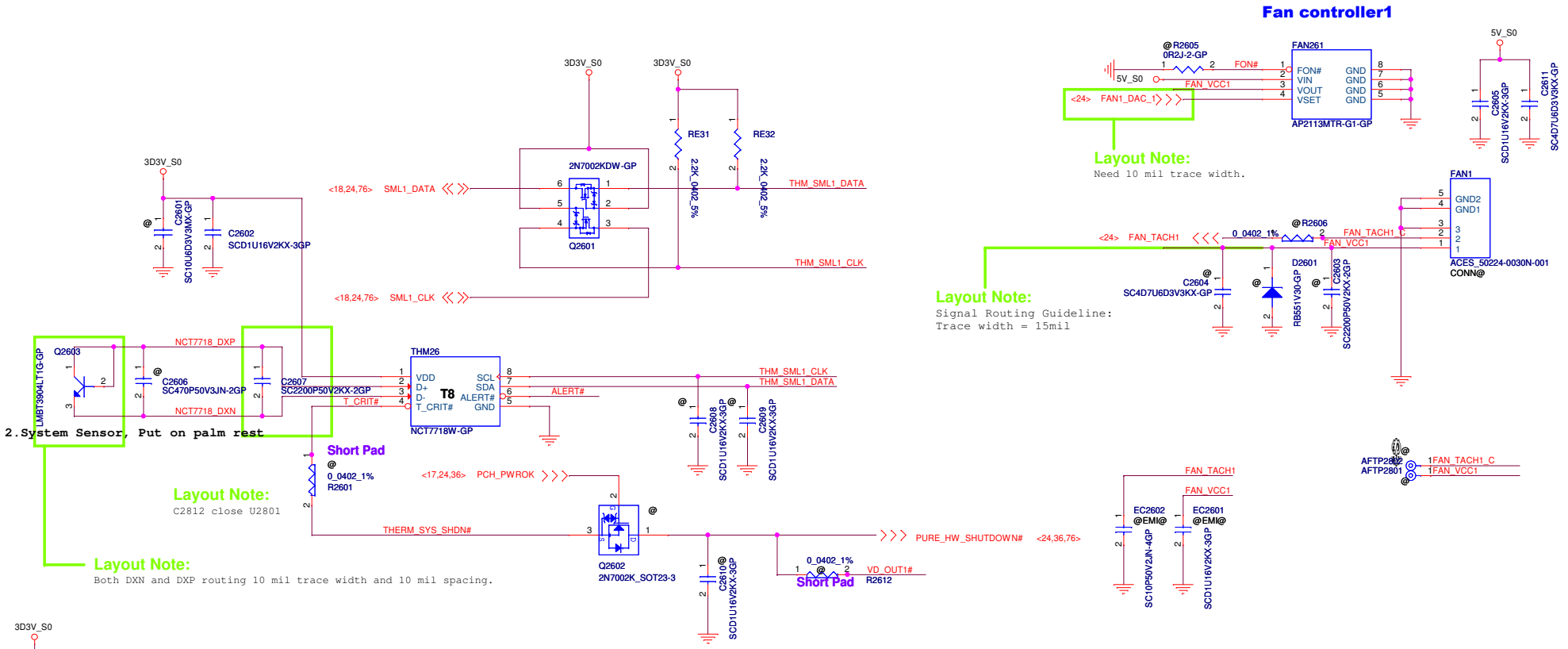
Compal Electronics, Inc.

Title: Flash/RTC

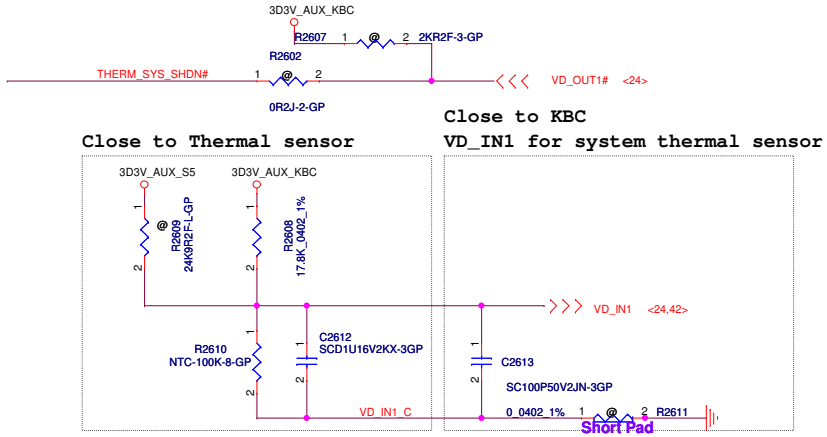
Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 25 of 102

Main Func = Thermal Sensor



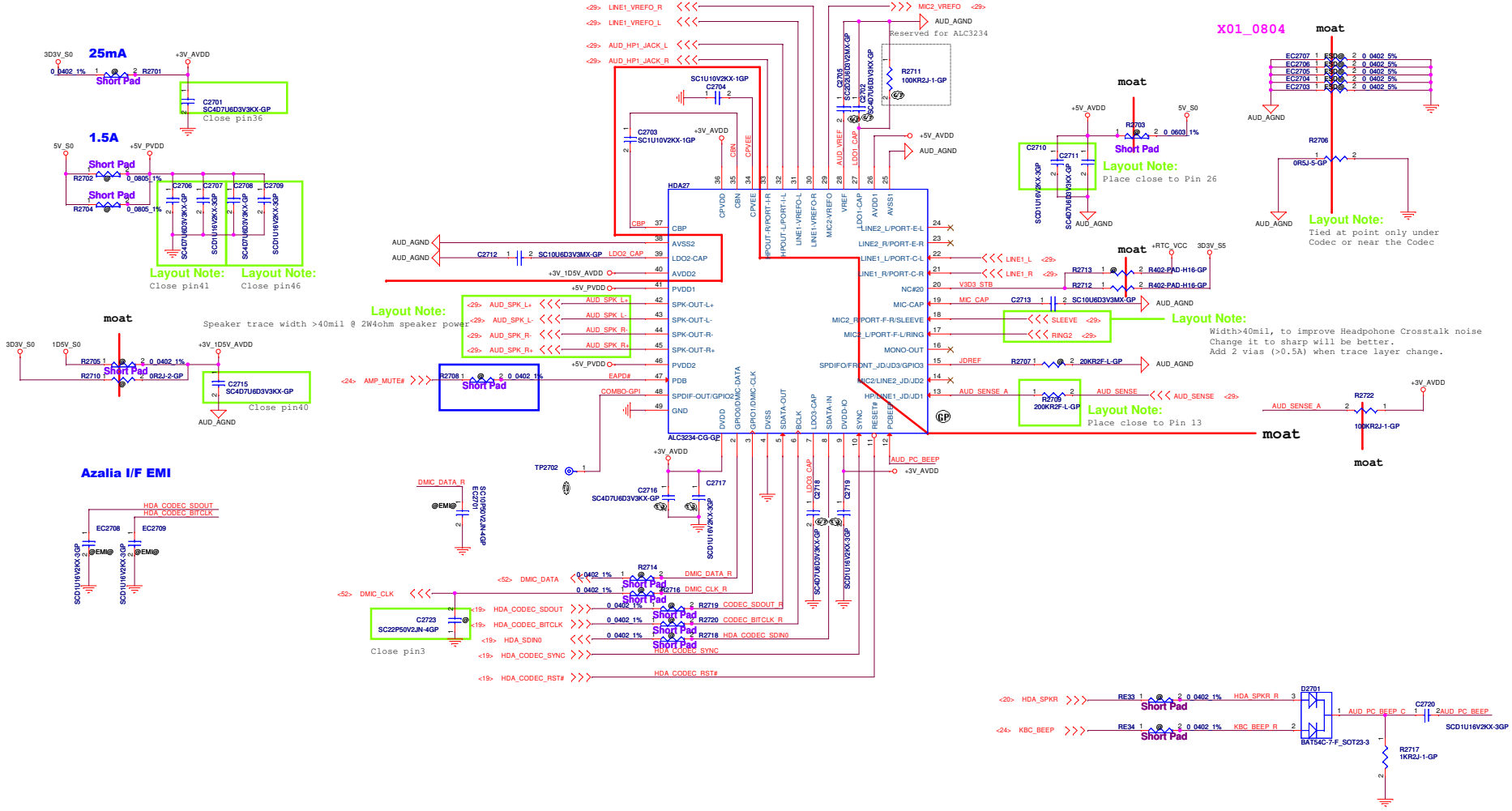
TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: THERMAL NCT7718W/Fan			
Size	Document Number: LA-B483P		Rev: A00
Date: Wednesday, January 21, 2015	Sheet 26 of 102		

Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.	
Title	Audio Codec ALC3234
Size	Document Number: LA-B483P
Rev	A00
Date: Wednesday, January 21, 2015	Sheet 27 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

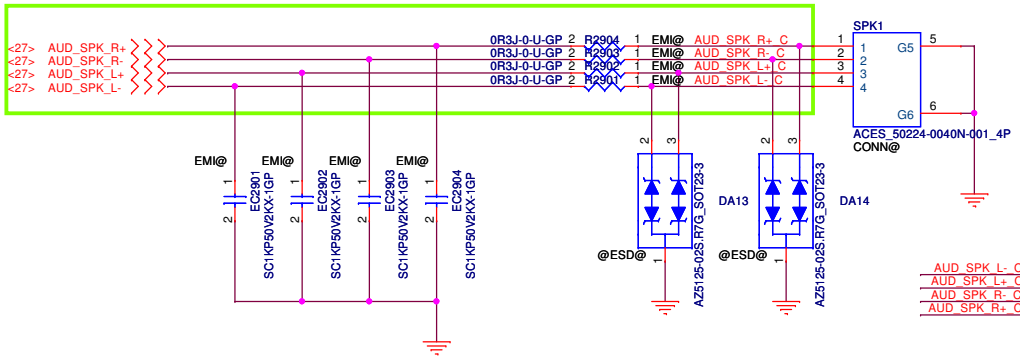
Title: **Reserved**

Size: LA	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 28 of 102	

Main Func = Audio

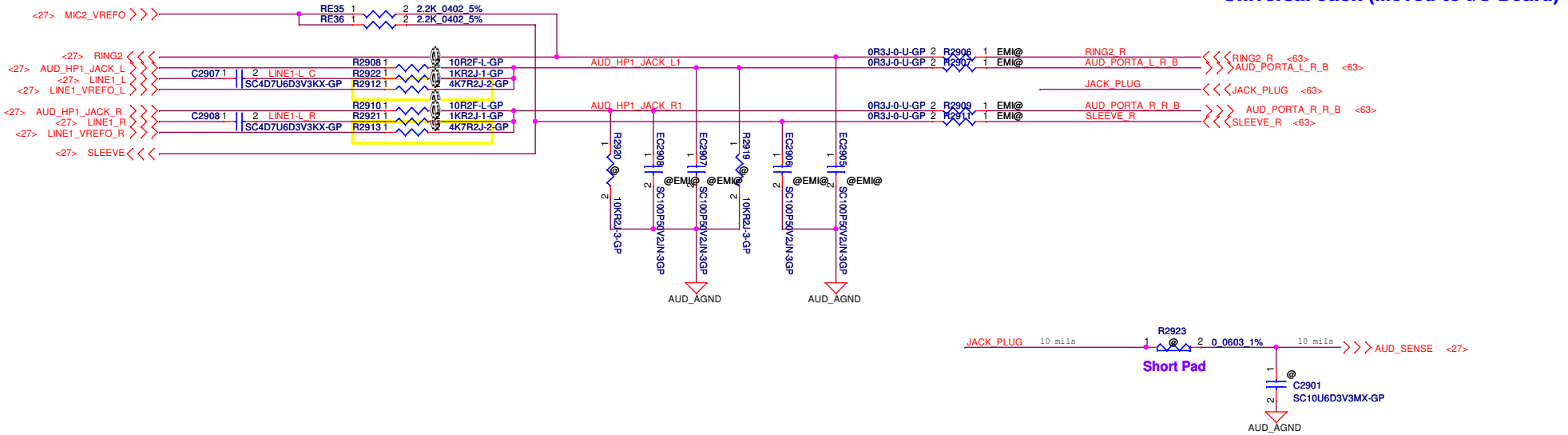
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)



Compal Electronics, Inc.

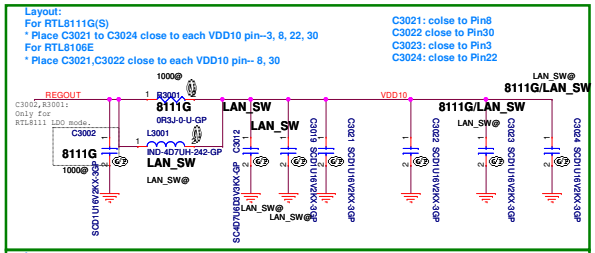
Title: SPEAKER/AUDIO JACK

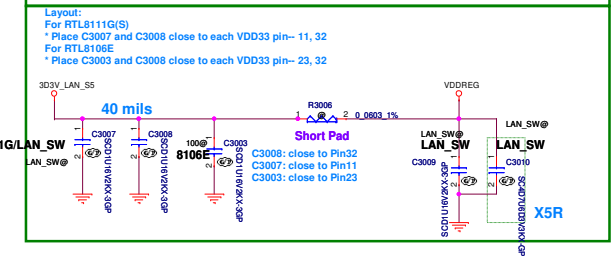
Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 29 of 102

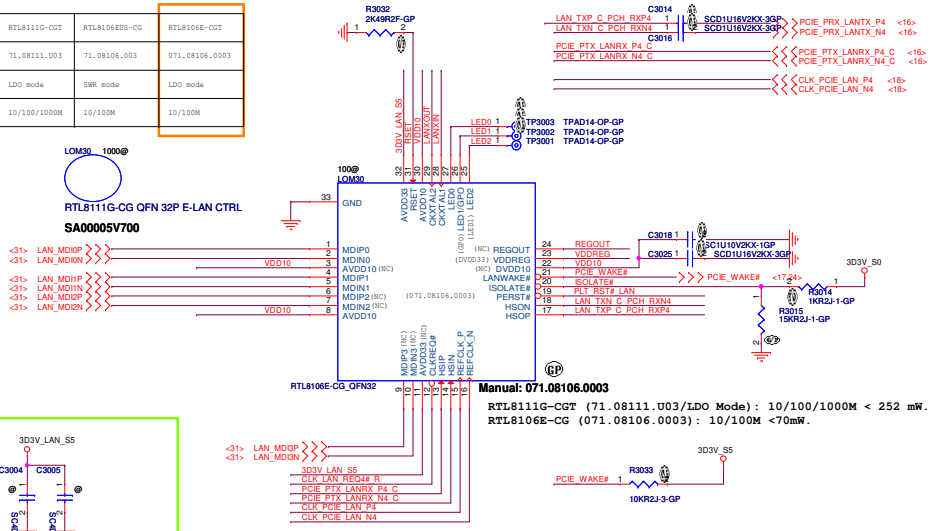
Main Func = LAN

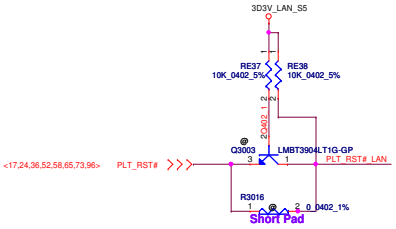
LAN CHIP (10/100/1000M & 10/100M co-lay)

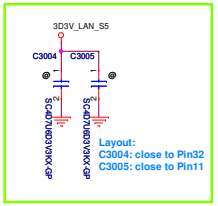




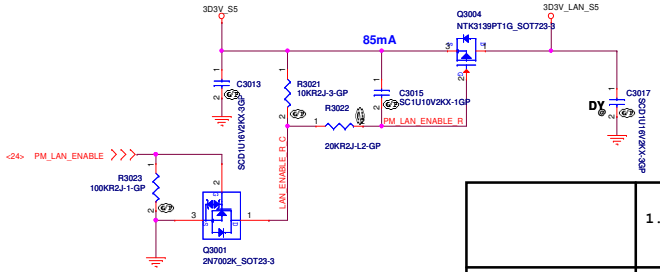
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CGT
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

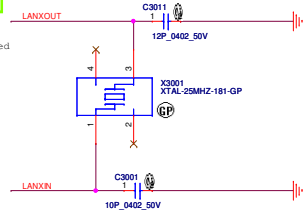


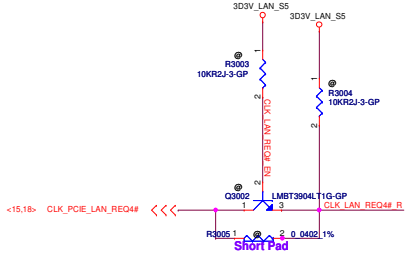




3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.







	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	O

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

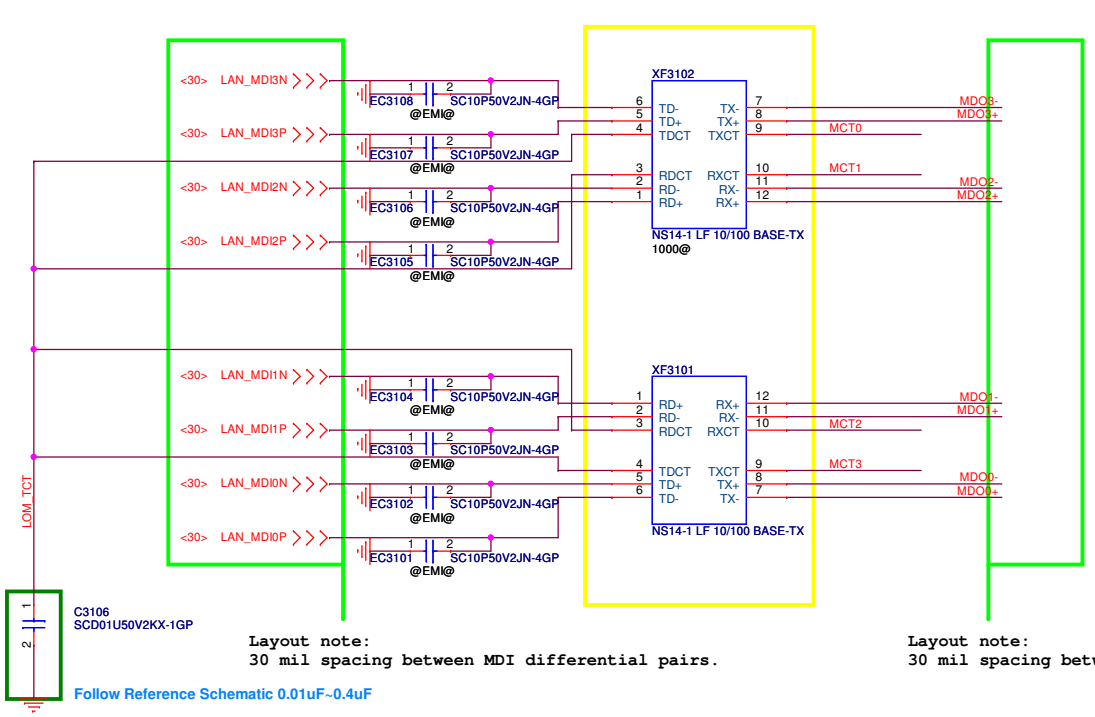
Title: LAN RTL8106

Size | Document Number: LA-B483P | Rev: A00

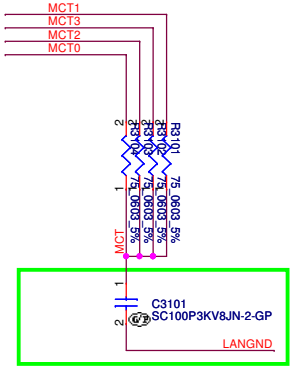
Date: Wednesday, January 21, 2015 | Sheet 30 of 102

Main Func = LAN

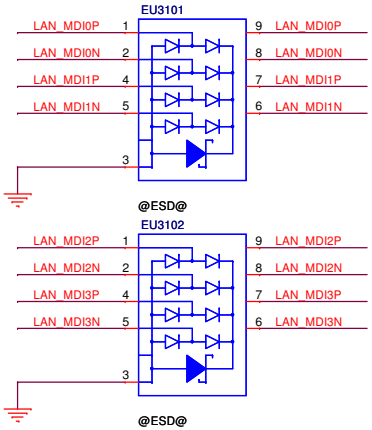
LAN TransFormer (10/100/1000M & 10/100M co-lay)

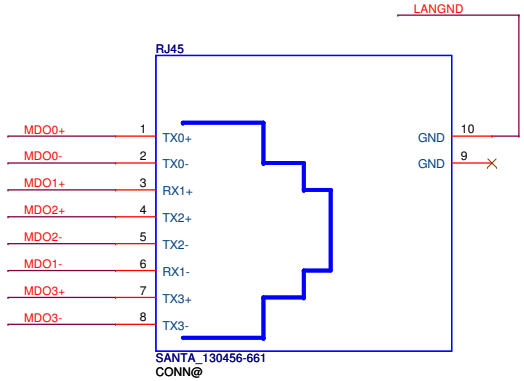


Layout note:
30 mil spacing between MDI differential pairs.



Layout note:
30 mil spacing between MDI differential pairs.



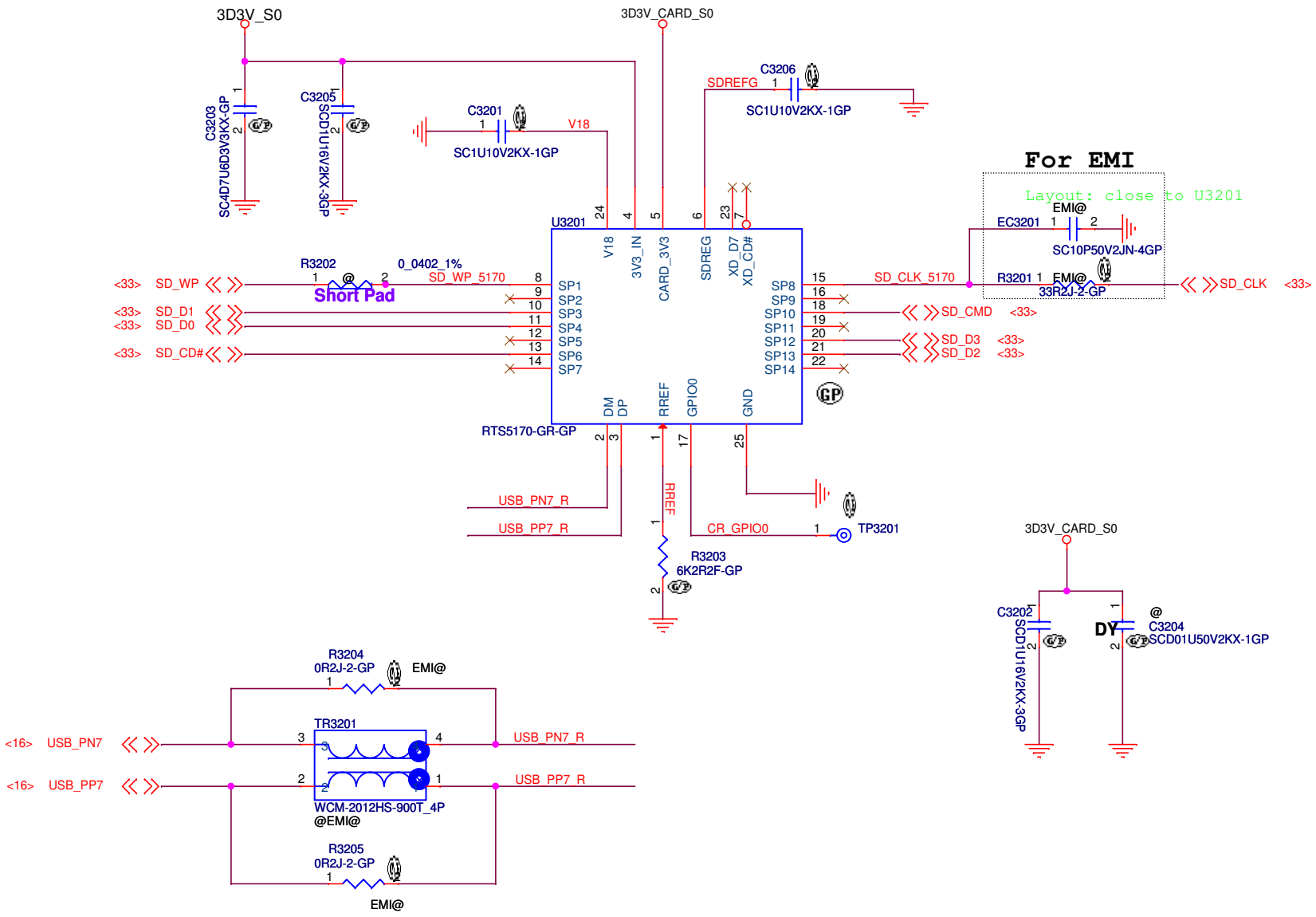


Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: XFOM&RJ45			
Size	Document Number: LA-B483P		Rev: A00
Date: Wednesday, January 21, 2015	Sheet 31 of 102		

Main Func = Card Reader

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/20	Deciphered Date	2015/12/31

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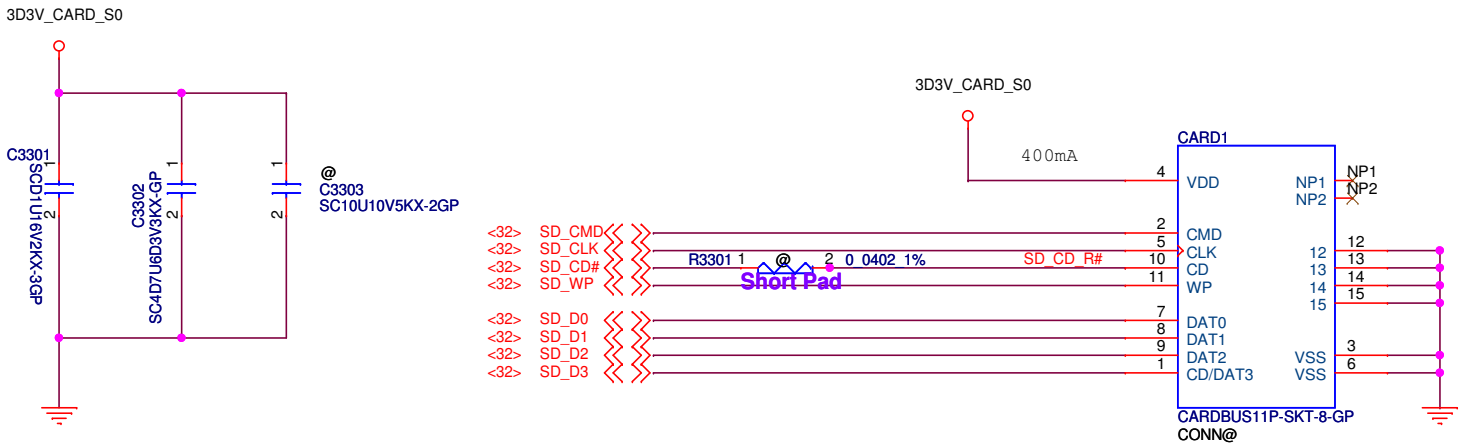
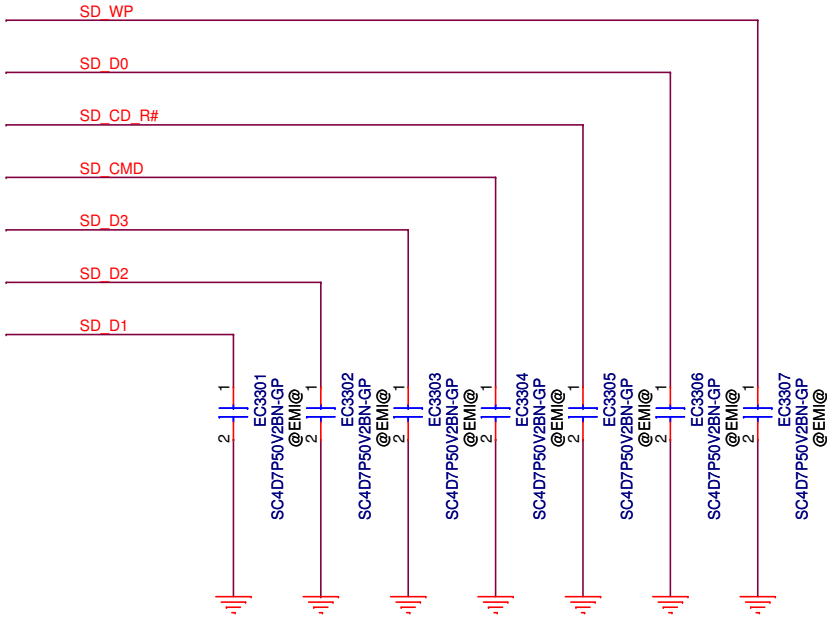
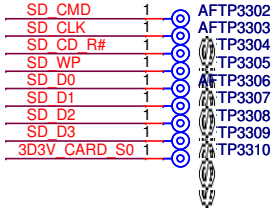
Title	Card Reader-RTS5170		
Size	Document Number		Rev
	LA-B483P		A00
Date:	Wednesday, January 21, 2015	Sheet	32 of 102

Main Func = Card Reader



For EMI Reserved





Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

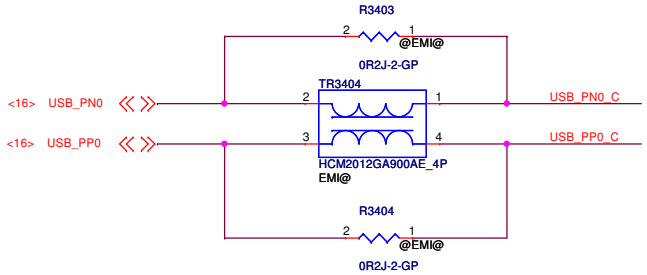
Title: **Card Reader-RTS5170**

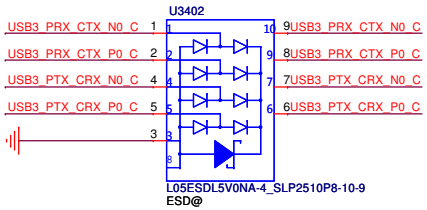
Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 33 of 102

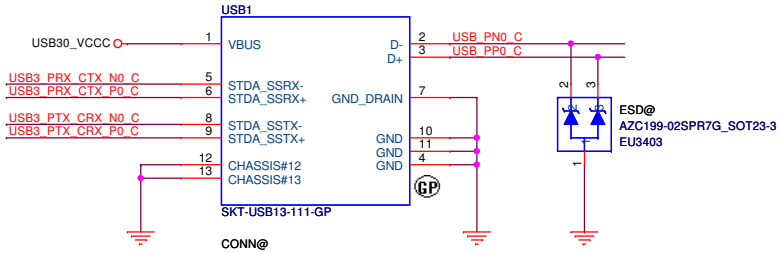
Main Func = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

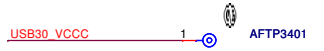


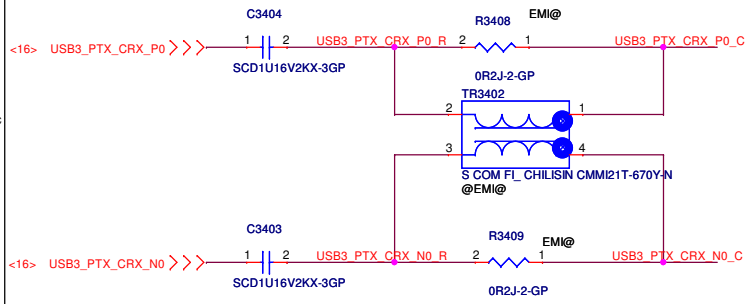


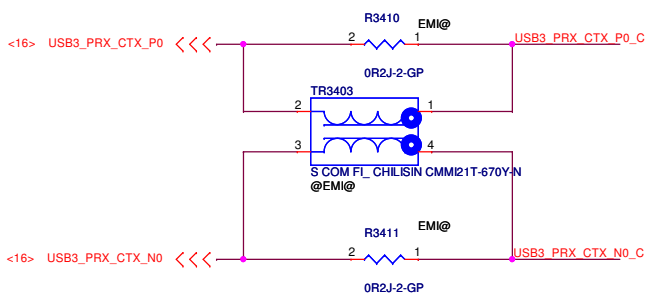
USB3.0 Port1



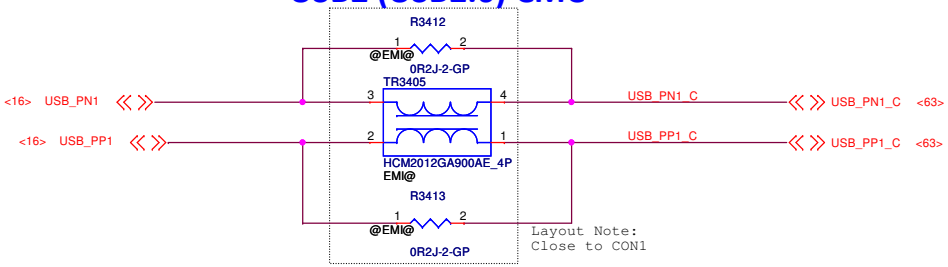
USB2.0/3.0 filter use SM070003Q00



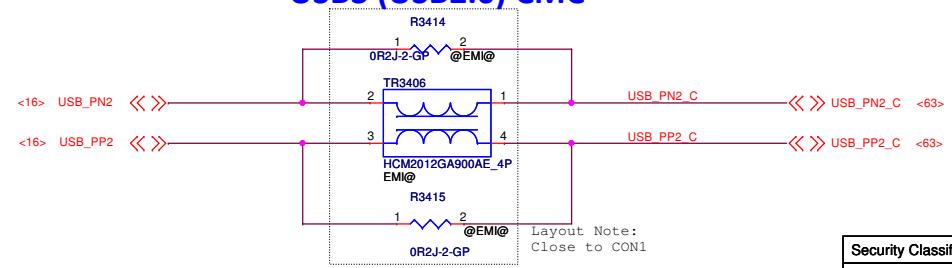




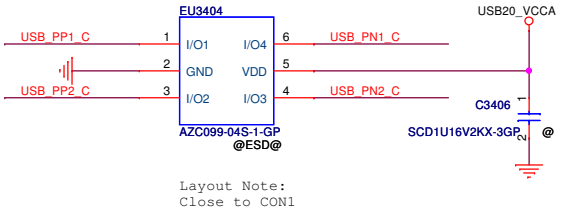
USB2 (USB2.0) CMC



USB3 (USB2.0) CMC



USB ESD Diode



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

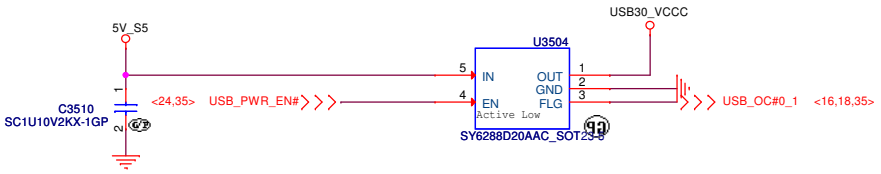
Compal Electronics, Inc.

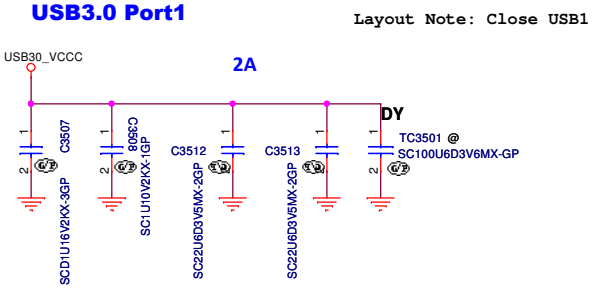
Title: USB3.0 CONN

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 Sheet 34 of 102

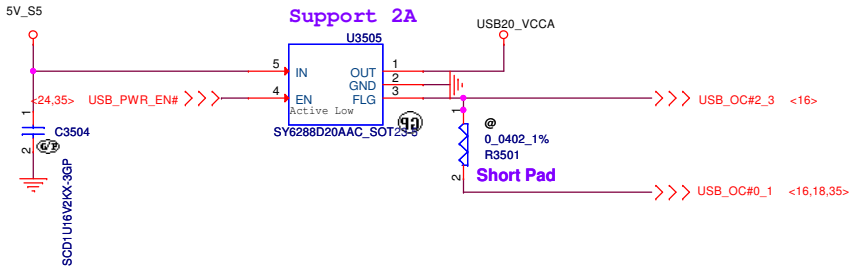
Main Func = USB3.0 Port1

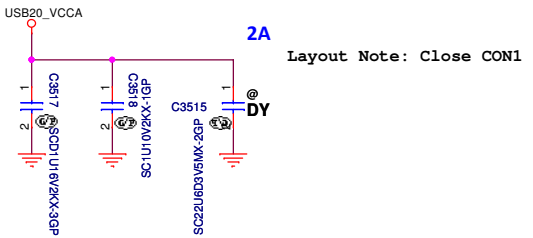




Main Func = USB2.0 Port2

Main Func = USB2.0 Port3





Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: *USB Power SW*

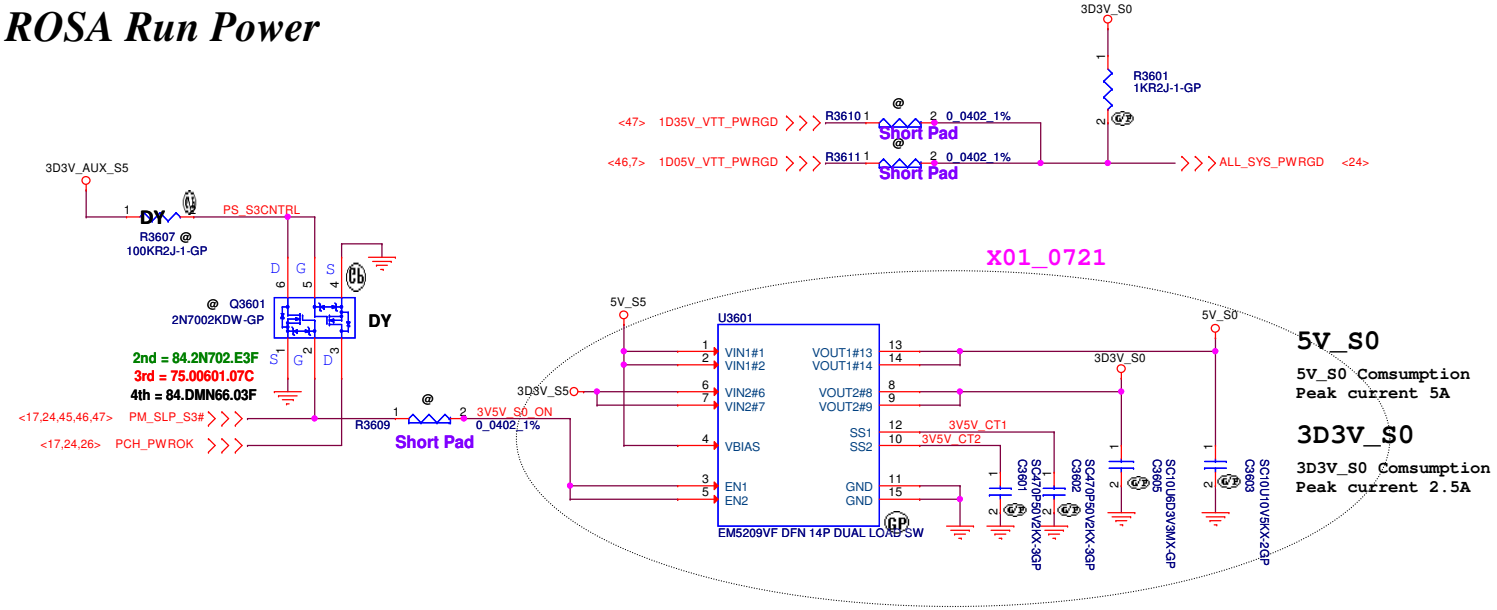
Size | Document Number: *LA-B483P* | Rev: A00

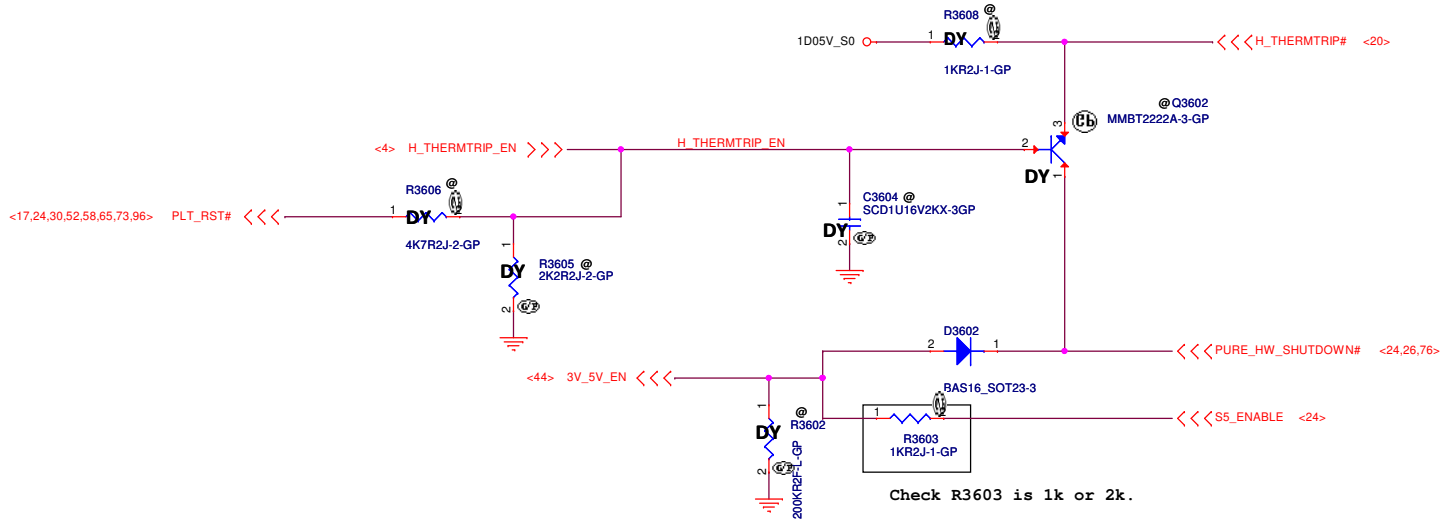
Date: Wednesday, January 21, 2015 | Sheet 35 of 102

Main Func = Power Plane & Sequence

Power Good

ROSA Run Power





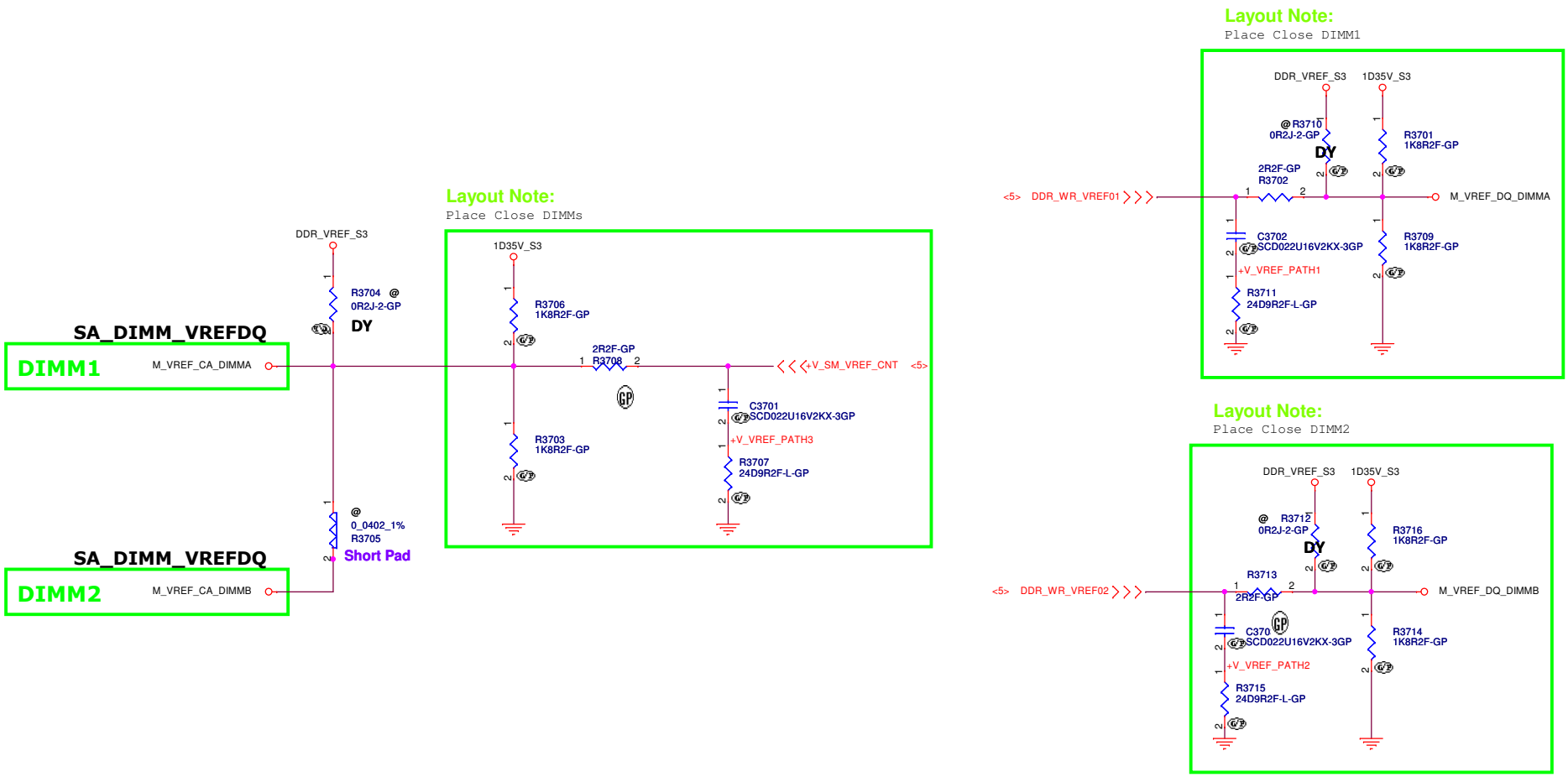
Compal Electronics, Inc.

Title: Power Plane Enable

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 36 of 102

Main Func = DIMM1
Main Func = DIMM2



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

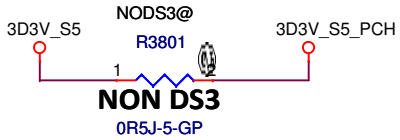
Compal Electronics, Inc.

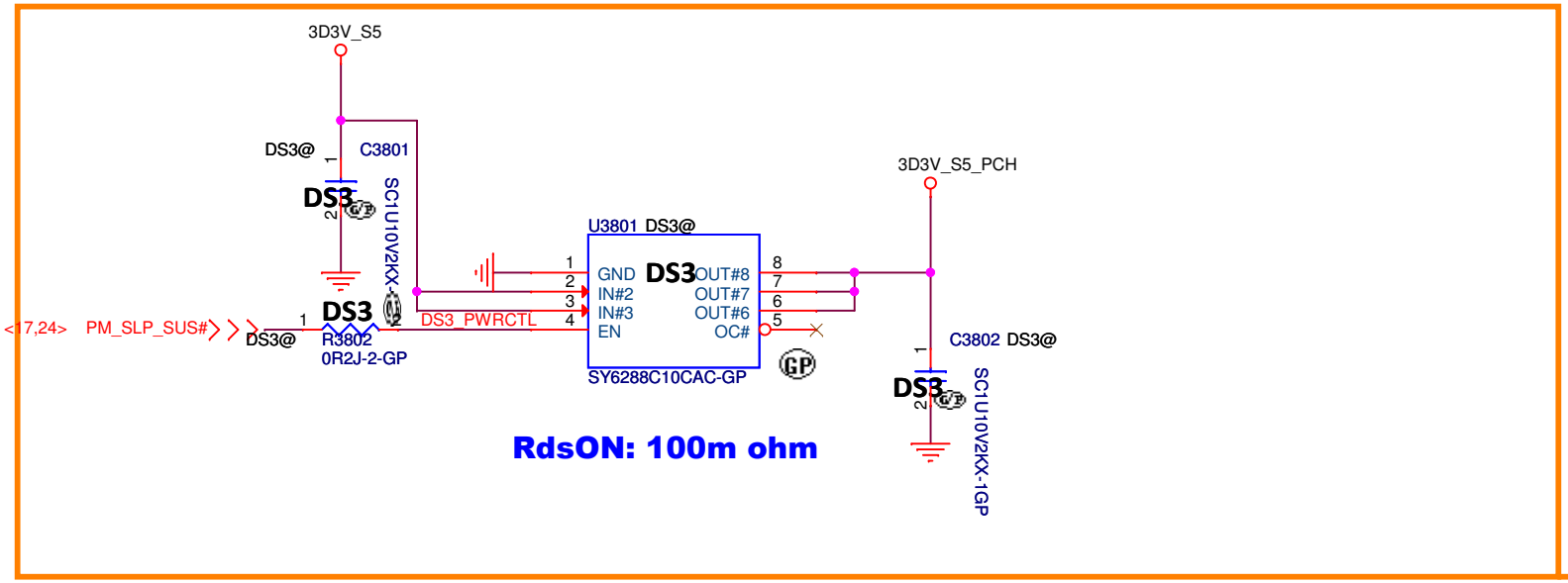
Title: S3 Reduction Circuit

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 Sheet 37 of 102

Main Func = Power Plane & Sequence





DS3

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DSW

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 38 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

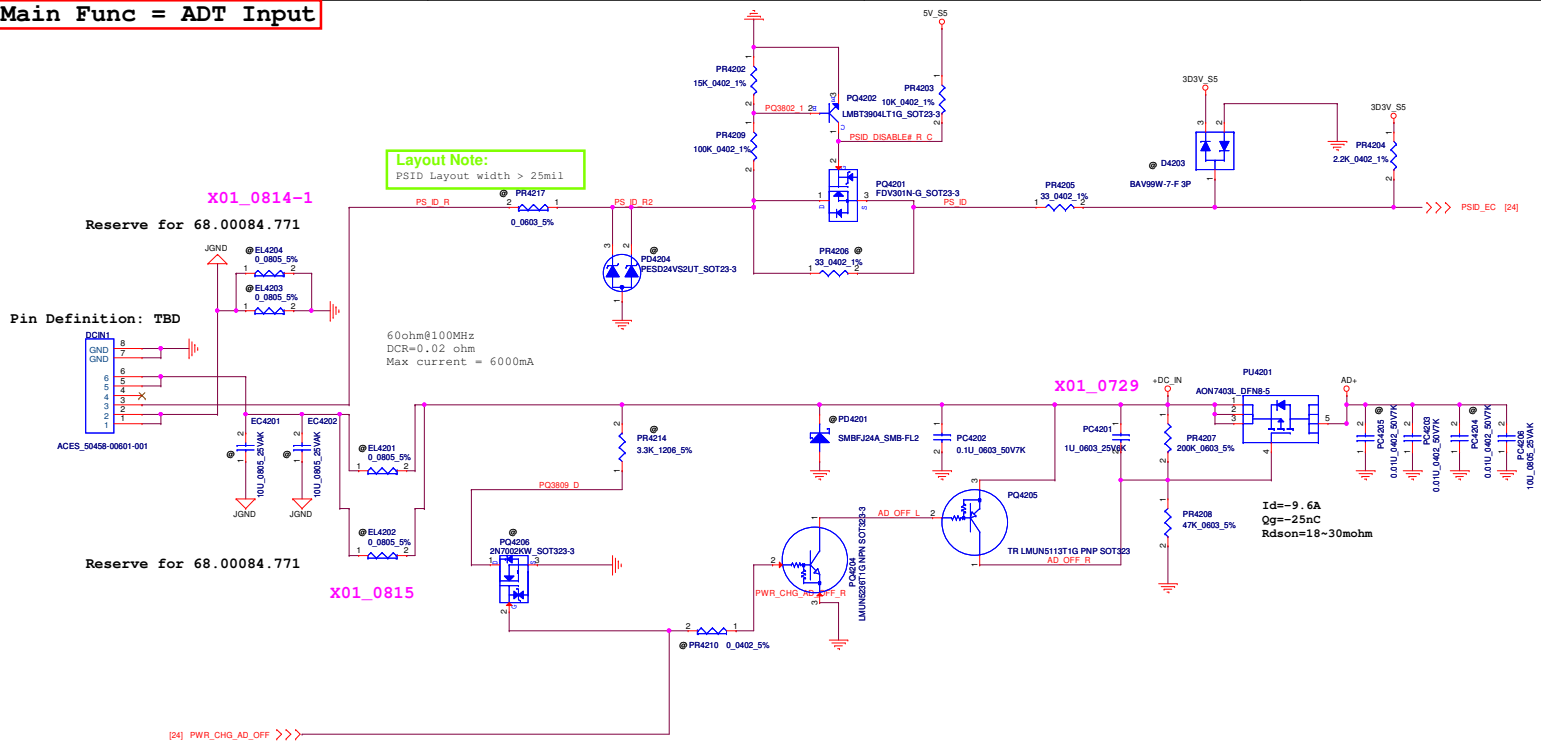
Compal Electronics, Inc.		
Title: (Reserved) 1D05_M		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 39 of 102	

(Blanking)

(Blanking)

Compal Electronics, Inc.		
Title: Reserved		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 41 of 102	

Main Func = ADT Input



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

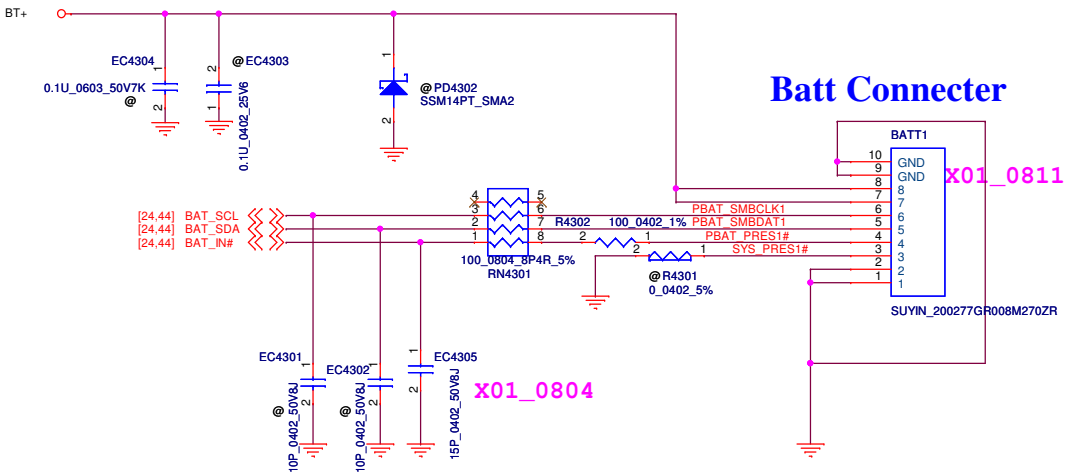
Compal Electronics, Inc.

Title: DCIN

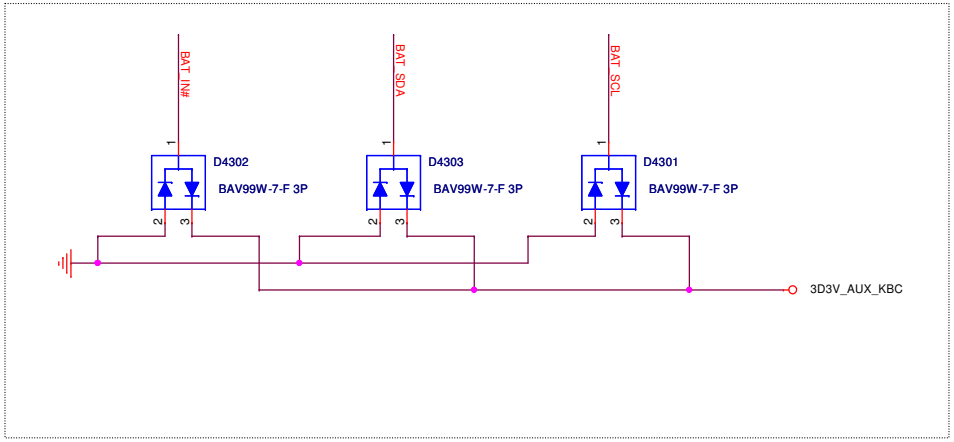
Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 42 of 102

Main Func = M-BAT Input



Placement: Close to Batt Connector



Compal Electronics, Inc.

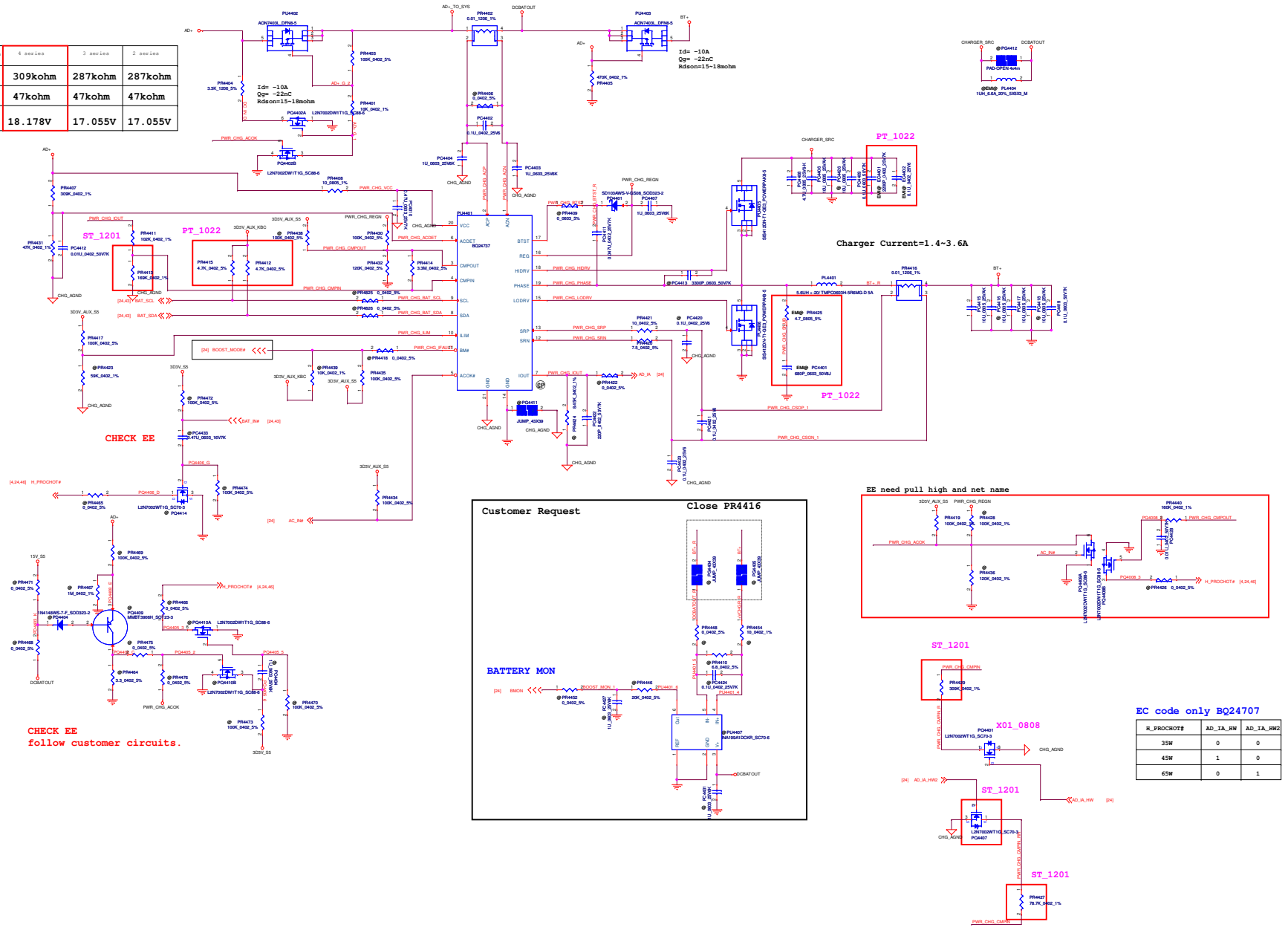
Title: BATT CONN

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 43 of 102

Main Func = Charger

Battery type	4 series	3 series	2 series
PR4407	309kohm	287kohm	287kohm
PR4431	47kohm	47kohm	47kohm
ACDET	18.178V	17.055V	17.055V



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

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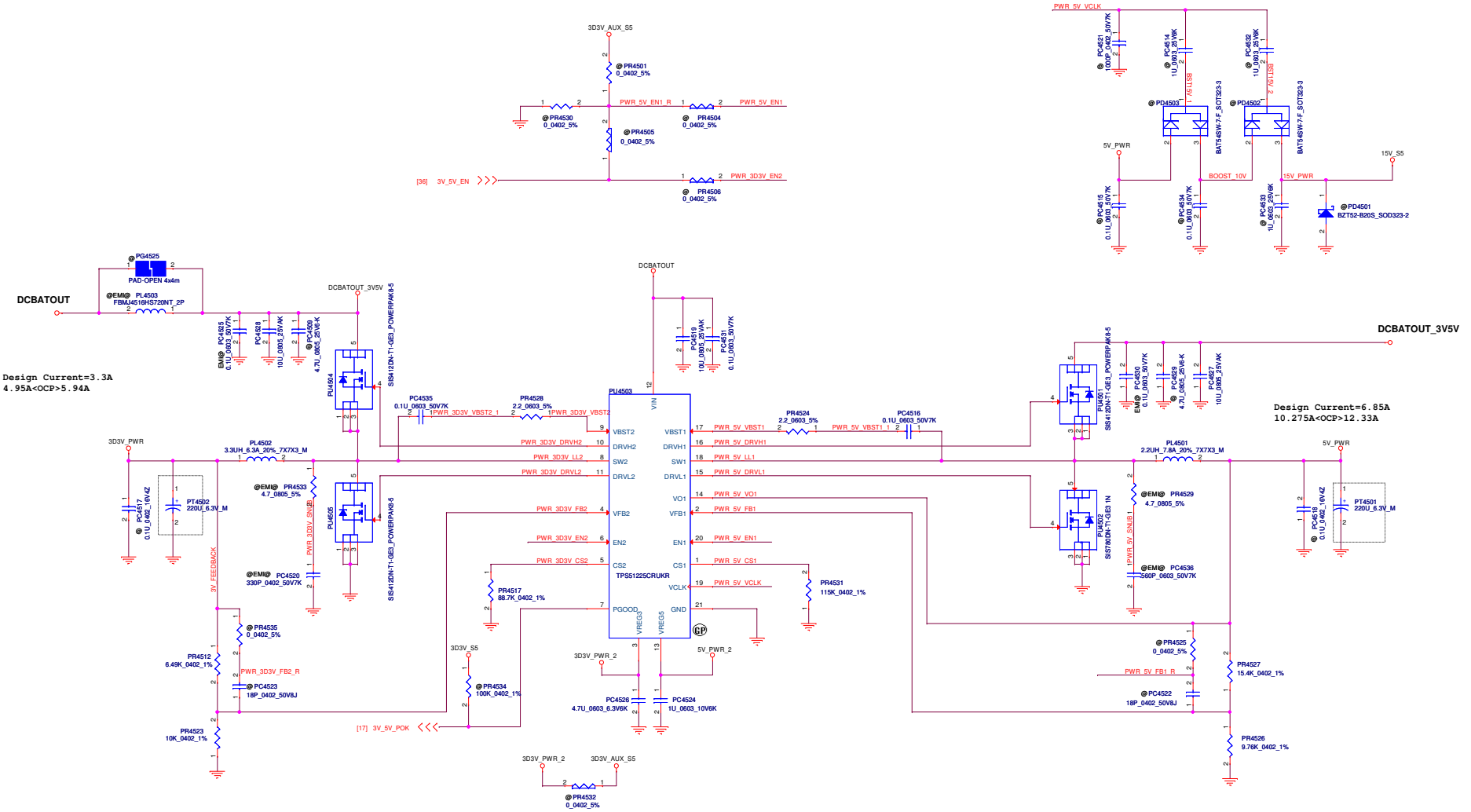
Compal Electronics, Inc.

Title: CHARGER BQ24770

Size: | Document Number: LA-B483P | Rev: A00

Date: Thursday, January 22, 2015 | Sheet 44 of 102

Main Func = 3D3V_5V



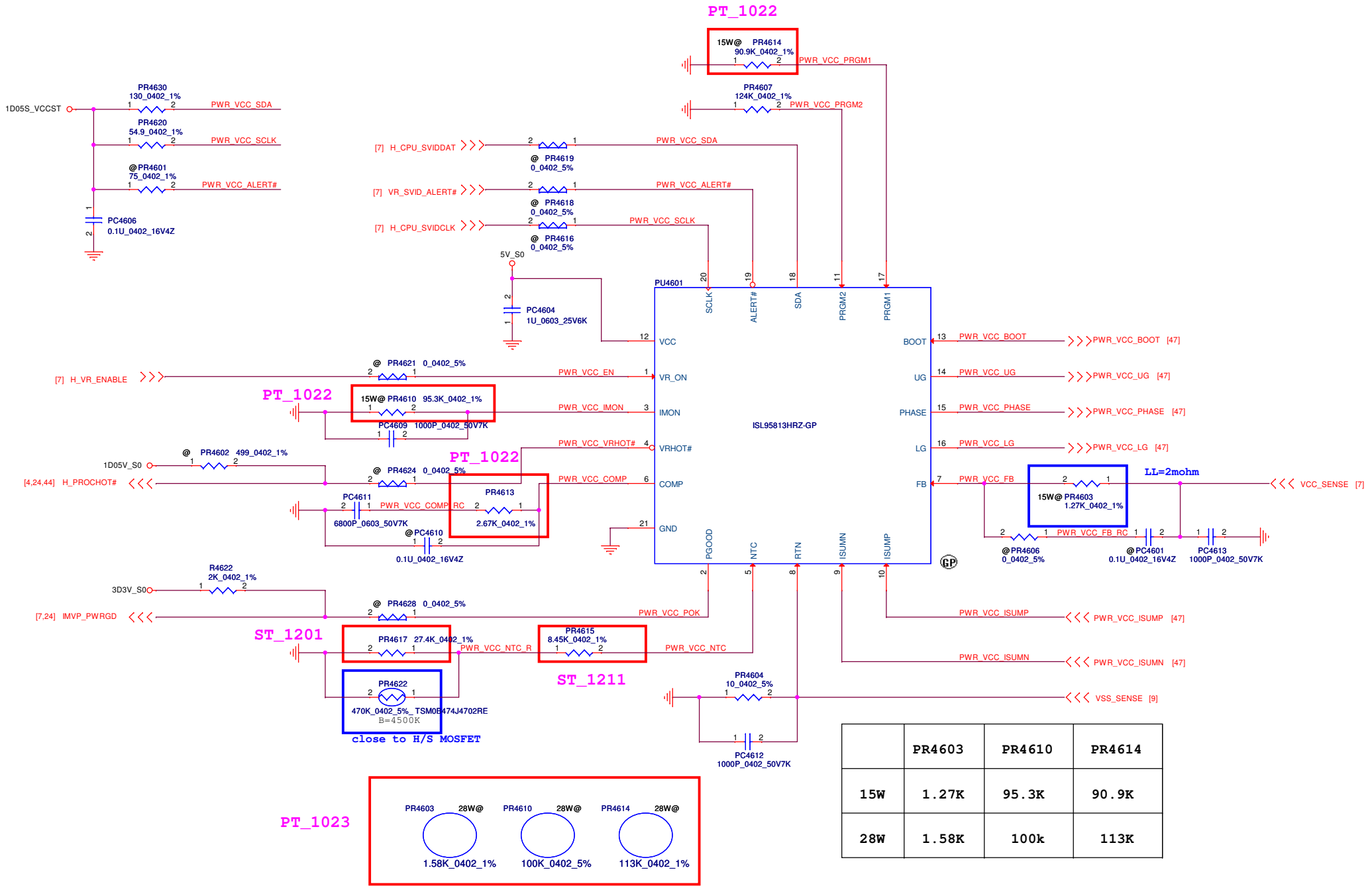
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	TPS51225_5V/3D3V		
Size	Document Number		Rev
	LA-B483P		A00
Date:	Wednesday, January 21, 2015	Sheet	45 of 102

Main Func = CPU_CORE



	PR4603	PR4610	PR4614
15W	1.27K	95.3K	90.9K
28W	1.58K	100k	113K

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

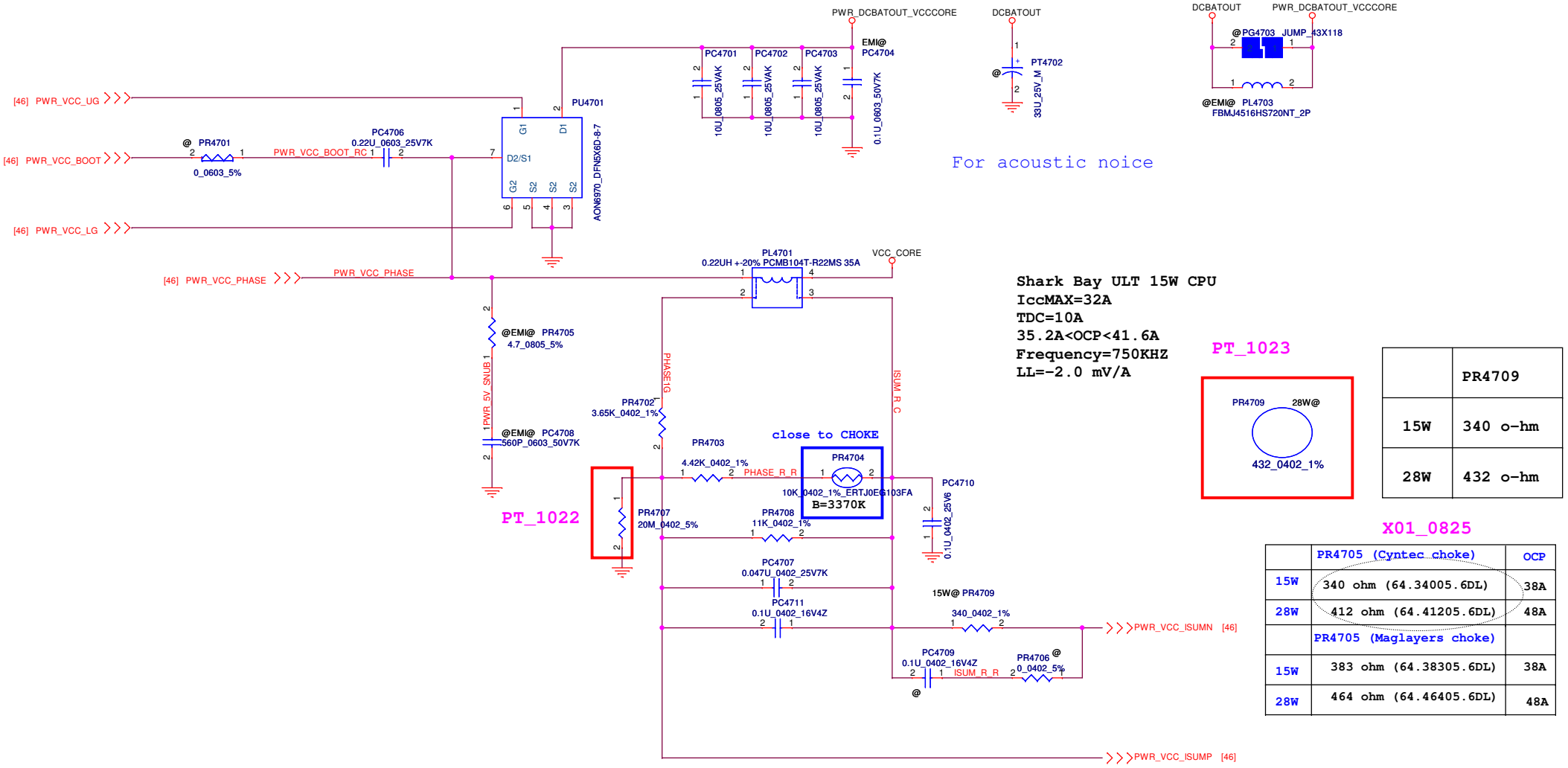
Compal Electronics, Inc.

Title: ISL95813_CPUCORE(1/2)

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 46 of 102

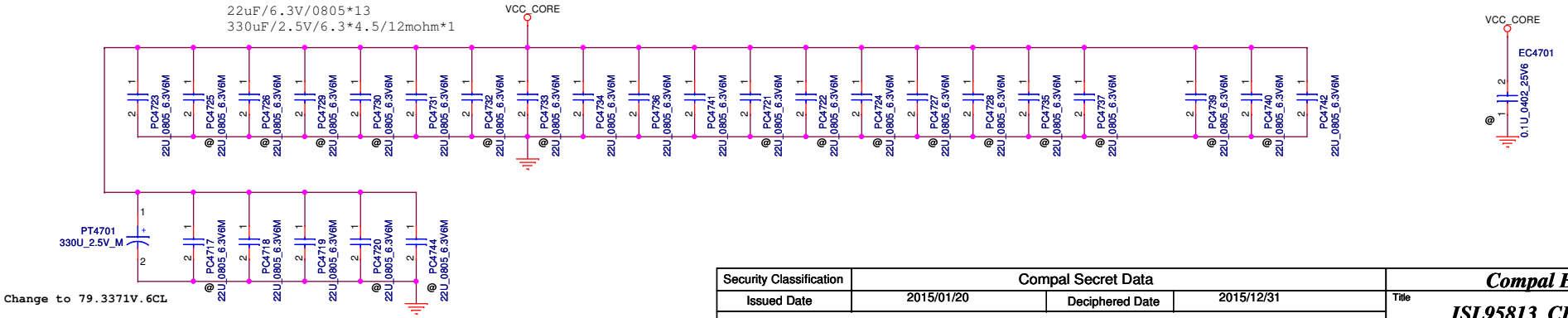
Main Func = CPU_CORE



	PR4709
15W	340 o-hm
28W	432 o-hm

X01_0825

	PR4705 (Cyntec choke)	OCP
15W	340 ohm (64.34005.6DL)	38A
28W	412 ohm (64.41205.6DL)	48A
	PR4705 (Maglayers choke)	
15W	383 ohm (64.38305.6DL)	38A
28W	464 ohm (64.46405.6DL)	48A



Security Classification	Compal Secret Data
Issued Date	2015/01/20
Deciphered Date	2015/12/31

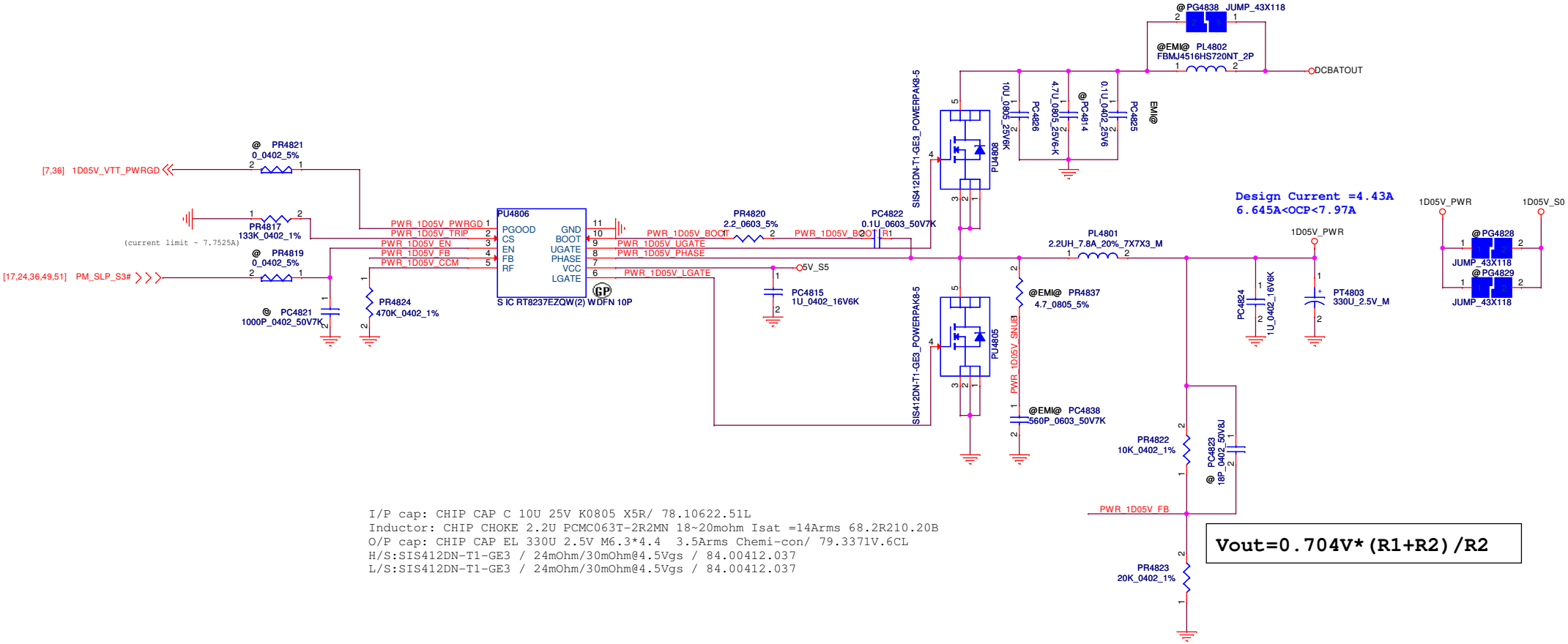
Compal Electronics, Inc.

Title: ISL95813_CPUCORE(2/2)

Size: | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 47 of 102

Main Func = 1D05V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/ 79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

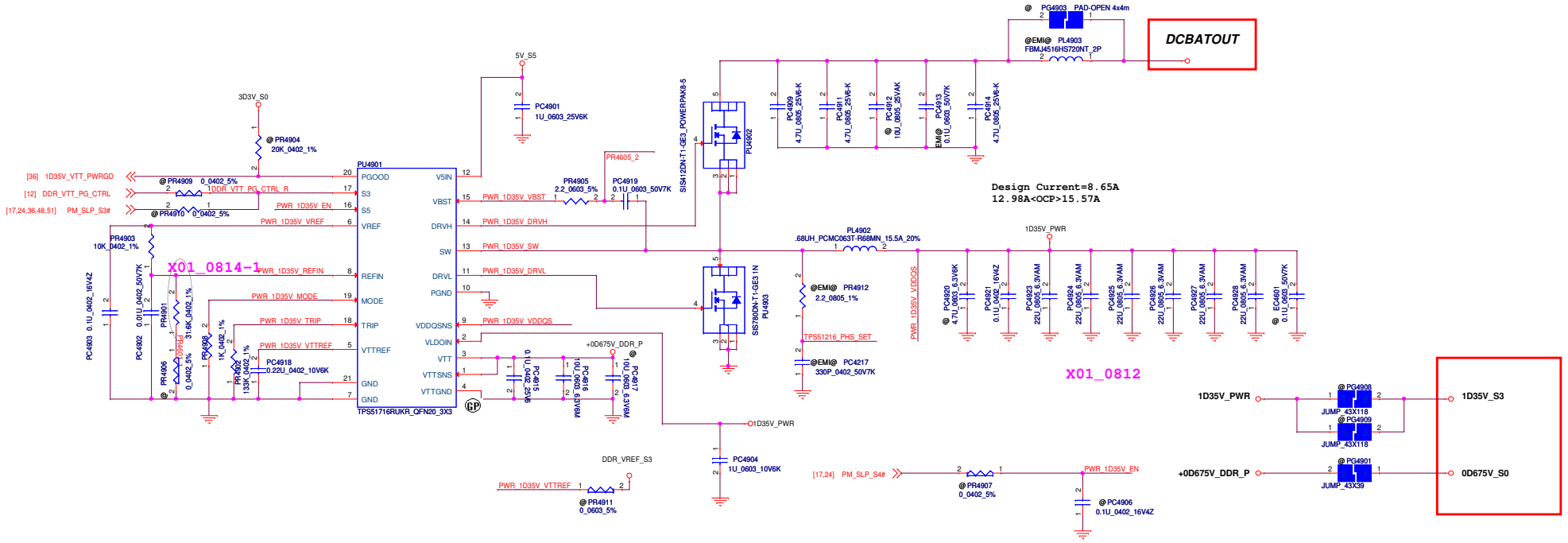
Compal Electronics, Inc.

Title: RT8237_1D05V

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 48 of 102

Main Func = VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.5U PCMC063T-1R5MN 14~15mohm Isat =18Arms 68.1R510.10K
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Component value	VRAM 4pcs (desugn current=8.65A)	VRAM 8pcs (desugn current=10.5A)	
PR4902	133K 64.13335.6DL	191K 64.19135.6DL	OCP setting
PC4927	DY	Stuff	output MLCC
PC4928	DY	Stuff	output MLCC

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: TPS51716_VDDQ_VTT

Size: | Document Number: LA-B483P | Rev: A00

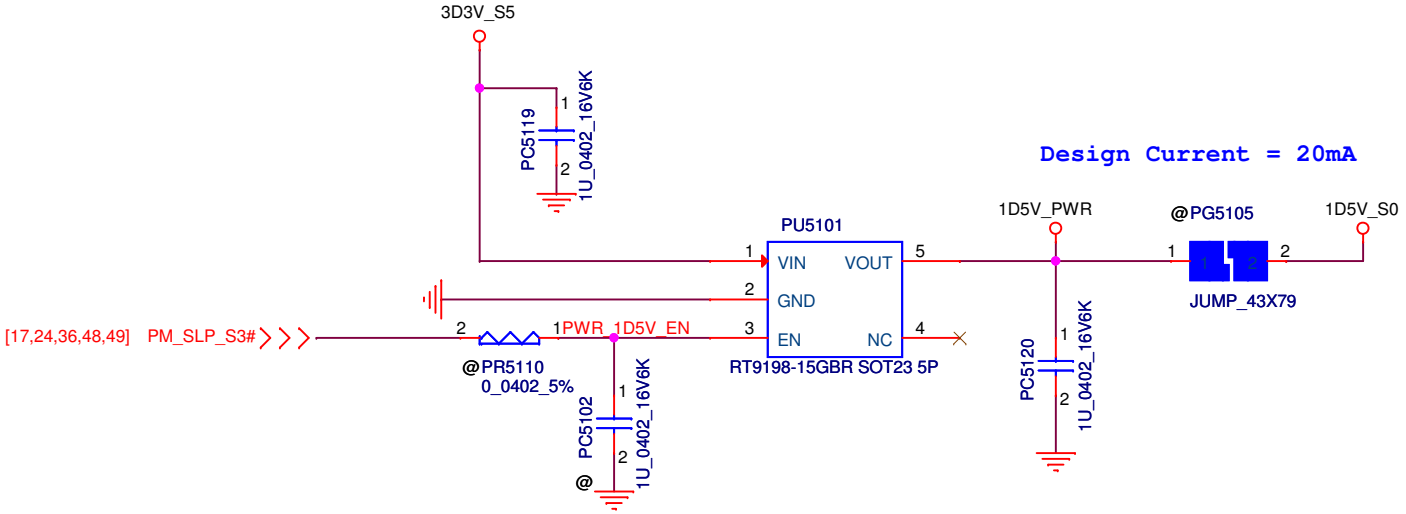
Date: Wednesday, January 21, 2015 | Sheet 49 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.		
Title: Reserved		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 50 of 102	

Main Func = 1D5V



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

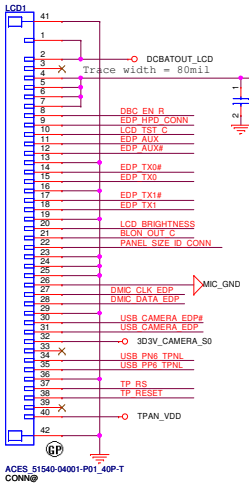
Compal Electronics, Inc.

Title: TLV70215_1D5V

Size | Document Number: LA-B483P | Rev: A00

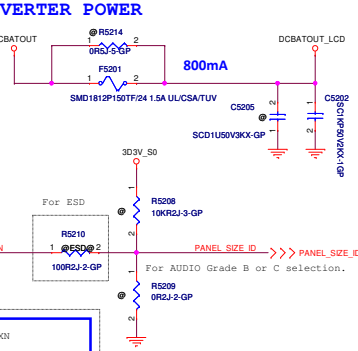
Date: Wednesday, January 21, 2015 | Sheet 51 of 102

Main Func = LCD



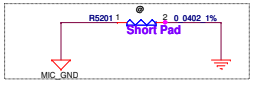
EE note: Never change R5211 to short pad after MP

INVERTER POWER

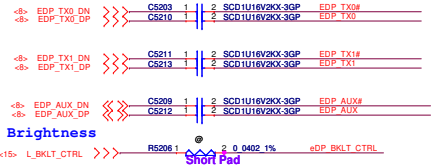


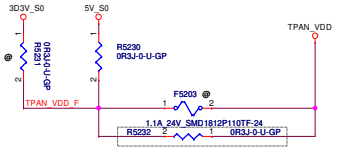
Intel PDG (#514849):
Recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.

Layout Note:
Colse to LCD1.



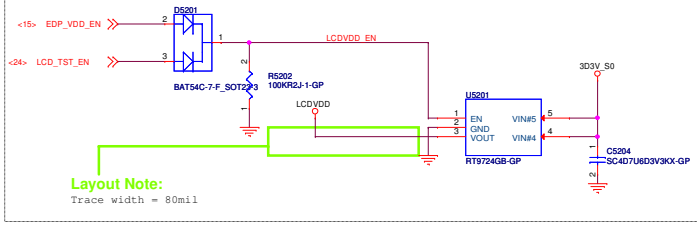
EC (BIST MODE)





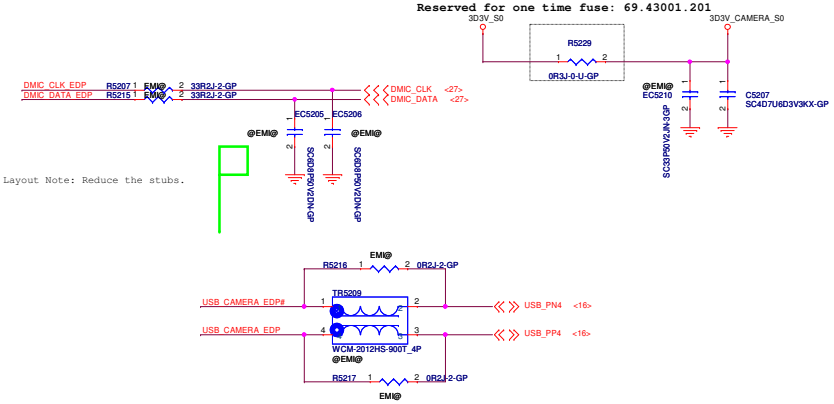
EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

LCDVDD



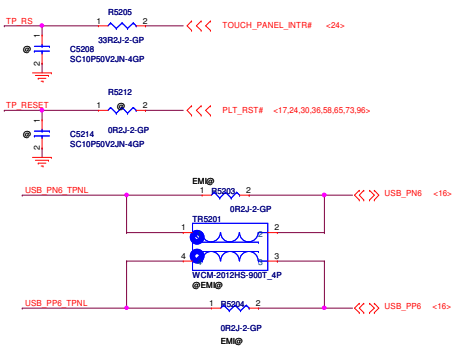
Main Func = CAM

EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201



Main Func = TS

Touch Panel



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Compal Electronics, Inc.	
Title	LCD/Inverter CONN
Size	Document Number: LA-B483P
Rev	A00
Date: Thursday, January 22, 2015	Sheet 52 of 102

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Security Classification	Compal Secret Data		
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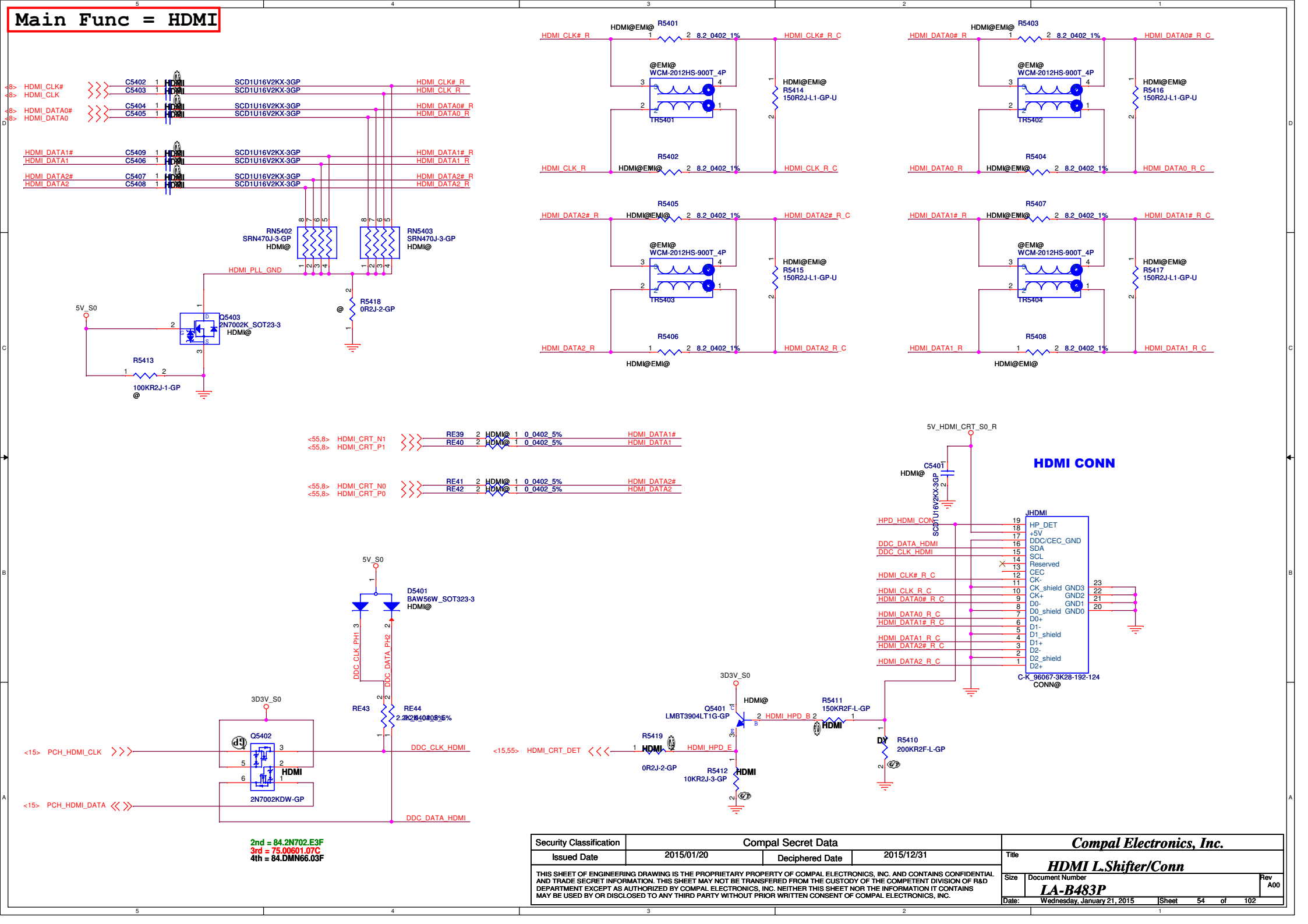
Compal Electronics, Inc.

Title: *(Reserved)*

Size | Document Number: *LA-B483P* | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 53 of 102

Main Func = HDMI



2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **HDMI L.Shifter/Conn**

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 54 of 102

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

CRT RGB
CRT H/VSYNC
CRT SMBUS

Layout note:
All cap need close to chip

	POL1_SDA(PIN22)	
POL2_SCL(PIN23)	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$

DEVICE ADDRESS

Figure 3. Slave Address Bits

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Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

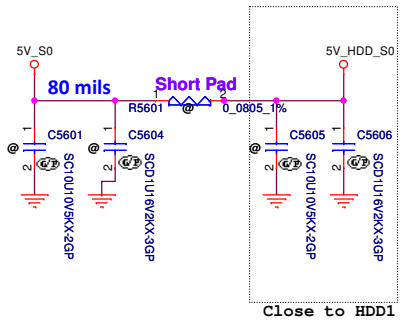
Title: **DP to VGA Converter**

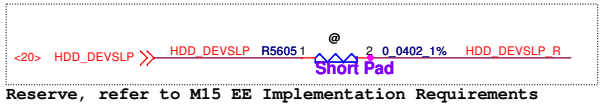
Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 55 of 102

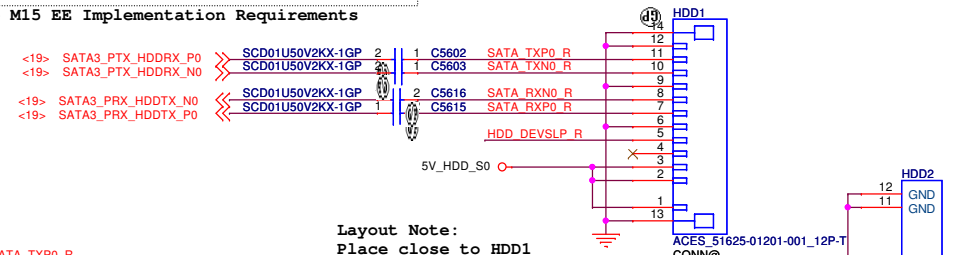
Main Func = HDD

SATA HDD Connector

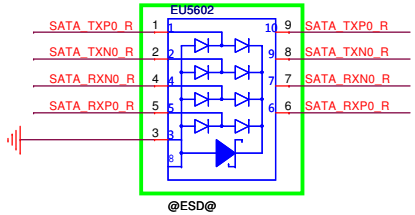




Reserve, refer to M15 EE Implementation Requirements

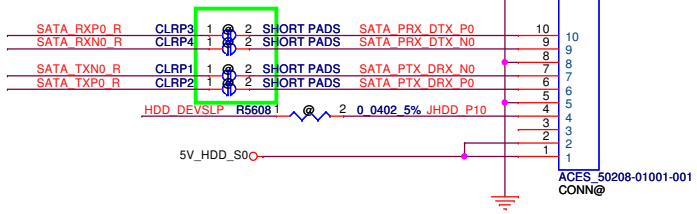


Layout Note:
Place near HDD1



Swap based on the swap report.

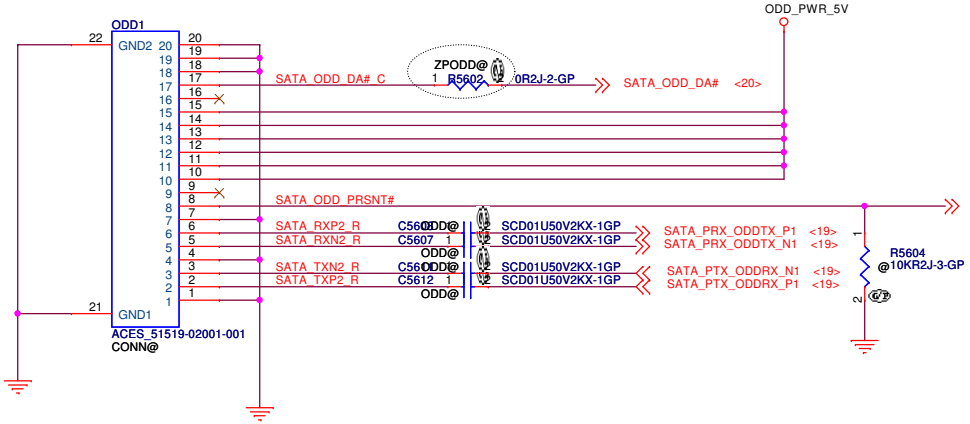
Layout Note:
Place close to HDD1



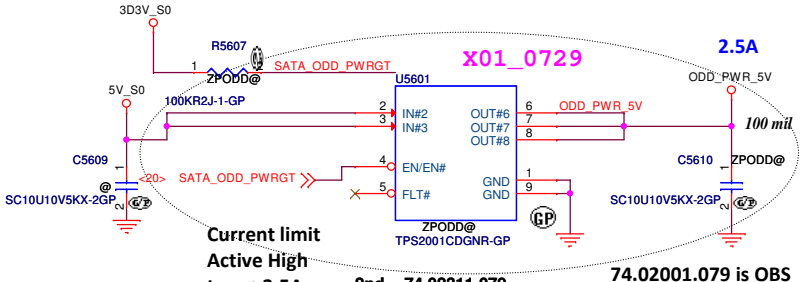
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector



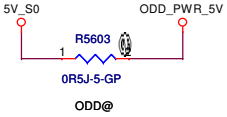
SATA Zero Power ODD

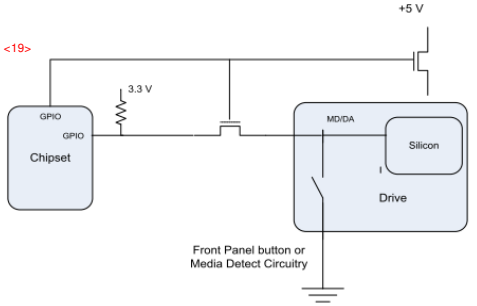


Current limit
Active High
typ =>2.5A

2nd = 74.02311.079

74.02001.079 is OBS
Will use 74.06288.079
but 74.06288.079 is also OBS
we will use 074.06288.0079.





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Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.	
Title	HDD/ODD
Size	Document Number: LA-B483P
Rev	A00
Date: Wednesday, January 21, 2015	Sheet 56 of 102

SSID = ESATA

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

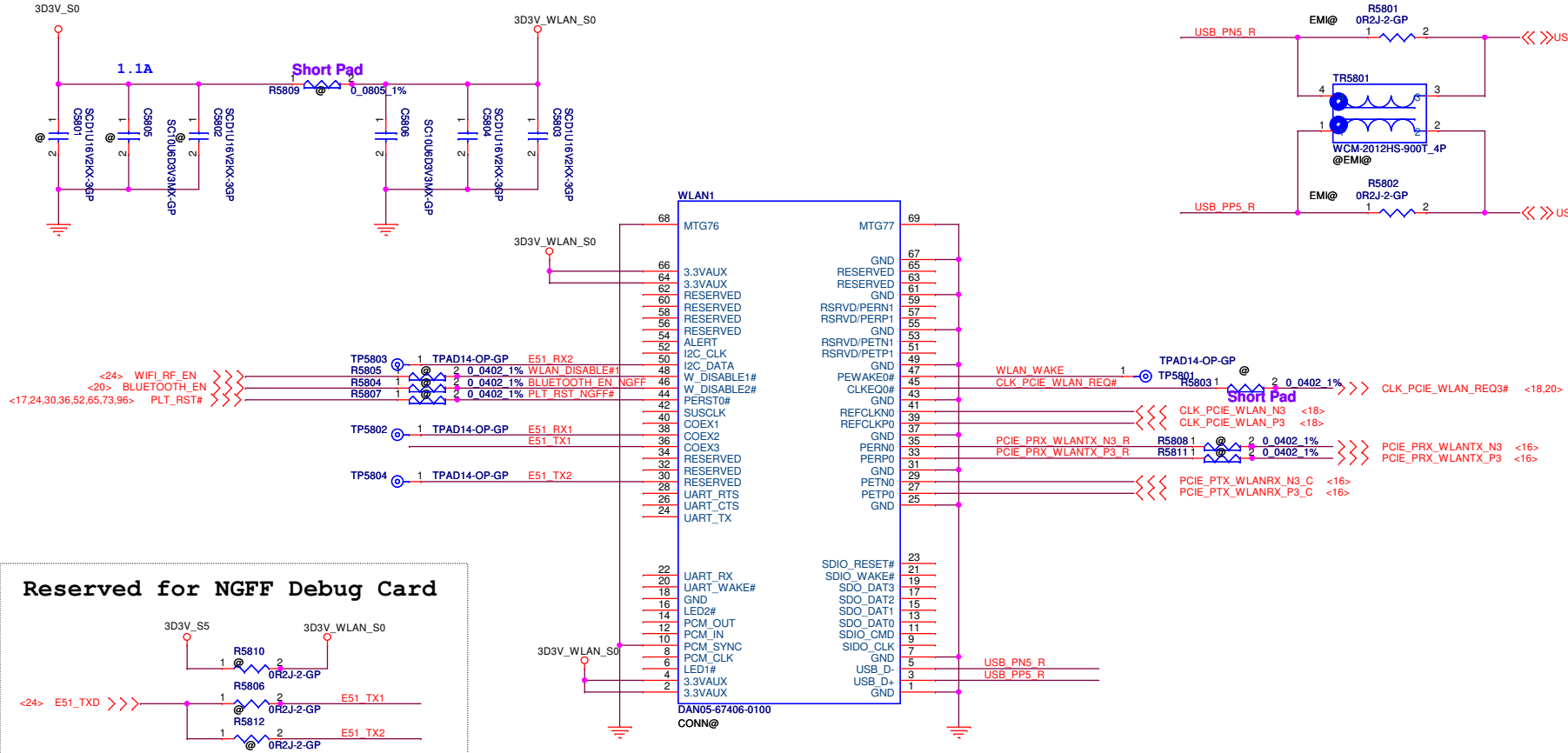
Compal Electronics, Inc.

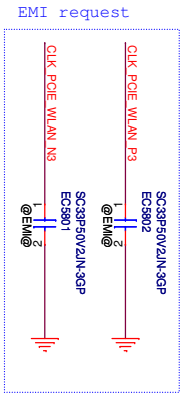
Title: eSATA

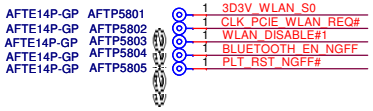
Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 57 of 102

Main Func = WLAN







Support: Intel Dual Band Wireless-AC 3160

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: NGFF_WLAN CONN

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 58 of 102

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Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 59 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

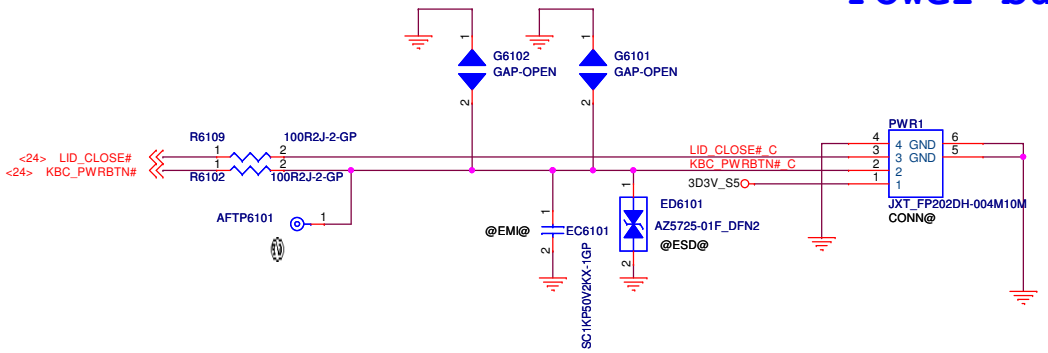
Title: **Reserved**

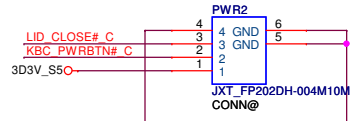
Size | Document Number: **LA-B483P** | Rev: A00

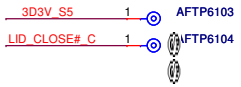
Date: Wednesday, January 21, 2015 | Sheet 60 of 102

Main Func = Power BTN

Power button

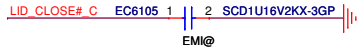




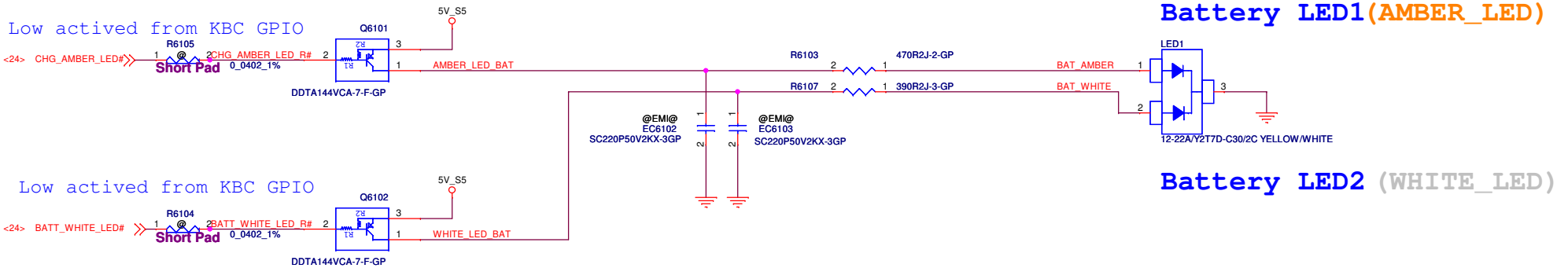


EC6101 must be used 1000pF.

For EMI Reserved



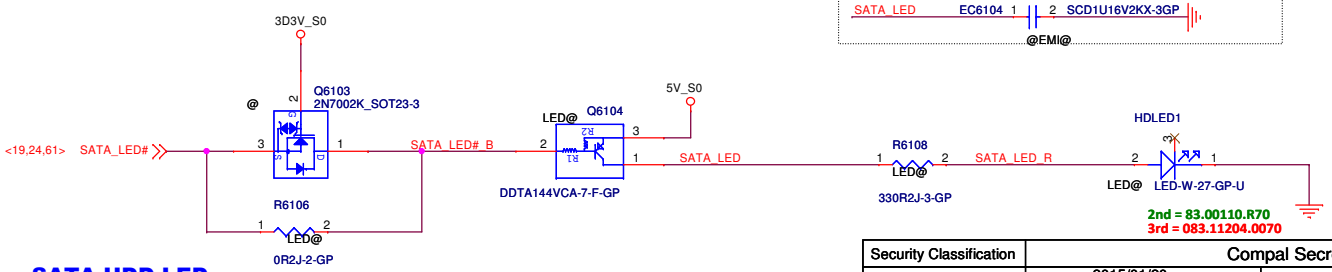
Main Func = Battery LED



Battery LED1(AMBER_LED)

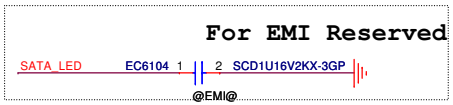
Battery LED2 (WHITE_LED)

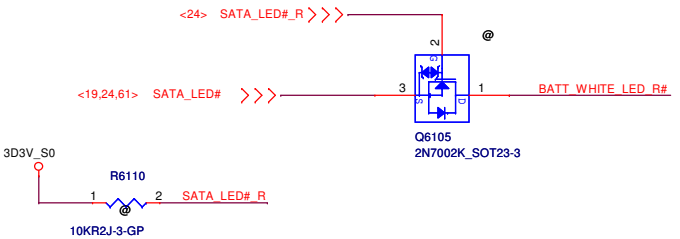
Main Func = HDD LED



SATA HDD LED
LOW actived from PCH GPIO

For EMI Reserved



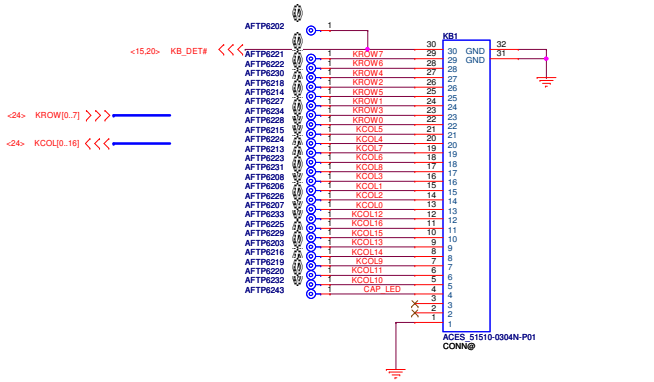


Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.	
Title	LED Bard/Power Button
Size	Document Number: LA-B483P
Rev	A00
Date:	Wednesday, January 21, 2015
Sheet	61 of 102

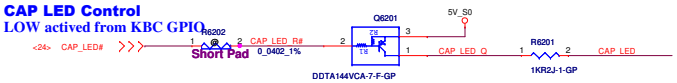
Main Func = KB

Internal Keyboard Connector (DVC40)

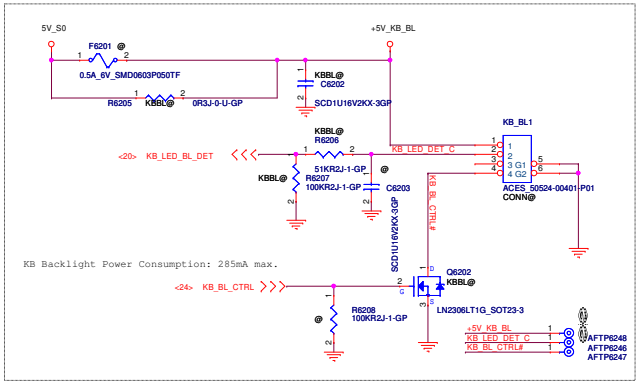


CAP LED Control

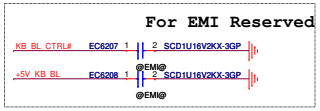
LOW actived from KBC GPIO



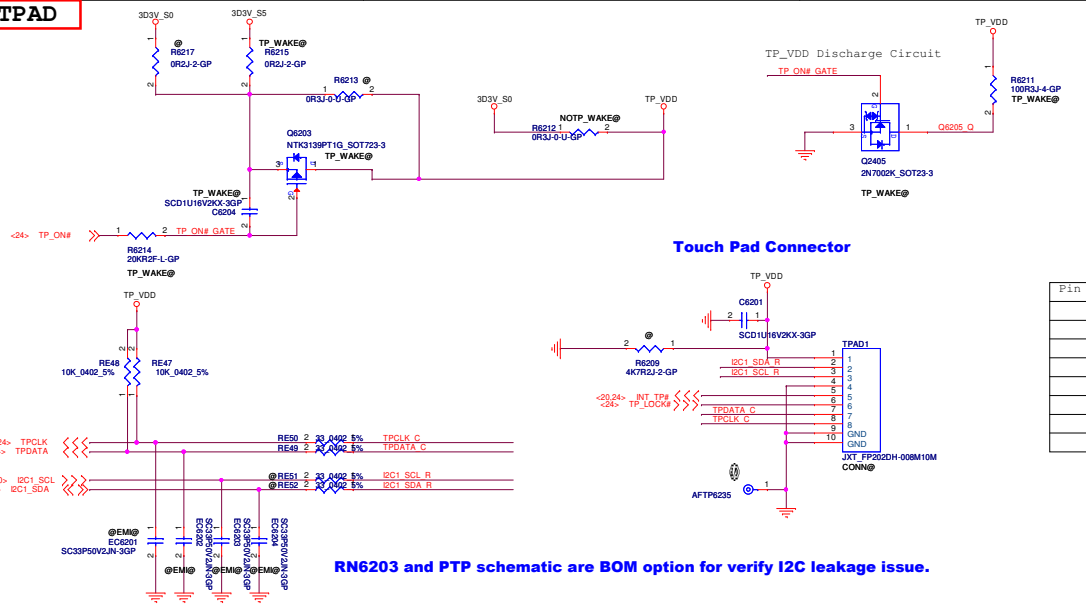
Keyboard Backlight (Reserved)



For EMI Reserved



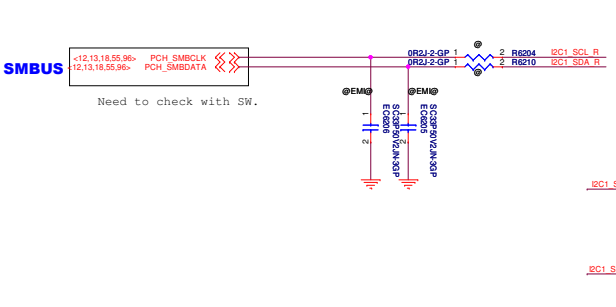
Main Func = TPAD

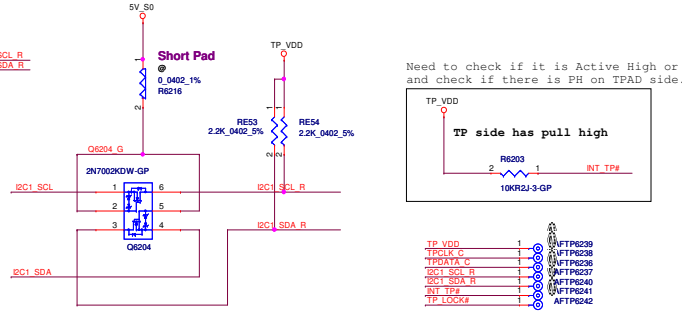


Touch Pad Connector

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

RN6203 and PTP schematic are BOM option for verify I2C leakage issue.





Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

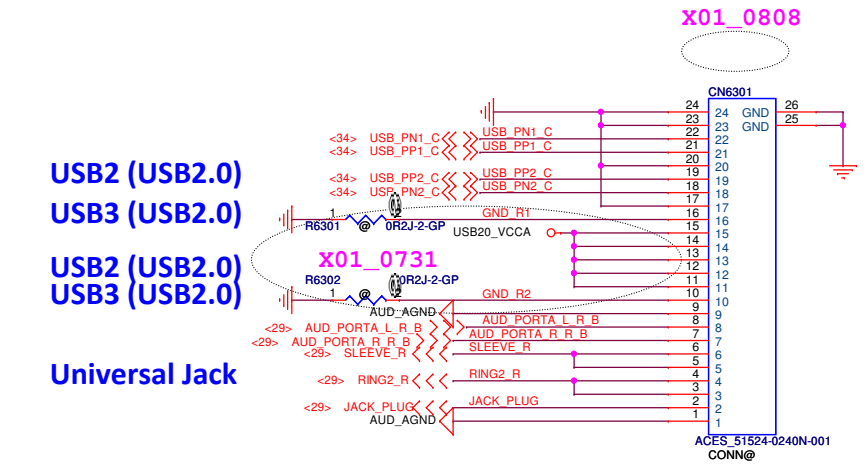
Title: **Keyboard/Touch Pad**

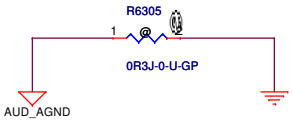
Size: | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 82 of 102

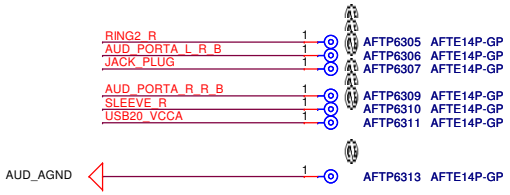
Main Func = IO Connector

I/O Board Connector





Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/20	Deciphered Date	2015/12/31
Title	IO Board Connector		
Size	Document Number		Rev
	LA-B483P		A00
Date:	Wednesday, January 21, 2015	Sheet	63 of 102

Main Func = Hall Sensor

Move to Power Button Board

(Blanking)

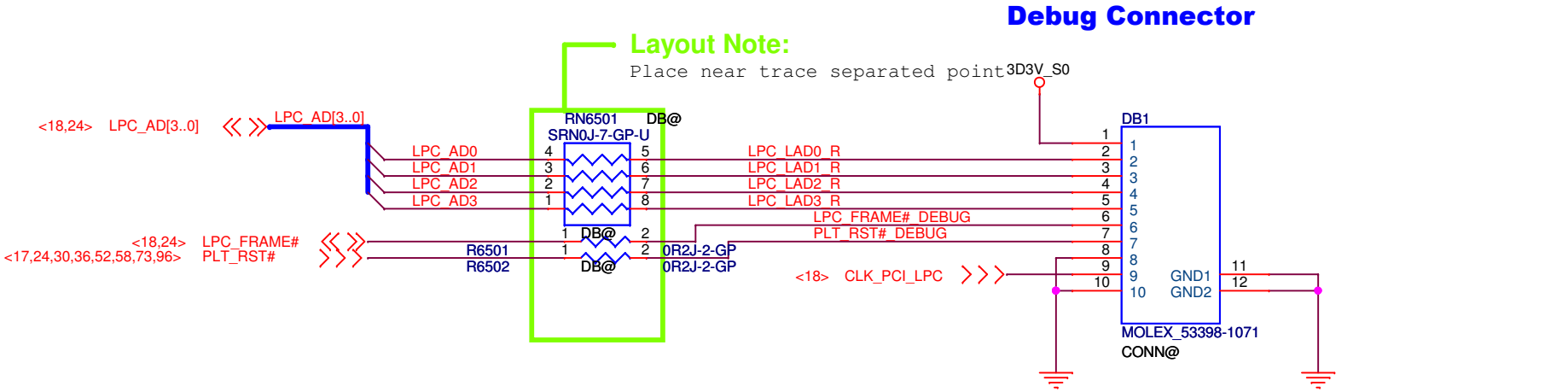
Compal Electronics, Inc.

Title: Hall Sensor

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 64 of 102

Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: Dubug connector

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 65 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 66 of 102

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Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 67 of 102

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Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 68 of 102

(Blanking)

Compal Electronics, Inc.		
Title: Reserved		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 69 of 102	

(Blanking)

Compal Electronics, Inc.		
Title: Reserved		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 70 of 102	

(Blanking)

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 71 of 102

(Blanking)

Compal Electronics, Inc.		
Title: *Reserved*		
Size	Document Number: *LA-B483P*	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 72 of 102	

Main Func = dGPU

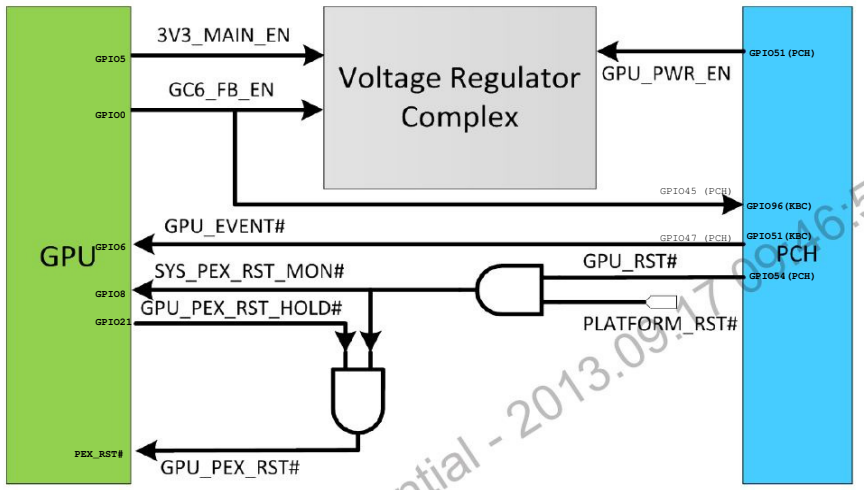

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

dGPU Reset

U7301 MC74VHC1G08DFT2G_SC70-5

GC6_20 R7312 10KR2J-3-GP

R7308 0R2J-2-GP GC6_20

D7301 BAT54A-7-F_SOT23-3

R7304 0R2J-2-GP

R7306 100KR2F-L1-GP

R7303 10KR2J-3-GP

Q7301 2N7002K_SOT23-3

R7305 0R2J-2-GP

R7313 NON_GC6 0R2J-2-GP

GPU1A 1 OF 14 — 1/14 PCI_EXPRESS — GK208/GF117/GF119

1.05V +/- 30mV
3.3A

Place close VDD ball

Place close Chip

Table 3-16. PEX_IOVVD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

3.3V +/- 5%
210mA

Place close Chip

POWER IC

1.05V +/- 30mV
150mA

L7301 TAI-TECH HCB1608KF-121T30 0603

N14M-GE-S-A2-GP

N15V-GM-S-A2: JG0YH
N15S-GT is PXP79

GPU1 N15V@ R3 — N15V-GM-S-A2 BGA 595P GPU — SA00007BR1L

GPU1 N16V@ R3 — N16V-GM-S-B1 BGA 595P GPU — SA000088R1L

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

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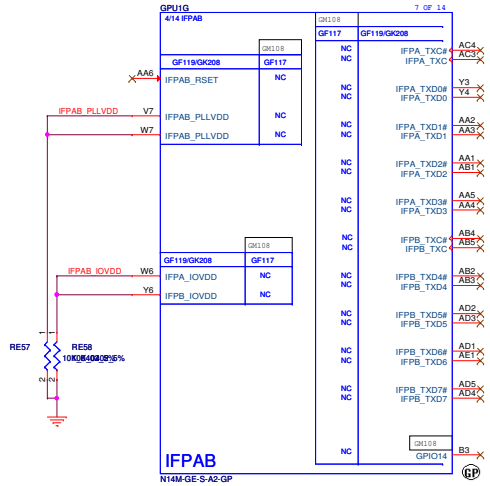
Title: GPU(1/5)PEG

Size: | Document Number: LA-B483P | Rev: A00

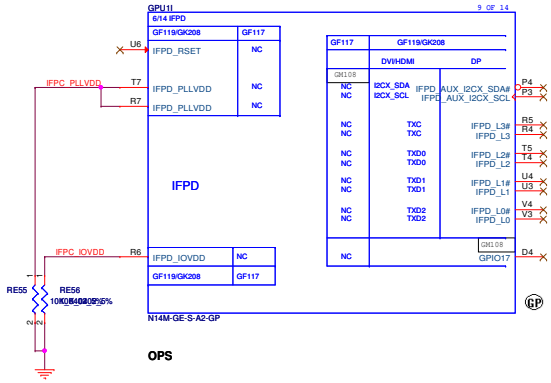
Date: Wednesday, January 21, 2015 | Sheet 73 of 102

Main Func = dGPU

LVDS Interface

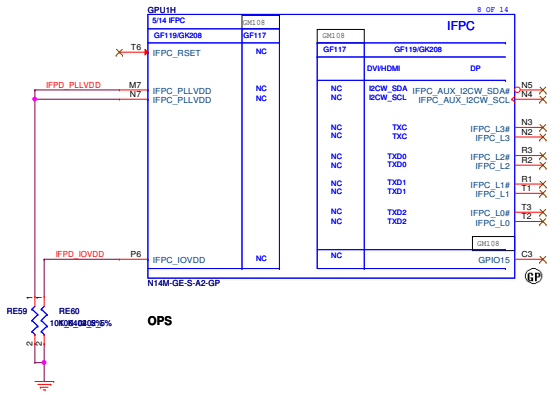


OPS



OPS

HDMI Interface



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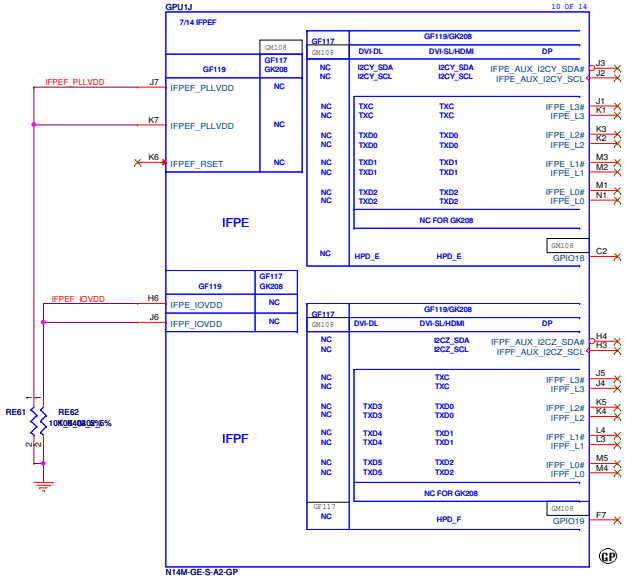

OPS

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Issued Date	2015/01/20	Deciphered Date	2015/12/31

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Title	GPU(2/5)DIGITALOUT
Size	Document Number: LA-B483P
Rev	A00
Date: Wednesday, January 21, 2015	Sheet 74 of 102

Main Func = dGPU

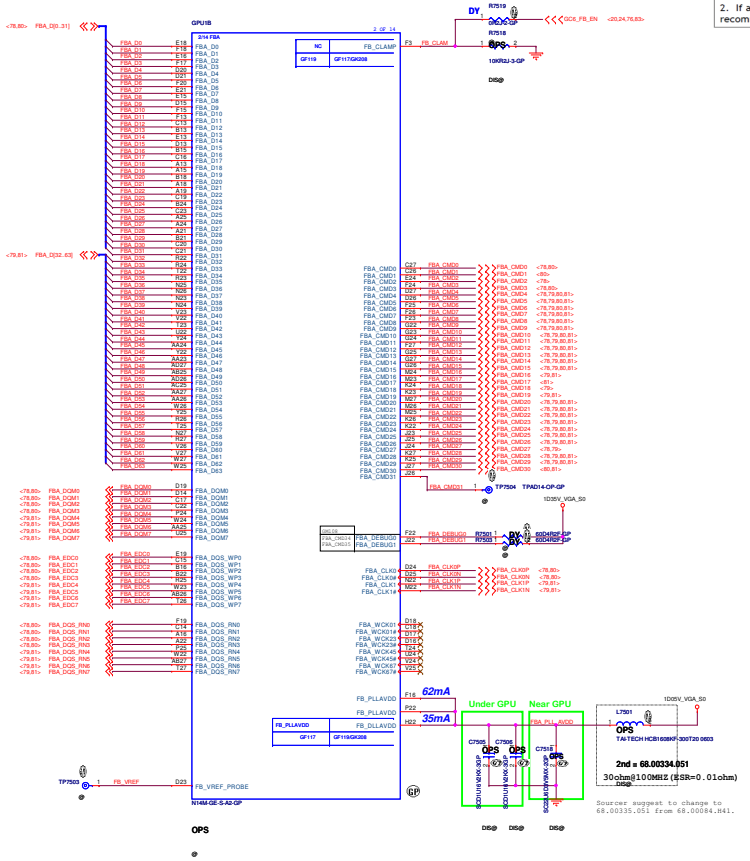
Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

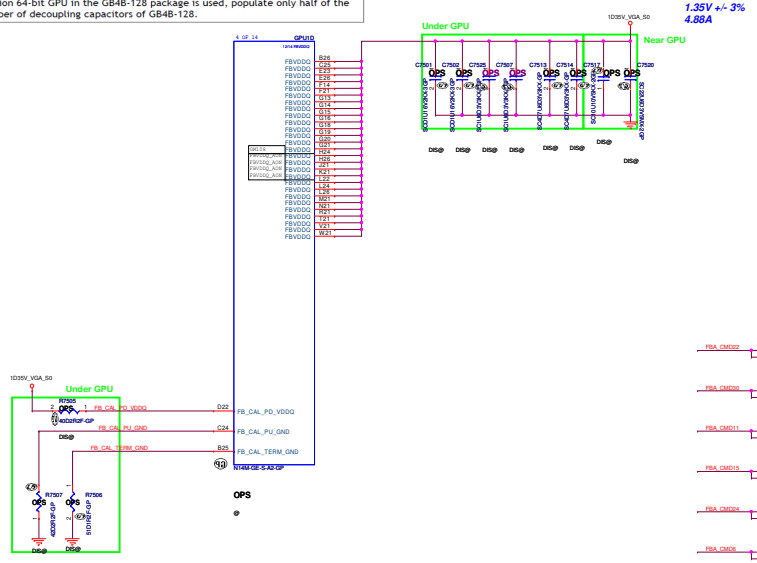
GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU
GB4B-128 DDR3	0.1µF	X7R	0402	4	4	Under GPU
	1 µF	X7R	0603	4	4	Under GPU
	4.7 µF	X6S	0603	4	4	Under GPU
	10 µF	X5R	0805	2	2	Near GPU
	22 µF	X5R	0805	2	2	Near GPU

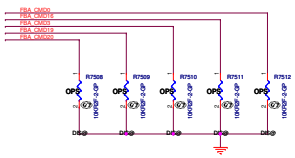
Notes:
1. The decoupling in this table applies to both single rank and dual rank designs.
2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU







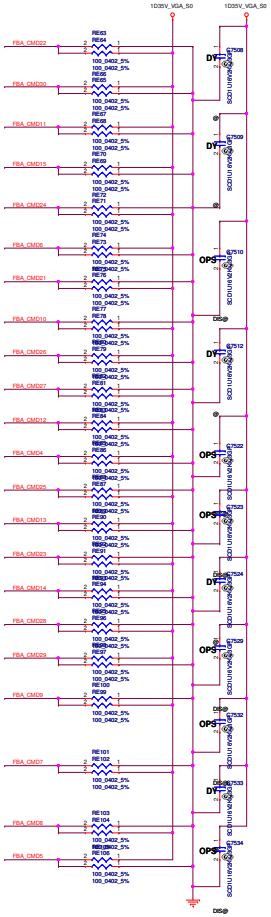


Table 6-4. Mode E Command Mapping

N15x DDR3 Mode E	Rank 0 Data Bits [31:0]	Rank 0 Data Bits [63:32]	Rank 1 Data Bits [31:0]	Rank 1 Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/20	Deciphered Date 2015/12/31	Title: GPU(3/5)VRAM I/F
			Size: Document Number: LA-B483P Rev: A00
			Date: Wednesday, January 21, 2015 Sheet 75 of 102

Main Func = dGPU

Straps

(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENDOR	10kΩ	*Pull-up to 3V3 if VBIOS ROM exists *Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

(RVL-06891-001)N15V-GM-S DDR3L Recommended Memories

		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

(DS-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	N15S-GV	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	N15S-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	All GB2-64 N14 and GB2B-64 N15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	N15S-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	N15S-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAP0	N15S-GV	USER[3]	USER[2]	USER[1]	USER[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)			
STRAP1	N15S-GV	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	N15S-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	N15S-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	N15S-GV	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF X7R	0402	1	Under GPU
		22 µF X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.05)	0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD + VID_PLLVDD	0.1 µF X7R	0402	1 per ball	Under GPU
		4.7 µF X5R	0603	1	Near GPU
		22 µF X5R	0805	1	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU

(RVL-06891-001)N15V-GT-S DDR3L Recommended Memories

		Strap	
128Mx16 DDR3L	Hynix	0x9	H5TC2G63FFR-11C
	Micron	0xA	MT41J128M16JT-093G:K
	Samsung	0xB	K4W2G1646E-BY11
256Mx16 DDR3L (4 pcs VRAM)	Hynix	0x3	H5TC4G63AFR-11C
	Micron	0x4	MT41J256M16HA-093G:E
	Samsung	0x5	K4W4G1646D-BC1A
256Mx16 DDR3L (8 pcs VRAM)	Hynix	0xC	H5TC4G63AFR-11C
	Micron	0xD	MT41J256M16HA-093G:E
	Samsung	0xE	K4W4G1646D-BC1A

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

	N15V-GM	N15S-GT
Chip	N15V-GM	N15S-GT
Device ID	0x1140	0x1341
Memory Interface	sDDR3	SDDR3
Package	595 ball BGA 23x23mm	595 ball BGA 23 x 23 mm 908 ball BGA 29 x 29 mm

R7640,R7641,R7642 for N15S-GT 4 pcs VRAM
R7619,R7638,R639 for N15S-GT 8 pcs VRAM

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

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Title: GPU(4/5)GPIO/STRAP

Size: Document Number: LA-B483P Rev: A00

Date: Wednesday, January 21, 2015 Sheet 78 of 102

Main Func = dGPU

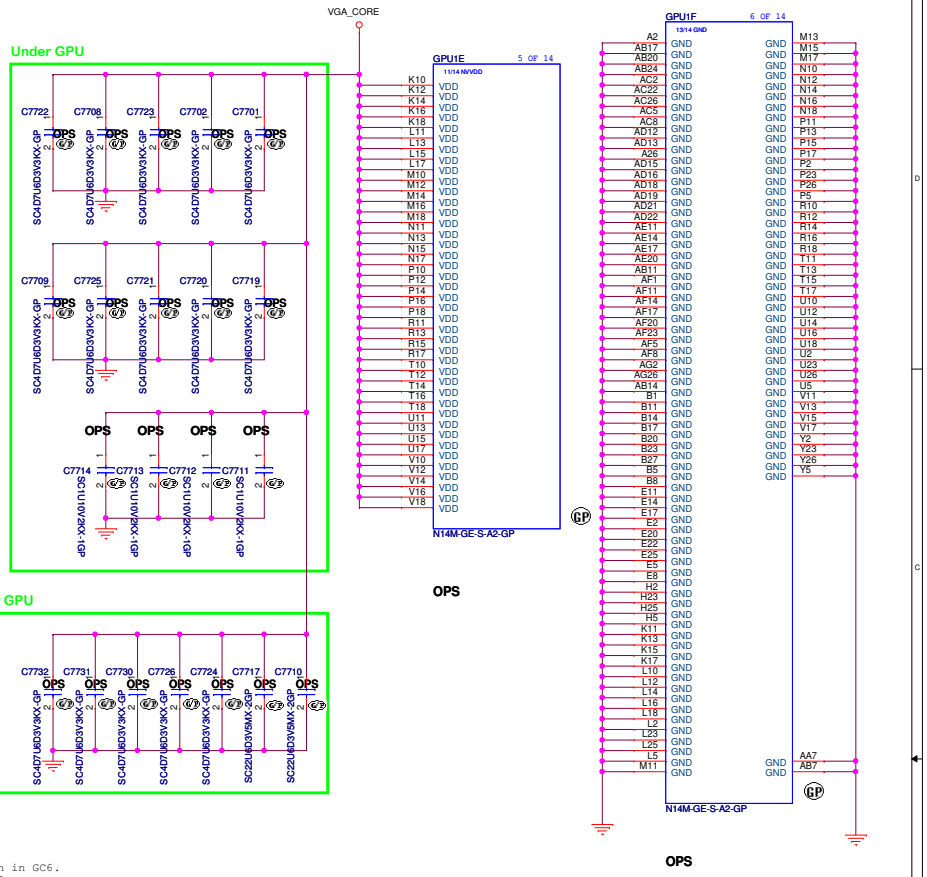
Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

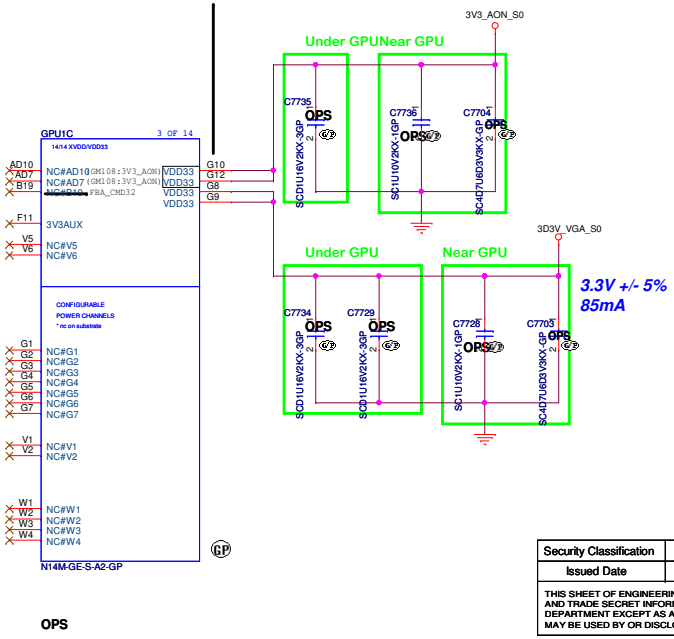
Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.



G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



1GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	2Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBGA595P	JG0YH	Hynix	H5TC2G63FFR-11C	X1PRC	72.52G63.N0U	1.35V	
		Samsung	K4W2G1646Q-BC1A	D0DP7	072.2G164.0A0U	1.35V	
		Micron	MT41K128M16JT-107G:K	HKKF2	72.41128.N0U	1.35V	

2GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBGA595P	JG0YH	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41K256M16HA-107G:E	R5RH5	72.41K26.00U	1.35V	Build in EVT

4GB, Dual Rank, 8 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15S-GT-S-A2 GB2-64 FCBGA595	PXP79	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41J256M16HA-093G:E	PP8TP	072.41256.0B0U	1.35V	

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

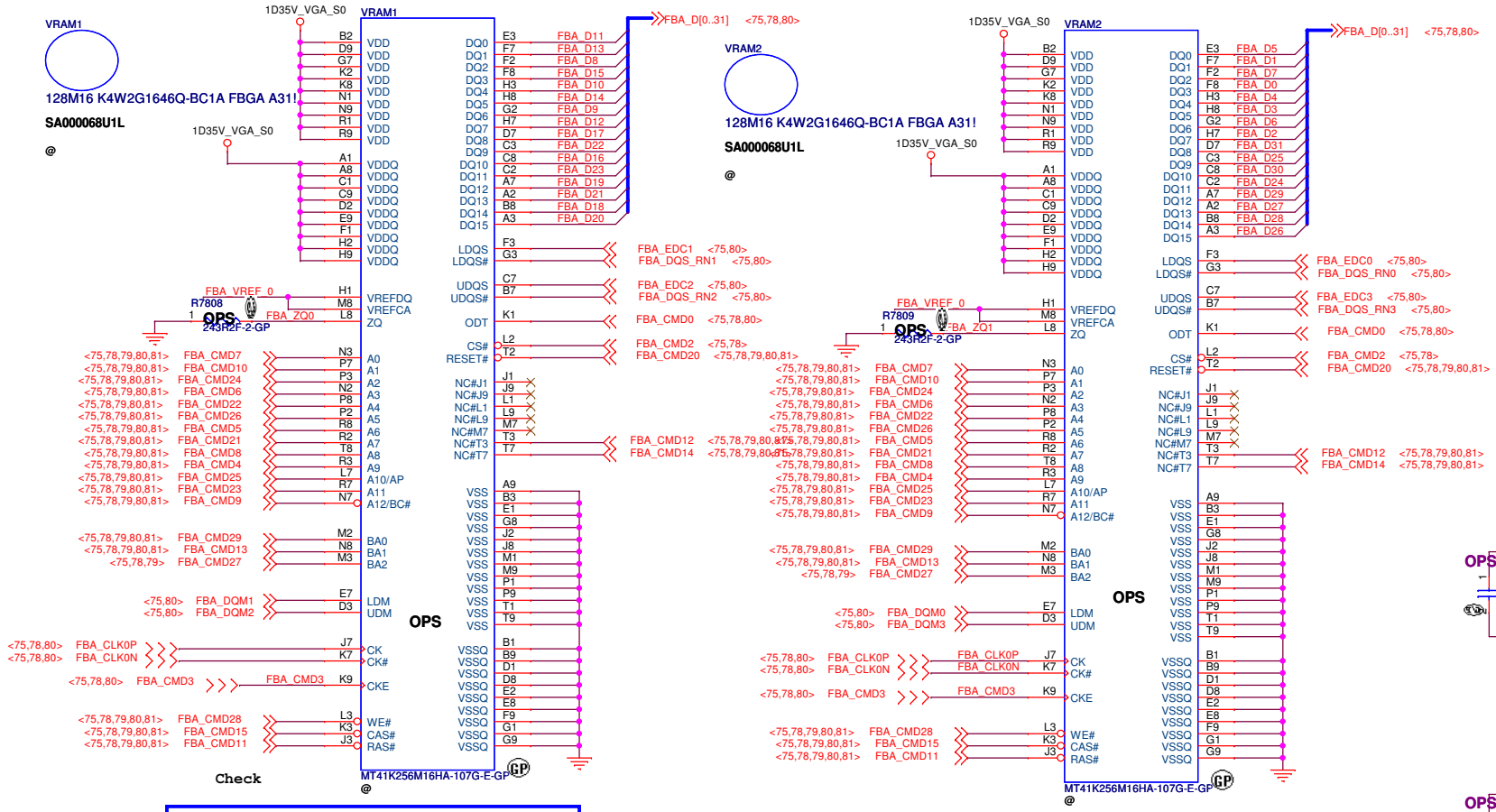
Title: GPU(5/5)PWR/GND

Size | Document Number: LA-B483P | Rev: A00

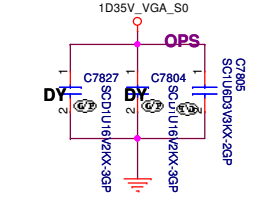
Date: Wednesday, January 21, 2015 | Sheet 77 of 102

Main Func = dGPU

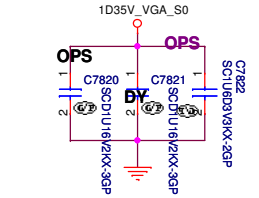
Data Bits 31:0 RANK 0



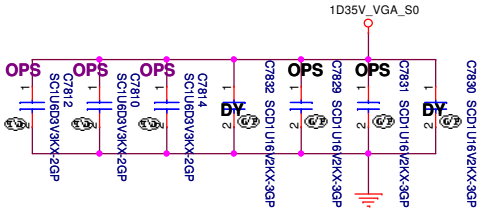
Place close VRAM1 VDD ball



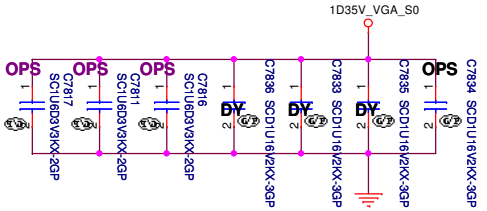
Place close VRAM2 VDD ball



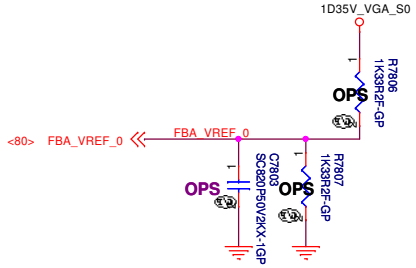
Place close VRAM1VDDQ ball

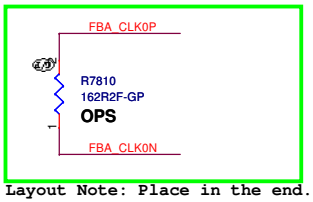


Place close VRAM2VDDQ ball



Frame Buffer Patition A-Lower Half





Layout Note: Place in the end.

FBCLK Termination place on VRAM side

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

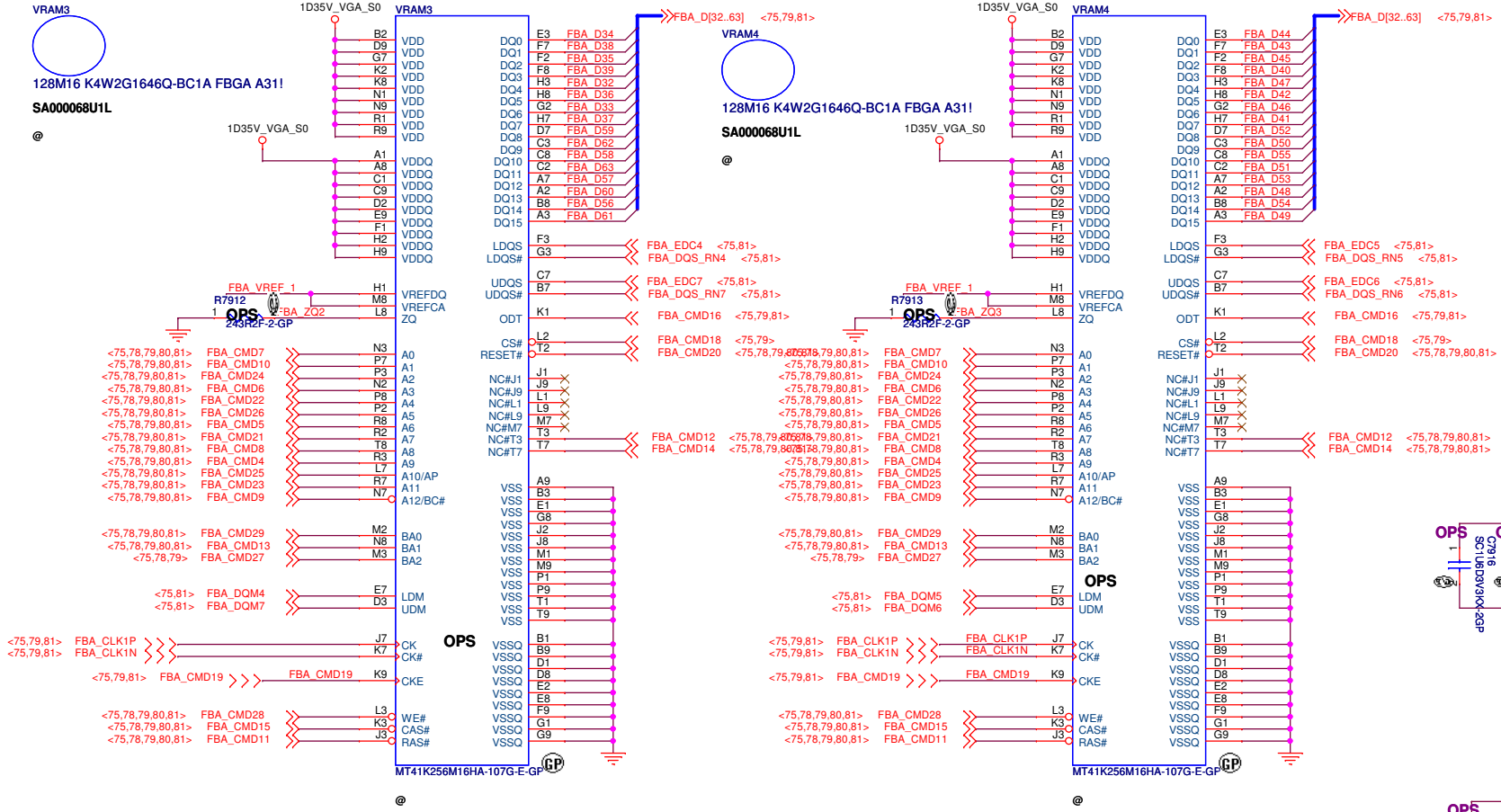
Title: GPU-VRAM1,2 (1/4)

Size | Document Number: LA-B483P | Rev: A00

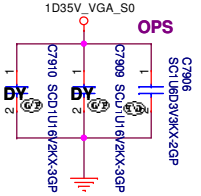
Date: Wednesday, January 21, 2015 | Sheet 78 of 102

Main Func = dGPU

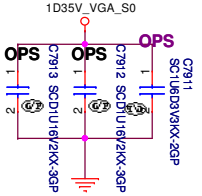
Data Bits 63:32 RANK 0



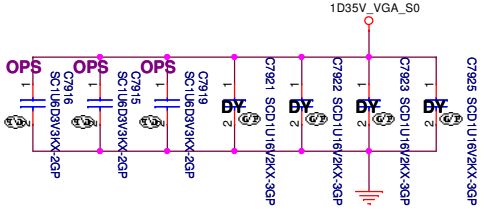
Place close VRAM3 VDD ball



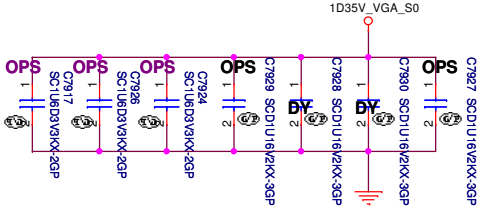
Place close VRAM4 VDD ball



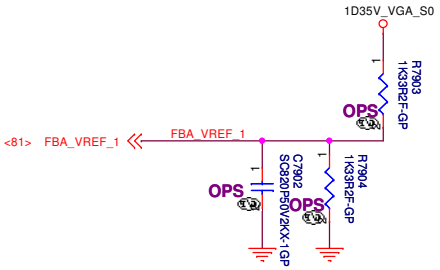
Place close VRAM3 VDDQ ball



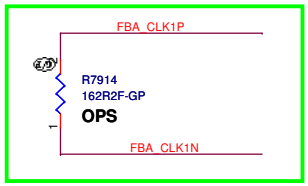
Place close VRAM4 VDDQ ball



Frame Buffer Patition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

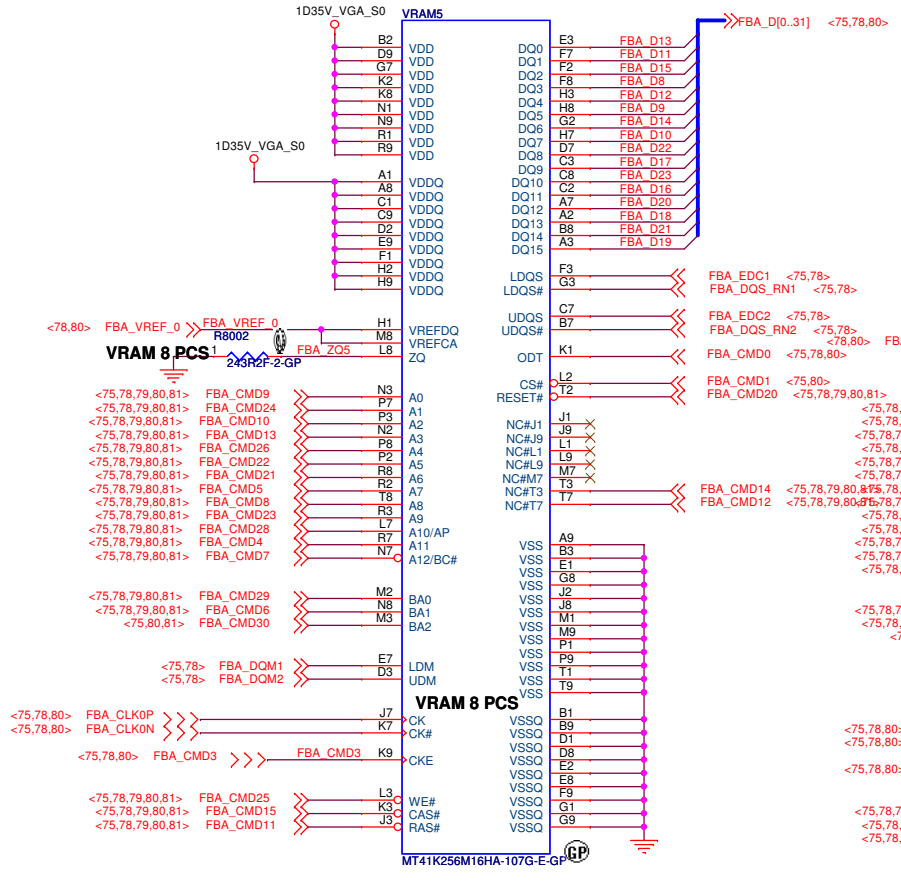
Title: GPU-VRAM3,4 (2/4)

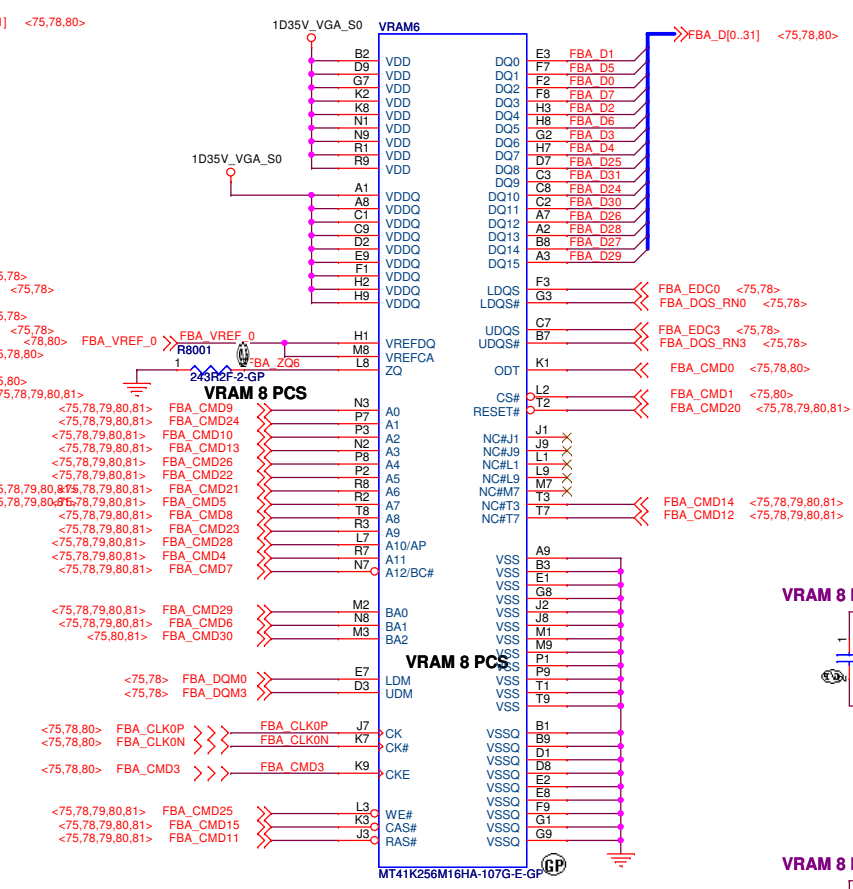
Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 79 of 102

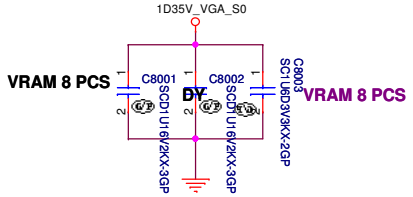
Main Func = dGPU

Data Bits 31:0 RANK 1

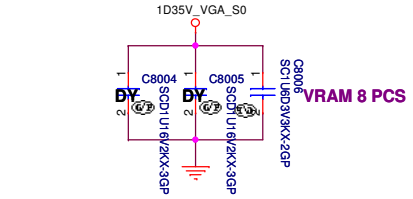




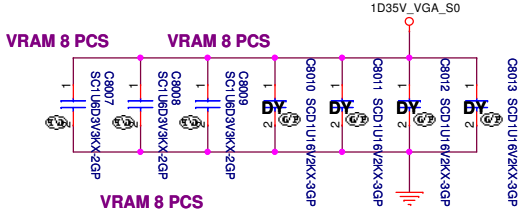
Place close VRAM5 VDD ball



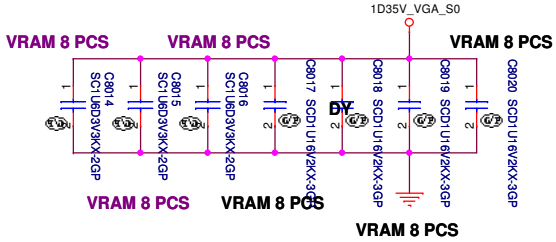
Place close VRAM6 VDD ball



Place close VRAM5VDDQ ball



Place close VRAM6VDDQ ball



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

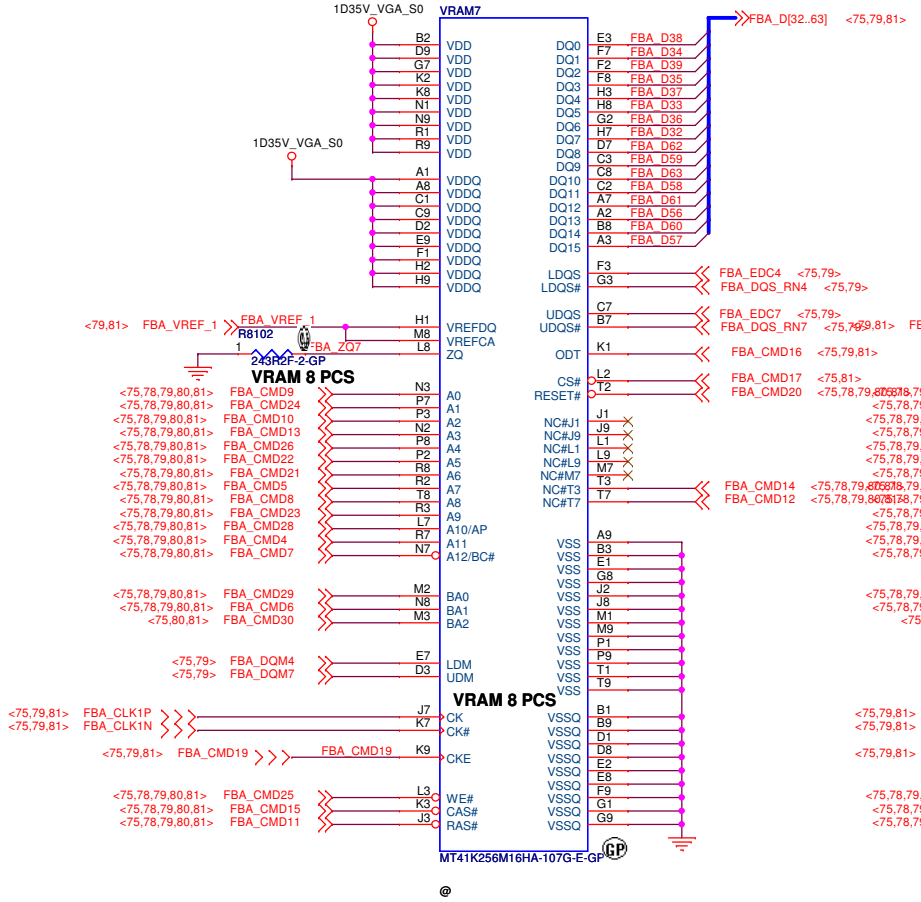
Title: GPU-VRAM5,6 (3/4)

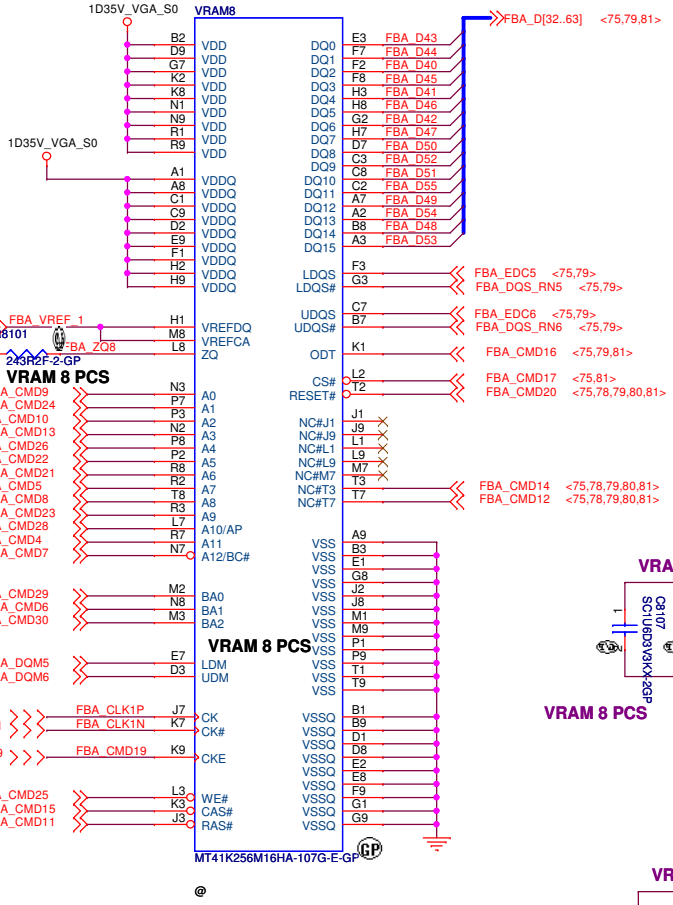
Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 80 of 102

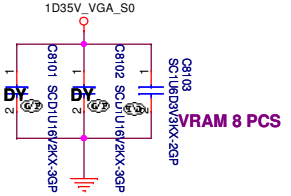
Main Func = dGPU

Data Bits 63:32 RANK 1

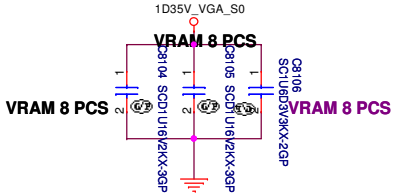




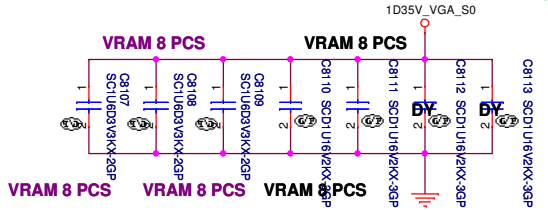
Place close VRAM7 VDD ball



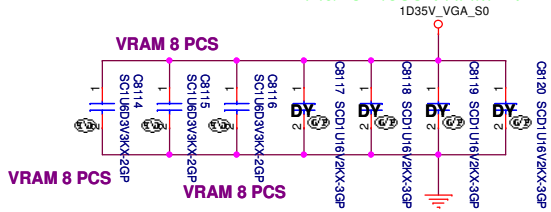
Place close VRAM8 VDD ball



Place close VRAM7 VDDQ ball



Place close VRAM8 VDDQ ball



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: GPU-VRAM7,8 (4/4)

Size: | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 81 of 102

Main Func = dGFX_CORE

PU8203, PU8205, PU8207 and PU8209 manually change to 84.SRA12.037

RT8812AGQW-GP
OPS

OCP setting (current limit ~ 60.3A)
OPS should be in DUMMY column.

For tuning VGA_CORE sequence.

N15V_GM_S
Config D

Design Current=33.5A
56.65A <OCP< 66.7A

Component value	N15V-GM-S Config D	N15-S-GT-S Config B
R1 (PR8222)	27K 64.27025.6DL	20K 64.20025.6DL
R2 (PR8206)	7.5K 64.75015.6DL	20K 64.20025.6DL
R3 (PR8208)	0 63.R0034.1DL	2K 64.20015.6DL
R4+R5 (PR8209)	7.87K 64.78715.6DL	18K 64.18025.6DL
C (PC8223)	5.6nF 78.56222.2FL	2.7nF 78.27224.2FL

78.56222.2FL:OBS REASON: 50V is more popular, chage to 78.56224.2FL

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMAX}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

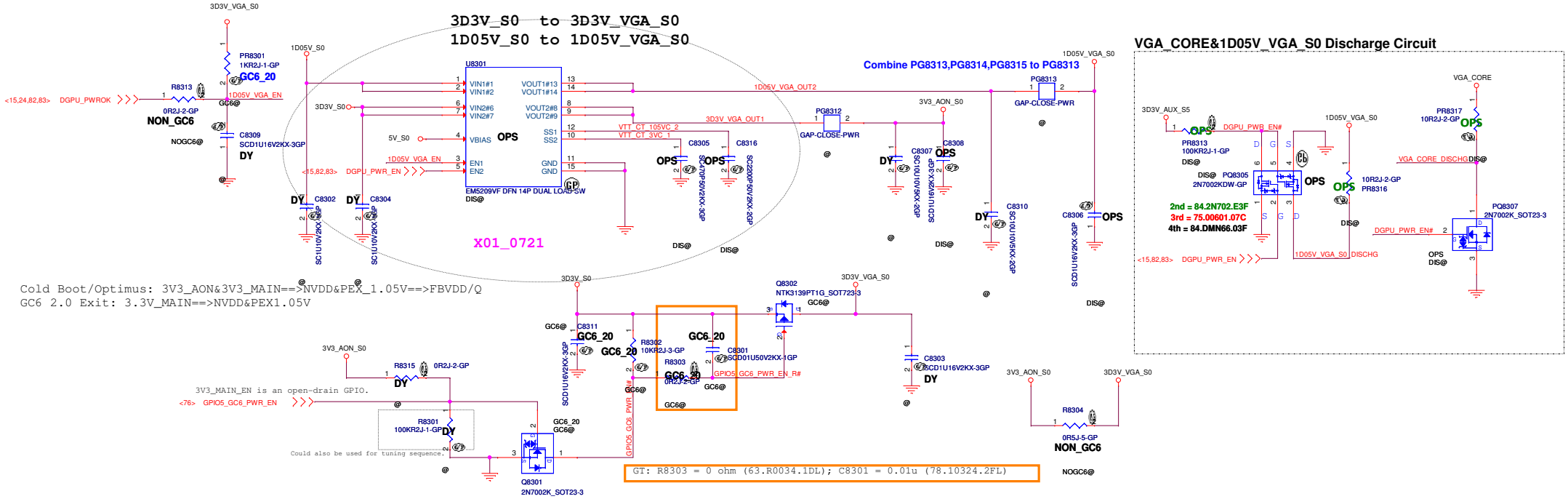
Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	RT8812_VGACORE		
Size	Document Number LA-B483P		Rev A00
Date: Wednesday, January 21, 2015	Sheet 82 of 102		

Main Func = dGPU

3D3V_VGA_S0
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

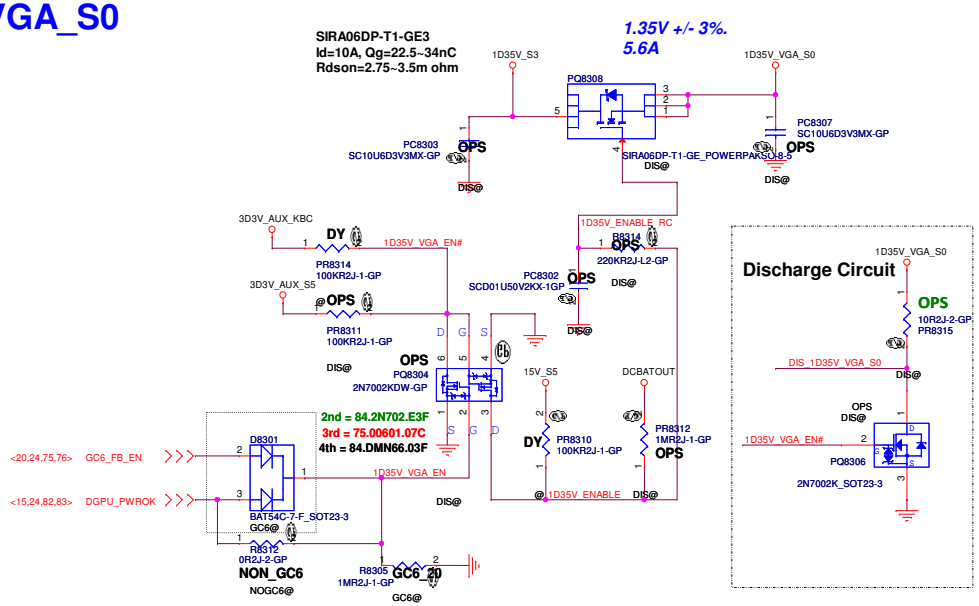


VGA_CORE&1D05V_VGA_S0 Discharge Circuit

1D35V_VGA_S0

SIRA06DP-T1-GE3
Id=10A, Qg=22.5~34nC
Rdson=2.75~3.5m ohm

1.35V +/- 3%.
5.6A



Discharge Circuit

CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/20	Deciphered Date 2015/12/31	Title: DISCRETE VGA POWER
			Size: — Document Number: LA-B483P Rev: A00
			Date: Wednesday, January 21, 2015 Sheet 83 of 102

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size: A	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 64 of 102	

(Blanking)

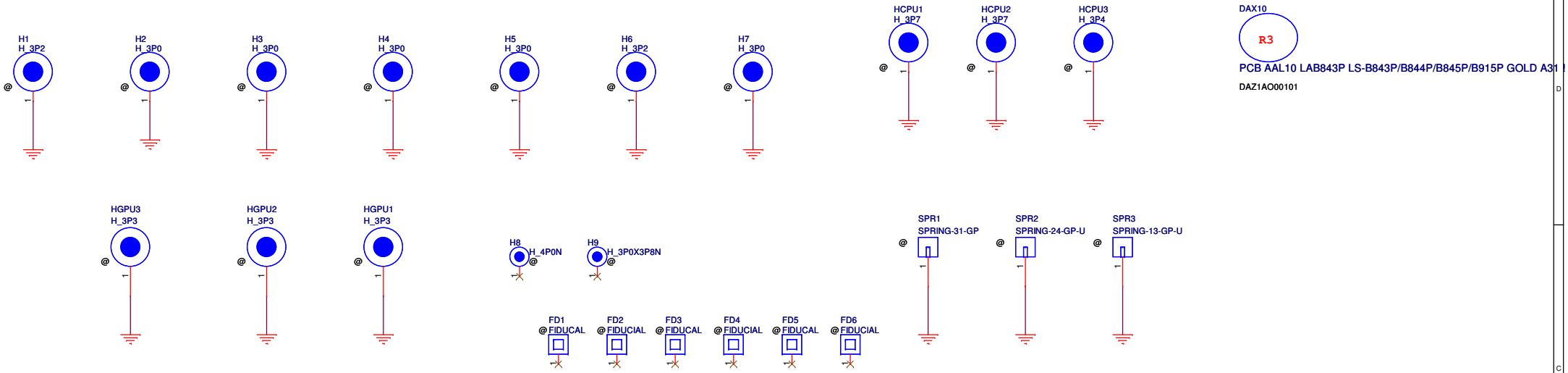
Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

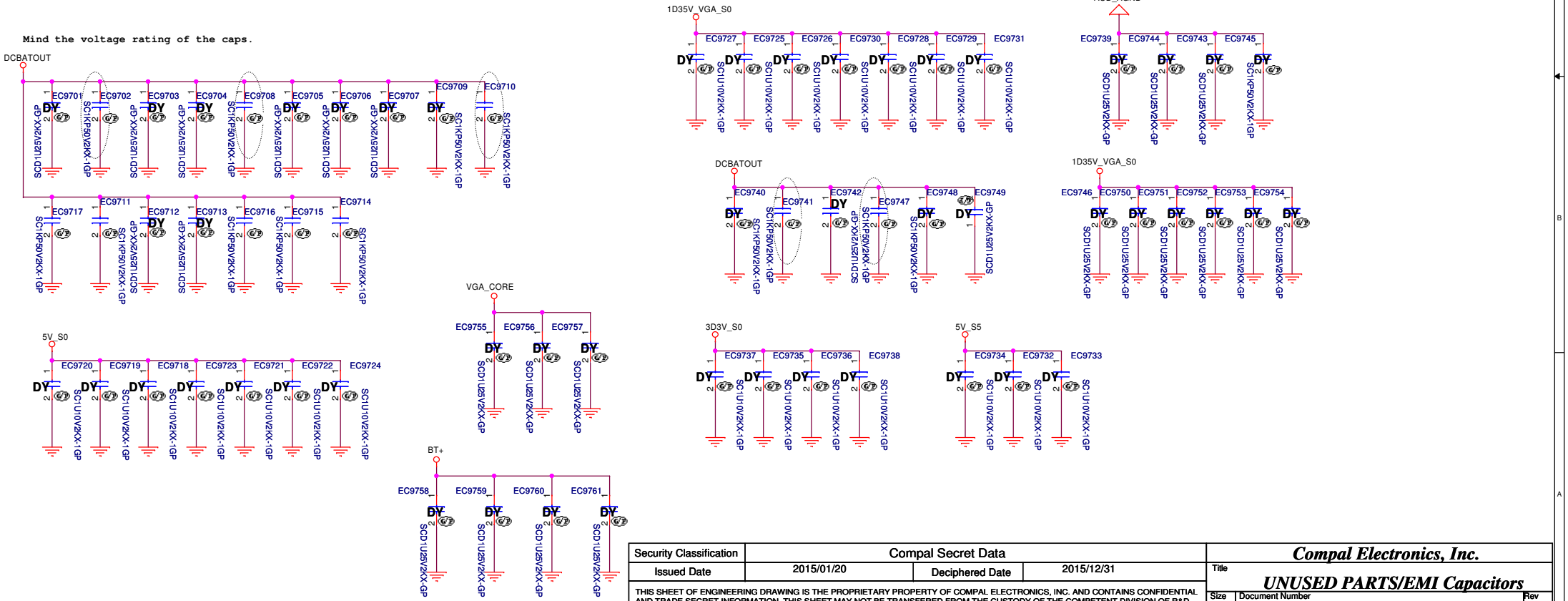
Date: Wednesday, January 21, 2015 | Sheet 85 of 102

Main Func = UnusedParts



Main Func = EMICapacitors

Mind the voltage rating of the caps.



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
	LA-B483P	A00

Date: Thursday, January 22, 2015 | Sheet 86 of 102

(Blanking)

Compal Electronics, Inc.		
Title: Reserved		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 87 of 102	

(Blanking)

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 88 of 102

(Blanking)

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 89 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 90 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.		
Title: Reserved		
Size	Document Number: LA-B483P	Rev: A00
Date: Wednesday, January 21, 2015	Sheet 91 of 102	

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 92 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 93 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 94 of 102

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.

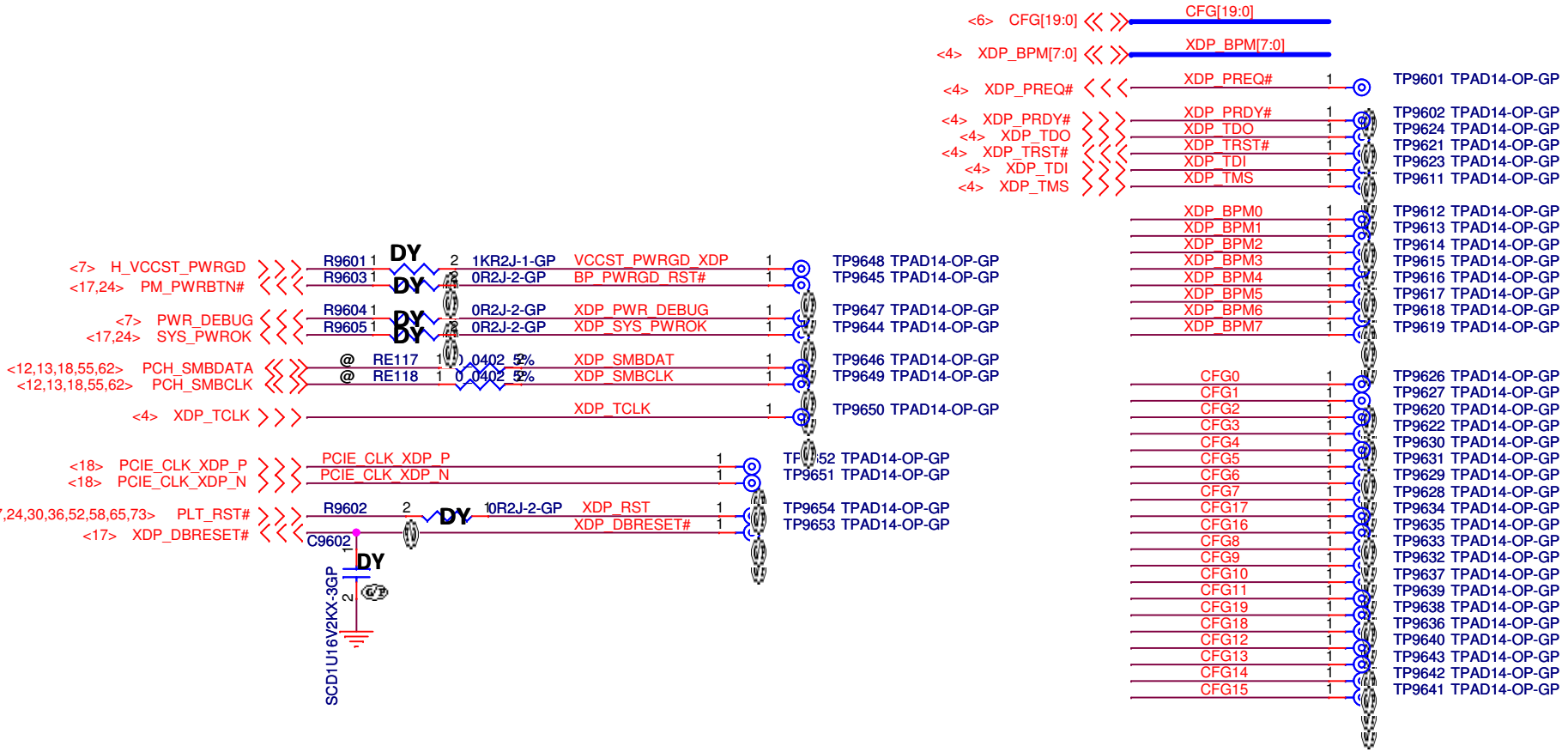
Title: **Reserved**

Size | Document Number: **LA-B483P** | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 95 of 102

Main Func = Debug

CPU XDP



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

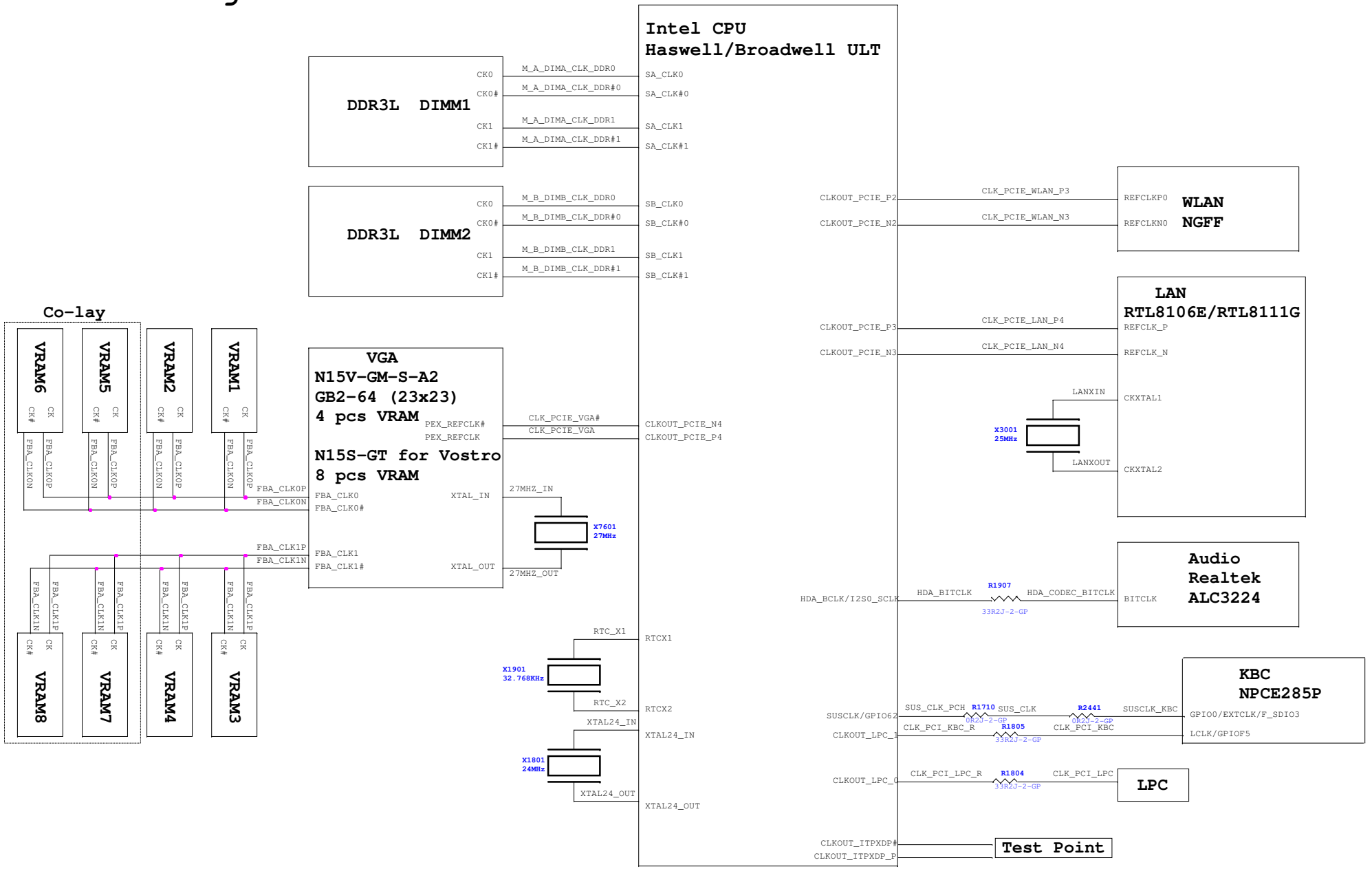
Compal Electronics, Inc.

Title: CPU_XDP;PCH_XDP

Size | Document Number: LA-B483P | Rev: A00

Date: Wednesday, January 21, 2015 | Sheet 96 of 102

CLK Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	CLK Block Diagram		
Size	Document Number		Rev
	LA-B483P		A00
Date:	Wednesday, January 21, 2015	Sheet	97 of 102

Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER

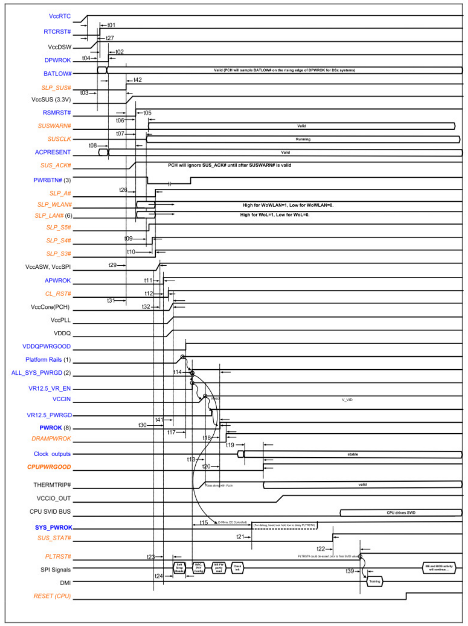
Compal Electronics, Inc.

Title: **Change History**

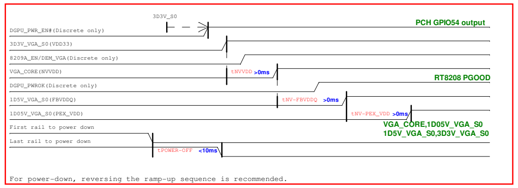
Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 98 of 102

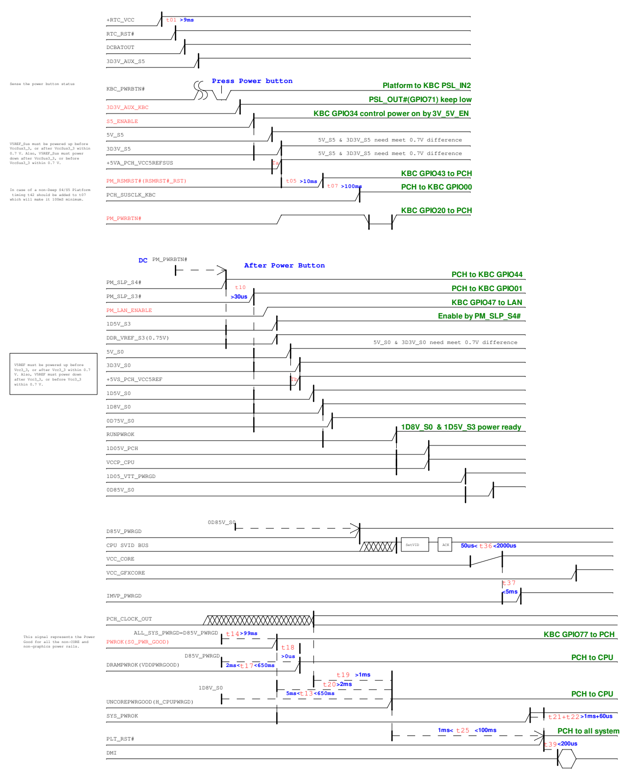
Shark Bay Platform Power Sequence



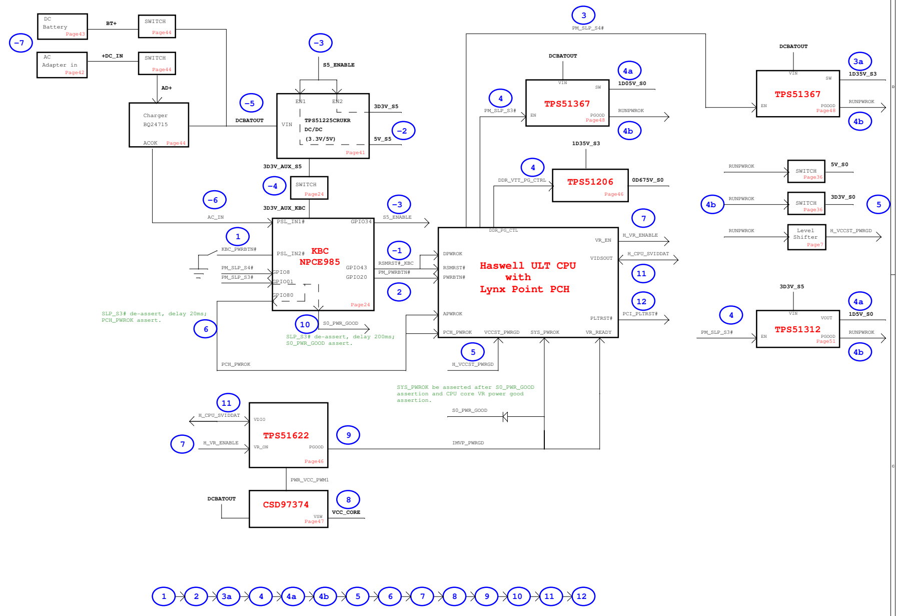
N14P-GT Power-Up/Down Sequence



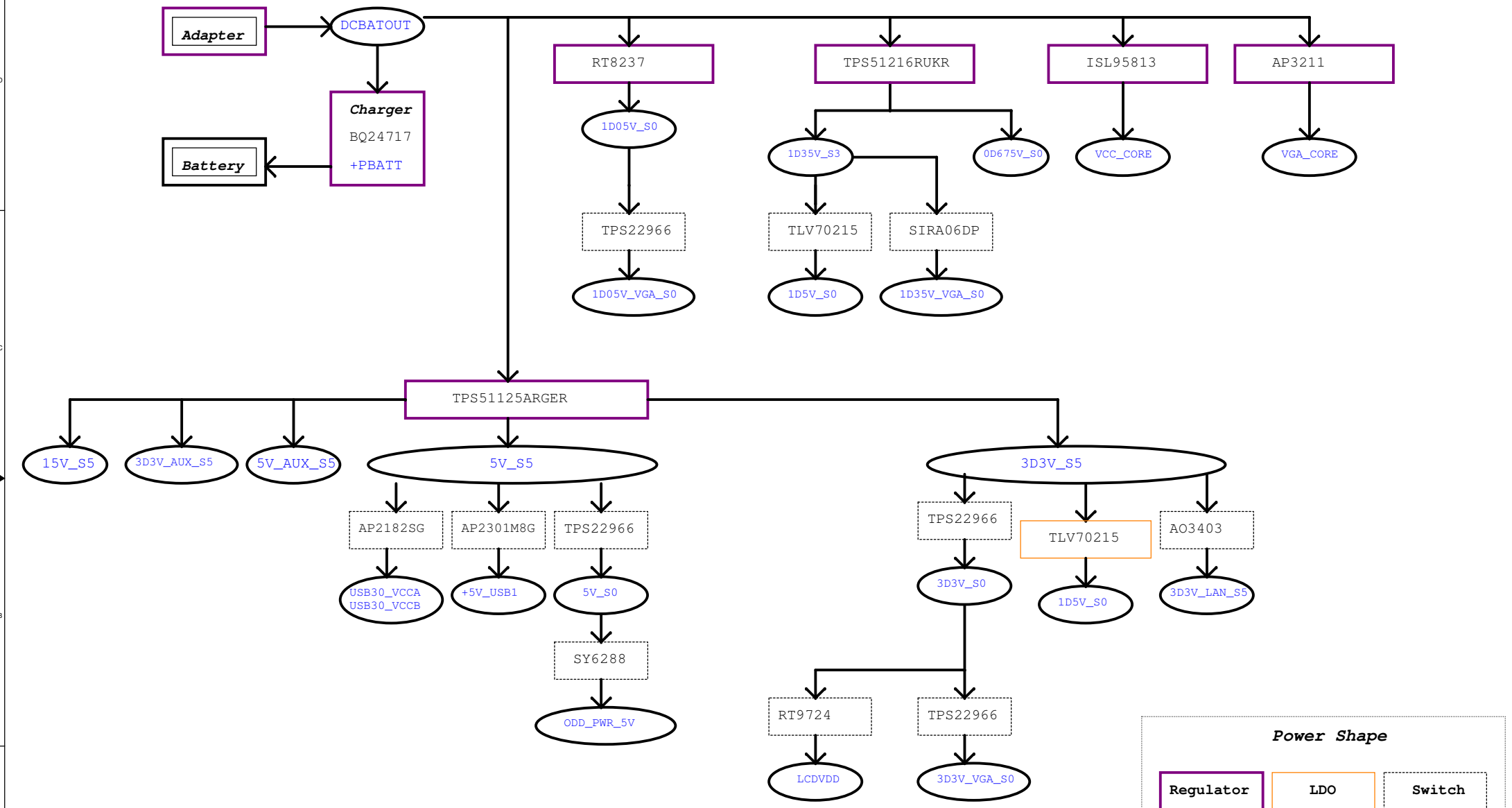
(DC mode)



Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title: Power Sequence
				Size / Document Number: LA-B483P / Rev A00
				Date: Wednesday, January 21, 2015 / Sheet 99 of 102



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

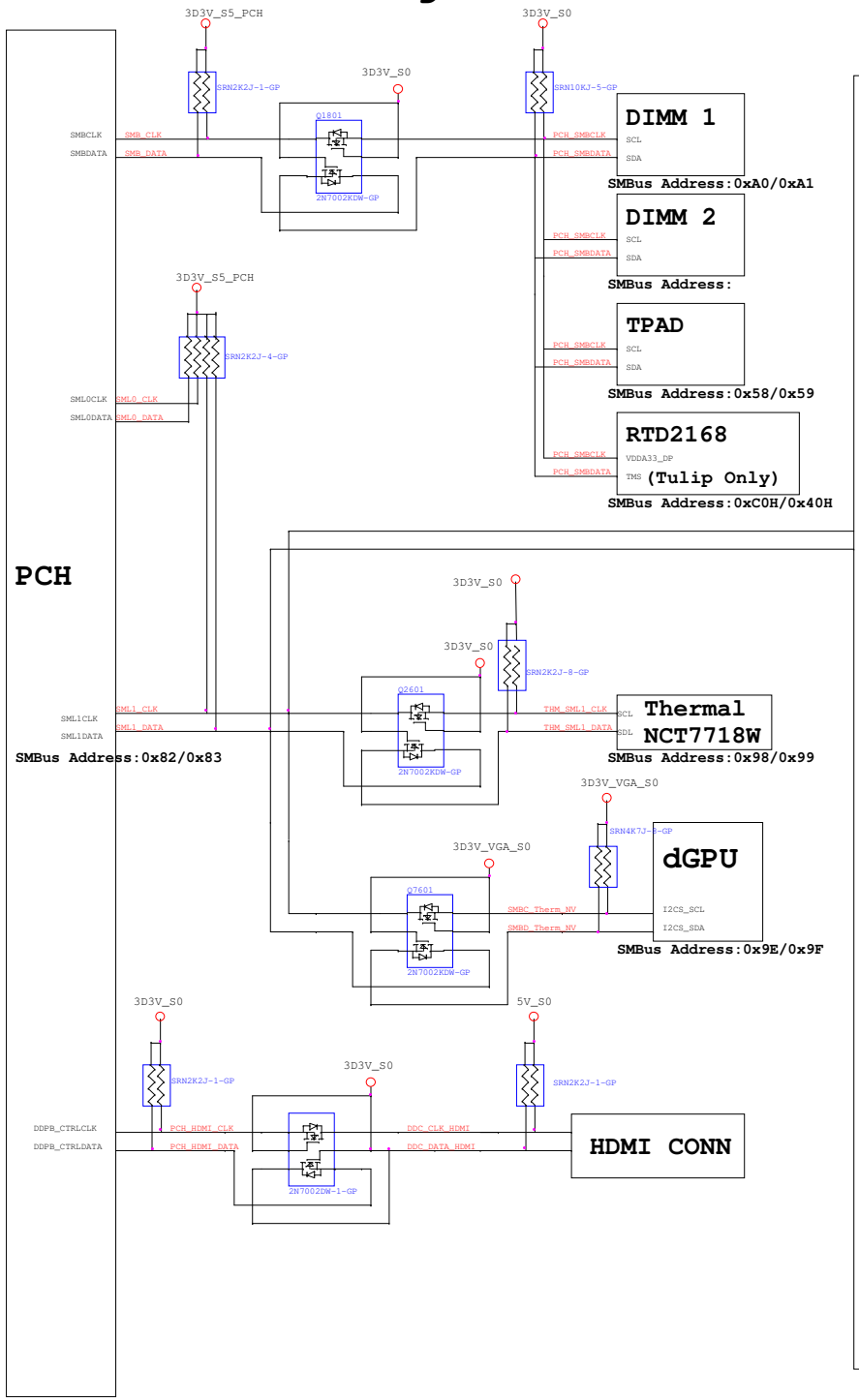
Compal Electronics, Inc.

Title: **Power Block Diagram**

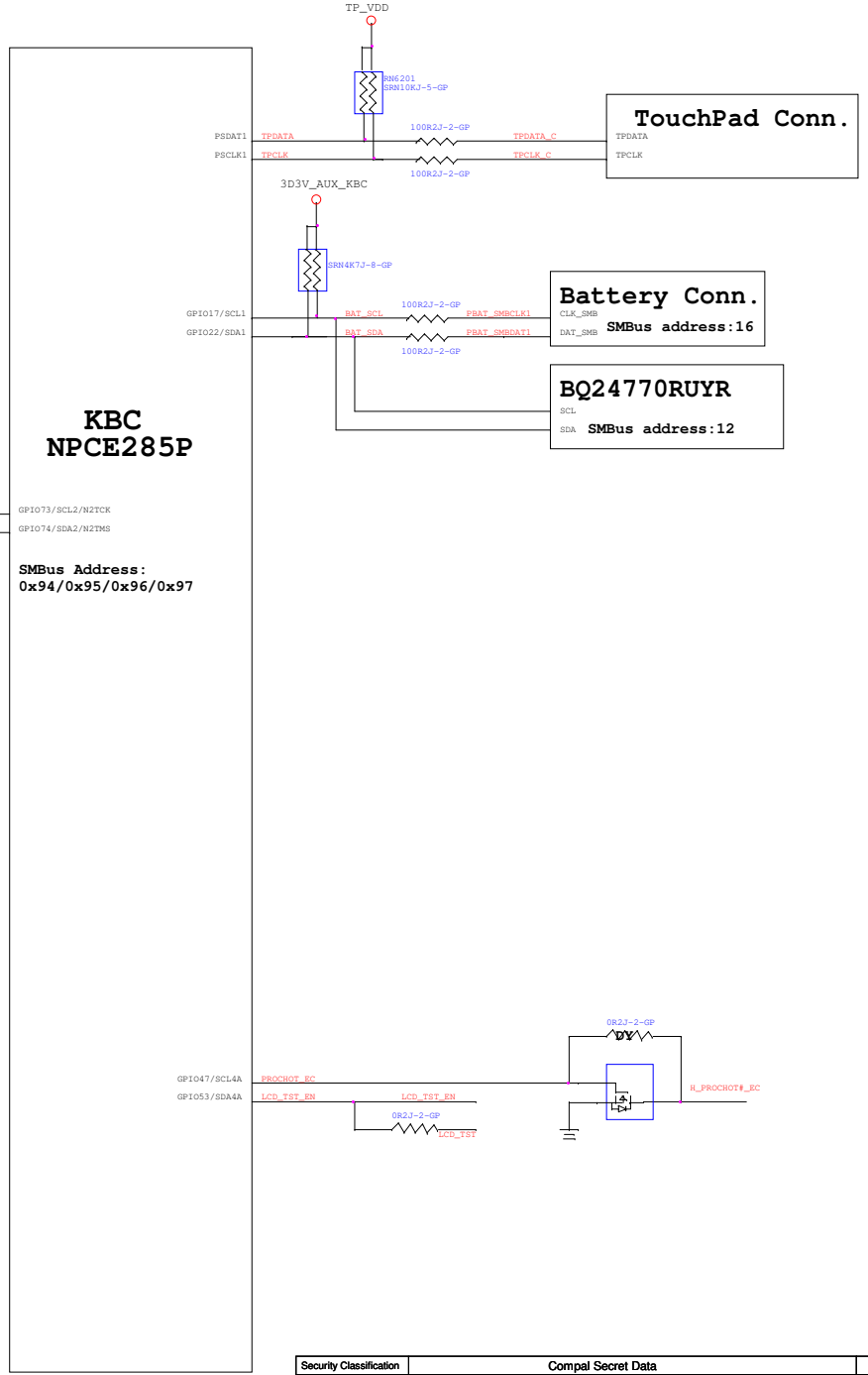
Size	Document Number	Rev
	LA-B483P	A00

Date: Wednesday, January 21, 2015 | Sheet 100 of 102

PCH SMBus Block Diagram



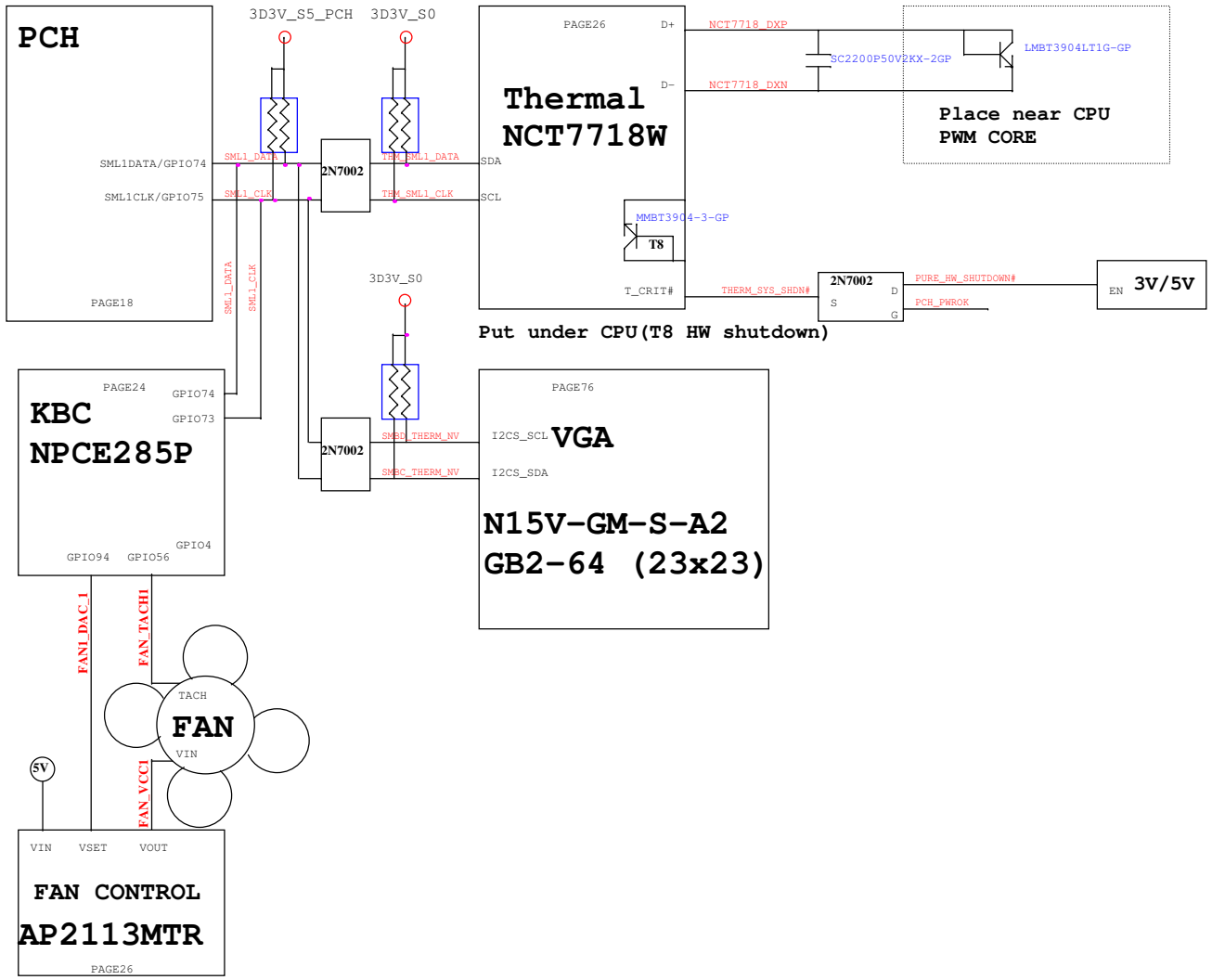
KBC SMBus Block Diagram



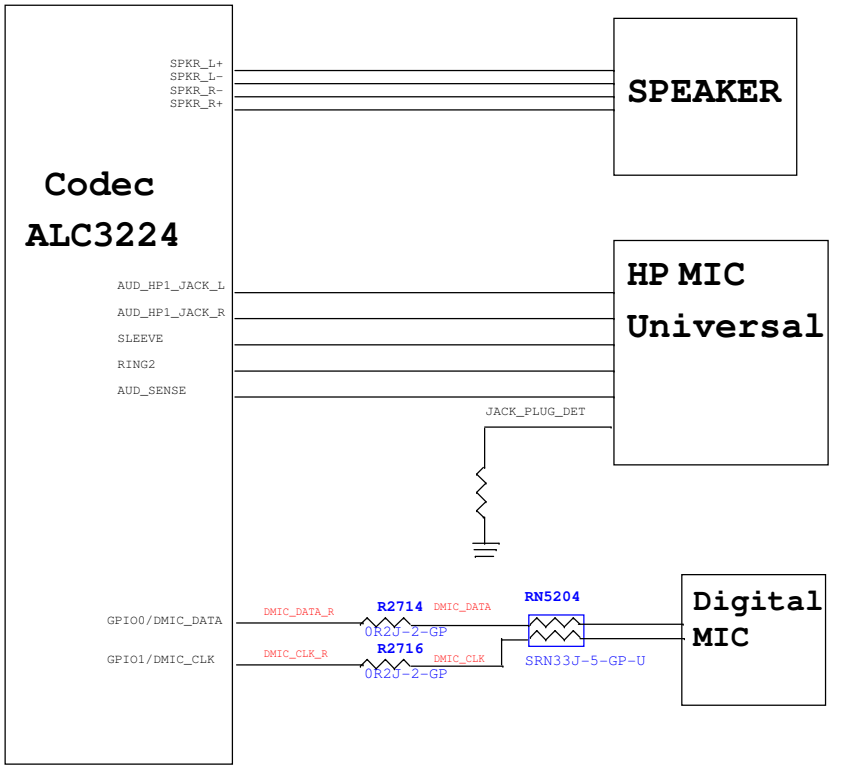
Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SMBUS Block Diagram			
Size	Document Number: LA-B483P		Rev: A00
Date: Wednesday, January 21, 2015	Sheet 101 of 102		

Thermal Block Diagram



Audio Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2015/01/20	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	Thermal/Audio Block Diagram		
Size	Document Number		Rev
	LA-B483P		A00
Date:	Wednesday, January 21, 2015	Sheet	102 of 102