Alba UMA Schematics

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2009-04-06

REV : -1

DY : Nopop Component

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 1 of 61

ALBA UMA Block Diagram

Project code : 91.4BK01.001
Part Number : 48.4BK04.0SA
PCB P/N : 08243
Revision : SA

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Clock Generator
SLG8SP513VTR 7

Intel Mobile CPU
Penryn
Socket P 8,9

FSB
800/1066MHz

Intel
Cantiga-GM
AGTL+ CPU I/F
DDR Memory I/F
External Graphics
10,11,12,13,14,15

CRT 42
LCD 41
RGB CRT
LVDS(Dual Channel)

DDRII 800 Channel A
DDR II 800 Channel B

DDRII 800 Slot 0 16
DDRII 800 Slot 1 17

DMIx4
CONTROL-LINK

Intel
ICH9-M
USB 2.0/1.1 ports (12)
PCI Express ports (6)
High Definition Audio
SATA ports (4)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
18,19,20,21

Power SW
TPS2231RGP 50

New Card
(On Express Card board) 50
PCIE x 1 & USB 2.0 x 1

10/100 LOM
RTL8103EL 25
PCIE x 1

RJ45 CONN 42

Left Side:
USB x 2 46
USB 2.0 x 2

PCIE

Mini-Card
802.11a/b/g/n 43
PCIE x 1

CAMERA
(Option) 47
USB 2.0 x 1

USB 2.0

Bluetooth 45
USB 2.0 x 1

Right Side:
USB x 1 51
USB 2.0 x 1

LPC Bus

CardReader
Realtek
RTS5159 50
USB2.0

(7 in 1)SD/MMC
MS/MS Pro/xD
(On Express Card board)

RJ11 42
MDC MODEM 46
AZALIA

Digital Mic Array
(Option) 47
Internal Mic 44

Azalia
CODEC
OP AMP
IDT
92HD81 22
AZALIA

MIC IN
HP OUT
(On Express Card board)

2CH SPEAKER 44

SATA
SATA

HDD 44
ODD 44

SPI

KBC
WINBOND
WPCE773L 26

Flash ROM
2MB 47
Touch PAD 45
Int. KB 45
Thermal & Fan
EMC2102 28,44

ISL6266A/CPU_CORE 34,35

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

TPS51117/1.05V 36

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

TPS51125/3V,5V 33

INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

TPS51116/1.8V,0.9V 38

INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

L6935TR/1.5V 37

INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

MAX8731A/CHARGER 32

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

RUN PWR/3V,5V 30

INPUTS	OUTPUTS
+5V_ALW +3.3V_ALW	+5V_RUN +3.3V_RUN

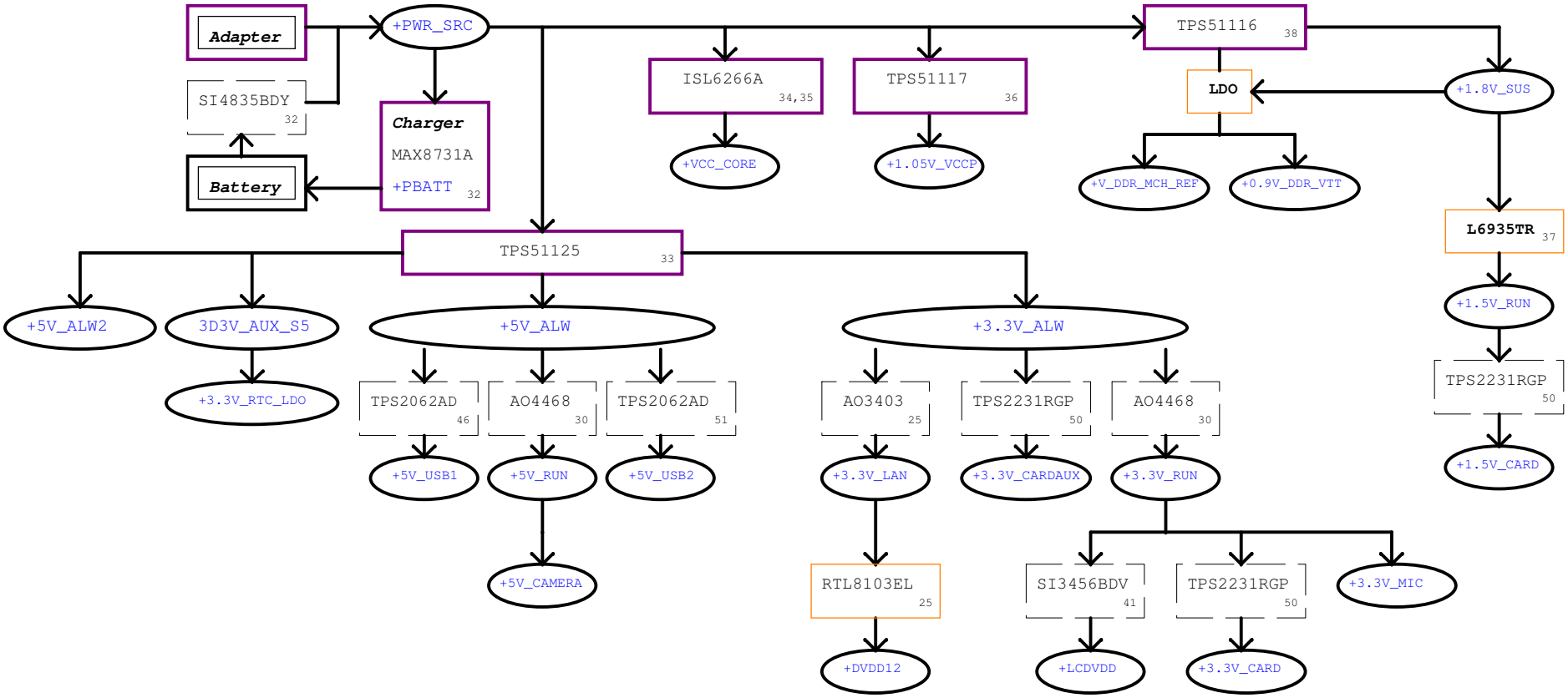
Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 2 of 61



Power Shape

Regulator	LDO	Switch

Alba UMA

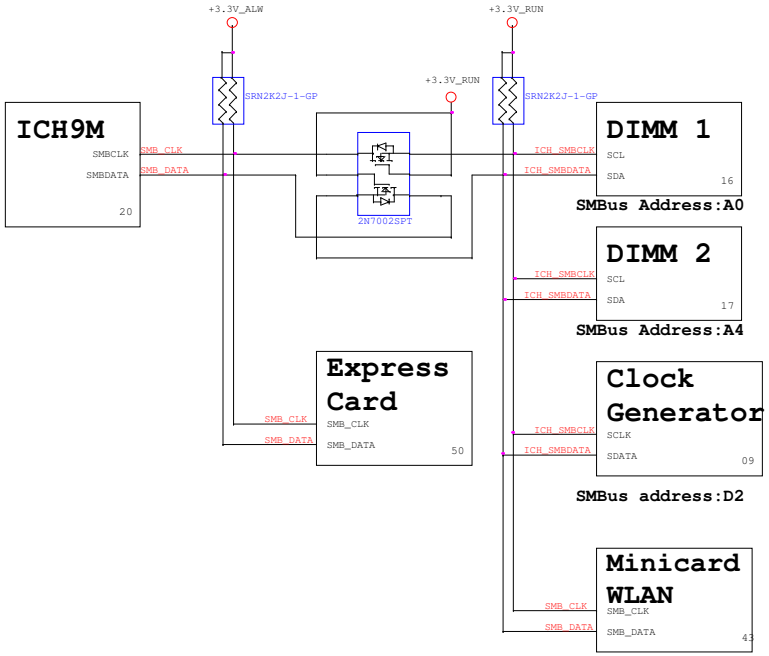
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

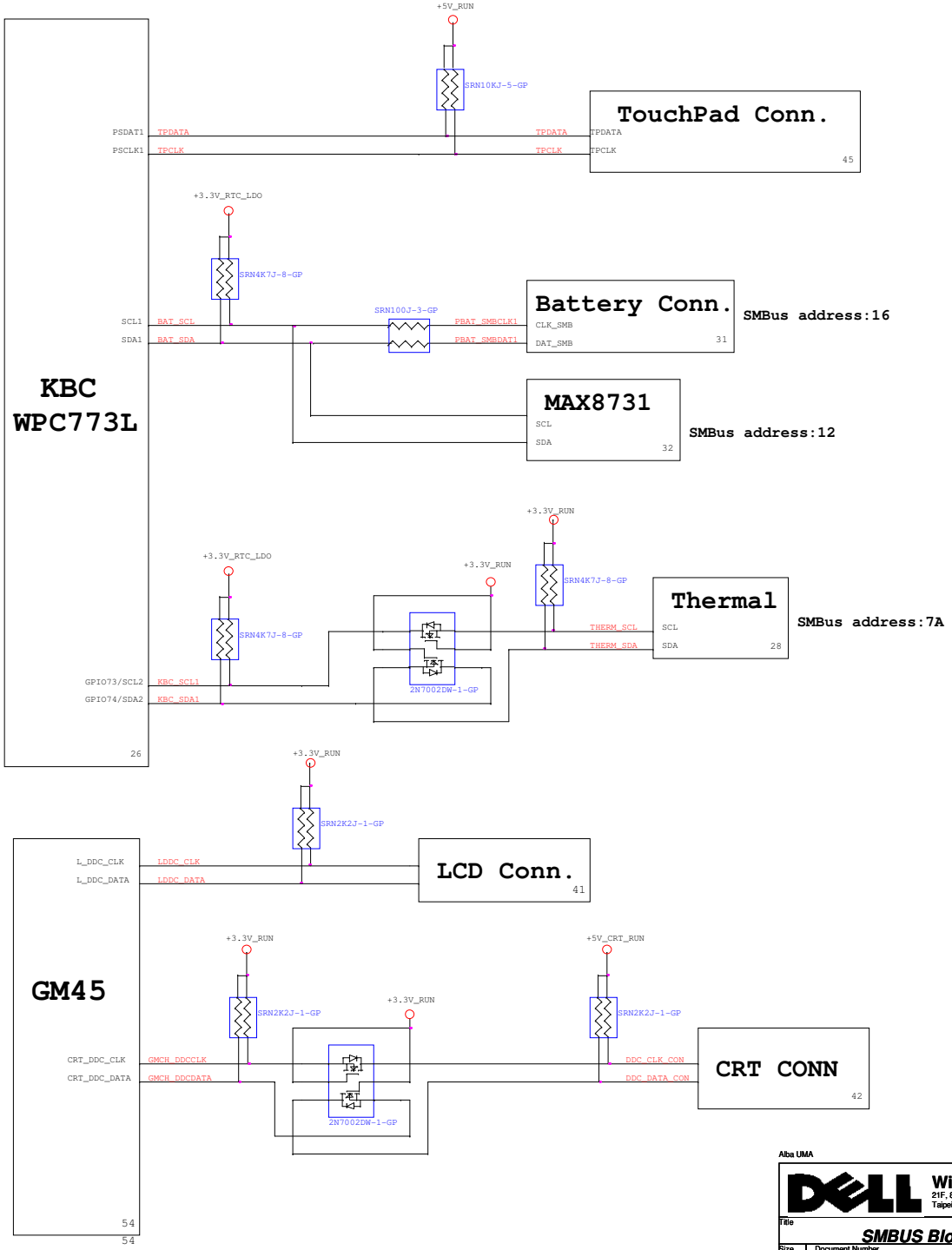
Size	Document Number	Rev
Custom	***Alba UMA***	-1

Date: Monday, April 06, 2009 Sheet 3 of 61

ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



Alba UMA

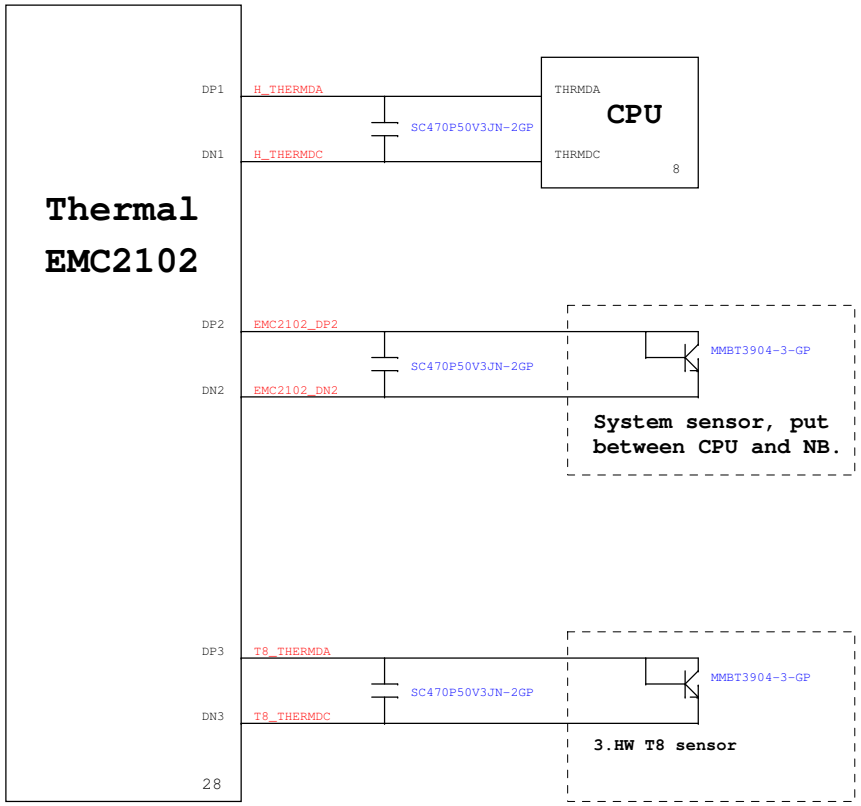
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

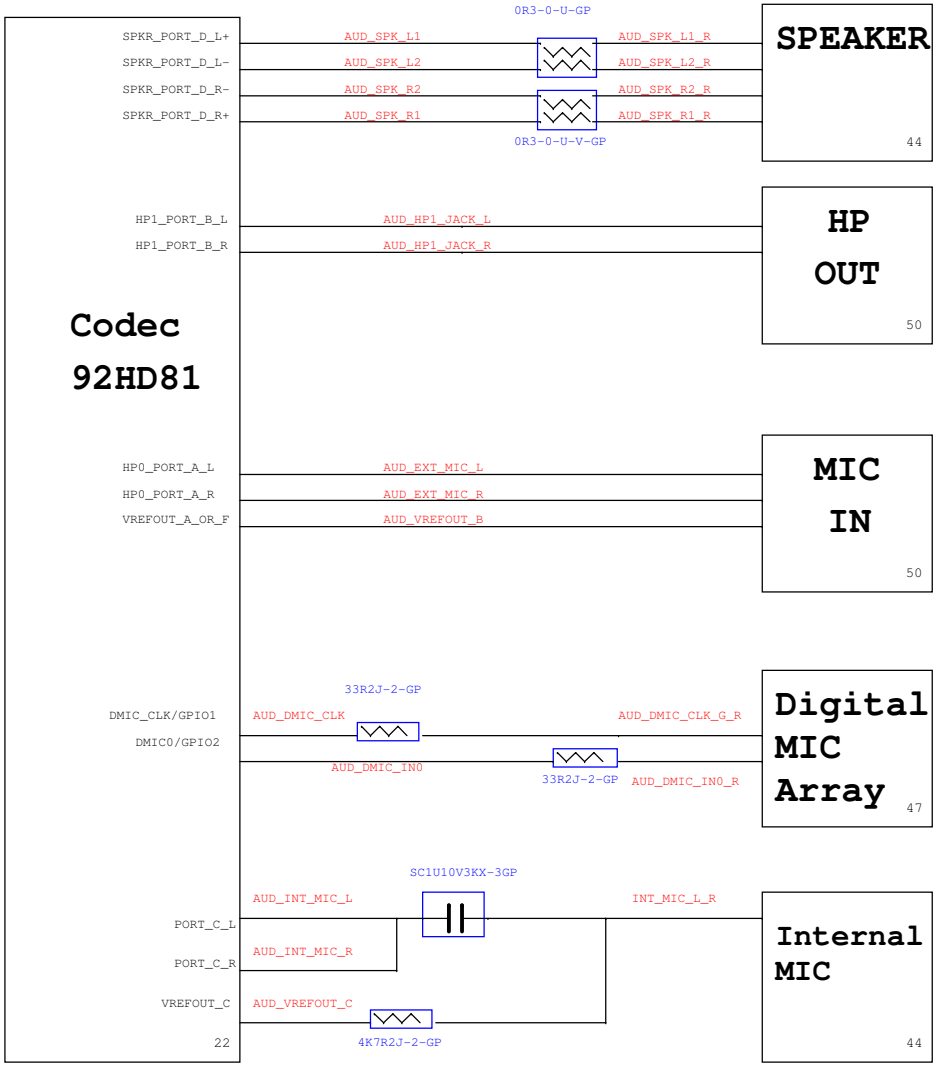
Size	Document Number	Rev
C	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 4 of 61

Thermal Block Diagram



Audio Block Diagram



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 5 of 61

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Alba UMA

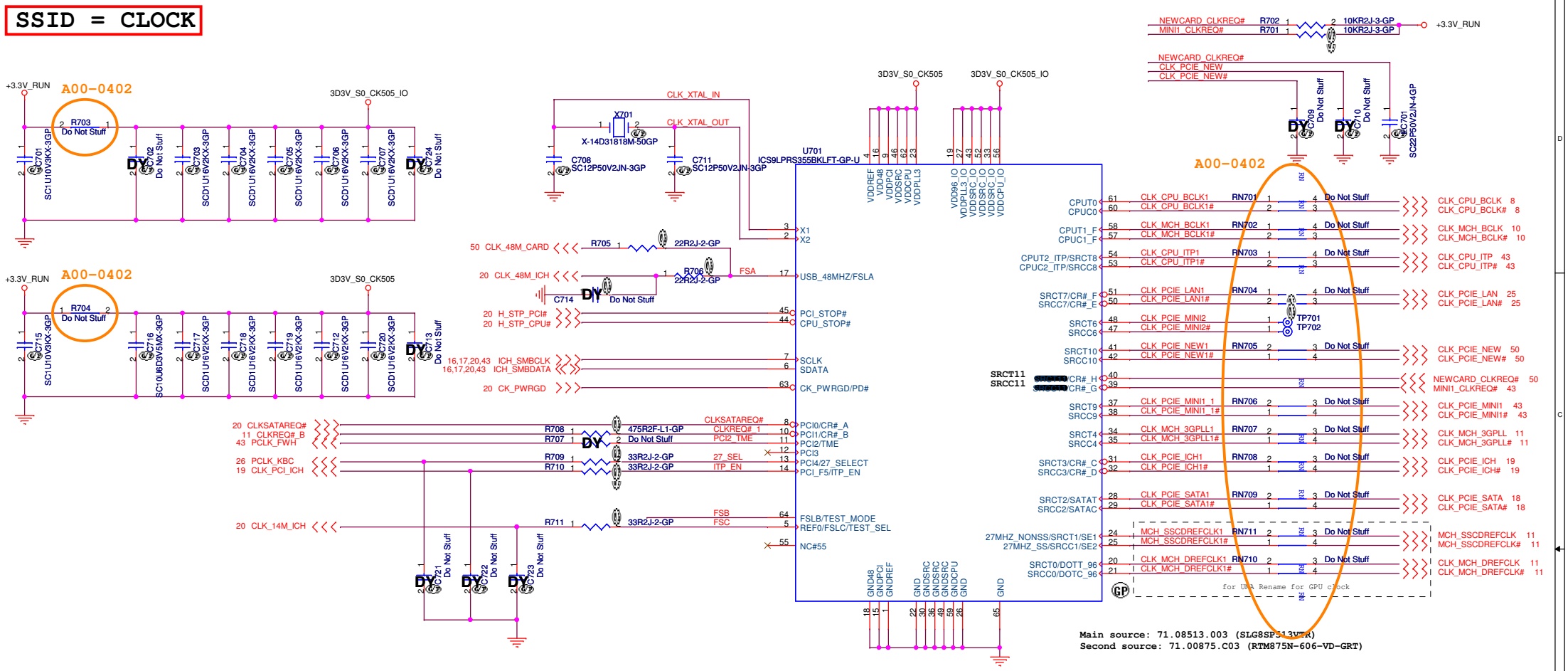
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

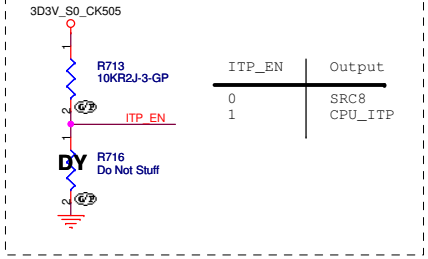
Title: Table of Content

Size: Custom | Document Number: Alba UMA | Rev: -1

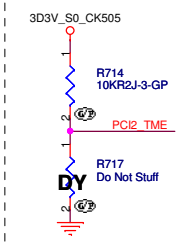
Date: Monday, April 06, 2009 | Sheet 6 of 61

SSID = CLOCK

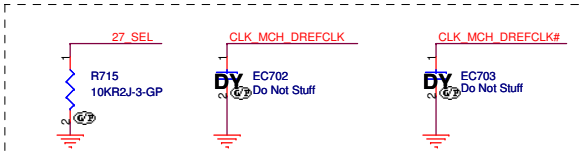




ITP_EN	Output
0	SRC8
1	CPU_ITP

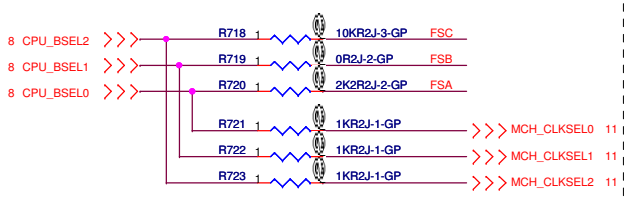


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed



27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	UMA
1	SRCT0	SRCC0	Discrete

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator SLG8SP513VTR

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 7 of 61

SSID = CPU

CPU1A 1 OF 4

ADDR GROUP 0

ADDR GROUP 1

XDP/ITP SIGNALS

THERMAL

ICH

HCLK

RESERVED

BGA479-SKT6-GPU7

62.10040.221

CPU1B 2 OF 4

DATA GRP2

DATA GRP3

MISC

BGA479-SKT6-GPU7

62.10040.221

H_THRMTRIP# should connect to ICH9 and MCH without T-ing.

Layout notes

Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

X01-0112

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-FSB(1/2)

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 8 of 61

SSID = CPU

X01-0106

X01-0106

X01-0106

A00-0402

layout note: "+1.5V_VCCA" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

VCC_SENSE and VSS_SENSE lines should be of equal length.

NCTF PIN

CPU1C 3 OF 4

BGA479-SKT6-GPU7
62.10040.221

CPU1D 4 OF 4

BGA479-SKT6-GPU7
62.10040.221

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-Power(2/2)

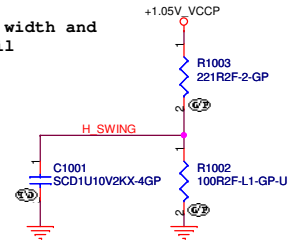
Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 9 of 61

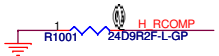
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

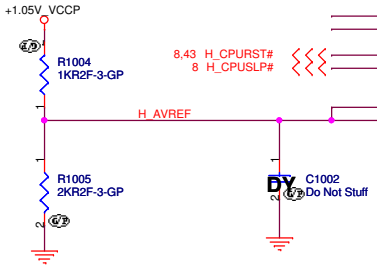
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)

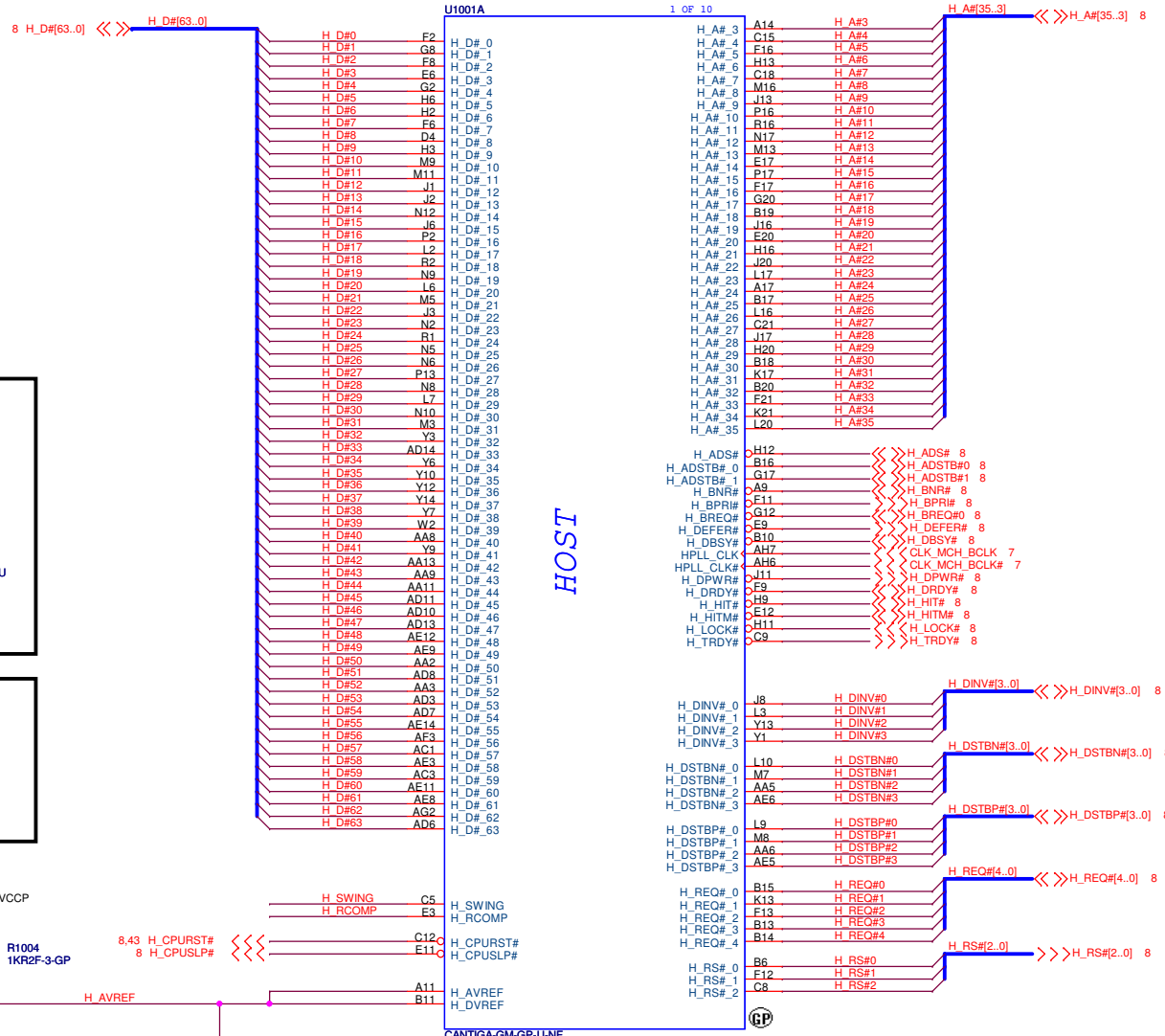


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")





Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cantiga-HOST(1/6)***

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 10 of 61

SSID = MCH

★ is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 ★
CFG 6	ITPM enable	ITPM disable ★
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality ★
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder ★
CFG 10	PCIE loopback enable	PCIE loopback disable ★
CFG 12	ALLZ mode enable	ALLZ mode disable ★
CFG 13	XOR mode enable	XOR mode disable ★
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable ★
CFG 19 DMI Lane Reserved	Normal operation ★	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational ★	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable ★	SDVO interface enable
L_DDC_DATA	LFP disable ★	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled ★	SDVO/iHDMI/DP interface enabled

U1001B — 2 OF 10 — CANTIGA-GM-GP-U-NF

RSVD: M36 RESERVED#M36, N36 RESERVED#N36, R33 RESERVED#R33, T33 RESERVED#T33, AH9 RESERVED#AH9, AH10 RESERVED#AH10, AH12 RESERVED#AH12, AH13 RESERVED#AH13, K12 RESERVED#K12, AL34 RESERVED#AL34, AK34 RESERVED#AK34, AN35 RESERVED#AN35, AM35 RESERVED#AM35, T24 RESERVED#T24, B31 RESERVED#B31, B2 RESERVED#B2, M1 RESERVED#M1, AY21 RESERVED#AY21, BG23 RESERVED#BG23, BF23 RESERVED#BF23, BH18 RESERVED#BH18, BF18 RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0 AP24 M_CLK_DDR0 16; SA_CK_1 AT21 M_CLK_DDR1 16; SB_CK_0 AV24 M_CLK_DDR2 17; SB_CK_1 AU20 M_CLK_DDR3 17; SA_CK#_0 AR24 M_CLK_DDR#0 16; SA_CK#_1 AR21 M_CLK_DDR#1 16; SB_CK#_0 AU24 M_CLK_DDR#2 17; SB_CK#_1 AV20 M_CLK_DDR#3 17; SA_CKE_0 BC28 M_CKE0 16; SA_CKE_1 AY28 M_CKE1 16; SB_CKE_0 AY36 M_CKE2 17; SB_CKE_1 BB36 M_CKE3 17; SA_CS#_0 BA17 M_CS0# 16; SA_CS#_1 AY16 M_CS1# 16; SB_CS#_0 AV16 M_CS2# 17; SB_CS#_1 AR13 M_CS3# 17; SA_ODT_0 BD17 M_ODT0 16; SA_ODT_1 AY17 M_ODT1 16; SB_ODT_0 BF15 M_ODT2 17; SB_ODT_1 AY13 M_ODT3 17; SM_RCOMP BG22 M_RCOMPP; SM_RCOMP# BH21 M_RCOMPN; SM_RCOMP_VOH BF28 SM_RCOMP_VOH; SM_RCOMP_VOL BH28 SM_RCOMP_VOL; SM_VREF AV42 CANTIGA_SM_VREF; SM_PWROK AR36; SM_REXT BF17 SM_REXT; SM_DRAMRST# BC36

CLK: DPLL_REF_CLK B38 CLK_MCH_DREFCLK; DPLL_REF_CLK# A38 CLK_MCH_DREFCLK#; DPLL_REF_SSCLK E41 MCH_SSCDREFCLK; DPLL_REF_SSCLK# F41 MCH_SSCDREFCLK#; PEG_CLK F43 CLK_MCH_3GPLL; PEG_CLK# E43 CLK_MCH_3GPLL#

DMI: DMI_RXN_0 AE41 DMI_ITXN0_MRXN0; DMI_RXN_1 AE37 DMI_ITXN1_MRXN1; DMI_RXN_2 AE47 DMI_ITXN2_MRXN2; DMI_RXN_3 AH39 DMI_ITXN3_MRXN3; DMI_RXP_0 AE40 DMI_ITXP0_MRXP0; DMI_RXP_1 AE38 DMI_ITXP1_MRXP1; DMI_RXP_2 AE48 DMI_ITXP2_MRXP2; DMI_RXP_3 AH40 DMI_ITXP3_MRXP3; DMI_TXN_0 AE35 DMI_IRXN0_MTXN0; DMI_TXN_1 AE43 DMI_IRXN1_MTXN1; DMI_TXN_2 AE46 DMI_IRXN2_MTXN2; DMI_TXN_3 AH42 DMI_IRXN3_MTXN3; DMI_TXP_0 AD35 DMI_IRXP0_MTXP0; DMI_TXP_1 AE44 DMI_IRXP1_MTXP1; DMI_TXP_2 AE46 DMI_IRXP2_MTXP2; DMI_TXP_3 AH43 DMI_IRXP3_MTXP3

CFG: CFG_0 T25, CFG_1 R25, CFG_2 P25, CFG_3 P20, CFG_4 P24, CFG_5 C25, CFG_6 N24, CFG_7 M24, CFG_8 F21, CFG_9 C23, CFG_10 C24, CFG_11 N21, CFG_12 P21, CFG_13 T21, CFG_14 R20, CFG_15 M20, CFG_16 L21, CFG_17 H21, CFG_18 P29, CFG_19 R28, CFG_20 T28

GRAPHICS VID: GFX_VID_0 B33, GFX_VID_1 B32, GFX_VID_2 G33, GFX_VID_3 F33, GFX_VID_4 E33; GFX_VR_EN C34

PM: PM_SYNC# R29, PM_DPRSTP# B7, PM_EXT_TS#_0 N33, PM_EXT_TS#_1 P32, PWROK AT40, RSTIN# AT11, THERMTRIP# T20, DPRSLPVR R32

ME: CL_CLK AH37, CL_DATA AH36, CL_PWROK AN36, CL_RST# AJ35, CL_VREF AH34 MCH_CLVREF

MISC: DDPC_CTRLCLK N28, DDPC_CTRLDATA M28, SDVO_CTRLCLK G36, SDVO_CTRLDATA E36, CLKREQ# K36, ICH_SYNC# H36, TSATN# B12

HDA: HDA_BCLK B28, HDA_RST# B30, HDA_SDI B29, HDA_SDO C29, HDA_SYNC A28

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

+1.8V_SUS
R1126 80D6R2F-L-GP
R1125 80D6R2F-L-GP
R1113 1KR2F-3-GP
R1109 3K01R2F-3-GP
R1111 1KR2F-3-GP
SM_RCOMP_VOH
SM_RCOMP_VOL
C1104 SC2D2U10V3KX-1GP
C1105 SCD01U16V2KX-3GP
C1102 SC2D2U10V3KX-1GP
C1103 SCD01U16V2KX-3GP

+1.8V_SUS
R1119 DY Do Not Stuff
R1139 Do Not Stuff
A00-0402
V_DDR_MCH_REF
R1123 499R2F-2-GP
DY C144 Do Not Stuff
DY C1143 Do Not Stuff
DY R1129 Do Not Stuff

+3.3V_RUN
RN1101 SRN10KJ-5-GP: PM_EXTTS#0, PM_EXTTS#1
R1105 DY Do Not Stuff CFG11
R1115 DY Do Not Stuff CFG18
R1110 DY Do Not Stuff CFG19
R1112 DY Do Not Stuff CFG20
R1128 DY Do Not Stuff CFG5
R1108 DY Do Not Stuff CFG6
R1107 DY Do Not Stuff CFG7
R1103 DY Do Not Stuff CFG8
R1127 DY Do Not Stuff CFG9
R1124 DY Do Not Stuff CFG10
R1102 DY Do Not Stuff CFG12
R1106 DY Do Not Stuff CFG13
R1104 DY Do Not Stuff CFG16

FSB setting
7 MCH_CLKSEL0
7 MCH_CLKSEL1
7 MCH_CLKSEL2
TP1103
TP1105
TP1101
TP1102
TP1104

20 PM_SYNC#
8,18,34 H_DPRSTP#
16 PM_EXTTS#0
17 PM_EXTTS#1
PWROK_R
RSTIN#
20,26,28 PM_PWROK
R1118 0R2J-2-GP
19,25,26,43,50 PLT_RST#
R1101 100R2J-2-GP
C1101 DY Do Not Stuff
8,18,26,30,54 H_THRMTRIP#
20,34 DPRSLPVR

+1.05V_VCCP
R1114 1KR2F-3-GP
C1106 SCD1U10V2KX-4GP
R1116 499R2F-2-GP
MCH_CLVREF ~= 0.35V
CL_CLK0 20
CL_DATA0 20
M_PWROK 20
CL_RST#0 20
CLKREQ#_B 7
MCH_ICH_SYNC# 20
TP1106

+1.05V_VCCP
+3.3V_RUN
R1121 56R2J-4-GP
R1122 DY Do Not Stuff
TSATN#_KBC
TSATN#_KBC 26
TSATN#
Q1101 DY Do Not Stuff GP
+3.3V_RUN
CLKREQ#_B
R1117 10KR2J-3-GP

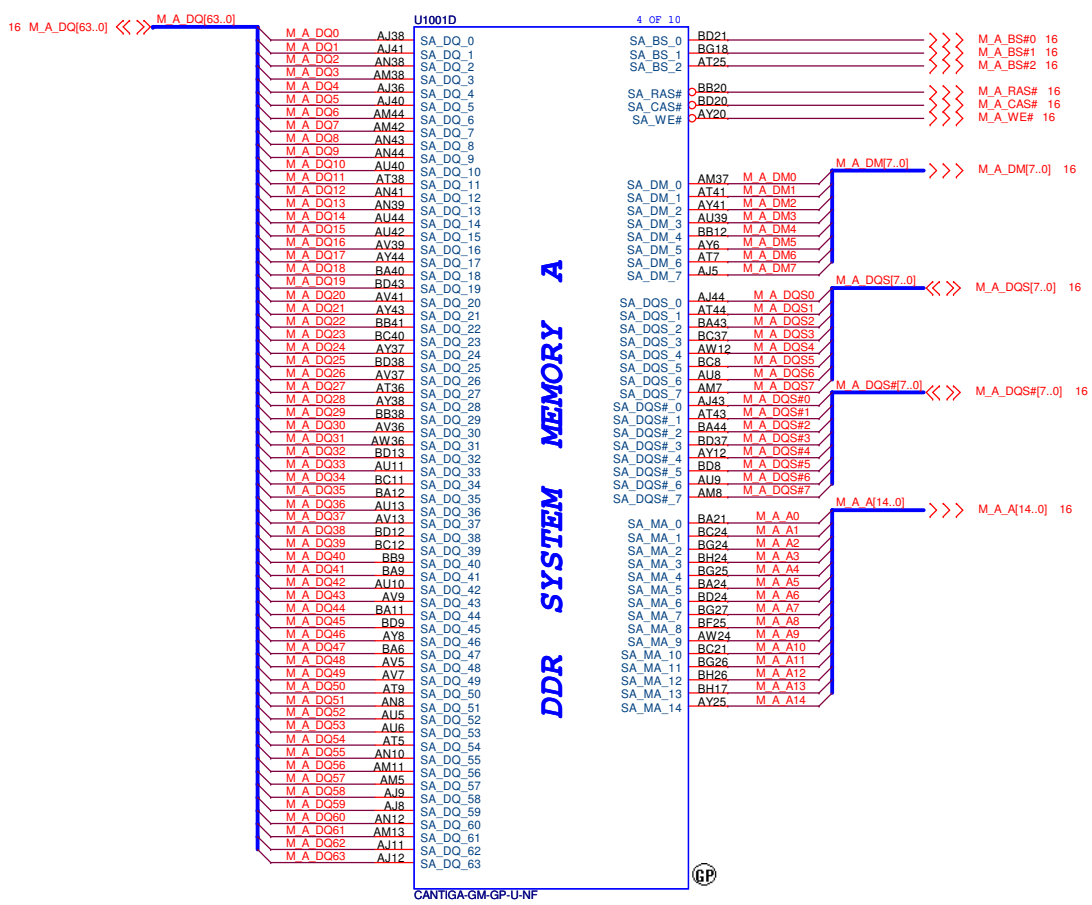
For UMA

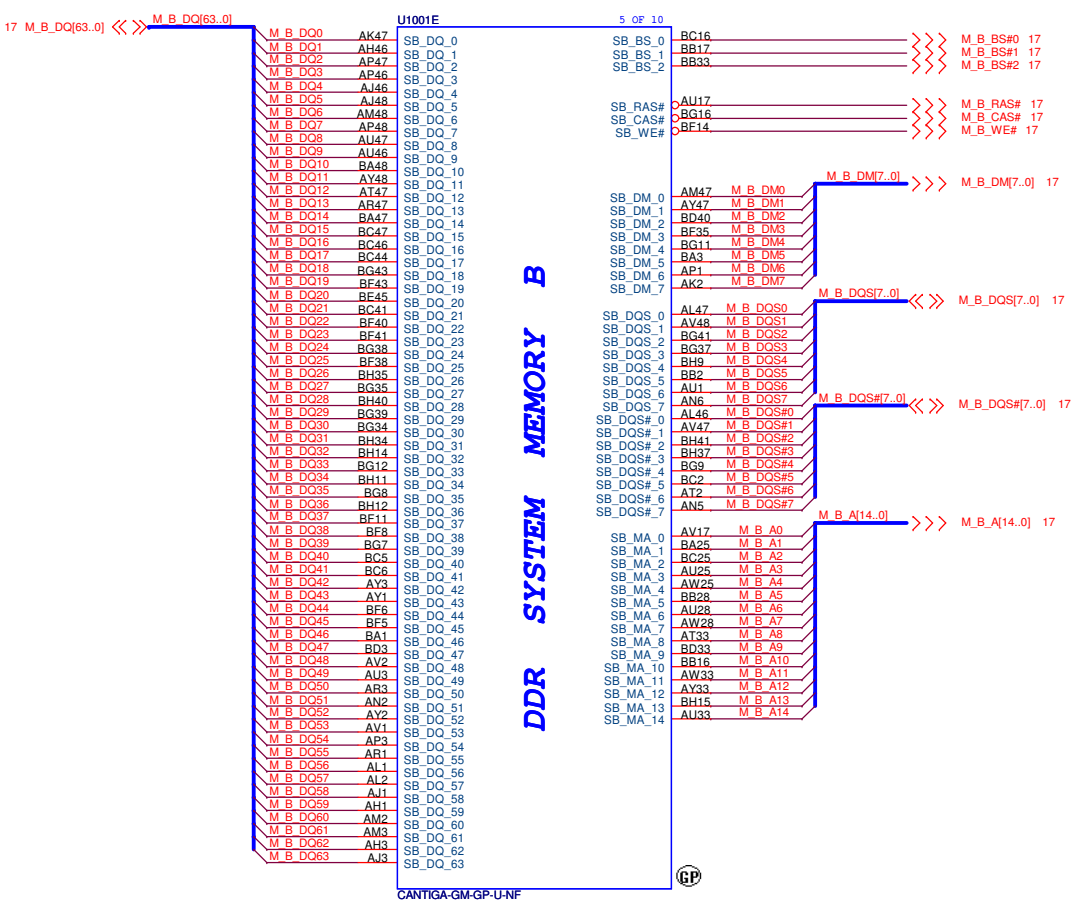
Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DMI/CFG(2/6)
Size: Custom | Document Number: Alba UMA | Rev: -1
Date: Monday, April 06, 2009 | Sheet 11 of 61

SSID = MCH





Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DDR(3/6)

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 12 of 61

SSID = MCH

U1001I — 9 OF 10

VSS

CANTIGA-GM-GP-U-NF

U1001J — 10 OF 10

VSS

VSS NCTF

VSS SCB

NC

CANTIGA-GM-GP-U-NF

NCTF PIN

NCTF PIN

+3.3V_RUN

RN1302 SRN2K2J-1-GP

RN1303 SRN10KJ-5-GP

41 LBKLT_CTL
26 GMCH_BL_ON

L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA

41 LDDC_CLK
41 LDDC_DATA

L_CTRL_CLK
L_CTRL_DATA
LDDC_CLK
LDDC_DATA

41 LCDVDD_EN

R1303 2K4R2F-GP

TP225

LIBG
LVDS_VBG

L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL

41 VGA_TXACLK-
41 VGA_TXACLK+
41 VGA_TXBCLK-
41 VGA_TXBCLK+

LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK

41 VGA_TXAOUT0-
41 VGA_TXAOUT1-
41 VGA_TXAOUT2-

LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3

41 VGA_TXAOUT0+
41 VGA_TXAOUT1+
41 VGA_TXAOUT2+

LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3

41 VGA_TXBOUT0-
41 VGA_TXBOUT1-
41 VGA_TXBOUT2-

LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3

41 VGA_TXBOUT0+
41 VGA_TXBOUT1+
41 VGA_TXBOUT2+

LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3

R1304 75R2F-2-GP TV_DACA
R1305 75R2F-2-GP TV_DACB
R1306 75R2F-2-GP TV_DACC

TVA_DAC
TVB_DAC
TVC_DAC
TV_RTN
TV_DCONSEL_0
TV_DCONSEL_1

UMA-SA

42 M_BLUE
42 M_GREEN
42 M_RED

R1307 150R2F-1-GP
R1308 150R2F-1-GP
R1309 150R2F-1-GP

M_BLUE
M_GREEN
M_RED

CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN

42 GMCH_HSYNC
42 GMCH_VSYNC

R1310 33R2J-2-GP
R1311 1K02R2F-1-GP
R1312 33R2J-2-GP

GMCH_DDCCLK
GMCH_DDCDATA
GMCH_HS
GMCH_VS
CRT_IREF

CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC

CRT_IREF routing Trace width use 20 mil.

U1001C — 3 OF 10

LVDS

PCI-EXPRESS GRAPHICS

TV

VGA

CANTIGA-GM-GP-U-NF

+1.05V_VCCP

R1301 49D9R2F-GP

Place R1301 close to MCH within 500 mils.

PEG_COMPI
PEG_COMPO
PEG_CMP

PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15

PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15

PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

RN1301 SRN2K2J-1-GP

Q1301 2N7002DW-7F-GP

GMCH_DDCDATA
DDC_DATA_CON
DDC_DATA_CON 46
46 DDC_CLK_CON
DDC_CLK_CON
GMCH_DDCCLK

5V @ ext. CRT side

Alba UMA

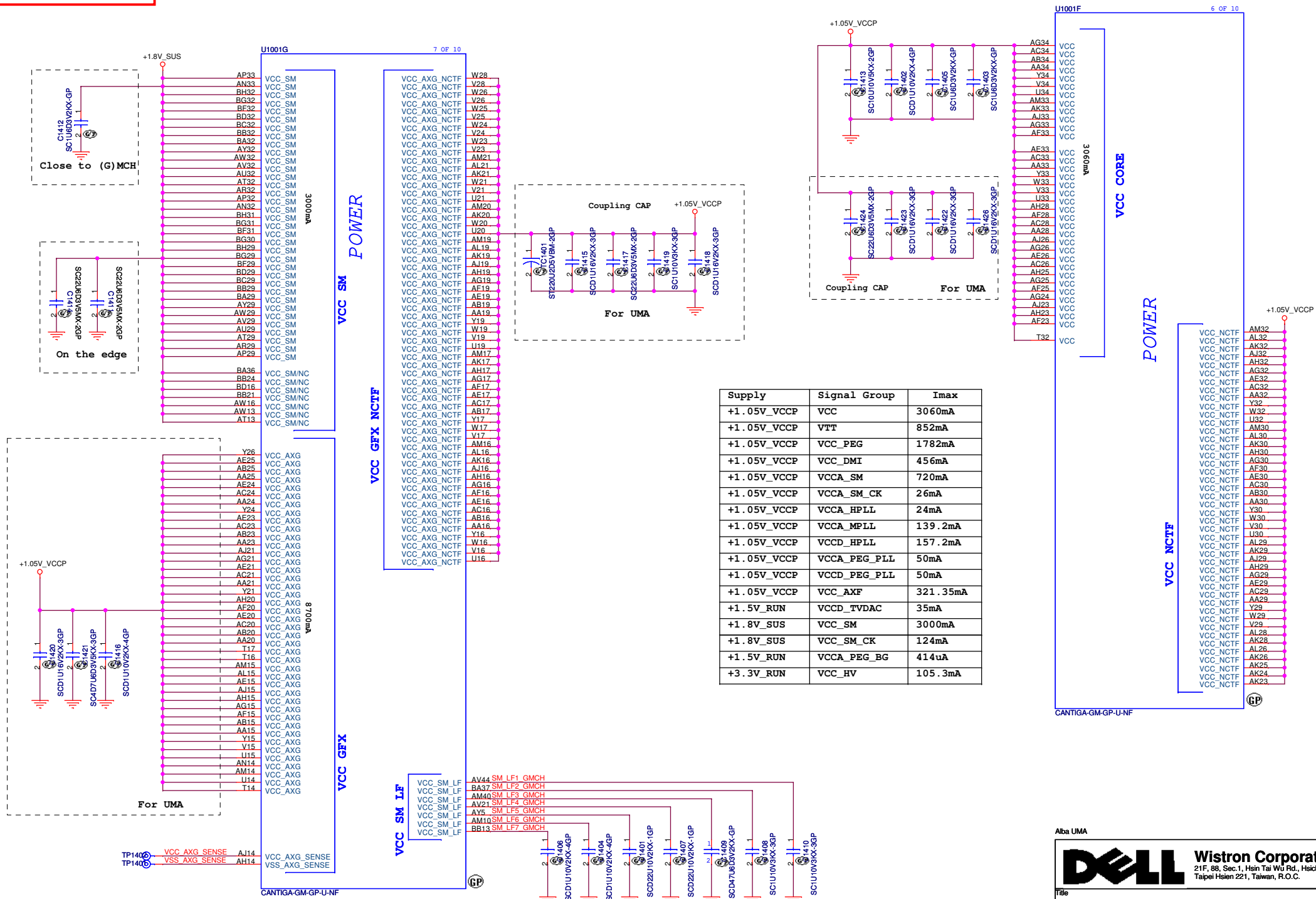
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-GND/LVDS/VGA(6/6)

Size: C | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 13 of 61

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

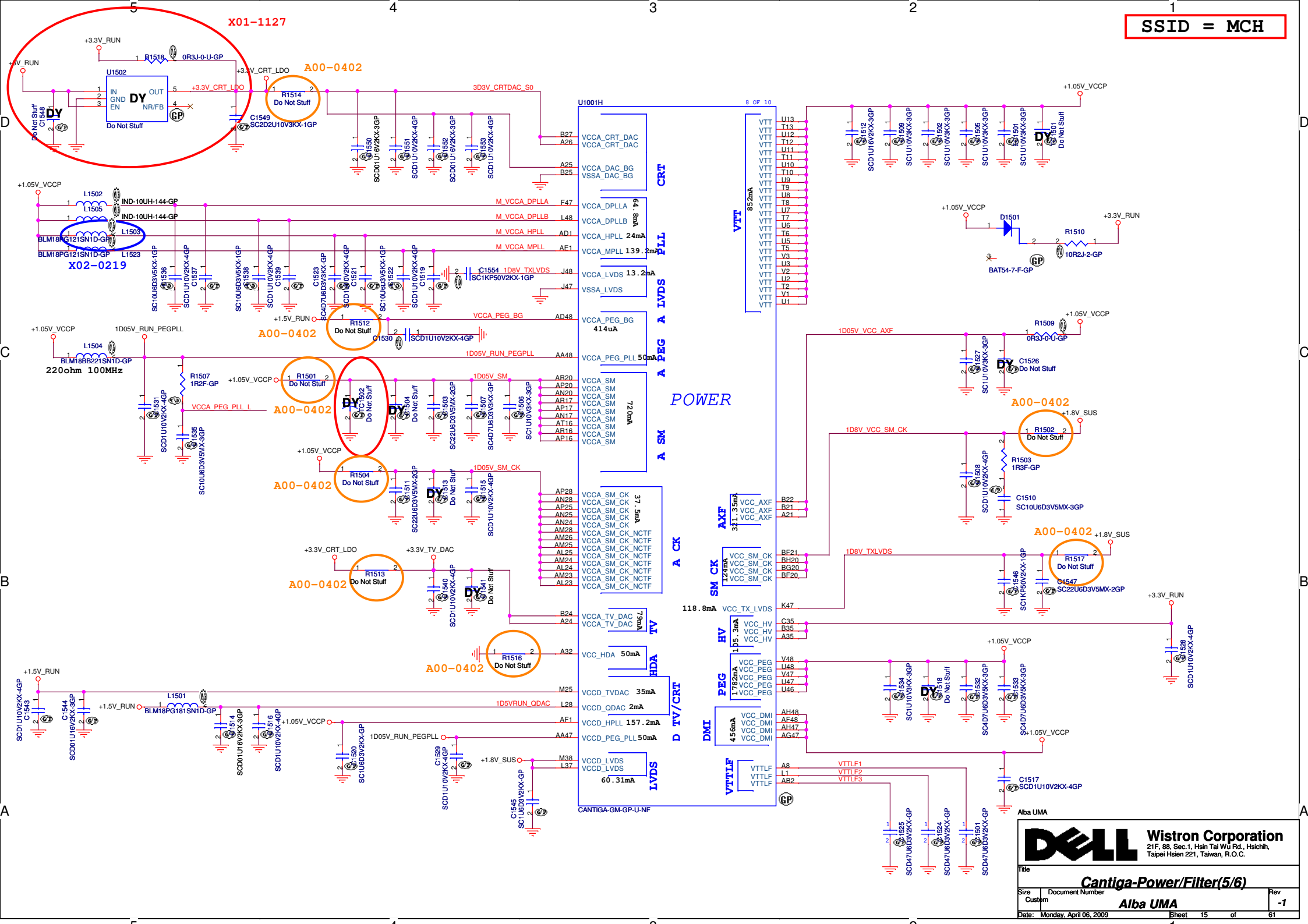
Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power(4/6)

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 14 of 61


SSID = MCH
X01-1127
X02-0219
A00-0402
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
U1001H
CANTIGA-GM-GP-U-NF
Alba UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Cantiga-Power/Filter(5/6)
Alba UMA
Monday, April 06, 2009
Sheet 15 of 61

SSID = MEMORY

12 M_A_DQS#[7..0]
12 M_A_DQ[63..0]
12 M_A_DM[7..0]
12 M_A_DQS[7..0]
12 M_A_A[14..0]

DM1

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
M_A_A14 86 A14
84 A15
12 M_A_BS#2 M_A_BS#2 85 A16/BA2
12 M_A_BS#0 M_A_BS#0 107 BA0
12 M_A_BS#1 M_A_BS#1 106 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 17 DQ2
M_A_DQ3 19 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 14 DQ6
M_A_DQ7 16 DQ7
M_A_DQ8 23 DQ8
M_A_DQ9 25 DQ9
M_A_DQ10 35 DQ10
M_A_DQ11 37 DQ11
M_A_DQ12 20 DQ12
M_A_DQ13 22 DQ13
M_A_DQ14 36 DQ14
M_A_DQ15 38 DQ15
M_A_DQ16 43 DQ16
M_A_DQ17 45 DQ17
M_A_DQ18 55 DQ18
M_A_DQ19 57 DQ19
M_A_DQ20 44 DQ20
M_A_DQ21 46 DQ21
M_A_DQ22 56 DQ22
M_A_DQ23 58 DQ23
M_A_DQ24 61 DQ24
M_A_DQ25 63 DQ25
M_A_DQ26 73 DQ26
M_A_DQ27 75 DQ27
M_A_DQ28 62 DQ28
M_A_DQ29 64 DQ29
M_A_DQ30 74 DQ30
M_A_DQ31 76 DQ31
M_A_DQ32 123 DQ32
M_A_DQ33 125 DQ33
M_A_DQ34 135 DQ34
M_A_DQ35 137 DQ35
M_A_DQ36 124 DQ36
M_A_DQ37 126 DQ37
M_A_DQ38 134 DQ38
M_A_DQ39 136 DQ39
M_A_DQ40 141 DQ40
M_A_DQ41 143 DQ41
M_A_DQ42 151 DQ42
M_A_DQ43 153 DQ43
M_A_DQ44 140 DQ44
M_A_DQ45 142 DQ45
M_A_DQ46 152 DQ46
M_A_DQ47 154 DQ47
M_A_DQ48 157 DQ48
M_A_DQ49 159 DQ49
M_A_DQ50 173 DQ50
M_A_DQ51 175 DQ51
M_A_DQ52 158 DQ52
M_A_DQ53 160 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 179 DQ56
M_A_DQ57 181 DQ57
M_A_DQ58 189 DQ58
M_A_DQ59 191 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 11 /DQS0
M_A_DQS#1 29 /DQS1
M_A_DQS#2 49 /DQS2
M_A_DQS#3 68 /DQS3
M_A_DQS#4 129 /DQS4
M_A_DQS#5 146 /DQS5
M_A_DQS#6 167 /DQS6
M_A_DQS#7 186 /DQS7

M_A_DQS0 13 DQS0
M_A_DQS1 31 DQS1
M_A_DQS2 51 DQS2
M_A_DQS3 70 DQS3
M_A_DQS4 131 DQS4
M_A_DQS5 148 DQS5
M_A_DQS6 169 DQS6
M_A_DQS7 188 DQS7

11 M_ODT0 M_ODT0 114 ODT0
11 M_ODT1 M_ODT1 119 ODT1

1 VREF
2 VSS
202 GND

/RAS 108
/WE 109
/CAS 113
M_A_RAS# 12
M_A_WE# 12
M_A_CAS# 12

/CS0 110
/CS1 115
M_CS0# 11
M_CS1# 11

CKE0 79
CKE1 80
M_CKE0 11
M_CKE1 11

CK0 30
/CK0 32
M_CLK_DDR0 11
M_CLK_DDR#0 11

CK1 164
/CK1 166
M_CLK_DDR1 11
M_CLK_DDR#1 11

DM0 10
DM1 26
DM2 52
DM3 67
DM4 130
DM5 147
DM6 170
DM7 185
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

SDA 195
SCL 197
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 7,17,20,43
ICH_SMBCLK 7,17,20,43

VDDSPD 199

SA0 198
SA1 200
ALBA X00

NC#50 50
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163
PM_EXTTS#0 11

VDD 81 82 87 88 95 96 103 104 111 112 117 118

VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196 201

DDR2-200P-10-U1
62.10017.881

Height 6.5mm

+1.8V_SUS

+3.3V_RUN

C1602 SCD1U16V2KX-3GP
DY C1601 Do Not Stuff

put near connector
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1603 Do Not Stuff
C1604 Do Not Stuff
C1623 Do Not Stuff
C1624 Do Not Stuff

Layout Note:
Place near SKT1
+1.8V_SUS
C1620 SC1U10V3KX-3GP
C1619 SC1U10V3KX-3GP
DY C1622 Do Not Stuff
DY C1621 Do Not Stuff
C1616 SC1U10V3KX-3GP
DY C1607 Do Not Stuff
C1613 SCD1U16V2KX-3GP
C1609 SC1U6D3V2KX-GP
C1612 SCD1U16V2KX-3GP
DY C1601 Do Not Stuff

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.
+0.9V_DDR_VTT
DY C1610 Do Not Stuff
C1627 SCD1U16V2KX-3GP
DY C1611 Do Not Stuff
C1608 SCD1U16V2KX-3GP
DY C1605 Do Not Stuff
DY C1630 Do Not Stuff
C1606 SCD1U16V2KX-3GP
DY C1614 Do Not Stuff
DY C1617 Do Not Stuff
C1618 SCD1U16V2KX-3GP
C1615 SCD1U16V2KX-3GP
C1629 SCD1U16V2KX-3GP
C1628 SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".
+0.9V_DDR_VTT
RN1601 SRN56J-5-GP
M_A_A5 M_A_A8 M_A_A9 M_A_A12
RN1605 SRN56J-4-GP
M_CKE0 M_A_BS#2
R1663 56R2J-4-GP
M_A_A13
RN1602 SRN56J-5-GP
M_ODT0 M_CS0# M_A_BS#1 M_A_RAS#
RN1606 SRN56J-5-GP
M_A_A3 M_A_A1 M_A_A10 M_A_BS#0
RN1603 SRN56J-5-GP
M_ODT1 M_CS1# M_A_CAS# M_A_WE#
RN1607 SRN56J-5-GP
M_A_A7 M_A_A11 M_A_A14 M_CKE1
RN1604 SRN56J-5-GP
M_A_A0 M_A_A2 M_A_A4 M_A_A6

+V_DDR_MCH_REF
C1626 SCD1U16V2KX-3GP
DY C1625 Do Not Stuff

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom
Document Number: Alba UMA
Rev: -1
Date: Monday, April 06, 2009
Sheet 16 of 61

SSID = MEMORY

12 M_B_DQS#[7..0]
12 M_B_DQ[63..0]
12 M_B_DM[7..0]
12 M_B_DQS[7..0]
12 M_B_A[14..0]

Layout Note:
Place near SKT2

+1.8V_SUS

C1716 SC1U10V3KX-3GP
DY C1707 Do Not Stuff
C1711 SC1U10V3KX-3GP
C1712 SC1U10V3KX-3GP
C1710 SC1U10V3KX-3GP
C1714 SCD1U10V2KX-4GP
DY C1717 Do Not Stuff
C1709 SC1U6D3V2KX-GP
C1715 SC1U6D3V2KX-GP
DY C1701 Do Not Stuff

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT

DY C1729 Do Not Stuff
C1726 SCD1U16V2KX-3GP
C1728 SCD1U16V2KX-3GP
DY C1727 Do Not Stuff
C1725 SCD1U16V2KX-3GP
C1723 SCD1U16V2KX-3GP
C1722 SCD1U16V2KX-3GP
C1706 SCD1U16V2KX-3GP
C1724 SCD1U16V2KX-3GP
DY C1713 Do Not Stuff
C1705 SCD1U16V2KX-3GP
DY C1721 Do Not Stuff
C1708 SCD1U16V2KX-3GP

DM2

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10/AP
M_B_A11 90 A11
M_B_A12 89 A12
M_B_A13 116 A13
M_B_A14 86 A14
12 M_B_BS#2 84 A15
M_B_BS#2 85 A16/BA2
M_B_BS#0 107 BA0
M_B_BS#1 106 BA1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 17 DQ2
M_B_DQ3 19 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 14 DQ6
M_B_DQ7 16 DQ7
M_B_DQ8 23 DQ8
M_B_DQ9 25 DQ9
M_B_DQ10 35 DQ10
M_B_DQ11 37 DQ11
M_B_DQ12 20 DQ12
M_B_DQ13 22 DQ13
M_B_DQ14 36 DQ14
M_B_DQ15 38 DQ15
M_B_DQ16 43 DQ16
M_B_DQ17 45 DQ17
M_B_DQ18 55 DQ18
M_B_DQ19 57 DQ19
M_B_DQ20 44 DQ20
M_B_DQ21 46 DQ21
M_B_DQ22 56 DQ22
M_B_DQ23 58 DQ23
M_B_DQ24 61 DQ24
M_B_DQ25 63 DQ25
M_B_DQ26 73 DQ26
M_B_DQ27 75 DQ27
M_B_DQ28 62 DQ28
M_B_DQ29 64 DQ29
M_B_DQ30 74 DQ30
M_B_DQ31 76 DQ31
M_B_DQ32 123 DQ32
M_B_DQ33 125 DQ33
M_B_DQ34 135 DQ34
M_B_DQ35 137 DQ35
M_B_DQ36 124 DQ36
M_B_DQ37 126 DQ37
M_B_DQ38 134 DQ38
M_B_DQ39 136 DQ39
M_B_DQ40 141 DQ40
M_B_DQ41 143 DQ41
M_B_DQ42 151 DQ42
M_B_DQ43 153 DQ43
M_B_DQ44 140 DQ44
M_B_DQ45 142 DQ45
M_B_DQ46 152 DQ46
M_B_DQ47 154 DQ47
M_B_DQ48 157 DQ48
M_B_DQ49 159 DQ49
M_B_DQ50 173 DQ50
M_B_DQ51 175 DQ51
M_B_DQ52 158 DQ52
M_B_DQ53 160 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 179 DQ56
M_B_DQ57 181 DQ57
M_B_DQ58 189 DQ58
M_B_DQ59 191 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

M_B_DQS#0 11 DQS0#
M_B_DQS#1 29 DQS1#
M_B_DQS#2 49 DQS2#
M_B_DQS#3 68 DQS3#
M_B_DQS#4 129 DQS4#
M_B_DQS#5 146 DQS5#
M_B_DQS#6 167 DQS6#
M_B_DQS#7 186 DQS7#

M_B_DQS0 13 DQS0
M_B_DQS1 31 DQS1
M_B_DQS2 51 DQS2
M_B_DQS3 70 DQS3
M_B_DQS4 131 DQS4
M_B_DQS5 148 DQS5
M_B_DQS6 169 DQS6
M_B_DQS7 188 DQS7

11 M_ODT2 M_ODT2 114 ODT0
11 M_ODT3 M_ODT3 119 ODT1

1 VREF
2 VSS

NP1 NP1
NP2 NP2

RAS# 108 M_B_RAS# 12
WE# 109 M_B_WE# 12
CAS# 113 M_B_CAS# 12

CS0# 110 M_CS2# 11
CS1# 115 M_CS3# 11

CKE0 79 M_CKE2 11
CKE1 80 M_CKE3 11

CK0 30 M_CLK_DDR2
CK0# 32 M_CLK_DDR#2
M_CLK_DDR2 11
M_CLK_DDR#2 11

CK1 164 M_CLK_DDR3
CK1# 166 M_CLK_DDR#3
M_CLK_DDR3 11
M_CLK_DDR#3 11

DM0 10 M_B_DM0
DM1 26 M_B_DM1
DM2 52 M_B_DM2
DM3 67 M_B_DM3
DM4 130 M_B_DM4
DM5 147 M_B_DM5
DM6 170 M_B_DM6
DM7 185 M_B_DM7

SDA 195 ICH_SMBDATA
SCL 197 ICH_SMBCLK
ICH_SMBDATA 7,16,20,43
ICH_SMBCLK 7,16,20,43

VDDSPD 199
SA0 198
SA1 200
+3.3V_RUN

NC#50 50 PM_EXTTS#1 11
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163

ALBA X00

C1701 SCD1U16V2KX-3GP
DY C1702 Do Not Stuff

+1.8V_SUS

VDD 81
VDD 82
VDD 87
VDD 88
VDD 95
VDD 96
VDD 103
VDD 104
VDD 111
VDD 112
VDD 117
VDD 118

VSS 3
VSS 8
VSS 9
VSS 12
VSS 15
VSS 18
VSS 21
VSS 24
VSS 27
VSS 28
VSS 33
VSS 34
VSS 39
VSS 40
VSS 41
VSS 42
VSS 47
VSS 48
VSS 53
VSS 54
VSS 59
VSS 60
VSS 65
VSS 66
VSS 71
VSS 72
VSS 77
VSS 78
VSS 121
VSS 122
VSS 127
VSS 128
VSS 132
VSS 133
VSS 138
VSS 139
VSS 144
VSS 145
VSS 149
VSS 150
VSS 155
VSS 156
VSS 161
VSS 162
VSS 165
VSS 168
VSS 171
VSS 172
VSS 177
VSS 178
VSS 183
VSS 184
VSS 187
VSS 190
VSS 193
VSS 196

GND 201
GND 202
GP

DDR2-200P-33-GP

Height 11mm

+V_DDR_MCH_REF

C1730 SCD1U16V2KX-3GP
C1720 SC2D2U10V3KX-1GP

put near connector

M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3

C1703 Do Not Stuff
C1704 Do Not Stuff
C1718 Do Not Stuff
C1719 Do Not Stuff

Layout Note:
Place these resistors close to DM2, all trace length Max=1.5".

+0.9V_DDR_VTT

RN1701 SRN56J-3-GP
M_B_A8
M_B_A5
M_B_A1
M_B_A3

RN1704 SRN56J-3-GP
M_CKE3
M_B_A14
M_B_A11
M_B_A6

RN1702 SRN56J-3-GP
M_ODT3
M_CS3#
M_B_A0

RN1705 SRN56J-3-GP
M_B_A7
M_B_A4
M_B_A2
M_B_BS#1

RN1703 SRN56J-3-GP
M_B_A10
M_B_BS#0
M_B_WE#
M_B_CAS#

RN1706 SRN56J-3-GP
M_B_RAS#
M_ODT2
M_CS2#
M_B_A13

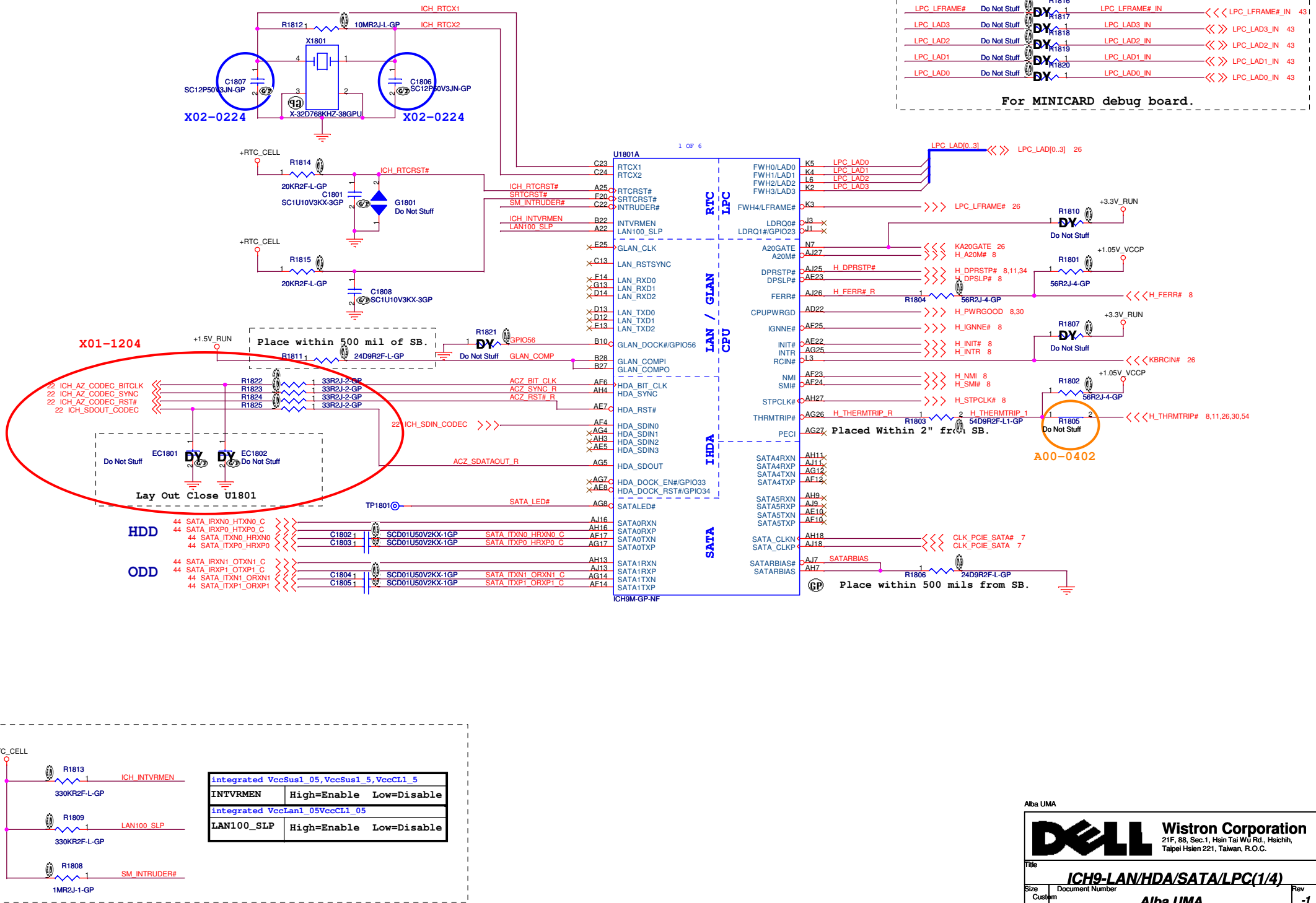
RN1707 SRN56J-3-GP
M_B_A12
M_B_BS#2
M_B_A9
M_CKE2

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2
Size: Custom | Document Number: Alba UMA | Rev: -1
Date: Monday, April 06, 2009 | Sheet 17 of 61

SSID = ICH



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 18 of 61

SSID = ICH

U1801E — 5 OF 6 — ICH9M-GP-NF

U1902 — DY — Do Not Stuff — R1907 — A00-0402

U1801B — 2 OF 6 — PCI / Interrupt I/F — ICH9M-GP-NF

RN1905 / RN1901 / RN1902 / RN1906 / RN1904 — SRN8K2J-4-GP

RP1901 — SRN10KJ-L3-GP

RN1903 — SRN8K2J-4-GP

U1801D — 4 OF 6 — PCI-Express / Direct Media Interface / SPI / USB — ICH9M-GP-NF

R1908 24D9R2F-L-GP

R1912 22D6R2F-L-GP

NCTF PIN

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Alba UMA

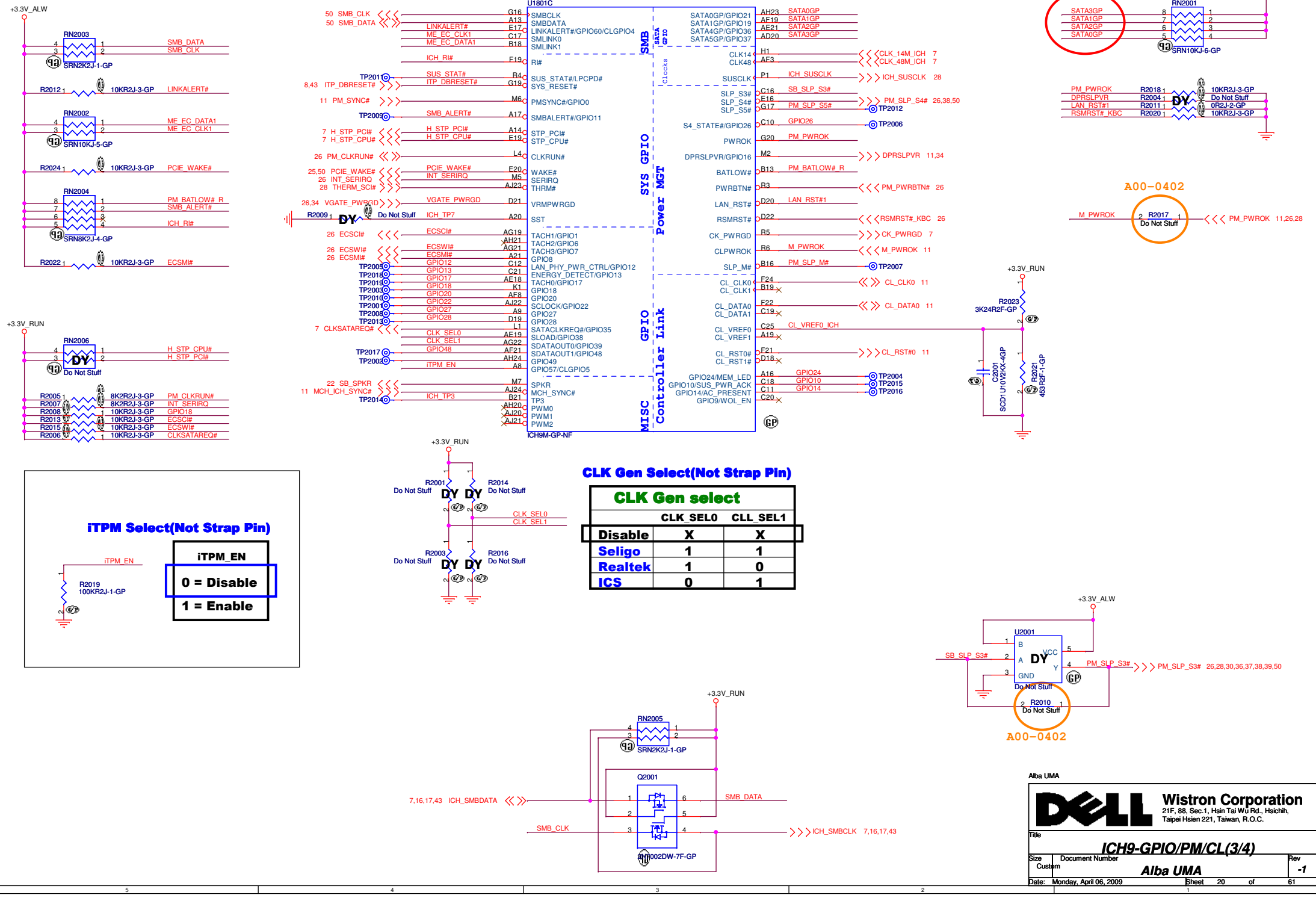
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-PCI/PCIE/DMI/USB/GND(2/4)

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 19 of 61

SSID = ICH



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-GPIO/PM/CL(3/4)**

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 20 of 61

SSID = ICH

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

U1801F 6 OF 6

ICH9M-GP-NF

Alba UMA

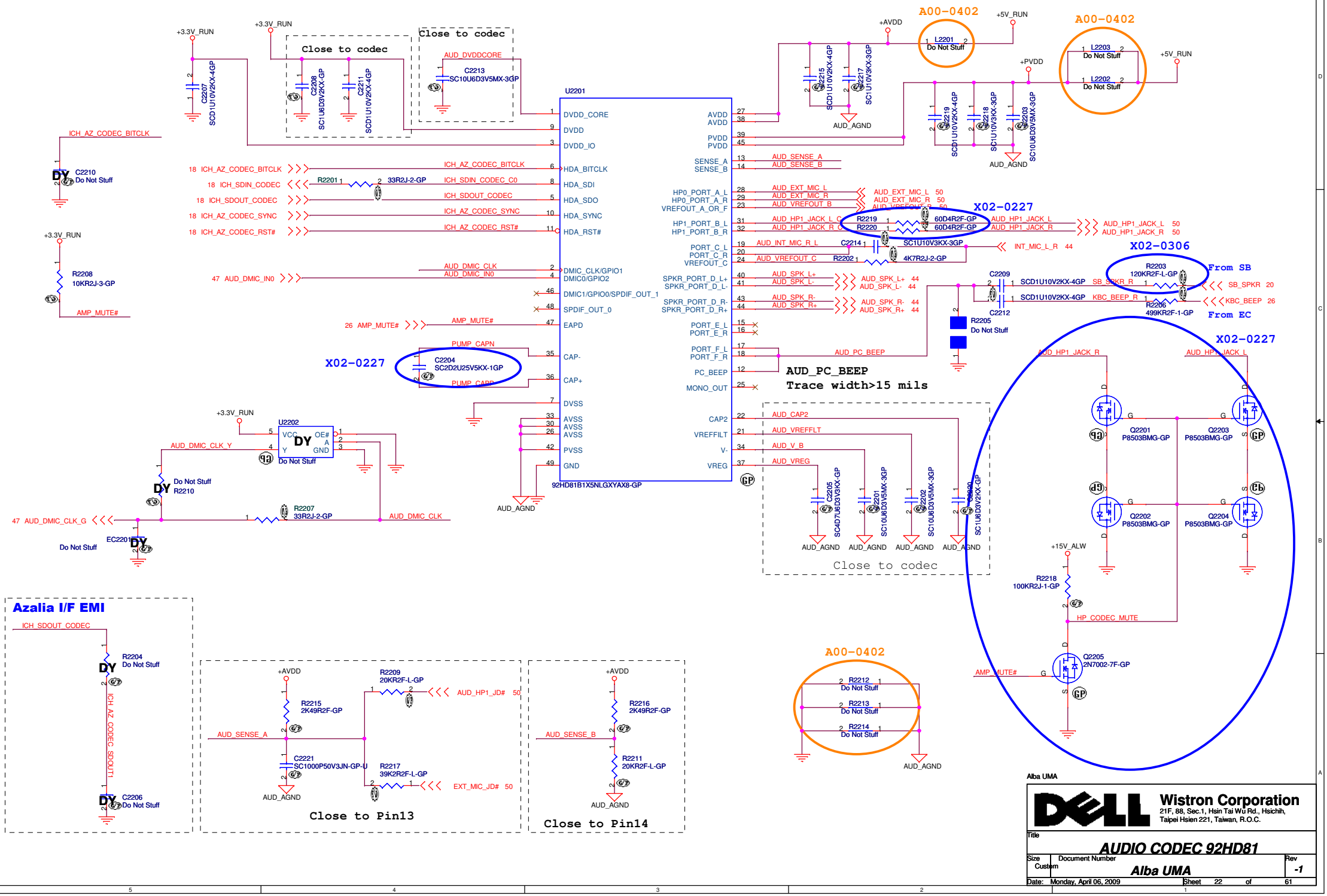
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-POWER(4/4)

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 21 of 61

SSID = AUDIO



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC 92HD81

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 22 of 61

(Blank)

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 23 of 61

(Blank)

Alba UMA

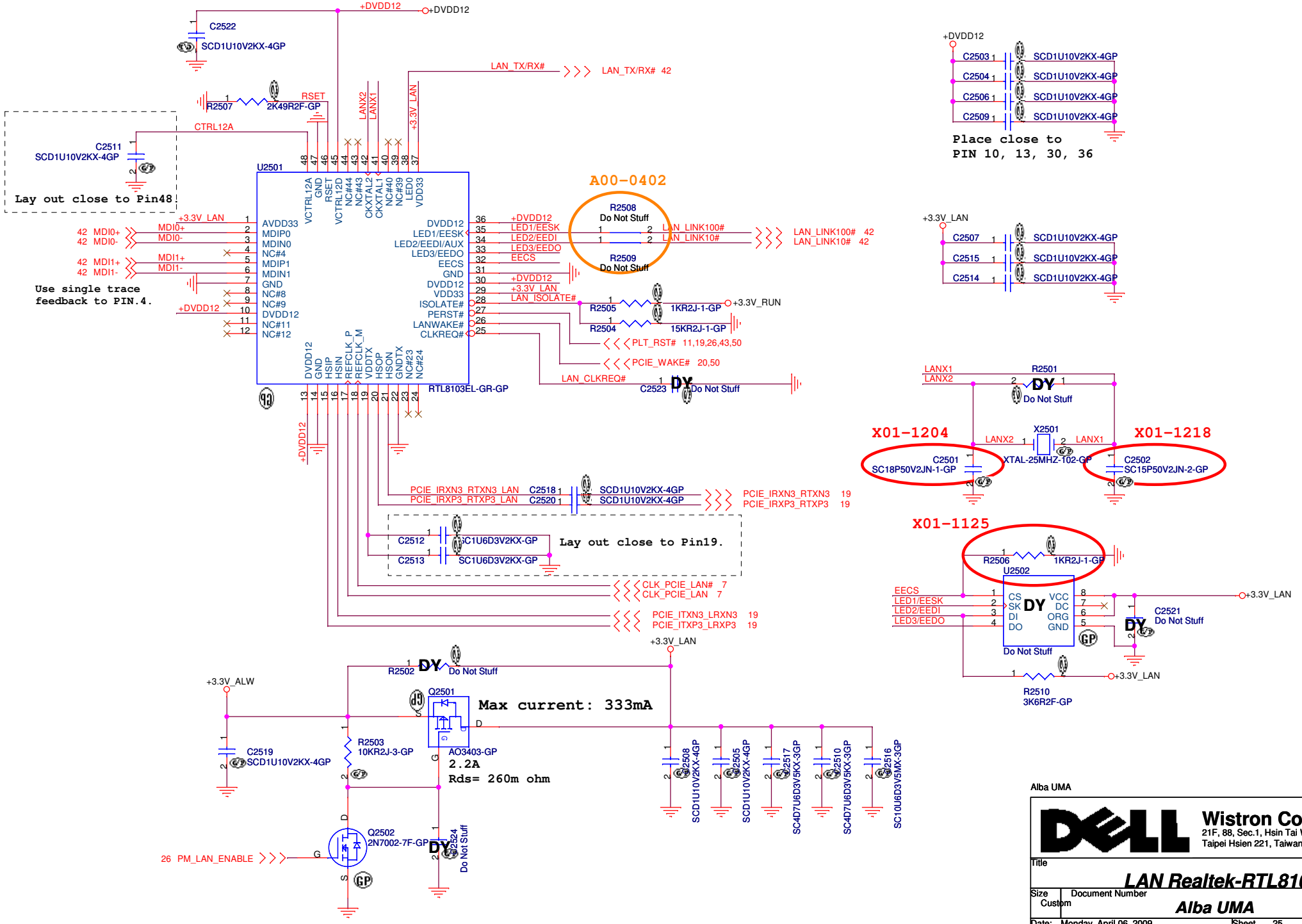
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 24 of 61

SSID = LOM



Alba UMA

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Realtek-RTL8102EL**

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 25 of 61

SSID = KBC

Put 0.1uf close to VCC-GND pin pair.

Pull High : Discrete
internal Pull Low for UMA

X01-0113

A00-0402

X02-0227

X02-0225

X02-0303

X02-0219

X01-1215

X02-0224

MB VERSION ID

MB VERSION ID	VER2	VER1	VER0
SA	0	0	1
SB	0	1	0
SC	0	1	0
-1	0	1	1

ALBA X00

KBC CLK EMI

KBC

PS/2

FIU

WPCE773LA0DG-GP

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Winbond WPC773L

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 26 of 61

(Blank)

Alba UMA

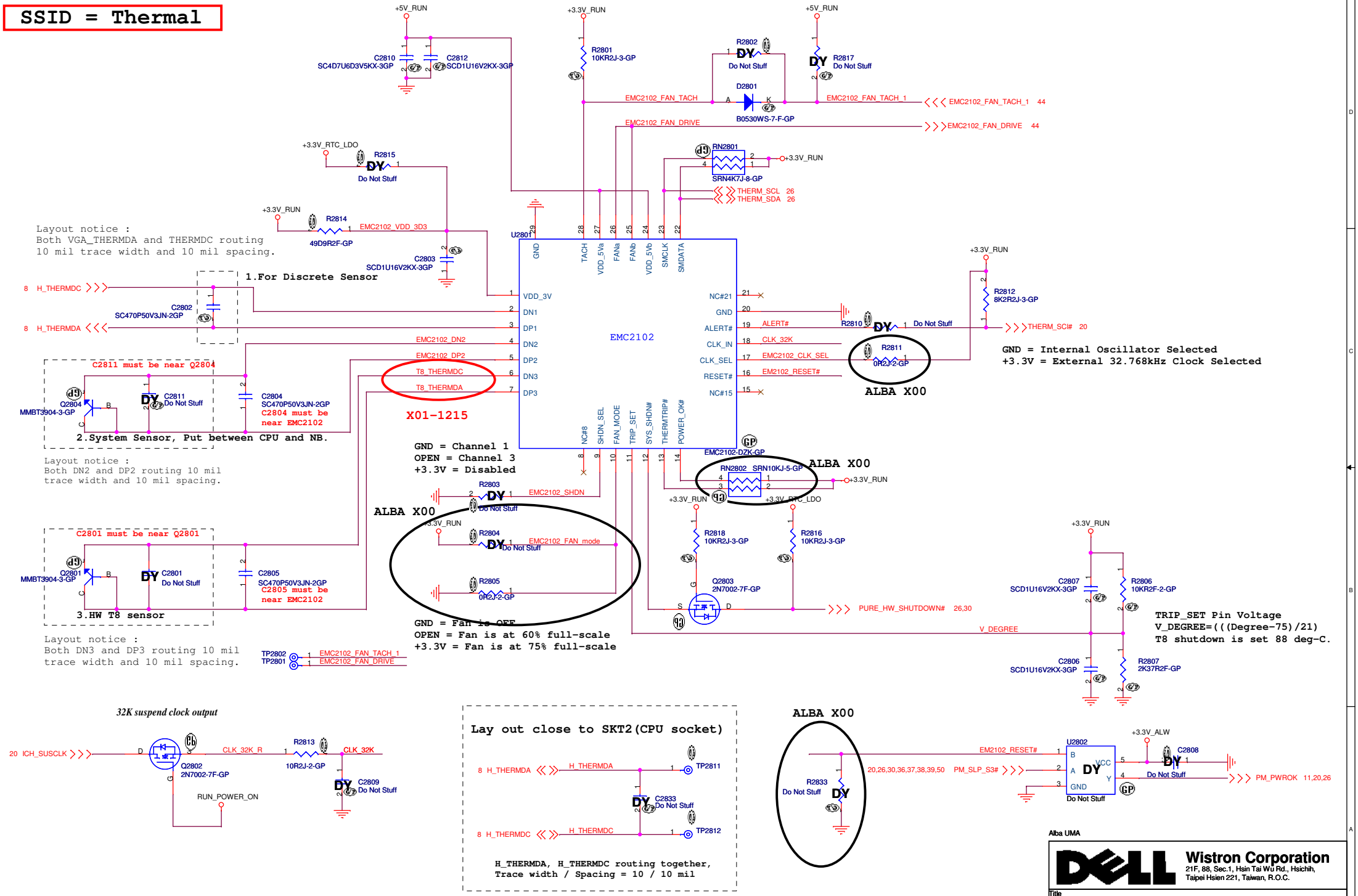
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 27 of 61

SSID = Thermal



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 28 of 61

(Blank)

Alba UMA

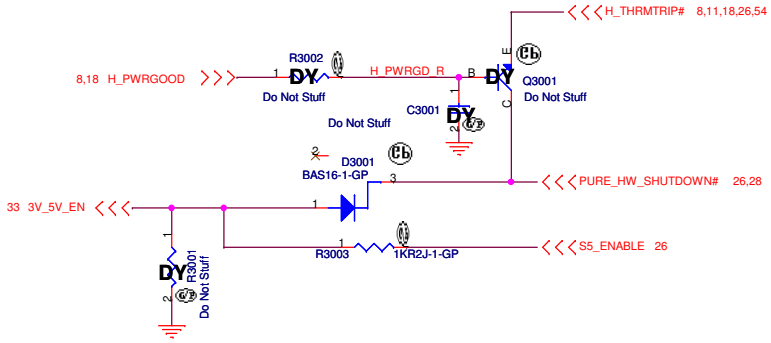
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

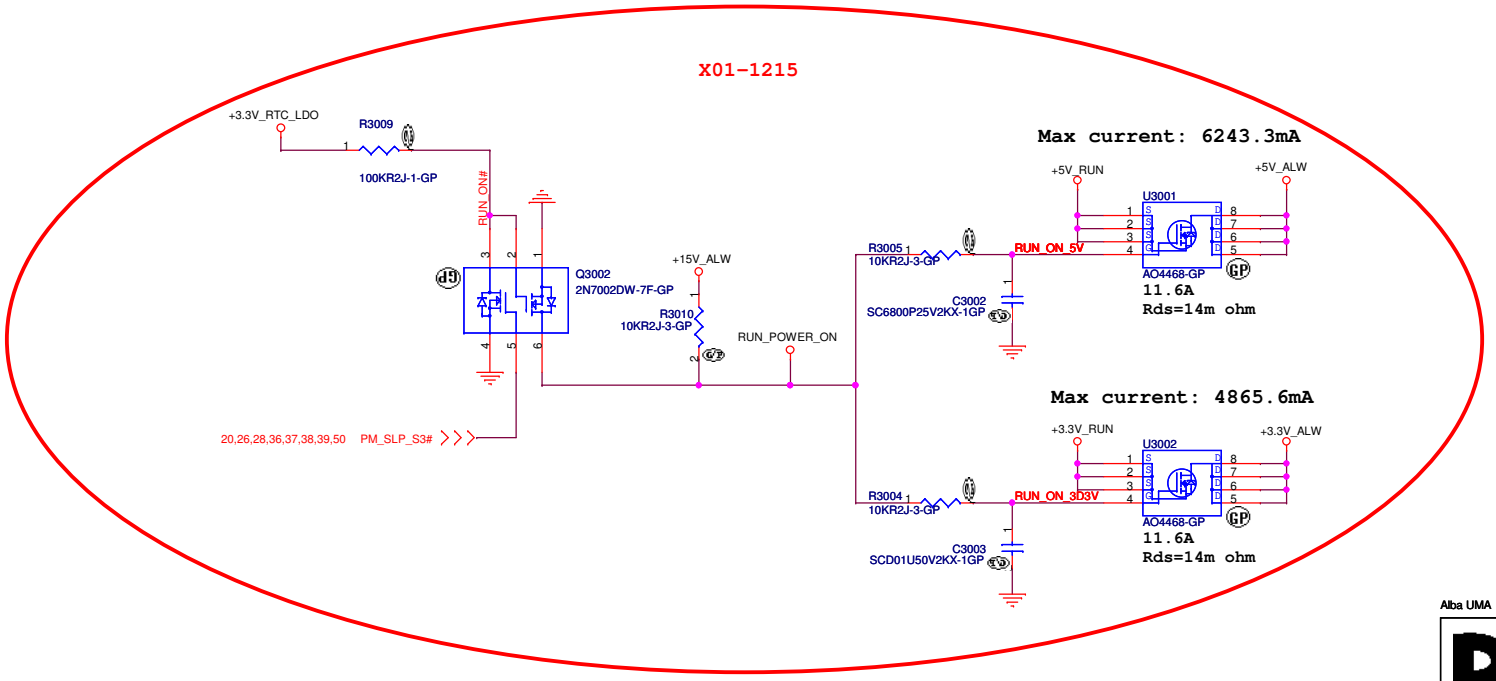
Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 29 of 61

SSID = Reset.Suspend



X01-1215



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

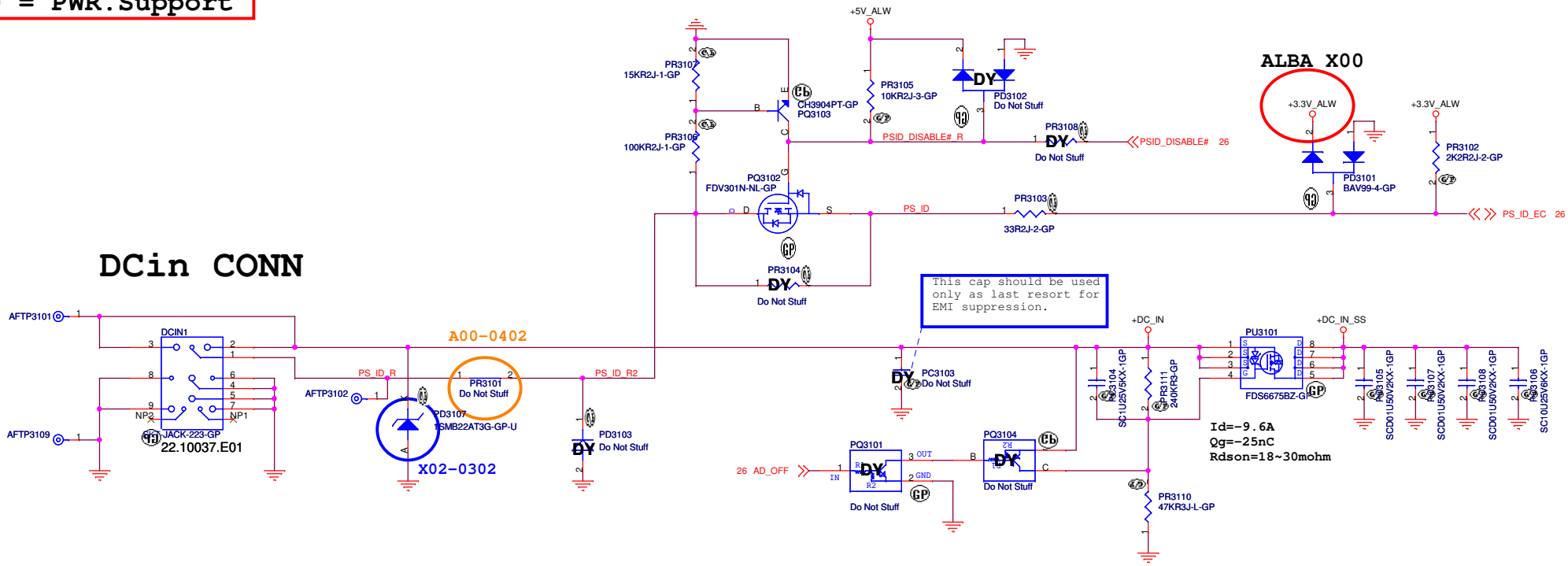
Title: ***Power Plane Enable***

Size: Custom | Document Number: ***Alba UMA*** | Rev: *-1*

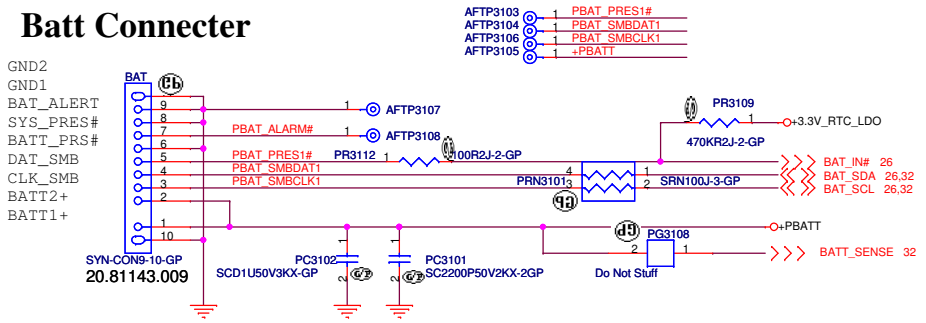
Date: Monday, April 06, 2009 | Sheet 30 of 61

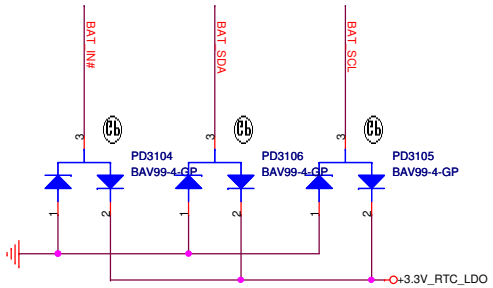
SSID = PWR.Support

DCin CONN



Batt Connecter





Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN/BATT CONN/USB CONN

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 31 of 61

SSID = Charger

Adaptor In Soft-Start Circuit

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
Layout Trace 250mil

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
Layout Trace 300mil

Layout Trace 300mil

Layout Trace 300mil

X02-0302

X02-0302

X01-1219

A00-0402

A00-0402

A00-0402

A00-0402

A00-0402

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR3202	PR3205	PR3207	PR3208
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor

ADAPT_TRIP_SEL=1 Adapter is 90w

ADAPT_TRIP_SEL=0 Adapter is 65w

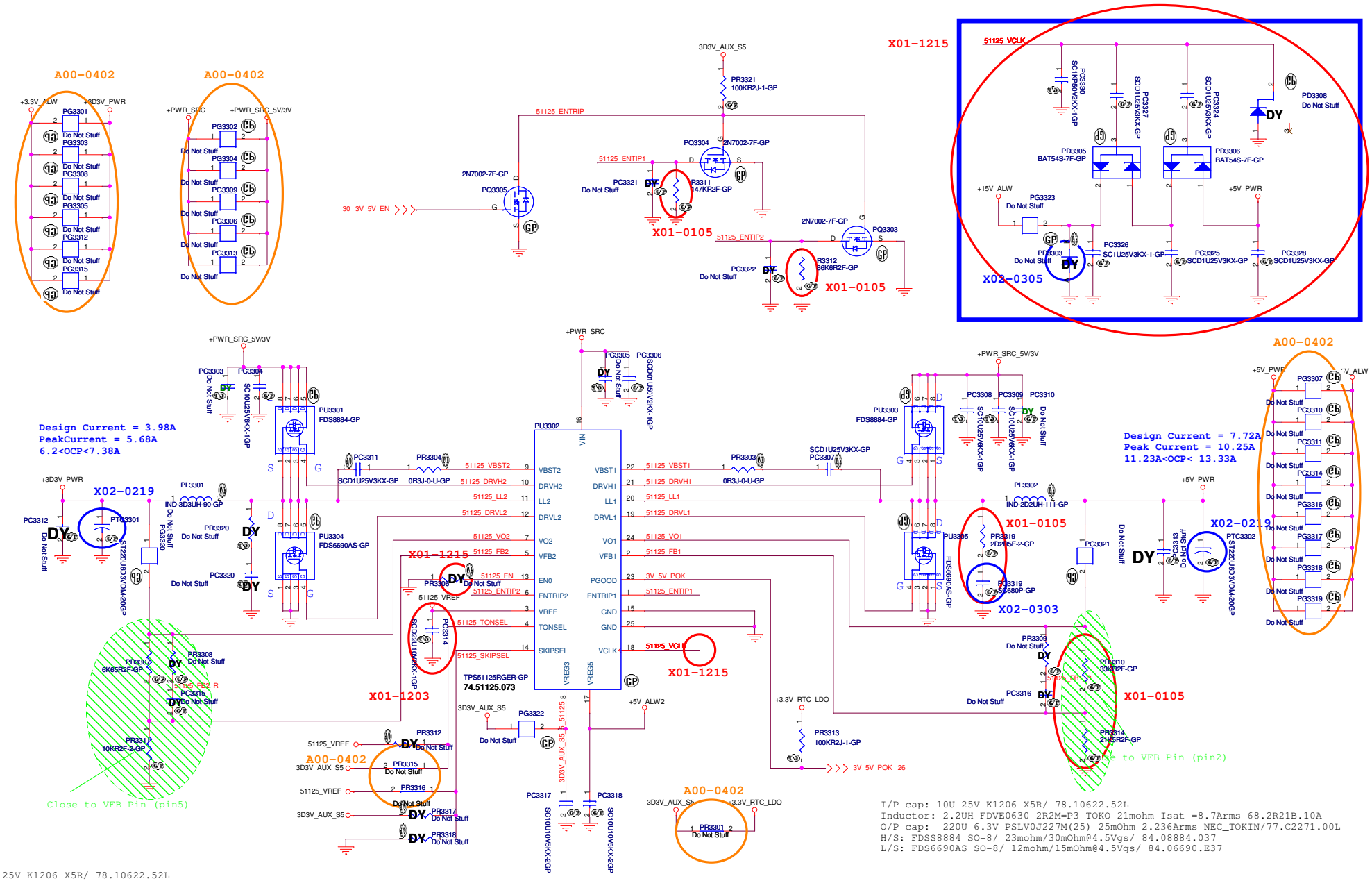
Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 32 of 61



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH FDV0630-3R3M=P3 TOKO 31mohm Isat =6.9Arms 68.3R31A.10E
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

X01-1219

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

Alba UMA

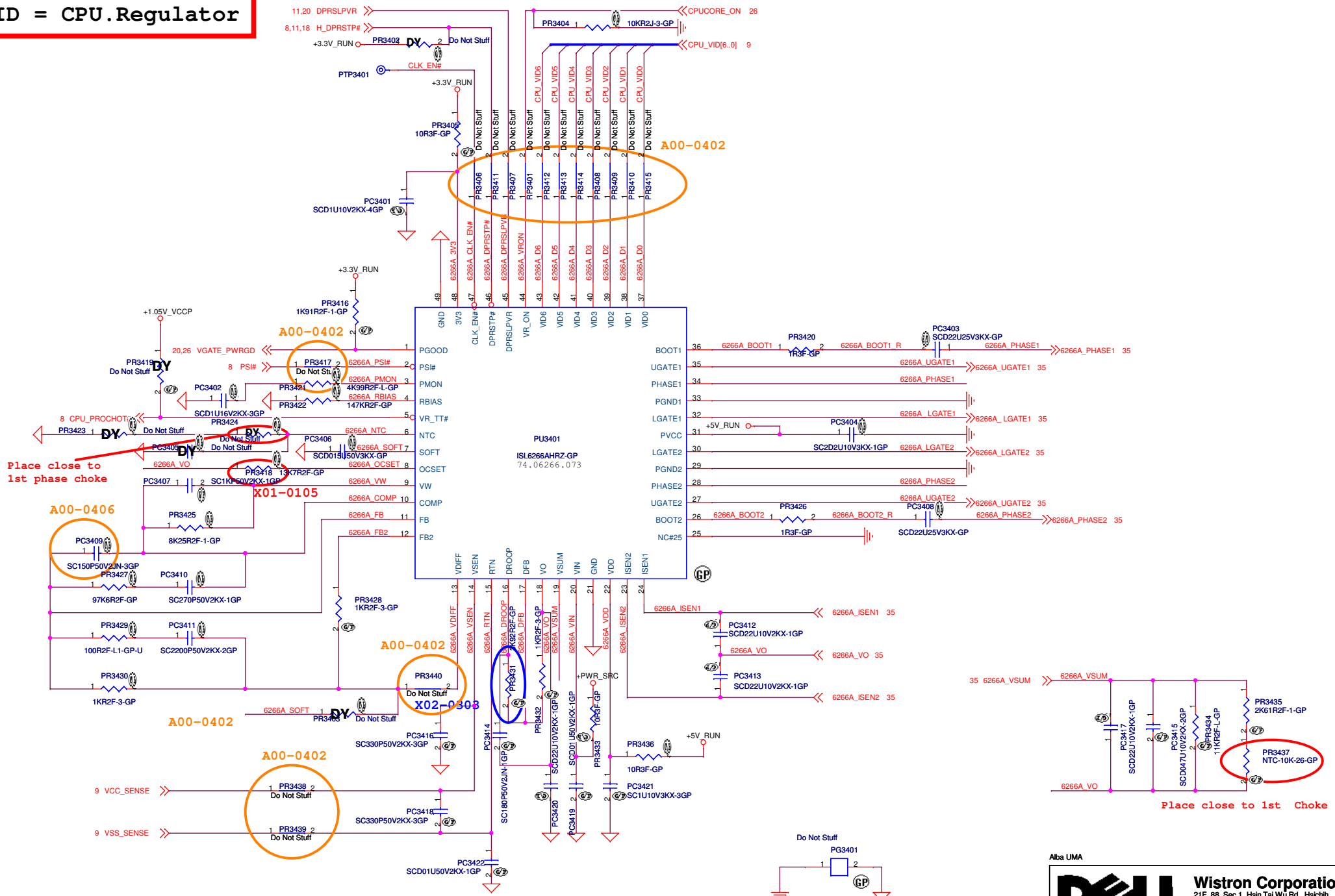
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 33 of 61

SSID = CPU.Regulator



Alba UMA

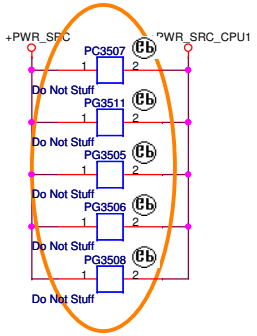
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

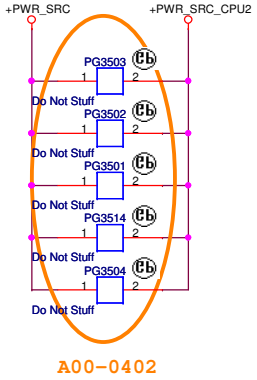
Title: CPU VCORE POWER(1/2)

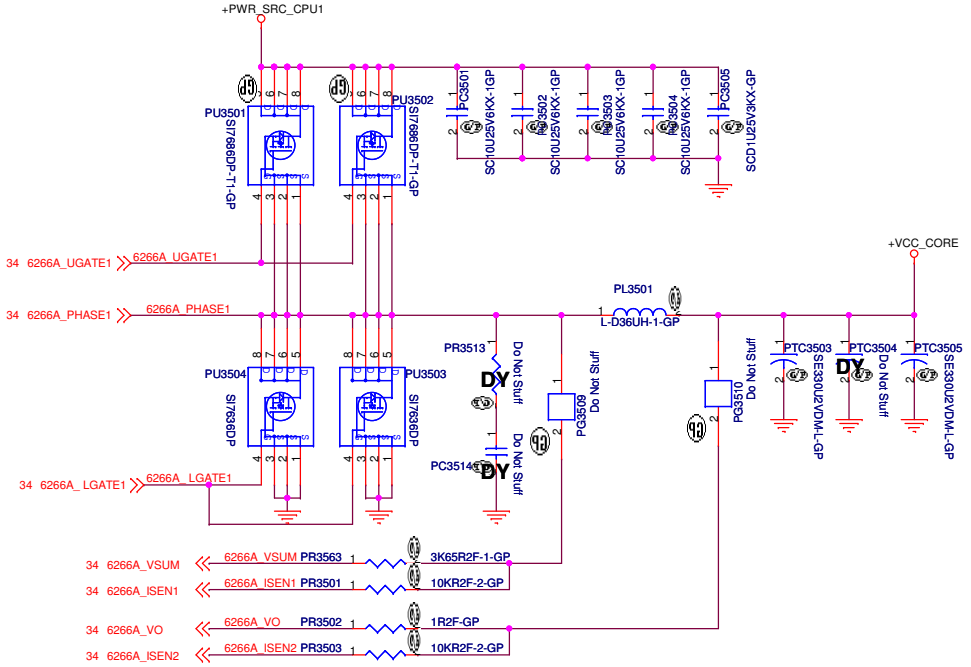
Size: Custom | Document Number: Alba UMA | Rev: -1

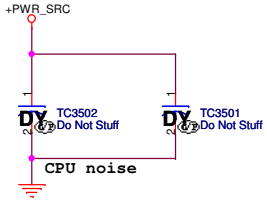
Date: Monday, April 06, 2009 | Sheet 34 of 61

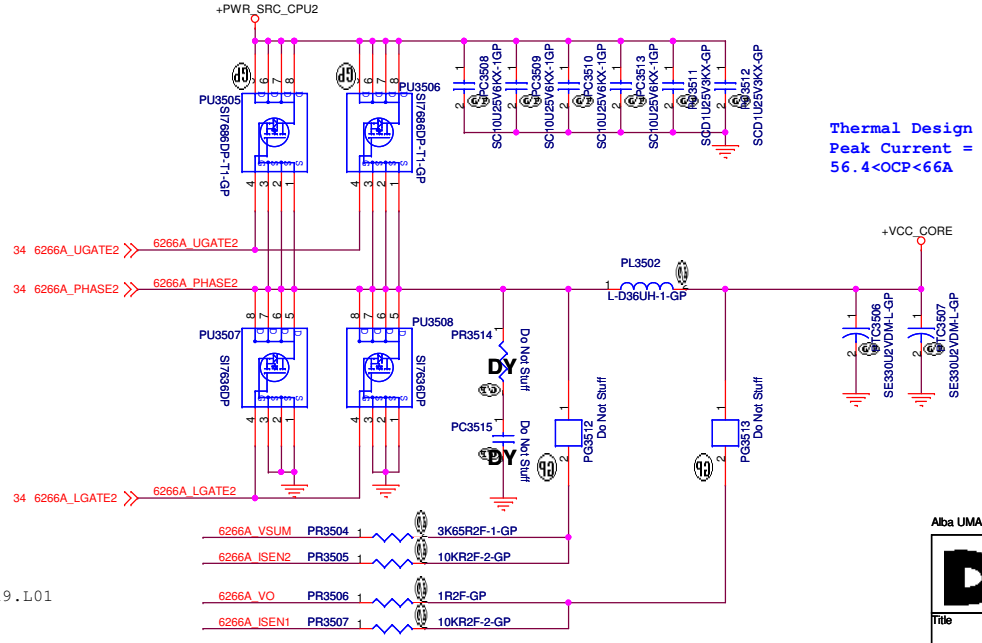
SSID = CPU.Regulator











Thermal Design Current = 36A(IMVP6+ Rev:1.35)
Peak Current = 47A
56.4<OCP<66A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

Alba UMA

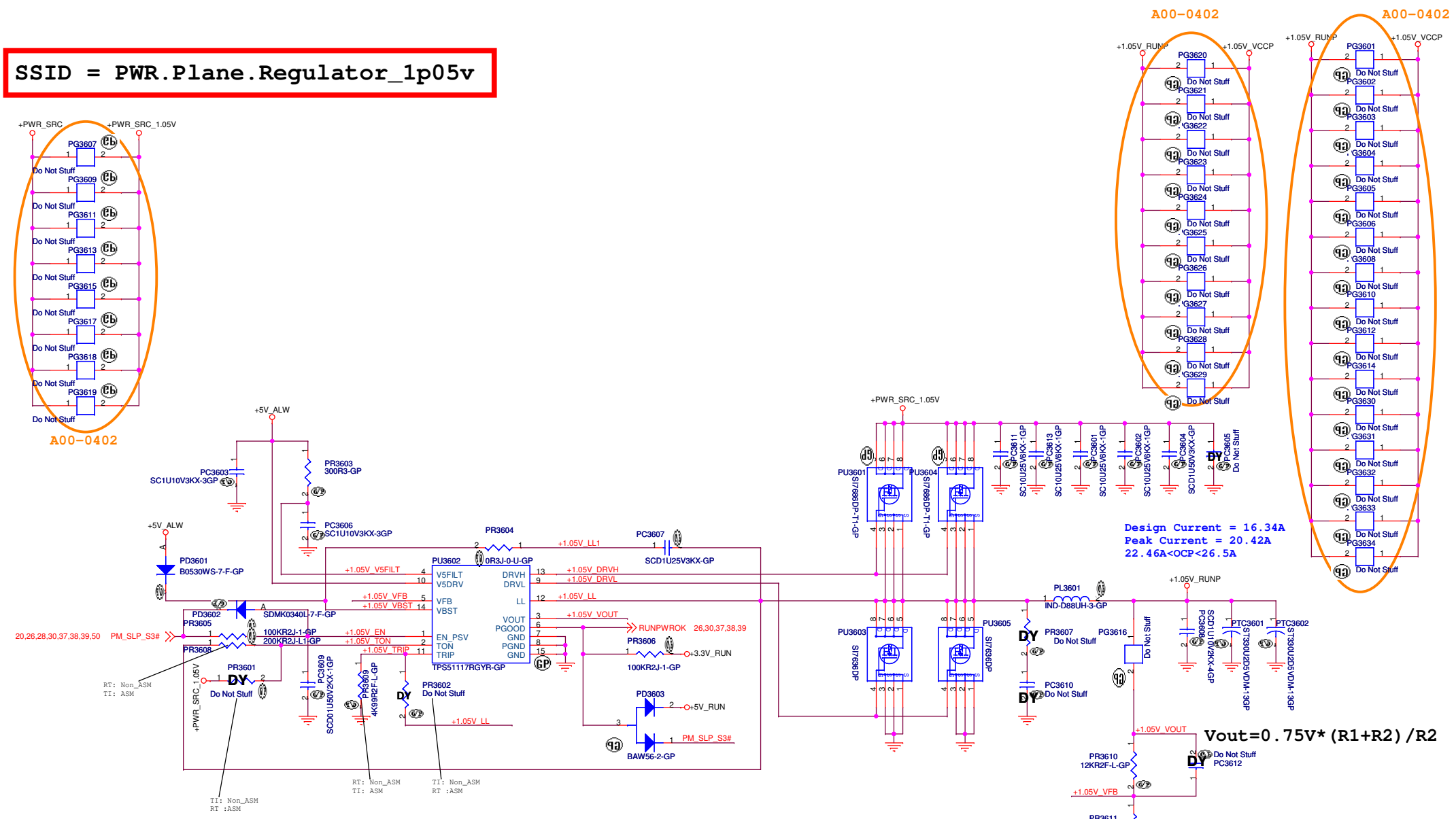
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 35 of 61

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.88UH FDU1040D-R88M=P3 TOKO DCR:2.3mohm Isat =22.2Arms 68.R8810.10B
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037
Switching freq-->350KHz

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1.05V**		
Size: Custom	Document Number: **Alba UMA**	Rev: -1
Date: Monday, April 06, 2009	Sheet 36 of 61	

SSID = PWR.Plane.Regulator_1p5v/1p1v

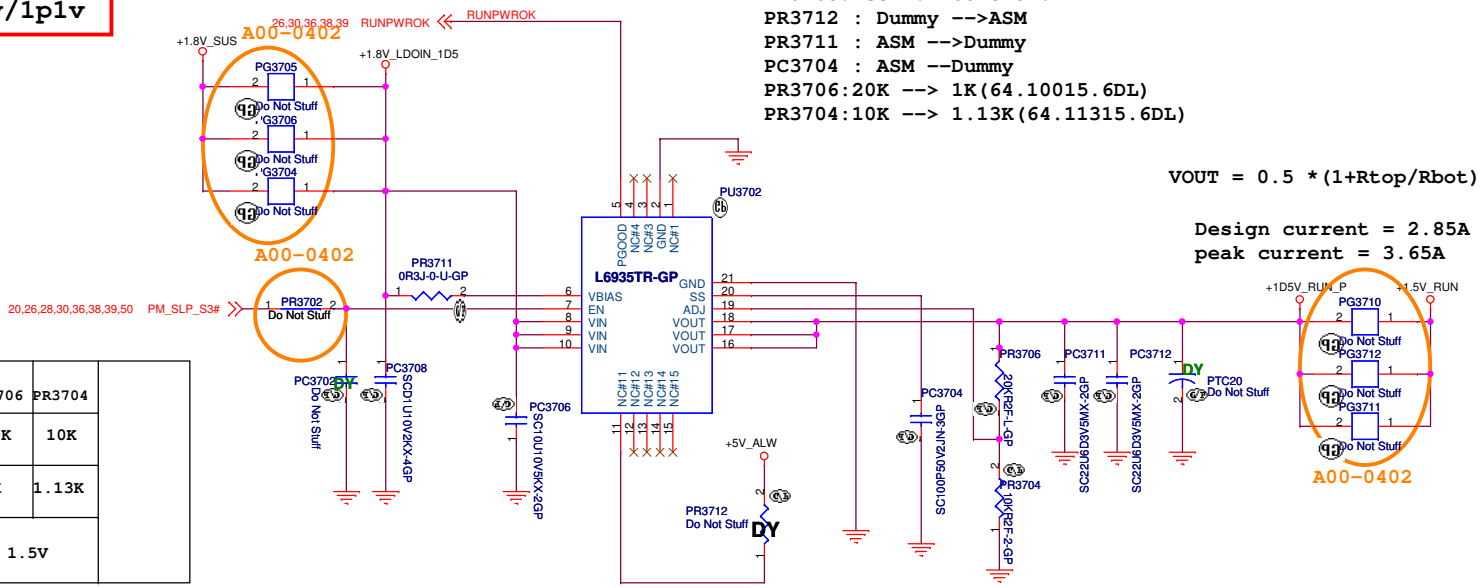
2nd Source BOM Control:
PR3712 : Dummy -->ASM
PR3711 : ASM -->Dummy
PC3704 : ASM --Dummy
PR3706:20K --> 1K(64.10015.6DL)
PR3704:10K --> 1.13K(64.11315.6DL)

VOUT = 0.5 *(1+Rtop/Rbot)

Design current = 2.85A
peak current = 3.65A

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

Vendor	PR3712	PR3711	PR3706	PR3704
L6935	DY	ASM	20K	10K
RTXX35	ASM	DY	1K	1.13K
			1.5V	



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

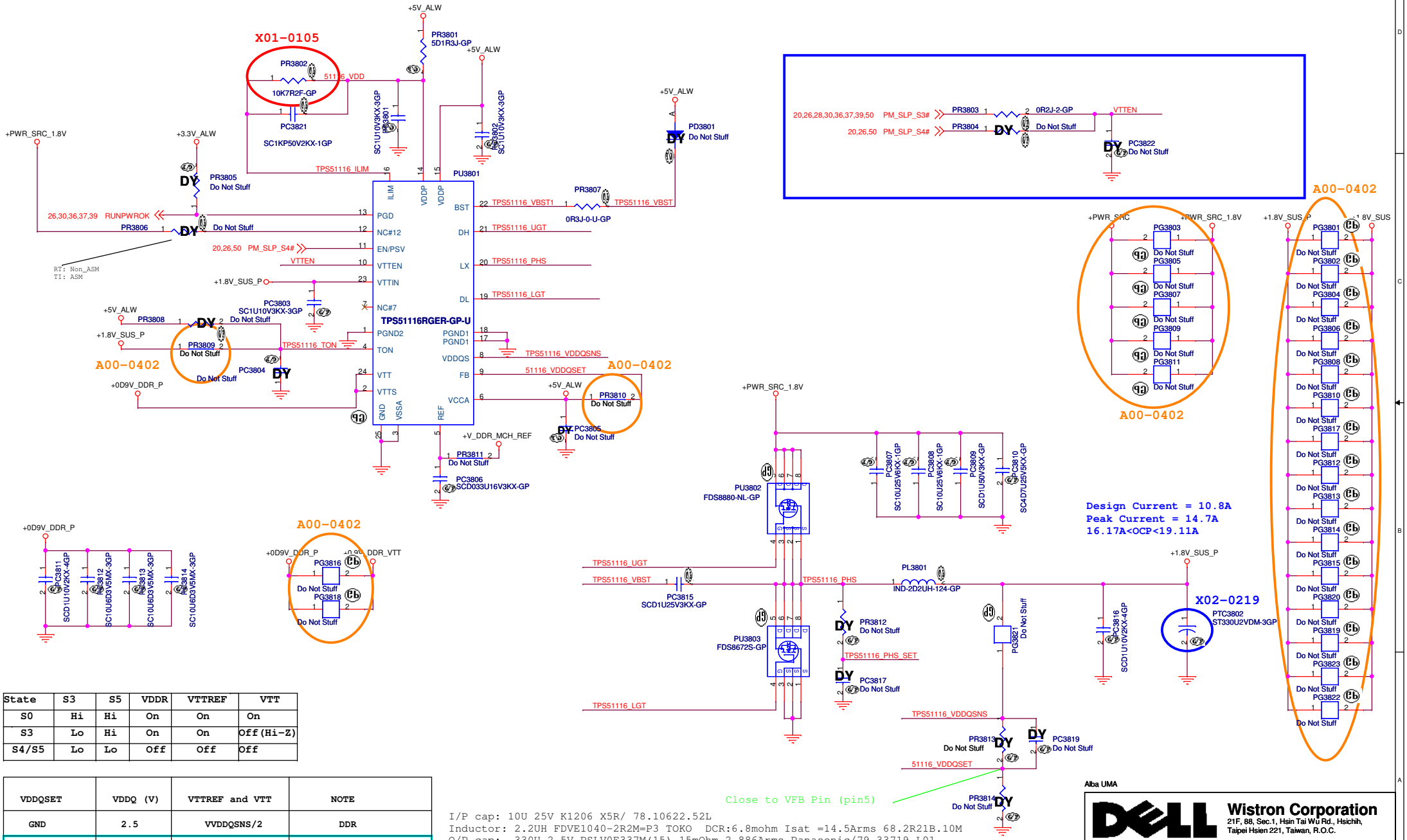
Title: DC to DC L6935_1.5V / L6935_1.1V

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 37 of 61

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms Panasonic/79.33719.L01
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A3784.07636.037

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 38 of 61

SSID = PWR.Plane.Regulator_gfx

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

Size: A3 | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 39 of 61

(Blank)

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

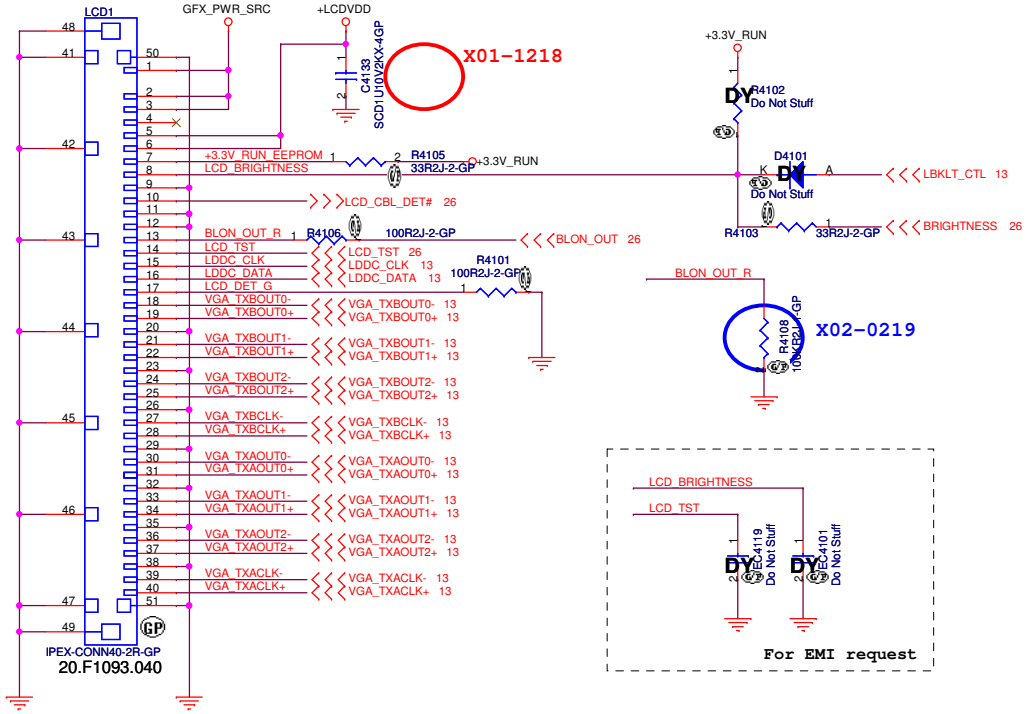
Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 40 of 61

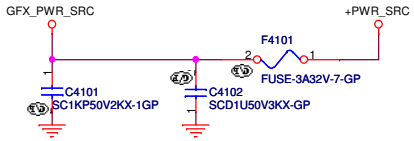
SSID = VIDEO

LVDS CONNECTOR

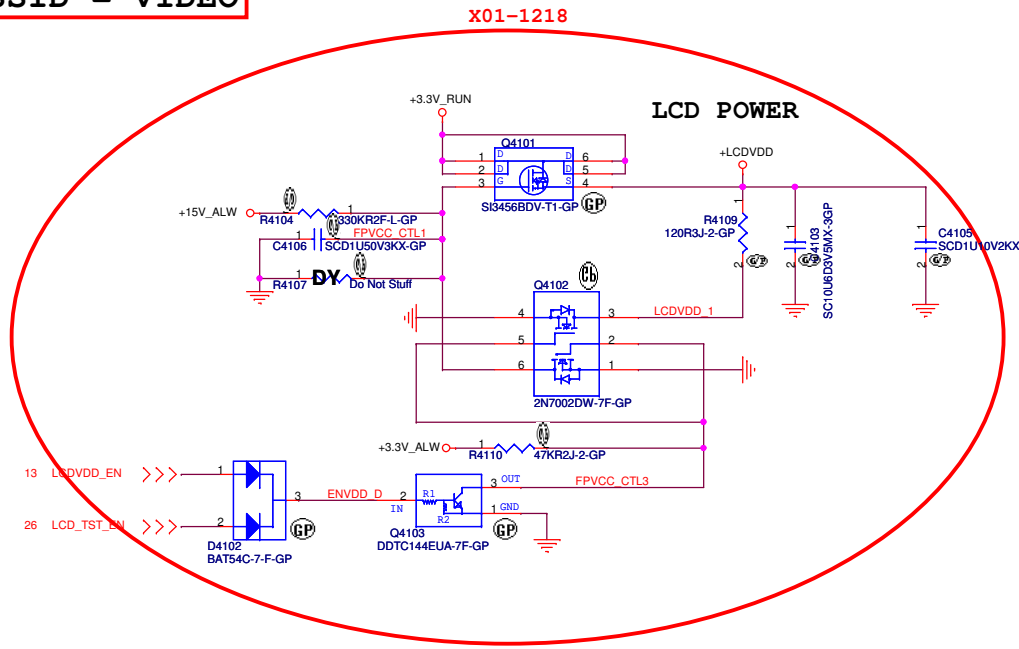


SSID = Inverter

INVERTER POWER



SSID = VIDEO



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD/Inverter Connector*

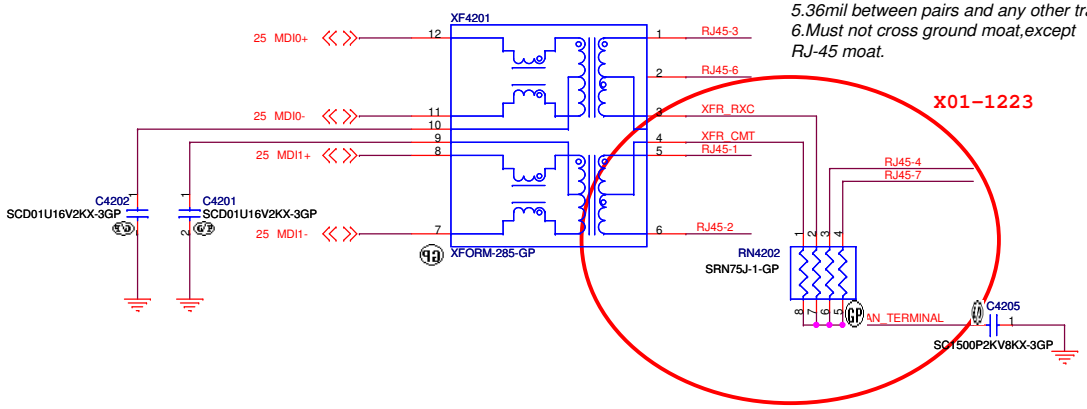
Size	Document Number	Rev
Custom	*Alba UMA*	-1

Date: Monday, April 06, 2009 Sheet 41 of 61

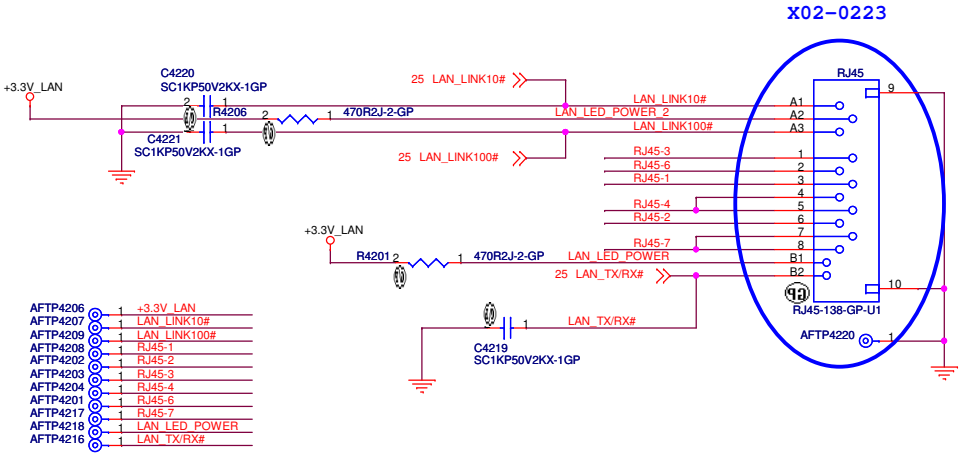
SSID = LOM

1.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
2.No vias, No 90 degree bends.
3.pairs must be equal lengths.
4.6mil trace width,12mil separation.
5.36mil between pairs and any other trace.
6.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer



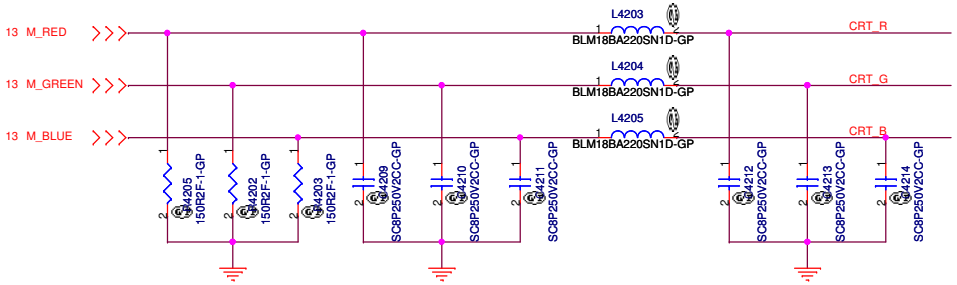
RJ45 Connector

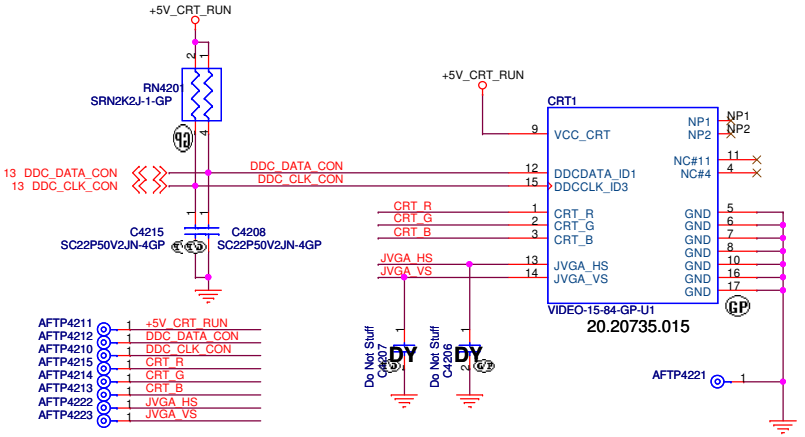


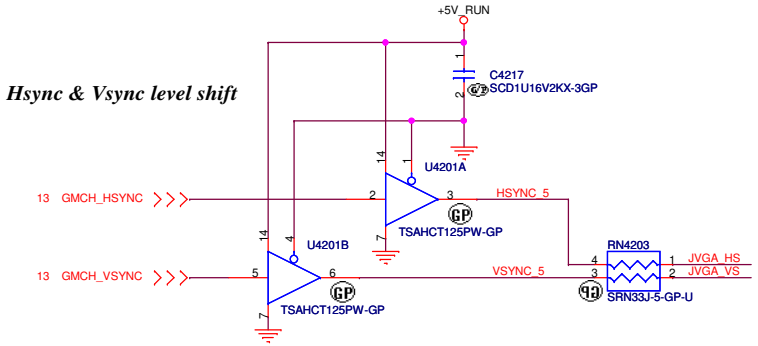
SSID = VIDEO

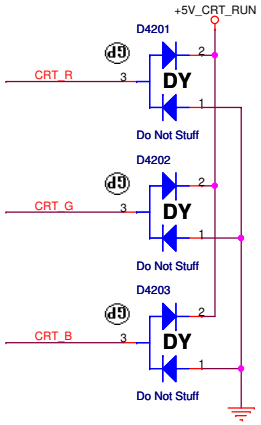
Layout Note:

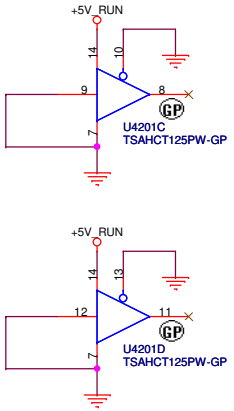
***Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.**
*** RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.**

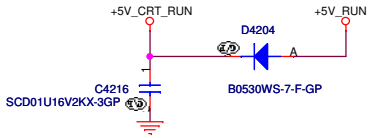












Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

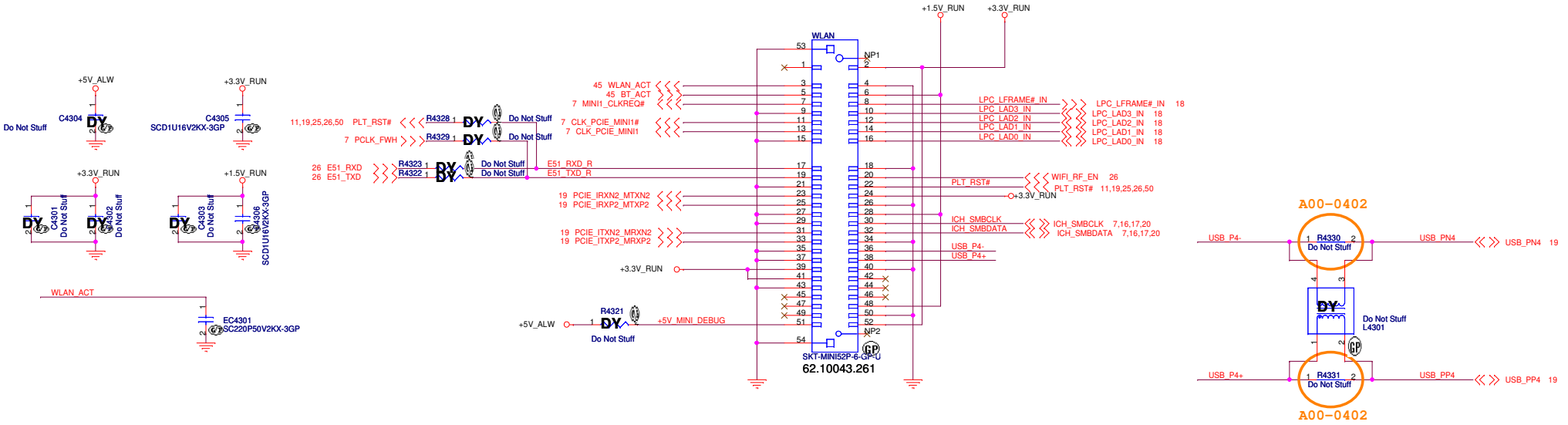
Title: **LAN/CRT Connector**

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 42 of 61

SSID = Wireless

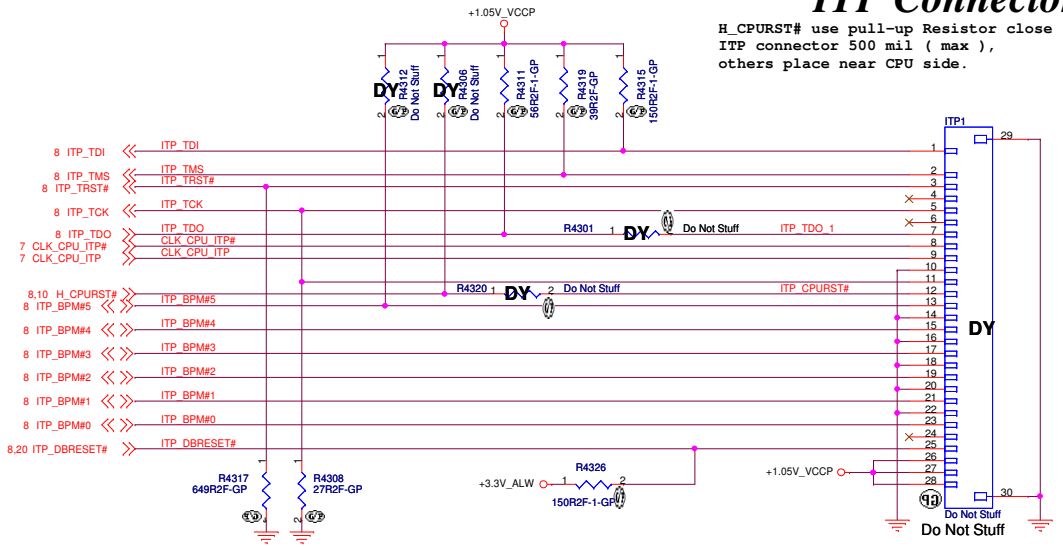
Mini Card Connector(802.11a/b/g/n)



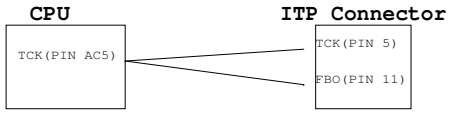
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

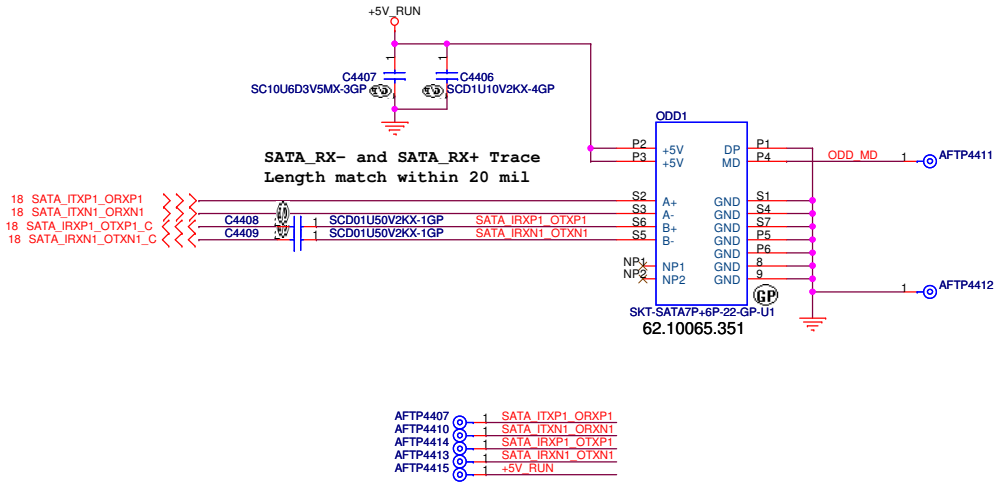
Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 43 of 61

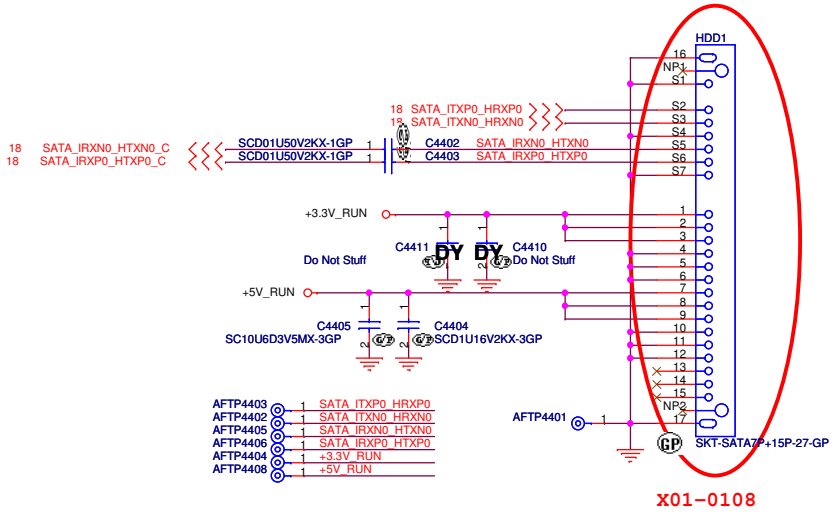
SSID = SATA

ODD Connector



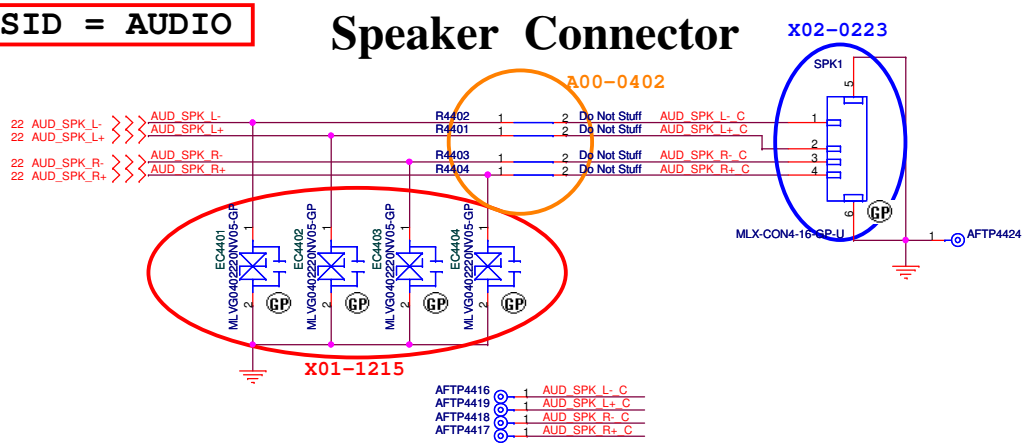
SSID = SATA

SATA HDD Connector



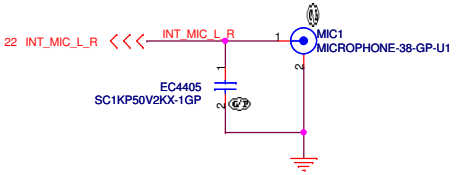
SSID = AUDIO

Speaker Connector



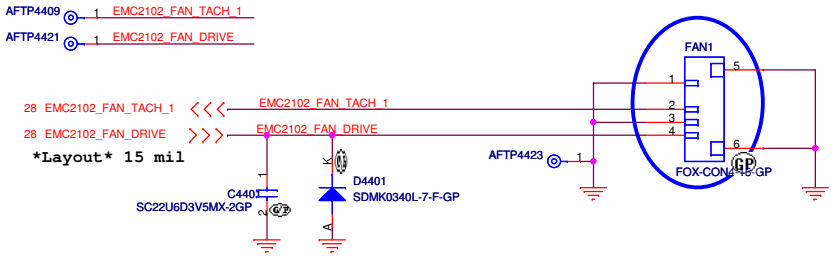
SSID = AUDIO

Internal MIC



SSID = Thermal

Fan Connector



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

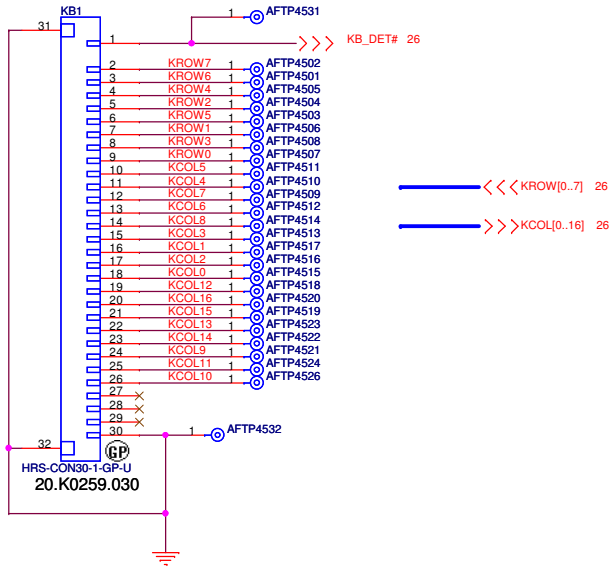
Title: HDD/ODD/FAN/SPEAKER/MIC

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 44 of 61

SSID = KBC

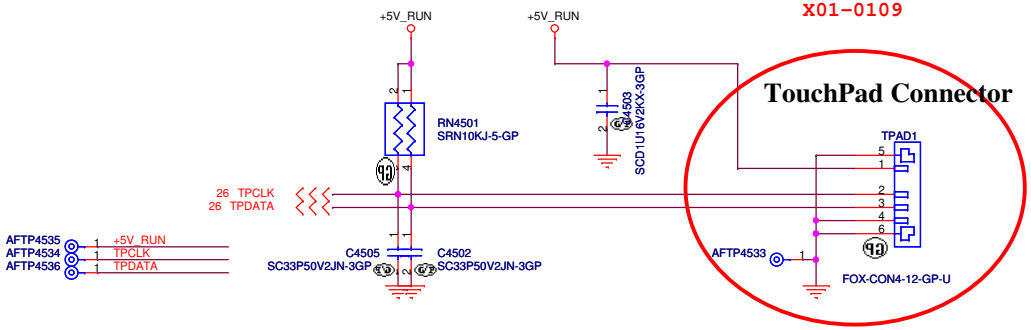
Internal KeyBoard Connector



SSID = Touch.Pad

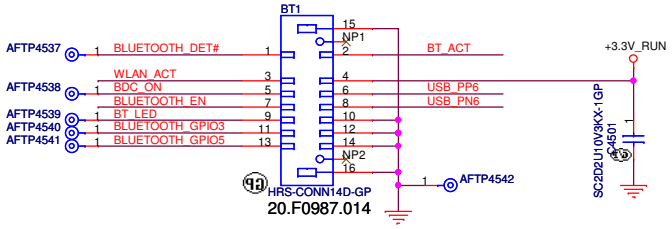
X01-0109

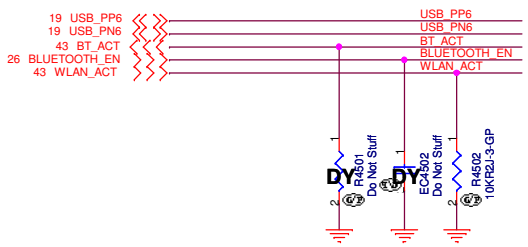
TouchPad Connector

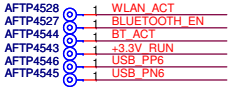


SSID = User.Interface

Bluetooth Module conn.







Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard/TouchPad/BT

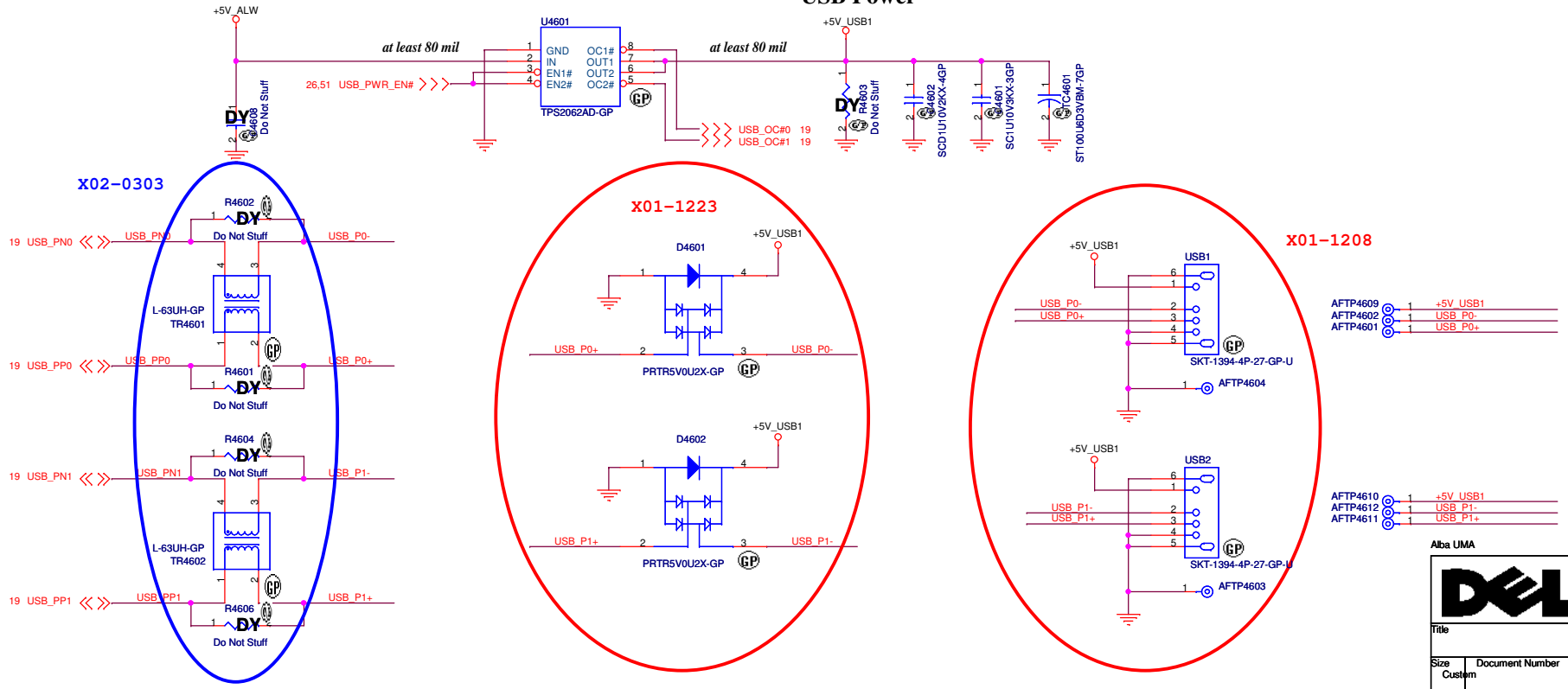
Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 45 of 61

SSID = Modem

X01-1204

USB Power



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

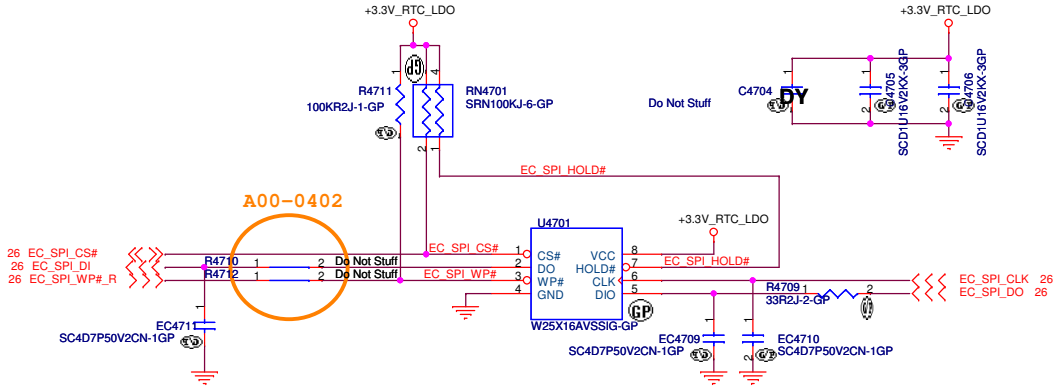
Title: MDC CONN

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 46 of 61

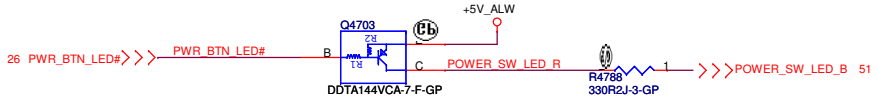
SSID = Flash.ROM

SPI FLASH ROM (16M bits)

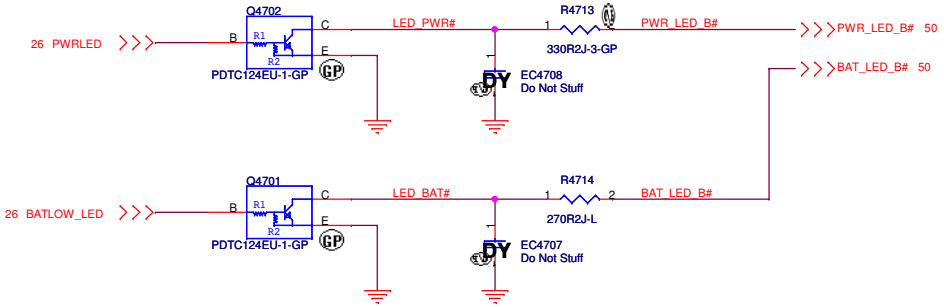


SSID = User.Interface

Power Button LED

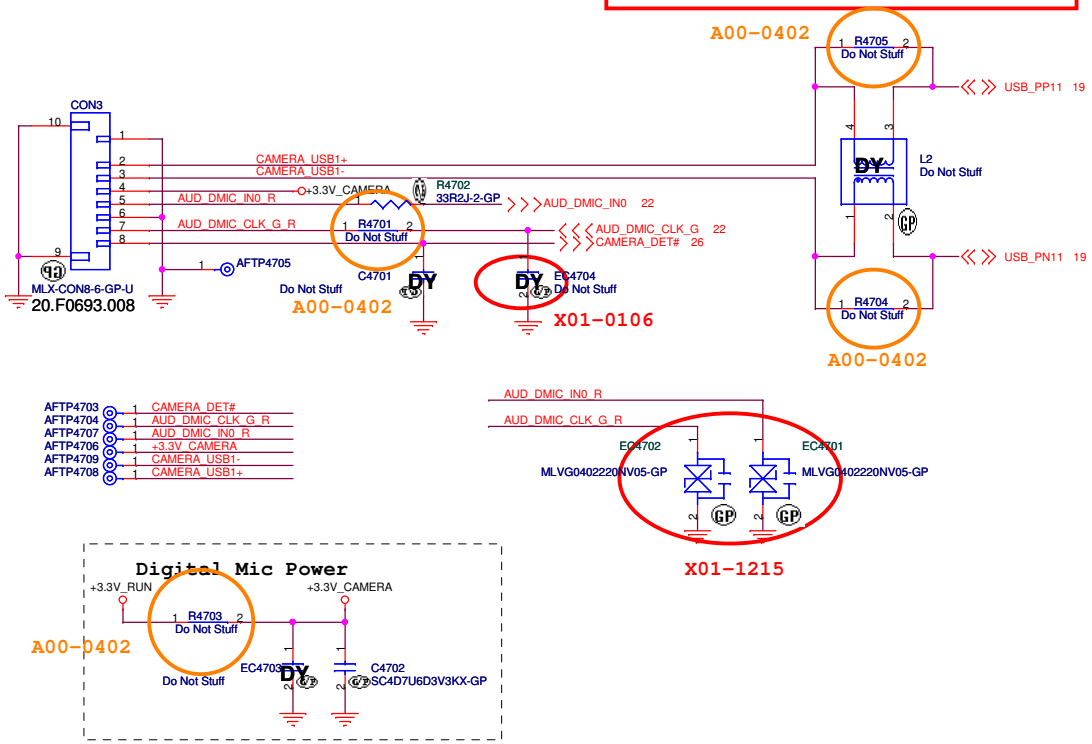


Power/Battery LED



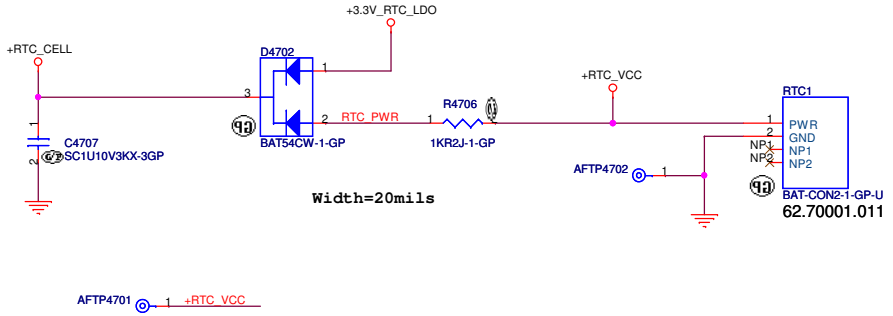
Camera Connector

SSID = User.Interface



SSID = RBATT

RTC Connector



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SPI Flash/LED/Camera/RTC	
Size: Custom	Document Number: Alba UMA	Rev: -1
Date: Monday, April 06, 2009	Sheet 47 of 61	

(Blank)

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 48 of 61

(Blank)

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

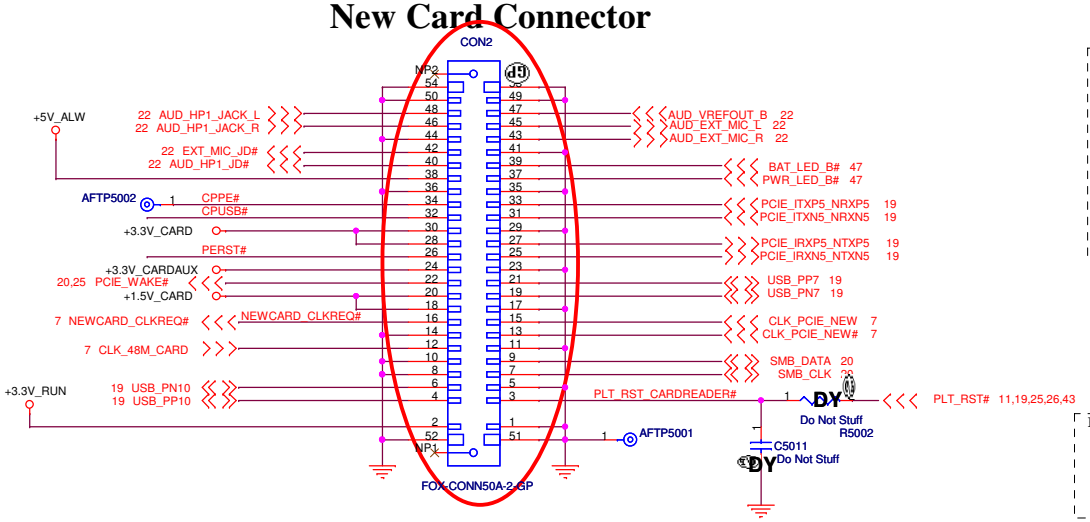
Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

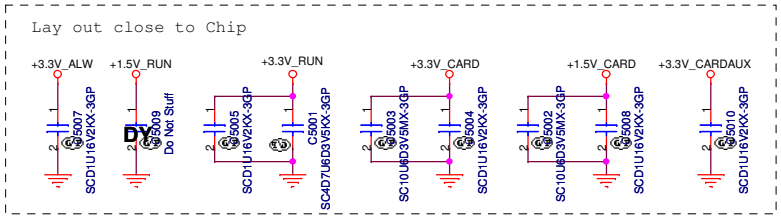
Date: Monday, April 06, 2009 | Sheet 49 of 61

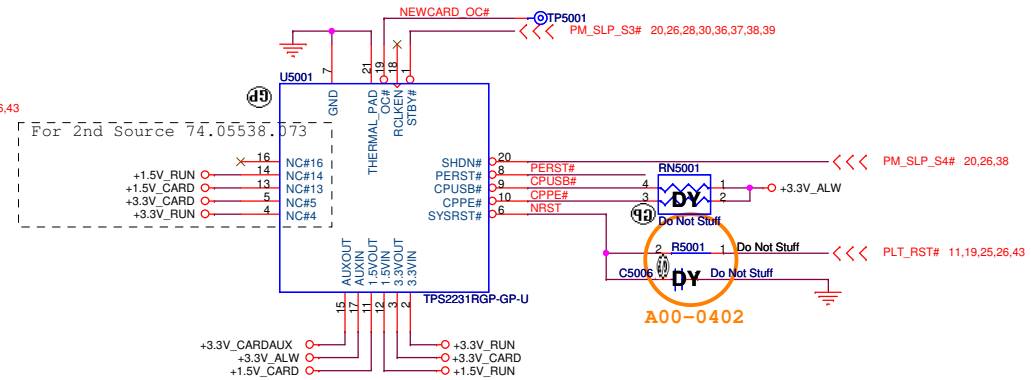
SSID = ExpressCard

New Card Connector



X01-0106





A00-0402

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

AFTP5029	1	PWR_LED_B#
AFTP5032	1	BAT_LED_B#
AFTP5031	1	+5V_ALW
AFTP5030	1	PLT_RST_CARDREADER#
AFTP5020	1	PCIE_ITXP5_NRXP5
AFTP5025	1	PCIE_ITXN5_NRXN5
AFTP5023	1	PCIE_IRXP5_NTXP5
AFTP5024	1	PCIE_IRXN5_NTXN5
AFTP5026	1	AUD_VREFOUT_B
AFTP5004	1	AUD_HP1_JACK_L
AFTP5006	1	AUD_HP1_JACK_R
AFTP5007	1	+3.3V_RUN
AFTP5009	1	CPUSB#
AFTP5005	1	USB_PP7
AFTP5008	1	USB_PN7
AFTP5011	1	AUD_EXT_MIC_L
AFTP5010	1	AUD_EXT_MIC_R
AFTP5017	1	EXT_MIC_JD#
AFTP5013	1	AUD_HP1_JD#
AFTP5014	1	CLK_48M_CARD
AFTP5012	1	NEWCARD_CLKREQ#
AFTP5019	1	+3.3V_CARD
AFTP5015	1	PERST#
AFTP5022	1	+3.3V_CARDAUX
AFTP5021	1	PCIE_WAKE#
AFTP5016	1	+1.5V_CARD
AFTP5018	1	SMB_DATA
AFTP5003	1	SMB_CLK
AFTP5027	1	USB_PN10
AFTP5028	1	USB_PP10

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

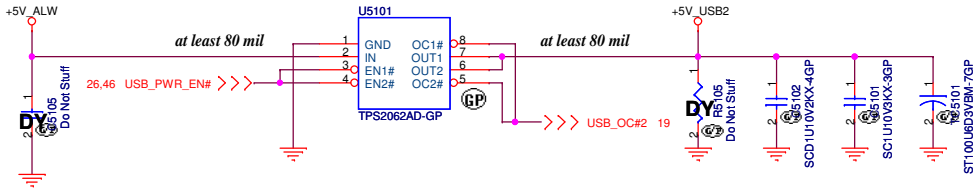
Title: Express Card Board CONN

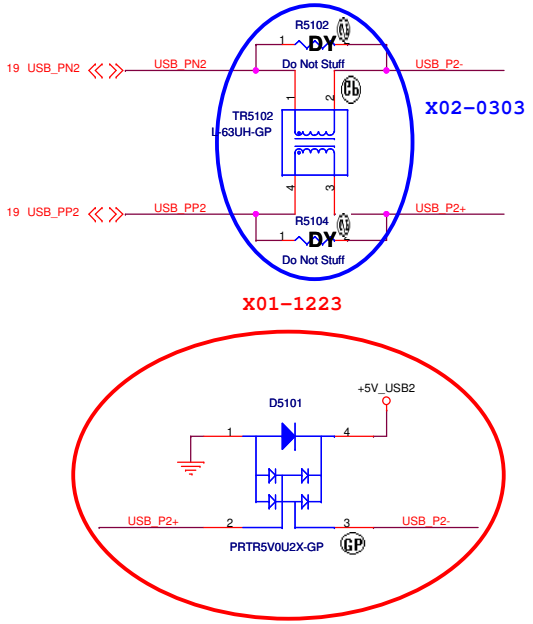
Size	Document Number	Rev
Custom	Alba UMA	-1

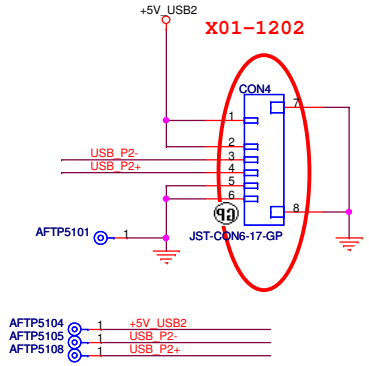
Date: Monday, April 06, 2009 Sheet 50 of 61

SSID = USB

USB Power

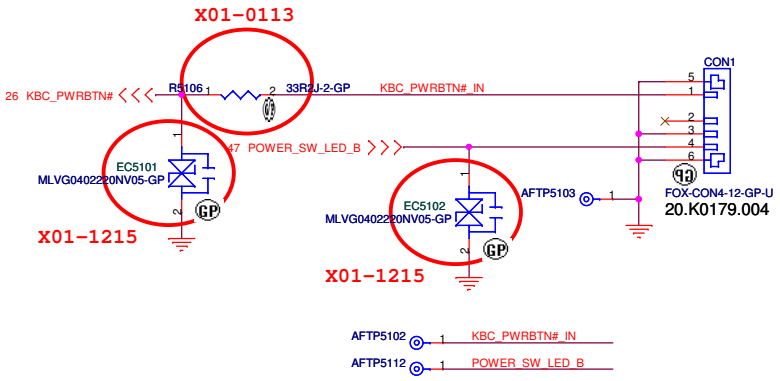


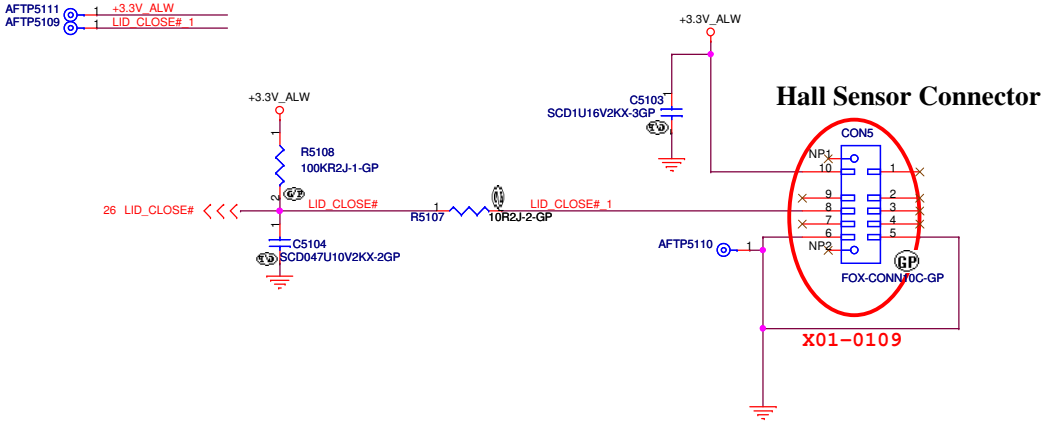




SSID = User.Interface

Power Button Board CONN





Alba UMA

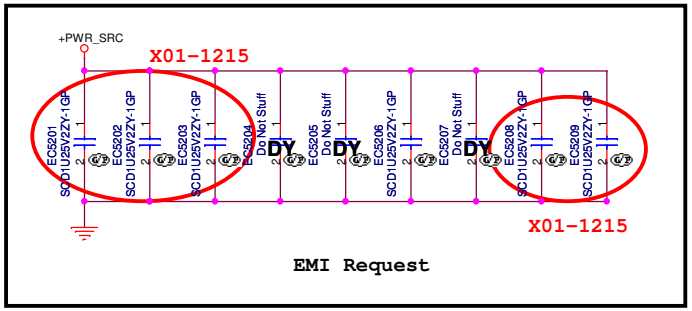
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

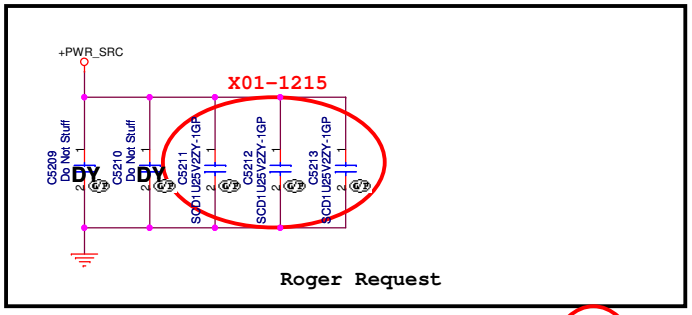
Title: Power Button/Hall Sensor/USB Board

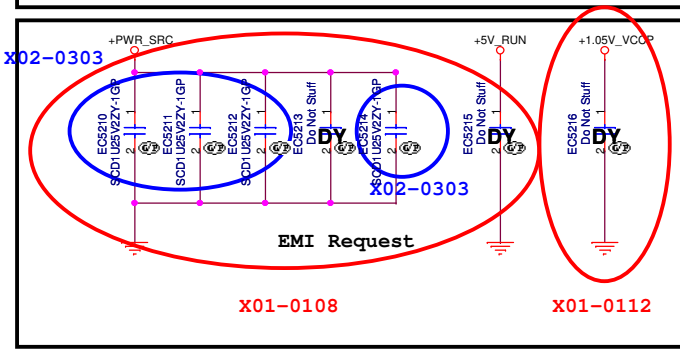
Size	Document Number	Rev
Custom	Alba UMA	-1

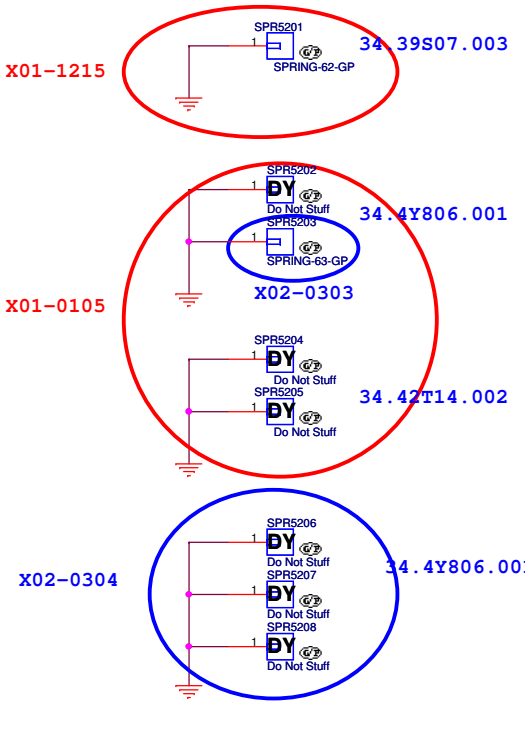
Date: Monday, April 06, 2009 Sheet 51 of 61

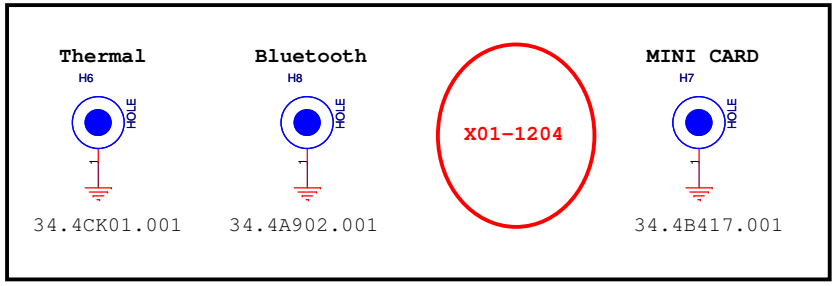
SSID = Mechanical











Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 52 of 61

SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 53 of 61

SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-TV/CRT/DP PORT

Size	Document Number	Rev
C	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 54 of 61

SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size	Document Number	Rev
A2	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 55 of 61

SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-MEMORY/STRAPS(4/4)

Size: A2 | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 56 of 61

SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 57 of 61

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20,26	2008/11/03	Wistron	UMA no need.	ICH gpio6 NC,KBC gpio45 NC,Remove R2030,R2635	X01
2	34	2008/11/19	Wistron	LoadLine is too low.	Change PR3431 to 3.48K ohm.	X01
3	25	2008/11/25	Realtek	Prevent for capacitance effect.	Change R2506 to 1K ohm.	X01
~~4~~	~~22~~	~~2008/11/27~~	~~IDT~~	~~PC beep issue.~~	~~Change R2203,R2206 to 10K ohm. Add R2218,R2219.~~	~~X01~~
5	26	2008/11/27	Wistron	MB version changed.	Change R2609 pop,R2608 dummy.	X01
6	15	2008/11/27	Wistron	Reserve +3.3V_RUN trace.	Add R1518.	X01
7	25	2008/12/18	KDS	Follow crystal vendor test result.	Change C2501 to 18pF,C2502 to 15pF	X01
8	18,46,52	2008/12/04	Dell	Remove MDC function.	Remove MDC schematics,holding,stand off.	X01
9	46	2008/12/04	Wistron	ID modify,Change USB connector.	Change USB connector from one dual port to two single port.(22.10218.T51)	X01
10	45	2008/12/04	Wistron	Change touch pad connector.	Change touch pad connector to 20.K0179.004	X01
11	42	2008/12/08	Wistron	Change RJ45 connector.	Change RJ45 connector to 22.10177.C81	X01
12	33	2008/12/15	Wistron	Add 15_ALW Schematics.	Add 15_ALW Schematics.	X01
13	30	2008/12/15	Wistron	Modify 3V 5V schematics.	Modify 3V 5V schematics.	X01
~~14~~	~~22~~	~~2008/12/15~~	~~Wistron~~	~~Diancetic mode sound is too slow.~~	~~Modify PC Beep schematcis.~~	~~X01~~
15	26,41	2008/12/15	Wistron	For Panel Test.	Add LCD_TST_EN for panel test. R2638 POP.	X01
16	52	2008/12/15	Wistron	EMI issue.	Add SPR5201.	X01
17	28	2008/12/15	Wistron	Rename trace name.	Rename T8_THERMDC and T8_THERMDA.	X01
18	41	2008/12/17	Wistron	CMO panel white screen issue.	Reseve R4108.	X01
19	41	2008/12/18	Wistron	LCD Power Sequence Issue.	Modify LCD Power schematics.~~Change LCD CONN part.~~	X01
20	52	2008/12/18	Wistron	EMI Issue.	Add SPR5202.	X01
~~21~~	~~42~~	~~2008/12/19~~	~~Wistron~~	~~CRT R.G.B EA test issue.~~	Change bead to 47ohm and depop capacitors for π filter.	~~X01~~
22	32	2008/12/10	Wistron	Prevent leakage from KBC.	Change PR3203 pull high from +3.3V_ALW to +3.3V_RTC_LDO.	X01

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List1 - EE

Size: A3 | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 58 of 61

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
23	44,52 51,47	2008/12/15	Wistron	Modify based on EMI test result.	EC5203/C5212/EC5202/C5211/C5213/EC5206/EC5201/EC5208 use 0.1u-Cap EC4701/EC4702/EC4401/EC4402/EC4403/EC4404/EC5101 use 22P5V-Varistor POWER_SW_LED_B add one 22P5V-Varistor Add EC5209 0.1uF cap.	X01
24	20,42,46	2008/12/23	Wistron	Layout request.	Swap TR4602,RN2001,RN4202,TR4601 net.	X01
25	46,51	2008/12/23	Wistron	For EMI request.	Add D4601,D4602,D5101	X01
26	52	2009/01/05	Wistron	Reserve 3 Spring.	Add SPR5203,SPR5204,SPR5205.Dummy SPR5202.	X01
27	15	2008/12/30	Wistron	Remove R1515.For layout get good performance.	Remove R1515,change R1549 to 2.2uF.	X01
28	50	2009/01/06	Wistron	Change CON2 connector.	Change CON2 connector to 20.F1400.050.	X01
29	9	2009/01/06	Wistron	For VCC_CORE sense.	Add PG901,PG902. Dummy C925,Pop C901	X01
30	47,52	2009/01/06	Wistron	For EMI request.	Reserve EC4704,EC5210,EC5211,EC5212,EC5213,EC5214	X01
31	26	2009/01/06	Wistron	Keyboard detect.	Pop R2625.	X01
32	52	2009/01/08	Wistron	For EMI request.	Reserve EC5215 for +5V_RUN	X01
33	44,51	2009/01/08	Wistron	Change HDD1,CON5 connector.	Modify HDD1,CON5 symbol.	X01
34	51	2009/01/09	Wistron	CON5 symbol layout concern.	Change CON5 pin5 to GND,pin7 to NC.	X01
35	45	2009/01/09	Wistron	Touch pad cable change.	Modify TPAD1 pin define.	X01
36	52	2009/01/12	Wistron	For EMI request.	Reserve EC5216.	X01
37	8	2009/01/12	Wistron	GTL issue.	Pop C802.	X01
38	22	2009/01/13	Wistron	Pop noise.	Add KBC GPIO33.	X01
39	51	2009/01/13	Wistron	KBC burn issue.	Change R5106 to 33 ohm.	X01
40	41	2009/02/19	Wistron	CMO panel white screen issue.	Pop R4108.	X02
41	26	2009/02/19	Wistron	Change board ID.	Pop R2601,R2608.Dummy R2602,R2609.	X02
42	31,42,44	2009/02/23	Wistron	Change connector.	Change SPK1,FAN1,RJ45 connector.	X02
43	18,26	2009/02/24	Wistron	Change 32.768K crystal cap size.	Change C1806,C1807,C2607,C2608 to 0603 size.	X02

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change List 2- EE*

Size: A3 | Document Number: *Alba UMA* | Rev: -1

Date: Monday, April 06, 2009 | Sheet 59 of 61

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
44	22	2009/02/27	Wistron	Codec pop noise.	Add Q2201~Q2205. Change C2204 to 2.2uF. Move 60.4 ohm from small board to MB.	X02
45	46,51,52	2009/03/03	Wistron	Modify based on EMI test result.	EC5212,EC5211,EC5210,EC5214 -- 0.1u cap on board TR4602,TR4601,TR5102 -- 67ohm common mode on board spr5203--spring on board	X02
46	26	2009/03/03	Wistron	Remove PAID for KB detection	Dummy R2625.	X02
47	52	2009/03/04	Wistron	For EMI request.	Add SPR5206,SPR5207,SPR5208.	X02
48	26	2009/04/02	Wistron	Board ID Changed.	Pop R2604,Dummy R2603.	X02

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change List 3 - EE*

Size: A3 | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 60 of 61

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	33	2008/12/15	Wistron	3D3V OCP over spec.	Change R3312 from 160K to 86.6K ohm.	X01
2	33	2009/01/05	Wistron	5V output voltage is too high.	Change PR3310 from 30.9K to 33K ohm. Change PR3314 from 20K to 21.5K ohm.	X01
3	33	2009/01/05	Wistron	5V H/S MOSFET VDS over spec.	Add Snubber PR3319 to 2.2K ohm, PC3319 to 560pF.	X01
4	33	2009/01/05	Wistron	5V OCP over spec.	Change R3311 from 160K to 147K ohm.	X01
5	33	2008/12/15	Wistron	Add 15V_ALW schematics	Add 15V_ALW schematics. DY PR3306	X01
6	34	2008/11/27	Wistron	LoadLine is too low.	Change PR3431 from 3.92K to 3.48K ohm.	X01
7	34	2009/01/05	Wistron	CPU_CORE OCP is too low.	Change PR3418 from 12.1K to 13.7K ohm.	X01
8	38	2009/01/05	Wistron	UMA 1D8V OCP is too low.	Change PR3802 from 8.06K to 10.7K ohm.	X01
9	39	2009/02/19	Wistron	Change main source.	Change PTC3301,PTC3302 to 77.22271.27L.	X02
10	38	2009/02/19	Wistron	Change main source.	Change PTC3802 to 79.33719.20D.	X02
11	32	2009/03/02	Wistron	Change cap from 25V to 50V.	Change PC3208,PC3209 to 78.10424.2BL	X02
12	31	2009/03/02	Wistron	Change main source.	Change PD3107 to 83.22R03.03G.	X02
13	33	2009/03/03	Wistron	Phase voltage is too high.	PC3319 change from 560pF to 680pF	X02
14	34	2009/03/03	Wistron	LoadLine is too high.	PR3431 change from 3.48K ohm to 3.92K ohm.	X02
15	33	2009/03/05	Wistron	15_ALW no need to install PD3303.	Dummy PD3303.	X02
16	32	2009/04/02	Wistron	Sequence issue.	Change PC3207 from 1uF to 0.1uF.	A00
17	32	2009/04/06	Wistron	For CPU transition response.	Change PC3409 from 100p to 150p.	A00

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change List - Power*

Size: A3 | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 61 of 61