

COMPAL CONFIDENTIAL

MODEL NAME : **VAW50**

PCB NO : **LA-A101P (DA8000WA000)**

BOM P/N :

GPIO MAP: 3.0

Alpine 15"

Haswell ULT

Gerber Date : 2013-08-22

REV : 1.0

@ : Nopop Component

1@ : M/B SPI ROM

TAA@ : TAA/B SPI ROM

CONN@ : Connector Component

DIS@ : Discrete Pop Component

UMA@ : UMA Pop Component

EMI@ : EMI Component

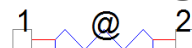
ESD@ : ESD Component

RF@ : RF Component

XDP@ : XDP Component


eTP@ : TS eTP Component

NeTP@ : TS non - eTP Component

 **@ : Short Pad**

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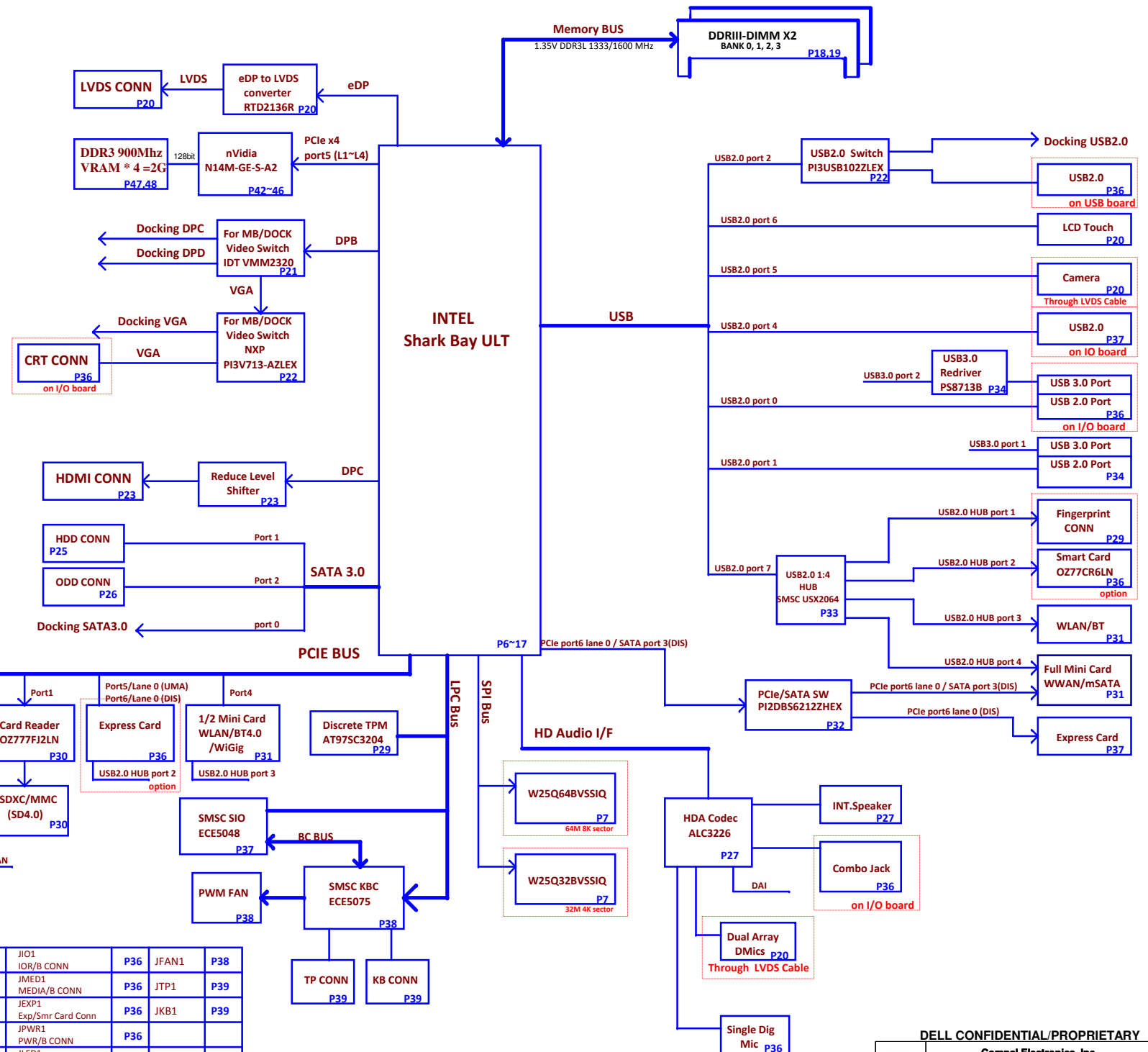
	Compal Electronics, Inc.		
	Title Cover Sheet		
	Size	Document Number LA-A101P	Rev 1.0
Date: Monday, September 23, 2013 Sheet 1 of 65			

- XDP Port P9
- WiFi ON/OFF on USB board
- DC/DC Interface P40
- LED P41
- FFS LNG3DM P25

- DAI
- SATA3.0 port 2
- USB2.0 port 3
- USB2.0 port 2
- USB3.0 port 4
- Docking DPC
- Docking DPD
- Docking VGA
- Docking LAN
- P35

PWR_+5V_ALW/3.3V_ALW	P52
PWR_+1.35V_MEN/+0.675V_DDR	P53
PWR_+1.05V_TTP	P54
PWR_1.5V_RUN	P55
PWR_+VCC_CORE	P56
PWR_Charger	P58
PWR_Selector	P59
PWR_VGA_CORE	P60
PWR_+1.5VDDR	P62

BATT Conn	P51	JTS(Touch Screen)	P22	JIO1 IOR/B CONN	P36	JFAN1	P38
DC-IN Conn	P51	JBIO(Finger print)	P29	JMED1 MEDIA/B CONN	P36	JTP1	P39
TAA CONN	P7	uSIM	P31	JEXP1 Exp/Smr Card Conn	P36	JKB1	P39
JAPS CONN	P9	JBT1 RTC Battery	P32	JPWR1 PWR/B CONN	P36		
XDP CONN	P9	JDOCK1	P35	JLED1 LED/B CONN	P36		
LVDS CONN	P20	JUDB1 USB/B CONN	P36	JDEG1	P38		



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UMA Block Diagram
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->MB-->LEFT
	USB3.0 2		USB3.0-->IOB-->Rear Right
PCIE 1	USB3.0 3		PCIE1-->MMI PCIE
PCIE 2	USB3.0 4		USB3.0-->Docking
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			GPU(DIS)/Express card(UMA)
PCIE 6		SATA 3	WWAN(mSATA)/Express card(PCIE)
		SATA 2	ODD
		SATA 1	HDD
		SATA 0	DOCK

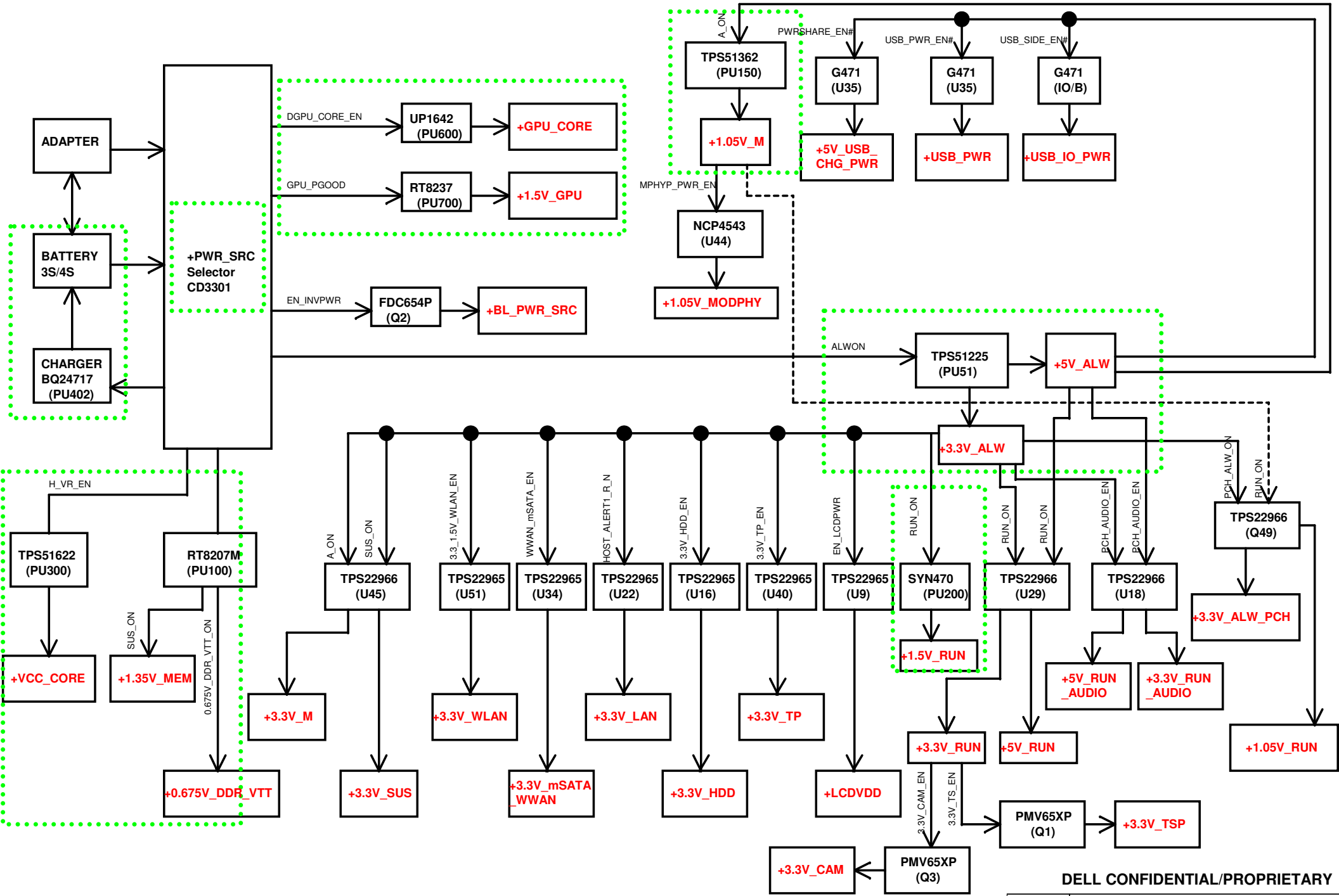
HSW ULT	USB PORT#	DESTINATION
	0	Ext Port 1(I/O) RIGHT
	1	Ext Port 2 (MB/Debug Port) LEFT
	2	USB 2.0 Switch
	3	E-DOCK1
	4	Ext Port 4 (I/O) USB2.0
	5	Camera
	6	Touch Screen
7	USB HUB	

OC#	USB Port	DESTINATION
USB_OC0#	0	IOR/B USB3.0
USB_OC1#	1	M/B USB3.0
USB_OC2#	2 (USB Switch)	USB/B USB2.0
USB_OC3#	4	IOR/B USB 2.0

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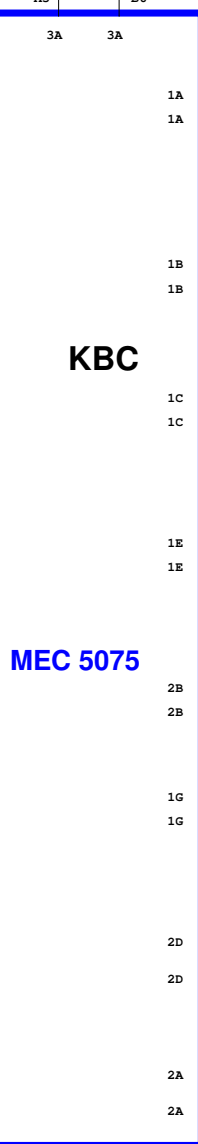
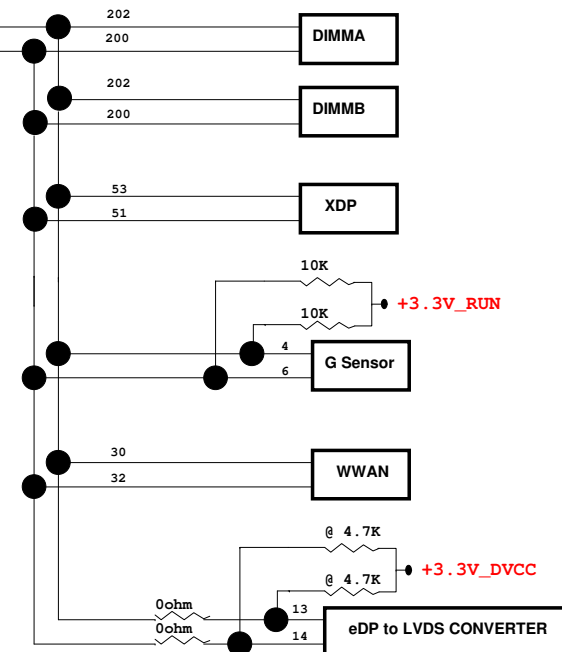
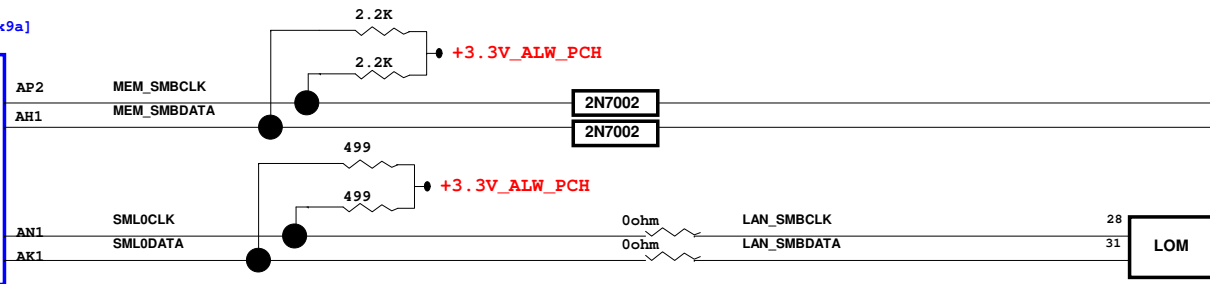
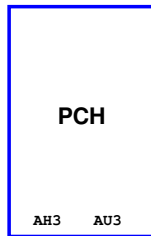
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Power Rail

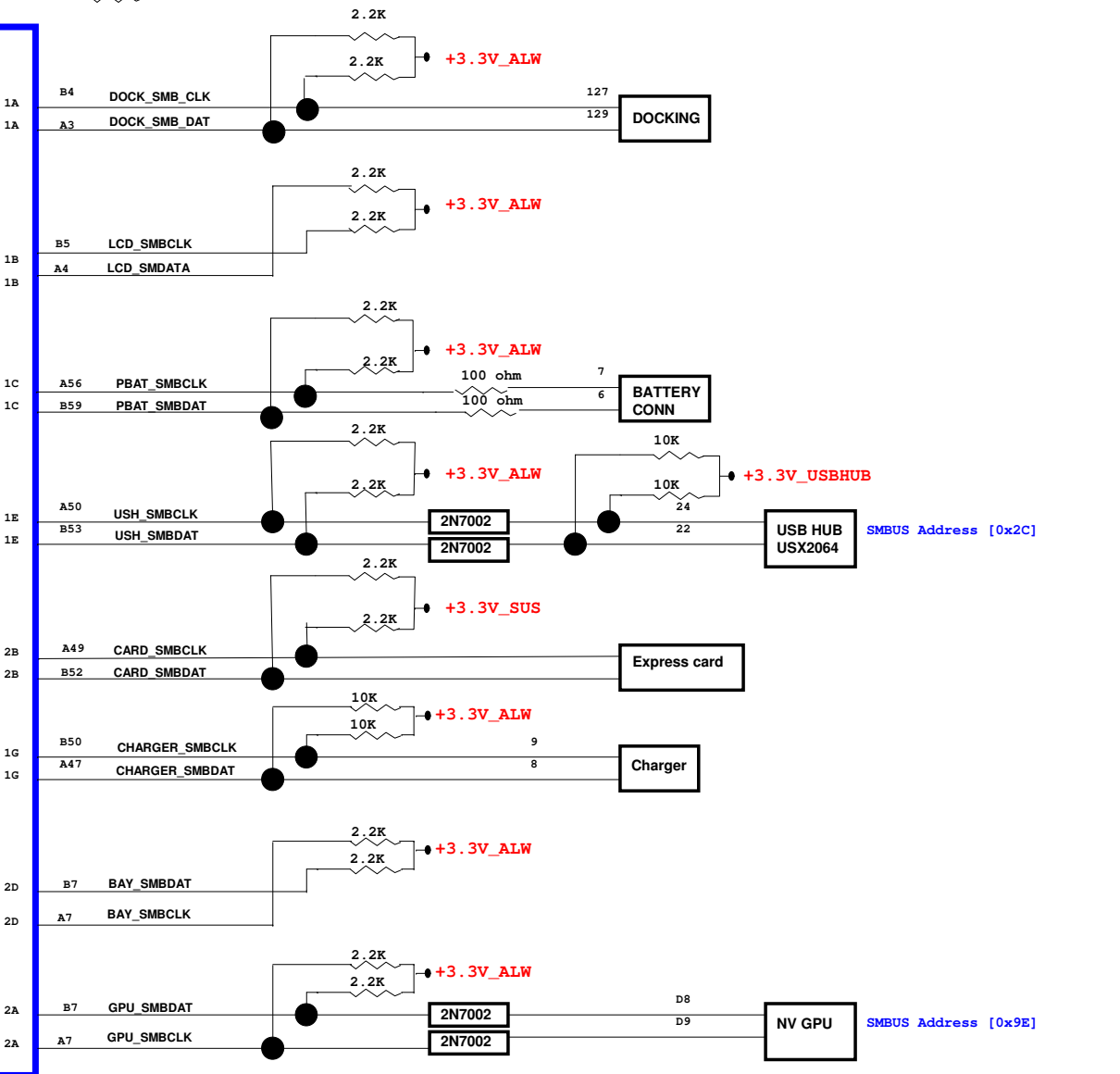
LA-A101P

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SMBUS Address [0x9a]

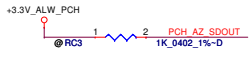
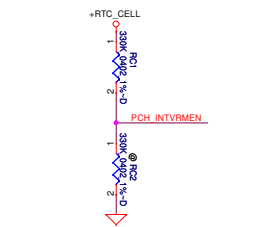


KBC



MEC 5075

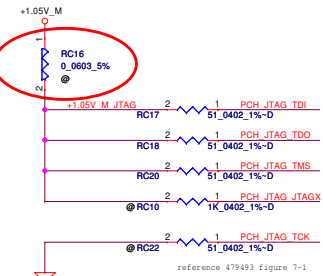
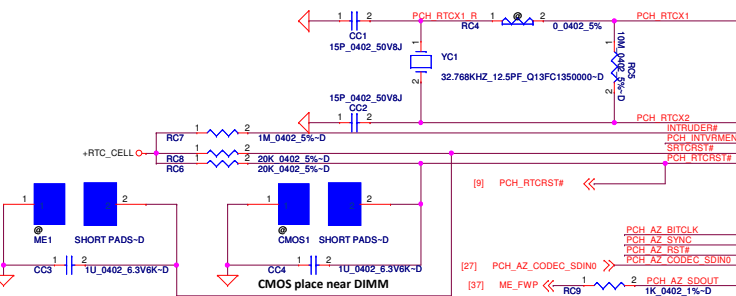
	Compal Electronics, Inc.		
	Title: SMBUS TOPOLOGY		
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INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
 ENABLE
 High - Enable Internal VRs
 Low - Enable External VRs

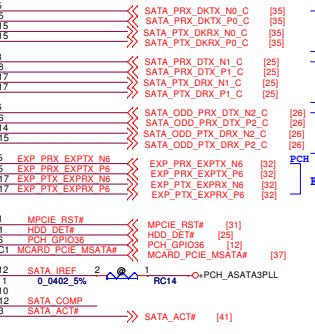
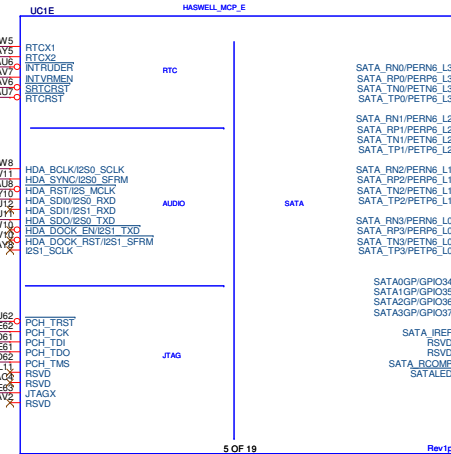
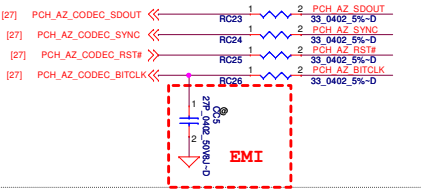
FLASH DESCRIPTOR SECURITY OVERRIDE
 LOW = DISABLED (DEFAULT)
 HIGH = ENABLED

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



reference 479493 Figure 7-1

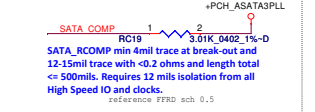
HDA for Codec



SATA_IREF
 SATA_IREF min 4mil trace at break-out and 12-15mil trace with <0.2 ohms and length total <= 500mils. Requires 12 mils isolation from all High Speed IO and clocks.

Shark_Bay_ViLT_P0G 0.5:
 the sampled value for the GPIO corresponding to the particular port during boot time.
 SATA3GP/GPIO37-->SATA3:
 1:SATA
 0:PCIe

SATA Impedance Compensation



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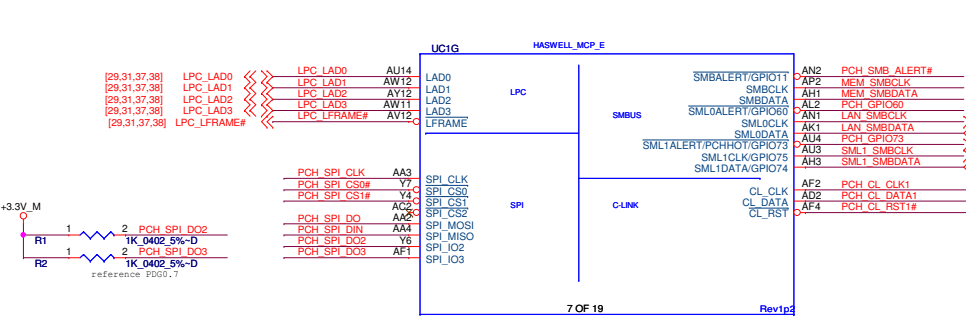
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Title: **MCP(1/12) RTC,SATA,HDA,JTAG**

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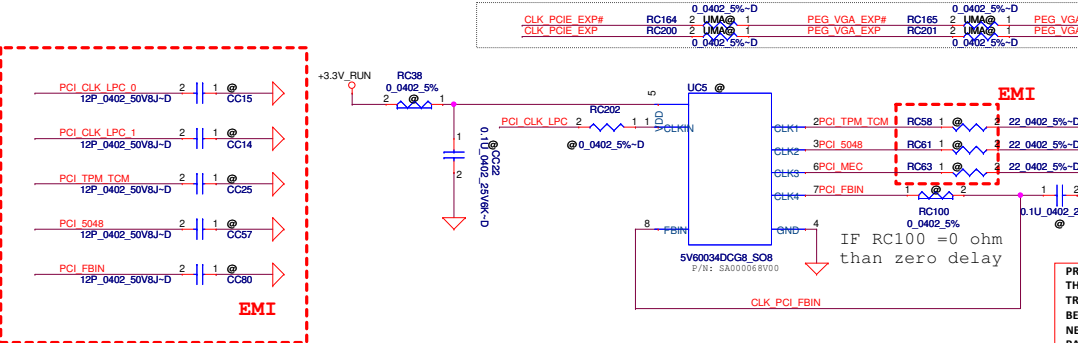
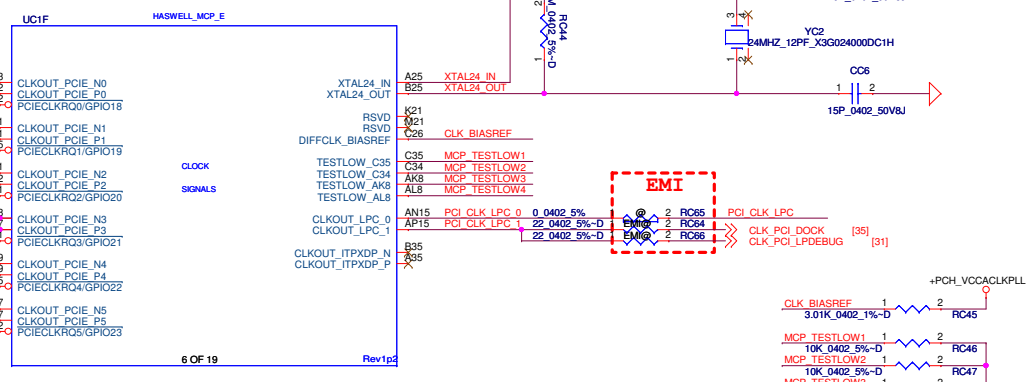
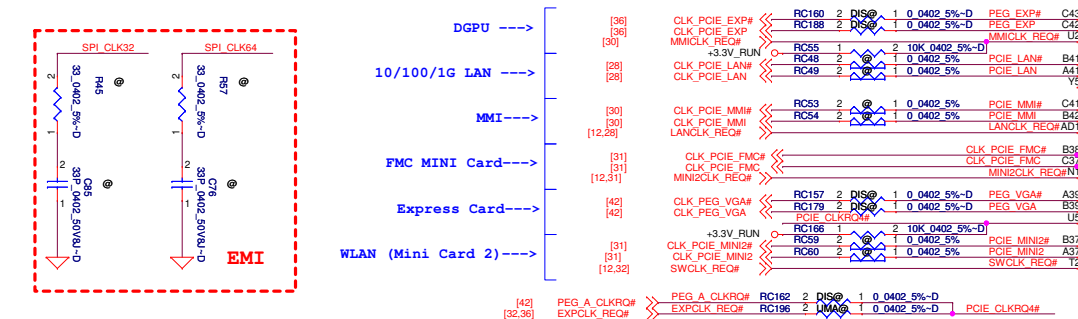
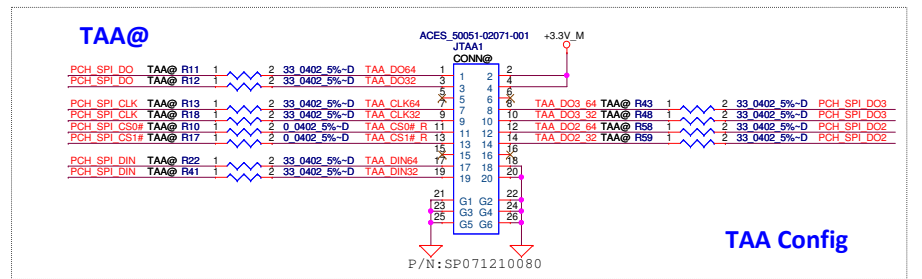
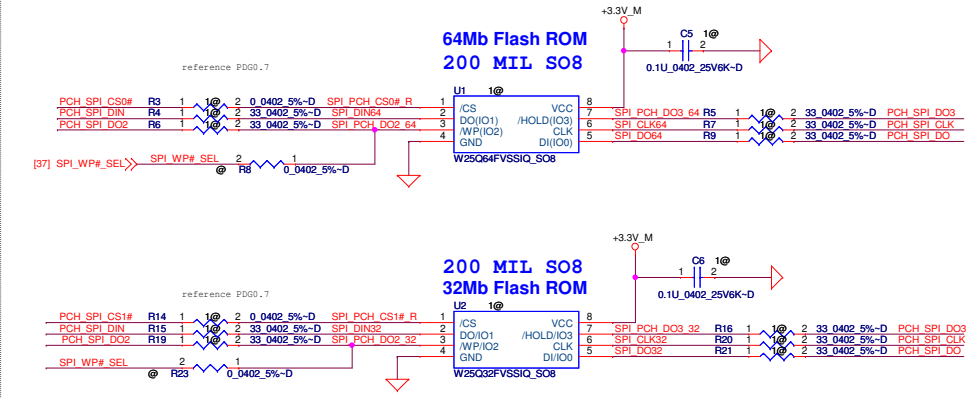


BIOS ROM (4MB + 8MB) Part Number:

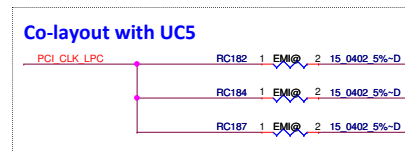
8MB	Micron N25Q064A	MXIC MX25L6475E
P/N	SA000069G00	SA00006CG00
4MB	Micron N25Q032A	MXIC MX25L3275E
P/N	SA00005KR00	SA00006DI00

BIOS ROM (4MB + 8MB) Selection:

- 1@ 8MB: Windbond W25Q64FVSSIQ, Micron N25Q064A, MXIC MX25L6475E, Atmel AT25DQ641A
 4MB: Windbond W25Q32FVSSIQ, Micron N25Q032A, MXIC MX25L3275E, Atmel AT25DQ321



RC164, RC200 co-layout with RC160, RC188
 RC165, RC201 co-layout with RC157, RC179

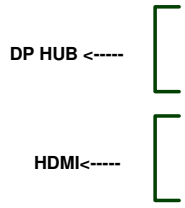


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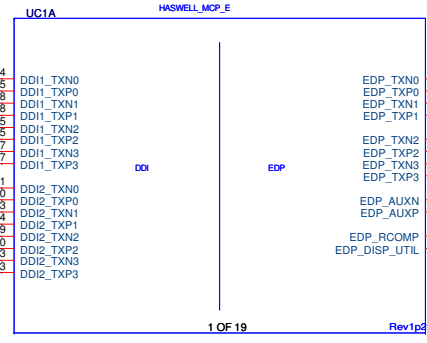
File	MCP(2/12)CLK,SMB,SPI,LPC,CL		
Size	Document Number	LA-A101P	Rev 1.0
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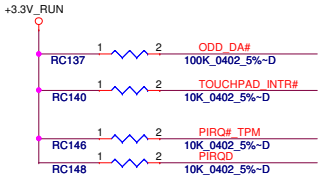
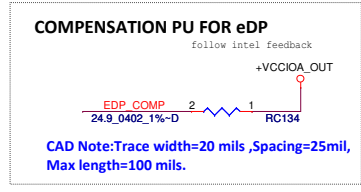


Intel check list has updated correctly

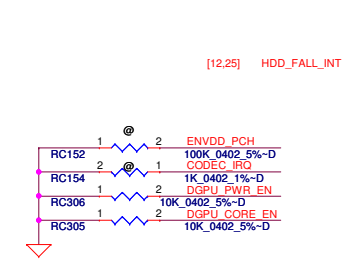
[21]	DDI1_LANE_N0	<<	DDI1_LANE_P0	>>	C54	DDI1_TXN0	<<	DDI1_TXN0	>>	C45	EDP_CPU_LANE_N0	<<	EDP_CPU_LANE_P0	>>	[20]
[21]	DDI1_LANE_P0	<<	DDI1_LANE_N1	>>	C55	DDI1_TXP0	<<	DDI1_TXP0	>>	B46	EDP_CPU_LANE_P0	<<	EDP_CPU_LANE_N0	>>	[20]
[21]	DDI1_LANE_N1	<<	DDI1_LANE_P1	>>	C58	DDI1_TXN1	<<	DDI1_TXN1	>>	A47	EDP_CPU_LANE_N1	<<	EDP_CPU_LANE_P0	>>	[20]
[21]	DDI1_LANE_P1	<<	DDI1_LANE_N2	>>	B55	DDI1_TXP1	<<	DDI1_TXP1	>>	B47	EDP_CPU_LANE_P1	<<	EDP_CPU_LANE_N1	>>	[20]
[21]	DDI1_LANE_N2	<<	DDI1_LANE_P2	>>	A55	DDI1_TXN2	<<	DDI1_TXN2	>>	C47	EDP_CPU_LANE_N2	<<	EDP_CPU_LANE_P1	>>	[20]
[21]	DDI1_LANE_P2	<<	DDI1_LANE_N3	>>	A57	DDI1_TXP2	<<	DDI1_TXP2	>>	C46	EDP_CPU_LANE_P2	<<	EDP_CPU_LANE_N1	>>	[20]
[21]	DDI1_LANE_N3	<<	DDI1_LANE_P3	>>	B57	DDI1_TXN3	<<	DDI1_TXN3	>>	A49	EDP_CPU_LANE_N3	<<	EDP_CPU_LANE_P1	>>	[20]
[21]	DDI1_LANE_P3	<<	TMDS_N2	>>	C51	DDI1_TXP3	<<	DDI1_TXP3	>>	B49	EDP_CPU_LANE_P3	<<	EDP_CPU_LANE_N2	>>	[20]
[23]	TMDS_N2	<<	TMDS_P2	>>	C50	DDI2_TXN0	<<	DDI2_TXN0	>>	A45	EDP_CPU_AUX#	<<	EDP_CPU_AUX#	>>	[20]
[23]	TMDS_P2	<<	TMDS_N1	>>	C53	DDI2_TXP0	<<	DDI2_TXP0	>>	B45	EDP_CPU_AUX	<<	EDP_CPU_AUX	>>	[20]
[23]	TMDS_N1	<<	TMDS_P1	>>	B54	DDI2_TXN1	<<	DDI2_TXN1	>>	D20	EDP_COMP	<<	EDP_COMP	>>	
[23]	TMDS_P1	<<	TMDS_N0	>>	C49	DDI2_TXP1	<<	DDI2_TXP1	>>	A43	EDP_DISP_UTIL	<<	EDP_DISP_UTIL	>>	
[23]	TMDS_N0	<<	TMDS_P0	>>	B50	DDI2_TXN2	<<	DDI2_TXN2	>>			<<		>>	
[23]	TMDS_P0	<<	TMDS_P0	>>	A53	DDI2_TXP2	<<	DDI2_TXP2	>>			<<		>>	
[23]	TMDS_CLK#	<<	TMDS_CLK#	>>	B53	DDI2_TXN3	<<	DDI2_TXN3	>>			<<		>>	
[23]	TMDS_CLK	<<	TMDS_CLK	>>	B53	DDI2_TXP3	<<	DDI2_TXP3	>>			<<		>>	



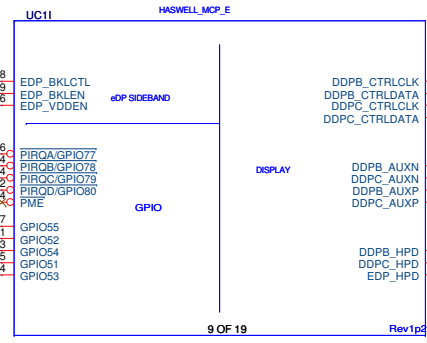
C45	EDP_CPU_LANE_N0	<<	EDP_CPU_LANE_P0	>>	[20]
B46	EDP_CPU_LANE_P0	<<	EDP_CPU_LANE_N0	>>	[20]
A47	EDP_CPU_LANE_N1	<<	EDP_CPU_LANE_P0	>>	[20]
B47	EDP_CPU_LANE_P1	<<	EDP_CPU_LANE_N1	>>	[20]
C47	EDP_CPU_LANE_N2	<<	EDP_CPU_LANE_P1	>>	[20]
C46	EDP_CPU_LANE_P2	<<	EDP_CPU_LANE_N1	>>	[20]
A49	EDP_CPU_LANE_N3	<<	EDP_CPU_LANE_P1	>>	[20]
B49	EDP_CPU_LANE_P3	<<	EDP_CPU_LANE_N2	>>	[20]
A45	EDP_CPU_AUX#	<<	EDP_CPU_AUX#	>>	[20]
B45	EDP_CPU_AUX	<<	EDP_CPU_AUX	>>	[20]
D20	EDP_COMP	<<	EDP_COMP	>>	
A43	EDP_DISP_UTIL	<<	EDP_DISP_UTIL	>>	



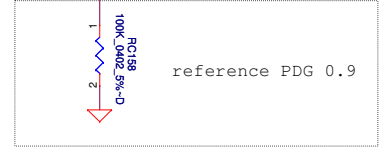
reference 0.55 design chane log WW23_2



[20]	EDP_BIA_PWM	<<	EDP_BIA_PWM	>>	B8	EDP_BKLCCTL	<<	DDPB_CTRLCLK	>>	B9	CPU_DPB_CTRLCLK	<<	DDPB_CTRLCLK	>>	
[20]	PANEL_BKLEN	<<	PANEL_BKLEN	>>	A9	EDP_BKLEN	<<	DDPB_CTRLDATA	>>	C9	CPU_DPB_CTRLDAT	<<	DDPB_CTRLDATA	>>	
[20,37]	ENVDD_PCH	<<	ENVDD_PCH	>>	C6	EDP_VDDEN	<<	DDPC_CTRLCLK	>>	D9	TMDS_DDC_SCL	<<	DDPC_CTRLDATA	>>	[23]
[26]	ODD_DA#	<<	ODD_DA#	>>	U6	PIRQA/GPIO77	<<	DDPB_AUXN	>>	C5	CPU_DPB_AUX#	<<	DDPB_AUXN	>>	[21]
[12,37,60,62]	0_0402_5%-D	<<	2 R73 PIRQF_TPM	>>	N4	PIROB/GPIO78	<<	DDPC_AUXN	>>	B6	CPU_DPC_AUX#	<<	DDPC_AUXN	>>	[21]
[12,25]	HDD_FALL_INT	<<	2 R75 PIRQD	>>	N2	PIROC/GPIO79	<<	DDPB_AUXP	>>	B5	CPU_DPB_AUX	<<	DDPB_AUXP	>>	[21]
[12,25]	HDD_FALL_INT	<<	0_0402_5%-D	>>	AD4	PIROD/GPIO80	<<	DDPC_AUXP	>>	A6	CPU_DPC_AUX	<<	DDPC_AUXP	>>	[21]
[12]	TOUCH_RST_N_GYRO_INT1	<<	TOUCHPAD_INTR#	>>	U7	GPI055	<<	DDPB_HPD	>>	C8	DPB_HPD	<<	DDPB_HPD	>>	[21]
[49]	DGPU_PWR_EN	<<	DGPU_PWR_EN	>>	L1	GPI052	<<	DDPC_HPD	>>	A8	TMDS_HPD	<<	DDPC_HPD	>>	[23]
[60]	DGPU_CORE_EN	<<	DGPU_CORE_EN	>>	R5	GPI054	<<	EDP_HPD	>>	D6	EDP_CPU_HPD	<<	EDP_HPD	>>	[20]
[60]	DGPU_CORE_EN	<<	CODEC_IRO	>>	L4	GPI051	<<		>>			<<		>>	
[60]	DGPU_CORE_EN	<<	CODEC_IRO	>>	L4	GPI053	<<		>>			<<		>>	

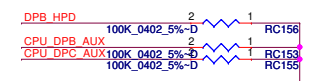
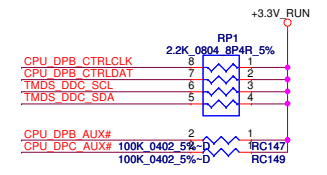


B9	CPU_DPB_CTRLCLK	<<	DDPB_CTRLCLK	>>	
C9	CPU_DPB_CTRLDAT	<<	DDPB_CTRLDATA	>>	
D9	TMDS_DDC_SCL	<<	DDPC_CTRLCLK	>>	[23]
D11	TMDS_DDC_SDA	<<	DDPC_CTRLDATA	>>	[23]
C5	CPU_DPB_AUX#	<<	CPU_DPB_AUX#	>>	[21]
B6	CPU_DPC_AUX#	<<	CPU_DPB_AUX#	>>	[21]
B5	CPU_DPB_AUX	<<	CPU_DPB_AUX	>>	[21]
A6	CPU_DPC_AUX	<<	CPU_DPB_AUX	>>	[21]
C8	DPB_HPD	<<	DPB_HPD	>>	[21]
A8	TMDS_HPD	<<	TMDS_HPD	>>	[23]
D6	EDP_CPU_HPD	<<	EDP_CPU_HPD	>>	[20]



Intel WW18 Strapping option

Intel WW18 Strapping option



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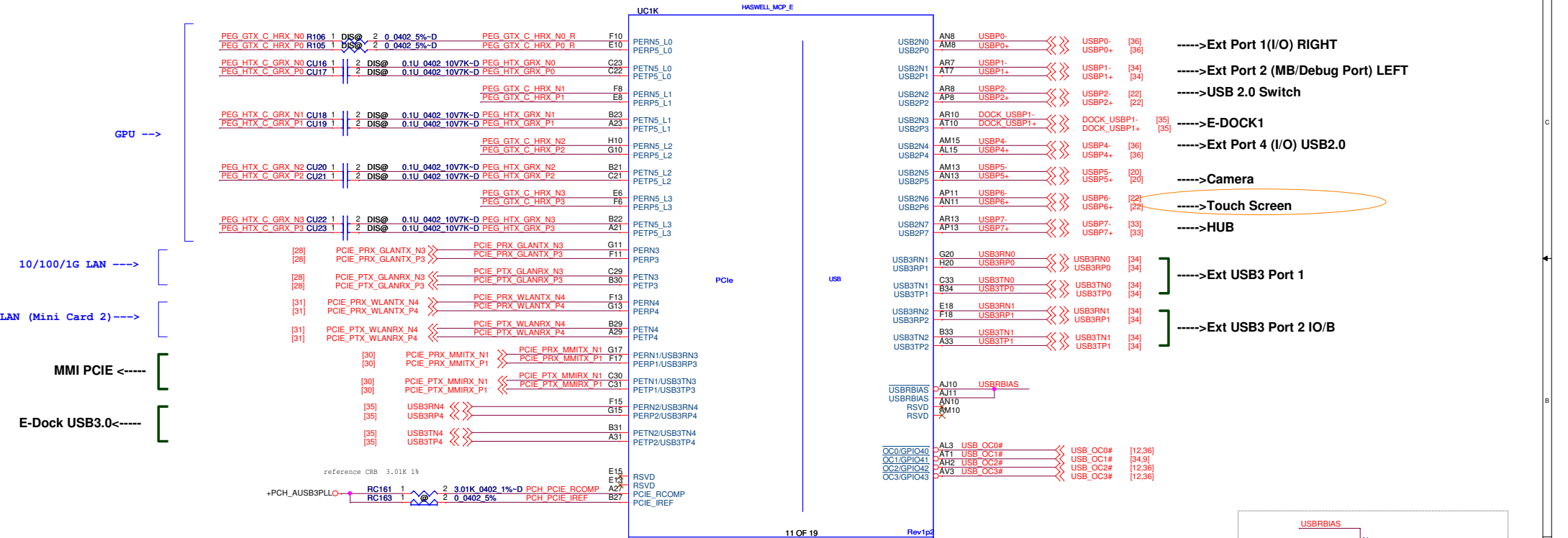


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Title			
MCP(5/12) DDI,EDP,GPIO			
Size	Document Number	Rev	1.0
Date:	Monday, September 23, 2013	Sheet	10 of 65

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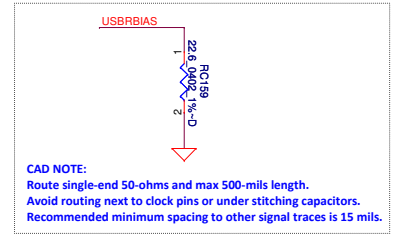
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 [42] PEG_GTX_C_HRX_P0_0.3] >> PEG_GTX_C_HRX_P0_0.3] <<
 [42] PEG_HTX_C_GRX_N0_0.3] >> PEG_HTX_C_GRX_N0_0.3] <<
 [42] PEG_HTX_C_GRX_P0_0.3] >> PEG_HTX_C_GRX_P0_0.3] <<

[32] PEG_GTX_C_HRX_N0_M] >> PEG_GTX_C_HRX_N0_M] << R101 1 UMA@ 2 0 0402 5%-D PEG_GTX_C_HRX_N0_R
 [32] PEG_GTX_C_HRX_P0_M] >> PEG_GTX_C_HRX_P0_M] << R100 1 UMA@ 2 0 0402 5%-D PEG_GTX_C_HRX_P0_R
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 [32] PEG_HTX_C_GRX_P0_M] >> PEG_HTX_C_GRX_P0_M] << R104 1 UMA@ 2 0 0402 5%-D PEG_HTX_C_GRX_P0



reference CRB 3.01K 1k
 +PCH_AUSB3PLLO RC161 1 2 3.01K 0402 1%-D PCH_PCIE_RCOMP E15
 RC163 1 2 0.0402 5% PCH_PCIE_IREF E16

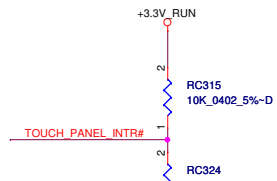
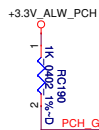
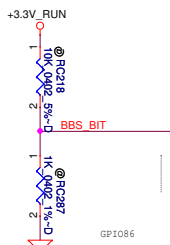
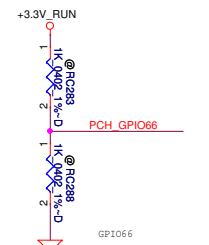
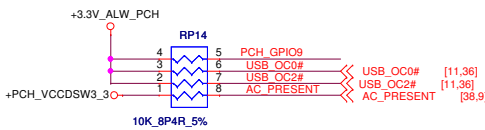
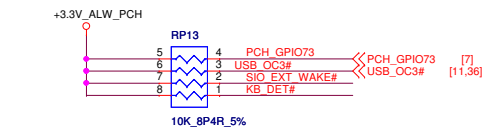
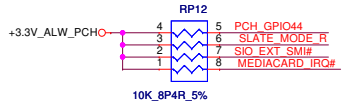
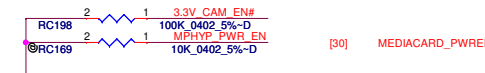
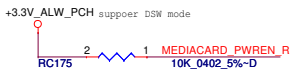
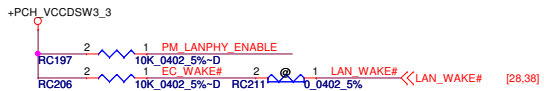
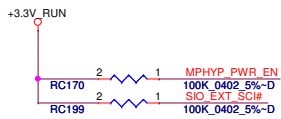
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MCP(6/12) PCIE,USB
LA-A101P
 Date: Monday, September 23, 2013 Sheet 11 of 65

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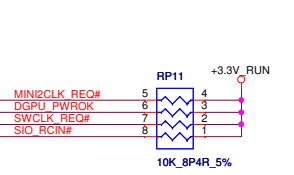
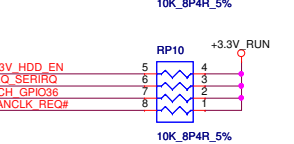
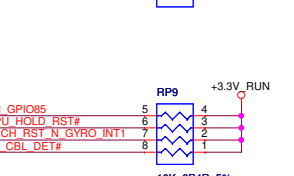
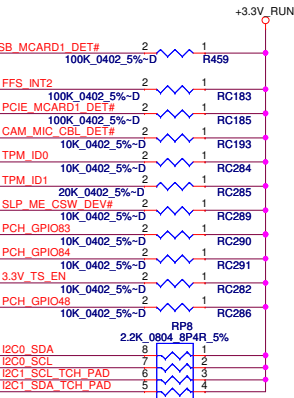
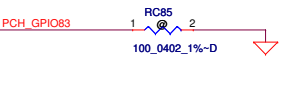
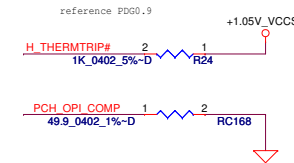
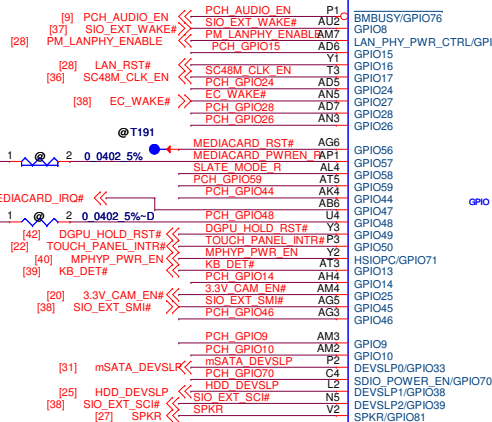
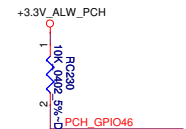


TOP-BLOCK SWAP OVERRIDE	
HIGH depop RC288 (DEFAULT)	LOW pop RC288

BOOT BIOS STRAP BIT BBS	
HIGH (DEFAULT)	LPC
LOW (DEFAULT)	SPI

TLS CONFIDENTIALITY	
HIGH	LOW (DEFAULT)

NO REBOOT STRAP	
HIGH	LOW (DEFAULT)



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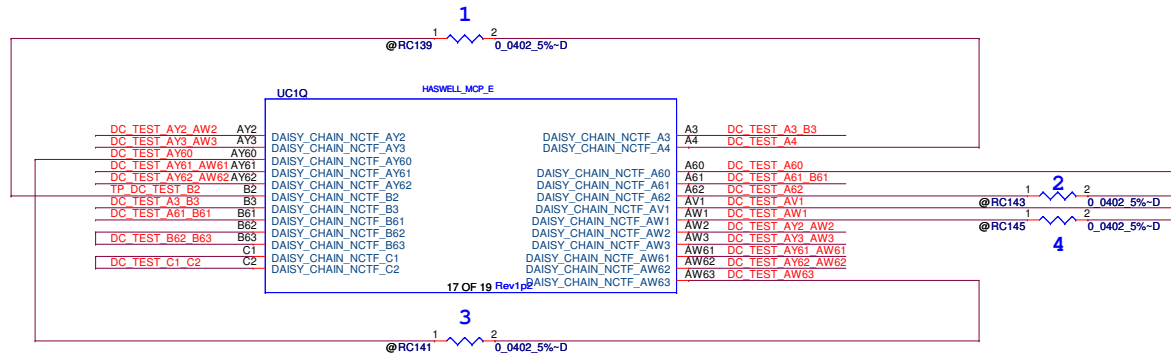
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Size: Document Number

LA-A101P

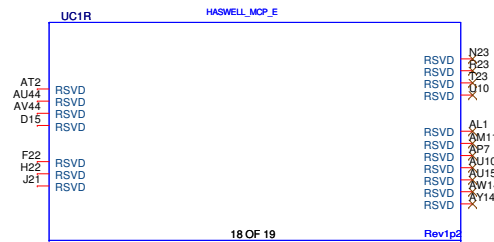
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Package Daisy Chain:

1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



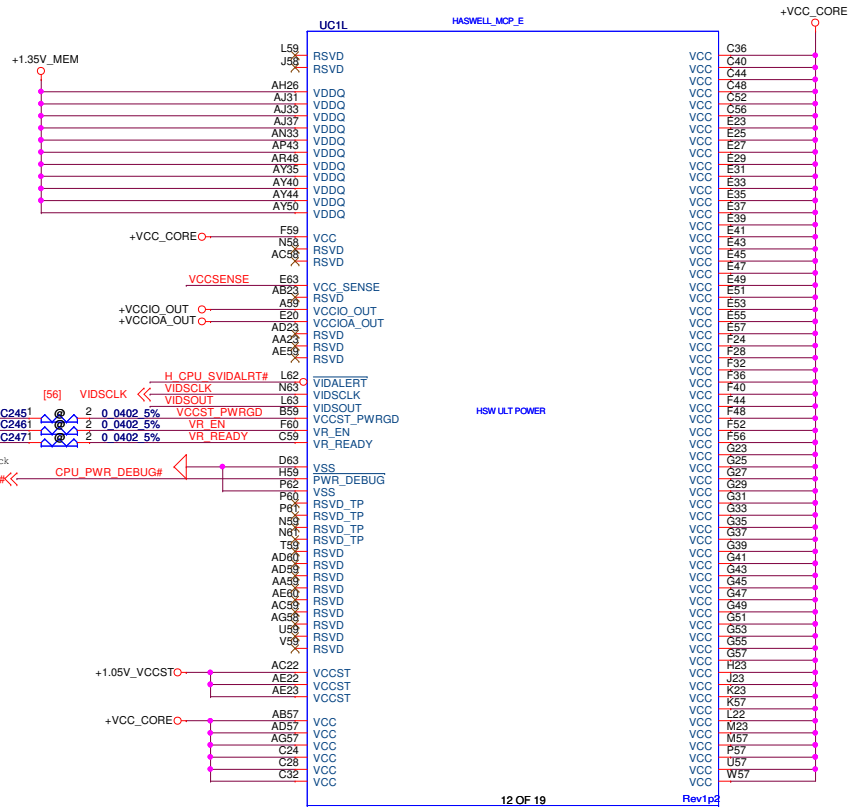
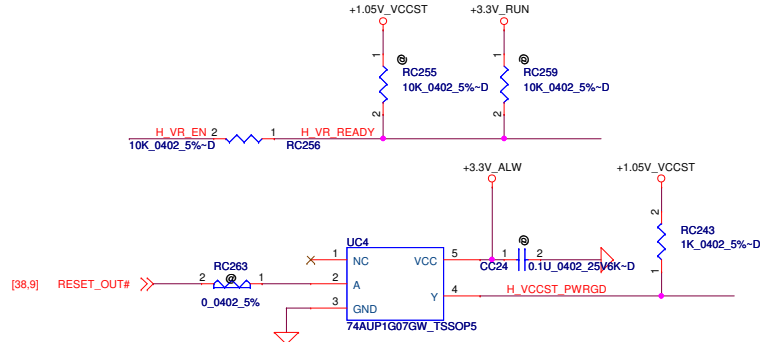
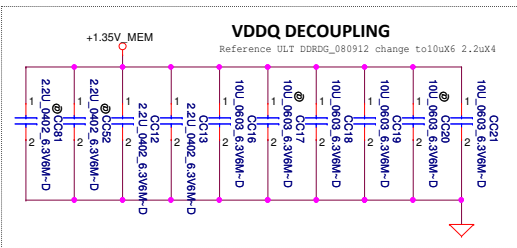
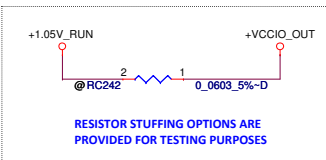
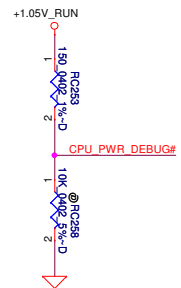
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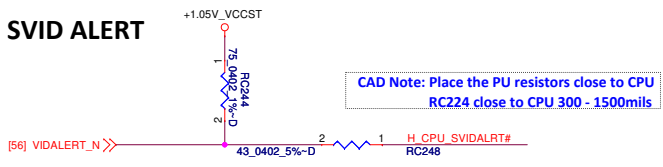
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Size	Document Number	Rev	1.0
Date: Monday, September 23, 2013		Sheet 14 of 65	



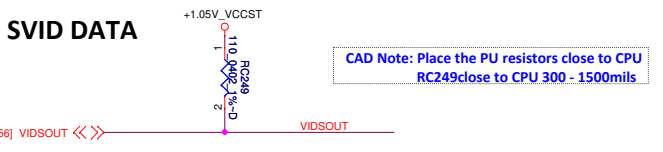
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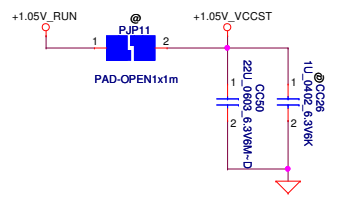
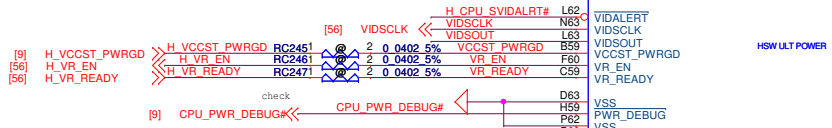
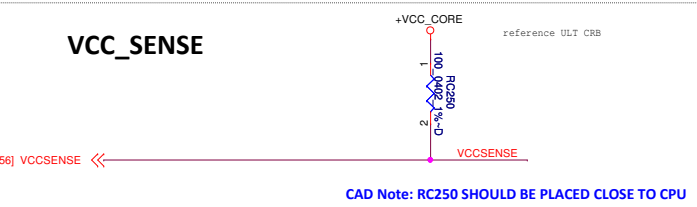
SVID ALERT



SVID DATA



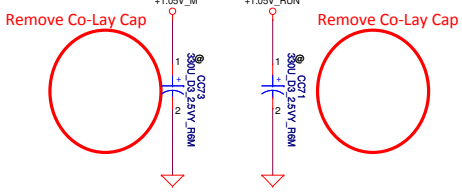
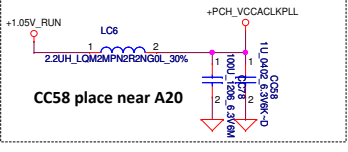
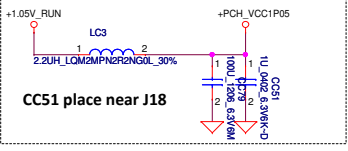
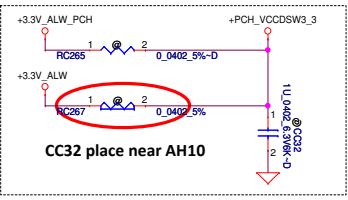
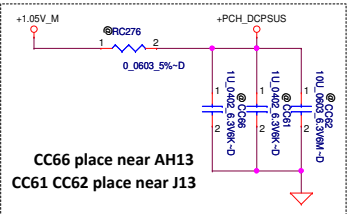
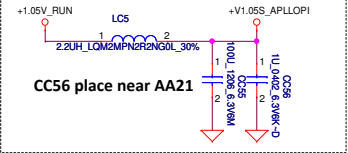
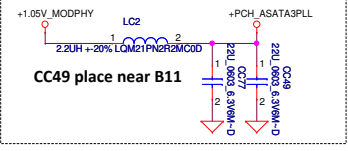
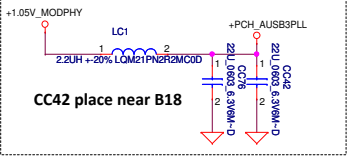
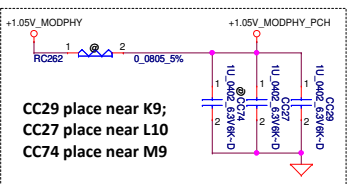
VCC_SENSE



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MCP(10/12) Power
LA-A101P
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DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86, R319, RC267	RC79, RC82, RC265
Depop	RC79, RC82, RC265	RC86, R319, RC267

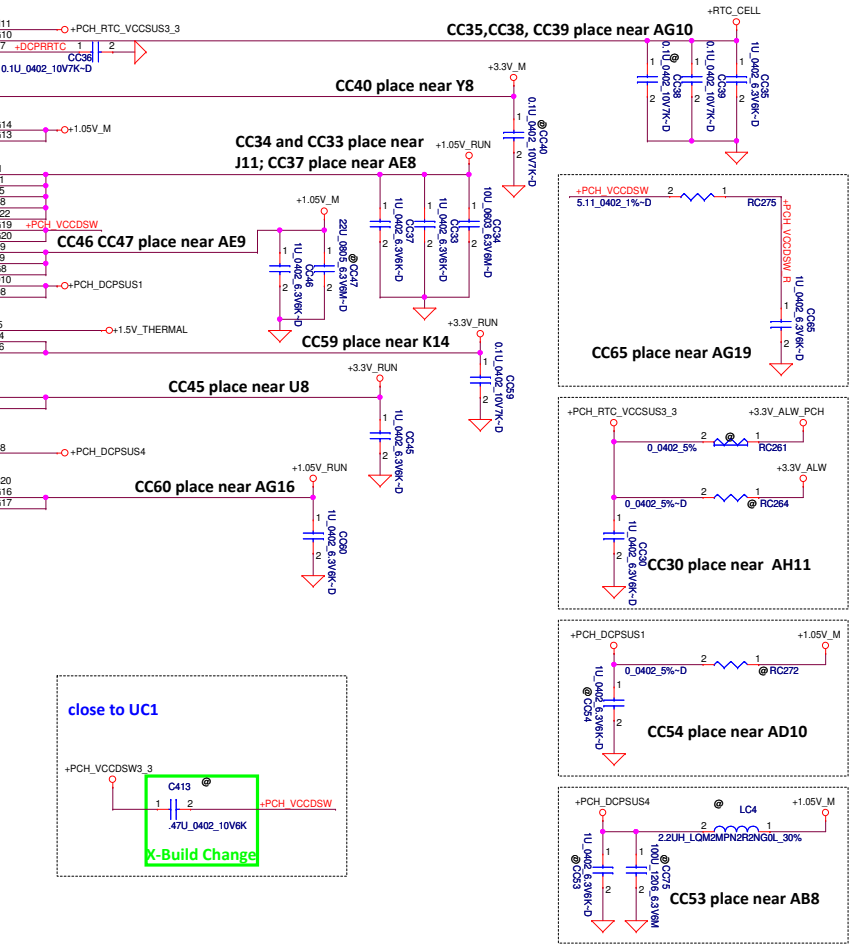
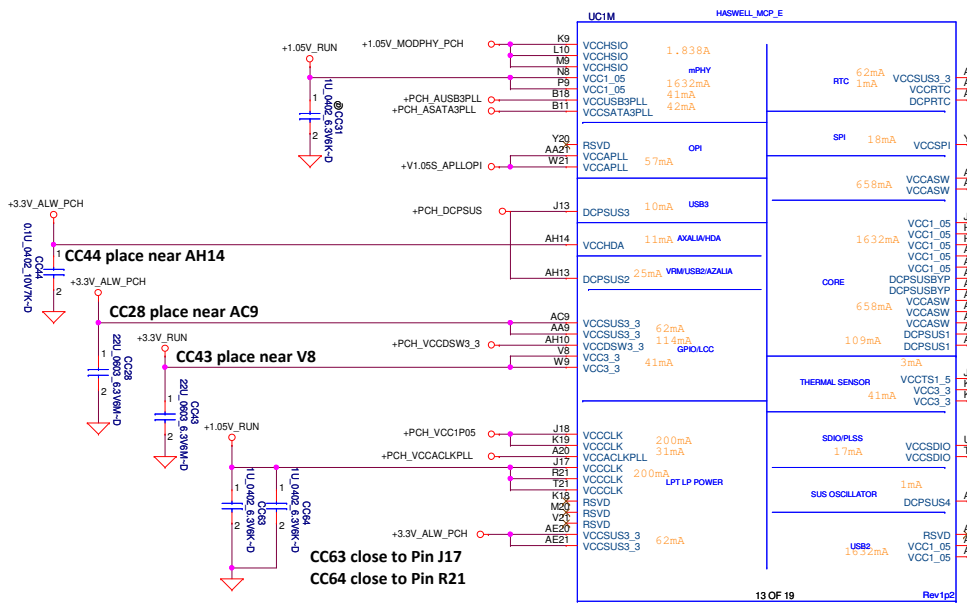
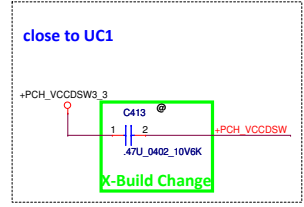
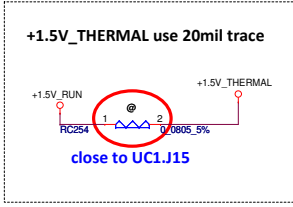


Table 6-3. Pre-Si I_{cc} max Estimates

Voltage Rail	Voltage (V)	S0 Iccmax Current (A) ¹	Sx Iccmax Current (A) ²	Deep Sx Iccmax (A) ³	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSP1	3.3	0.018	0	0	0
VCCSDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1 ⁴	1.05	0.109	0.014	0	0
DcpSus2 ⁴	1.05	0.025	0.001	0	0
DcpSus3 ⁴	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μA See notes 1, 2



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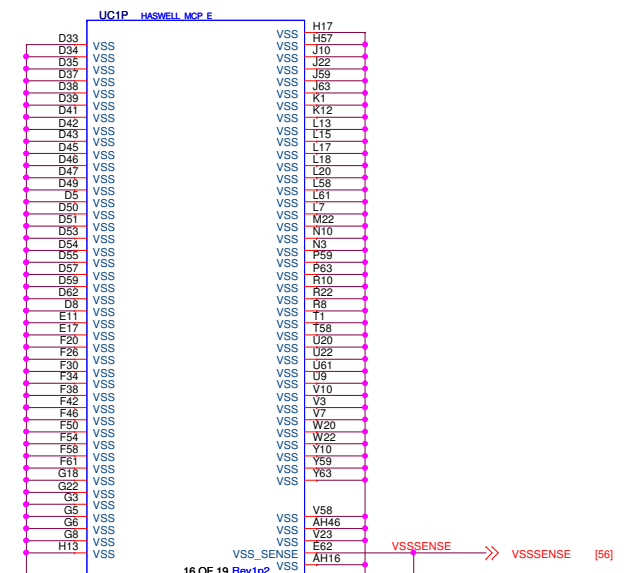
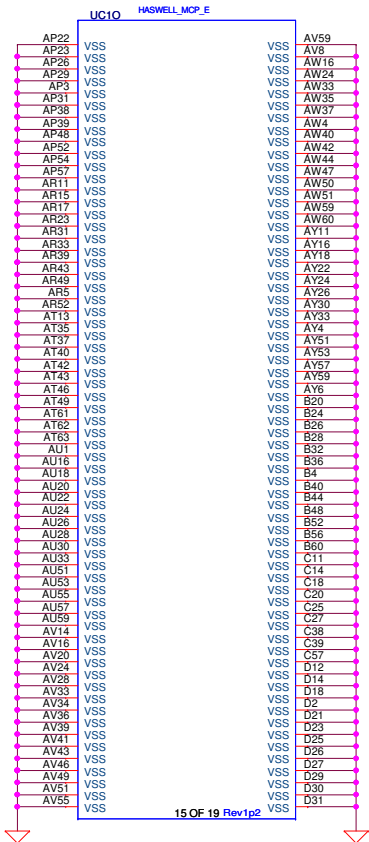
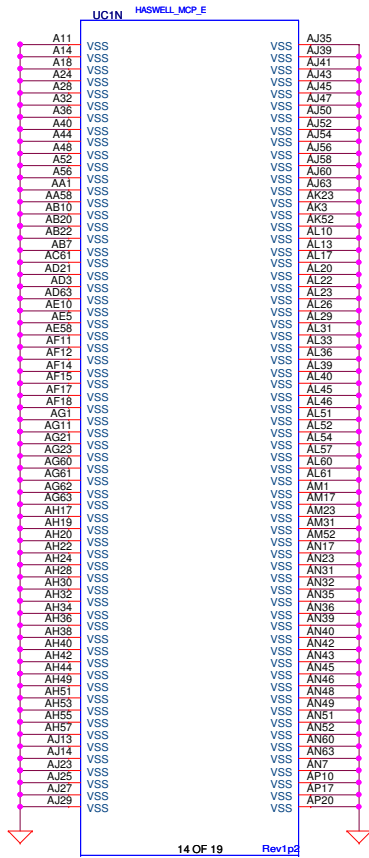
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MCP(11/12) Power

LA-A101P

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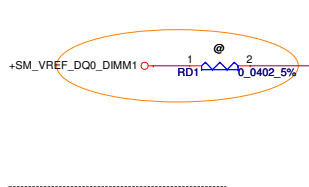
CAD Note: RC260 SHOULD BE PLACED CLOSE TO CPU

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Compal Electronics, Inc.		
Title		
MCP(12/12) VSS		
Size	Document Number	Rev
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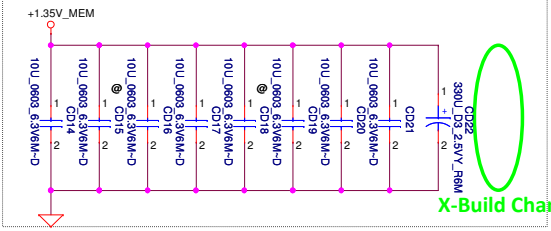
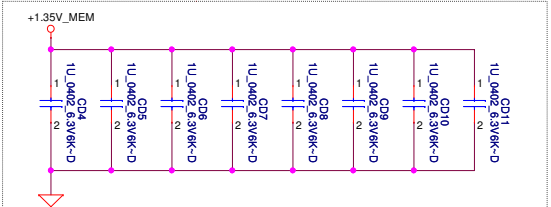


All VREF traces should have 10 mil trace width

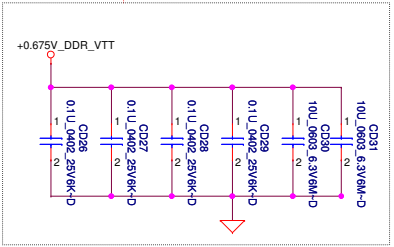
- [8] DDR_A_DQS#[0..7] <<>
- [8] DDR_A_D[0..63] <<>
- [8] DDR_A_DQS[0..7] <<>
- [8] DDR_MA[0..15] <<>

Layout Note:
Place near JDIMM1

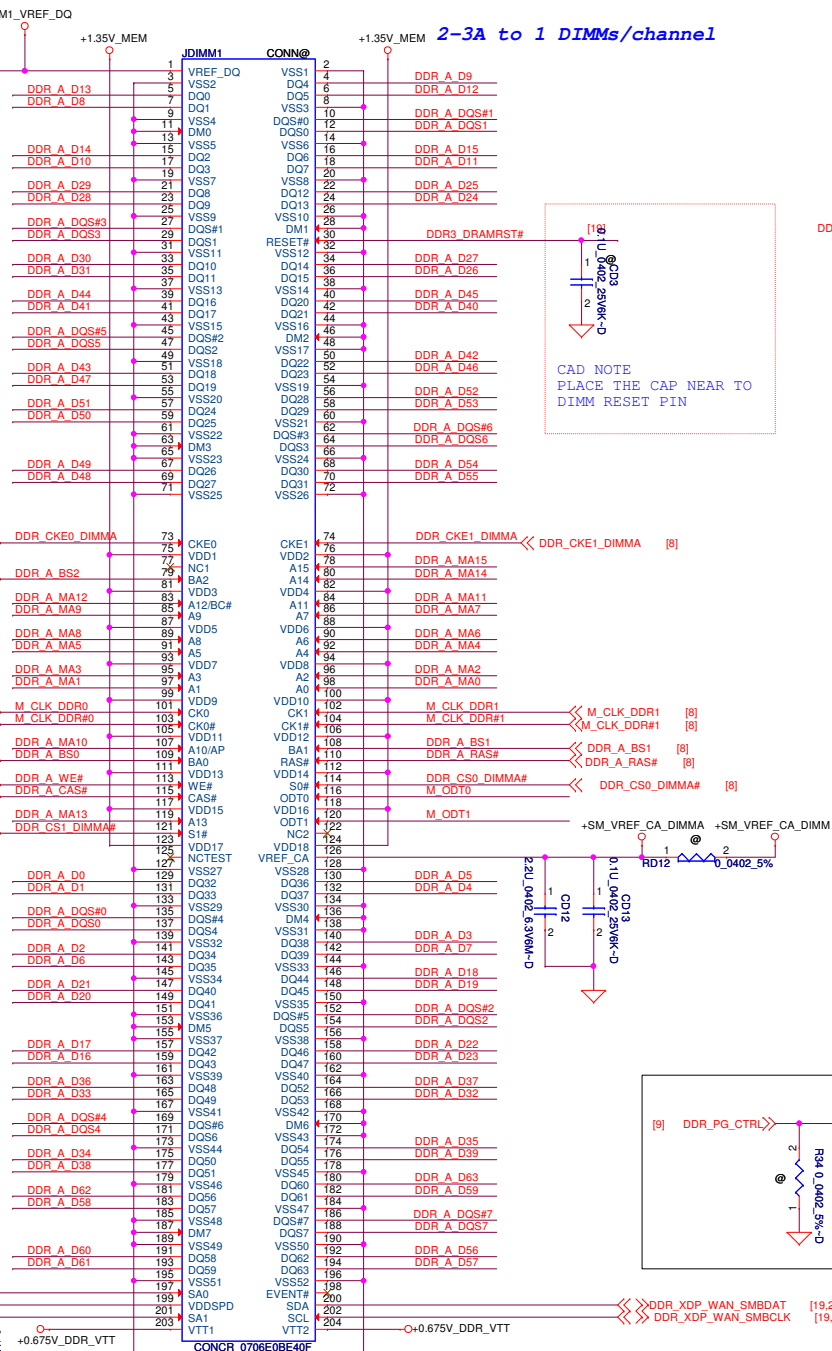
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



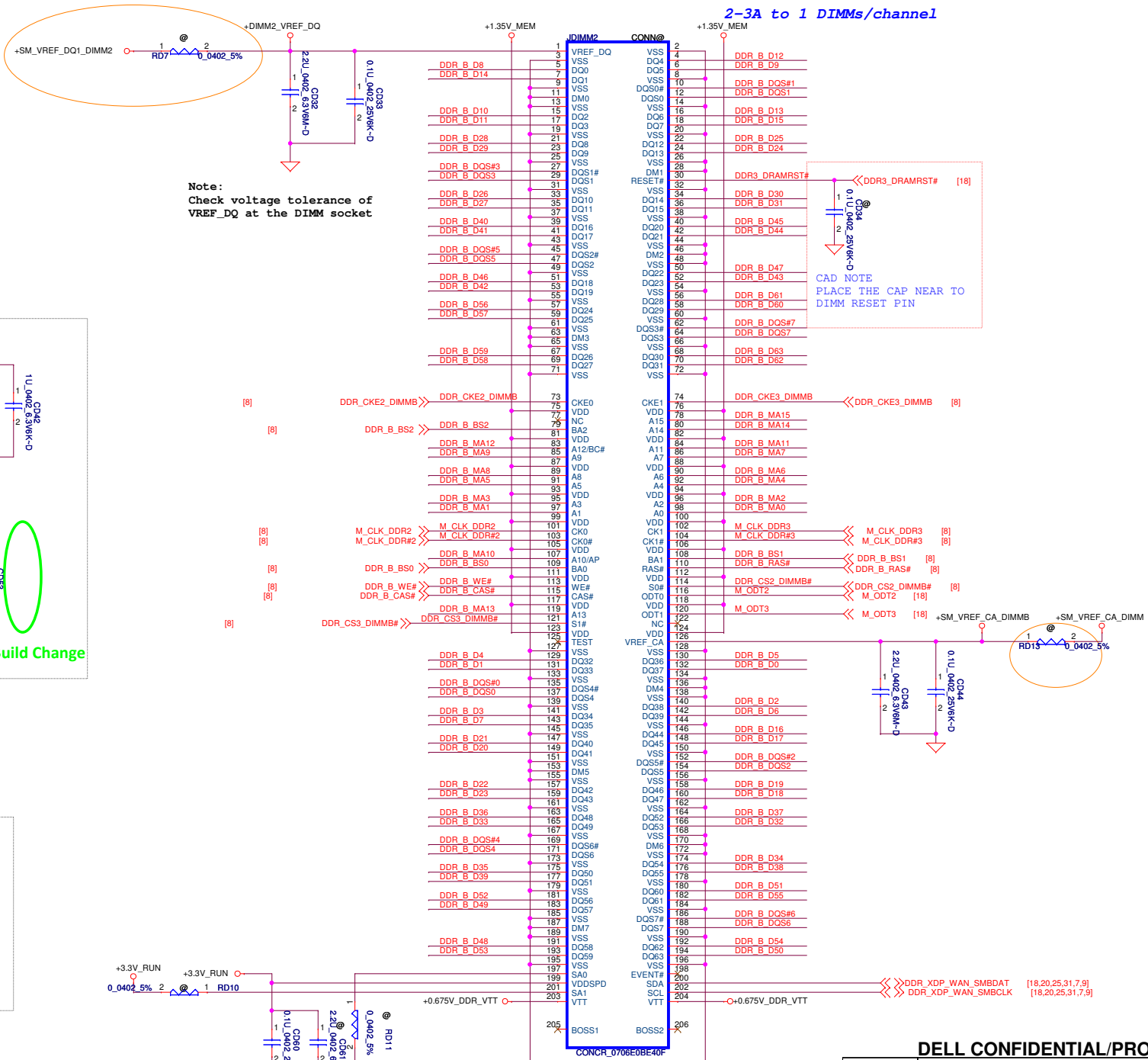
Layout Note:
Place near JDIMM1.203, 204



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- [8] DDR_A_BS2 <<> DDR_A_BS2
- [8] M_CLK_DDR0 <<> M_CLK_DDR0
- [8] M_CLK_DDR#0 <<> M_CLK_DDR#0
- [8] DDR_A_MA10 <<> DDR_A_MA10
- [8] DDR_A_BS0 <<> DDR_A_BS0
- [8] DDR_A_WE# <<> DDR_A_WE#
- [8] DDR_A_CAS# <<> DDR_A_CAS#
- [8] DDR_MA13 <<> DDR_MA13
- [8] DDR_CS1_DIMMA# <<> DDR_CS1_DIMMA#



2-3A to 1 DIMMs/channel



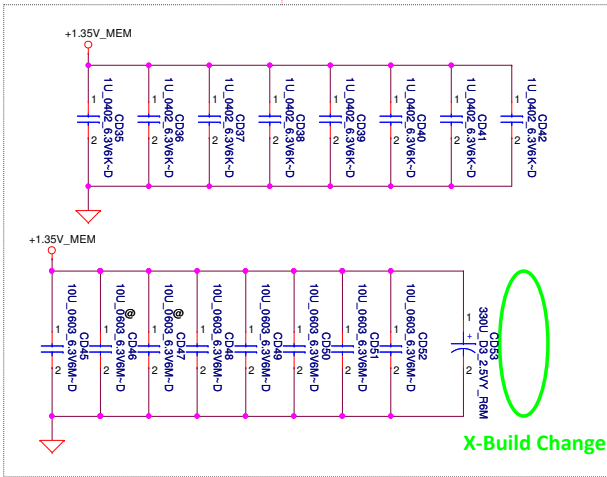
All VREF traces should have 10 mil trace width

- [8] DDR_B_DQS#(0..7) <<<>>>
- [8] DDR_B_D(0..63) <<<>>>
- [8] DDR_B_DQS(0..7) <<<>>>
- [8] DDR_B_MA(0..15) <<<>>>

Layout Note:
Place near JDIMM2

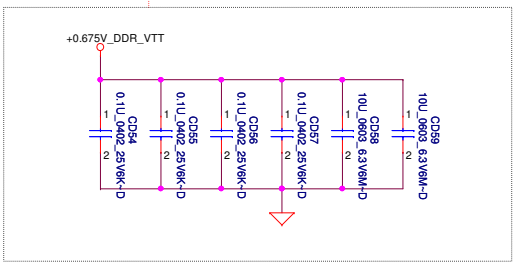
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



X-Build Change

Layout Note:
Place near JDIMM2.203,204



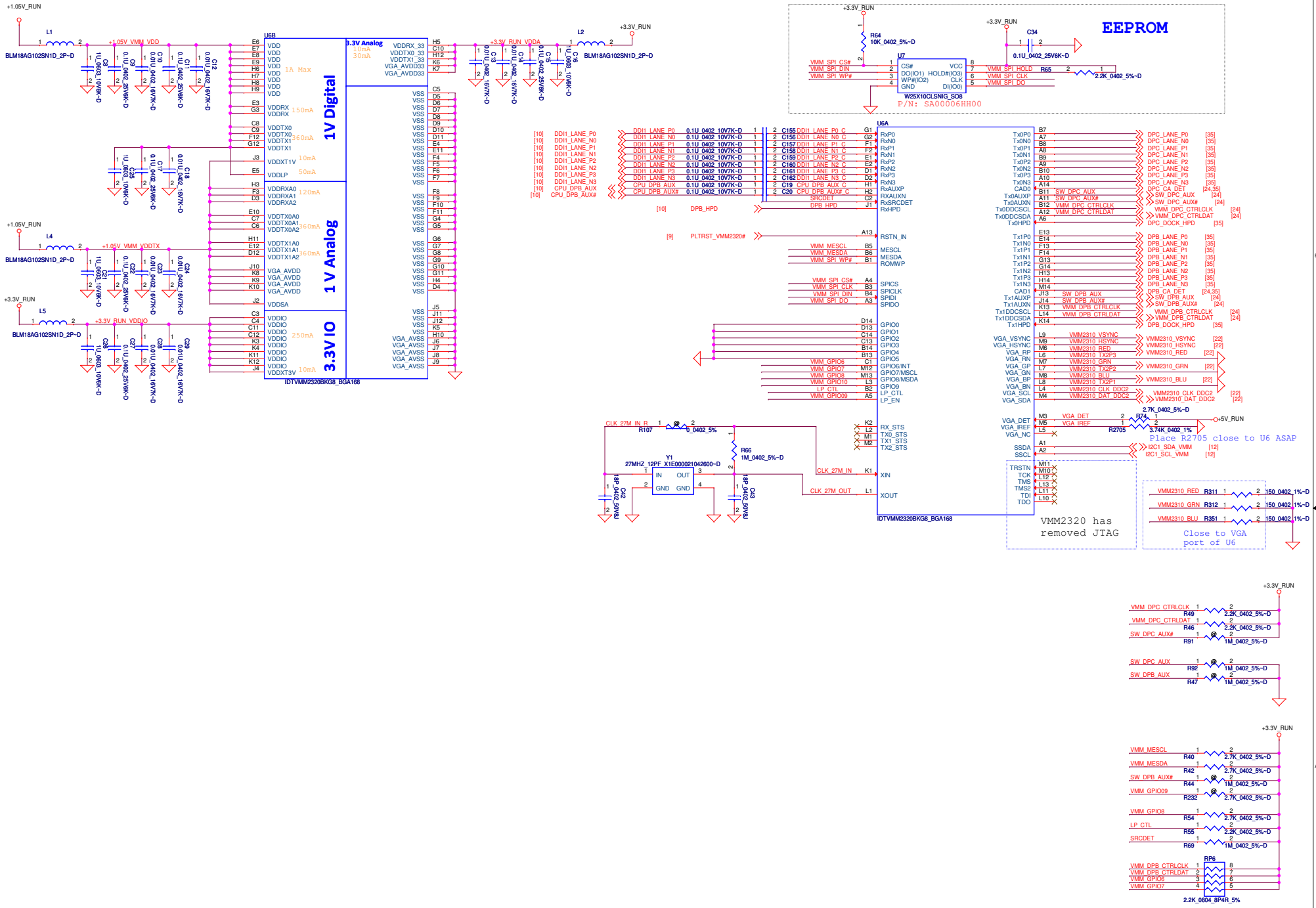
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DDRIII-SODIMM SLOT2			
LA-A101P			
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Rev 1.0



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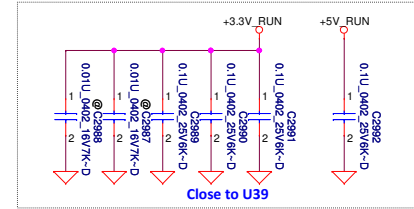
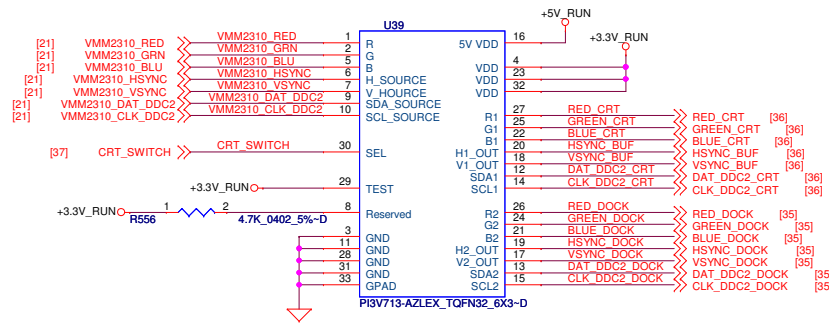
IDT VMM2320 DP and VGA SW

LA-A101P

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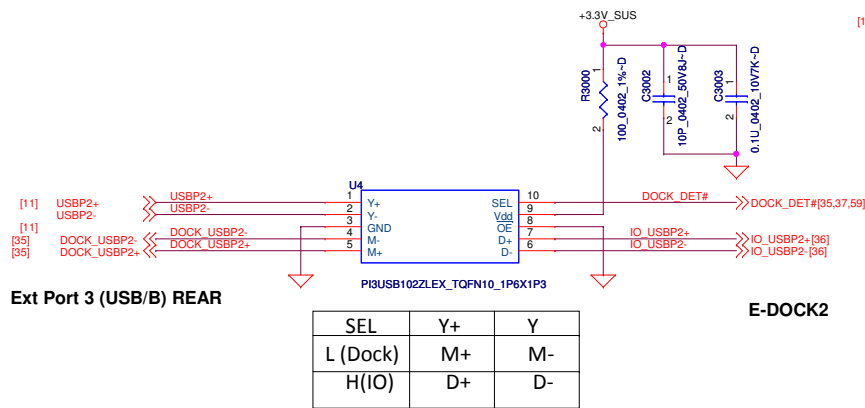
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CRT SW for MB/DOCK



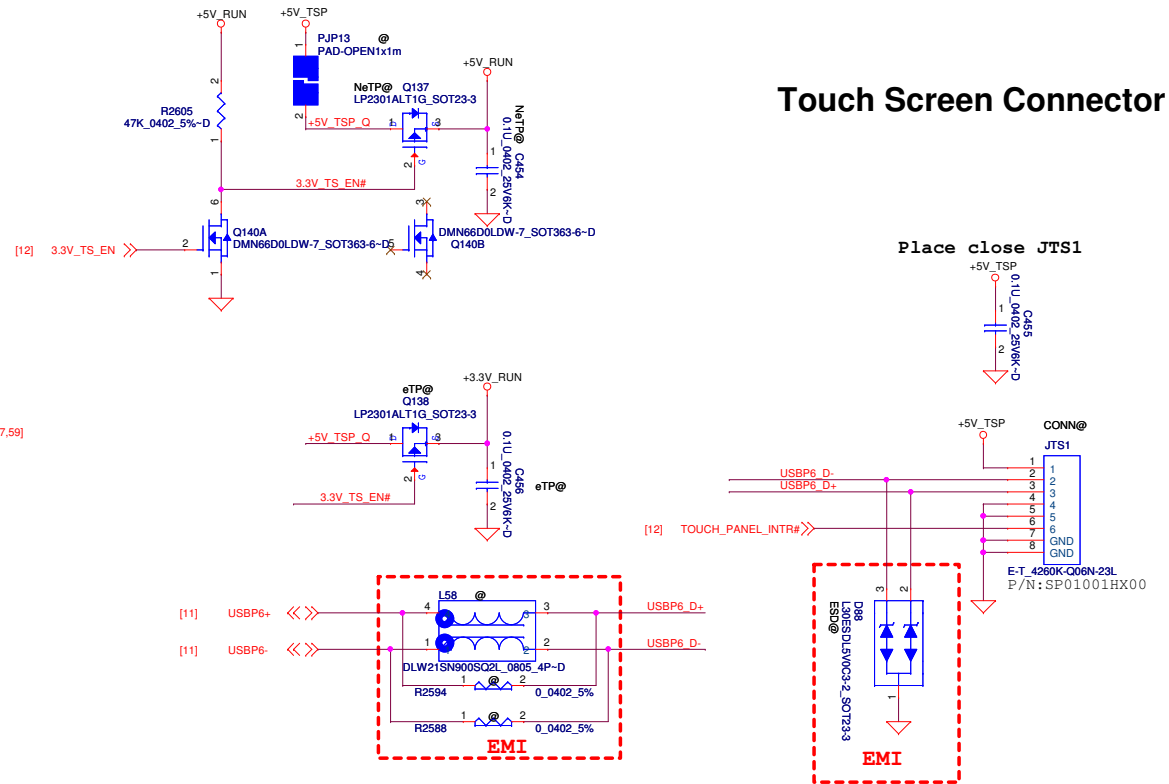
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

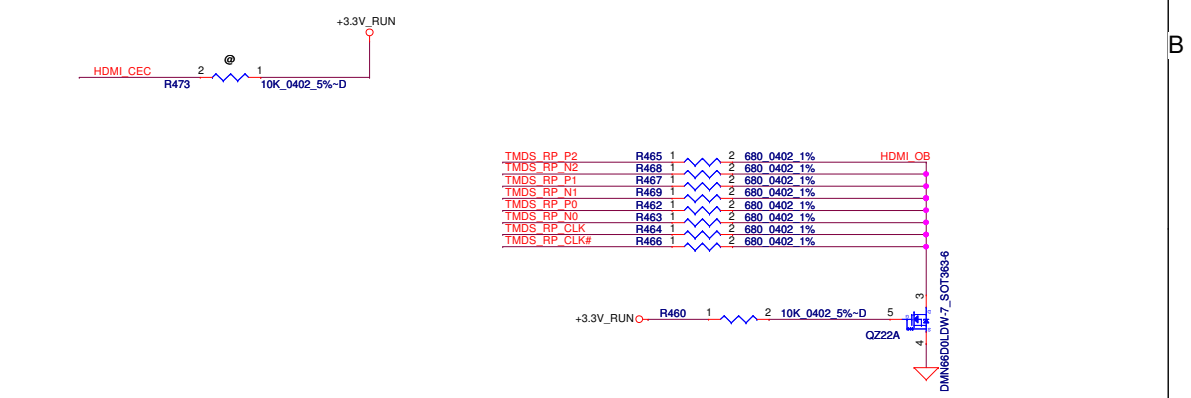
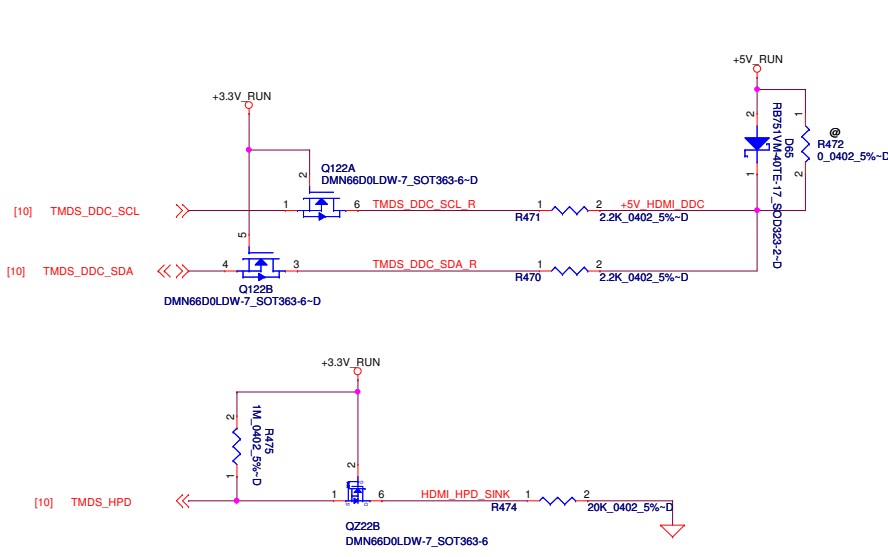
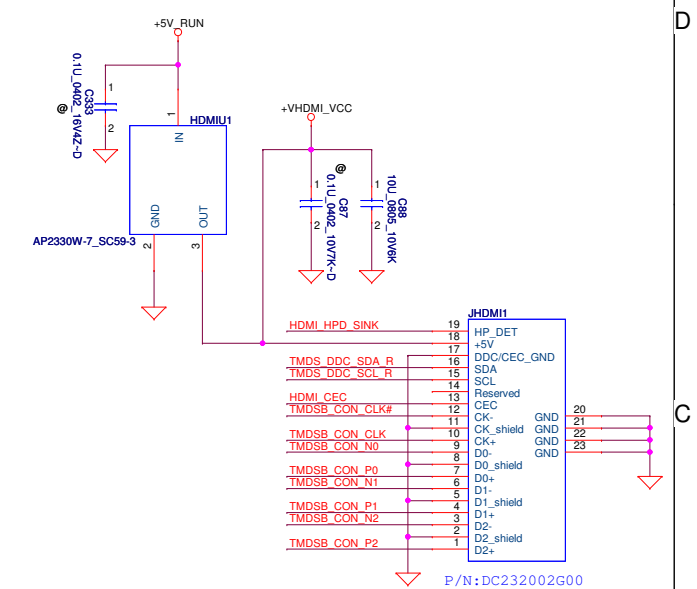
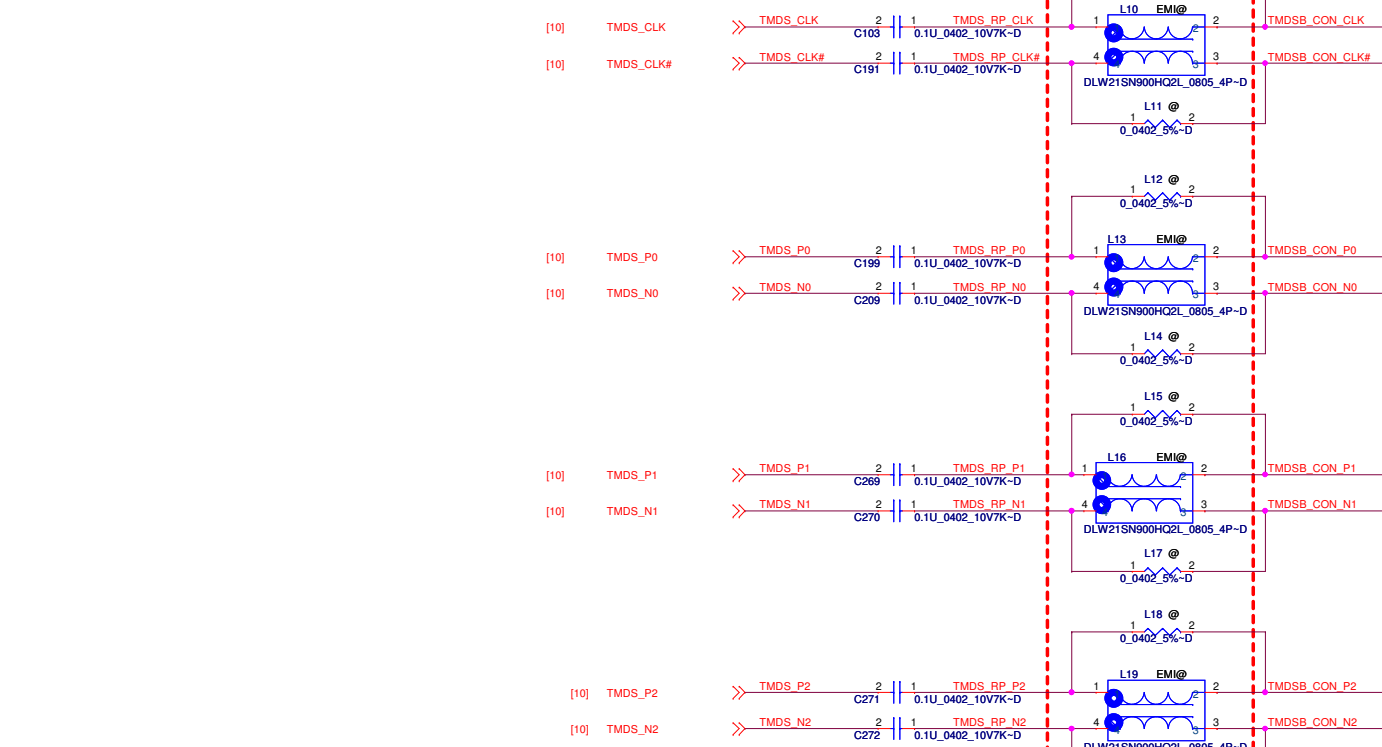
USB 2.0 Switch



SEL	Y+	Y
L (Dock)	M+	M-
H (IO)	D+	D-

Touch Screen Connector



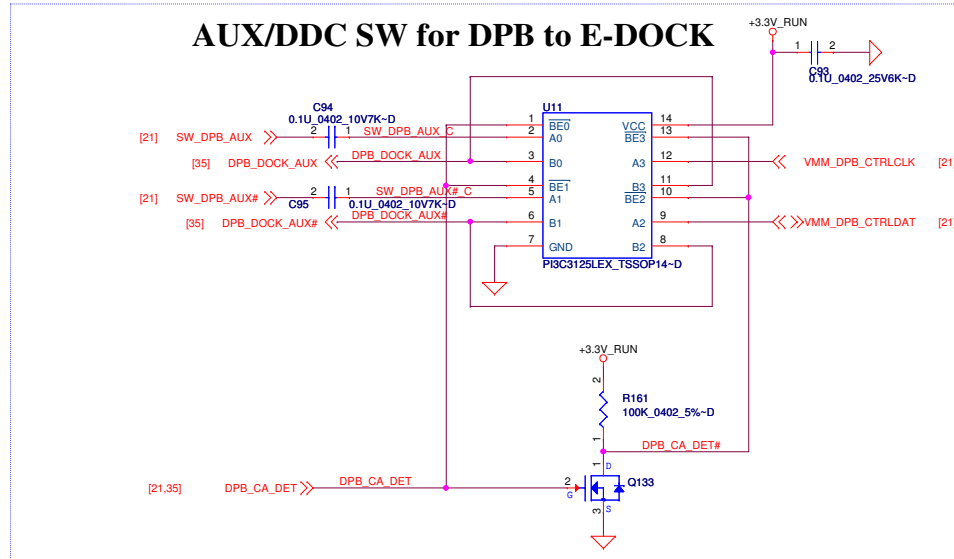


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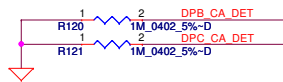
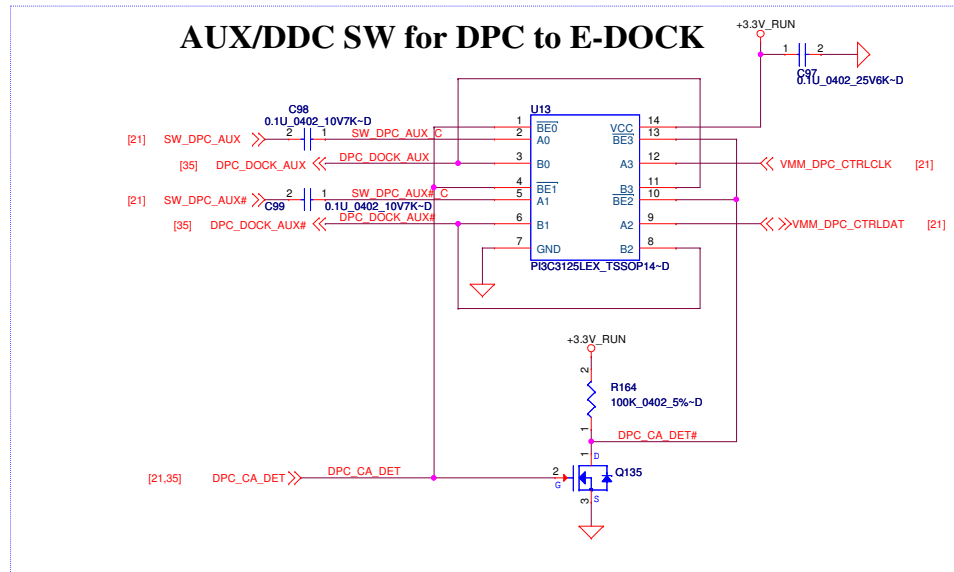
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Compal Electronics, Inc.			
HDMI Conn			
Size	Document Number	LA-A101P	
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AUX/DDC SW for DPB to E-DOCK



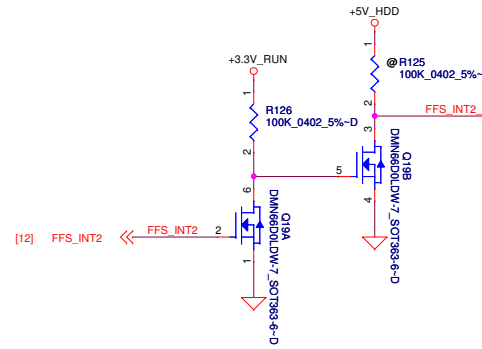
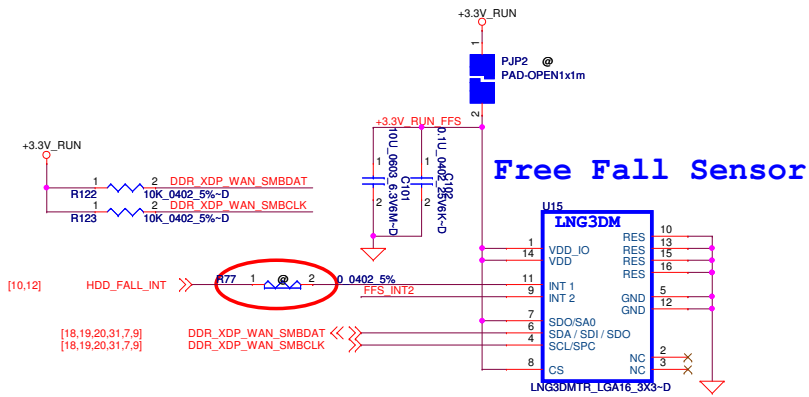
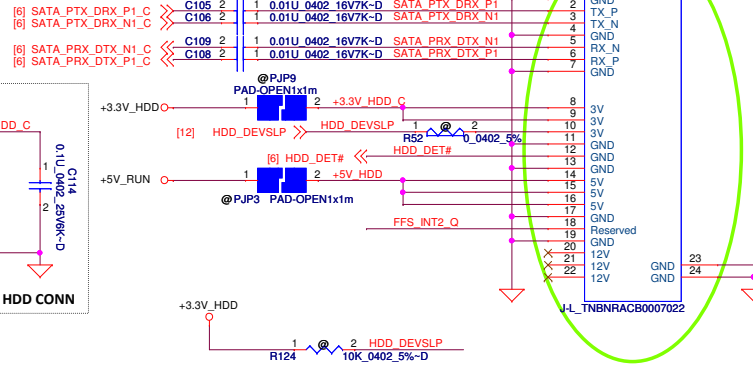
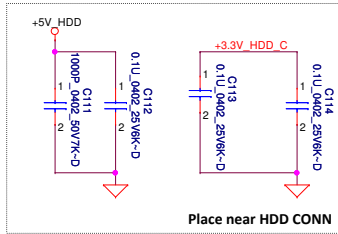
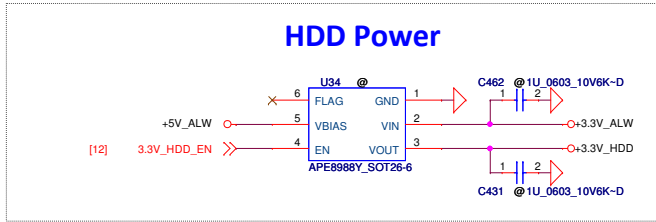
AUX/DDC SW for DPC to E-DOCK



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Title DP SW DP125			
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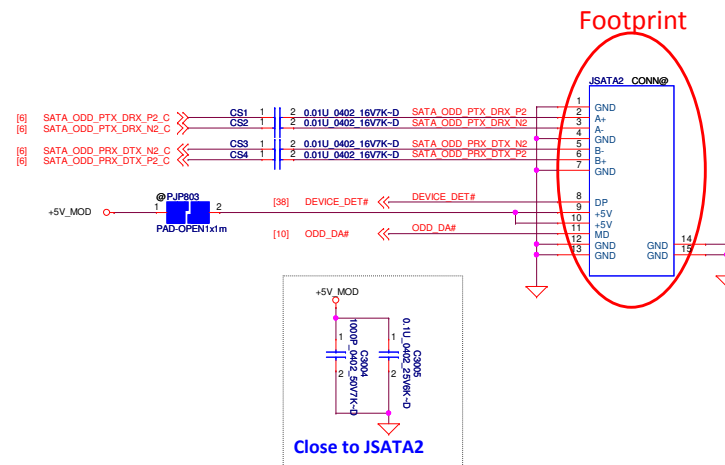
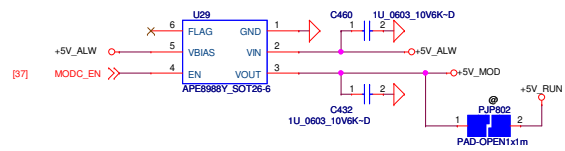


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Title			HDD CONN		
Size	Document Number				Rev
	LA-A101P				1.0
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ODD power



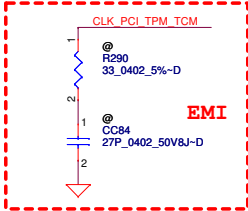
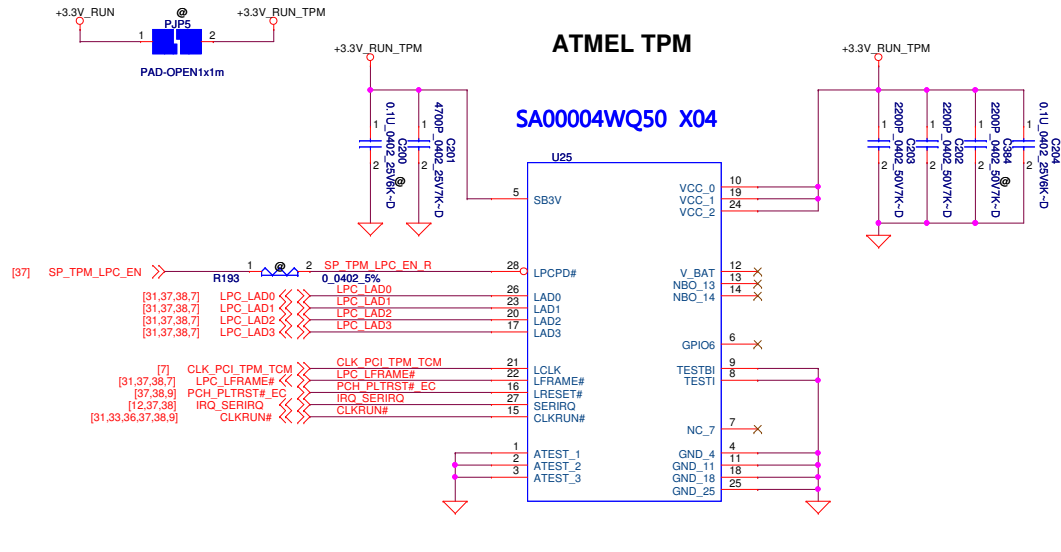
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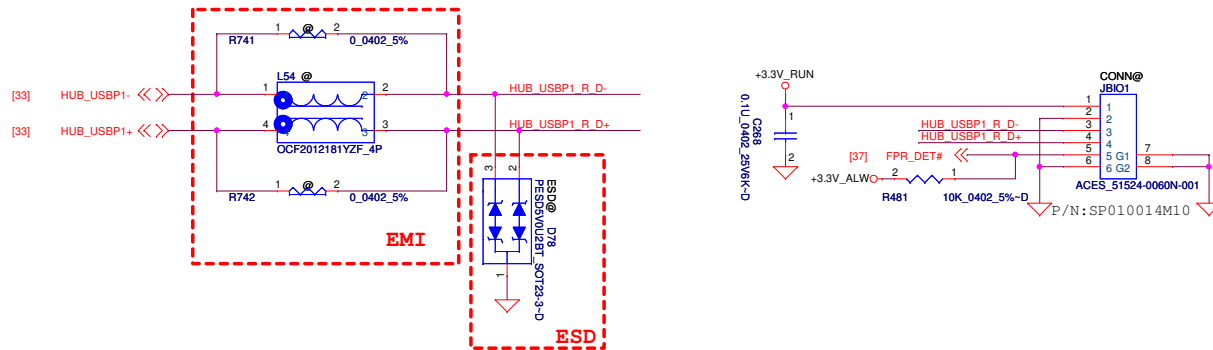


Title	ODD module	
Size	Document Number	Rev
	LA-A101P	1.0
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Finger print module



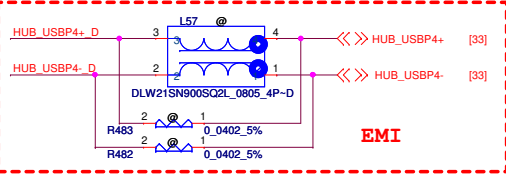
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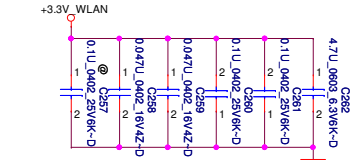
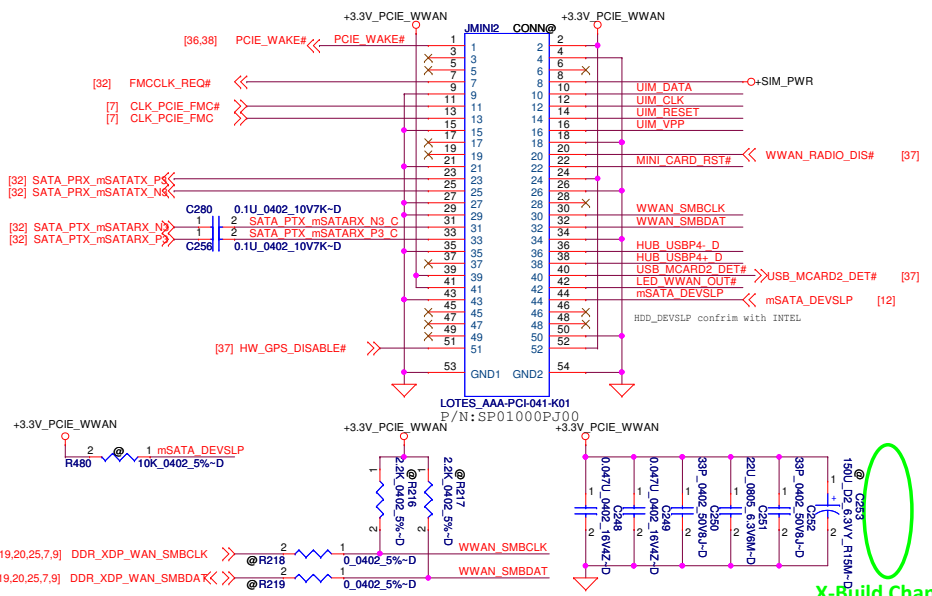
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Title			TPM/FP		
Size	Document Number		Rev		1.0
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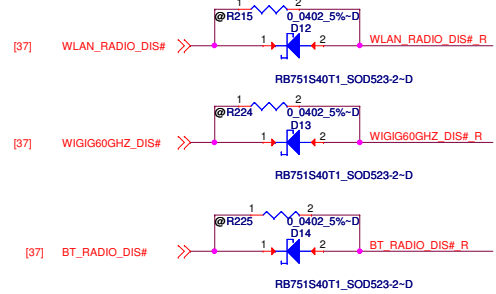
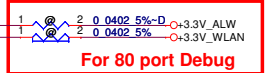
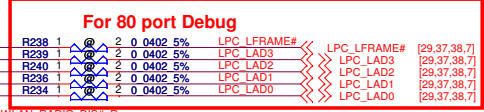
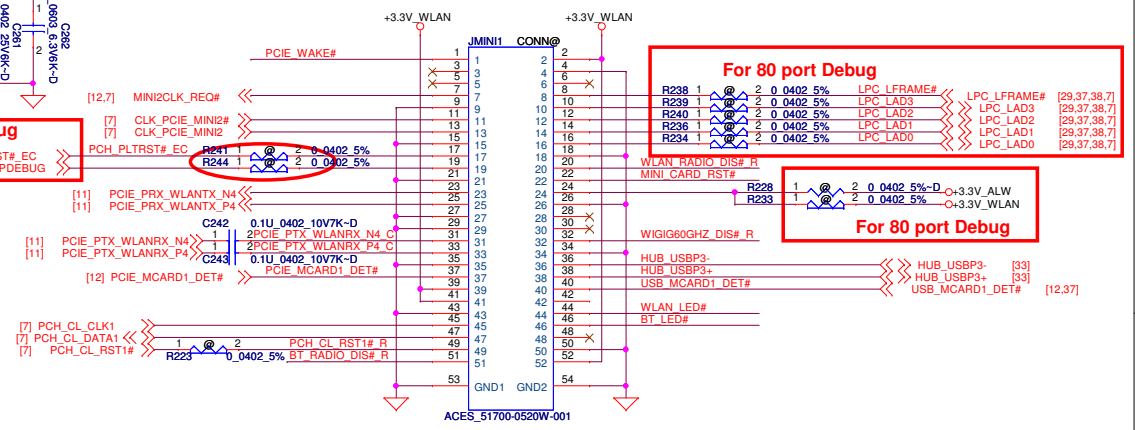


FMC: Mini WWAN/LTE H=8



For 80 port Debug
(29,31,33,36,37,38,9) PCH_PLTRST#_EC
(7) CLK_PCLPDEBUG

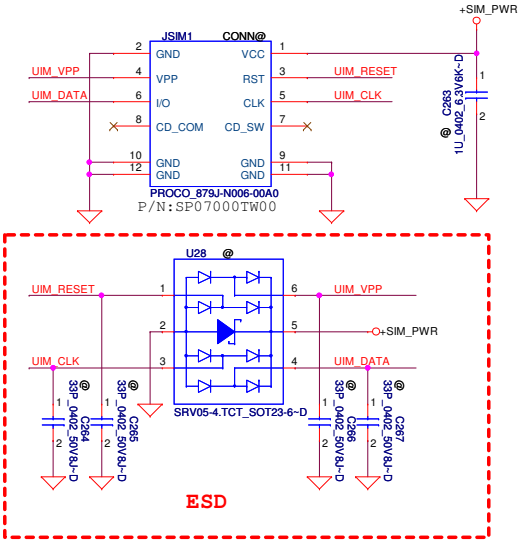
HMC: Mini WLAN/WiFi/BT H=4



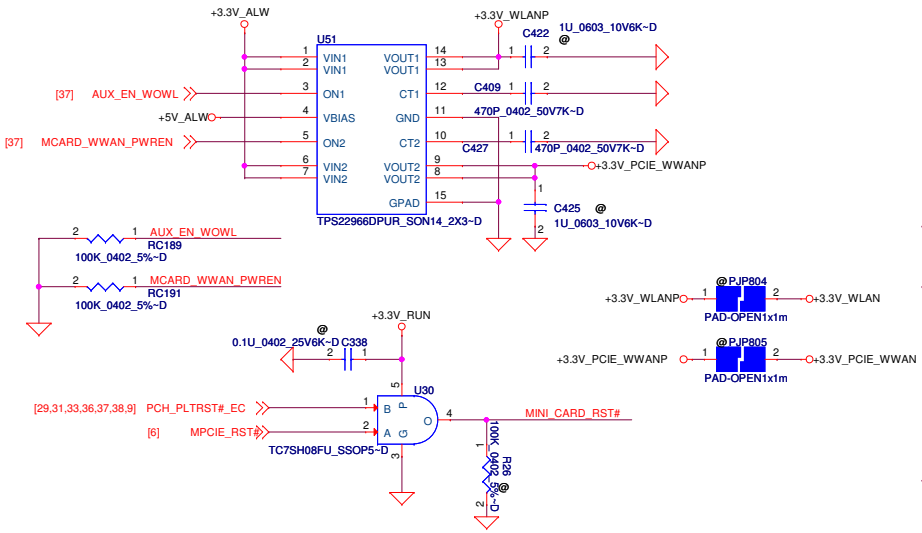
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)

X-Build Change

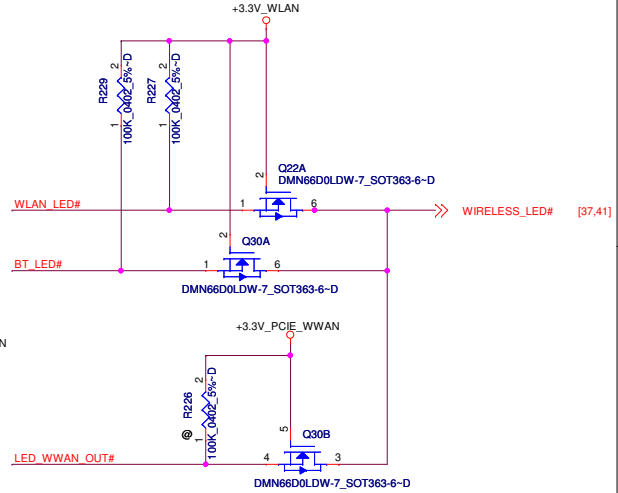
uSIM Card Push-Push



ESD



LED control circuit



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Mini Card/SIM Card

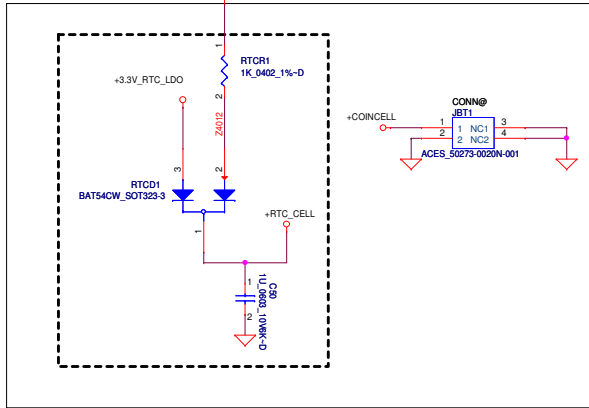
LA-A101P

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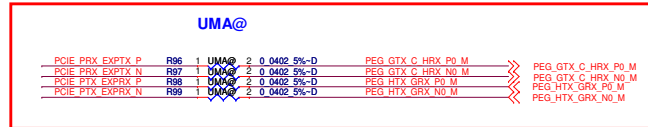
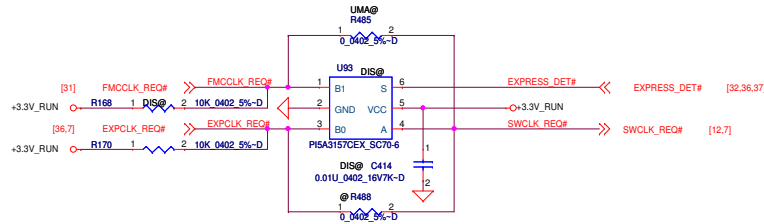
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EXP/FMC PCIe clock/REQ Switch

COIN RTC Battery

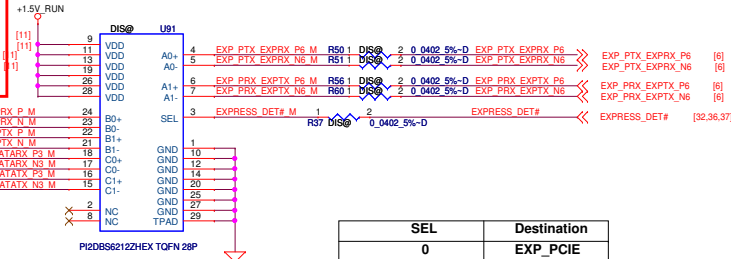
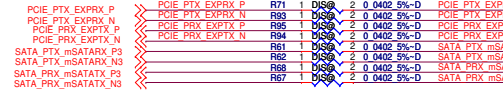


B \ S	EXPRESS_DET#
EXPCLK_REQ#	0
FMCCCLK_REQ#	1

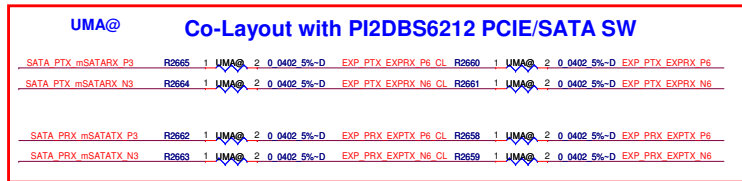


EXPRESS <----- [36]
 [36]
 [36]
 [31]
 [31]
 [31]

WWAN FMC <----- [31]
 [31]
 [31]



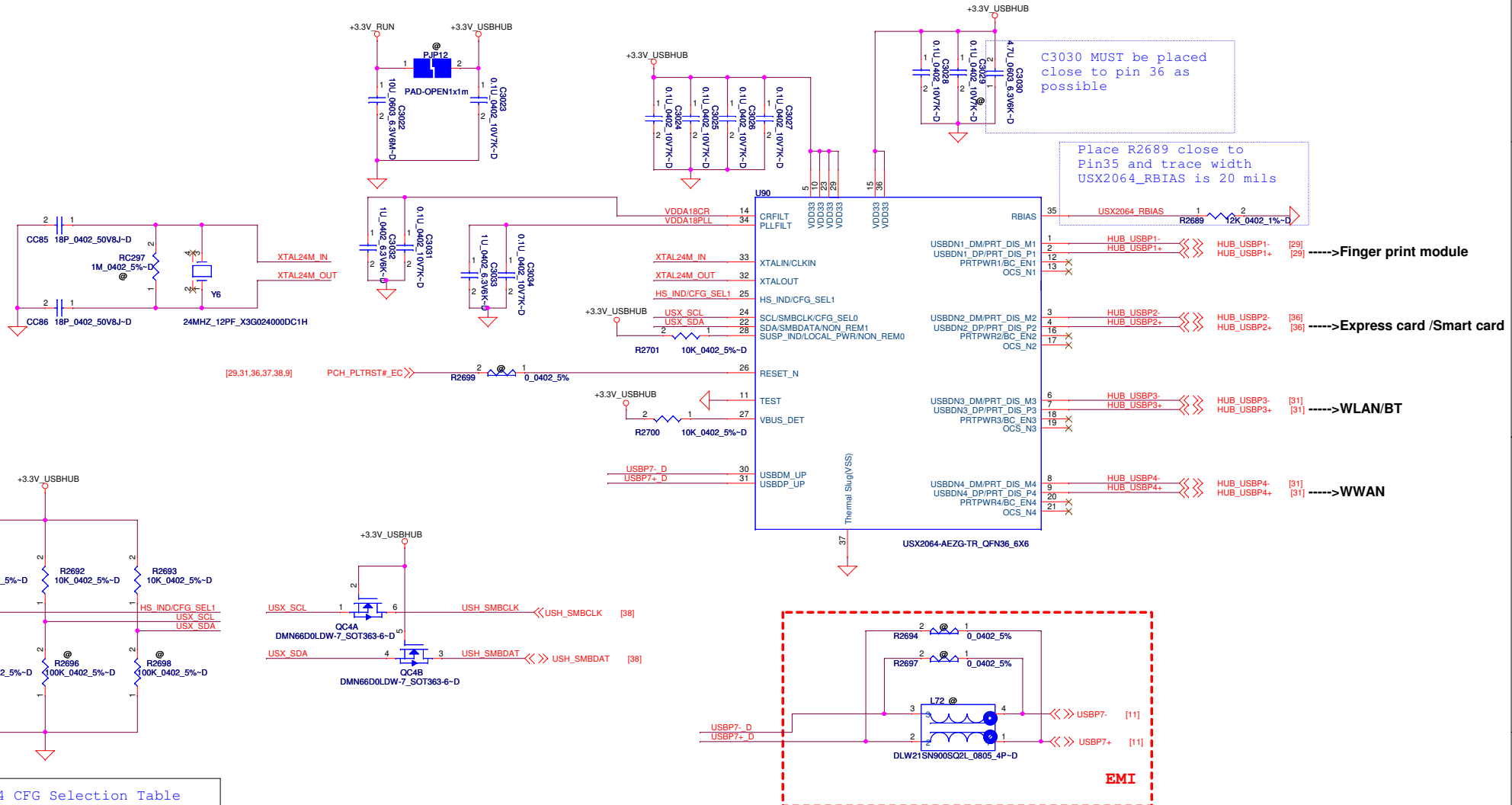
SEL	Destination
0	EXP_PCIE
1	mSATA



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		Compal Electronics, Inc.	
		RTC Batt/PCIE SATA SW	
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USX2064 CFG Selection Table

CFG_SEL[0]	CFG_SEL[1]	0	1
0	Default	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM	

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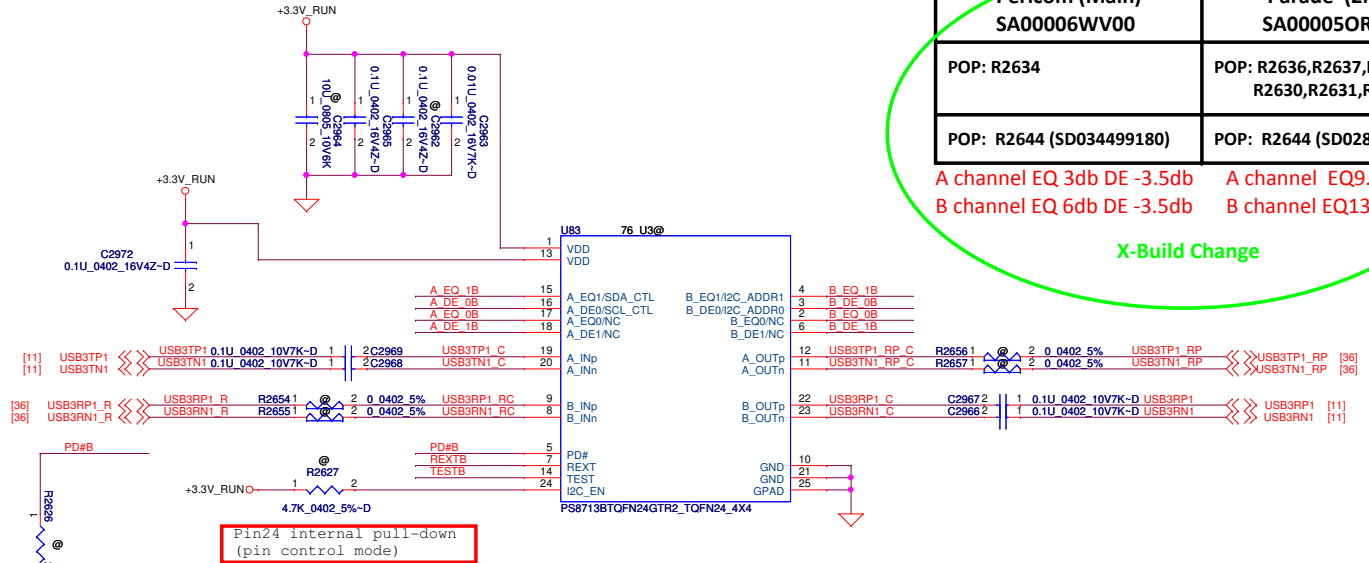
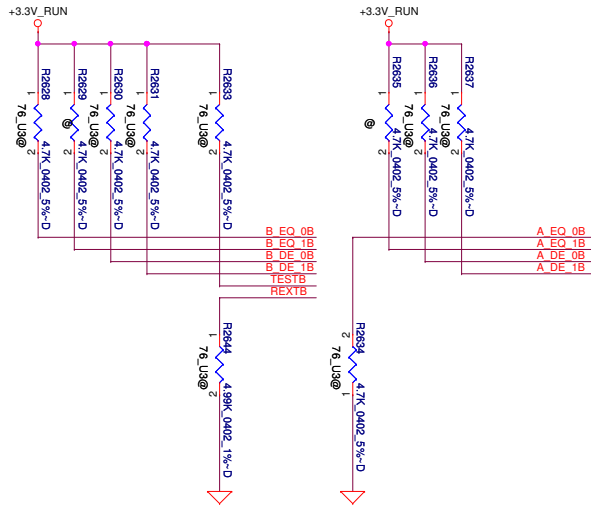
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USB2.0 HUB-USX2064

LA-A101P

Title	USB2.0 HUB-USX2064		
Size	Document Number	Rev 1.0	
Date	Monday, September 23, 2013	Sheet	33 of 65

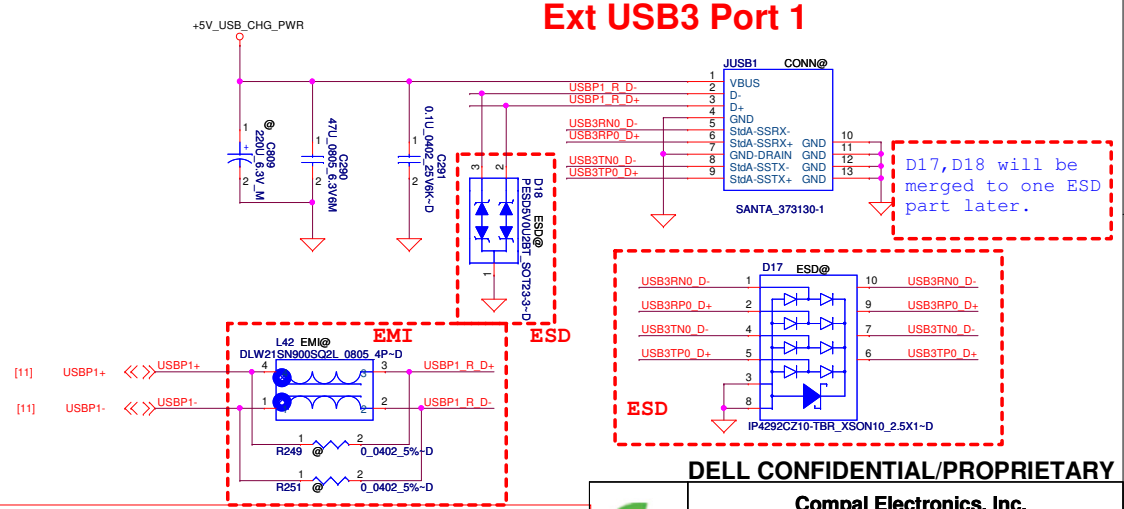
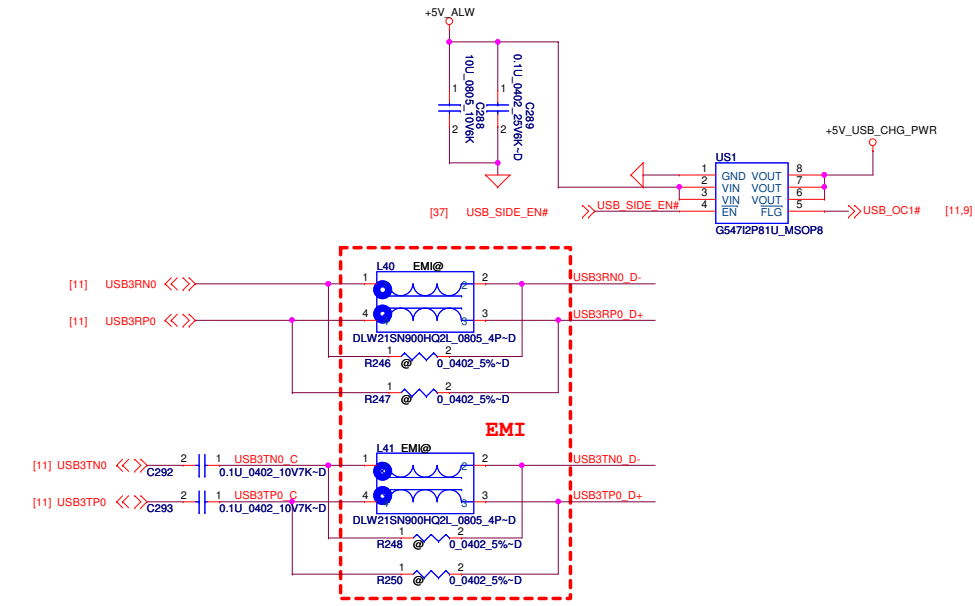
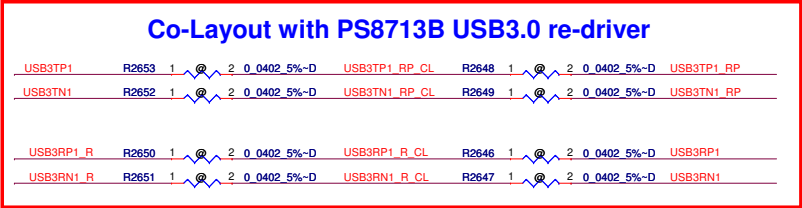
USB 3.0 Re-driver for IOB



Pericom (Main) SA00006WV00	Parade (2nd) SA00005OR20
POP: R2634	POP: R2636, R2637, R2628, R2630, R2631, R2633,
POP: R2644 (SD034499180)	POP: R2644 (SD028430180)

A channel EQ 3db DE -3.5db A channel EQ9.5 DE 5
 B channel EQ 6db DE -3.5db B channel EQ13 DE 5

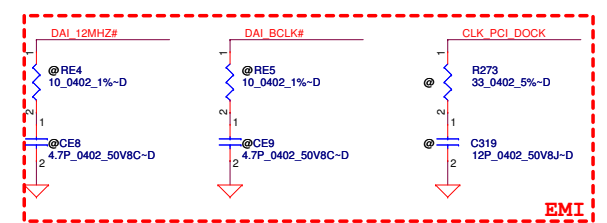
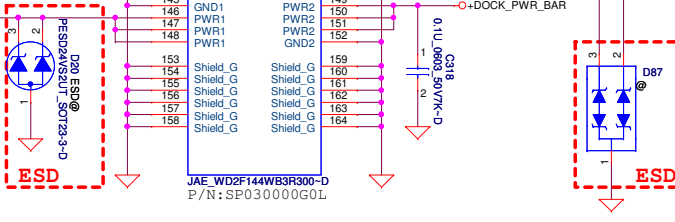
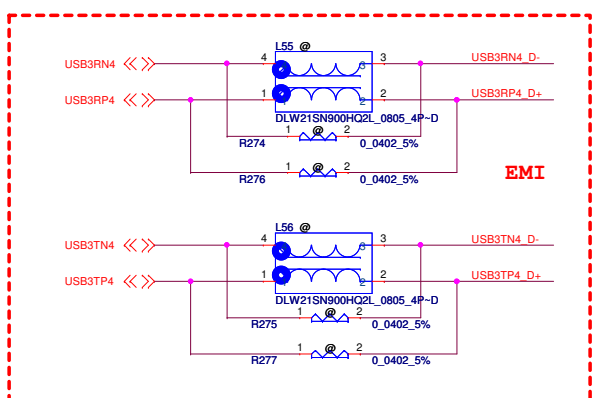
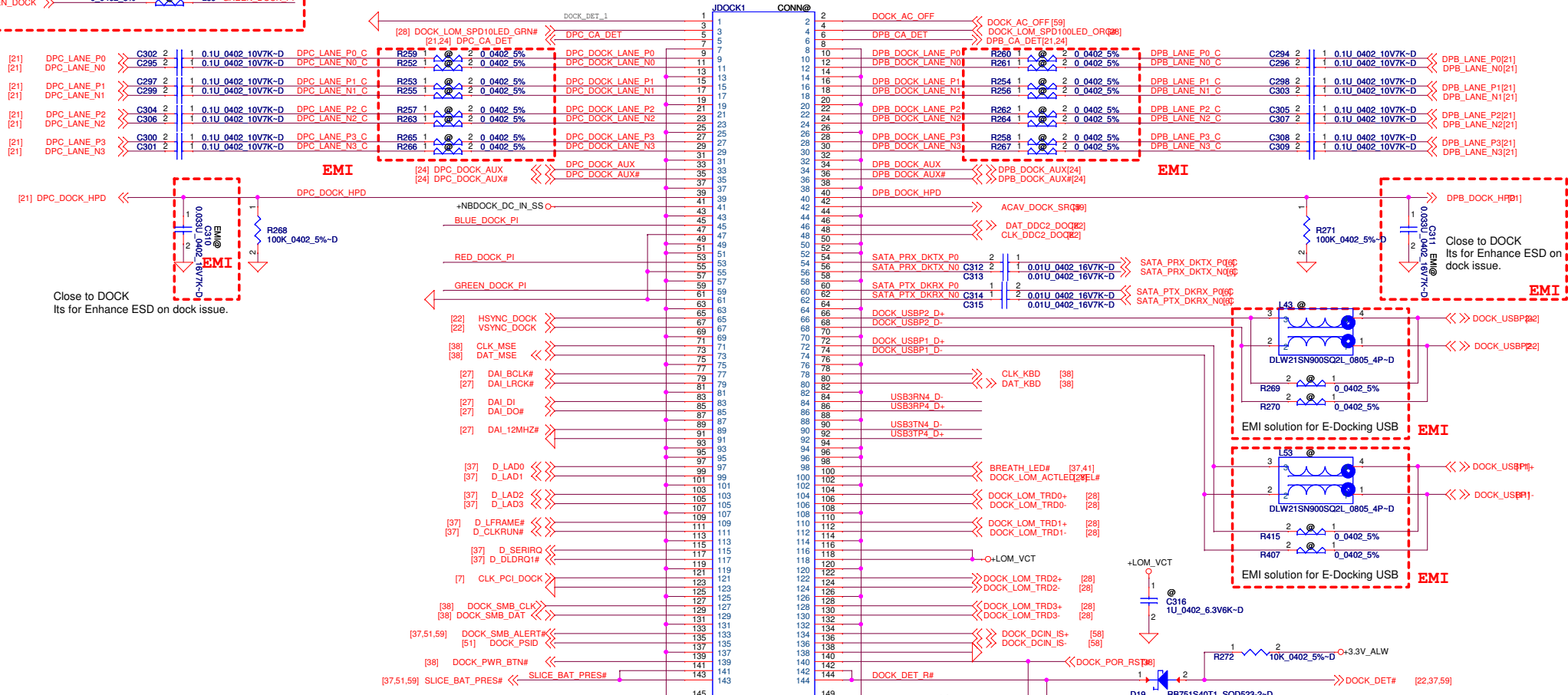
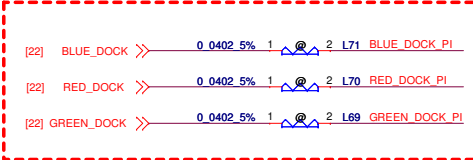
X-Build Change



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USB on MB/Redriver			
File	LA-A101P		
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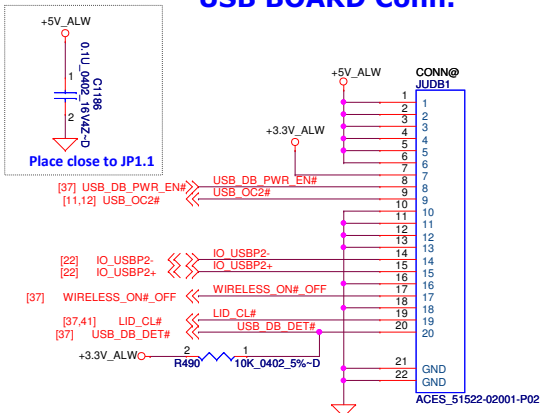
Compal Electronics, Inc.

E series Dock Connector

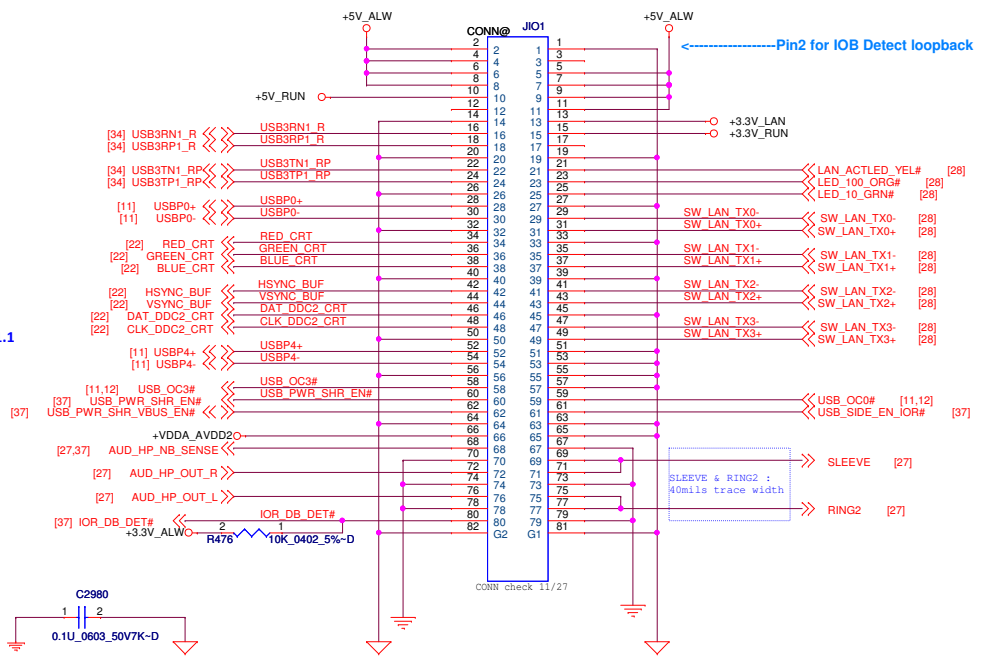
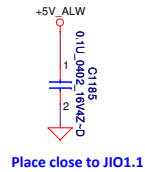
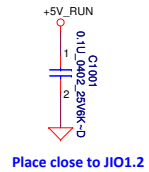
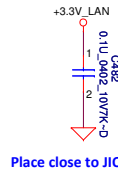
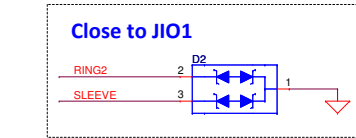
LA-A101P

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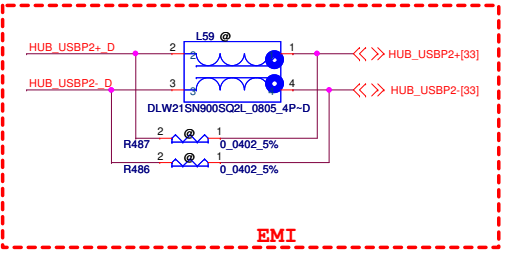
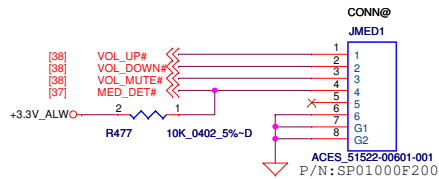
USB BOARD Conn.



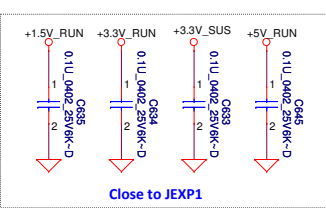
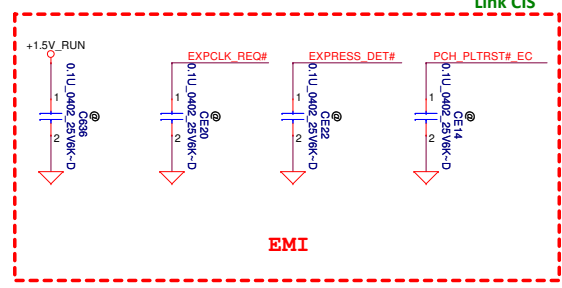
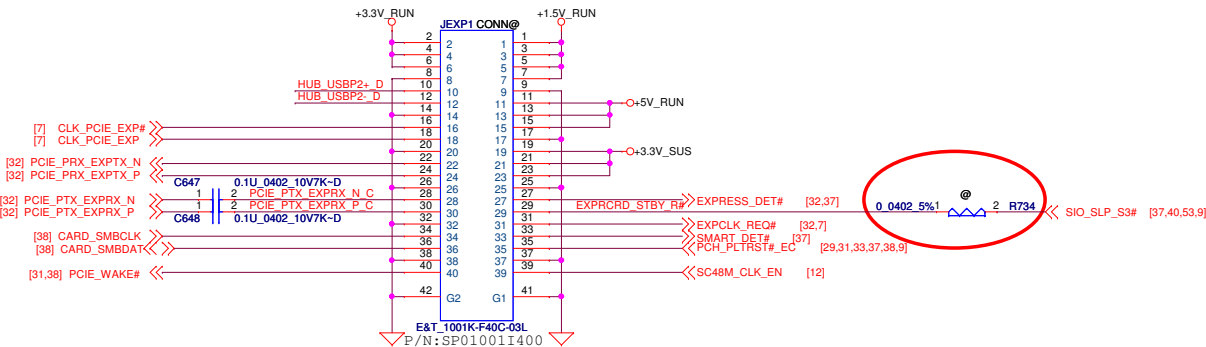
Close to JIO1



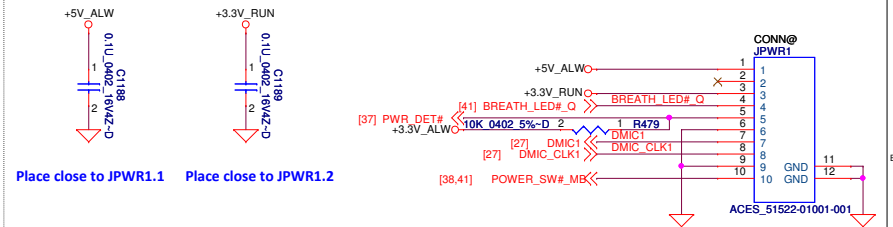
MEDIA BOARD Conn.



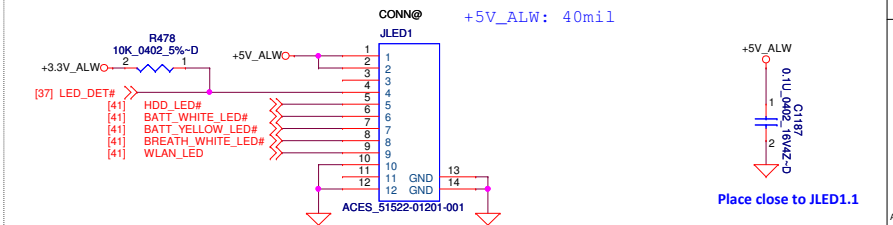
Express/Smart Card Conn.



POWER BOARD Conn.



LED EXTERNAL BOARD Conn.



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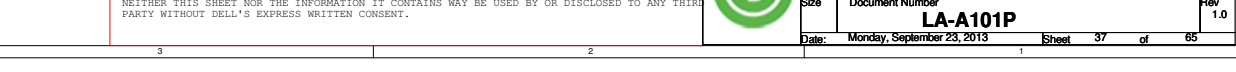
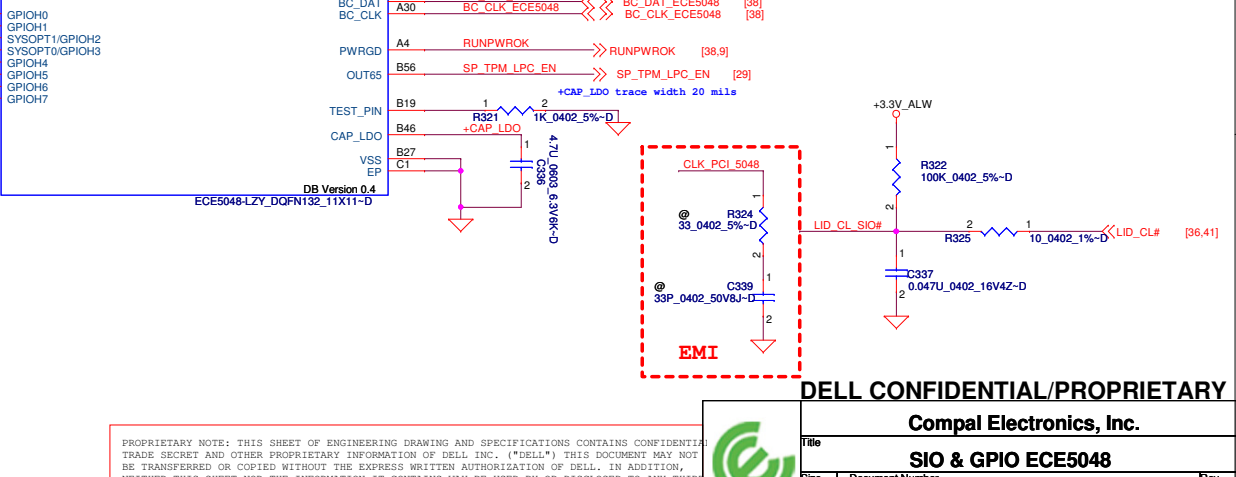
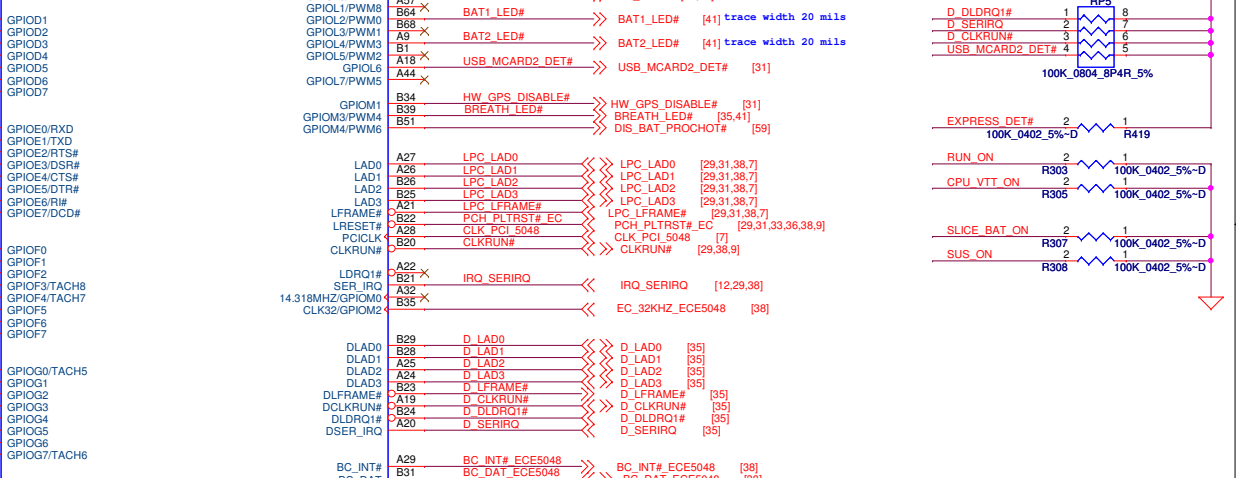
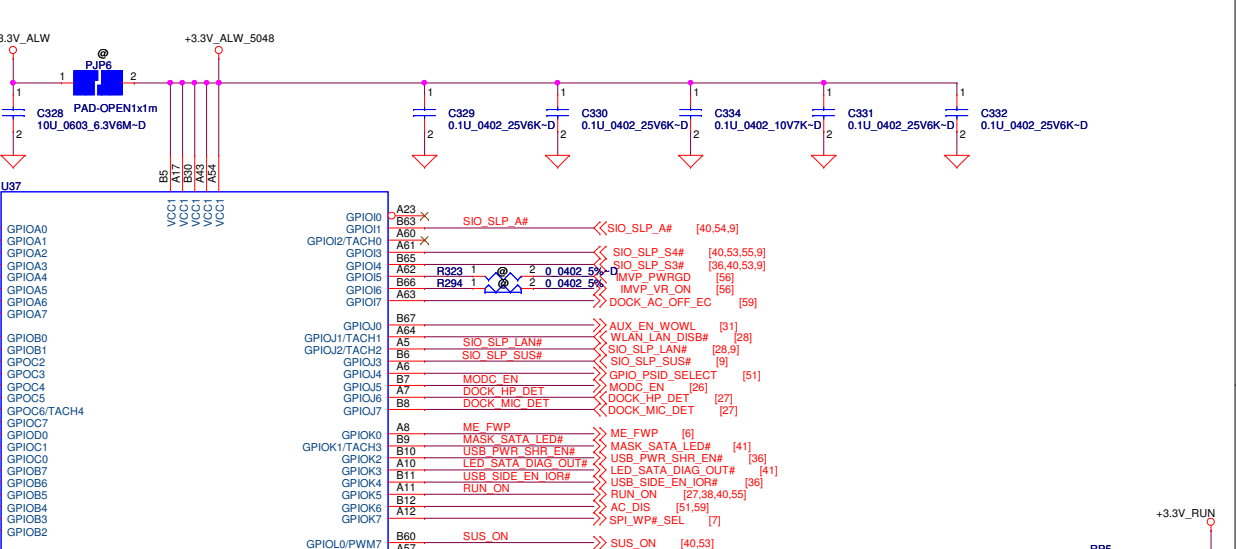
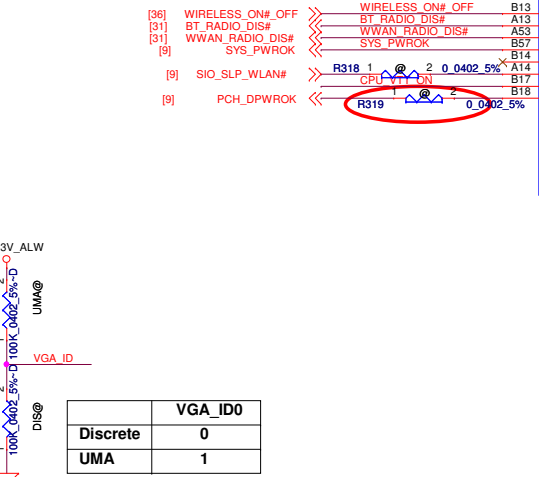
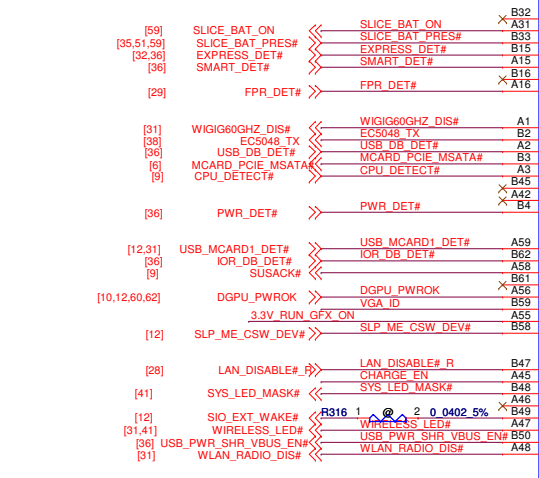
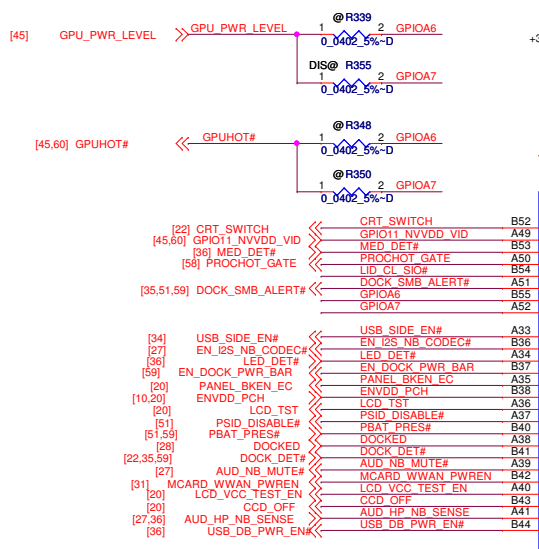
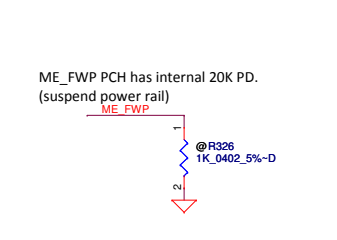
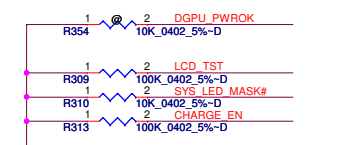
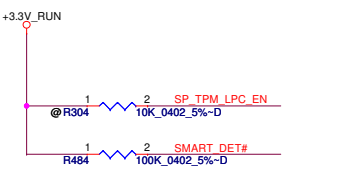
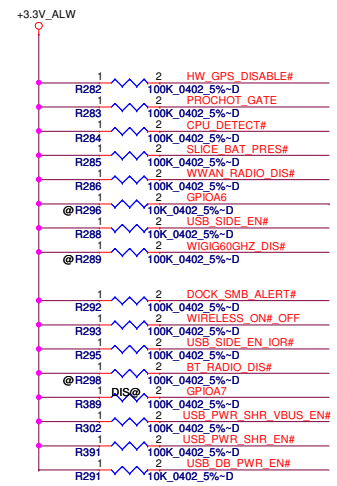
Compal Electronics, Inc.

I/O Conn

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	VGA_ID0
Discrete	0
UMA	1

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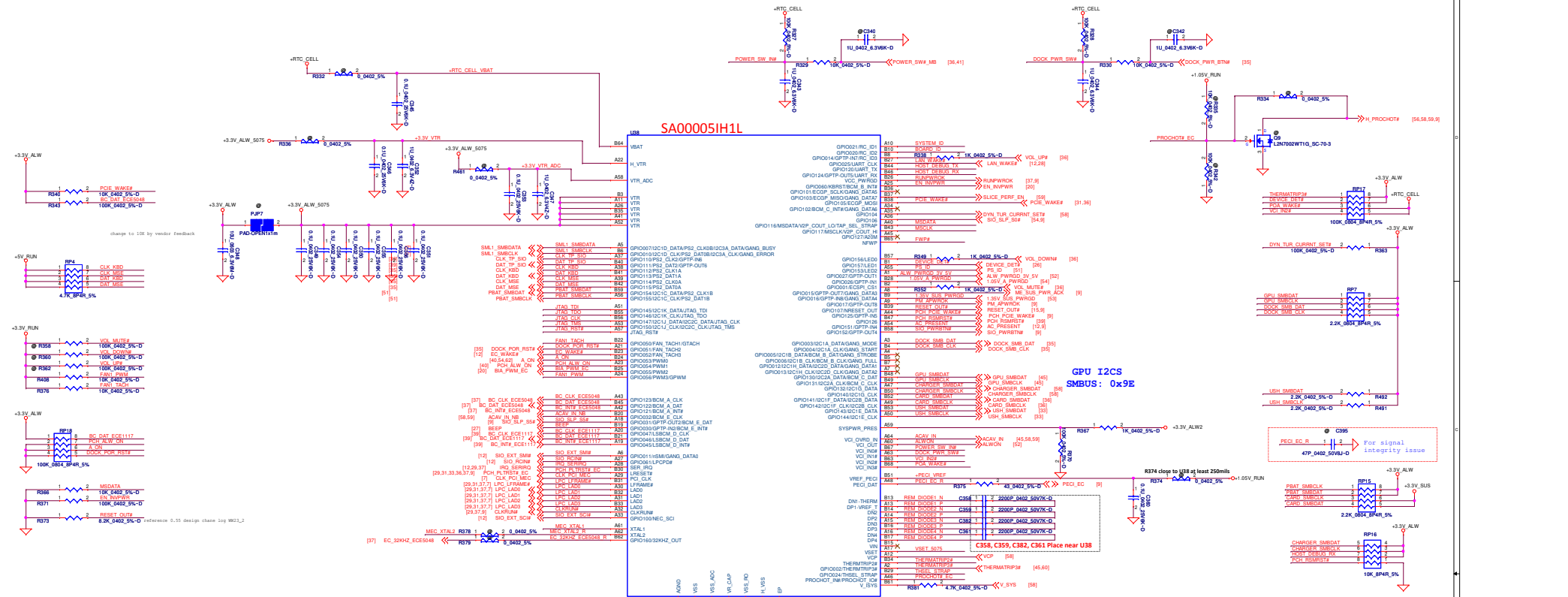
Compal Electronics, Inc.

SIO & GPIO ECE5048

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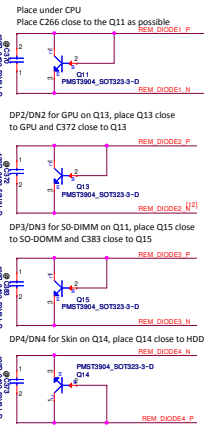
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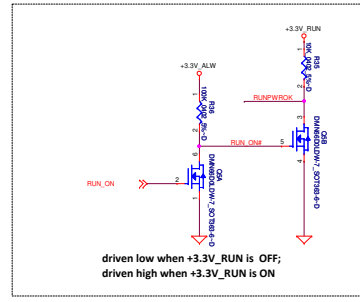
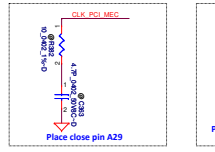
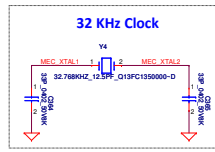
5075 Setting for Thermal Design

Thermal diode mapping

5075 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	Skin
DP3/DN3	SO-DIMM
DP4/DN4	HDD



1: Channel 1 will provide Thermistor Readings
 0: Channel 1 will provide Diode Readings



R392	C366	REV
240K	4700p	X00
130K	4700p	X01(P1)
62K	4700p	X01(P2)
33K	4700p	X02
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

80 Port Debug/ LPC BUS --> WLAN conn.

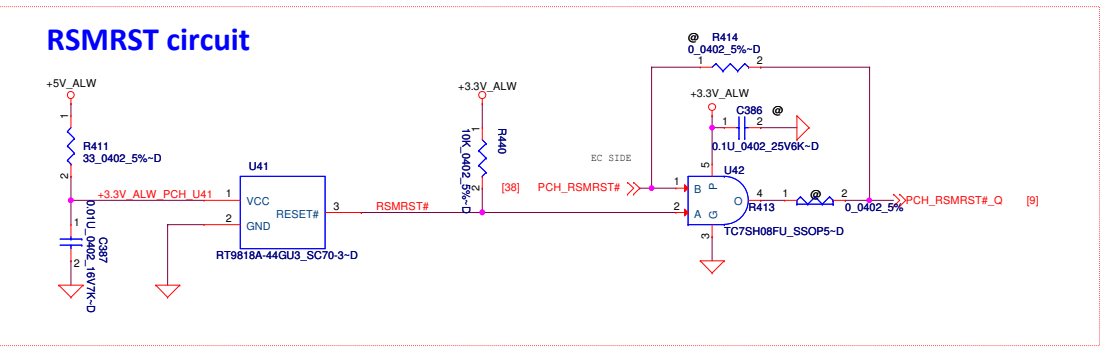
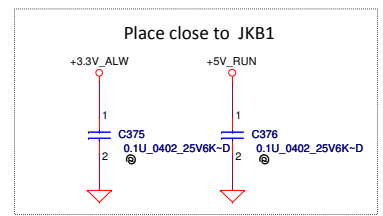
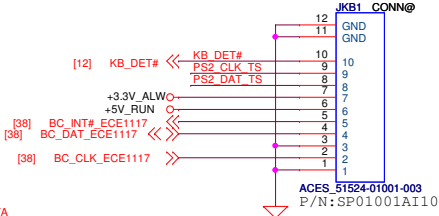
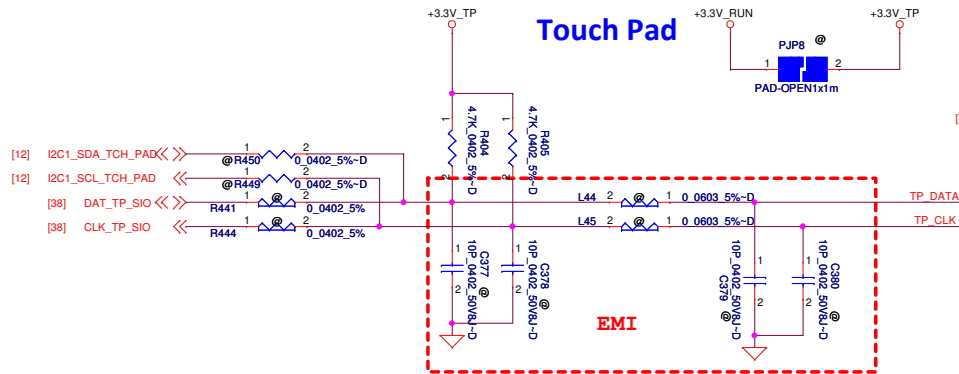
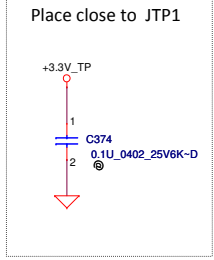
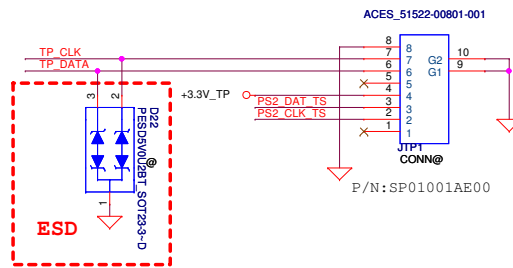
BOARD_ID rise time is measured from 5%~68%.

CHIPSET_ID for BID function

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KBC & GPIO MEC5075
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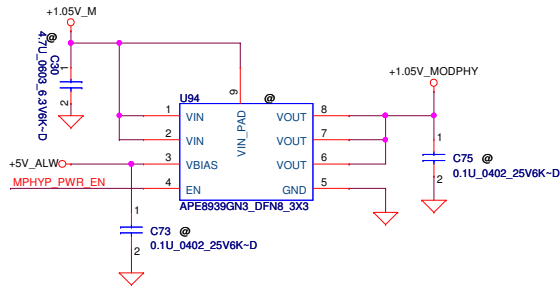
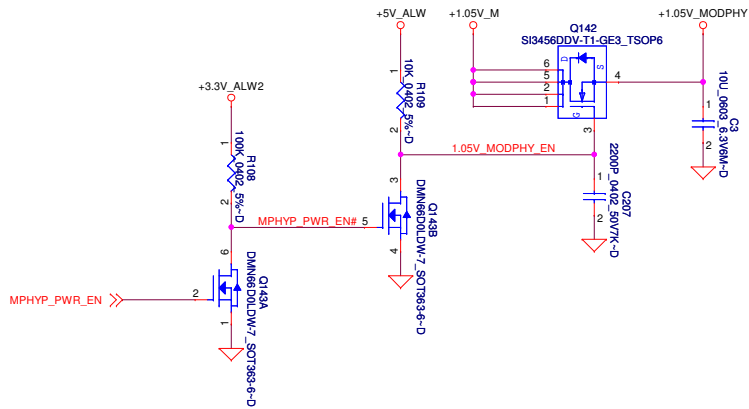
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Size: **LA-A101P**

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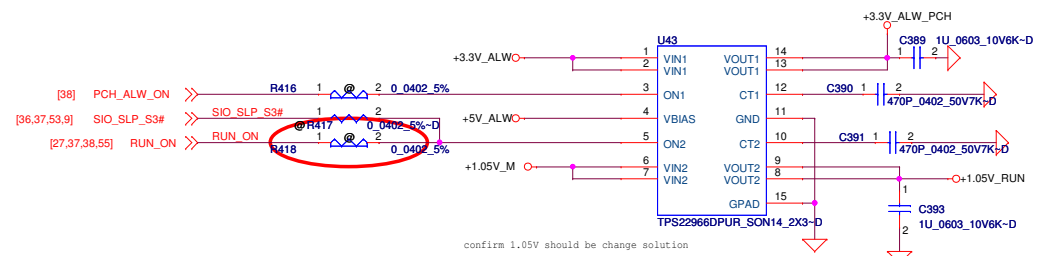
Rev: 1.0

+1.05V_MODPHY source

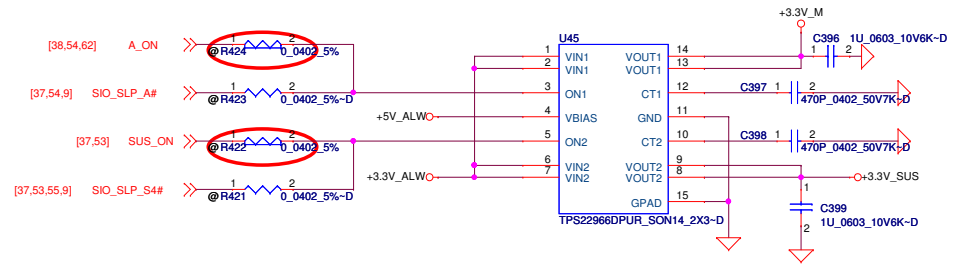


DC/DC Interface

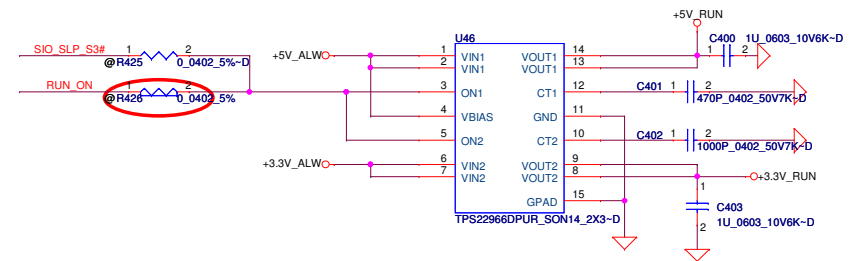
+3.3V_ALW_PCH/+1.05V_RUN source



+3.3V_SUS/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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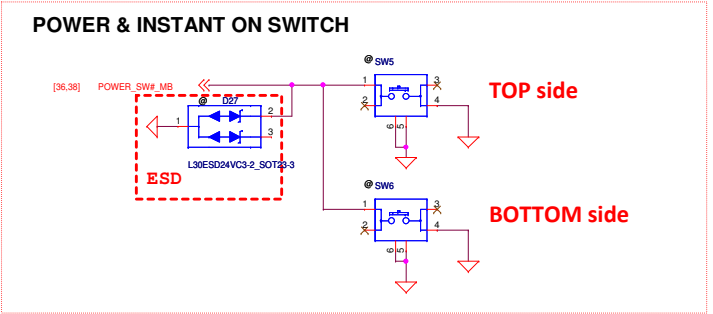
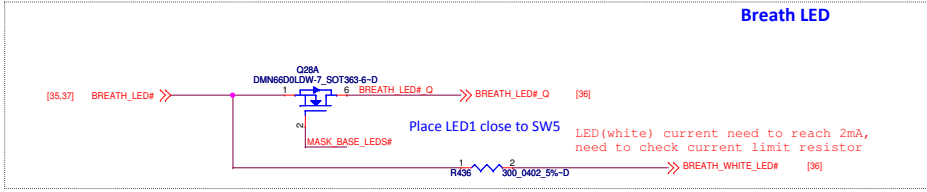
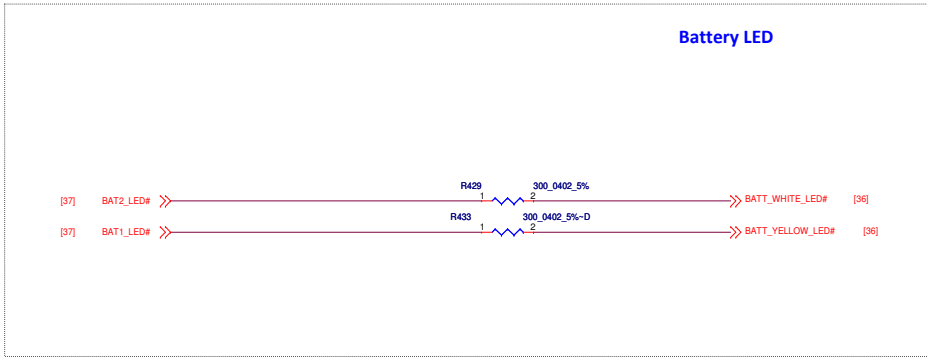
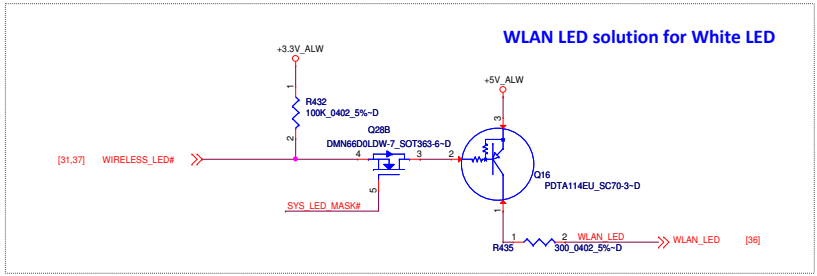
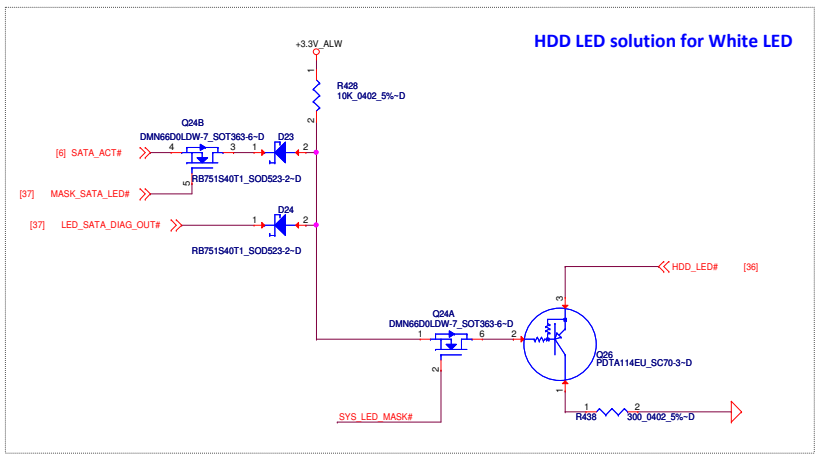
POWER CONTROL

LA-A101P

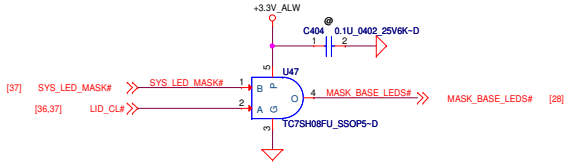
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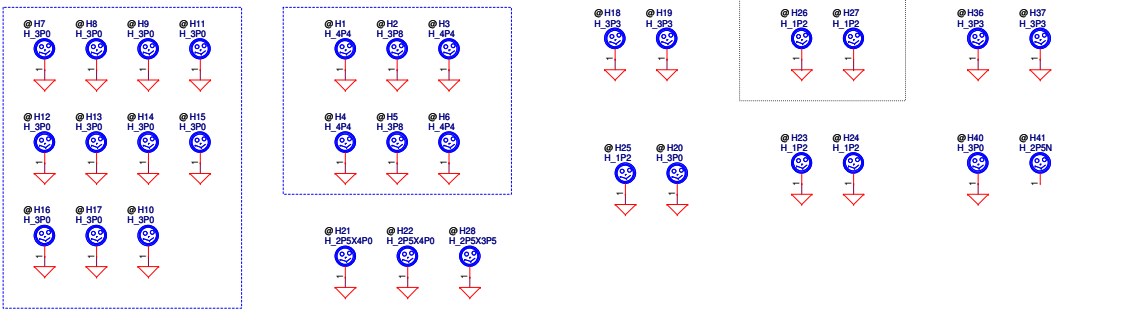


Lid has been moved to DB.



- #### Fiducial Mark
- FD1 FIDUCIAL MARK-D
 - FD2 FIDUCIAL MARK-D
 - FD3 FIDUCIAL MARK-D
 - FD4 FIDUCIAL MARK-D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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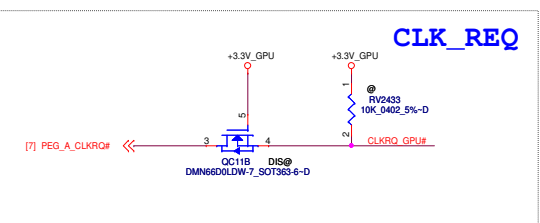
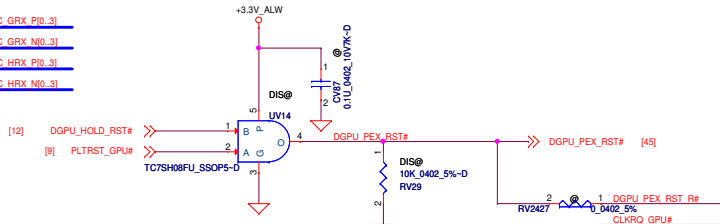
PAD & ME & LED

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Monday, September 23, 2013

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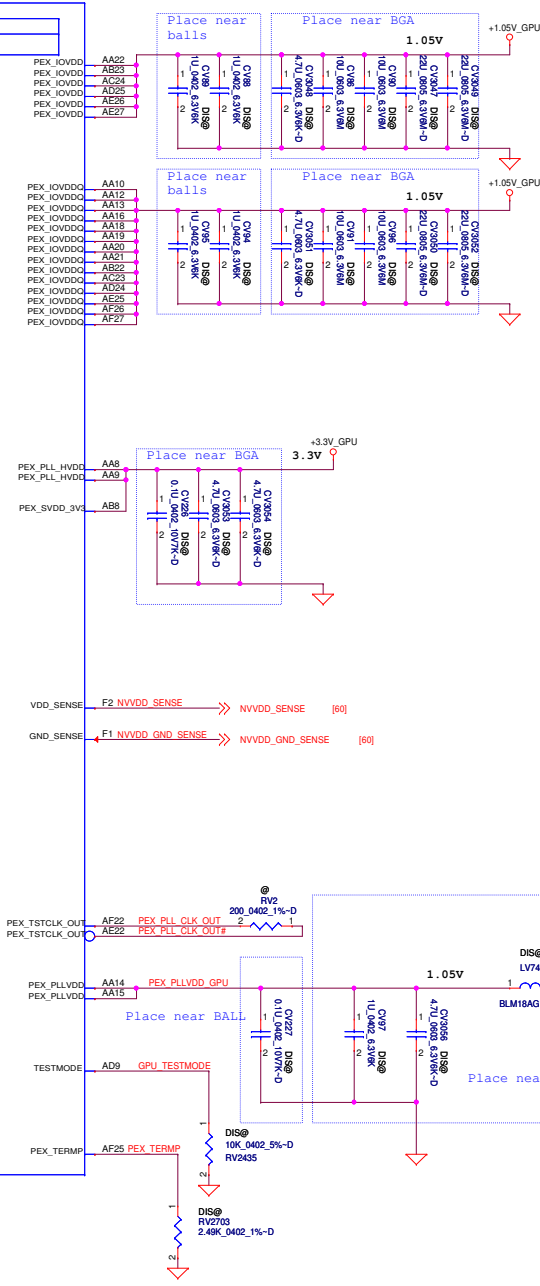
[11] PEG_HTX_C_GRX_P[0..3] >> PEG_HTX_C_GRX_P[0..3]
 [11] PEG_HTX_C_GRX_N[0..3] >> PEG_HTX_C_GRX_N[0..3]
 [11] PEG_GTX_C_HRX_P[0..3] >> PEG_GTX_C_HRX_P[0..3]
 [11] PEG_GTX_C_HRX_N[0..3] >> PEG_GTX_C_HRX_N[0..3]



PEG_GTX_C_HRX_P0 0.1U 0402 10V7K-D DIS@ 1 2 CV2402 PEG_GTX_HRX_P0 AC9
 PEG_GTX_C_HRX_N0 0.1U 0402 10V7K-D DIS@ 1 2 CV2403 PEG_GTX_HRX_N0 AB9
 PEG_HTX_C_GRX_P0 AG6
 PEG_HTX_C_GRX_N0 AG7
 PEG_GTX_C_HRX_P1 0.1U 0402 10V7K-D DIS@ 1 2 CV2404 PEG_GTX_HRX_P1 AB10
 PEG_GTX_C_HRX_N1 0.1U 0402 10V7K-D DIS@ 1 2 CV2405 PEG_GTX_HRX_N1 AC10
 PEG_HTX_C_GRX_P1 AF7
 PEG_HTX_C_GRX_N1 AE7
 PEG_GTX_C_HRX_P2 0.1U 0402 10V7K-D DIS@ 1 2 CV2406 PEG_GTX_HRX_P2 AD11
 PEG_GTX_C_HRX_N2 0.1U 0402 10V7K-D DIS@ 1 2 CV2407 PEG_GTX_HRX_N2 AC11
 PEG_HTX_C_GRX_P2 AE9
 PEG_HTX_C_GRX_N2 AF9
 PEG_GTX_C_HRX_P3 0.1U 0402 10V7K-D DIS@ 1 2 CV2408 PEG_GTX_HRX_P3 AC12
 PEG_GTX_C_HRX_N3 0.1U 0402 10V7K-D DIS@ 1 2 CV2401 PEG_GTX_HRX_N3 AB12
 PEG_HTX_C_GRX_P3 AG9
 PEG_HTX_C_GRX_N3 AG10

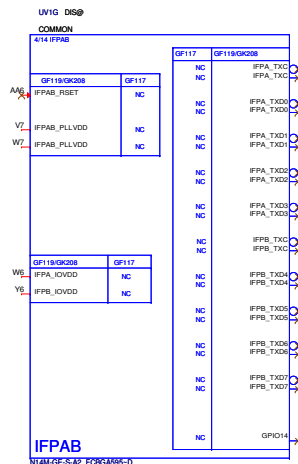
COMMON		U14 PCI_EXPRESS	
AB6	PEX_WAKE	GN208/GF117/GF119	NC
AC7	PEX_RST		
AC6	PEX_CLKREQ		
AE8	PEX_REFCLK		
AD8	PEX_REFCLK		
PEX_TX8			
PEX_TX0			
PEX_RX9			
PEX_RX0			
PEX_TX1			
PEX_TX1			
PEX_RX1			
PEX_RX1			
PEX_TX2			
PEX_TX2			
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GF119		GF117	
		GN208	

NT4M-GE-S-A2_FCBGA596-D

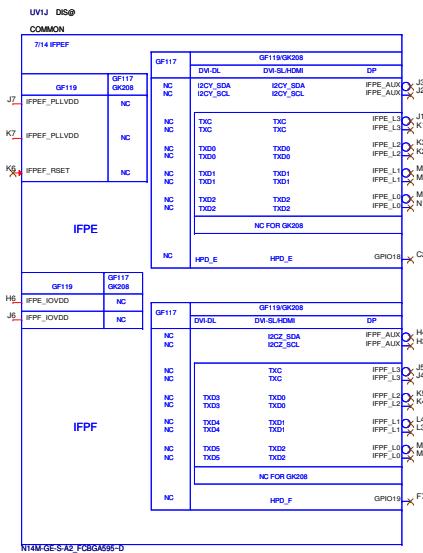


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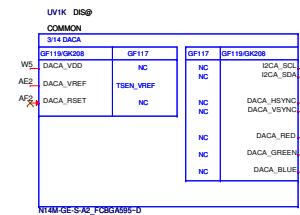
IFPA/B



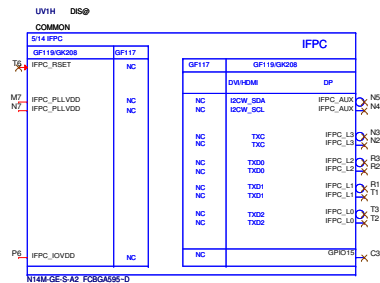
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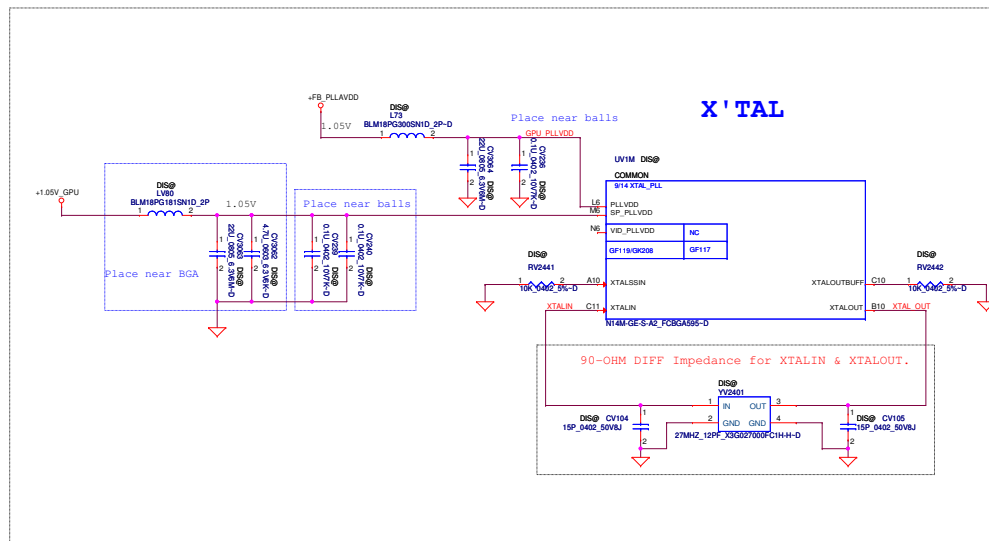
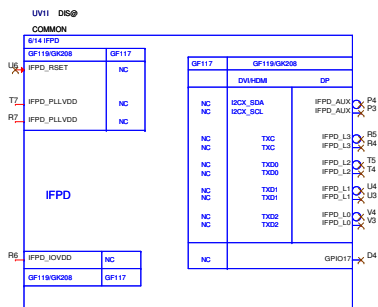
DAC_A

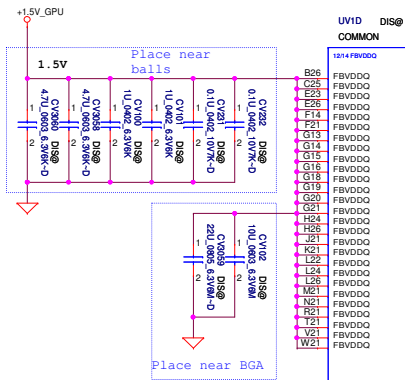


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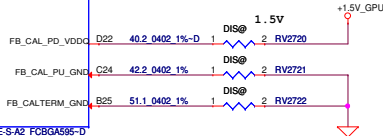


IFPD

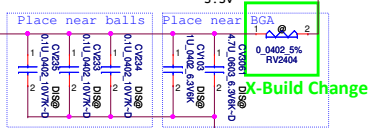




- UV1D DIS@
COMMON
- B26 FBVDDQ
 - C26 FBVDDQ
 - D26 FBVDDQ
 - E26 FBVDDQ
 - F26 FBVDDQ
 - G26 FBVDDQ
 - H26 FBVDDQ
 - J26 FBVDDQ
 - K26 FBVDDQ
 - L26 FBVDDQ
 - M26 FBVDDQ
 - N26 FBVDDQ
 - P26 FBVDDQ
 - R26 FBVDDQ
 - T26 FBVDDQ
 - V26 FBVDDQ
 - W26 FBVDDQ

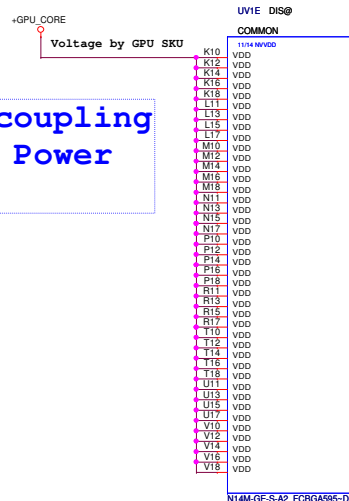


- UV1C DIS@
COMMON
- 14x4 xVDDQVDD33
- VDD33 G19
 - VDD33 G12
 - VDD33 G8
 - VDD33 G9
- AD10 NC
- AD08 NC
- AD06 NC
- F11 3V3AUX_NC
- V5 FERM1_RSVD1_NC
- V6 FERM1_RSVD2_NC
- CONFIGURABLE POWER CHANNELS
*nc on substrate
- G1 XPWR_G1
 - G2 XPWR_G2
 - G3 XPWR_G3
 - G4 XPWR_G4
 - G5 XPWR_G5
 - G6 XPWR_G6
 - G7 XPWR_G7
- W1 XPWR_W1
 - W2 XPWR_W2
 - W3 XPWR_W3
 - W4 XPWR_W4

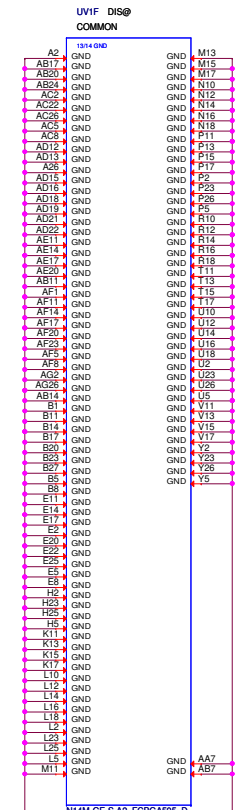


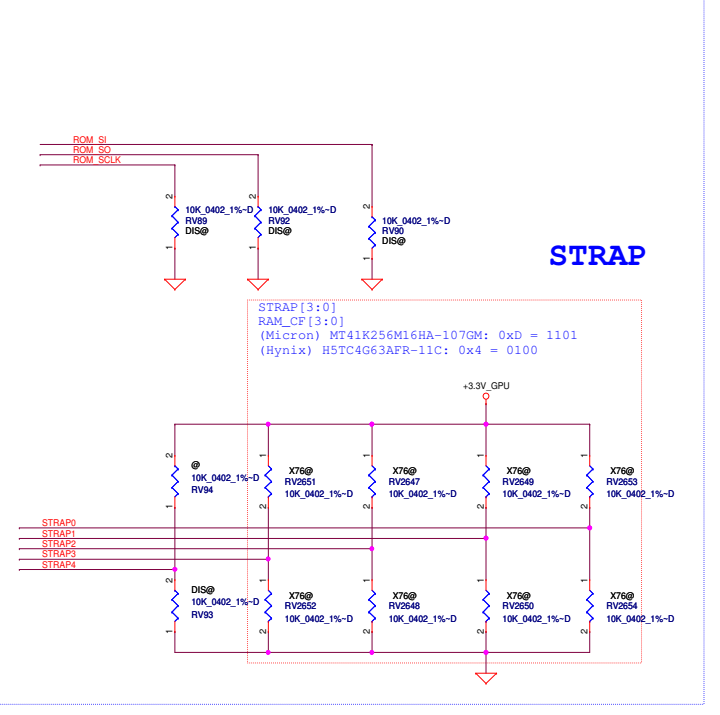
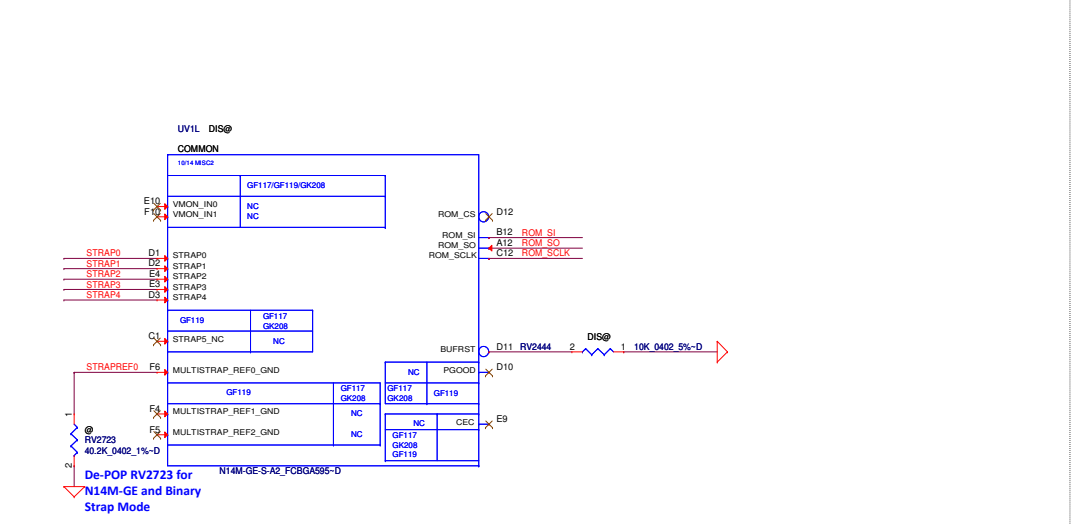
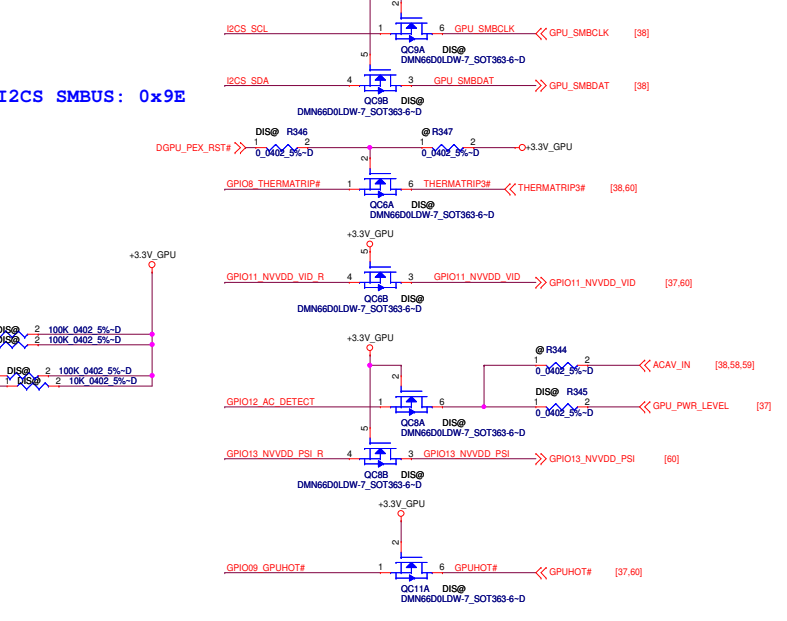
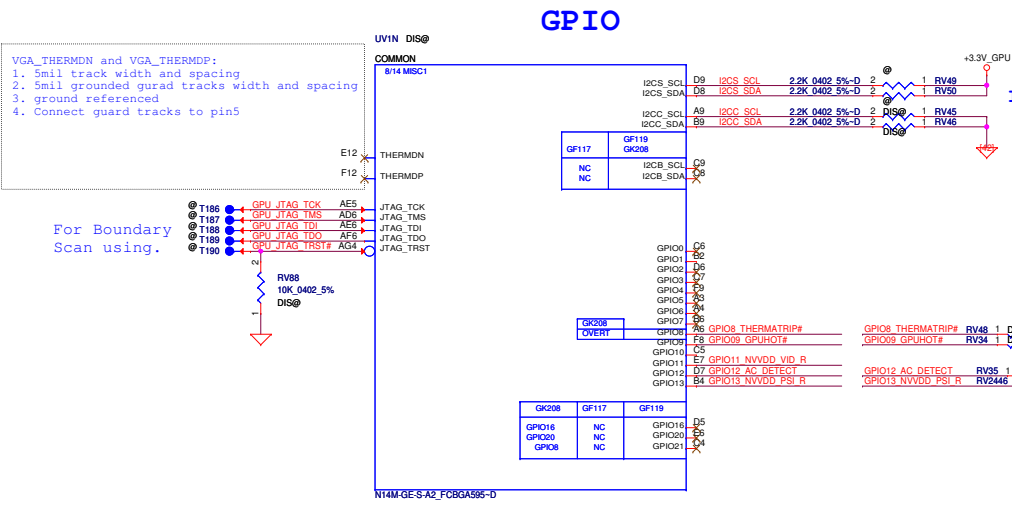
** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

GPU_Decoupling CAPs @ Power Page



- UV1E DIS@
COMMON
- 1314 REV00
- K10 VDD
 - K12 VDD
 - K14 VDD
 - K16 VDD
 - K18 VDD
 - L11 VDD
 - L13 VDD
 - L15 VDD
 - L17 VDD
 - M10 VDD
 - M12 VDD
 - M14 VDD
 - M16 VDD
 - M18 VDD
 - N11 VDD
 - N13 VDD
 - N15 VDD
 - N17 VDD
 - P10 VDD
 - P12 VDD
 - P14 VDD
 - P16 VDD
 - P18 VDD
 - R11 VDD
 - R13 VDD
 - R15 VDD
 - R17 VDD
 - T10 VDD
 - T12 VDD
 - T14 VDD
 - T16 VDD
 - T18 VDD
 - U11 VDD
 - U13 VDD
 - U15 VDD
 - U17 VDD
 - V10 VDD
 - V12 VDD
 - V14 VDD
 - V16 VDD
 - V18 VDD

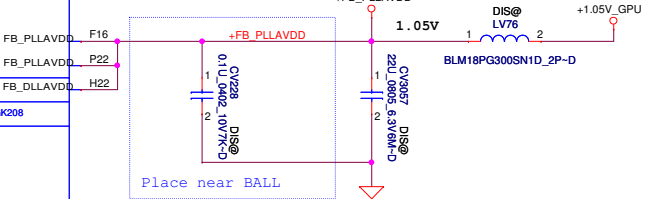
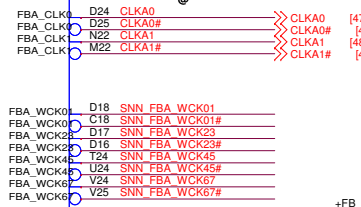
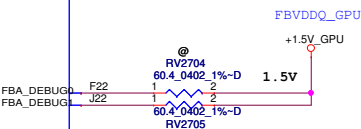
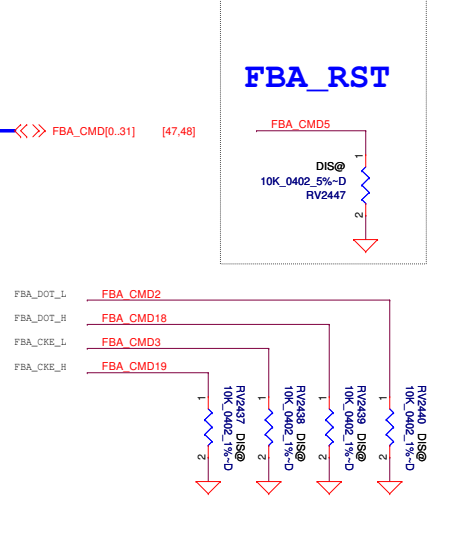
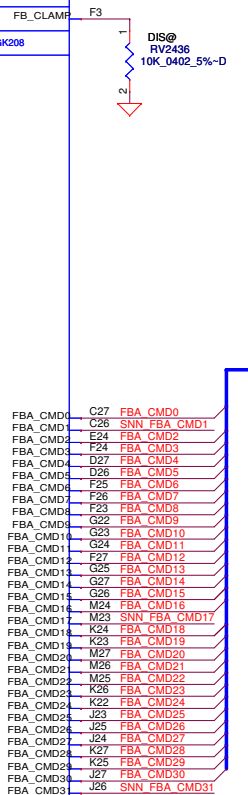
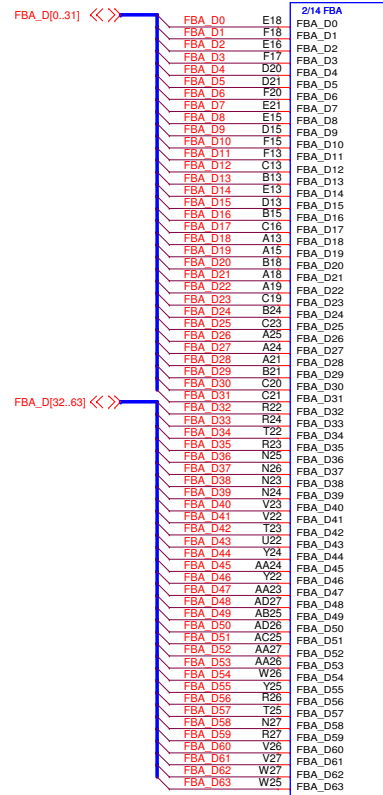




UV1B DIS@ COMMON N14M-GE-S-A2_FCBGA595-D

NC	FB_CLAMP
GF119	GF117/GK208

FB_PLLAVDD	FB_DLLAVDD
GF117	GF119/GK208



For VRAM DEBUG using
 @ T171 FB_VREF D23 FB_VREF_PROBE

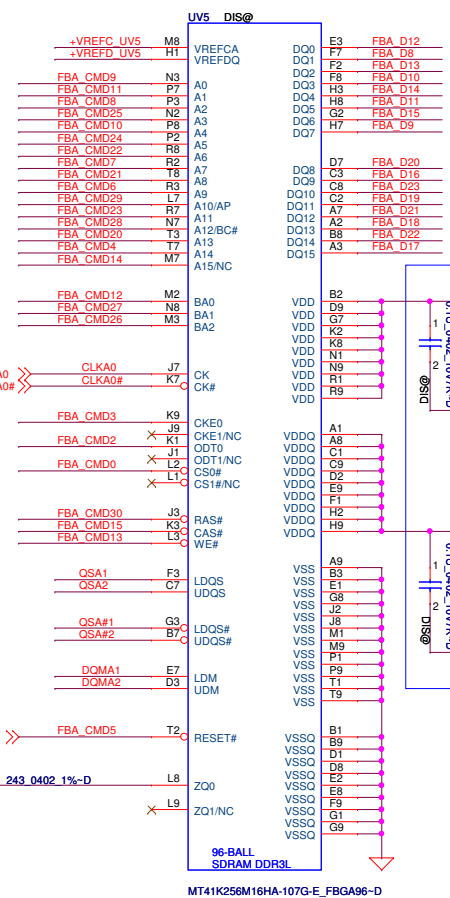
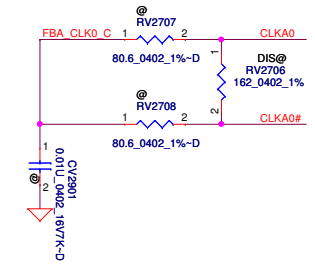
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Issued Date	2011/07/15	Deciphered Date
2012/07/15		
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Compal Electronics, Inc.	
NY(5/5)-MEMORY FBA	
Document Number	LA-A101P
Date: Monday, September 23, 2013	Rev 1.0
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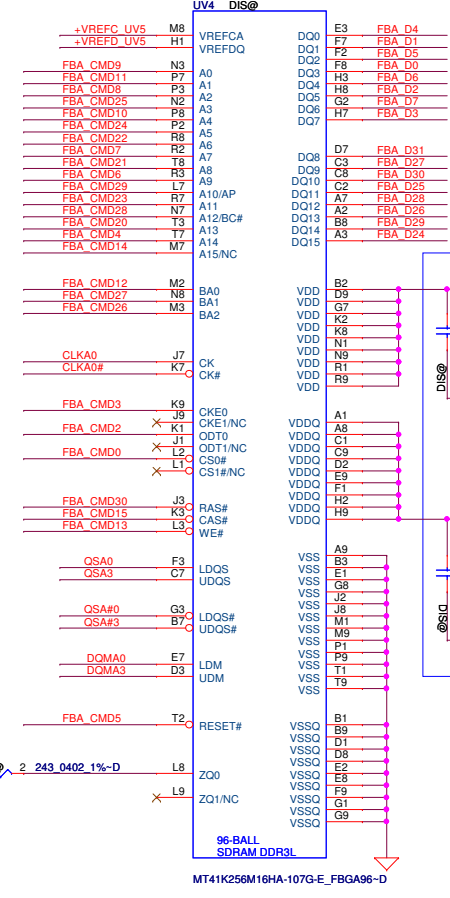
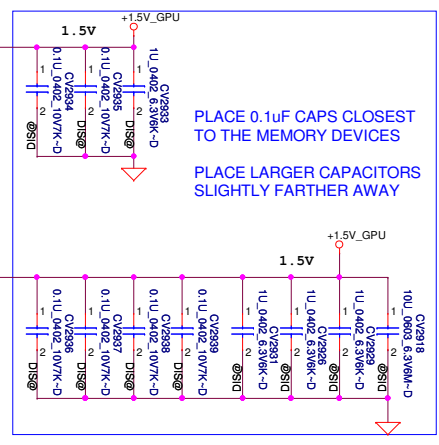
Memory Partition A - Lower 32 bits [31..0]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

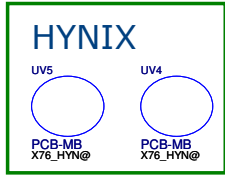
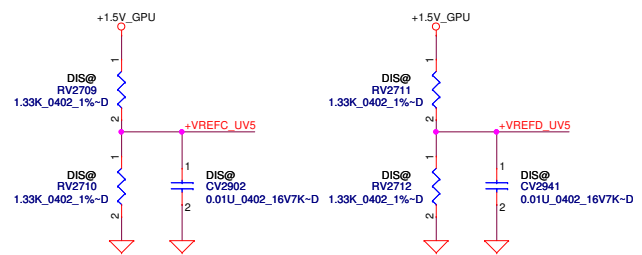
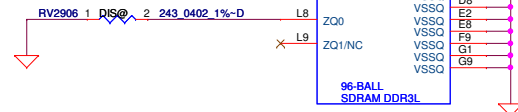
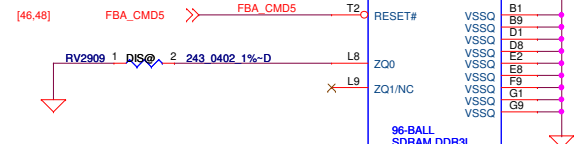
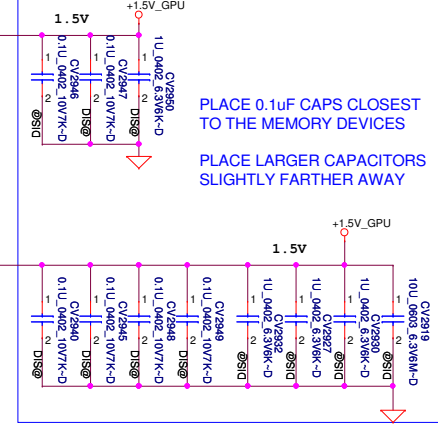
VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E



- [46] FBA_D[0..31] <<>>
- [46] DQMA[3..0] <<>>
- [46] QSA[3..0] <<>>
- [46] QSA[3..0] <<>>
- [46,48] FBA_CMD[0..31] <<>>



- [46] FBA_D[0..31] <<>>
- [46] DQMA[3..0] <<>>
- [46] QSA[3..0] <<>>
- [46] QSA[3..0] <<>>
- [46,48] FBA_CMD[0..31] <<>>



A15 is not required for any x16 device, even up to 4Gb density.

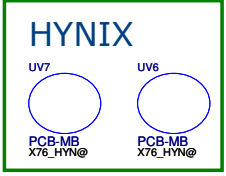
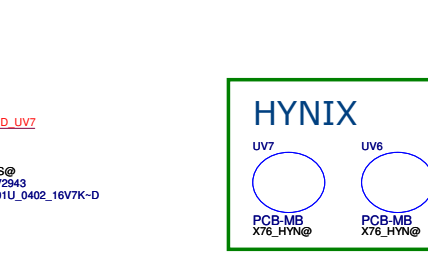
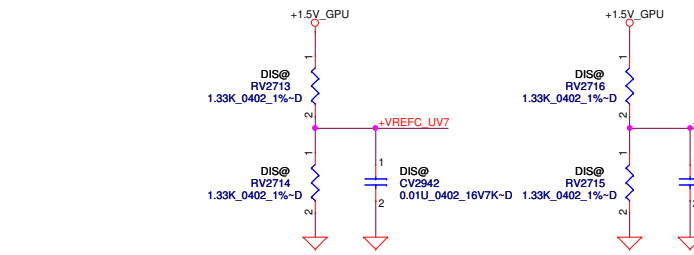
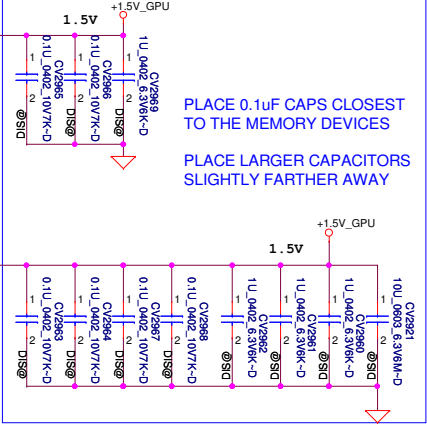
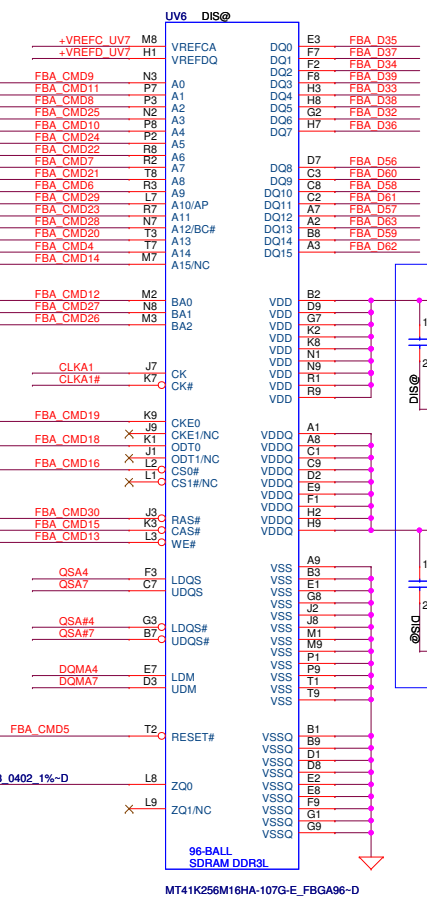
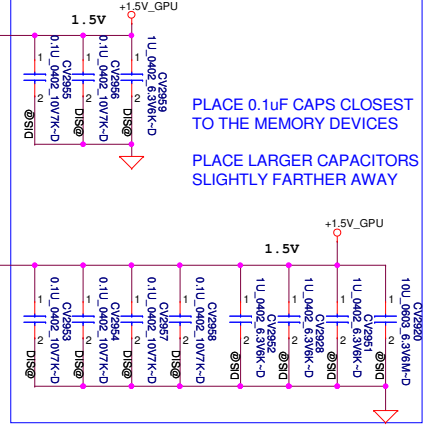
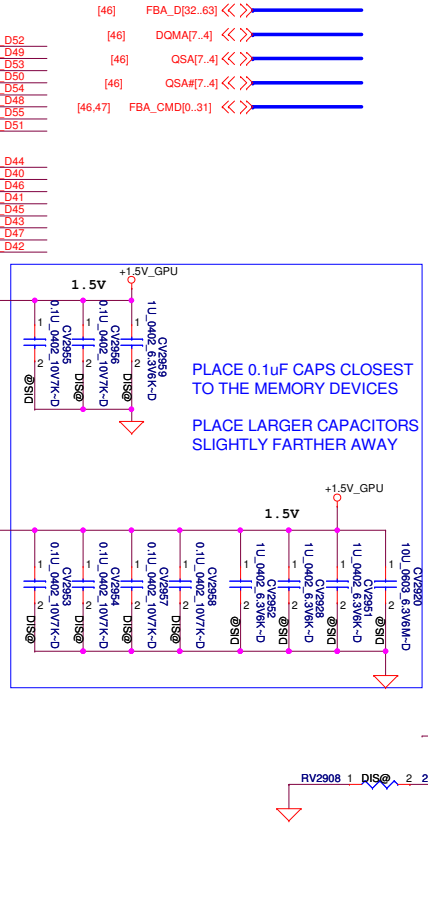
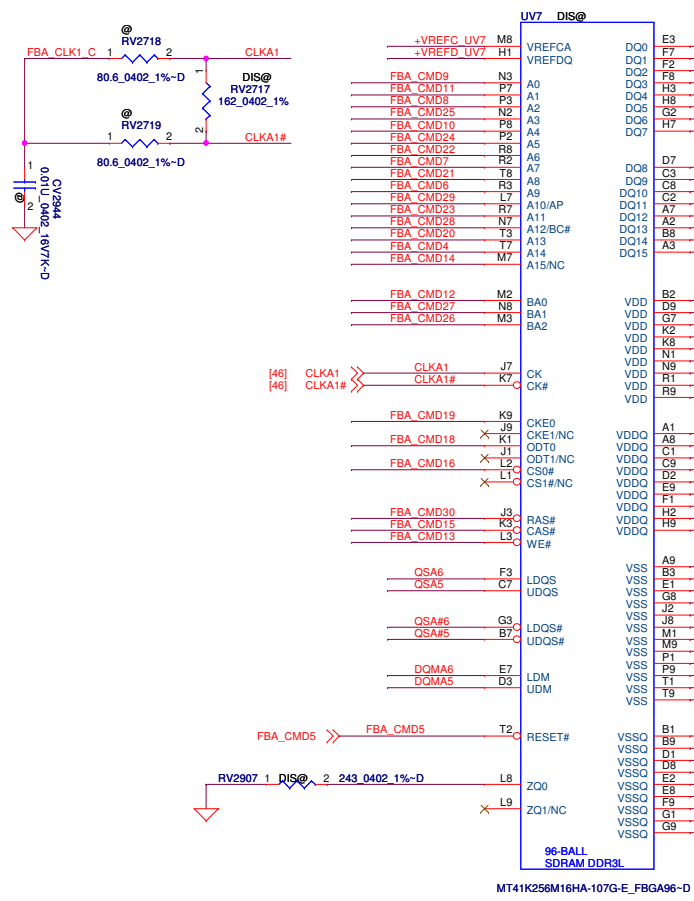
A15 is only needed if we support x8 configurations, and only at 4Gb.

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Memory Partition A - Upper 32 bits [64..32]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

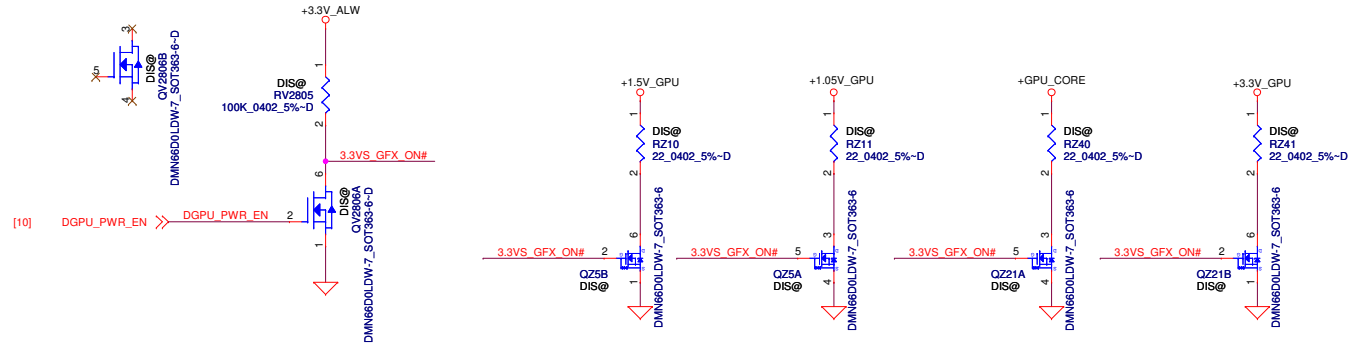
VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E



A15 is not required for any x16 device, even up to 4Gb density.
A15 is only needed if we support x8 configurations, and only at 4Gb.

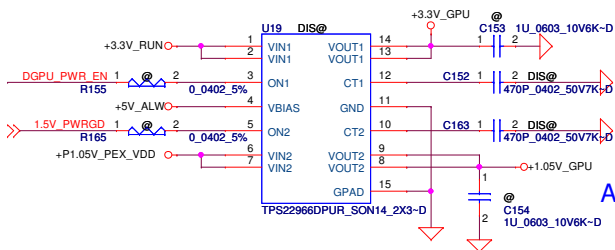
Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	VRAM DDR3 A Upper
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GPU Power Discharge Path



+3.3V_RUN to +3.3V_RUN_GFX

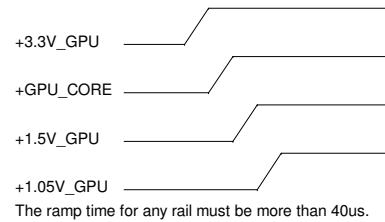
Around 1.4 A



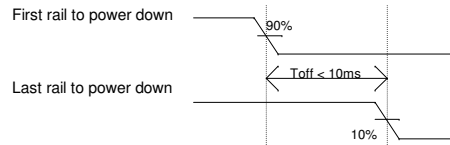
+1.05V_MP to +1.05V_PEX_VDD

Around 3 A

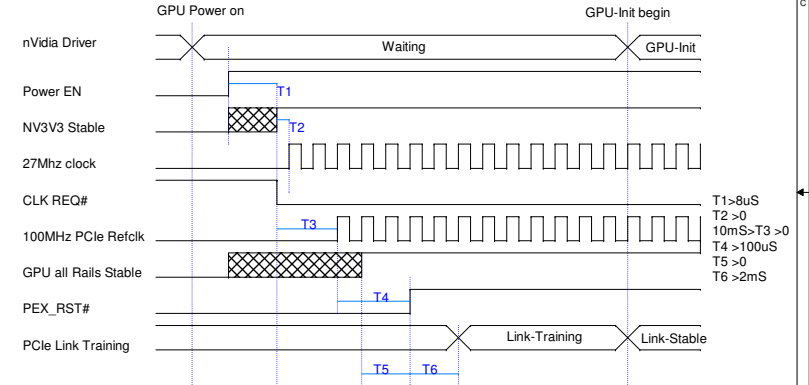
GPU Power Up Power Rail Sequence



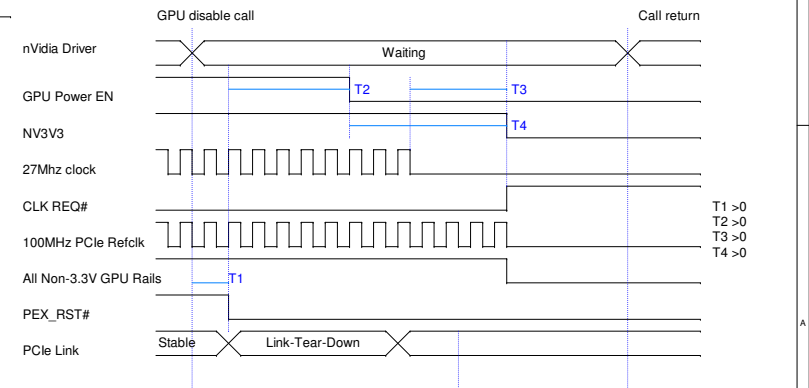
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence




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				VGA DC/DC Interface
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			Compal Electronics, Inc.	
Title		BLANK PAGE		
Size	Document Number	Rev		
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EMI (47.1)

Primary Battery Connector

37.1

EMI (47.1)

Others (37.1)
PWR support

Dell feature: ESD&EMI

PSID circuit (39.1)
Adapter Battery support
Dell feature

47.2 for ESD

Dell feature: Support dock

DC_IN+ Source

Dell feature
peak power

EMI (47.1)

37.1

Charger (40.2)

EMI (47.1)

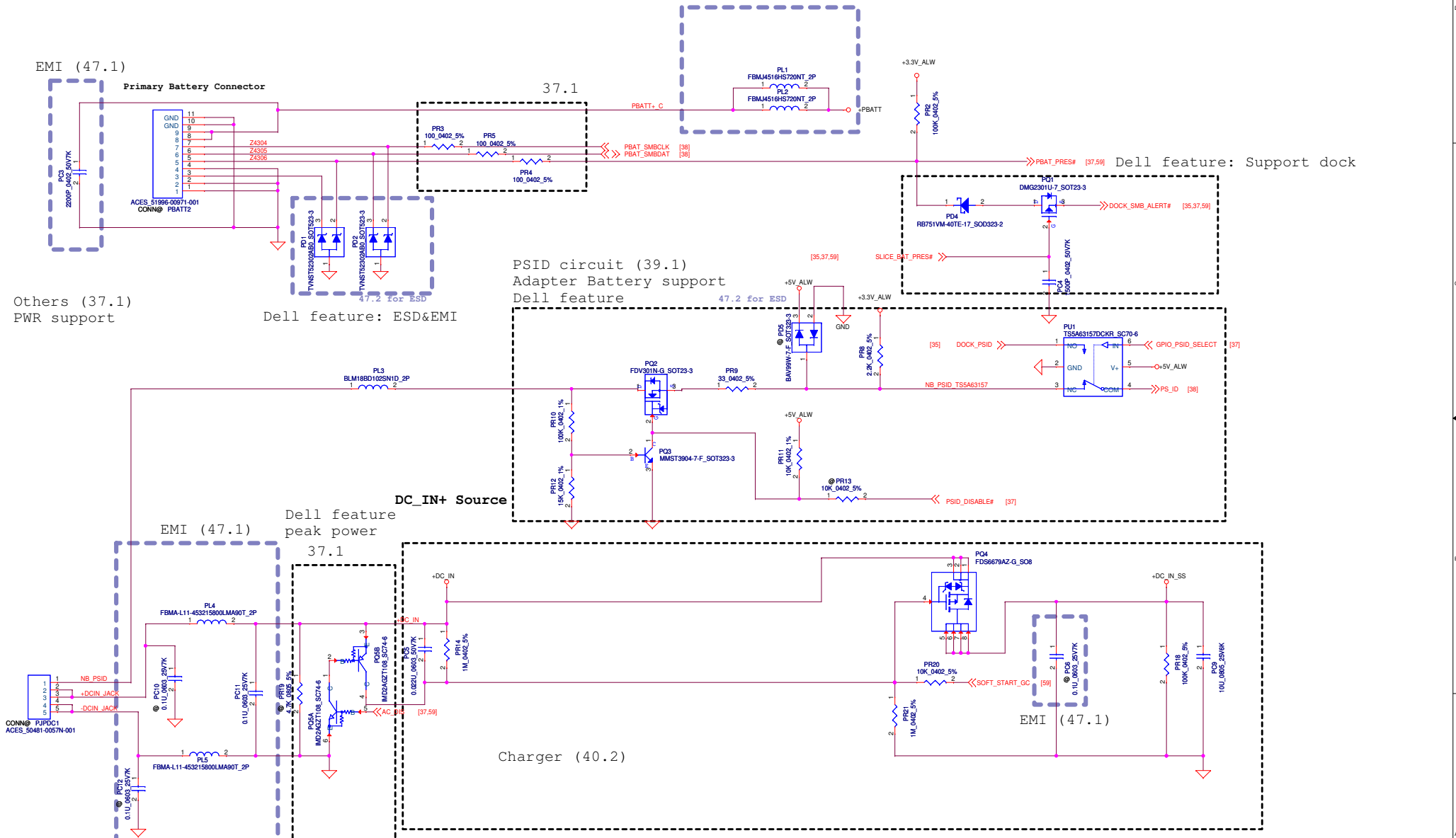
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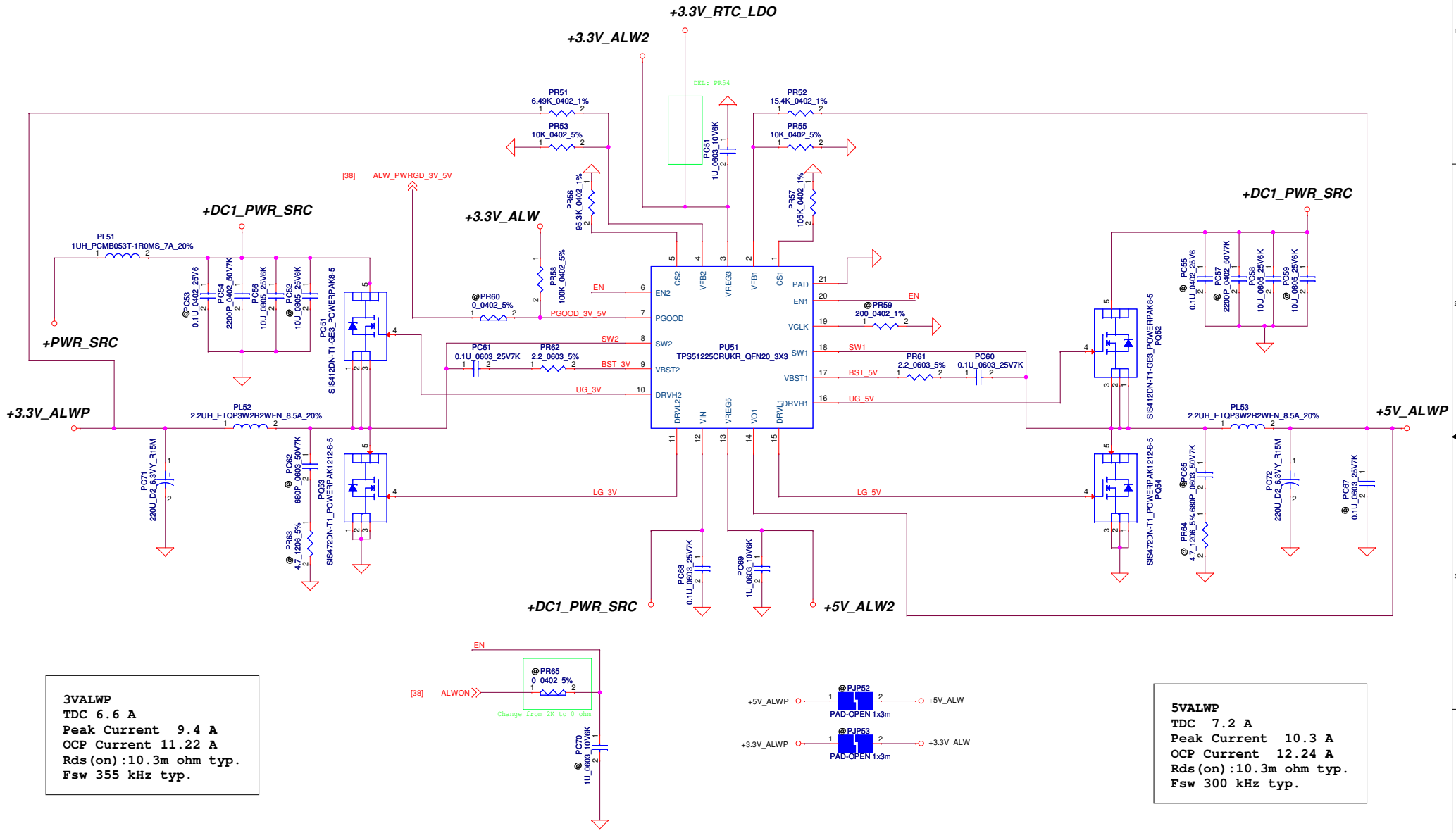
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+DCIN

Title	+DCIN		
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3VALWP
 TDC 6.6 A
 Peak Current 9.4 A
 OCP Current 11.22 A
 Rds (on) :10.3m ohm typ.
 Fsw 355 kHz typ.

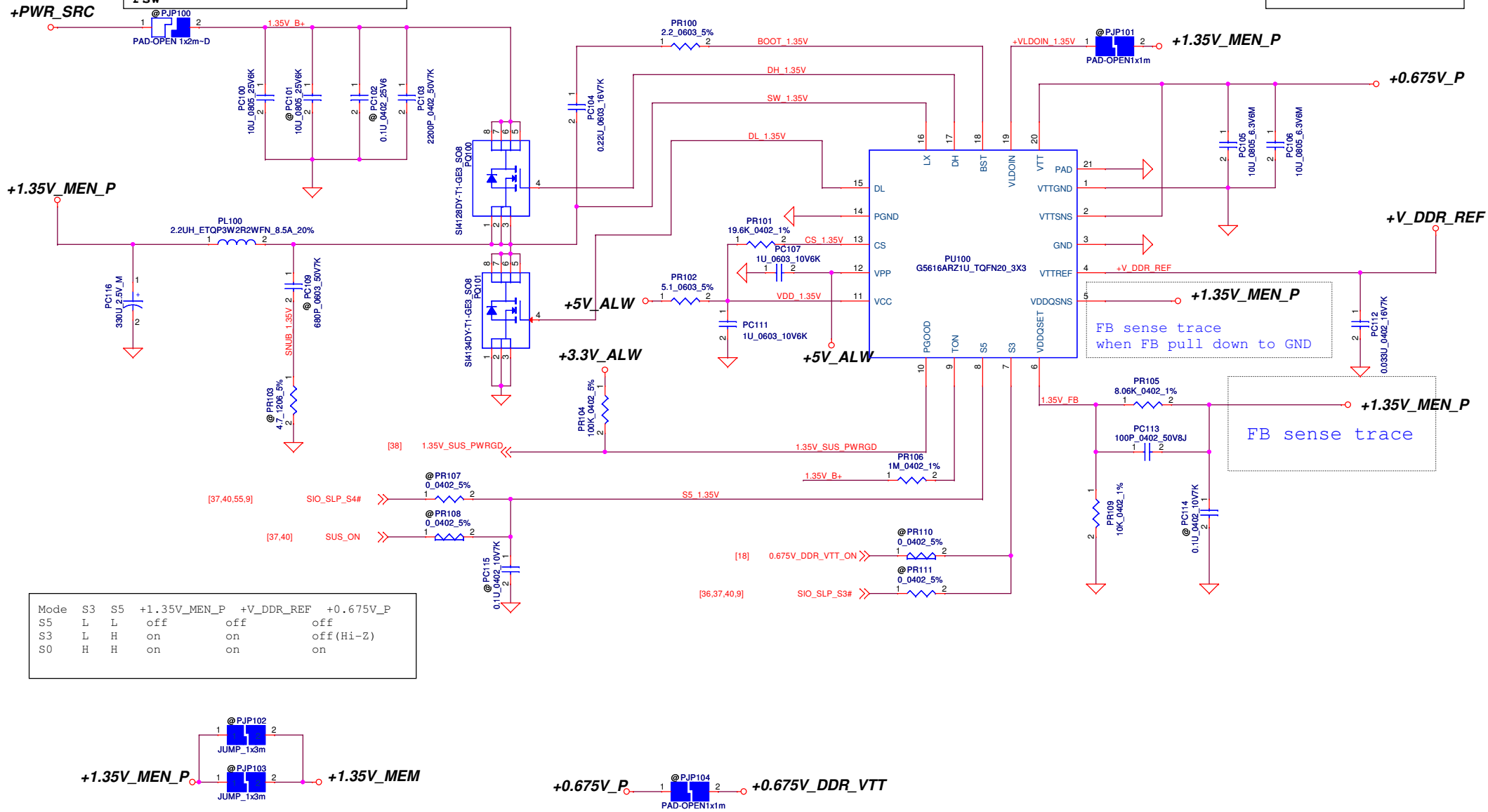
5VALWP
 TDC 7.2 A
 Peak Current 10.3 A
 OCP Current 12.24 A
 Rds (on) :10.3m ohm typ.
 Fsw 300 kHz typ.

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				Compal Electronics, Inc.	
				PWR +5V ALW/3.3V ALW	
Title					Rev
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1.35Volt +/- 5%
 TDC: 7.2 A
 Peak Current: 10.3 A
 OCP current: 12.24 A
 Rds(on) :14.5m ohm typ
 Fsw

0.675Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.8925A



Mode	S3	S5	+1.35V_MEN_P	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

FB sense trace
 when FB pull down to GND

FB sense trace



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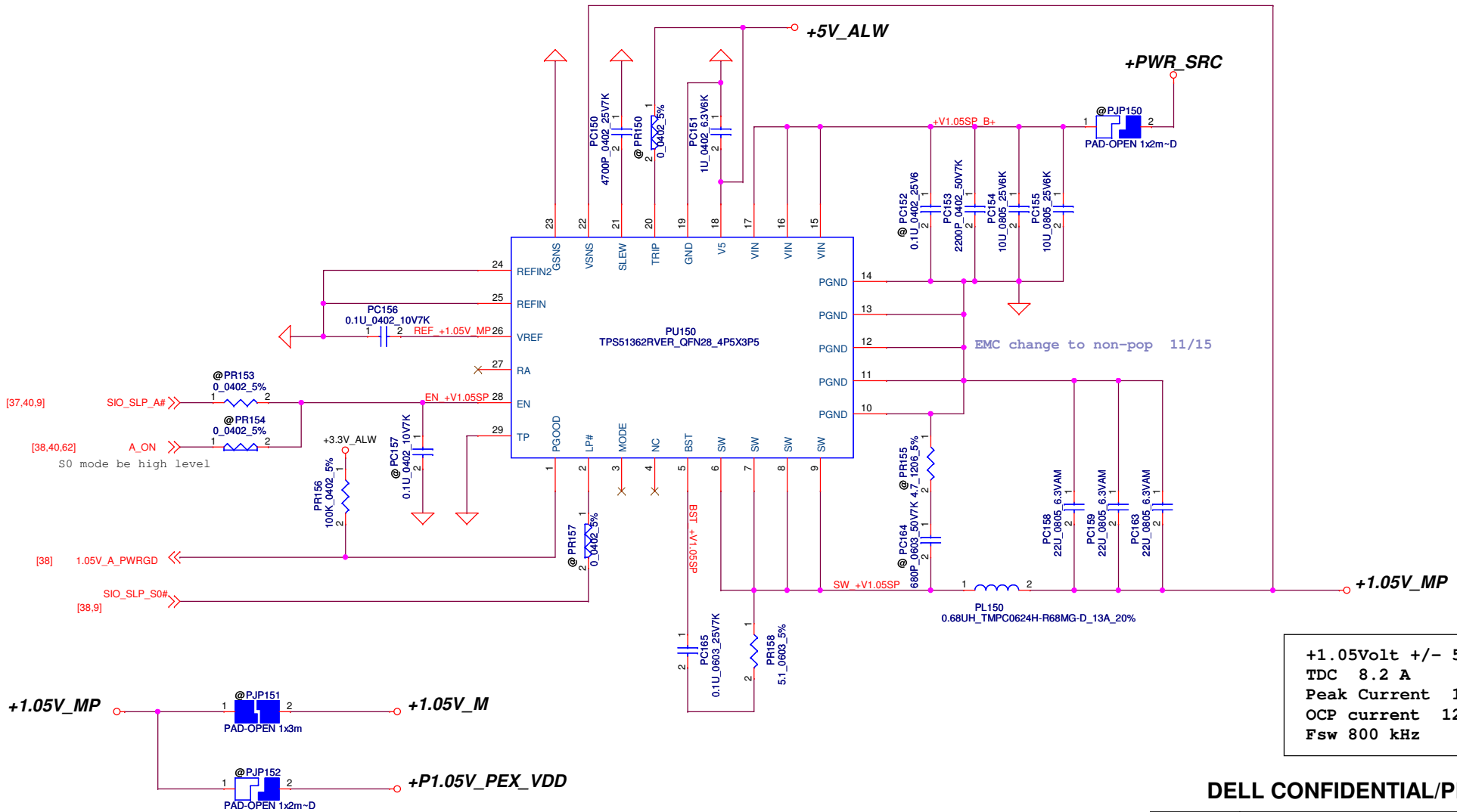
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Title: PWR +1.35V MEN/+0.675V_DDR

Size: Document Number: LA-A101P Rev: 1.0

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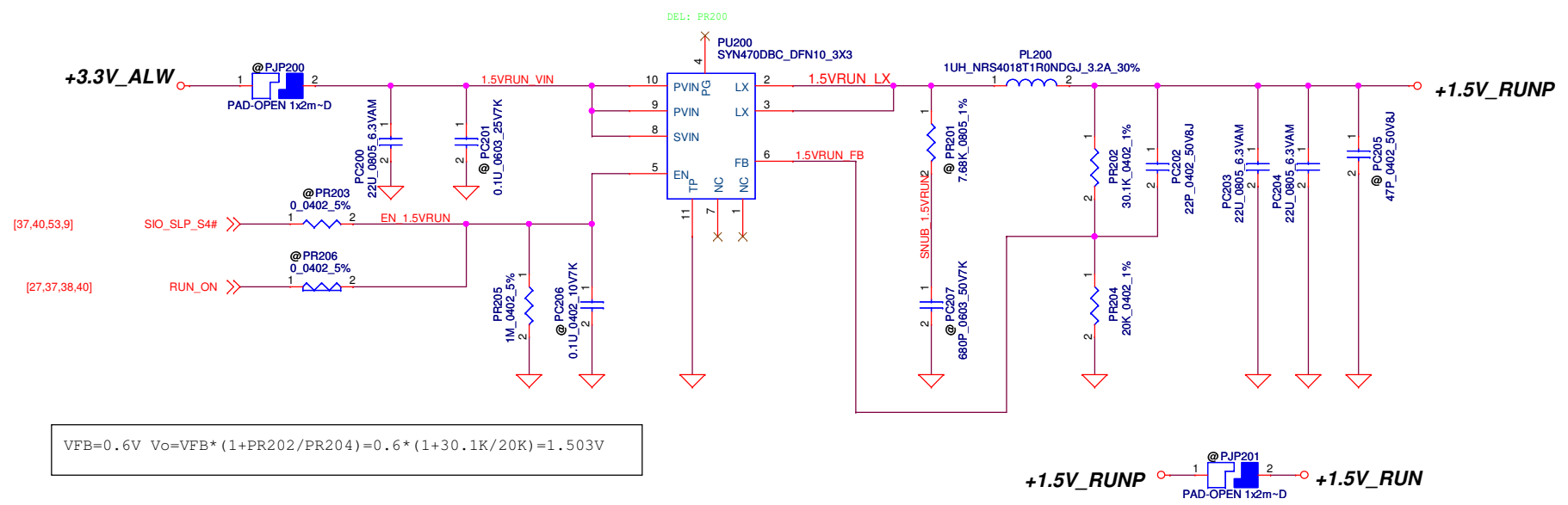
+1.05V_{olt} +/- 5%
 TDC 8.2 A
 Peak Current 11.62 A
 OCP current 12A (Fix)
 Fsw 800 kHz

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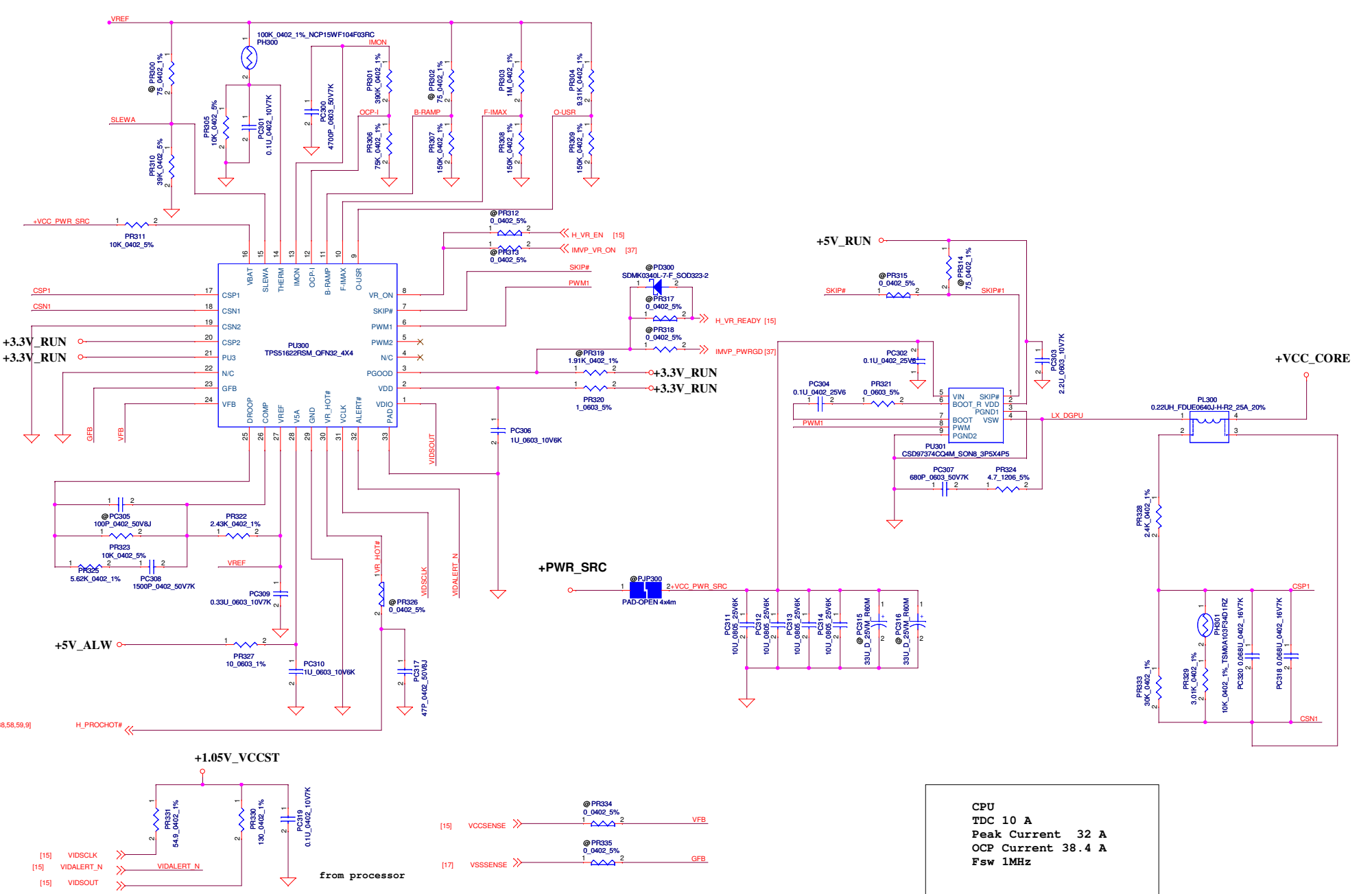
				Compal Electronics, Inc.	
				PWR +1.05VTTTP	
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1.5Volt
 Frequency 1MHz
 TDC 0.65A
 Peak Current 0.93A
 OCP current 3.5A (Fix)



$V_{FB}=0.6V$ $V_o=V_{FB} * (1+PR202/PR204)=0.6 * (1+30.1K/20K)=1.503V$

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CPU
 TDC 10 A
 Peak Current 32 A
 OCP Current 38.4 A
 Fsw 1MHz

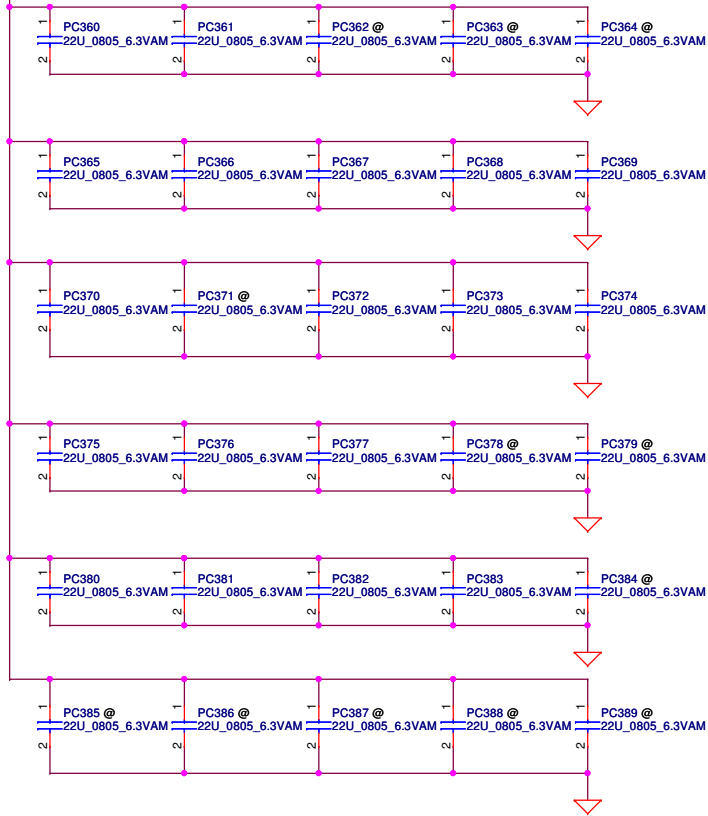
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File	PWR +VCC_CORE
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+VCC_CORE



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			Compal Electronics, Inc.	
			Title PWR PROCESSOR DECOUPLING	
Size	Document Number	Rev		
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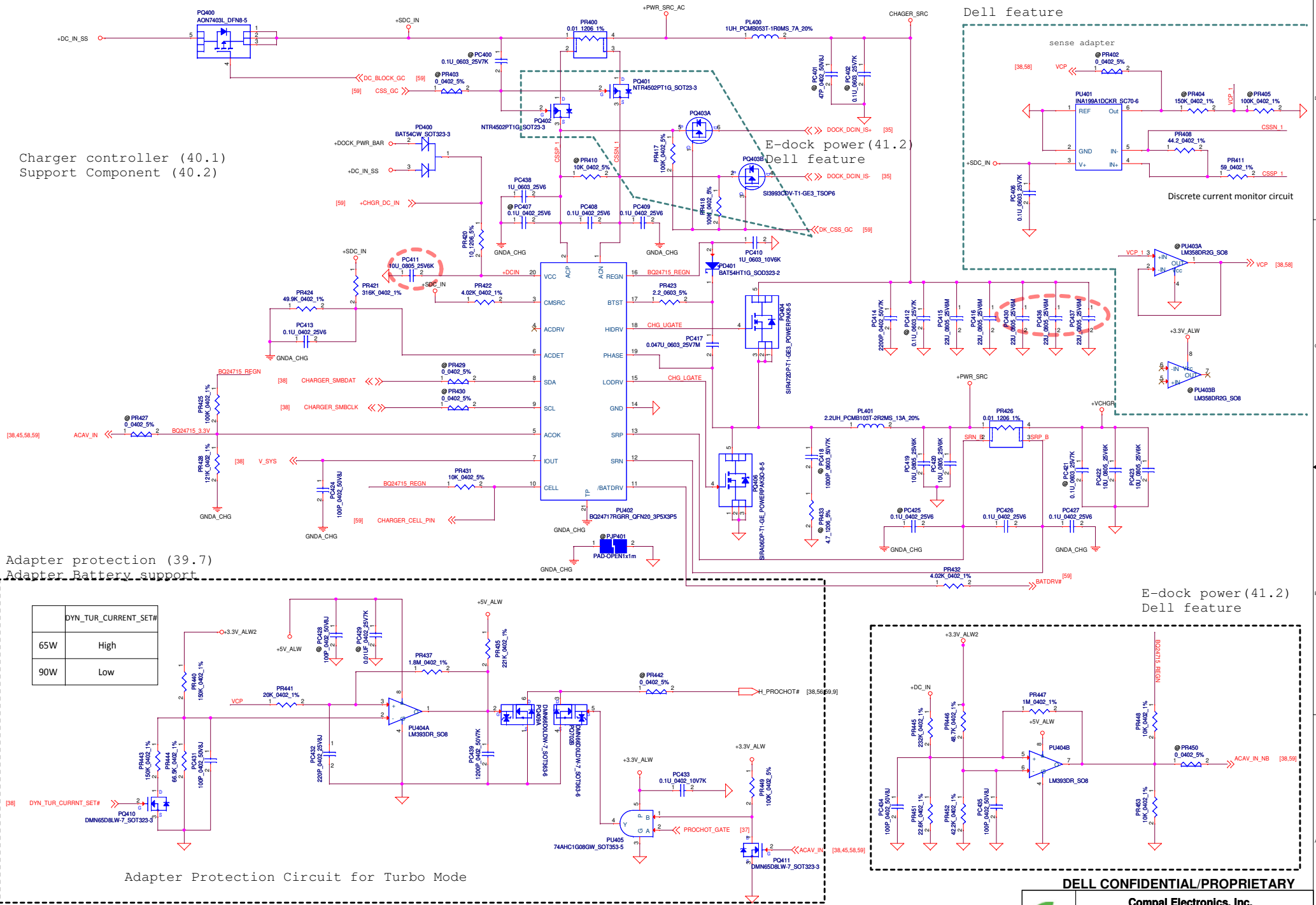
Charger controller (40.1)
Support Component (40.2)

Adapter protection (39.7)
Adapter Battery support

E-dock power (41.2)
Dell feature

Dell feature

E-dock power (41.2)
Dell feature



Adapter Protection Circuit for Turbo Mode

DYN_TUR_CURRENT_SET#	
65W	High
90W	Low

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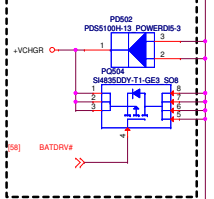
PWR Chager

LA-A101P

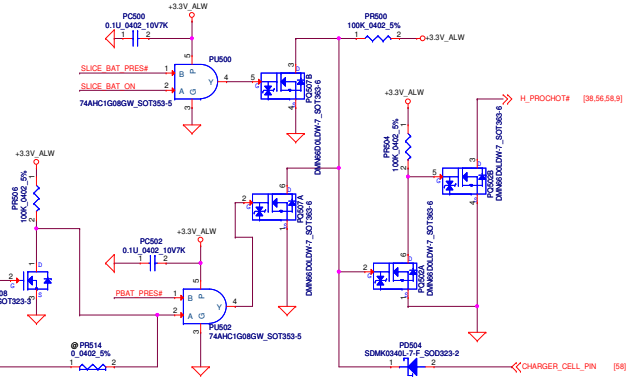
File: _____
Size: _____ Document Number: _____
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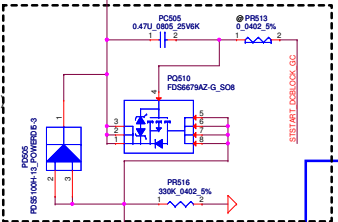
Charger (40.2)



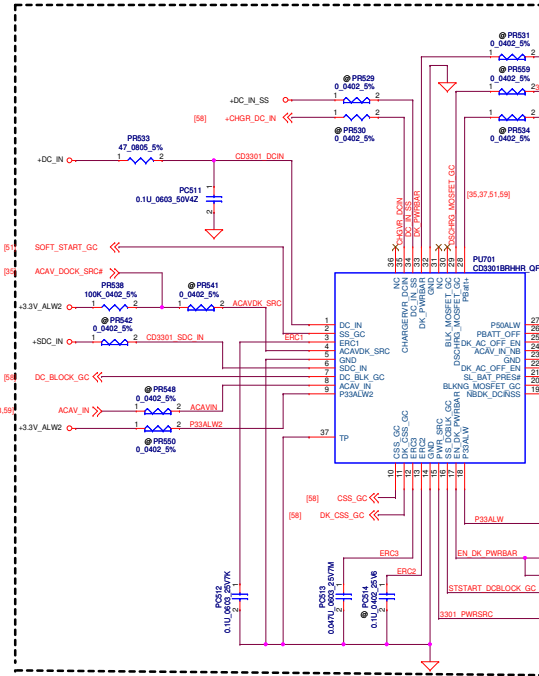
Battery select (39.3)
Dell feature



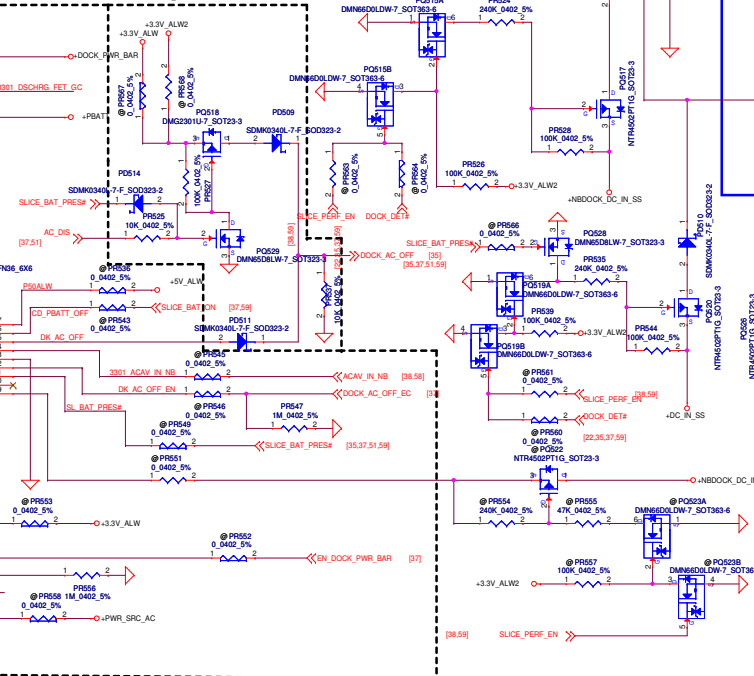
E-dock power (41.2)
Dell feature



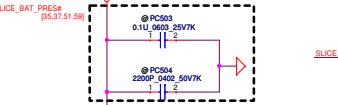
Edock controller (41.1), support component (41.2)
Dell feature



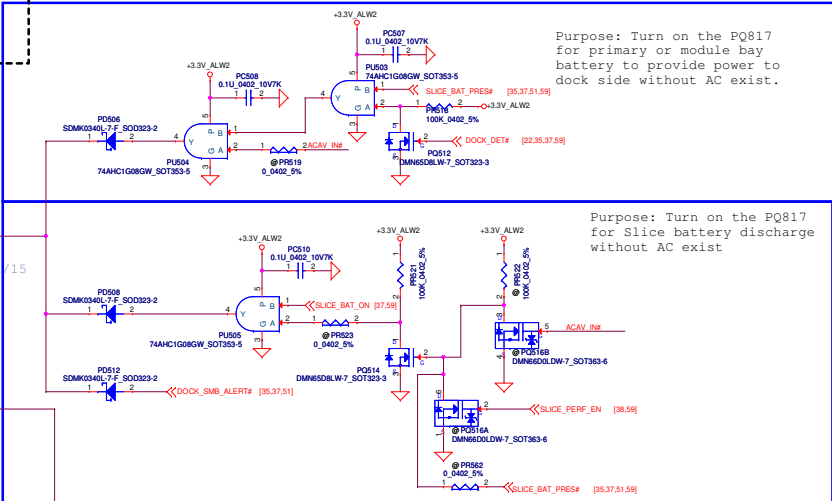
Charger (37.1)
Dell feature
Peak power



EMI (47.1)



Purpose: Turn on the PQ817 for primary or module battery to provide power to dock side without AC exist.

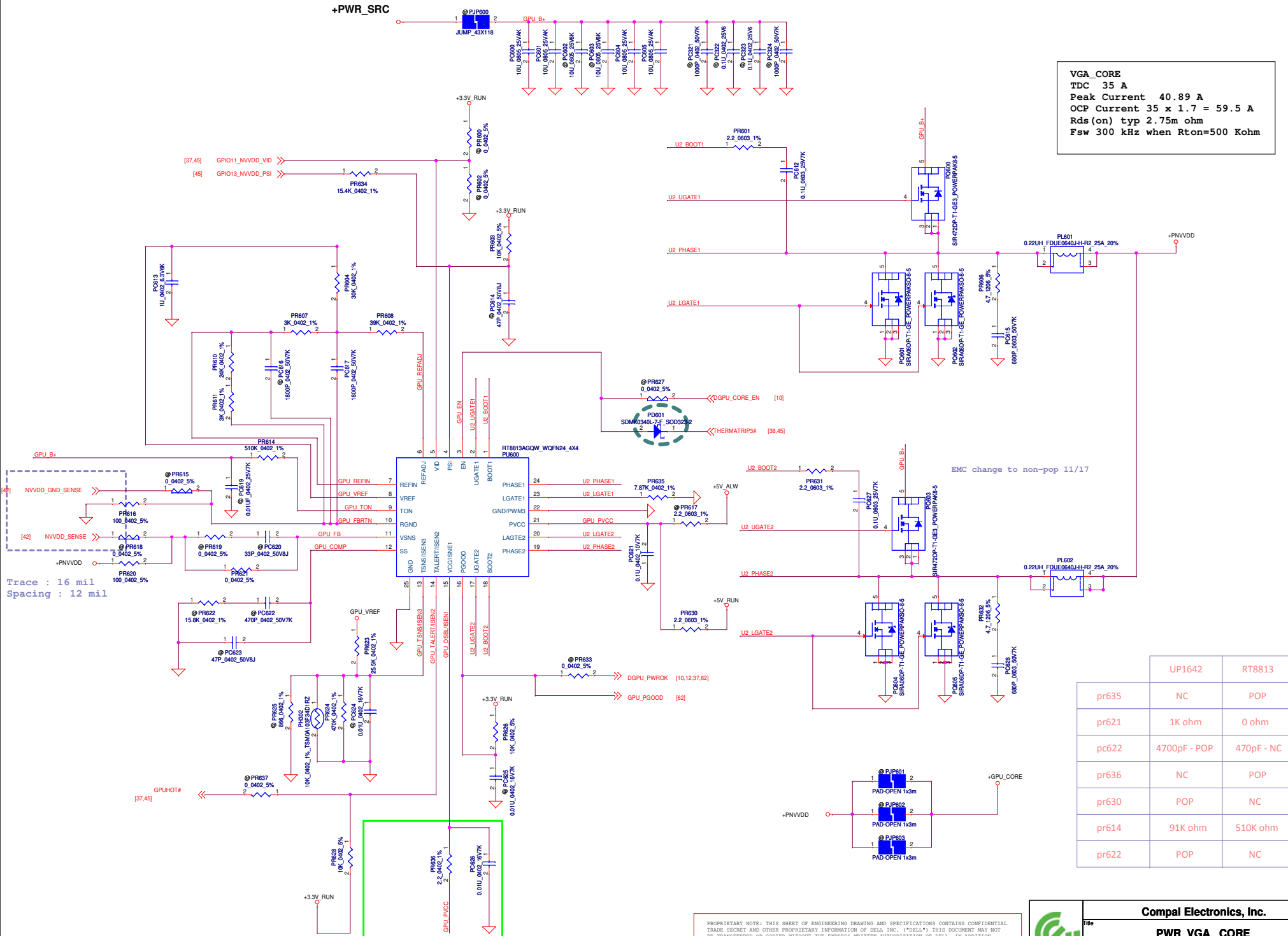


Purpose: Turn on the PQ817 for Slice battery discharge without AC exist

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+PWR_SRC

VGA_CORE
 TDC 35 A
 Peak Current 40.89 A
 OCP Current 35 x 1.7 = 59.5 A
 Rds (on) typ 2.75m ohm
 Fsw 300 kHz when Rton=500 Kohm



Trace : 16 mil
 Spacing : 12 mil

EMC change to non-pop 11/17

	UP1642	RT8813
pr35	NC	POP
pr21	1K ohm	0 ohm
pc22	4700pF - POP	470pF - NC
pr36	NC	POP
pr30	POP	NC
pr14	91K ohm	510K ohm
pr22	POP	NC

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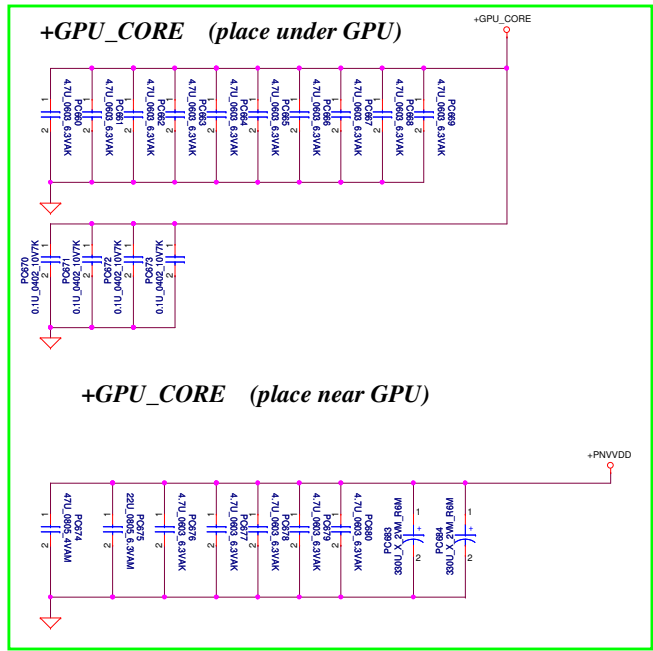
Compal Electronics, Inc.

PWR VGA CORE

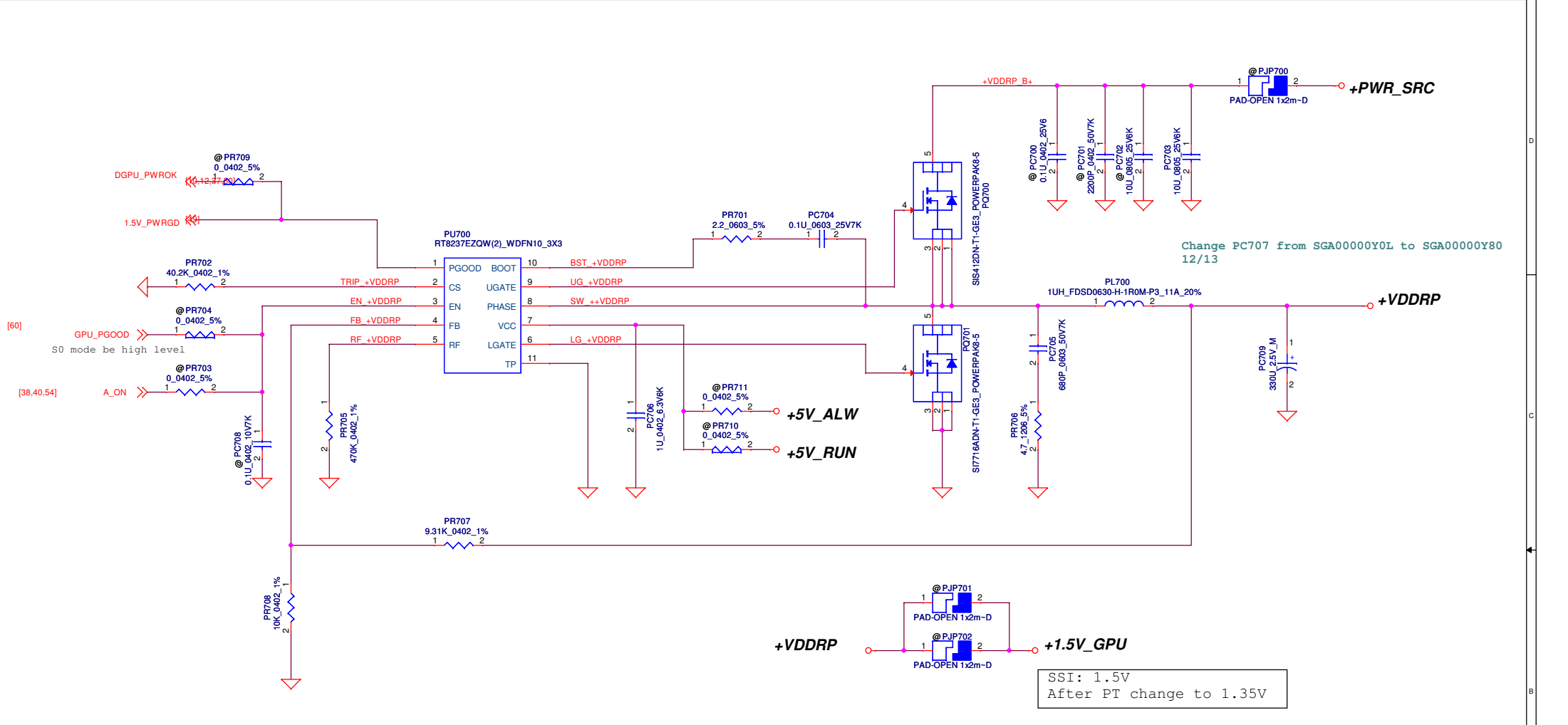
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+VDDRP (1.35V)
 TDC 2.94A
 Peak Current 4.2A
 OCP current 5A
 Rds(on) :13.5m ohm typ
 Fsw 290 kHz when Rrf=470 Kohm

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PWR +1.5VDDR		
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	58	Adapter Protection Circuit	2013/1/30	Power	PC432 220pF is not popular part	Change to 0402 size	X00
2	59	P59-PWR_Selector	2013/2/4	Power	Battery voltage leakage to docking if only battery	Add: PD513, PQ526, PR565, PR540, PQ527, PU506, PC515	X00
3	56	Vcore fine tune	2013/2/7	Power	Vcore fine tune	Modify: PR306, PR301, PR333, PR328, PR325, PR322, PL300	X00
4	57	Vcorecapacitor reduce	2013/2/7	Power	Vcore output capacitor reduce	NC: PC364, PC371, PC378, PC385, PC386	X00
5	58	Charger	2013/2/18	Power	Reserve H_PROCHOT# delay time fine tune by soft ware	Add "MODULE_BATT_PRES#" and PR454(Cancel 3/19)	X00
6	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 240K to 100K: PR503, PR528, PR544, PR565	X00
7	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 47K to 240K: PR501, PR524, PR535, PR540	X00
8	59	P59-PWR_Selector	2013/2/26	Power	SUT will unexpected shut down if un-docking during S0/S3	Add: PQ528, PR566	X00
9	51	"PBAT_PRES#" ESD fail	2013/3/4	Power	ESD PD1 fail, even connect 3.3V to VBUS pin	Change PD1 to PD1, PD2(TVNST52302AB0)	X00
10	59	P59-PWR_Selector	2013/3/6	Power	SB903380020 FDN338P derating fail	PQ500, PQ517, PQ520, PQ522, PQ526 change to SB000007900, PQ1change to SB000007900	X00
11	51	PC5 down size	2013/3/12	Power	PC5 down size	Change PC5 from 0805 to 0603 size	X00
12	51,59	AC_DIS# net change	2013/3/12	Power	AC_DIS# should high enable, not low enable	AC_DIS# change to AC_DIS	X00
13		EMC open issue	2013/3/18	Power	Add parts for EMI	PR606, PC615, PR632, PC628, PR706, PC705, PR324, PC307	X00
14	60, 62	PU600, PU601 VCC	2013/3/19	Power	DIS S3 power consumption voer 200mW	Add PR630 PR711, PR710 for reserve +5V_RUN	X00
15	61	Change DGPU output cap	2013/3/19	Power	EA test fail- 15"	Change PC683, PC684	X00
16	62	GPU DDR change to 1.35V	2013/3/19	Power	Change VDDR output voltage from 1.5V to 1.35V	Change PR707 from 11.5K to 9.1K	X00
17	54	+1.05V dynamic load test	2013/3/19	Power	+1.05V dynamic load over spec	Change PL150 from luH to 0.68uH	X00
18	58	Change output chock	2013/3/20	Power	Same as 14" for height limit	Charger output choke change to 2.2uH	X00
19	60	0 ohm resistor	2013/3/21	Power	0 ohm 1% vender is not correct in ISPD	Change PR621 0ohm from 1% to 5%	X00
20	54	1.05V dynamic over spec	2013/3/21	Power	1.05V dynamic over spec	Change PL150 from luH to 0.68uH	X00
21	59	Modify for Peak power	2013/3/21	Power	Modify schematic	PQ529, PQ518, PR527 and PR567	X00
22	52	Del +5V_ALWP output cap co-layput	2013/5/7	Power	PL52, PL53 two choke placement too closely issue.	Del PC66 and fine tune PL52/53 location	X01
23	62	DGPU DDR voltage fine tune	2013/5/10	Power	VRAM 1.35V output fine tune from 1.342V to 1.36V	PR707 change from 9.1K to 9.31K	X01
24	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
25	51	15" 組裝問題	2013/5/10	Power	PC9 short battery latch snap	Move location	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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24	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
25	51	15" 組裝問題	2013/5/10	Power	PC9 short battery latch snap	Move location	X01
26	56	15" Vcore find tune	2013/5/29	Power	14" Vcore find tune for LL and DIMON	PR322=4.53K->2.43K; non-POP:PC379, PC388; POP:PC365, PC366	X02
27	59	Selector	2013/5/30	Power	For 3V/5V volgate level, change VDS rating from 30V to 20V	PQ1, PQ518 change to 20V rating DMG2301U-7_SOT23-3	X02
28	62	Thermal de-ratgin issue	2013/5/29	Power	MLCC are exceeded derating criteria (75C)	Change to X6S/X7R: PC600, PC601, PC604, PC605, PC674	X02
29	59	Change part number	2013/6/6	Power	Part number ~NO is for other customer	SE043474KN0 change to SE043474K80	X02
30	NA	15" NPI report request (,6/6)	2013/6/7	Power	Component pad too small	PL100/PL52/PL53/PL150 pad ?度change from 8 to 8.4mm	X02
31	NA	15" NPI report request (,6/6)	2013/6/7	Power	Co-lay need select 1 component	Del NC: PC681, PC682, PJP1, PL301, PC707, PC110, PC64, PJP400, PL600, PJP51	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	27	Change to bead	2013/08/02	EMI	Populate bead 70 ohm(BLM15AG700SN1) on R137 and R139		1.0
2	27	音壓測試fail	2013/08/02	Safety	R162 , R166 change from 9.1 ohm to 18 ohm		1.0
3	9, 44	Change to short-pad	2013/08/02	EE	Location : RC194,RC204,RC208,RC209, RV2404		1.0
4	28	Change CPN	2013/08/02	EE	Type change to T & R	SA000066W4L	1.0
5	34	USB3.0 Re-driver	2013/08/02	EE	Pull-up and Pull-down resistor	R2628, R2629, R2630, R2631, R2633, R2634, R2635, R2636, R2637, R2644	1.0
6	18, 19 31	Del Cap	2013/08/02	EE	Delete Co-Lay cap	C810, CD100, CD101	1.0
7	25	Modify footprint	2013/08/14	EE	Location : JSATA1	NPI	1.0
8	41	銅柱 Size	2013/08/22	EE	Location : H1, H2, H3, H4, H5, H6		1.0
9	16	BT issue	2013/08/22	EE	Add 0.47uF between "+PCH_VCCDSW3_3" and "+PCH_VCCDSW"	C413	1.0
10	36	EMI Request	2013/08/22	EMI	Add D2 on "Sleeve" & "Ring2" and connect to DGND		1.0
11	41	LED resistor	2013/08/22	EE	Change to 300 ohm	R429, R433, R436, R438, R436	1.0
12	41	POWER BOTTON		EE	Un-pop power botton.	SW6	1.1

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