

Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-04

REV : A00

DY :None Installed

UMA:UMA ONLY installed

DN15: ONLY FOR DN15 installed.

DQ15:ONLY FOR DQ15 installed.

PSL: KBC795 PSL circuit for 10mW solution installed.

10mW: External circuit for 10mW solution installed.

MUXLESS:MUXLESS solution installed.

OPTIMUS:OPTIMUS solution installed.

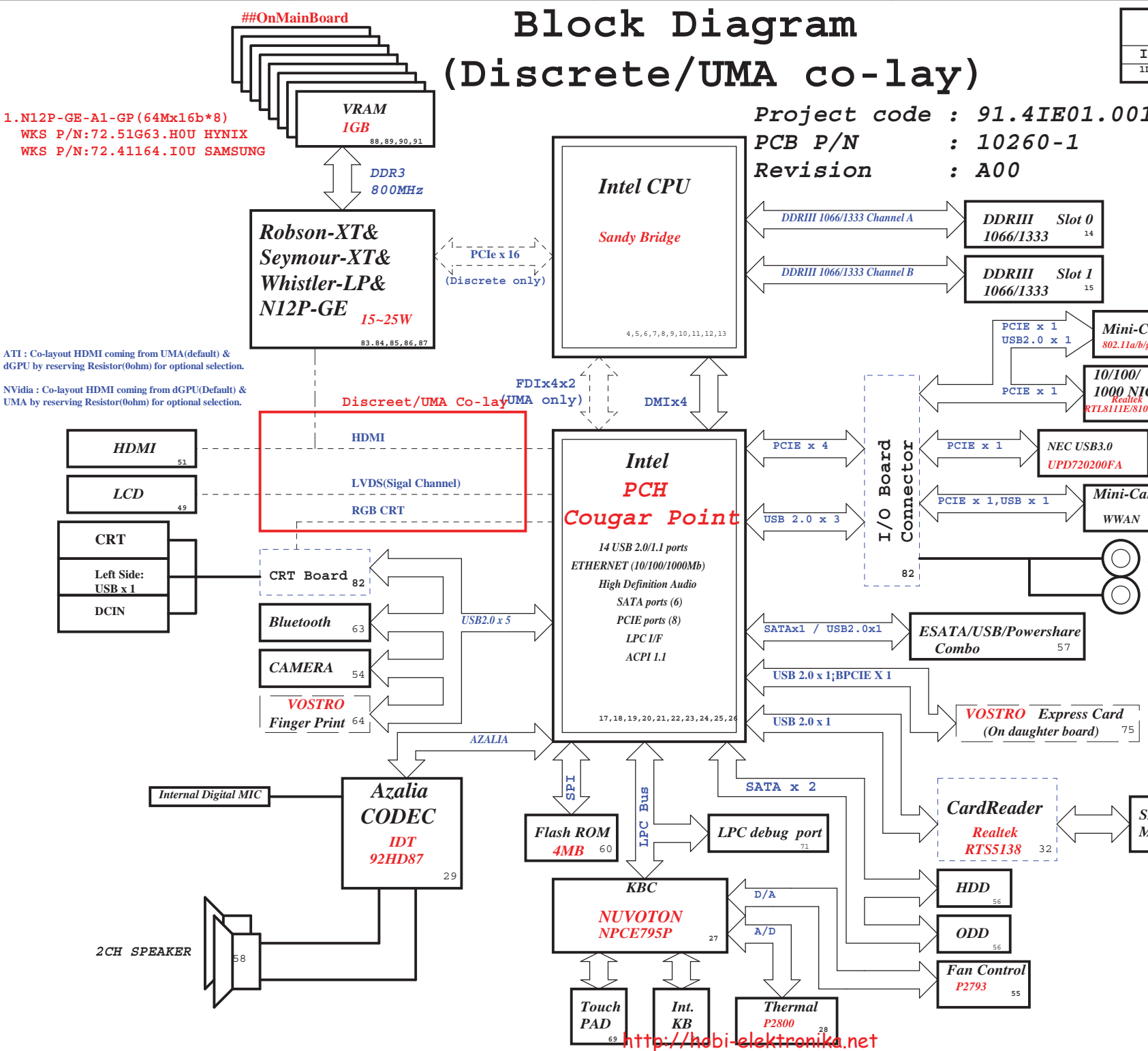
<Core Design>



Title			Cover Page		
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Block Diagram (Discrete/UMA co-lay)

SYSTEM LDO APL5916 48		CPU DC/DC ISL95831HRTZ 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0	DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51218 45		SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT	DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC TPS51216RUKR 46		SYSTEM DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	DCBATOUT	VCC GFXCORE
VGA RT8208B 92		TI CHARGER BQ24745 40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC TPS51311 47		SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_S0	1D5V_S3	1V_VGA_S0
Switches			
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0	1D5V_S0 5V_S0 3D3V_S0	3D3V_S0
PCB LAYER			
L1:Top	L4:Signal	L2:VCC	L5:GND
L3:Signal	L6:Bottom		



Project code : 91.4IE01.001
PCB P/N : 10260-1
Revision : A00

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kf[- 10-kf[weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

PCIE Routing

LANE1	Card Reader
LANE2	Mini Card1 (WLAN)
LANE3	Mini Card2 (WWAN)
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	Express Card

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is 0: connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB		
		Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

Variant Names

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

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<http://hobi-elektronika.net>

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

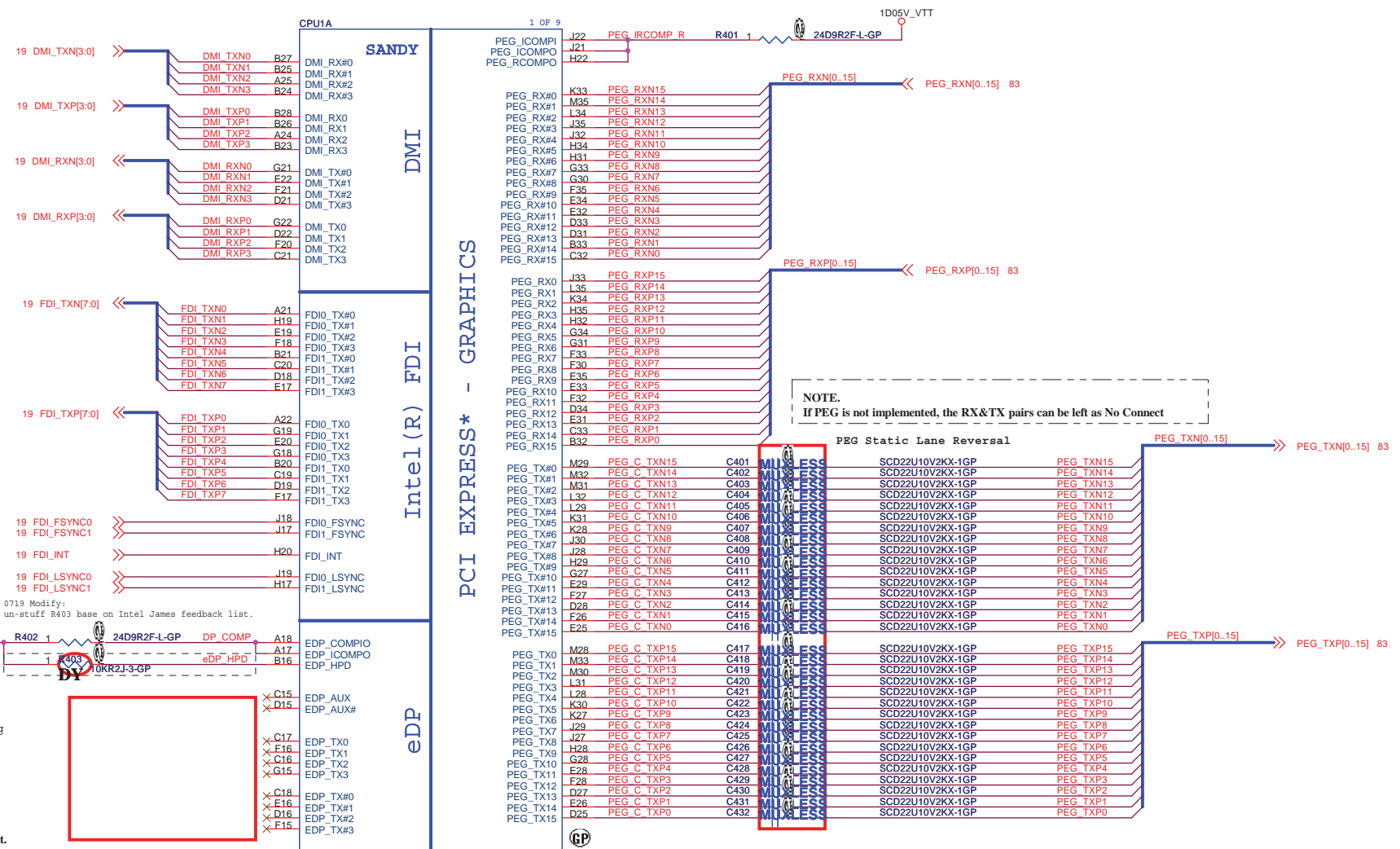
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-k Ω pull-Up resistor on the motherboard.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



NOTE:
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

<Variant Name>

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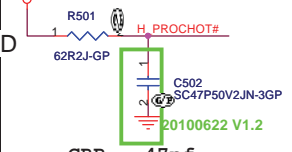
Title: **CPU (PCIe/DMI/FDI)**

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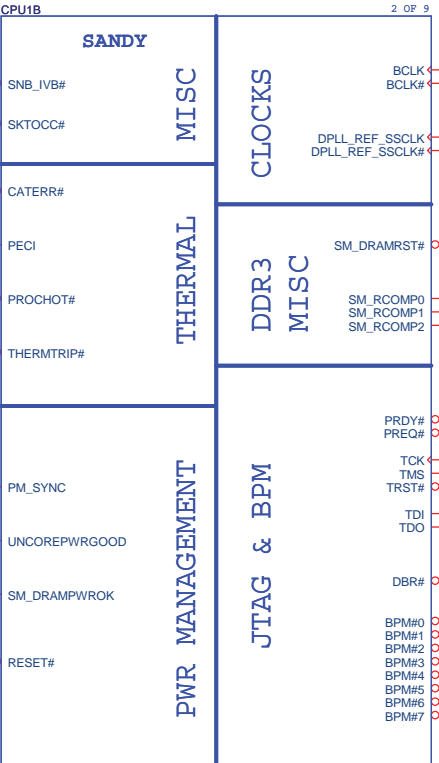
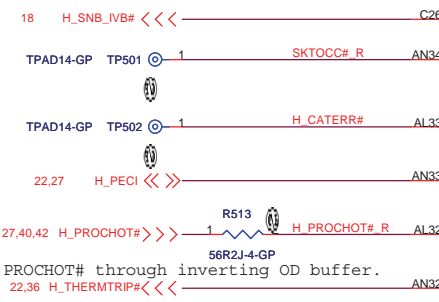
SSID = CPU

0625 Modify: Add C502 47pF 0402 on H_PROCHOT#.



CRB : 47pf
CEKLT: 43pf

Connect EC to PROCHOT# through inverting OD buffer.

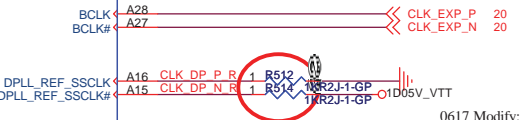
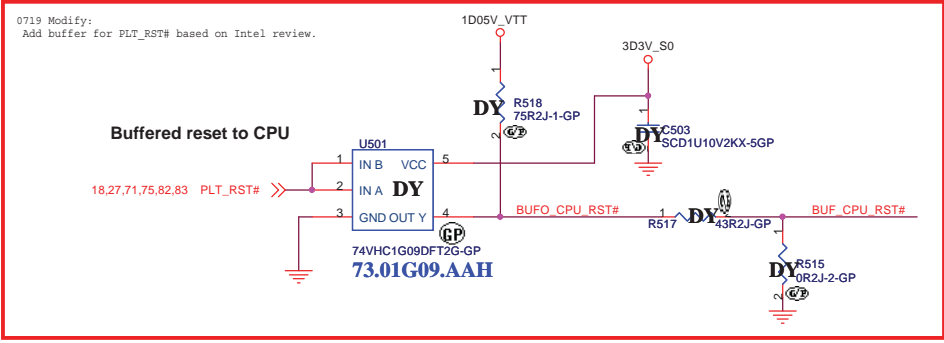


SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

0617 Modify: Joseph Removed U501 Buffer reset to CPU circuit.

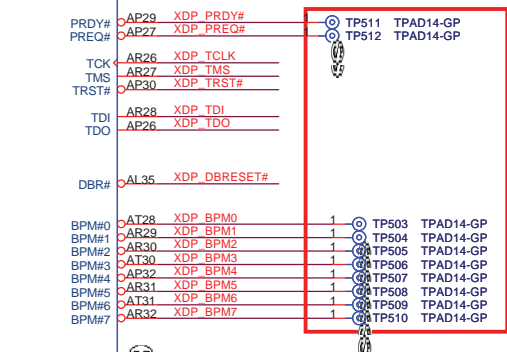
0719 Modify: Add buffer for PLT_RST# based on Intel review.



0617 Modify: Joseph change RN501 to R512.R514 1K 0402 Resistor.

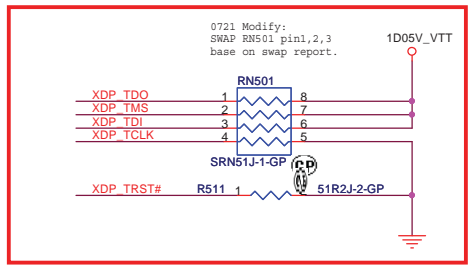


Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

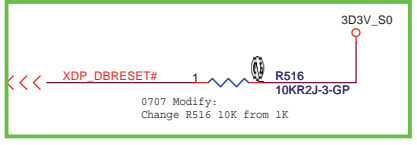


0630 Modify: Removed XDP1101 connector related circuit by layout limitation.

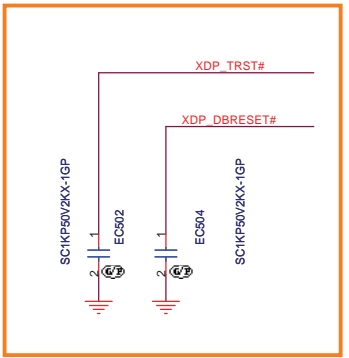
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor power (~15 mW) may be wasted.



0721 Modify: SWAP RN501 pin1,2,3 base on swap report.



0707 Modify: Change R516 10K from 1K

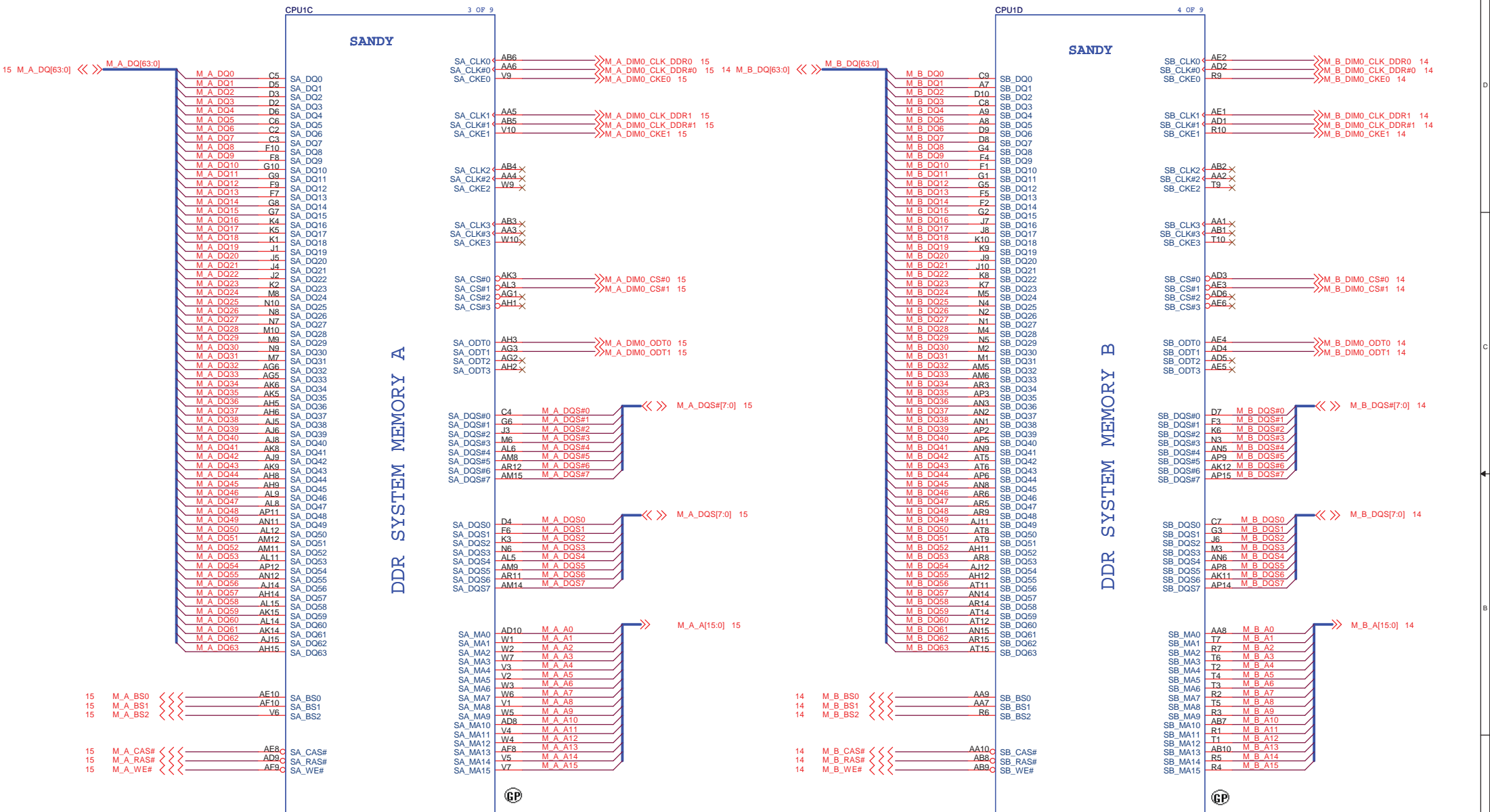


A00 1229 EMI

<Variant Names>

Dell Wistron Corporation logo and address. Title: CPU (THERMAL/CLOCK/PM). Size A3, Document Number QUEEN 15, Rev A00. Date: tuesday, January 04, 2011. Sheet 5 of 108.

SSID = CPU



SANDY
62.10055.421
 2nd = 62.10040.771
 3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

SANDY
62.10055.421
 2nd = 62.10040.771
 3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

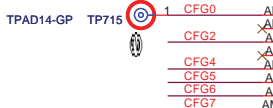
<Variant Names>



Title CPU (DDR)		
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SSID = CPU

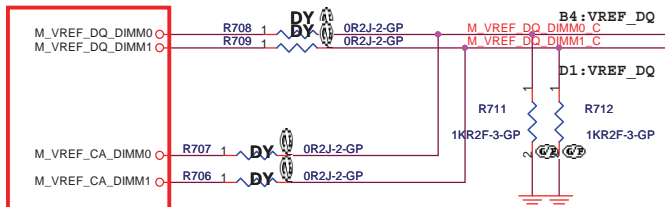
0630 Modify:
Reserved TP715 on CFG0.



0707 Modify:
Removed CFG1, CFG3, CFG8-17 TP.

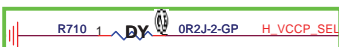
0617 Modify:
Joseph Change M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1, M_VREF_CA_DIMM0, M_VREF_CA_DIMM1 from net to power.

M3 - Processor Generated SO-DIMM VREF_DQ



20 mils

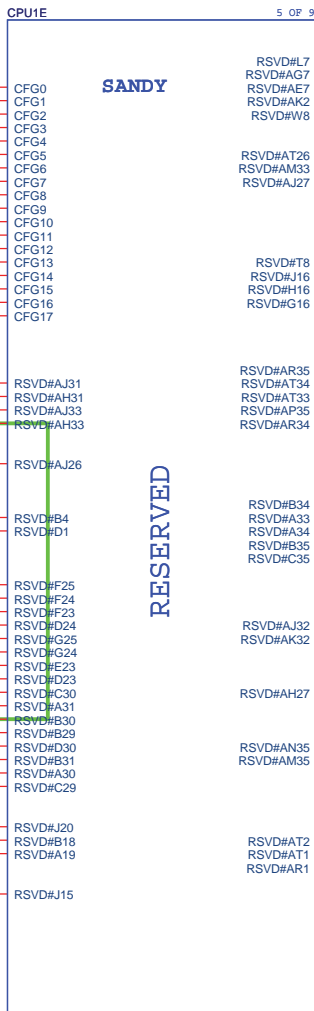
0629 Modify:
Reserved R710 0ohm to GND to follow EV board schematic.



1D05V_VTT



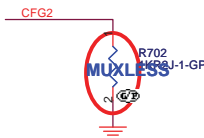
0719 Modify:
Reserved EC701 0.1uF near R711(BOTTOM) for EMC NEO suggestion.



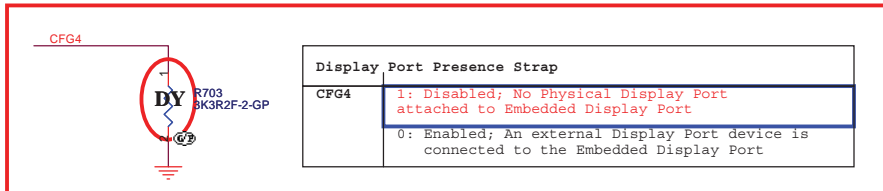
RESERVED

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771
3rd = 62.10055.321

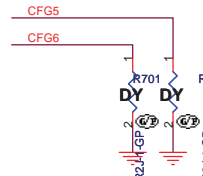
A00 0103 add 3rd foxconn CPU1 at XBuild batch run



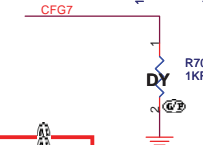
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
	00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEPER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

0702 Modify:
Removed CLK_XDD ITP PaN and reserved TP713, TP714.



0630 Modify:
Removed CLK_XDD ITP PaN and reserved TP713, TP714.

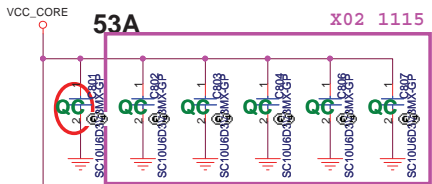
<Variant Name>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (RESERVED)			
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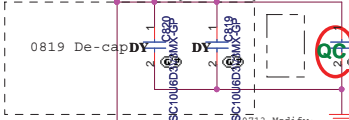
Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

1115 X02 Modify:
Reserved C802-C804, C806, C807 10uF 0603
for power team fine tune Vcore quality.

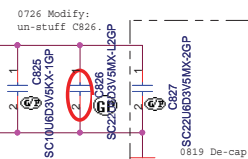
PROCESSOR CORE POWER



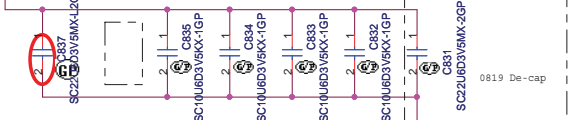
0713 Modify:
Removed C802, C811 10uF 0603
cap base on layout limitation.



0713 Modify:
Removed C818 10uF 0603
base on layout limitation.



0721 Modify:
Removed C822, C823, C824



0726 Modify:
un-stuff C837.

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

- VCC_CORE
- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
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- R2 VCC
- R1 VCC
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- P28 VCC
- P27 VCC
- P26 VCC

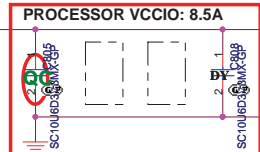
CORE SUPPLY

SVID

SENSE LINES

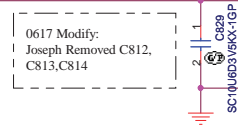
PEG AND DDR

- VCCIO AH13
- VCCIO AH10
- VCCIO AG10
- VCCIO AG10
- VCCIO Y10
- VCCIO L10
- VCCIO P10
- VCCIO J14
- VCCIO J14
- VCCIO J13
- VCCIO J12
- VCCIO J11
- VCCIO H14
- VCCIO H12
- VCCIO H11
- VCCIO G14
- VCCIO G13
- VCCIO G12
- VCCIO F14
- VCCIO F13
- VCCIO F12
- VCCIO F11
- VCCIO E14
- VCCIO E12
- VCCIO E11
- VCCIO D14
- VCCIO D13
- VCCIO D12
- VCCIO D11
- VCCIO C14
- VCCIO C13
- VCCIO C12
- VCCIO C11
- VCCIO B14
- VCCIO B12
- VCCIO A14
- VCCIO A13
- VCCIO A12
- VCCIO A11
- VCCIO J23



0713 Modify:
Removed C810, C806, C807 10uF 0603
base on layout limitation.

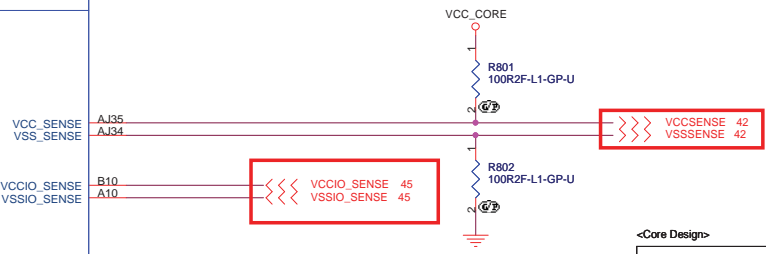
No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.



For CRB VIDSOUT need to pull high 130 ohm closer to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



0705 Modify:
Removed R805, R806, already PH closed PWM side.



<Core Design>



Title			CPU (VCC CORE)		
Size	Document Number	Rev			
Custom	QUEEN 15	A00			
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SSID = CPU

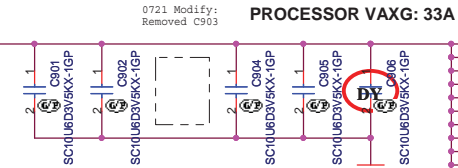
VAXG Output Decoupling Recommendation:

- 2 x 470 uF at Bottom Socket Edge
- 2 x 22 uF at Top Socket Cavity
- 4 x 22 uF at Top Socket Edge
- 2 x 22 uF at Bottom Socket Cavity
- 4 x 22 uF at Bottom Socket Edge

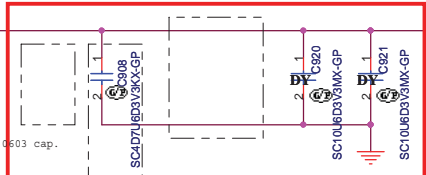
0726 Modify:
un-stuff C906.

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

VCC_GFXCORE



0624 Modify:
Removed C918,C919 10uF 0603 for VCC_GFXCORE.



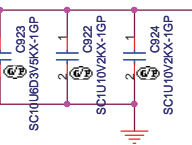
0713 Modify:
Removed C907 10uF 0603 cap.
0726 Modify:
stuff C908 10uF.

Removed DIS_ONLY Disable Resistor.
R904,R905,R901,R903

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A



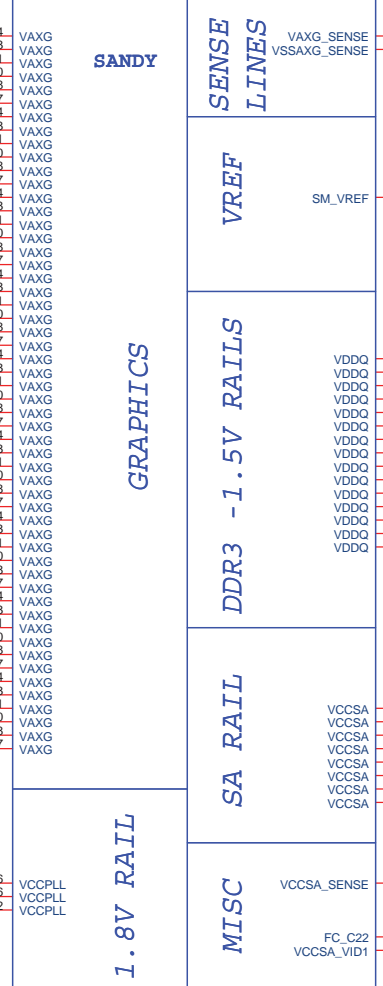
0617 Modify:
Joseph Removed TC902,
TC903 330uF cap.

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

POWER

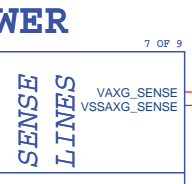
CPU1G

7 OF 9



SANDY
62.10055.421
2nd = 62.10040.771
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

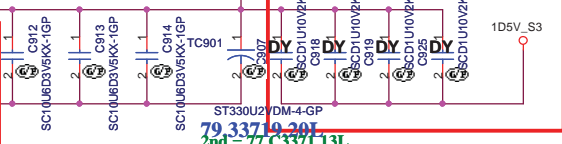
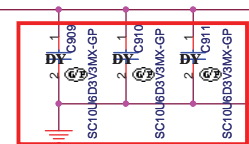


Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.
+V_SM_VREF_CNT should have 10 mil trace width



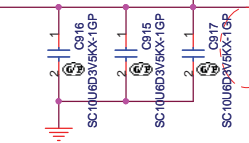
Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

PROCESSOR VDDQ: 10A



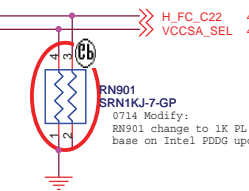
VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

PROCESSOR VCCSA: 6A

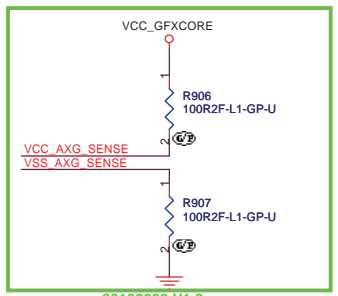


0617 Modify:
Joseph Removed TC902,TC903 330uF cap.
0719 Modify:
Reserved EC902 0.1uF near C917 for EMC NEO suggestion.
VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0624 Modify:
Removed R902 10ohm closed CPU side.
0713 Modify:
Add R908 100ohm PH to 0D85V_S0.
0714 Modify:
Removed R908 PH.



1122 X02 Modify:
stuff EC901 0.1uF from EMC Neo suggestion.



20100609 V1.0

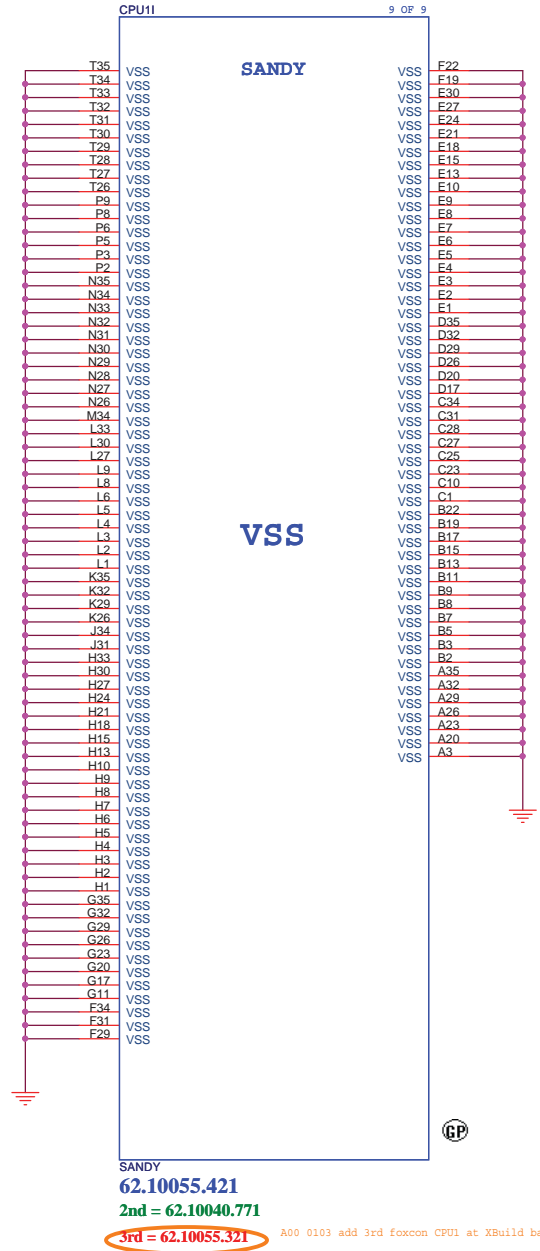
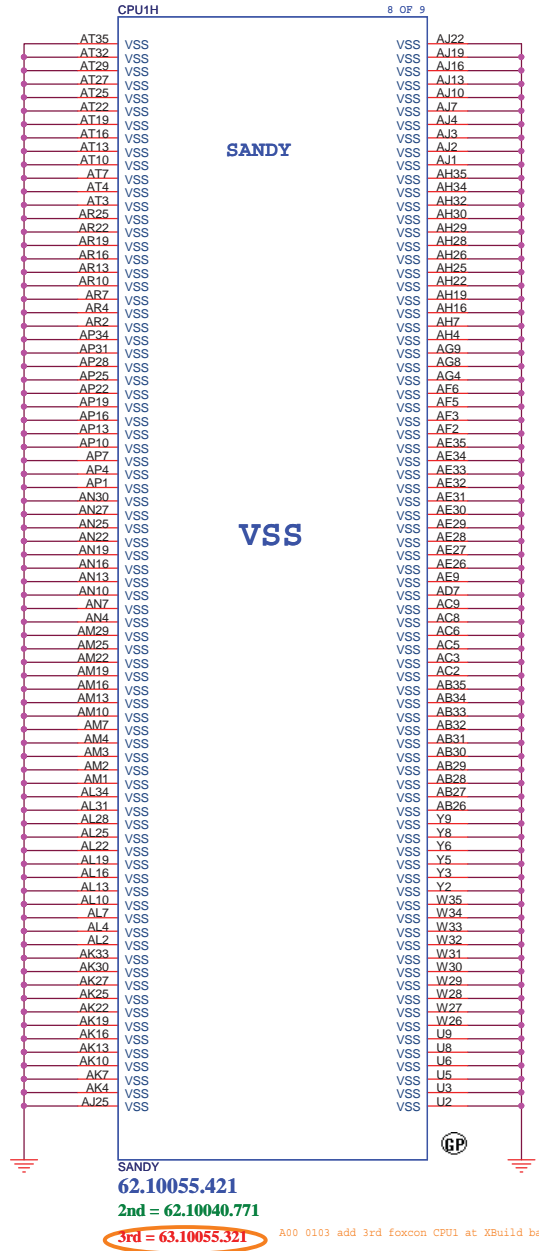
0719 Modify:
Add C907,C918,C919,C925 0402 0.1 uF stitching capacitors between 1D5V_S3 & 1D5V_S0 based on Intel's review

<Core Design>



Title			CPU (VCC GFXCORE)		
Size	Document Number	Rev			
A3	QUEEN 15	A00			
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SSID = CPU



<Variant Name>

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet: 10	of 108


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<Variant Name>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
XDP		
Size	Document Number	Rev
A3	QUEEN 15	A00
Date:	Tuesday, January 04, 2011	Sheet 11 of 108


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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet 12	of 108

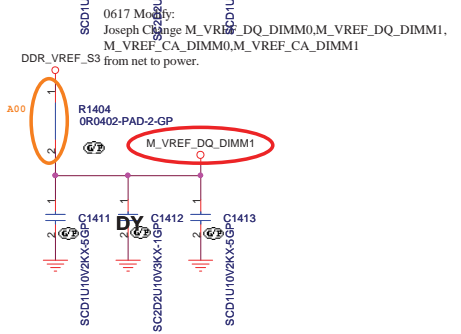
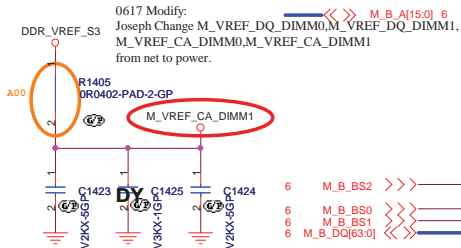
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<Core Design>

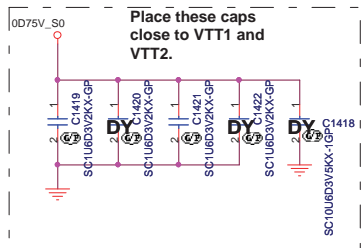
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet 13	of 108

SSID = MEMORY

0624 Modify: SWAP DM1 and DM2 location.



0707 Modify: Change R1404, R1405 to 0ohm G402 from short pad.



M_B A0	98	A0
M_B A1	97	A1
M_B A2	96	A2
M_B A3	95	A3
M_B A4	92	A4
M_B A5	91	A5
M_B A6	86	A6
M_B A7	80	A7
M_B A8	89	A8
M_B A9	85	A9
M_B A10	107	A10/AP
M_B A11	84	A11
M_B A12	83	A12
M_B A13	119	A13
M_B A14	80	A14
M_B A15	78	A15
M_B BSA0	109	BA0
M_B BSA1	108	BA1
M_B DQ0	5	DO0
M_B DQ1	7	DO1
M_B DQ2	15	DO2
M_B DQ3	17	DO3
M_B DQ4	4	DO3
M_B DQ5	6	DO4
M_B DQ6	16	DO5
M_B DQ7	18	DO6
M_B DQ8	21	DO7
M_B DQ9	23	DO9
M_B DQ10	25	DO10
M_B DQ11	26	DO11
M_B DQ12	22	DO12
M_B DQ13	24	DO13
M_B DQ14	34	DO14
M_B DQ15	36	DO15
M_B DQ16	39	DO16
M_B DQ17	41	DO17
M_B DQ18	53	DO18
M_B DQ19	57	DO19
M_B DQ20	40	DO20
M_B DQ21	42	DO21
M_B DQ22	50	DO22
M_B DQ23	52	DO23
M_B DQ24	57	DO24
M_B DQ25	59	DO24
M_B DQ26	67	DO26
M_B DQ27	68	DO27
M_B DQ28	69	DO28
M_B DQ29	58	DO28
M_B DQ30	68	DO30
M_B DQ31	70	DO31
M_B DQ32	129	DO32
M_B DQ33	131	DO32
M_B DQ34	141	DO34
M_B DQ35	143	DO35
M_B DQ36	130	DO36
M_B DQ37	132	DO37
M_B DQ38	140	DO38
M_B DQ39	142	DO39
M_B DQ40	147	DO40
M_B DQ41	149	DO41
M_B DQ42	157	DO42
M_B DQ43	159	DO43
M_B DQ44	148	DO44
M_B DQ45	148	DO45
M_B DQ46	158	DO46
M_B DQ47	160	DO47
M_B DQ48	163	DO48
M_B DQ49	165	DO49
M_B DQ50	175	DO50
M_B DQ51	177	DO51
M_B DQ52	164	DO52
M_B DQ53	166	DO53
M_B DQ54	174	DO54
M_B DQ55	176	DO55
M_B DQ56	181	DO56
M_B DQ57	183	DO57
M_B DQ58	191	DO58
M_B DQ59	193	DO59
M_B DQ60	180	DO60
M_B DQ61	182	DO61
M_B DQ62	182	DO62
M_B DQ63	194	DO63
M_B DQS#0	10	DQS0#
M_B DQS#1	27	DQS1#
M_B DQS#2	45	DQS2#
M_B DQS#3	62	DQS3#
M_B DQS#4	135	DQS4#
M_B DQS#5	152	DQS5#
M_B DQS#6	169	DQS6#
M_B DQS#7	186	DQS7#
M_B DQS0	12	DQS0
M_B DQS1	29	DQS1
M_B DQS2	47	DQS2
M_B DQS3	64	DQS3
M_B DQS4	137	DQS4
M_B DQS5	154	DQS5
M_B DQS6	171	DQS6
M_B DQS7	188	DQS7
M_B DIM0_ODT0	116	ODT0
M_B DIM0_ODT1	120	ODT1
M_VREF_CA_DIMM1	126	VREF_CA
M_VREF_DQ_DIMM1	1	VREF_DQ
RESETP#	30	RESET#
VTT1	203	VTT1
VTT2	204	VTT2

6 M_B_DQS[7:0] 6
6 M_B_DQS[7:0] 6

6 M_B_DIM0_ODT0
6 M_B_DIM0_ODT1
M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1

15,37 DDR3_DRAMRST#

0617 Modify: Joseph Change M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1, M_VREF_CA_DIMM0, M_VREF_CA_DIMM1 from net to power.

H = 5.2mm
DDR3-204P-48-GP
62.10017.P61

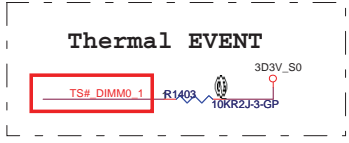
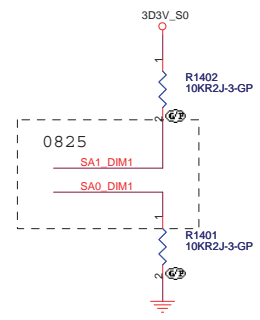
2nd = 62.10017.N41
3rd = 62.10017.P41
4th = 62.10024.E21

<http://hobi-elektronika.net>

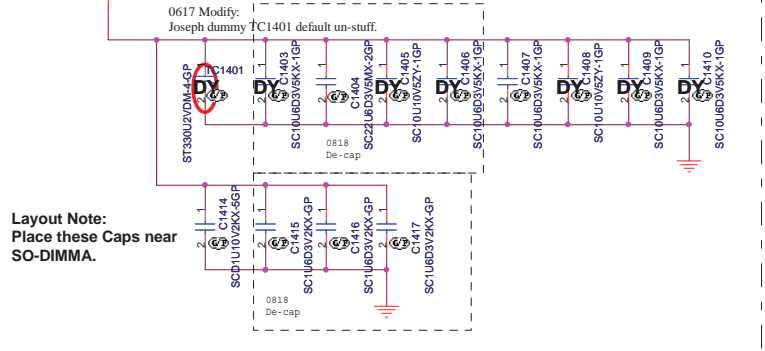
NP1	71	NP1
NP2	72	NP2
RAS#	110	M_B_RAS# 6
WE#	113	M_B_WE# 6
CAS#	115	M_B_CAS# 6
CS0#	114	M_B_DIM0_CS#0 6
CS1#	121	M_B_DIM0_CS#1 6
CKE0	73	M_B_DIM0_CKE0 6
CKE1	74	M_B_DIM0_CKE1 6
CK0	101	M_B_DIM0_CLK_DDR0 6
CK0#	103	M_B_DIM0_CLK_DDR#0 6
CK1	102	M_B_DIM0_CLK_DDR1 6
CK1#	104	M_B_DIM0_CLK_DDR#1 6
DM0	11	
DM1	28	
DM2	46	
DM3	63	
DM4	136	
DM5	153	
DM6	170	
DM7	187	
SDA	200	PCH_SMBDATA 15,20,79,82
SCL	202	PCH_SMBCLK 15,20,79,82
EVENT#	198	TS#_DIMM0_1 15
VDDSPD	199	
SA0	197	SA0_DIM1
SA1	201	SA1_DIM1
NC#1	77	X
NC#2	122	X
NC#TEST	125	X
VDD1	75	
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	119	
VDD17	123	
VDD18	124	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	13	
VSS	14	
VSS	19	
VSS	20	
VSS	25	
VSS	26	
VSS	31	
VSS	32	
VSS	37	
VSS	38	
VSS	43	
VSS	44	
VSS	48	
VSS	49	
VSS	54	
VSS	55	
VSS	58	
VSS	60	
VSS	61	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	127	
VSS	128	
VSS	133	
VSS	134	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	150	
VSS	151	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	167	
VSS	168	
VSS	172	
VSS	173	
VSS	179	
VSS	184	
VSS	185	
VSS	189	
VSS	190	
VSS	195	
VSS	196	
VSS	205	
VSS	206	

1110 X02 Modify: DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from MR updated connector list.

PART NUMBER	Height	TYPE
62.10017.P61	5.2mm	REVERSED
62.10017.N41(2nd)	5.2mm	REVERSED
62.10017.P41(3rd)	5.2mm	REVERSED
62.10024.E21(4th)	5.2mm	REVERSED



SODIMM A DECOUPLING



Layout Note: Place these Caps near SO-DIMMA.

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

<Variant Name>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Hsi Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

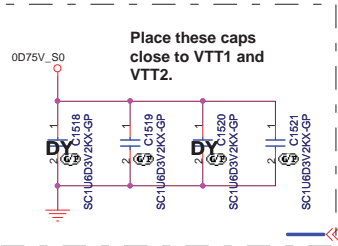
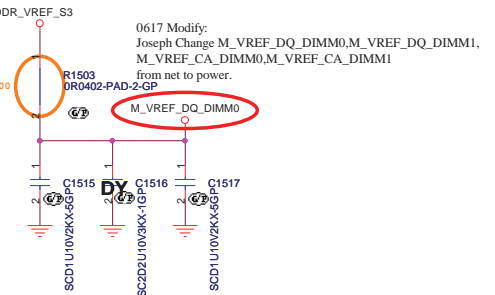
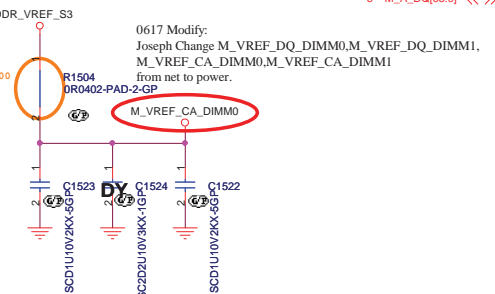
Title: **DDR3-SODIMM2**

Size Custom: **QUEEN 15**

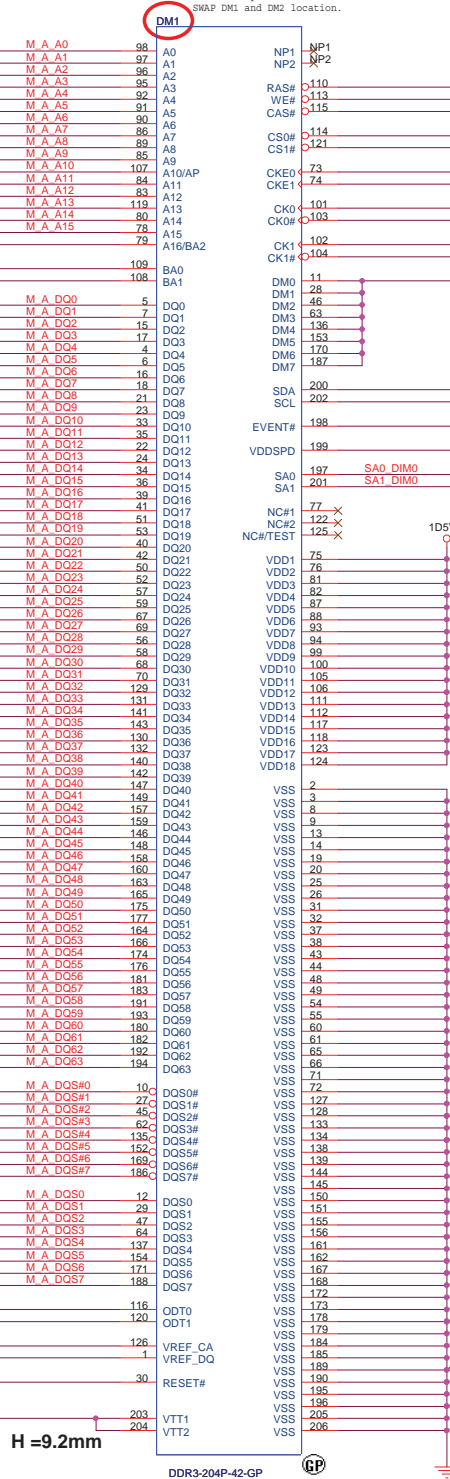
Date: **uesday, January 04, 2011** Sheet 14 of 108

SSID = MEMORY

0707 Modify:
Change R1503, R1504 to 0ohm 0402 from short pad.

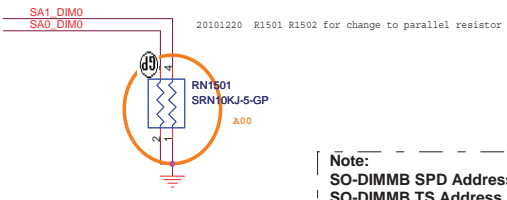
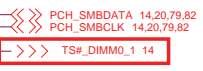
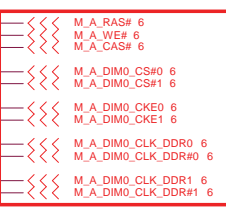


0617 Modify:
Joseph Change M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1, M_VREF_CA_DIMM0, M_VREF_CA_DIMM1 from net to power.



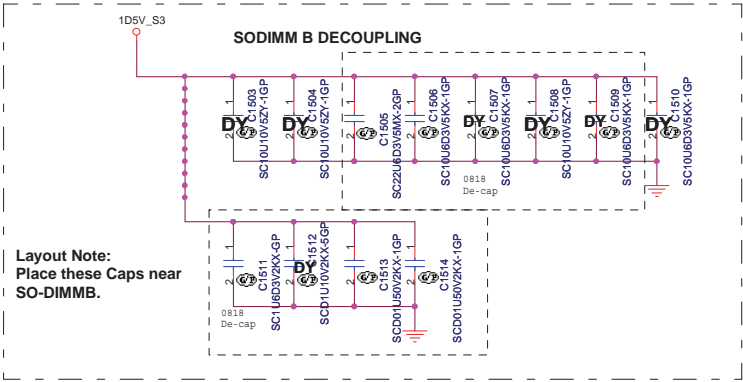
DM1

62.10017.Q41
2nd = 62.10017.N11
3rd = 62.10017.N61
4th = 62.10024.D91



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q41	9.2mm	REVERSED
62.10017.N11(2nd)	9.2mm	REVERSED
62.10017.N61(3rd)	9.2mm	REVERSED
62.10024.D91(4th)	9.2mm	REVERSED

1110 X02 Modify:
DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on S7 stage from ME updated connector list.

<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.


Title: **DDR3-SODIMM1**

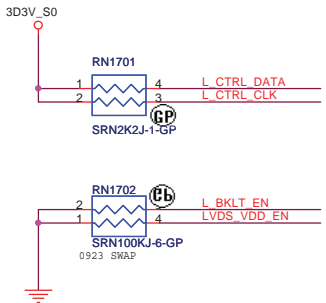
Size Custom: Document Number **QUEEN 15** Rev **A00**

Date: **1**uesday, January 04, 2011 Sheet **15** of **108**

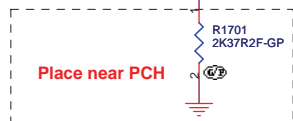
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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet	16 of 108



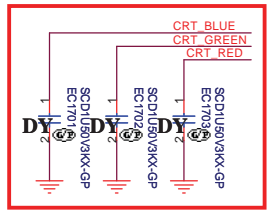
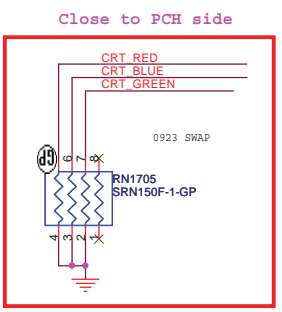
L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display



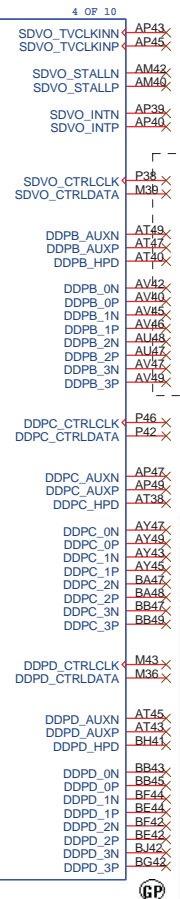
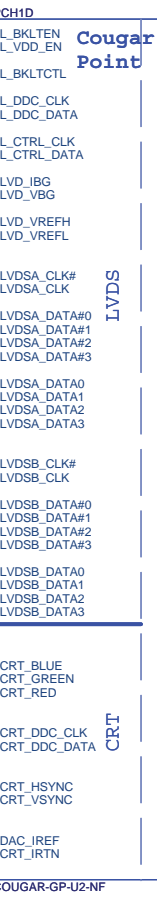
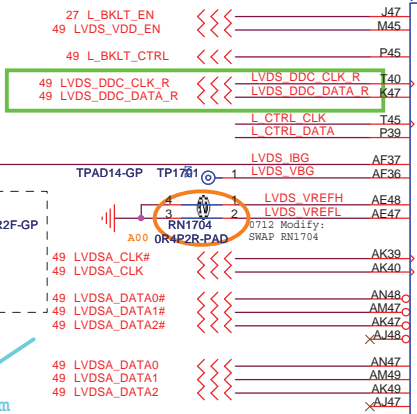
Impedance: 90 ohm

0617 Modify:
Joseph Removed LVDSB related net for single LVDS channel base on Dell updated spec.

0917 X01 Modify:
Add R1703-R1705 on RGB signal and reserved ECI1701-EC1703 0.1u from EMC Neo suggestion.



Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402



0804 Remove HDMI from PCH.

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_0]P	SDVO_RED	DDPB_0]P	TMDSB_DATA2
	DDPB_0]N	SDVO_RED#	DDPB_0]N	TMDSB_DATA2#
	DDPB_1]P	SDVO_GREEN	DDPB_1]P	TMDSB_DATA1
	DDPB_1]N	SDVO_GREEN#	DDPB_1]N	TMDSB_DATA1#
	DDPB_2]P	SDVO_BLUE	DDPB_2]P	TMDSB_DATA0
	DDPB_2]N	SDVO_BLUE#	DDPB_2]N	TMDSB_DATA0#
	DDPB_3]P	SDVO_CLK	DDPB_3]P	TMDSB_CLK
	DDPB_3]N	SDVO_CLK#	DDPB_3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA

<Variant Name>

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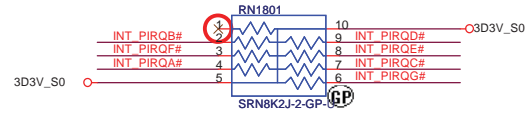
Title: **PCH (LVDS/CRT/DDI)**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

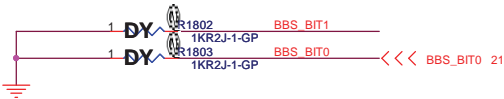
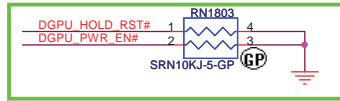
Date: Tuesday, January 04, 2011 Sheet 17 of 108

SSID = PCH

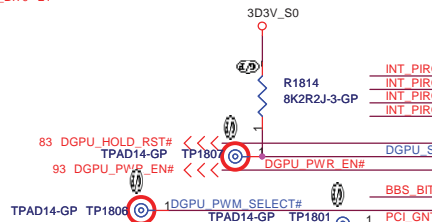
0709 Modify:
Removed INT_PIRQ# on RN1801 pin1.



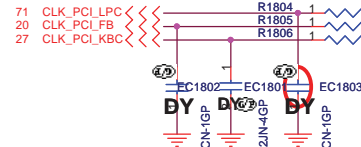
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



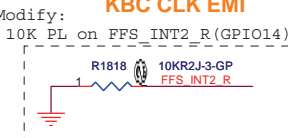
0709 Modify:
Add R1817 0ohm and connect to KB_LED_BL_DET.
(5V Tolerance High Active)



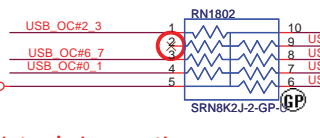
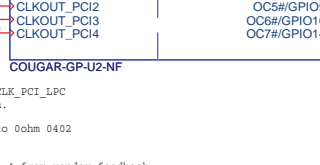
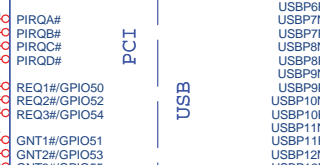
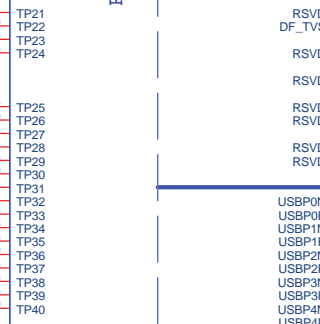
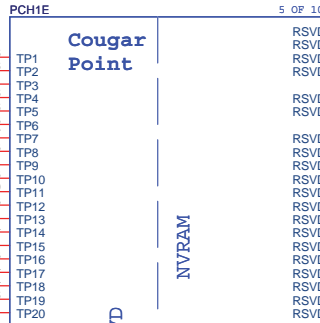
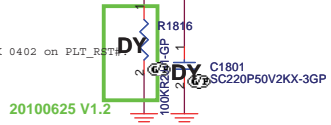
0617 Modify:
Joseph Remove PLT_RST AND gate logic IC U1801/C1802.



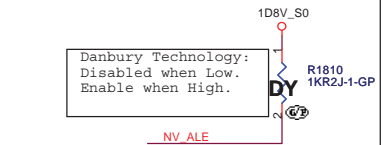
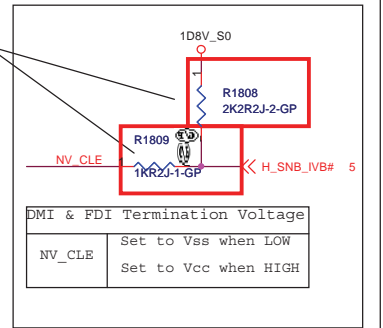
0908 X01 Modify:
Add R1818 10K PL on FFS INT2 R(GPIO14)



0629 Modify:
Reserved R1816 100K 0402 on PLT_RST#



0719 Modify:
DP_TVS (NV_CLE) connect PROC_SELECT# (H_SNB_IVB#) with R1808 2.2K(05% pull up resistor to PCH_VCCPND rail and a R1809 1K(05% series resistor base on Intel feedback.



USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

1120 X02 Modify:
Reserved USB_OC#_1 connect from PCH GPIO59.

USB 2.0 Overcurrent Pin Default Usage

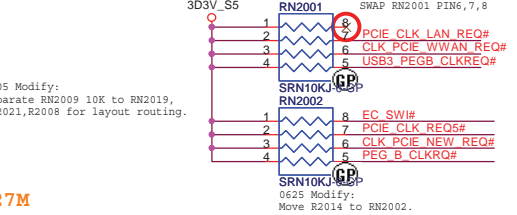
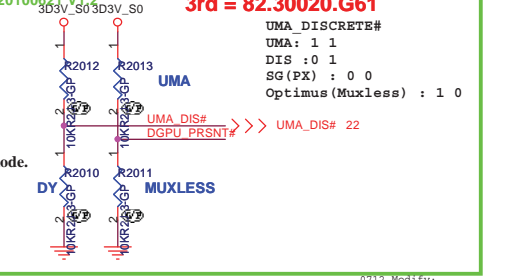
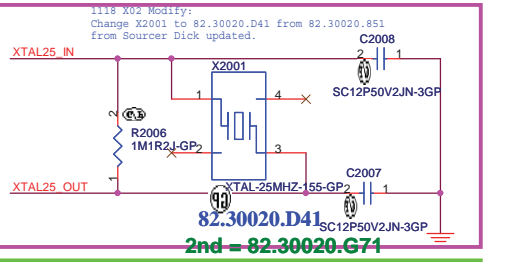
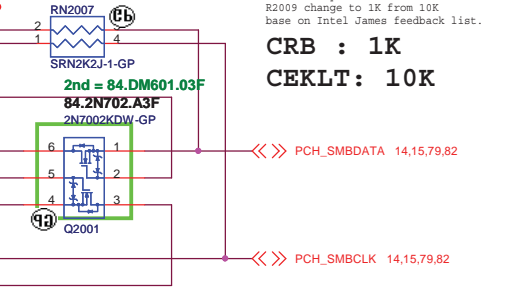
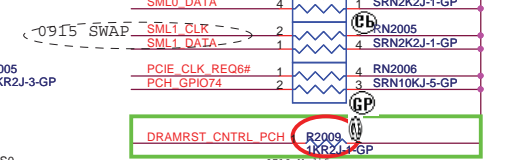
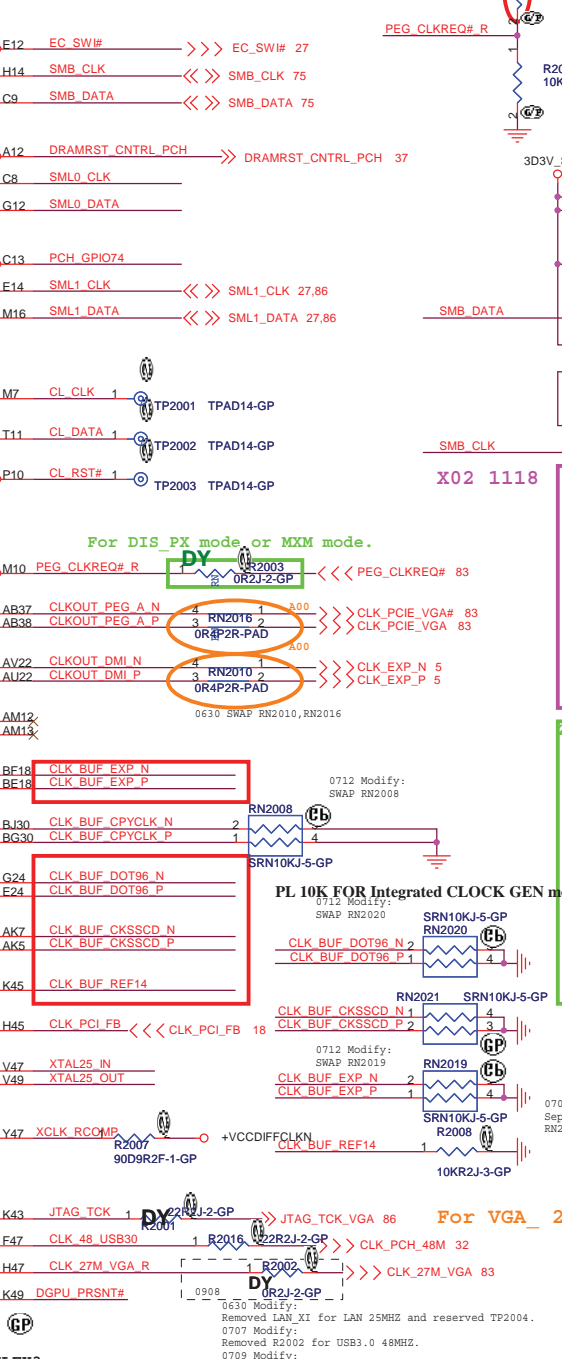
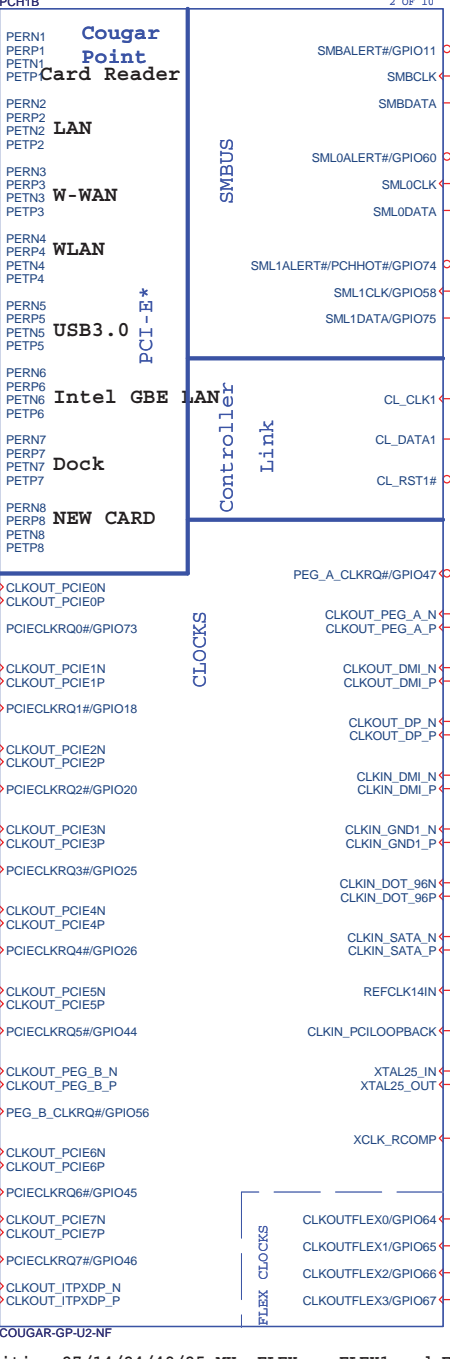
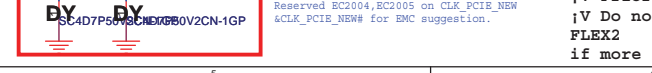
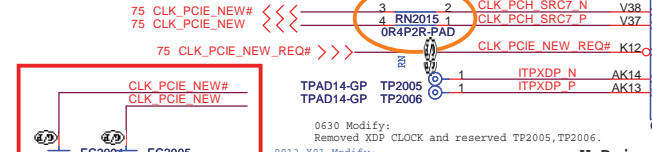
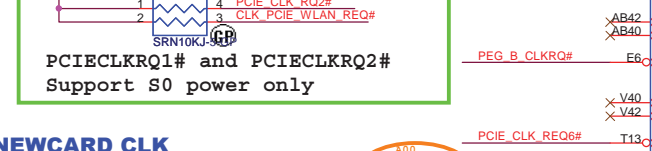
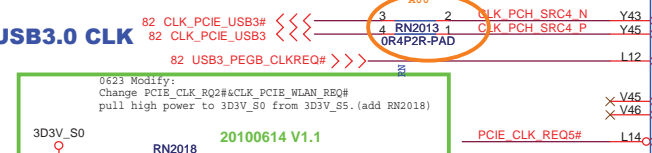
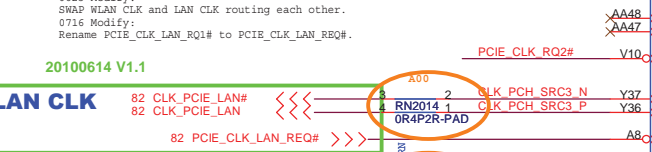
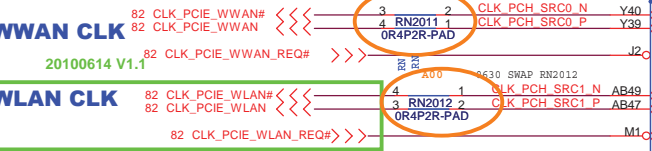
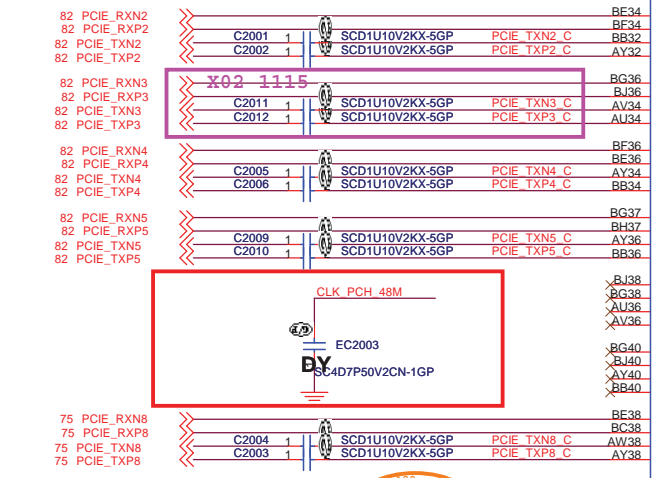
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used



Title			PCH (PCI/USB/NVRAM)		
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SSID = PCH

1112 X02 Modify:
Dell required us to disable PCIE port of WWAN slot
,If PCIE port 1 is disabled, it will cause all PCIE port
disabled,so change WWAN to PCIE port 3 from port1
at ST stage.



0630 Modify: Removed XDP CLOCK and reserved TP2005, TP2006.
0913 X01 Modify: Reserved EC2004, EC2005 on CLK_PCIE_NEW & CLK_PCIE_NEW# for EMC suggestion.
iV Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
iV Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if more than 2 PCI clocks + PCI loopback are present

<http://hebi.elektronika.net>

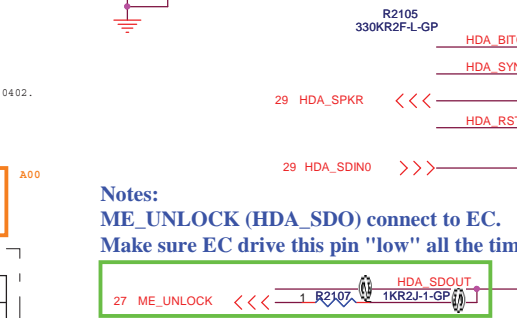
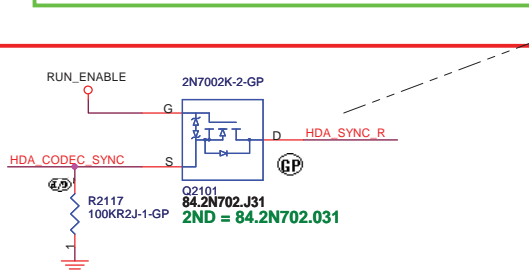
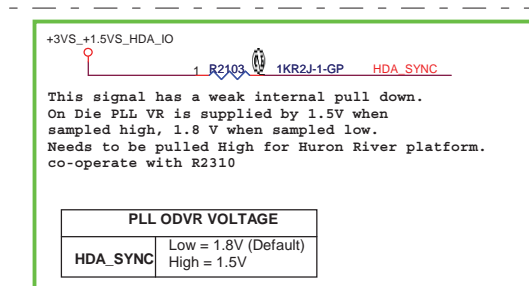
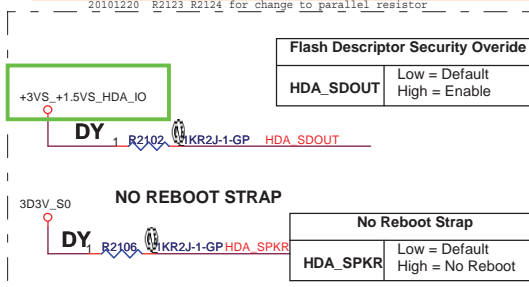
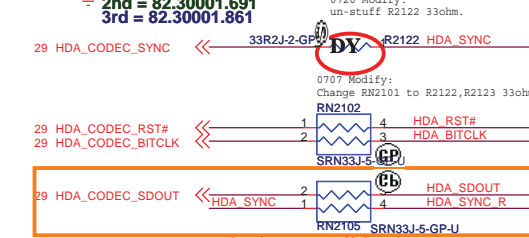
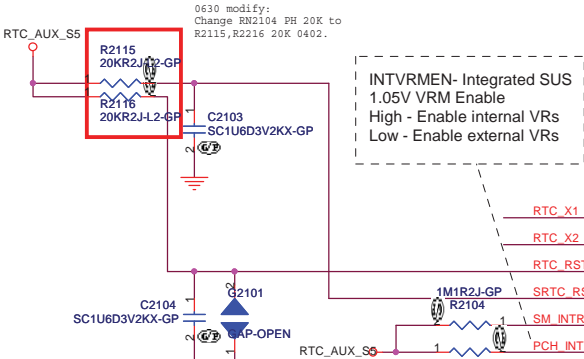
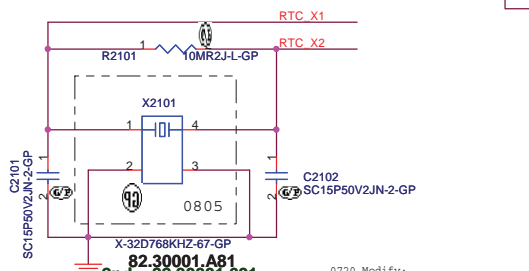
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Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

Date: Tuesday, January 04, 2011 Sheet 20 of 108

SSID = PCH

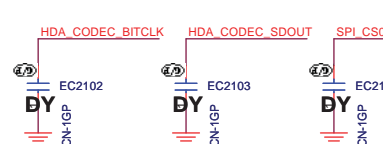


Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

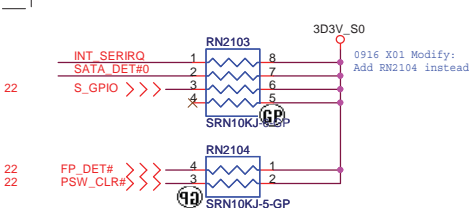
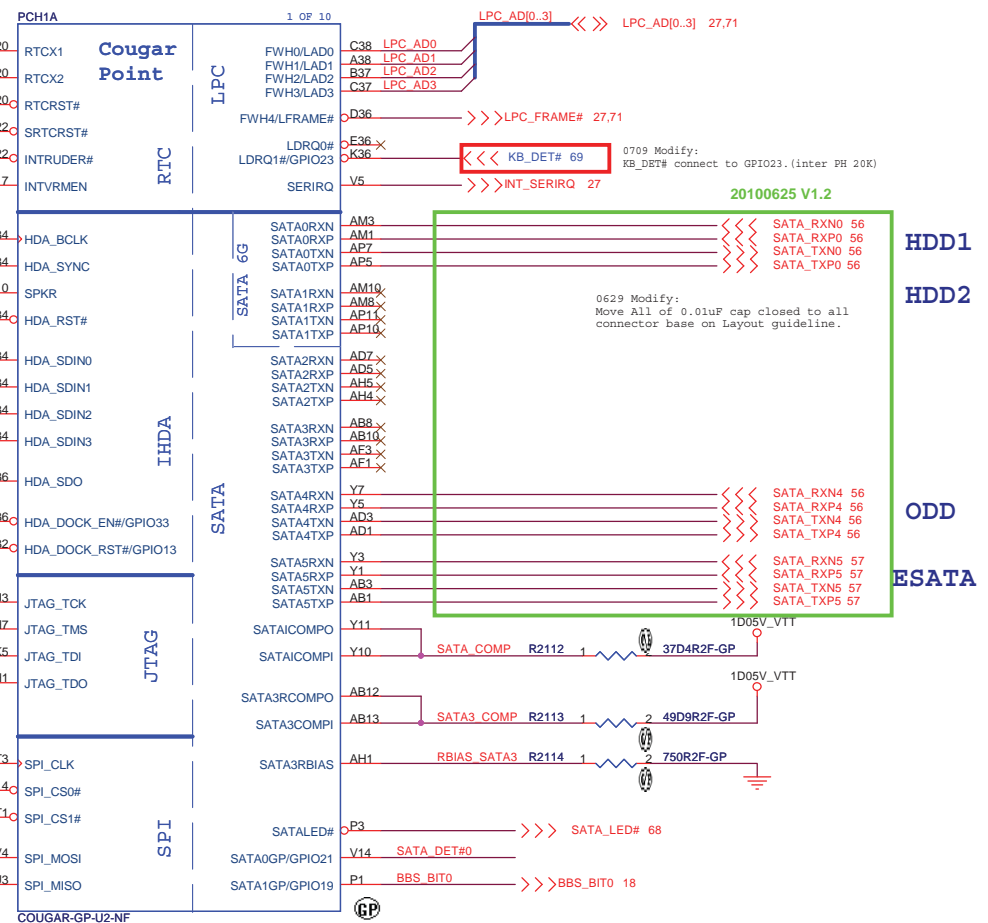


HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

0625 Modify: Reserved EC2102, EC2103 on HDA_CODEC_BITCLK&HDA_CODEC_SDOUT for BMC NEO suggestion.



<http://hobi-elektronika.net>



0916 X01 Modify: Add RN2104 instead of R2111 10K.

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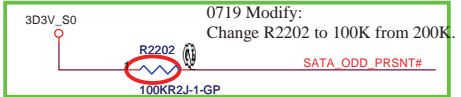
DELL

File: **PCH (SPI/RTC/LPC/SATA/IHDA)**

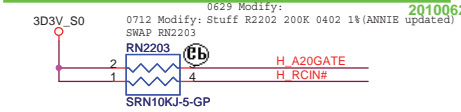
Size A3 Document Number **QUEEN 15** Rev **A00**

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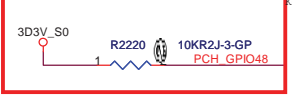
SSID = PCH



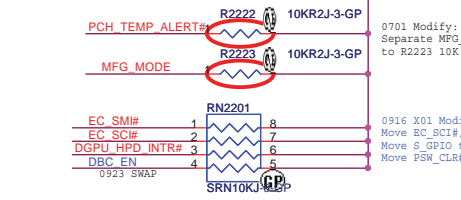
Note:
For PCH debug with XDP, need to NO STUFF R2218



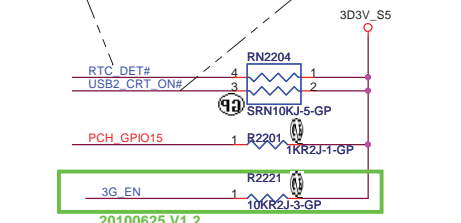
GPIO27 has a weak [20K] internal pull up.
To enable on-die PLL Voltage regulator, should not place external pull down.



0701 Modify:
Separate PCH_TEMP_ALERT# from RN2201 to R2222 10K base on layout limitation.

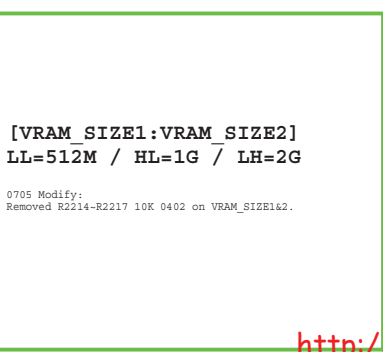
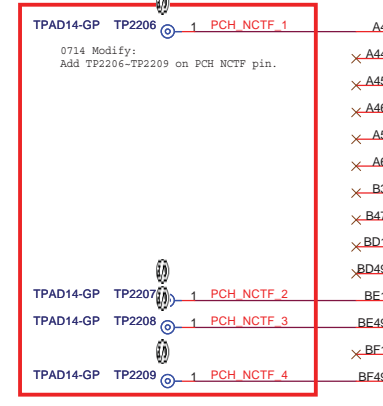
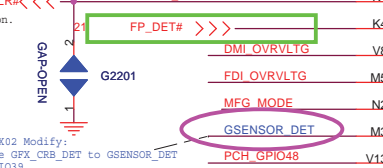
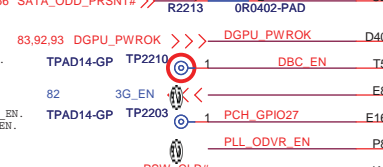
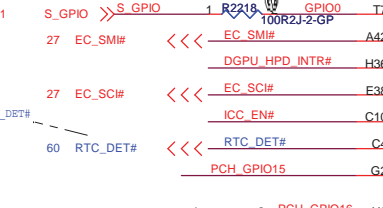


1120 X02 Modify:
Rename PCH_GPIO12 to RTC_DET# on GPIO12.

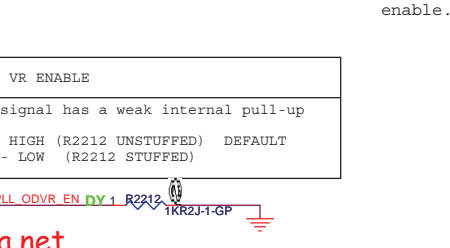
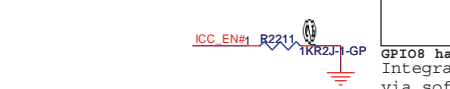
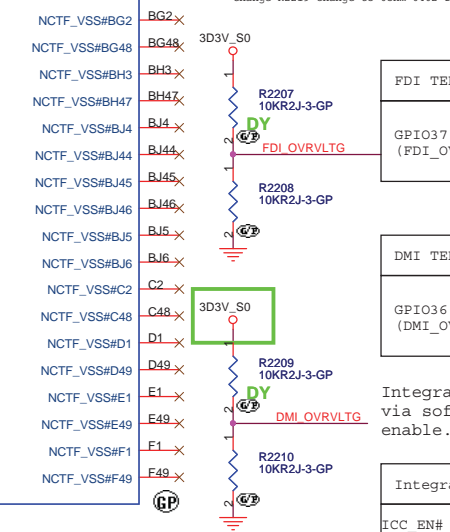
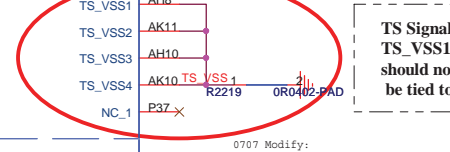
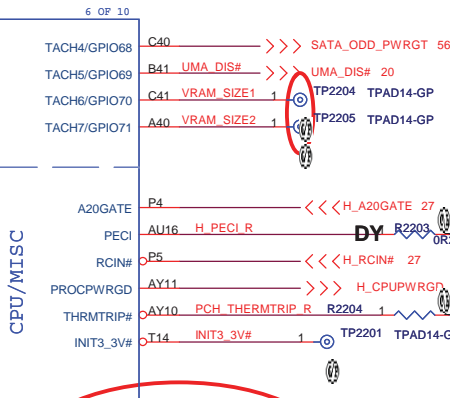
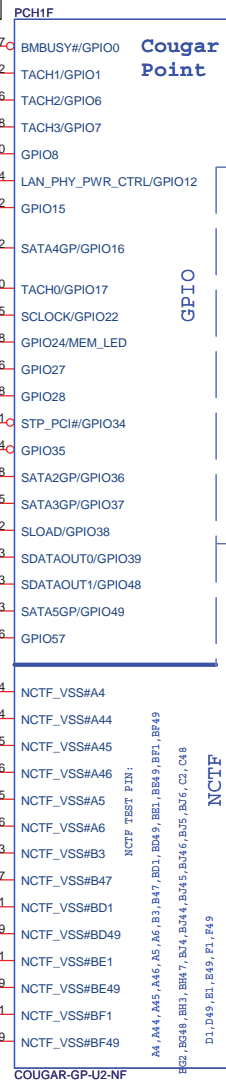


0629 Modify:
Add R2221 10K 0402 on PCH_GPIO24 (ANNIE updated)

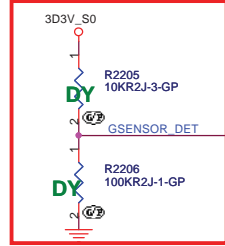
0709 Modify:
Rename PCH_GPIO24 to 3G_EN on R2221.



0705 Modify:
Removed R2214-R2217 10K 0402 on VRAM_SIZE1&2.



	GSENSOR_ST	GSENSOR_ADI
R2205	DY	10K
R2206	100K	DY



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE

GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)
----------------------	---

DMI TERMINATION VOLTAGE OVERRIDE

GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)
----------------------	---

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable

ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT]
	LOW (R2211) - ENABLED

GPIO8 has a weak [20K] internal pull up. Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K

ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT

DISABLED -- LOW (R2212 STUFFED)

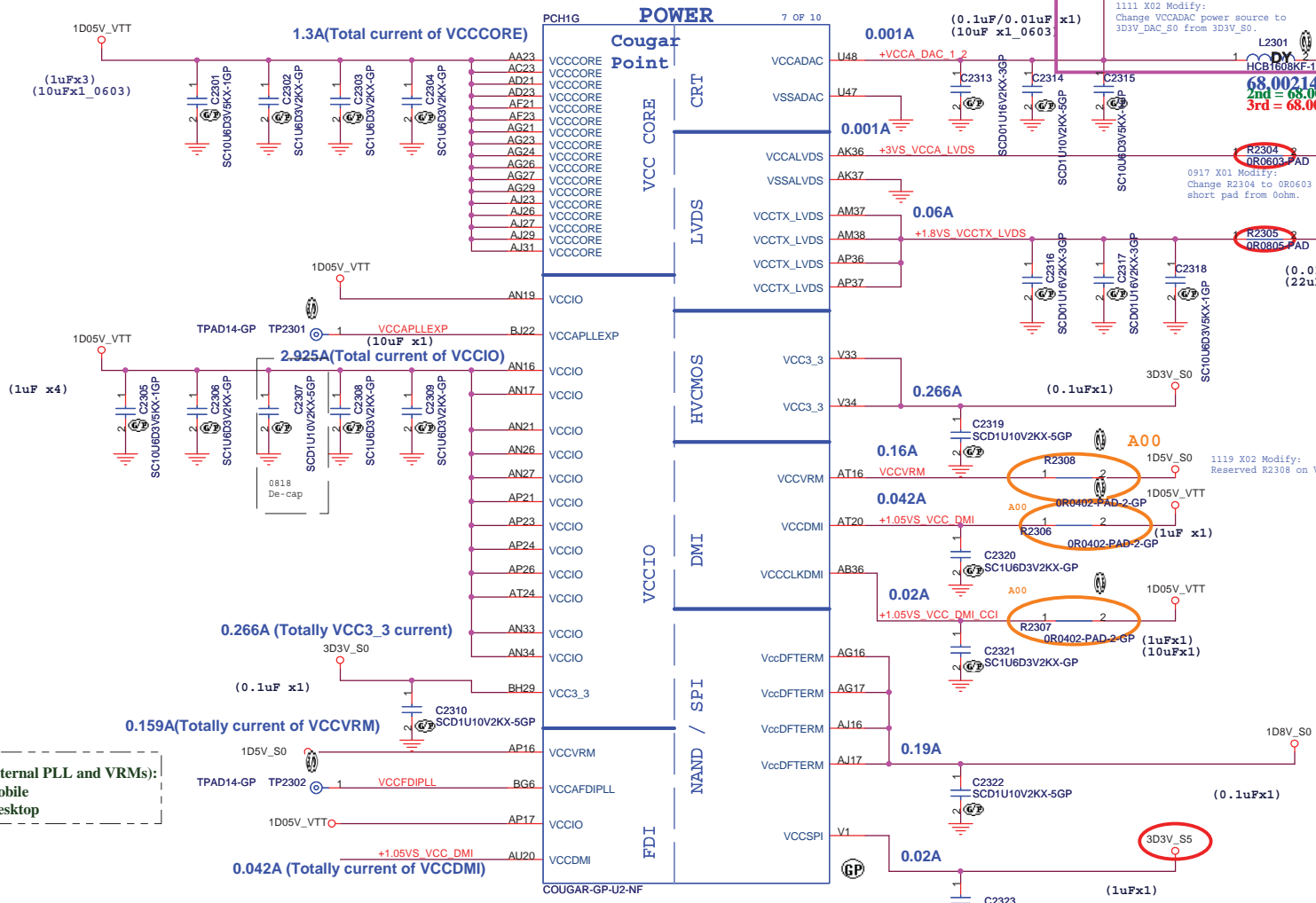
<Variant Name>

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Title: **PCH (GPIO/CPU)**

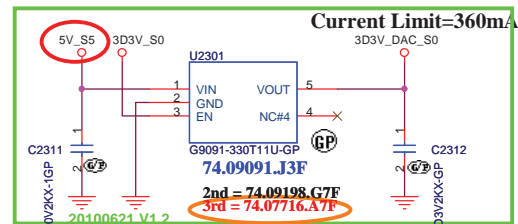
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VCCVRM (Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop

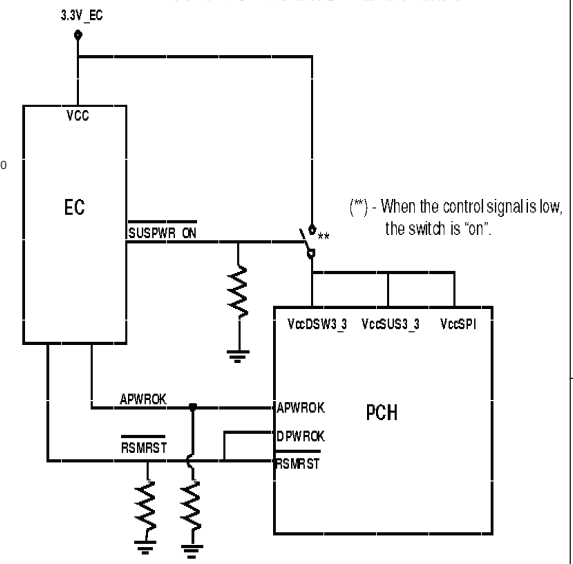
1122 X02 Modify:
Removed U2302 LDO for VCCVRM.



1117 X02 Modify:
Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue.
1122 X02 Modify:
base on layout condition change 3D3V_DAC_S0 circuit.

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture



(*) - When the control signal is low, the switch is "on".

<Variant Name>

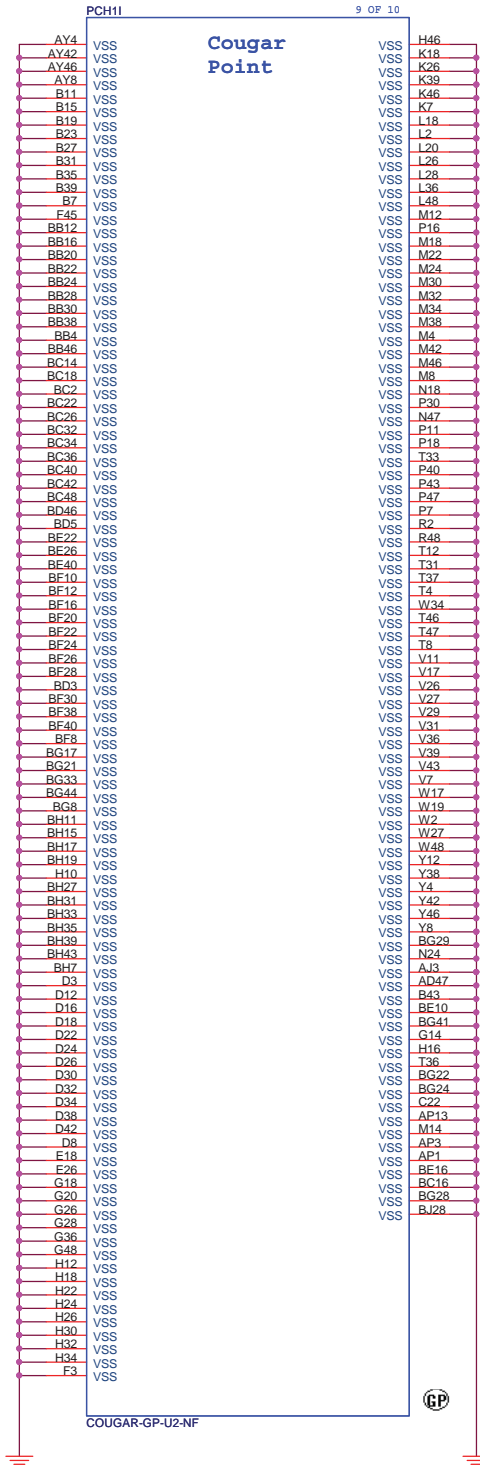
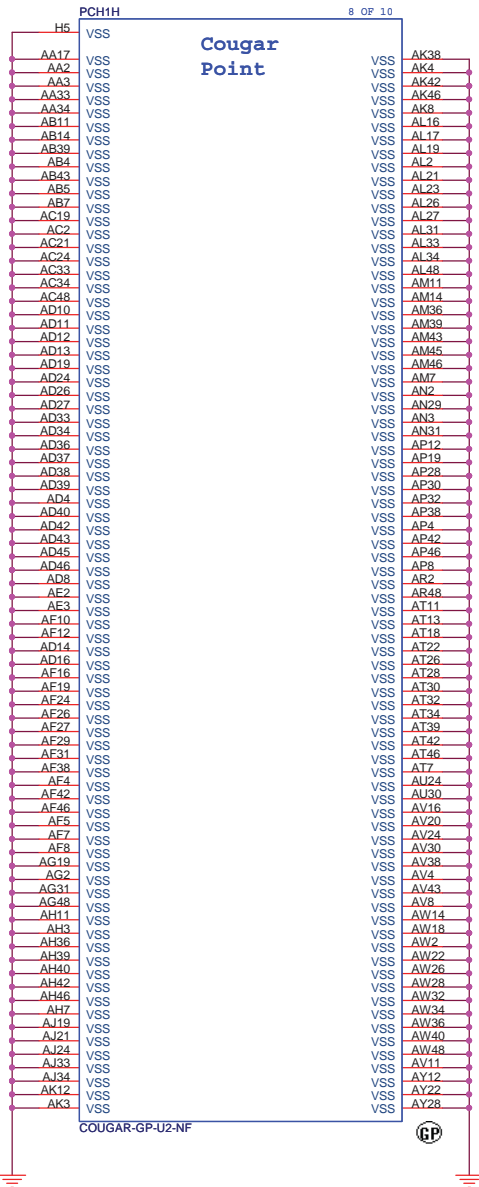
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

Date: Tuesday, January 04, 2011 Sheet 23 of 108

SSID = PCH



<http://hobi-elektronika.net>

<Variant Name>

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

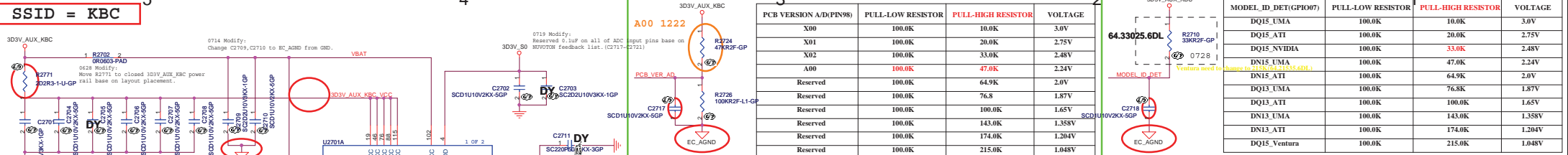
Size A3	Document Number	Rev
	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 25 of 108

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<Variant Name>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number QUEEN 15	Rev A00
Date: Tuesday, January 04, 2011	Sheet 26 of	108

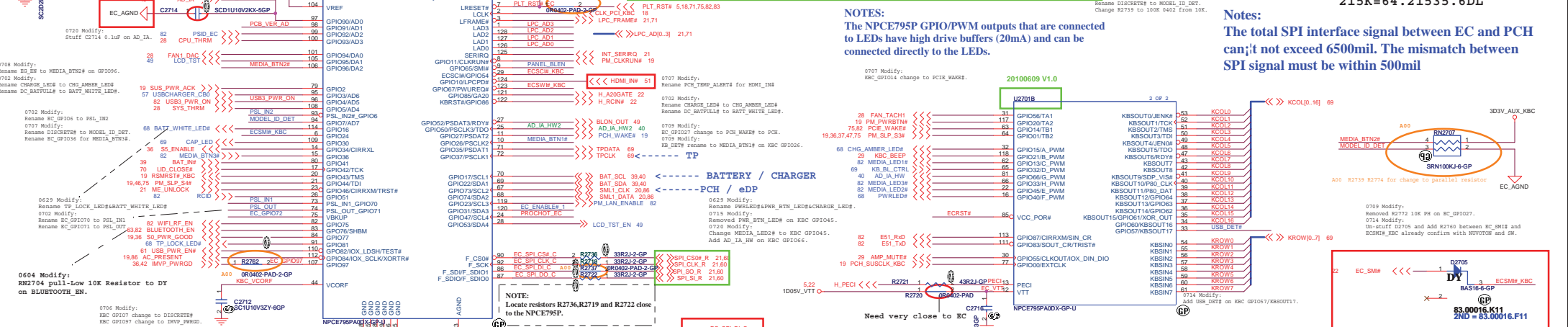


PCB VERSION A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	300.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

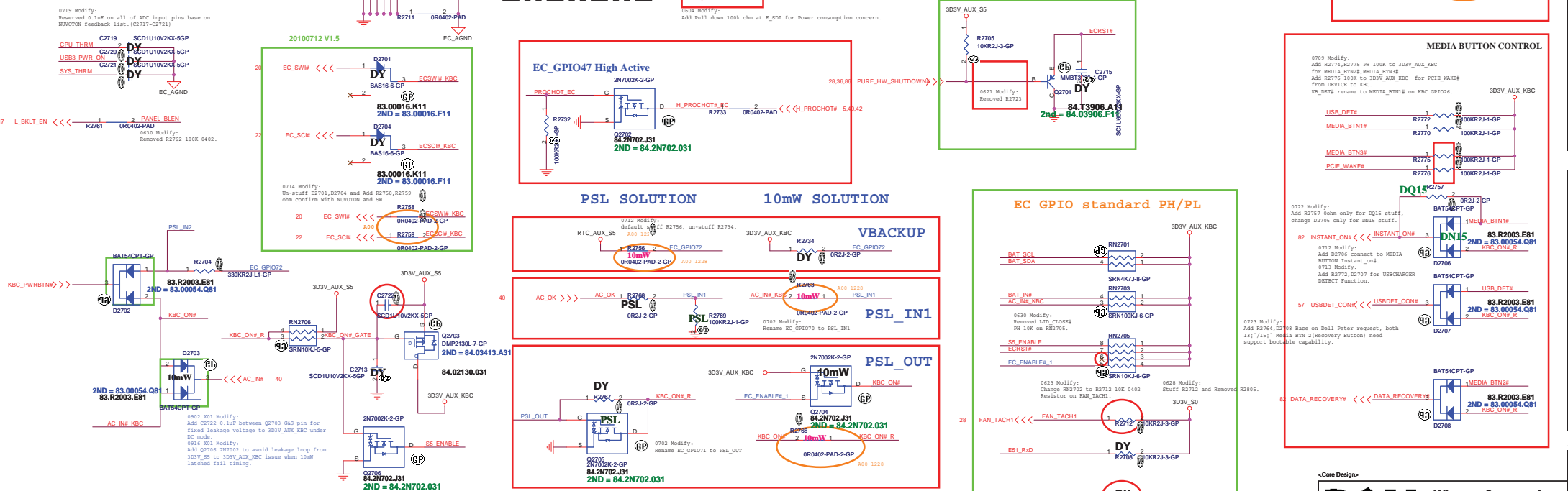
MODEL_ID_DET(GPIO#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMI	100.0K	10.0K	3.0V
DQ15_ATA	100.0K	20.0K	2.75V
DQ15_NVidia	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K	2.24V
DN15_ATI	100.0K	64.9K	2.0V
DQ13_ATA	100.0K	76.8K	1.87V
DQ13_UMI	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.358V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V

NOTES:
 The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.

Notes:
 The total SPI interface signal between EC and PCH can't exceed 6500mil. The mismatch between SPI signal must be within 500mil



ROSA Multi GPIO setting



NOTES:
 Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

DELL Wistron Corporation
 2/F, 88, Sec. 1, Han Tai Wu Rd., Hsinchu, Taipei Hsein 321, Taiwan, R.O.C.

KBC NuvoTon NPCE795
QUEEN 15

File: _____
 Size A2 Document Number _____ Rev A00
 Date: Tuesday, January 04, 2011 Sheet 27 of 108

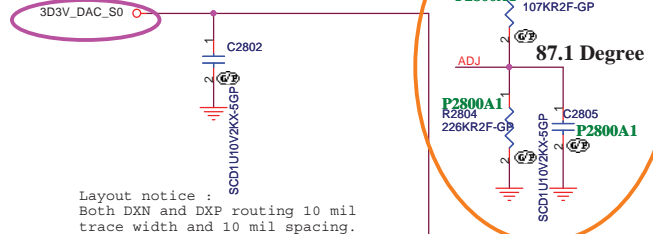
SSID = Thermal

Thermal sensor P2800

0705 Modify:
R2802 change to 0ohm 0402 from short pad and default un-stuff.

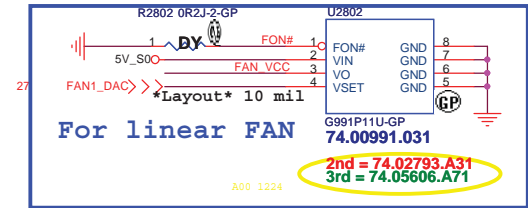
Fan controller P2793

1119 X02 Modify:
Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0.



Layout notice :
Both DXN and DXF routing 10 mil trace width and 10 mil spacing.

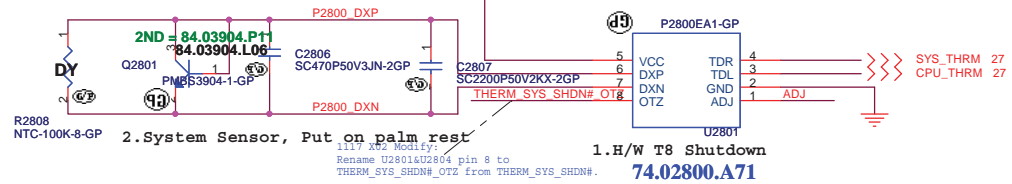
	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low (<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm



For linear FAN

2nd = 74.02793.A31
3rd = 74.05606.A71

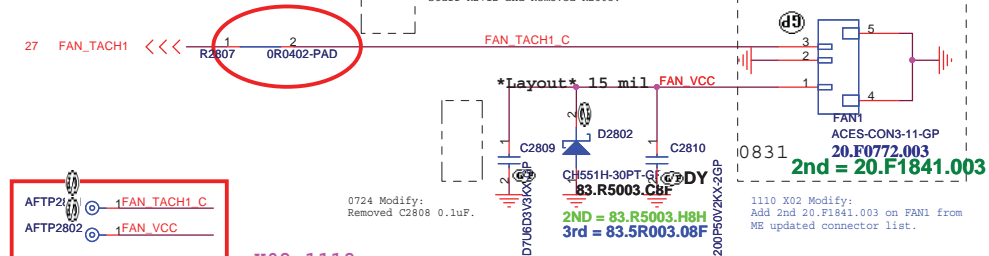
0614 Modify:
Change FAN1 connector part number to 20.D0210.103 base on ME EMN and DXF.
0712 Modify:
Change FAN1 part number to 20.F1639.004 from 20.D0210.103 base on latest EMN and DXF.



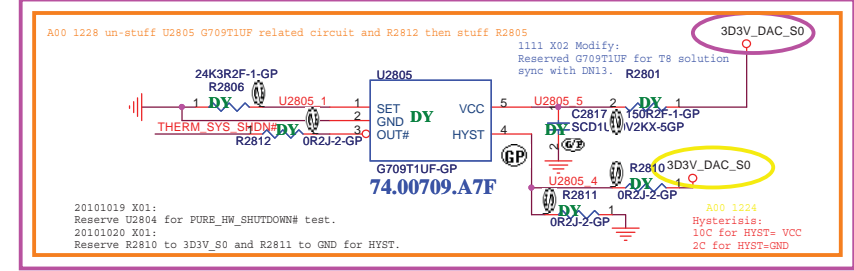
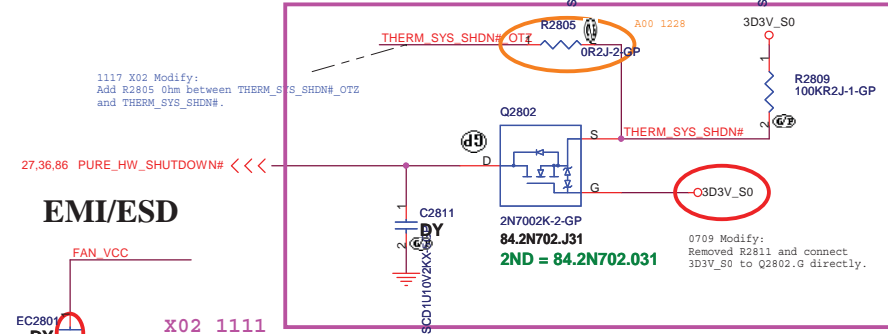
1.H/W T8 Shutdown
74.02800.A71

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



EMI/ESD



A00 1228 Cancel VGA Thermal sensor P2800 circuit

1111 X02 Modify:
ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.

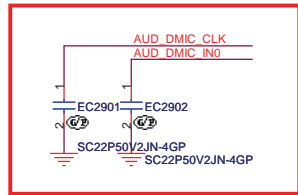
<Core Design>



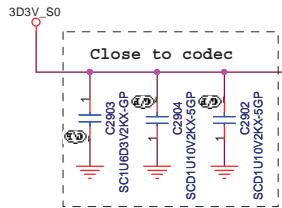
Title Thermal P2800/Fan Controller P2793		
Size A3	Document Number QUEEN 15	Rev A00
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SSID = AUDIO

For EMI



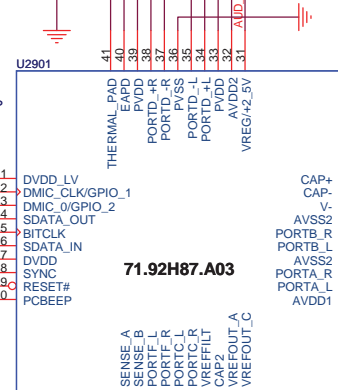
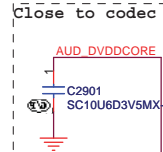
1122 X02 Modify:
change R2920, R2921 to 22ohm from 0ohm and
stuff SC2901, EC2902 22p from BMC Neo updated.



21 HDA_CODEC_SDOOUT
21 HDA_CODEC_BITCLK
21 HDA_SDIN0

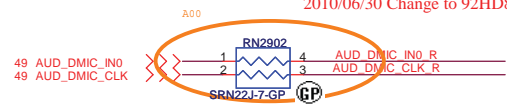
21 HDA_CODEC_SYNC
21 HDA_CODEC_RST#

27 AMP_MUTE# >>> AMP_MUTE#



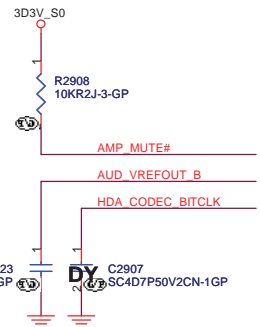
0707 Modify:
updated U2901 part number from data base.

92HD87B1A5NDGXTB8-GP
2010/06/30 Change to 92HD87 (71.92H87.A03)

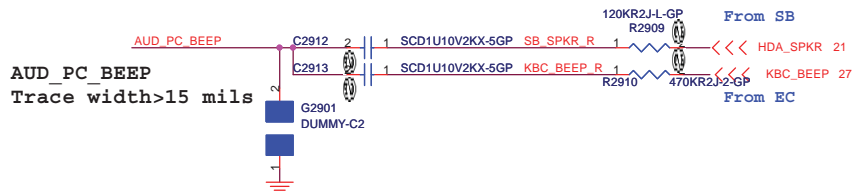


49 AUD_DMIC_IN0
49 AUD_DMIC_CLK

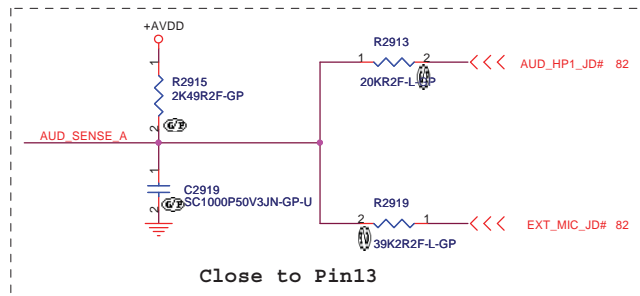
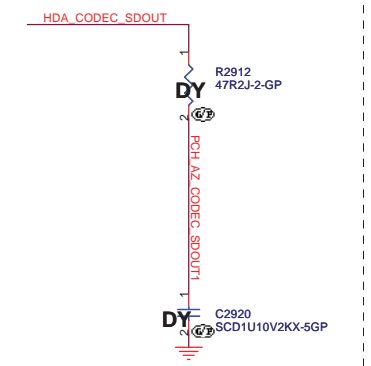
20101220 R2920 R2921 for change to parallel resistor



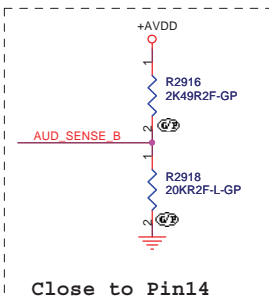
AUD_PC_BEEP
Trace width > 15 mils



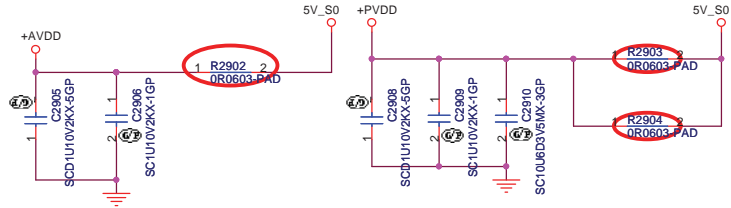
Azalia I/F EMI



Close to Pin3

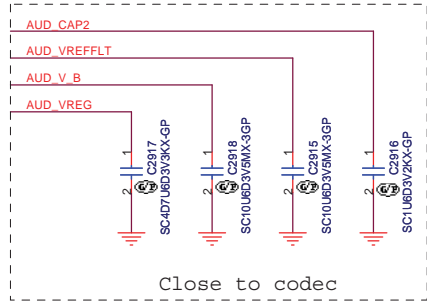


Close to Pin4



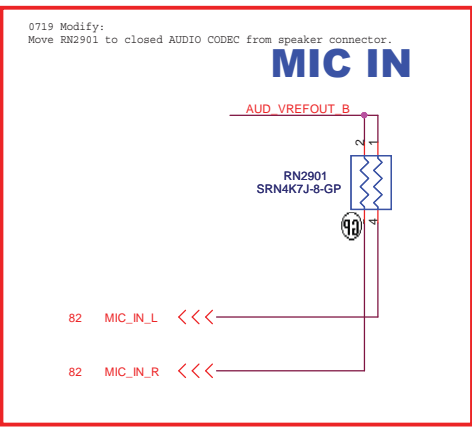
CLOSE TO CODEC

Put C2921 and C2922 close to codec



Close to codec

0707 Modify:
Change R2911, R2914, R2917 change
to 0ohm 0603 from short pad.
0726 Modify:
Removed all of AUD_AGND and R2911, R2914, R2917.



0719 Modify:
Move RN2901 to closed AUDIO CODEC from speaker connector.

MIC IN

82 MIC_IN_L <<<
82 MIC_IN_R <<<

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<Core Design>


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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec 92HD87B1**

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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
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<Core Design>

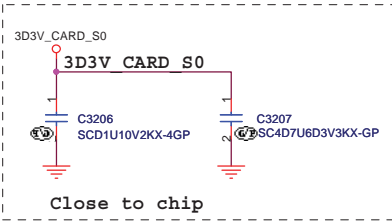
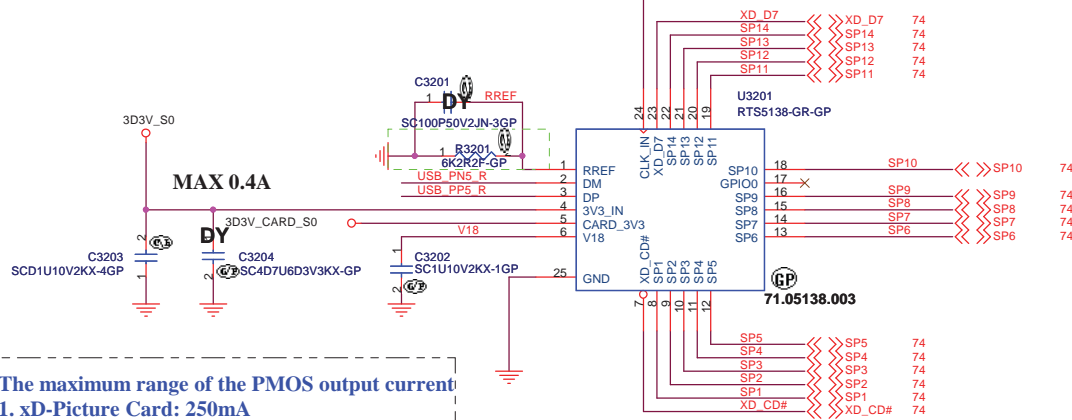
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Title			
Reserved			
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SSID = SDIO

48MHz clock input trace of characteristic impedance (Z_0) must be 50 Ω \pm 15%.

20 CLK_PCH_48M >>>

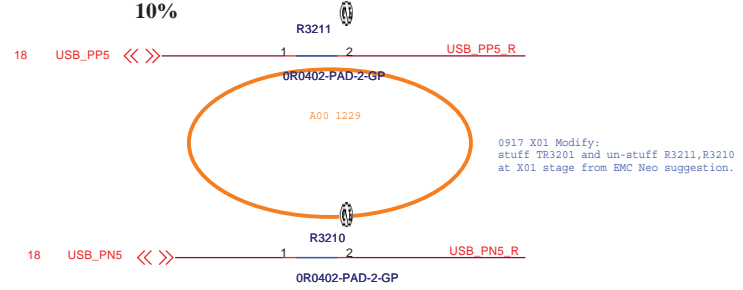
PCH GPIO67(48M) confirm with SW



The maximum range of the PMOS output current
 1. xD-Picture Card: 250mA
 2. SD/MMC Card: 250mA
 3. MS/MSPRO/Duo-HG: 250mA

- POWER TRACE**
1. RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
 2. RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
 3. RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum). Keep the trace routing lengths as short as possible.
 4. RTS5138: pin 1 (RREF) trace fixed width is 12 mils (minimum).
 5. RTS5138: pin 1 (RREF) trace must far away 48MHz clock trace.
 6. De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
 7. It is recommended that use of ferrites bead on power trace.
 8. Via size: Pad >= 32 mils, Finished hole >= 16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Z_{diff}) is 90 Ω \pm 10%



<Core Design>


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Title: **Card Reader-RTS5138**

Size: A3	Document Number: QUEEN 15	Rev: A00
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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
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<Core Design>

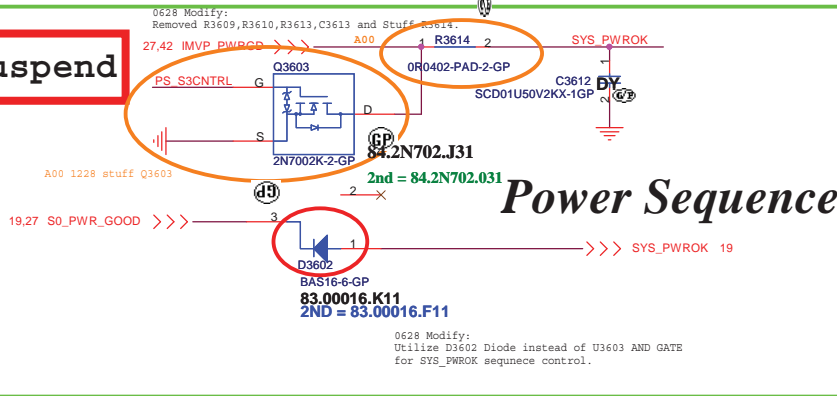
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Reserved		
Size	Document Number	Rev
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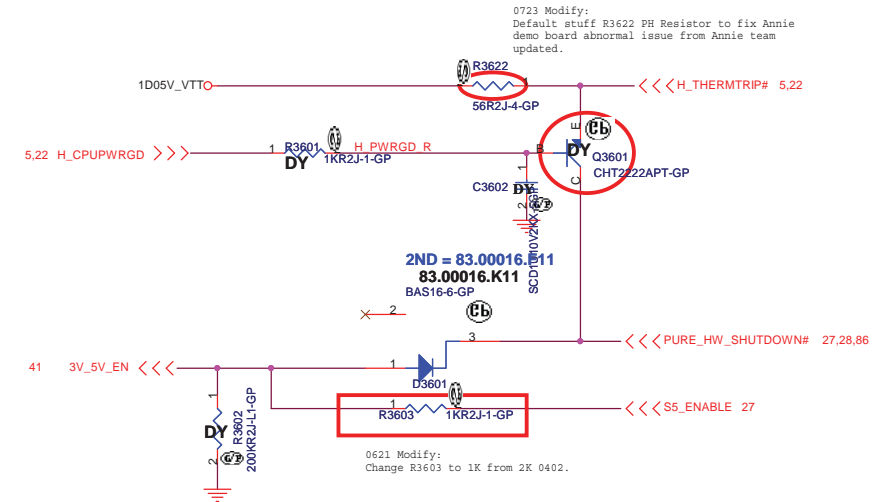
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Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
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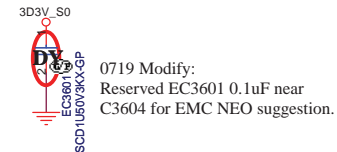
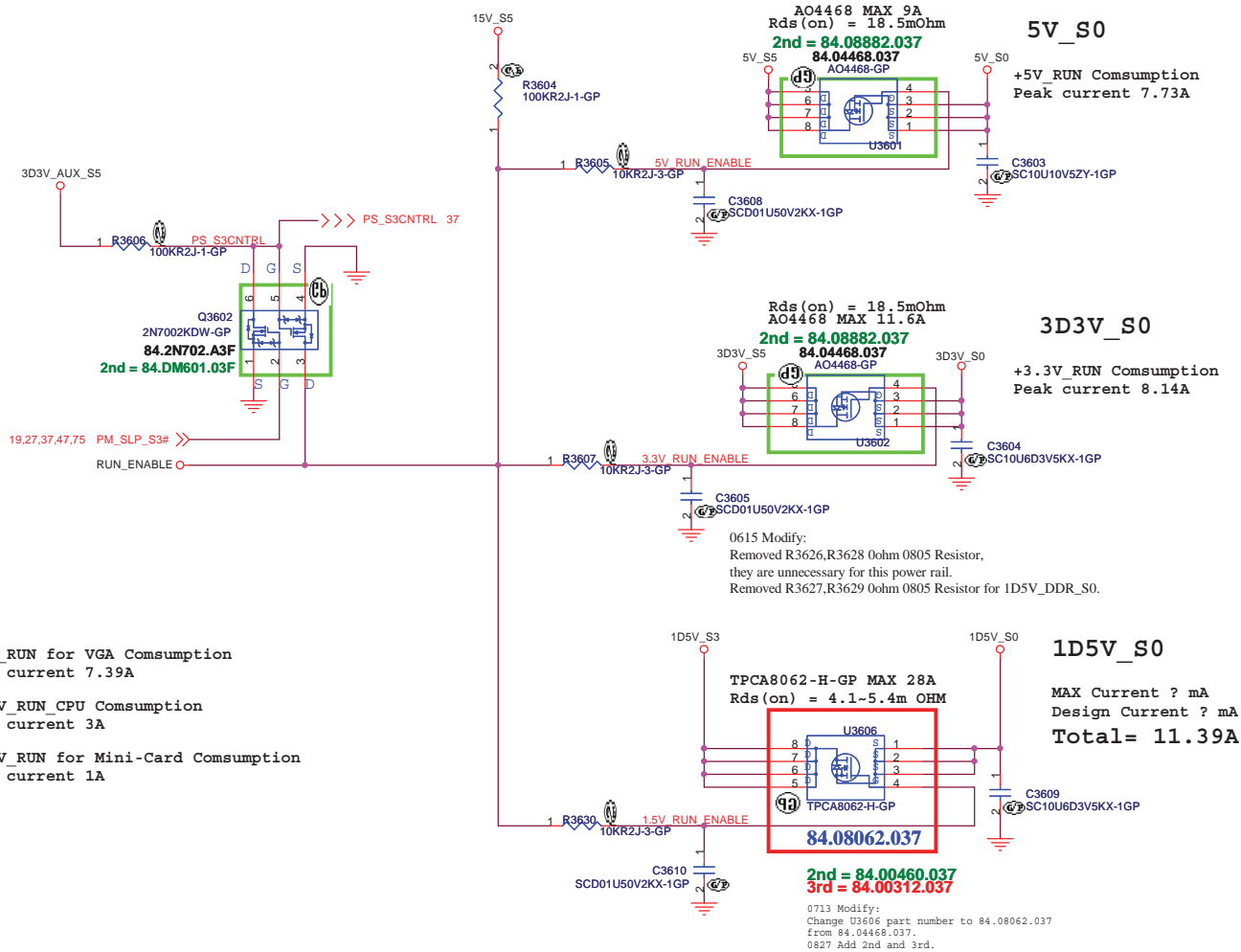
SSID = Reset.Suspend



Power Sequence



ROSA Run Power



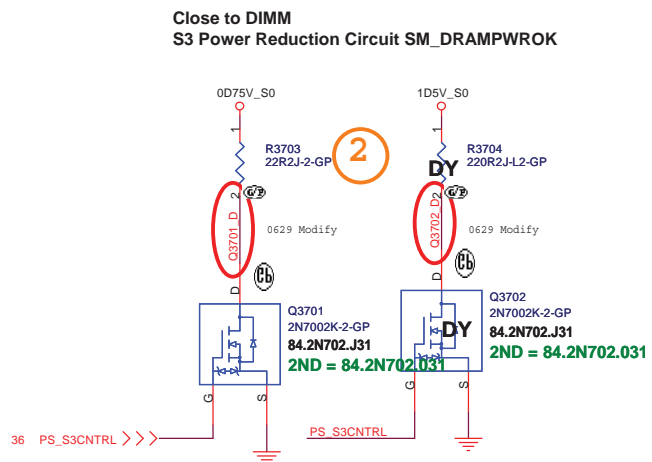
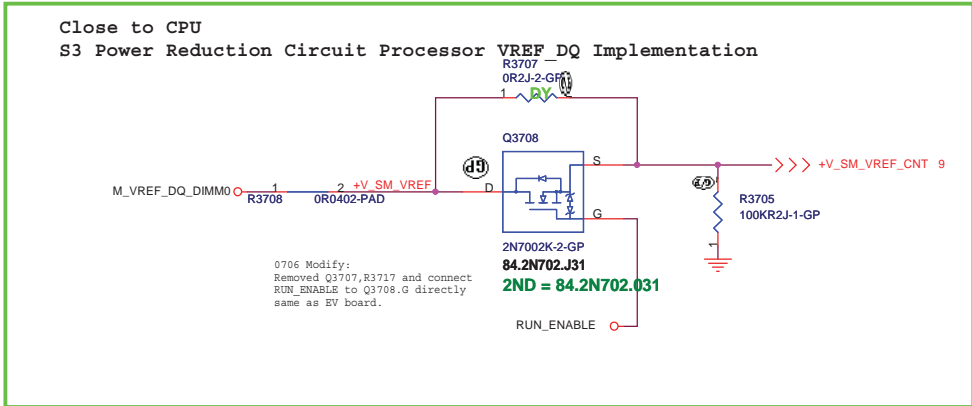
<http://hobi-elektronika.net>

<Core Design>

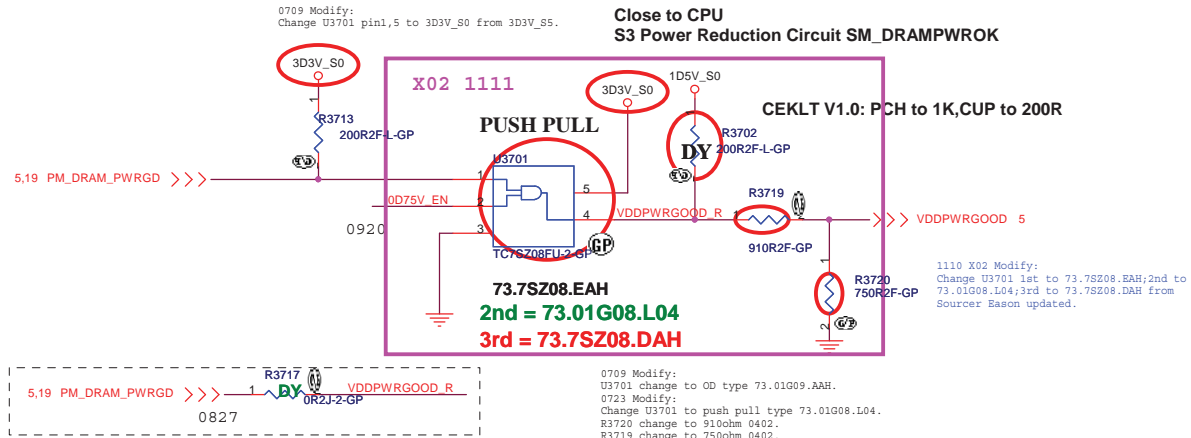
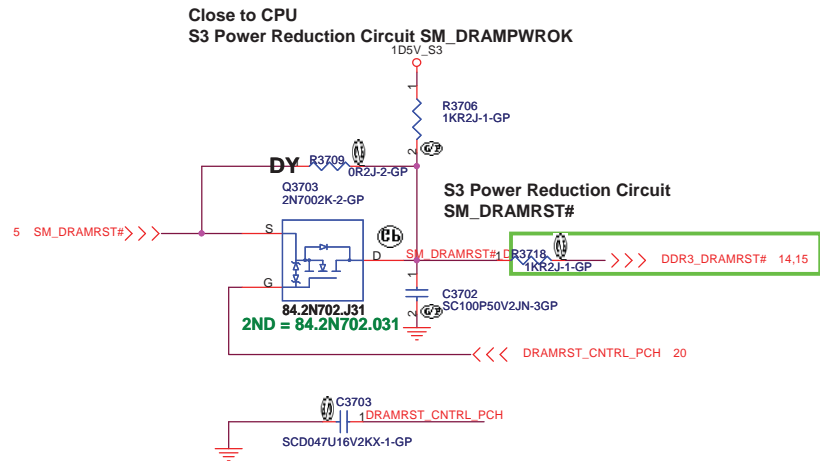
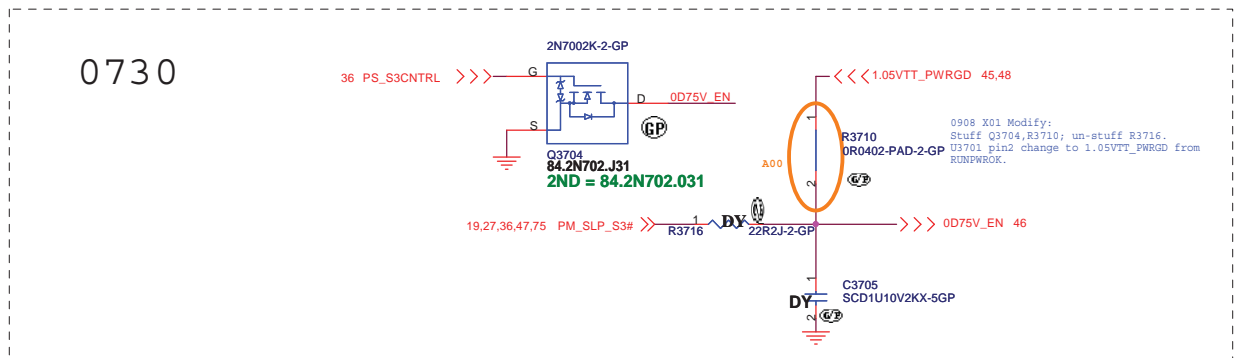
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

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5 S3 Power Reduction X01 20091111



SM DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55; 200mV and the edge must be monotonic

DN15ATI

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

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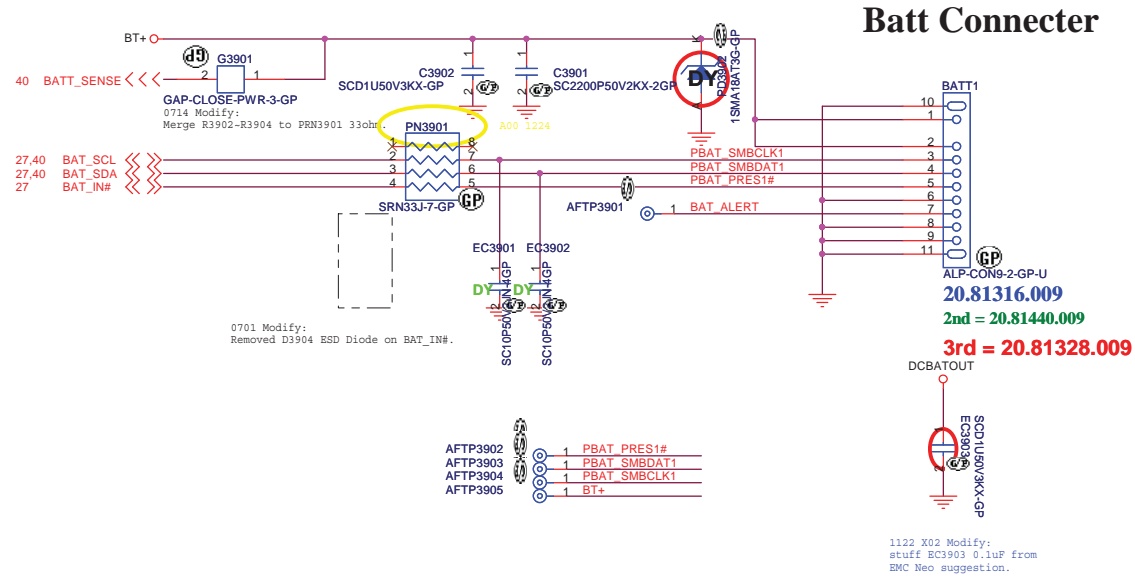
SSID = PWR.Support

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<Core Design>

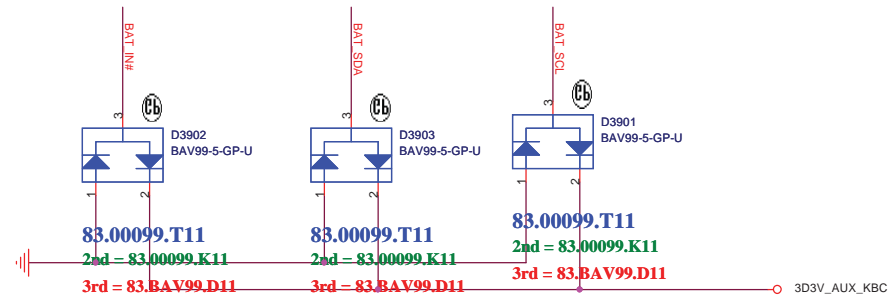


Title		DCIN	
Size	Document Number	Rev	
A3	QUEEN 15	A00	
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For actual location, need to be swap all pin

Close to Batt Connector



0930 X01 Modify:
Change D3901-D3903 main source to 83.00099.T11
for 83.BAV99.D11 shortage issue.

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<Core Design>

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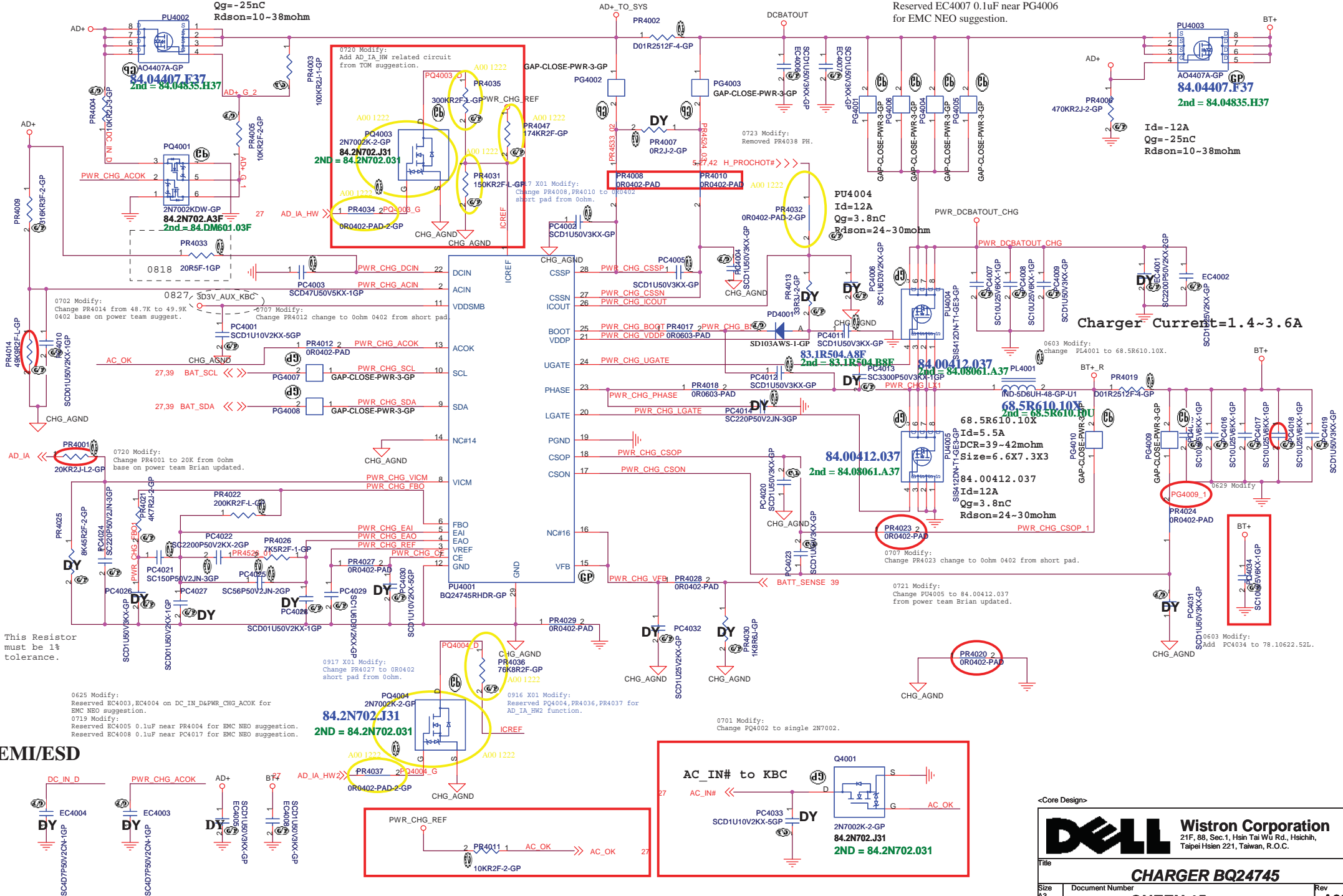
Title		
BATT CONN		
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SSID = Charger

Id=-12A
Qg=-25nC
Rdson=10~38mohm

0719 Modify:
Reserved EC4006 0.1uF near PR4002
for EMC NEO suggestion.

0719 Modify:
Reserved EC4007 0.1uF near PG4006
for EMC NEO suggestion.



Charger Current=1.4~3.6A

This Resistor must be 1% tolerance.

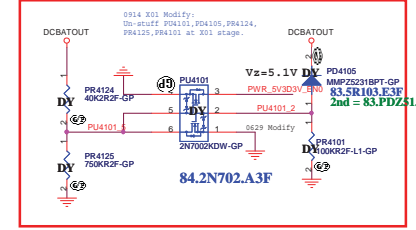
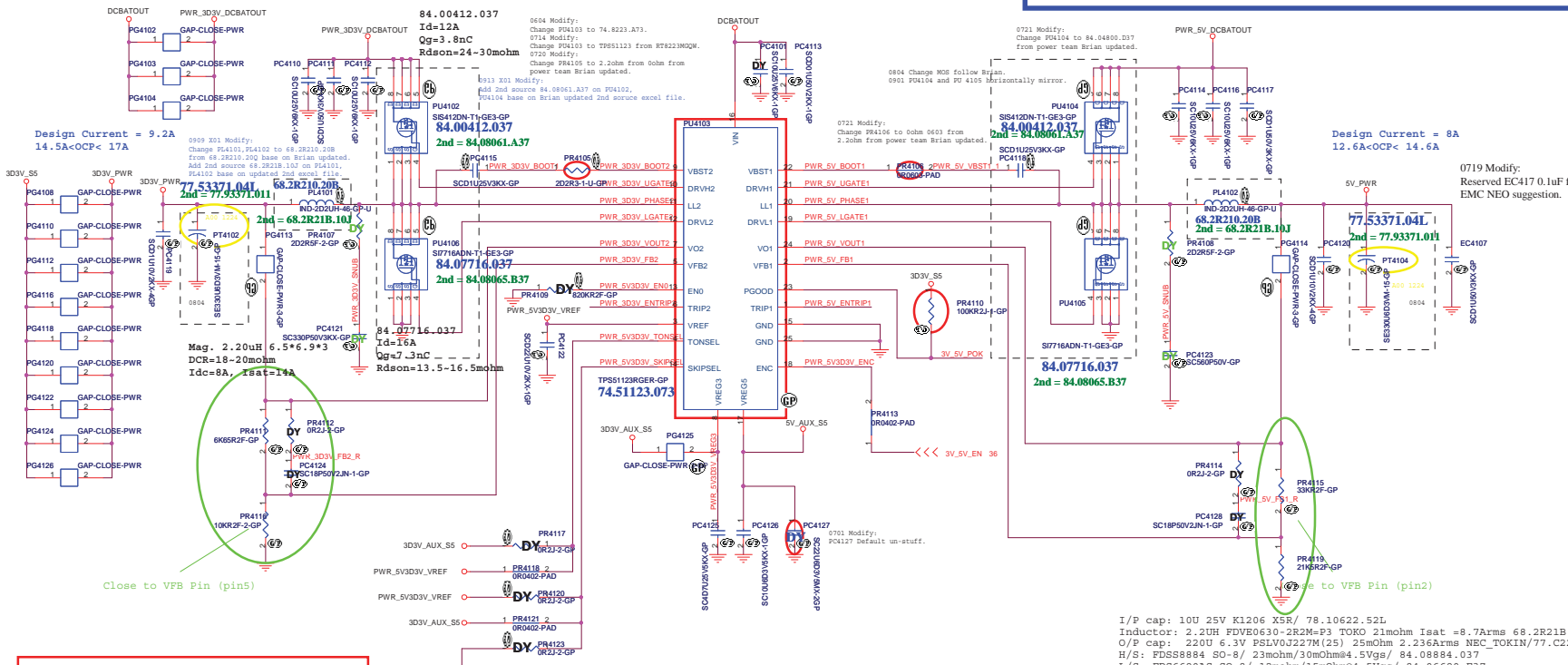
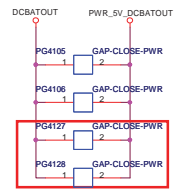
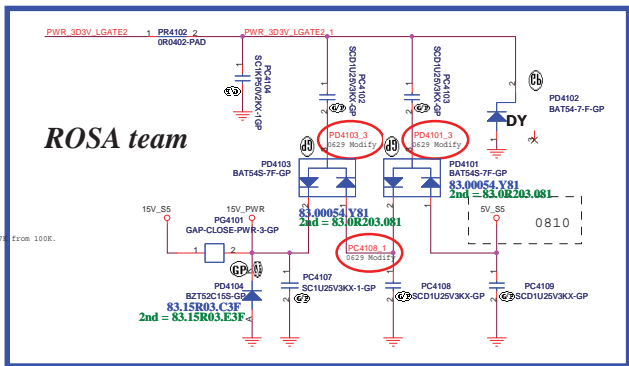
EMI/ESD

<http://hobi-elektronika.net>

<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER BQ24745		Rev
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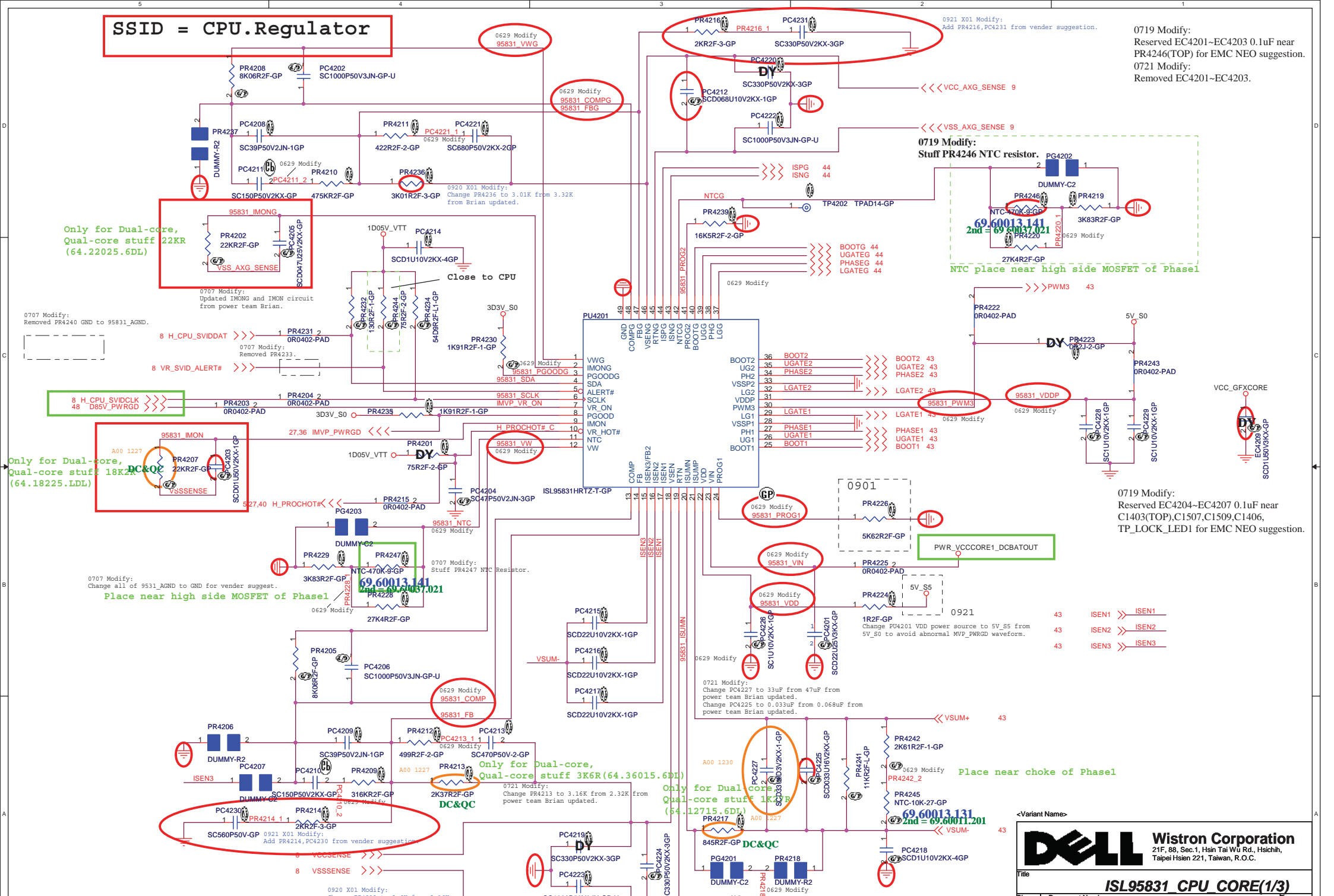


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K1206 XSR/ 79.10622.52L
 Inductor: 2.2uH FDV0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
 H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
 L/S: FDS690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SSSID = CPU.Regulator



0921 X01 Modify:
Add PR4216, PC4231 from vender suggestion

0719 Modify:
Reserved EC4201-EC4203 0.1uF near PR4246(TOP) for EMC NEO suggestion.
0721 Modify:
Removed EC4201-EC4203.

Only for Dual-core,
Qual-core stuff 22K (64.22025.6DL)

0707 Modify:
Removed PR4240 GND to 95831_AGND.

Only for Dual-core,
Qual-core stuff 18K (64.18225.LDL)

0719 Modify:
Stuff PR4246 NTC resistor.
NTC place near high side MOSFET of Phase1

0707 Modify:
Change all of 9531_AGND to GND for vender suggest.
Place near high side MOSFET of Phase1

0719 Modify:
Reserved EC4204-EC4207 0.1uF near C1403(TOP), C1507, C1509, C1406, TP_LOCK_LED1 for EMC NEO suggestion.

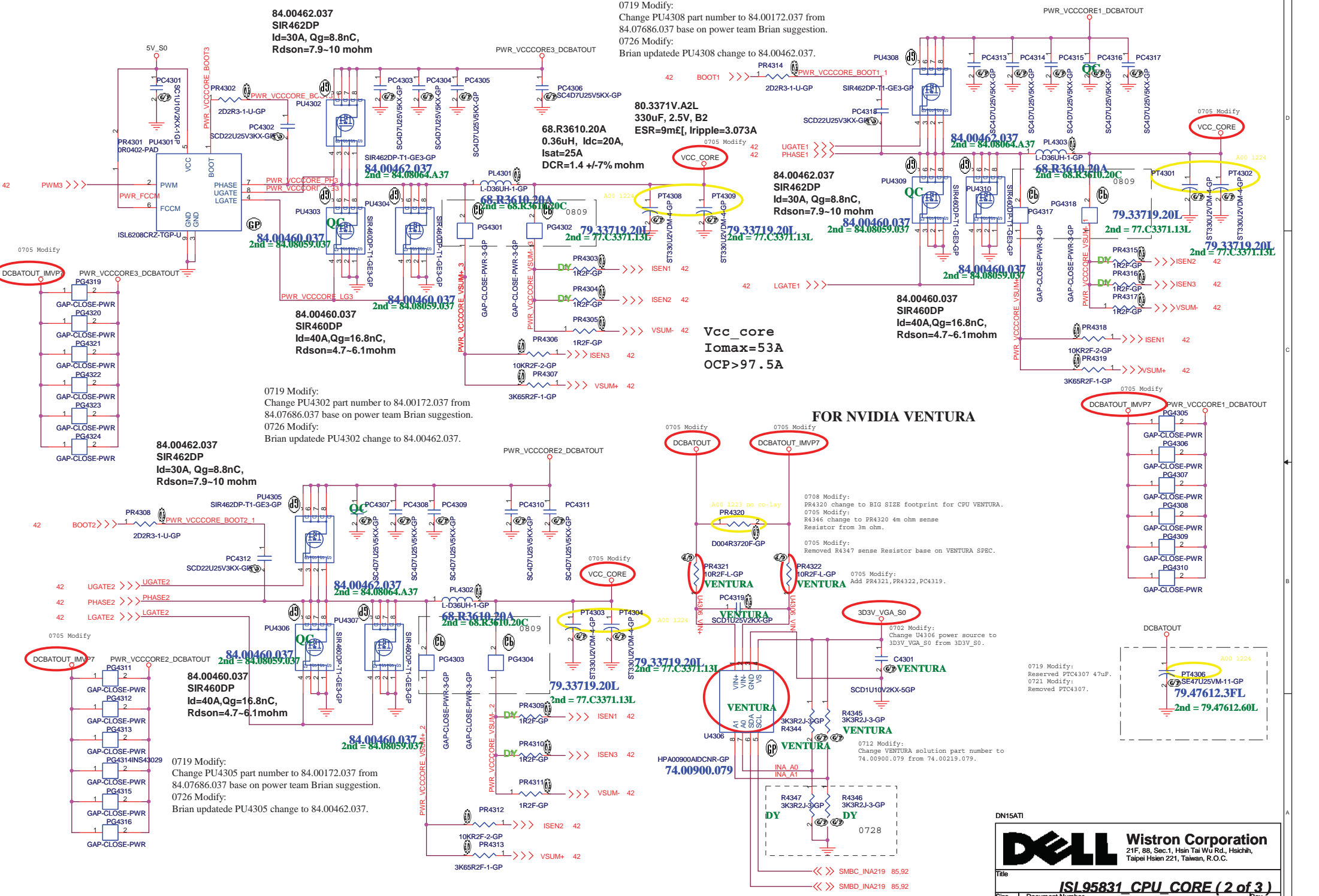
<http://hobi-elektronika.net>

0721 Modify:
Change PU4201 VDD power source to 5V_S5 from 5V_S0 to avoid abnormal MVP_PWRGD waveform.

0721 Modify:
Change PC4227 to 33uF from 47uF from power team Brian updated.
Change PC4225 to 0.033uF from 0.068uF from power team Brian updated.

0721 Modify:
Change PR4217 to 1K from 690ohm from power team Brian updated.

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ISL95831 CPU CORE(1/3)			
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84.00462.037
SIR462DP
 Id=30A, Qg=8.8nC,
 R_{dson}=7.9-10 mohm

0719 Modify:
 Change PU4308 part number to 84.00172.037 from
 84.07686.037 base on power team Brian suggestion.
 0726 Modify:
 Brian updated PU4308 change to 84.00462.037.

80.3371V.A2L
 330uF, 2.5V, B2
 ESR=9mΩ, Irripple=3.073A

84.00462.037
 Id=30A, Qg=8.8nC,
 R_{dson}=7.9-10 mohm

Vcc_core
 I_{omax}=53A
 OCP>97.5A

84.00460.037
SIR460DP
 Id=40A, Qg=16.8nC,
 R_{dson}=4.7-6.1mohm

0719 Modify:
 Change PU4302 part number to 84.00172.037 from
 84.07686.037 base on power team Brian suggestion.
 0726 Modify:
 Brian updated PU4302 change to 84.00462.037.

84.00462.037
SIR462DP
 Id=30A, Qg=8.8nC,
 R_{dson}=7.9-10 mohm

84.00460.037
SIR460DP
 Id=40A, Qg=16.8nC,
 R_{dson}=4.7-6.1mohm

0719 Modify:
 Change PU4305 part number to 84.00172.037 from
 84.07686.037 base on power team Brian suggestion.
 0726 Modify:
 Brian updated PU4305 change to 84.00462.037.

FOR NVIDIA VENTURA

0708 Modify:
 PR4320 change to BIG SIZE footprint for CPU VENTURA.
 0705 Modify:
 R4346 change to PR4321 4m ohm sense
 Resistor from 3m ohm.
 0705 Modify:
 Removed R4347 sense Resistor base on VENTURA SPEC.

0705 Modify:
 Add PR4321, PR4322, PC4319.

0702 Modify:
 Change U4306 power source to
 3D3V_VGA_S0 from 3D3V_S0.

0712 Modify:
 Change VENTURA solution part number to
 74.00900.079 from 74.00219.079.

DN15AT1

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Title **ISL95831 CPU CORE (2 of 3)**

Size Custom Document Number **QUEEN 15** Rev **A00**

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Would be instead of INA219 by HPA00900

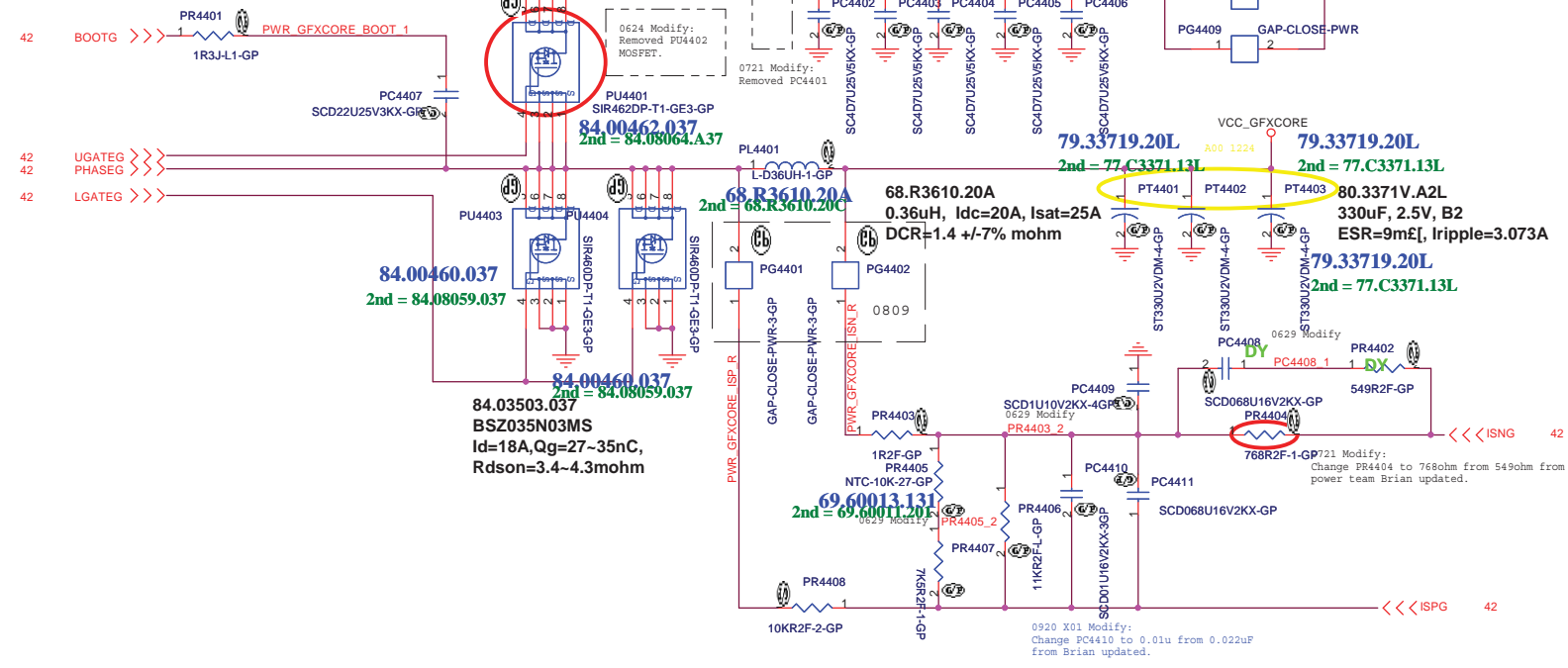
0705 Modify

DCBATOUT_IMVP7

PWR_GFXCORE_DCBATOUT

0719 Modify:
 Change PU4401 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.
 0720 Modify:
 Change PU4401 part number to 84.00462.037 from 84.00172.037 base on power team Brian suggestion.

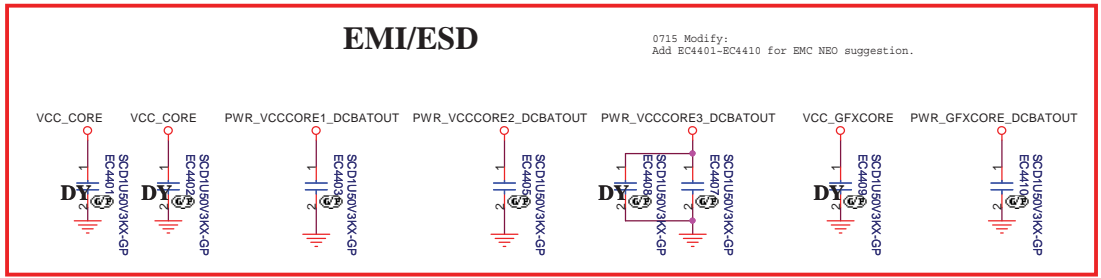
84.00462.037
SIR462DP-T1-GE3-GP
 Id=30A, Qg=8.8nC,
 Rds(on)=7.9 mohm



VCC_GFXCORE
 I_{omax}=33A
 OCP>50A

EMI/ESD

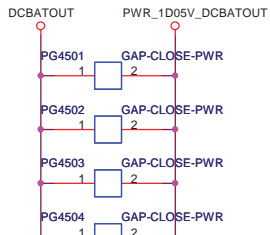
0715 Modify:
 Add EC4401-EC4410 for EMC NEO suggestion.



DN15ATI

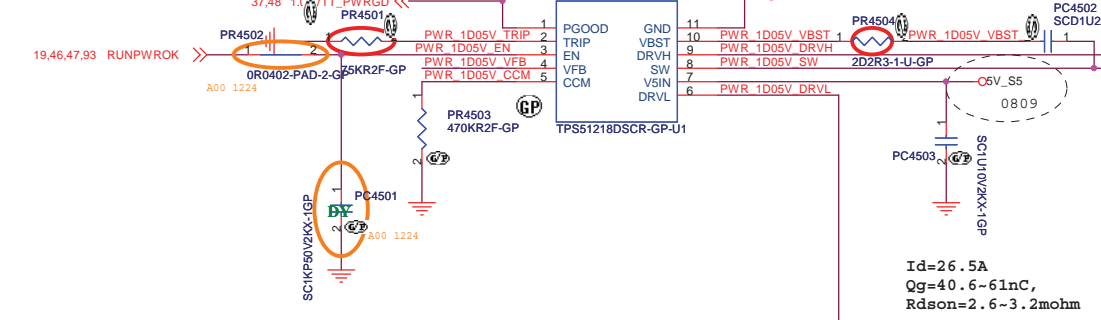


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TPS51218 for 1D05V

1123 X02 Modify:
Change PR4501 to 75K from 45.3K
for 1.05V OCP set to 20A from Brian.



84.00172.037
BSZ115N03MSC
Id=20A, Qg=9.8nC,
Rdson=8.9 mOhm

Id=26.5A
Qg=40.6-61nC,
Rdson=2.6-3.2mOhm

0719 Modify:
Change PU4502 part number to 84.00172.037 from
84.07686.037 base on power team Brian suggestion.

1122 X02 Modify:
stuff EC4501 0.1uF from
EMC Neo suggestion.

84.00172.037
2nd = 84.08065.037

0909 X01 Modify:
Change PL4501 to 68.2R210.20C
from IND-D56UH-27-GP base on
Brian updated.

84.00460.037
2nd = 84.08059.037

0721 Modify:
Brian suggest change PU4503 to 84.00460.037.
Change PR4506 to 9.76K from 10K from
power team Brian updated.

Mag. 2.20uH 10*11.5*4
DCR=6.7-7mOhm
Idc=12A, Isat=27A

Design Current = 9.9A
15.6A<OCP< 18.3A

79.3971V.30L
2nd = 77.93971.02L

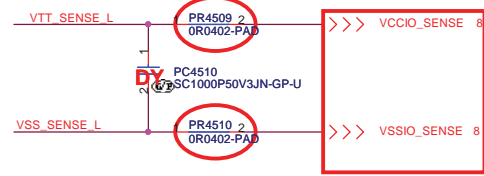
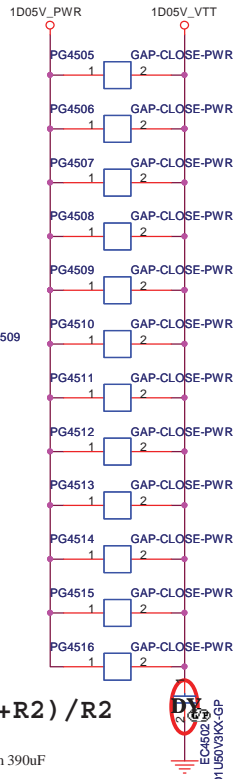
$$V_{out} = 0.704V * (R1 + R2) / R2$$

0617 Modify:
Joseph Change PTC4502 to 330uF from 390uF
base on layout placement status.

0721 Modify:
Brian Add PC4511 1uF. Reserved EC4502, EC4503 0.1uF near
PG4516(TOP) for EMC NEO suggestion.

0901 X01 Modify:
Change PTC4502 to 79.3971V.30L from
79.33719.L01 from power team Brian updated.
0913 X01 Modify:
Add 2nd source 77.93971.02L on PTC4502
base on Brian updated 2nd source excel file.

0727 Modify:
PR4505, PR4508 change to 100ohm from 10ohm.
stuff PR4509, PR4510 0ohm from Brian updated.



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Title: **TPS51218 +1.05V VTT**

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0719 Modify:
Change PU4602 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.

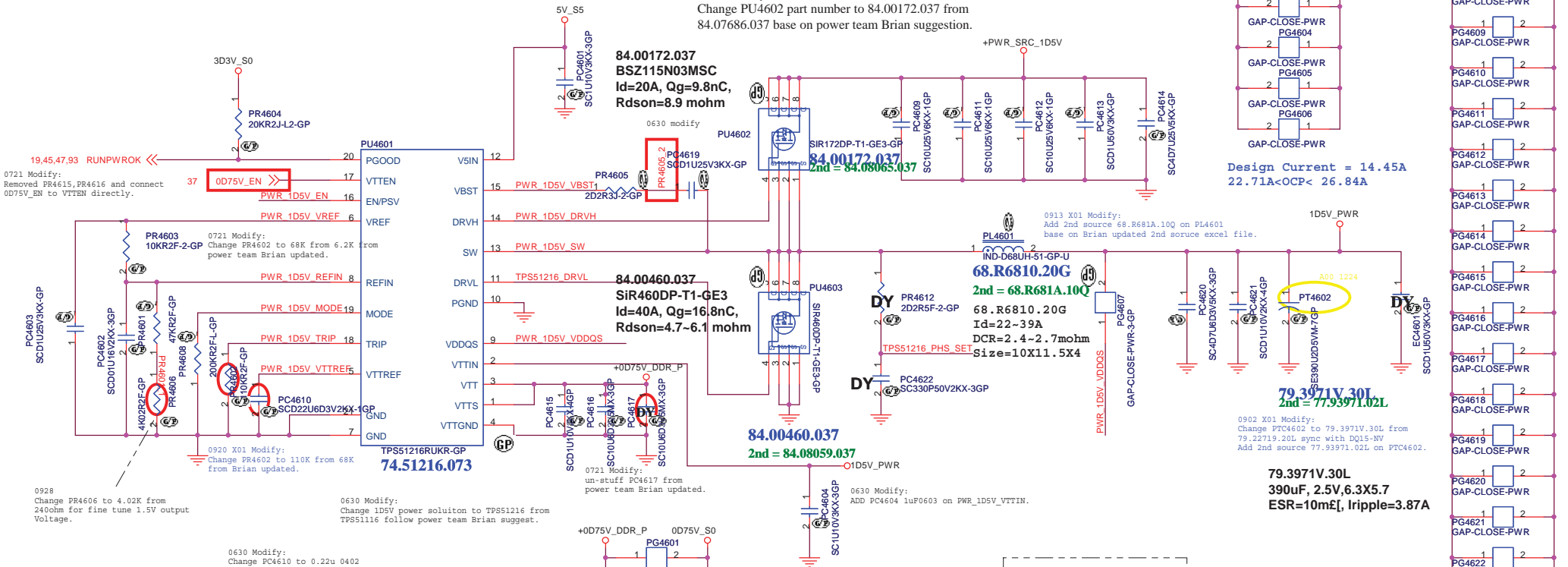
84.00172.037
BSZ115N03MSC
Id=20A, Qg=9.8nC,
Rdson=8.9 mohm

84.00460.037
SIR460DP-T1-GE3
Id=40A, Qg=16.8nC,
Rdson=4.7-6.1 mohm

Design Current = 14.45A
22.71A < OCP < 26.84A

79.3971V.30L
2nd = 77.93971.02L

79.3971V.30L
390uF, 2.5V, 6.3X5.7
ESR=10mE[, Iripple=3.87A



0721 Modify:
Removed PR4615, PR4616 and connect 0D75V_EN to VTTEN directly.

0721 Modify:
Change PR4602 to 68K from 6.2K power team Brian updated.

0920 X01 Modify:
Change PR4602 to 110K from 68K from Brian updated.

0928
Change PR4606 to 4.02K from 240ohm for fine tune 1.5V output Voltage.

0630 Modify:
Change 1D5V power solution to TPS51216 from TPS51116 follow power team Brian suggest.

0630 Modify:
Change PC4610 to 0.22u 0402 from 0603 from Brian.

0721 Modify:
un-stuff PC4617 from power team Brian updated.

0630 Modify:
ADD PC4604 1uF0603 on PWR_1D5V_VTTIN.

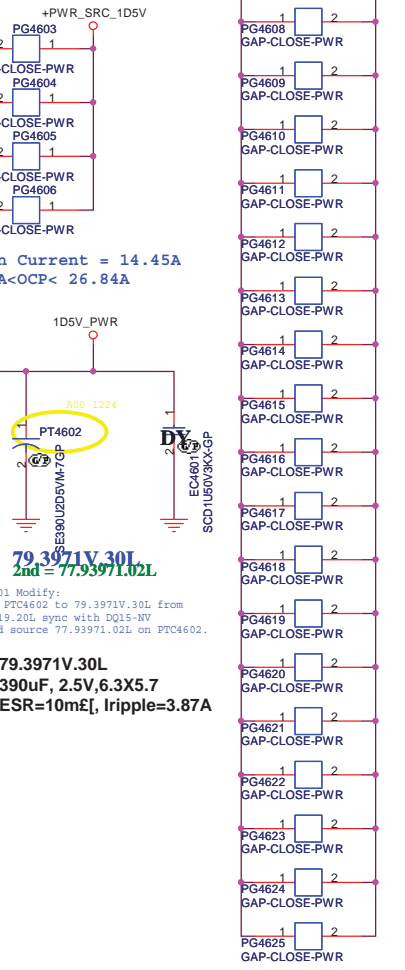
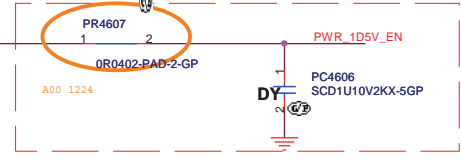
0721 Modify:
Removed PR4615, PR4616 and connect 0D75V_EN to VTTEN directly.



0702 Modify:
Add PR4611 0ohm 0603 pad on PWR_1D5V_VTTREF.

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR5003	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	Non-tracking Discharge
68k ohm	400kHz	
47k ohm		



<Variant Name>

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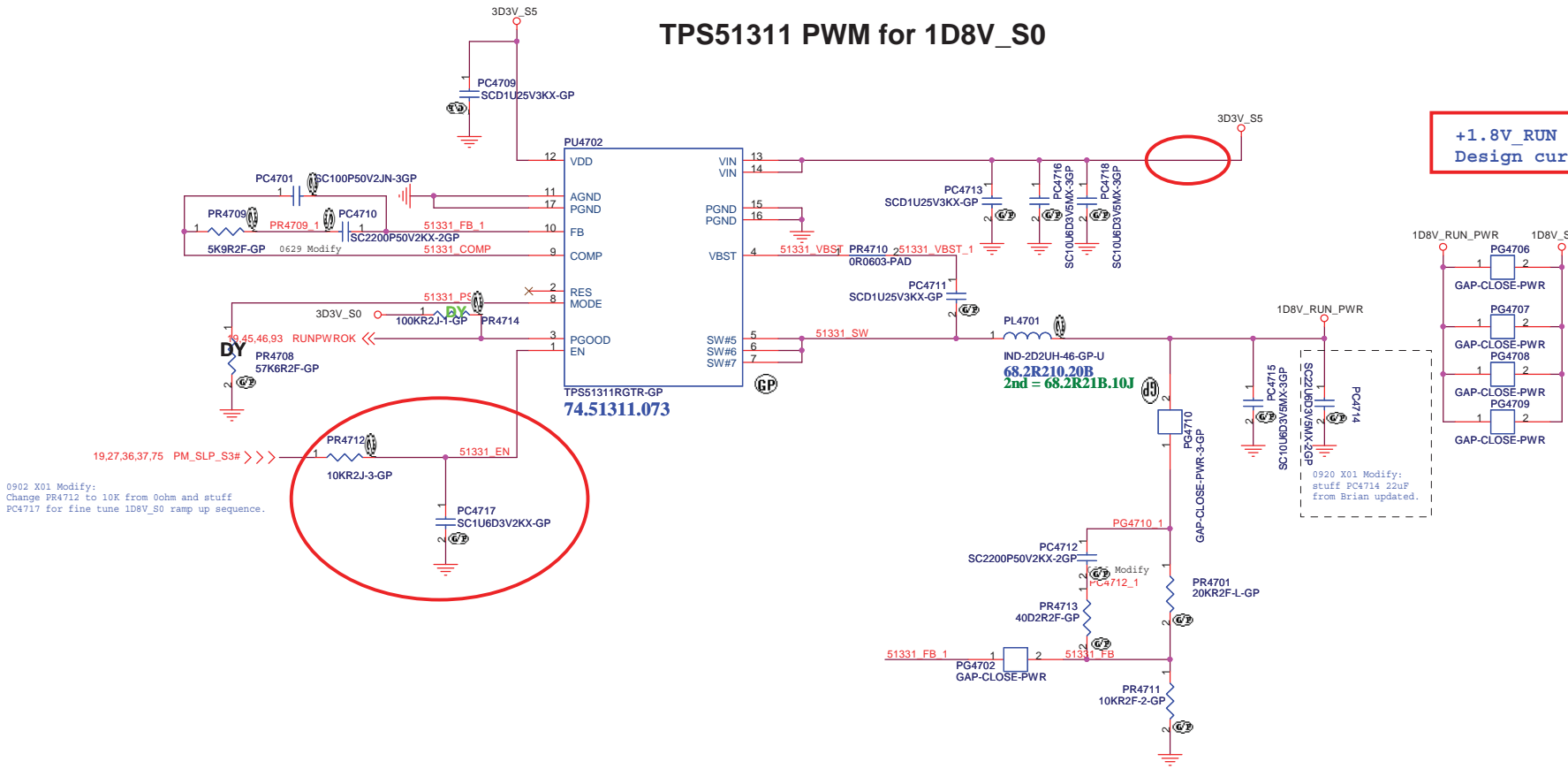
Title: **TPS51116 +1.5V SUS**

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SSID = PWR.Plane.Regulator_1D8V_S0

TPS51311 PWM for 1D8V_S0

+1.8V_RUN
Design current = 2.7985A



0902 X01 Modify:
Change PR4712 to 10K from 0ohm and stuff
PC4717 for fine tune 1D8V_S0 ramp up sequence.

0920 X01 Modify:
stuff PC4714 22uF
from Brian updated.

DN15ATI Whister

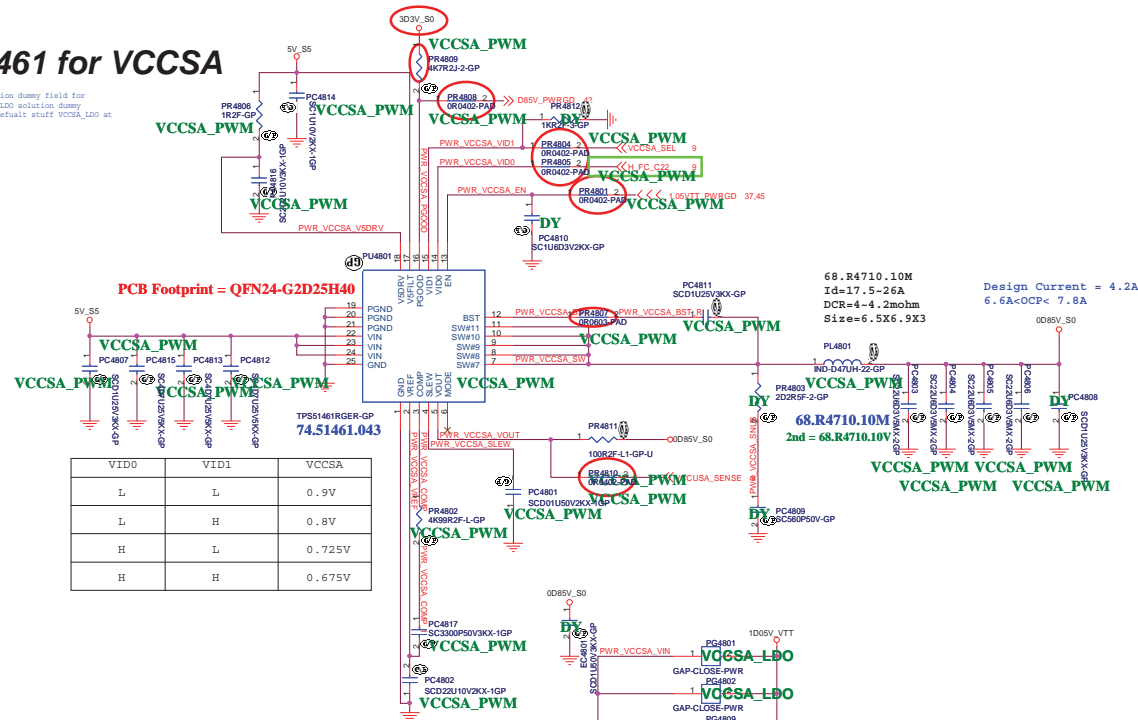
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Title: **TPS51311 for 1D8V_S0**

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TPS51461 for VCCSA

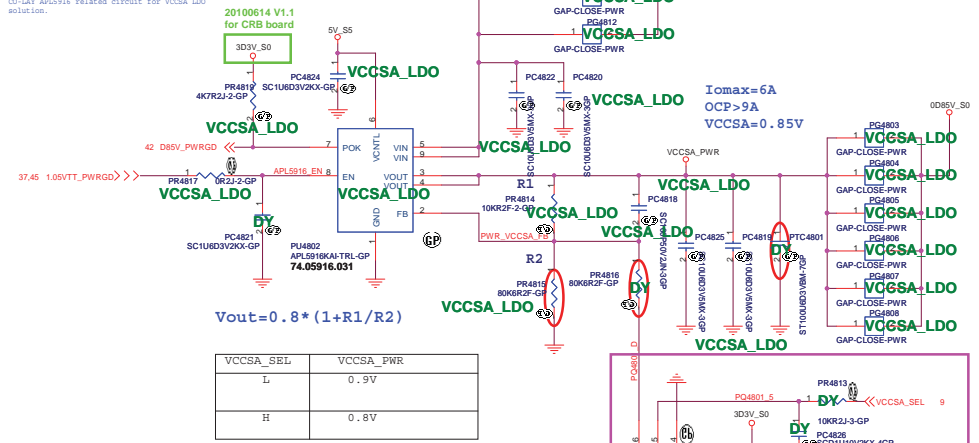
1112 X02 Modify:
set TPS51461 PWM solution dummy field for
VCCSA_PWM and APL5916 LDO solution dummy
field for VCCSA_LDO. default stuff VCCSA_LDO at
GP stage.



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

APL5916 for VCCSA

1112 X02 Modify:
CO-LAY APL5916 related circuit for VCCSA LDO
solution.



VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

$$V_{out} = 0.8 * (1 + R1/R2)$$

<Core Design>

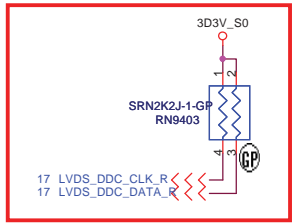
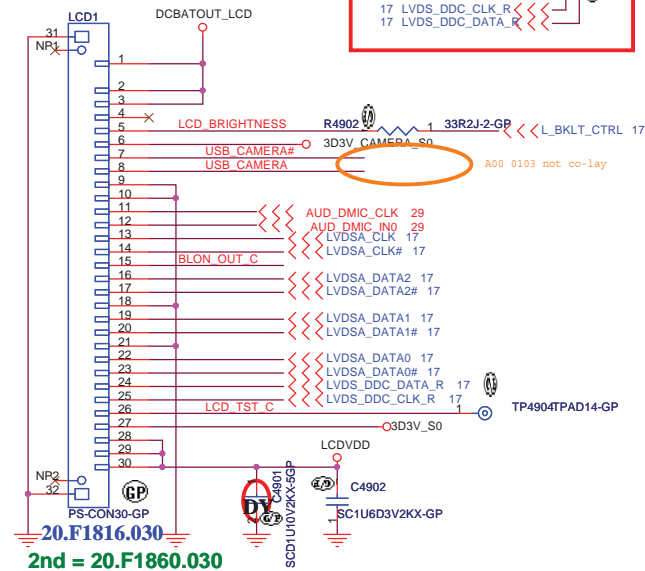
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File		TPS51461 VCCSA	
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SSID = VIDEO

0909 X01 Modify:
Change LCD1 to 20.F1816.030 for 30pin
Re-assign LCD1 pin define base on Roy updated
cable pin define list.

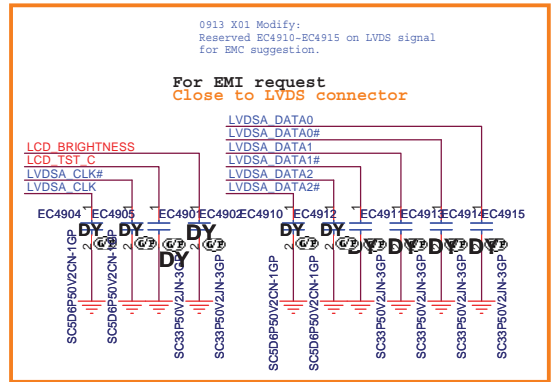
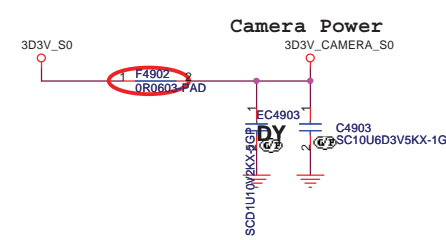
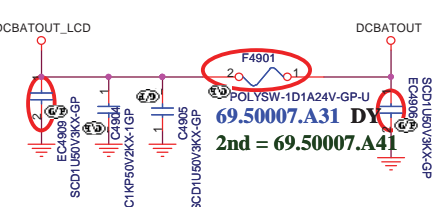
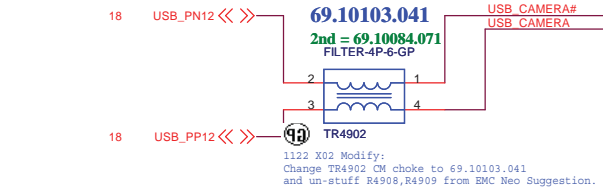
LVDS CONNECTOR



(MB Pin Define)

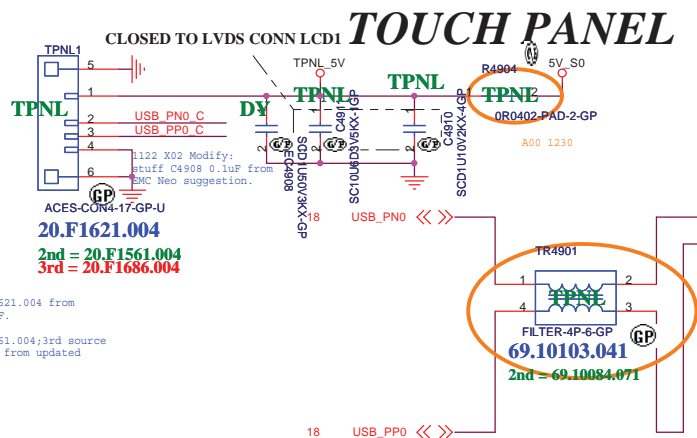
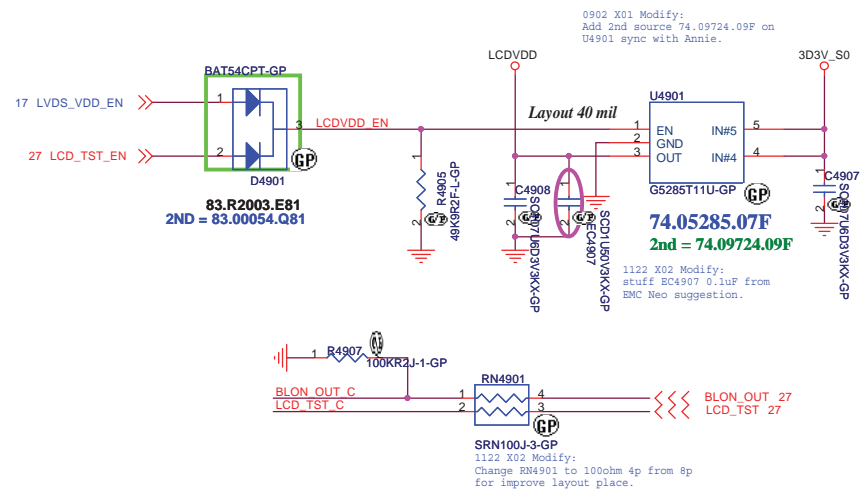
MB CONN. (WIRE)

Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	NC
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	BLON_OUT_C
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD



SSID = VIDEO

LCD POWER for ROSA



0916 X01 Modify:
Change TPNL1 to 20.F1621.004 from
Double updated EMN&DXF.
0917 X01 Modify:
Add 2nd source 20.F1561.004; 3rd source
20.F1686.004 on TPNL1 from updated
connector list.

DN15ATI Whistler

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File
LCD Connector


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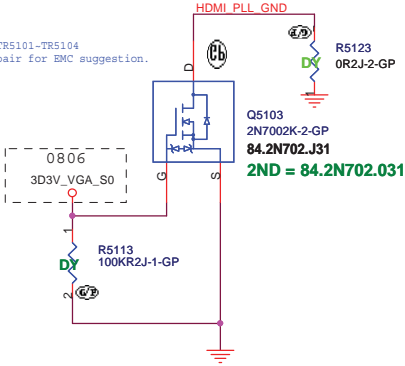
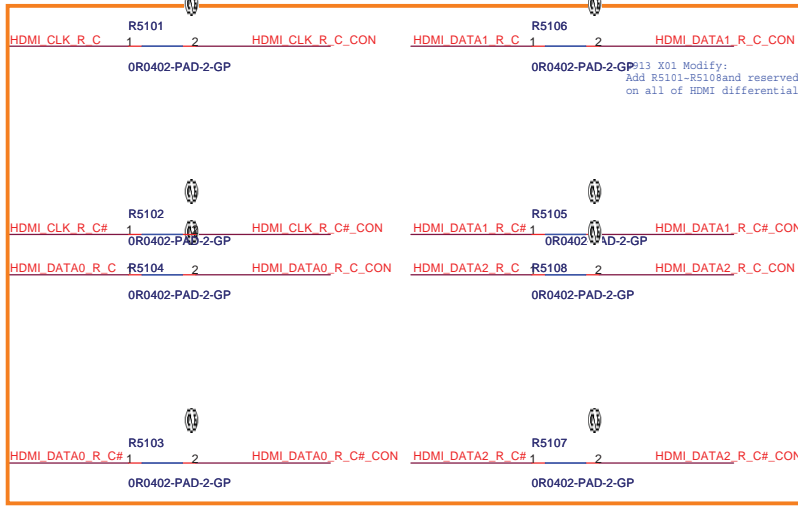
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<Variant Name>

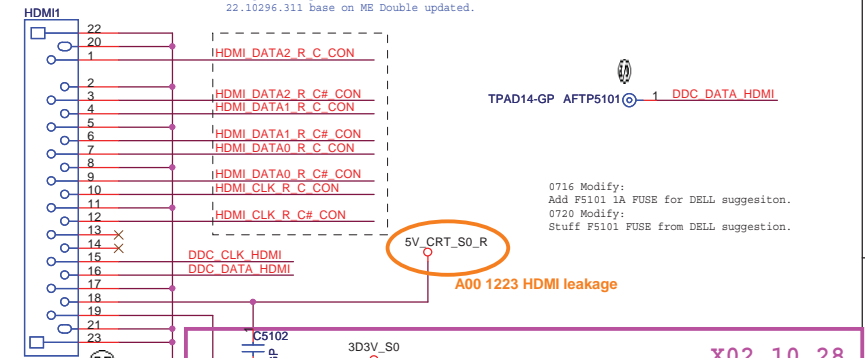
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CRT Connector		
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SSID = VIDEO

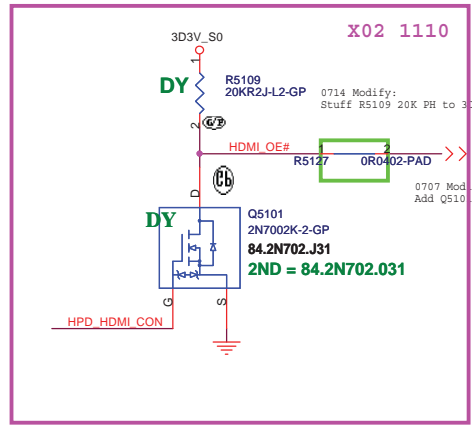
HDMI Level Shifter & CONNECTOR



HDMI CONN



Close to HDMI Connector



Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<http://hobi-elektronika.net>


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Title: **HDMI Level Shifter/Connector**

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<Core Design>

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Title			
Reserved			
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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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SSID = User.Interface

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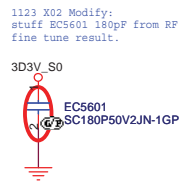
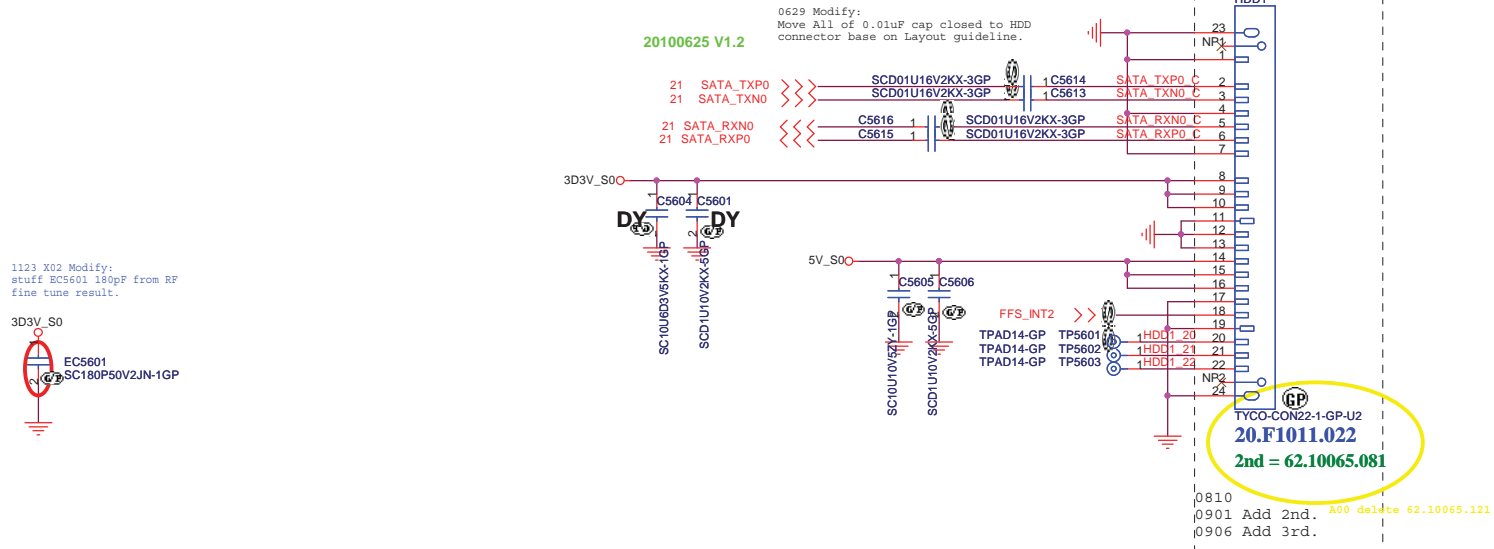
<Core Design>



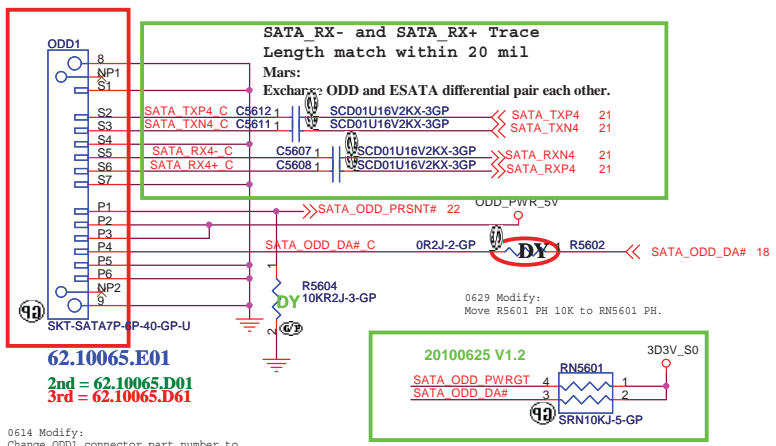
Title		
ITP/Fan Connector		
Size	Document Number	Rev
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SSID = SATA

SATA HDD Connector

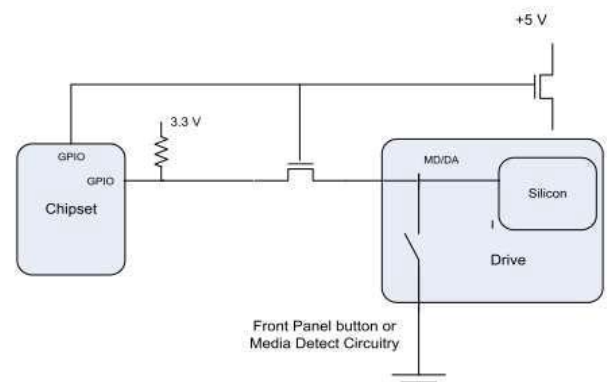


ODD Connector

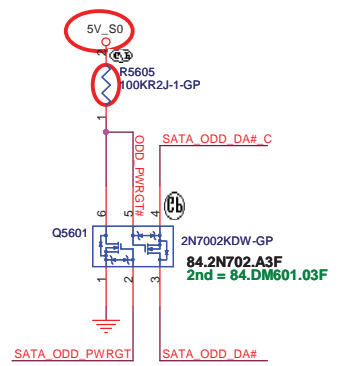


0614 Modify:
Change ODD1 connector part number to 22.10300.421 base on ME BMN and DXF.
0707 Modify:
Change ODD1 connector part number to 62.10065.E01 base on latest BMN and DXF.

SUPPORT ZERO SATA ODD

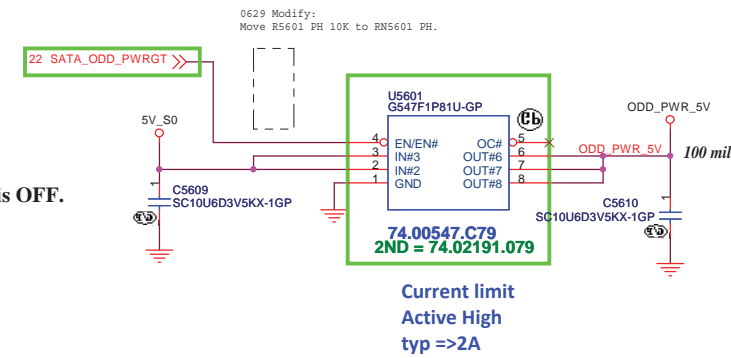


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



0707 Modify:
Change R5605 to 100K, 2W for 100K, 1W (P2) instead between PCH and ODD.
<http://hobi-elektronika.net>

SATA Zero Power ODD



<Variant Name>

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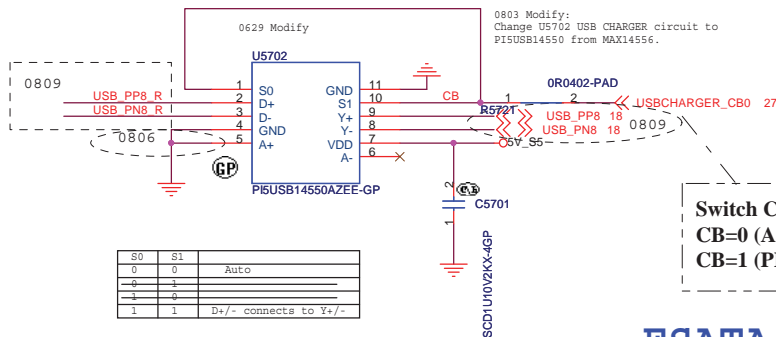
Title: **HDD/ODD**

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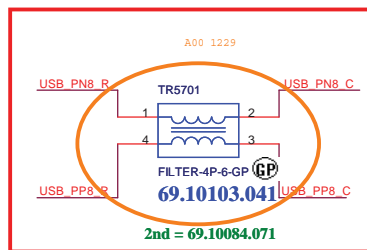
SSID = ESATA

USB CHARGER

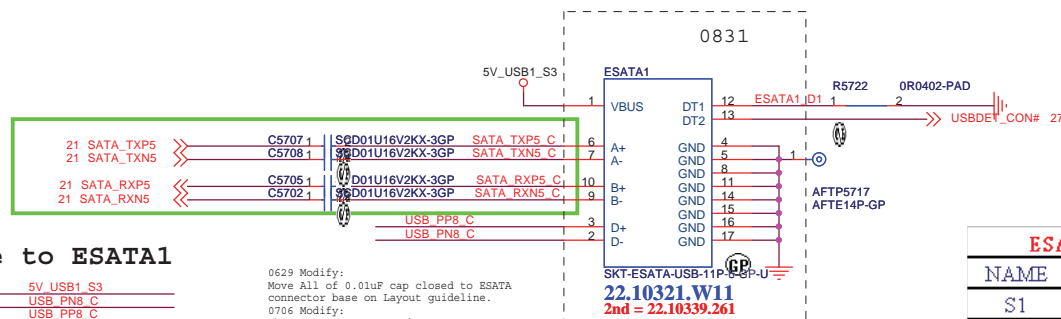


Switch Control Bit:
CB=0 (AM): auto detection charger identification active.
CB=1 (PM): connect DP/DM to TDP/TDM.

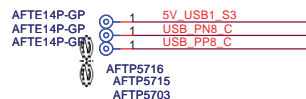
1122 X02 Modify:
 Change TR5701CM choke to 69.10103.041 and un-stuff R5718, R5719 from EMC Neo Suggestion.
 1123 X02 Modify:
 Change R5718, R5719 to 0603 from 0402.



ESATA CONN



close to ESATA1



E-SATA USB 2.0 Combo
CE/H=-0.16/2.83mm with detect function

ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

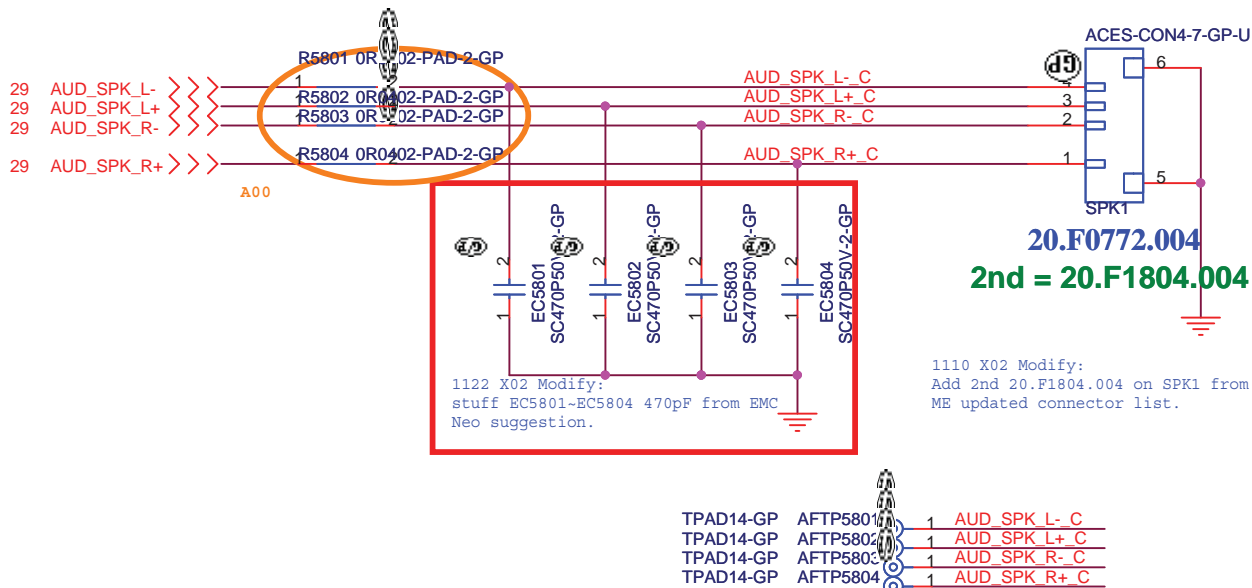
<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title ESATA		
Size A3	Document Number QUEEN 15	Rev A00
Date: Tuesday, January 04, 2011	Sheet 57 of 108	

SSID = AUDIO

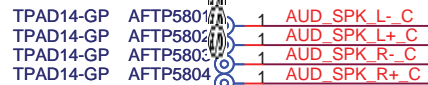
Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

0913 X01 Modify:
 Change SPK1 to 20.F0772.004 from
 20.F1647.004 from Double updated.
 0914 X01 Modify:
 Re-assign SPK1 pin define base on
 Roy updated excel file for 20.F0772.004

1110 X02 Modify:
 Add 2nd 20.F1804.004 on SPK1 from
 ME updated connector list.



<Core Design>




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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
SPEAKER CONN		
Size A4	Document Number QUEEN 15	Rev A00
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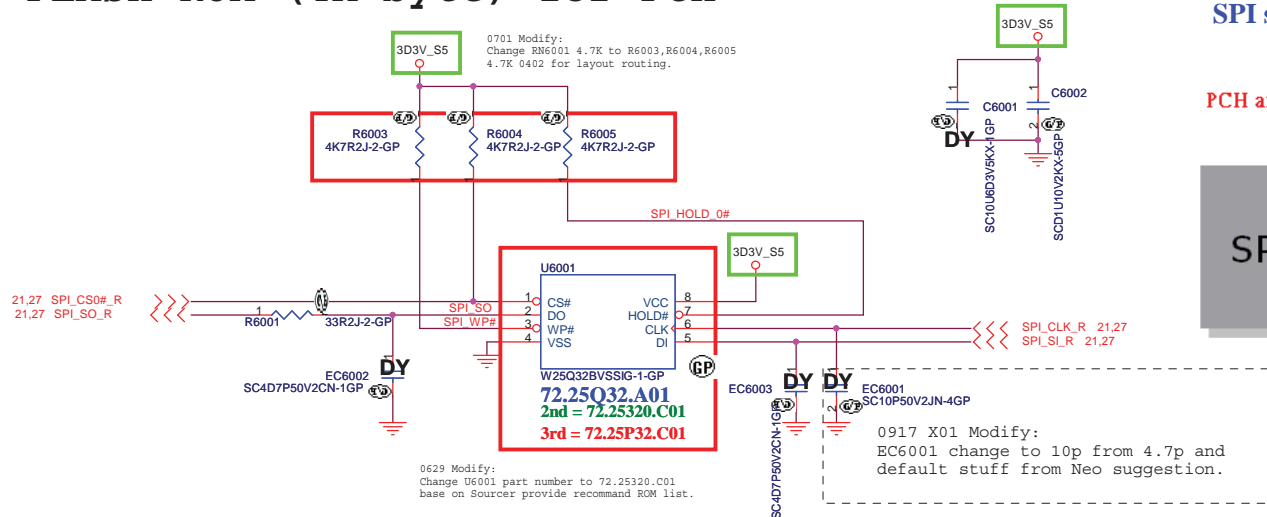
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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

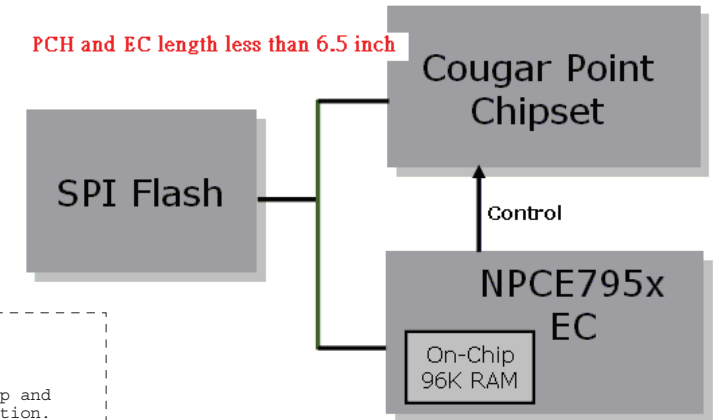


0629 Modify:
Change U6001 part number to 72.25320.C01
base on Sourcer provide recommend ROM list.

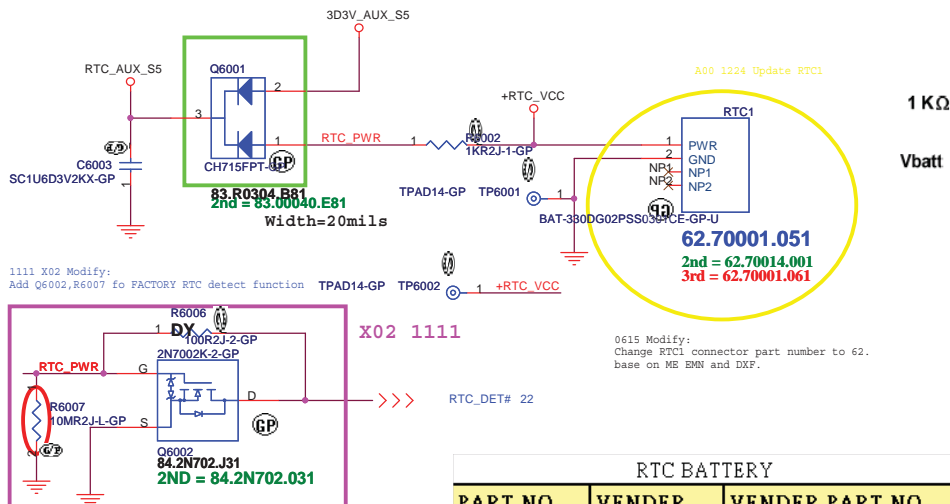
	Priority	Wistron P/N	Manufacturer	Vendor P/N
X02	1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
	2	72.25320.C01	MXIC	MX25L3206EM2L-12G
X02	3	72.25P32.C01	Numonyx	M25PX32-VMW6F

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT

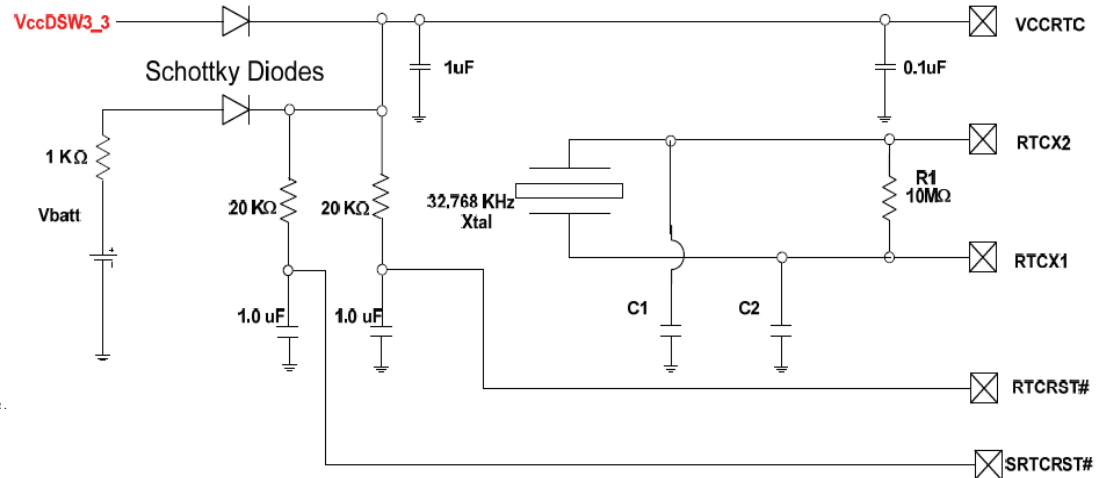


1111 X02 Modify:
Add Q6002, R6007 to FACTORY RTC detect function TPAD14-GP TP6002

0615 Modify:
Change RTC1 connector part number to 62.
base on ME EMN and DXF.

RTC BATTERY		
PART NO	VENDER	VENDER PART NO.
23.20023.311	MITSUBISHI	CR2032 MITSUBISHI
23.20023.341	HENSHEN	CR-2032L/DBE
23.20068.001	KTS	BBBCR2032BX

<http://hobi-elektronika.net>



VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

<Variant Name>

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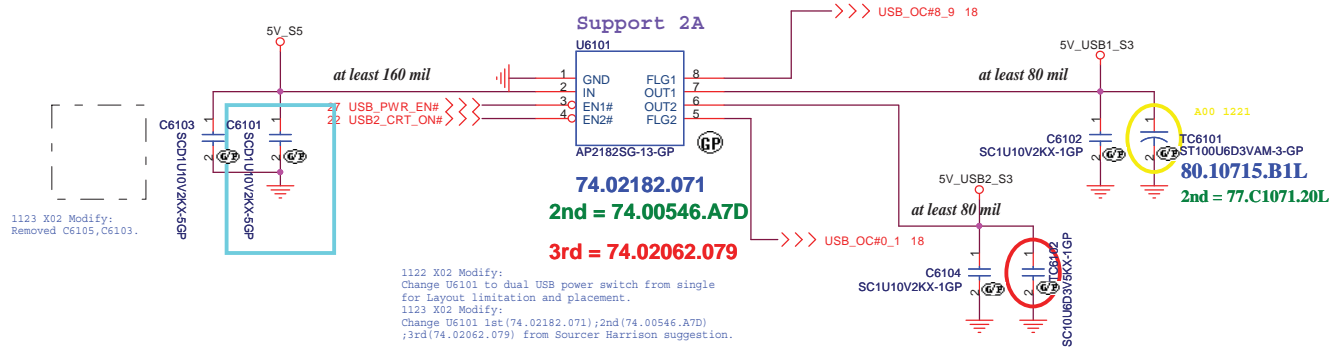
Title: **Flash/RTC**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

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SSID = USB

CRT Board and COMBO USB Power



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<Core Design>


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Title: **USB Power SW**

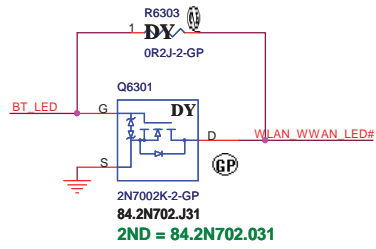
Size	Document Number	Rev
	QUEEN&NIRVANA 15	A00
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<Core Design>

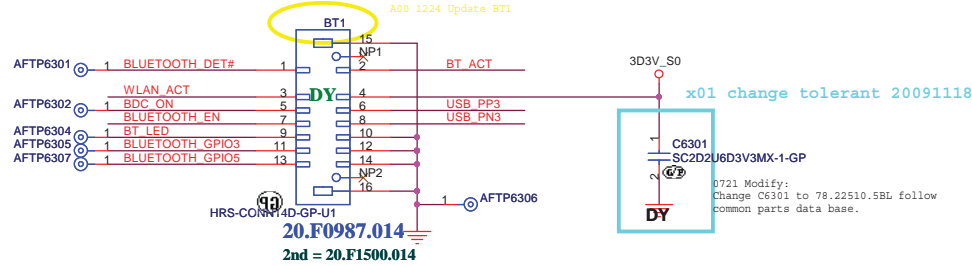
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
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SSID = User.Interface



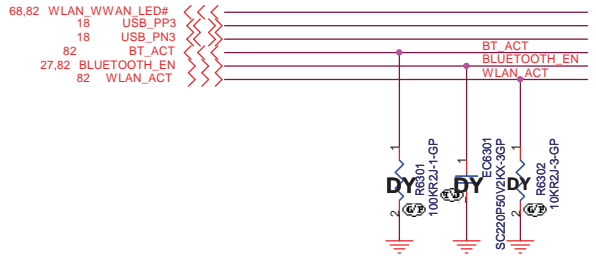
0722 Modify:
Add Q6301 and combine BT_LED to
WLAN_WWAN_LED#.

Bluetooth Module conn.



x01 change tolerant 20091118

0721 Modify:
Change C6301 to 78.22510.58L follow
common parts data base.



- AFTP6309 1 WLAN_ACT
- AFTP6310 1 BLUETOOTH_EN
- AFTP6308 1 BT_ACT
- AFTP6311 1 3D3V_S0
- AFTP6312 1 USB_PP3
- AFTP6313 1 USB_PN3

0709 Modify:
PM confirmed there is no stand-alone BT module,
so DF BT1 connector, add BT enable signal
and 5V_S5 power option on WLAN connector pin 51.
0712 Modify:
Stuff BT relatek component to verify function.

<Core Design>

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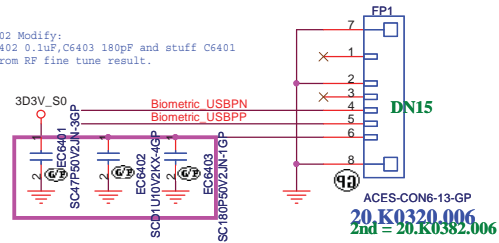
Title: **Bluetooth**

Size: A3	Document Number: QUEEN 15	Rev: A00
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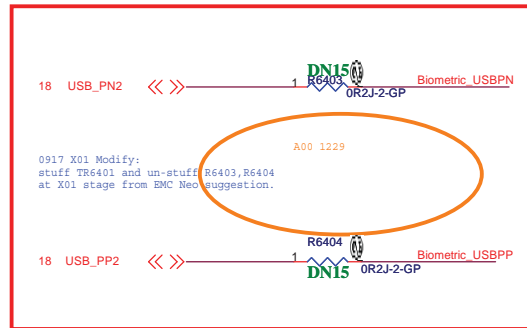
Finger Printer Connector

0707 Modify:
Add FP_DET# signal on FP1 pin1.
0715 Modify:
Add FP_DET# signal on FP1 pin1.
0806 Swap pin.
0810 Change to 4 pin.
0827 Change to 6 pin.

1123 X02 Modify:
Add C6402 0.1uF, C6403 180pF and stuff C6401
47pF from RF fine tune result.



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0



0917 X01 Modify:
stuff TR6401 and un-stuff R6403, R6404
at X01 stage from EMC Neo suggestion.

AFTP42 1 3D3V_S0
AFTP43 1 Biometric_USBPN
AFTP44 1 Biometric_USBPP


0615 Modify:
Change FP1 connector part number to 20.K0320.004
base on ME EMN and DXF.
0630 Modify:
Change FP1 connector part number to 20.K0320.006
base on ME EMN and DXF.
0707 Modify:
Reassign Finger print pin define base on EXCEL FILE.
0713 Modify:
Reassign Finger print pin define base on EXCEL FILE.
Removed FP_DET# on FP1.

<Core Design>

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Title			
RESERVED			
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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RESERVED		
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<Core Design>



Title		Reserved	
Size	Document Number	Rev	
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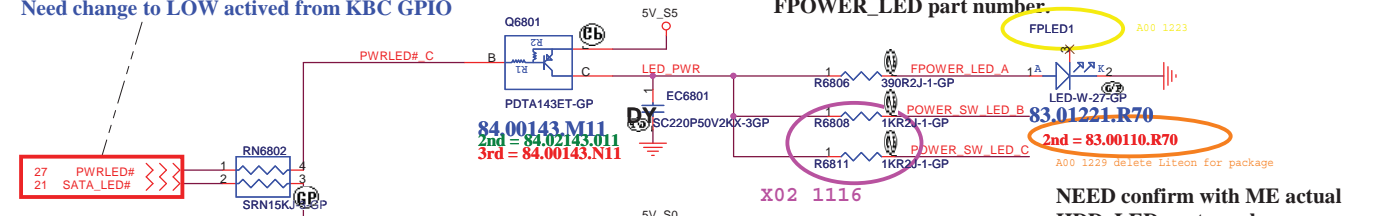
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
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SSID = User.Interface

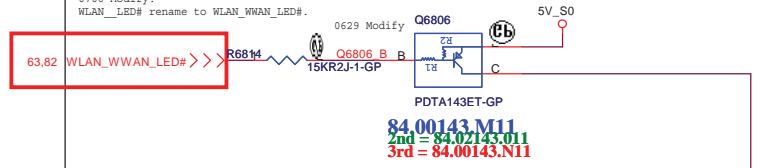
FRONT POWER LED

Need change to LOW acted from KBC GPIO



WLAN_LED

0706 Modify:
WLAN_LED# rename to WLAN_WWAN_LED#.



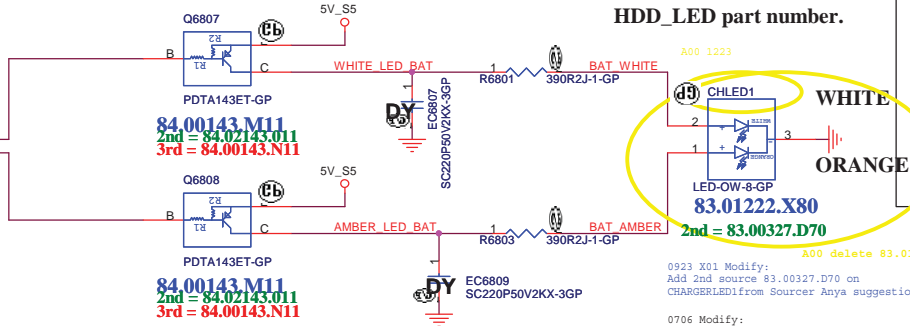
SATA HDD LED(White)

84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

Battery LED2 (WHITE_LED)

Need change to LOW acted from KBC GPIO

0702 Modify:
Rename CHARGE_LED# to CHG_AMBER_LED#.
Rename DC_BATFULL# to BATT_WHITE_LED#.

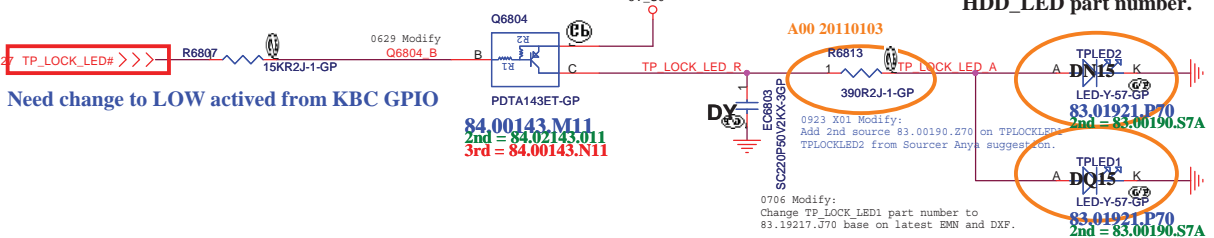


Battery LED1 (AMBER_LED)

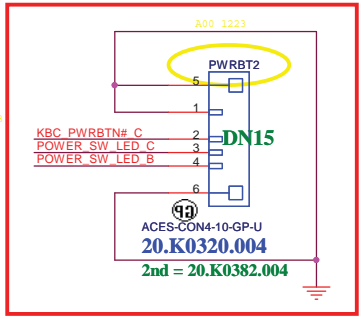
Need change to LOW acted from KBC GPIO

TPLOCK LED

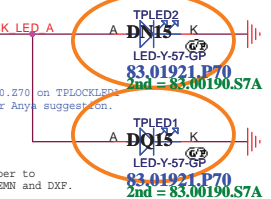
Need change to LOW acted from KBC GPIO



SKEW	ITEM1	ITEM2
DQ15	PWRBTN1	TP_LOCK_LED1
DN15	PWRBTN2	TP_LOCK_LED2



NEED confirm with ME actual
HDD_LED part number.



0715 Modify:
Removed PWR_BTN_LED# control circuit
base on Dell feedback.

<Core Design>

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Title: **LED Bard/Power Button**

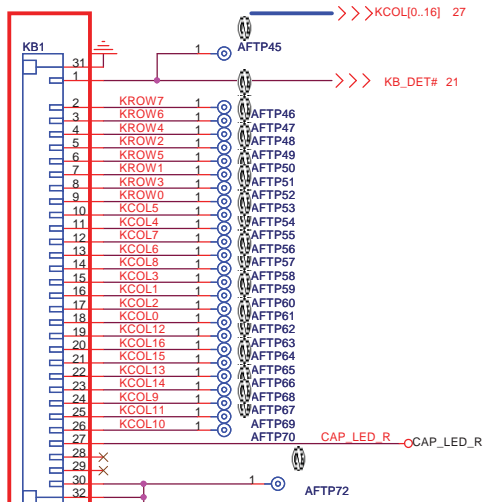
Size A3 Document Number: **QUEEN 15** Rev: **A00**

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SSID = KBC

Internal Keyboard Connector

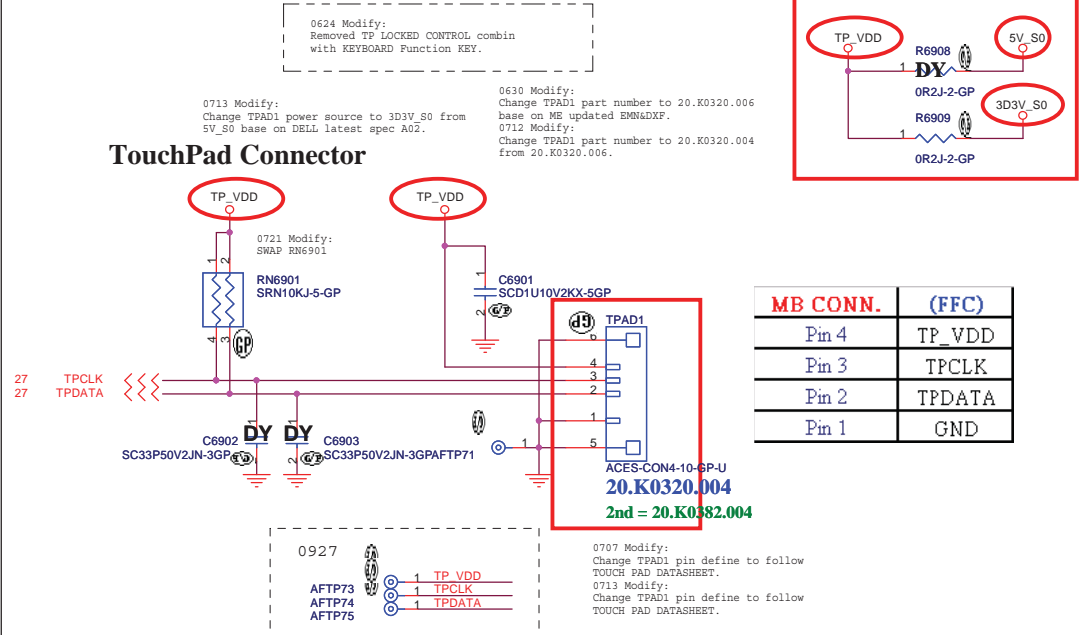
0630 Modify:
Change KB1 part number to 20.K0565.030
base on ME updated EMN and DXF.



MB Pin	Description
1	Diag_Loop3 = GPIO_1 (TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	NC (reserved for Caps LK LED)
28	NC (reserved for Num LK LED)
29	NC (reserved for Scroll LK LED)
30	GND

SSID = Touch.Pad

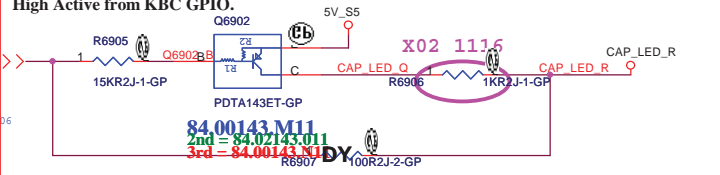
TouchPad Connector



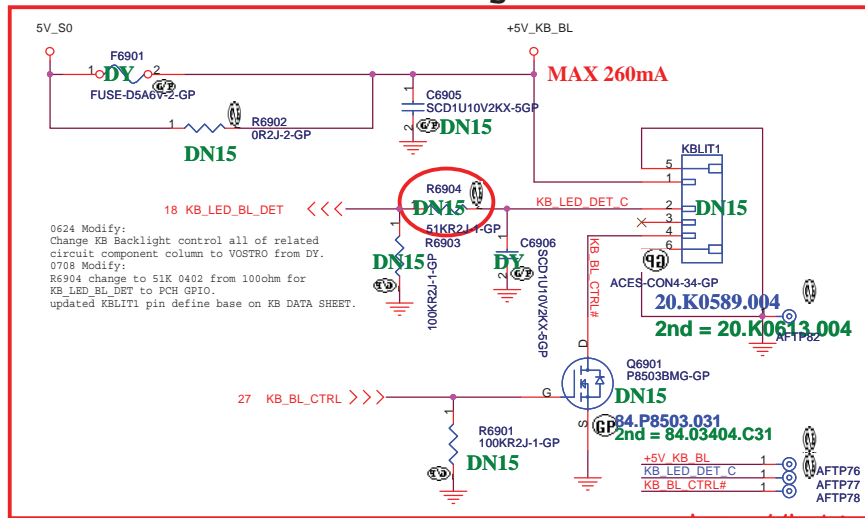
MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

SKEW	OPTION1	OPTION2	PIN	Feature	REMARK
DQ13	C12S		30		S is mean small
DN13	C12S	C12SB	30/25	Backlight	SB is mean small with backlight
DN15	C12S	C12SB	30/25	Backlight	
DQ15	C12SN		30	KB_DET#,CAP LED	SN is mean small with numpad

CAP LED CONTROL



KB Backlight Connector



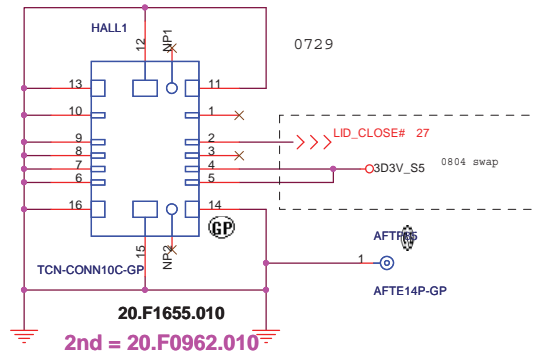
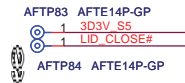
MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin 2	KB_LED_DET_C
Pin 3	NC
Pin 4	KB_BL_CTRL#

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File: **Key Board/Touch Pad**

Size: A3 Document Number: **QUEEN 15** Rev: **A00**

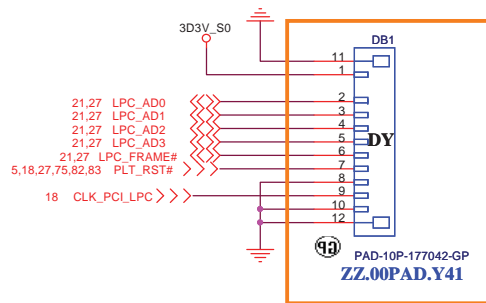
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1110 X02 Modify:
 Add 2nd 20.F0962.010 on HALL1 from
 ME updated connector list.

<Core Design>

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Title			
Hall Sensor			
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A00 1229 DB1 change to ZZ.00PAD.Y41(solder kmask type)
and keep un-stuffat X-Build stage

<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
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<Core Design>

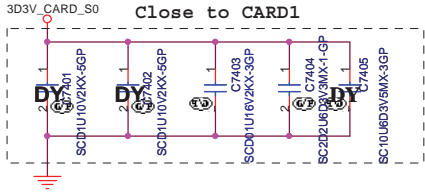
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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<Core Design>

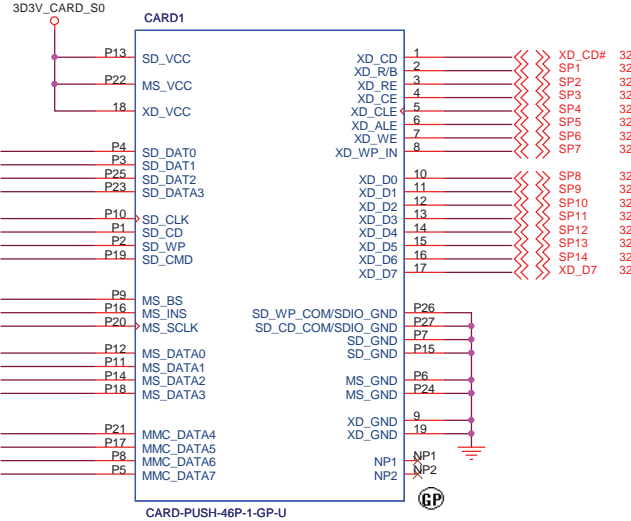
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Title			
Reserved			
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SSID = SDIO



SD/XD/MS/MMC+ Card Reader

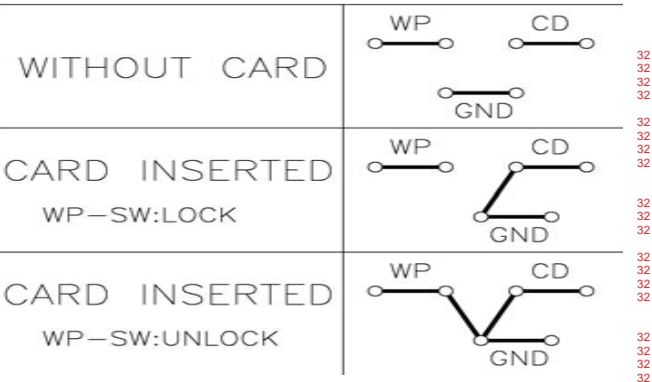
0906 X01 Modify:
Change CARD1 to 20.10129.001 from 62.10051.931
from MS double updated latest DXF&MN on X01.



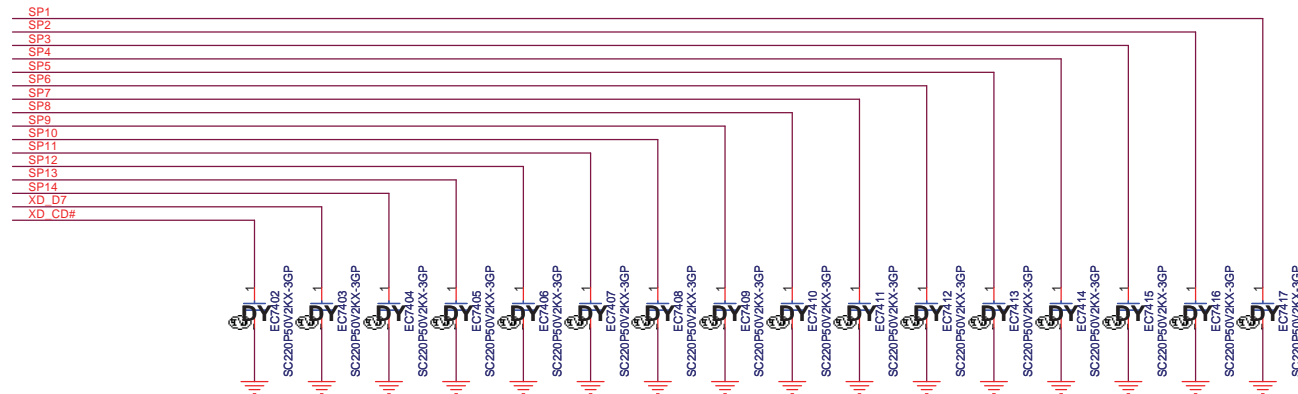
20.10129.001

2nd = 20.10135.001

1119 X02 Modify:
Add 2nd 20.10135.001 on HALL1 from
ME updated connector list.



For EMI Reserved



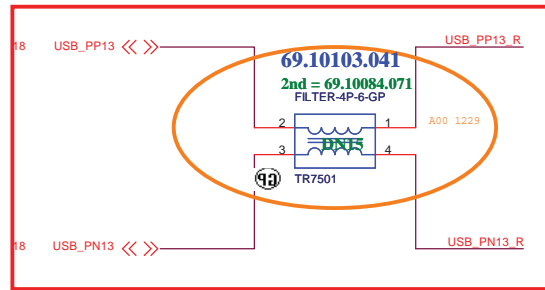
20.10129.001			
Pin	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

<Core Design>



Title		
SD/XD/MS/MMC Card CONN		
Size	Document Number	Rev
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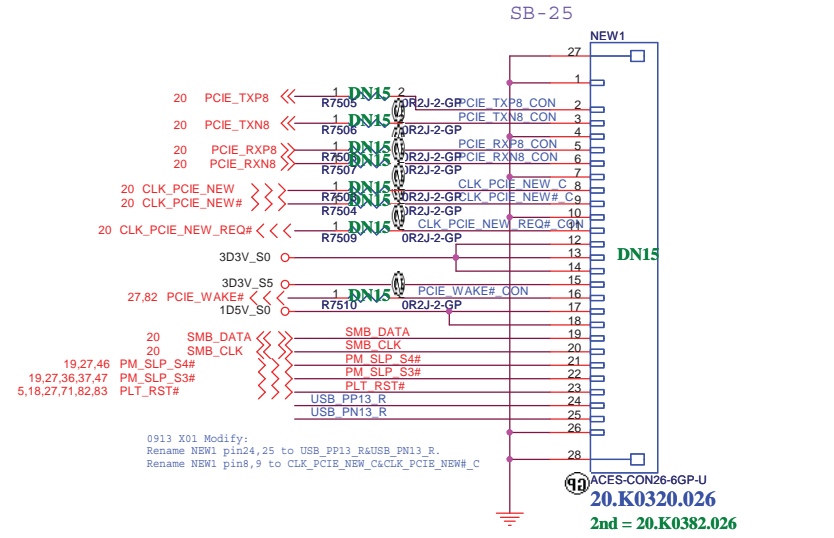
1122 X02 Modify:
 Change TR7501 CM choke to 69.10103.041
 and un-stuff R7501,R7502 from EMC Neo Suggestion.
 Change R7501,R7502 to 0603 from 0402.



A00	1	3D3V_S5
A00	1	3D3V_S0
A00	1	1D5V_S0
A00	1	USB_PN13_R
A00	1	USB_PP13_R
A00	1	CLK_PCIE_NEW_REQ#_CON
A00	1	SMB_CLK
A00	1	SMB_DATA
A00	1	PM_SLP_S3#
A00	1	PM_SLP_S4#
A00	1	PLT_RST#
A00	1	CLK_PCIE_NEW#_C
A00	1	CLK_PCIE_NEW_C
A00	1	PCIE_TXN8_CON
A00	1	PCIE_TXP8_CON
A00	1	PCIE_RXN8_CON
A00	1	PCIE_RXP8_CON
A00	1	PCIE_WAKE#_CON

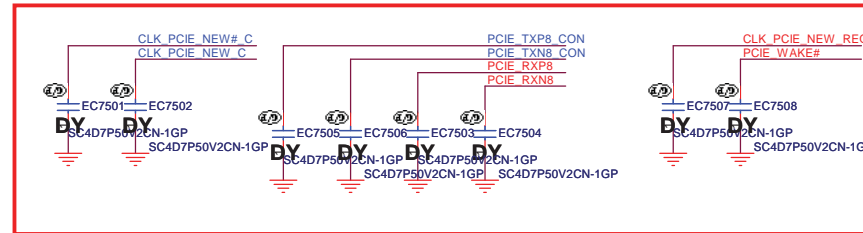
1D5V_S0_CARD Max. 650mA, Average 500mA.
 3D3V_S0_CARD Max. 1300mA, Average 1000mA
 3D3V_S5_CARDAUX Max. 275mA

0824 X01 Modify:
 Due to our NEW1 change to Express card to
 bottom side so re-assign NEW1 pin define same
 as DQ15-WY.
 0906 X01 Modify:
 Add 2nd source 20.K0382.026 on NEW1 base on
 updated connector list.



0913 X01 Modify:
 Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R.
 Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C

For EMI




0913 X01 Modify:
 Add R7503, R7504 and reserved EC7501, EC7502 on
 CLK_PCIE_NEW & CLK_PCIE_NEW# for EMC suggestion.
 0921 X01 Modify:
 Add R7505-R7508 0ohm and reserved EC7503-EC7506
 on PCIE_TXP8&RX8 signal base on EMC Lance suggestion.
 Add R7509, R7510 0ohm and reserved EC7507, EC7508
 on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base
 on EMC Lance suggestion.

<Core Design>

DELL		Wistron Corporation	
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Title: Express Card			
Size: A3	Document Number: QUEEN 15	Rev: A00	
Date: Tuesday, January 04, 2011	Sheet: 75	of:	108


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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	QUEEN 15	A00
Date:	Tuesday, January 04, 2011	Sheet 76 of 108


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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet	77 of 108

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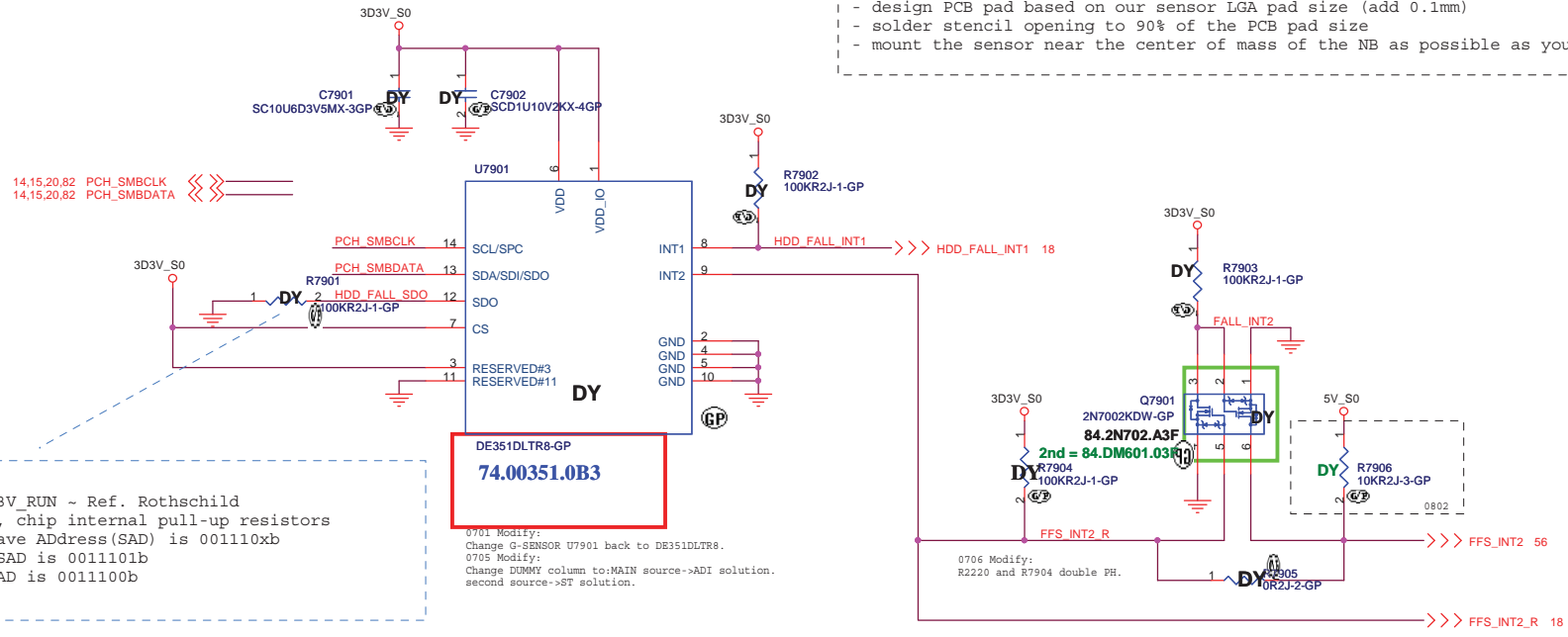
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
 (#1) Just pull +3.3V_RUN ~ Ref. Rothschild
 (#2) FAE/ DY is ok, chip internal pull-up resistors
 (#3) From spec, Slave Address(SAD) is 001110xb
 Pull HIGH SAD is 0011101b
 Pull GND SAD is 0011100b

0701 Modify:
 Change G-SENSOR U7901 back to DE351DLTR8.
 0705 Modify:
 Change DUMMY column to:MAIN source->ADI solution.
 second source->ST solution.

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>


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Title: **Free Fall Sensor**

Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet: 79	of 108


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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet	80 of 108

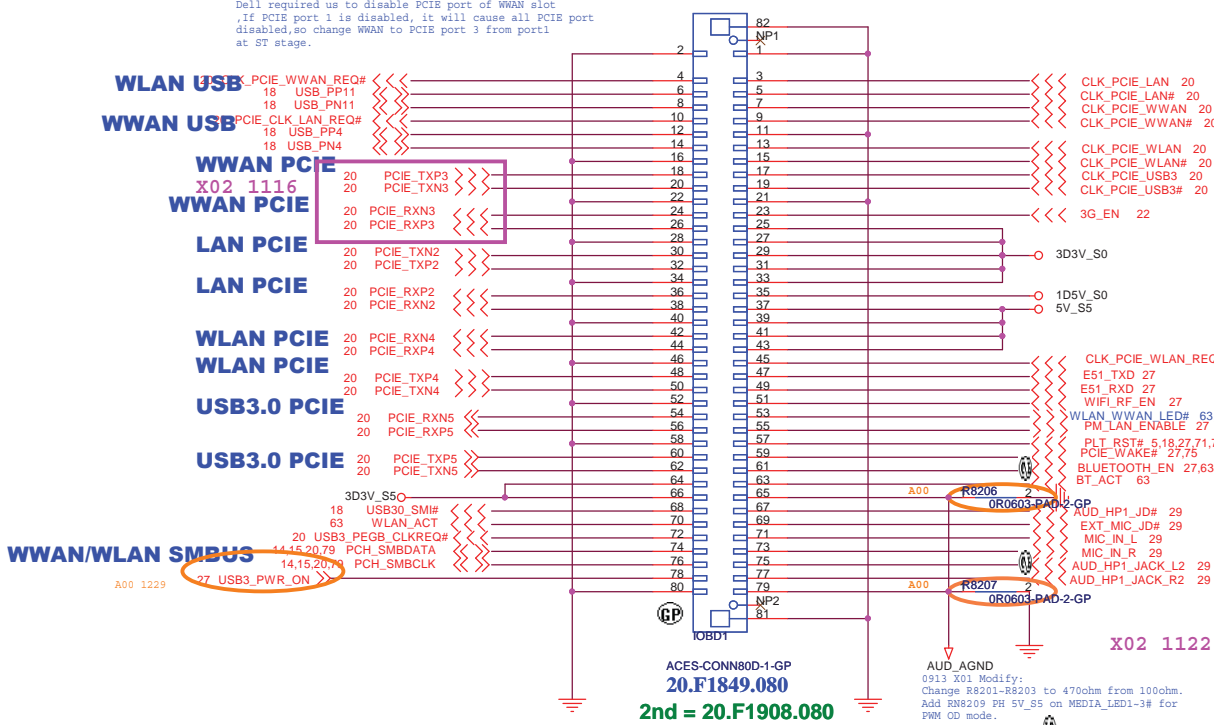
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<Core Design>

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Title			
Reserved			
Size	Document Number	Rev	
A3	QUEEN 15	A00	
Date:	Tuesday, January 04, 2011	Sheet 81	of 108

IO Board CONN 80 pin

1112 X01 Modify:
Dell required us to disable PCIE port of WWAN slot
, If PCIE port 1 is disabled, it will cause all PCIE port
disabled, so change WWAN to PCIE port 3 from port1
at ST stage.



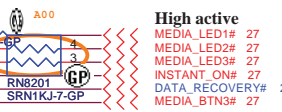
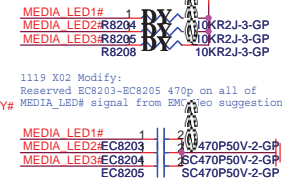
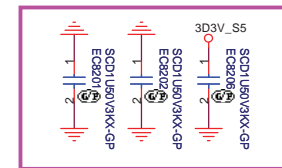
LAN CLK
CLK_PCIE_LAN# 20
CLK_PCIE_LAN# 20
CLK_PCIE_WWAN# 20
CLK_PCIE_WWAN# 20

WWAN CLK
CLK_PCIE_WLAN 20
CLK_PCIE_WLAN# 20
CLK_PCIE_USB3 20
CLK_PCIE_USB3# 20

WLAN CLK
CLK_PCIE_WLAN 20
CLK_PCIE_WLAN# 20
CLK_PCIE_USB3 20
CLK_PCIE_USB3# 20

0916 X01 Modify:
Keep original X00 IOBD1 pin define.
0917 X01 Modify:
Change IOBD1 part number to 20.F1849.080
base on Double updated latest DAF&ENM.
0920 X01 Modify:
Re-assign IOBD1 pin define due to updated
connector pin define is different as before.
Add R8206, R8207 to isolated AGND and DGND.

1122 X02 Modify:
stuff EC8201, EC8202 0.1u(closed H3)
between GND and GND from EMC Neo suggestion.
stuff EC8206 between 3D3V_S5 and GND from
EMC Neo suggestion.

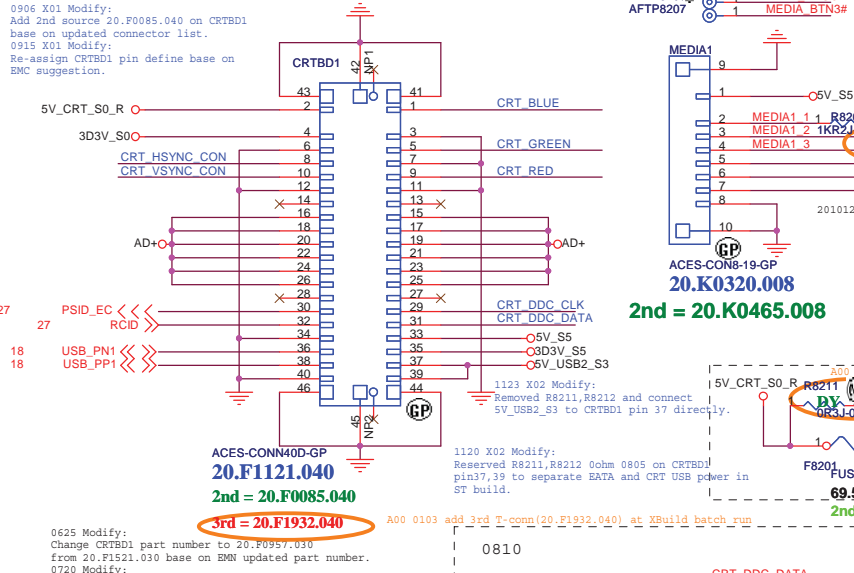


1110 X02 Modify:
Add 2nd 20.R0465.008 on MEDIA1 from
ME updated connector list.
1112 X02 Modify:
change Media resistor from 430 ohm to 1K on
both DQ/DN15 (R8201, R8202, R8203)
for Media button LED light spot issue

USB3.0 PCIE USB3.0 PCIE

SIGNAL	PIN	PIN	SIGNAL
5V_CRT_S0_R	2	1	CRT_BLUE_R
3D3V_S0	4	3	GND
GND	6	5	CRT_GREEN_R
CRT_HSYNC_CON	8	7	GND
CRT_VSYNC_CON	10	9	CRT_RED_R
GND	12	11	GND
NC	14	13	NC
AD+	16	15	AD+
AD+	18	17	AD+
AD+	20	19	AD+
AD+	22	21	AD+
AD+	24	23	AD+
AD+	26	25	AD+
NC	28	27	NC
PSID_EC	30	29	DDCCLK
RCID	32	31	DDCDATA
GND	34	33	5V_S5
USB_PN1	36	35	3D3V_S5
USB_PP1	38	37	5V_USB1_S3
GND	40	39	5V_USB1_S3

CRT Board Connector



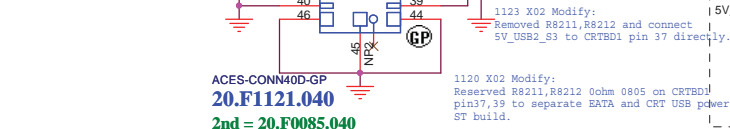
0906 X01 Modify:
Add 2nd source 20.F0085.040 on CRTBD1
base on updated connector list.
0915 X01 Modify:
Re-assign CRTBD1 pin define base on
EMC suggestion.

AFTP8201 1 MEDIA1_1
AFTP8202 1 MEDIA1_2
AFTP8203 1 MEDIA1_3
AFTP8204 1 5V_S5
AFTP8205 1 INSTANT_ON#
AFTP8206 1 DATA_RECOVERY#
AFTP8207 1 MEDIA_BTN3#

1119 X02 Modify:
Reserved EC8203-EC8205 470p on all of
MEDIA_LED# signal from EMC Neo suggestion.

High active
MEDIA_LED1# 27
MEDIA_LED2# 27
MEDIA_LED3# 27
INSTANT_ON# 27
DATA_RECOVERY# 27
MEDIA_BTN3# 27

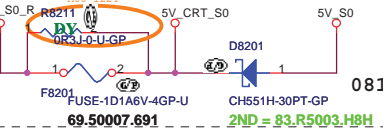
1110 X02 Modify:
Add 2nd 20.R0465.008 on MEDIA1 from
ME updated connector list.
1112 X02 Modify:
change Media resistor from 430 ohm to 1K on
both DQ/DN15 (R8201, R8202, R8203)
for Media button LED light spot issue



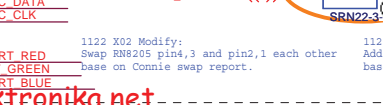
1123 X02 Modify:
Removed R8211, R8212 and connect
5V_USB2_S3 to CRTBD1 pin 37 directly.

1120 X02 Modify:
Reserved R8211, R8212 500m 0805 on CRTBD1
pin37, 39 to separate EAPR and CRT USB power in
ST build.

1120 X02 Modify:
Swap R8205 pin4, 3 and pin2, 1 each other
base on Connie swap report.



1120 X02 Modify:
Add R8205
base on HSYNC&VSYNC report.



SIGNAL	PIN	PIN	SIGNAL
GND	80	79	GND
CLK_PCIE_WWAN_REQ#	78	77	CLK_PCIE_LAN
USB_PP11	76	75	CLK_PCIE_LAN#
USB_PN11	74	73	CLK_PCIE_WWAN
PCIE_CLK_LAN_REQ#	72	71	CLK_PCIE_WWAN#
USB_PP4	70	69	GND
USB_PN4	68	67	CLK_PCIE_WLAN
GND	66	65	CLK_PCIE_WLAN#
PCIE_TXP1	64	63	CLK_PCIE_USB3
PCIE_TXN1	62	61	CLK_PCIE_USB3#
GND	60	59	GND
PCIE_RXN1	58	57	3G_EN
PCIE_RXP1	56	55	3D3V_S0
GND	54	53	3D3V_S0
PCIE_TXN2	52	51	3D3V_S0
PCIE_TXP2	50	49	3D3V_S0
GND	48	47	3D3V_S0
PCIE_RXN2	46	45	1D5V_S5
GND	42	41	5V_S5
PCIE_RXN4	40	39	5V_S5
PCIE_RXP4	38	37	5V_S5
GND	36	35	CLK_PCIE_WLAN_REQ#
PCIE_TXP4	34	33	E51_TXD
PCIE_TXN4	32	31	E51_RXD
GND	30	29	WIFI_RF_EN
IOBD1_28	28	27	WLAN_WWAN_LED#
IOBD1_26	26	25	PM_LAN_ENABLE
GND	24	23	PLT_RST#
IOBD1_22	22	21	PCIE_WAKE#
IOBD1_20	20	19	BLUETOOTH_EN
3D3V_S5	18	17	BT_ACT
3D3V_S5	16	15	GND
IOBD1_14	14	13	AUD_HP1_JD#
WLAN_ACT	12	11	EXT_MIC_JD#
USB3_PEGB_CLKREQ#	10	9	MIC_IN_L
PCH_SMBDATA	8	7	MIC_IN_R
PCH_SMBCLK	6	5	AUD_HP1_JACK_L2
USB3_PWR_ON	4	3	AUD_HP1_JACK_R2
GND	2	1	GND

<Core Design>

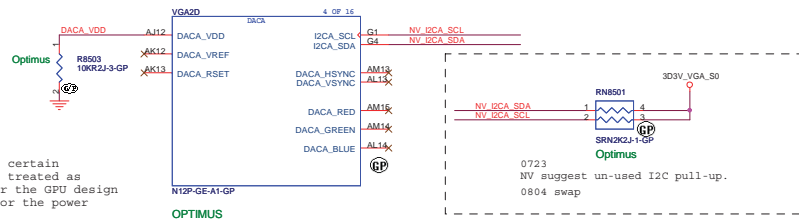
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File
IO Board Connector

Size A3 Document Number **QUEEN 15** Rev **A00**

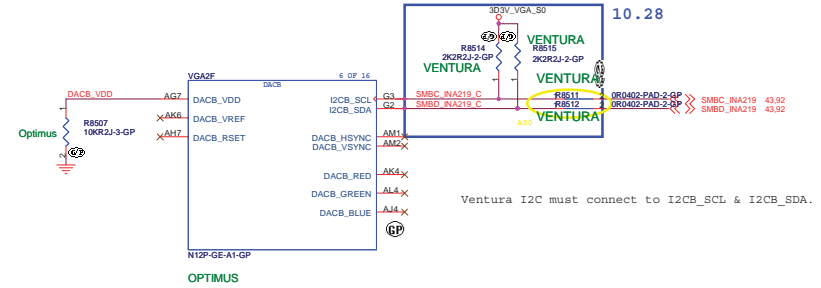
Date: Tuesday, January 04, 2011 Sheet 82 of 108

If a DAC interface is not required, it should be disabled by:
 1. Adding a pull-down to the DACx_VDD with a 10 kilohm resistor to GND.
 2. All other DAC I/O pins can be left floating.

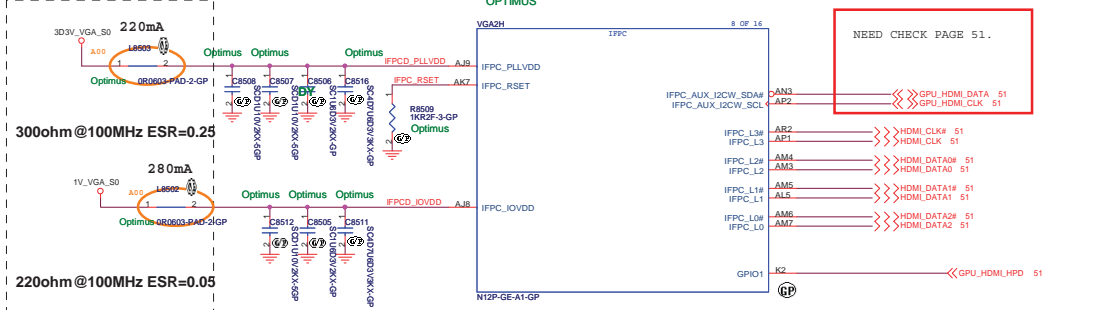
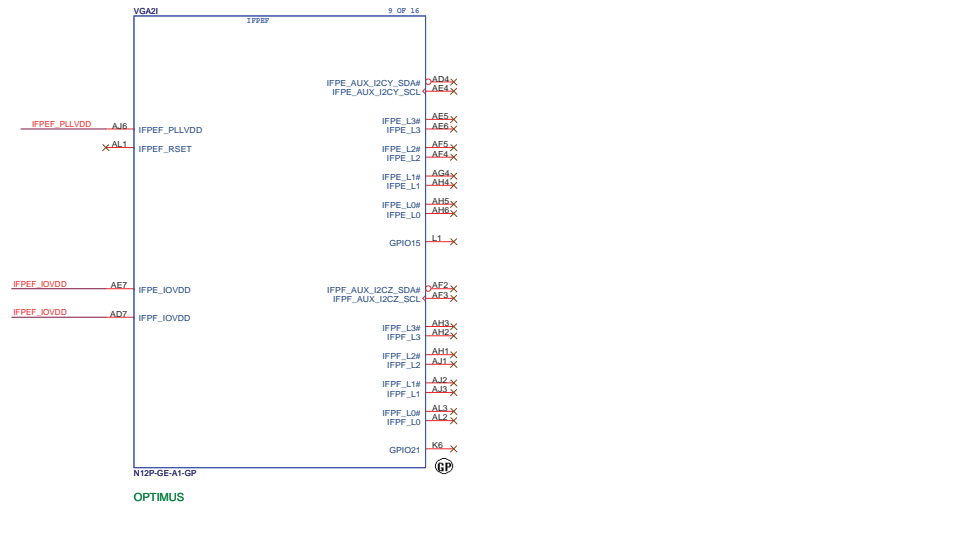
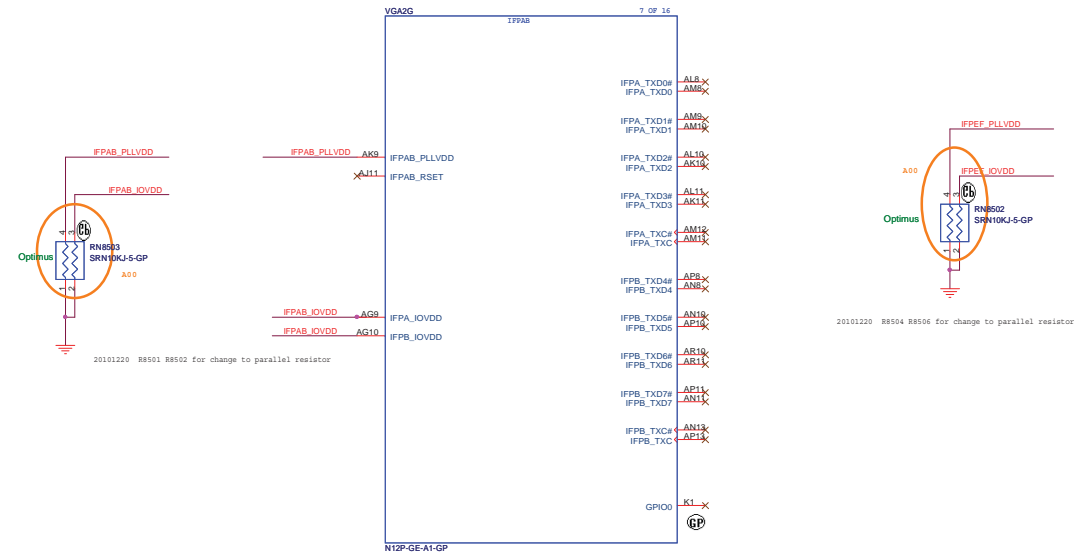


In Optimus mode the GPU does not drive certain interfaces. These interfaces should be treated as unused and appropriate terminations per the GPU design guide should be applied to the signal or the power supply block.

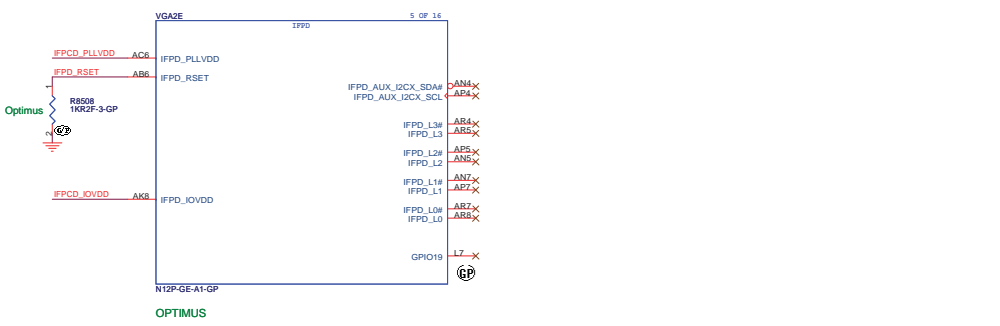
The following guidelines only apply to a fully unused IFP macro:
 1. Pull down IFPxy_IOVDD with 10 kilohm resistor.
 2. Pull down IFPxy_PLLVDD with 10 kilohm resistor.
 3. The other IO pins can be NC; this includes unused data lines.



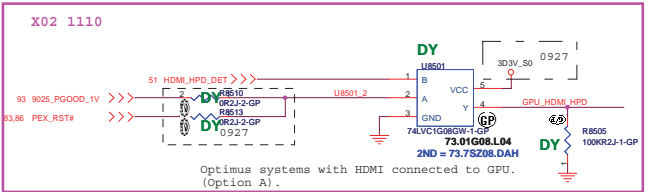
Ventura I2C must connect to I2CB_SCL & I2CB_SDA.



NEED CHECK PAGE 51.

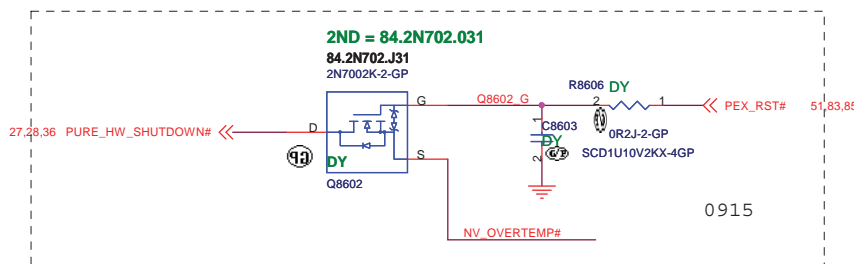
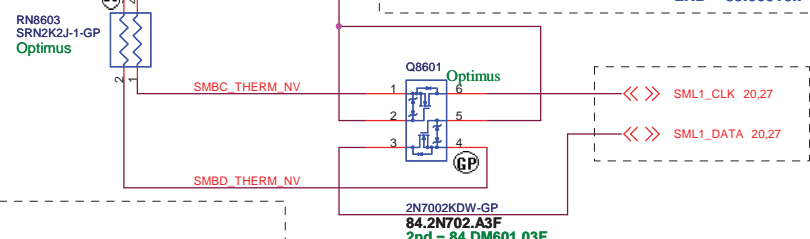
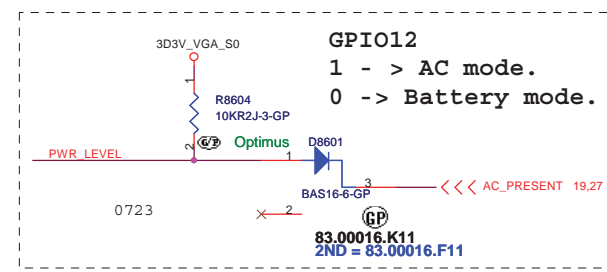
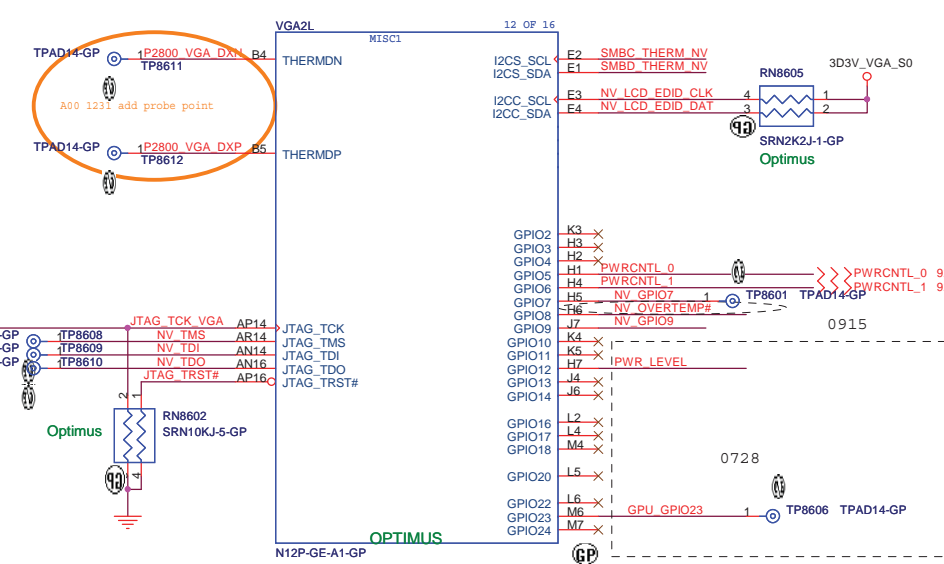
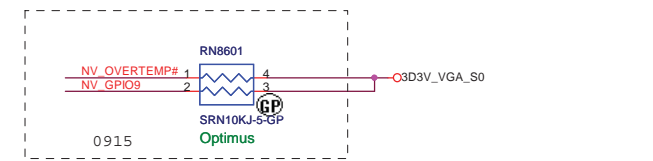
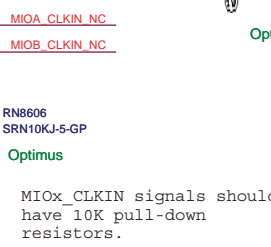
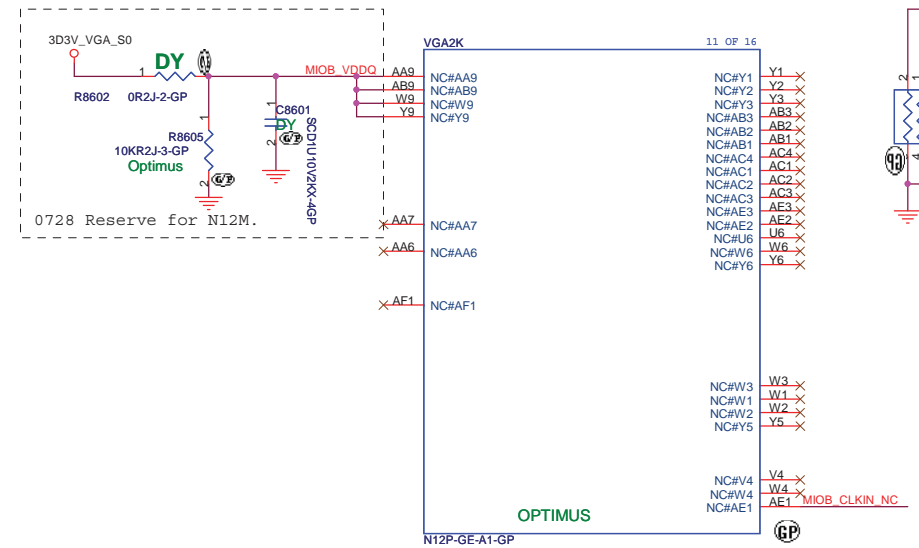
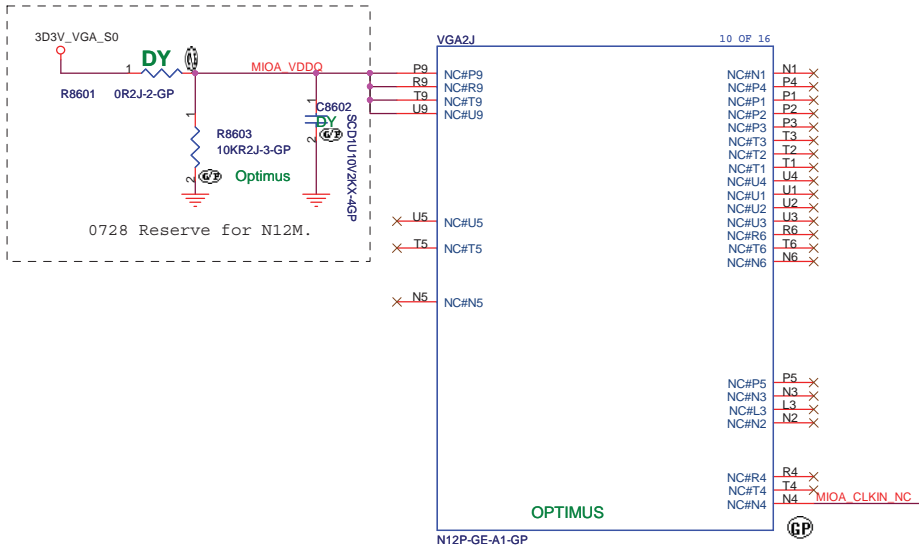


Optimus: If IFPC or IFPD is used, then the whole IFPCD interface is considered as being used. This is because IFPC and IFPD share one macro design so one IO interface cannot be independently disabled.



Optimus systems with HDMI connected to GPU. (Option A).

<http://hobi-elektronika.net>



MIOA/B Support

Package	MIOA	MIOB
GB1-192	15-bit, available	TBD
GB2-128	Not available	Not available

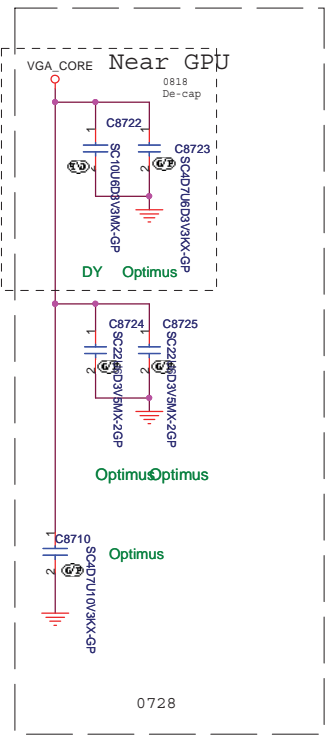
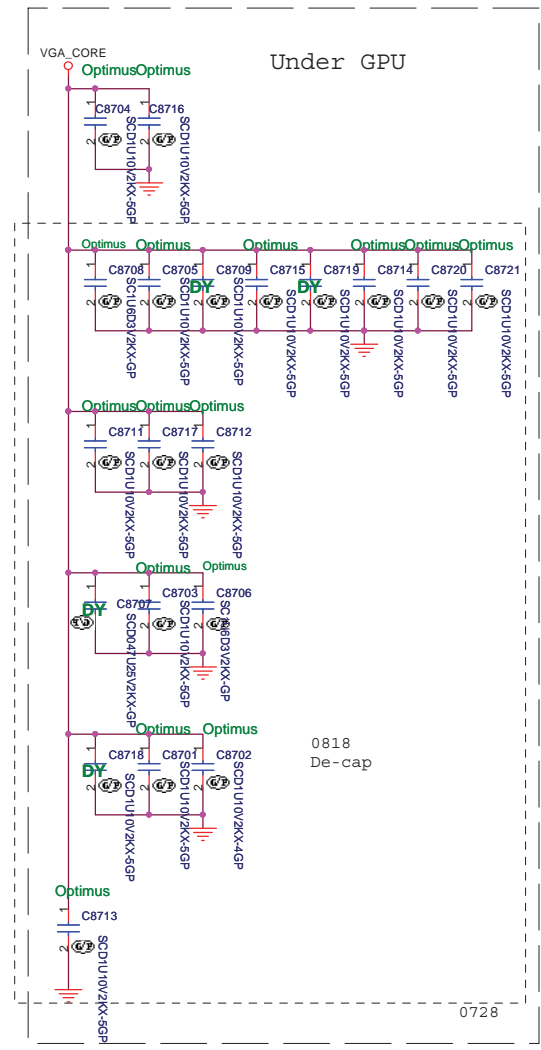
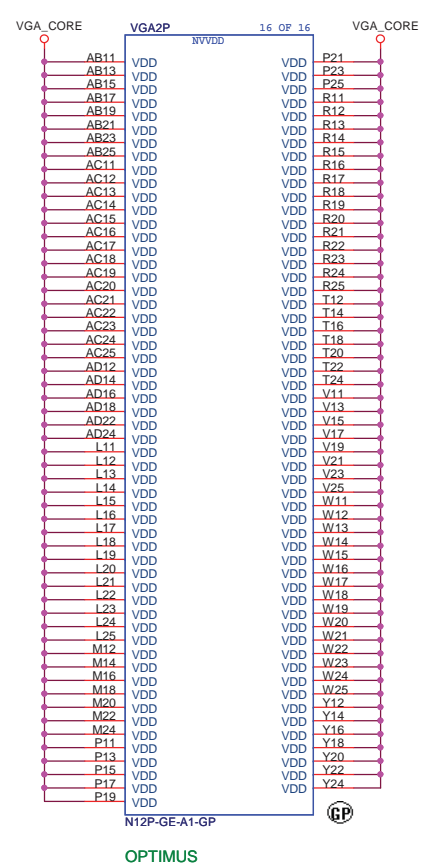
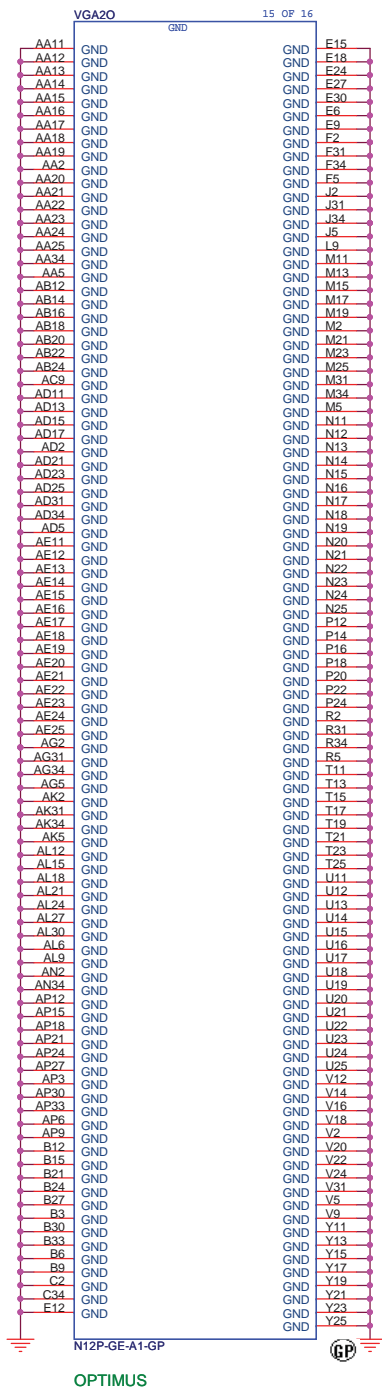
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Title: **N12P(5/6) MIO/ GPIO**

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<Variant Name>

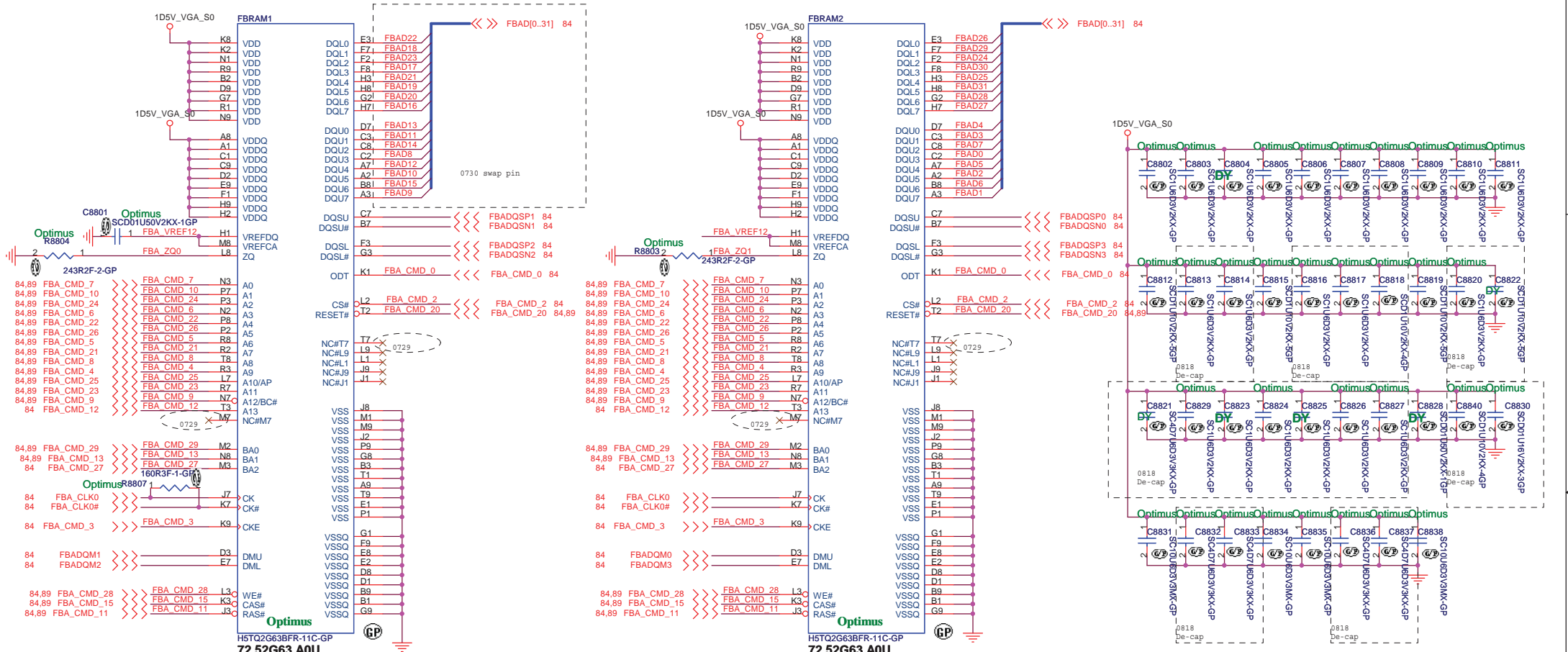


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Title: **N12P(6/6) POWER**

Size A3	Document Number	Rev
	QUEEN 15	A00
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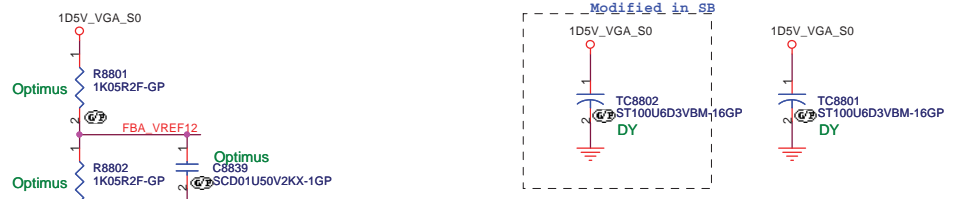
Frame Buffer Partition A Lower 32 bits.



2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133H48) from BGA96D0913H48

GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function	32..63
CMD25	CMD0	ODT	
CMD23	CMD1	CS1*	
CMD2	CMD2	CS2*	
CMD0	CMD3	CKE	
CMD10	CMD4	A8	A11
CMD6	CMD5	A6	A7
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	RA0*	BA2*
CMD18	CMD12	A13	A14
CMD9	CMD13	BA1	A3
CMD26	CMD14	A14	A13
CMD8	CMD15	CAS*	CAS*
CMD27	CMD16	CKE	
CMD5	CMD17	CS1*	
CMD11	CMD18	CS2*	
CMD16	CMD19	ODT	
CMD28	CMD20	RST	RST
CMD3	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A15
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD20	CMD30	A15	BA2



<Variant Name>

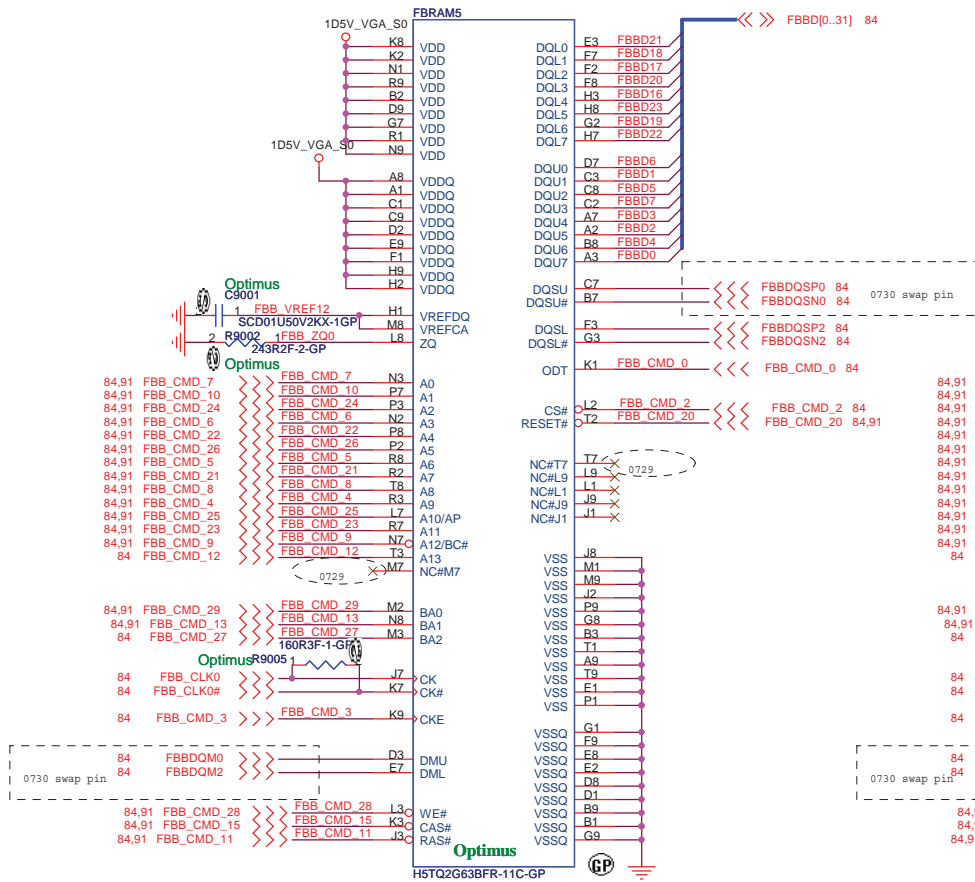
Wistron Corporation
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Title: **VRAM(1/4)**

Size: A3
Document Number: **QUEEN 15**
Date: Tuesday, January 04, 2011
Sheet: 88 of 108

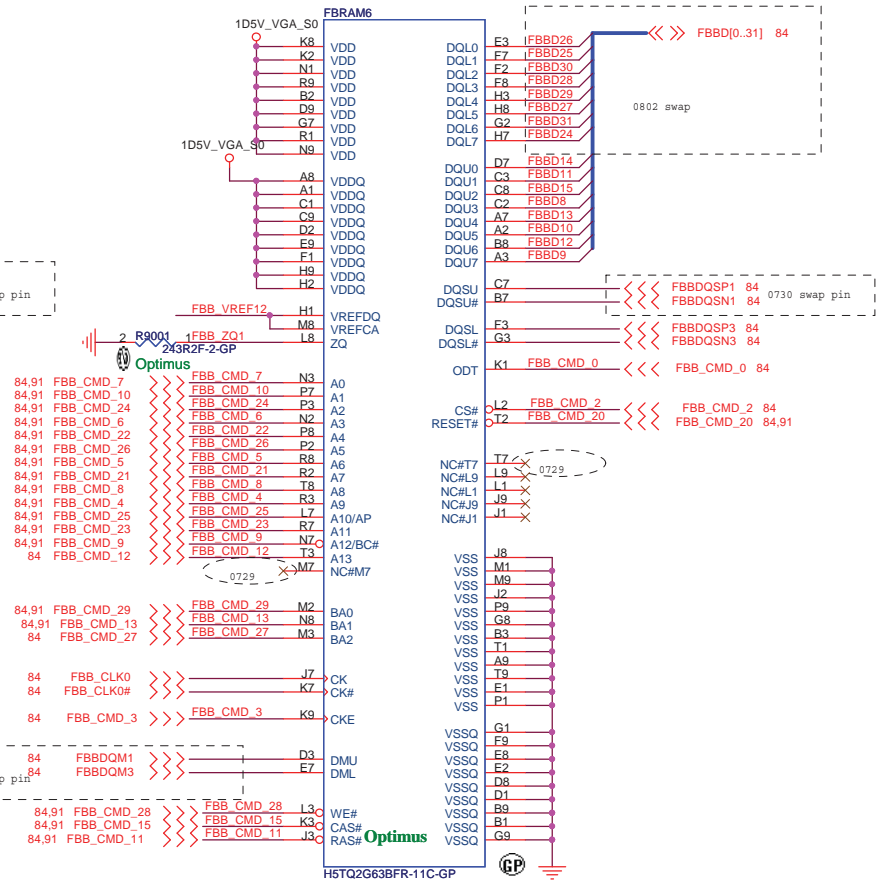
Rev: **A00**

Frame Buffer Partition B Lower 32 bits.



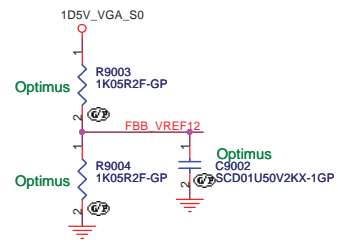
72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
 All of VRAM PCB footprint change to CO-LAY type
 (DUMMY-BGA96D075133H48) from BGA96D0913H48



72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
 All of VRAM PCB footprint change to CO-LAY type
 (DUMMY-BGA96D075133H48) from BGA96D0913H48



<Variant Name>

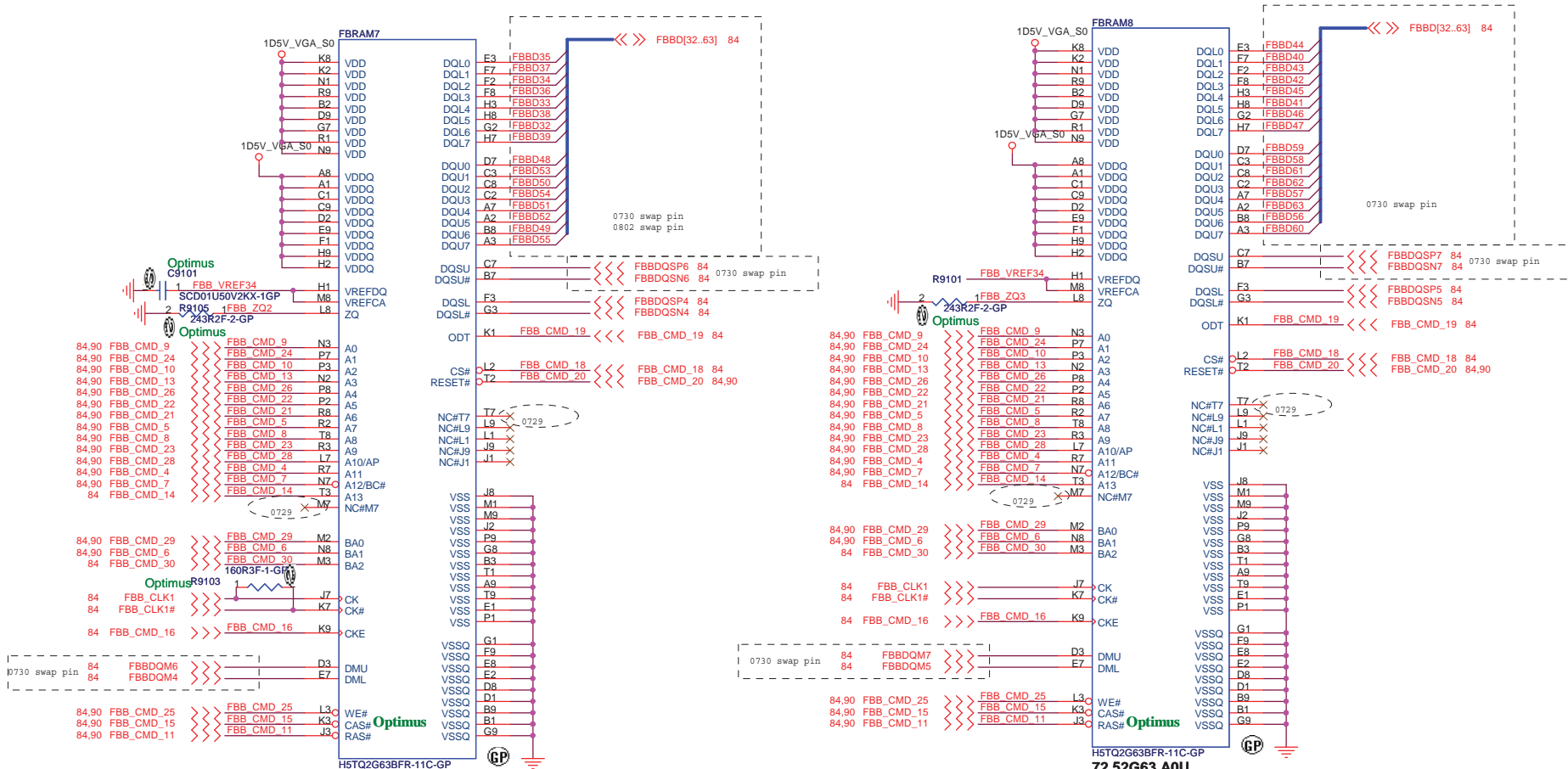
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 Taipei Hsein 221, Taiwan, R.O.C.

Title: **VRAM(3/4)**

Size A3 Document Number **QUEEN 15** Rev **A00**

Date: Tuesday, January 04, 2011 Sheet 90 of 108

Frame Buffer Partition B Upper 32 bits.

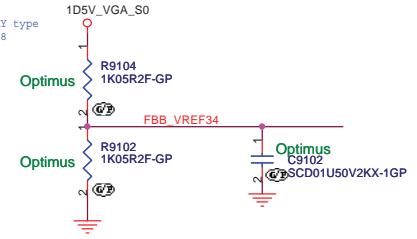


72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
 All of VRAM PCB footprint change to CO-LAY type
 (DUMMY-BGA96D075133H48) from BGA96D0913H48

1112 X02 Modify:
 All of VRAM PCB footprint change to CO-LAY type
 (DUMMY-BGA96D075133H48) from BGA96D0913H48



<Variant Name>

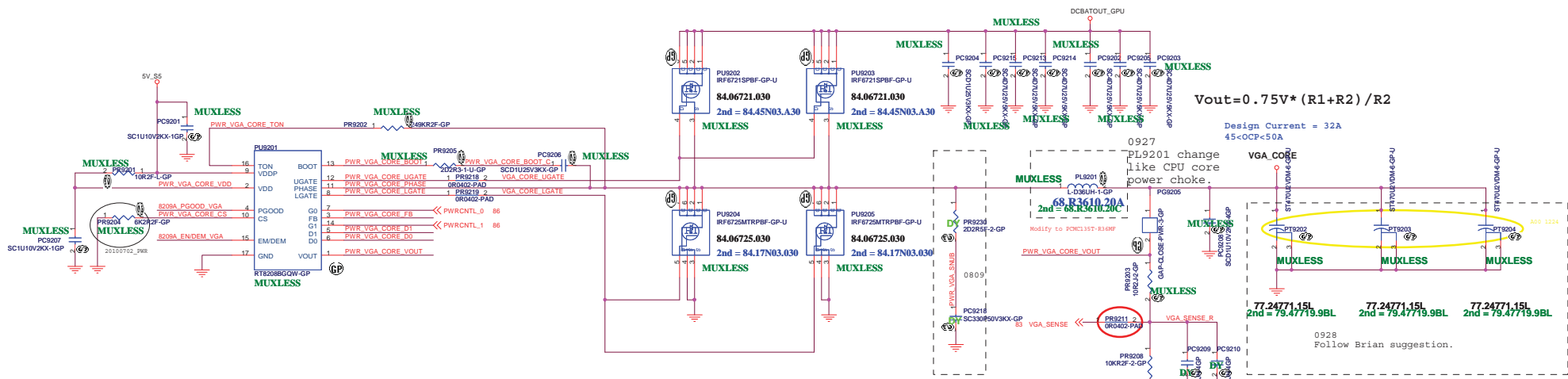
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(4/4)**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

Date: Tuesday, January 04, 2011 Sheet 91 of 108

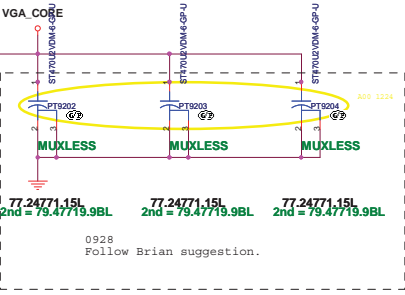
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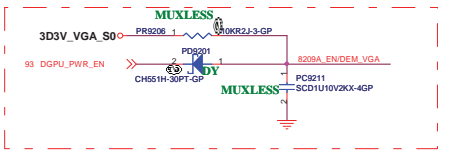
$V_{out} = 0.75V * (R1+R2) / R2$

Design Current = 32A
45<OCP<50A

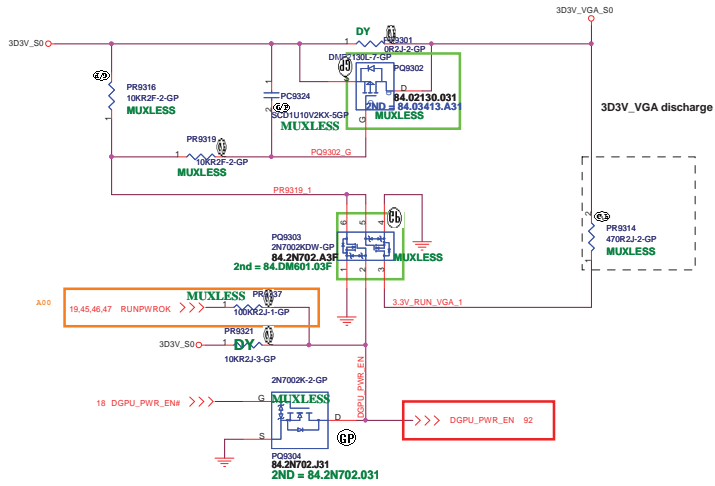
PL9201 change like CPU core power choke.



0928 Follow Brian suggestion.



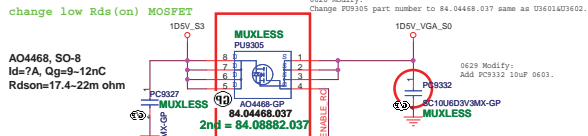
3D3V_S0 to 3D3V_VGA_S0 Transfer



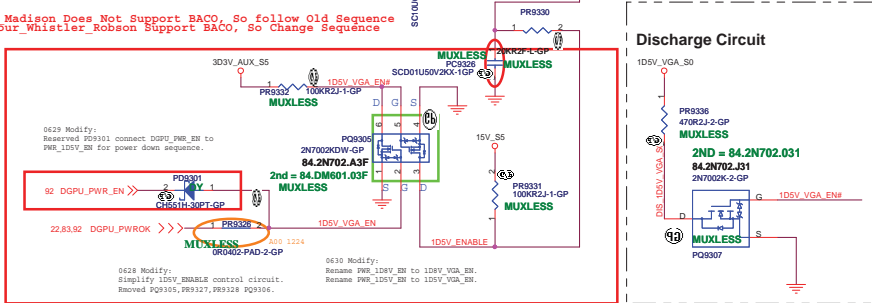
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

NV do not need 1.8V

1D5V_VGA_S0



Park Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

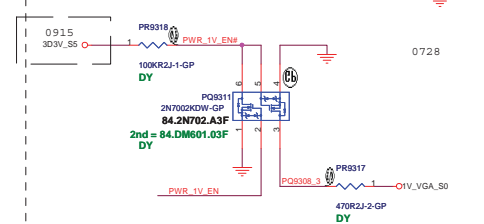
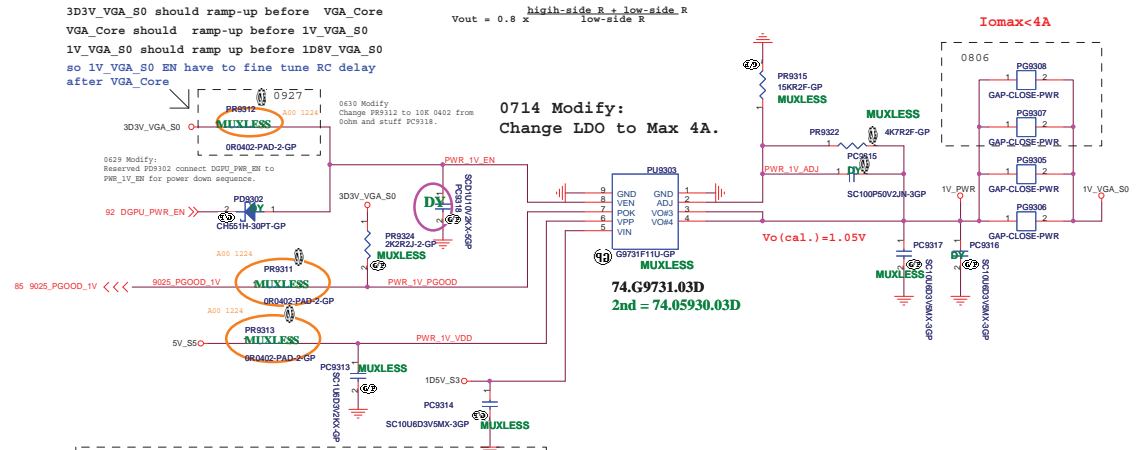


G9731F11U-GP for 1V_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core


$$V_{out} = 0.8 \times \frac{\text{high-side } R + \text{low-side } R}{\text{low-side } R}$$

0714 Modify:
Change LDO to Max 4A.




(Blanking)

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
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(Blanking)


<Variant Name>

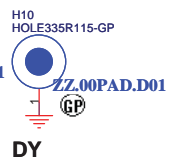
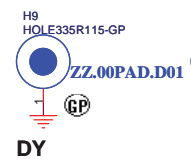
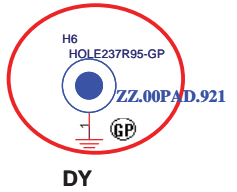
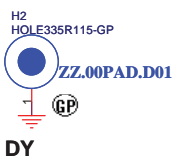
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
CRT Switch					
Size	Document Number				Rev
A3	QUEEN 15				A00
Date:	Tuesday, January 04, 2011			Sheet	95 of 108

SSID = SDIO

(Blanking)

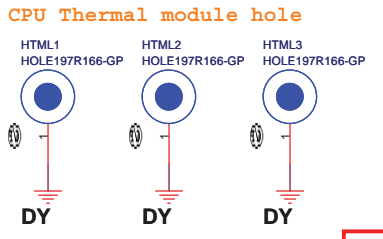
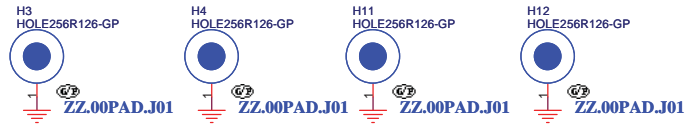
<Variant Name>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
TOUCH PANEL		
Size A3	Document Number QUEEN 15	Rev A00
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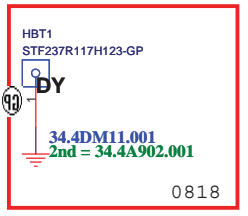
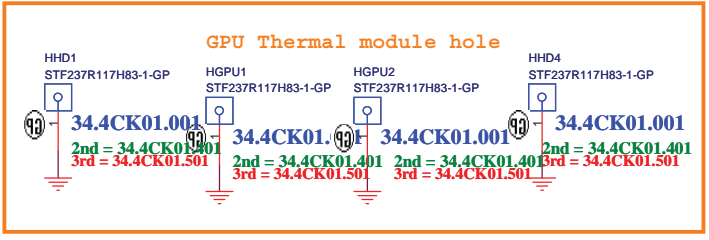
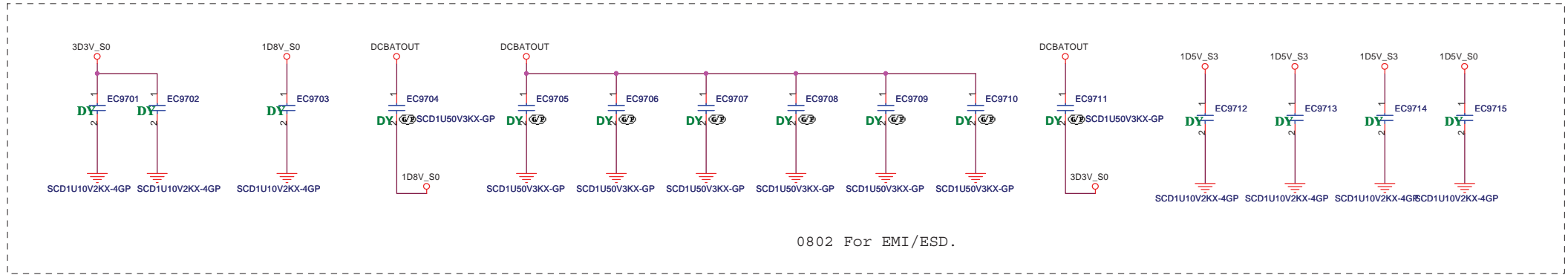
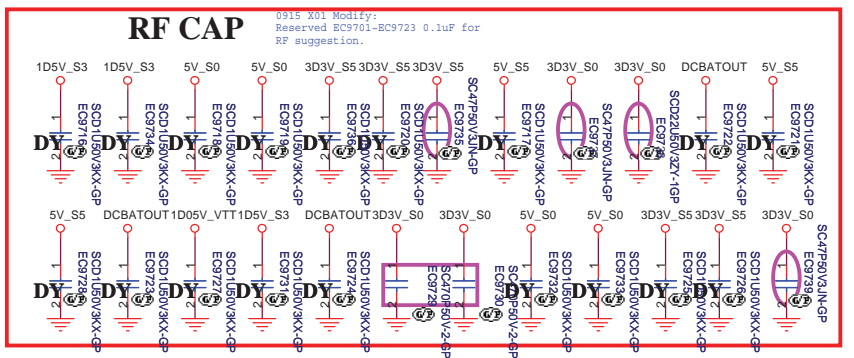
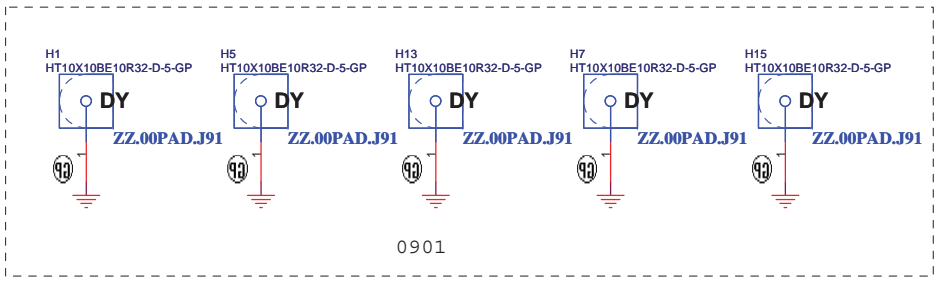
Check test point

0624 Modify:
Removed AFTP1,AFTP7-AFTP13.



stand off

0721 Modify:
Removed SPR1



A00 0103 add 3rd LIDON(34.4CK01.501) on HDD1,HDD4,HGPU1,HGPU2 at XBuild batch run

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<Variant Name>

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Title
UNUSED PARTS/EMI Capacitors

Size A3 Document Number
QUEEN 15

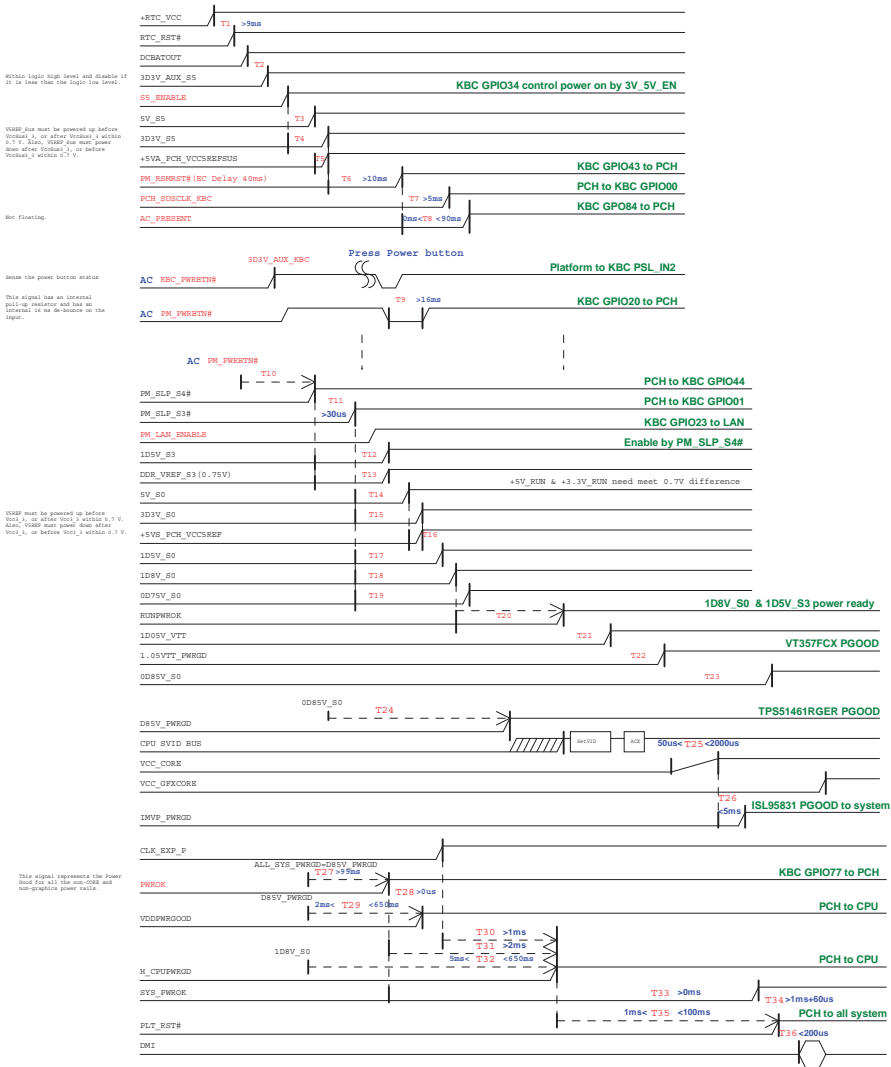
Date: Tuesday, January 04, 2011 Sheet 97 of 108

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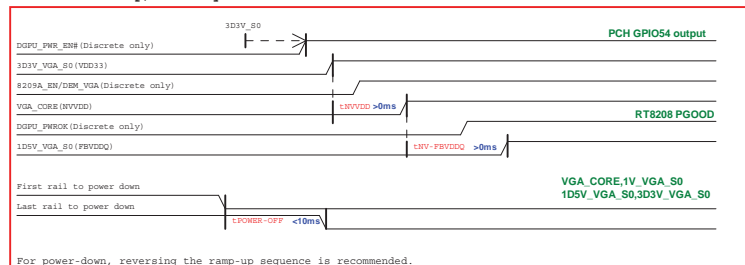
Huron River Platform Power Sequence

(AC mode)

red word: KBC GPIO

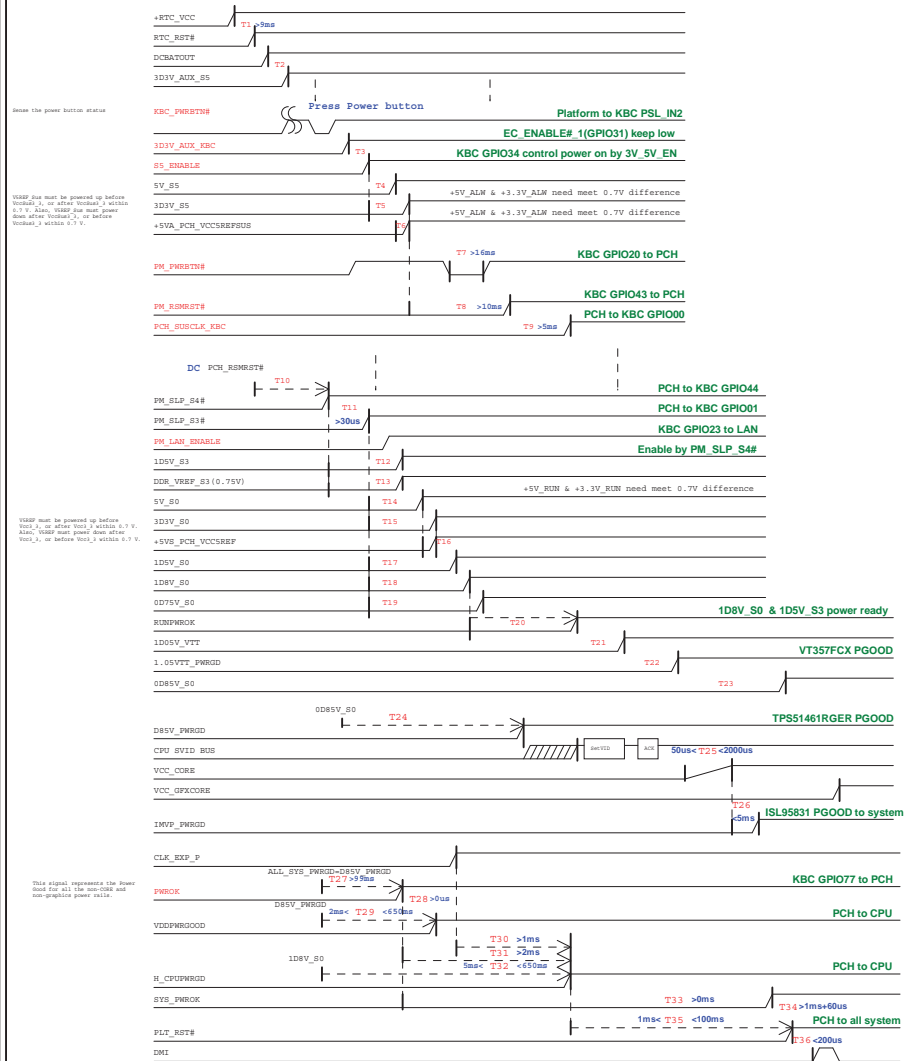


N12P-GE Power-Up/Down Sequence



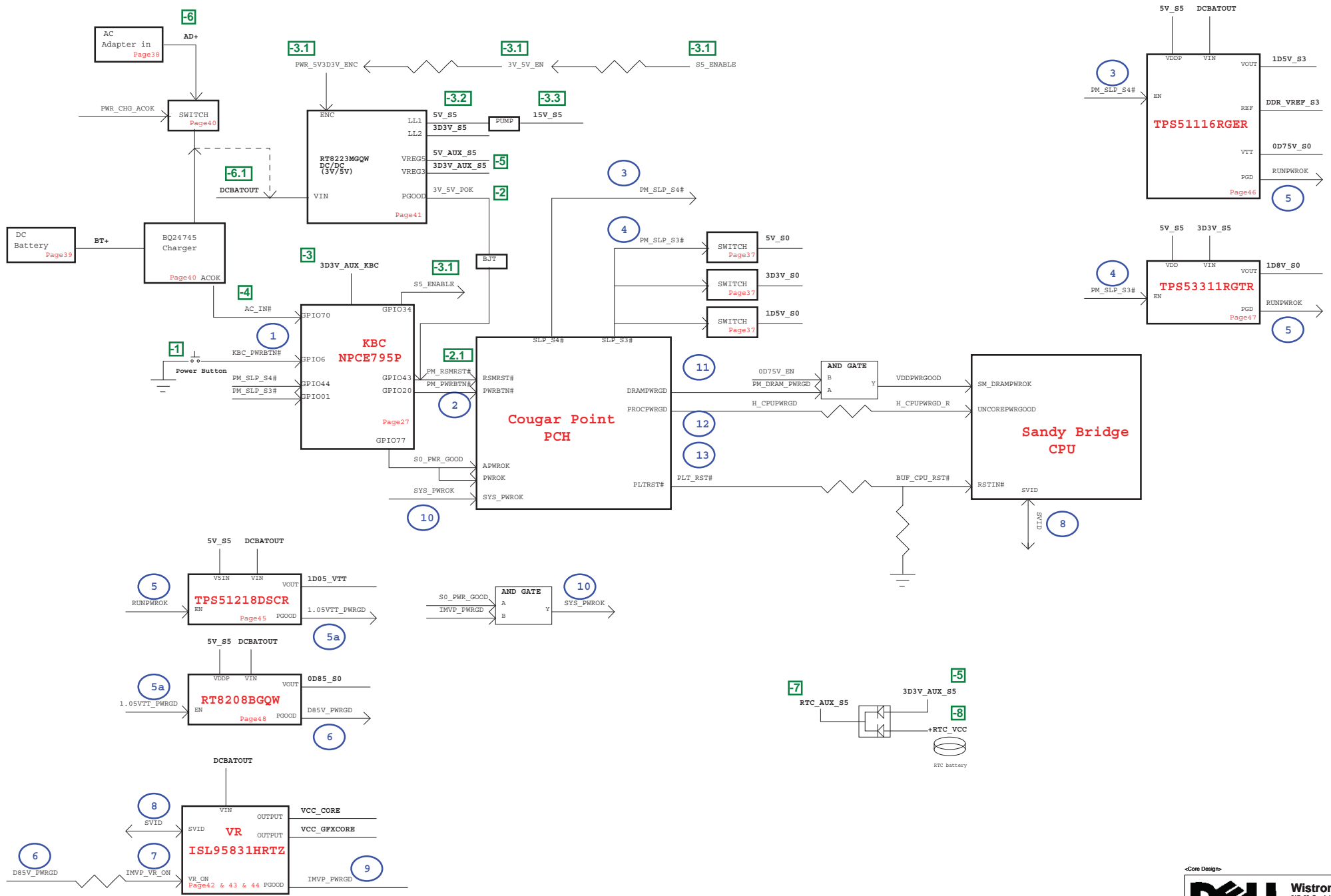
(DC mode)

red word: KBC GPIO



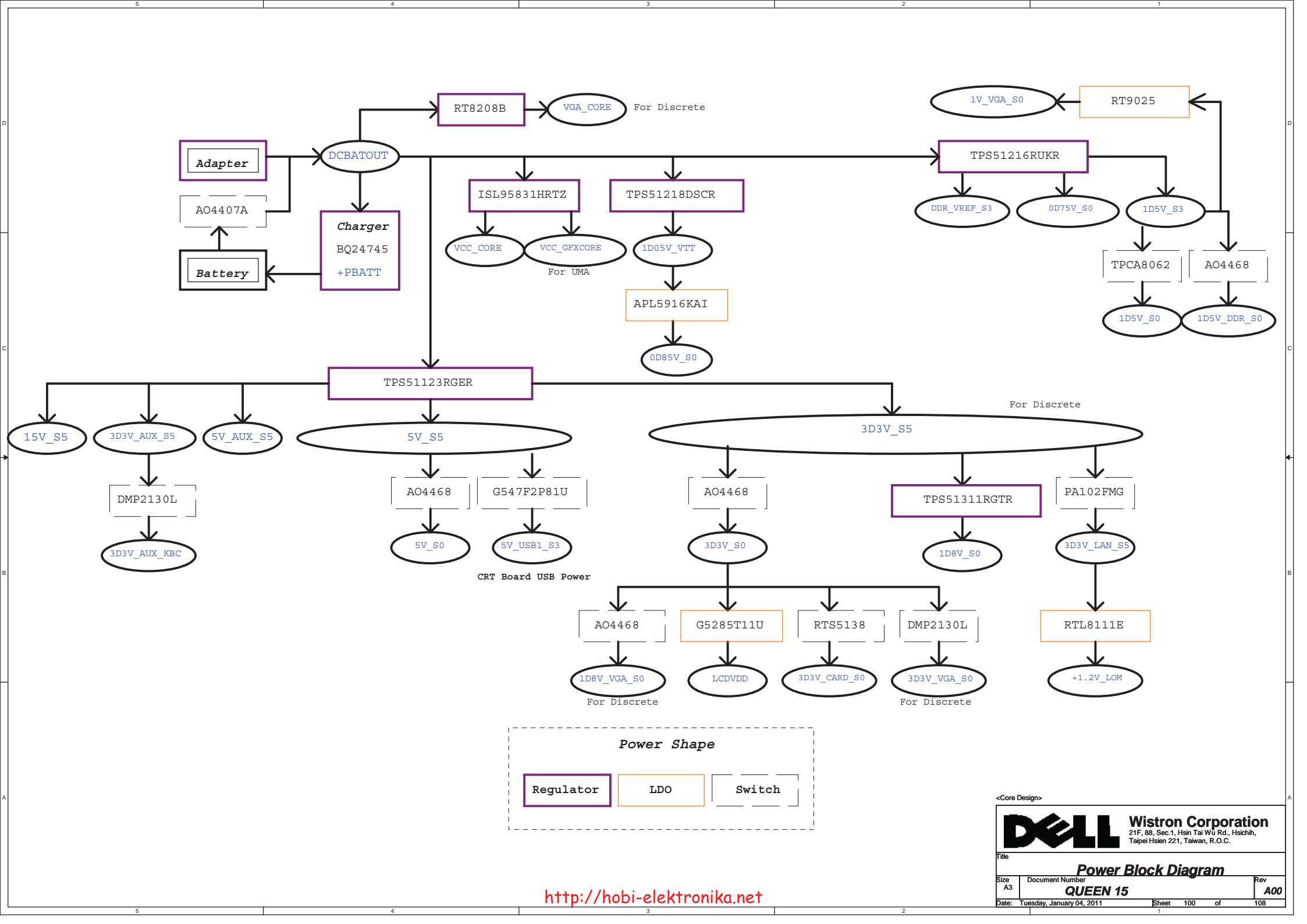
<http://hobi-elektronika.net>

Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



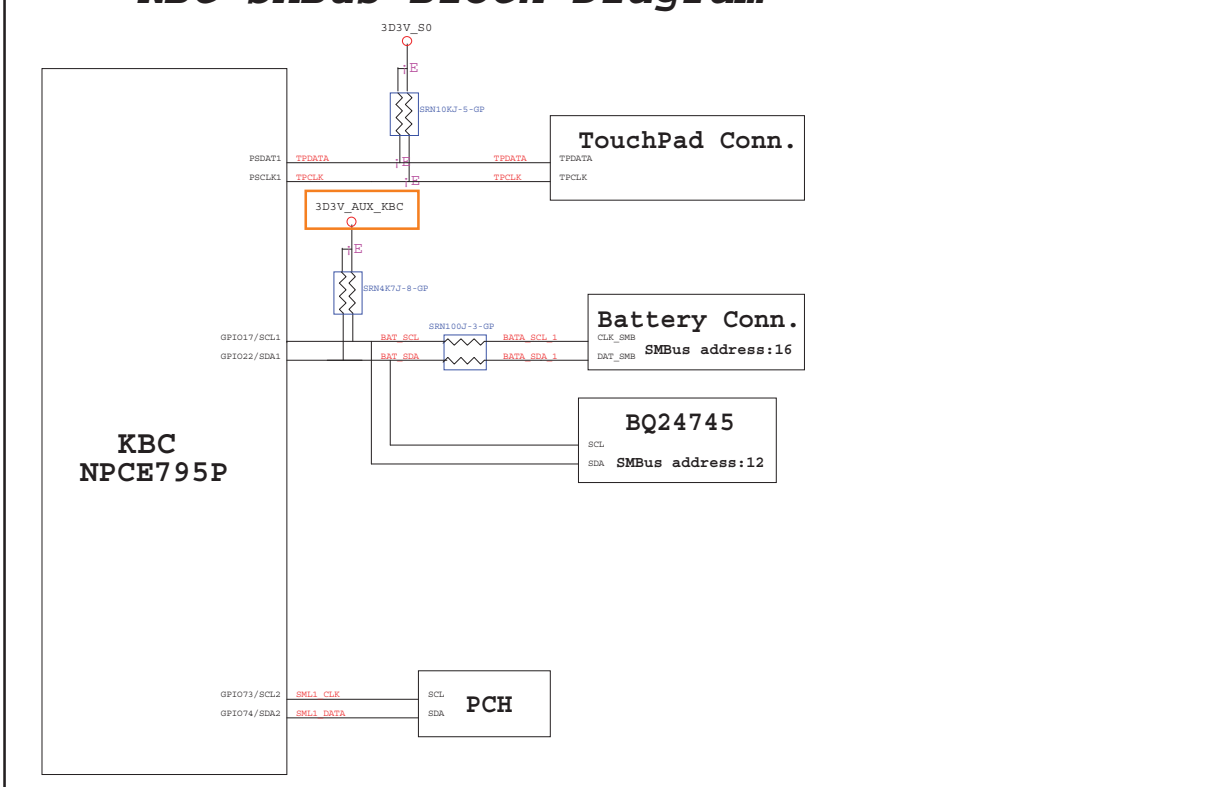
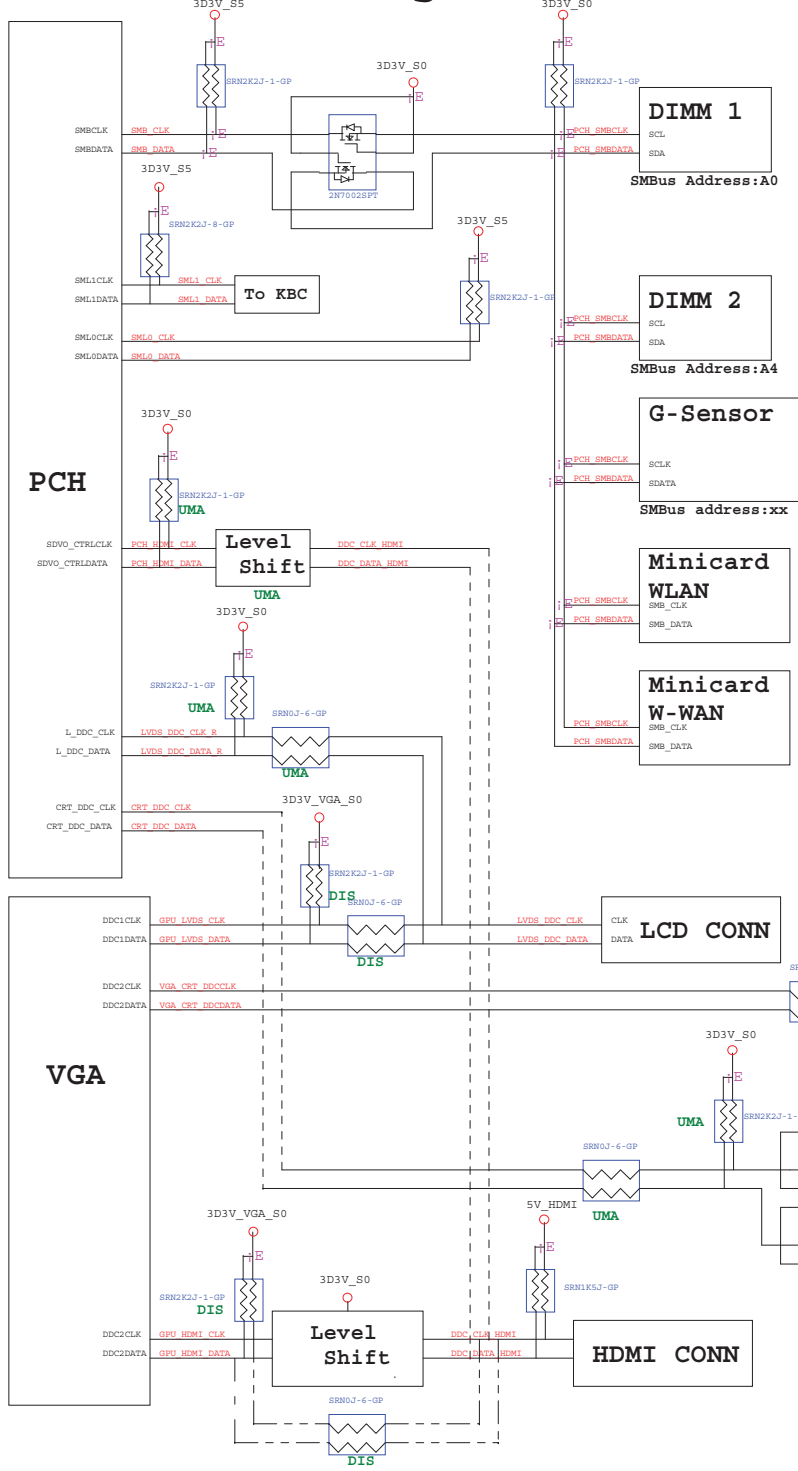
Power Up Sequence: -8 ~ 13

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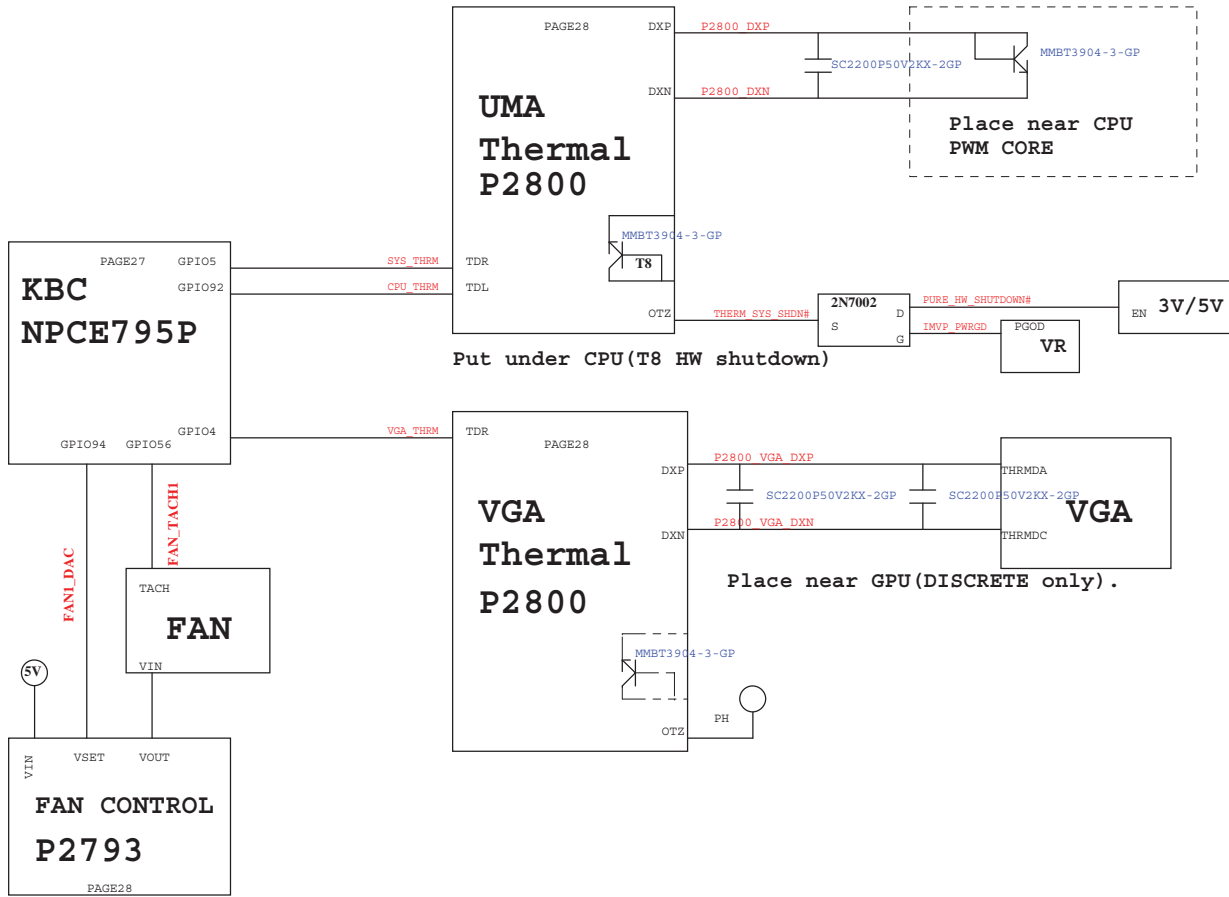
PCH SMBus Block Diagram

KBC SMBus Block Diagram

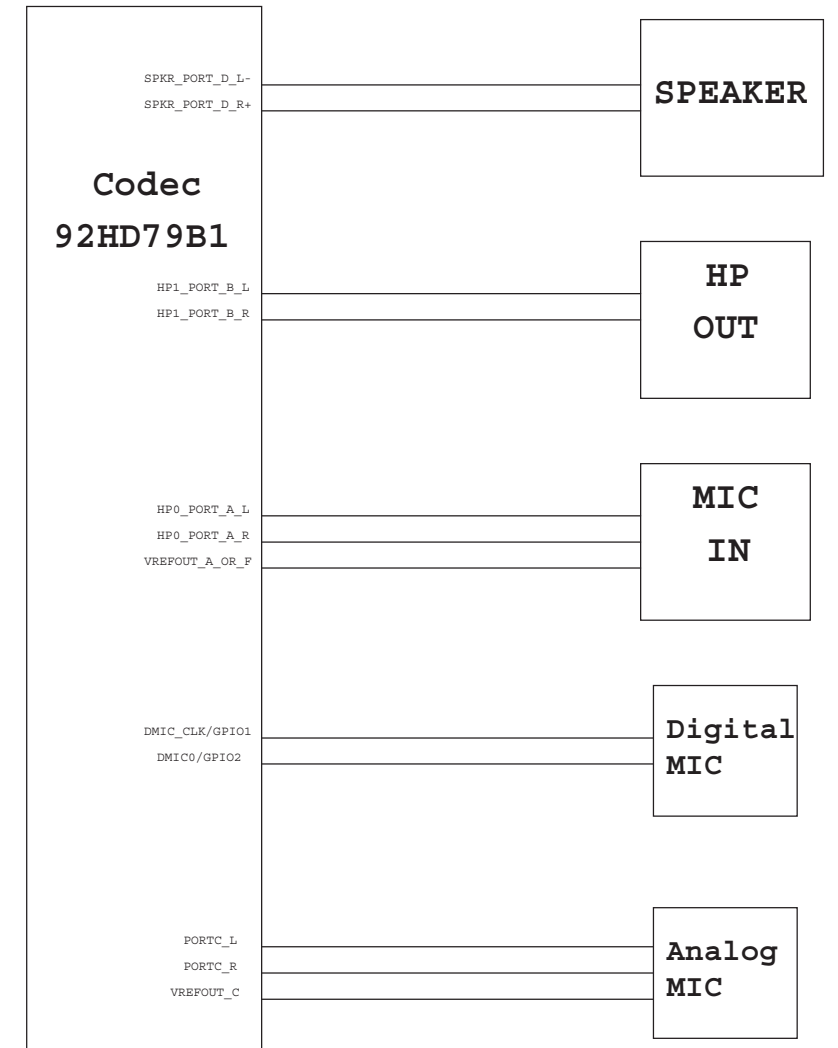


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Thermal Block Diagram



Audio Block Diagram



<Core Design>

VERSION	DATA	PAGE	Change Item
	08/25	14	SWAP SA0_DM1 and SA1_DIM1 each other for DM2 can't boot up issue.
	08/29	28	Change U2802 Main source to 74.00991.031, 2nd 74.02793.A31,3rd 74.05606.071
	08/29	61	Add 2nd 77.C1071.20L on TC6101.
	08/29	64	Re-assign FP1 pin define.
	08/29	71	Un-stuff Debug port connector(DB1) on X01.
	08/29	37	Change U3701 pin2 to RUNPWROK from 0D75V_EN. Reserved R3717 0ohm between PM_DRAM_PWRGD and VDDPWGOOD_R.
	08/29	37	Change R2724 to 20K 0402 from 10K for X01 stage.
	08/29	40	Change 3D3V_AUX_S5 to 3D3V_AUX_KBC to avoid leakage Voltage to 3D3V_AUX_KBC under DC mode.
	08/31	51	HDMI1 change to 22.10296.311 from 22.10296.271
	08/31	28	FAN1 change to 20.F0772.003 from 20.F1639.004
	08/31	57	E-SATA1 change to 22.10321.W11 from 22.10290.141
	09/01	41	PU4104 and PU 4105 horizontally mirror.
	09/01	83	R8305 Change to 30K ohm.
	09/01	97	H1, HS, H13, H7 and H15 change to ZZ.00PAD.J91 from ZZ.00PAD.D01.
	09/01	56	HDD1 add 2nd=62.10065.121.
	09/01	79	U7901 change main source to 74.00351.0B3.
	09/01	42	PR4226 change to 5.62K ohm.
	09/01	45	PTC4502 change to 79.3971V.30L.
	09/03	61	U6101 add 2nd=74.00547.079.
	09/03	49	U4901 add 2nd=74.09724.09F.
	09/03	40	PU4002 and PU4003 add 2nd=84.P1403.B37.
	09/03	24	L2401,L2402,L2403 add 2nd=68.10090.10B.
	09/03	27	DY C2713. Add C2722.
	09/03	47	Add PR4702
	09/03	22	Change FFS_INT2_R from PCH GPIO48 to GPIO15 Removed R2220 and change R2201 default pull up to pull down.
	09/06	20	X2001 add 3rd=82.30020.A31.
	09/06	56	U5601 add 2nd=74.02191.079.
	09/06	93	PU9303 add 2nd=74.05930.03D.
	09/06	37	U3701 add 2nd=73.7SZ08.DAH.
	09/06	23	Add 2nd and 3rd for L2301.
	09/06	23	R434 change name to PR9321. Add PC9324 and PR9319 for soft start.
	09/06	61	TC6101=80.10715.B1L, 2nd=77.C1071.21L, 3rd=77.C1071.20L.
	09/06	56	ODD1 add 2nd and 3rd source. HDD1 add 3rd source.
	09/06	49	LCD1 add 2nd source.
	09/06	69	TPAD1 add 2nd.


X01

VERSION	DATA	PAGE	Change Item
	09/06	15	DM1 2nd=62.10017.Q31, 3rd=62.10017.K01.
	09/06	14	DM2 2nd=62.10017.P31, 3rd=62.10017.K11.
	09/07	68	Add 2nd source 20.K0343.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/07	69	Add 2nd source 20.K0343.004 on KBLIT1 base on updated connector list.
	09/07	82	Add 2nd source 20.F0085.040 on CRTBD1 base on updated connector list.
	09/07	64	Add 2nd source 20.K0382.006 on FP1 base on updated connector list.
	09/07	75	Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.
	09/07	4-10	Updated CPU1 footprint to SKT-BGA989C470395-1H180 from SKT-BGA989C470395-1H186 base on data base updated. Add 2nd source 62.10040.771 on CPU1 base on updated connector list.
	09/07	75	Change CARD1 to 20.I0129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.
	09/07	93	PQ9308 change name to PQ9311.
	09/07	ALL	Change all of single 2N7002 to 84.2N702.J31 from 84.2N702.D31 due to 84.2N702.D31 will EOL.
	09/07	28	Change U2801,U2803 to 74.02800.A71 from 74.02800.071 from vender updated parts. Change R2803&R2817 to 107K from 499K,R2804&R2818 to 226K from 102K base on updated ADJ Table.
	09/08	18, 22	Change FFS_INT2_R from PCH GPIO48 to GPIO14 Keep PCH_GPIO5 PH R2201,PCH_GPIO48 PH R2220. Add R1818.
	09/08	82	1.Rename IOBD1 pin20,22,26,28 to IOBD1_20,22,26,28 from PCIE_TXN5,PCIE_TXP5,PCIE_RXP5,PCIE_RXN5. 2.Add RN8207,RN8208 for optional USB3.0 PCIE or USB2.0 signal.
	09/08	18	Reserved USBP9-USBP10 to IOBD1 pin20,22,26,28.
	09/08	37	Stuff Q3704,R3710; un-stuff R3716. U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.
	09/08	20	DY R2002.
	09/08	47	Mount PC4710.
	09/08	98	Update N12P power sequence.
	09/09	82	R8201, R8202 and R8203 change to 62 ohm.
	09/10	45	Change PL4501 to 68.2R210.20C from IND-D56UH-27-GP base on Brian updated.
	09/10	41	Change PL4101,PL4102 to 68.2R210.20B from 68.2R210.20Q base on Brian updated.
	09/10	82	Rename IOBD1 pin14 to IOBD1_14 from USB30_SMI#. Add R8207 for USB20 USB_OC#10_11 Add R8206 for USB30 USB30_SMI# Add R8208 for USB20 USB signal. Add R8207 for USB30 PCIE signal.
	09/10	49	Add TPNL1 for touch panel solution 4pin connector. Change LCD1 to 20.F1816.030 for 30pin Re-assign LCD1 pin define base on Roy updated cable pin define list.
	09/10	51	Change HDMI1 part number to 22.10296.331 from 22.10296.311 base on ME Double updated.

X01

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<Core Design>

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Change History			
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	09/13	83	Change X8501 to 82.30034.641;2nd 82.30034.651;3rd 82.30034.681 from sourcer suggestion.
	09/13		Change KBLIT1, PWRBTN2 and TPAD1 2nd source from 20.K0343.004 to 20.K0382.004.
	09/13	47	Change 1.8V power solution.
	09/14	82	Change R8201-R8203 to 470ohm from 100ohm. Add RN8209 PH 5V_S5 on MEDIA_LED1-3# for PWM OD mode.
	09/14	40	Add 2nd source 84.04835.H37 on PU4002,PU4003 base on Brian updated 2nd source excel file.
	09/14	58	Change SPK1 to 20.F0772.004 from 20.F1647.004 from Double updated.
	09/14	51	Add R5101-R5108and reserved TR5101-TR5104 on all of HDMI differential pair for EMC suggestion. Rename HDMI1 CONN NET name.
	09/14	29	Add R2920,R2921 and reserved EC2901,EC2902 on AUD_DMIC_CLK &AUD_DMIC_IN0 for EMC suggestion.
	09/14	75	Add R7503,R7504 and reserved EC7501,EC7502 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion. Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R. Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C
	09/14	20	Reserved EC2004,EC2005 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion.
	09/14	49	Reserved EC4910-EC4915 on LVDS signal for EMC suggestion.
	09/15	58	Re-assign SPK1 pin define base on Roy updated excel file for 20.F0772.004
	09/15	51	Add 2nd source 22.10296.311 on HDMI1 from updated connector list.
	09/15	68	Add 2nd source 20.K0382.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	49	Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.
	09/15	28, 51,82	Add test point for WKS AFTE request.
	09/15	All	ADD 2nd source follow Power team suggestion.
	09/15	92, 93	Modify PR9318 and PR9228 power source from 3D3V_AUX_S5 to 3D3V_S5.
	09/15	86	Reserve Q8602, C8603 and R8606 for VGA over temp.
	09/15	20	RN2005 swap net.
	09/15	19	RN2005 swap net.
	09/15	48	Change PR4809 to 10K from 100K PH power source change to 3D3V_S0 from S5.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	97	Reserved EC9701-EC9723 0.1uF for RF suggestion.
	09/15	41	Un-stuff PU4101,PD4105,PR4124, PR4125,PR4101 at X01 stage for 5mW issue.
	09/15	69	un-stuff R6907 and stuff R6905,Q6902,R6906 for 5V drive CAP LED.
	09/17	82	Change IOBD1 part number to 20.F1849.080 base on Double updated latest DXF&EMN.
	09/17	49,57 32,64	stuff TR4901 and un-stuff R4911,R4912 at X01 stage from EMC Neo suggestion. stuff TR4902 and un-stuff R4908,R4909 at X01 stage from EMC Neo suggestion. stuff TR5701 and un-stuff R5718,R5719 at X01 stage from EMC Neo suggestion. stuff TR3201 and un-stuff R3211,R3210 at X01 stage from EMC Neo suggestion. stuff TR6401 and un-stuff R6403,R6404 at X01 stage from EMC Neo suggestion.
	09/17	20	Change RN2010-RN2016 to 33ohm from 0ohm from EMC Neo suggestion.
	09/17	37	Change R3710 to 100K from 0ohm to avoid impact L05VTT_PWRGD turn off sequence directly.
	09/17	17	Add R1703-R1705 on RGB signal and reserved EC1701-EC1703 0.1u from EMC Neo suggestion.

VERSION	DATA	PAGE	Change Item
	09/17	40,41	Stuff EC4002 0.1uF from EMC Neo suggestion. Stuff EC4008 0.1uF from EMC Neo suggestion. Stuff EC4102,EC4103 0.1uF from EMC Neo suggestion. Stuff EC4107 0.1uF from EMC Neo suggestion. Stuff PC4119,PC4120 0.1uF from EMC Neo suggestion. Stuff EC4006,EC4007 0.1uF from EMC Neo suggestion.
	09/17	60,18	EC6001 change to 10p from 4.7p and default stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default stuff from Neo suggestion.
	09/17	44	default stuff EC4407,EC4405,EC4403,EC4410 base on EMC Neo suggestion.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	82	Change R8201-R8203 to 430ohm.
	09/17	48	Change PR4809 to 4.7K from 100K PH power source change to 3D3V_S0 from S5.
	09/17	40,27,83	Rename PCIE_RST# to AD_IA_HW2 on KBC GPIO50 for power Tom suggest. Reserved PQ4004,PR4036,PR4037 for AD_IA_HW2 function.
	09/17	68	Rename CHARGER_LED1 to CHARGERLED1. Rename FPOWER_LED1 to FPOWERLED1. Rename HDD_LED1 to HDDLED1. Rename TP_LOCK_LED1 to TPLOCKLED1. Rename TP_LOCK_LED2 to TPLOCKLED2. Rename WLAN_LED1 to WLANLED1
	09/17	21,22	Base on layout routing,Add RN2104 10K instead of R2111 10K. Move EC_SCI#_DBC_EN to RN2201. Move S_GPIO to RN2103. Move PSW_CLR# to RN2104.
	09/17	56	Change R5605 to 100K from 10K and PH to 5V_S0 from 3D3V_S0 to meet Vgs>2V turn on.
	09/17	56	Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.
	09/17	ALL	Change all of 0402 0ohm to 0R0402 short pad. PR4008,PR4010,PR4012,PR4020,PR4023,PR4024,PR4027,PR4028,PR4029,PR4225,PR4102,PR4113,PR4118, PR4121,PR4203,PR4204,PR4215,PR4222,PR4231,PR4243,PR4301,PR4509,PR4510,PR4801,PR4804,PR4805, PR4808,PR4810,PR9211 F4902,PR4017,PR4018,PR4106,PR4611,PR4710,PR4807,R2304,R2403,R2406,R2409,R2702,R2902,R2903,R2904 R2305
	09/20	9	Add 2nd for TC901.
	09/20	83	Add 2nd for L8303.
	09/20	82	Add 2nd for LD8201.
	09/20	86	Add 2nd for Q8601.
	09/20	83	Add R8321. C8353 and C8354 change to 12pF.
	09/20	82	Redefine IOBD1.
	09/20	75	AFTP111 and AFTP110 connect to USB_PP13_R and USB_PN13_R.
	09/20	51	Change P/N of Q5102.
	09/21	42	Change PU4201 VDD power source to 5V_S5 from 5V_S0 to avoid abnormal MVP_PWRGD waveform.
	09/21	47	stuff PC4714 22uF from Brian updated.

X01

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<Core Design>



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Title: **Change History**

Size A3	Document Number QUEEN 15	Rev A00
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VERSION	DATA	PAGE	Change Item
	09/21	45	Change PR4507 to 20K from 20.5K from Brian updated.
	09/21	46	Change PR4602 to 110K from 68K from Brian updated.
	09/21	42	Change PR4217 to 1.27K from 1K from Brian updated. Change PR4213 to 3.6K from 3.16K from Brian updated. Change PR4236 to 3.01K from 3.32K from Brian updated.
	09/21	44	Change PC4410 to 0.01u from 0.022uF from Brian updated.
	09/21	39	Add 2nd 83.00099.K11;3rd 83.00099.T11 on D3901,D3902,D3903 from Sourcer Eden suggestion.
	09/21	39	Add 2nd 84.02143.011;3rd 84.00143.N11 on 6801,Q6804,Q6805,Q6806,Q6807,Q6808 from Sourcer Eden suggestion.
	09/21	43	Change PU4303,PU4306,PU4309 dummy field only for QC CPU stuff. Change PC4307,PC4316 dummy field only for QC CPU stuff. Add 2nd for PTC4306.
	09/21	41	PD4101, PD4103, PD4104 and PD4105 add 2nd source.
	09/21	69	Q6902 add 2nd source.
	09/21	40	PD4001 add 2nd source.
	09/21	19	move PCH_WAKE# to RN1901 pin4;Add R1909 PH 100K on AC_PRESENT.
	09/21	37	R3710 change to 0ohm. Remove R3701 and C3701.
	09/21	42	Add PR4214, PC4230, PR4216 and PC4231 from Brian updated.
	09/23	20	RN2016, RN2010, RN2011, RN2012, RN2014 and RN 2013 keep 0ohm.
	09/23	ALL	PR9216, R504, R1812,R1813,R1815,R1817, R1903, R1906,R1910,R1912,R1913,R1924,R1925, R2213,R2219, R2711,R2720,R2733,R2761, R2807,R2814, R3708, R5125, R5127, R5721, R5722.
	09/23	75	Add R7505-R7508 0ohm and reserved EC7503-EC7506 on PCIE_TX8&RX8 signal base on EMC Lance suggestion. Add R7509,R7510 0ohm and reserved EC7507,EC7508 on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base on EMC Lance suggestion.
	09/23	ALL	RN5101, RN2201, RN1702, RN1901, RN1705 swap pin.
	09/23	79	DUMMY G-SENSOR.
	09/23	92	Update value of PR9210, PR9209 and PR9213 for N12P.
	09/23	43	PR4320 change to 4 m ohm.
	09/23	68	Add 2nd source 83.00110.J70 on FPOWERLED1,HDDLED1,WLANLED1 from Sourcer Anya suggestion. Add 2nd source 83.00326.G70 on CHARGERLED1from Sourcer Anya suggestion. Add 2nd source 83.00190.Z70 on TPLOCKLED1,TPLOCKLED2 from Sourcer Anya suggestion.
	09/23	69	Change KBLIT1 part number to 20.K0589.004 and re-assign pin define base on Roy updated.
	09/23	42, 44	Add 2nd source 69.60011.201 on PR4405,PR4245 from Sourcer Kitty suggestion.
	09/23	42	Add 2nd source 69.60037.021 on PR4246,PR4247 from Sourcer Kitty suggestion.
	09/24	23	Add 2nd source 68.00214.211 on L2301 updated from DN13ATI.
	09/24	68, 69	Change R6806,R6808,R6811-R6813,R6801,R6803,R6815,R6906 to 390ohm from 1K to fine tune all of MB LED for 5mA spec.
	09/27	51	Reserve R5114 and R5115.
	09/27	85	Reserve R8510 and R8513.
	09/27	83	DY U8301, mount R8323.
	09/27	92	R9206 change to 10K, PC9211 mount 0.1u.
	09/27	93	R9312 change to 1K.

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VERSION	DATA	PAGE	Change Item
	09/27	49, 57 32, 64	TR4901, TR4902, TR5701, TR3201 and TR6401 DY. Stuff 0 ohm.
	09/27	69	AFTP73 connect to TP_VDD.
	09/27	85	U8501 power change to 3D3V_S0.
	09/27	92	PL9201 change like CPU core power choke.
	09/28	83, 84	L8303, L8401, L8402, L8502 and L8503 follow NV DG spec.
	09/28	46	Change PR4606 to 4.02K from 240ohm for fine tune 1.5V output Voltage.
	09/28	92	PTC9202, PTC9203 and PTC9204 2nd=79.47719.9BL
	09/28	22	Change R2220 to 10K from 100K.
	09/28	60	EC6001 change to 10p from 4.7p and default un-stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default un-stuff from Neo suggestion
	09/28	27	Change R2710, R2739, R2724 and R2726 change to 1%.
	09/29	27	Default mount R2756, Dummy R2734.
	10/04	24	Add 2nd source 68.1001E.10N on L2401,L2402,L2403 from sourcer Renee Lee updated.
	10/07	43	PTC4306 cahnge second source to 79.47612.60L.
	10/09	85	Change L8503 to 68.00375.091,and add second source 68.00206.171
	10/09	85	Change L8502 to 68.00115.191,and add second source 68.00206.131
	10/09	84	Change L8401 and L8402 to 68.00115.181,and add second source 68.00206.341
	10/09	83	Change L8303 to 68.00375.101,and add second source 68.00119.101
	10/09	83	Change L8301 to 68.00115.161,and add second source 68.00206.111
	10/09	42	Change PR4217 to 64.84505.6DL for Dual-core OCP
	10/09	42	Change PR4213 to 64.23715.6DL for Dual-core loadline
	10/09	42	Change PR4207 to 64.22025.6DL for CPU(35W) Turbo setting
	10/09	42	Change PR4202 to 64.22025.6DL for GFX Turbo setting
	10/09	20,83	Dummy R2004 R2003 and PQ8309, stuff R2005
	10/19	28	Change R2817 from 107K to 124K (64.12435.6DL) for VGA temperature setting change
	10/25	84	Change R8402 from 40D2R to 60D4R (64.60R45.6DL) for meeting the spec
	10/25	14 15	Add DM1 and DM2 second source:62.10017.Q41 and 62.10017.P61
	10/25	85	Ventura SMBC_INA219_C and SMBD_INA219_C add 3.3V pull high schematic
	11/01	51 85	Change HDMI HPD schematic for cost down
	11/10	27	Change R2724 to 64.33025.6DL for PCB version change
	11/10	83	Change L8301 to 68.00115.181,and add second source 68.00206.341

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	11/11	14	DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.
	11/11	15	DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.
	11/11	60	U6001 1st change to 72.25Q32.A01; 2nd change to 72.25320.C01; 3rd change to 72.25P32.C01 on ST stage
	11/11	68	Change CHARGERLED1 2nd to 83.00327.D70 from Sourcer updated.
	11/11	37	Change U3701 1st to 73.7SZ08.EAH;2nd to 73.01G08.L04;3rd to 73.7SZ08.DAH from Sourcer Eason updated.
	11/11	69	Add 2nd 20.K0592.030 on KB1 from ME updated connector list.
	11/11	82	Add 2nd 20.K0465.008 on MEDIA1 from ME updated connector list.
	11/11	58	Add 2nd 20.F1804.004 on SPK1 from ME updated connector list.
	11/11	28	Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.
	11/11	70	Add 2nd 20.F0962.010 on HALL1 from ME updated connector list.
	11/11	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0.
	11/11	60	Add Q6002,R6007 fo FACTORY RTC detect function
	11/11	28	ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.
	11/11	28	Reserved G709T1UF for T8 solution sync with DN13.
	11/12	82	Change R8201, R8202, R8203 from 430 ohm to 1K ohm (63.10234.IDL) for soluting media board LED brightness is too light issue
	11/15	49	Add 2nd 20.F1860.030 on LCD1 from ME updated connector list.
	11/15	8	Reserved C802-C804,C806,C807 10uF 0603 for power team fine tune Vcore quality
	11/15	88 89 90 91	All of VRAM(VRAM1-VRAM8) PCB footprint change to CO-LAY type (DUMMY-BGA96D075133H48) from BGA96D0913H48 same as DW30.
	11/15	68 69	Change R6813, R6906 from 390 ohm to 1K ohm (63.10234.IDL) for soluting LED brightness is too light issue
	11/15	20	Dell required us to disable PCIE port of WWAN slot ,If PCIE port 1 is disabled, it will cause all PCIE port disabled,so change WWAN to PCIE port 3 from port1 at ST stage.
	11/16	97	Change HHD1 HDD4 HGPU1 HGPU2 2nd from 34.4CK01.201 to 34.4CK01.401 from ME update connector list
	11/16	68	Change R6808, R6811 from 390 ohm to 1K ohm (64.10234.IDL) for soluting LED brightness is too light issue
	11/16	28	stuff both G709T1UF and P2800 related circuit, add R2805 0ohm default un-stuff at ST stage.
	11/17	48	CO-LAY APL5916 related circuit for VCCSA LDO solution.
	11/18	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2301 and un-stuff L2301.
	11/18	28	Add R2805 0hm between THERM_SYS_SHDN#_OTZ and THERM_SYS_SHDN#. Add R2812 0ohm between THERM_SYS_SHDN# and U2805 pin3.

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VERSION	DATA	PAGE	Change Item
	11/18	28	Rename U2801&U2804 pin 8 to THERM_SYS_SHDN#_OTZ from HERM_SYS_SHDN#.
	11/18	20	Change X2001 to 82.30020.D41 from 82.30020.851 from Sourcer Dick updated.
	11/18	23	Reserved R2308,R2309 on VCCVRM power rail.Reserved U2302 LDO circuit on VCCVRM power rail
	11/18	22 82	Rename USB3_PWR_ON to PCH_GPIO57. Add R8209,R8210 for PM_SLP_S4# and VGA_THRM to control USB3_PWR_ON
	11/18	48	Change PTC4801 to 100u(77.21071.07L) from 150u from power team Brian updated
	11/19	74	Add 2nd 20.I0135.001 on CARD1 from ME updated connector list.
	11/19	82	Add 2nd 20.F1908.080 on IOBD1 from ME updated connector list.
	11/20	3	Updated PCIE ROUTING
	11/20	28	Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2812, un-stuff R2805
	11/20	23	Reserved R2308 on VCCVRM power rail. Reserved U2302 LDO circuit on VCCVRM power rail.
	11/20	48	Set TPS51461 PWM solution dummy field for VCCSA_PWM and APL5916 LDO solution dummy field for VCCSA_LDO. default stuff VCCSA_LDO at ST stage
	11/20	22	Rename GFX_CRB_DET to GSENSOR_DET on GPIO39.
	11/20	60	Un-stuff R6007 10M.
	11/20	82	Reserved EC8201,EC8202 0.1u(closed H3) between AGND and GND from EMC Neo suggestion.
	11/20	82	Reserved EC8203-EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/20	82	Add RN8205 base on HSYNC&VSYNC report
	11/20	61	Removed R6101 and connect USB_PWR_EN# to U6101 pin4 directly.
	11/20	22	Rename PCH_GPIO12 to RTC_DET# on GPIO12.
	11/20	61 22 18	Reserved U6102 USB POWER related circuit to separate EATA and CRT USB power in ST build. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/20	82	Reserved R8211,R8212 0ohm 0805 on CRTBD1 pin37,39 to separate EATA and CRT USB power in ST build.
	11/22	82	Swap RN8205 pin4,3 and pin2,1 each other base on Connie swap report.
	11/22	82	stuff EC8201,EC8202 0.1u(closed H3) between GND and GND from EMC Neo suggestion. stuff EC8206 between 3D3V_S5 and GND from EMC Neo suggestion.
	11/22	23	base on layout condition change 3D3V_DAC_S0 circuit. Stuff R2301 and un-stuff L2301.
	11/22	82	stuff EC8203-EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/22	23	Removed U2302 LDO for VCCVRM.

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	11/22	29	change R2920,R2921 to 22ohm from 0ohm and stuff EC2901,EC2902 22p from EMC Neo updated.
	11/22	61	Change U6101 to dual USB power switch from single for Layout limitation and placement. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/22	49	stuff C4908 0.1uF from EMC Neo suggestion.
	11/22	57	Change TR5701 to 69.10103.041 and un-stuff R5718,R5719 from EMC Neo Suggestion.
	11/22	49	Change TR4902 CM choke to 69.10103.041 and un-stuff R4908,R4909 from EMC Neo Suggestion.
	11/22	49	Swap TR4901 pin4,3 and pin2,1 each other base on Connie swap report. Change TR4901 CM choke to 69.10103.041 and un-stuff R4911,R4912 from EMC Neo Suggestion.
	11/22	75	Change TR7501 CM choke to 69.10103.041 and un-stuff R7501,R7502 from EMC Neo Suggestion.
	11/22	58	stuff EC5801-EC5804 470pF from EMC Neo suggestion.
	11/22	9 39 45 49	stuff EC901, EC3903, EC4501, EC4909, EC4907 0.1uF from EMC Neo suggestion.
	11/22	49	Change RN4901 to 100ohm 4p from 8p for improve layout place.
	11/22	48	Updated VCCSA_LDO circuit from Power team Brian updated.
	11/22	83 84 85	Change L8301 L8401 L8402 to 0 ohm resistor (63.00000.00L)
	11/22	60	stuff R6007 10M.
	11/23	49 57 75	SWAPTR4901 TR4902 TR5701 TR7501 pin1&4 and pin2&3 each other base on Connie swap report.
	11/23	60	Change U6101 1st(74.02182.071);2nd(74.00546.A7D);3rd(74.02062.079) from Sourcer Harrison suggestion.
	11/23	64	Add C6402 0.1uF,C6403 180pF and stuff C6401 47pF from RF fine tune result.
	11/23	57 49 75	Change R5718,R5719,R4908,R4909,4911,R4912,R7501,R7502 to 0ohm 0603 from 0402.
	11/23	56 97	stuff EC9739,EC9737,EC9735 47pF from RF fine tune result. stuff EC5601 180pF from RF fine tune result. Stuff EC9738 0.22uF closed EC9739 from RF fine tune result.
	11/23	97	stuff ECEC9729,EC9730 470pF from EMC Neo suggestion.
	11/23	45	Change PR4501 to 75K from 45.3K for 1.05V OCP set to 20A from Brian.
	11/23	82	Removed R8211,R8212 and connect 5V_USB2_S3 to CRTBD1 pin 37 directly.
	11/23	61	Removed C6105,C6103.
	11/23	69 70	Change AFTP 80 81 to AFTP 83 84; change AFTP 83 to AFTP82; change AFTP 82 to AFTP85.
	11/24	20	Add 2nd(82.30020.G71);3rd(82.30020.G61) on X2001 from Sourcer Dick updated.
	11/24	69	Add 2nd(20.K0613.004)on KBLIT1 from Karl updated.


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VERSION	DATA	PAGE	Change Item
	11/24	57	Add 2nd(22.10339.261)on ESATA1 from Karl updated.
	11/24	28	un-stuff VGA P2800 related circuit from Niki confirmed.
	11/24	64	rename C6401,C6402,C6403 to EC6401,EC6402,EC6403
	11/24	22	Dummy R2206
	11/25	28	Dummy R2817 R2818 C2816
	11/25	69	Add 3rd(83.00110.R70) on FPOWERLED1,HDDLED1,WLANLED1 from Anya provide
	11/25	69	Add 3rd(83.00192.J70) on TPLOCKLED1 and TPLOCKLED2 from Anya provide.
	11/25	69	Add 3rd(83.01108.070) on CHARGERLED1 from Anya provide.
	11/26	43 92	Change PC9217 PC4319 to 0.1u 50V
	11/29	83	Change C8353 C8354 to 15PF ,R8320 stuff from vendor suggestion.
	11/29	36	Stuff D3602
	11/30	68	Change 2nd source to 83.00322.070 from 83.00110.J70
	11/30	85	Change L8502 L8503 to 0 ohm
	11/30	92	Stuff PR9237 DY PR9321
	12/01	8	Change C837,C826 to 22uF from 10uF and default stuff from Power Brian updated.
	12/01	8	Change C801-C807 and C817 10uF stuff at QC CONFIG from power Brian updated.
	12/21	ALL	Change 0402 pad(ZZ.00PAD.M11): R1404 R1405 R1503 R1504 R1703 R1704 R1705 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R2762 R3614 R3710 R5114 R5801 R5802 R5803 R5804 R8210 R8323 R8511 R8512
	12/21	82	Change 0603 pad(ZZ.00PAD.M21): R8206 R8207
	12/21	17 20	Change resistor pad(ZZ.0R04P.ZZZ): RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2015 RN2016
	12/21	83 84 85	Change L8301, L8401,L8402,L8502,L8503 to 0R0603 pad(ZZ.00PAD.M21)
	12/21	ALL	Change to Parallel resistor R1501 ,R1502; R2739 ,R2774;R8202 ,R8203;R8501 ,R8502;R8506 ,R8507;R2123 ,R2124
	12/21	82	RN8205 change to R8201, R8202
	12/21	93	PR9237 rename to PR9337
	12/21	56 61 68	Delete 77.C1071.21L(TC6101), delete 83.01108.070(CHARGERLED) , delete 62.10065.121(HDD1)

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	12/22	27	R2724 change to 47K resistor for XBuild
	12/22	27	R2301 change to 0 resistor for CRT debug
	12/22	40	1.Change PR4032,PR4034,PR4037 to ZZ.00PAD.M11 2.Stuff PQ4003,PQ4004 3.Change PR4047 to 174K(64.17435.6DL) 4.Change PR4035 to 300K(64.30035.6DL) 5.Change PR4036 to 76.8K(64.76825.6DL) 6.Change PR4031 to 150K(64.15035.6DL)
	12/23	68	1.FPOWERLED1 rename to FPLED1 2.HDDLED1 rename to HDLED1 3.CHARGERLED1 renamtp to CHLED1 4.WLANLED1 rename to WLED1 5.TPLOCKLED2 rename to TPLED2 6.TPLOCKLED1 rename to TPLED1 7.PWRBTN1 rename to PWRBT1 8.PWRBTN2 rename to PWRBT2
	12/23	43	Delete PR4323,PR4324,PR4325; Stuff PR4320 for all BOM ,not co-lay Ventura
	12/23	92	Delete PR9220,PR9222,PR9223; Stuff PR9217 for all BOM ,not co-lay Ventura
	12/23	51	Change 5V_HDMI to 5V_CRT_S0_R for HDMI power leakage
	12/24	All	PRN3901 rename to PN3901 PTC9202-04 rename to PT9202-04 PTC4301-04 rename to PT4301-04 PTC4306 rename to PT4306 PTC4308-09 rename to PT4308-09 PTC4401-03 rename to PT4401-03 PTC4502 rename to PT4502 PTC4602 rename to PT4602 PTC4102 rename to PT4102 PTC4104 rename to PT4104
	12/24	28	Change U2802 3rd to 74.05606.A71 at X-Build batch run
	12/24	82	Change RN8205 to 66.22036.04L from 66.22036.040at X-Build stage
	12/24	82	Reserved R8211 0603 0ohm on F8201
	12/24	36	Reserved Q3603 2N702 on IMVP_PWRGD to fine tune glitch waveform when AC lose and DC lose.
	12/24	28	Change 3D3V_S0 to 3D3V_DAC_S0
	12/24	45 46 93	Change to short pad: PR4502,PR4607,PR9311,PR9312,PR9326. DUMMY PC4501
	12/27	28	If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.
	12/27	42	PR4207,PR4213,PR4217 DUMMY field set to DC&QC option
	12/28	51	Change 5V_HDMI to 5V_CRT_S0_R on RN5101
	12/28	28	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at XBuild

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	12/28	27	Change R2756, R2763, R2766 to short pad
	12/28	36	Stuff Q3603
	12/28	28 86	Cancel VGA Thermal sensor P2800 circuit
	12/28	27 28 82	Change to VGA_THRM to USB3_PWR_ON
	12/28	23	Change R2301 to short pad
	12/29	51	Change HDMI resistor to short pad
	12/29	49,57,75	Delete USB DUMMY resistor for no-lay
	12/29	32	Change USB 0 resistor to short pad for no-lay
	12/29	5	Reserve EC502 ,EC504 for EMI suggestion,add DUMMY EC505 for EMI
	12/29	82	Delete PM_SLP_S4# line, directly link to USB3_PWR_ON
	12/29	23	Add 3rd Richtek(74.09198.G7F) on U2301 at XBuild batch run config
	12/29	68	Not use Liteon LED(83.00322.070) for package
	12/30	5	Add DUMMY diode EC506 for BUF_CPU_RST# as EMI suggestion
	12/30	42	PC4227 change to 78.33420.5FL as 78.33423.5FL obsoleted
	12/30	49	Change R4904 to short pad
	12/31	86	Add probe point for P2800_VGA_DNX/P2800_VGA_DXP
	01/03	68	Change TPLED1,2 1st to 83.01921.P70 ,2nd to 83.00190.S7A,3rd to 83.00191.H70; R6813 change to 390R from 1K same as DN13 LED part.
	01/03	49	Delete R4908, R4909 for USB_Camera not co-lay
	01/03	4-10	Add 3rd foxconn(62.10055.321) on CPU1 at X-Build batch run config
	01/03	82	Add 3rd T-conn(20.F1932.040) on CRTDB1at X-Build batch run config
	01/03	97	Add 3rd LIDON(34.4CK01.501) on HHD1,HHD4,HGPU1,HGPU2 at X-Build batch run config
	01/04	68	Delete 83.00191.H70 for TPLED1,2 as cost high
	01/04	49,57,75	Add 2nd TAI-TECH(69.10084.071) on TR4901,TR4902,TR5701,TR7501 at X-Build batch run config

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