PROJECT :ZAVA1/ZAVC1
PCB NO : DA60018A000 LA-B016P-R1.0

Compal Confidential

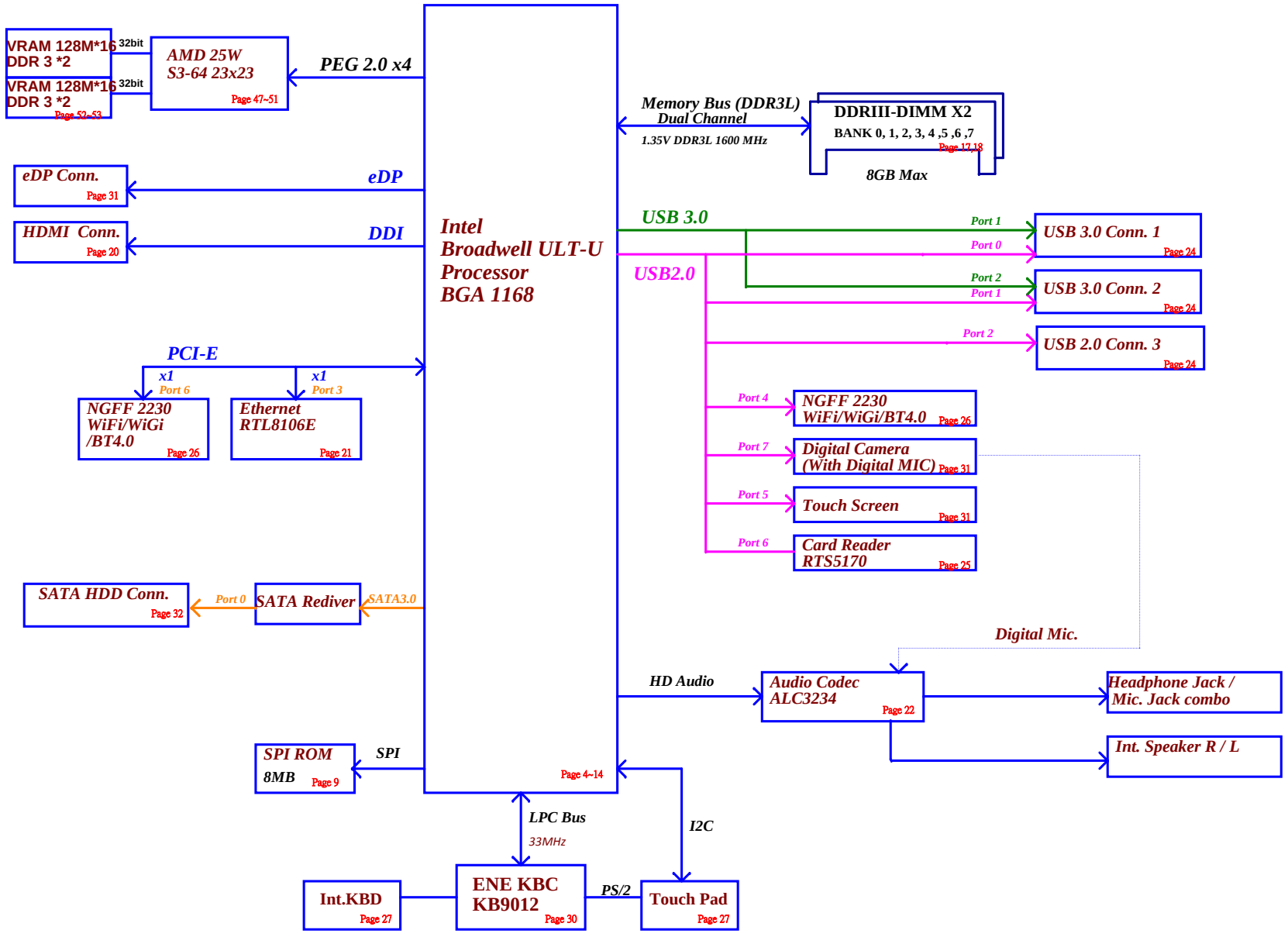
Schematic Document

Intel Shark Bay ULT
UMA / DIS AMD 25W/S3+DDR3x4

2014-10-20 Rev: 1.0

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2018/03/31

Compal Electronics, Inc.		
Title: *Cover Page*		
Size:	Document Number: *LA-B016P*	Rev: 1.0
Date: Friday, October 24, 2014	Sheet 1 of 56	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/26	Deciphered Date	2018/03/31

Title	Block Diagram		
Size	Document Number		Rev
	LA-B016P		1.0
Date:	Friday, October 24, 2014	Sheet 2 of 56	

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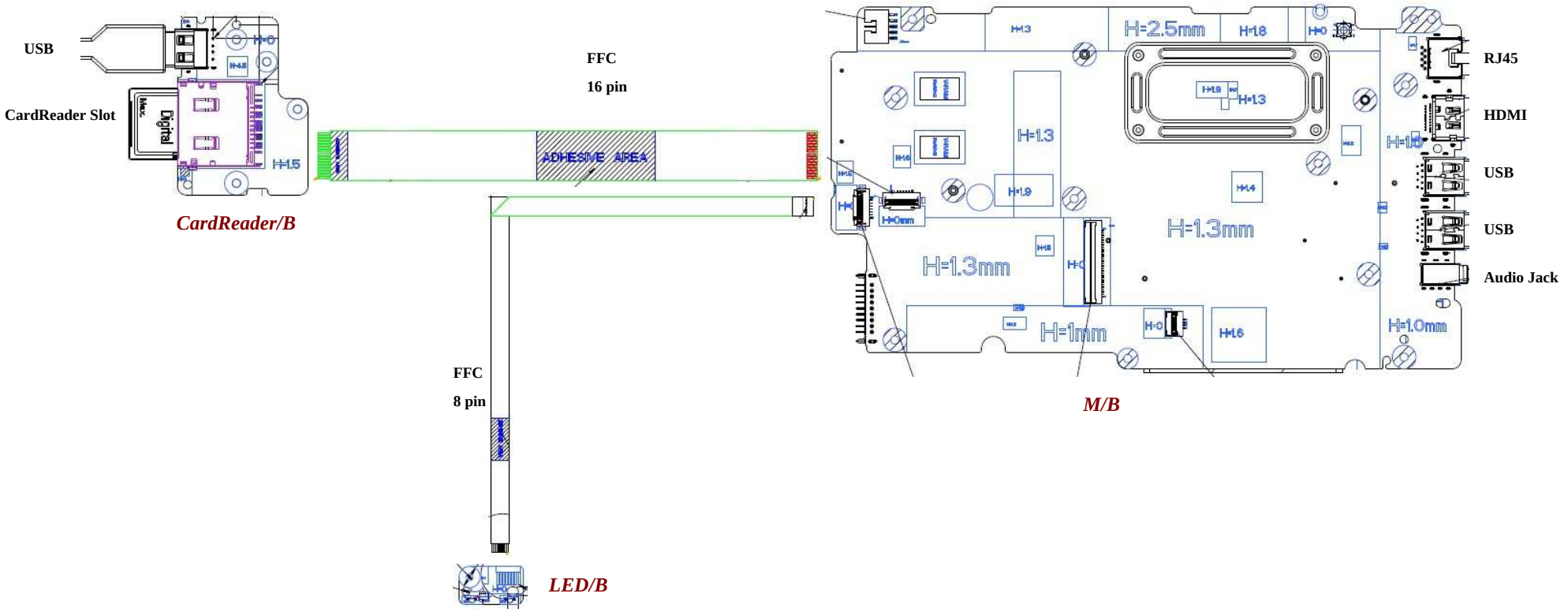
Project: ZAVA1/ZAVC1
File Name : LA-B016P



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2018/03/31

Compal Electronics, Inc.		
Title: MB & DB Ass'y		
Size	Document Number: LA-B016P	Rev: 1.0
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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

BDW 3D BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	Pre-SSI		
1		Pre-SSI	
2			Pre-SSI
3	SSI		
4		SSI	
5			SSI
6	PT		
7		PT	
8			PT
9	ST		
10		ST	
11			ST
12	1.0		
13		1.0	
14			1.0

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V	V		V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

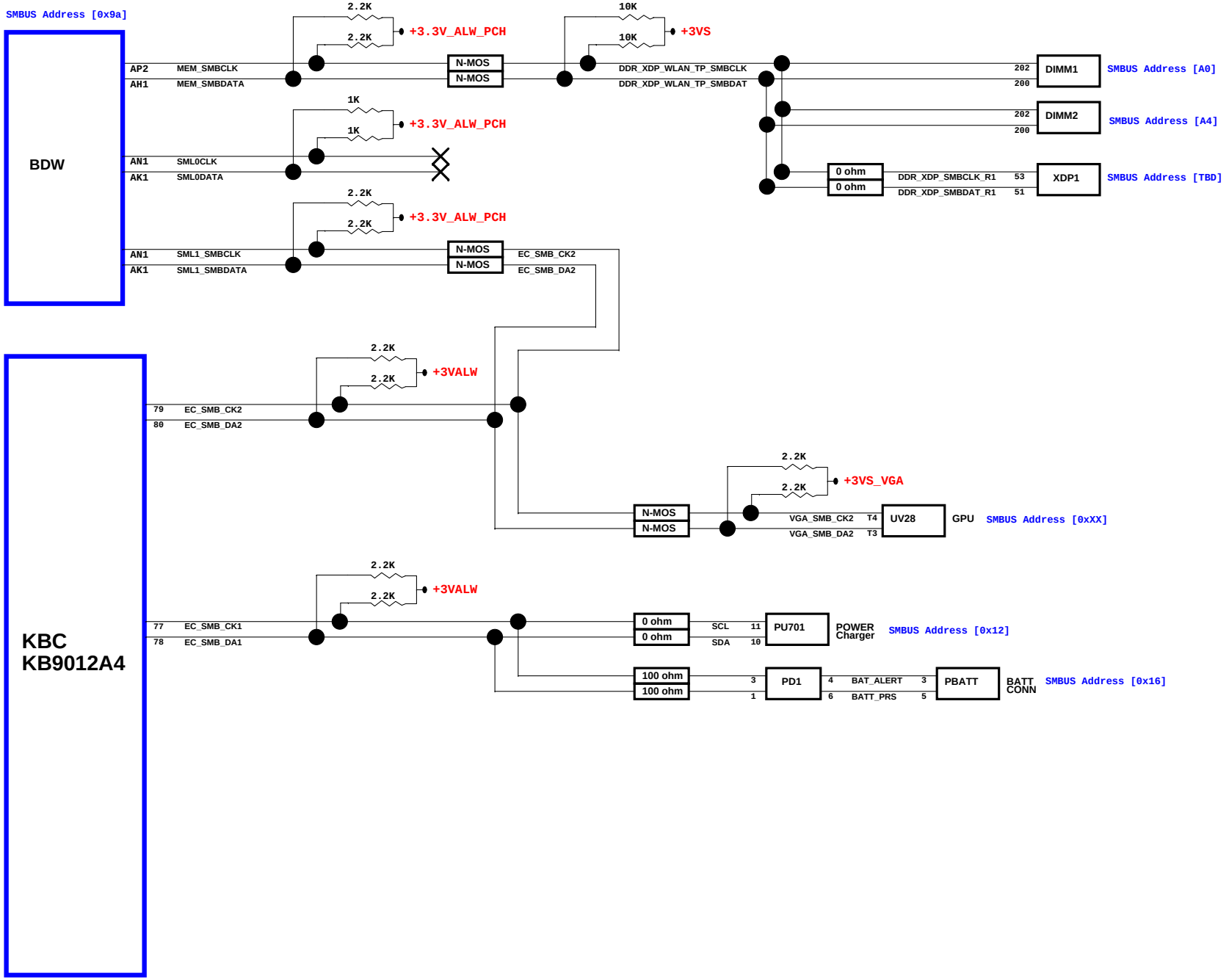
ULT	USB3.0	
	Port1	USB connector 1
	Port2	USB connector 2
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 1
	Port1	USB connector 2
	Port2	USB connector 3 (D/B)
	Port3	
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (AMD JET/TOBAZ)
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	
	SATA2	
	SATA3	

Compal Electronics, Inc.

Title: Notes

Size | Document Number: LA-B016P | Rev: 1.0

Date: Friday, October 24, 2014 | Sheet 4 of 56



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Compal Electronics, Inc.

Title: **SMBUS connection**

Size: C | Document Number: **LA-B016P** | Rev: 1.0

Date: Friday, October 24, 2014 | Sheet 5 of 56

i3-4020U-15W-GT2-MP

UC1 I3R1@ — CL8064701552800 QEZ5 D0 1.8G — **SA00007MG0L**

UC1 I3R3@ — CL8064701478202 SR16Q C1 1.7G A31! — **SA00006SX2L** **TBD**

i5-4210U-15W-GT2-MP

UC1 I5R1@ — CL8064701477802 QEAK D0 1.7G — **SA00007LO0L**

UC1 I5R3@ — CL8064701477702 SR170 C1 1.6G A31! — **SA00006SM3L** **TBD**

i7-4510U-15W-GT2-MP

UC1 I7R1@ — CL8064701477301 QEAF D0 2G BGA — **SA00007M70L**

UC1 I7R3@ — CL8064701477202 SR16Z C1 1.8G A31! — **SA00006SL2L** **TBD**

Broadwell

UC1 QFSY@ — CL8064701614813 QFSY C0 1.6G — **SA00007AM0L**

UC1 QG21@ — CL8065801674128 QG21 C0 1.2G — **SA00007OS0L**

UC1 QG22@ — CL8065801675027 QG22 C0 1.2G — **SA00007OT0L**

UC1A HASWELL_MCP_E

DDI1_LANE_N0 C54 DDI1_TXN0
DDI1_LANE_P0 C55 DDI1_TXP0
DDI1_LANE_N1 B58 DDI1_TXN1
DDI1_LANE_P1 C58 DDI1_TXP1
DDI1_LANE_N2 B55 DDI1_TXN2
DDI1_LANE_P2 A55 DDI1_TXP2
DDI1_LANE_N3 A57 DDI1_TXN3
DDI1_LANE_P3 B57 DDI1_TXP3

CS1 DDI2_TXN0
CS2 DDI2_TXP0
C52 DDI2_TXN1
B52 DDI2_TXP1
C49 DDI2_TXN2
B51 DDI2_TXP2
A52 DDI2_TXN3
B53 DDI2_TXP3

DDI — EDP — 1 OF 19 — Rev1p2

EDP_TXN0 C45 EDP_TX0# <31>
EDP_TXP0 B46 EDP_TX0 <31>
EDP_TXN1 A47 EDP_TX1# <31>
EDP_TXP1 B47 EDP_TX1 <31>
EDP_TXN2 C47
EDP_TXP2 C46
EDP_TXN3 X
EDP_TXP3 B49

EDP_AUXN A45 EDP_AUX# <31>
EDP_AUXP B45 EDP_AUX <31>
EDP_RCOMP D20 EDP_COMP
EDP_DISP_UTIL A43 EDP_DISP_UTIL — 1 — 2 — EDP_BIA_PWM <10,31>
@ RC72 0_0402_5%

COMPENSATION PU FOR eDP

+VCCIOA_OUT — 2 — 1 — RC71 24.9_0402_1%-D

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

+1.05VS_PCH — 1 — @RC58 49.9_0402_1% 2 — H_CATERR# — 1 — RC60 62_0402_5% 2 — H_PROCHOT#

SYS_RESET# — SYS_RESET# <10>

SYS_RESET# — 2 — RC362 1K_0402_1% — 1 — +3VS

1 — CC17 0.1U_0402_10V7K 2

H_CPUPWRGD — 1 — RC66 10K_0402_5% — 2

1 — CC27 100P_0402_50V8J @EMI@ — 2

ESD solution

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

DDR3 COMPENSATION SIGNALS

200_0402_1% 2 — 1 RC68 — SM_RCOMP0
120_0402_1% 2 — 1 RC69 — SM_RCOMP1
100_0402_1% 2 — 1 RC70 — SM_RCOMP2

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

UC1B HASWELL_MCP_E

<30> PECI_EC — H_CATERR# D61 — PECI_EC N62

<30,34> H_PROCHOT# — 1 — RC67 — 2 — H_PROCHOT#_R K63 — 56_0402_5%

H_CPUPWRGD C61

H_PROCHOT# — 1 — @EMI@ CC42 — 2 — 22P_0402_50V8J

SM_RCOMP0 AU60
SM_RCOMP1 AV60
SM_RCOMP2 AU61
AV15
AV61

<17> DDR3_DRAMRST#_CPU
<17> DDR_PG_CTRL

PROC_DETECT — CATERR — PECI — MISC — JTAG — PROCHOT — THERMAL — PROCPWRGD — PWR — SM_RCOMP0 — SM_RCOMP1 — SM_RCOMP2 — SM_DRAMRST — SM_PG_CNTL1 — DDR3

2 OF 19 — Rev1p2

PRDY J62
PREQ J62
PROC_TCK E60 XDP_TCK
PROC_TMS E61 XDP_TMS @ T123
PROC_TRST E59 XDP_TRST#
PROC_TDI F63 XDP_TDI @ T122
PROC_TDO F62 XDP_TDO

1 — R3 — 2 — 0_0402_5% — PCH_JTAG_RST# — PCH_JTAG_RST# <8>

BPM#0 J60 XDP_OBS0_R — RC141 1 — @ — 2 0_0402_1%
BPM#1 H60 XDP_OBS1_R
BPM#2 H61 @ T111
BPM#3 H62 @ T112
BPM#4 K59 @ T113
BPM#5 H63 @ T114
BPM#6 K60 @ T115
BPM#7 J61 @ T116

+1.05VS_PCH

XDP_TDO 1 — 8
XDP_TCK 2 — 7
XDP_TRST# 3 — 6
4 — 5
RP45 51_8P4R_5%

PU/PD for JTAG signals

DDR3_DRAMRST#_CPU — CC35 @ESD@ — 1 — 0.047U_0402_16V4Z — 2

Place CC35 on BOT

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

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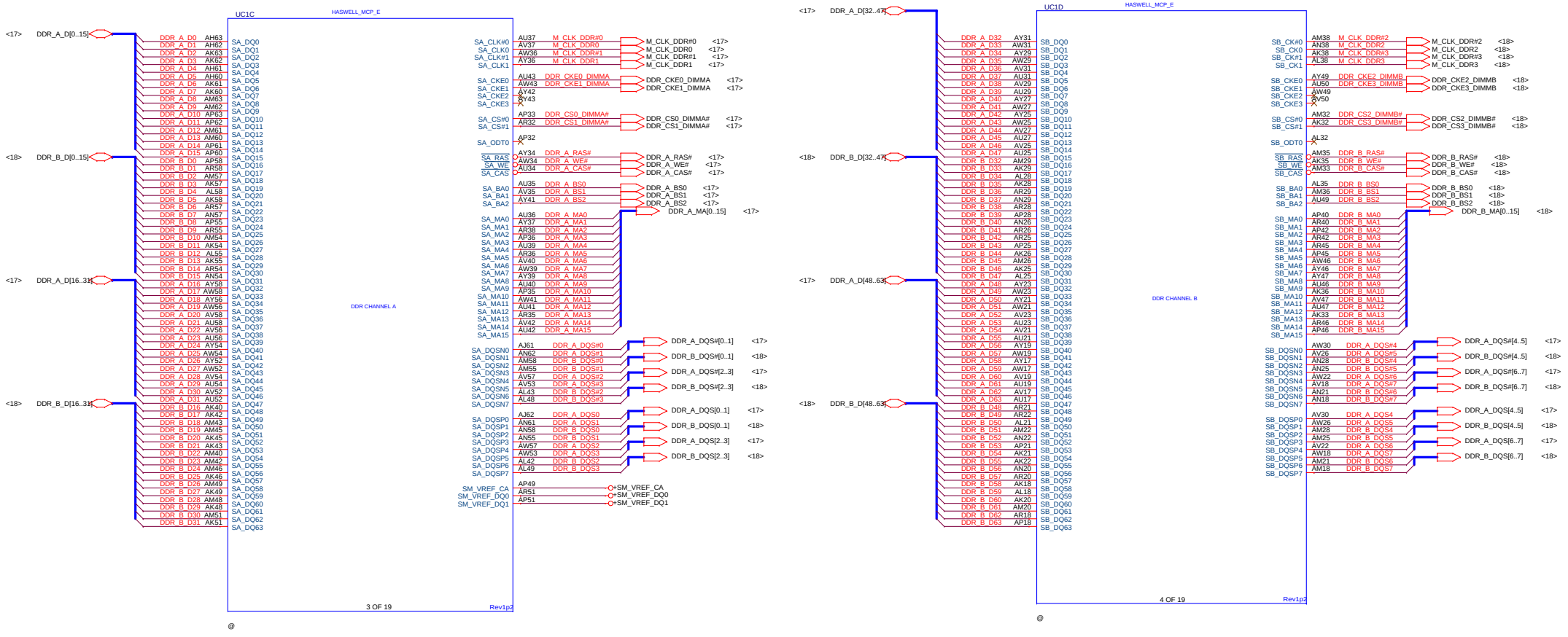
Compal Electronics, Inc.

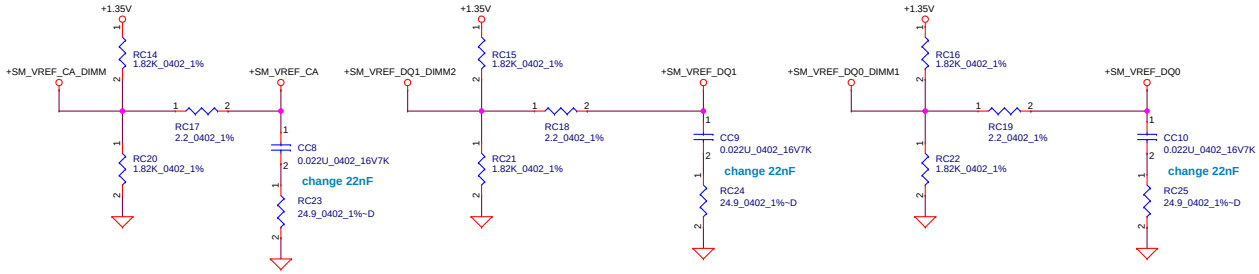
Title: MCP(1,2/19) eDP,XDP,MISC

Size: — Document Number: LA-B016P — Rev: 0.1

Date: Monday, October 20, 2014 — Sheet 6 of 56

Interleaved Memory





confirm by intel request PDG P141

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **MCP(3,4/19) DDR3**

Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 7 of 56

RTC Battery

+RTCBATT
+CHGRTC
RC10 1K_0402_5%
W=20mils
W=20mils
DC1 BAT54CW_SOT323-3
+RTCVCC
W=20mils
CC26 1U_0603_10V6K

+RTCVCC
JP14 JUMP_43X39
+CHGRTC
JP12 JUMP_43X39
+3VLP

For GCLK

<19> PCH_RTCX1 PCH_RTCX1

+RTCVCC
RC1 330K_0402_1%
PCH_INTVRMEN
RC2 330K_0402_1%

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3VS
@RC3 PCH_AZ_SDOUT 1K_0402_5%

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CC1 XTAL@ 15P_0402_50V8J
XTAL@ YC1 32.768KHZ_12.5PF_Q13FC1350000
XTAL@ RC4 10M_0402_5%
CC2 XTAL@ 15P_0402_50V8J
PCH_RTCX1
PCH_RTCX2
PCH_INTVRMEN
SRTCRST#
PCH_RTCRST#
+RTCVCC
RC7 1M_0402_5%
RC5 20K_0402_5%
RC6 20K_0402_5%
CC3 1U_0402_6.3V6K
@ CMOS1 SHORT PADS~D
CC4 1U_0402_6.3V6K

UC1E HASWELL_MCP_E

RTCX1 RTCX2 INTRUDER INTVRMEN SRTCRST RTCRST — RTC

HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_RST/I2S_MCLK
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_DOCK_EN/I2S1_TXD
HDA_DOCK_RST/I2S1_SFRM
I2S1_SCLK
— AUDIO

PCH_AZ_BITCLK
PCH_AZ_SYNC
PCH_AZ_RST#
PCH_AZ_CODEC_SDIN0
<22> PCH_AZ_CODEC_SDIN0
<30> ME_EN
RC8 1K_0402_5%
PCH_AZ_SDOUT

PCH_TRST PCH_TCK PCH_TDI PCH_TDO PCH_TMS RSVD RSVD JTAGX RSVD — JTAG

SATA_RN0/PERN6_L3 SATA_RP0/PERP6_L3 SATA_TN0/PETN6_L3 SATA_TP0/PETP6_L3
SATA_RN1/PERN6_L2 SATA_RP1/PERP6_L2 SATA_TN1/PETN6_L2 SATA_TP1/PETP6_L2
SATA_RN2/PERN6_L1 SATA_RP2/PERP6_L1 SATA_TN2/PETN6_L1 SATA_TP2/PETP6_L1
SATA_RN3/PERN6_L0 SATA_RP3/PERP6_L0 SATA_TN3/PETN6_L0 SATA_TP3/PETP6_L0
— SATA

SATA_PRX_DTX_N0_C <32>
SATA_PRX_DTX_P0_C <32>
SATA_PTX_DRX_N0_C <32>
SATA_PTX_DRX_P0_C <32>
SATA HDD

SATA0GP/GPIO34 SATA1GP/GPIO35 SATA2GP/GPIO36 SATA3GP/GPIO37
SATA_IREF RSVD RSVD SATA_RCOMP SATALED

5 OF 19 Rev1p2

PCH Rx side need use strap pin to update PCIE +/-

+3VS
RC107 10K_0402_5%
EC_SMI# <30>
ODD_DETECT#
+1.05VS_ASATA3PLL
SATA_IREF RC126 1 @ 2 0_0603_1%
SATA_RCOMP RC131 1 2 3.01K_0402_1%
SATA_ACT# <25>
within 500 mils

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5

CMOS place near DIMM

RTC discharge by EC

SRTCRST#
PCH_RTCRST#
@ DMN66D0LDW-7_SOT363-6 QC2B
@ DMN66D0LDW-7_SOT363-6 QC2A
<30> RTC_DIS
@ RC368 100K_0402_5%

<6> PCH_JTAG_RST#
T175
PCH_JTAG_RST# PCH_TCK PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TMS

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec

<22> PCH_AZ_CODEC_SDOUT EMI@ R2356 1 2 33_0402_5% PCH_AZ_SDOUT
<22> PCH_AZ_CODEC_SYNC EMI@ R2357 1 2 33_0402_5% PCH_AZ_SYNC
<22> PCH_AZ_CODEC_RST# EMI@ R2358 1 2 33_0402_5% PCH_AZ_RST#
<22> PCH_AZ_CODEC_BITCLK EMI@ R2359 1 2 33_0402_5% PCH_AZ_BITCLK
1 @EMI@ CC5 27P_0402_50V8J 2

EMI depop location

+3VS
ODD_DETECT# PCH_GPIO35 PCH_GPIO37
RP37 10K_8P4R_5%

+1.05VS_PCH
PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TMS
RP48 51_8P4R_5%

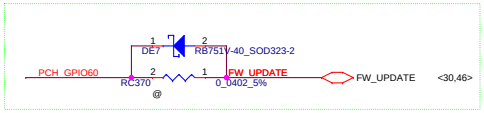
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

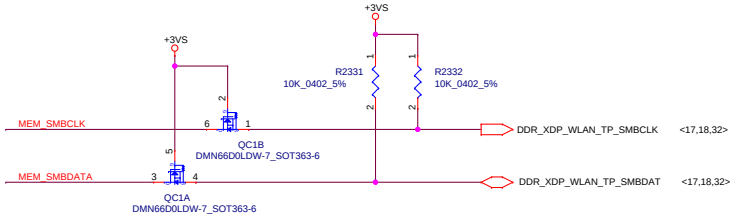
Title: MCP(5/19) RTC,SATA,HDA,JTAG

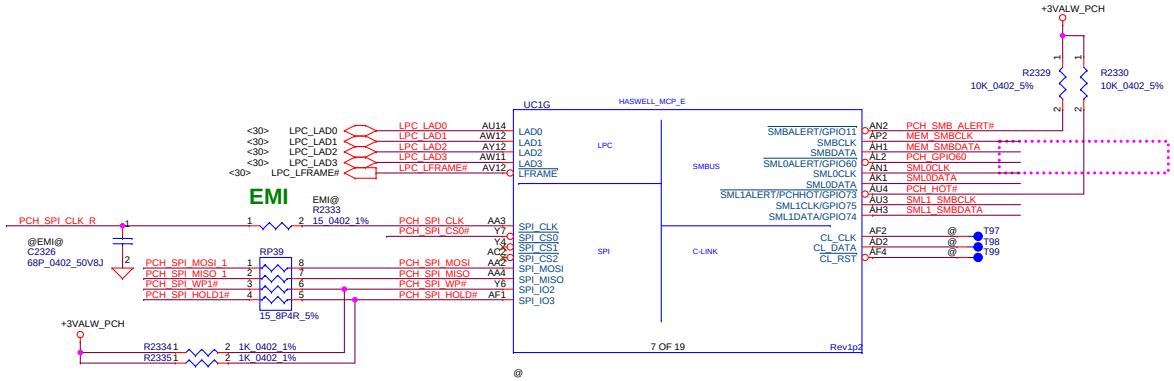
Size: A3 | Document Number: LA-B016P | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 8 of 56

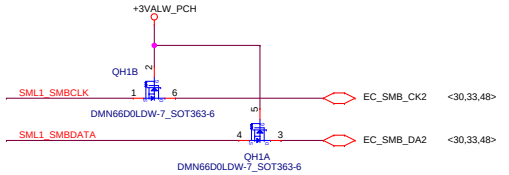


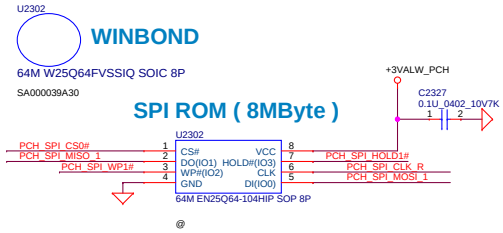
MEM Bus : DDR/XDP/WLAN/TP

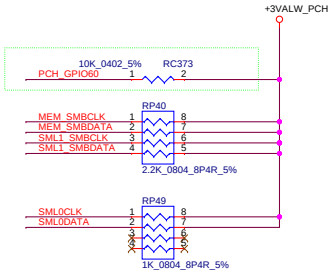




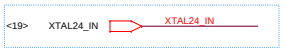
SML1 Bus : EC/Sensors

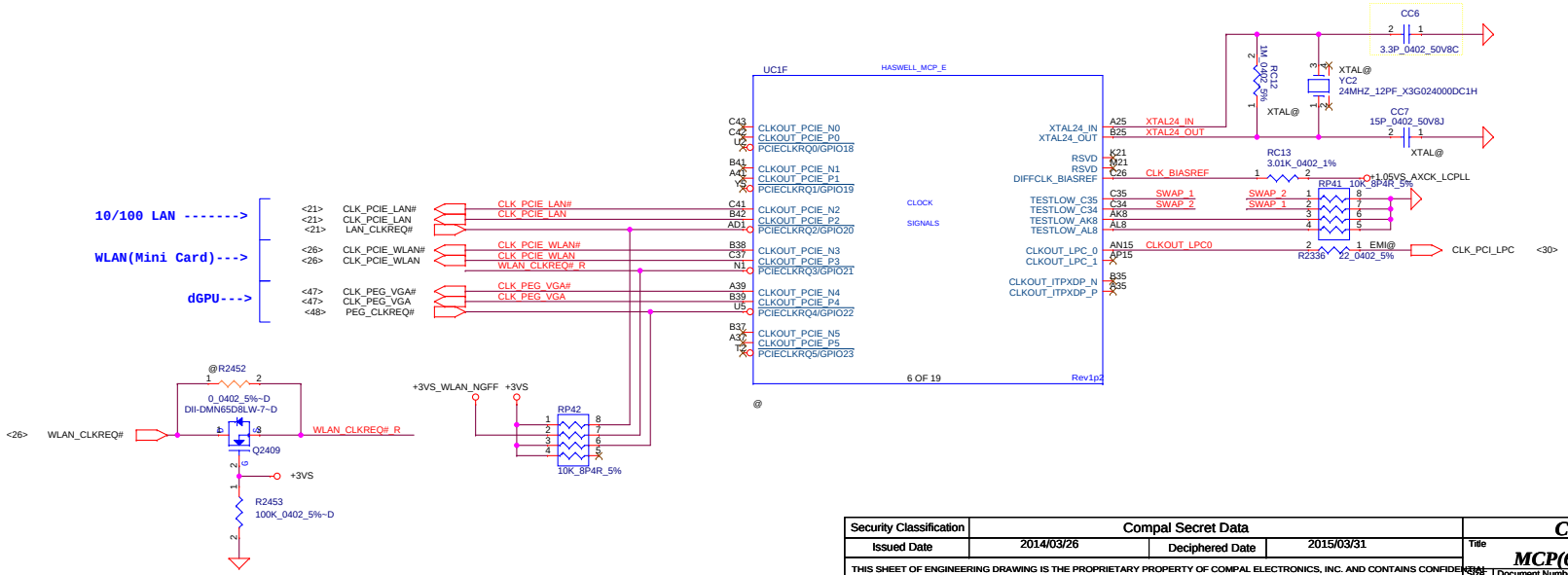






For GCLK





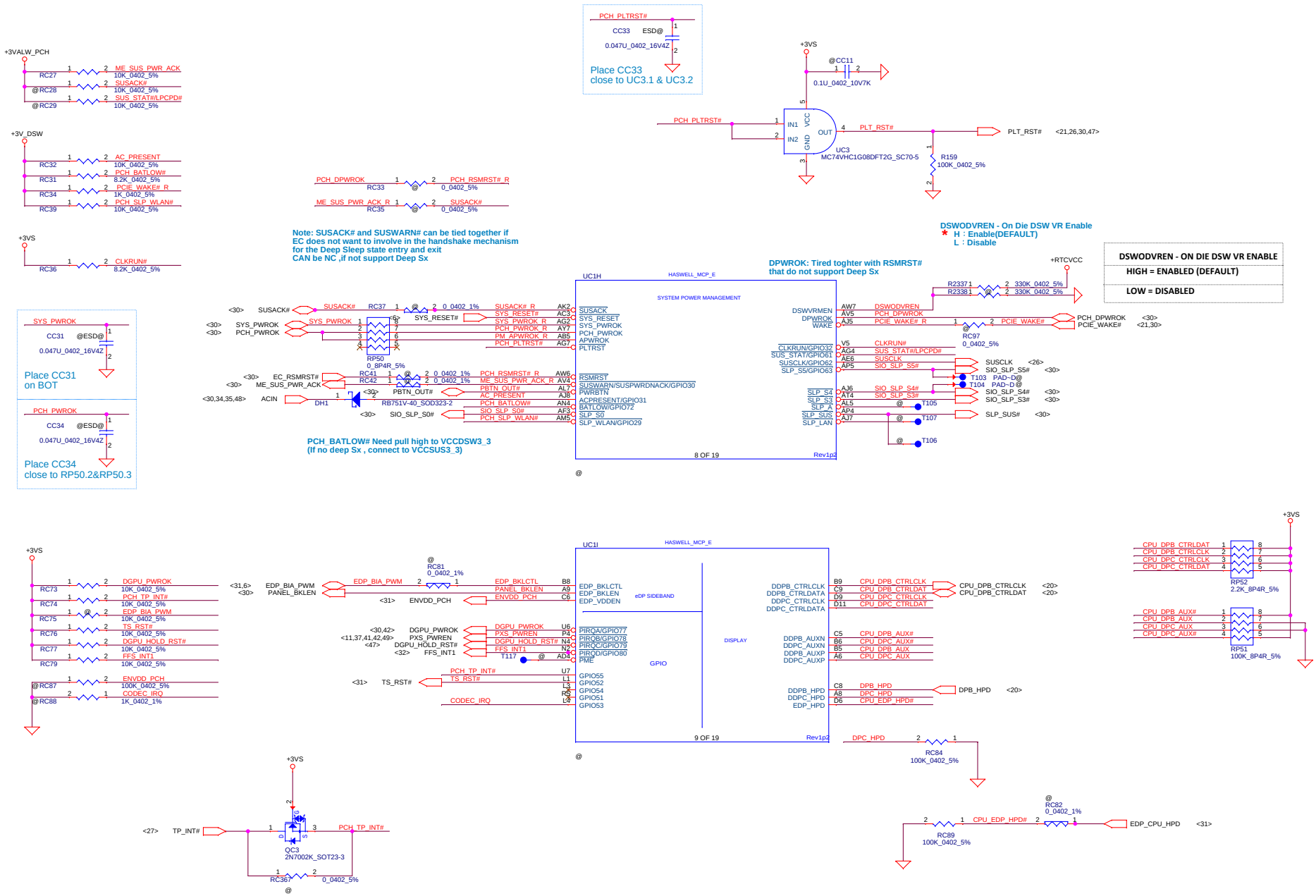
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **MCP(6,7/19) CLK,SMB,SPI,LPC**

Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 9 of 56



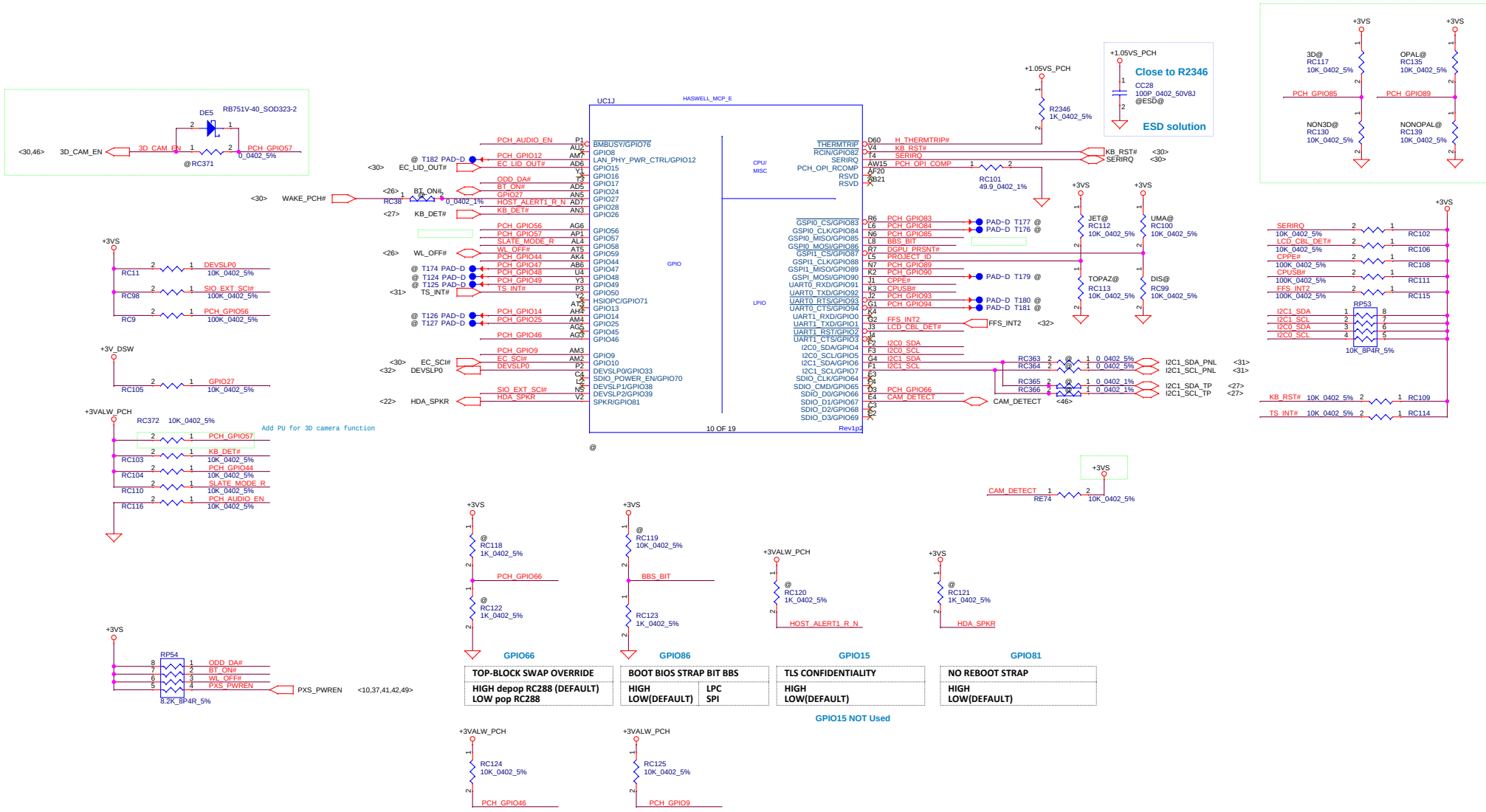
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: MCP(8,9/19) DDI,EDP,GPIO

Size: A3 | Document Number: LA-B016P | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 10 of 56



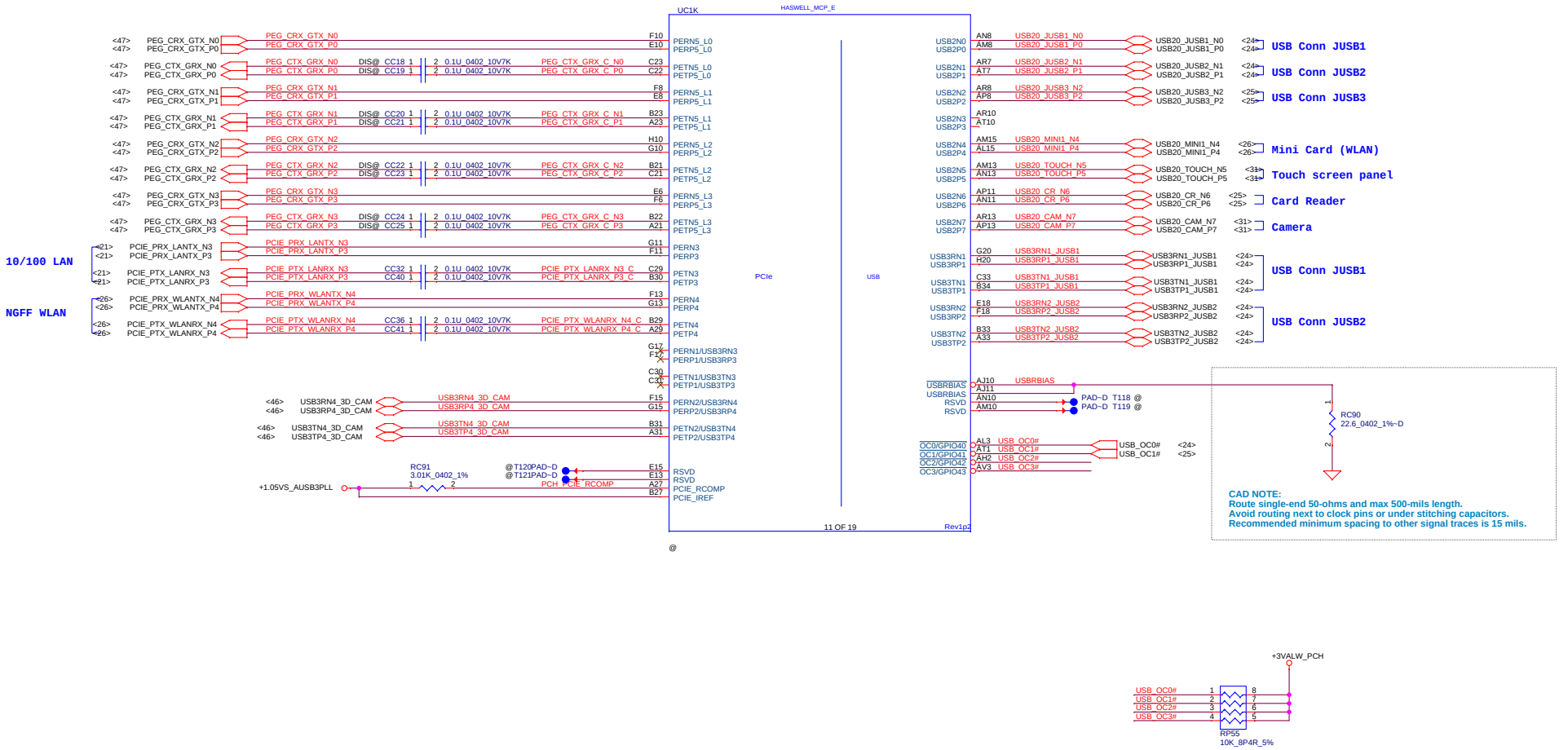
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **MCP(10/19) GPIO,LPIO,MISC**

Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 11 of 56



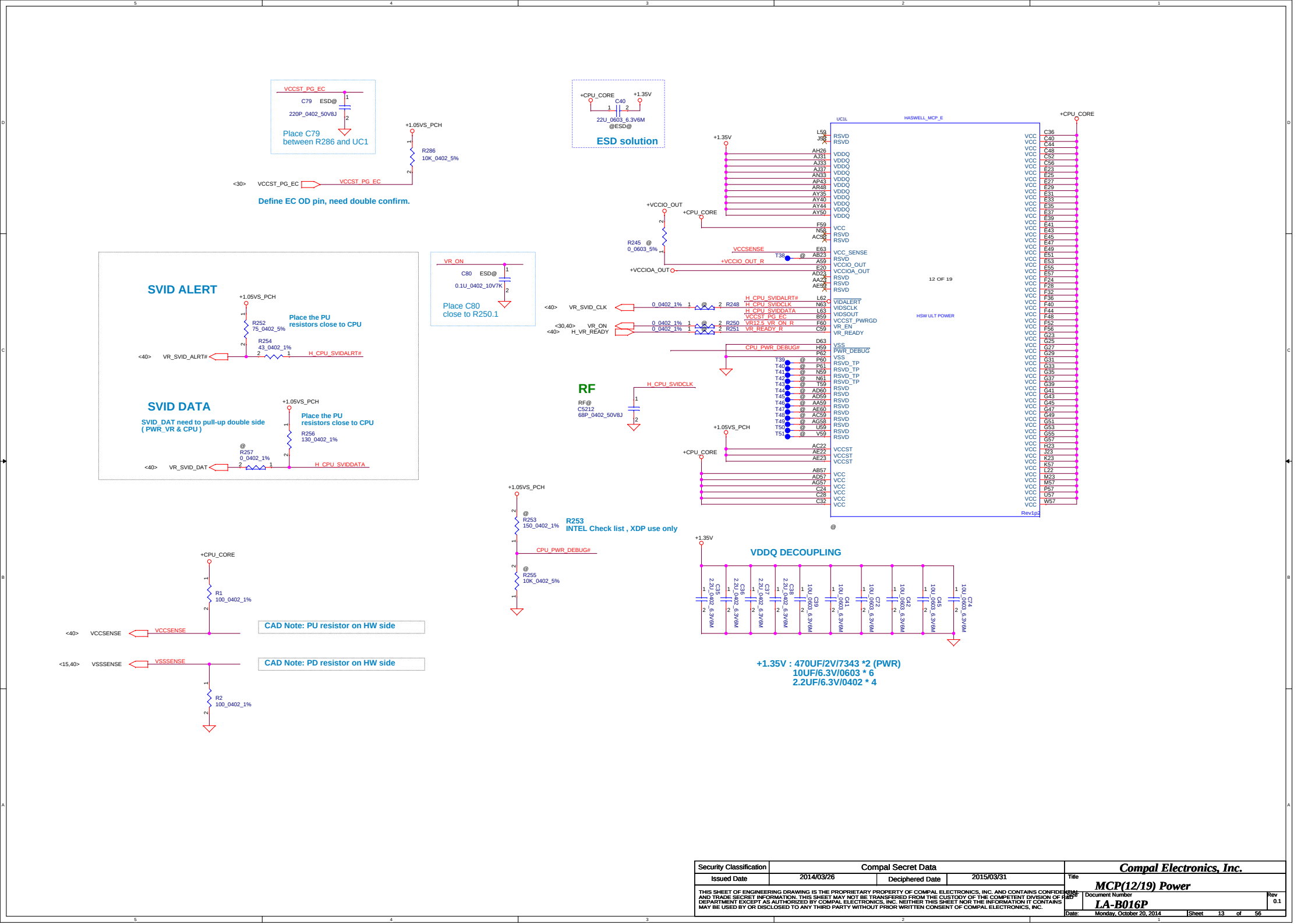
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **MCP(11/19) PCIE,USB**

Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 12 of 56



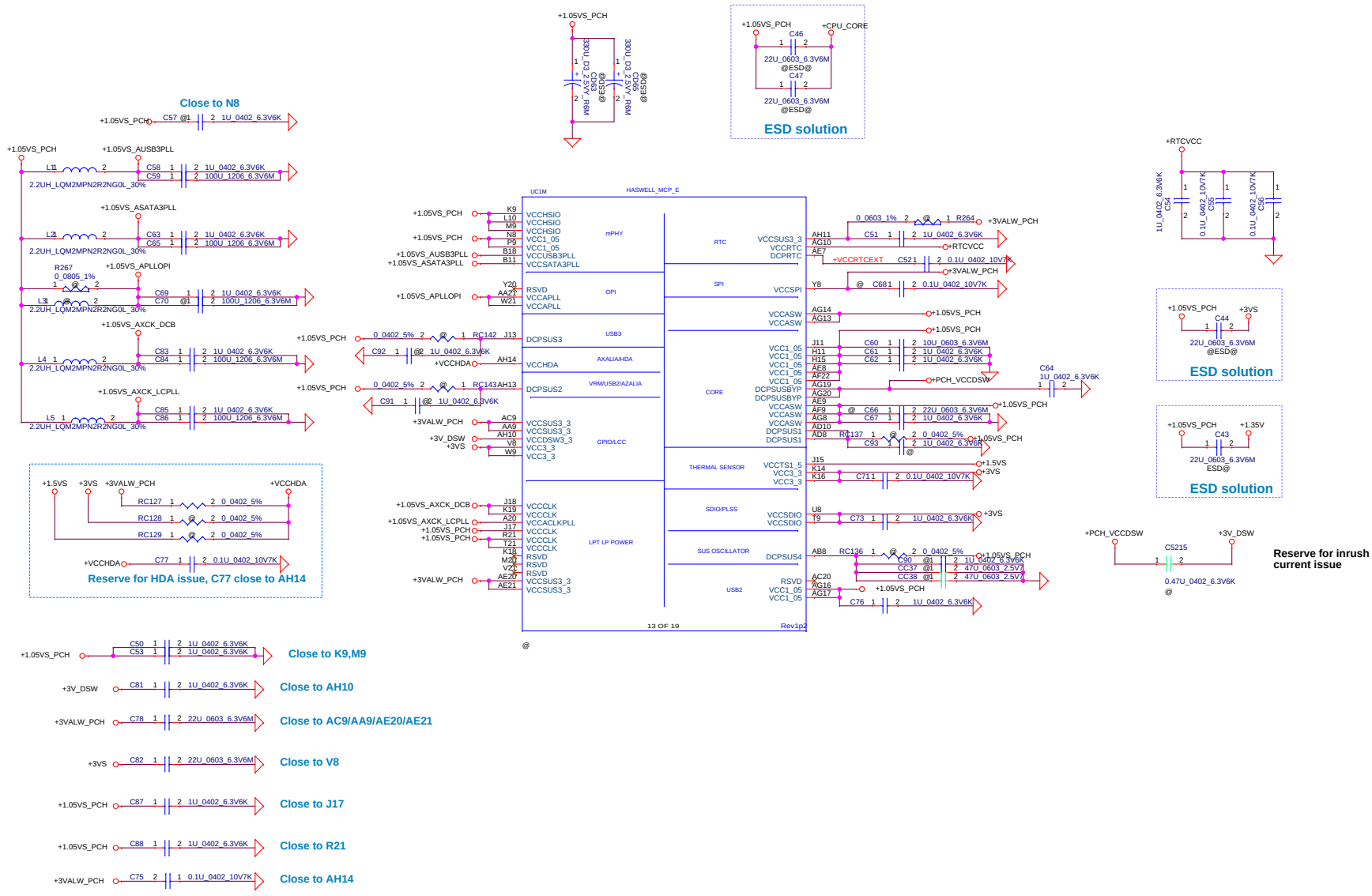
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **MCP(12/19) Power**

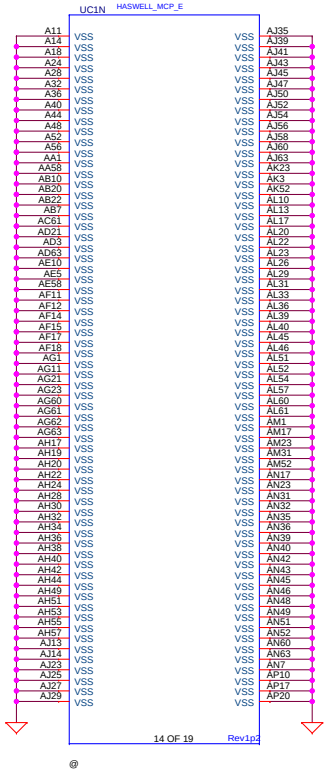
Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

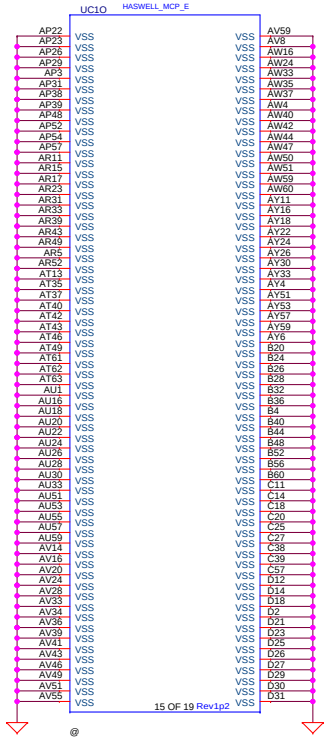
Date: Monday, October 20, 2014 | Sheet 13 of 56

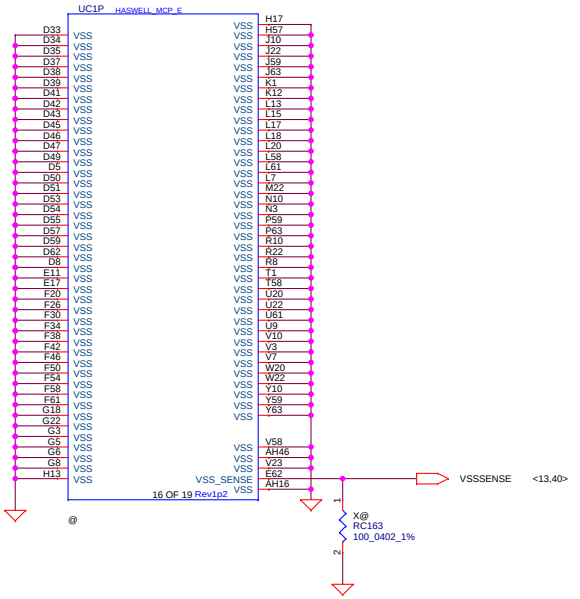


Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.			
Title: MCP(13/19) Power			
Size: A3	Document Number: LA-B016P		Rev: 0.1
Date: Monday, October 20, 2014	Sheet 14 of 56		







CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

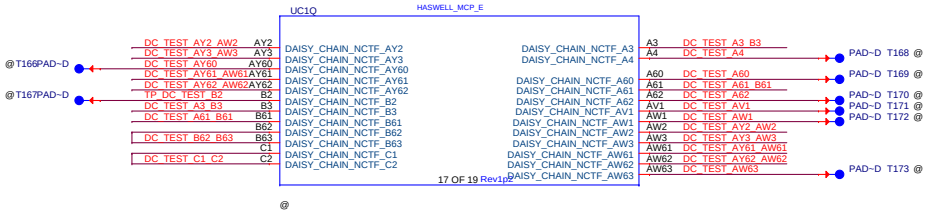
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

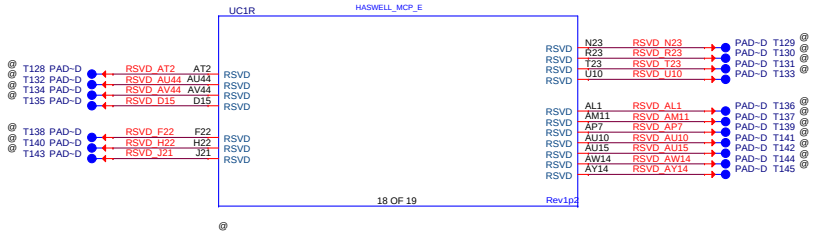
Compal Electronics, Inc.

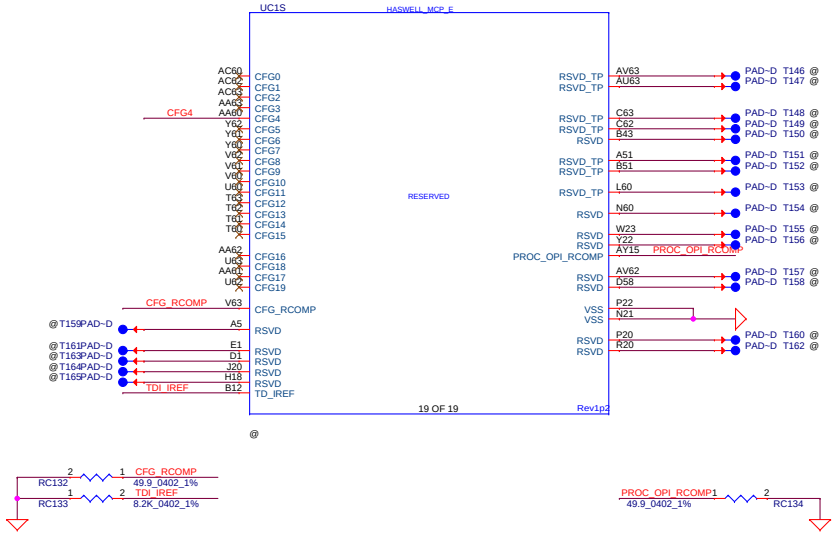
Title: **MCP(14,15,16/19) VSS**

Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

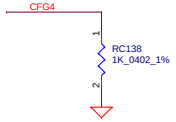
Date: Monday, October 20, 2014 | Sheet 15 of 56







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size: A3 | Document Number: LA-B016P | Rev: 0.1

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H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

ESD solution

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: DDRIII DIMMA

Document Number: LA-B016P

Rev: 0.1

Date: Monday, October 20, 2014 Sheet 17 of 56

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM2

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

JDIMM2
BELLW_80011-1021
CONN@

Security Classification	Compal Secret Data
Issued Date	2014/03/26
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Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: C | Document Number: LA-B016P | Rev: 0.1

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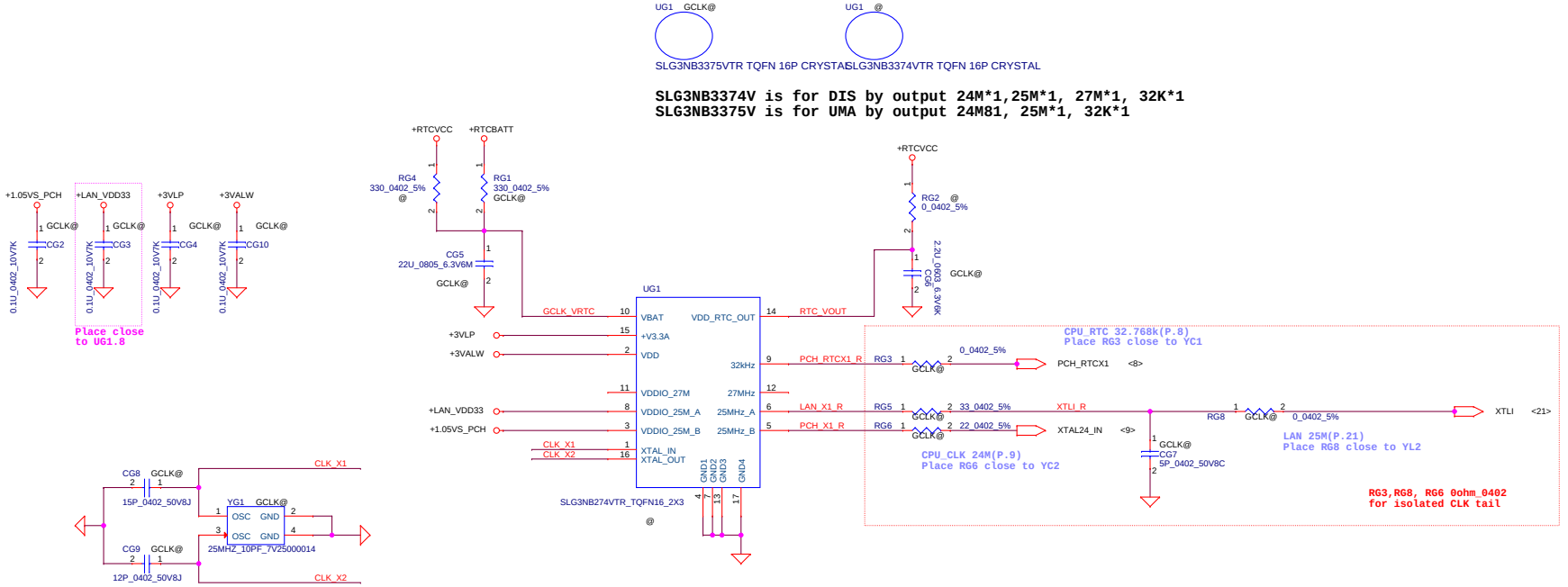
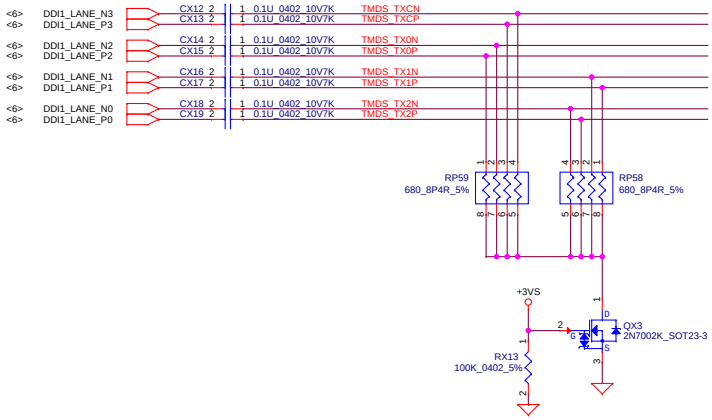
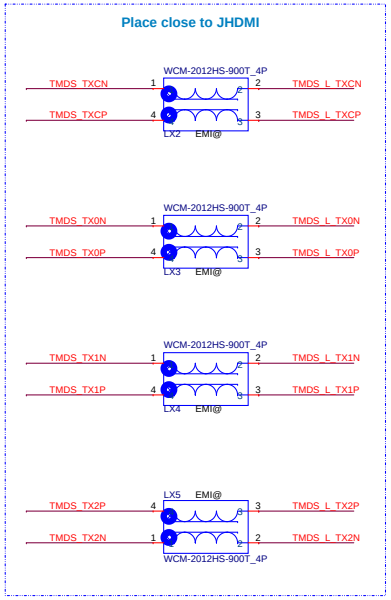
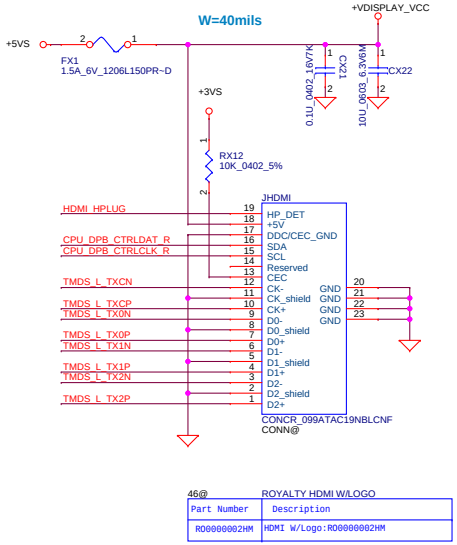


Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.			
Title: Green CLK			
Size: A3	Document Number: LA-B016P		Rev: 0.1
Date: Monday, October 20, 2014	Sheet 19 of 56		

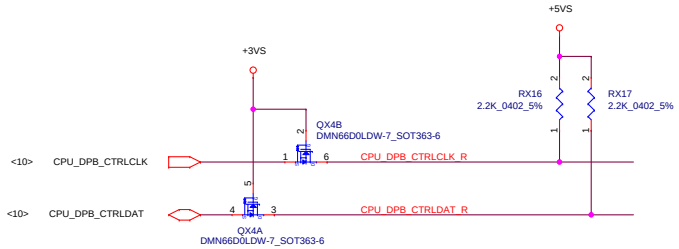


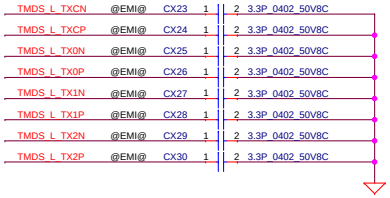


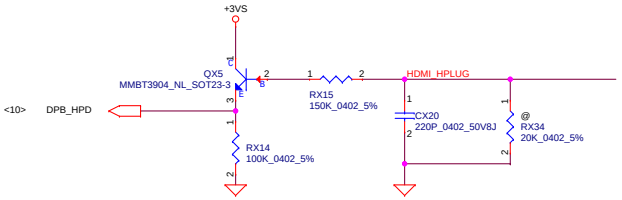


46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM







Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **HDMI**

Size: A3 | Document Number: **LA-B016P** | Rev: 0.1

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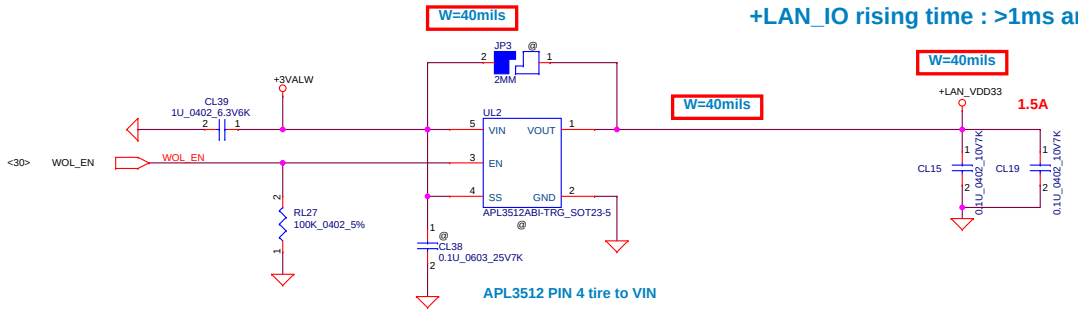

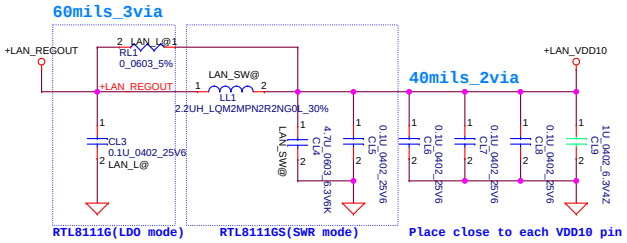

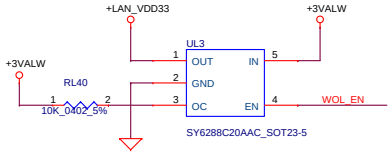

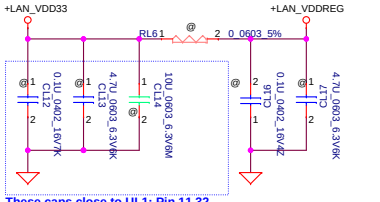

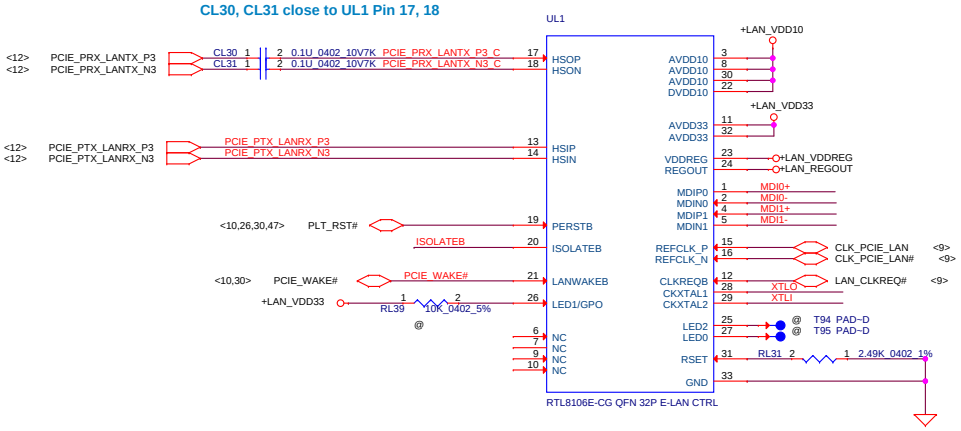

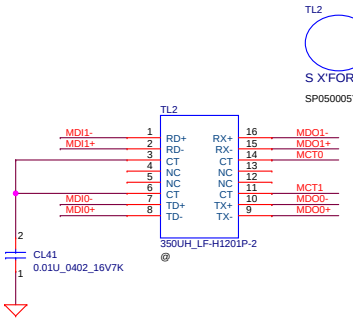

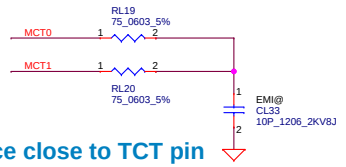

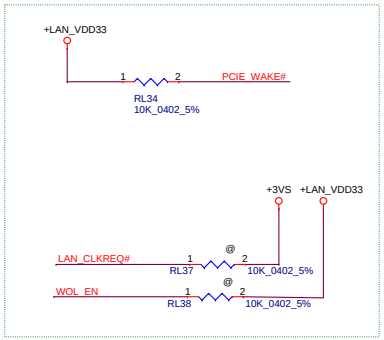

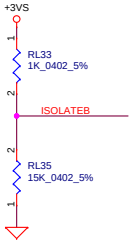

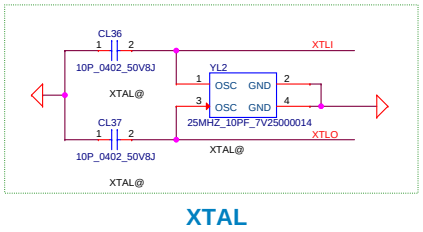

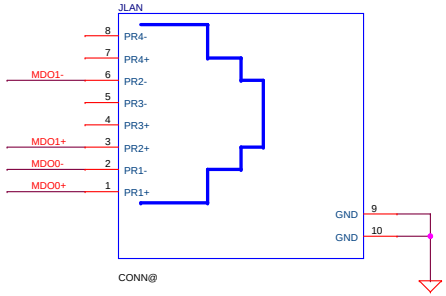

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Title: LAN RTL8106EUS

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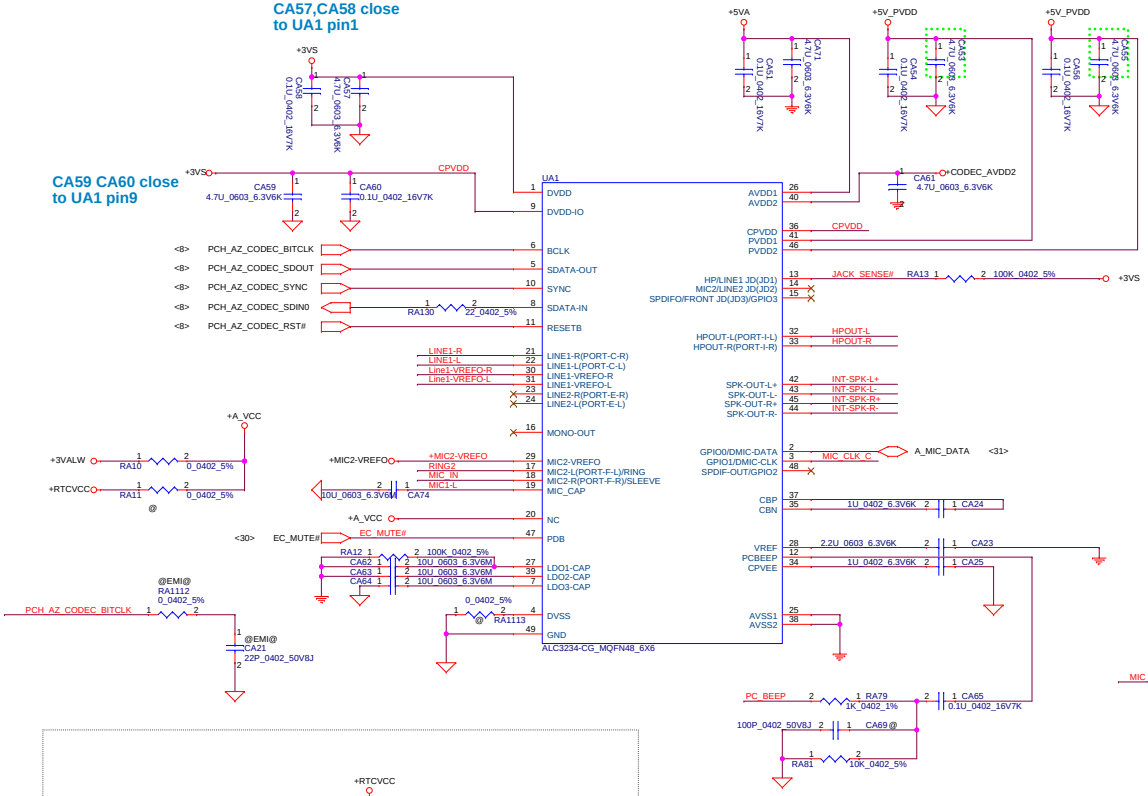
CA71, CA51 place close to Pin 26

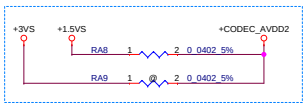
CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

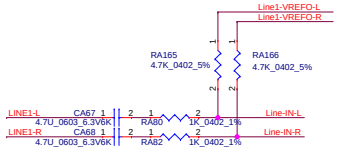
CA57,CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

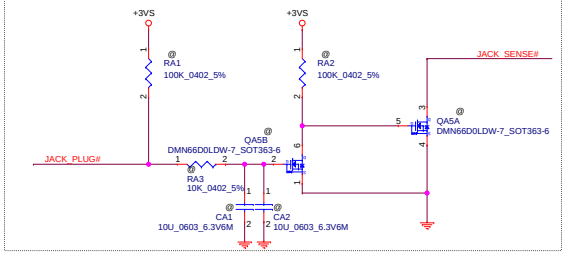


Reserve for HDA issue

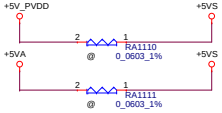


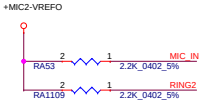


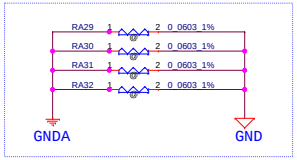
JACK_PLUG Delay circutis



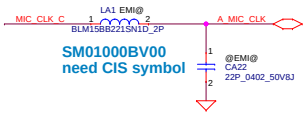
Reserve for cancel Delay circutis



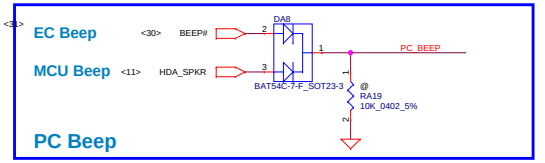


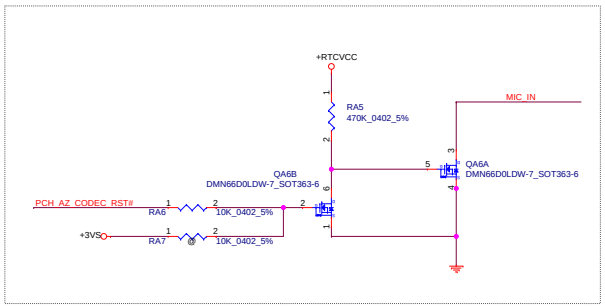


Place on the moat between GND & GNDA.



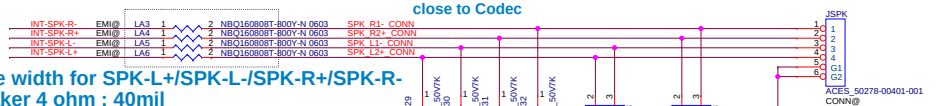
SM01000BV00 need CIS symbol





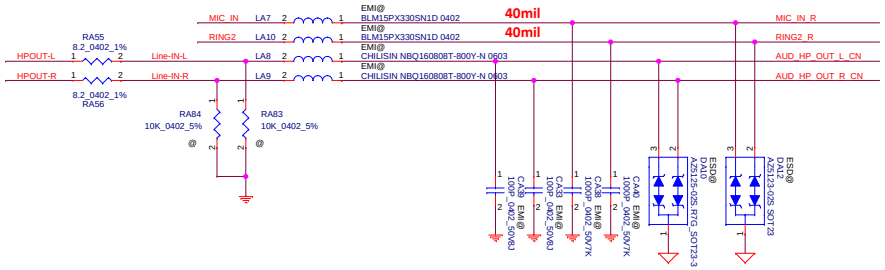
Close to UA1 Pin11,13,14,16

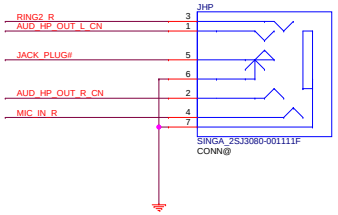
close to Codec



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack





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Issued Date	2014/03/26	Deciphered Date	2015/03/31

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Compal Electronics, Inc.

Title: Audio Codec ALC3234

Document Number: LA-B016P

Rev: 0.1

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Compal Electronics, Inc.

Title: **Reserved Page**

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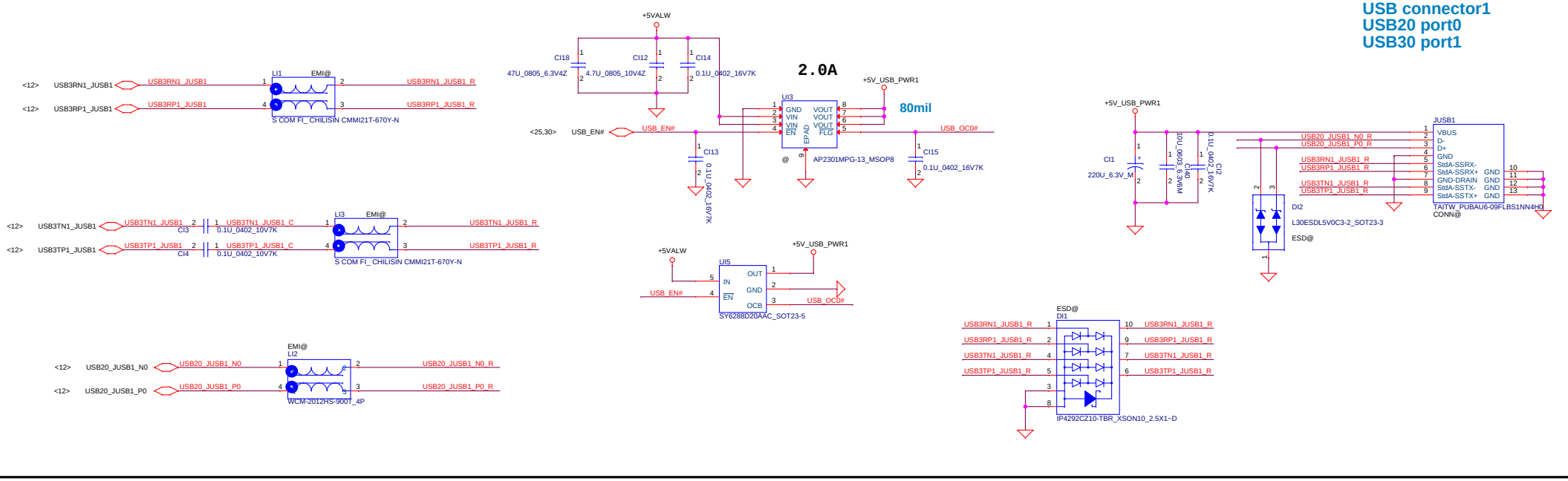

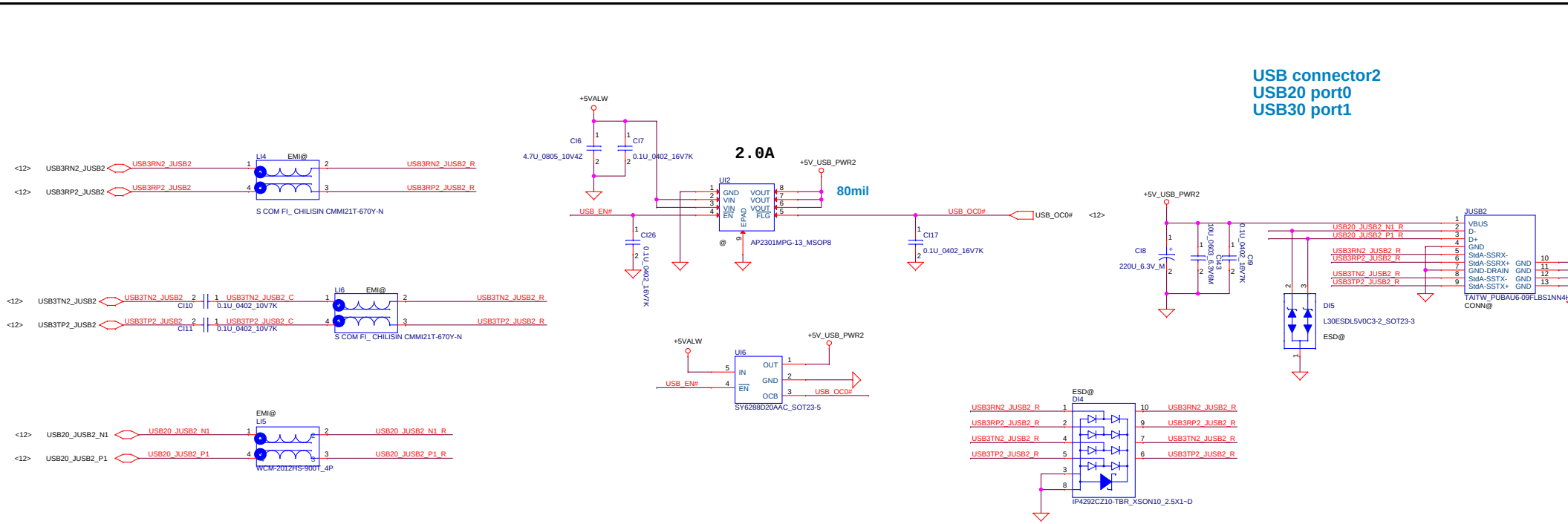

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **USB3.0**

Size: Document Number: **LA-B016P** Rev: 0.1

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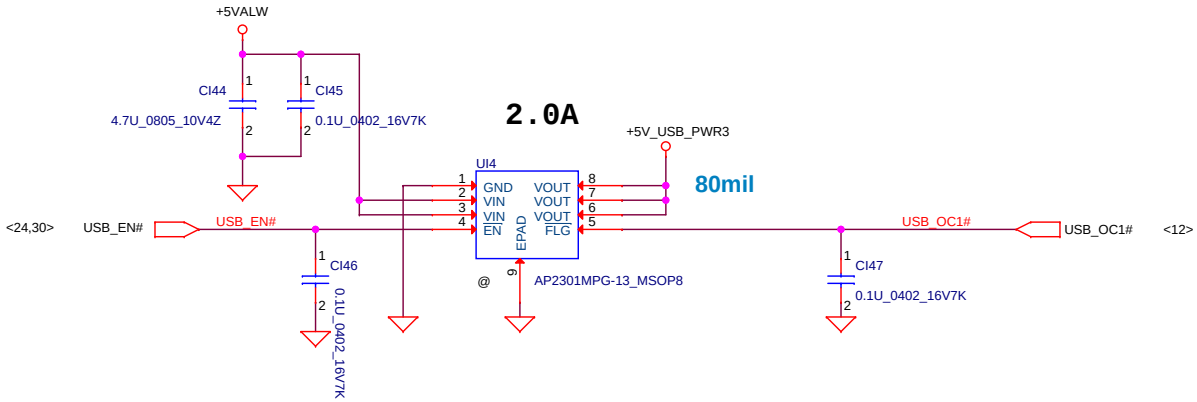
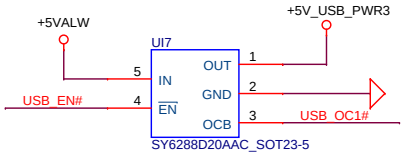
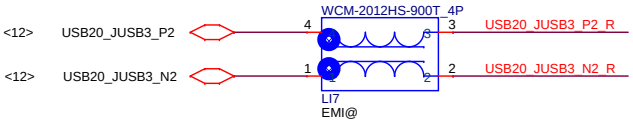
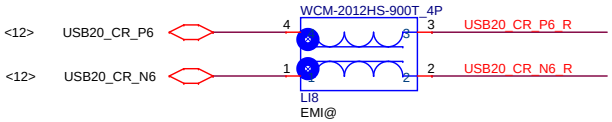
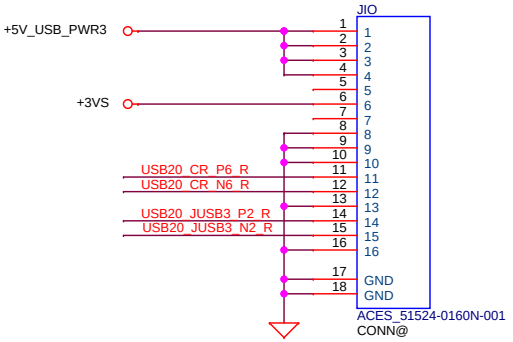




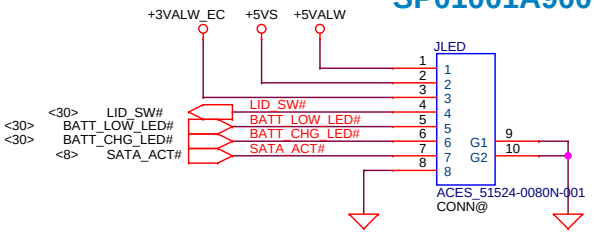




IO to MB CONN
Substitute:SP01001FS00



LED/B TO M/B
SP01001A900



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Title: *IO/B, LED/B*

Size: B | Document Number: *LA-B016P* | Rev: 0.1

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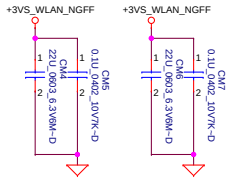
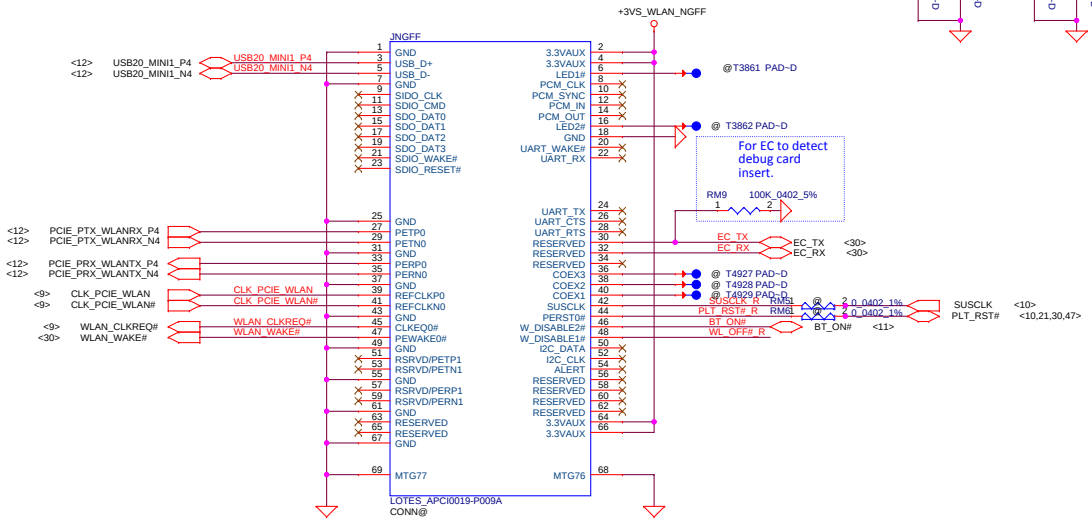
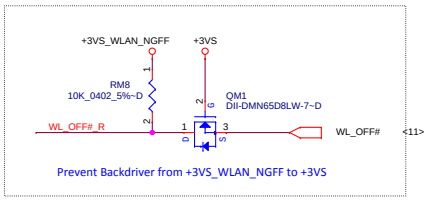
NGFF WL Con (E Key)

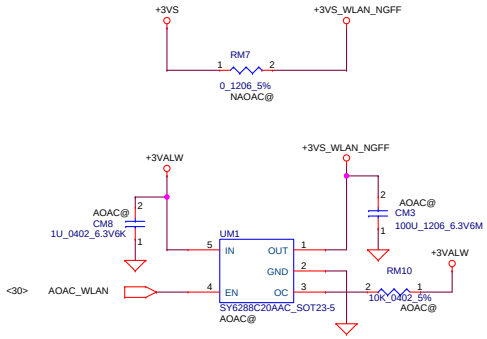
closed to pin 2, 4 closed to pin 64, 66







+3VALW TO +3VS_WLAN_NGFF



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: NGFF WLAN

Size: A3 | Document Number: LA-B016P | Rev: 0.1

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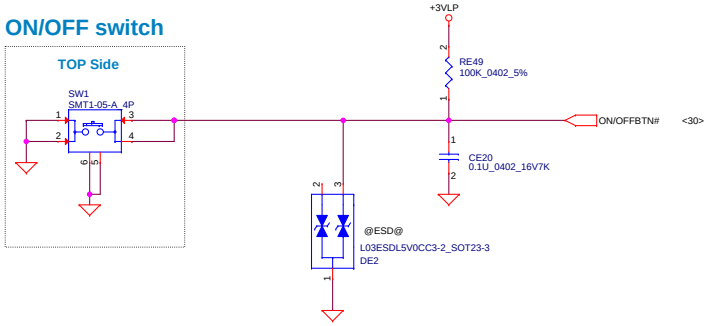
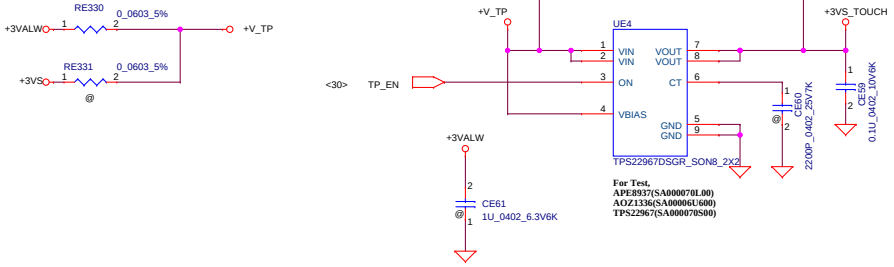
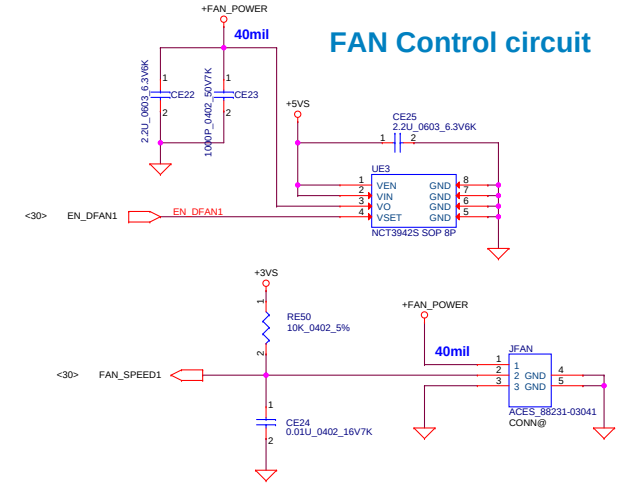
Power ON Circuit

ON/OFF switch

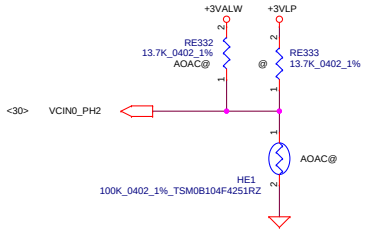




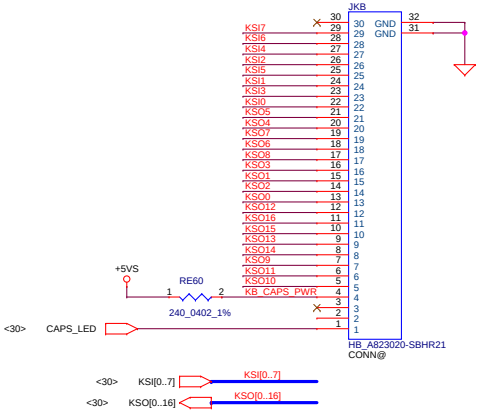
FAN Control circuit



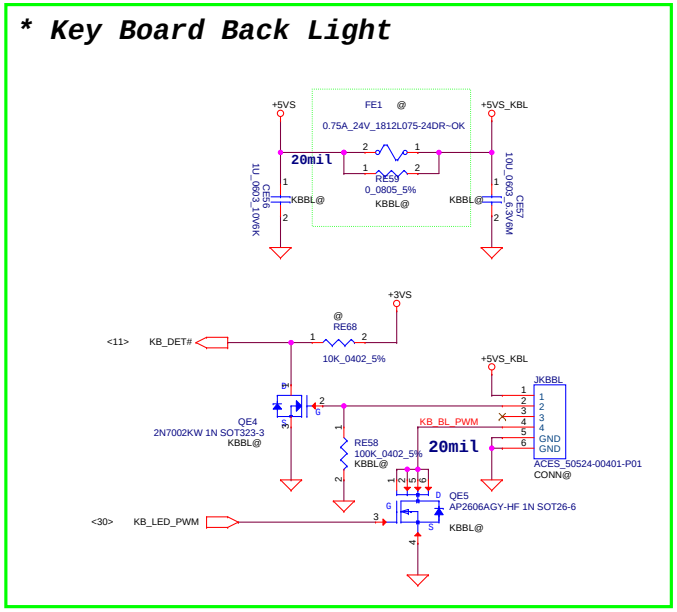
HE1 place around FAN area.



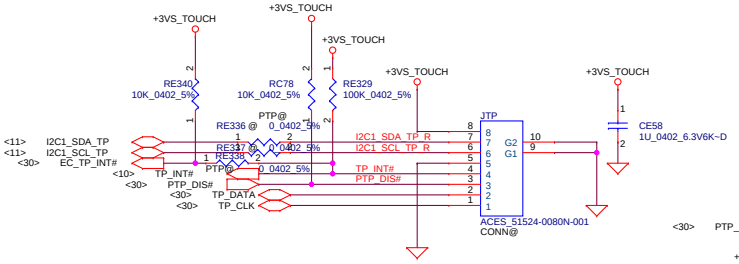
INT_KBD Connector



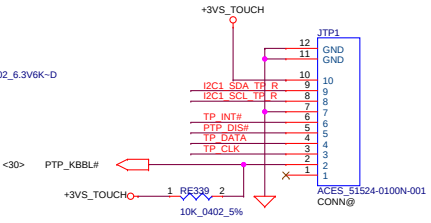
* Key Board Back Light



Touch pad



PTP



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

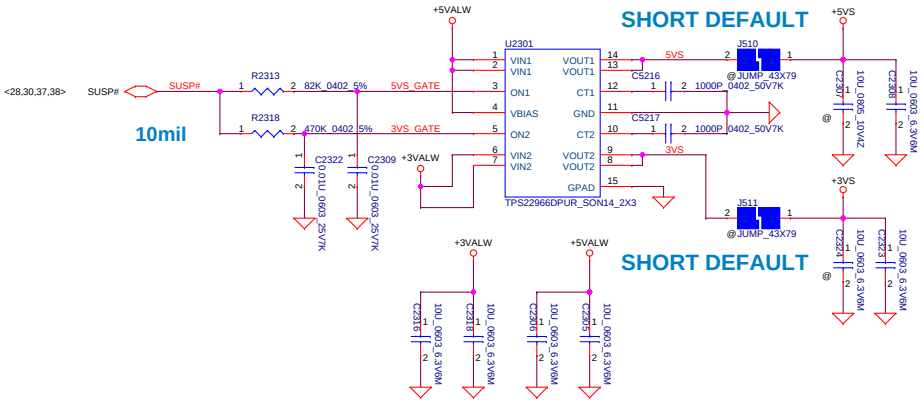
Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size: A3 | Document Number: LA-B016P | Rev: 0.1

Date: Friday, October 24, 2014 | Sheet 27 of 56

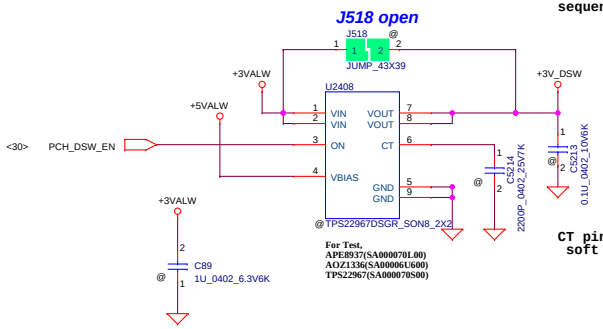
+5VS and +3VS switch



+3VALW TO +3V_DSW

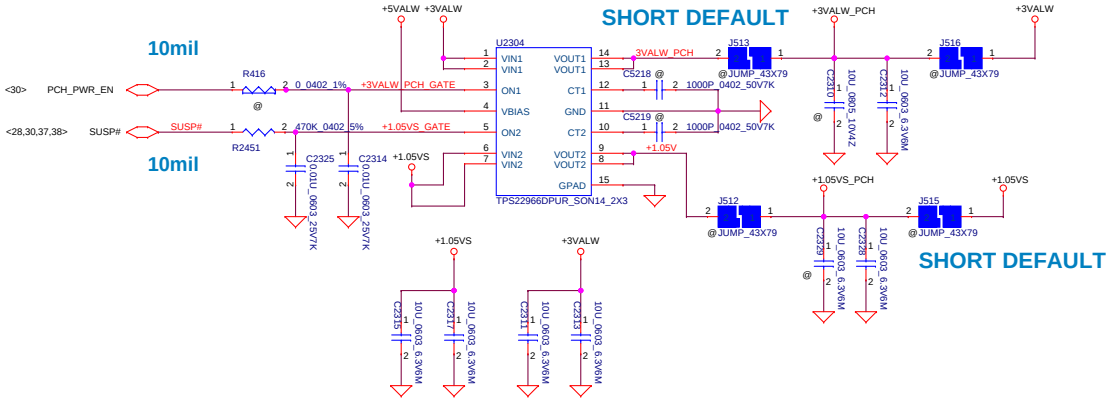
J518 open

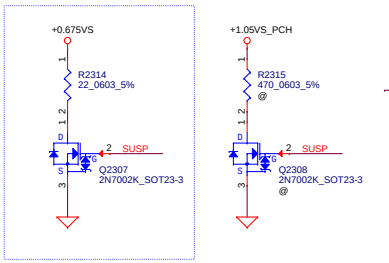
+3V_DSW have soft start sequence: +3V_DSW stable > +3VALW_PCH > 0ms

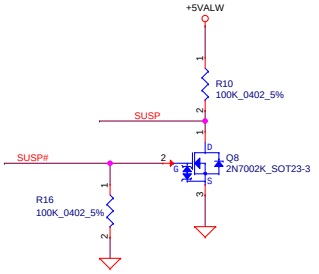


CT pin use 2200pf for soft start tuning

+3VALW_PCH switch







For Intel S3 Power Reduction

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: DC/DC Interface

Document Number: LA-B016P

Rev: 0.1

Date: Monday, October 20, 2014 Sheet 28 of 56

Screw Hole

ZZZ

PCB 13P LA-B011P REV0 M/B

DA60013U000

H1 H_2P8N @
H20 H_2P8N @
H21 H_2P8N @
H22 H_2P8X3P3N @
H23 H_2P8X4P8N @

H2 H_2P8 @
H3 H_2P8 @
H4 H_2P8 @
H5 H_2P8 @
H6 H_2P8 @
H7 H_2P8 @
H8 H_2P8 @
H9 H_2P8 @

H10 H_3P0 @

H11 H_2P8 @
H12 H_2P8 @

H13 H_3P6 @
H14 H_3P6 @
H15 H_3P6 @
H16 H_3P6 @

CPU bracket

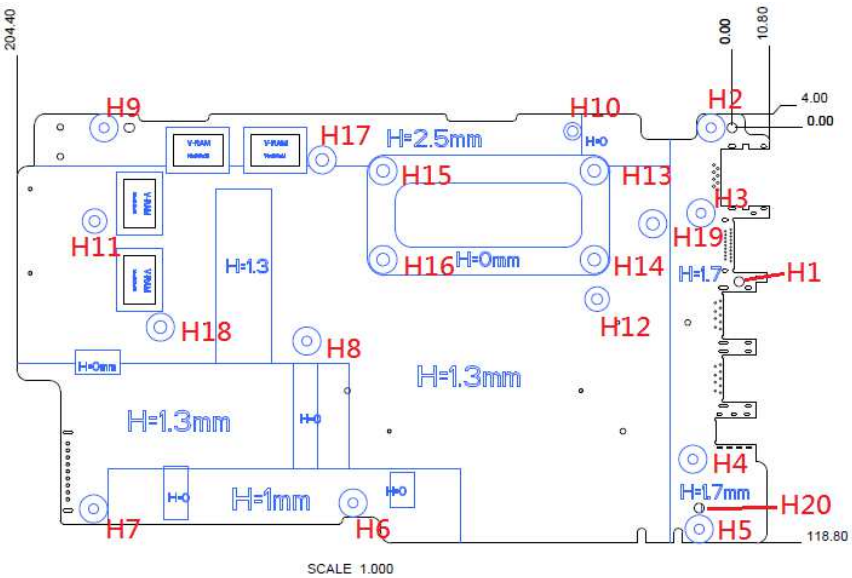
H17 H_3P3 @
H18 H_3P3 @

VGA stand-off

H19 H_3P3 @

NGFF stand-off

FD1 @FIDUCAL
FD2 @FIDUCIAL
FD3 @FIDUCAL
FD4 @FIDUCIAL



SCALE 1.000

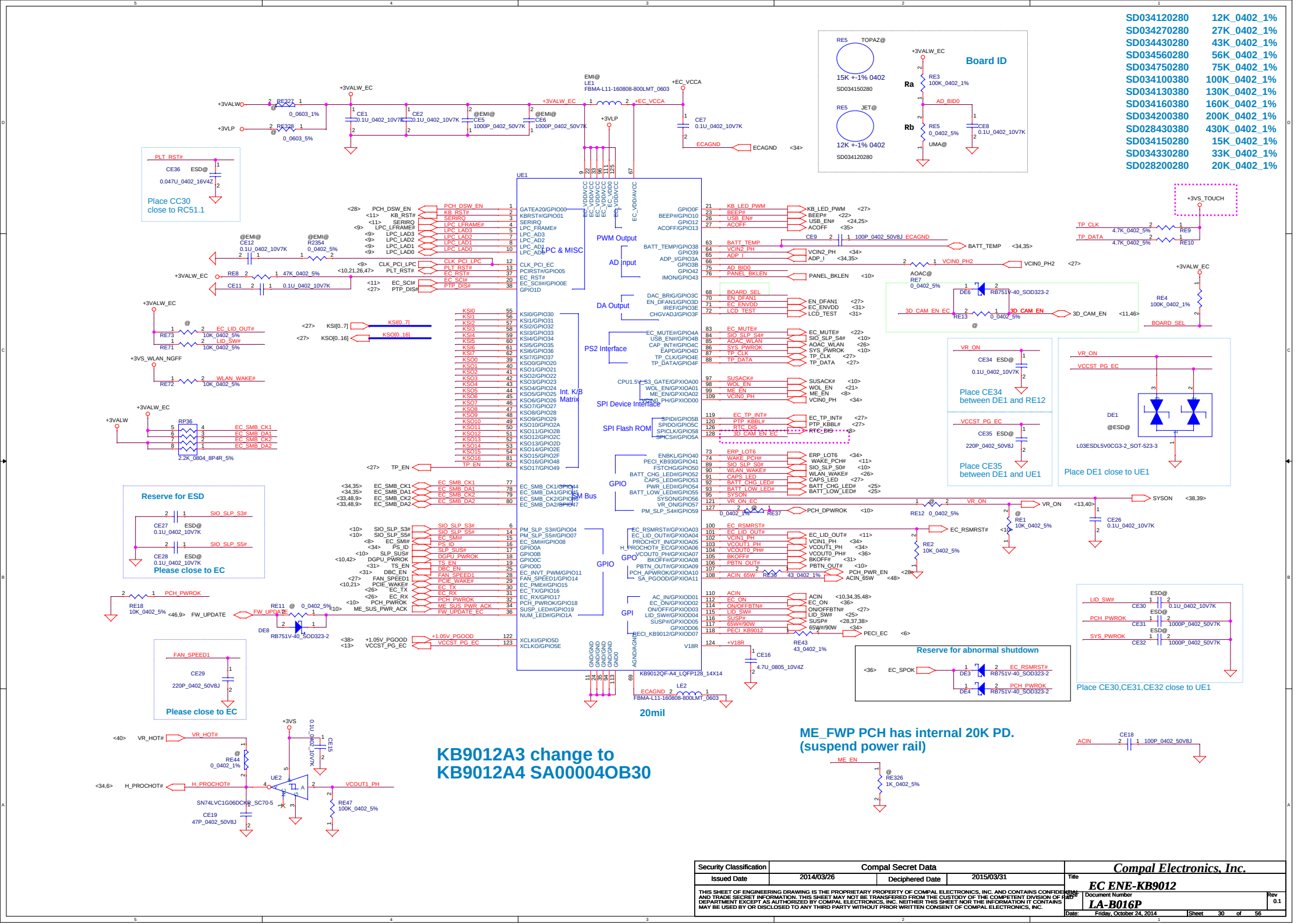
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 29 of 56


SD034120280 12K_0402_1%
SD034270280 27K_0402_1%
SD034430280 43K_0402_1%
SD034560280 56K_0402_1%
SD034750280 75K_0402_1%
SD034100380 100K_0402_1%
SD034130380 130K_0402_1%
SD034160380 160K_0402_1%
SD034200380 200K_0402_1%
SD028430380 430K_0402_1%
SD034150280 15K_0402_1%
SD034330280 33K_0402_1%
SD028200280 20K_0402_1%
Board ID
15K +-1% 0402
SD034150280
12K +-1% 0402
SD034120280
UE1
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
PC & MISC
Place CC30 close to RC51.1
Place CE34 between DE1 and RE12
Place CE35 between DE1 and UE1
Place DE1 close to UE1
Reserve for ESD
Please close to EC
Reserve for abnormal shutdown
Place CE30,CE31,CE32 close to UE1
20mil
KB9012A3 change to KB9012A4 SA00004OB30
ME_FWP PCH has internal 20K PD. (suspend power rail)
Compal Secret Data
2014/03/26
2015/03/31
Compal Electronics, Inc.
EC ENE-KB9012
LA-B016P
Rev 0.1
Friday, October 24, 2014
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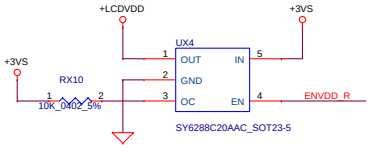
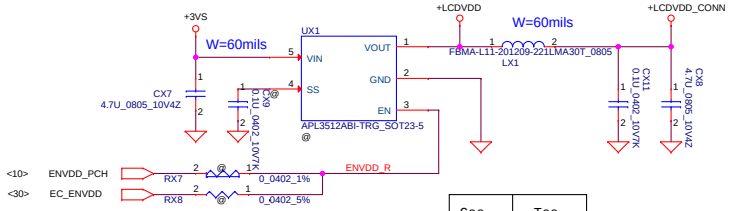
LCD PWR CTRL

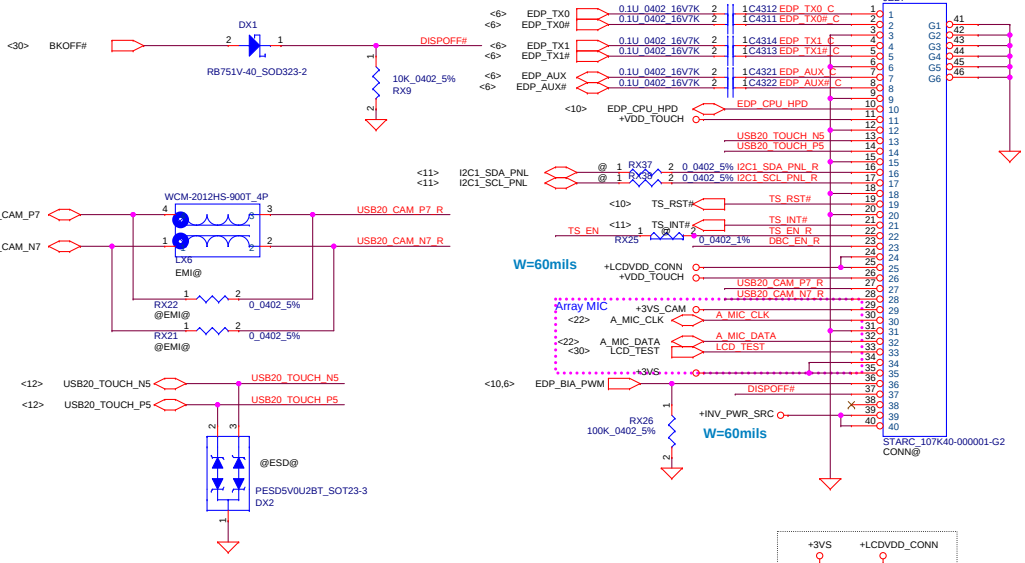


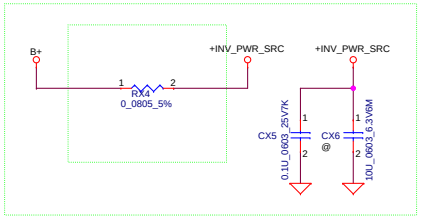


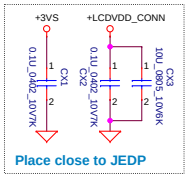
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

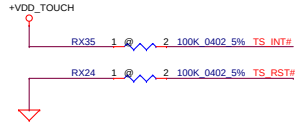
SS table

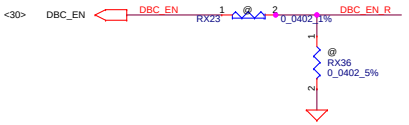
eDP Connector



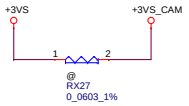




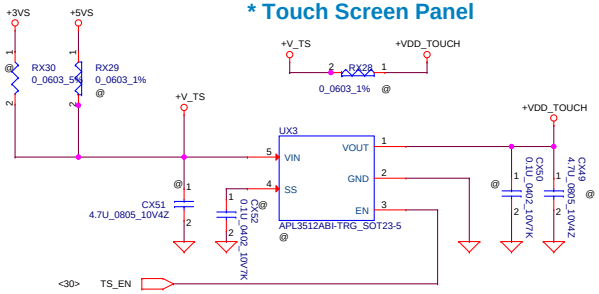


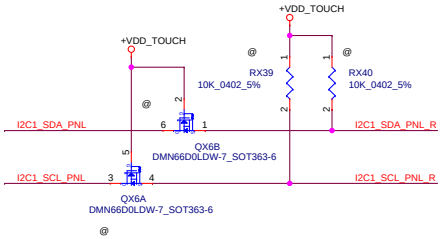


Webcam PWR CTRL



* Touch Screen Panel





Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

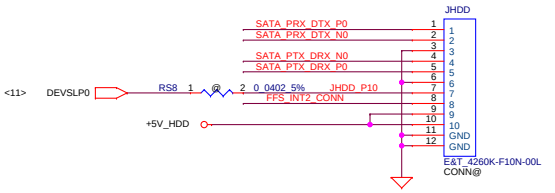
Compal Electronics, Inc.

Title: eDP / webcam / TouchScreen

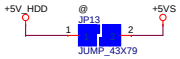
Size: A3 | Document Number: LA-B016P | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 31 of 56

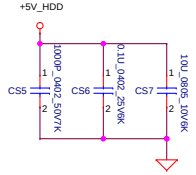
SATA HDD Connector

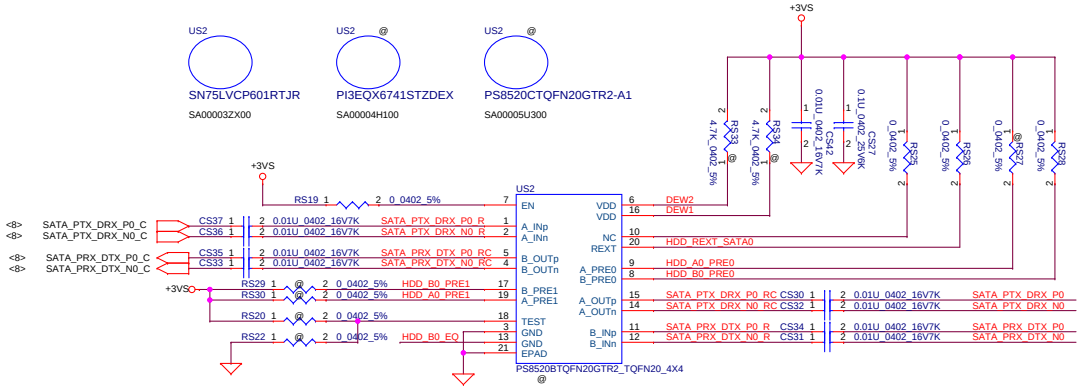


+5V_HDD Source

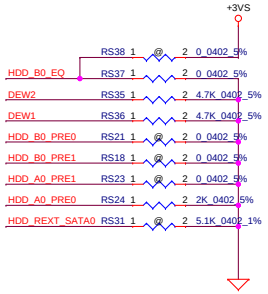


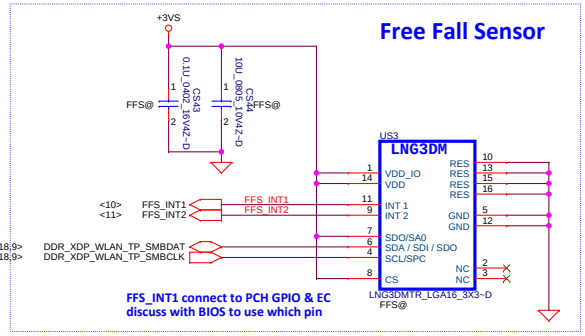
SHORT DEFAULT

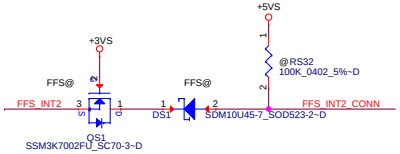




	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007TU00	7.5K	NC	V	V	V	NC	NC







Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

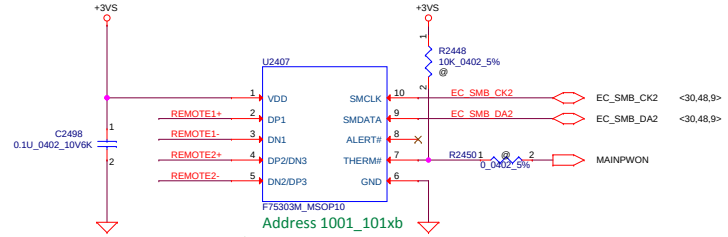
Title: HDD

Size: Document Number: LA-B016P

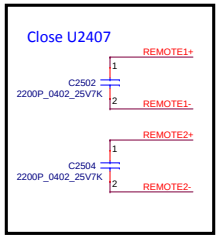
Rev: 0.1

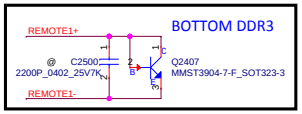
Date: Monday, October 20, 2014 Sheet 32 of 56

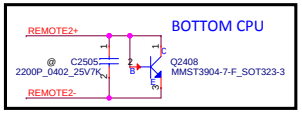
Fintek thermal sensor
placed near by TOP DDR3



2nd source
SA000029210-->EMC1403-2-AIZL-TR







REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

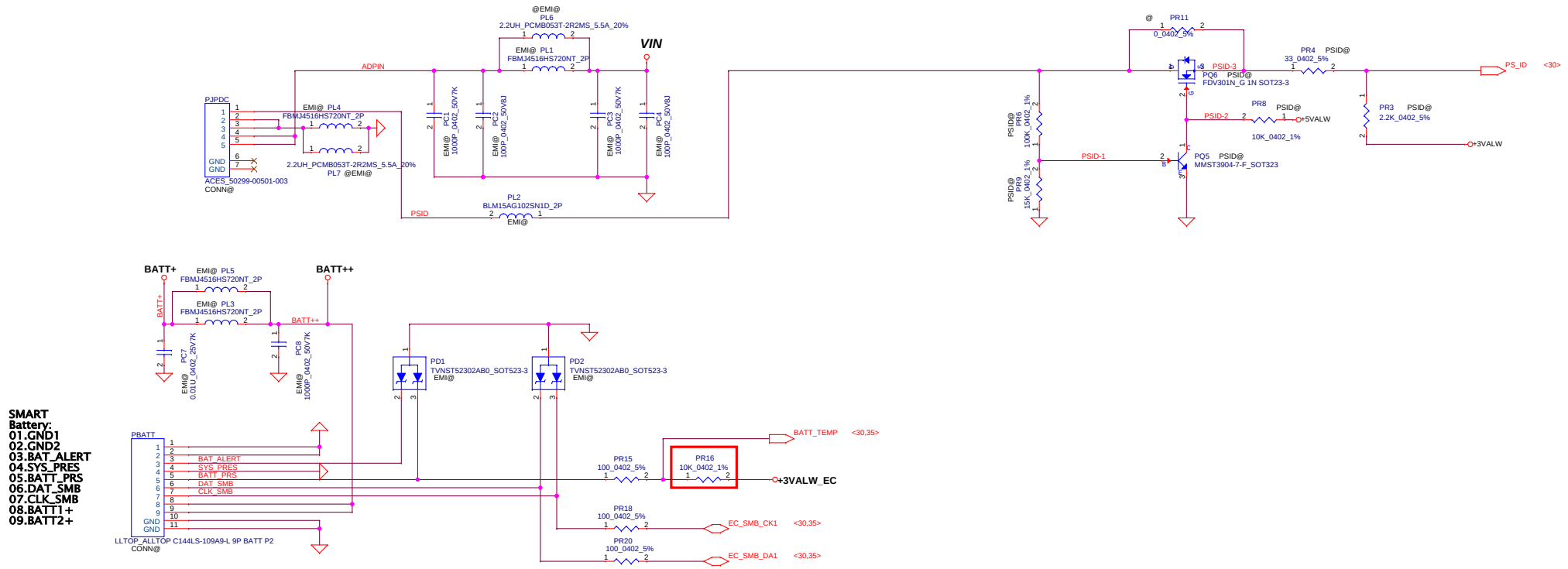
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

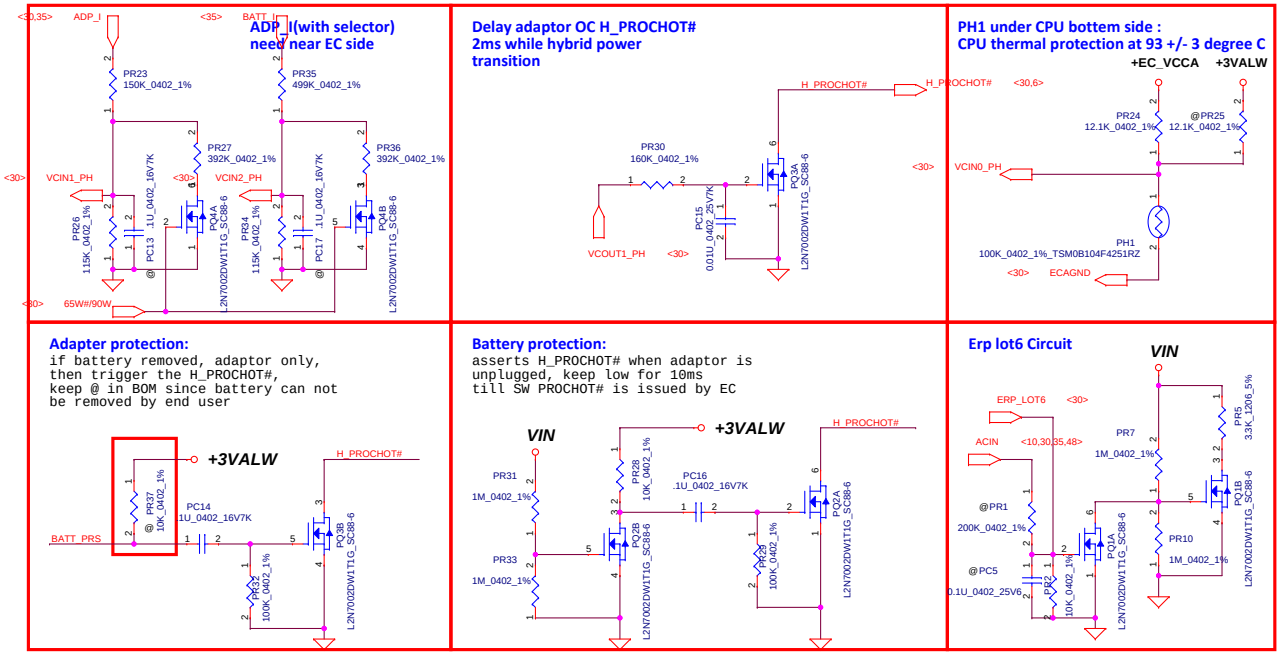
Title: **Thermal Sensor**

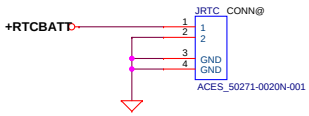
Size: | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 33 of 56



Other component (37.1)





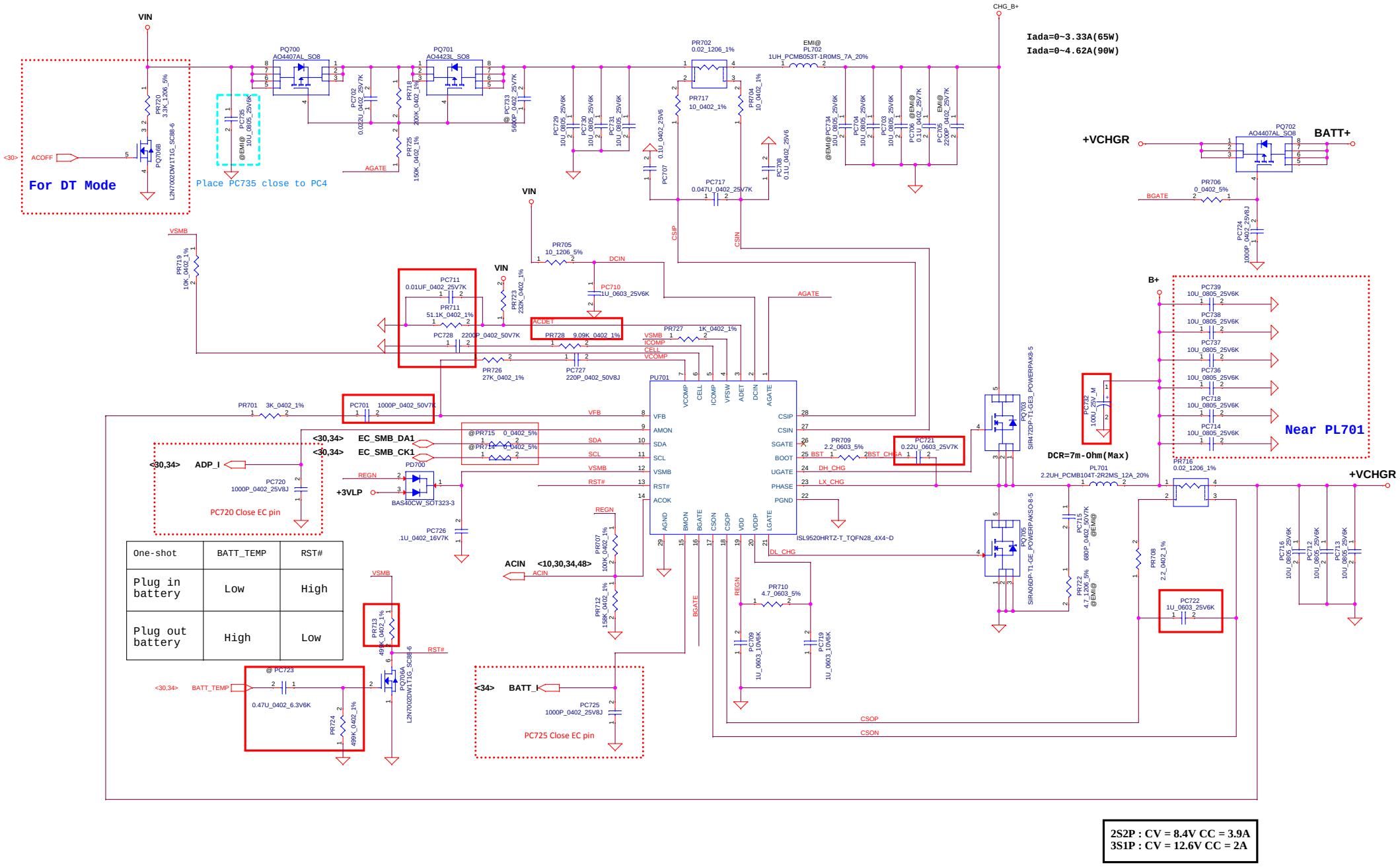
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

Size: C | Document Number: LA-B016P | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 34 of 56



One-shot	BATT_TEMP	RST#
Plug in battery	Low	High
Plug out battery	High	Low

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

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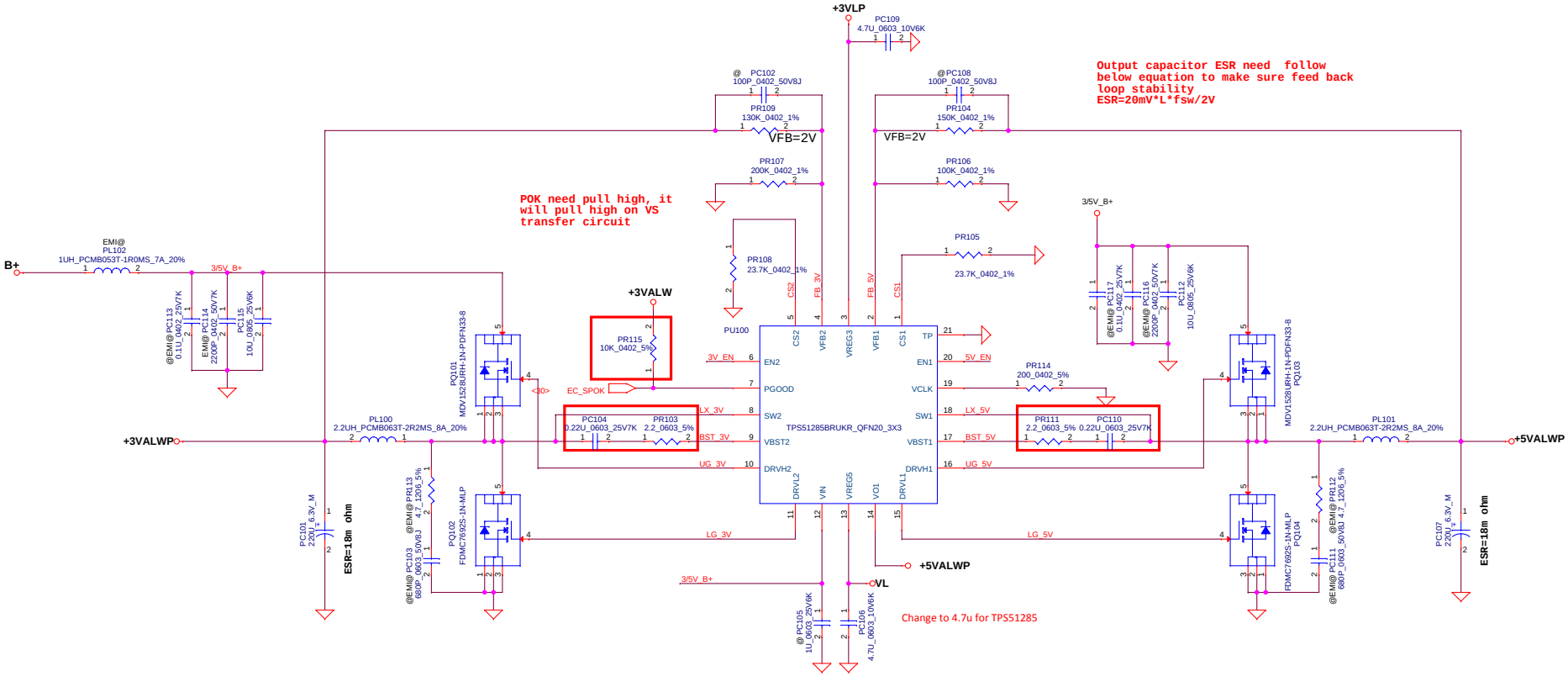
Compal Electronics, Inc.

Title: PWR_CHARGER

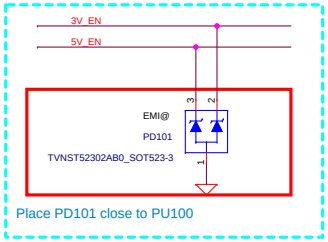
Size: A3 | Document Number: LA-B016P | Rev: 0.1

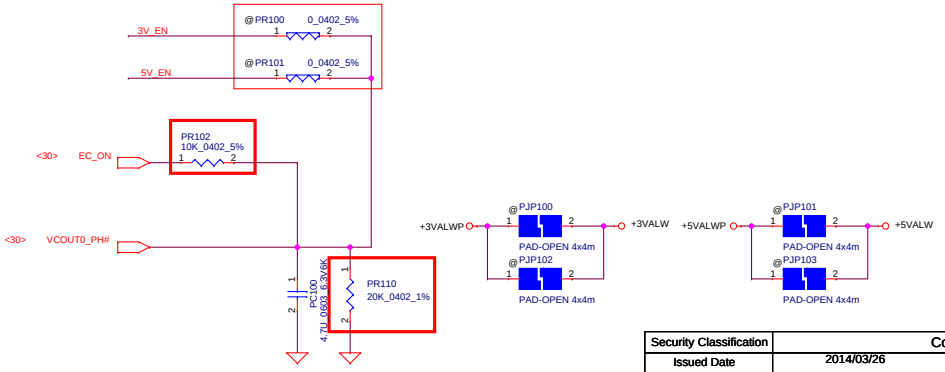
Date: Monday, October 20, 2014 | Sheet 35 of 56



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm





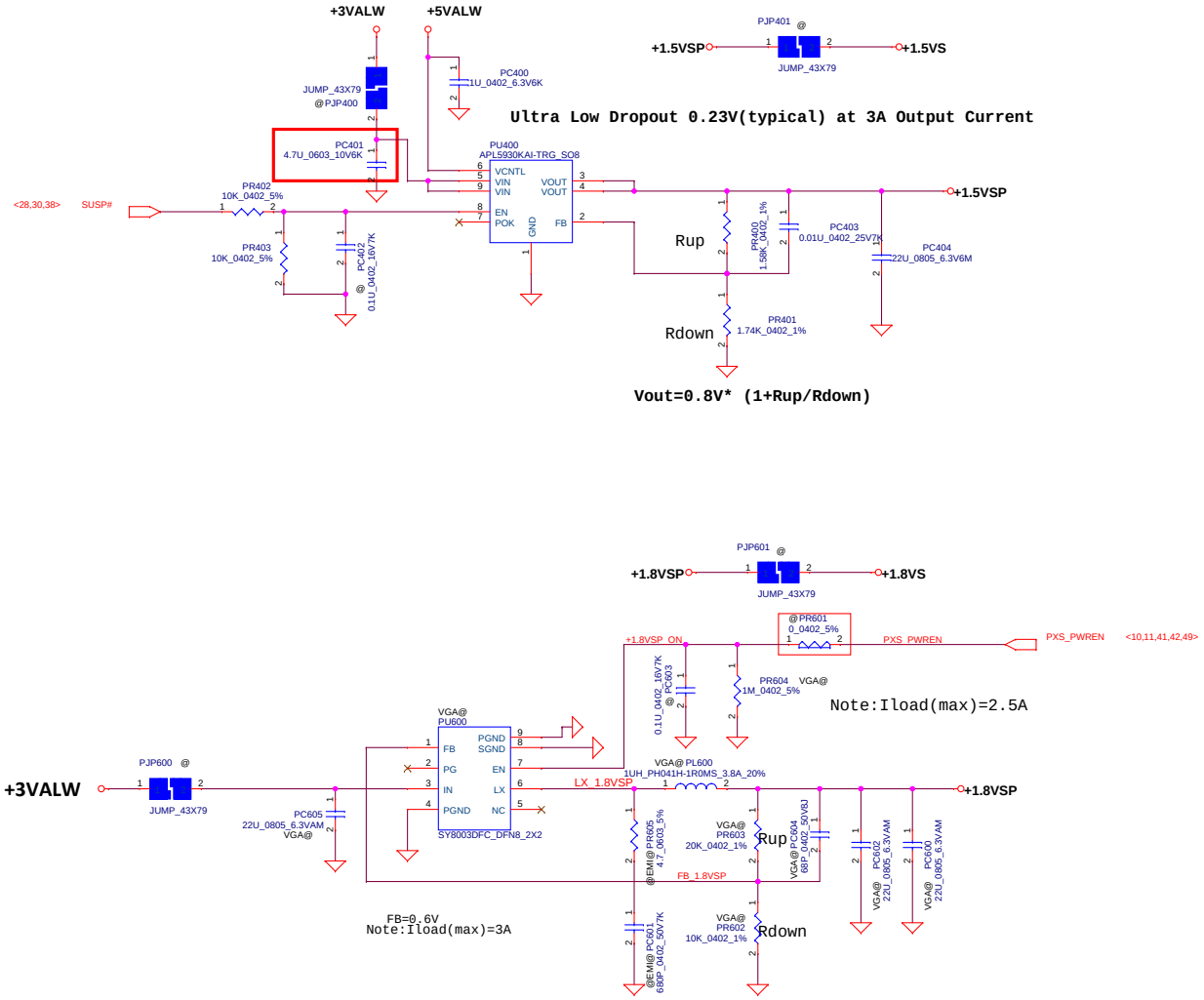
5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title	PWR_3.3VALWP/5VALWP
Size	
Document Number	LA-B016P
Rev	0.1
Date:	Monday, October 20, 2014
Sheet	36 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

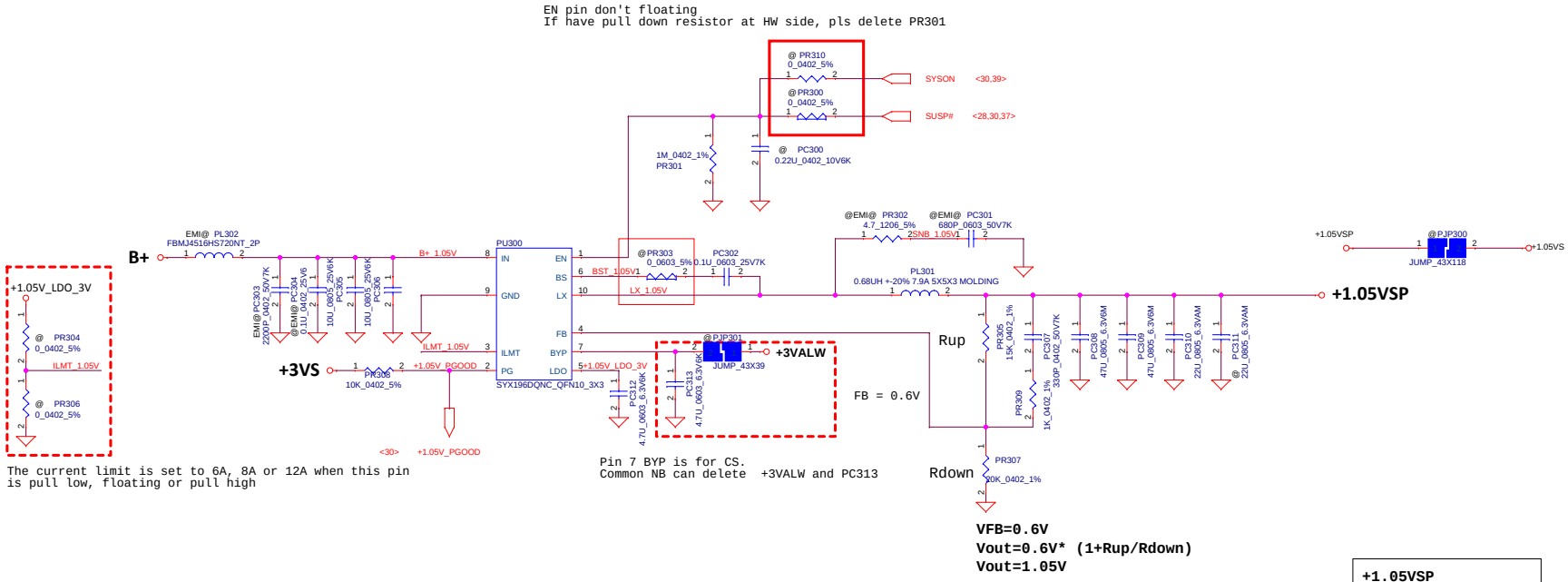
Compal Electronics, Inc.

Title: PWR_1.5VSP / 1.8VSP

Size: Document Number: LA-B016P

Rev: 0.1

Date: Monday, October 20, 2014 Sheet 37 of 56



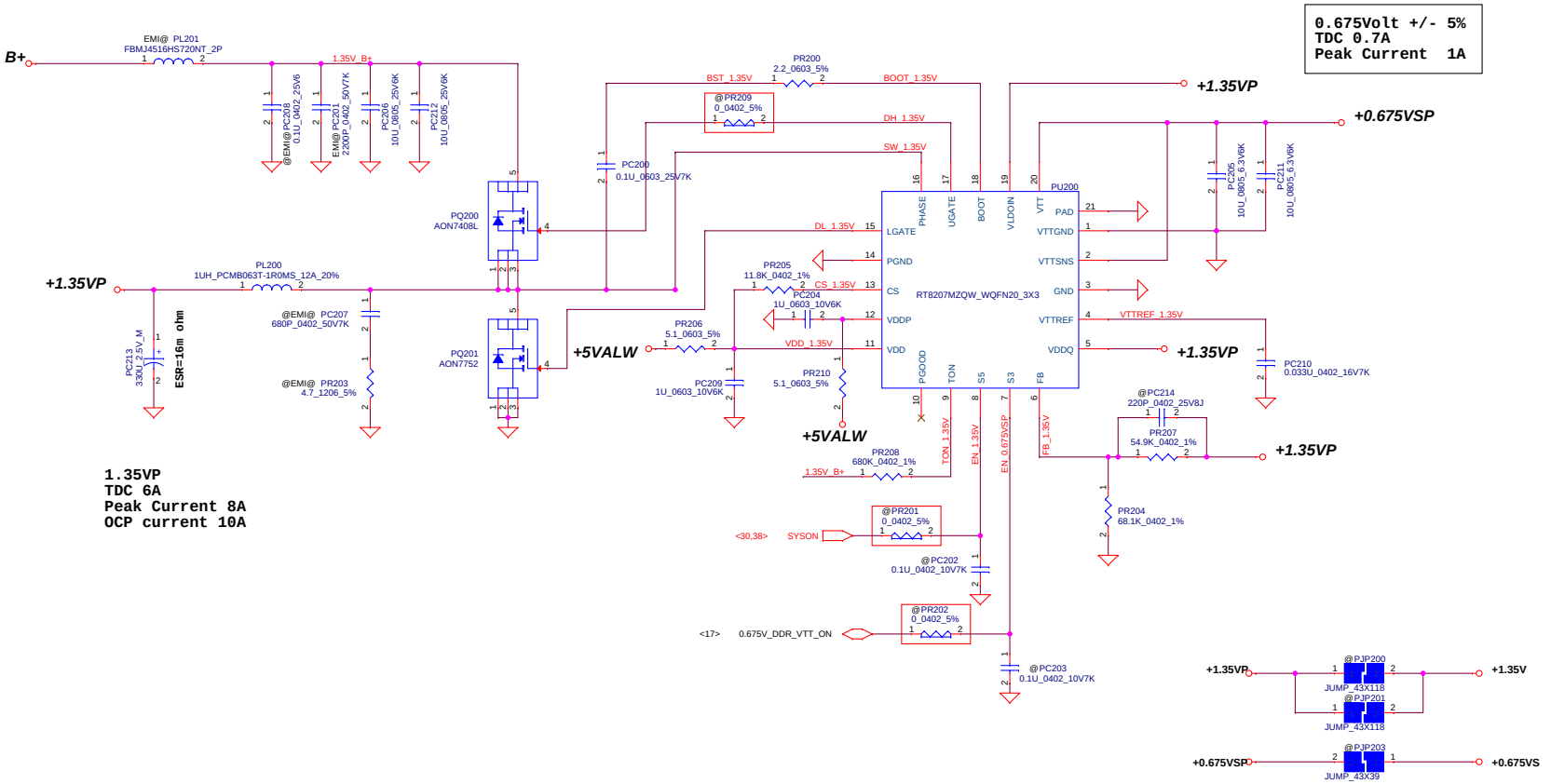
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: PWR_+VCCIO

Size: C | Document Number: LA-B012P | Rev: 0.1

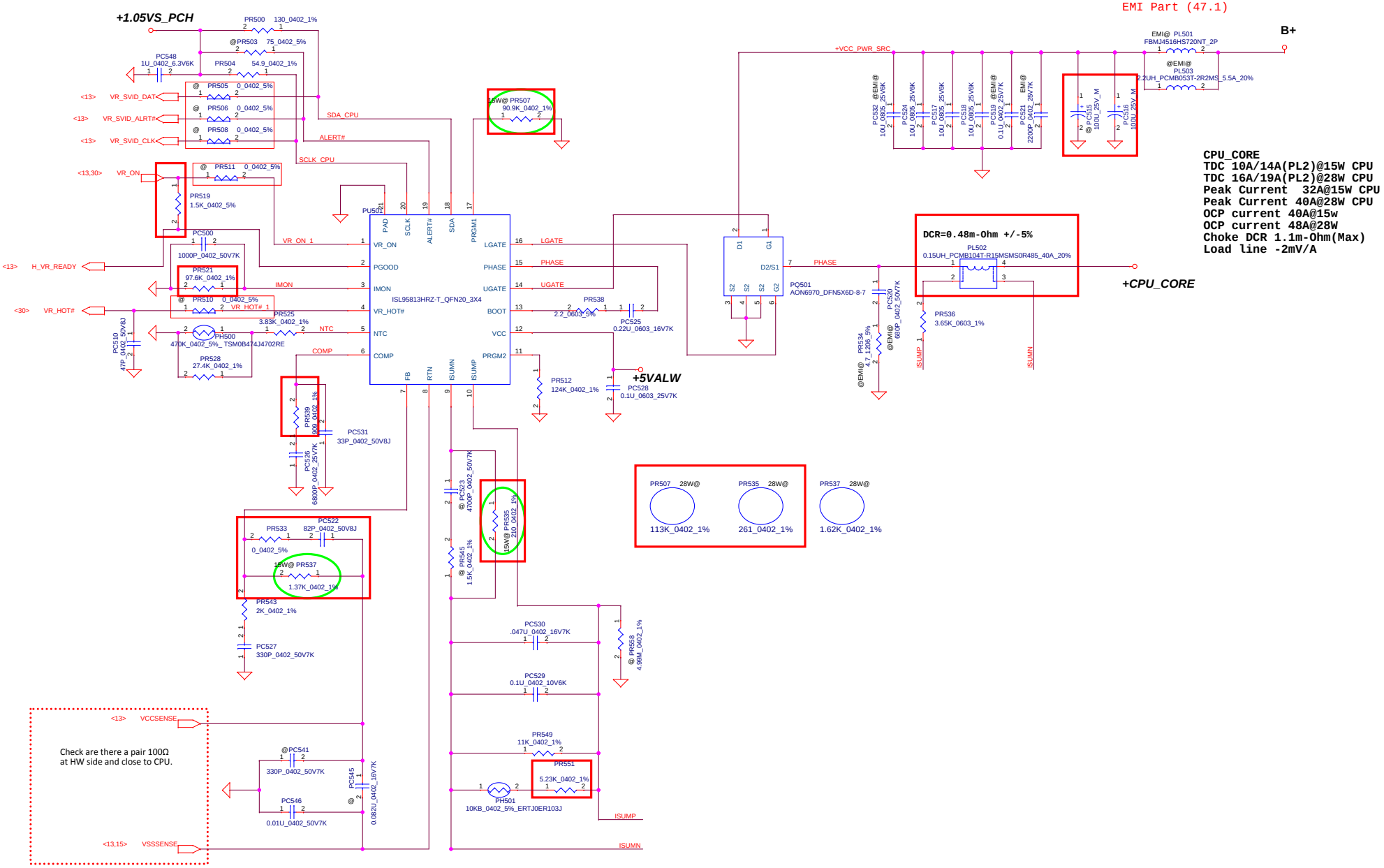
Date: Monday, October 20, 2014 | Sheet 38 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.			
Title	PWR_+1.35VP/0.675VSP		
Size	Document Number		Rev
	LA-B016P		0.1
Date:	Monday, October 20, 2014	Sheet	39 of 56

EMI Part (47.1)



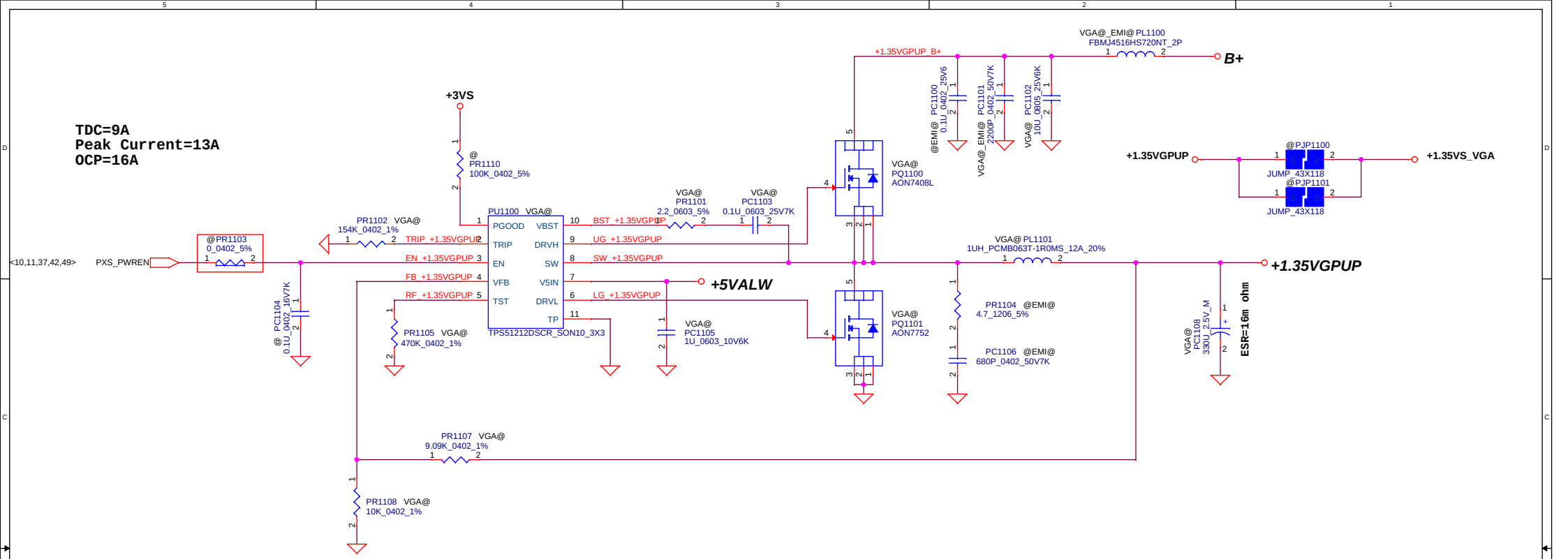
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: PWR_VCORE

Size: C | Document Number: LA-B016P | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 40 of 56



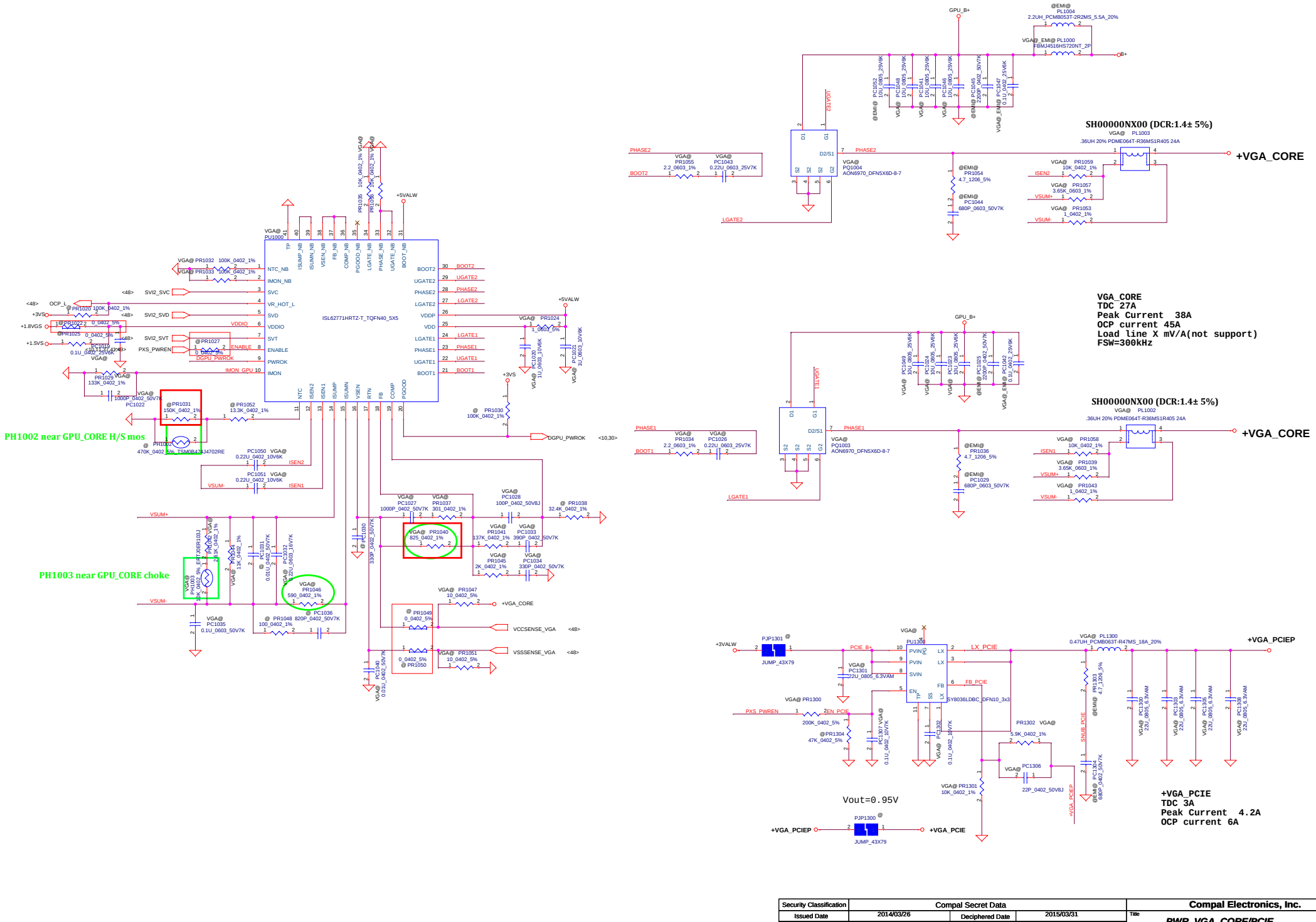
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **PWR_+1.35VGPU**

Size: B | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 41 of 56



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/26	Deciphered Date 2015/03/31	Title PWR_VGA_CORE/PCIE
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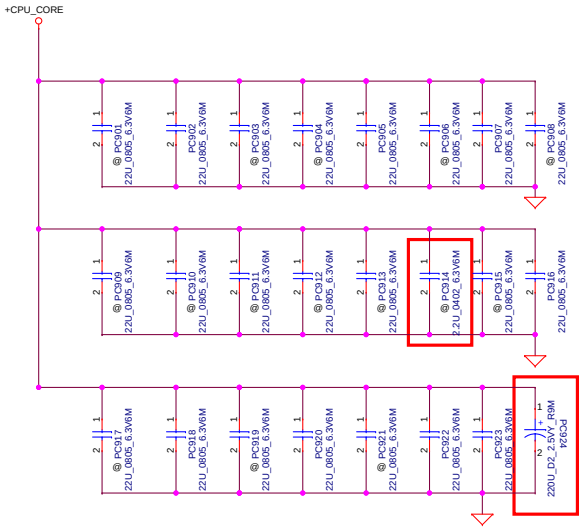
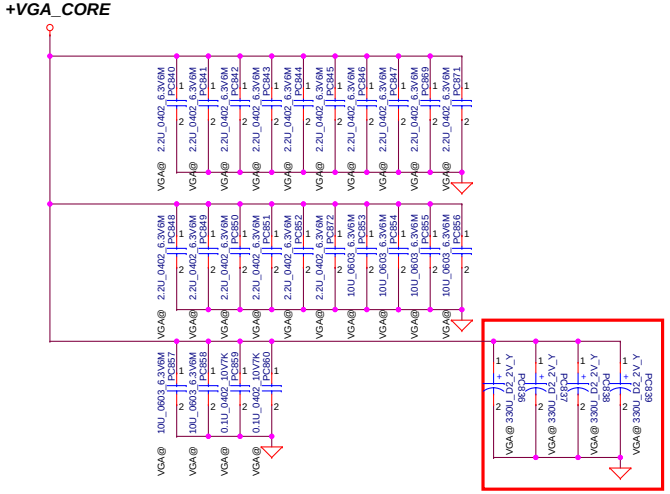
			Date: Monday, October 20, 2014 / Sheet 42 of 56





Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

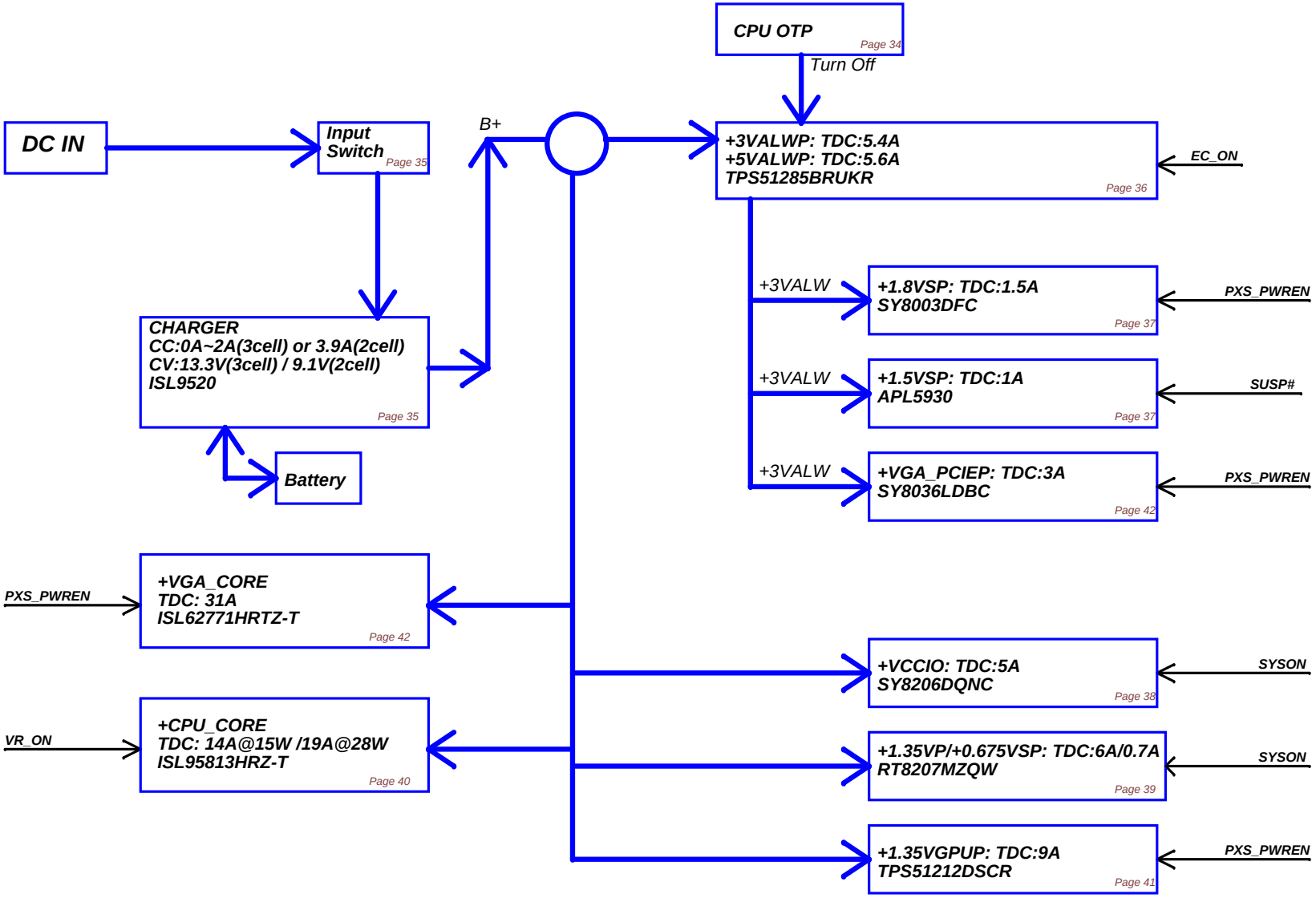
Compal Electronics, Inc.

Title: PWR_PROCESSOR DECOUPLING

Size: A3 | Document Number: LA-B016P | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 43 of 56

Power block



Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number	LA-B016P	Rev 0.1
Date: Monday, October 20, 2014	Sheet 44 of 56		

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PL502 from SH00000NM00 to SH00000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

Vendor	PS8713B	TI	Spec				schematic netname	3Vs		GND	
1	VDD	VCC	Same								
2	B_EQ0	EQ1	**LL:** 9.5dB (default)	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_EQ1_P0	RI23	@	RI32	@
3	DE0	DE1	LL: 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE1_P0	RI26	@	RI35	@
4	EQ1	OS1	**LL:** 9.5dB	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_OS1_P0	RI22	@	RI40	@
5	PD#	EN_RXD	it can be left open				USB3_ERD_P0	RI44	@	RI48	@
6	B_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN6	RI53	@	RI49	@
7	REXT	NC		4.99K						RI56	4.99K
8	B_Inn	RX1-	Same								
9	B_Inp	RX1+	Same								
10	GND	GND	Same								
11	A_OUTn	TX2-	Same								
12	A_OUTp	TX2+	Same								
13	VDD	VCC	Same								
14	TST/NC	CM	4.7K ohm resistor for perfomance adjustment				USB3_CM_P0	RI42	@	RI46	@
15	A_EQ1	OS2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_OS2_P0	RI19	@	RI87	@
16	A_DE0	DE2	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE2_P0	RI20	@	RI31	@
17	A_EQ0	EQ2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_EQ2_P0	RI21	@	RI36	@
18	A_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN18	RI52	@	RI50	@
19	A_Inp	RX2+	Same								
20	A_Inn	RX2-	Same								
21	GND	GND	Same								
22	B_OUTp	TX1+	Same								
23	B_OUTn	TX1-	Same								
24	I2C_EN	NC	this pin canbe NC or connected to GND				NC			RI57	@

+3VALW TO +5V_3DCAM

J518 open

+5VALW — C94 1U_0402_6.3V6K — J521 @ JUMP_43X39 — +5V_CAM

U2409 TPS22967DSGR_SON8_2X2: VIN VIN VOUT VOUT ON CT VBIAS GND GND

RI90 100K_0402_5%

C5220 2200P_0402_25V7K — C5221 0.1U_0402_10V6K

For Test,
APE8937(SA000070L00)
AOZ1336(SA00006U600)
TPS22967(SA000070S00)

CT pin use 2200pf for soft start tuning

+3VS

RI53 1 @ 2 3.3K_0402_5% USB3_P0_PIN6
RI52 1 @ 2 3.3K_0402_5% USB3_P0_PIN18
RI421 2 4.7K_0402_5%-D USB3_CM_P0
RI441 @ 2 4.7K_0402_5%-D USB3_ERD_P0
RI191 @ 2 4.7K_0402_5%-D USB3_OS2_P0
RI201 @ 2 4.7K_0402_5%-D USB3_DE2_P0
RI211 @ 2 4.7K_0402_5%-D USB3_EQ2_P0
RI221 @ 2 4.7K_0402_5%-D USB3_OS1_P0
RI261 @ 2 4.7K_0402_5%-D USB3_DE1_P0
RI231 @ 2 4.7K_0402_5%-D USB3_EQ1_P0

RI871 @ 2 4.7K_0402_5%-D USB3_OS2_P0
RI311 @ 2 4.7K_0402_5%-D USB3_DE2_P0
RI361 @ 2 4.7K_0402_5%-D USB3_EQ2_P0
RI401 @ 2 4.7K_0402_5%-D USB3_OS1_P0
RI351 @ 2 4.7K_0402_5%-D USB3_DE1_P0
RI321 @ 2 4.7K_0402_5%-D USB3_EQ1_P0

RI461 @ 2 4.7K_0402_5%-D USB3_CM_P0
RI481 @ 2 4.7K_0402_5%-D USB3_ERD_P0
RI49 1 @ 2 0_0402_5%-D USB3_P0_PIN6
RI50 1 @ 2 0_0402_5%-D USB3_P0_PIN18

@RI3 1 2 0_0402_5%-D
USB3RN4_R_C — EMI@ LI10 — USB3RN4_R
USB3RP4_R_C — EMI@ LI10 — USB3RP4_R
S COM FI_ CHILISIN CMMI21T-670Y-N
@RI4 1 2 0_0402_5%-D

@RI5 1 2 0_0402_5%-D
USB3TN4_R_C — EMI@ LI9 — USB3TN4_R
USB3TP4_R_C — EMI@ LI9 — USB3TP4_R
S COM FI_ CHILISIN CMMI21T-670Y-N
@RI6 1 2 0_0402_5%-D

+3VALW_PCH — +3VS — RI55 10K_0402_5% — RI89 @ 10K_0402_5% — FW_UPDATE

+3VALW_PCH — +3VS — RI54 10K_0402_5% — RI88 @ 10K_0402_5% — 3D_CAM_EN

CI23 0.01U_0402_16V7K~D
CI20 .1U_0402_16V7K~D

UI8 PS8713BTQFN24GTR2-A0_TQFN24_4X4

			1	VCC	NC	7	RI56 1	2 3.3K_0402_1%	
			13	VCC	NC	24	@RI57 1	2 0_0402_5%-D	
<12>	USB3RN4_3D_CAM	USB3RN4 CI22 1 2 0.1U_0402_10V6K~D	USB3RN4_L	11	TX2-	RX2-	20	USB3RN4_R_C	
<12>	USB3RP4_3D_CAM	USB3RP4 CI19 1 2 0.1U_0402_10V6K~D	USB3RP4_L	12	TX2+	RX2+	19	USB3RP4_R_C	
		USB3_OS2_P0		15	OS2				
		USB3_DE2_P0		16	DE2	EN_RXD	5	USB3_ERD_P0	
		USB3_EQ2_P0		17	EQ2	CM	14	USB3_CM_P0	
<12>	USB3TN4_3D_CAM	USB3TN4 CI16 1 2 0.1U_0402_10V6K~D	USB3TN4_L	8	RX1-	TX1-	23	USB3TN4_RC CI21 1 2 0.1U_0402_10V6K~D	USB3TN4_R_C
<12>	USB3TP4_3D_CAM	USB3TP4 CI5 1 2 0.1U_0402_10V6K~D	USB3TP4_L	9	RX1+	TX1+	22	USB3TP4_RC CI24 1 2 0.1U_0402_10V6K~D	USB3TP4_R_C
		USB3_OS1_P0		4	OS1				
		USB3_DE1_P0		3	DE1	GND	6	USB3_P0_PIN6	
		USB3_EQ1_P0		2	EQ1	GND	10		
						GND	18	USB3_P0_PIN18	
				25	PGND	GND	21		

<11> <30,9> CAM_DETECT FW_UPDATE

CAM_DETECT 1 — RI58 0_0402_5%-D — 2 DETECT

FW_UPDATE — RI91 100K_0402_5% @ — +5V_CAM

JCAM3D

USB3RN4_R	2	2	USB3RN4_R
USB3RP4_R	3	3	USB3RP4_R
	4	4	
USB3TN4_R	5	5	USB3TN4_R
USB3TP4_R	6	6	USB3TP4_R
DETECT	7	7	
	8	8	
	9	9	
	10	10	
	11	11	GND
	12	12	GND

ACES_50463-0104A-001

DI3 — S DIO(BR) TVWDF1004AD0 DFN ESD @

USB3RN4_R	1	10	USB3RN4_R
USB3RP4_R	2	9	USB3RP4_R
USB3TN4_R	4	7	USB3TN4_R
USB3TP4_R	5	6	USB3TP4_R
	3		
	8		

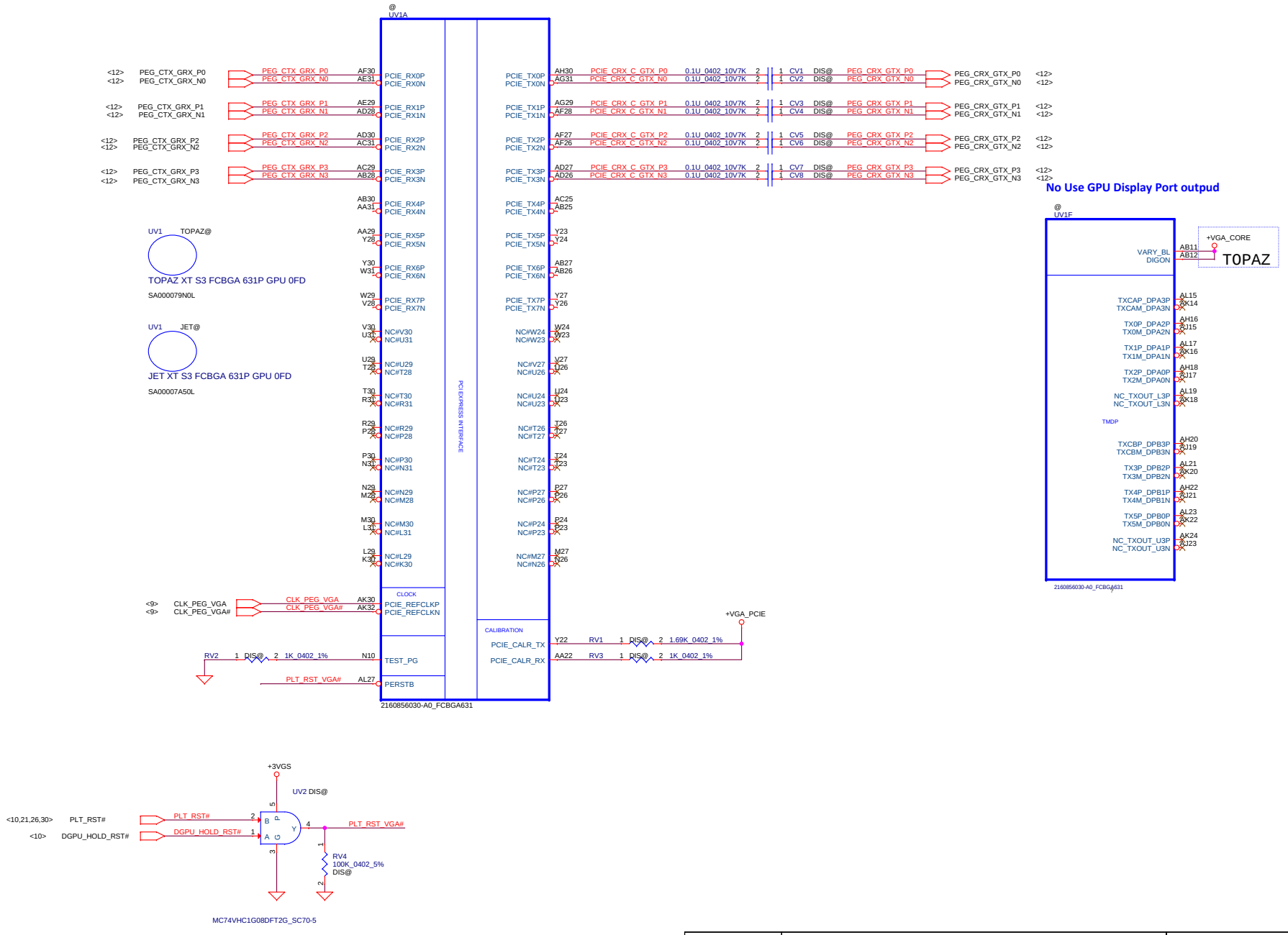
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **LED / B**

Size: B — Document Number: **LA-B016P** — Rev: 0.1

Date: Friday, October 24, 2014 — Sheet 46 of 56



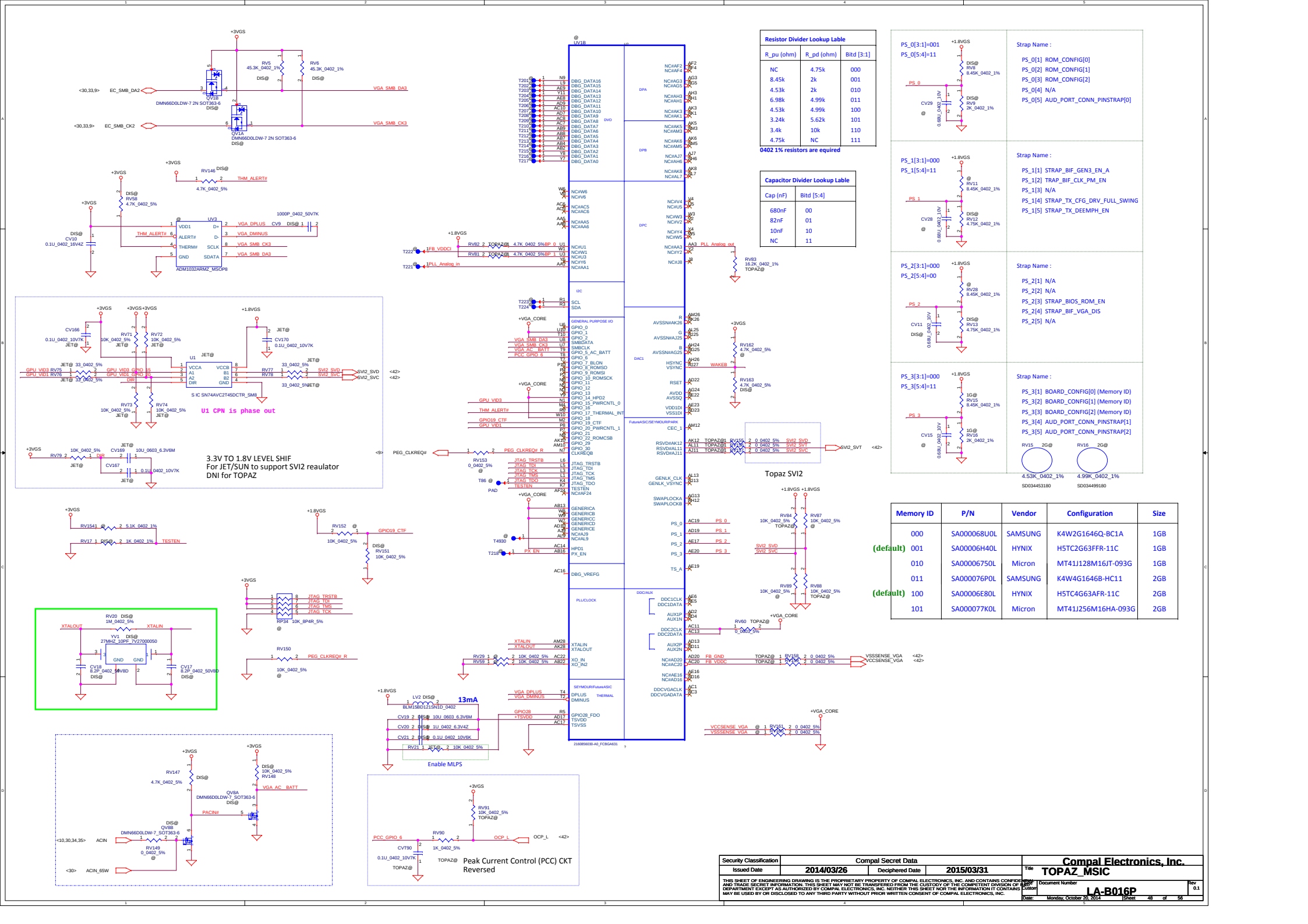
Security Classification	Compal Secret Data		
Issued Date	2014/03/26	Deciphered Date	2015/03/31

Compal Electronics, Inc.

Title: **TOPAZ_PCIE/DP**

Size: Custom | Document Number: **LA-B016P** | Rev: 0.1

Date: Monday, October 20, 2014 | Sheet 47 of 56


Resistor Divider Lookup Lable
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
0402 1% resistors are equired
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=00
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
4.53K_0402_1%
4.99K_0402_1%
SD034453180
SD034499180
U1 CPN is phase out
3.3V TO 1.8V LEVEL SHIF
For JET/SUN to support SVI2 reaulator
DNI for TOPAZ
Topaz SVI2
13mA
Enable MLPS
Peak Current Control (PCC) CKT
Reversed
Memory ID | P/N | Vendor | Configuration | Size
000 | SA000068U0L | SAMSUNG | K4W2G1646Q-BC1A | 1GB
(default) 001 | SA00006H40L | HYNIX | H5TC2G63FFR-11C | 1GB
010 | SA00006750L | Micron | MT41J128M16JT-093G | 1GB
011 | SA000076P0L | SAMSUNG | K4W4G1646B-HC11 | 2GB
(default) 100 | SA00006E80L | HYNIX | H5TC4G63AFR-11C | 2GB
101 | SA000077K0L | Micron | MT41J256M16HA-093G | 2GB
Security Classification
Compal Secret Data
Issued Date 2014/03/26
Deciphered Date 2015/03/31
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Size B
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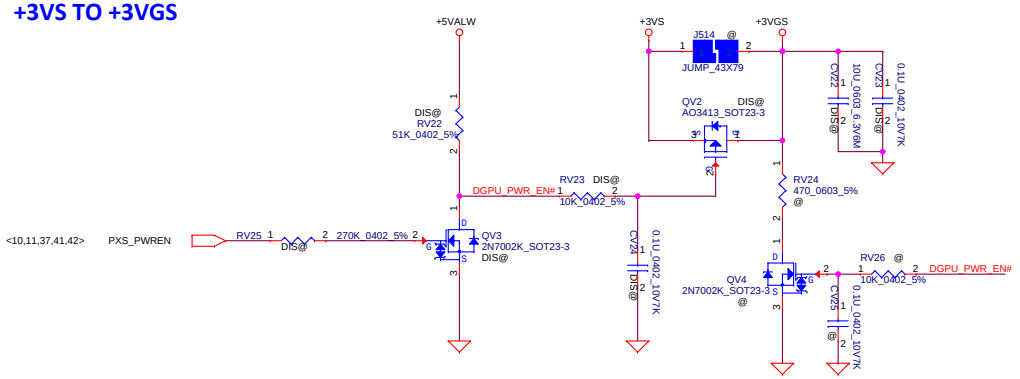
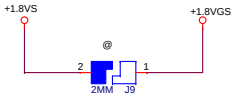
+3VS TO +3VGS



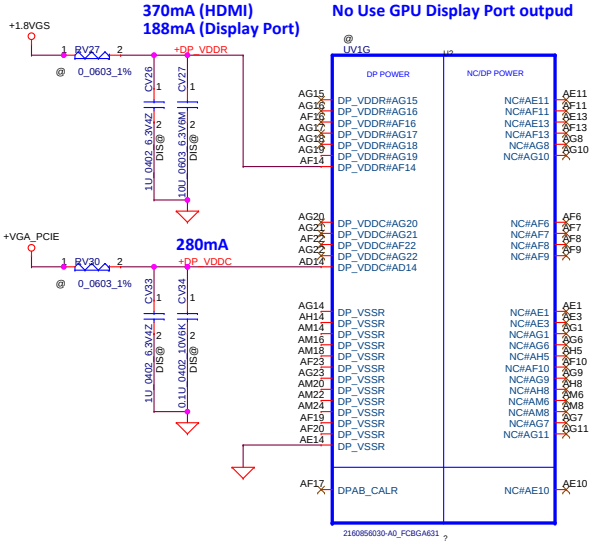
+1.35VS_VGA TO +1.35V_MEM_GFX

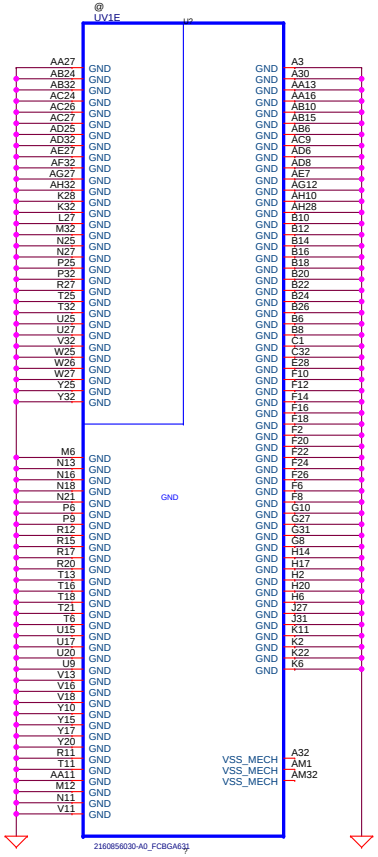
SHORT DEFAULT

+1.8VS TO +1.8VGS



SHORT DEFAULT





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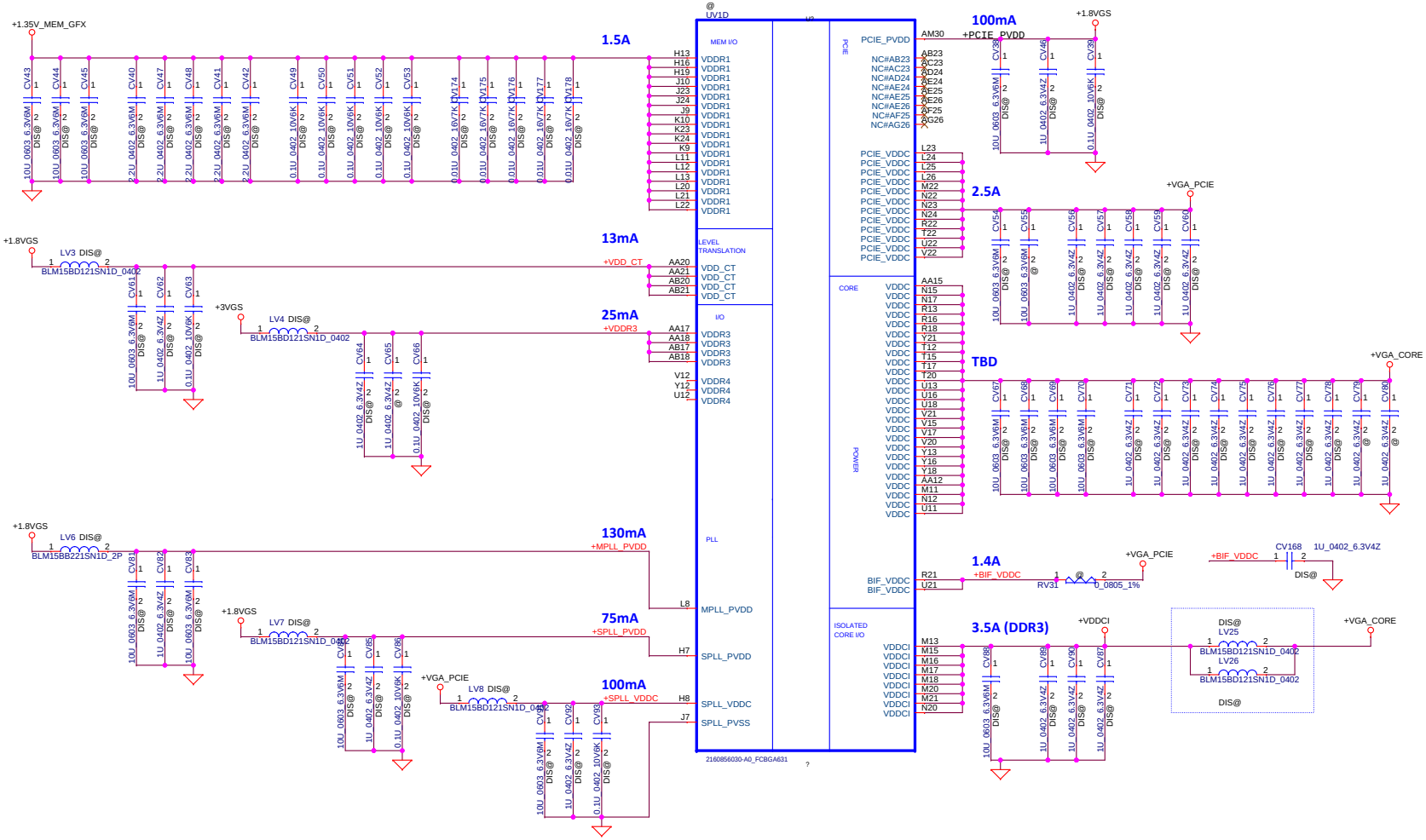
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+VGA_PCIE		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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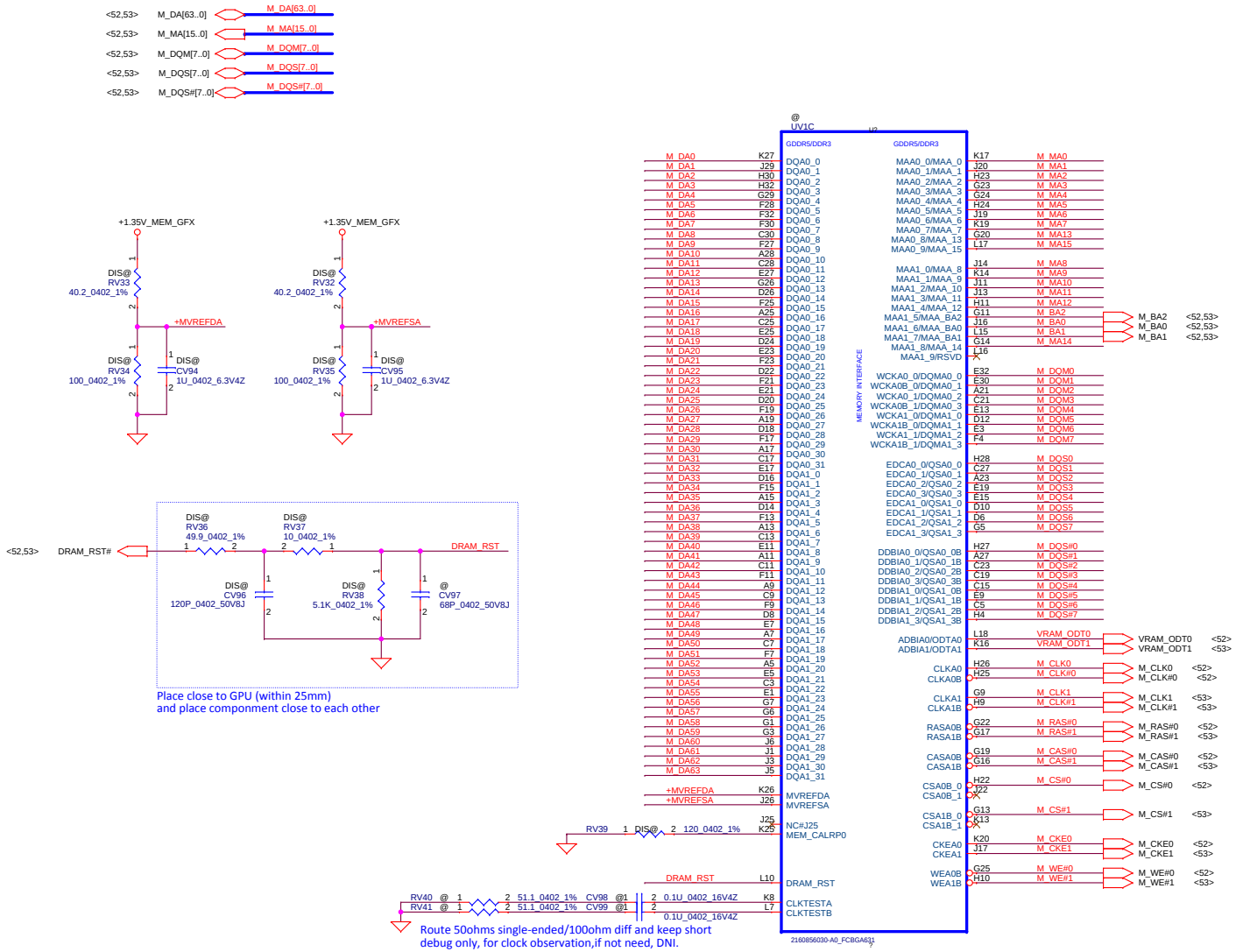

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Title: **TOPAZ_MEM**

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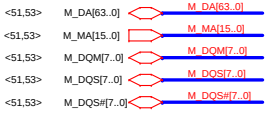
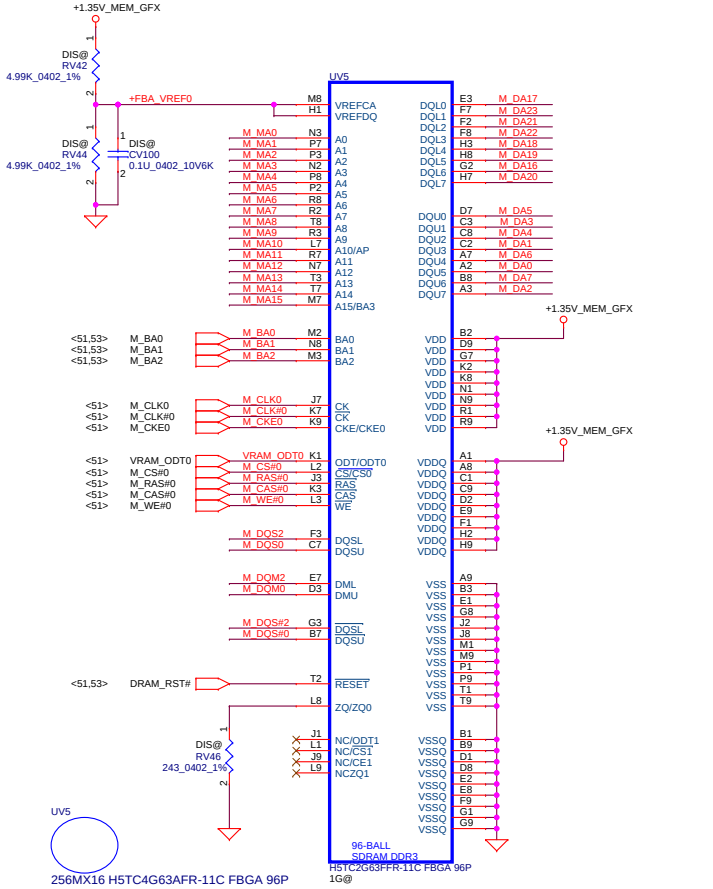
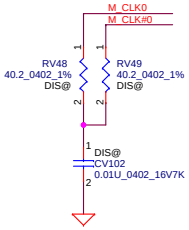
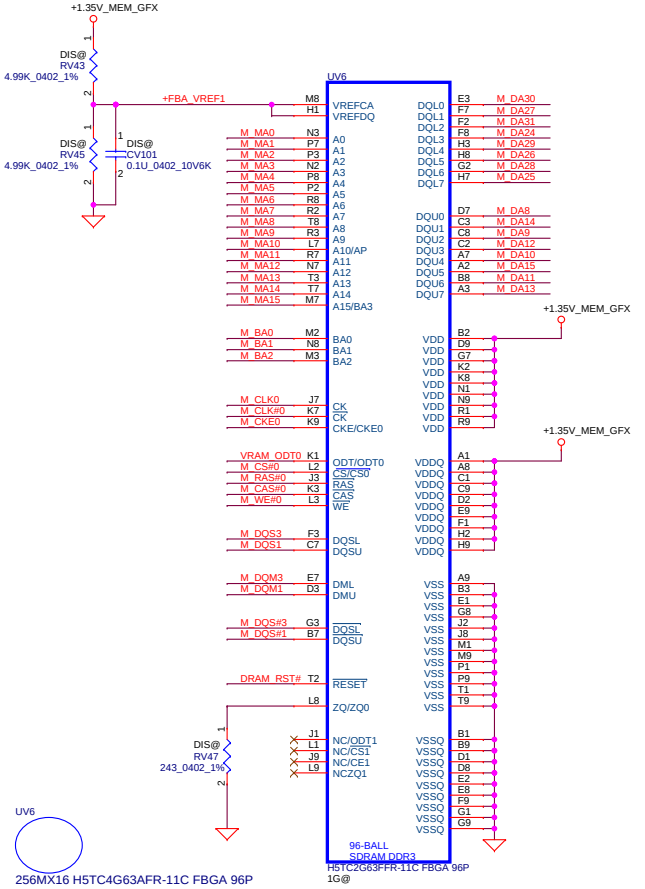
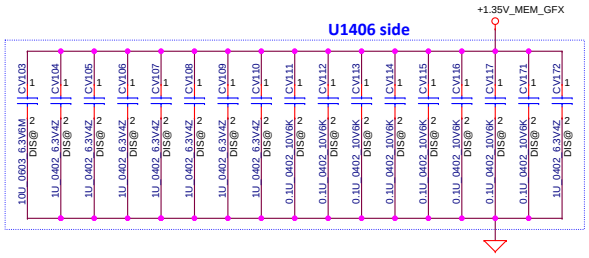
Memory Partition A - Lower 32 bits

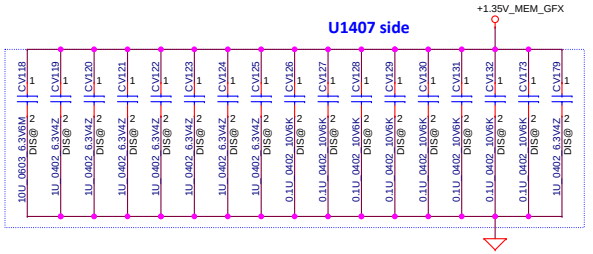












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Title: TOPAZ_VRAM A Lower

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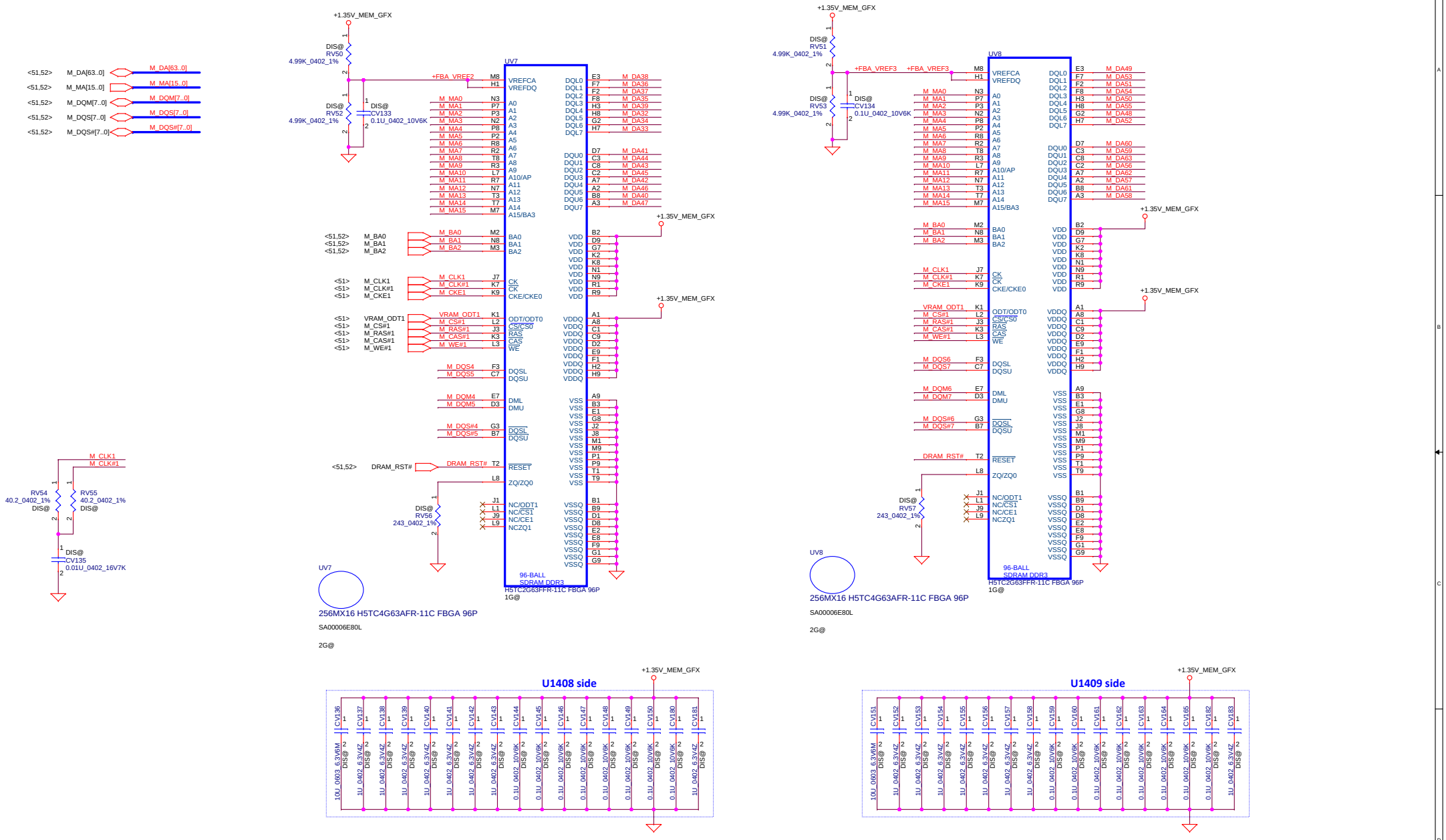
Memory Partition A - Upper 32 bits



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Title: TOPAZ_VRAM A Upper

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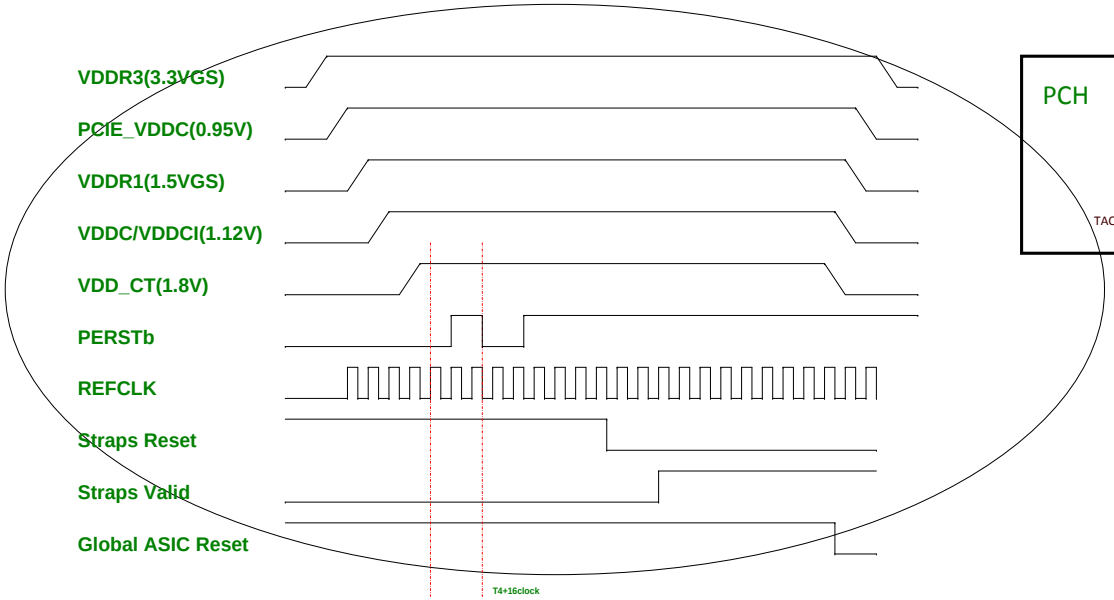
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

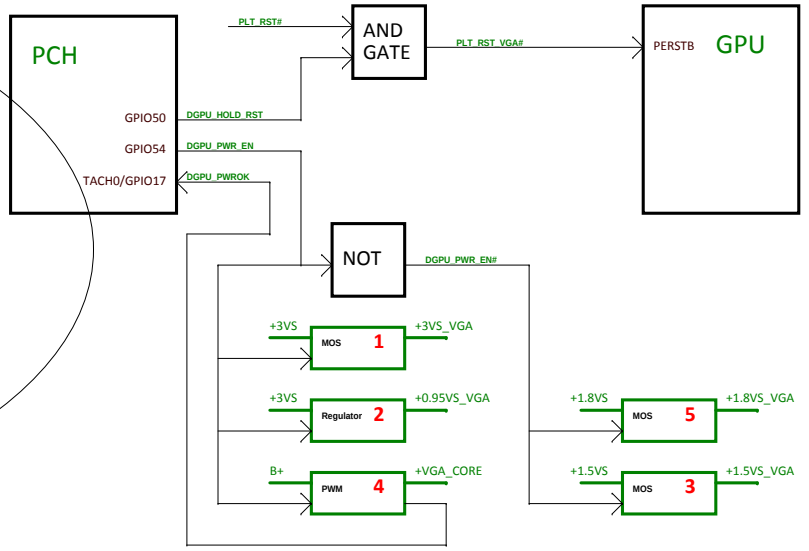
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



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