

Model Name: KML50 DIS
PCB NO: LA-4595PR04
BOM P/N: DA80000DR00

Half Penny Bridge 15.4 Compal Confidential

Schematic Document

Cantiga + ICH9

2009 / 02 / 17 Rev:1.0 (A00)



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Voltage Rails O MEANS ON X MEANS OFF

power plane				
State		+5VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1V_GFX_PCIEP
	+B	+3VALW		
s0	O	O	O	O
s1	O	O	O	O
s3	O	O	O	X
s5 s4/AC	O	O	X	X
s5 s4/ Battery only	O	X	X	X
s5 s4/AC & Battery don't exist	X	X	X	X

Symbol Note :

-  : means Digital Ground
-  : means Analog Ground
- @ : means just reserve , no build
- CON@ : means ME connectors
- TPM@ : means TPM function

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
1	CAMERA	
2	JUSBP3 TOP	
3	Felica	
4	Blue Tooth	
5	Finger Printer	
6	JMINI2-WLAN	
7	Express card	
8	JUSBP3 BOT	
9	JMINI1-WWAN	
10	JUSBP4	
11	NA	

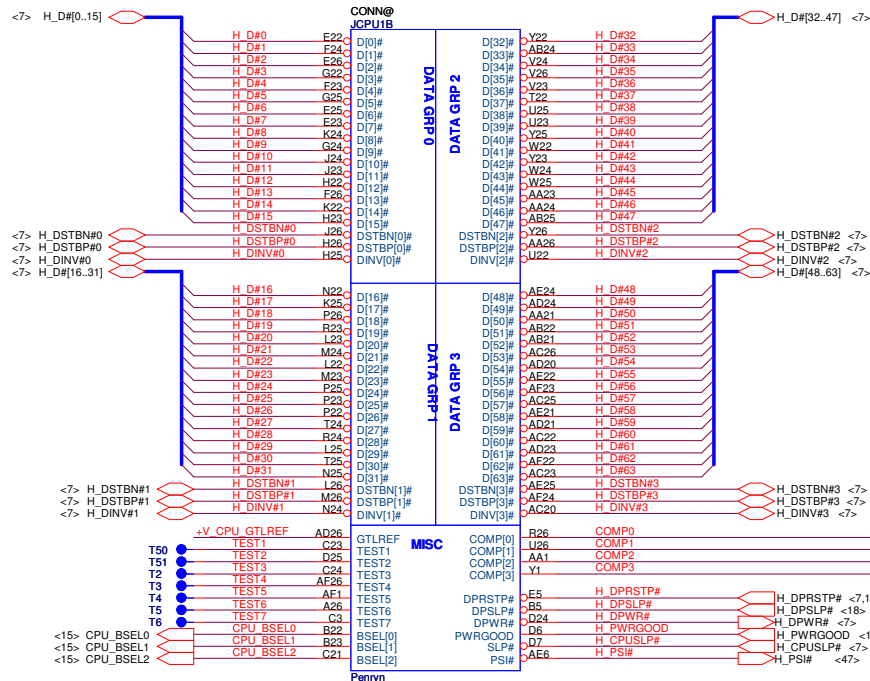
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

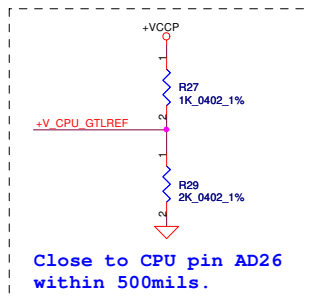
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
LED panel	58	01011000

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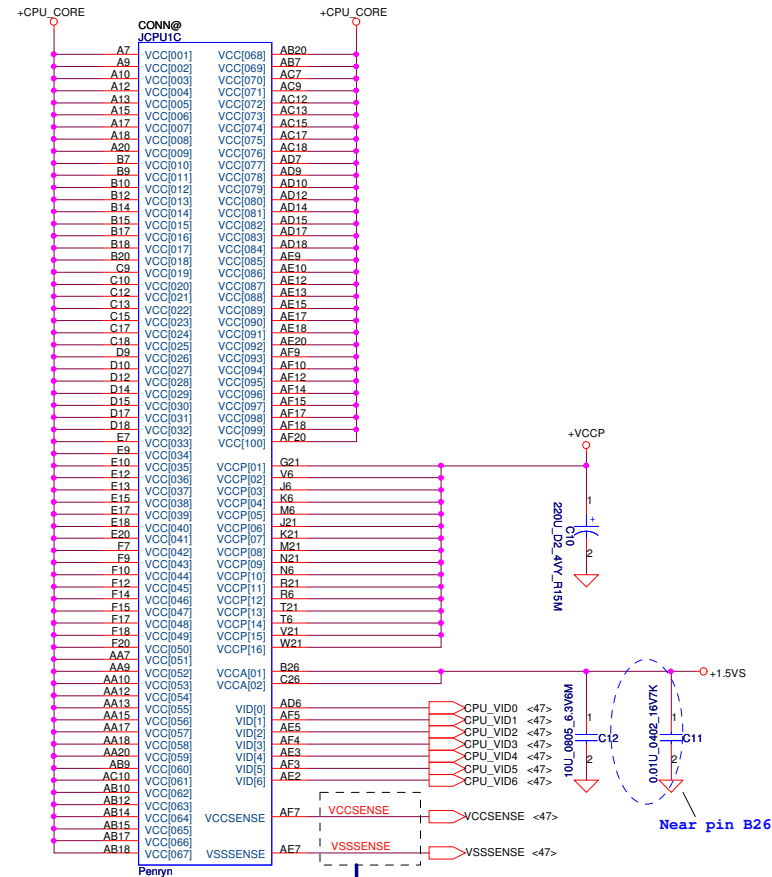


layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

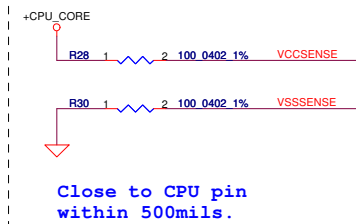
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



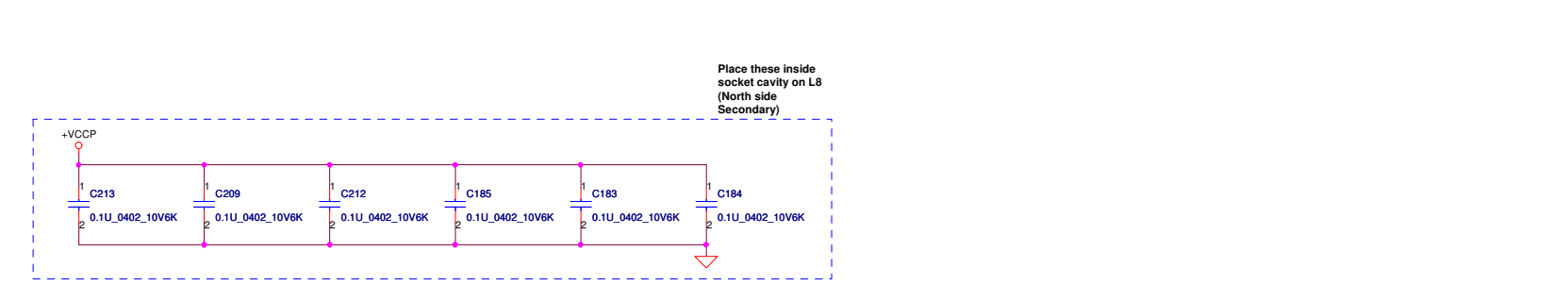
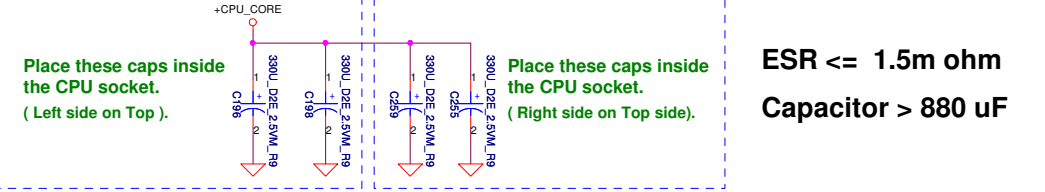
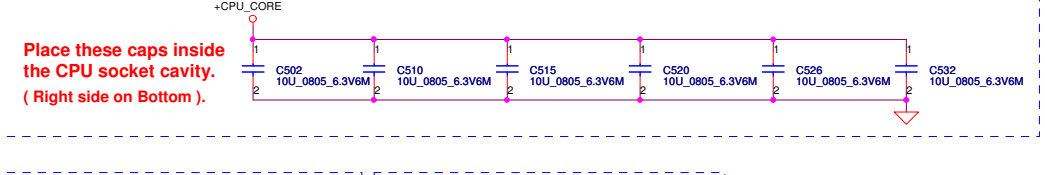
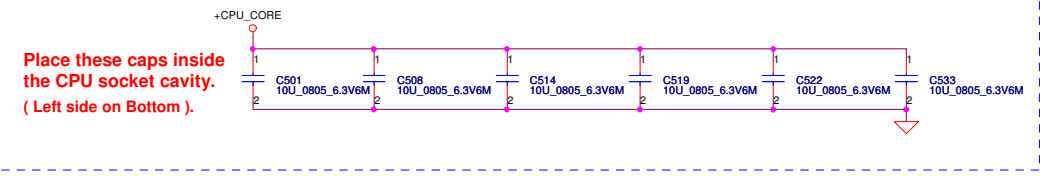
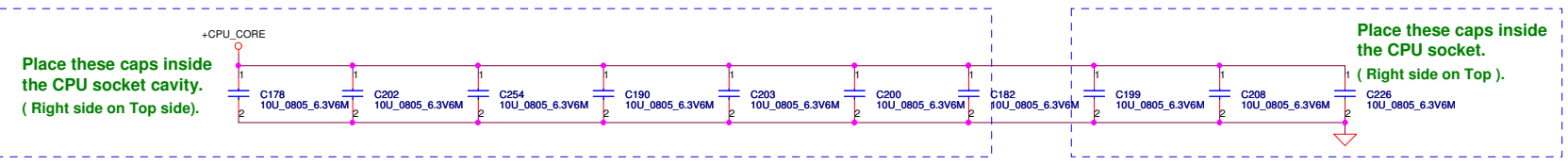
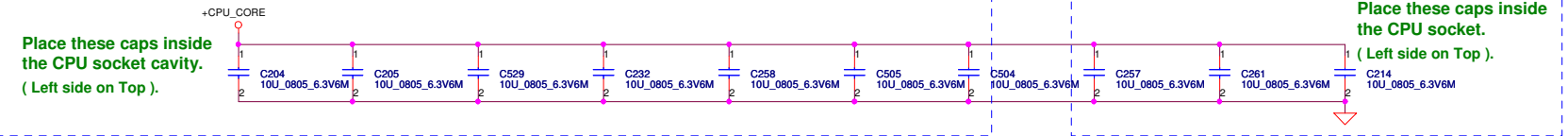
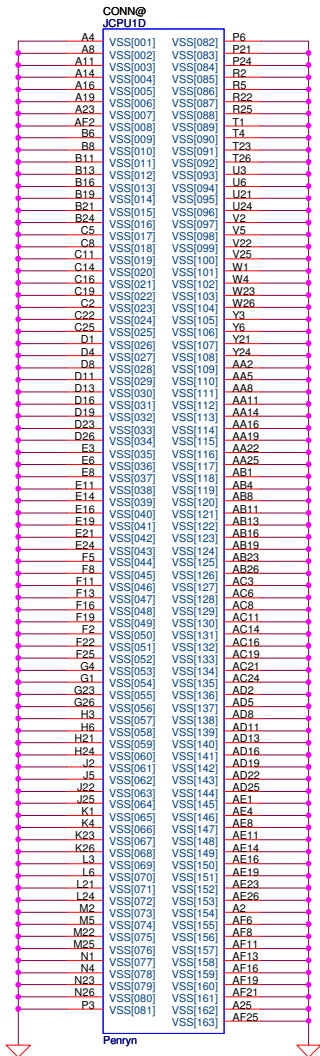
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4

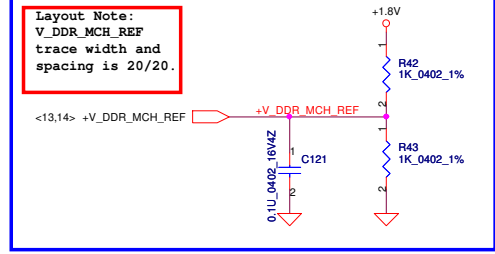
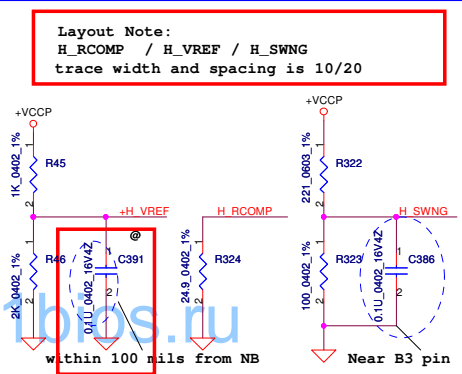
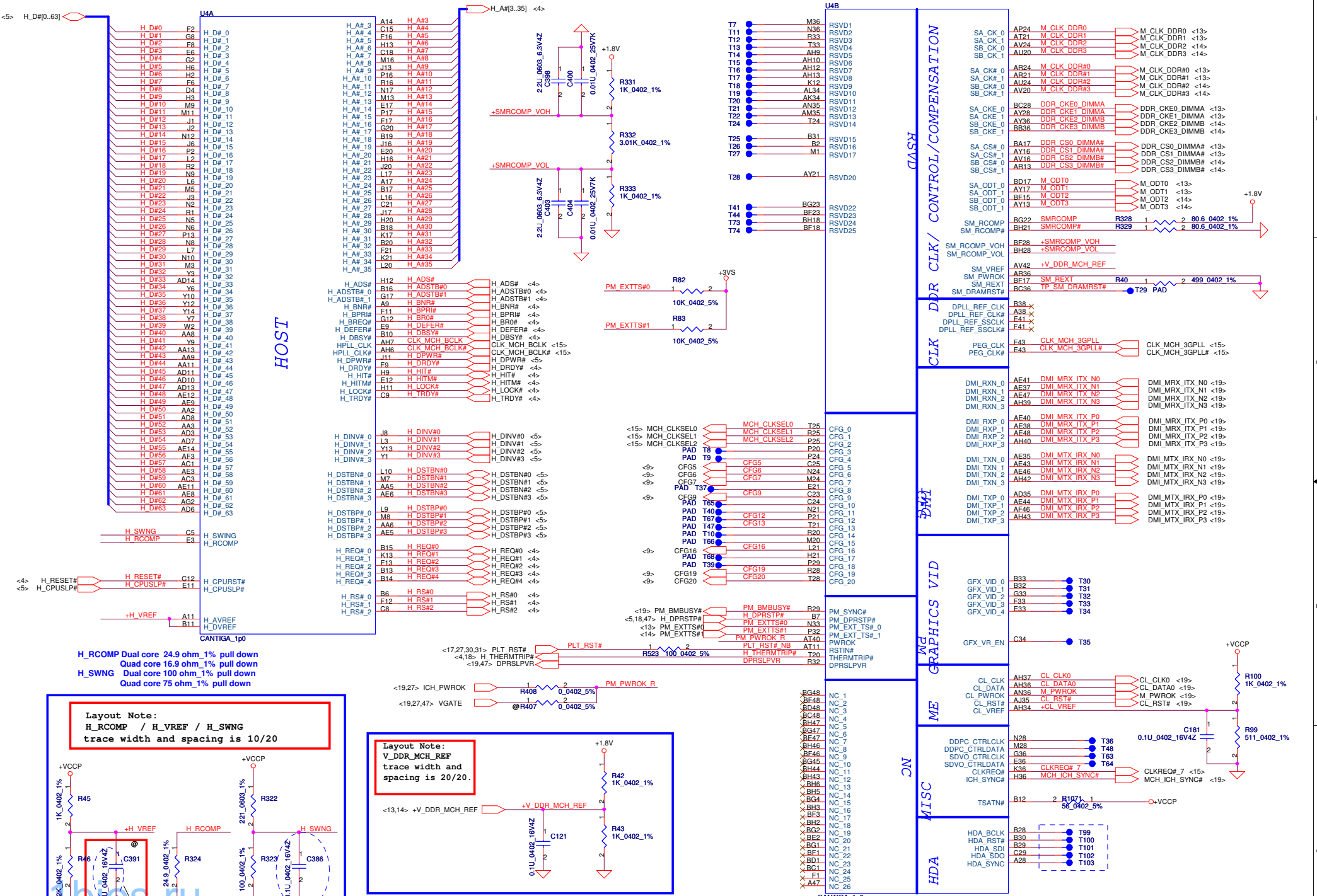


For 8 layer condition Length match within 25 mils. Z0=27.4 ohm The trace width/space/other is 20/7/25.



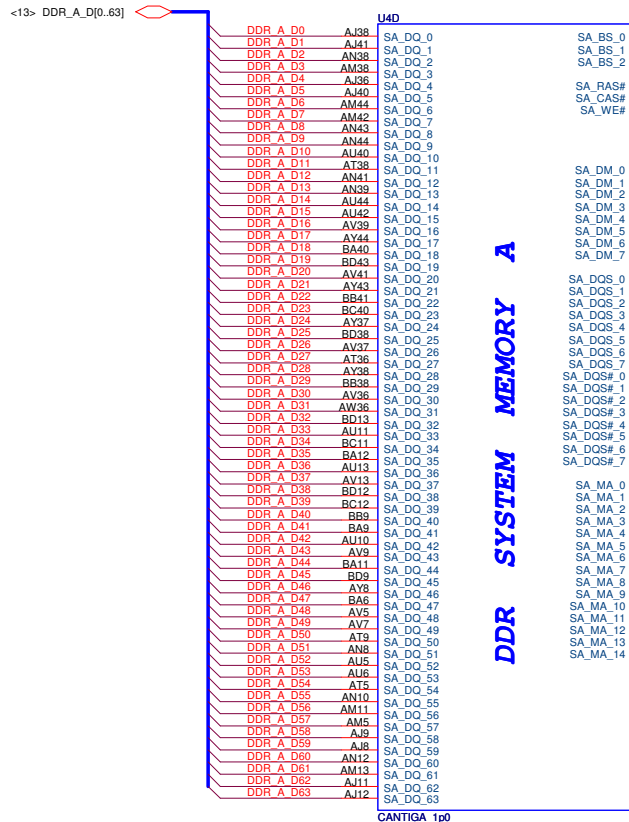
High Frequency Decoupling 10uF 0805 X5R -> 85 degree.



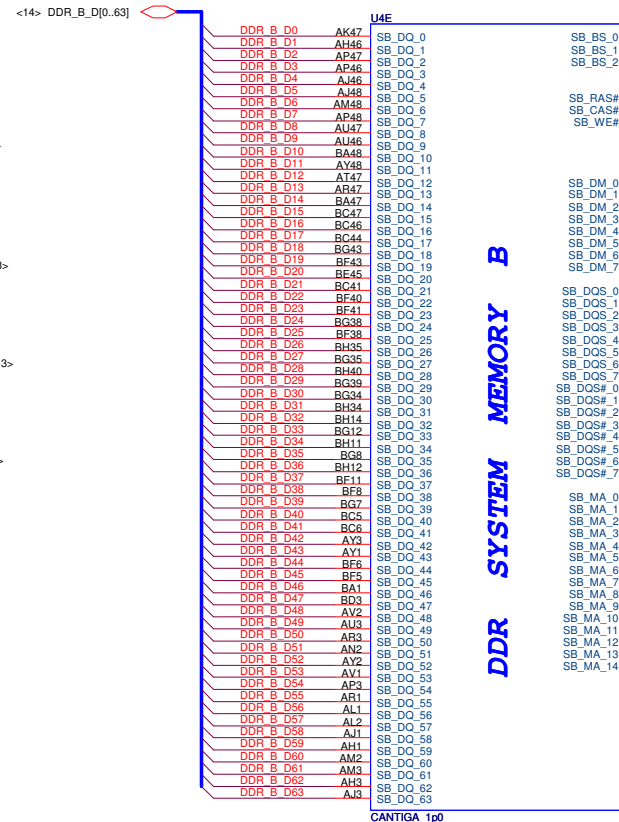


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CRB-no stuff
Checklist-no
10/16



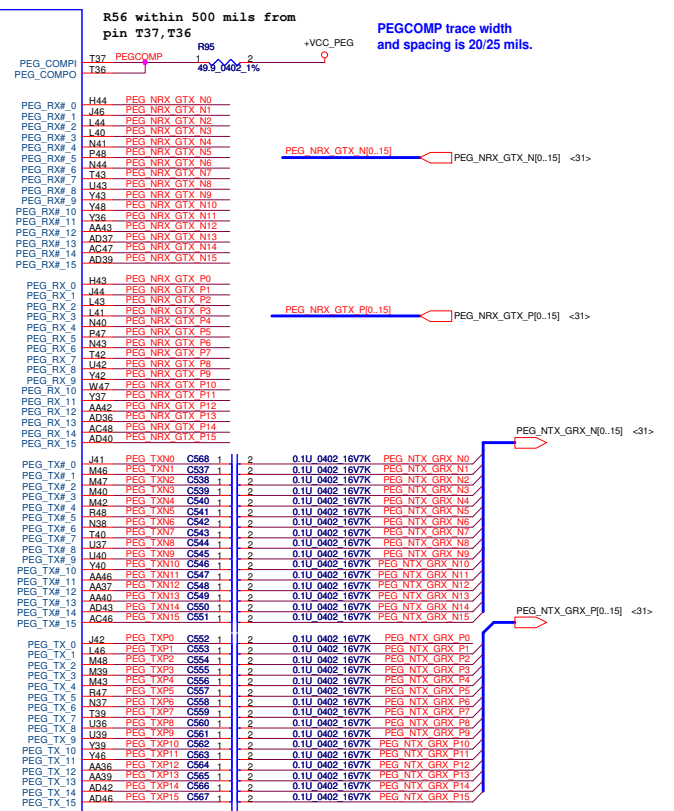
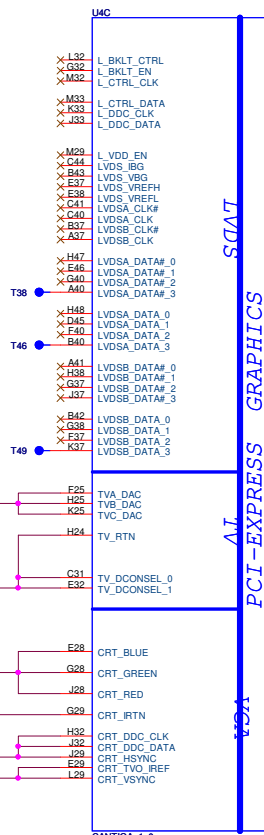
CANTIGA_1p0



CANTIGA_1p0

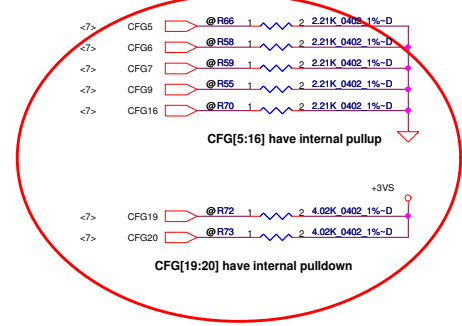
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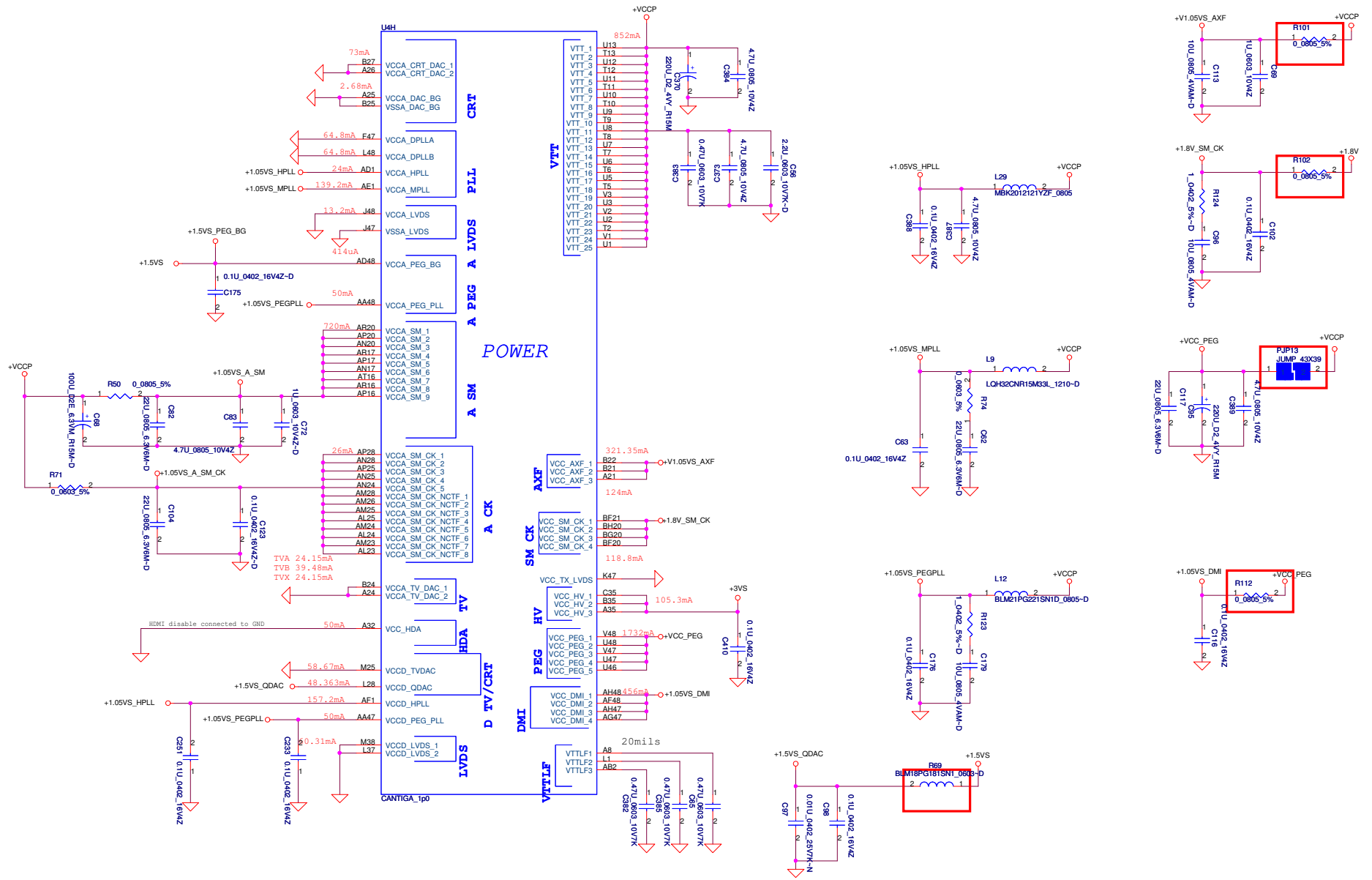
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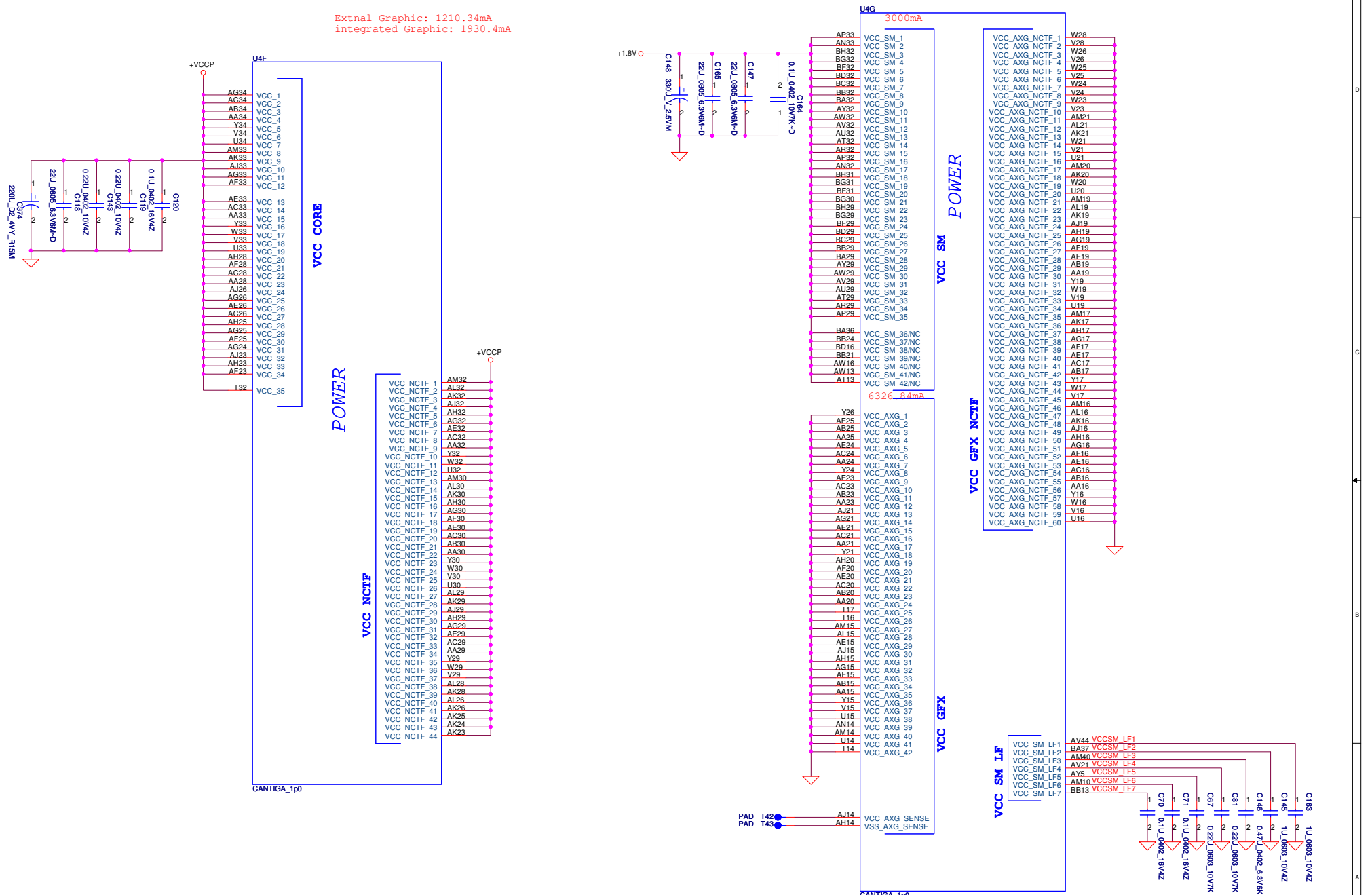
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable * 1 = The ITPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



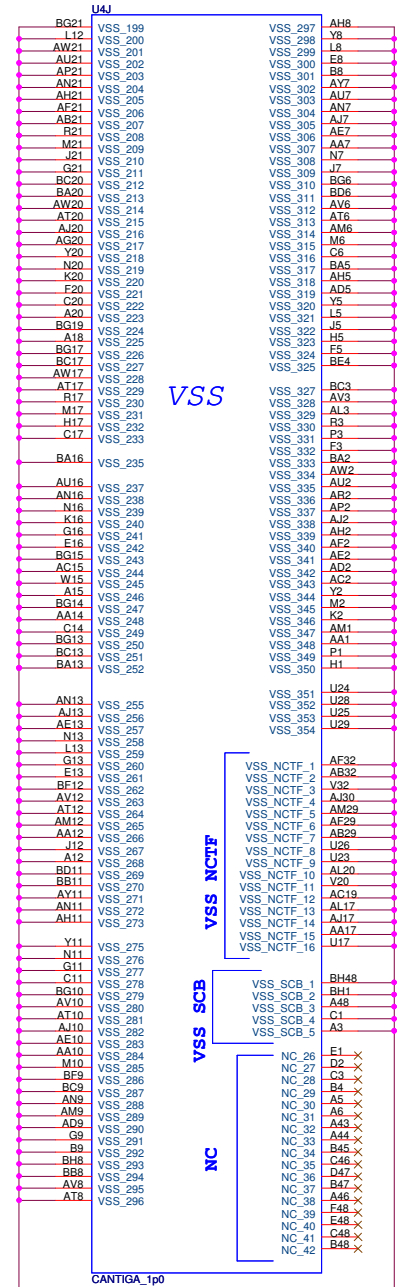
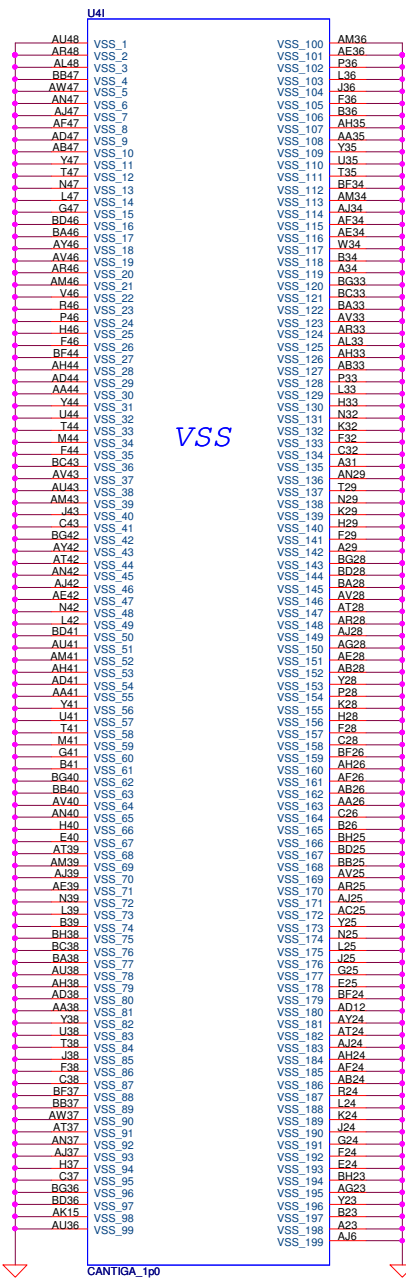


Extenal Graphic: 1210.34mA
 integrated Graphic: 1930.4mA



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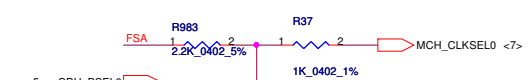
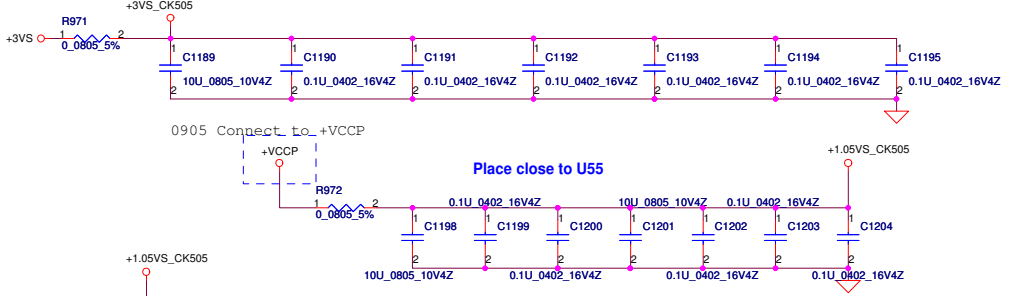
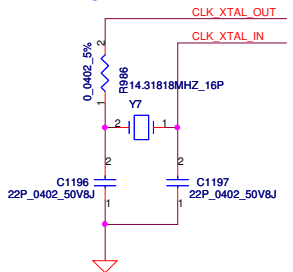
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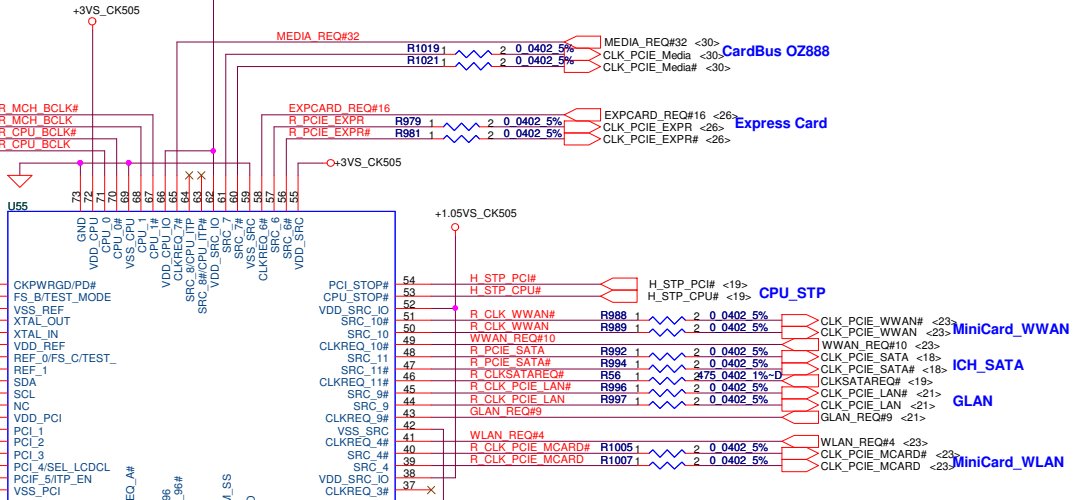
FSC	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0
0	0	1	133	100	33.3	14.318	96.0
0	1	0	200	100	33.3	14.318	96.0
0	1	1	166	100	33.3	14.318	96.0
1	0	0	333	100	33.3	14.318	96.0
1	0	1	100	100	33.3	14.318	96.0
1	1	0	400	100	33.3	14.318	96.0
1	1	1					

Reserved

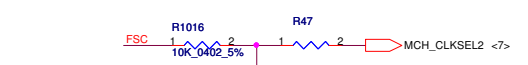
Routing the trace at least 10mil



- NB CPU**
- <7> CLK_MCH_BCLK#
 - <7> CLK_MCH_BCLK
 - <4> CLK_CPU_BCLK#
 - <4> CLK_CPU_BCLK

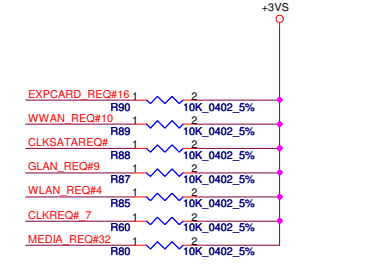
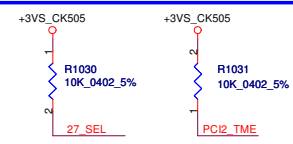


- SB, MINI PCI**
- <19> CK_PWRGD
 - <19> CLK_14M_ICH
 - <13,14,19> ICH_SM_DA
 - <13,14,19> ICH_SM_CLK



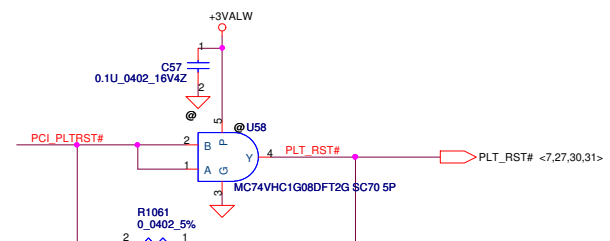
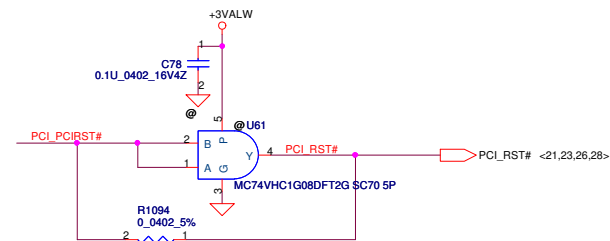
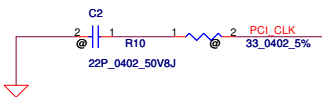
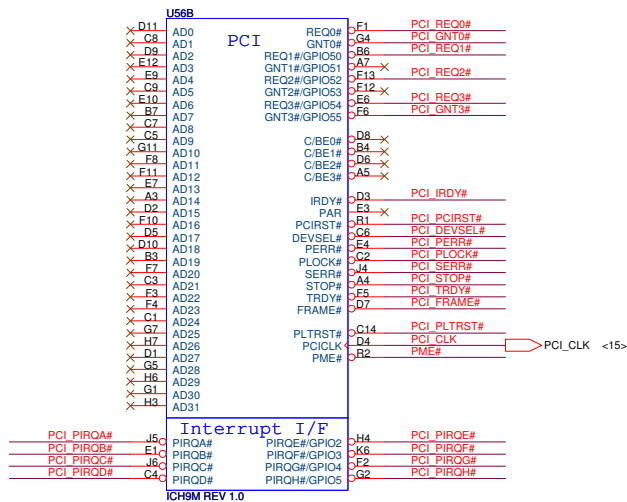
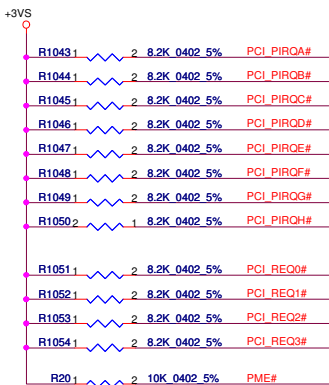
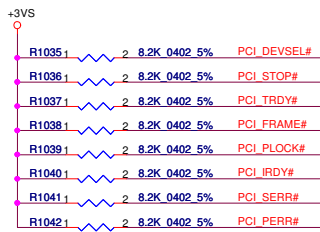
- VGA (Discrete)**
- <31> CLK_PCIE_VGA
 - <31> CLK_PCIE_VGA#

ITP_EN	*0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) *1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed



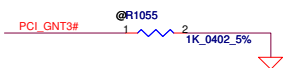
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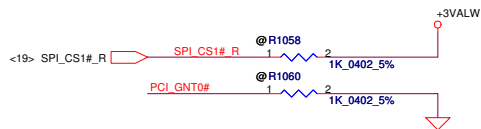


A16 swap override Strap

Low= A16 swap override Enable
High= Default *

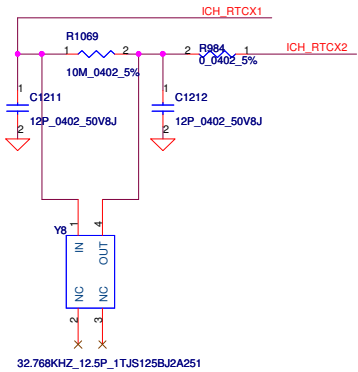
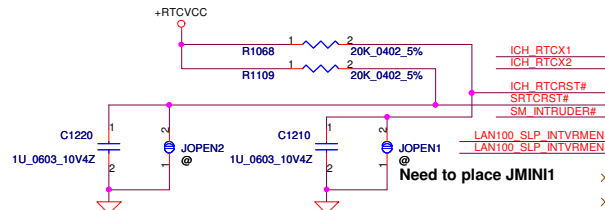
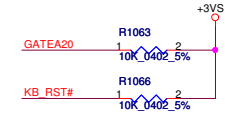
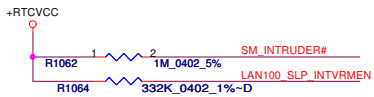


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

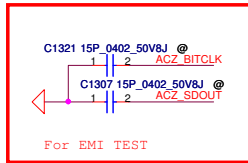


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32.768KHZ_12.5P_1TJS125B,J2A251

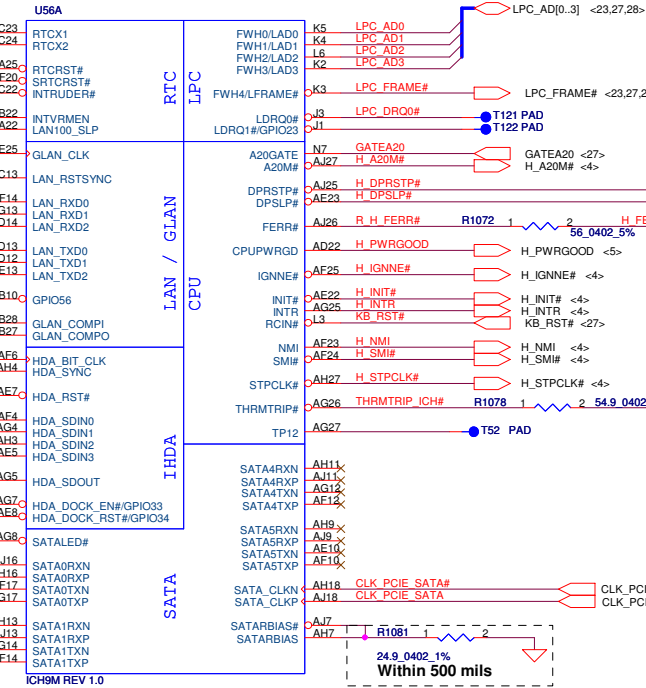
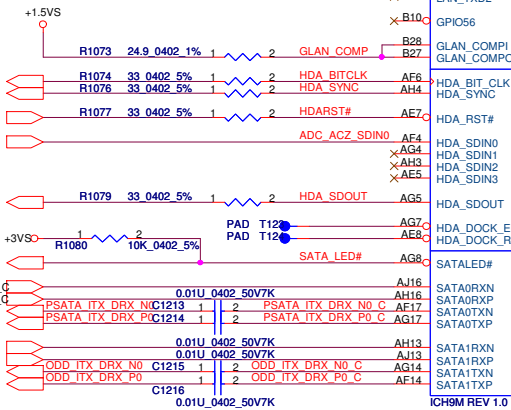


- <24> ACZ_BITCLK
- <24> ACZ_SYNC
- <24> ACZ_RST#
- <24> ADC_ACZ_SDINO
- <24> ACZ_SDOUT

HDD

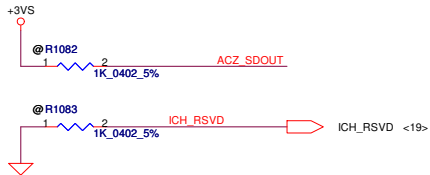
ODD

- <28> SATA_LED#
- <22> PSATA_IRX_DTX_N0_C
- <22> PSATA_IRX_DTX_P0_C
- <22> PSATA_ITX_DRX_N0
- <22> PSATA_ITX_DRX_P0
- <22> ODD_IRX_DTX_N0_C
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- <22> ODD_ITX_DRX_N0
- <22> ODD_ITX_DRX_P0



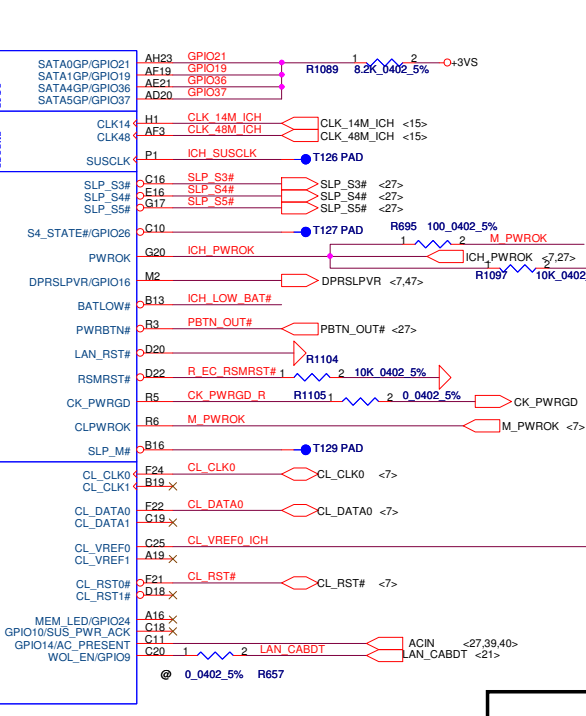
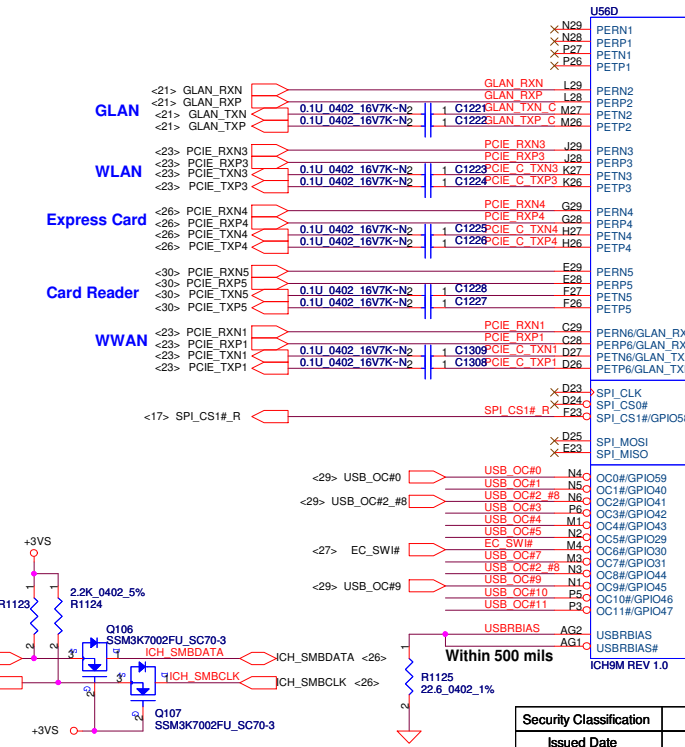
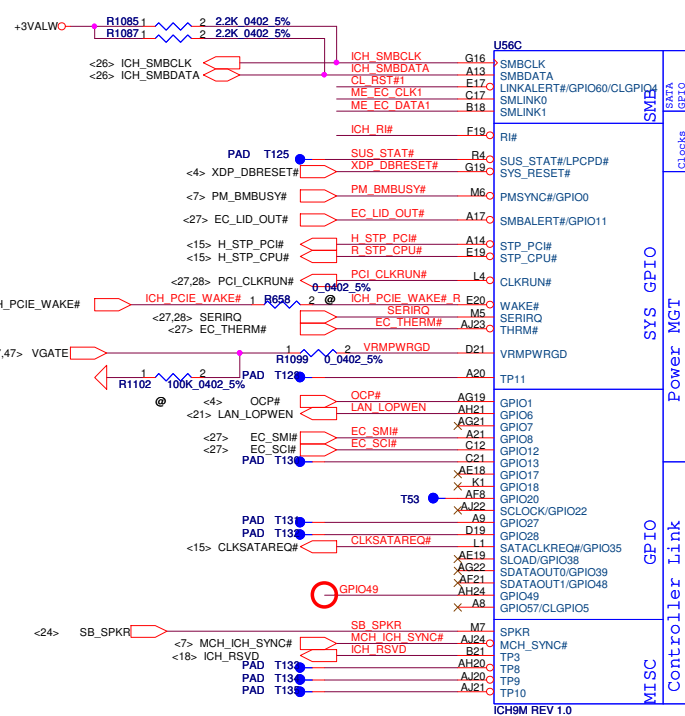
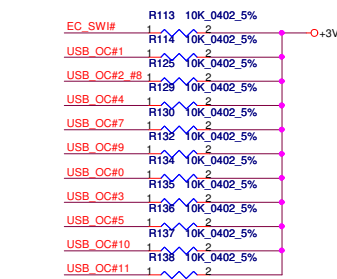
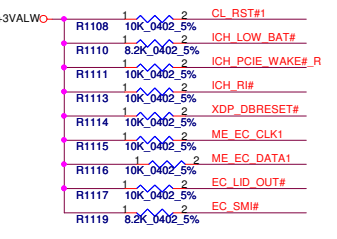
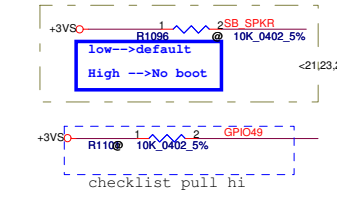
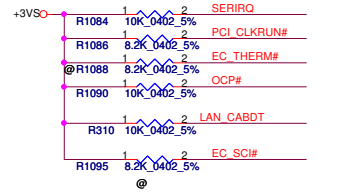
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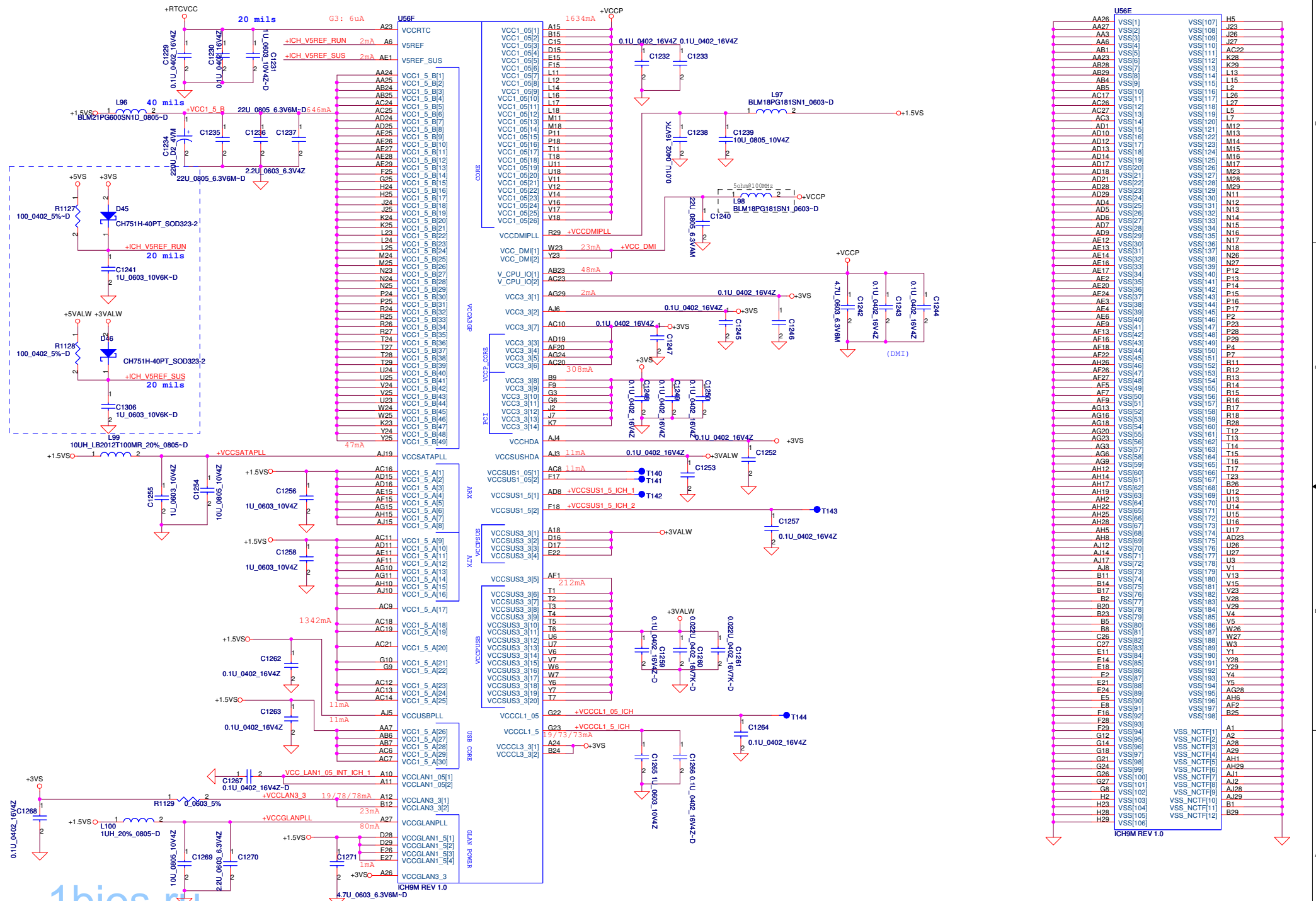
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				CUSTOMER: ICH9(2/4) LAN,HD,IDE,LPC		
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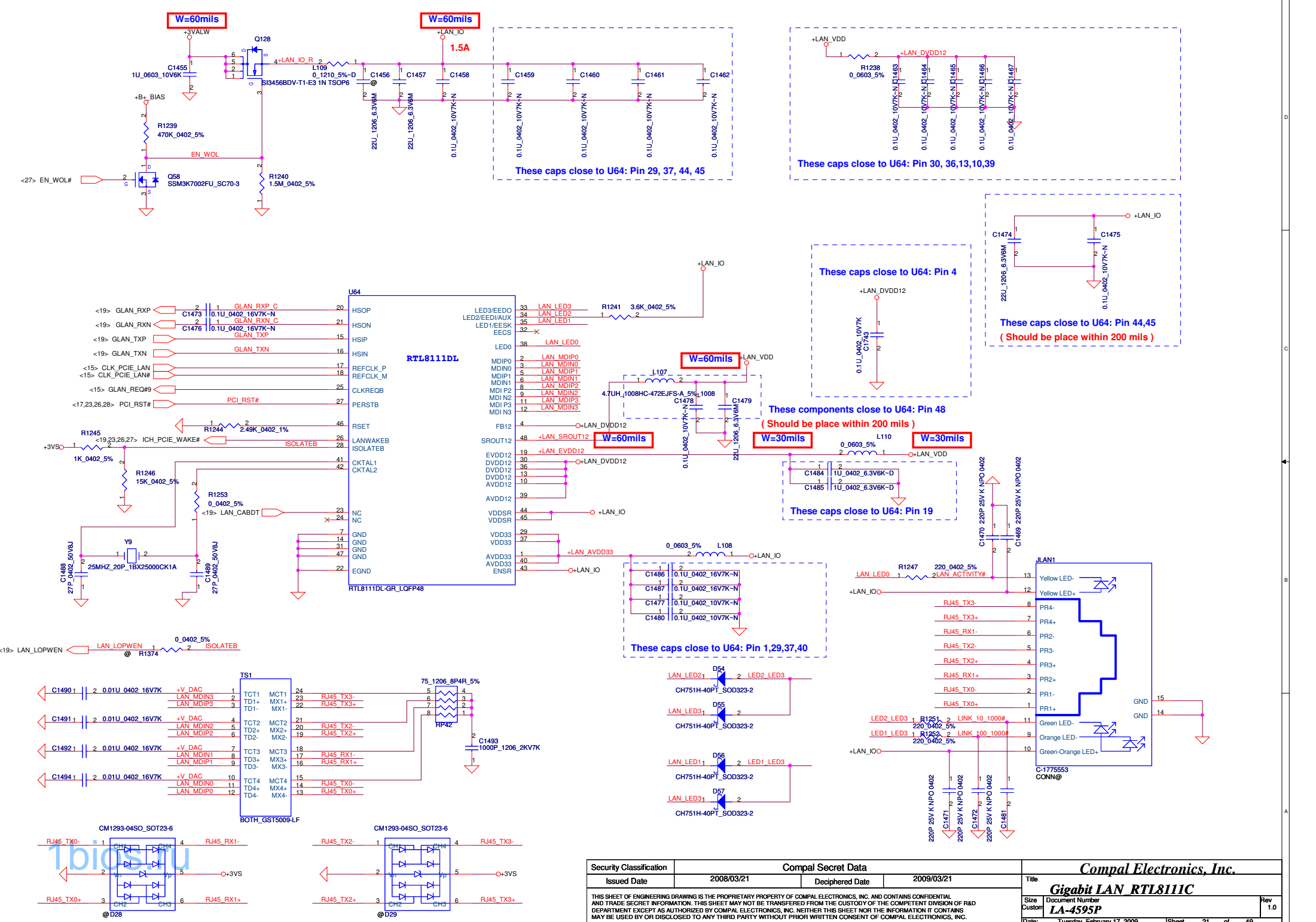




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	AA4	VSS[4]	VSS[110]	J27
	AA5	VSS[5]	VSS[111]	AC22
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	AA7	VSS[7]	VSS[113]	K29
	AA8	VSS[8]	VSS[114]	L13
	AA9	VSS[9]	VSS[115]	L15
	AA10	VSS[10]	VSS[116]	L2
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	AA103	VSS[103]	VSS[209]	
	AA104	VSS[104]	VSS[210]	
	AA105	VSS[105]	VSS[211]	
	AA106	VSS[106]	VSS[212]	

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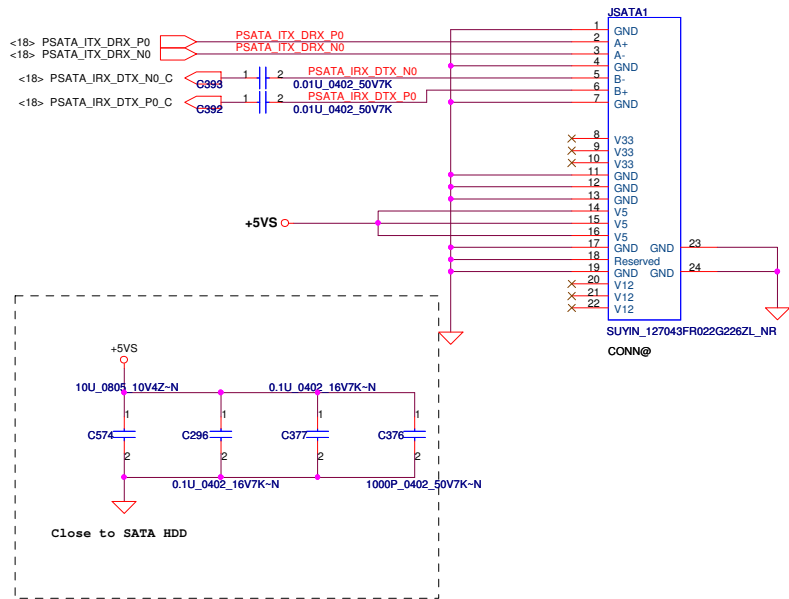


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Issued Date	2008/03/21	Deciphered Date
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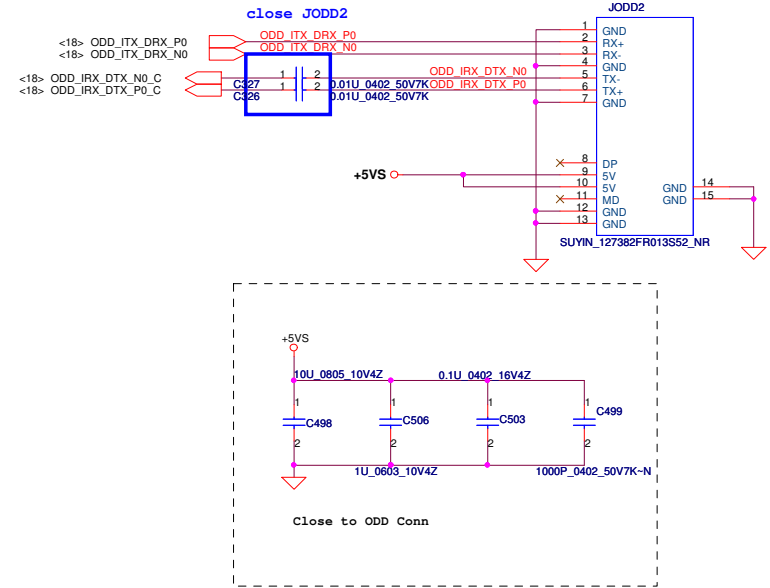
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Gigabit LAN RTL8111C		
Title	Document Number	Rev
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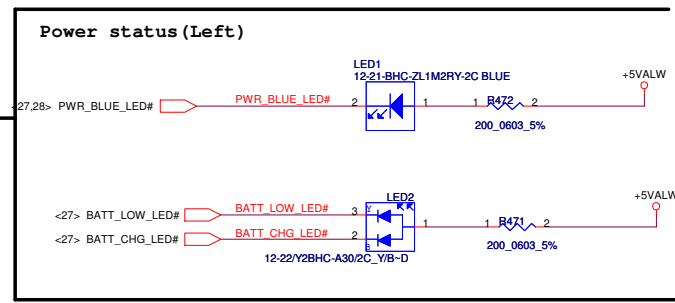
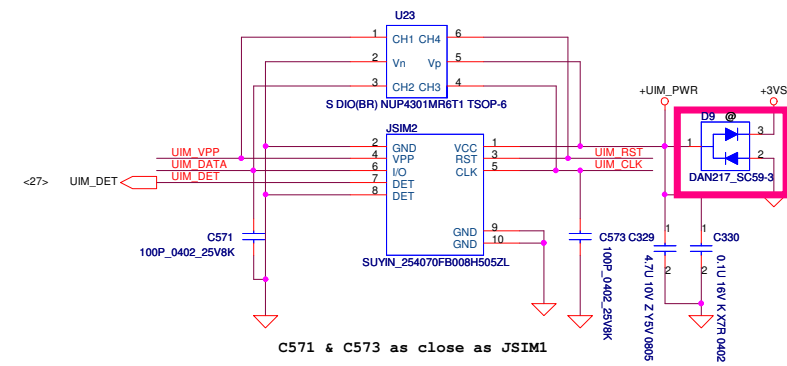
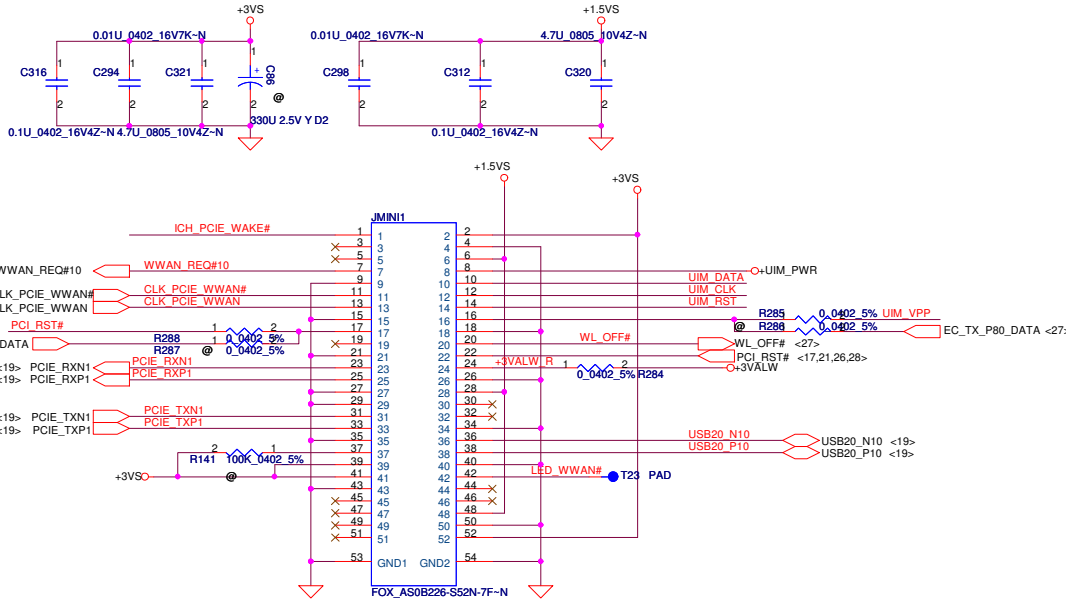


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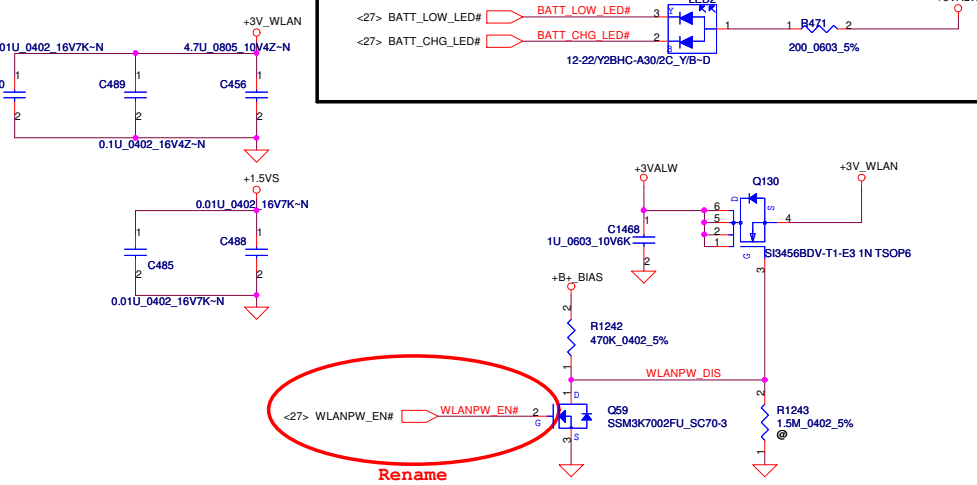
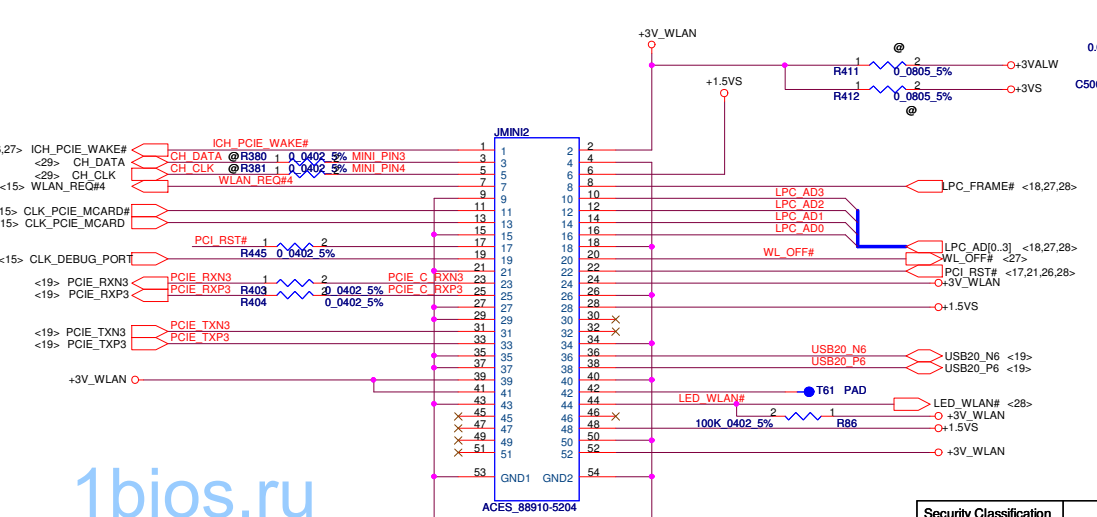


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WWAN

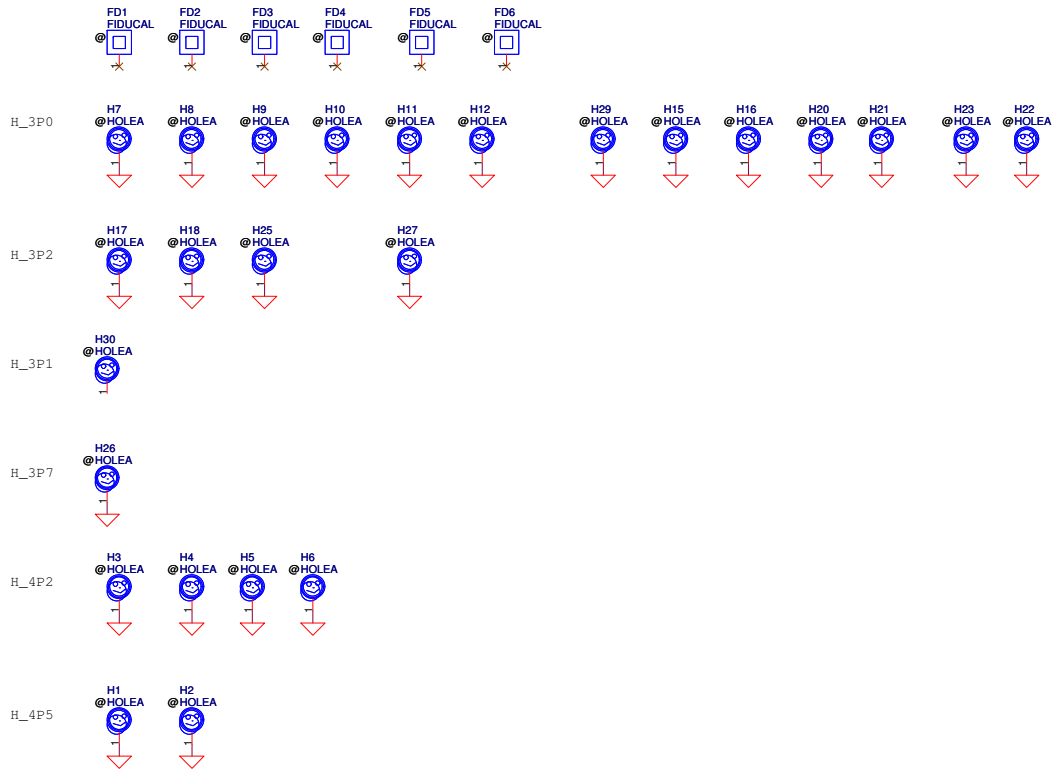


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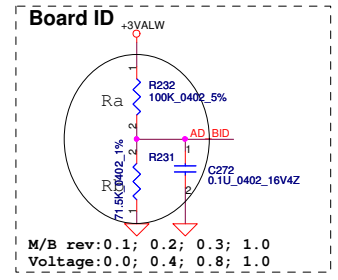
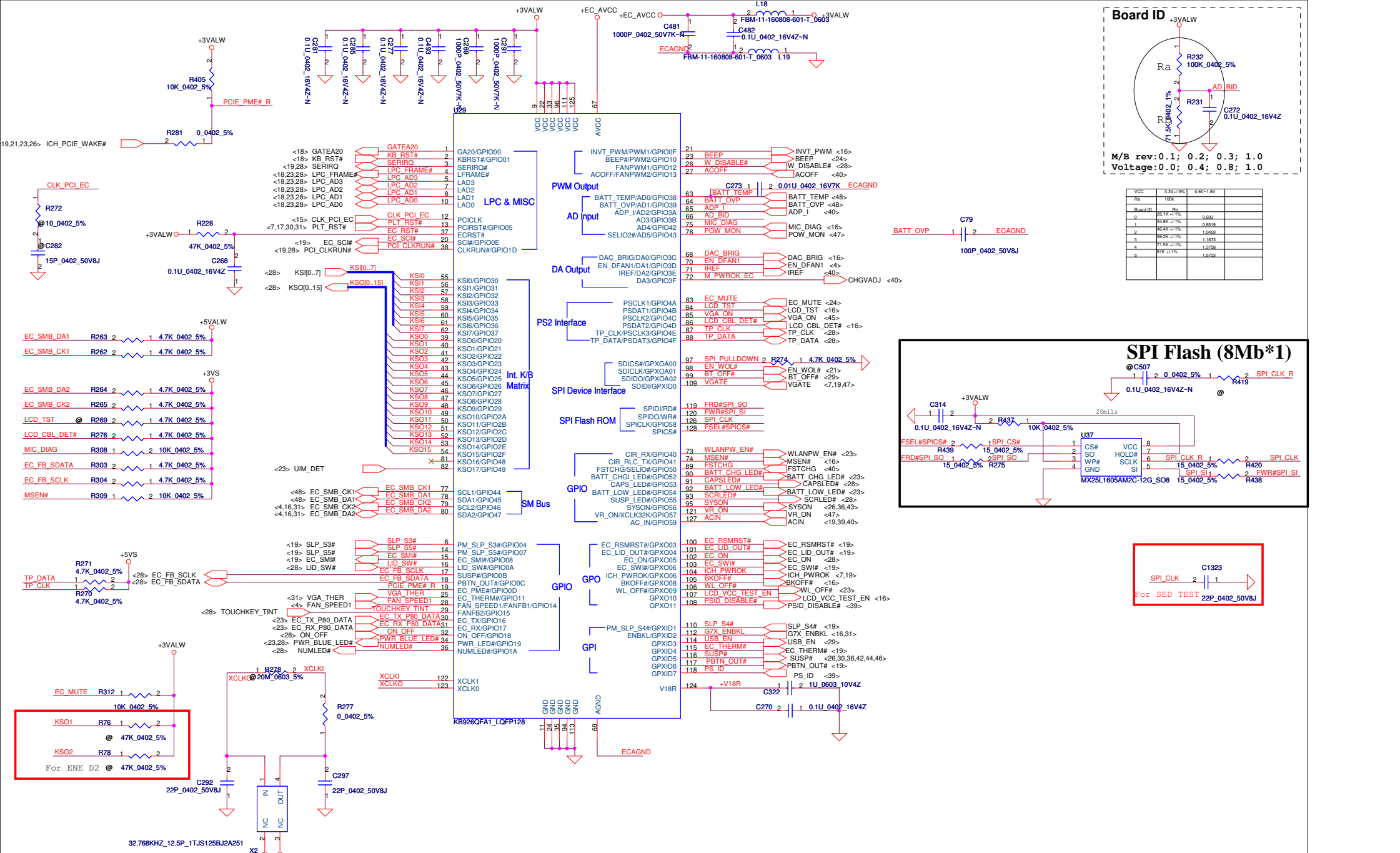


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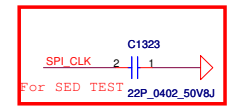
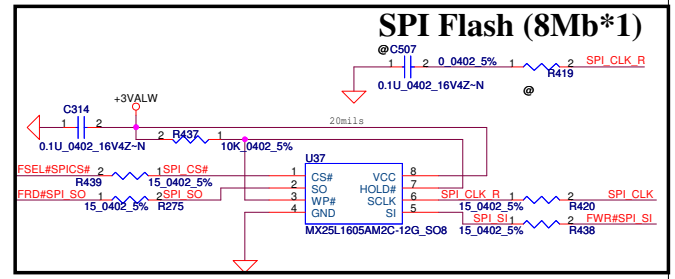


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				Date:	Tuesday, February 17, 2009	Sheet



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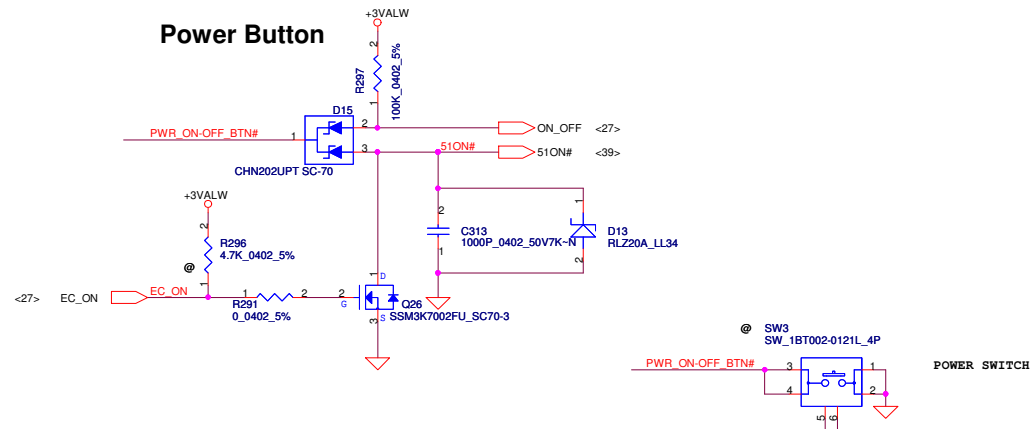
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Rg	10K	10K
Rh	10K	10K
Ri	10K	10K
Rj	10K	10K
Rk	10K	10K
Rl	10K	10K
Rm	10K	10K
Rn	10K	10K
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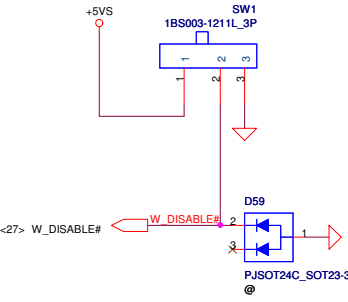
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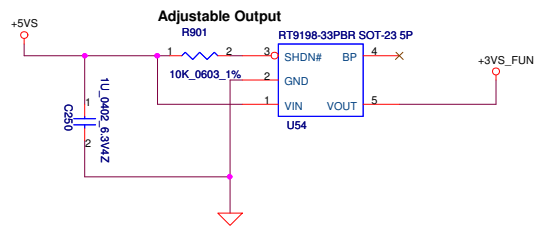
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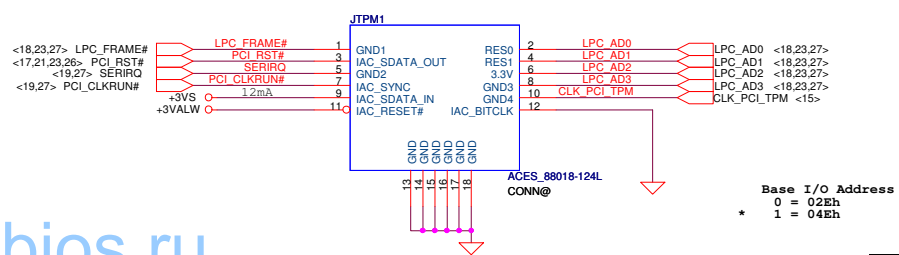
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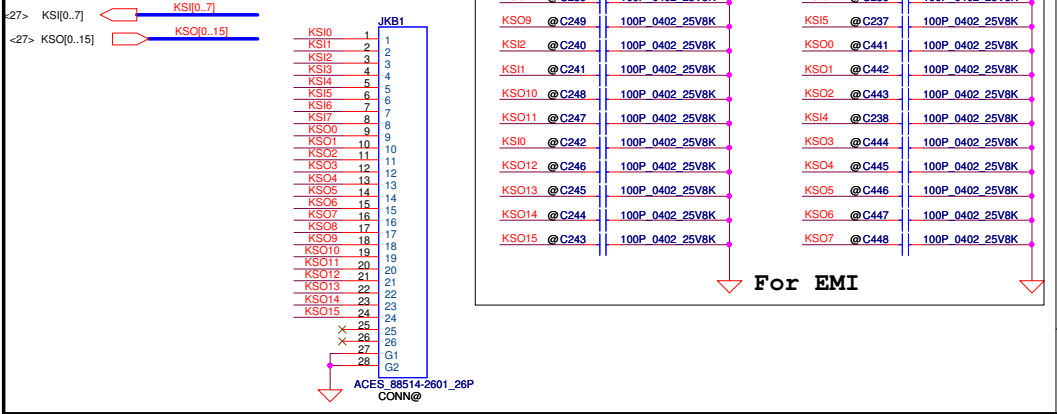


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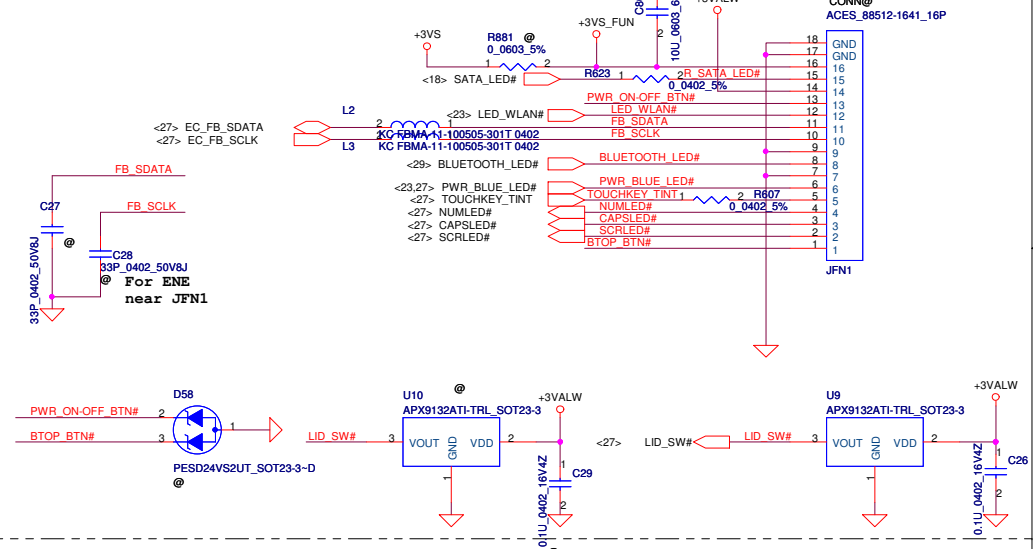


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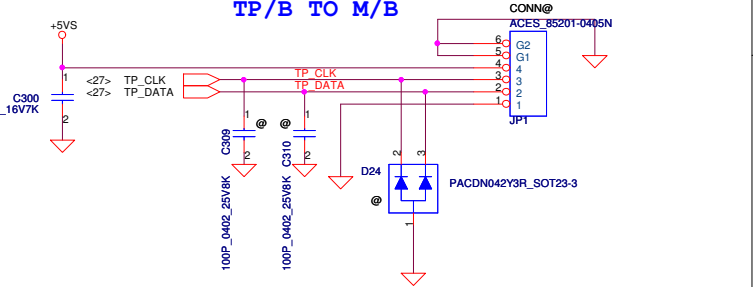
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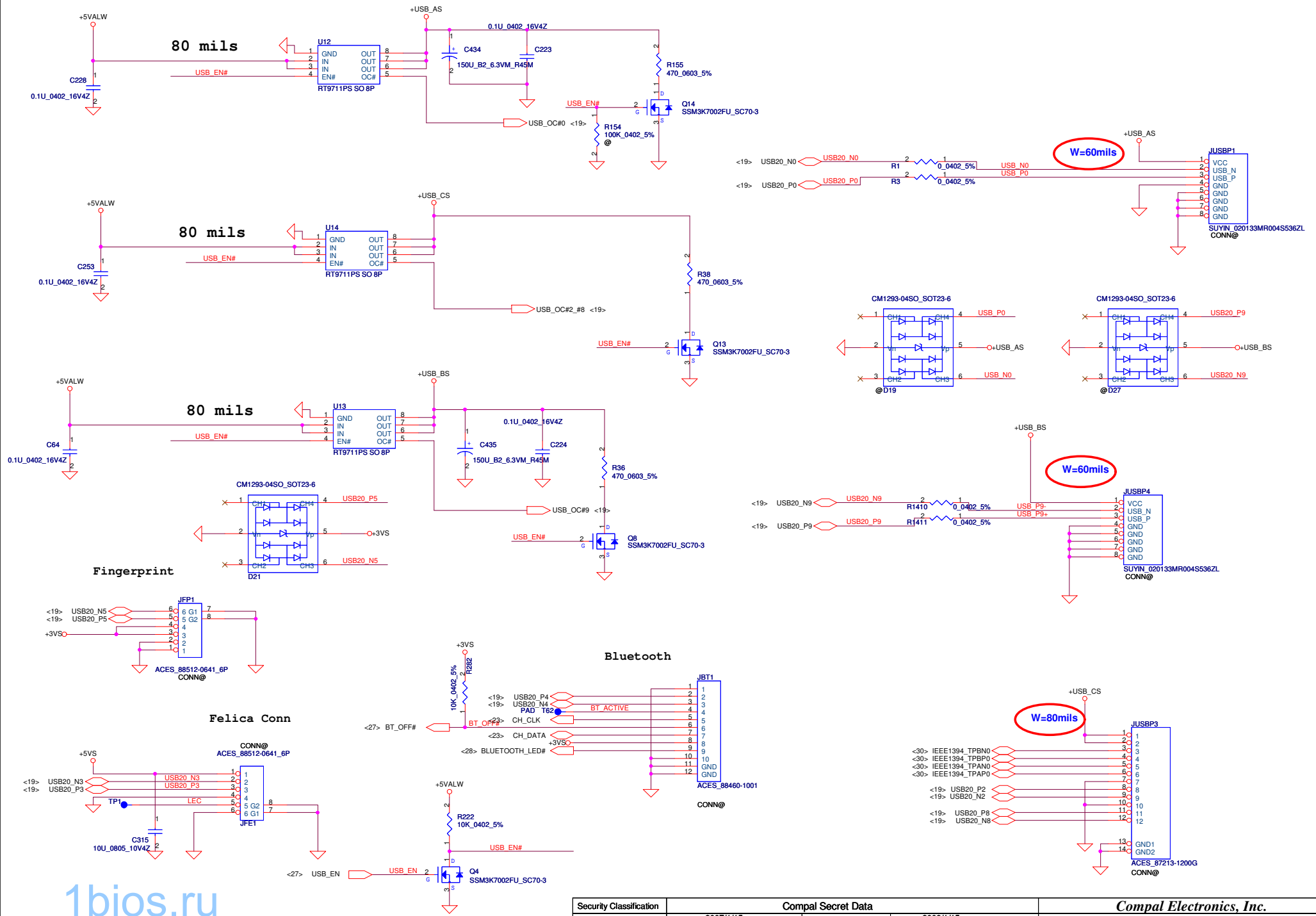
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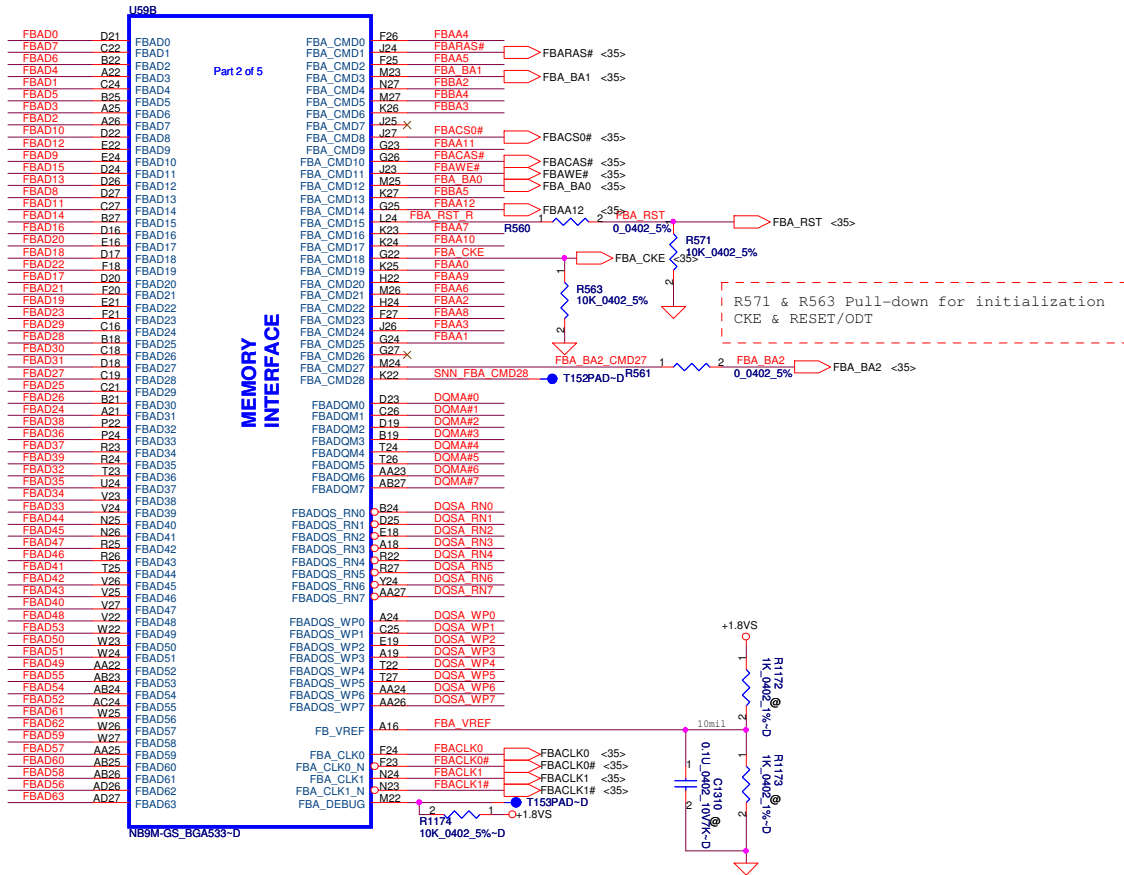
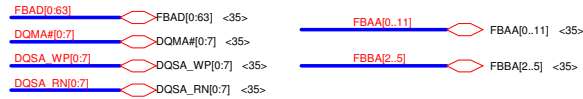


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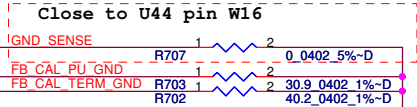
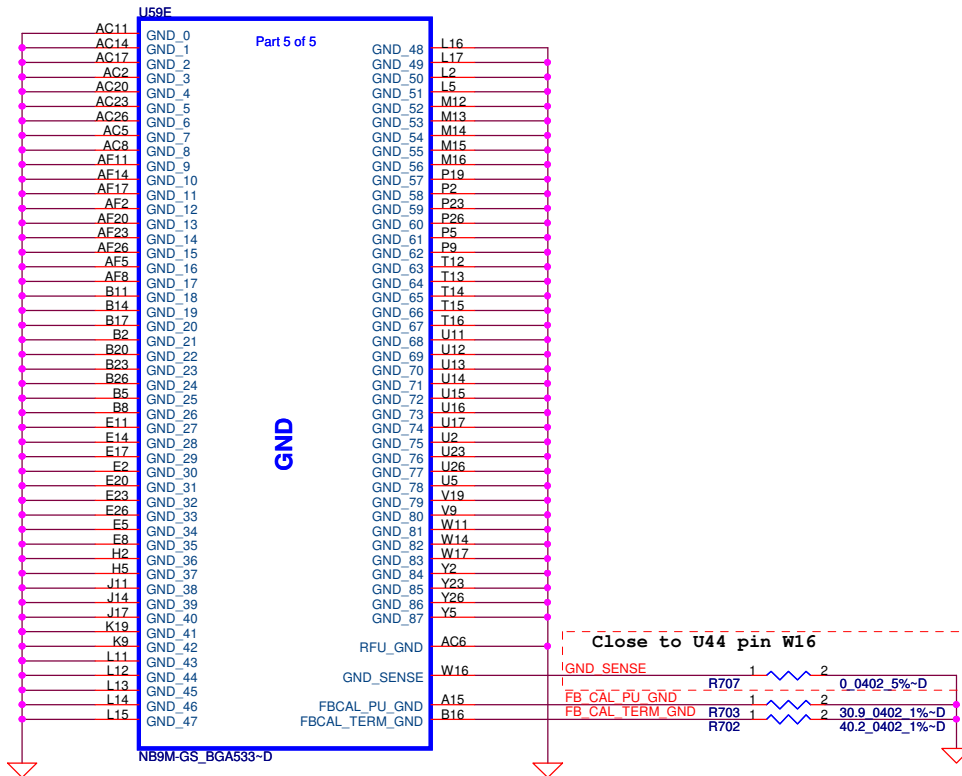
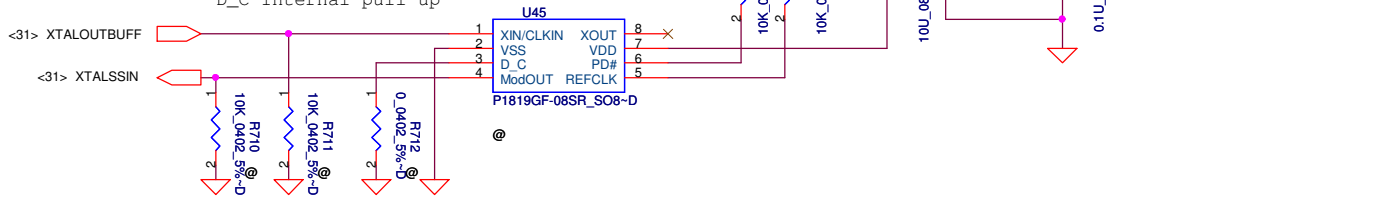


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		NVG98 Memory Interface	
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±0.875% (CENTER)	1

D_C Internal pull up

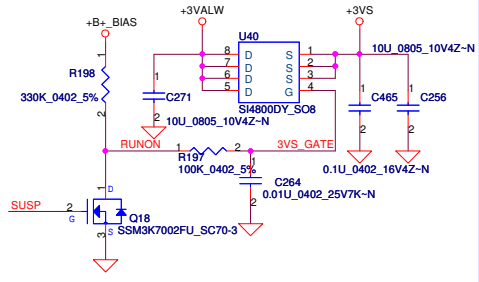


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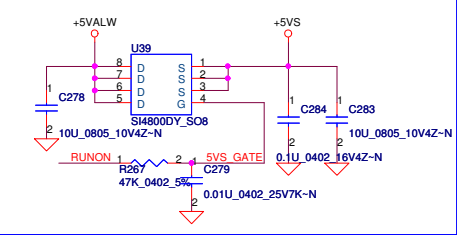
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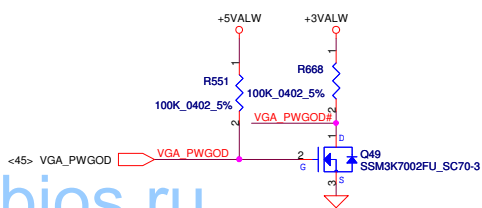
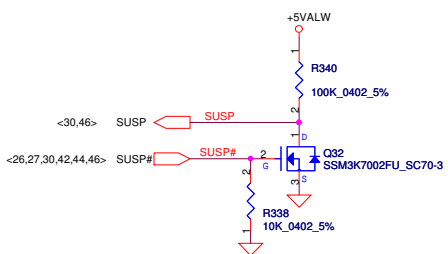
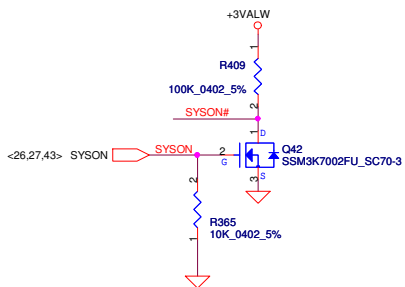
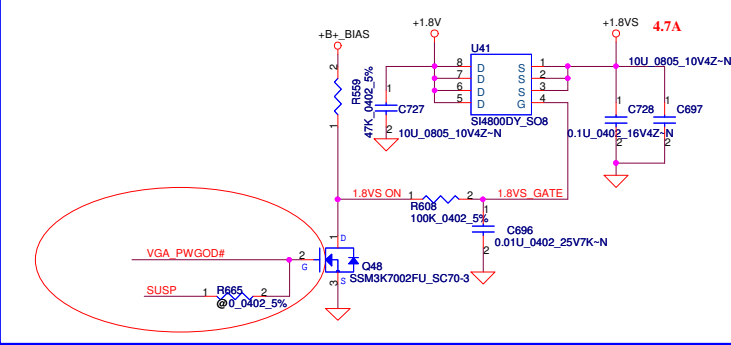
+3VALW to +3VS Transfer



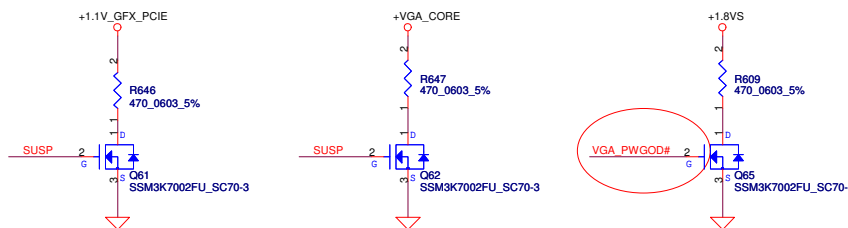
+5VALW to +5VS Transfer



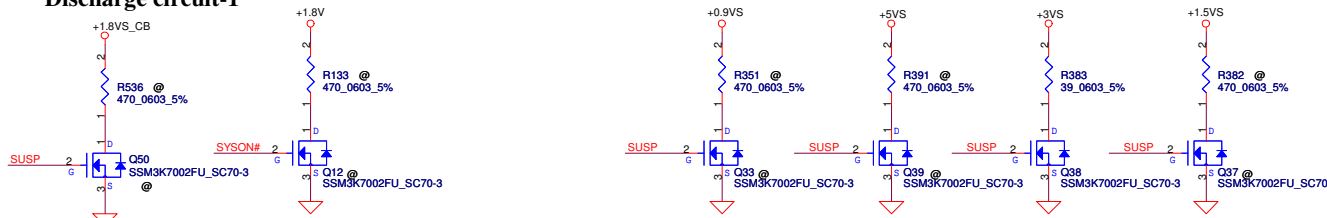
+1.8V to +1.8VS Transfer



VGA Discharge circuit



Discharge circuit-1

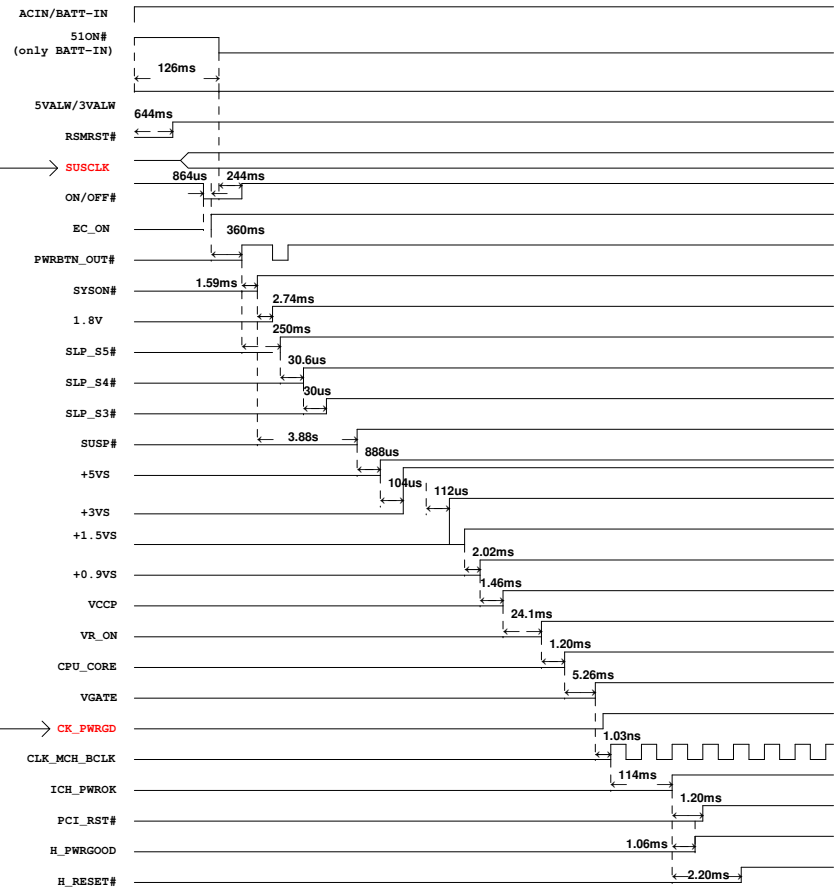


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SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

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				Date:	Tuesday, February 17, 2009	Sheet 36 of 49

KAL80 POWER UP SEQUENCE



Suspend Clock (32KHz)
ICH9 internal clock

This signal is asserted high when both SLP_S5# and VRMPWRGD are high

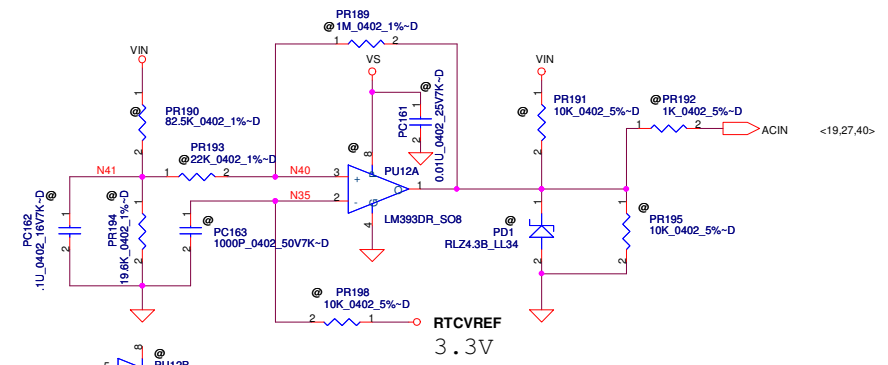
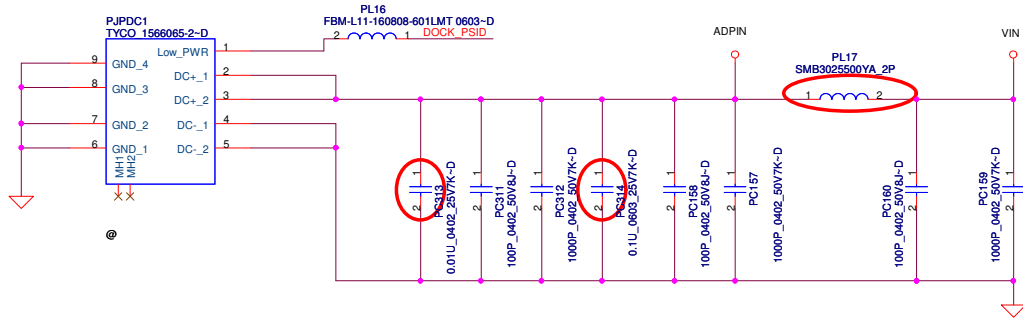
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Version Change List (P. I. R. List)

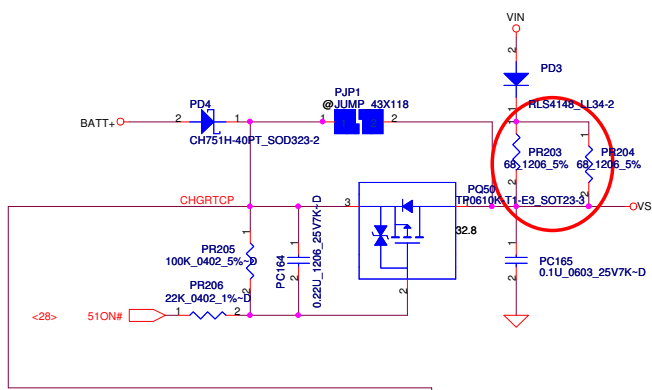
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1		Swap SW1	12/02	EE			
2		Update JUSBP3 pin define	12/02	EE			
3		R405 POP	12/02	EE			
4		U50 unPOP & R1190 POP	12/02	EE			
5		WWAN move to PORT6	12/02	BIOS			
6		Add C1391 & C1392	12/02	Nvidia	LVDS single channel issue	Short U59.V2 & U59.V3. Add C1391 C1392 for IFPB_IOVDD	
7		Swap JSPK1 Pin	12/02	EE			
8		R101	12/04	EE	Change to 0805		
9		TPM Con	12/04	EE	Modify to Con		
10		R76 & R78 UnPOP	12/09	EE	EC update to Rev:C1		
11		Q7 & Q9	12/09	EE	Update Q7 & 9 footprint		
12		R658 & R281	12/11	EE	R685 UnPOP & R281 UnPOP for wake on LAN		
13		U89 & WLANPW_DIS#	12/11	EE	Add U89 for wake on LAN. Add WLANPW_DIS# of EC		
14		C1484 & C1485	12/11	EE	C1484 & C1485 modify to 1U form LAN vendor		
15		Update PW schematic	12/12	PW			
16		C260 & C252	12/15	EE	IDT ask UnPop		
17		Add D29 D28	12/15	ESD	ESD for LAN		
18		U9 Pop & U10 UnPop	12/15	ME			
19		Wake On WLAN	12/16	EE	Modify WLANPW_DIS# circuit		
20		Add T49 & T53	12/16	Layout			
21		C696	12/16	EE	Update PN		
22		WLANPW_DIS#	12/17	EE	Move WLANPW_DIS# to EC-GPIO40 and Del BTOP_ON		
23		L42 & L43	12/17	EMI	L42 & L43 update to Bead from 0 ohm		
24		C3 C4 C6 C14 C17	12/17	EMI	POP 100 P		
25		R69	12/17	EE	Update to Bead drom 100 ohm		
26		Cap	12/17	EMI	Add C1469 C1470 C1471 C1472 C1481 R81		
27		D21 D12 D17	12/17	ESD	ESD ask POP		
28		Update PW schematic	12/17	PW			
29		Update Q128 Q130 PN	12/18	EE			
30		Update Board ID	12/18	EE	R231		
31		Add U16 for OZ888	12/18	EE			
32		C1323 POP	12/18	EE	For Kepar		
33		R1421 UnPOP	12/22	EE			
34		C292 C297	12/22	EE	Modify to 22P form 18P (Crystal Vendor)		
35		C1745 C1749	12/22	EE	Modify to 18P form 10P(C1749) and 15P from 10P(C1745)(Crystal Vendor)		
36		C1211	12/22	EE	Modify to 12P form 15P (Crystal Vendor)		
37		R1423 & R1422	01/07	EE	Add for O2		
38		L6 & R1190	01/10	EE	Change to 0805		
39		Modify LDO to +5VS	01/12	EE			
40		Add C80 & D59 & D60	01/12	EE			
41		Add components of JHP1	01/13	EE	For vendor		
42		R360 & R361	01/19	EE	Update R360 & R361 to 56 ohm		
43		U37	01/19	EE	Update U37 to SA00001KN10		
44		R231	01/19	EE	Update Board ID		

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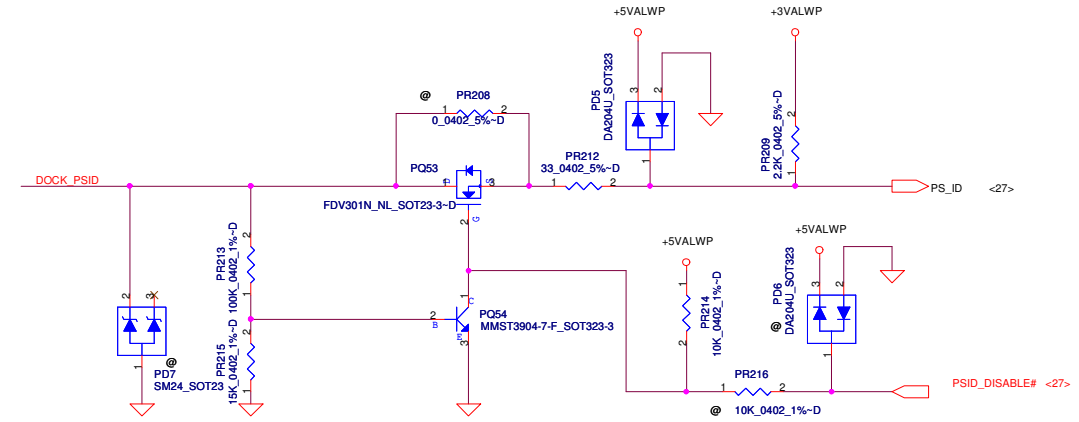
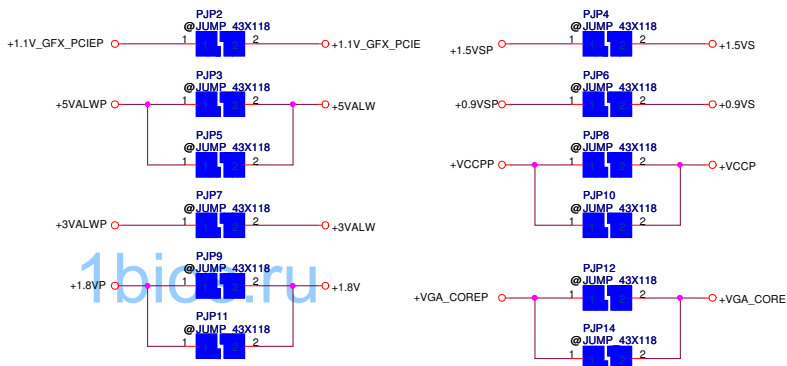
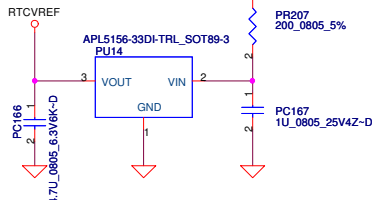
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	EEW PIR-1	
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Vin Detector			
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

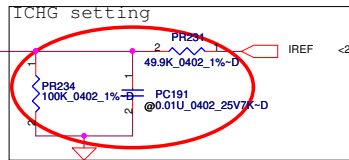
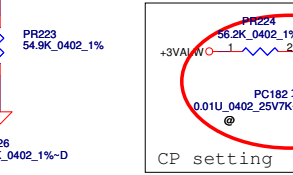
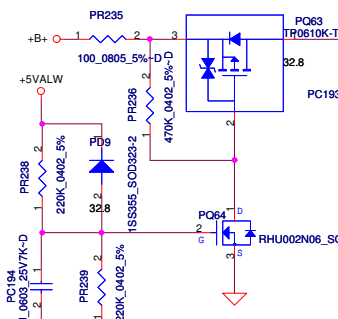
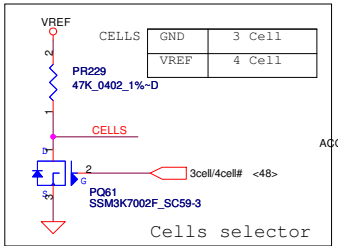


3.3V



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Issued Date	2006/10/1	Deciphered Date	2007/5/01	DCIN / Vin Detector	
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				Date: Tuesday, February 17, 2009	Sheet 39 of 49

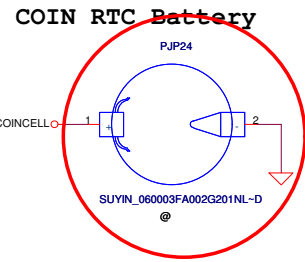
90W adapter
 $I_{charge} = (V_{rset}/V_{vdac}) * (0.1/PR34) = 3.34A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR17) = 4.27A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



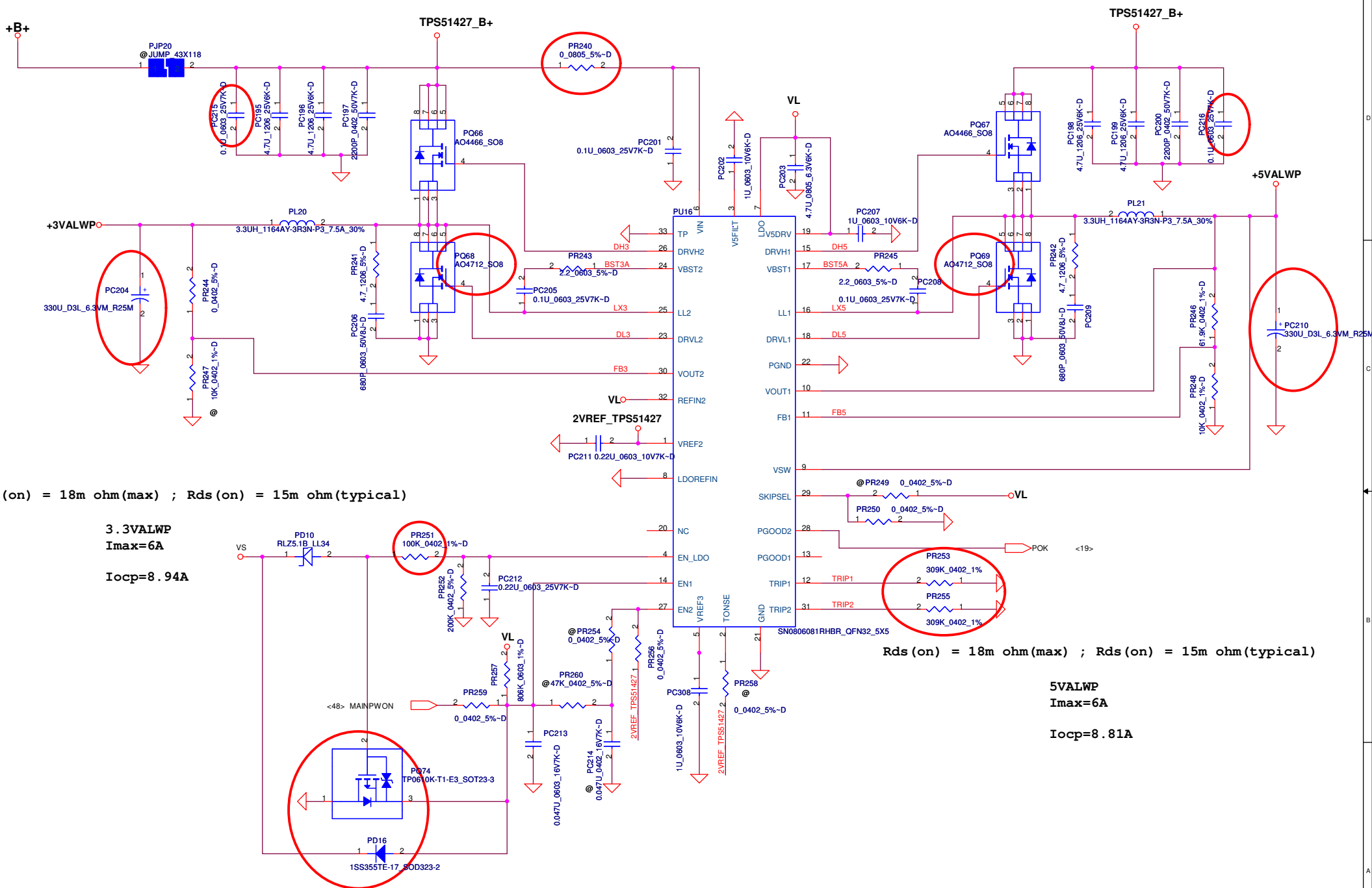
CHGVADJ	Pre Cell
3.282V	4.35V
0V	4V

IREF	Current
2.968V	3A

$CHGVADJ = 9.3755 * (\text{charger voltage per cell} - 4)$
 $PR53 = 210K$
 CHGVADJ要接到EC DA pin



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Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

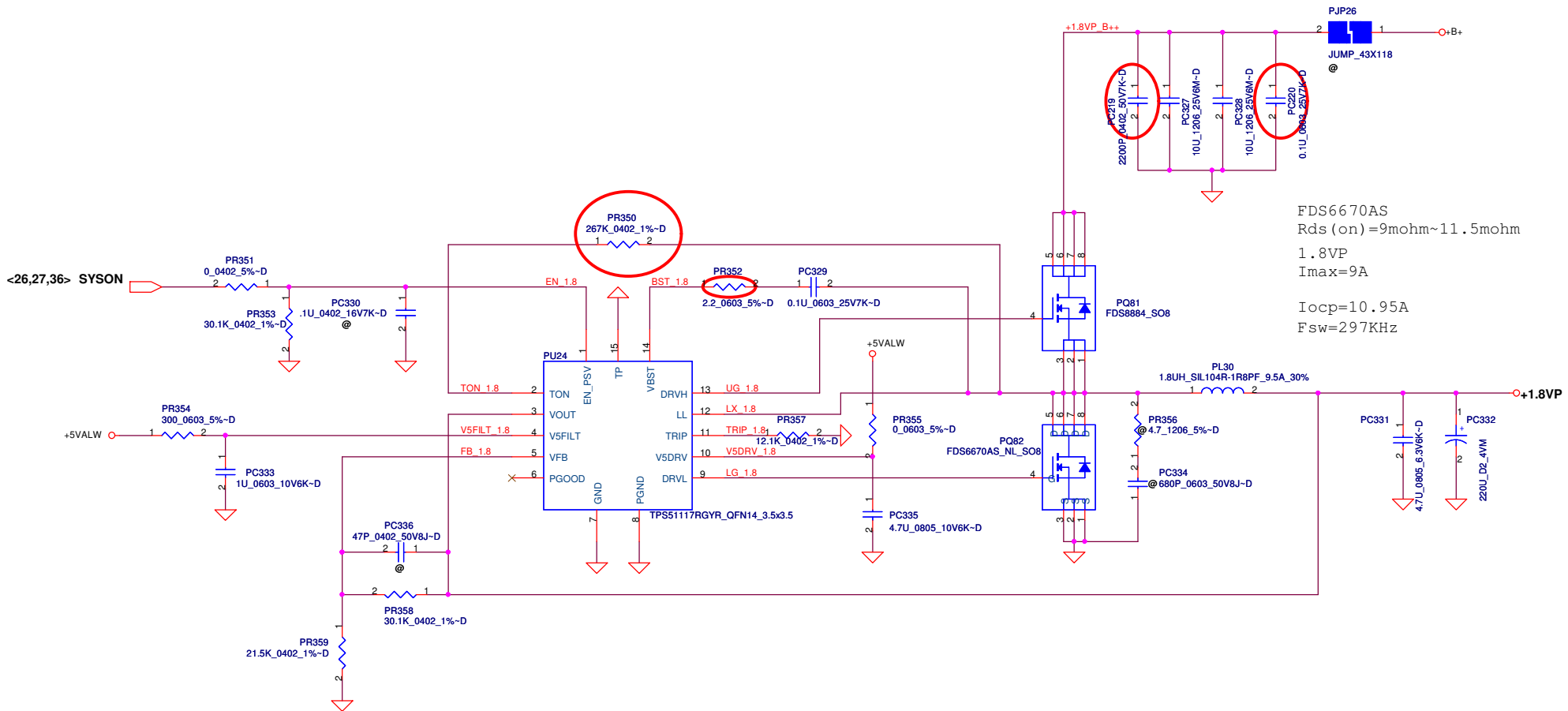
3.3VALWP
 I_{max}=6A
 I_{ocp}=8.94A

Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

5VALWP
 I_{max}=6A
 I_{ocp}=8.81A

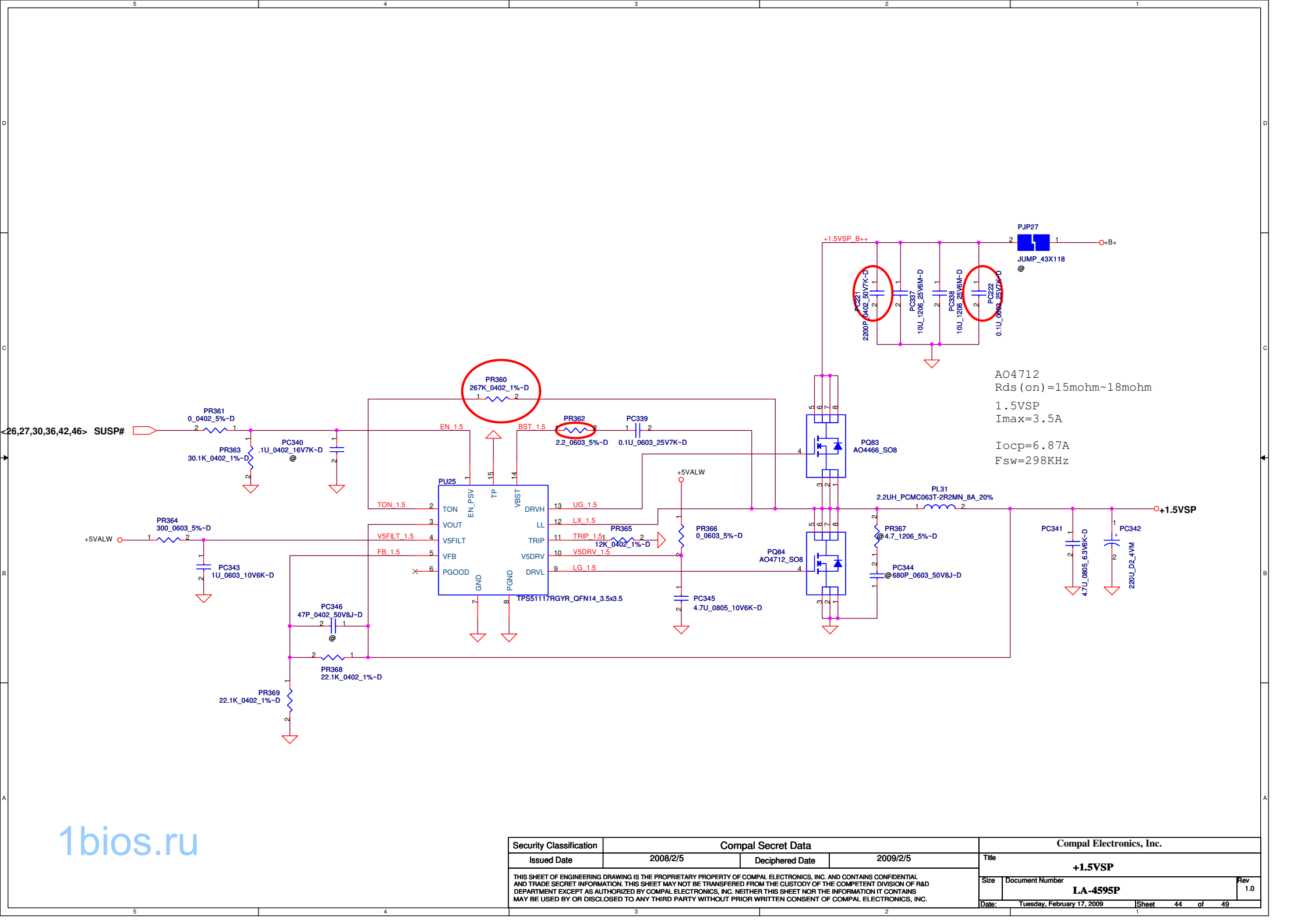
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FDS6670AS
 Rds(on) = 9mohm ~ 11.5mohm
 1.8VP
 I_{max} = 9A
 I_{ocp} = 10.95A
 F_{sw} = 297KHz

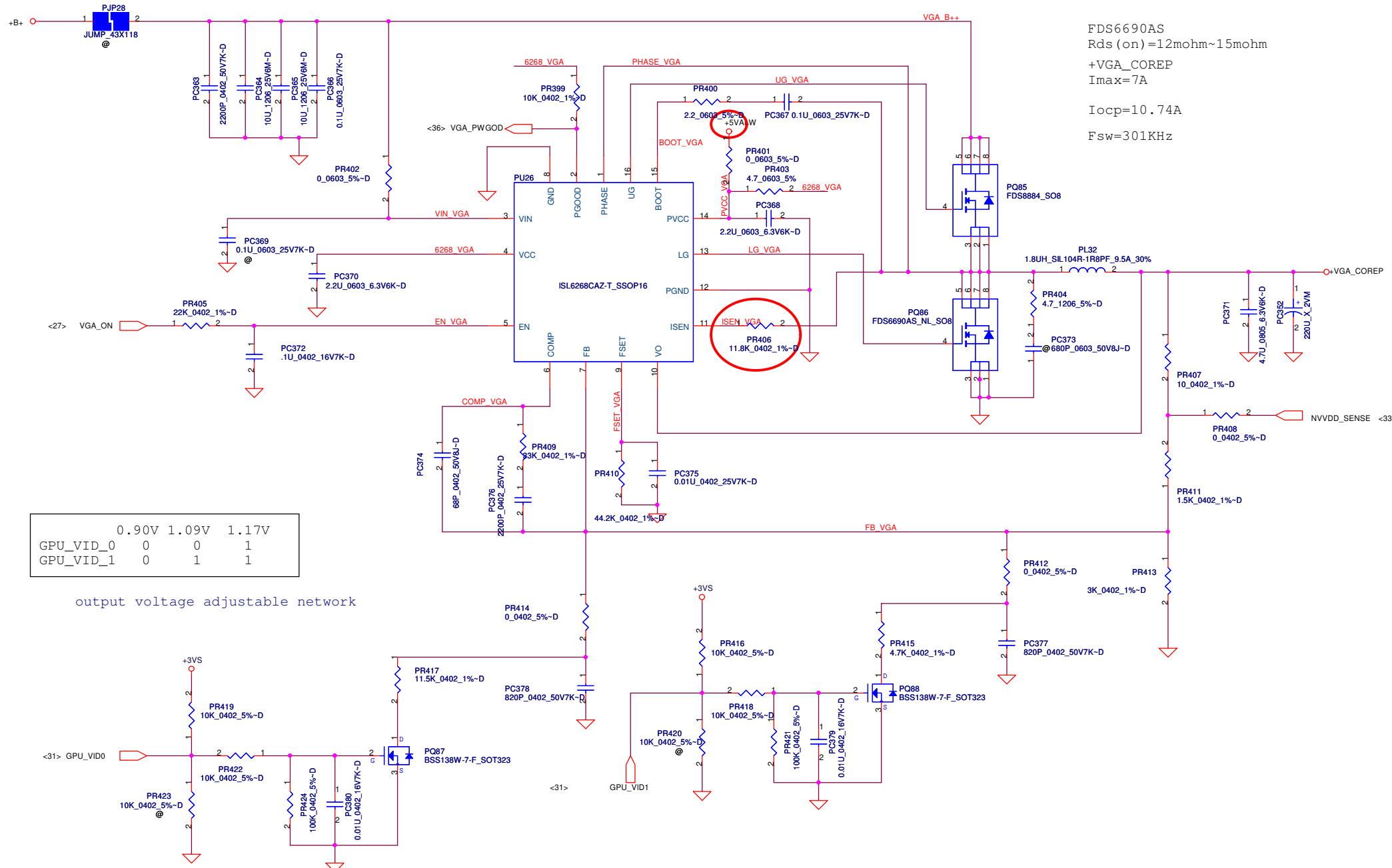
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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title	+1.8VP
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AO4712
 Rds(on)=15mohm~18mohm
 1.5VSP
 I_{max}=3.5A
 I_{ocp}=6.87A
 F_{sw}=298KHz

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Size	Document Number			Rev	
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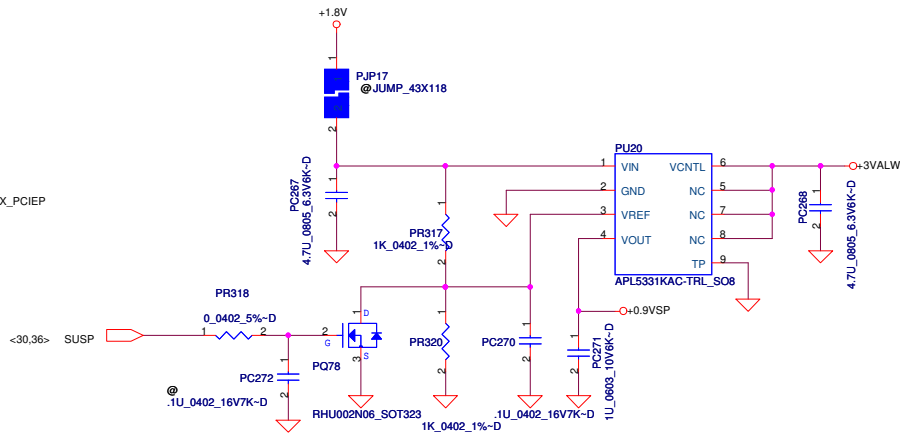
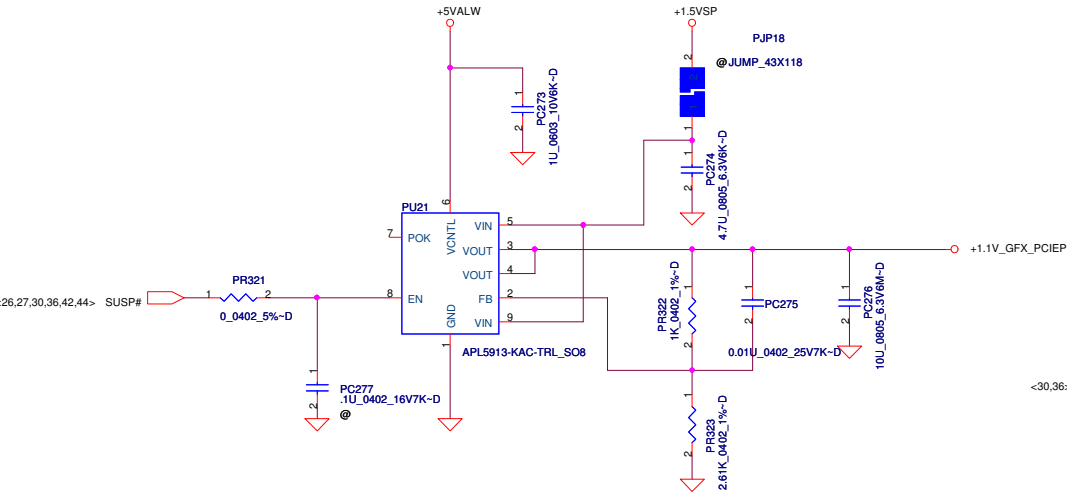
FDS6690AS
 Rds (on) = 12mohm~15mohm
 +VGA_COREP
 I_{max} = 7A
 I_{ocp} = 10.74A
 F_{sw} = 301KHz

	0.90V	1.09V	1.17V
GPU_VID_0	0	0	1
GPU_VID_1	0	1	1

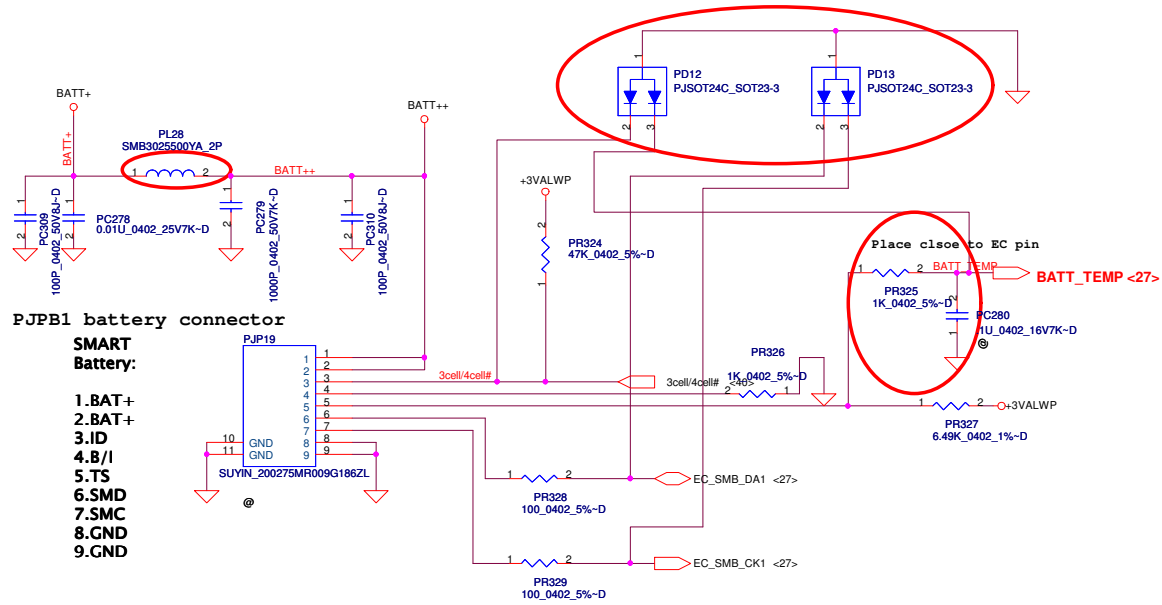
output voltage adjustable network

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				Rev	1.0



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Title	+0.9VSP/+1.1V_GFX_PCIEP			
Size	Document Number	Rev		
Custom	LA-4595P	1.0		
Date:	Tuesday, February 17, 2009	Sheet	46	of 49



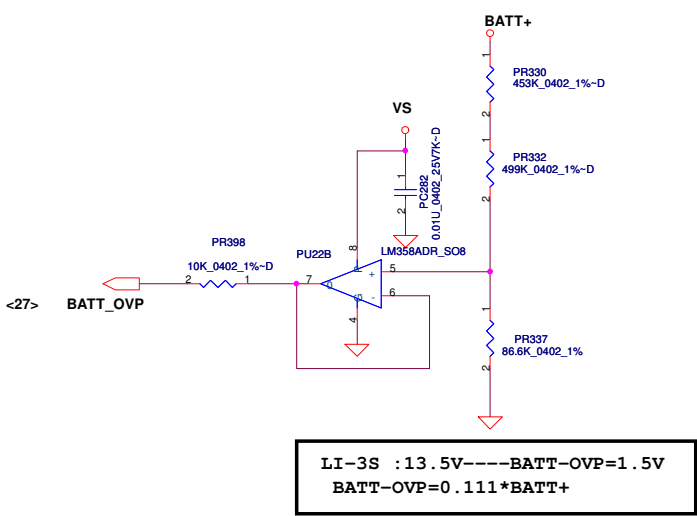
PJPB1 battery connector

SMART Battery:

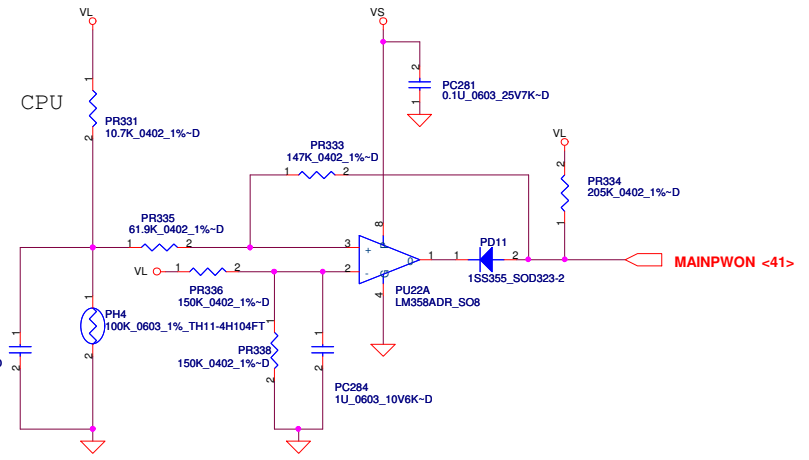
- 1.BAT+
- 2.BAT+
- 3.ID
- 4.B/I
- 5.TS
- 6.SMD
- 7.SMC
- 8.GND
- 9.GND

Battery Connect/OTP

CPU
PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



**LI-3S : 13.5V --- BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+**



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				BATTERY CONN
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	40	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	48	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	39	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	42	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	43	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	44	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
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				Custom	LA-4595P
Date: Tuesday, February 17, 2009				Sheet	49 of 49