Berry Discrete/UMA Schematics Document

AMD Danube CPU S1g4

AMD GPU Madison-LP/M96-LP M2

RS880M + SB820M

2010-03-08

REV : A00

DY : Nopop Component

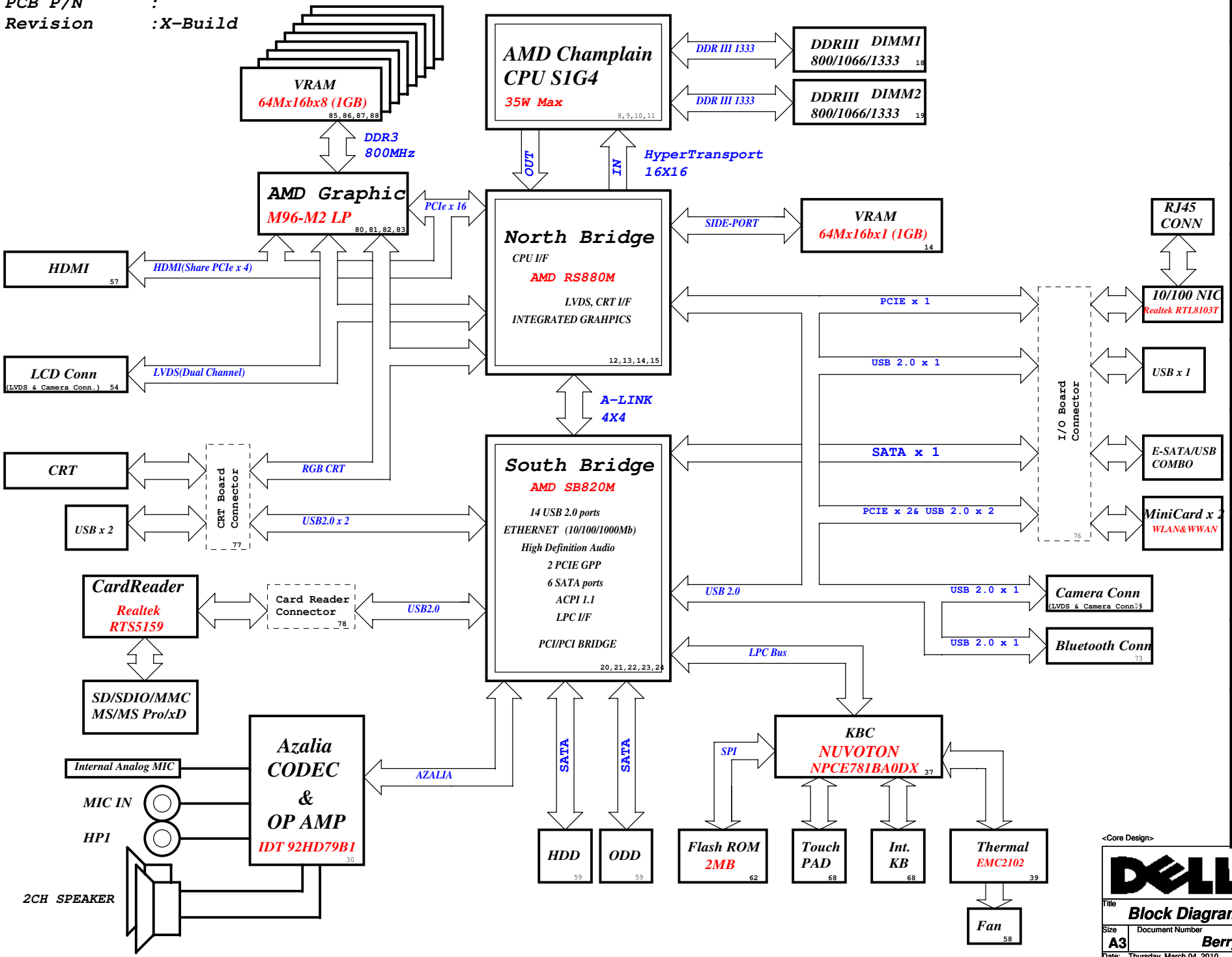
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Monday, March 08, 2010	Sheet 1 of 95	

Project code :91.4HH01.001
PCB P/N :
Revision :X-Build

Berry DG15 Discrete/UMA Block Diagram



CHARGER	
BQ24745	45
INPUTS	OUTPUTS
+DC_IN_SS +VCHGR	+PWR_SRC

SYSTEM DC/DC	
RT8205B	46
INPUTS	OUTPUTS
+PWR_SRC	+3.3V_RTC_LDO +5V_ALW +3.3V_ALW

CPU VDDR	
RT9025	48
INPUTS	OUTPUTS
+1.5V_SUS	+CPU_VDDR

CPU CORE	
ISL6265AHRTZ-T-GP	47
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

AMD RS880M CORE	
RT8209	50
INPUTS	OUTPUTS
+PWR_SRC	+NB_VDDC

AMD SB820M S5 POWER	
RT9025	48
INPUTS	OUTPUTS
+3.3V_ALW	+1.1V_ALW

DDR III SUS&VTT	
RT8207	49
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

DDR III SUS&VTT	
RT8207	49
INPUTS	OUTPUTS
+PWR_SRC	+0.75V_DDR_VTT

AMD GPU CORE	
RT8208B	89
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

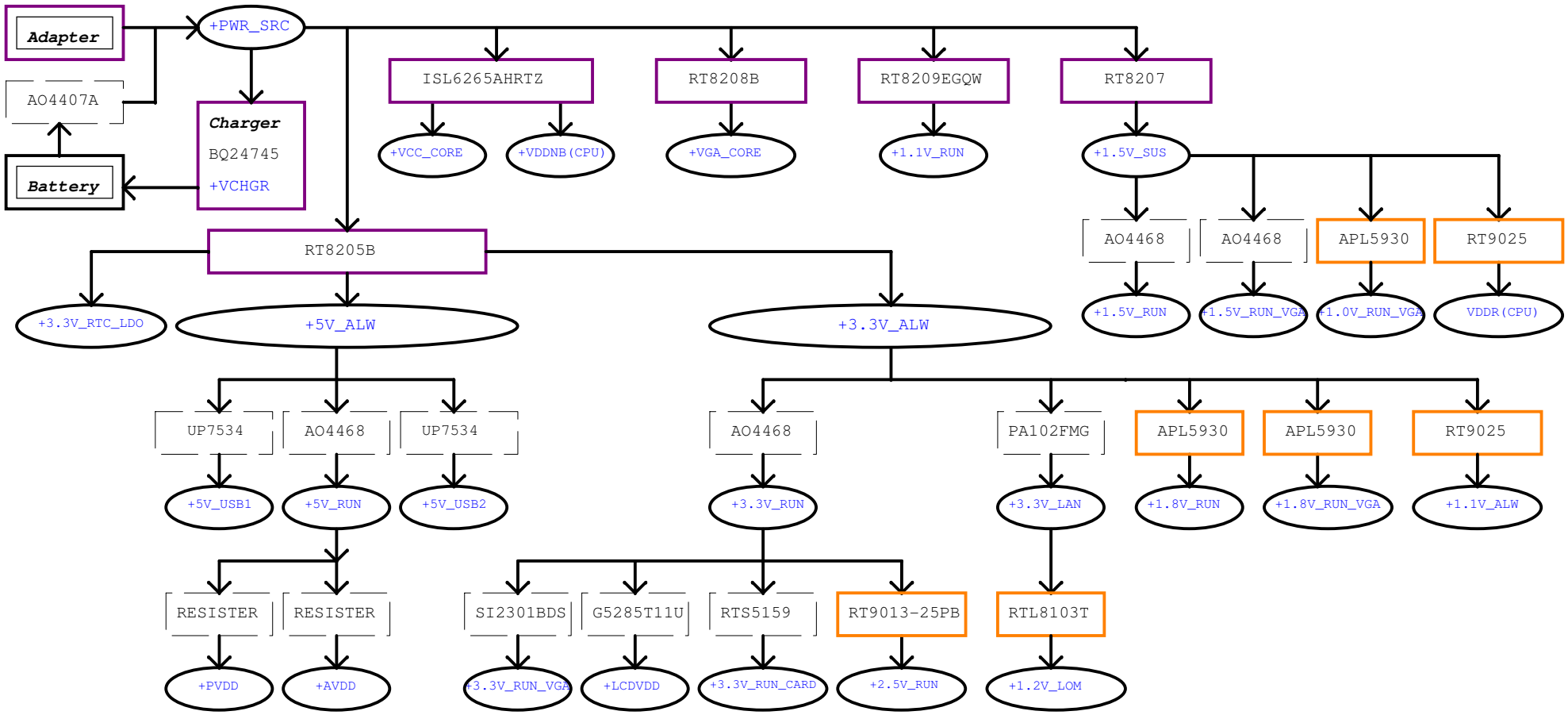
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 2 of 95

Power Block Diagram

Power Shape

Regulator | LDO | Switch

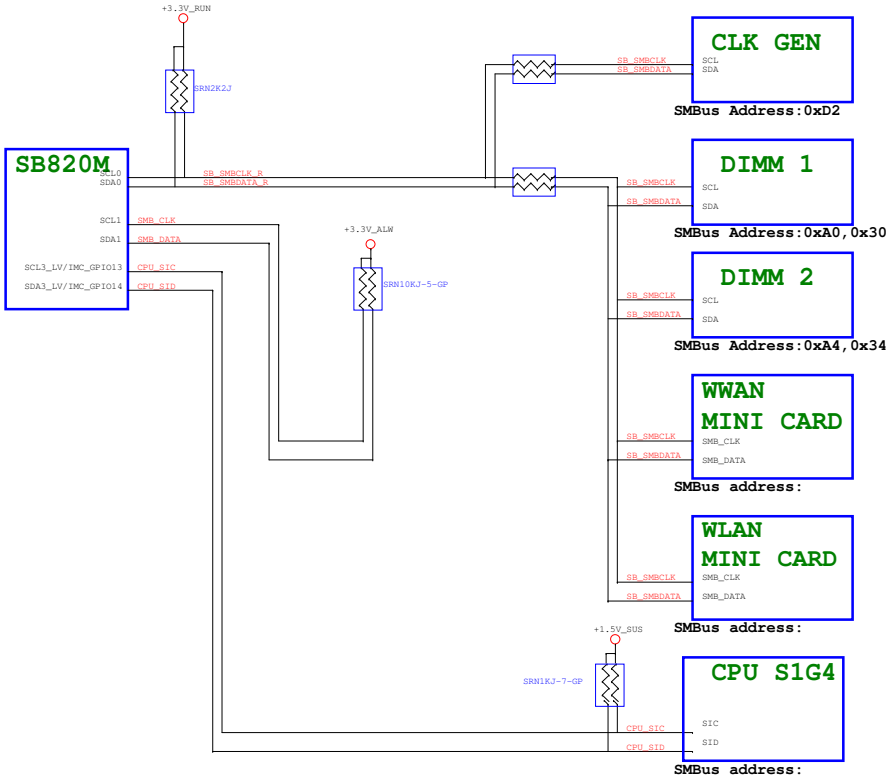


<Core Design>

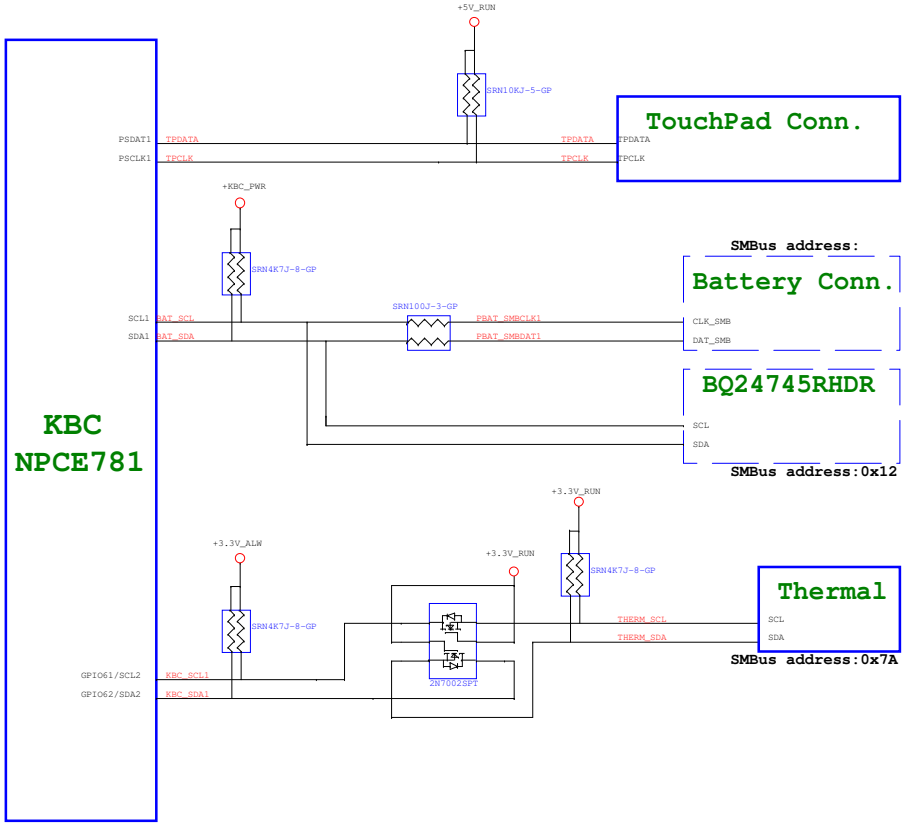
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram		
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 3 of 95	

SB820M SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

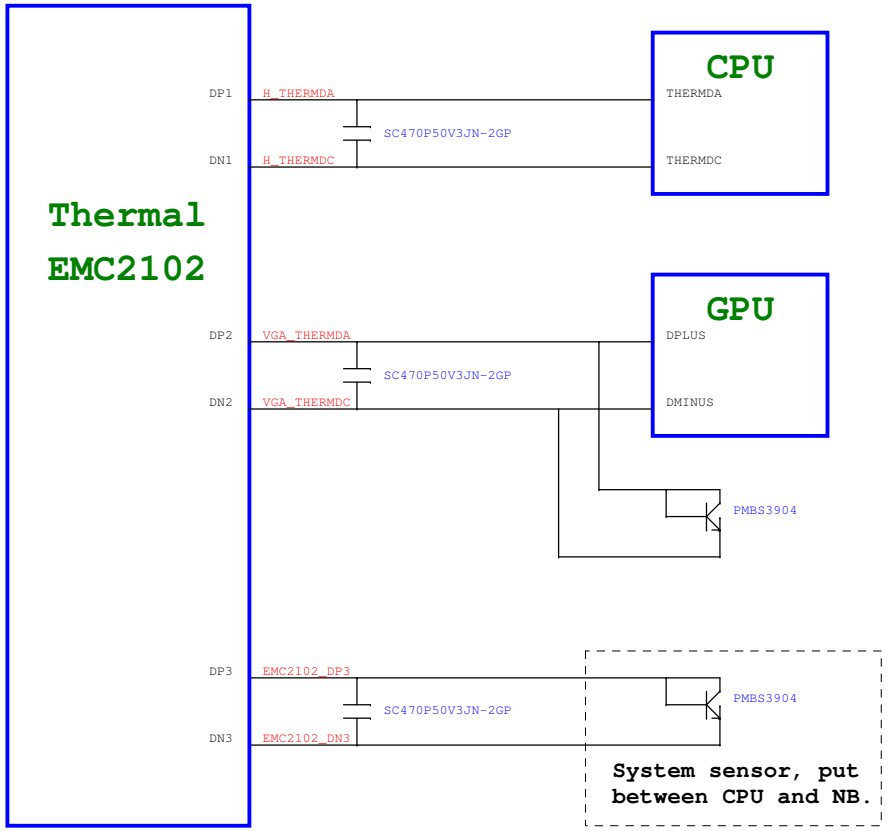
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

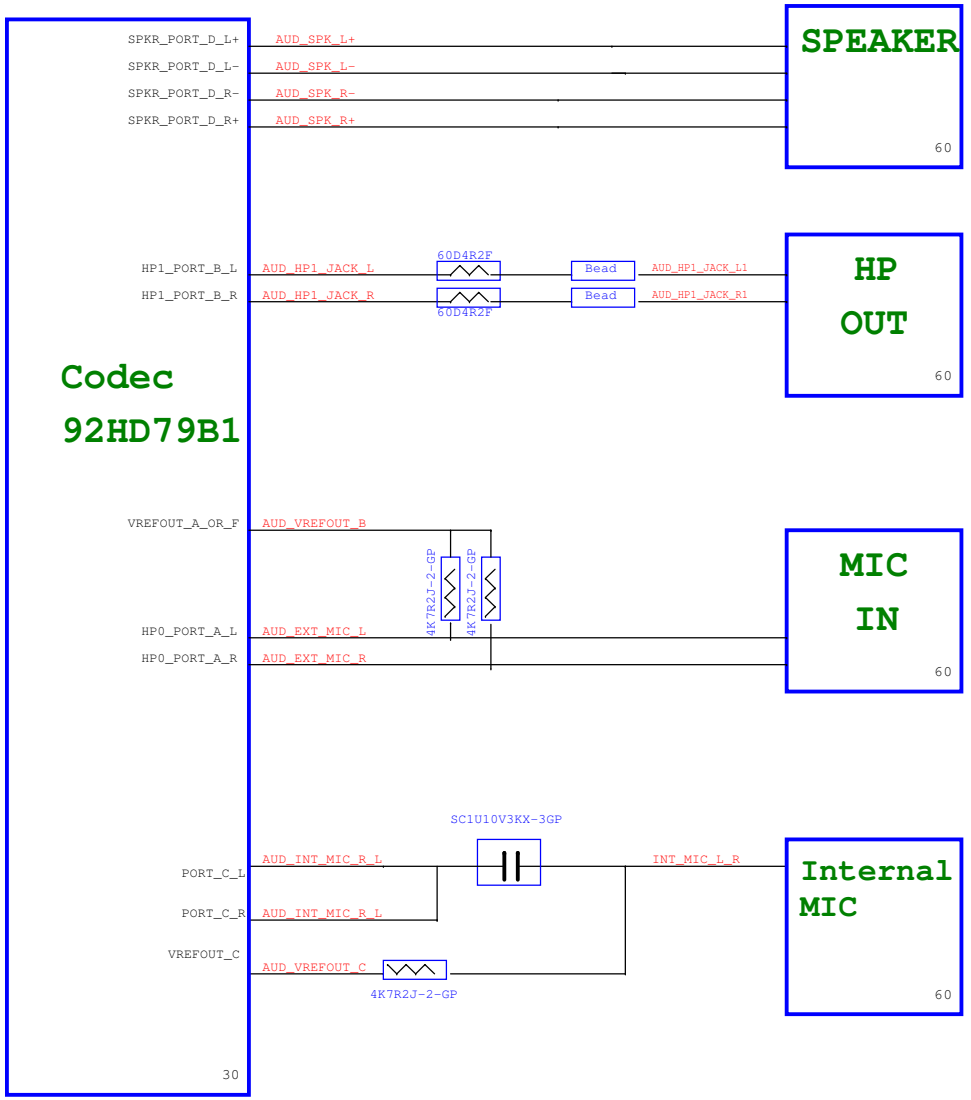
Size	Document Number	Rev
A2	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 4 of 95

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/AUDIO BLOCK DIAGRAM		
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 5 of 95	

SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	**Embedded Controller (EC)** * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub * 0V / 3.3V / LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	**Defines clock generator** * 0V – External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. 3.3V– Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	**Set PCIe to Gen II mode** 0V– Force PCIe interface at Gen I mode * 3.3V– PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	**Watchdog function** * 0V– Disable the boot fail timer function 3.3V– Enable the boot fail timer function
PCICLK3	DefaultStrapMode	**Default Debug Straps** * 0V– Disable Debug Straps. 3.3V– Select external Debug Straps
PCICLK4	CPUClkSel	**CPU/NB HT Clock Selection** 0V– Reserved. * 3.3V– Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	**Slow down core clock for low power platform.** * 0V– Performance mode 3.3V– Low Power mode

RS880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available(UMA) 1: Not available(Discrete)
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB0 (I/O Board/ESATA)
1	USB1 (I/O Board)
2	USB2 (CRT Board)
3	USB3 (CRT Board)
4	WLAN USB
5	WWAN USB
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA (LVDS CONN)
12	RESERVED
13	RESERVED

PCIE Routing

	RS880M
LANE0	MiniCard WLAN
LANE1	LAN
LANE2	MiniCard WWAN

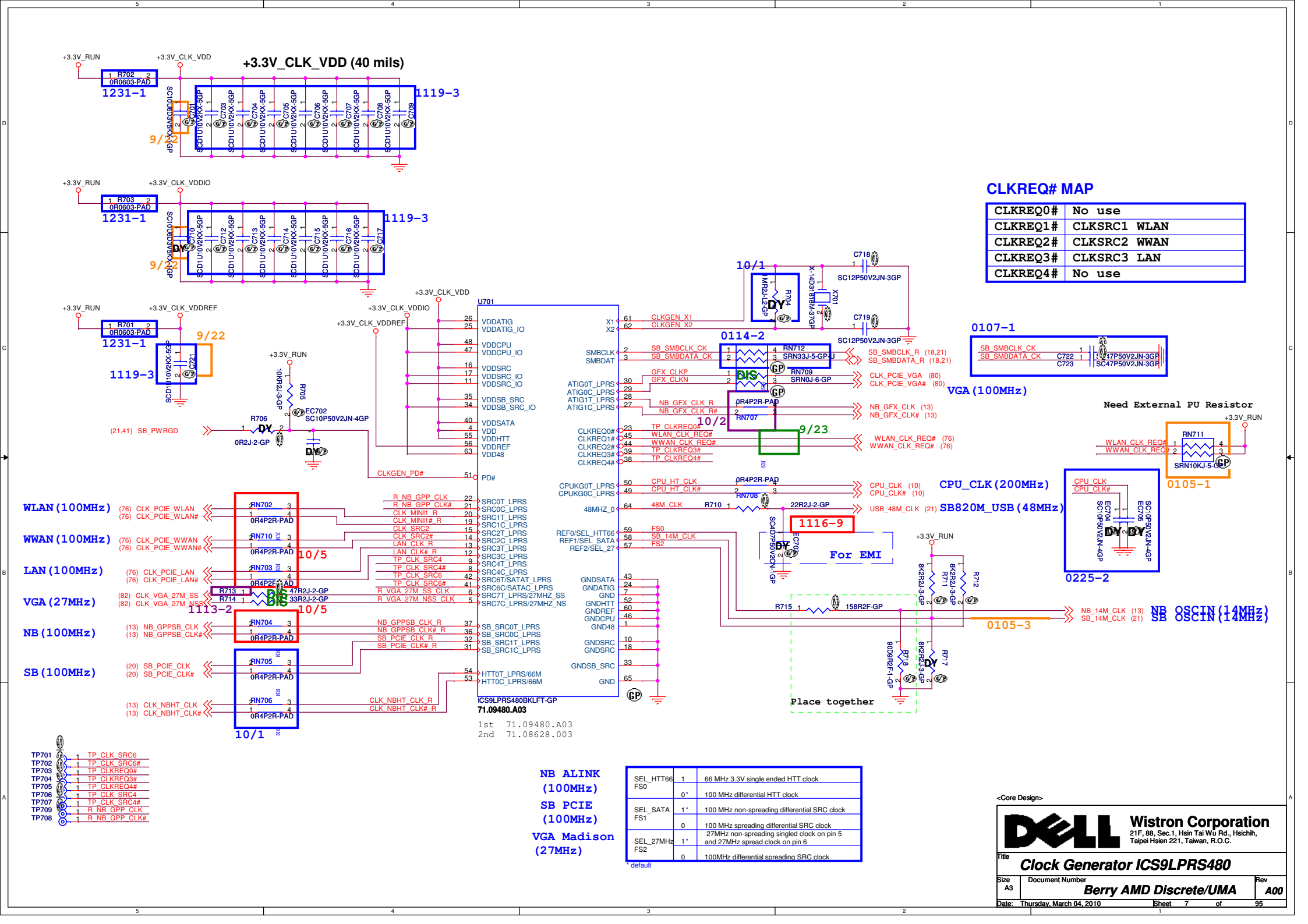
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

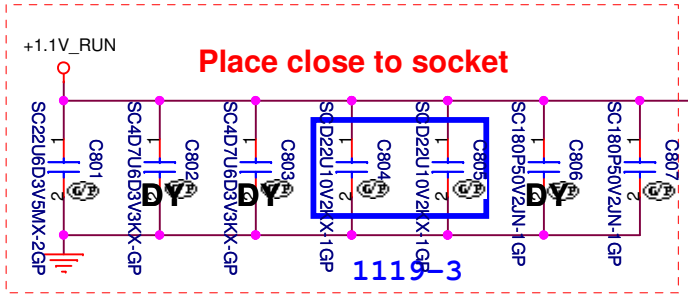
Title: Table of Content

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 6 of 95


+3.3V_CLK_VDD (40 mils)
CLKREQ# MAP
CLKREQ0# No use
CLKREQ1# CLKSRC1 WLAN
CLKREQ2# CLKSRC2 WWAN
CLKREQ3# CLKSRC3 LAN
CLKREQ4# No use
U701
ICS9LPRS480BKLFT-GP
71.09480.A03
1st 71.09480.A03
2nd 71.08628.003
WLAN(100MHz)
WWAN(100MHz)
LAN(100MHz)
VGA(27MHz)
NB(100MHz)
SB(100MHz)
VGA(100MHz)
CPU_CLK(200MHz)
SB820M_USB(48MHz)
NB OSCIN(14MHz)
SB OSCIN(14MHz)
Need External PU Resistor
For EMI
Place together
NB ALINK (100MHz)
SB PCIE (100MHz)
VGA Madison (27MHz)
SEL_HTT66 FS0
SEL_SATA FS1
SEL_27MHz FS2
66 MHz 3.3V single ended HTT clock
100 MHz differential HTT clock
100 MHz non-spreading differential SRC clock
100 MHz spreading differential SRC clock
27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
100MHz differential spreading SRC clock
* default
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Clock Generator ICS9LPRS480
Berry AMD Discrete/UMA
A00
Thursday, March 04, 2010
Sheet 7 of 95

SSID = CPU



1.1V(1.5A) for VLDT

CPU1A 1 OF 6

DANUBE

D1	VLDT_A0		VLDT_B0	AE2	
D2	VLDT_A1		VLDT_B1	AE3	
D3	VLDT_A2		VLDT_B2	AE4	
D4	VLDT_A3		VLDT_B3	AE5	
E3	L0_CADIN_H0		L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0 (12)
E2	L0_CADIN_L0		L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0 (12)
E1	L0_CADIN_H1		L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1 (12)
F1	L0_CADIN_L1		L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1 (12)
G3	L0_CADIN_H2		L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2 (12)
G2	L0_CADIN_L2		L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2 (12)
G1	L0_CADIN_H3		L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3 (12)
H1	L0_CADIN_L3		L0_CADOUT_L3	AA3	HT_CPU_NB_CAD_L3 (12)
J1	L0_CADIN_H4		L0_CADOUT_H4	W2	HT_CPU_NB_CAD_H4 (12)
K1	L0_CADIN_L4		L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4 (12)
L3	L0_CADIN_H5		L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5 (12)
L2	L0_CADIN_L5		L0_CADOUT_L5	U1	HT_CPU_NB_CAD_L5 (12)
L1	L0_CADIN_H6		L0_CADOUT_H6	U2	HT_CPU_NB_CAD_H6 (12)
M1	L0_CADIN_L6		L0_CADOUT_L6	U3	HT_CPU_NB_CAD_L6 (12)
N3	L0_CADIN_H7		L0_CADOUT_H7	T1	HT_CPU_NB_CAD_H7 (12)
N2	L0_CADIN_L7		L0_CADOUT_L7	R1	HT_CPU_NB_CAD_L7 (12)
E5	L0_CADIN_H8		L0_CADOUT_H8	AD4	HT_CPU_NB_CAD_H8 (12)
F5	L0_CADIN_L8		L0_CADOUT_L8	AD3	HT_CPU_NB_CAD_L8 (12)
F3	L0_CADIN_H9		L0_CADOUT_H9	AD5	HT_CPU_NB_CAD_H9 (12)
F4	L0_CADIN_L9		L0_CADOUT_L9	AC5	HT_CPU_NB_CAD_L9 (12)
G5	L0_CADIN_H10		L0_CADOUT_H10	AB4	HT_CPU_NB_CAD_H10 (12)
H5	L0_CADIN_L10		L0_CADOUT_L10	AB3	HT_CPU_NB_CAD_L10 (12)
H3	L0_CADIN_H11		L0_CADOUT_H11	AB5	HT_CPU_NB_CAD_H11 (12)
H4	L0_CADIN_L11		L0_CADOUT_L11	AA5	HT_CPU_NB_CAD_L11 (12)
K3	L0_CADIN_H12		L0_CADOUT_H12	Y5	HT_CPU_NB_CAD_H12 (12)
K4	L0_CADIN_L12		L0_CADOUT_L12	W5	HT_CPU_NB_CAD_L12 (12)
L5	L0_CADIN_H13		L0_CADOUT_H13	V4	HT_CPU_NB_CAD_H13 (12)
M5	L0_CADIN_L13		L0_CADOUT_L13	V3	HT_CPU_NB_CAD_L13 (12)
M3	L0_CADIN_H14		L0_CADOUT_H14	V5	HT_CPU_NB_CAD_H14 (12)
M4	L0_CADIN_L14		L0_CADOUT_L14	U5	HT_CPU_NB_CAD_L14 (12)
N5	L0_CADIN_H15		L0_CADOUT_H15	T4	HT_CPU_NB_CAD_H15 (12)
P5	L0_CADIN_L15		L0_CADOUT_L15	T3	HT_CPU_NB_CAD_L15 (12)
J3	L0_CLKIN_H0		L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0 (12)
J2	L0_CLKIN_L0		L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0 (12)
J5	L0_CLKIN_H1		L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1 (12)
K5	L0_CLKIN_L1		L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1 (12)
N1	L0_CTLIN_H0		L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0 (12)
P1	L0_CTLIN_L0		L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0 (12)
P3	L0_CTLIN_H1		L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1 (12)
P4	L0_CTLIN_L1		L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1 (12)

(12) HT_NB_CPU_CAD_H0 … (12) HT_NB_CPU_CAD_L15

(12) HT_NB_CPU_CLK_H0, (12) HT_NB_CPU_CLK_L0, (12) HT_NB_CPU_CLK_H1, (12) HT_NB_CPU_CLK_L1

(12) HT_NB_CPU_CTL_H0, (12) HT_NB_CPU_CTL_L0, (12) HT_NB_CPU_CTL_H1, (12) HT_NB_CPU_CTL_L1

SKT-BGA638H176

1'nd 62.10055.111

2'nd 62.10055.171

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 8 of 95

SSID = CPU

1231-2

Set empty: C905,C906,C903,C909,C913,C910,C915

4.7UF*4
0.22UF*4
1000PF*4
180PF*4

+CPU_VDDR

Place near to CPU

SC470U6D3V8XX-GP C901 DY
SC470U6D3V8XX-GP C902
SC470U6D3V8XX-GP C903 DY
SC470U6D3V8XX-GP C913
SD22U10V2K-1GP C904
SD22U10V2K-1GP C914
SD22U10V2K-1GP C905 DY
SD22U10V2K-1GP C906 DY
SC470U6D3V2KX-GP C907 DY
SC1000P50V3JN-GP-U C915
SC1000P50V3JN-GP-U C908 DY
SC1000P50V3JN-GP-U C909 DY
SC180P50V2JN-1GP C910 DY
SC180P50V2JN-1GP C911
SC180P50V2JN-1GP C916
SC180P50V2JN-1GP C912

1119-3 1231-2

0.9V, 1.25A--DDR1066
1.05V, 1.75A---DDR1333

+CPU_VDDR

+1.5V_SUS

R901 1 39D2R2F-L-GP MEMZP
R903 1 39D2R2F-L-GP MEMZN
SC10U6D3V3MX-GP C917

CPU1B 2 OF 6 DANUBE

D10 VDDR		W10 VDDR
C10 VDDR		AC10 VDDR
B10 VDDR		AB10 VDDR
AD10 VDDR		AA10 VDDR
		A10 VDDR
AE10 MEMZP		
AE10 MEMZN		Y10 VDDR_SENSE
H16 MA_RESET#		W17 MEMVREF
T19 MA0_ODT0		B18 MB_RESET#
V22 MA0_ODT1		
U21 MA1_ODT0		W26 MB0_ODT0
V19 MA1_ODT1		W23 MB0_ODT1
		Y26 MB1_ODT0
T20 MA0_CS#0		V26 MB0_CS#0
U19 MA0_CS#1		W25 MB0_CS#1
U20 MA1_CS#0		U22 MB1_CS#0
V20 MA1_CS#1		
J22 MA_CKE0		J25 MB_CKE0
J20 MA_CKE1		H26 MB_CKE1
N19 MA_CLK_H5		P22 MB_CLK_H5
N20 MA_CLK_L5		R22 MB_CLK_L5
E16 MA_CLK_H1		A17 MB_CLK_H1
F16 MA_CLK_L1		A18 MB_CLK_L1
Y16 MA_CLK_H7		AE18 MB_CLK_H7
AA16 MA_CLK_L7		AF17 MB_CLK_L7
P19 MA_CLK_H4		R26 MB_CLK_H4
P20 MA_CLK_L4		R25 MB_CLK_L4
N21 MA_ADD0		P24 MB_ADD0
M20 MA_ADD1		N24 MB_ADD1
N22 MA_ADD2		P26 MB_ADD2
M19 MA_ADD3		N23 MB_ADD3
M22 MA_ADD4		N26 MB_ADD4
L20 MA_ADD5		L23 MB_ADD5
M24 MA_ADD6		N25 MB_ADD6
L21 MA_ADD7		L24 MB_ADD7
L19 MA_ADD8		M26 MB_ADD8
K22 MA_ADD9		K26 MB_ADD9
R21 MA_ADD10		T26 MB_ADD10
L22 MA_ADD11		L26 MB_ADD11
K20 MA_ADD12		L25 MB_ADD12
V24 MA_ADD13		W24 MB_ADD13
K24 MA_ADD14		J23 MB_ADD14
K19 MA_ADD15		J24 MB_ADD15
R20 MA_BANK0		R24 MB_BANK0
R23 MA_BANK1		U26 MB_BANK1
J21 MA_BANK2		J26 MB_BANK2
R19 MA_RAS#		U25 MB_RAS#
T22 MA_CAS#		U24 MB_CAS#
T24 MA_WE#		U23 MB_WE#

(18) DDR3_A_DRAMRST#
(18) MEM_MA0_ODT0
(18) MEM_MA0_ODT1
(18) MEM_MA0_CS#0
(18) MEM_MA0_CS#1
(18) MEM_MA_CKE0
(18) MEM_MA_CKE1
(18) MEM_MA_CLK0_P
(18) MEM_MA_CLK0_N
(18) MEM_MA_CLK1_P
(18) MEM_MA_CLK1_N
(18) MEM_MA_ADD[0..15]
(18) MEM_MA_BANK0
(18) MEM_MA_BANK1
(18) MEM_MA_BANK2
(18) MEM_MA_RAS#
(18) MEM_MA_CAS#
(18) MEM_MA_WE#

DDR3_B_DRAMRST# (19)
MEM_MB0_ODT0 (19)
MEM_MB0_ODT1 (19)
MEM_MB0_CS#0 (19)
MEM_MB0_CS#1 (19)
MEM_MB_CKE0 (19)
MEM_MB_CKE1 (19)
MEM_MB_CLK0_P (19)
MEM_MB_CLK0_N (19)
MEM_MB_CLK1_P (19)
MEM_MB_CLK1_N (19)
MEM_MB_ADD[0..15] (19)
MEM_MB_BANK0 (19)
MEM_MB_BANK1 (19)
MEM_MB_BANK2 (19)
MEM_MB_RAS# (19)
MEM_MB_CAS# (19)
MEM_MB_WE# (19)

+0.75V_SUS_CPU_M_VREF
TP901 DY
TP_CPU_VDDR_SENSE

+1.5V_SUS

1119-3
SD1U10V2KX-5GP C918
1KR3F-GP R902
SC1000P50V3JN-GP-U C919
SD1U10V2KX-5GP C920
1KR3F-GP R905

1119-1 CLOSE TO CPU

1117-8 Remove

3 OF 6 CPU1C DANUBE

(18) M_A_DQ[63..0]

M_A_DQ0	G12	MA_DATA0	MB_DATA0 C11 M_B_DQ0
M_A_DQ1	F12	MA_DATA1	MB_DATA1 A11 M_B_DQ1
M_A_DQ2	H14	MA_DATA2	MB_DATA2 A14 M_B_DQ2
M_A_DQ3	G14	MA_DATA3	MB_DATA3 B14 M_B_DQ3
M_A_DQ4	H11	MA_DATA4	MB_DATA4 G11 M_B_DQ4
M_A_DQ5	H12	MA_DATA5	MB_DATA5 E11 M_B_DQ5
M_A_DQ6	C13	MA_DATA6	MB_DATA6 D12 M_B_DQ6
M_A_DQ7	E13	MA_DATA7	MB_DATA7 A13 M_B_DQ7
M_A_DQ8	H15	MA_DATA8	MB_DATA8 A15 M_B_DQ8
M_A_DQ9	E15	MA_DATA9	MB_DATA9 A16 M_B_DQ9
M_A_DQ10	E17	MA_DATA10	MB_DATA10 A19 M_B_DQ10
M_A_DQ11	H17	MA_DATA11	MB_DATA11 A20 M_B_DQ11
M_A_DQ12	E14	MA_DATA12	MB_DATA12 C14 M_B_DQ12
M_A_DQ13	F14	MA_DATA13	MB_DATA13 D14 M_B_DQ13
M_A_DQ14	C17	MA_DATA14	MB_DATA14 C18 M_B_DQ14
M_A_DQ15	G17	MA_DATA15	MB_DATA15 D18 M_B_DQ15
M_A_DQ16	G18	MA_DATA16	MB_DATA16 D20 M_B_DQ16
M_A_DQ17	C19	MA_DATA17	MB_DATA17 A21 M_B_DQ17
M_A_DQ18	D22	MA_DATA18	MB_DATA18 D24 M_B_DQ18
M_A_DQ19	E20	MA_DATA19	MB_DATA19 C25 M_B_DQ19
M_A_DQ20	E18	MA_DATA20	MB_DATA20 B20 M_B_DQ20
M_A_DQ21	F18	MA_DATA21	MB_DATA21 C20 M_B_DQ21
M_A_DQ22	B22	MA_DATA22	MB_DATA22 B24 M_B_DQ22
M_A_DQ23	C23	MA_DATA23	MB_DATA23 C24 M_B_DQ23
M_A_DQ24	F20	MA_DATA24	MB_DATA24 E23 M_B_DQ24
M_A_DQ25	F22	MA_DATA25	MB_DATA25 E24 M_B_DQ25
M_A_DQ26	H24	MA_DATA26	MB_DATA26 G25 M_B_DQ26
M_A_DQ27	J19	MA_DATA27	MB_DATA27 G26 M_B_DQ27
M_A_DQ28	E21	MA_DATA28	MB_DATA28 C26 M_B_DQ28
M_A_DQ29	E22	MA_DATA29	MB_DATA29 D26 M_B_DQ29
M_A_DQ30	H20	MA_DATA30	MB_DATA30 G23 M_B_DQ30
M_A_DQ31	H22	MA_DATA31	MB_DATA31 G24 M_B_DQ31
M_A_DQ32	Y24	MA_DATA32	MB_DATA32 AA24 M_B_DQ32
M_A_DQ33	AB24	MA_DATA33	MB_DATA33 AA23 M_B_DQ33
M_A_DQ34	AB22	MA_DATA34	MB_DATA34 AD24 M_B_DQ34
M_A_DQ35	AA21	MA_DATA35	MB_DATA35 AE24 M_B_DQ35
M_A_DQ36	W22	MA_DATA36	MB_DATA36 AA25 M_B_DQ36
M_A_DQ37	W21	MA_DATA37	MB_DATA37 AD26 M_B_DQ37
M_A_DQ38	Y22	MA_DATA38	MB_DATA38 AE25 M_B_DQ38
M_A_DQ39	AA22	MA_DATA39	MB_DATA39 AC22 M_B_DQ39
M_A_DQ40	Y20	MA_DATA40	MB_DATA40 AD22 M_B_DQ40
M_A_DQ41	AA20	MA_DATA41	MB_DATA41 AE20 M_B_DQ41
M_A_DQ42	AA18	MA_DATA42	MB_DATA42 AF20 M_B_DQ42
M_A_DQ43	AB18	MA_DATA43	MB_DATA43 AF24 M_B_DQ43
M_A_DQ44	AB21	MA_DATA44	MB_DATA44 AF23 M_B_DQ44
M_A_DQ45	AD21	MA_DATA45	MB_DATA45 AC20 M_B_DQ45
M_A_DQ46	AD19	MA_DATA46	MB_DATA46 AD20 M_B_DQ46
M_A_DQ47	Y18	MA_DATA47	MB_DATA47 AD18 M_B_DQ47
M_A_DQ48	AD17	MA_DATA48	MB_DATA48 AE18 M_B_DQ48
M_A_DQ49	W16	MA_DATA49	MB_DATA49 AC14 M_B_DQ49
M_A_DQ50	W14	MA_DATA50	MB_DATA50 AD14 M_B_DQ50
M_A_DQ51	Y14	MA_DATA51	MB_DATA51 AF19 M_B_DQ51
M_A_DQ52	Y17	MA_DATA52	MB_DATA52 AC18 M_B_DQ52
M_A_DQ53	AB17	MA_DATA53	MB_DATA53 AF16 M_B_DQ53
M_A_DQ54	AB15	MA_DATA54	MB_DATA54 AE15 M_B_DQ54
M_A_DQ55	AD15	MA_DATA55	MB_DATA55 AF13 M_B_DQ55
M_A_DQ56	AB13	MA_DATA56	MB_DATA56 AC12 M_B_DQ56
M_A_DQ57	AD13	MA_DATA57	MB_DATA57 AB11 M_B_DQ57
M_A_DQ58	Y12	MA_DATA58	MB_DATA58 Y11 M_B_DQ58
M_A_DQ59	W11	MA_DATA59	MB_DATA59 AE14 M_B_DQ59
M_A_DQ60	AB14	MA_DATA60	MB_DATA60 AF14 M_B_DQ60
M_A_DQ61	AA14	MA_DATA61	MB_DATA61 AF11 M_B_DQ61
M_A_DQ62	AB12	MA_DATA62	MB_DATA62 AD11 M_B_DQ62
M_A_DQ63	AA12	MA_DATA63	MB_DATA63 M_B_DQ63

M_B_DQ[63..0] (19)

(18) M_A_DM[7..0]

M_A_DM0	E12	MA_DM0	MB_DM0 A12 M_B_DM0
M_A_DM1	C15	MA_DM1	MB_DM1 B16 M_B_DM1
M_A_DM2	E19	MA_DM2	MB_DM2 A22 M_B_DM2
M_A_DM3	F24	MA_DM3	MB_DM3 E25 M_B_DM3
M_A_DM4	AC24	MA_DM4	MB_DM4 AB26 M_B_DM4
M_A_DM5	Y19	MA_DM5	MB_DM5 AE22 M_B_DM5
M_A_DM6	AB16	MA_DM6	MB_DM6 AC16 M_B_DM6
M_A_DM7	Y13	MA_DM7	MB_DM7 AD12 M_B_DM7

M_B_DM[7..0] (19)

(18) M_A_DQS0
(18) M_A_DQS#0
(18) M_A_DQS1
(18) M_A_DQS#1
(18) M_A_DQS2
(18) M_A_DQS#2
(18) M_A_DQS3
(18) M_A_DQS#3
(18) M_A_DQS4
(18) M_A_DQS#4
(18) M_A_DQS5
(18) M_A_DQS#5
(18) M_A_DQS6
(18) M_A_DQS#6
(18) M_A_DQS7
(18) M_A_DQS#7

G13	MA_DQS_H0	MB_DQS_H0	C12 M_B_DQS0 (19)
H13	MA_DQS_L0	MB_DQS_L0	B12 M_B_DQS#0 (19)
G16	MA_DQS_H1	MB_DQS_H1	D16 M_B_DQS1 (19)
G15	MA_DQS_L1	MB_DQS_L1	C16 M_B_DQS#1 (19)
C22	MA_DQS_H2	MB_DQS_H2	A24 M_B_DQS2 (19)
C21	MA_DQS_L2	MB_DQS_L2	A23 M_B_DQS#2 (19)
G22	MA_DQS_H3	MB_DQS_H3	F26 M_B_DQS3 (19)
G21	MA_DQS_L3	MB_DQS_L3	E26 M_B_DQS#3 (19)
AD23	MA_DQS_H4	MB_DQS_H4	AC25 M_B_DQS4 (19)
AC23	MA_DQS_L4	MB_DQS_L4	AC26 M_B_DQS#4 (19)
AB19	MA_DQS_H5	MB_DQS_H5	AF21 M_B_DQS5 (19)
AB20	MA_DQS_L5	MB_DQS_L5	AF22 M_B_DQS#5 (19)
Y15	MA_DQS_H6	MB_DQS_H6	AE16 M_B_DQS6 (19)
W15	MA_DQS_L6	MB_DQS_L6	AD16 M_B_DQS#6 (19)
W12	MA_DQS_H7	MB_DQS_H7	AE12 M_B_DQS7 (19)
W13	MA_DQS_L7	MB_DQS_L7	AF12 M_B_DQS#7 (19)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 9 of 95

SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

CPU_CLK(200MHz)

For HDT DBG

Close To CPU

Close CPU

9/11 S1g4 no support LDTREQ#

S1G4 not support MEMHOT

LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

HDT Connectors

For old HDT tool (3.3V level)

<Core Design>

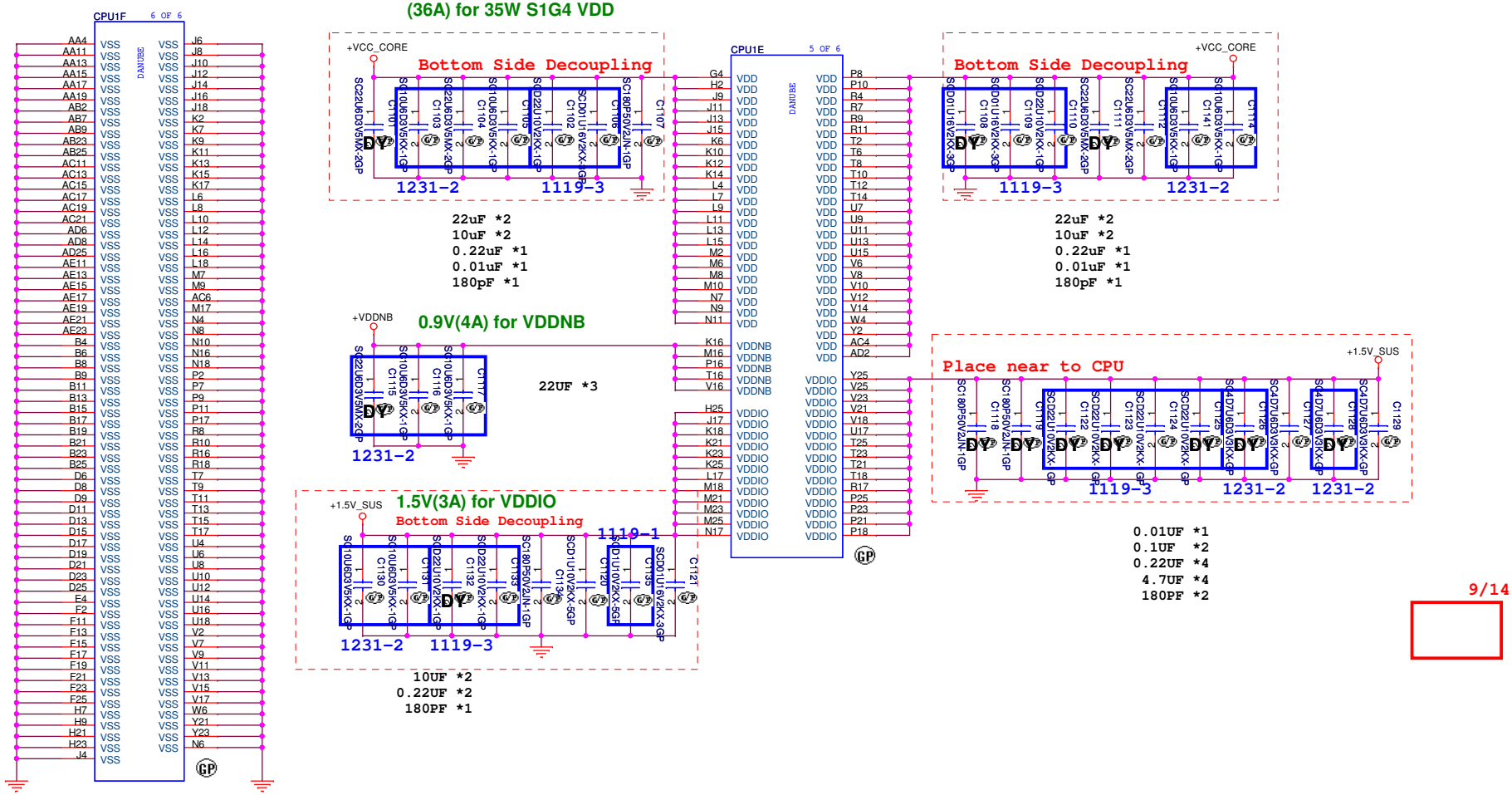
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 10 of 95

SSID = CPU



9/14

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 11 of 95	

SSID = N.B

RS880M : 71.RS880.M05

U1A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS880M-1-GP

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

U1B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS880M-1-GP

LANE REVERSAL

9/15

9/11

1119-3

WLAN
LAN
WWAN

A-LINK

Place < 100mils from pin AC8 and AB8

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_HT LINK&PCIe(1/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 12 of 95

SSID = N.B

RS880M : 71.RS880.M05

UMA DAC Signal:
GREEN/BLUE: Connected to GND through two separate 150- 1% resistors.

RED: Connected to GND through two separate 133- 1% resistors.(For match resistor on CRT/B 150- 1%)

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use DAC_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use DAC_HSYNC)
1 = Memory Side port Not available DIS
0 = Memory Side port available UMA_SPM

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT

+1.1V_RUN 1.1V, 65mA — L1308 BLM15AG221SS1D-GP 220R, 0.3A — PLLVDD — SC1U6D3V2KX-GP C1312 — 10/8 UMA/DIS

+1.8V_RUN 1.8V, 20mA — L1307 BLM15AG221SS1D-GP 220R, 0.3A — PLLVDD18 — SC2D2U6D3V3KX-GP C1311 — UMA/DIS

Layout Note
Trace at least 15 mil

+1.8V_RUN 1.8V, 20mA — L1301 BLM15AG221SS1D-GP 220R, 0.3A — +1.8V_VDDA18HTPLL — SC1U6D3V2KX-GP C1302, SCD1U10V2KX-5GP C1303 — 10/8 — 1119-3

9/22 R1343 0R0603-PAD — +1.8V_VDDA18PCIEPLL 1.8V, 120mA — SC2D2U6D3V3KX-GP C1304, SCD1U10V2KX-5GP C1305 — 1119-3 — SC22U6D3V5MX-2GP C1301

+3.3V_RUN — R1342 0R3J-0-U-GP UMA — 0106-2

+3.3V_RUN_AVDD 3.3V, 110mA — SC1U6D3V2KX-GP C1307 — UMA/DIS — 10/8

+1.8V_RUN — R1333 0R3J-0-U-GP UMA

+1.8V_RUN_AVDDDI 1.8V, 20mA — SCD1U10V2KX-5GP C1306 — UMA/DIS

+1.8V_RUN — R1344 0R3J-0-U-GP UMA — 1119-1

+1.8V_RUN_AVDDDQ 1.8V, 4mA — C1308 SC2D2U6D3V3KX-GP — UMA/DIS

UMA: DAC_CLK and DATA with 5V-tolerant. not need level shift

Trace at least 10 mil

9/22 — (77) M_RED — R1326 150R2F-1-GP UMA
(77) M_GREEN — R1327 150R2F-1-GP UMA
(77) M_BLUE — R1328 150R2F-1-GP UMA

(77) VGA_HSYNC — VGA_HSYNC
(77) VGA_VSYNC — VGA_VSYNC
(77) DDC_CLK_CON — DDC_CLK_CON
(77) DDC_DATA_CON — DDC_DATA_CON

R1306 715R2F-GP — DAC_RSET

PLLVDD
PLLVDD18

+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL

(20,37,80) PLTRST#_NB_GPU
(41) NB_PWRGD_IN — 9/16 — SC180P50V2JN-1GP EC1301, SC180P50V2JN-1GP EC1302

+1.1V_RUN — R1312 4K7R2F-GP, R1313 4K7R2F-GP

(7) NB_14M_CLK — 1231-2 — R1341 0R0402-PAD

(7) CLK_NBHT_CLK
(7) CLK_NBHT_CLK#

NB_LDT_STOP#
NB_ALLOW_LDTSTOP
NB_REFCLK_P
NB_REFCLK_N

(7) NB_GFX_CLK — NB_GFX_CLK
(7) NB_GFX_CLK# — NB_GFX_CLK# — SCD1U10V2KX-5GP C1315 — 10/2 — TP1306 TP1307 — 10/7

NB_GPP_CLK
NB_GPP_CLK#

(7) NB_GPPSB_CLK
(7) NB_GPPSB_CLK#

(55) LDDC_CLK
(55) LDDC_DATA
(57) NB_DDC_DATA0
(57) NB_DDC_CLK0 — 9/15

1120-6 — STRP_DATA — TP1305 — TP_NB_RESERVED — RS780_AUX_CAL — R1318 2KR2J-1-GP, R1319 150R2F-1-GP

9/25

+1.5V_RUN — R1309 300R2J-4-GP — R1322 DY 0R2J-2-GP — U1301 NC7WZ07P6X-1GP — (10,20) CPU_LDT_STOP# — NB_LDT_STOP# — SCD1U10V2KX-5GP C1314

+1.8V_RUN — R1311 2K2R2J-2-GP — 9/15

+1.8V_RUN — R1315 1KR2J-1-GP — (20) ALLOW_LDTSTOP — NB_ALLOW_LDTSTOP — R1316 0R0402-PAD

ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted

+3.3V_RUN — R1302 3KR2J-2-GP, R1303, R1304 3KR2J-2-GP, R1305 DY — SPM_Disable — SPM_Enable — VGA_VSYNC — VGA_HSYNC

U1C — PART 3 OF 6

CRT/TVOUT: AVDD1, AVDD2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, C_Pr, Y, COMP_Pb, RED, REDb, GREEN, GREENb, BLUE, BLUEb, DAC_HSYNC, DAC_VSYNC, DAC_SCL, DAC_SDA, DAC_RSET

PLL PWR: PLLVDD, PLLVDD18, PLLVSS, VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

CLOCKs PM: SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP, HT_REFCLKP, HT_REFCLKN, REFCLK_P/OSCIN, REFCLK_N, GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP, GPPSB_REFCLKN

MIS.: I2C_CLK, I2C_DATA, DDC_DATA0/AUX0N, DDC_CLK0/AUX0P, DDC_CLK1/AUX1P, DDC_DATA1/AUX1N, STRP_DATA, RESERVED, AUX_CAL

LVTM: TXOUT_L0P/N, TXOUT_L1P/N, TXOUT_L2P/N, TXOUT_L3P/N, TXOUT_U0P/N, TXOUT_U1P/N, TXOUT_U2P/N, TXOUT_U3P/N, TXCLK_LP/LN, TXCLK_UP/UN, VDDLTP18, VSSLTP18, VDDLT18_1, VDDLT18_2, VDDLT33_1, VDDLT33_2, VSSLT1–VSSLT7

RS880M-1-GP

VGA_TXAOUT0+ (55) … VGA_TXAOUT2- (55)
VGA_TXBOUT0+ (55) … VGA_TXBOUT2- (55)
VGA_TXACLK+ (55) … VGA_TXBCLK- (55)

+1.8V_RUN — VDDLTP18_R — 1.8V, 15mA — 1119-1 — L1305 220R, 0.3A BLM15AG221SS1D-GP UMA — C1309 SC2D2U6D3V3KX-GP UMA/DIS

VDDLT18_R — 1.8V, 300mA — L1306 PBY160808T-221Y-N-GP 220R, 2A UMA — SCD1U10V2KX-5GP C1310 UMA — SC4D7U6D3V3KX-GP C1313 UMA/DIS

11/12-4

LVDS_DIGON — NB_LCDPWR_EN (55)
LVDS_BLON — NB_BL_PWM (55)
LVDS_ENA_BL — NB_BL_EN (55)

RN1301 SRN10KJ-5-GP UMA — 9/22

TMDS_HPD — TP_TMDS_HPD TP1308 — 0225-1
HPD — HDMI_HPD_DET — R1317 0R2J-2-GP UMA — HDMI_HPD_DET (57,82)

SUS_STAT# — NB_SUS_STAT# — SUS_STAT# (21)

THERMALDIODE_P
THERMALDIODE_N

TESTMODE — TESTMODE_NB — R1320 1K8R2F-GP

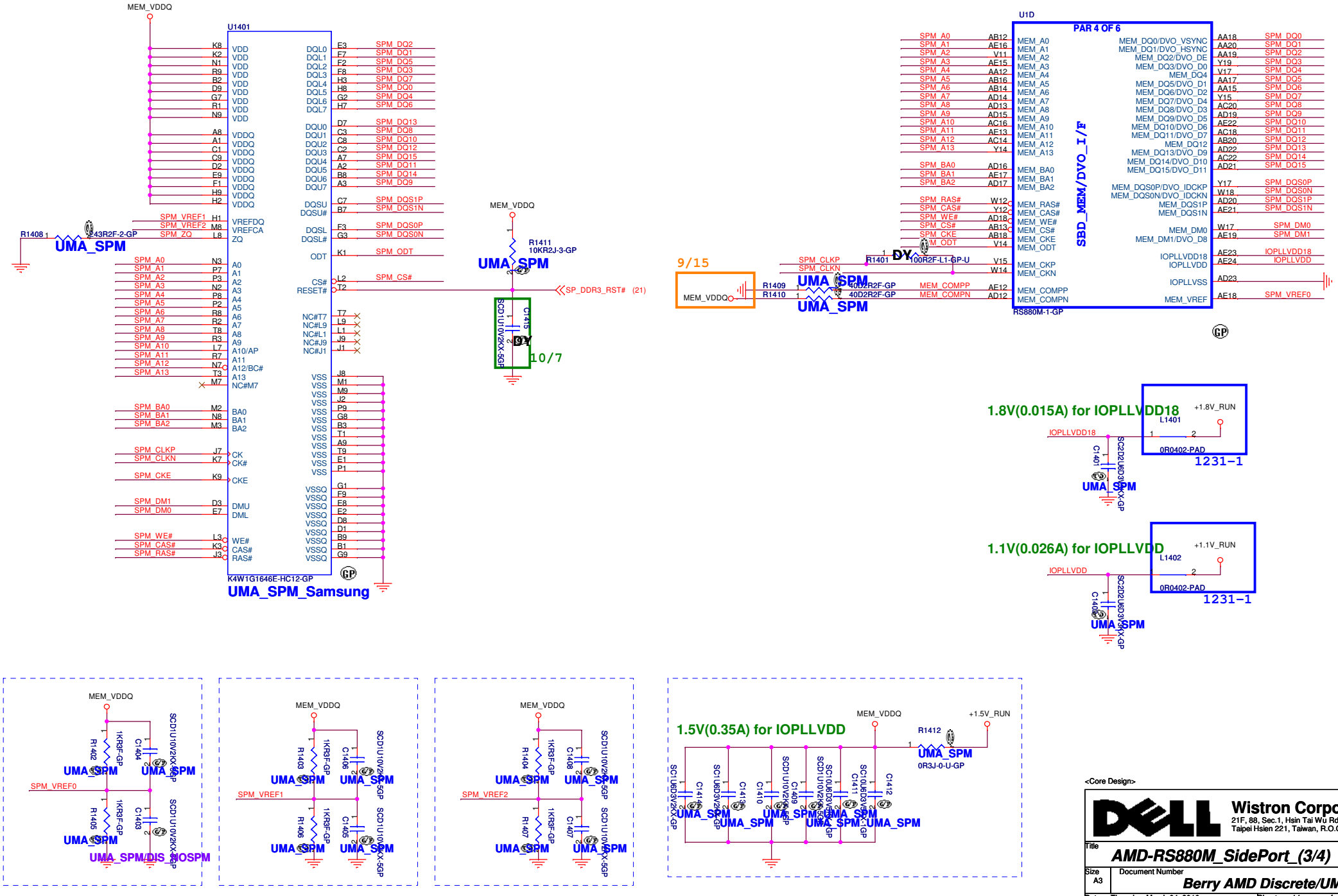
<Core Design>

+3.3V_RUN — 11/6 — R1314 4K7R2J-2-GP — NB_SUS_STAT# — R1321 3KR2J-2-GP DY

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_LVDS&CRT_(2/4)
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00
Date: Thursday, March 04, 2010 | Sheet 13 of 95

SSID = N.B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AMD-RS880M_SidePort_(3/4)	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 14 of 95	

SSID = N.B

1.1V(0.6A) for VDDHT

1.1V(0.7A) for VDDHTRX

1.1V(0.4A) for VDDHTTX

1.8V(0.7A) for VDDA18PCIE

1.8V(0.01A) for VDD18

1.8V(0.025A) for VDD18

1.1V(2.5A) for VDDPCIE

0.95~1.1V(12A) for VDDC

SBD MEM ENABLE

1.5V(0.1A) for VDD_MEM

3.3V(0.06A) for VDD33

PART 5/6 POWER

PART 6/6 GROUND

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_PWR&GD_(4/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 15 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 16 of 95

(Blanking)

<Core Design>

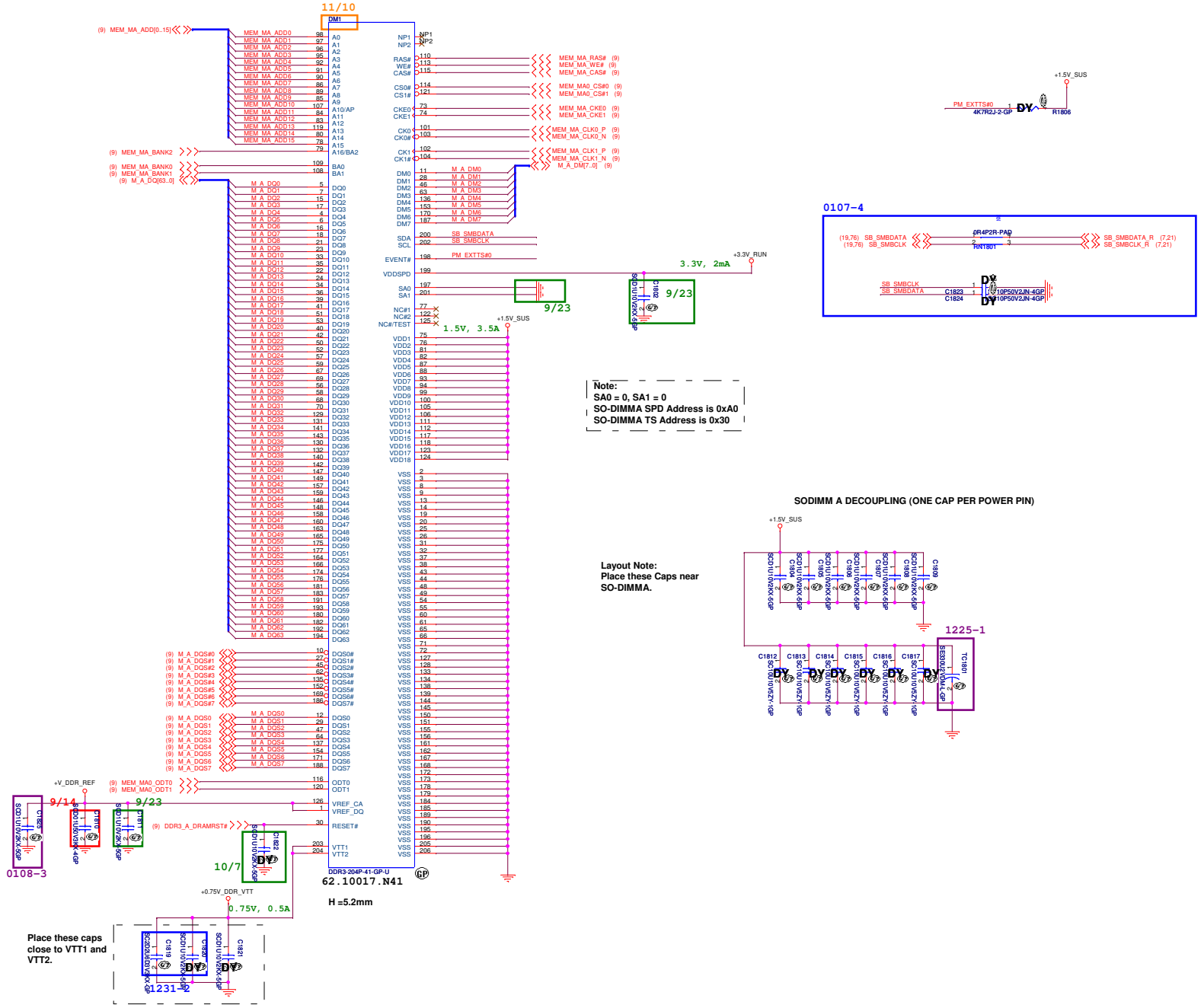
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 17 of 95

SSID = MEMORY



Note:
SA0 = 0, SA1 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

SODIMM A DECOUPLING (ONE CAP PER POWER PIN)

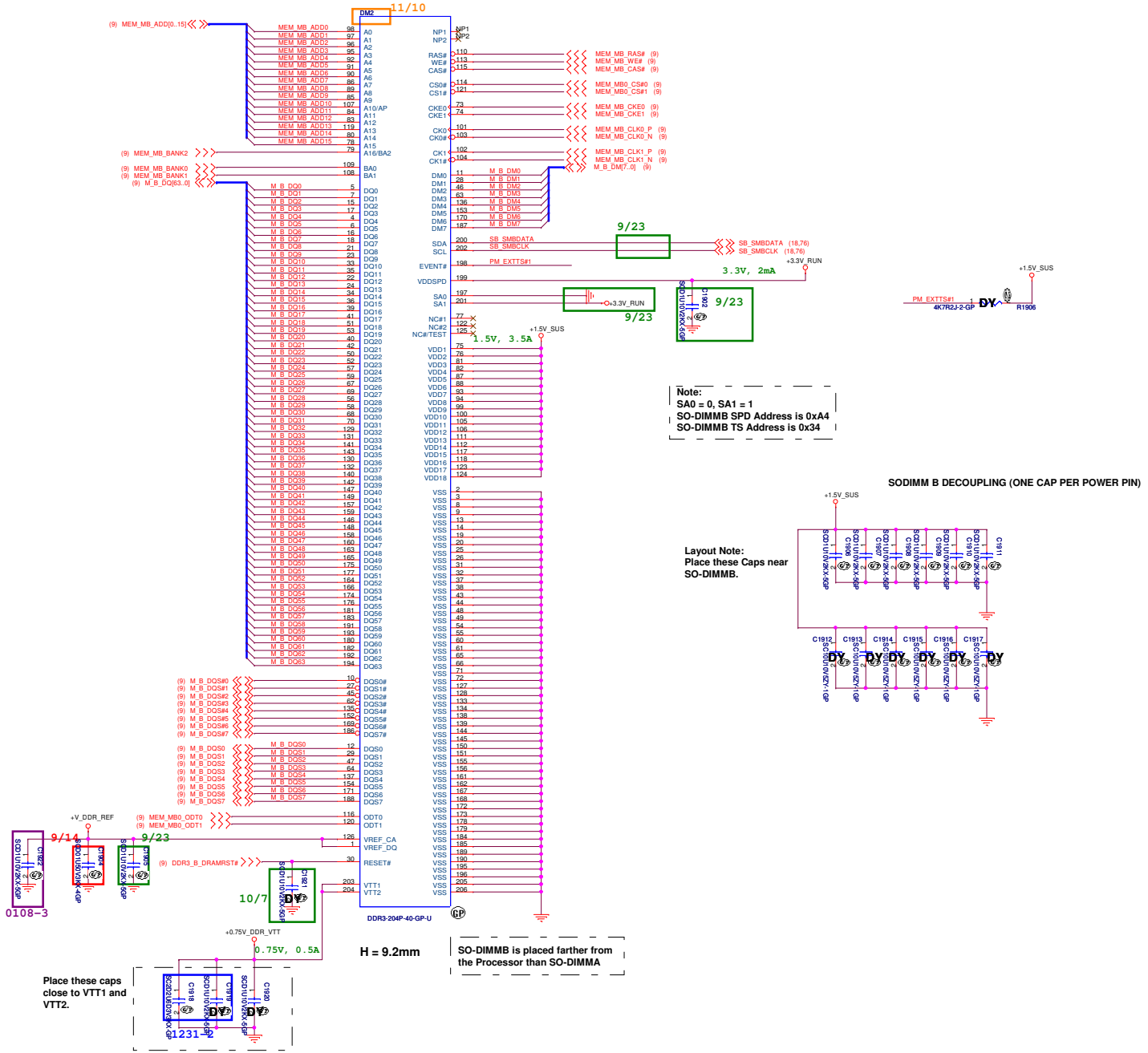
Layout Note:
Place these Caps near SO-DIMMA.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DDR3-SODIMM1		
Size	Document Number	Rev
	Berry AMD Discrete/UMA	A00
Date: Thursday, March 04, 2010	Sheet 18 of 95	

SSID = MEMORY



SODIMM B DECOUPLING (ONE CAP PER POWER PIN)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 19 of 95

SSID = S.B

SB820M : 71.SB820.M02

U2A

Part 1 of 5

SB820M-1-GP

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

PCI CLKS

LPC

CPU

RTC

STRAP PIN

Place R <100mils form pins AD29,AD28

NOTE: SB8XX ONLY SUPPORTS 2 GPP
PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

LPC Bus Routing first connects to MINICARD then connects to KBC

to EC

1nd 82.30020.791
2nd 82.30020.851

<Core Design>

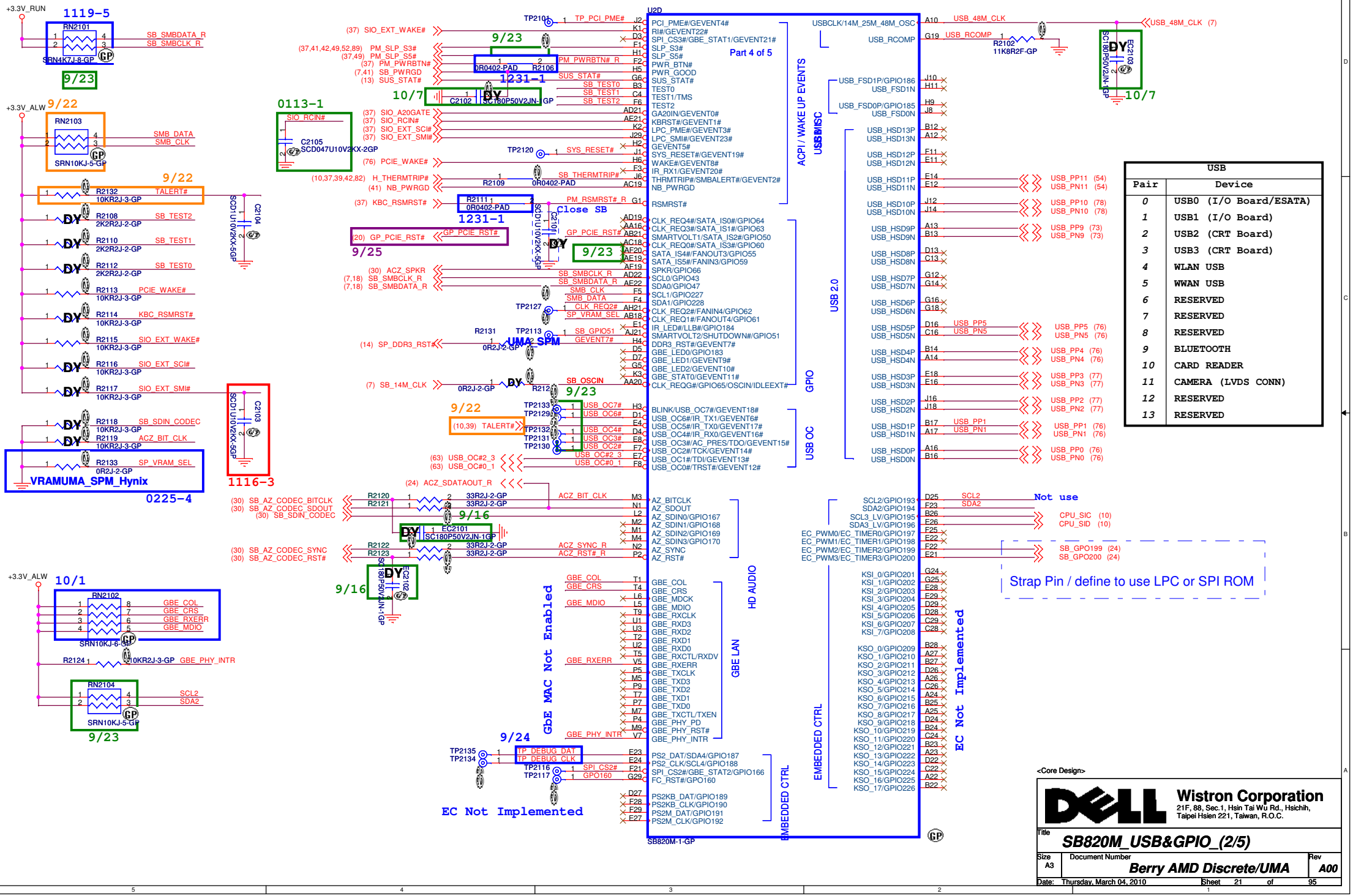
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_PCIE&PCI_(1/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Friday, March 05, 2010 | Sheet 20 of 95

SSID = S.B



USB	
Pair	Device
0	USB0 (I/O Board/ESATA)
1	USB1 (I/O Board)
2	USB2 (CRT Board)
3	USB3 (CRT Board)
4	WLAN USB
5	WWAN USB
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA (LVDS CONN)
12	RESERVED
13	RESERVED

<Core Design>

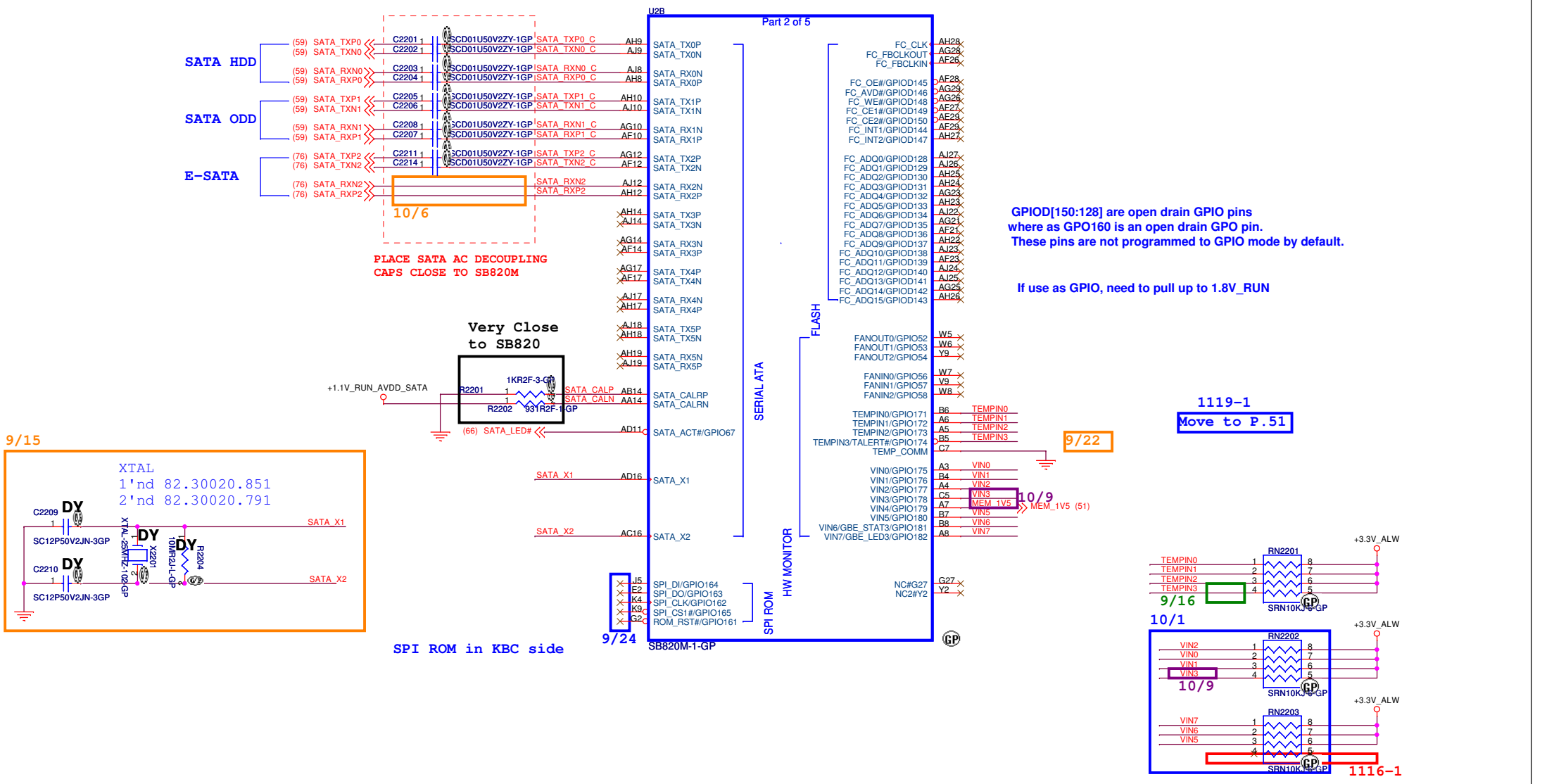
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_USB&GPIO_(2/5)

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 21 of 95

SSID = S.B



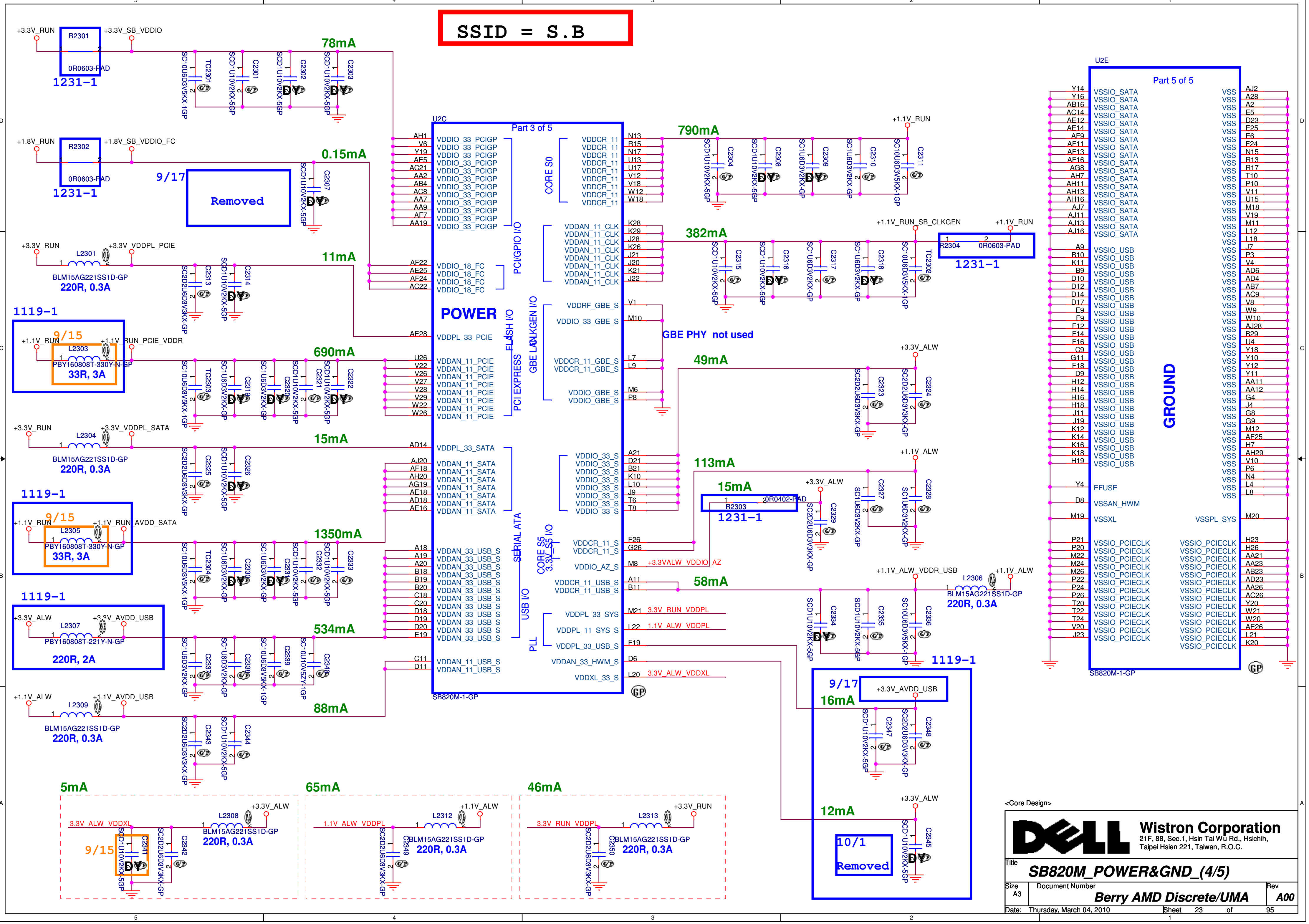
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_SATA-IDE_(3/5)

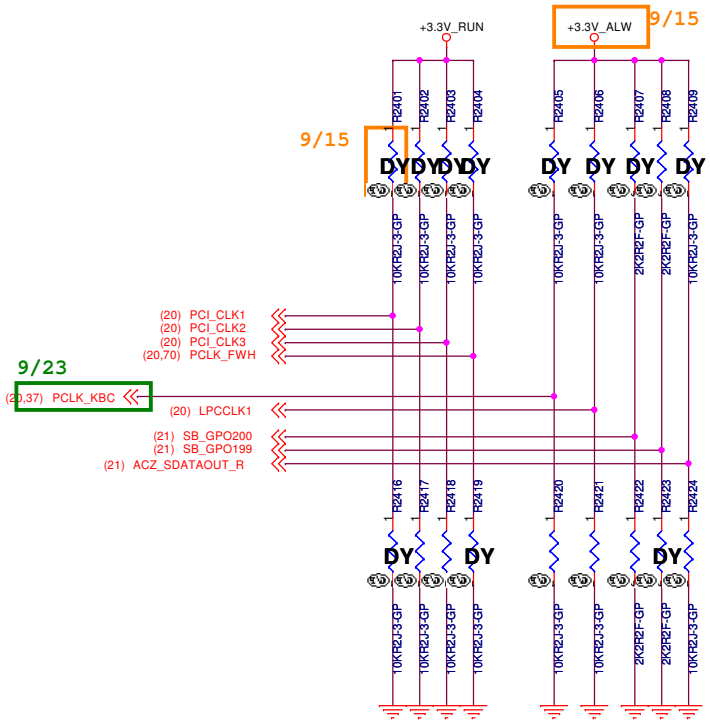
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 22 of 95

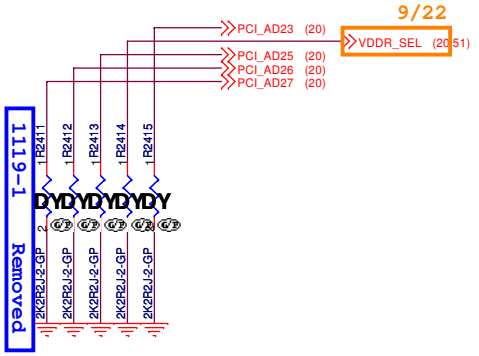

SSID = S.B
U2C
Part 3 of 5
POWER
VDDIO_33_PCIGP
VDDIO_18_FC
VDDPL_33_PCIE
VDDAN_11_PCIE
VDDPL_33_SATA
VDDAN_11_SATA
VDDAN_33_USB_S
VDDAN_11_USB_S
VDDCR_11
VDDAN_11_CLK
VDDRF_GBE_S
VDDIO_33_GBE_S
VDDCR_11_GBE_S
VDDIO_GBE_S
VDDIO_33_S
VDDCR_11_S
VDDIO_AZ_S
VDDCR_11_USB_S
VDDPL_33_SYS
VDDPL_11_SYS_S
VDDPL_33_USB_S
VDDAN_33_HWM_S
VDDXL_33_S
CORE S0
PCI/GPIO I/O
CLKGEN I/O
FLASH I/O
GBE LAN
PCI EXPRESS
SERIAL ATA
CORE S5
3.3V_S5 I/O
USB I/O
PLL
SB820M-1-GP
GBE PHY not used
U2E
Part 5 of 5
GROUND
VSSIO_SATA
VSSIO_USB
EFUSE
VSSAN_HWM
VSSXL
VSSPL_SYS
VSSIO_PCIECLK
VSS
SB820M-1-GP
78mA
0.15mA
11mA
690mA
15mA
1350mA
534mA
88mA
790mA
382mA
49mA
113mA
15mA
58mA
16mA
12mA
5mA
65mA
46mA
1231-1
1119-1
9/17
9/15
10/1
Removed
+3.3V_RUN
+3.3V_SB_VDDIO
+1.8V_RUN
+1.8V_SB_VDDIO_FC
+3.3V_VDDPL_PCIE
+1.1V_RUN
+1.1V_RUN_PCIE_VDDR
+3.3V_VDDPL_SATA
+1.1V_RUN_AVDD_SATA
+3.3V_ALW
+3.3V_AVDD_USB
+1.1V_ALW
+1.1V_AVDD_USB
+1.1V_RUN_SB_CLKGEN
+1.1V_ALW_VDDR_USB
+3.3VALW_VDDIO_AZ
3.3V_RUN_VDDPL
1.1V_ALW_VDDPL
3.3V_ALW_VDDXL
R2301 0R0603-PAD
R2302 0R0603-PAD
R2303 0R0402-PAD
R2304 0R0603-PAD
L2301 BLM15AG221SS1D-GP 220R, 0.3A
L2303 PBY160808T-330Y-N-GP 33R, 3A
L2304 BLM15AG221SS1D-GP 220R, 0.3A
L2305 PBY160808T-330Y-N-GP 33R, 3A
L2307 PBY160808T-221Y-N-GP 220R, 2A
L2309 BLM15AG221SS1D-GP 220R, 0.3A
L2306 BLM15AG221SS1D-GP 220R, 0.3A
L2308 BLM15AG221SS1D-GP 220R, 0.3A
L2312 BLM15AG221SS1D-GP 220R, 0.3A
L2313 BLM15AG221SS1D-GP 220R, 0.3A
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
SB820M_POWER&GND_(4/5)
Size A3
Document Number
Berry AMD Discrete/UMA
Rev A00
Date: Thursday, March 04, 2010
Sheet 23 of 95

SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCLK_KBC (PCI_CLK3)	PCLK_FWH (PCI_CLK4)	LPCCLK0	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	DEFAULT CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820M has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Friday, March 05, 2010 | Sheet 24 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
	Berry AMD Discrete/UMA	***A00***

Date: Thursday, March 04, 2010 Sheet 25 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
	Berry AMD Discrete/UMA	*A00*

Date: Thursday, March 04, 2010 Sheet 26 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 27 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 28 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 29 of 95

SSID = AUDIO

9/23

3.3V, 25mA

Close to codec

Close to codec

84mA

1.4A

1231-1

1231-1

1231-1

9/17

1129-2

11/9

AUD_PC_BEEP
Trace width>15 mils

Close to codec

Reserve

Azalia I/F EMI

Close to Pin13

Close to Pin14

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD79B1

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 30 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 31 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 32 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 33 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 34 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	***Berry AMD Discrete/UMA***	***A00***

(Blanking)

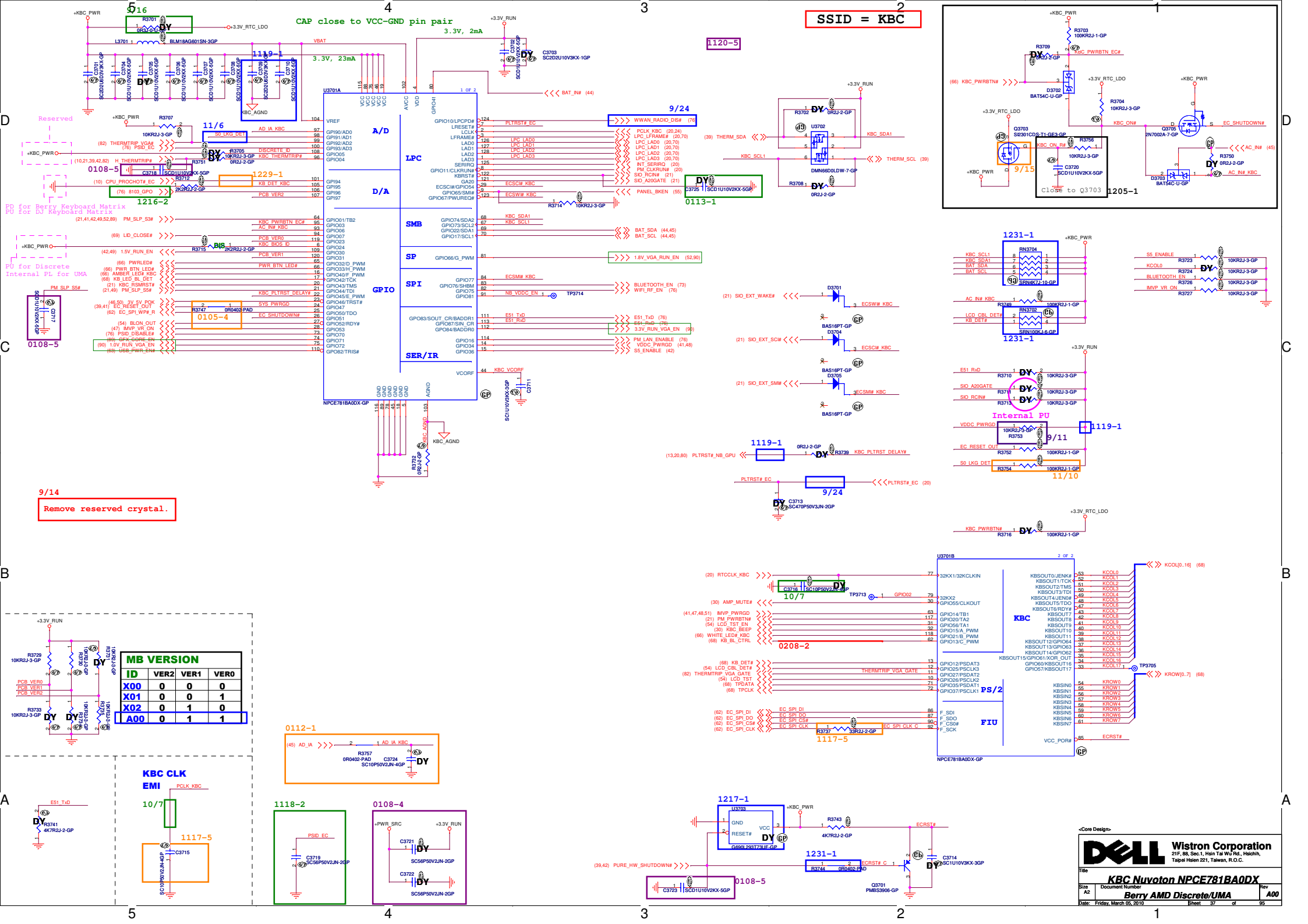
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 36 of 95


SSID = KBC
CAP close to VCC-GND pin pair
3.3V, 2mA
3.3V, 23mA
Reserved
PD for Berry Keyboard Matrix
PU for DJ Keyboard Matrix
PU for Discrete
Internal PL for UMA
U3701A
NPCE781BA0DX-GP
A/D
LPC
D/A
SMB
SP
GPIO
SPI
SER/IR
9/14
Remove reserved crystal.
MB VERSION
ID VER2 VER1 VER0
X00 0 0 0
X01 0 0 1
X02 0 1 0
A00 0 1 1
KBC CLK
EMI
Close to Q3703
Internal PU
U3701B
KBC
PS/2
FIU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
Berry AMD Discrete/UMA
A00
Friday, March 05, 2010

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 38 of 95

SSID = Thermal

+5V_RUN
5V, 600mA
C3901 SC10U10V5KX-2GP
C3902 SCD1U10V2KX-5GP
+3.3V_RUN
R3901 10KR2J-3-GP
R3915 DY 0R2J-2-GP
R3916 10KR2J-3-GP DY
D3901 CH751H-40PT-GP
9/25
EMC2102_FAN_TACH
EMC2102_FAN_TACH (58)
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE (58)
RN3901 SRN4K7J-8-GP
THERM_SCL (37)
THERM_SDA (37)
+3.3V_RUN
R3902 49D9R2F-GP
3.3V, 0.75mA
EMC2102_VDD_3D3
C3903 SCD1U10V2KX-5GP
U3901
EMC2102
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
EMC2102-DZK-GP
Please near to CPU side
(10) H_THERMDC
(10) H_THERMDA
C3910 SC470P50V3JN-2GP DY
C3904 SC470P50V3JN-2GP
1.For CPU Sensor
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
(82) VGA_THERMDC
(82) VGA_THERMDA
0107-5
Removed
C3905 SC470P50V3JN-2GP
EMC2102_DN3
EMC2102_DP3
Q3904 PMBS3904-1-GP UMA
VGA_THERMDC
VGA_THERMDA
0107-3
2.VGA Sensor
Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.
Q3901 PMBS3904-1-GP
C3906 DY SC470P50V3JN-2GP
C3907 SC470P50V3JN-2GP
3.HW T8 sensor
Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
R3905 DY 10KR2J-3-GP
EMC2102_SHDN
R3907 DY 10KR2J-3-GP
EMC2102_FAN_mode
R3910 0R0402-PAD
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
+3.3V_RUN
R3903 DY 0R2J-2-GP
TALERT# (10,21)
0105-4 Remove
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
R3914 DY 0R2J-2-GP
EC_RESET_OUT (37,41)
EM2102_RESET#
ALERT#
CLK_32K
RN3902 SRN10KJ-5-GP
0226-1
R3906 DY 0R2J-2-GP
H_THERMTRIP# (10,21,37,42,82)
THERM_POWER_OK#
THERMTRIP#
1119-1
+KBC_PWR
R3908 10KR2J-3-GP
THERMAL_P_HW_SHT
R3909 10KR2J-3-GP
Q3902 2N7002A-7-GP
PURE_HW_SHUTDOWN# (37,42)
THERM_SYS_SHDN#
V_DEGREE
C3908 SCD1U10V2KX-5GP
R3911 10KR2F-2-GP
TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is 88 deg-C.
C3909 SCD1U10V2KX-5GP
R3912 2K37R2F-GP
32K suspend clock output
Q3903 2N7002A-7-GP
(20) RTC_CLK
CLK_32K_R
R3913 10R2J-2-GP
CLK_32K
C3911 DY SC4D7P50V2CN-1GP
(42) RUN_ENABLE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: A3
Document Number: Berry AMD Discrete/UMA
Rev: A00
Date: Thursday, March 04, 2010
Sheet 39 of 95

(Blanking)

<Core Design>

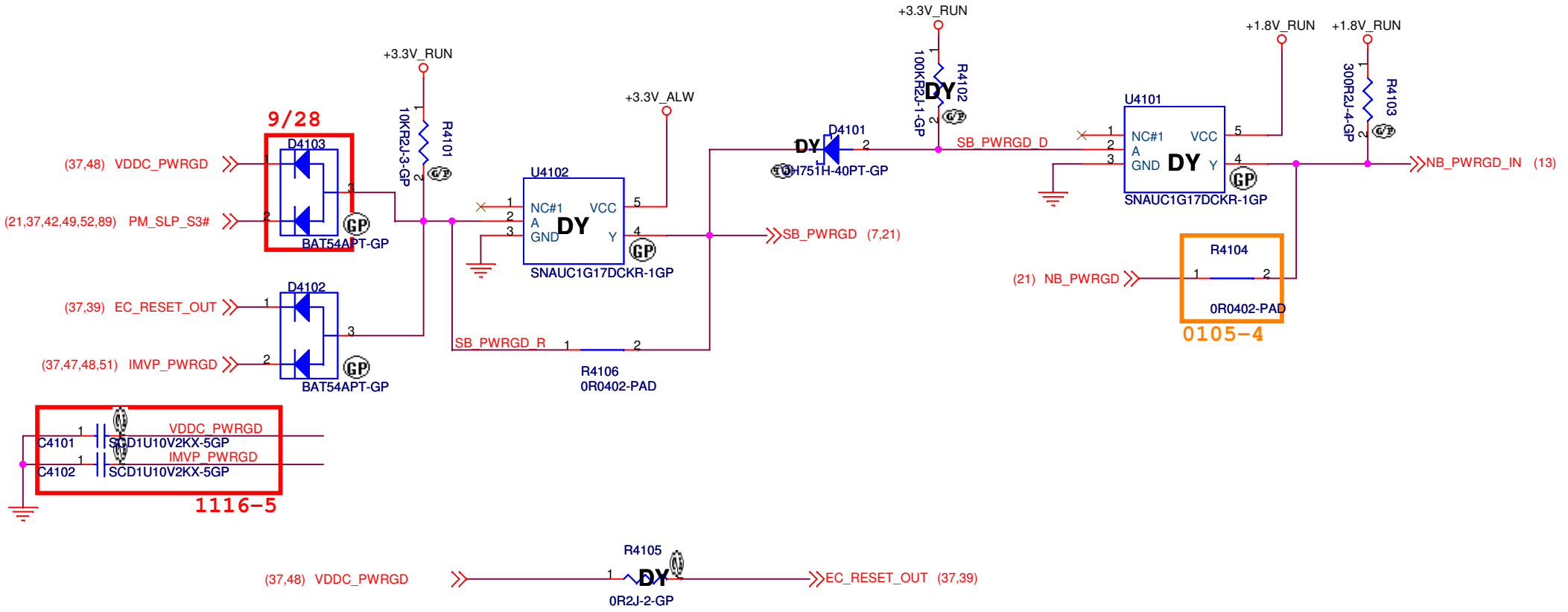
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 40 of 95

SSID = Reset.Suspend



<Core Design>

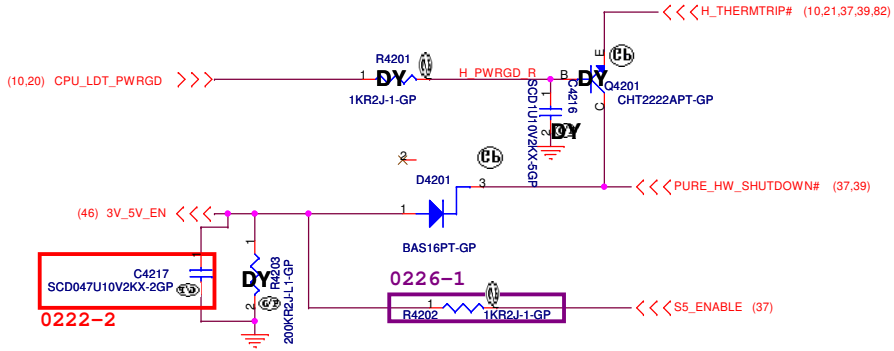
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power On Logic***

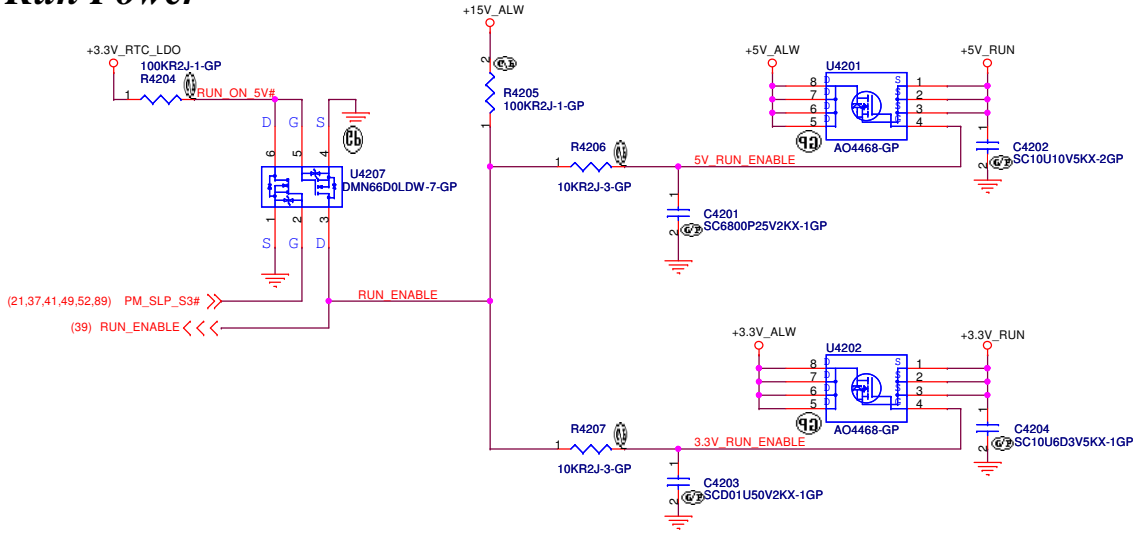
Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	*A00*

Date: Thursday, March 04, 2010 Sheet 41 of 95

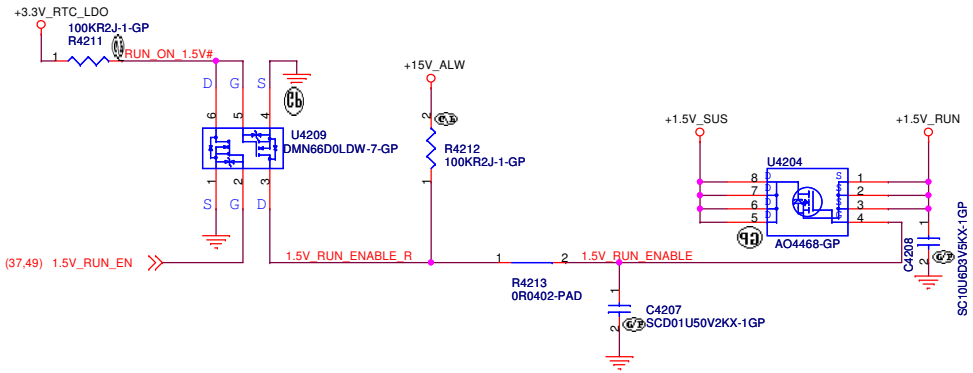
SSID = Reset.Suspend

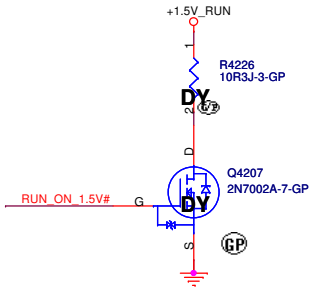


Run Power



1117-2
Remove





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 42 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

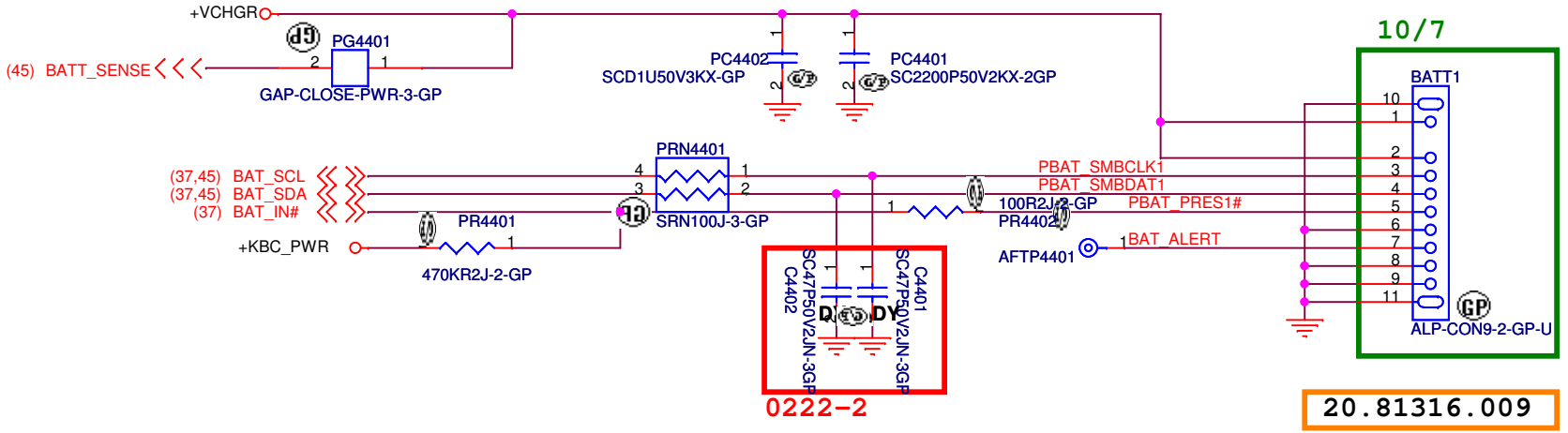
Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 43 of 95

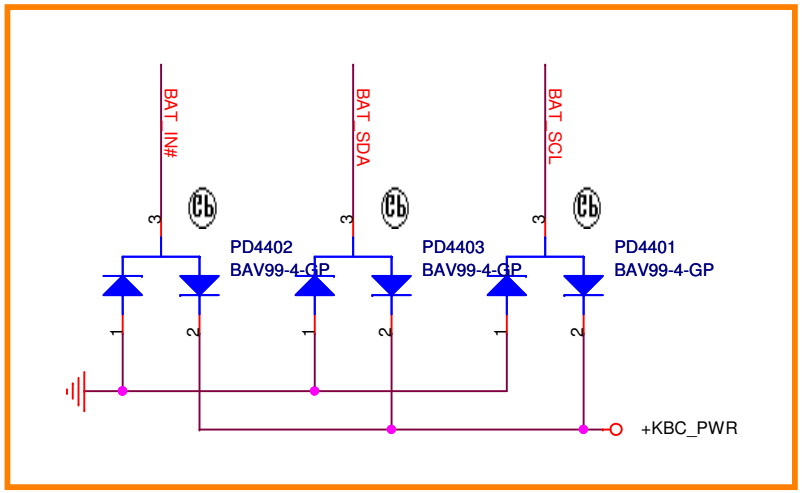
SSID = BATT CONN

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



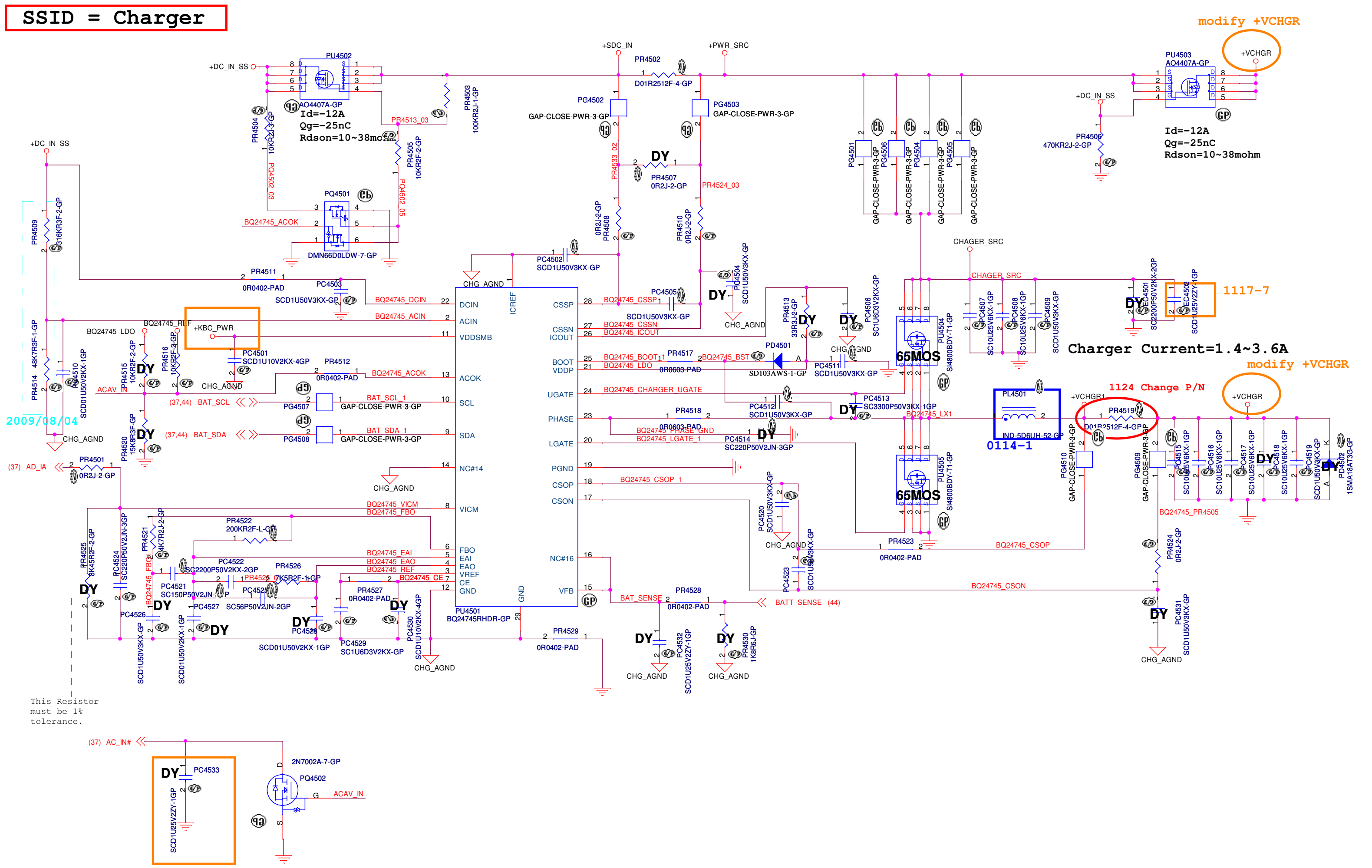
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

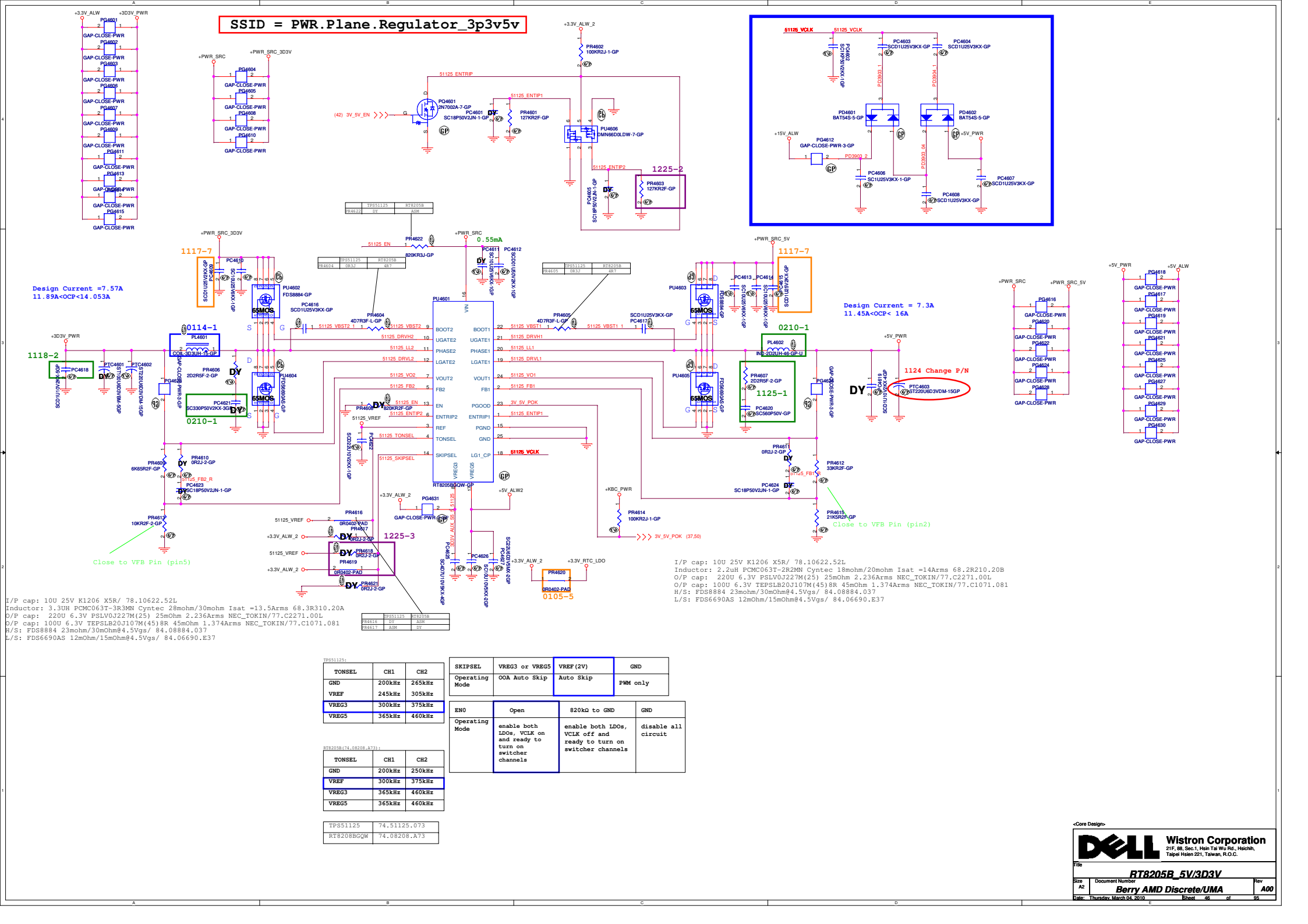
Date: Thursday, March 04, 2010 Sheet 44 of 95



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER BQ24745	
Size A2	Document Number: Berry AMD Discrete/UMA	Rev A00
Date: Monday, March 08, 2010	Sheet 45 of 95	



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8208BGQW	74.08208.A73

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

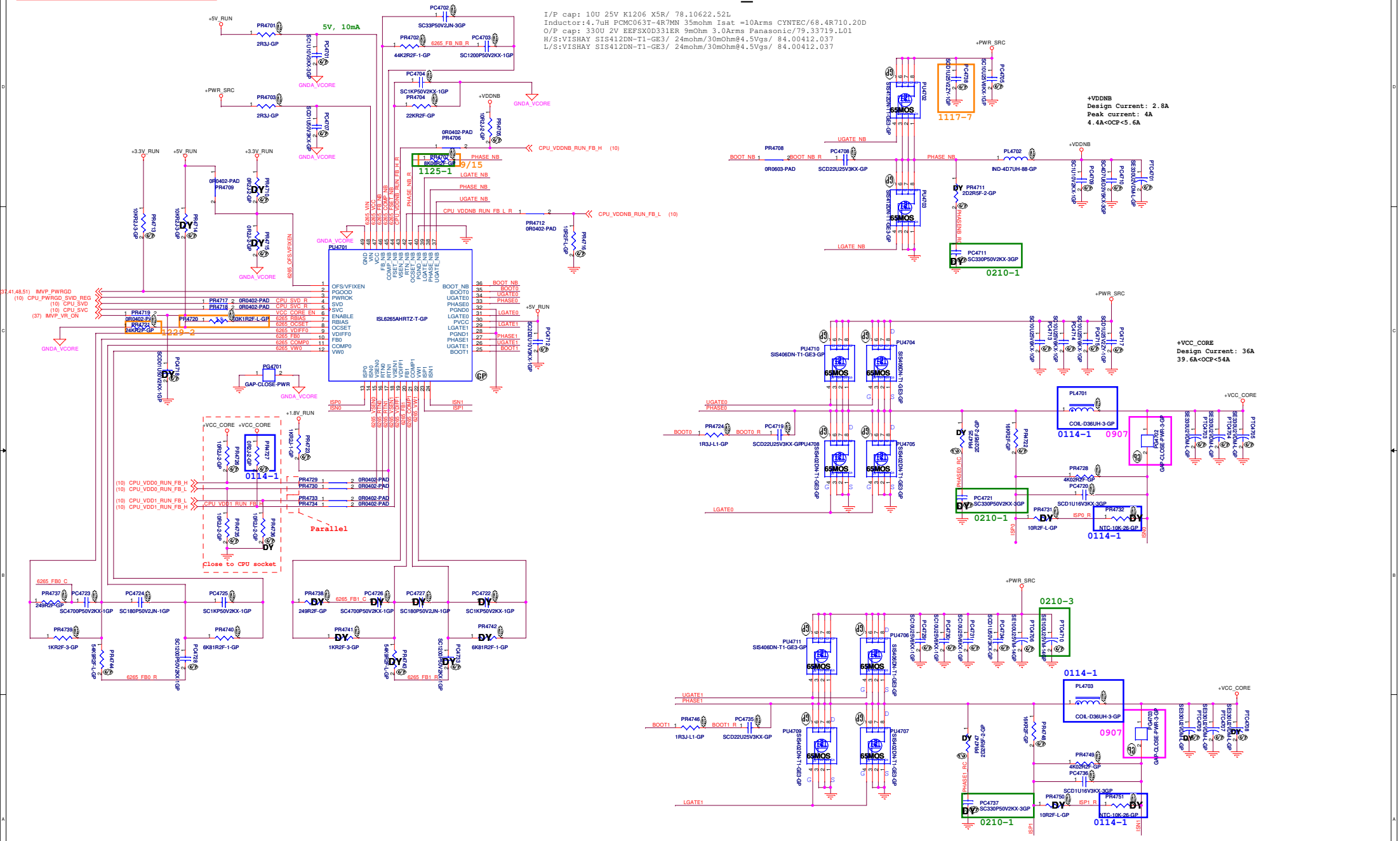
Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 46 of 95

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SiR462DP/ POWERPAK-8.2/810mOhm/ 4.5Vgs/ 84.00462.037
L/S:VISHAY SI7658ADP/ POWERPAK-2.3/ 2.8mOhm/ 4.5Vgs/ 84.07658.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 47 of 95

SSID = PWR.Plane.Regulator_+1.1V_RUN

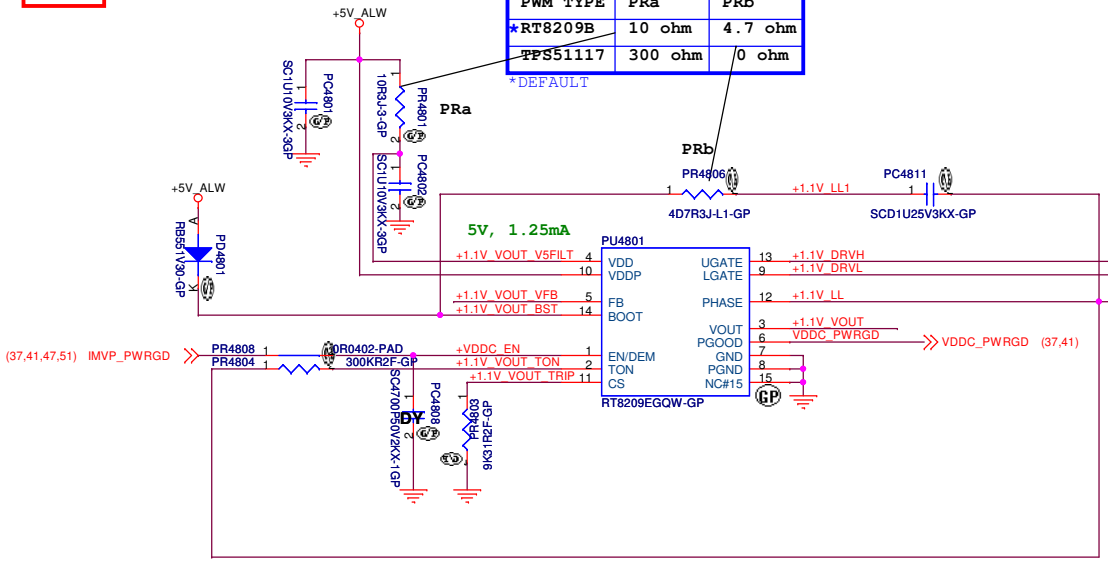
1117-2

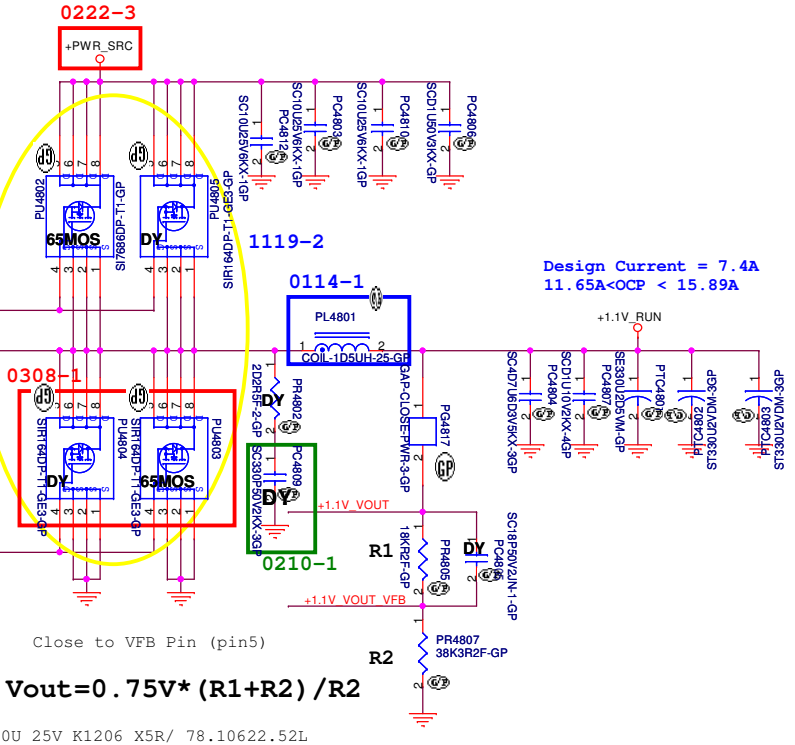
RT8209EGQW for +1.1V_RUN

0222-3 Remove

PWM TYPE	PRa	PRb
*RT8209B	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT





Close to VFB Pin (pin5)

Vout=0.75V*(R1+R2)/R2

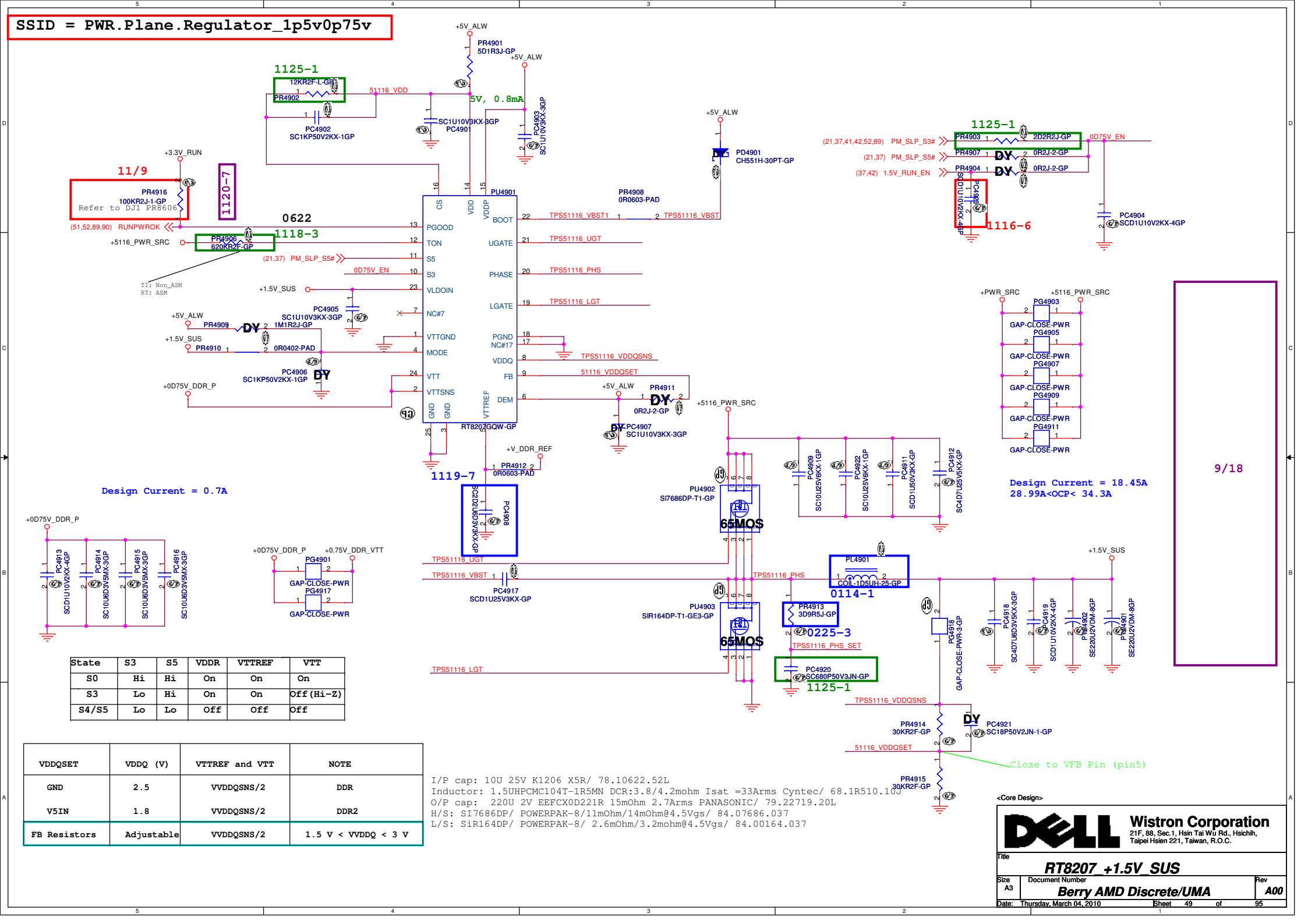
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN 33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E_+1.1V_RUN
Size: A3
Document Number: Berry AMD Discrete/UMA
Rev: A00
Date: Monday, March 08, 2010
Sheet 48 of 95

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207_+1.5V_SUS

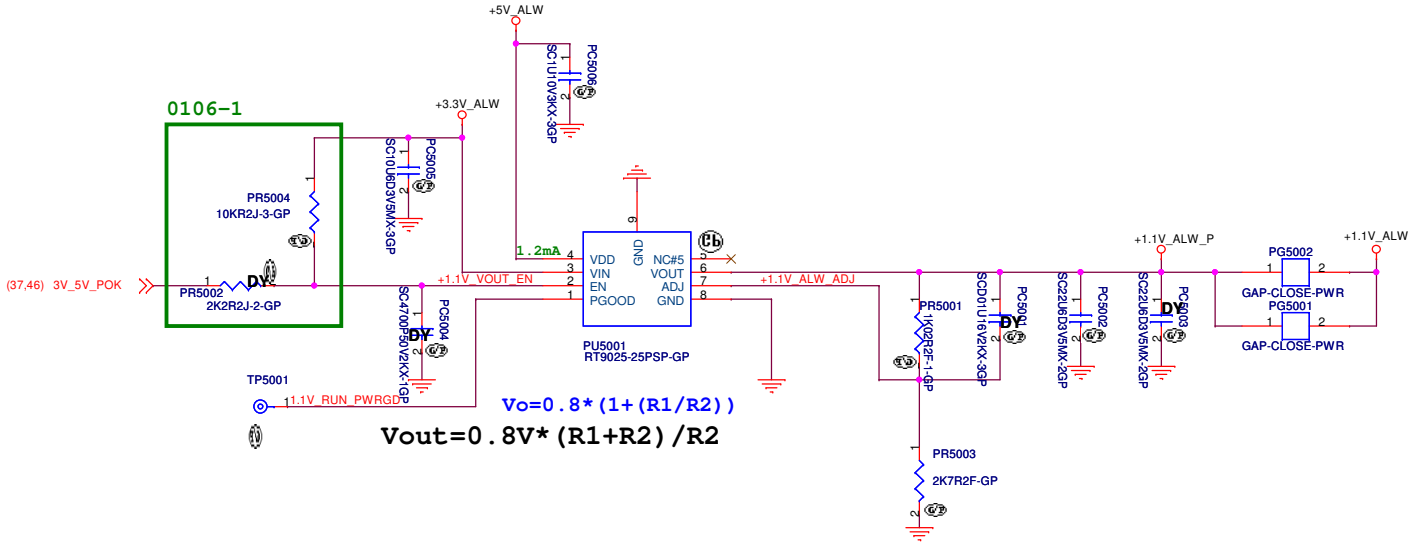
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 49 of 95

SSID = PWR.Plane.Regulator_+1.1V_ALW

1117-2

RT9025 for +1.1V_ALW



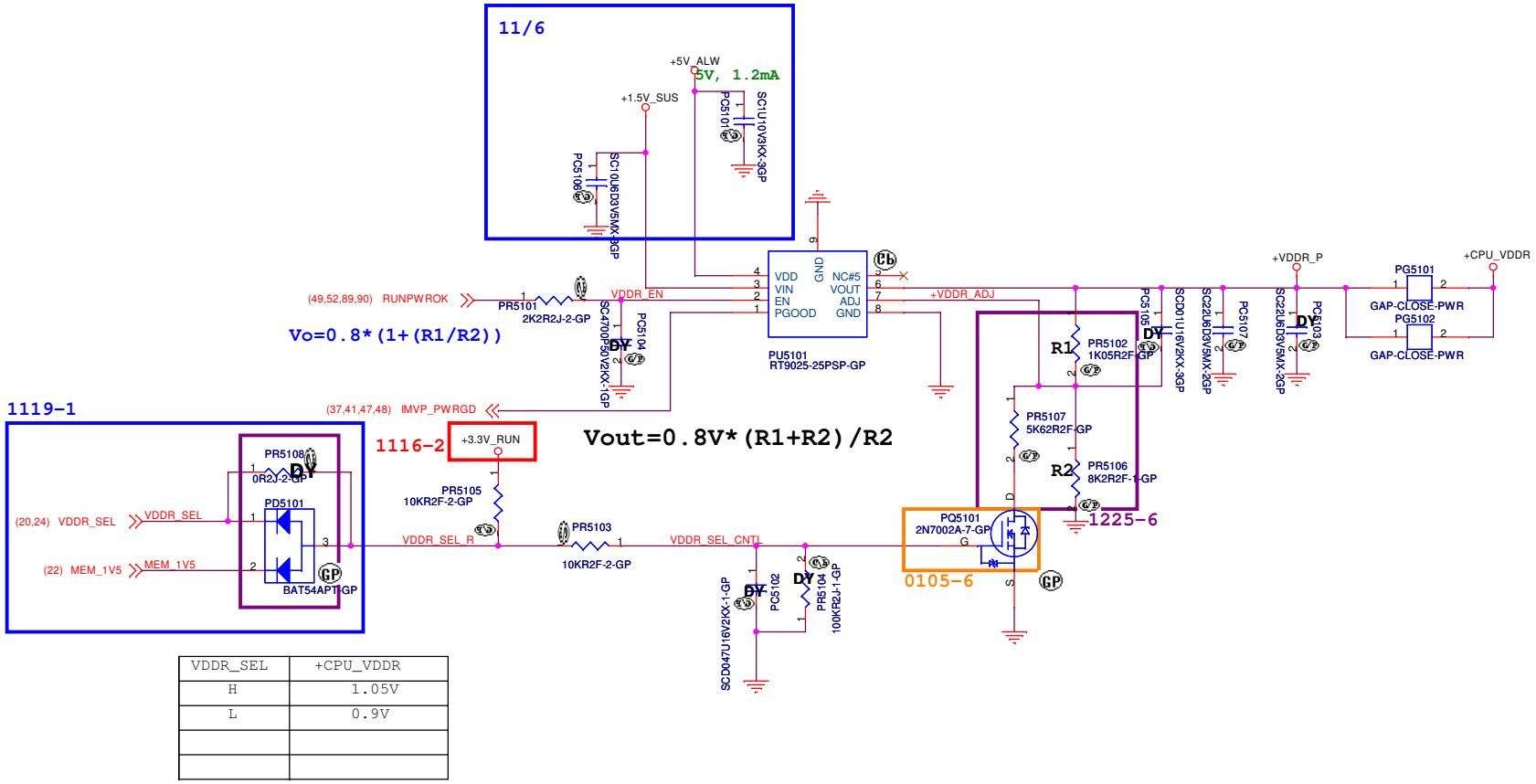
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9025_+1.1V_ALW	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 59 of 95	

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

10/2

+1.5V_RUN +/- 5%
Design Current: 0.805A
Peak current 1.15A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

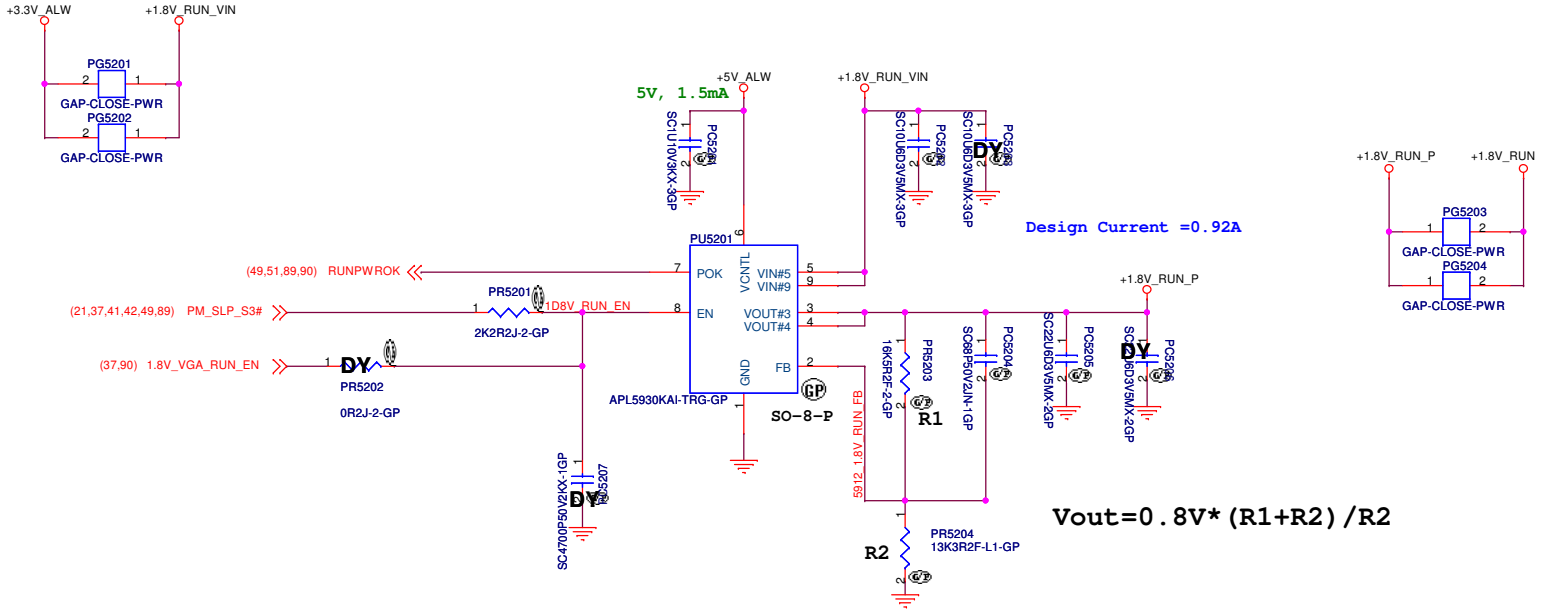
Title: RT9025 +VDDR

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 51 of 95

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

<Core Design>

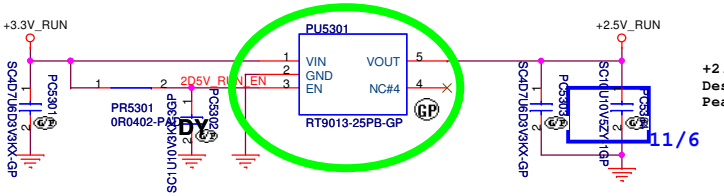
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930_+1.8V_RUN	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 52 of 95	

SSID = PWR.Plane.Regulator_0P9v

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



+2.5V_RUN +/- 5%
Design Current: 175mA
Peak current 250mA

CHECK CURRENT IS ENOUGH OR NOT (CPU)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

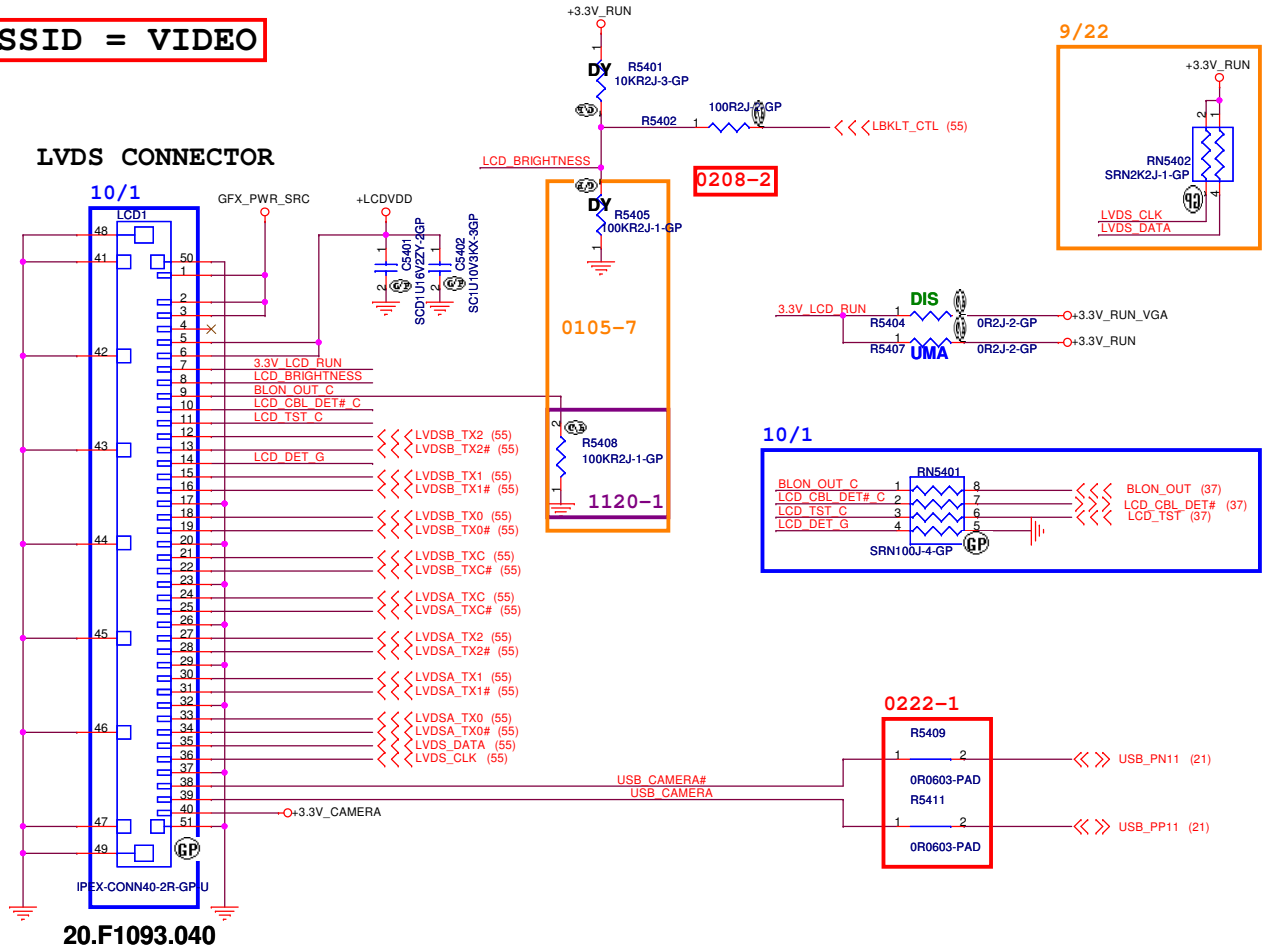
Title: VREG : +CPU_VDDR&+2.5V_RUN

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

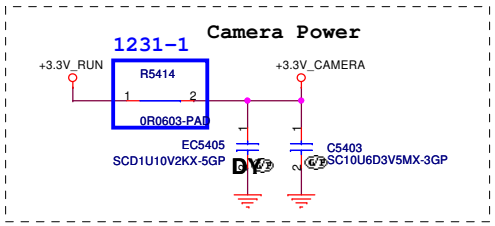
Date: Thursday, March 04, 2010 | Sheet 53 of 95

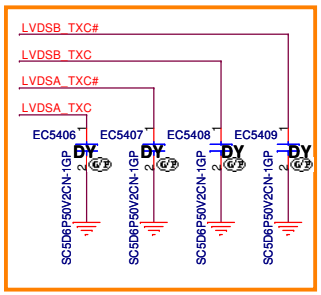
SSID = VIDEO

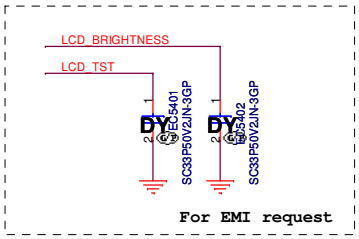
LVDS CONNECTOR



20.F1093.040

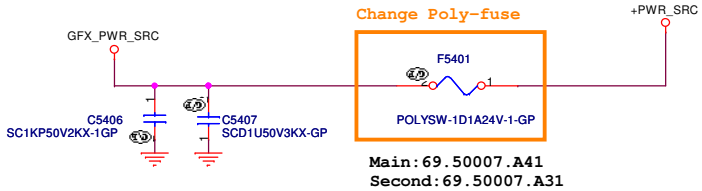






SSID = Inverter

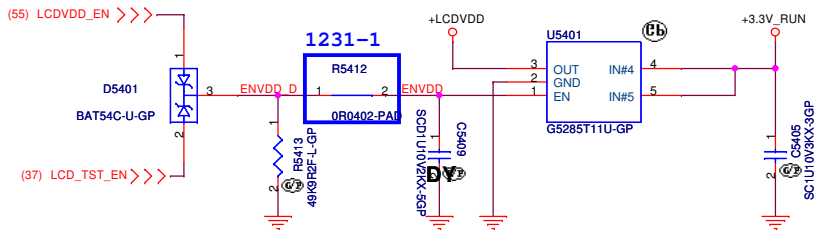
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER



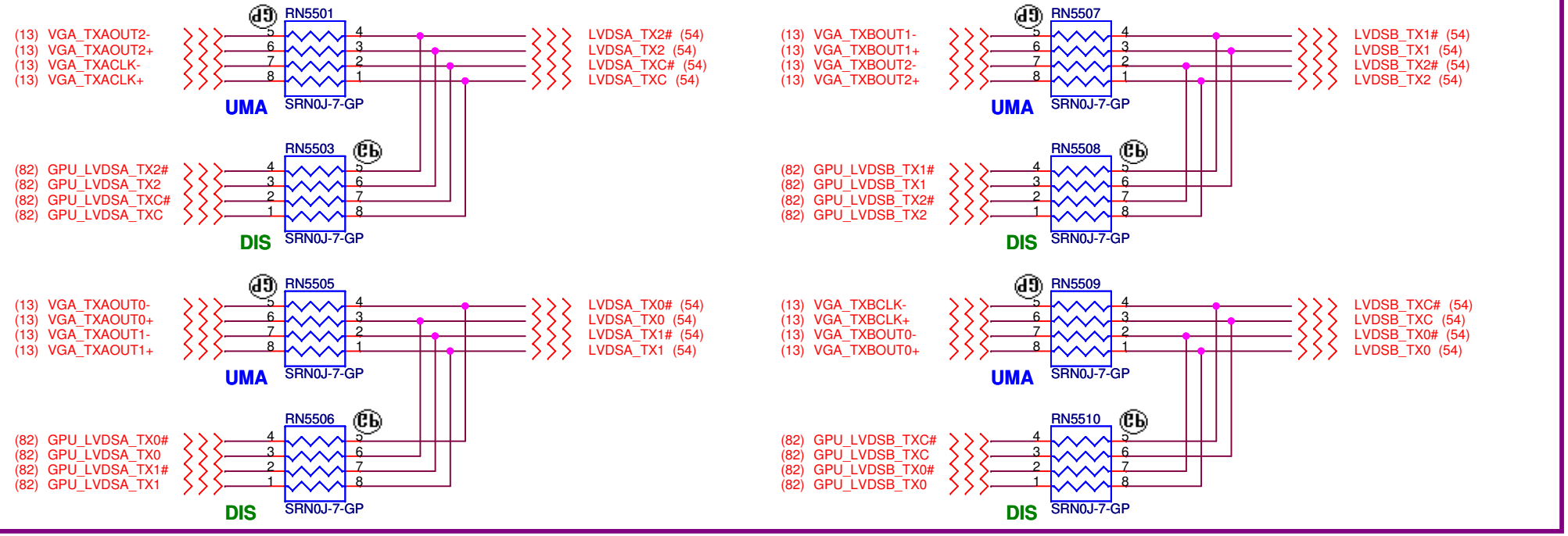
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

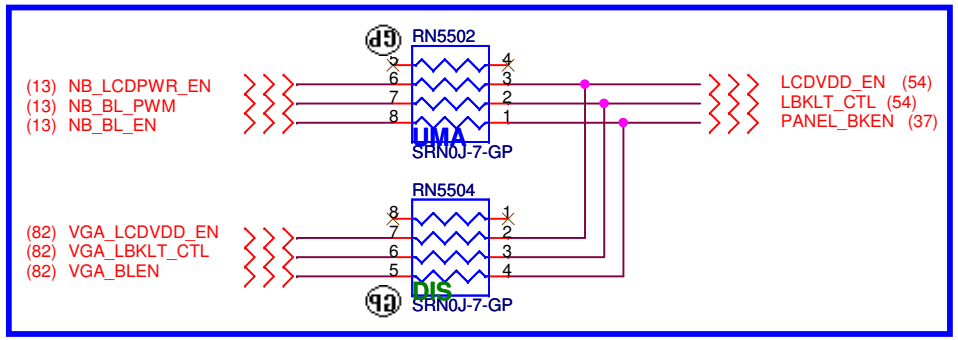
Title	LCD/Inverter Connector	
Size A3	Document Number: Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 54 of 95	

SSID = VIDEO

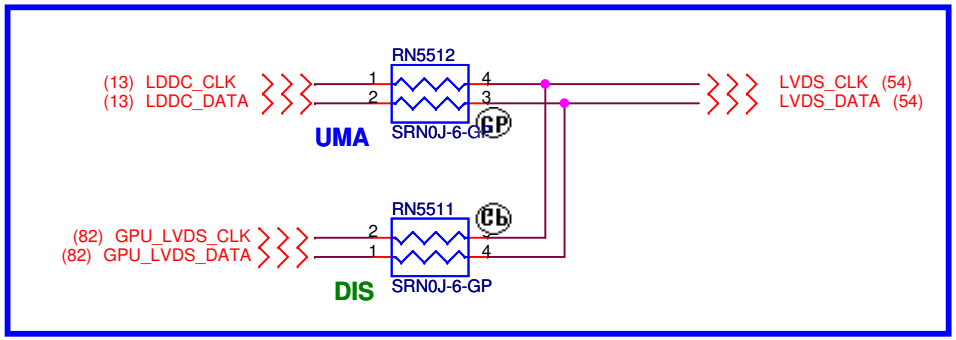
9/18



10/1



10/1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LVDS_Switch***

Size	Document Number	Rev
	Berry AMD Discrete/UMA	***A00***

Date: Thursday, March 04, 2010 Sheet 55 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 56 of 95

SSID = VIDEO

HDMI CONNECTOR

(12) PCIE_NTX_GRX_P[12..15] >>> PCIE_N_H_TX_GRX_P[12..15] (80)

(12) PCIE_NTX_GRX_N[12..15] >>> PCIE_N_H_TX_GRX_N[12..15] (80)

HDMI DISCRETE/ UMA Co-lay

10/1

PCIE_NTX_GRX_N13 PCIE_NTX_GRX_P13 PCIE_NTX_GRX_N12 PCIE_NTX_GRX_P12 → RN5708 SRN0J-7-GP → NB_HDMI_TX0N NB_HDMI_TX0P NB_HDMI_TXCN NB_HDMI_TXCP

NB_HDMI_TXCN NB_HDMI_TXCP NB_HDMI_TX0N NB_HDMI_TX0P → RN5707 SRN0J-7-GP → HDMI_CN_CLK# HDMI_CN_CLK HDMI_CN_DATA0# HDMI_CN_DATA0

PCIE_NTX_GRX_N15 PCIE_NTX_GRX_P15 PCIE_NTX_GRX_N14 PCIE_NTX_GRX_P14 → RN5710 SRN0J-7-GP → NB_HDMI_TX2N NB_HDMI_TX2P NB_HDMI_TX1N NB_HDMI_TX1P

NB_HDMI_TX1N NB_HDMI_TX1P NB_HDMI_TX2N NB_HDMI_TX2P → RN5709 SRN0J-7-GP → HDMI_CN_DATA1# HDMI_CN_DATA1 HDMI_CN_DATA2# HDMI_CN_DATA2

PCIE_NTX_GRX_P12 PCIE_NTX_GRX_N12 PCIE_NTX_GRX_P13 PCIE_NTX_GRX_N13 → RN5706 SRN0J-7-GP → PCIE_N_H_TX_GRX_P12 PCIE_N_H_TX_GRX_N12 PCIE_N_H_TX_GRX_P13 PCIE_N_H_TX_GRX_N13

(82) HDMI_PCH_DATA0# (82) HDMI_PCH_DATA0 (82) HDMI_PCH_CLK# (82) HDMI_PCH_CLK → C5703 C5704 C5709 C5702 DIS SCD1U10V2KX-5GP → HDMI_CN_DATA0# HDMI_CN_DATA0 HDMI_CN_CLK# HDMI_CN_CLK

11/12-3

PCIE_NTX_GRX_P14 PCIE_NTX_GRX_N14 PCIE_NTX_GRX_P15 PCIE_NTX_GRX_N15 → RN5712 SRN0J-7-GP → PCIE_N_H_TX_GRX_P14 PCIE_N_H_TX_GRX_N14 PCIE_N_H_TX_GRX_P15 PCIE_N_H_TX_GRX_N15

(82) HDMI_PCH_DATA2# (82) HDMI_PCH_DATA2 (82) HDMI_PCH_DATA1# (82) HDMI_PCH_DATA1 → C5707 C5708 C5705 C5706 DIS SCD1U10V2KX-5GP → HDMI_CN_DATA2# HDMI_CN_DATA2 HDMI_CN_DATA1# HDMI_CN_DATA1

9/23

HDMI CONN

10/1

22.10296.211

HDMI1 SKT-HDMI19-GP

HDMI_CN_DATA2 → AFTP5703
HDMI_CN_DATA2# → AFTP5705
HDMI_CN_DATA1 → TP5704
HDMI_CN_DATA1# → AFTP5701
HDMI_CN_DATA0 → TP5702
HDMI_CN_DATA0# → AFTP5711
HDMI_CN_CLK → TP5710
HDMI_CN_CLK# → AFTP5708
DDC_CLK_HDMI → AFTP5707
DDC_DATA_HDMI → AFTP5706
HPD_HDMI_CON → AFTP5713
AFTP5709

+5V_RUN → AFTP5712 → C5701 SCD1U10V2KX-5GP

9/15

+5V_RUN

10/5

RN5701 SRN4K7J-8-GP

5V Tolerance

(13) NB_DDC_CLK0 (13) NB_DDC_DATA0 → RN5714 SRN0J-6-GP → DDC_CLK_HDMI

(82) GPU_HDMI_CLK (82) GPU_HDMI_DATA → RN5713 SRN0J-6-GP → DDC_DATA_HDMI

HDMI_CN_CLK# HDMI_CN_CLK HDMI_CN_DATA0# HDMI_CN_DATA0 HDMI_CN_DATA1# HDMI_CN_DATA1 HDMI_CN_DATA2# HDMI_CN_DATA2 → 499R2F-2-GP → R5715 R5716 R5717 R5718 R5719 R5720 R5721 R5722

+5V_RUN

R5724 0R0402-PAD

HDMI_PLL_GATE → R5714 100KR2J-1-GP

Q5703 2N7002A-7-GP

HDMI_PLL_GND

9/22

+3.3V_RUN

Q5702 PMBS3904-1-GP

HPD_HDMI_1 → R5710 150KR2J-L1-GP → HPD_HDMI_CON

(13,82) HDMI_HPD_DET → R5713 10KR2J-3-GP

R5712 DY 200KR2J-L1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

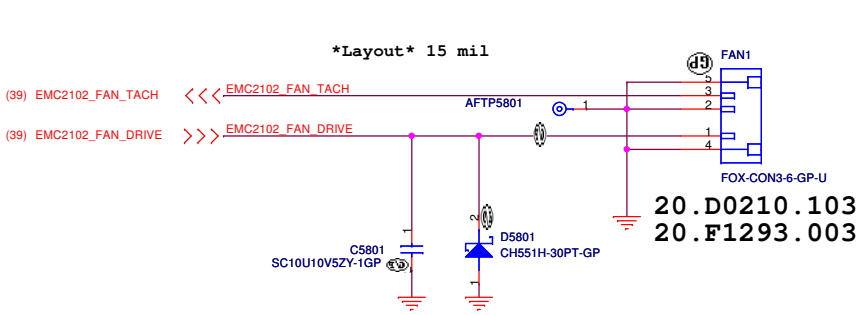
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

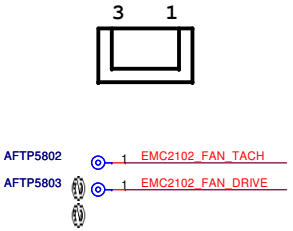
Date: Thursday, March 04, 2010 | Sheet 57 of 95

SSID = User.Interface

SSID = Thermal

Fan Connector





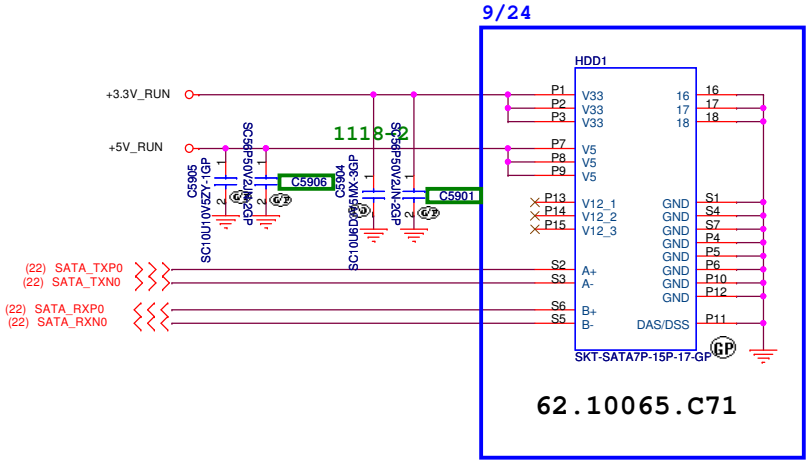
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

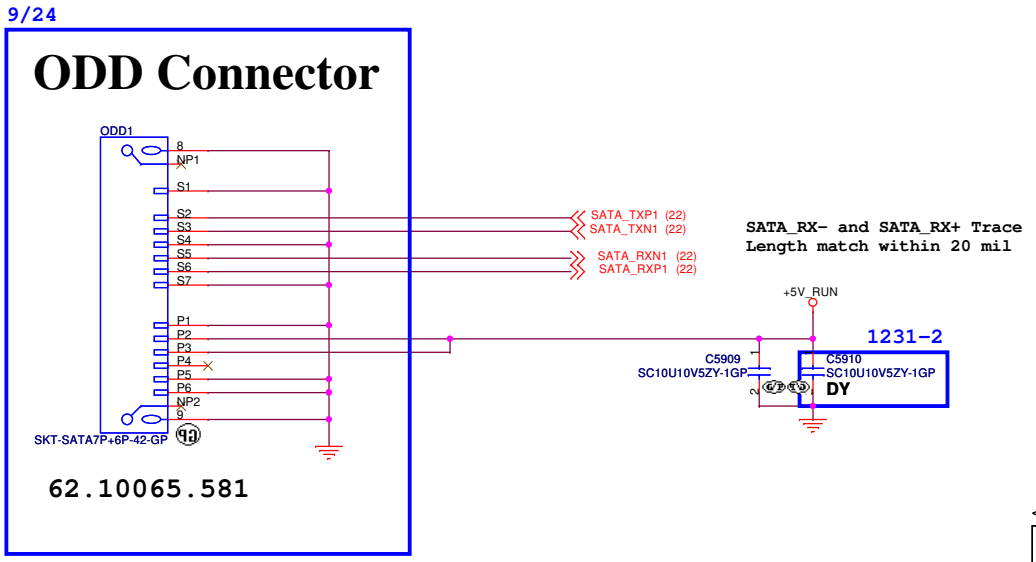
Title: ITP/Fan Connector		
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 58 of 95	

SSID = SATA

SATA HDD Connector



ODD Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

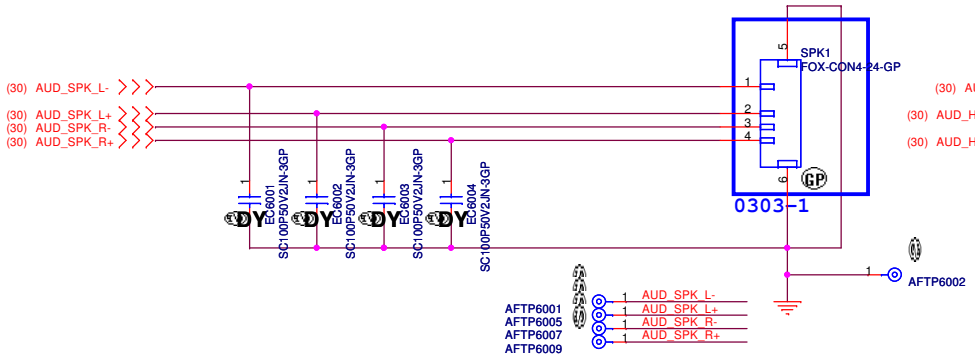
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 59 of 95

SSID = AUDIO

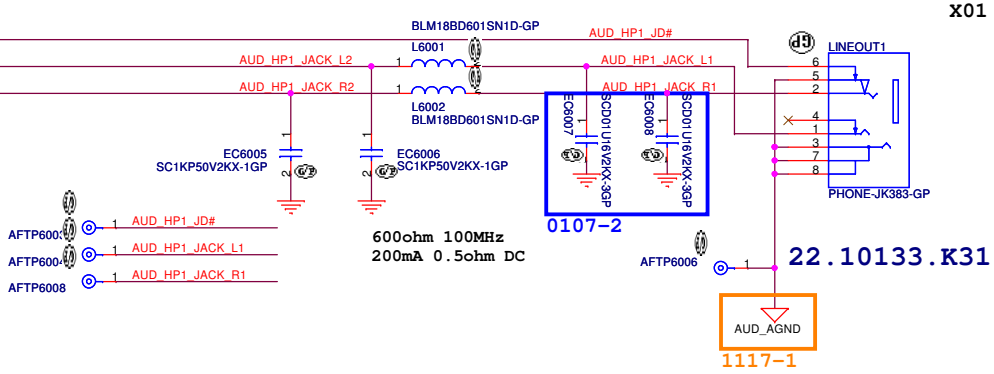
Speaker Connector

Main 20.F0693.004
SEC. 20.F0693.004

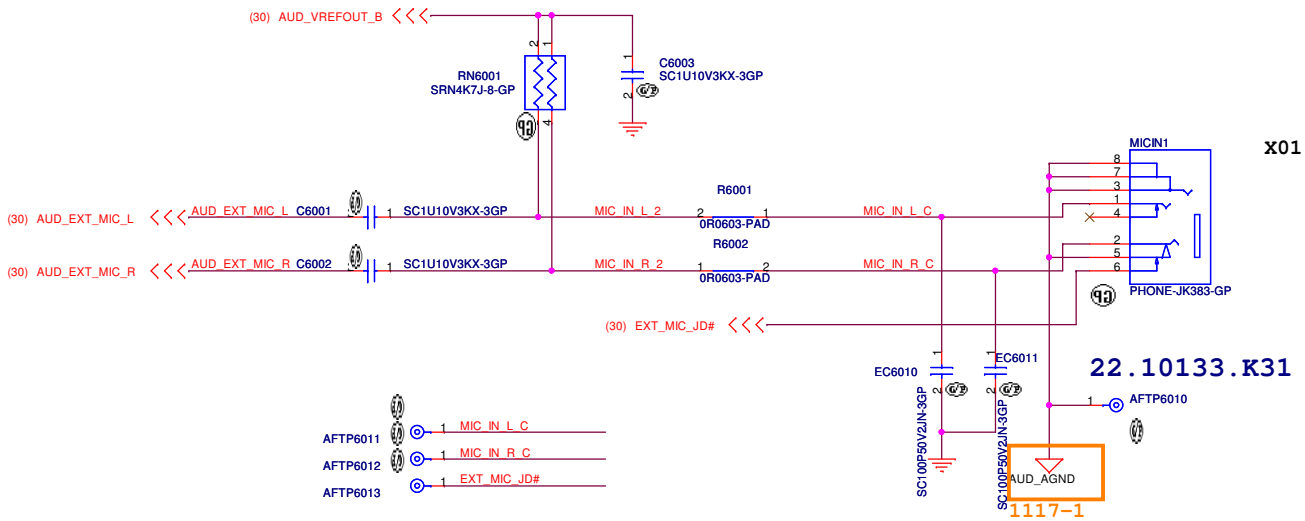


LINE1 OUT

X01 0713

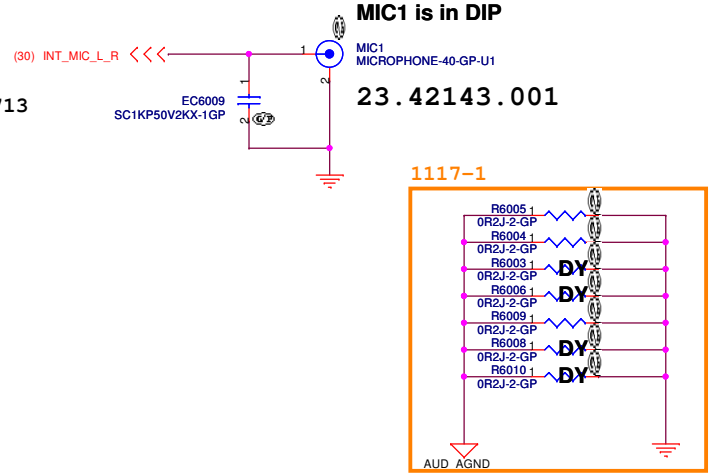


MIC IN



Internal Microphone

X01 0713



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 60 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

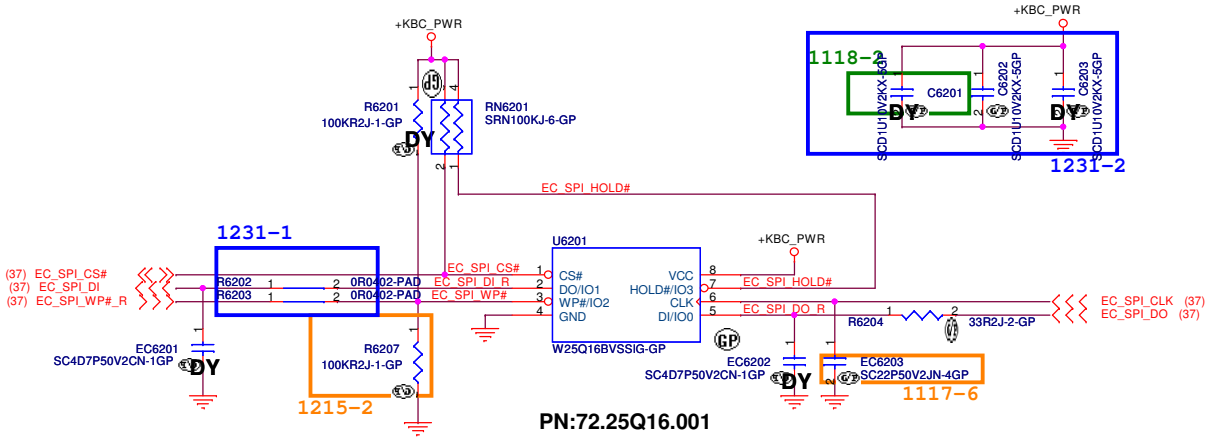
Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 61 of 95

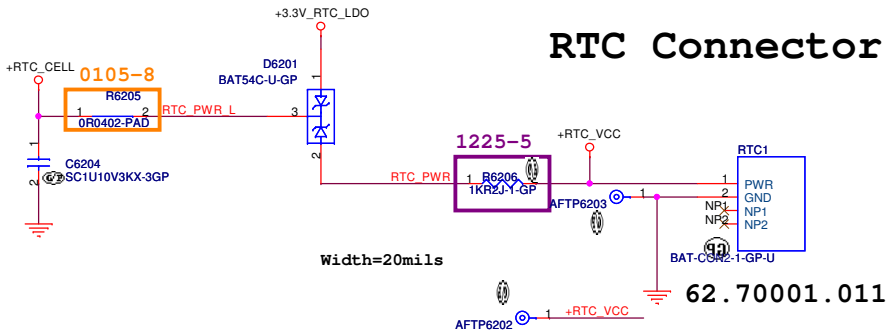
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

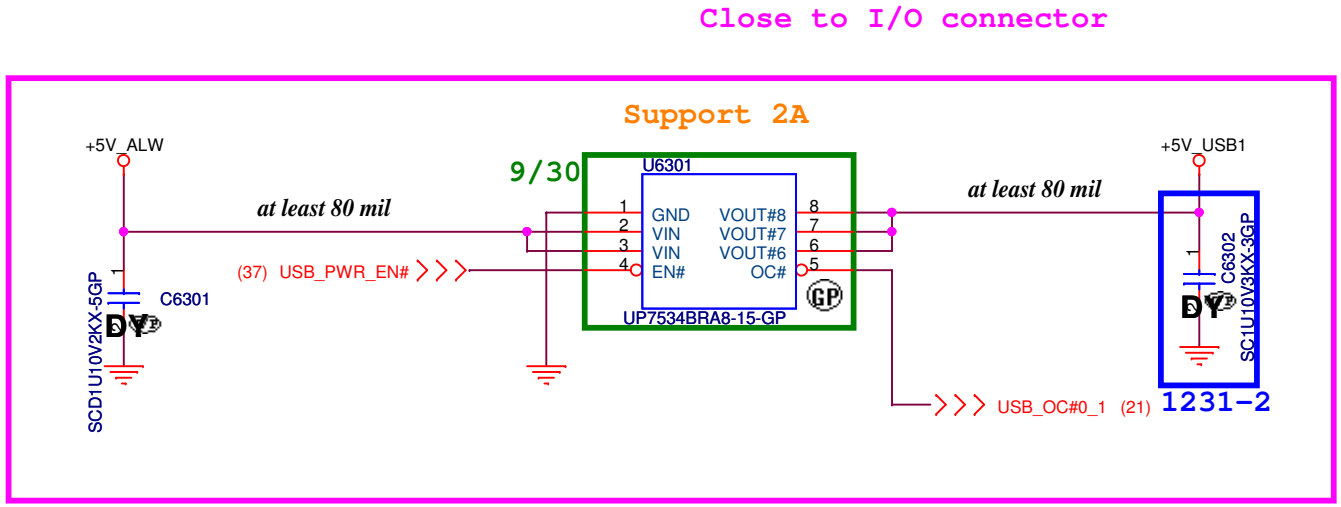
Title: Flash/RTC

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

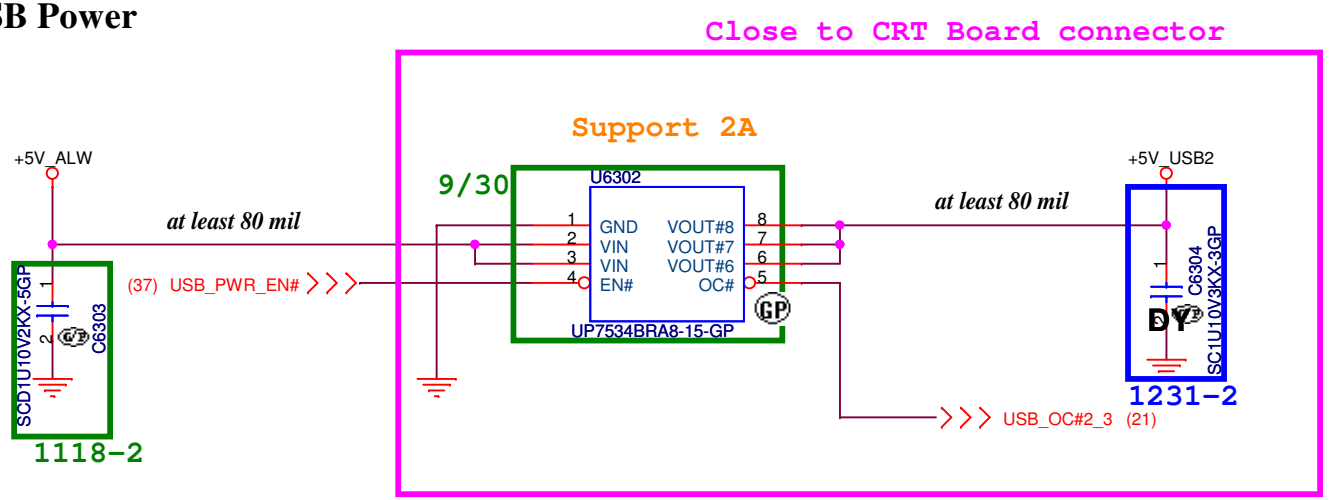
Date: Thursday, March 04, 2010 Sheet 62 of 95

SSID = USB

IO Board USB Power



CRT Board USB Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB Power SW***	
Size	Document Number: ***Berry AMD Discrete/UMA***	Rev: ***A00***
Date: Thursday, March 04, 2010	Sheet 63 of 95	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 64 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

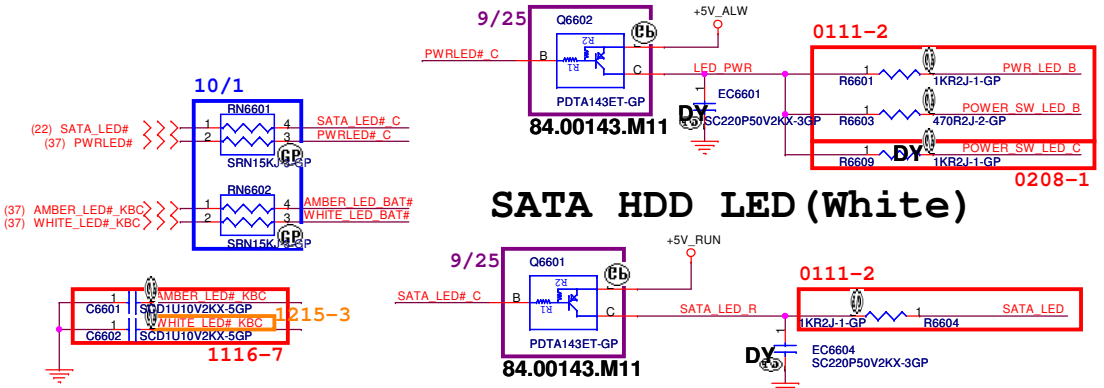
Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 65 of 95

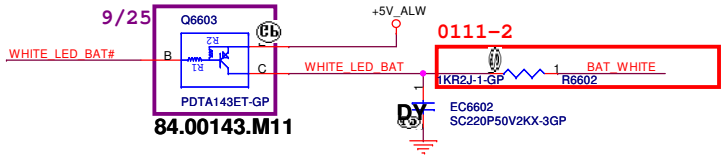
SSID = User.Interface

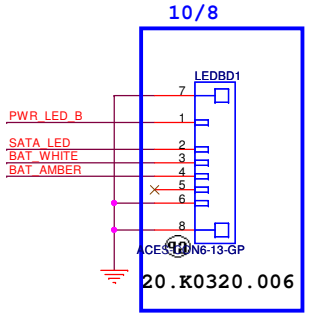
Power LED(White)



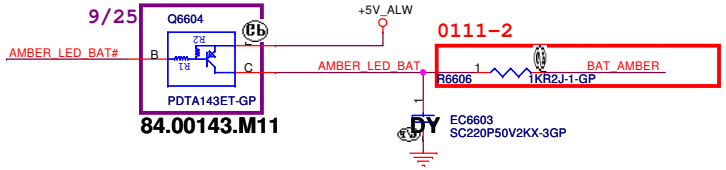
SATA HDD LED(White)

Battery LED1(White)

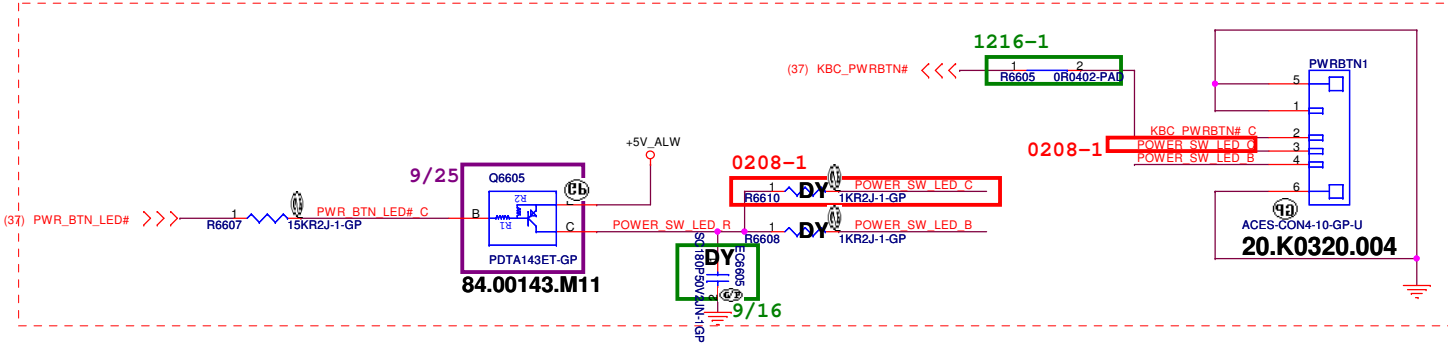




Battery LED2(Amber)



Power button LED(White)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A3	Berry	A00

Date: Thursday, March 04, 2010 Sheet 66 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

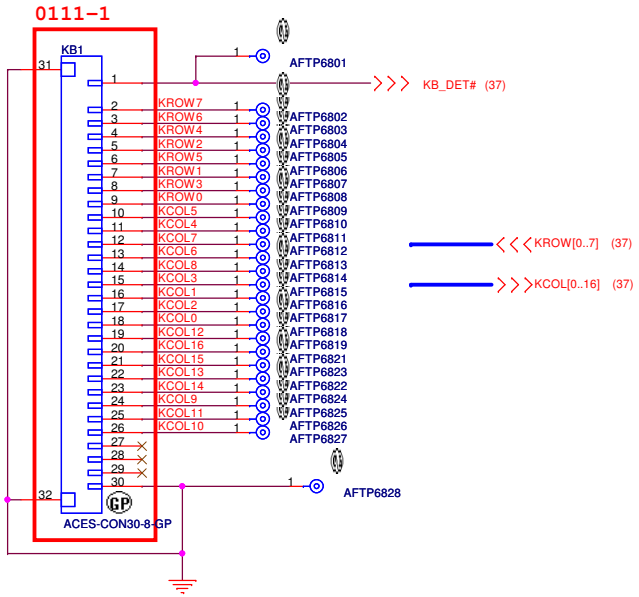
Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 67 of 95

SSID = KBC

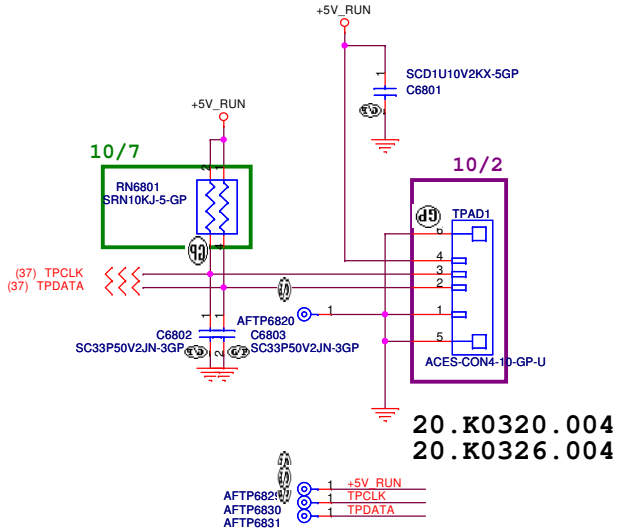
Internal KeyBoard Connector



20.K0524.030
20.K0461.030

SSID = Touch.Pad

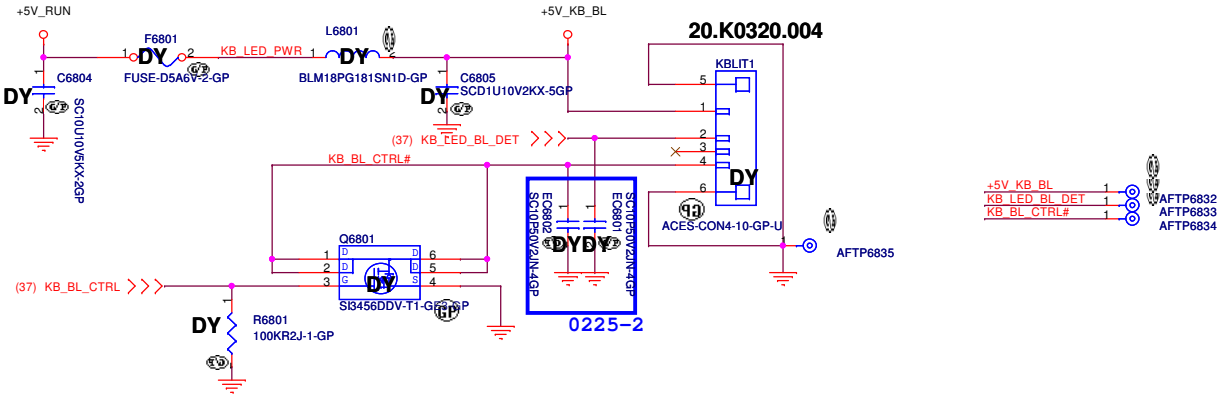
TouchPad Connector



20.K0320.004
20.K0326.004

KB Backlight Connector

0208-2

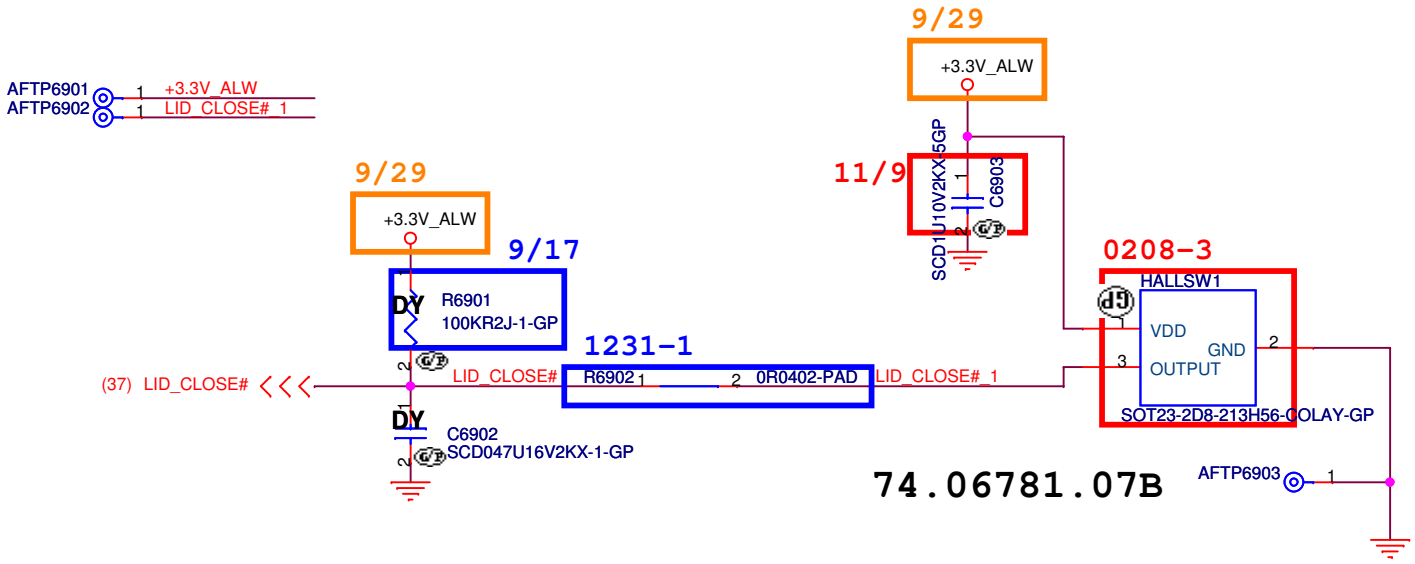


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 68 of 95	

SSID = Hall.Sensor



<Core Design>

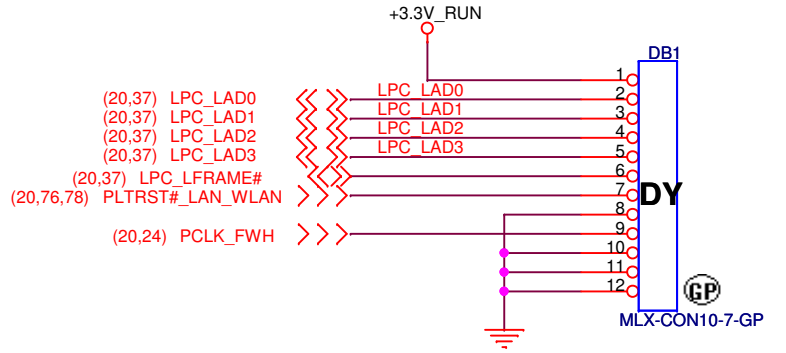
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Effect Sensor***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 69 of 95

SSID = Debug



20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 70 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 71 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

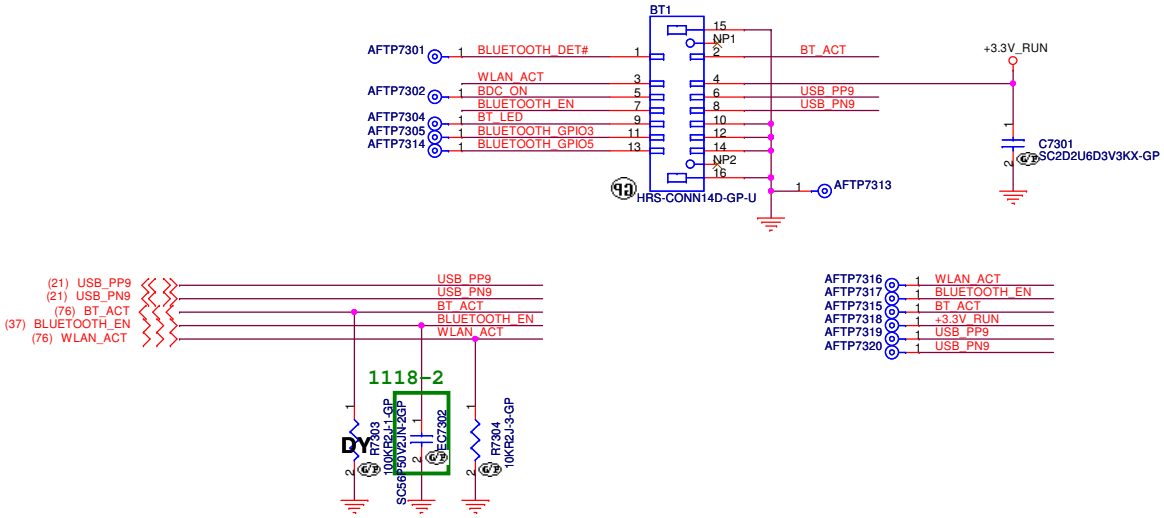
Title
RESERVED

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 72 of 95

SSID = User.Interface

Bluetooth Module conn.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Bluetooth		
Size: A3	Document Number: Berry	Rev: A00
Date: Thursday, March 04, 2010	Sheet 73 of 95	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 74 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

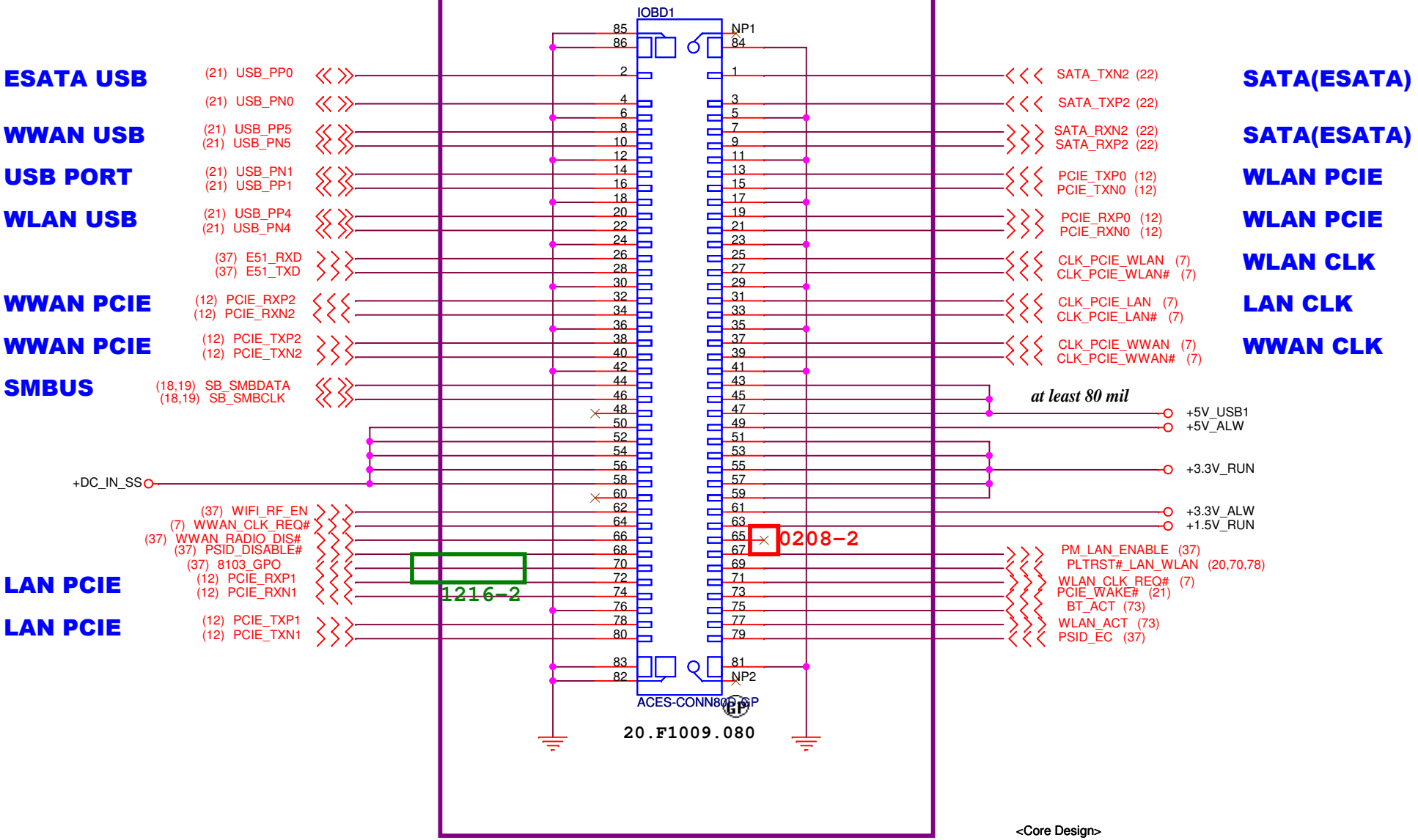
Reserved

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 75 of 95

SSID = Int.Conn

10/9



0107-6

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

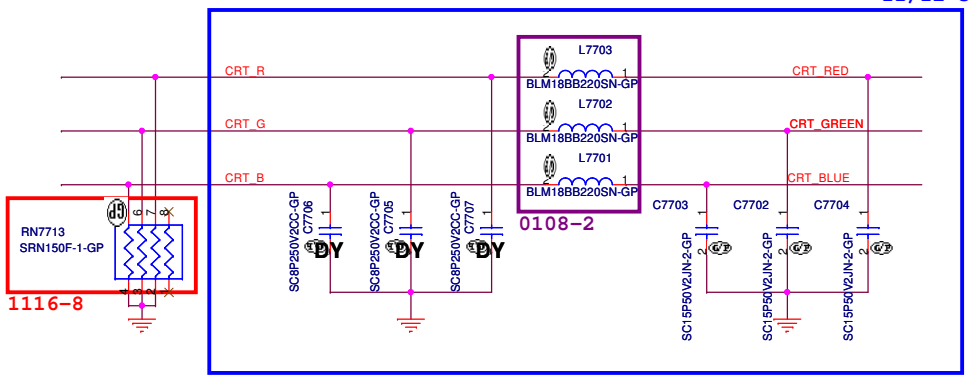
Title: *IO Board Connector*

Size	Document Number	Rev
A4	*Berry AMD Discrete/UMA*	*A00*

Date: Thursday, March 04, 2010 Sheet 76 of 95

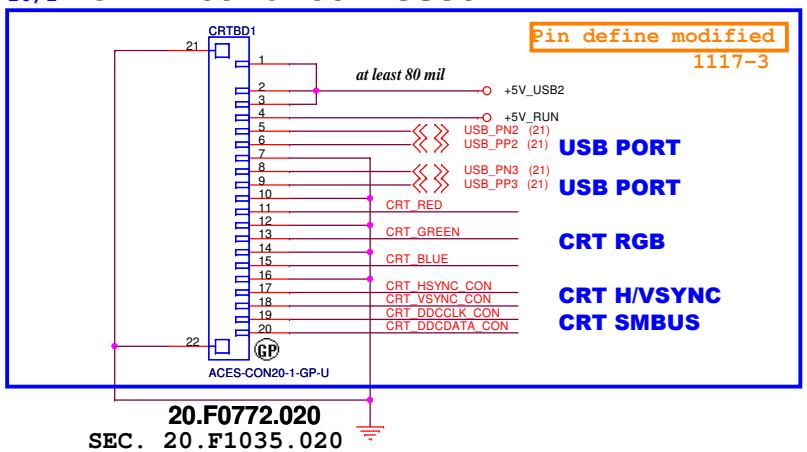
SSID = Int.Conn

11/12-5



10/1

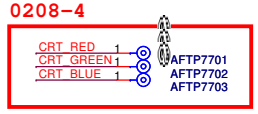
CRT Board Connector



20.F0772.020

SEC. 20.F1035.020

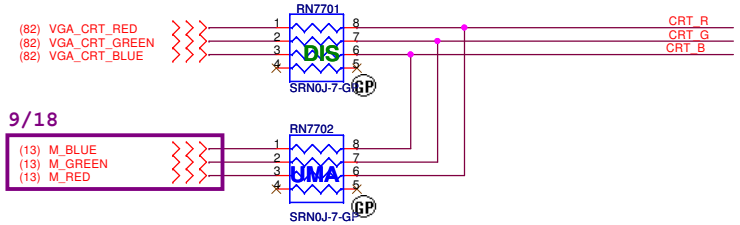
0208-4



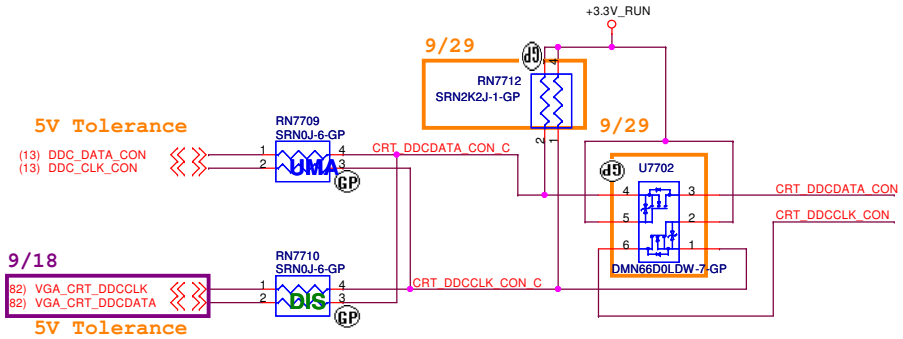
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board



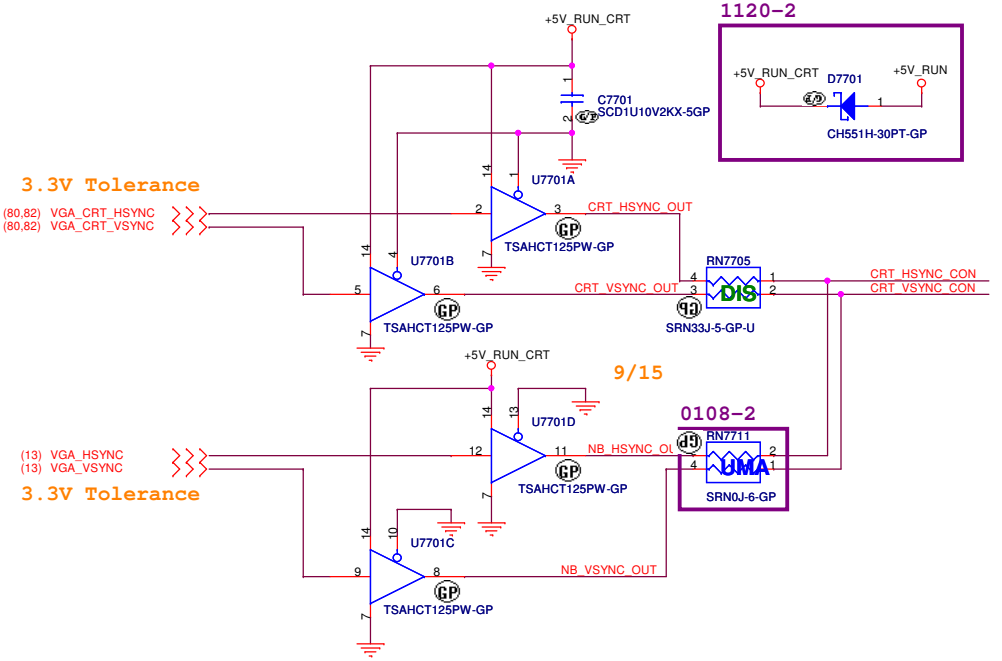
CRT DDCDATA & DDCCLK



Pull High 5V Design on CRT Board

CRT Hsync & Vsync level shift

Close to CRT Board CONN



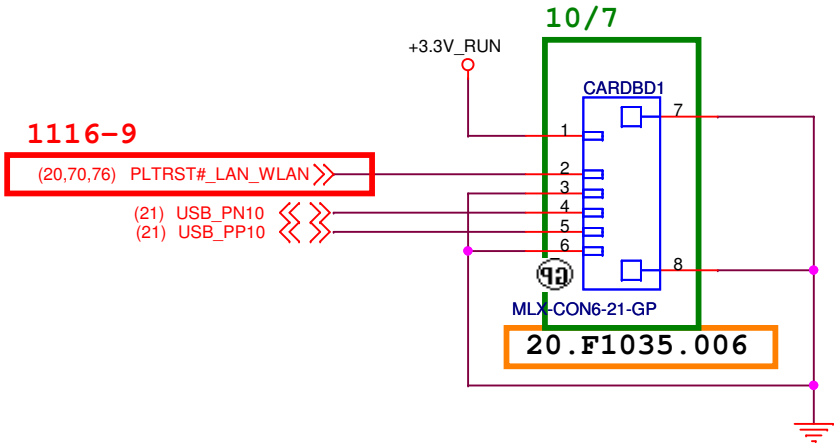
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Board Connector	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 77 of 95	

SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 78 of 95

H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H6 HTE95BE95R29-R-5-GP
H7 HTE95BE95R29-R-5-GP
H8 HTE95BE95R29-R-5-GP
H9 HTE95BE95R29-R-5-GP
H5 HOLE256R111-GP
H11 HOLE256R111-GP
H10 HOLE335R115-GP DY

CPU Thermal module hole
HTML1 HOLE197R166-GP DY
HTML2 HOLE197R166-GP DY
HTML3 HOLE197R166-GP DY

GPU Thermal module hole
HGPU1 STF237R117H83-1-GP

0210-2
stand off
HBT1 STF237R117H123-GP

EMI Reserve
+PWR_SRC
EC7901 SCD1U25V2KX-GP
EC7902 SCD1U25V2KX-GP
EC7904 DY SCD1U25V2KX-GP
EC7903 SCD1U25V2KX-GP
EC7905 DY SCD1U25V2KX-GP
EC7906 SCD1U25V2KX-GP
+VGA_CORE
1118-2
EC7907 SCD1U10V2KX-5GP
10/6
+3.3V_RUN
EC7910 DY SCD1U25V2KX-GP
+5V_ALW
EC7911 DY SCD1U25V2KX-GP
EC7912 DY SCD1U25V2KX-GP
10/5
SPR1 SPRING-58-GP DY

EMI Reserve 1117-4
+PWR_SRC
EC7924 DY SC10P50V2JN-4GP
+3.3V_RUN
EC7916 DY SC10P50V2JN-4GP
EC7920 DY SC10P50V2JN-4GP
EC7923 DY SC10P50V2JN-4GP
EC7917 DY SC10P50V2JN-4GP
+3.3V_RUN +5V_RUN
EC7922 DY SC10P50V2JN-4GP
EC7915 DY SC10P50V2JN-4GP
+5V_RUN +VCC_CORE
EC7919 DY SC10P50V2JN-4GP
EC7921 DY SC10P50V2JN-4GP
+5V_RUN +PWR_SRC
EC7914 DY SC10P50V2JN-4GP
EC7913 DY SC10P50V2JN-4GP
+5V_RUN +1.5V_RUN
EC7918 DY SC10P50V2JN-4GP

1118-2 RF Team Solution
+3.3V_ALW
C7909 SC56P50V2JN-2GP
C7906 SC56P50V2JN-2GP
+1.5V_RUN
C7905 SC56P50V2JN-2GP
C7904 SC56P50V2JN-2GP
+5V_RUN
C7902 SC56P50V2JN-2GP
C7917 SC56P50V2JN-2GP
+15V_ALW
C7907 SCD1U25V2KX-GP
C7915 SCD1U25V2KX-GP
C7911 SCD1U25V2KX-GP
+1.1V_RUN
C7910 SC56P50V2JN-2GP
C7908 SC56P50V2JN-2GP
+1.8V_RUN
C7919 SC56P50V2JN-2GP
+3.3V_RUN
C7920 SC56P50V2JN-2GP

0106-3 RF Team Solution
+PWR_SRC
C7922 SC56P50V2JN-2GP
+1.5V_SUS
C7921 SC56P50V2JN-2GP

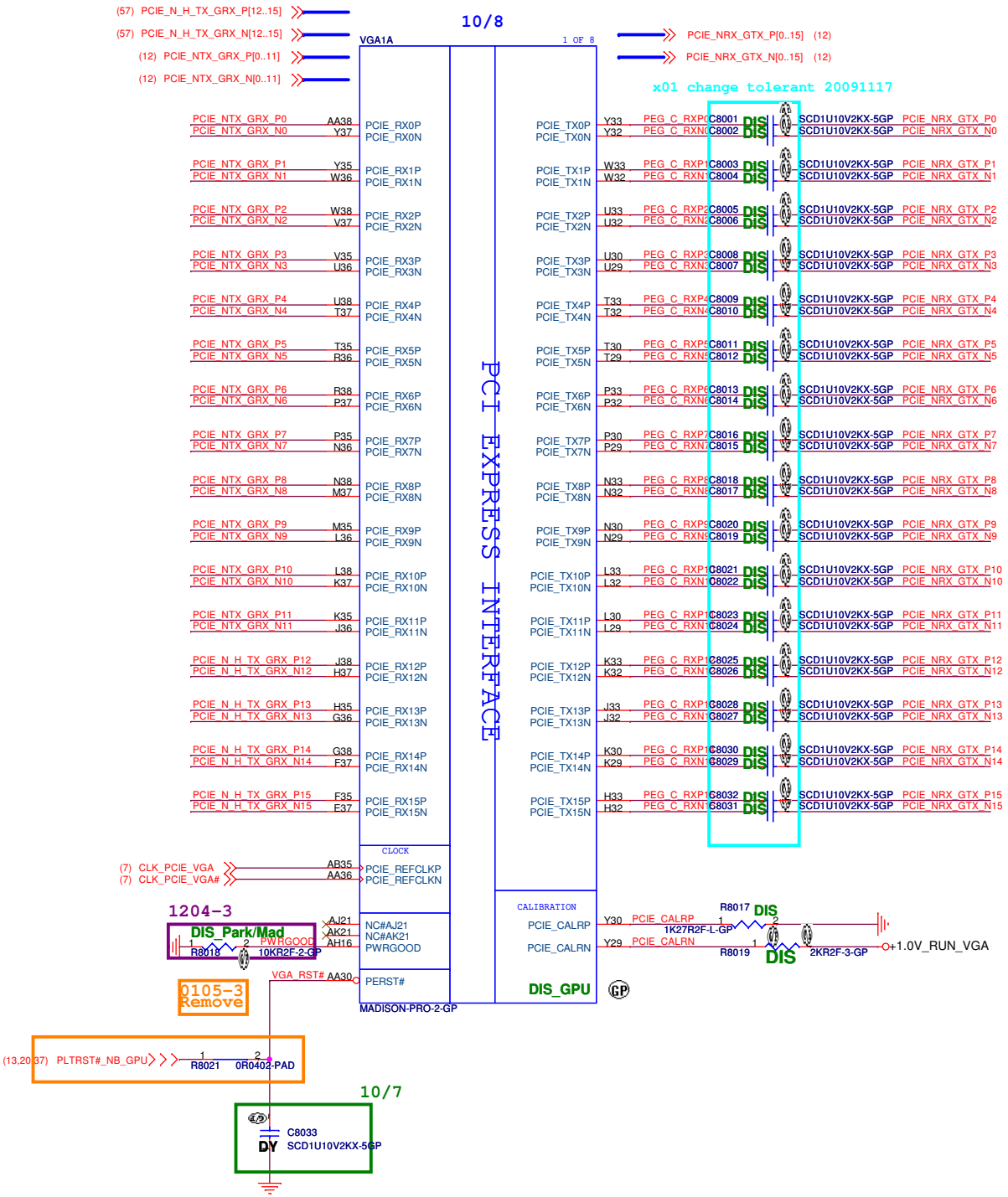
0108-1 EMC reserved
+PWR_SRC
EC7927 SC56P50V2JN-2GP
+1.5V_SUS
EC7926 SC56P50V2JN-2GP
EC7925 SC56P50V2JN-2GP

0224-1
+PWR_SRC
EC7930 SC56P50V2JN-2GP
EC7931 SC56P50V2JN-2GP
0225-5
+DC_IN_SS
EC7929 SC56P50V2JN-2GP
+SDC_IN
EC7932 SC56P50V2JN-2GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Berry
Rev: A00
Date: Thursday, March 04, 2010
Sheet 79 of 95



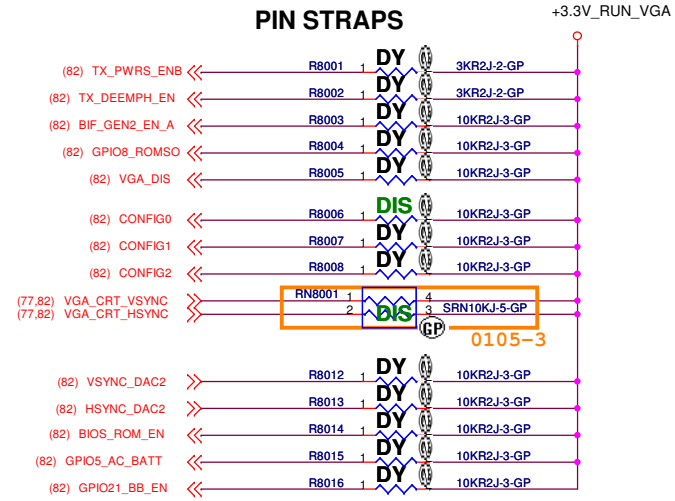
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



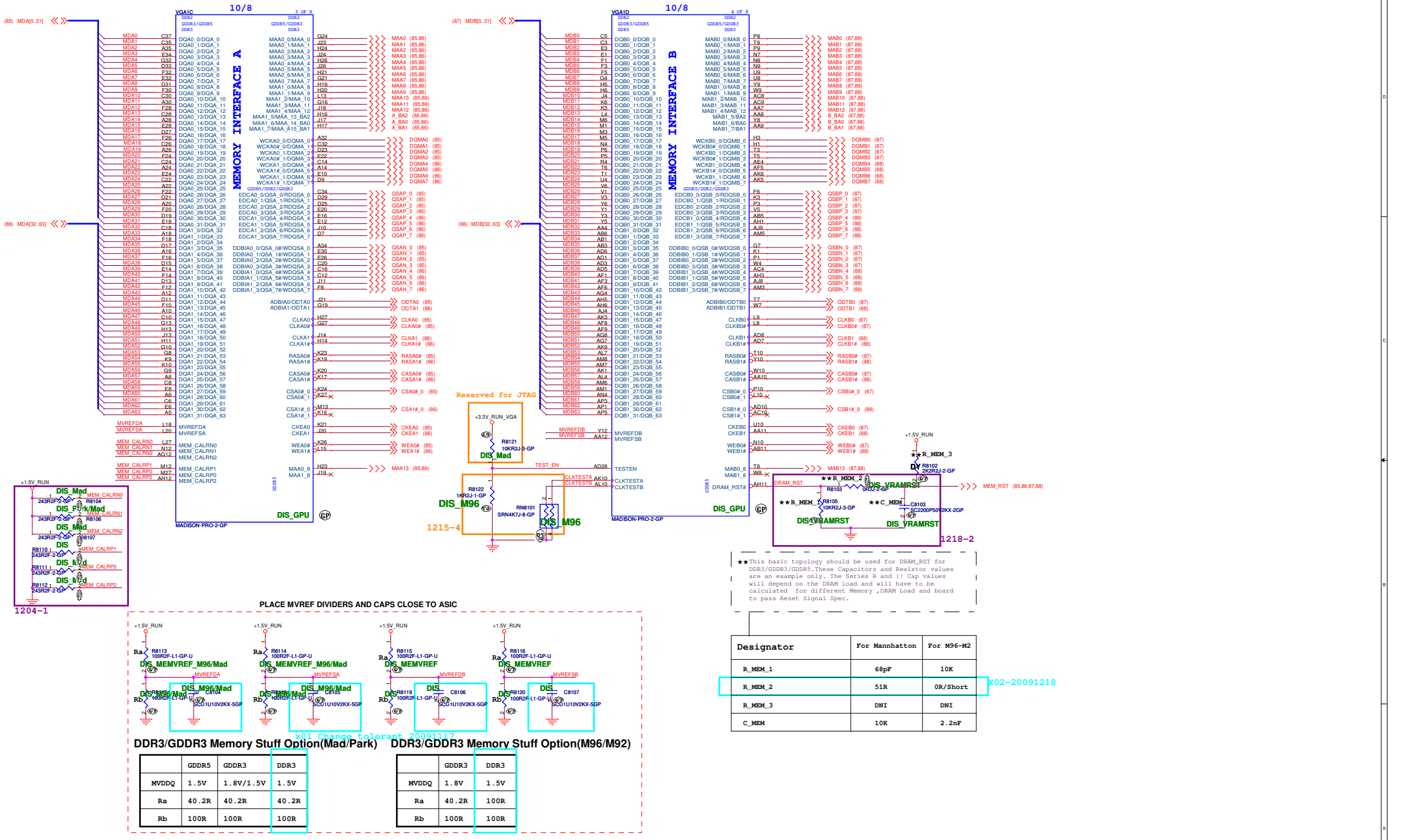
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A3	Berry	A00

Date: Thursday, March 04, 2010 Sheet 80 of 95



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

DDR3/GDDR3 Memory Stuff Option(M96/M92)

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

Designator

Designator	For Mannhatton	For M96-M2
R_MEM_1	68pF	10K
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	10K	2.2nF

X02-20091218

**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size	Document Number	Rev
A2	Berry	A00

Date: Thursday, March 04, 2010 Sheet 81 of 95

MEMORY ID Table

DVPDATA[0:3]	Description
1000	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
0000	DDR3 Samsung-K4W1G1646E-HC12 (800MHz)

DVPDATA[0:3] Default:Pull down

Madison Only JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode
TESTEN	"1"(PU)	"1"(PU)
JTAG_TRST#	"0"(PD)	"1"(PU)
JTAG_TCK	CLK	"1"(PU)
JTAG_TMS	"1"(PU)	"1"(PU)

LVDS Interface

MEM_ID Control

VRAMDIS_Hynix

DDC channel for LVDS

Straps

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

DDC channel for CRT

DDC channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

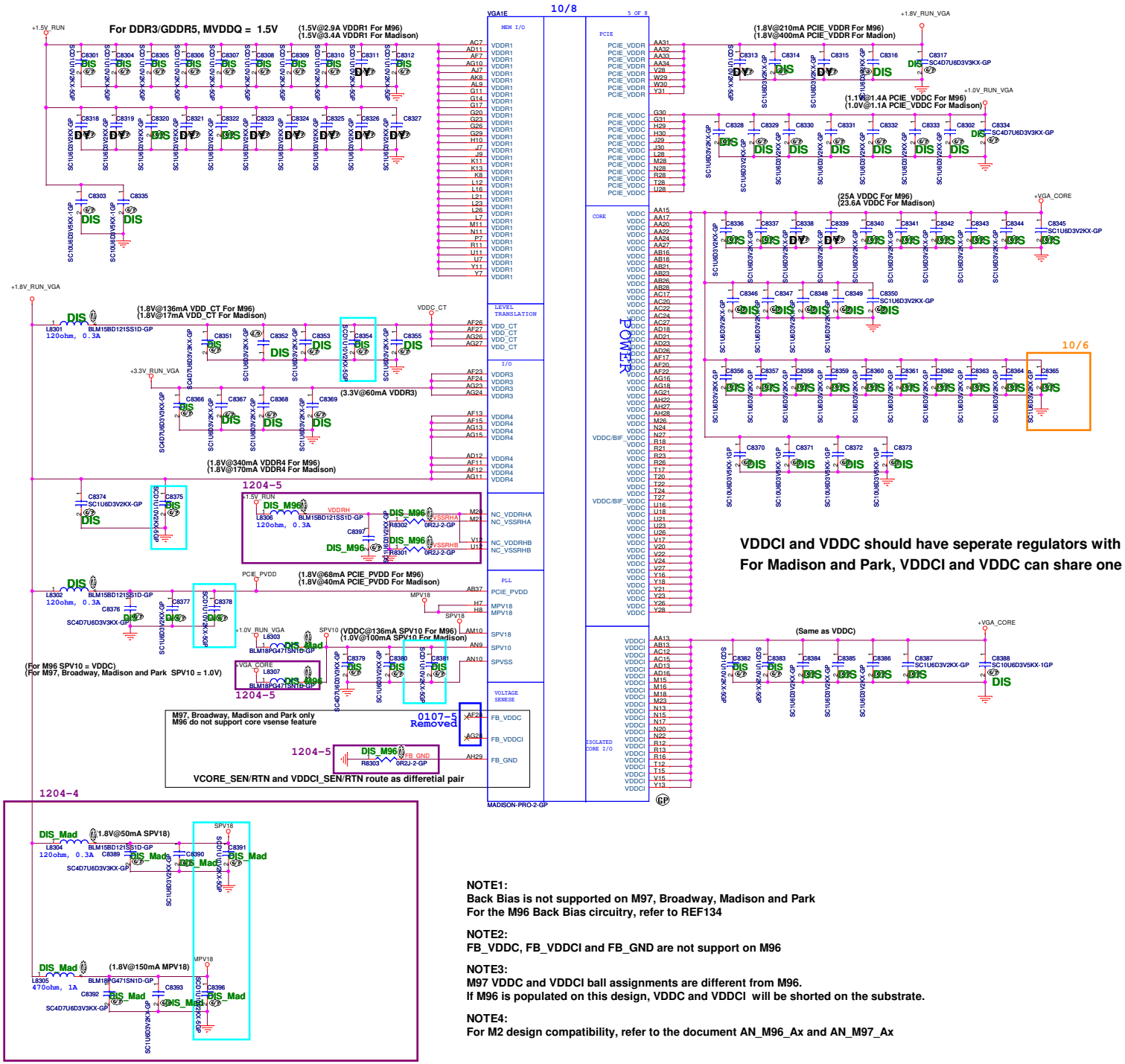
<Core Design>

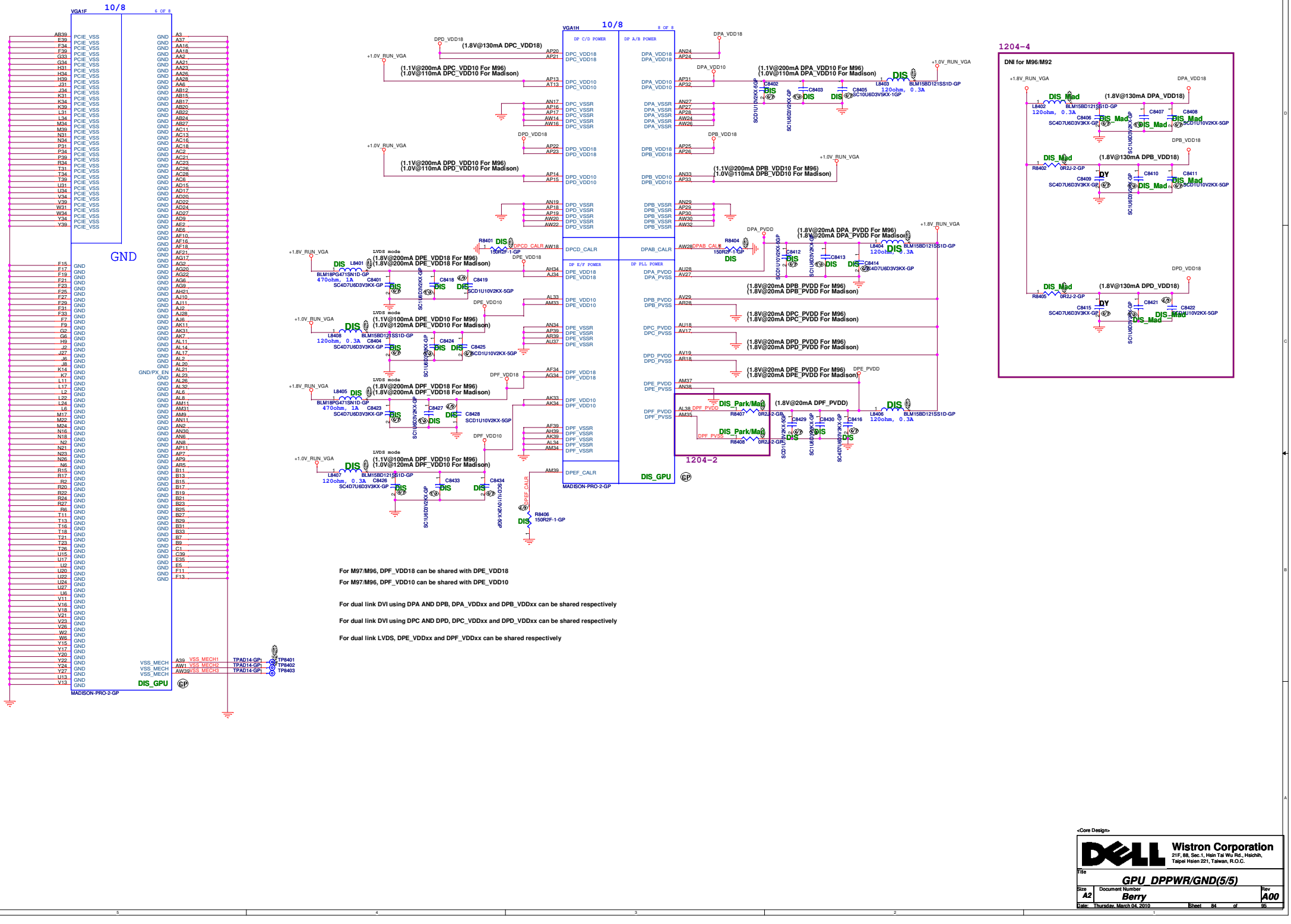
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 82 of 95


For DDR3/GDDR5, MVDDQ = 1.5V
(1.5V@2.9A VDDR1 For M96)
(1.5V@3.4A VDDR1 For Madison)
(1.8V@210mA PCIE_VDDR For M96)
(1.8V@400mA PCIE_VDDR For Madion)
(1.1V@1.4A PCIE_VDDC For M96)
(1.0V@1.1A PCIE_VDDC For Madison)
(25A VDDC For M96)
(23.6A VDDC For Madison)
(1.8V@136mA VDD_CT For M96)
(1.8V@17mA VDD_CT For Madison)
(3.3V@60mA VDDR3)
(1.8V@340mA VDDR4 For M96)
(1.8V@170mA VDDR4 For Madison)
(1.8V@68mA PCIE_PVDD For M96)
(1.8V@40mA PCIE_PVDD For Madison)
(1.8V@50mA SPV18)
(1.8V@150mA MPV18)
(VDDCI@136mA SPV10 For M96)
(1.0V@100mA SPV10 For Madison)
(Same as VDDC)
(For M96 SPV10 = VDDC)
(For M97, Broadway, Madison and Park SPV10 = 1.0V)
M97, Broadway, Madison and Park only
M96 do not support core vsense feature
0107-5
Removed
VCORE_SEN/RTN and VDDCI_SEN/RTN route as differetial pair
1204-5
1204-4
10/8
10/6
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU_POWER(4/5)
Berry
A00
Thursday, March 04, 2010
83
85



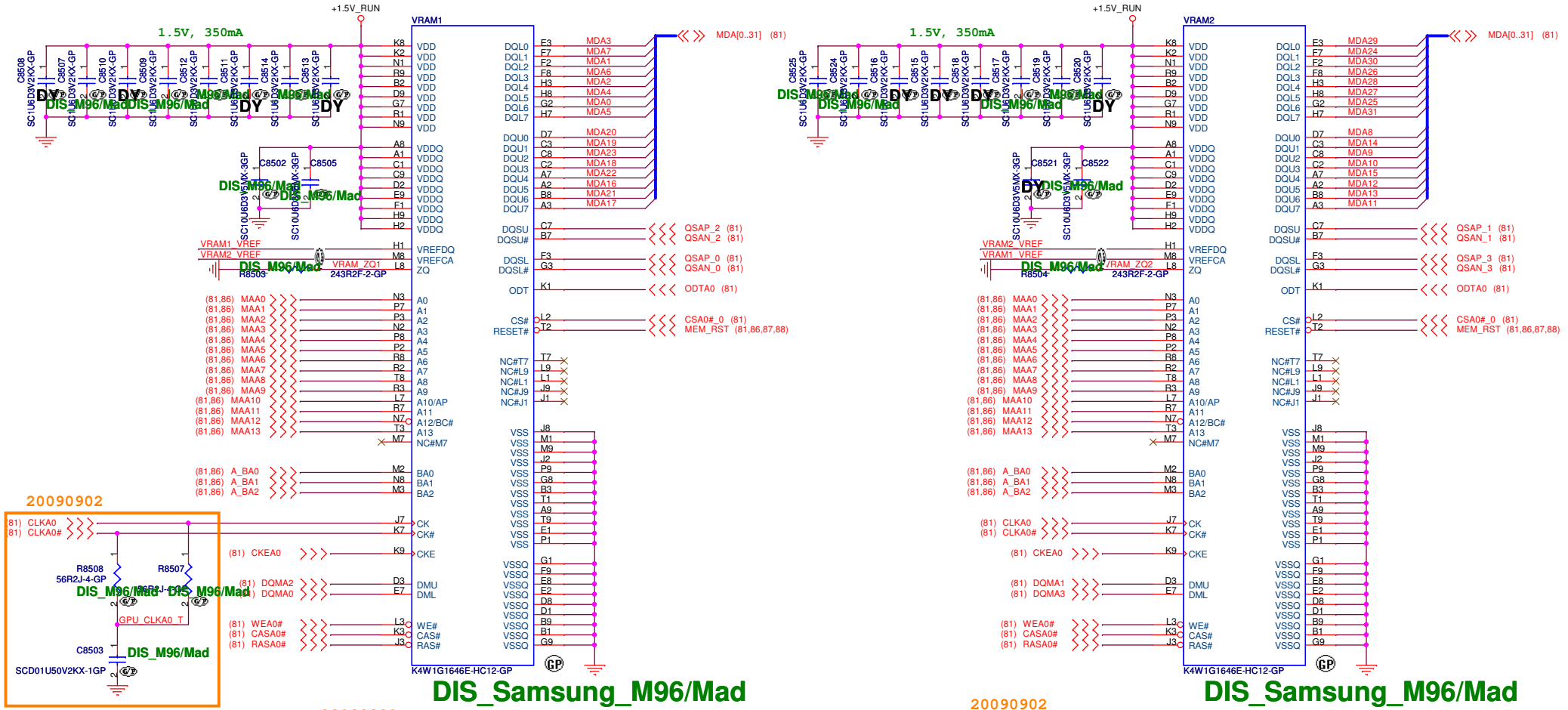
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A2	Berry	A00

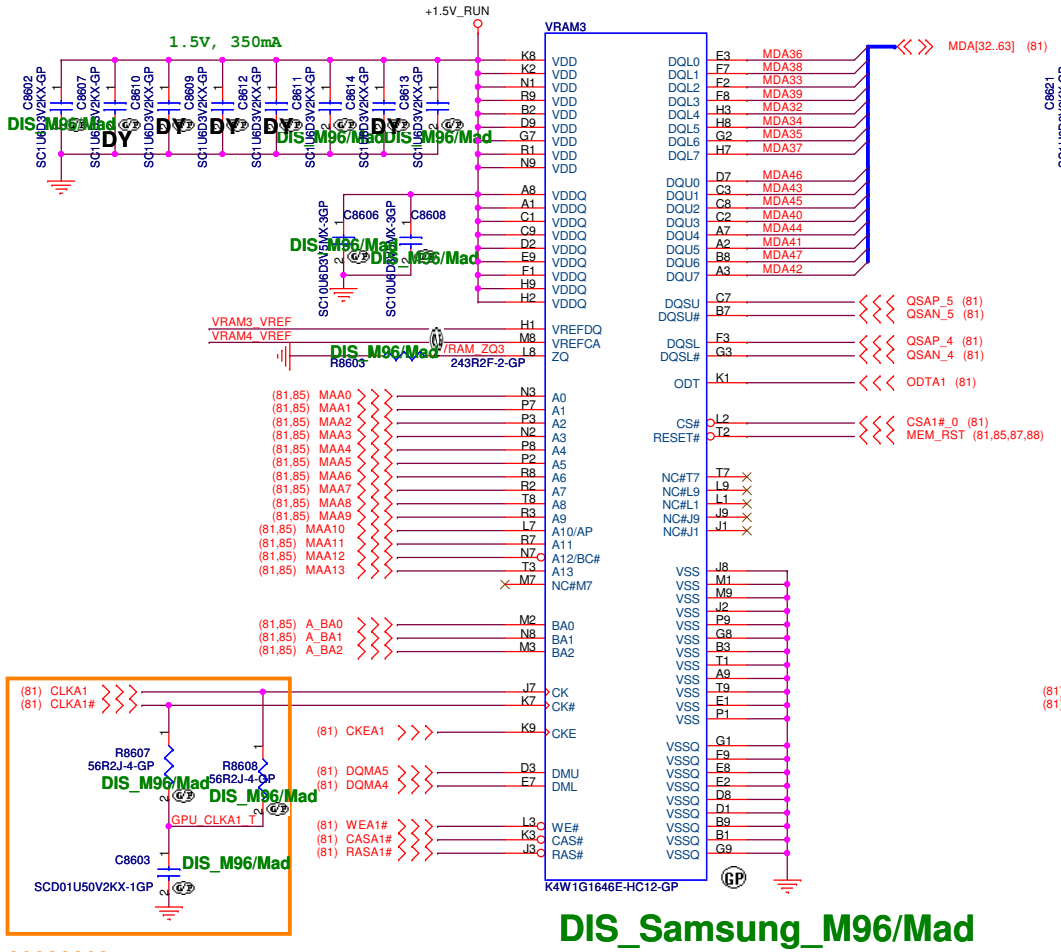
Date: Thursday, March 04, 2010 Sheet 84 of 85



Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A3	Berry	A00

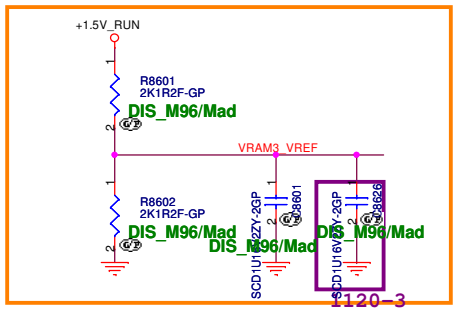
Date: Thursday, March 04, 2010 Sheet 85 of 95

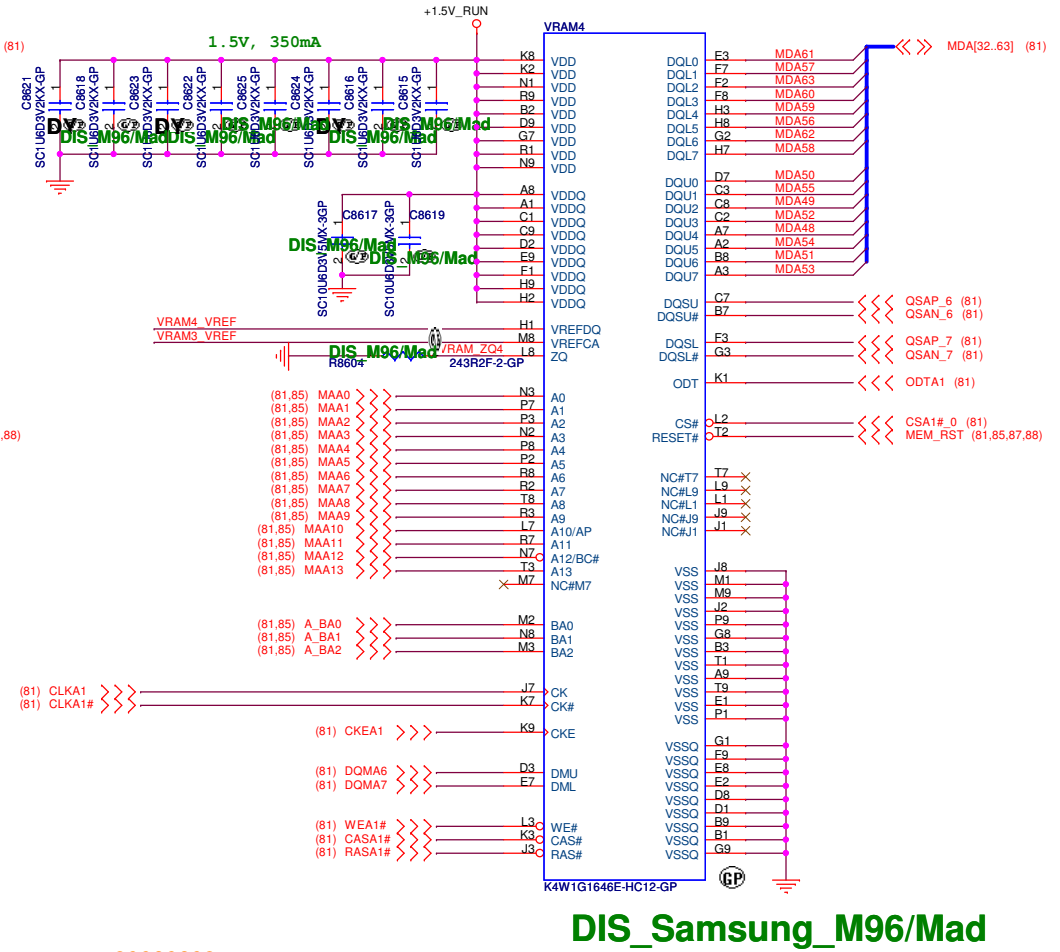


DIS_Samsung_M96/Mad

20090902

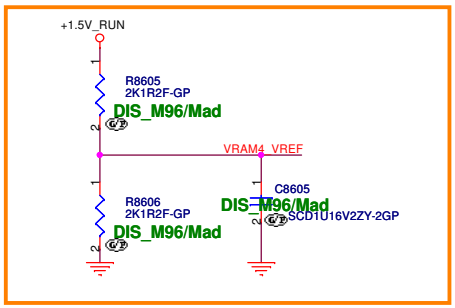
20090902





DIS_Samsung_M96/Mad

20090902



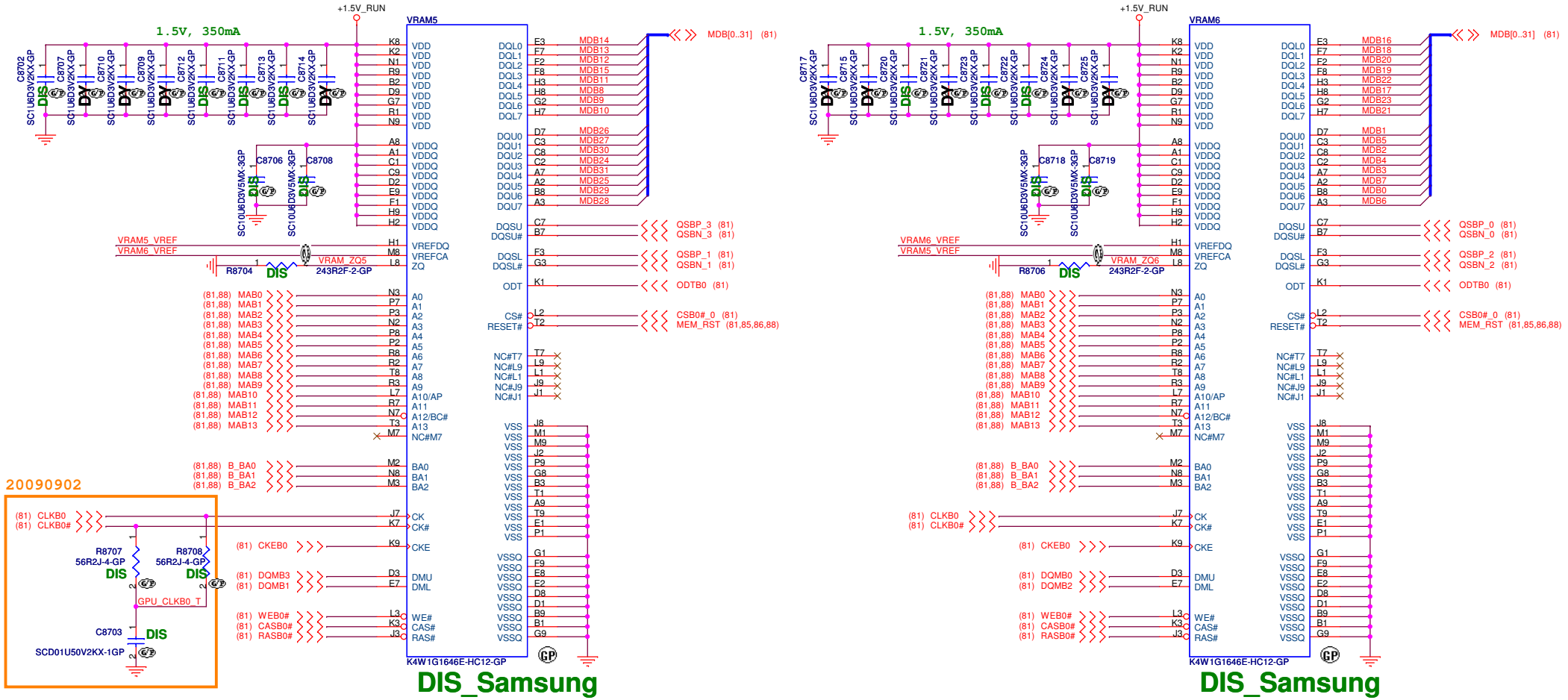
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 86 of 95



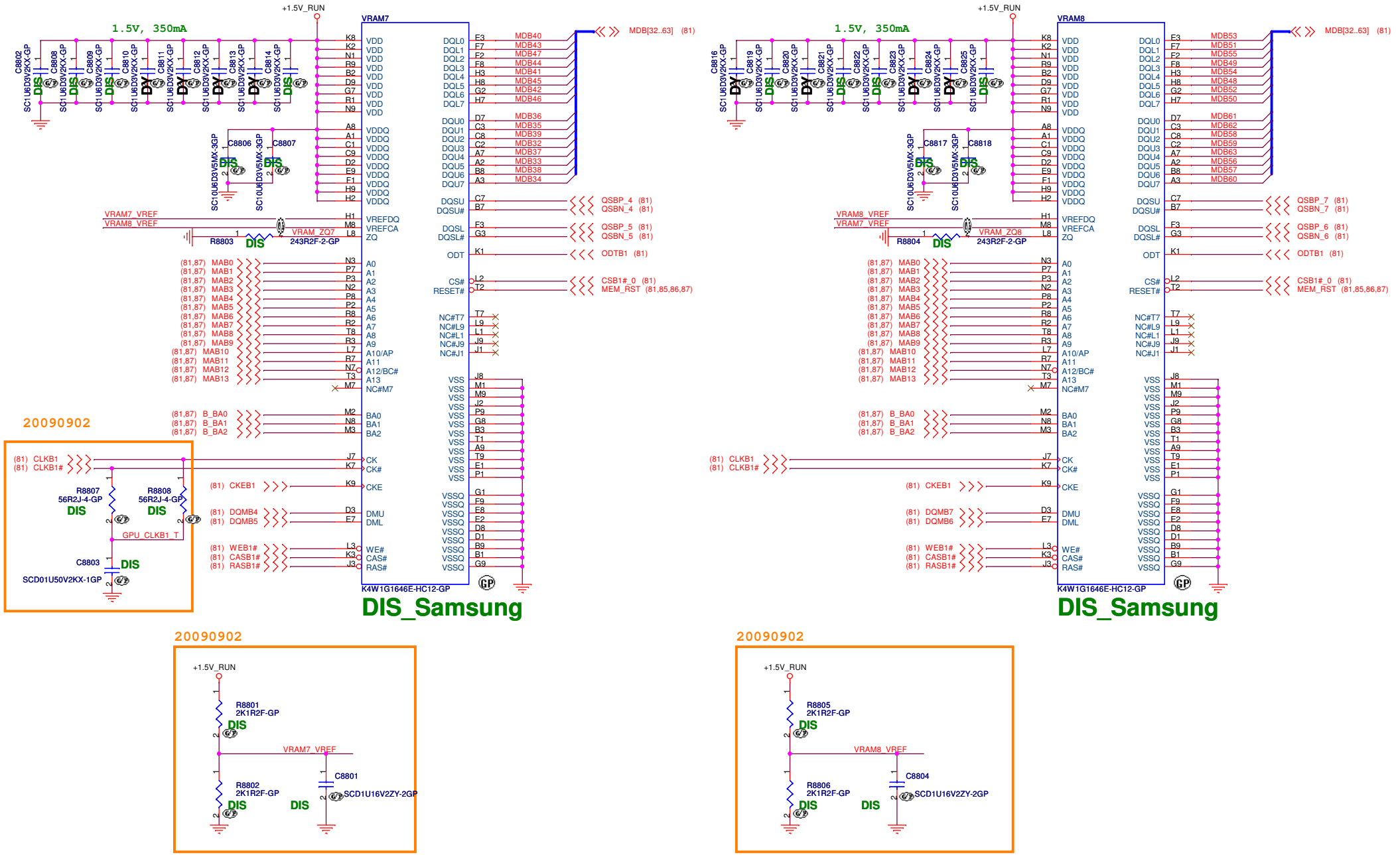
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 87 of 95



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

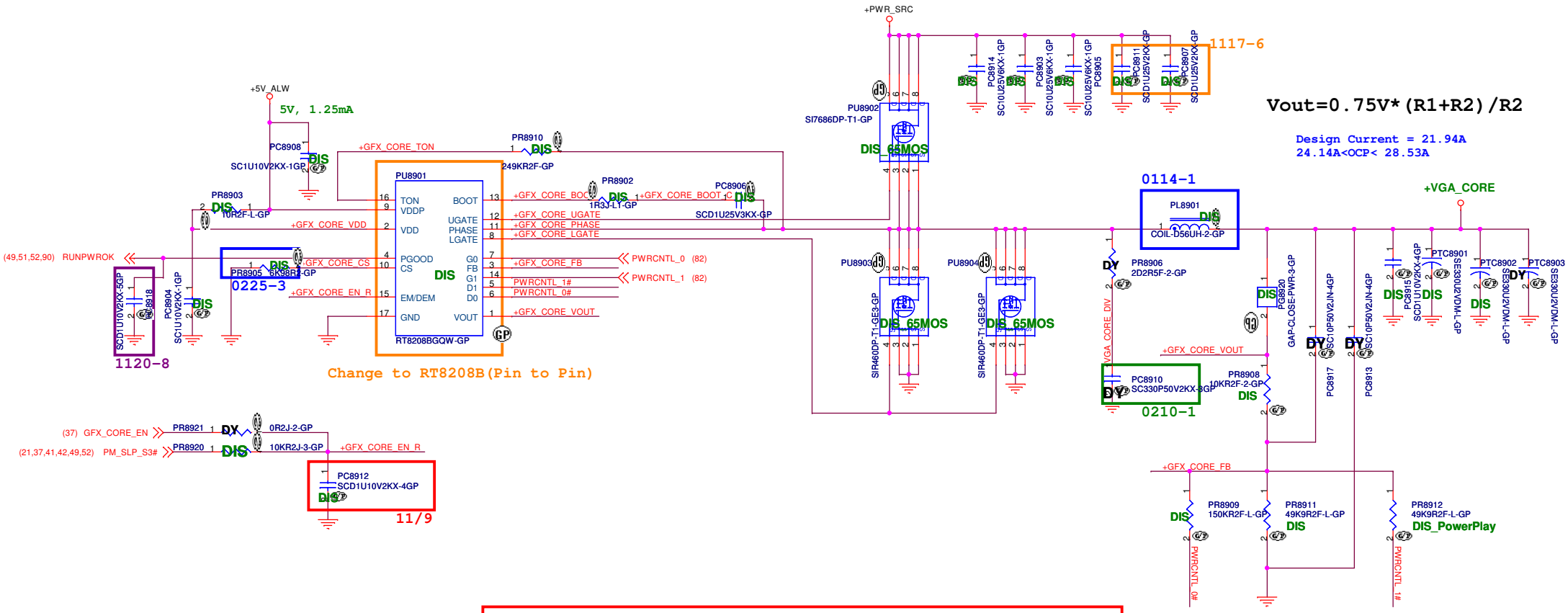
Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 88 of 95

SSID = Video.PWR.Regulator

RT8208AGQW for +VCC_GFX_CORE



M96 Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

PR8912=49.9KR
64.49925.6DL

Park Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

PR8912=49.9KR
64.44225.6DL

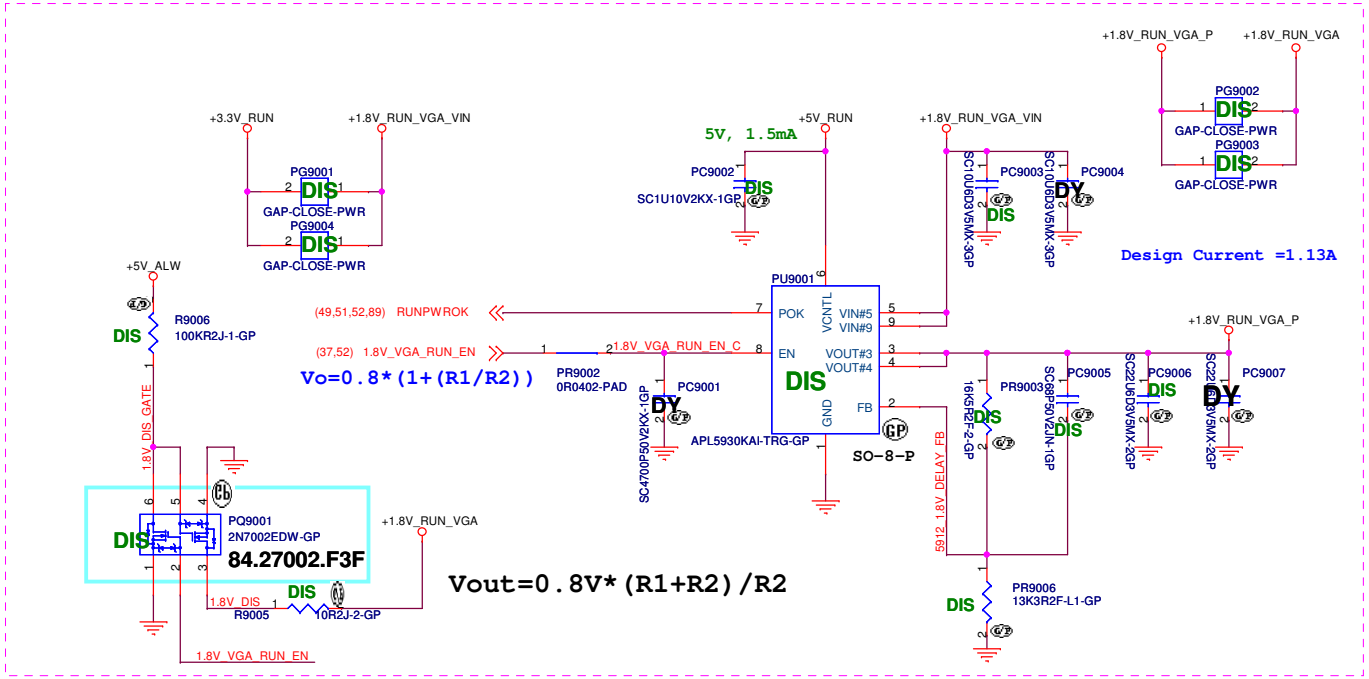
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

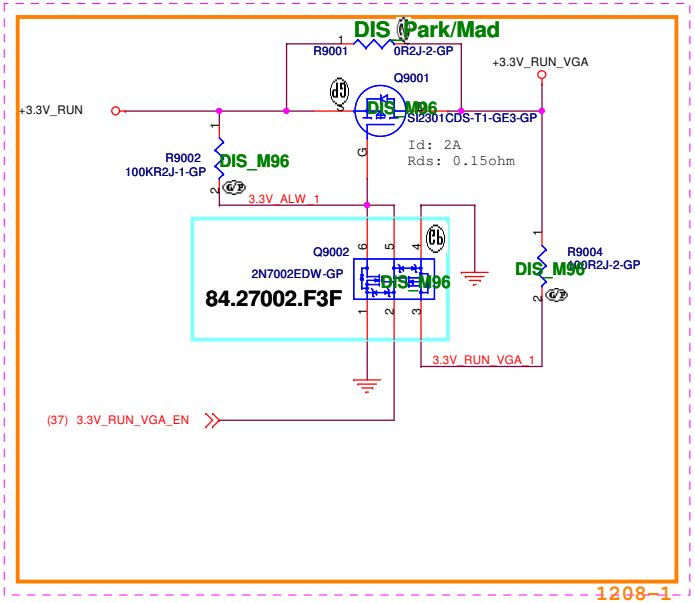
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VCC_GFXCORE
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00
Date: Thursday, March 04, 2010 | Sheet 89 of 95

APL5930 for +1.8V_RUN_VGA

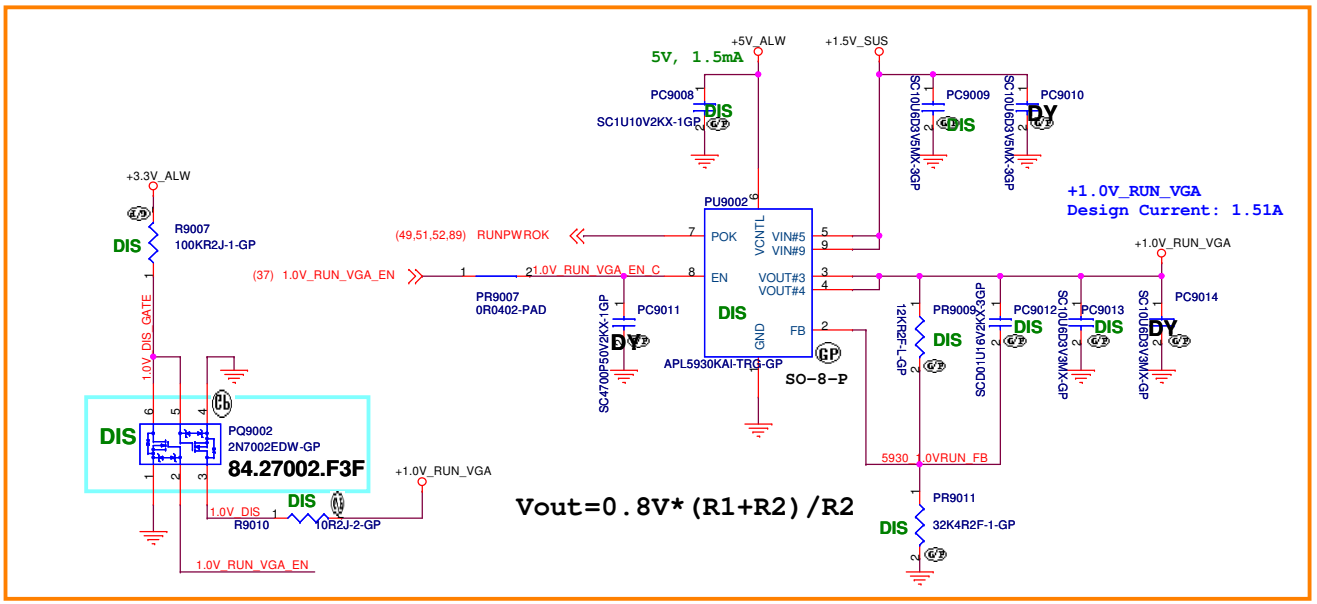


+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA

Will be Change to +1.0V_RUN_VGA

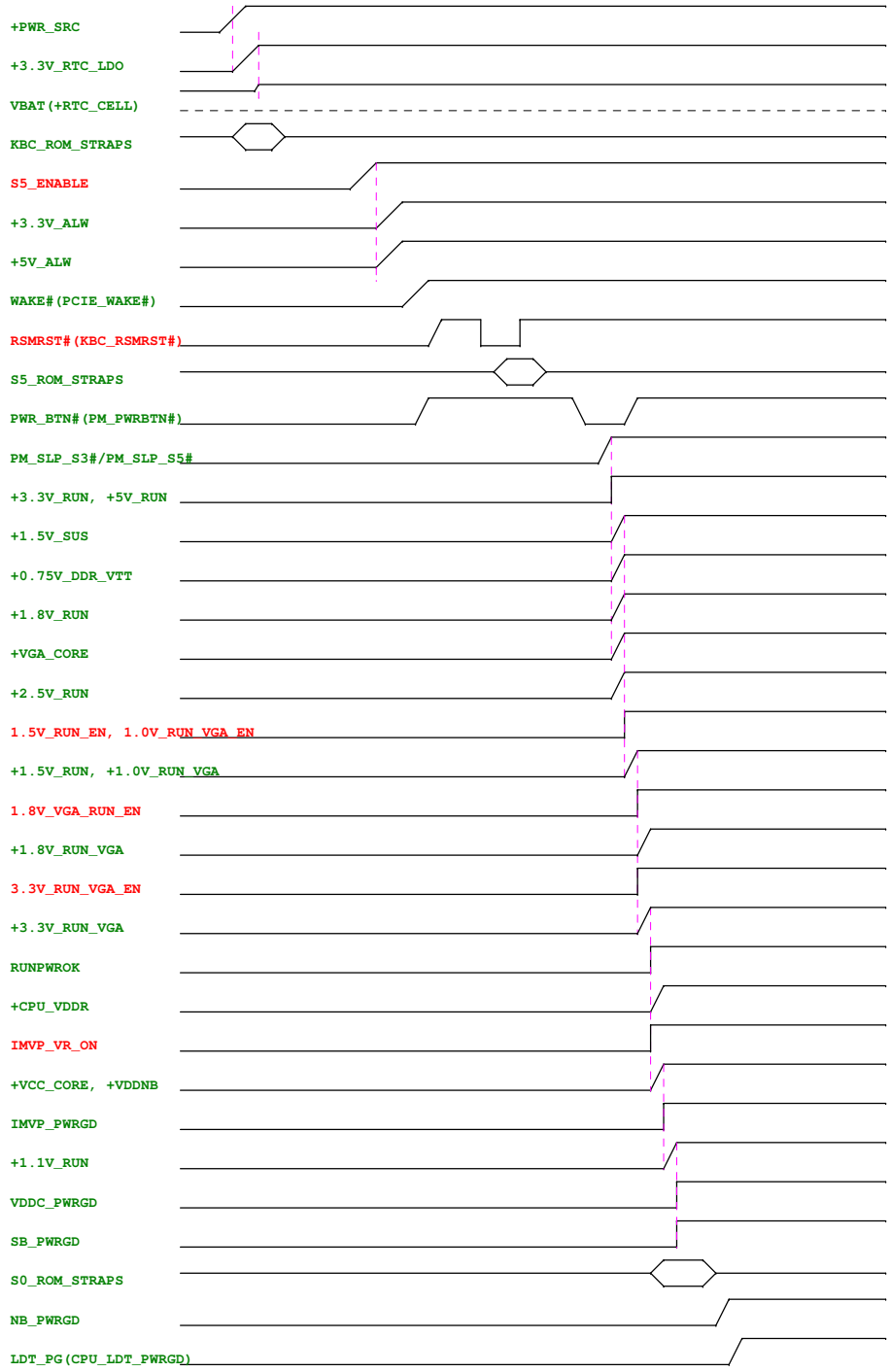


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DISCRETE VGA POWER	
Size: A3	Document Number: Berry	Rev: A00
Date: Tuesday, March 09, 2010	Sheet 90 of 95	

POWER SEQUENCE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER SEQUENCE		
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 91 of 95	

Change notes – Page 1

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/6	1	10	Add C1002 10uF, C1007, EC1001 0.1uF, C1008 10pF.	Insure signal quality.	EE
		2	13	Change R1314 to 4.7K.	Meet CRB.	EE
		3	51	Swap PU5101 pin3, pin4.	Correct input voltage level.	EE
		4	82	Add R8210 0R.	Reserve GPU clock input source.	EE
	11/9	1	30	Change C3014 to 2.2uF.	Reduce package size.	EE
		2	69	Change C6903 to 0.1uF.	Reduce package size.	EE
		3	49	Add PR4916 100KR.	To prevent leakage in S3 status.	EE
	11/10	1	18,19	Change DIMM socket Part Number.	Request by ME.	ME
		2	37	Add R3754 100KR.	To detect leakage current.	EE
	11/11	1	10	Modify R1028 pull-up to +1.5V_RUN.	Solve leakage in S3 status.	EE
	11/12	1	20	Change C2011 to 18pF, C2012 to 15pF.	Set accurate clock frequency.	EE
		2	37	Add C3717 10pF.	Stable singal level.	EE
		3	57	Delete RN5711, RN5705.	Redundant parts.	EE
		4	13	Delete R1331, R1332, R1308.	Redundant parts.	EE
		5	77	Add Pi-filter.	Cure EMI.	EMC
	11/13	1	20	Change X2001 P/N.	Request by Sourcer.	Sourcer
		2	7	Change R713 to 47R.	Fine tune damping.	EE
		3	82	Add R8211 80.6R, R8220 150R.	Set a voltage divider to 1.8V level swing.	EE
		4	21	Add R2133 1KR.	For UMA VRAM vendor selection.	EE
	11/16	1	22	Delete RN2203 pin 4, pin 5 connection.	Solve S5 leakage.	EE
		2	51	Change PR5105 pull-up to +3.3V_RUN.	Prevent leakage.	EE
		3	21	Add C2103, C2104 0.1uF.	For signal stability.	EE
		4	37	Add C3718 0.1uF.	For signal stability.	EE
		5	41	Add C4101, C4102 0.1uF.	For signal stability.	EE
		6	49	Add PC4923 0.1uF.	For signal stability.	EE
		7	66	Add C6601, C6602 0.1uF.	For signal stability.	EE
		8	77	Add RN7713 150R.	Move impedance matching resistor from CRT/B to M/B.	EMC
		9	78	Change CARDBD1 pin 2 link to PLTRST#_LAN_WAN.	Change card reader chip to RTS5159 to solve EMI.	EMC
	11/17	1	30	Add R3014, R3017, R3020 0R to link AGND and GND.	Issue for pop noise when system boot.	EE
		2	42,48,50	Merge 1.1V power solution on main board.	Save components.	EE, Power
		3	77	Modify CRTBD1 pin define.	Relief EMI.	EMC
		4	79	Add some decoupled capacitors.	Request by EMC.	EMC
		5	37	Change R3737 to 33R, stuff C3715 10pF.	Request by EMC.	EMC
		6	62,89	Sutff EC6203 22pF, PC8911, PC8907 0.1uF.	Request by EMC.	EMC
		7	45,46,47	Stuff EC4502 0.1uF, PC4605, PC4609, PC4738 0.1uF.	Request by EMC.	EMC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change notes

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 92 of 95

Change notes – Page 2

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/17	8	9	Delete R904.	Remove redundant layout trace.	EE
	11/18	1	81	Swap R8105, C8103 location.	Meet CRB.	EE
		2	79	Add some decoupled capacitor.	By RF team request.	RF
		3	49	Change PR4903 to 620KR.	Change to common part.	Power
	11/19	1	All	Synchronize with DJ schematic.	Schematic standardlize.	EE
		2	48	Change P/N for PU4802, PU4803, PU4804, PU4805.	Rquest by Power team	Power
		3	All	Review all capacitors tolerance.	Total review for deratig.	EE
		4	21	Add RN2105 0R.	Reserve to fine tune signal quality.	EE
		5	21	Change RN2101 to 4.7KR.	Fine tuned value for signal.	EA
		6	37	Add RN3705, R3755 0R.	To isolate layout trace to DB1 connector.	EA
		7	49	Change PC4908 to 2.2uF.	Changed by EA report.	EA
	11/20	1	54	Modify R5408 connection.	To synchronize with DJ.	EE
		2	57	Add D7701.	To prevent leakage from RGB monitor.	EE
		3	86	Add C8626 0.1uF.	By EA report.	EA
		4	37	Add R3756 10KR, C3720 0.1uF.	Synchronize with DJ.	EE
		5	37	Delete RN3705, R3755.	For more layout space.	EE
		6	13	Delete TP1303, TP1304.	For more layout space.	EE
		7	49	Delete PR4905.	For more layout space.	EE
		8	89	Add PC8918 0.1uF.	Stable signal quality.	EE
	11/24	1	46,49	Change PU4601, PU4901 Power components.	Request by Power team.	Power
	11/25	1	46,47,49,89	Change power components.	Request by Power team.	Power
	11/29	1	10	Change C1008 to 10pF.	Fine tuned signal slew rate to meet specification.	EE
		2	30	Change R3007 to 2.2KR.	By FAE suggestion.	EE
X02	12/04	1	81	Set BOM mark R8104, R8106, R8107, R8110, R8111, R8112.	Implement co-layout Madison and M96.	EE
		2	82,84	Add R8407, R8408 0R.	Implement co-layout Madison and M96.	EE
		3	80	Add R8016 10KR.	Implement co-layout Madison and M96.	EE
		4	83,84	Set BOM mark.	Implement co-layout Madison and M96.	EE
		5	83	Add L8306, L8307, C8397, R8301, R8302, R8303.	Implement co-layout Madison and M96.	EE
	12/05	1	37	Change R3756, C3720 connection.	Correct soft-start for EC power.	EE
	12/08	1	90	Set BOM mark.	Implement co-layout Madison and M96.	EE
	12/15	1	15	Delete RN1501, Add G1501~G1504.	Synchronize with DJ and supply sufficient power rail.	EE
		2	62	Add R6207 100KR.	Insure SPI Write-Protect pin signal level.	EE
		3	66	Change C6602 net name.	Correct signal name.	EE
		4	81	Add R8122 1KR, RN8101 4.7KR.	Meet M96 schematic check list.	EE
		5	82	Swap CLK_VGA_27M_NSS and CLK_VGA_27M_SS connection.	Solve external RGB display tremble issue.	EE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change notes

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 93 of 95

Change notes – Page 3

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	12/16	1	66	Change R6605 to 0R.	Assure power button level set to low.	EE
		2	37,76	Add net "8103_GPO".	Implement LAN DSM hardware function.	EE
	12/17	1	37	Add U3703.	To solve SPI WP signal malfunction on EC.	EE
	12/18	1	82	Add R8222 1MR.	Assure crystal resonant clock stable.	EE
		2	81	Set VRAM reset circuit.	Follow M96 reset circuit and reseve BOM option.	EE
	12/25	1	18	Change TC1801 to 330uF, 2V tolerance.	Implement common part for 1.5V power rail.	EE
		2	46	Change PR4603 to 127KR.	Set 5V current limitation.	Power
		3	46	Empty PR4618 and stuff PR4619.	Set Ultra-sonic mode to keep +15V_ALW voltage level.	Power
		4	10	Set RN1006 PU to +1.5V_SUS.	Follow AMD check list and cure +1.5V_RUN leakage.	EE
		5	62	Change R6206 to 1KR.	According to Safety request, verified OK.	Safety
		6	51	Change PR5102 1KR, PR5106 8.2KR, PR5107 5.62KR.	Set VDDR low voltage level to 0.9V.	EE
	12/29	1	10,37	Add Q1005, R1039, R1040.	Request by AMD to set CPU into HTC mode in DOS.	EE
		2	47	Change PR4720 93.1KR, PR4721 24KR.	Set power OCP value.	Power
	12/31	1	ALL	Change some resistors as short-pad or resistor array.	Save component counts.	EE
		2	ALL	Change some capacitors with smaller value or empty.	Save component counts.	EE
	01/04	1	15	Change R1507,R1508,R1509,R1510,R1511 to bead.	Filter power noise.	EMC
	01/05	1	7	Combine R707,R721 as RN711.	For more layout space.	EE
		2	81	Delete TP8101,TP8102.	Remove useless test point for more layout space.	EE
		3	7,80	Delete R716,R8020, combine R8009,R8010 as RN8001.	Redundant part.	EE
		4	37,39,41	R3747,R4104 short pad, delete R3722,R3904.	Redundant part.	EE
		5	46	Change PR4620 as short pad.	Redundant part.	EE
		6	51	Change PQ5101 with ESD protector.	Change to common part.	Power
		7	54	Empty R5405 and Stuff R5408.	Avoid LCD white panel.	EE
		8	62	Change R6205 to 0R.	Already have one 1KR ahead.	EE
	01/06	1	50	Add PR5004 10KR and empty PR5002.	Avoid +1.1V_ALW leakage in South Bridge.	EE
		2	13	Change R1342 to size 0603.	Synchronous schematic w/DJ.	EE
		3	79	Add R7921 and R7922.	Reserved RF team solution.	RF
	01/07	1	7	Add RN712,C722,C723	Reserve for SMBus signal quality tuning.	EE
		2	60	Change EC6007,EC6008 to 0.01uF.	According FAE Request.	IDT FAE
		3	39	Add Q3904.	According thermal team request.	Thermal
		4	21,18	Change location RN2105 to RN1801, add C1823,C1824.	For SMBus signal quality fine tune.	EE
		5	39,82,83	Remove C3912,TP8301,TP8302,TP8213.	Remove dummy part for more layout space.	EE
		6	76	Reserve C7601, C7602.	Fine tune USB signal quality.	EE
	01/08	1	79	Reserve EC7925,EC7926,EC7927.	Reserve by EMC team.	EMC
		2	77	Change RN7711 to 0R, L7701,L7702,L7703 to bead 22R.	According EMC measurement result.	EMC

0108

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change notes

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 94 of 95

Change notes - Page 4

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory requst.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory requset to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE
	03/08	1	48	Stuff PU4803 and empty PU4804.	Place the H/S and L/S MOS at the same surface.	Power

0308-1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Change notes	
Size A3	Document Number Berry	Rev A00
Date: Monday, March 08, 2010	Sheet 95 of 95	