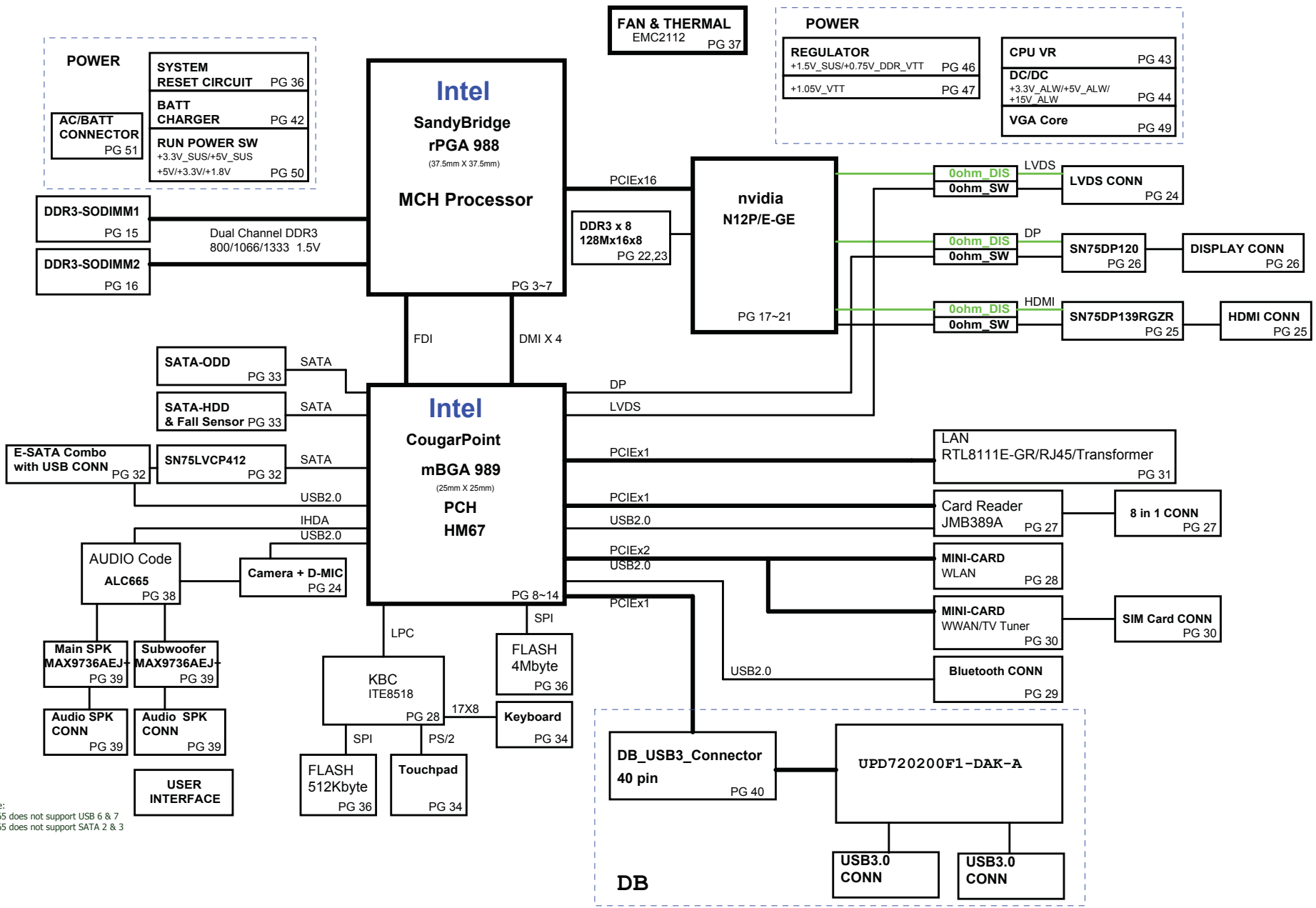


GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:

_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only




Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3


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2	Front Page
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24	LCD CONN
25	HDMI CONN
26	MINI DP CONN
27	Card Reader (JMB389)
28	SIO (ITE8502)
29	MINI-Card (WLAN/WPAN)
30	MINI-Card (WWAN)
31	LAN(RTL8111EL/RJ-45)
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33	SATA (HDD & ODD)
34	TP / KEYBOARD
35	SWITCH / LED / T-Screen
36	FLASH / RTC/ RESET CIRCUIT
37	FAN / THERMAL
38	AUDIO CODEC
39	AUDIO AMP
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41	BLANK
42	Charger (ISL88731)
43	CPU CORE(NCP6131S)
44	3V/5V (TPS51427A)
45	1.8V_RUN(RT8015DGQW)
46	1.5_DDR/0.75(RT8207A)
47	1.05V_VTT(VT358)
48	VCCSA(TPS51461)
49	VGA_N12x-dGFX(NCP3218MNR)
50	Run Power Switch
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52	PAD & SCREW
53	SMBUS BLOCK
54	THERMAL MAP
55	Power Block Diagram
56	Power sequence Block
57	power sequence(DIS)
58	power sequence(UMA)
59	power sequence(OPTIMUS)

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

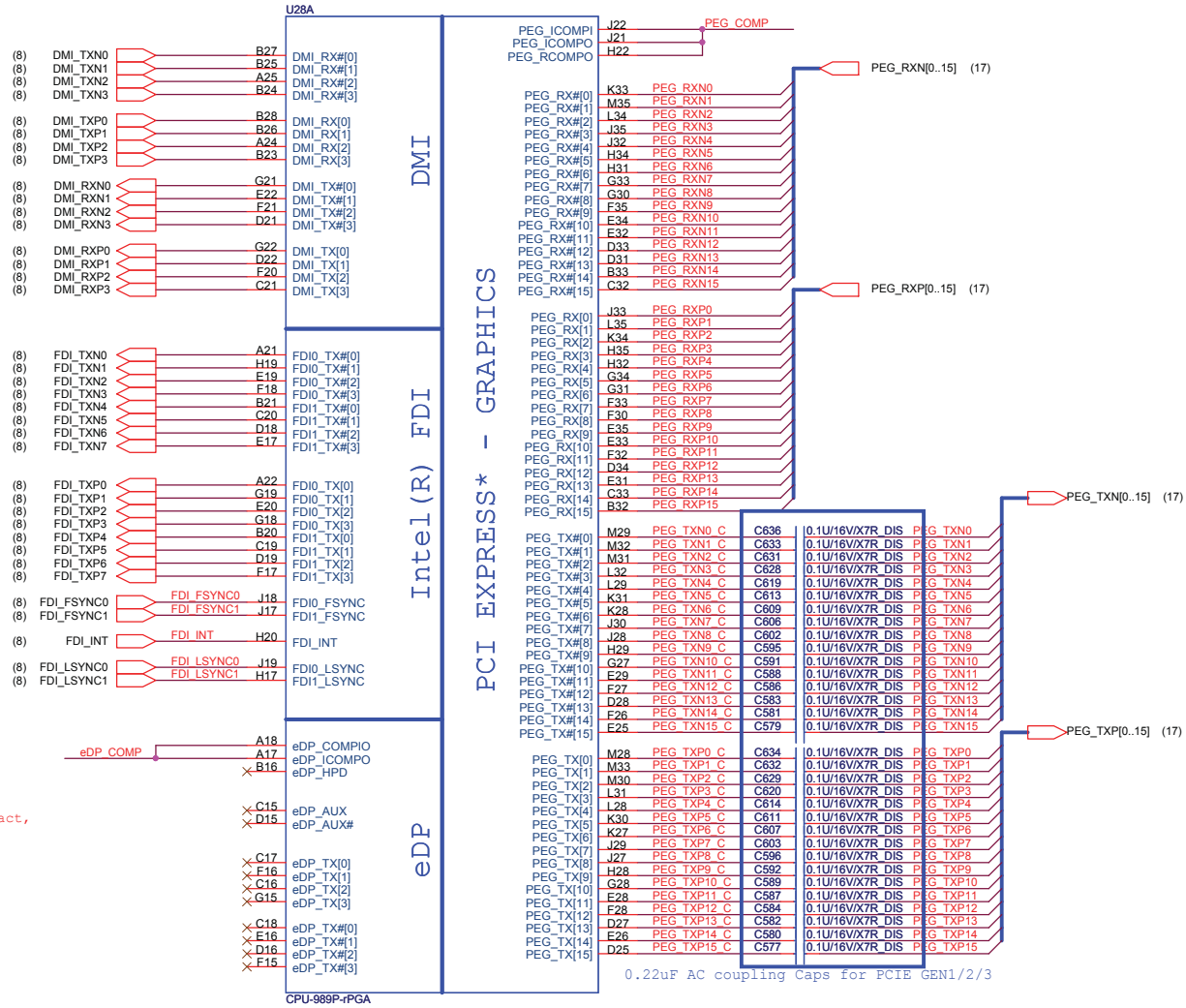
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



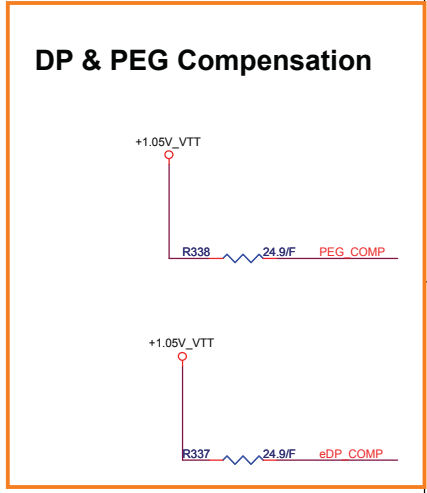
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Frontage	1A
Date: Friday, January 07, 2011		Sheet 2 of 59

Sandy Bridge Processor (DMI, PEG, FDI)

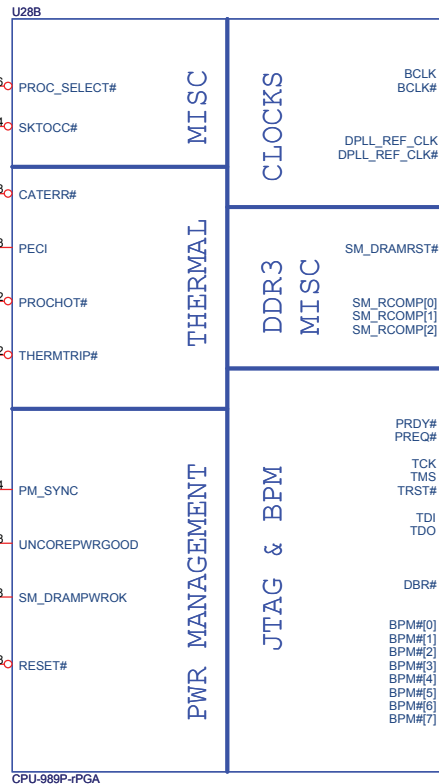


- DG (V0.5) P66:
- FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be tied to GND (through 1K ±5% resistors); In addition, can be ganged together with one resistor [1K ±5% resistors].
 - If left as no connect, there is no functional impact, but power (~15mW) may be wasted.



Sandy Bridge Processor (CLK, MISC, JTAG)

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)

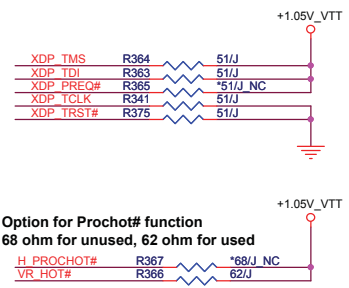


	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

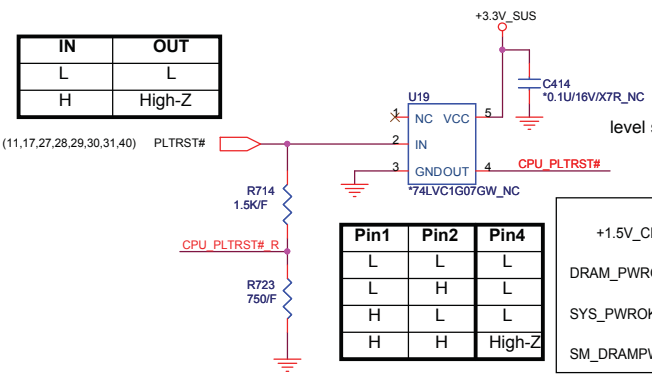
26.1 change to 25 ohm

shut down when asserted
Over 130 degree C will drive low

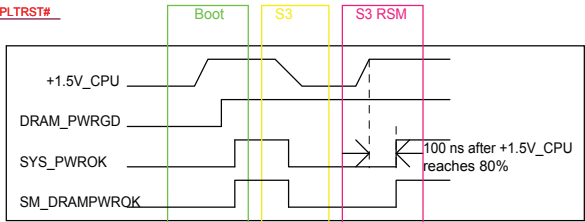
provide power management status (form PCH to CPU)



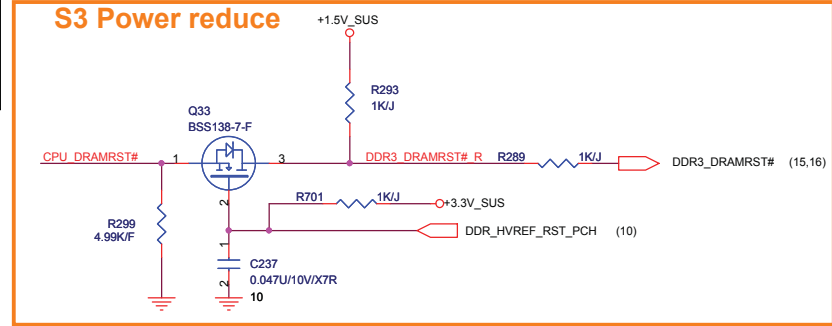
IN	OUT
L	L
H	High-Z



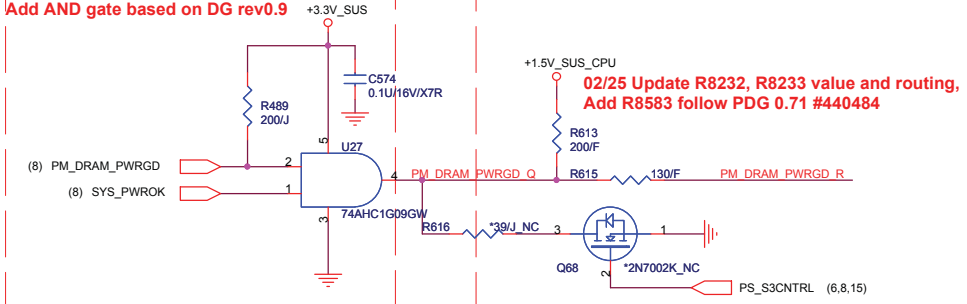
level shift for reset pin(07/12)



+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3 (Because can't reset DRAM when into S3)

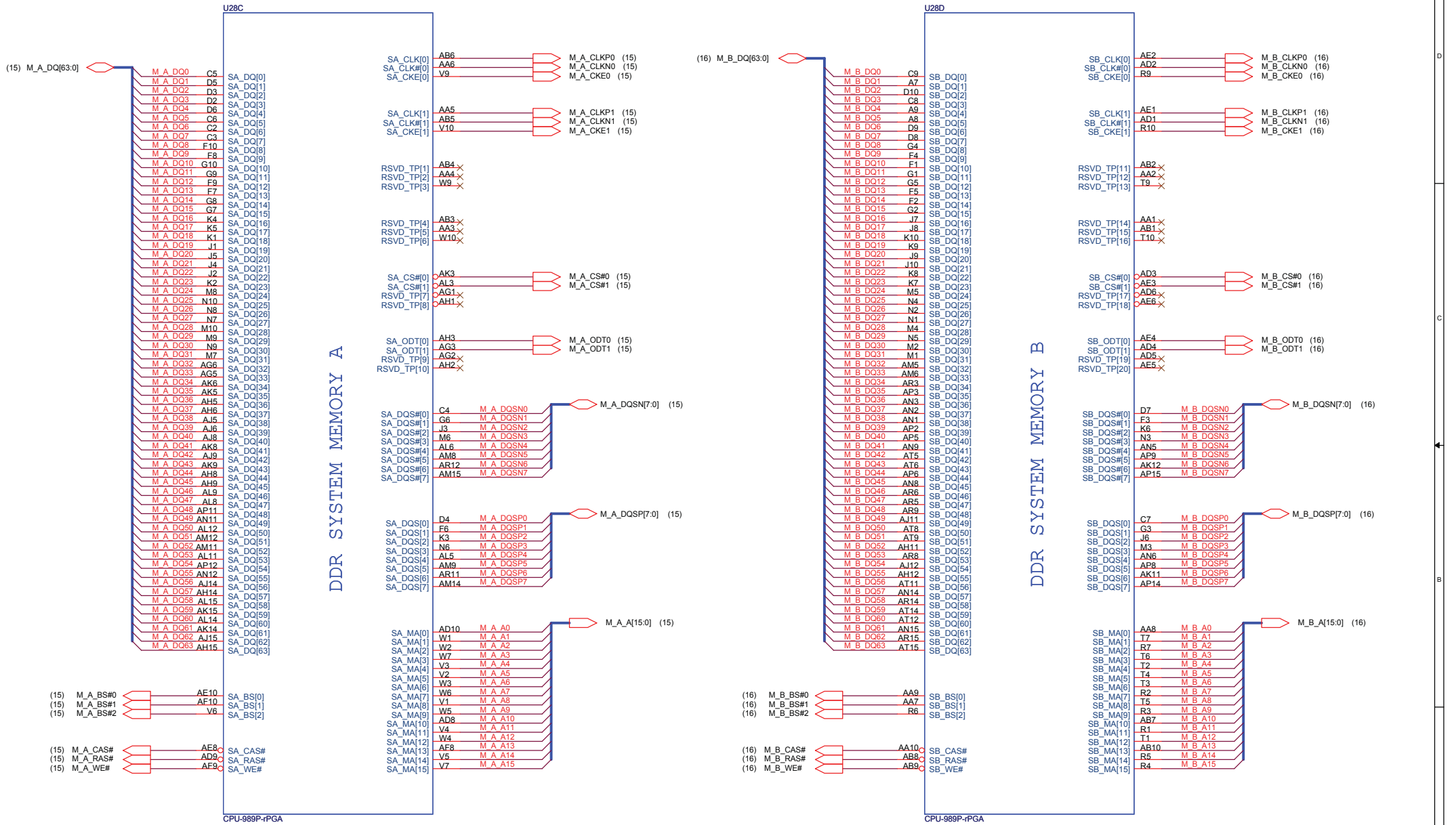


3/16 Change topology; Add AND gate based on DG rev0.9

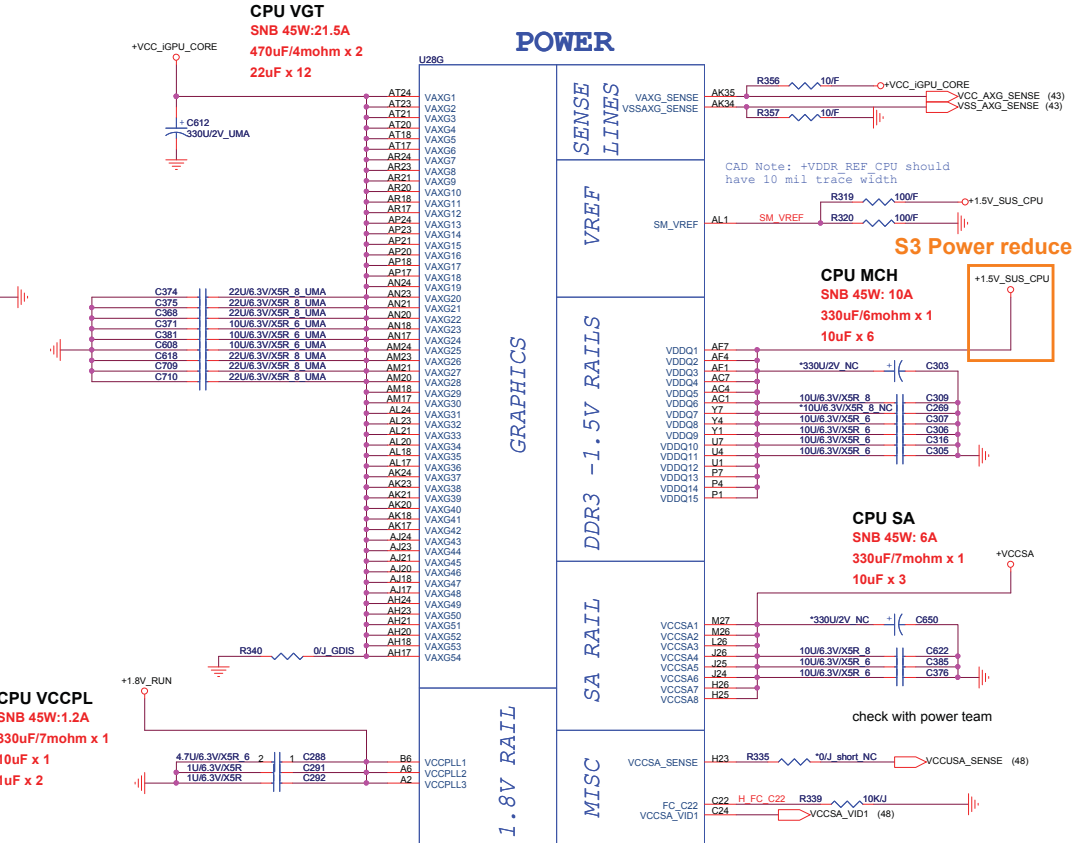
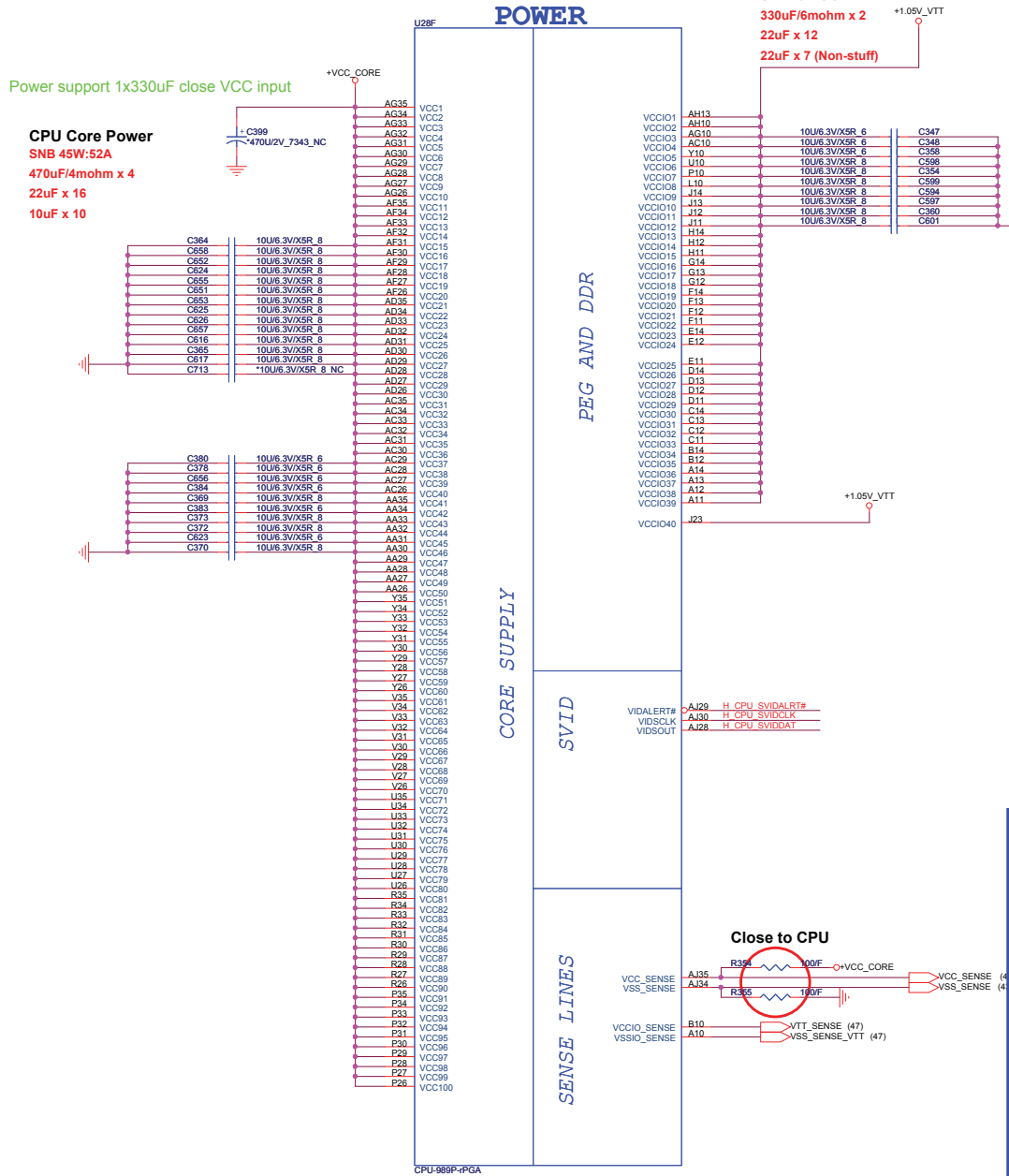


02/25 Update R8232, R8233 value and routing, Add R8583 follow PDG 0.71 #440484

Sandy Bridge Processor (DDR3)



Sandy Bridge Processor (POWER)



Power support 1x330uF close VCC input

CPU Core Power
 SNB 45W:52A
 470uF/4mohm x 4
 22uF x 16
 10uF x 10

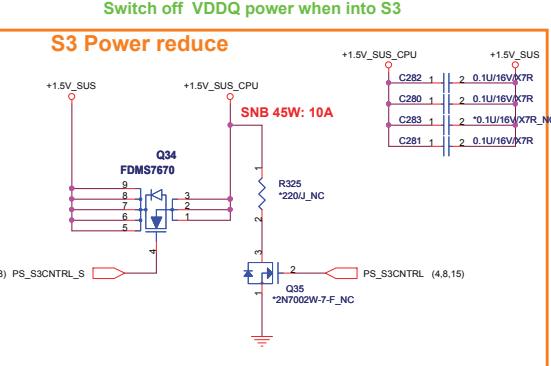
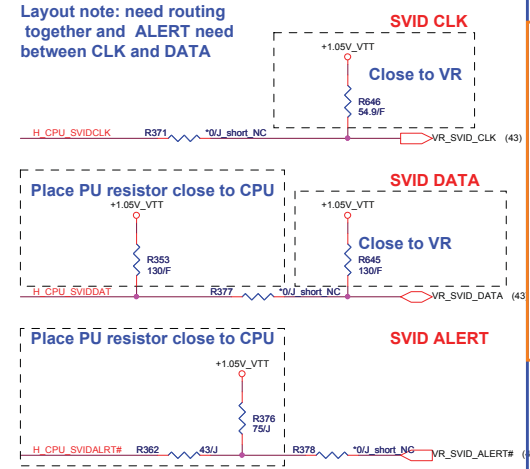
CPU VTT
 SNB 45W:8.5A
 330uF/6mohm x 2
 22uF x 12
 22uF x 7 (Non-stuff)

CPU VGT
 SNB 45W:21.5A
 470uF/4mohm x 2
 22uF x 12

CPU MCH
 SNB 45W: 10A
 330uF/6mohm x 1
 10uF x 6

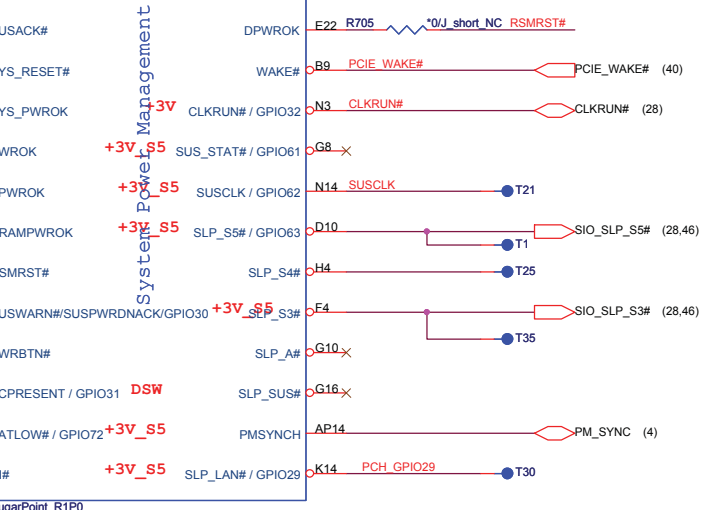
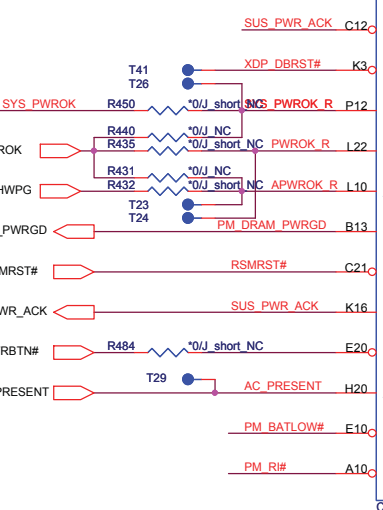
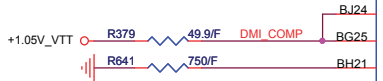
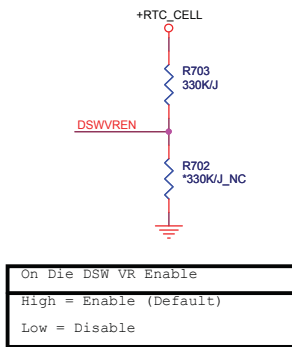
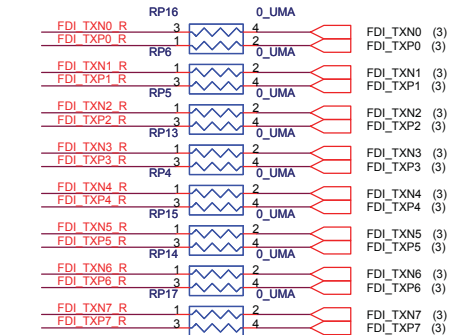
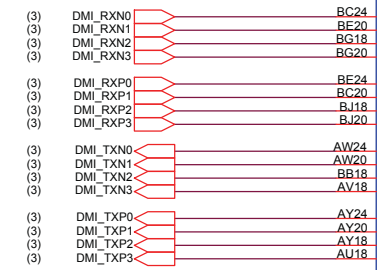
CPU SA
 SNB 45W: 6A
 330uF/7mohm x 1
 10uF x 3

CPU VCCPL
 SNB 45W:1.2A
 330uF/7mohm x 1
 10uF x 1
 1uF x 2

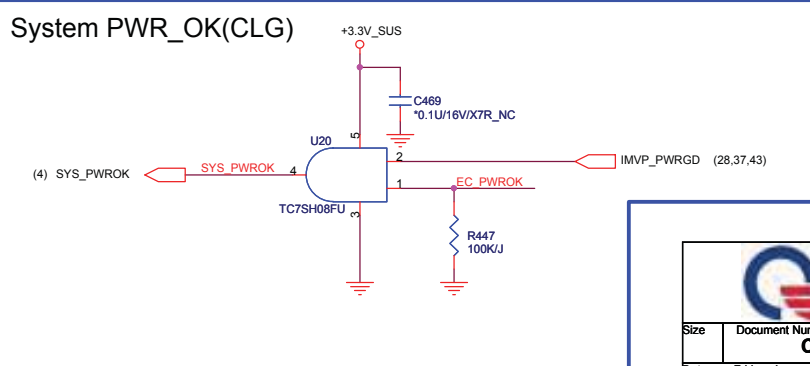
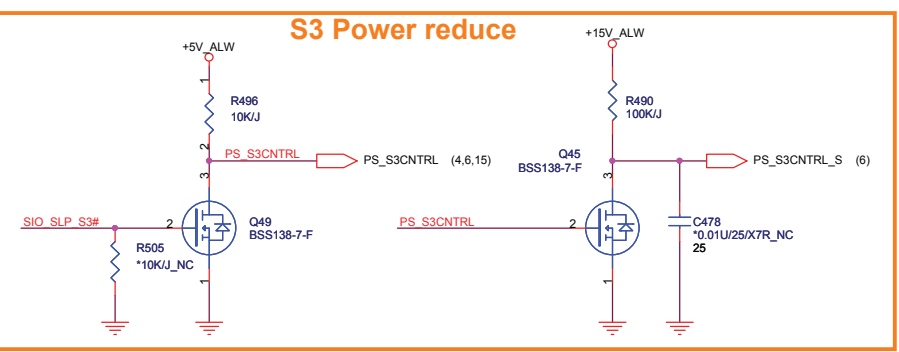
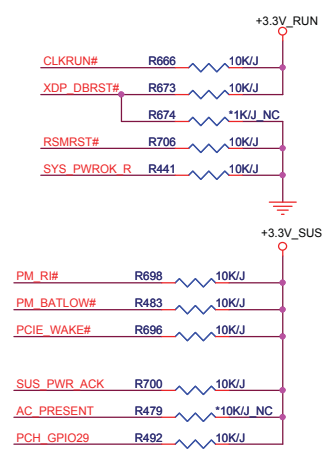


Cougar Point (DMI, FDI, PM)

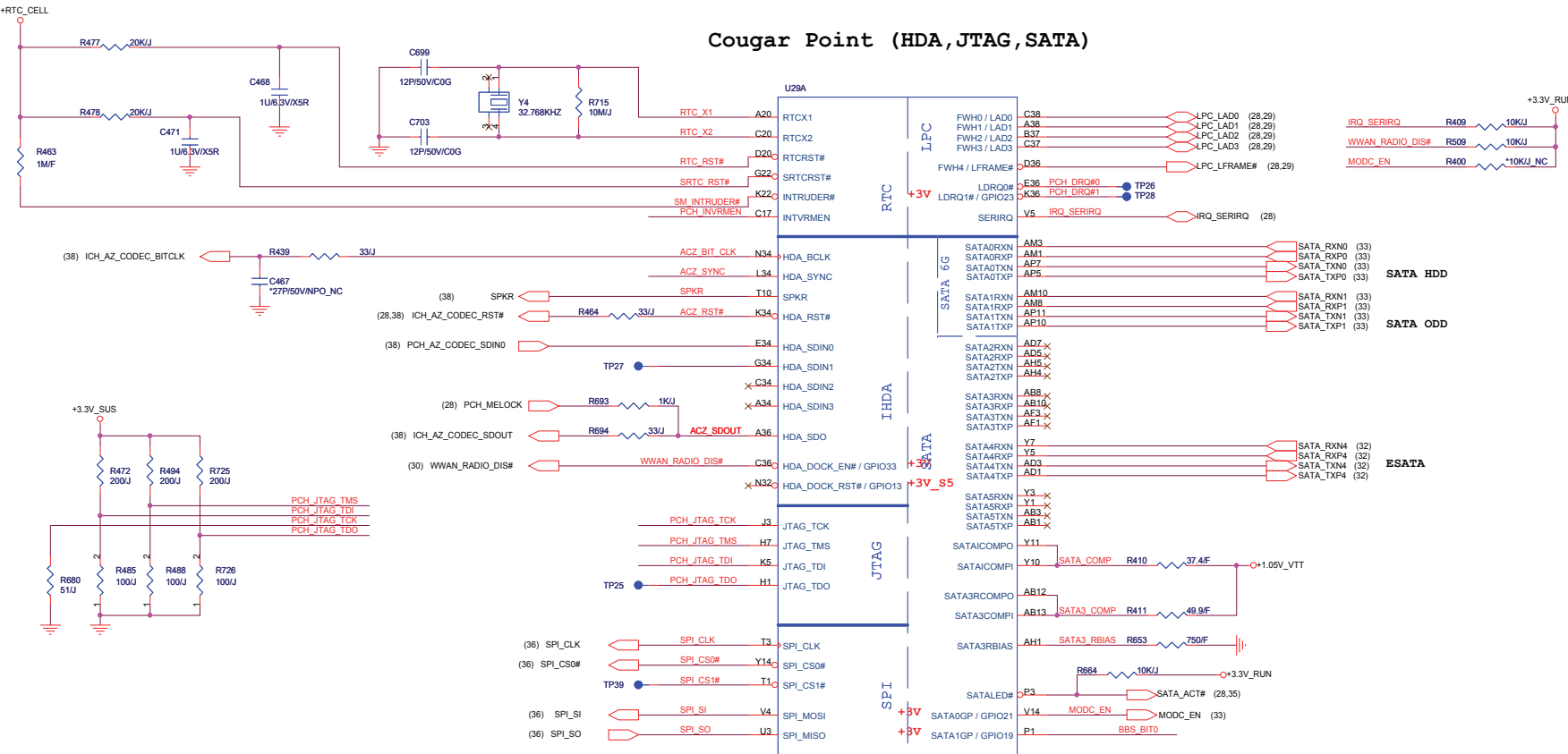
U29C



PCH Pull-high/low(CLG)



Cougar Point (HDA, JTAG, SATA)



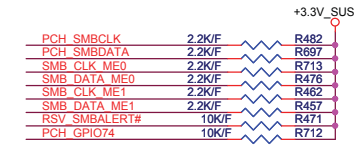
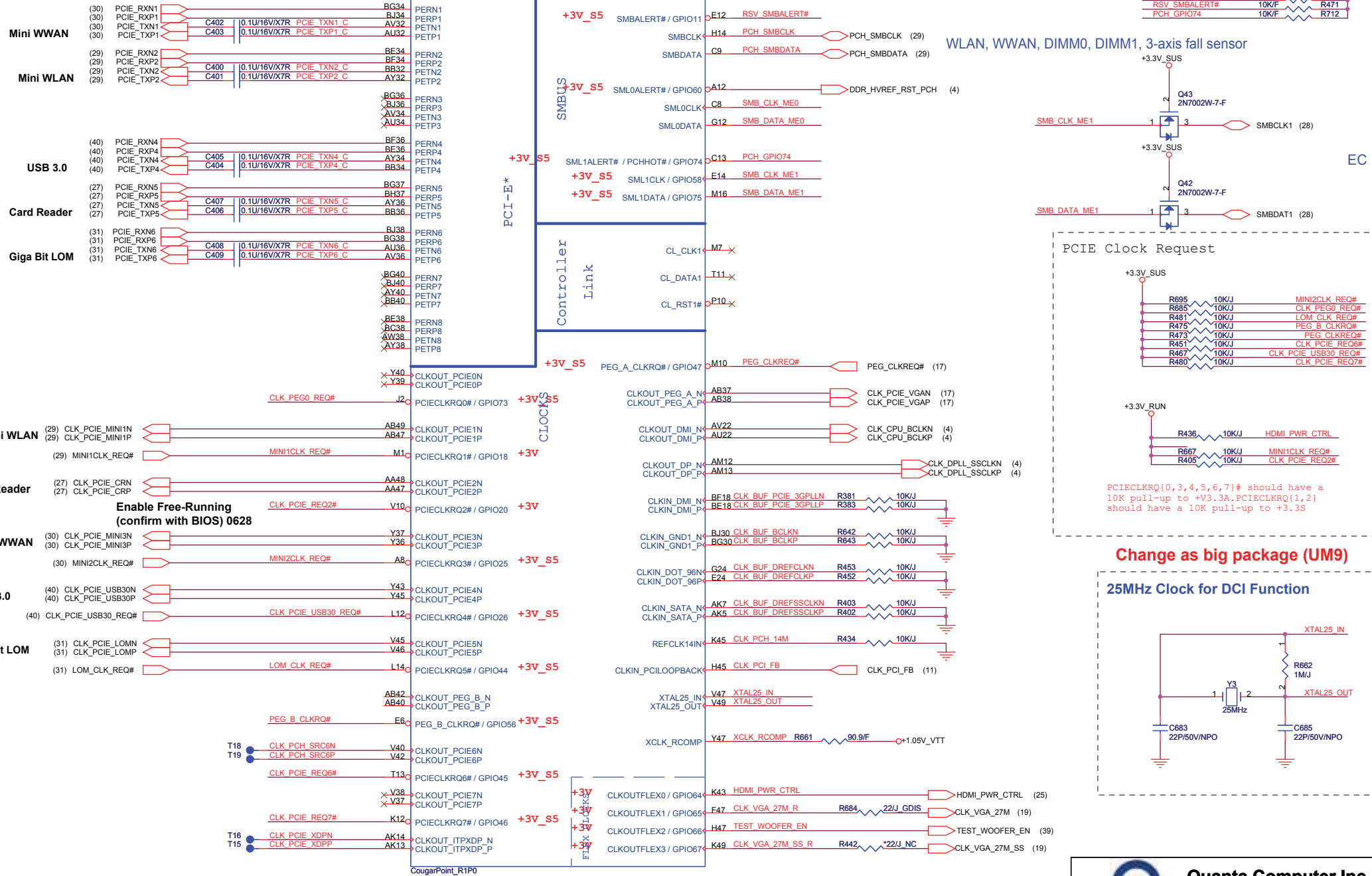
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	PCI_GNT3# (11)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	<p>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</p> BBS_BIT1 (11) BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SYNC	On-Die PLL VR Volatage Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	<p>(38) ICH_AZ_CODEEC_SYNC</p>									
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS ACZ_SDOOUT									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3.3V_SUS PLL_ODVR_EN (12)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL PCH_INVRMEN									
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm 0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	+1.8V_RUN DF_TV5 (12)									

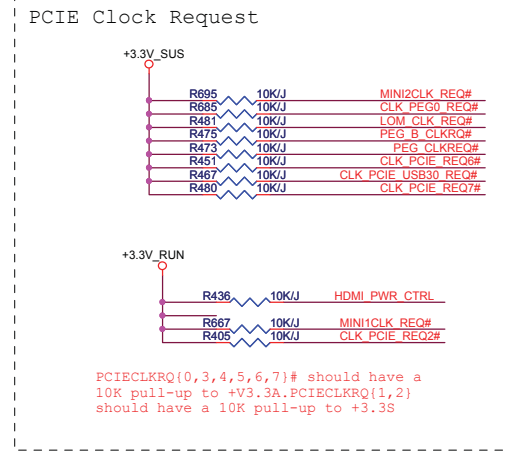
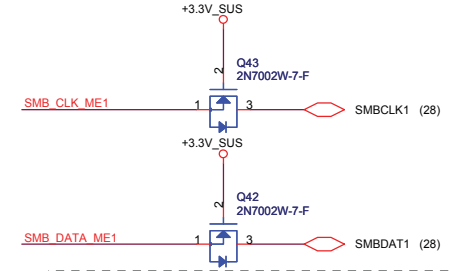
Cougar Point-M (PCI-E, SMBUS, CLK)

Note: Place TX DC blocking caps close to PCH.

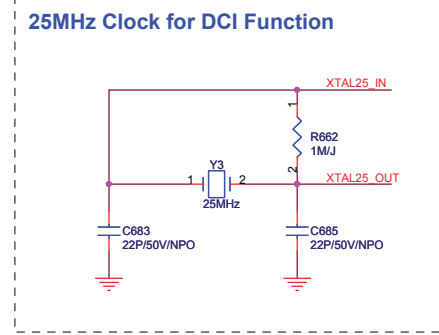
U298



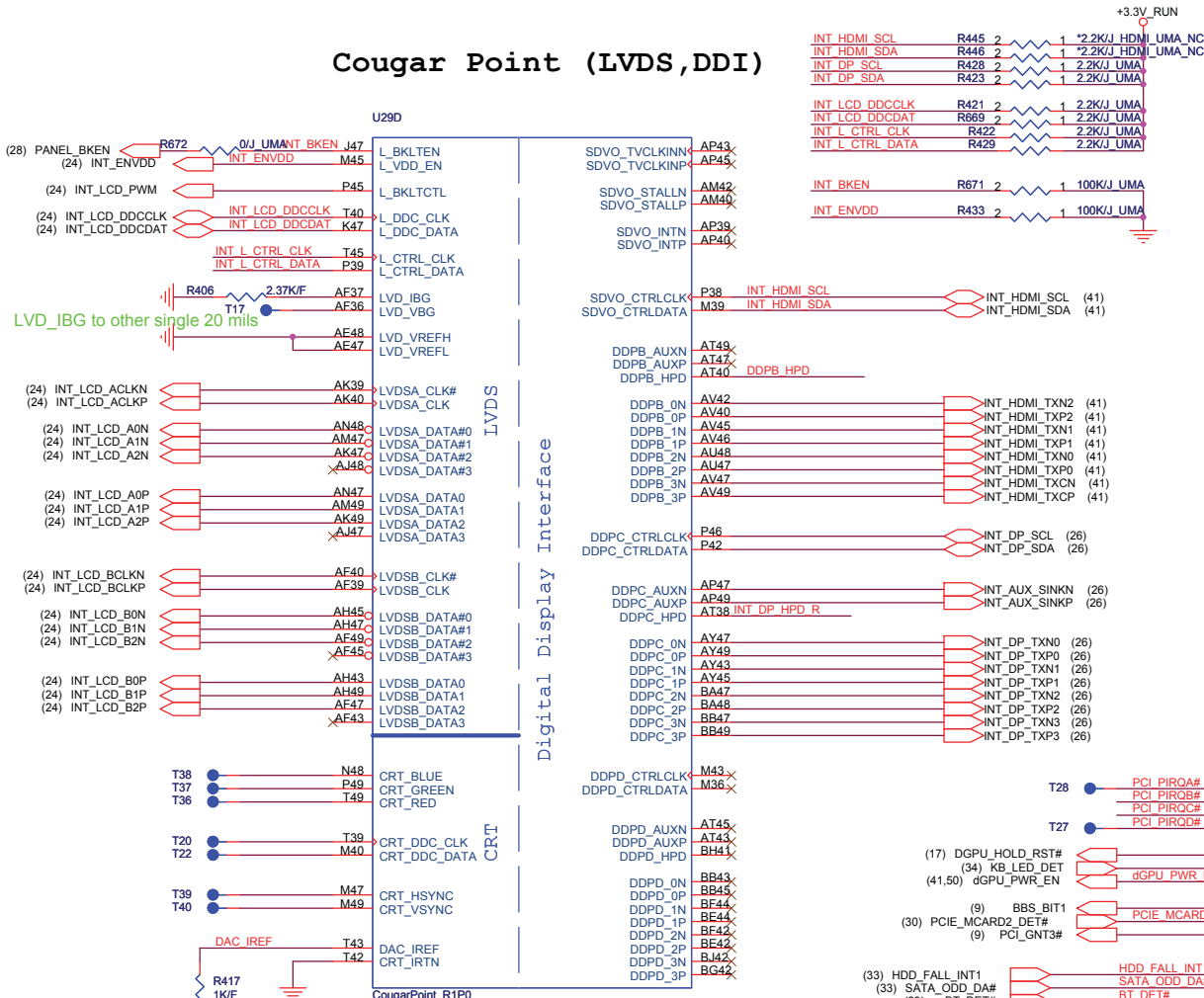
WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor



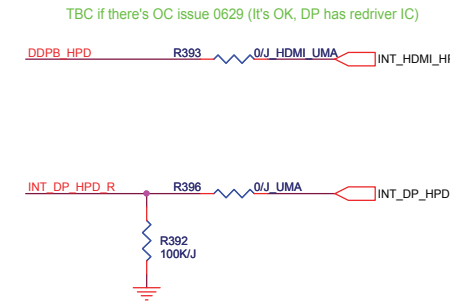
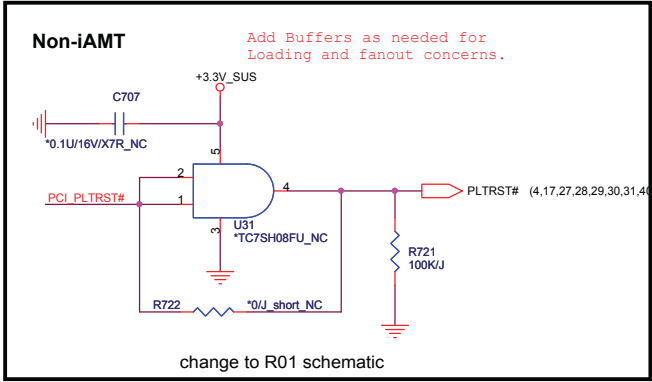
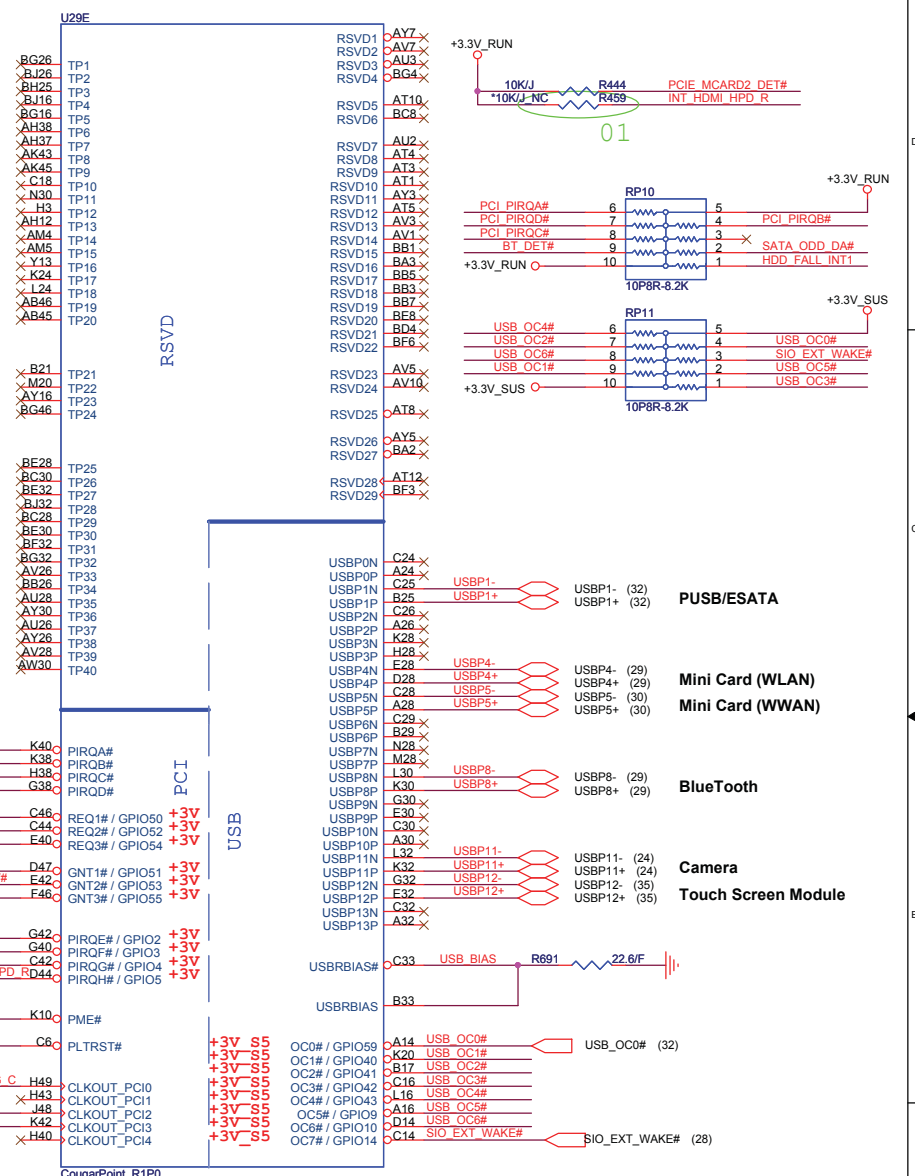
Change as big package (UM9)



Cougar Point (LVDS, DDI)



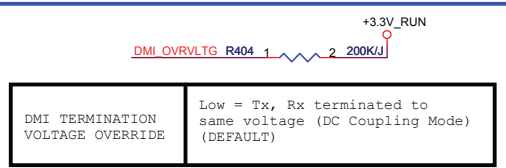
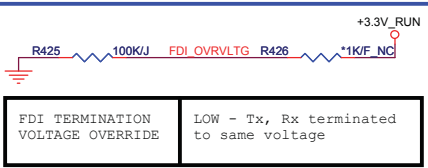
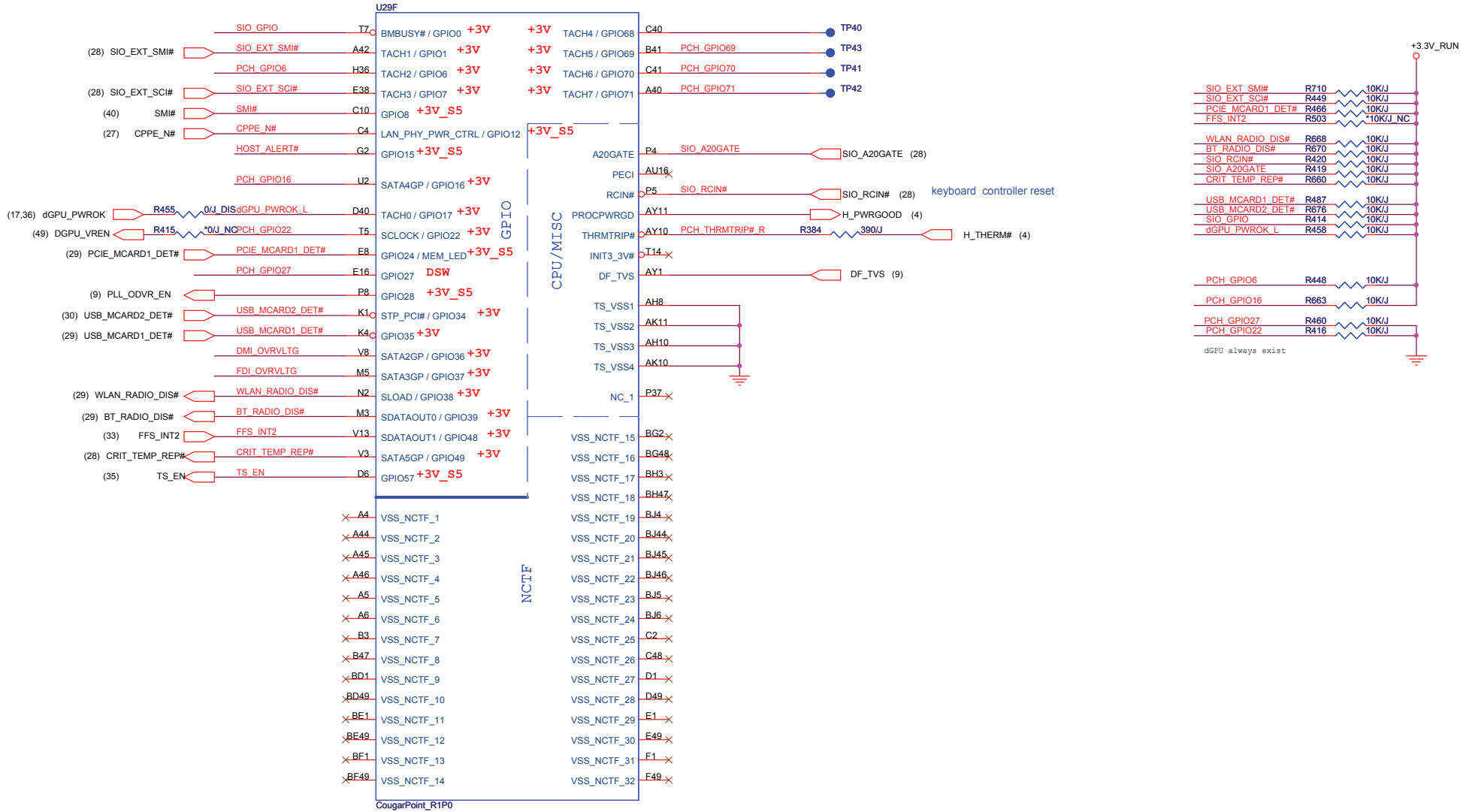
Cougar Point-M (PCI, USB, NVRAM)



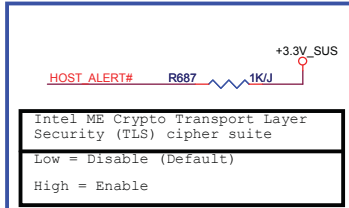
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

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Cougar Point (GPIO, VSS_NCTF, RSVD)



internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)

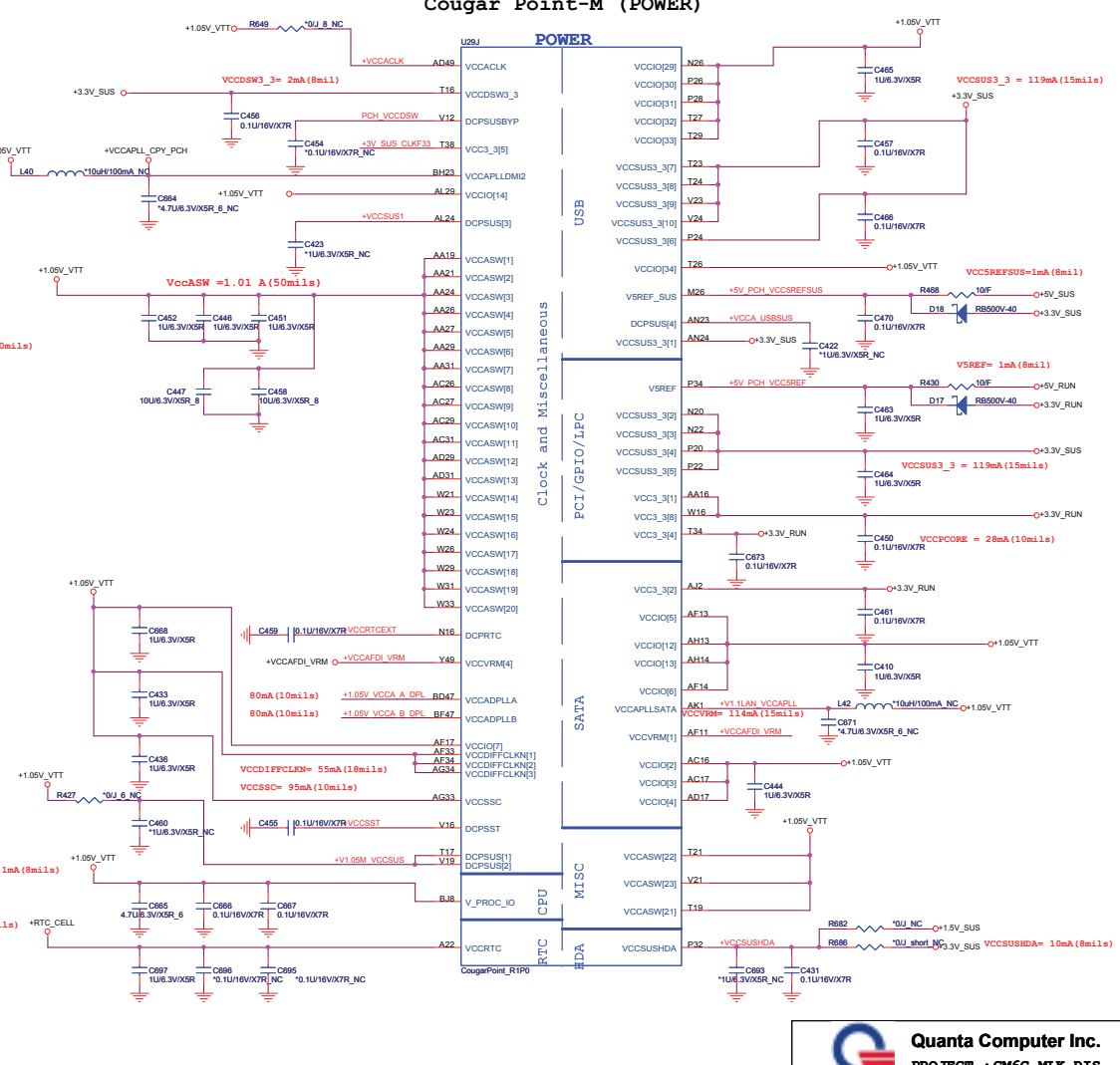
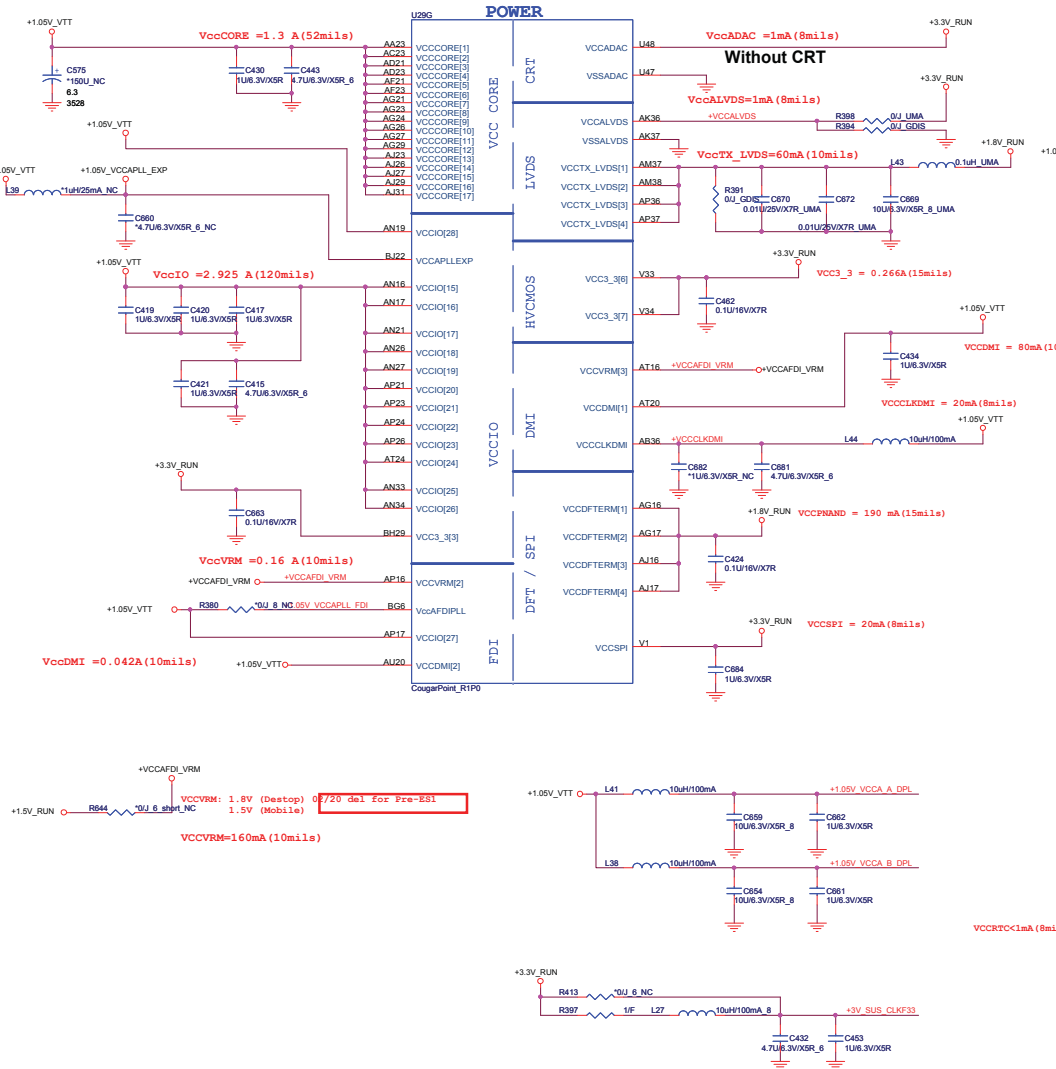


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PROJECT : GM6C MLK DIS

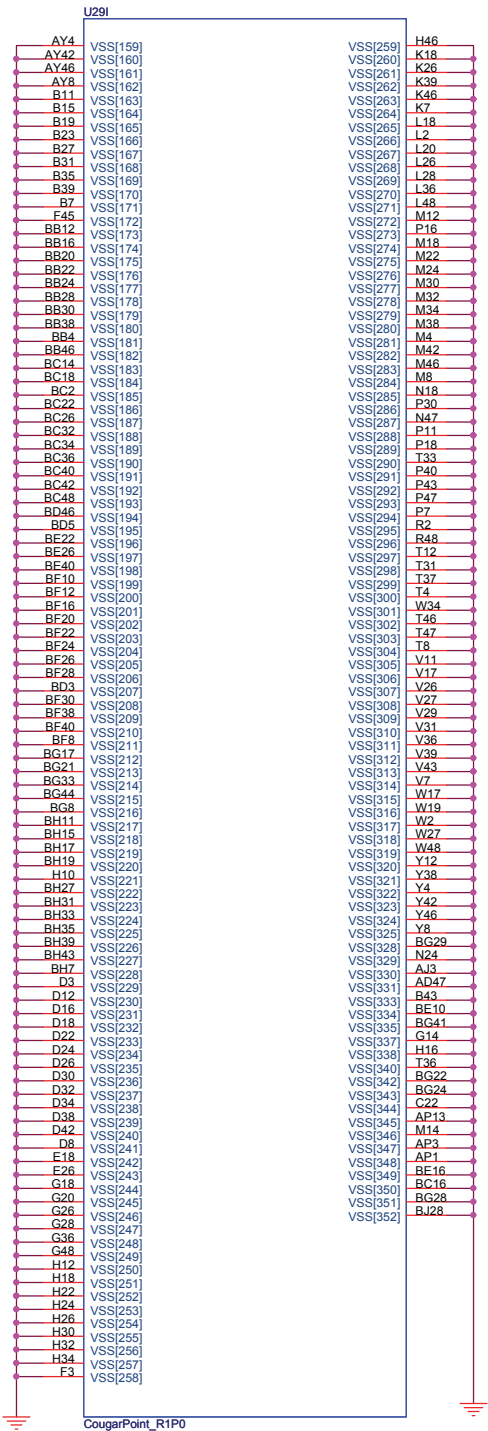
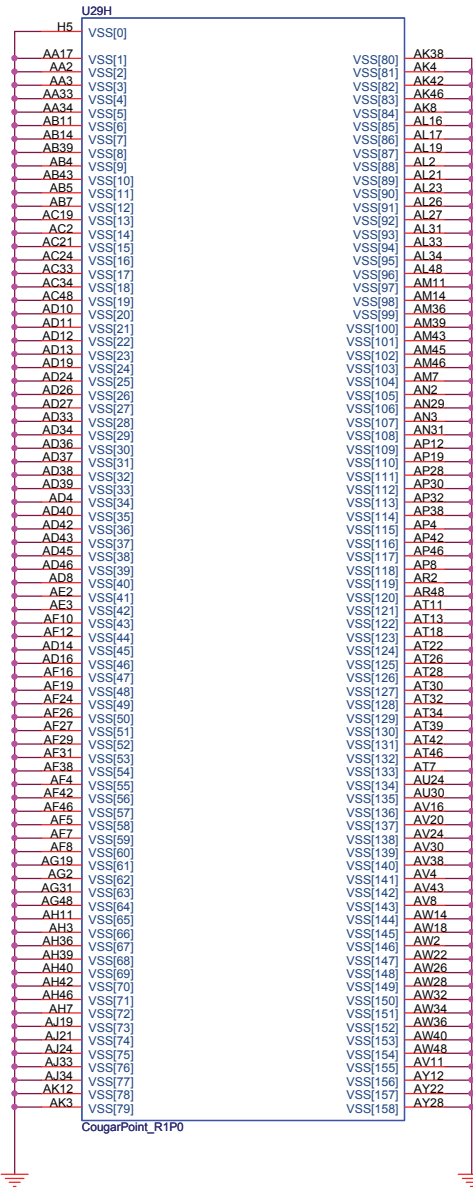

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Cougar Point 5/7			

COUGAR POINT (POWER)

Cougar Point-M (POWER)



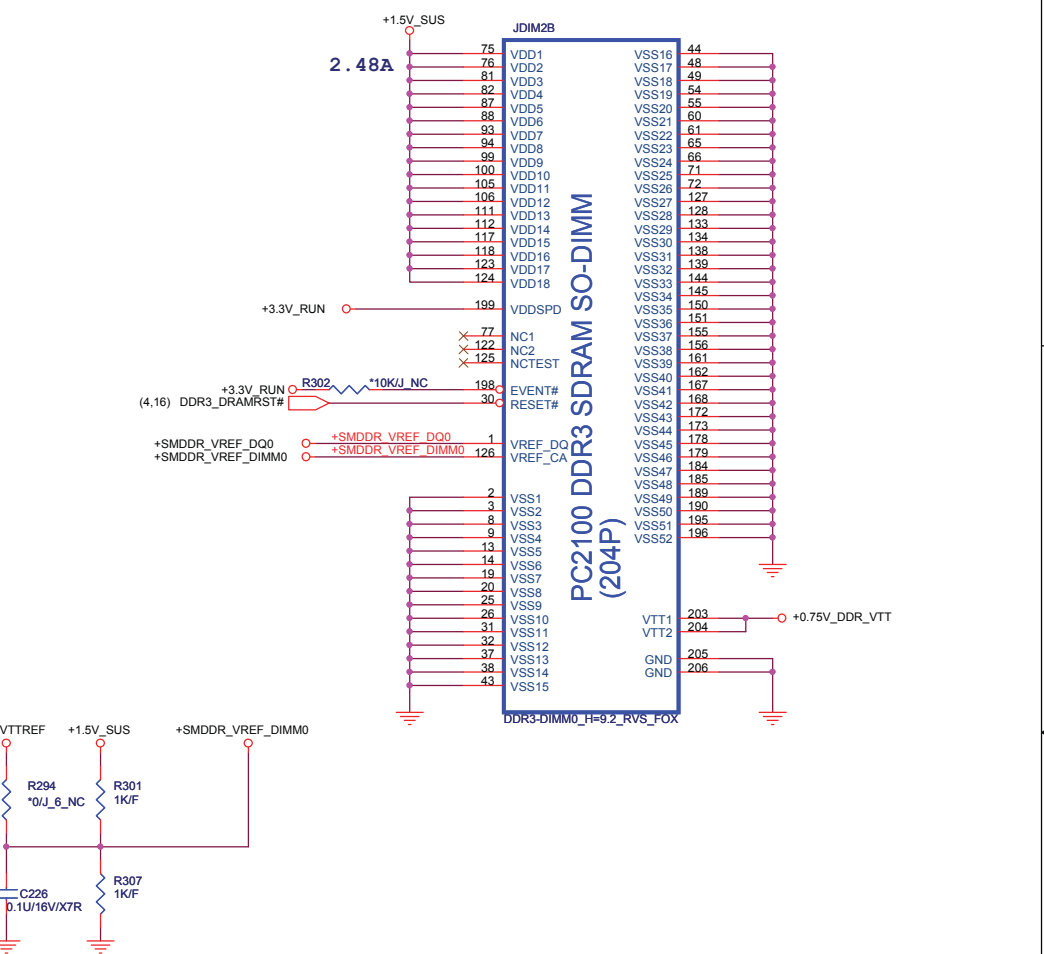
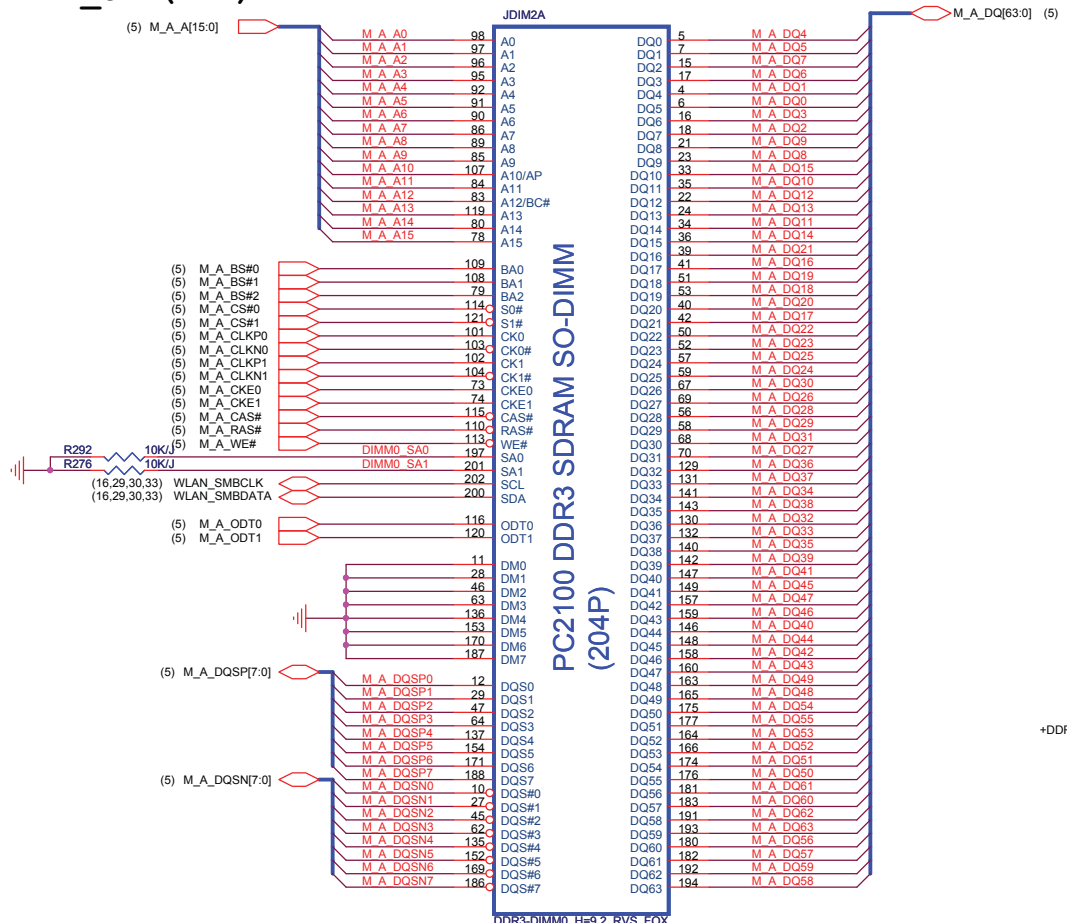
IBEX PEAK-M (GND)

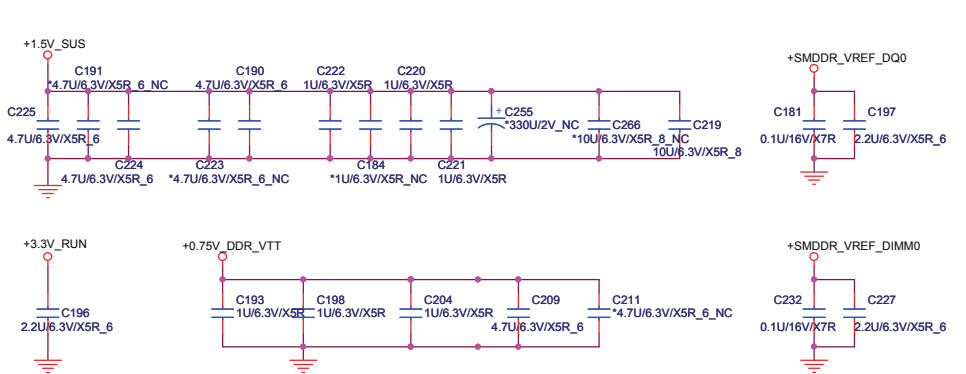
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

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	Cougar Point 717	1A
Date:	Friday, January 07, 2011	Sheet 14 of 59

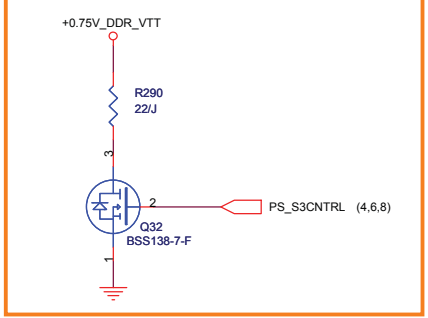
DDR STD (DDR)



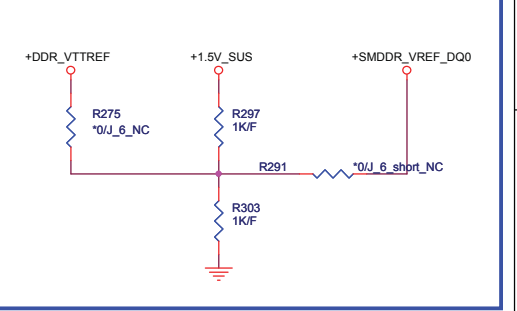
Place these Caps near So-Dimm0.

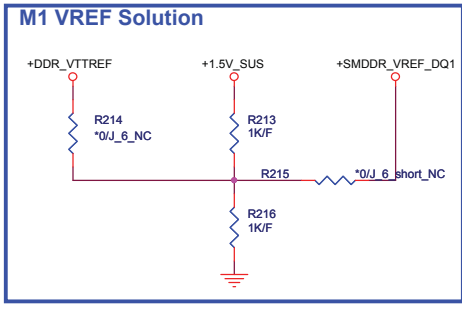
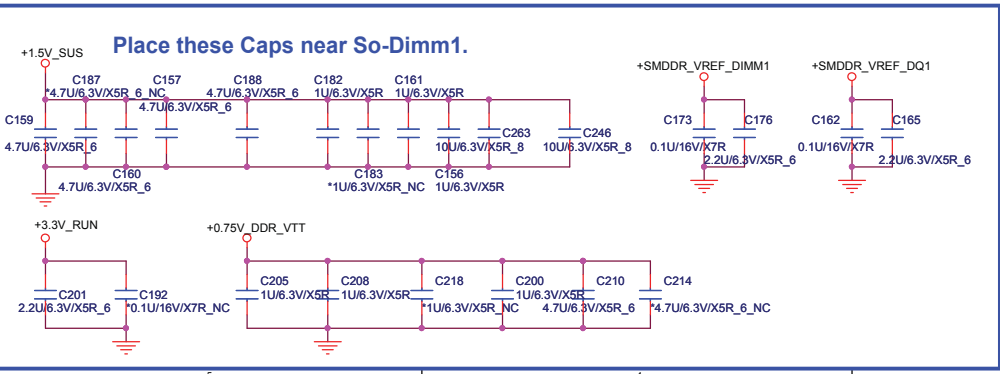
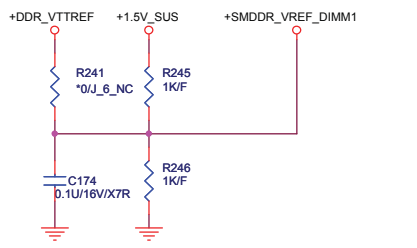
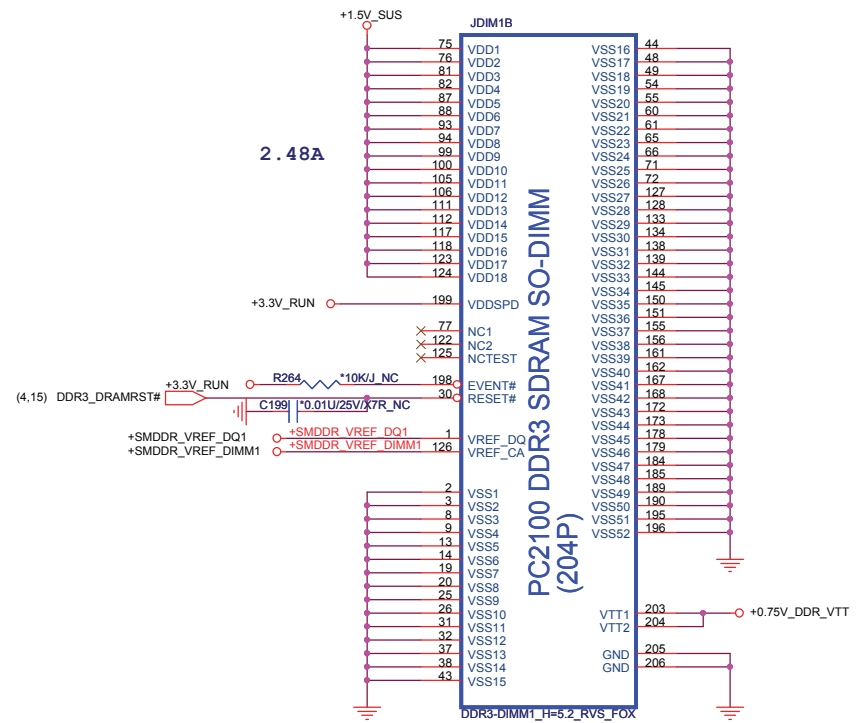
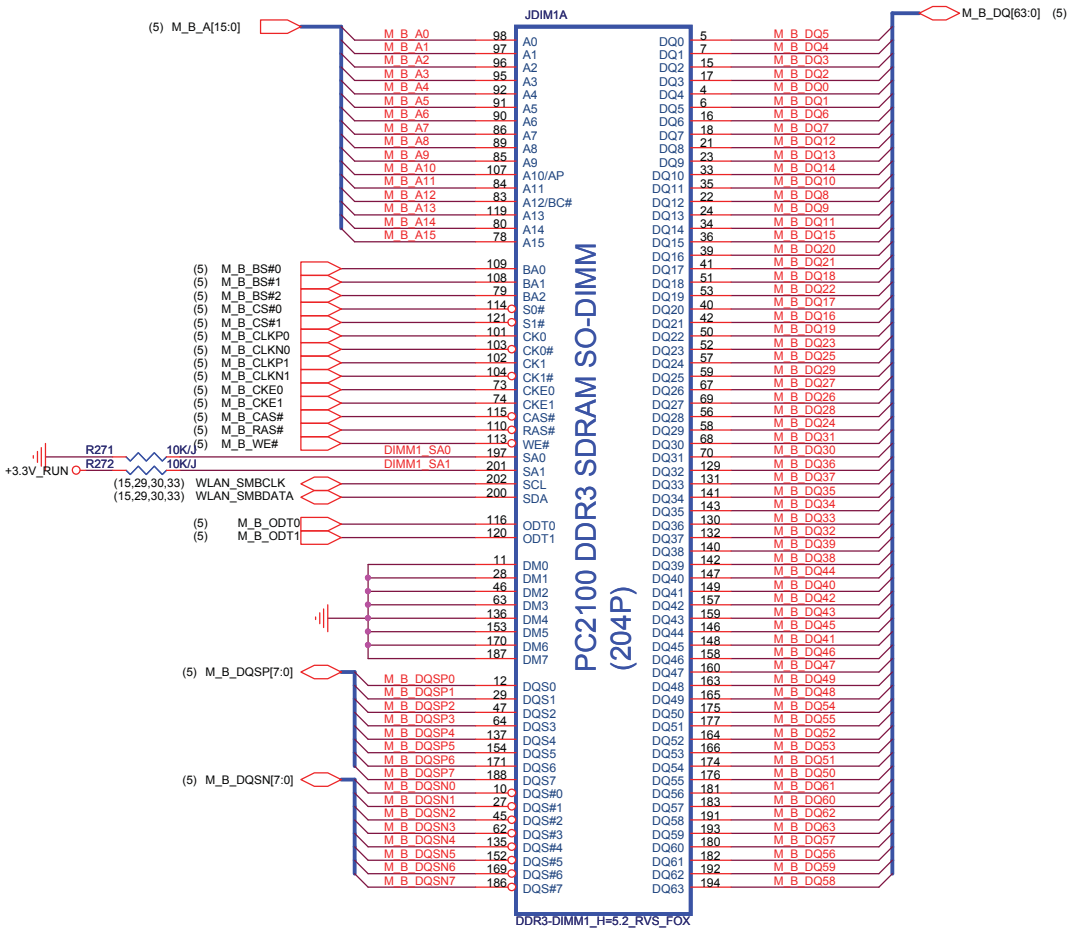


S3 Power reduce

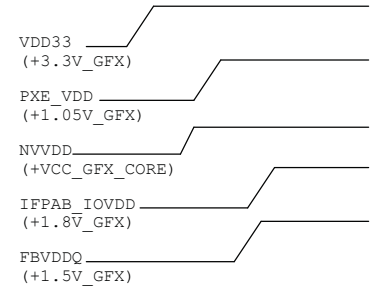


M1 VREF Solution

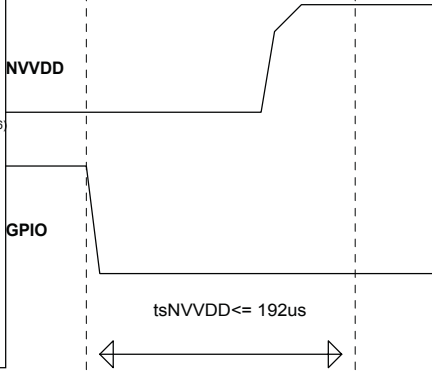




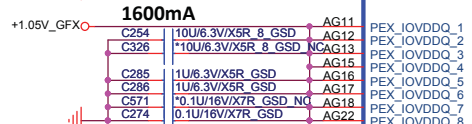
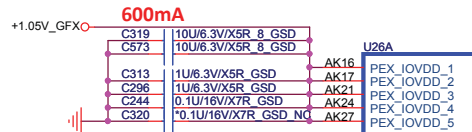
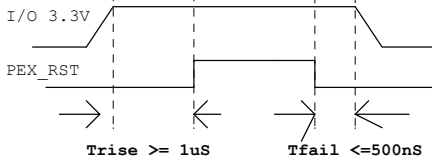
power up sequence



NVVDD Maximum Settling Time



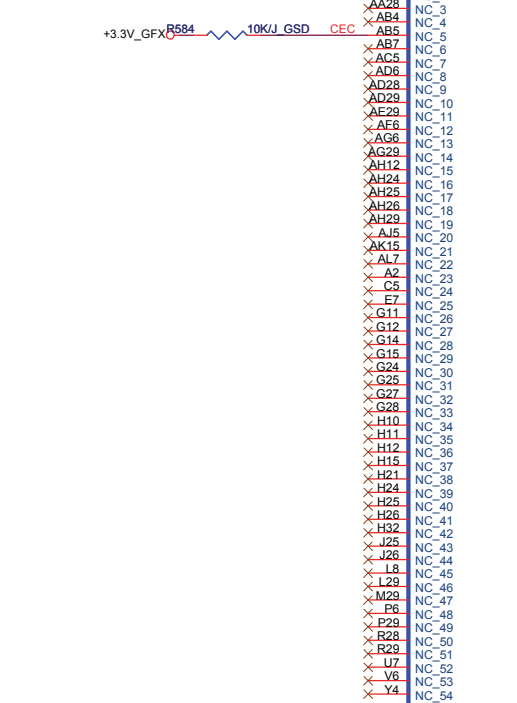
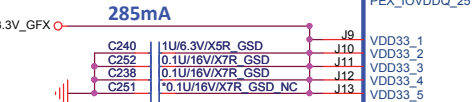
PEX_RST timing



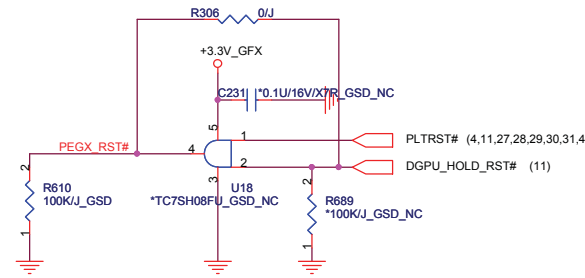
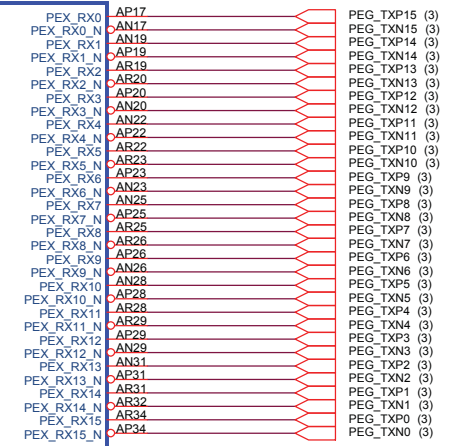
CAP CLOSE TO BGA

PEX_IOVDDQ
 DG-05093-001_V02:Page 71
 Remove 0.1uF-C10117, C10162, C10048, C10041, C10032
 Scott-0710

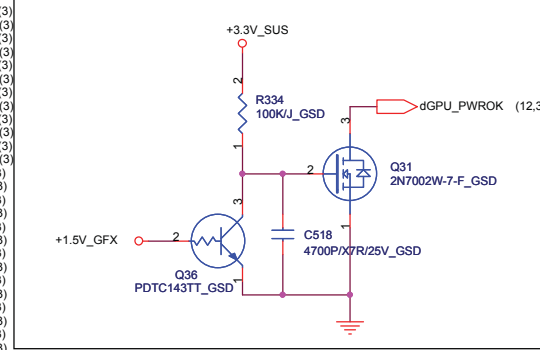
VDD33
 DG-05093-001_V02:Page 168
 120mA/non-SLI, 285mA/SLI
 Scott-0710



[PEG Interface]



GPU all PWROK

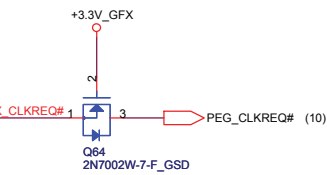


PEX_TSTCLK_OUT/PEX_TSTCLK_OUT_N
 DG-05093-001_V02:Page 70
 default can be unstuffed
 Scott-0711

PEX_CLKREQ_N
 DG-05093-001_V02:Page 70
 Pull down 2.49K/F
 Scott-0711

PEX_TERM
 DG-05093-001_V02:Page 70
 Pull down 2.49K/F
 Scott-0711

TESTMODE
 DG-05093-001_V02:Page 207
 Pull down 10K
 Scott-0711



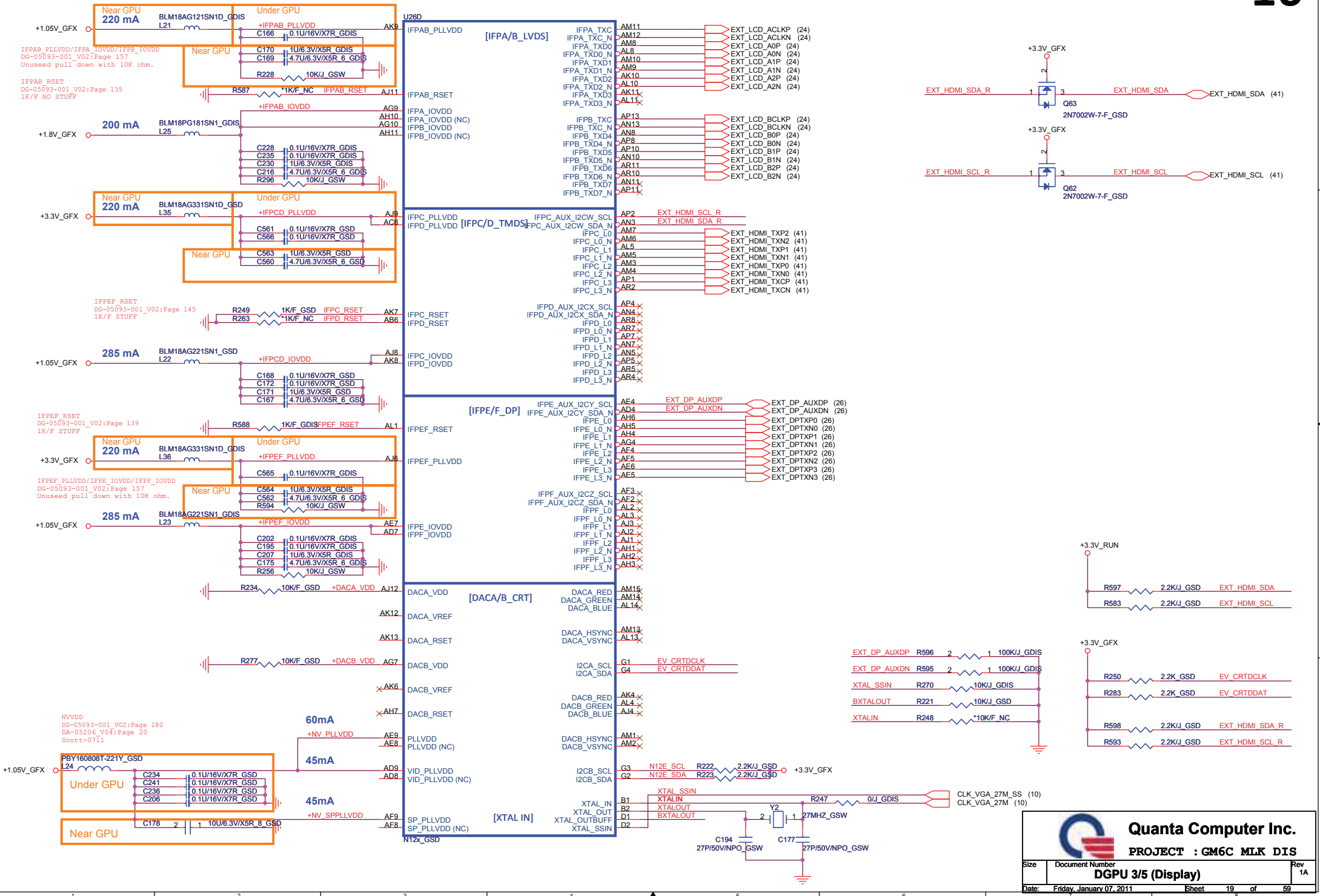
PEX_CLKREQ# circuite is different with GM6.
 Confirm with GM6

PEX_PLLVDD
 DG-05093-001_V02:Page 71,72
 120mA each
 Scott-0710

240mA
24~32 mils width

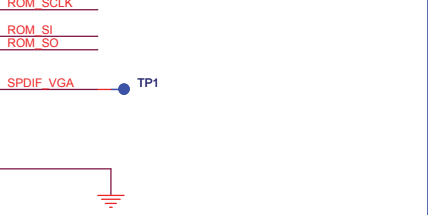
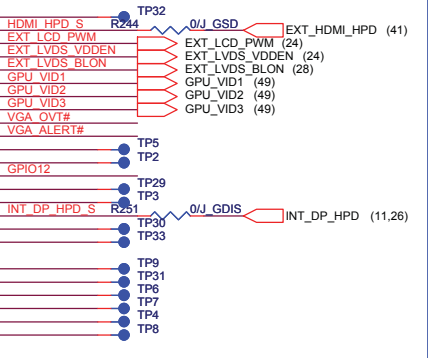
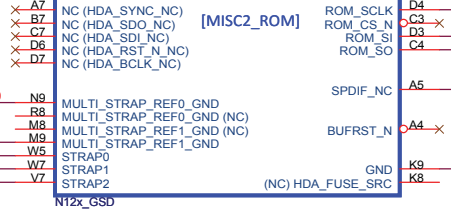
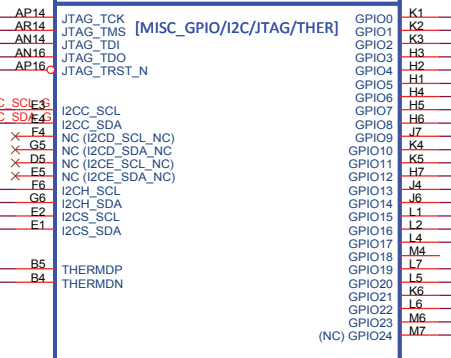
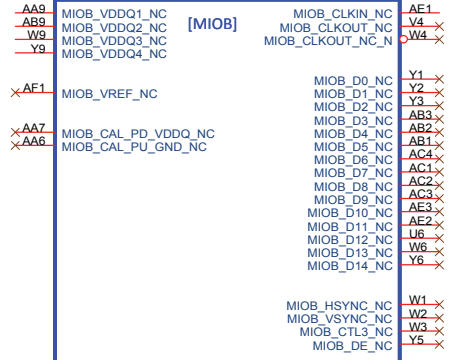
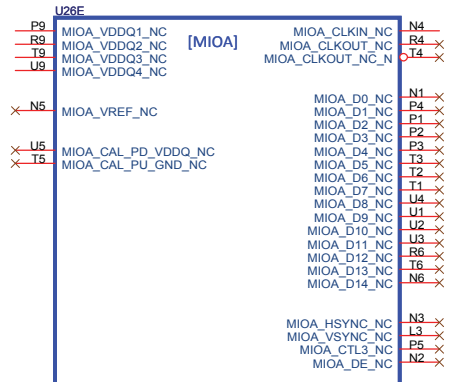
Quanta Computer Inc.
 PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A
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Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 3/5 (Display)	1A
Date:	Friday, January 07, 2011	Sheet 19 of 59



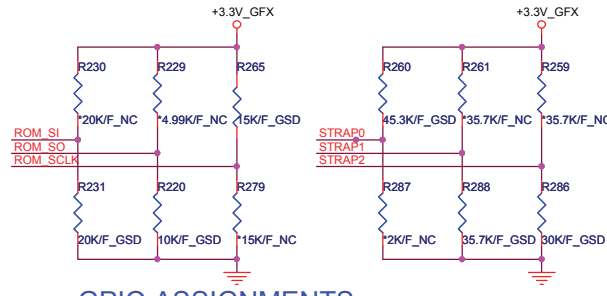
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGH7500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63BFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

ROM_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

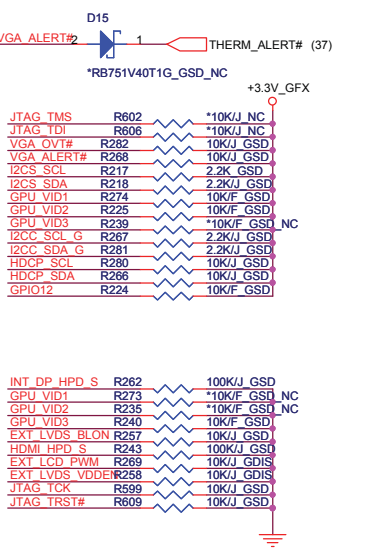



STRAP2 ROM_SCLK

	PD	PU	PU	
N12P-GE (AJON12P0f02)	30K	15K	0xDF5	
N12P-GT (AJON12P0f03)	35K	15K	0xDF6	
N12P-GS (AJON12P0f04)	25K	15K	0xDF4	

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC Power Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	





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Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A
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31.56A

+VCC_GFX_CORE

U28F	[GPU VDD]	VDD_057	P21
AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T18
AC24	VDD_022	VDD_078	T20
AC25	VDD_023	VDD_079	T22
AD12	VDD_024	VDD_080	T24
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V19
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

N12x_GSD

+VCC_GFX_CORE

U28G	[GPU GND]	GND_97	E9
AA2	GND_1	GND_97	E9
AA5	GND_2	GND_98	E12
AA11	GND_3	GND_99	E15
AA12	GND_4	GND_100	E18
AA13	GND_5	GND_101	E24
AA14	GND_6	GND_102	E27
AA15	GND_7	GND_103	E30
AA16	GND_8	GND_104	F2
AA17	GND_9	GND_105	F5
AA18	GND_10	GND_106	F31
AA19	GND_11	GND_107	F34
AA20	GND_12	GND_108	J2
AA21	GND_13	GND_109	J5
AA22	GND_14	GND_110	J31
AA23	GND_15	GND_111	J34
AA24	GND_16	GND_112	L9
AA25	GND_17	GND_113	M2
AA34	GND_18	GND_114	M5
AB12	GND_19	GND_115	M11
AB14	GND_20	GND_116	M13
AB16	GND_21	GND_117	M15
AB18	GND_22	GND_118	M17
AB20	GND_23	GND_119	M19
AB22	GND_24	GND_120	M21
AB24	GND_25	GND_121	M23
AC9	GND_26	GND_122	M25
AD11	GND_27	GND_123	M31
AD13	GND_28	GND_124	M34
AD15	GND_29	GND_125	N11
AD17	GND_30	GND_126	N12
AD2	GND_31	GND_127	N13
AD5	GND_32	GND_128	N14
AD21	GND_33	GND_129	N15
AD23	GND_34	GND_130	N16
AD25	GND_35	GND_131	N17
AD31	GND_36	GND_132	N18
AD34	GND_37	GND_133	N19
AE11	GND_38	GND_134	N20
AE12	GND_39	GND_135	N21
AE13	GND_40	GND_136	N22
AE14	GND_41	GND_137	N23
AE15	GND_42	GND_138	N24
AE16	GND_43	GND_139	N25
AE17	GND_44	GND_140	P12
AE18	GND_45	GND_141	P14
AE19	GND_46	GND_142	P16
AE20	GND_47	GND_143	P18
AE21	GND_48	GND_144	P20
AE22	GND_49	GND_145	P22
AE23	GND_50	GND_146	P24
AE24	GND_51	GND_147	R2
AE25	GND_52	GND_148	R5
AG2	GND_53	GND_149	R31
AG31	GND_54	GND_150	R34
AG34	GND_55	GND_151	T11
AK2	GND_56	GND_152	T13
AG5	GND_57	GND_153	T15
AK31	GND_58	GND_154	T17
AK34	GND_59	GND_155	T19
AK5	GND_60	GND_156	T21
AL6	GND_61	GND_157	T23
AL9	GND_62	GND_158	T25
AL12	GND_63	GND_159	U11
AL15	GND_64	GND_160	U12
AL18	GND_65	GND_161	U13
AL21	GND_66	GND_162	U14
AL24	GND_67	GND_163	U15
AL27	GND_68	GND_164	U16
AL30	GND_69	GND_165	U17
AN2	GND_70	GND_166	U18
AN34	GND_71	GND_167	U19
AP3	GND_72	GND_168	U20
AP6	GND_73	GND_169	U21
AP9	GND_74	GND_170	U22
AP12	GND_75	GND_171	U23
AP15	GND_76	GND_172	U24
AP18	GND_77	GND_173	U25
AP21	GND_78	GND_174	V2
AP24	GND_79	GND_175	V5
AP27	GND_80	GND_176	V8
AP30	GND_81	GND_177	V12
AP33	GND_82	GND_178	V14
B3	GND_83	GND_179	V16
B6	GND_84	GND_180	V18
B9	GND_85	GND_181	V20
B12	GND_86	GND_182	V22
B15	GND_87	GND_183	V24
B21	GND_88	GND_184	V31
B24	GND_89	GND_185	Y11
B27	GND_90	GND_186	Y13
B30	GND_91	GND_187	Y15
B33	GND_92	GND_188	Y17
C2	GND_93	GND_189	Y19
C34	GND_94	GND_190	Y21
E6	GND_95	GND_191	Y23
	GND_96	GND_192	Y25

N12x_GSD

PLACE UNDER BALLS

+VCC_GFX_CORE	Component	Value	Footprint
	C250	0.01U/25V/X7R	GSD
	C247	0.01U/25V/X7R	GSD
	C243	0.01U/25V/X7R	GSD
	C265	*0.01U/25V/X7R	GSD NC
	C284	0.01U/25V/X7R	GSD
	C311	0.01U/25V/X7R	GSD
	C289	*0.01U/25V/X7R	GSD NC
	C257	*0.01U/25V/X7R	GSD NC
	C253	0.022U/16V/X7R	GSD
	C277	0.022U/16V/X7R	GSD
	C267	0.022U/16V/X7R	GSD
	C248	0.047U/10V/X7R	GSD
	C271	0.047U/10V/X7R	GSD
	C239	0.047U/10V/X7R	GSD
	C301	0.1U/16V/X7R	GSD
	C299	0.1U/16V/X7R	GSD
	C258	0.22U/6.3V/X5R	GSD
	C295	0.22U/6.3V/X5R	GSD
	C297	0.22U/6.3V/X5R	GSD
	C276	1U/6.3V/X5R	GSD

NV/VDD DA-05206_V04:Page 20 Scott-0710

PLACE NEAR BALLS

+VCC_GFX_CORE	Component	Value	Footprint
	C294	4.7U/6.3V/X5R	6_GSD
	C711	22U/6.3V/X5R	8_GSD
	C712	22U/6.3V/X5R	8_GSD
	C270	22U/6.3V/X5R	8_GSD
	C308	22U/6.3V/X5R	8_GSD
	C317	22U/6.3V/X5R	8_GSD
	C318	22U/6.3V/X5R	8_GSD

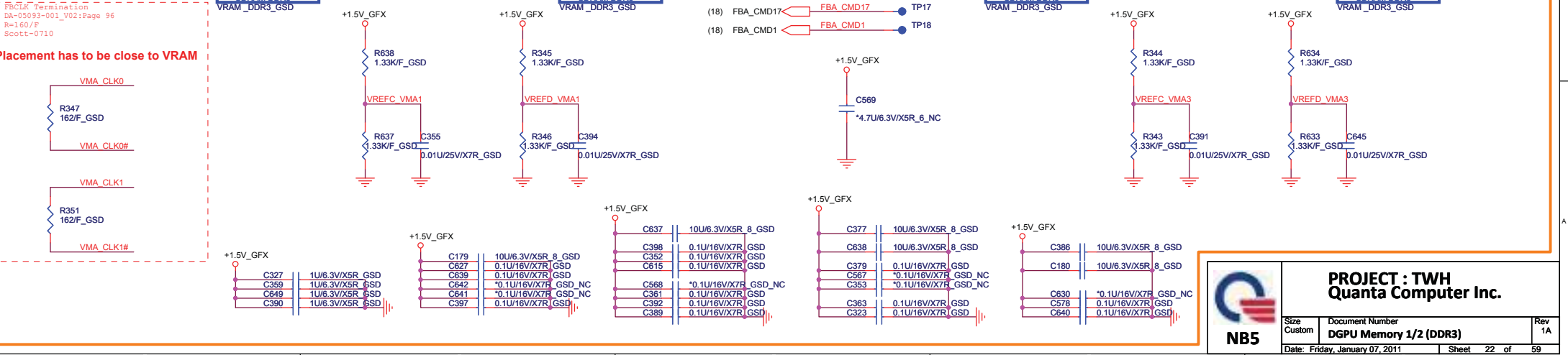
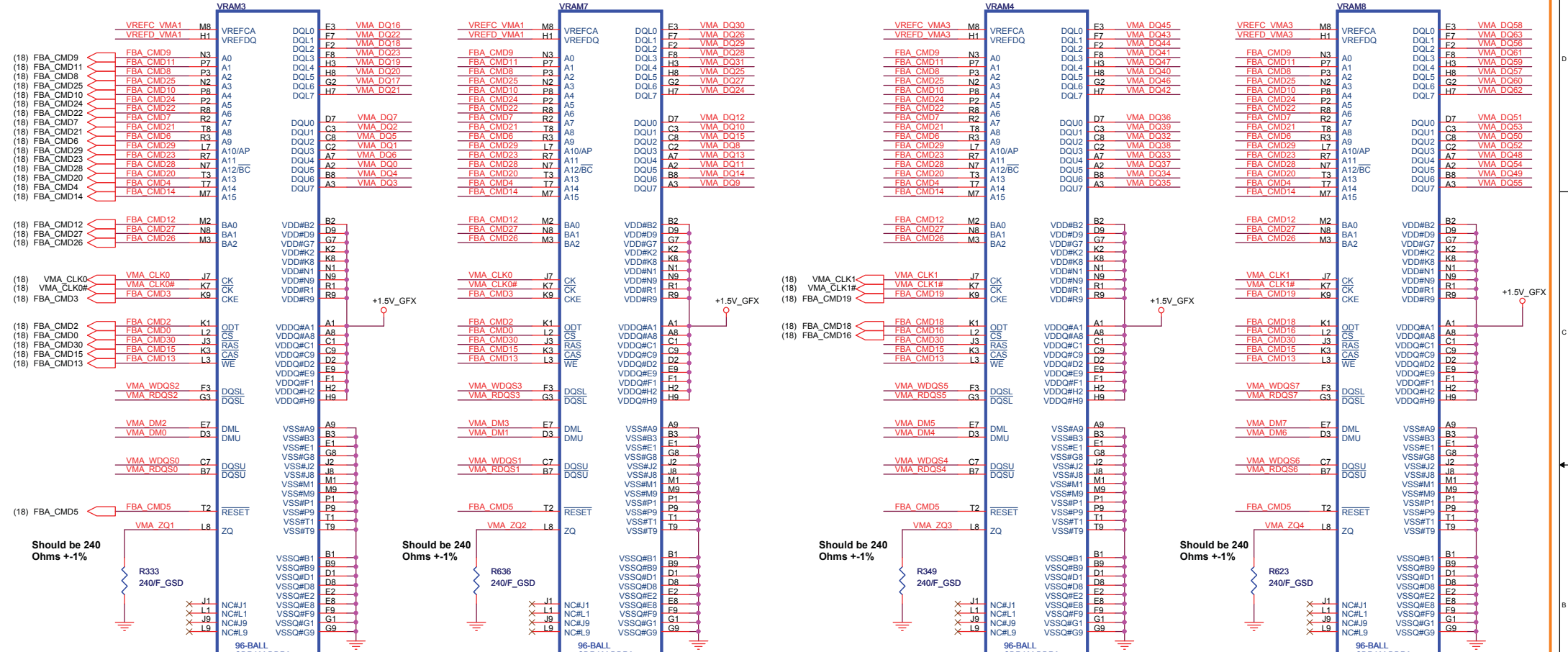


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PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A
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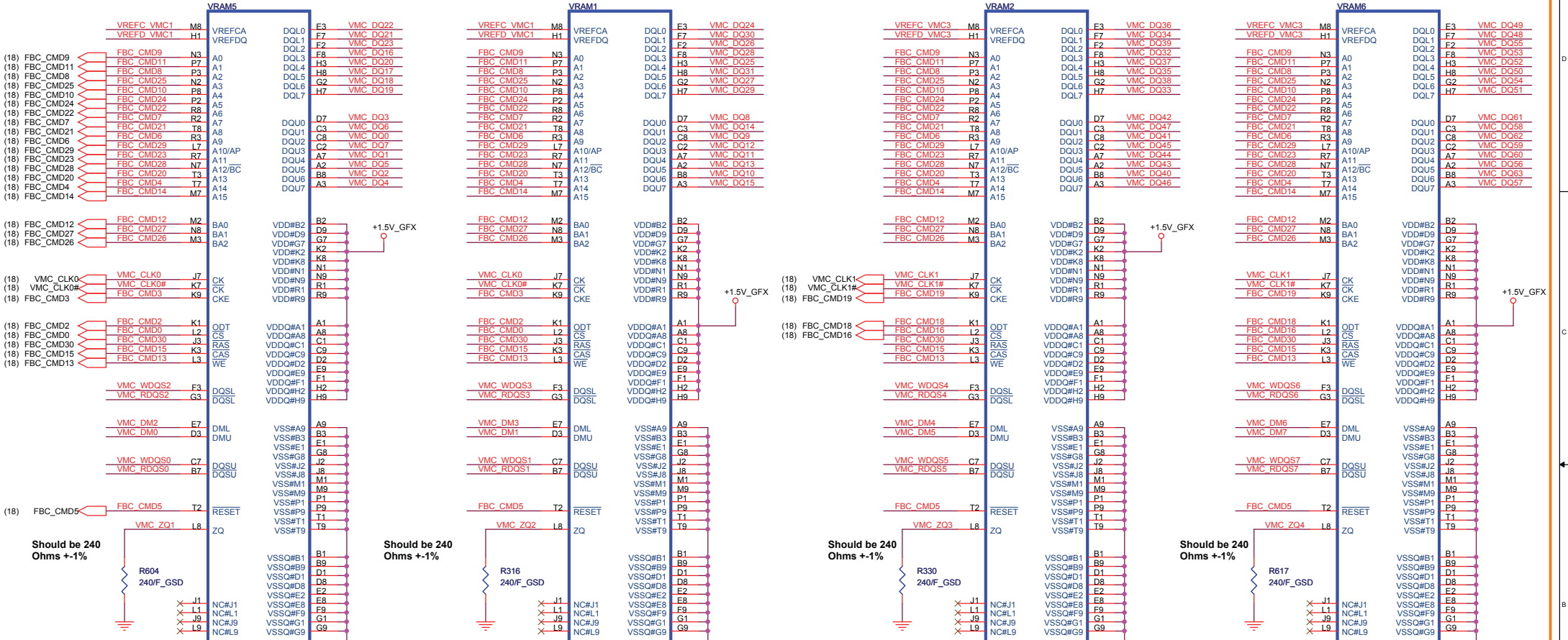
CHANNEL A: 256MB/512MB DDR3



PROJECT : TWH
Quanta Computer Inc.

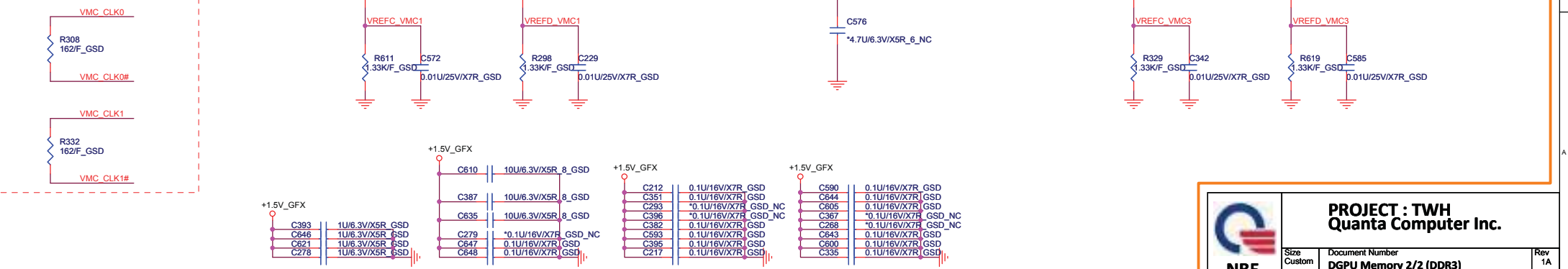
Size Custom	Document Number DGPU Memory 1/2 (DDR3)	Rev 1A
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CHANNEL B: 256MB/512MB DDR3



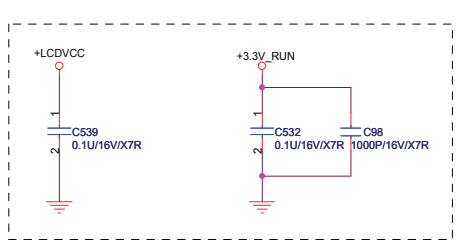
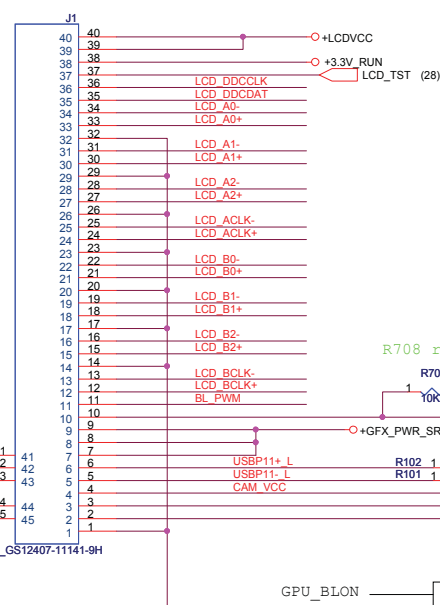
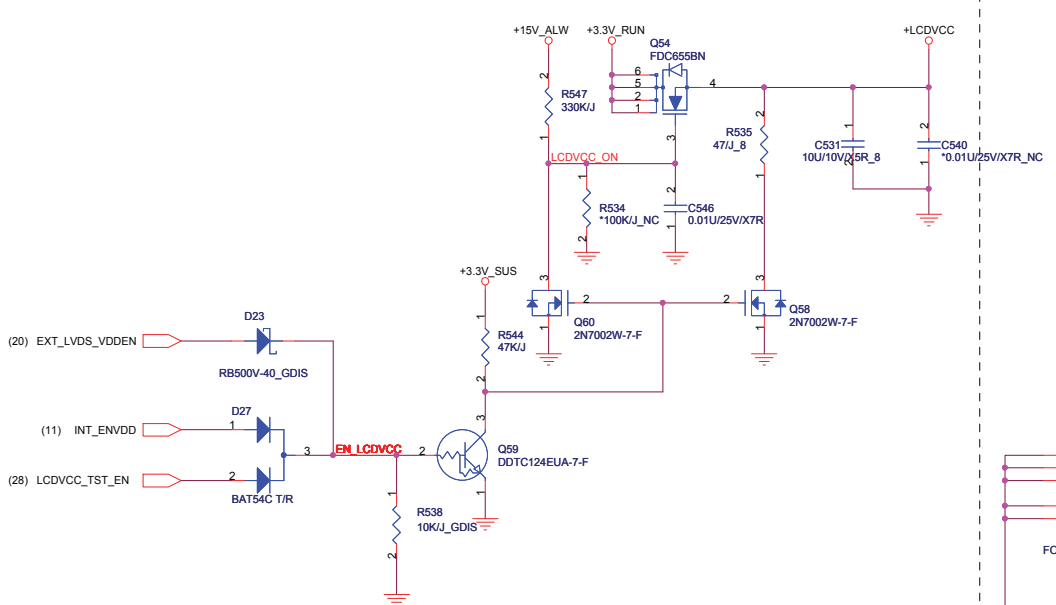
FBC_CLK Termination
 DA-05093-001_V02:Page 96
 R=160/F
 Scott=0710

Placement has to be close to VRAM



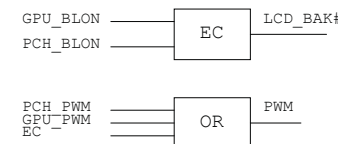
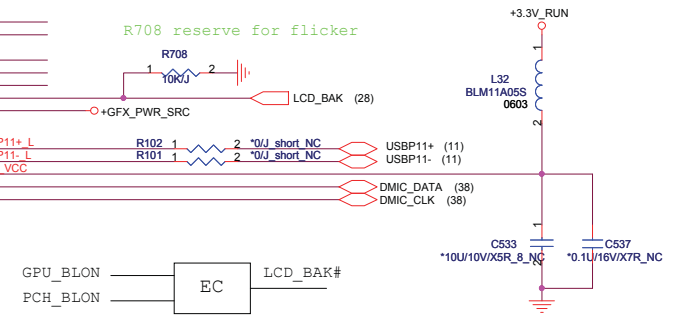
PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	DGPU Memory 2/2 (DDR3)	
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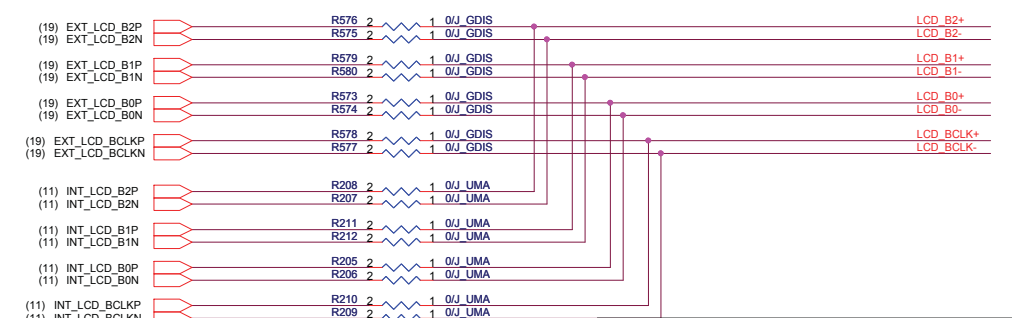
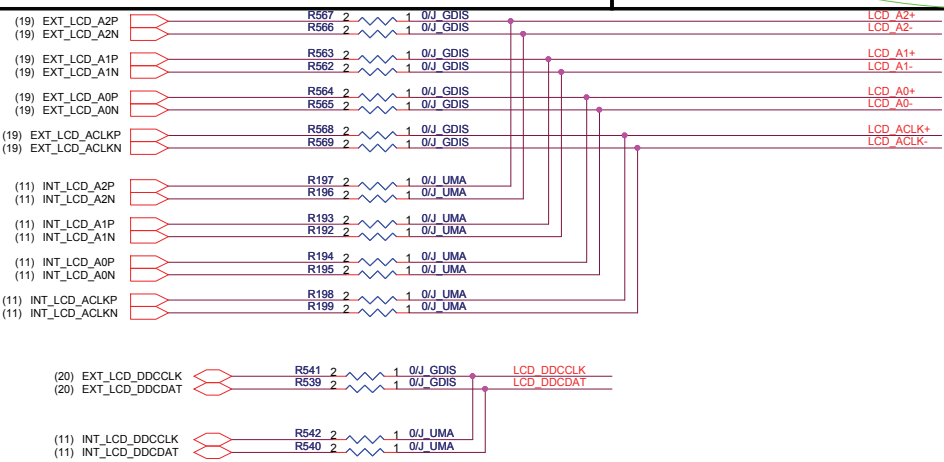
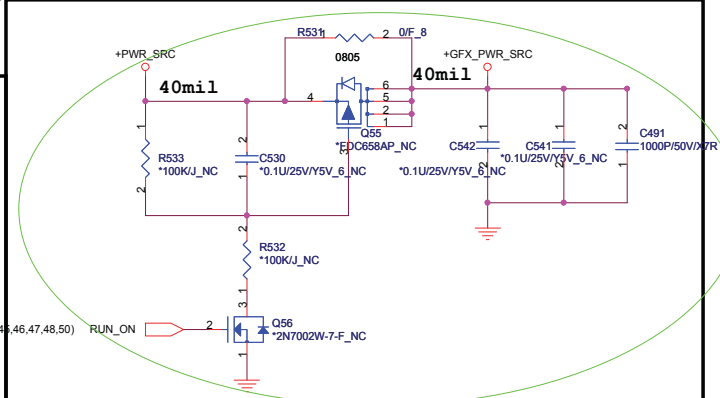
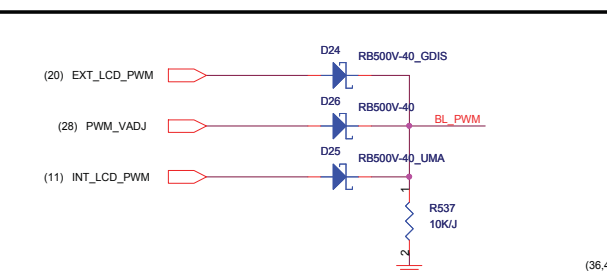
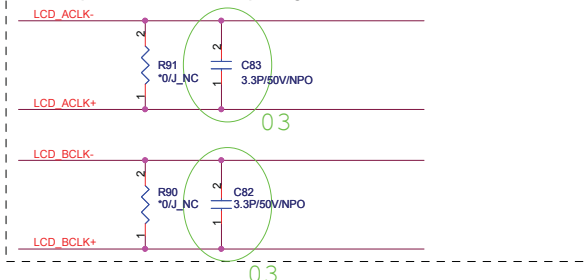


Address : A9H --Contrast
AAH --Backlight

R708 reserve for flicker

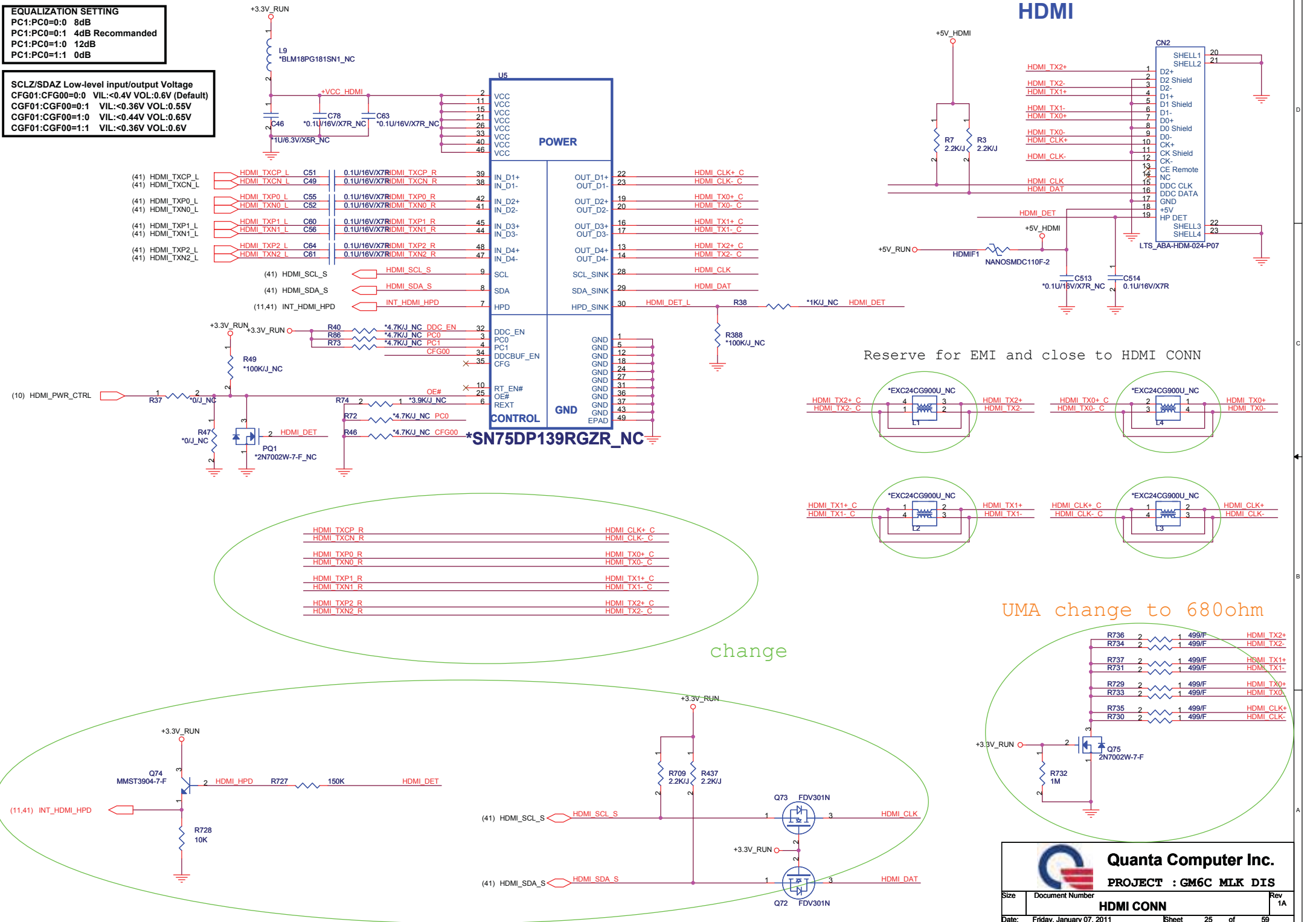


Shunt capacitors on LVDS for improving WWAN.

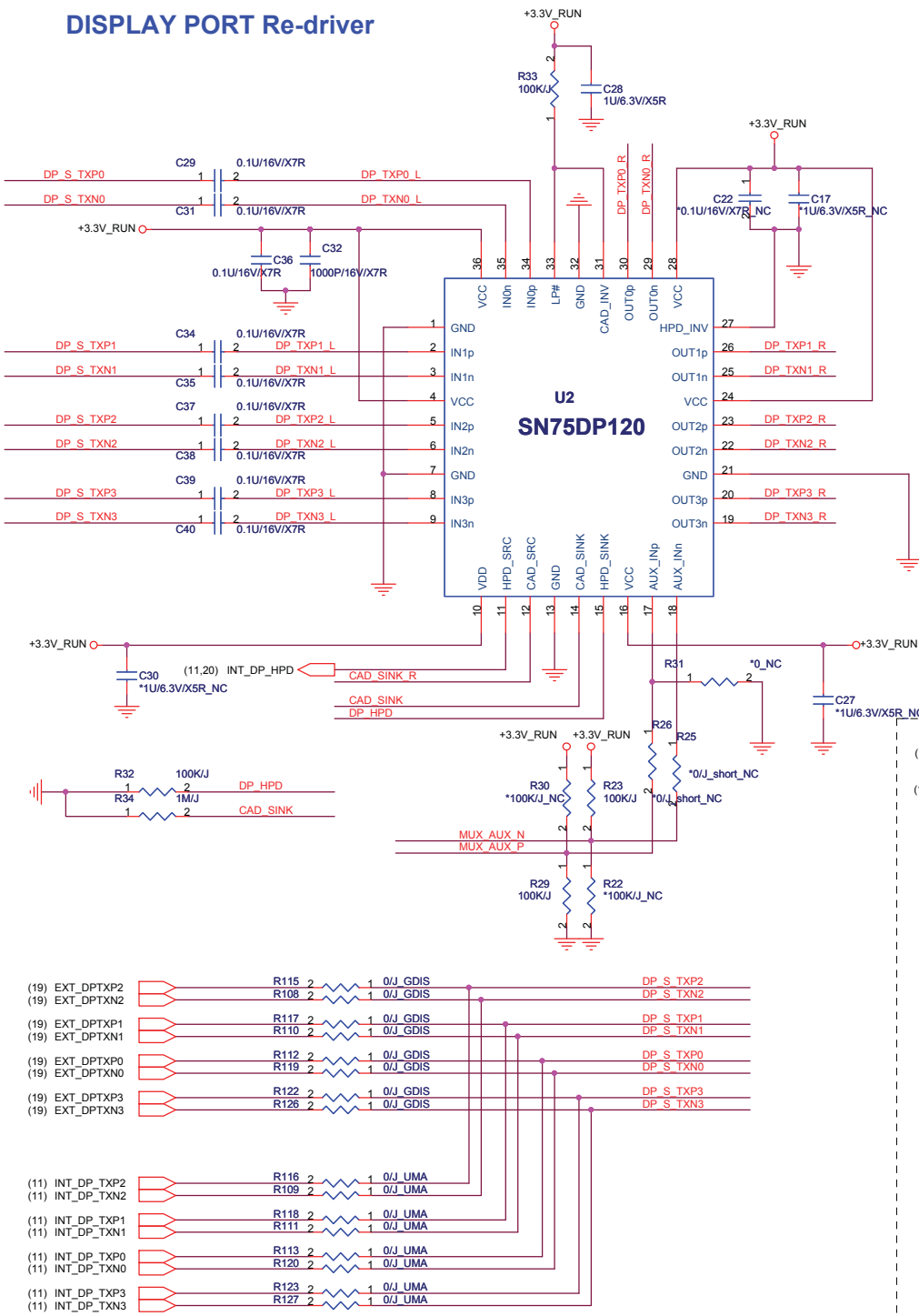


EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

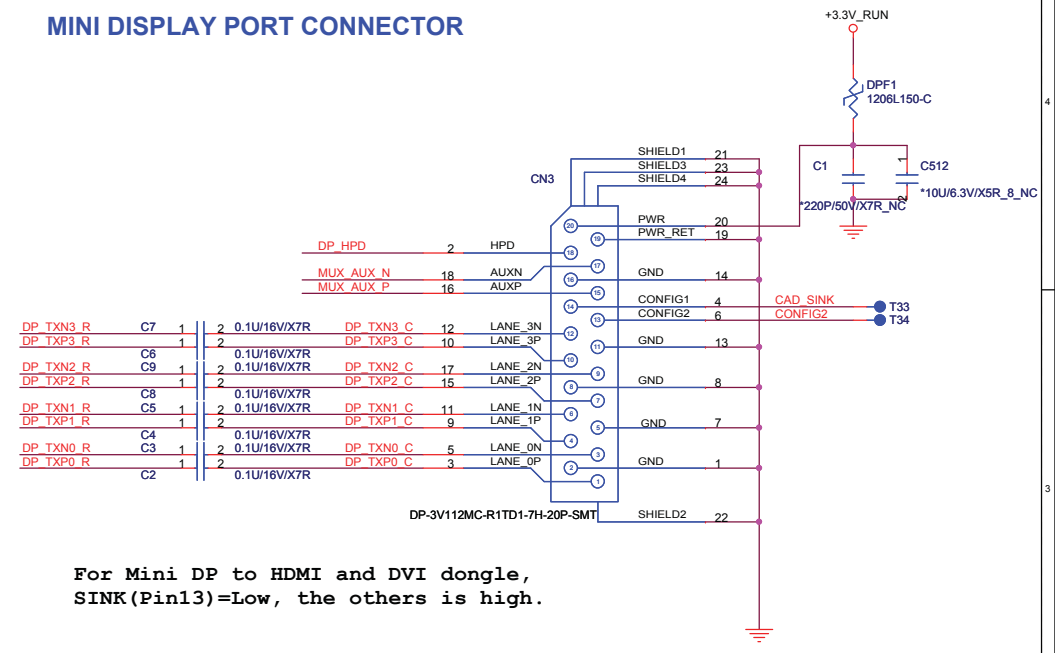
SCLZ/SDAZ Low-level input/output Voltage
 CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
 CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
 CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V



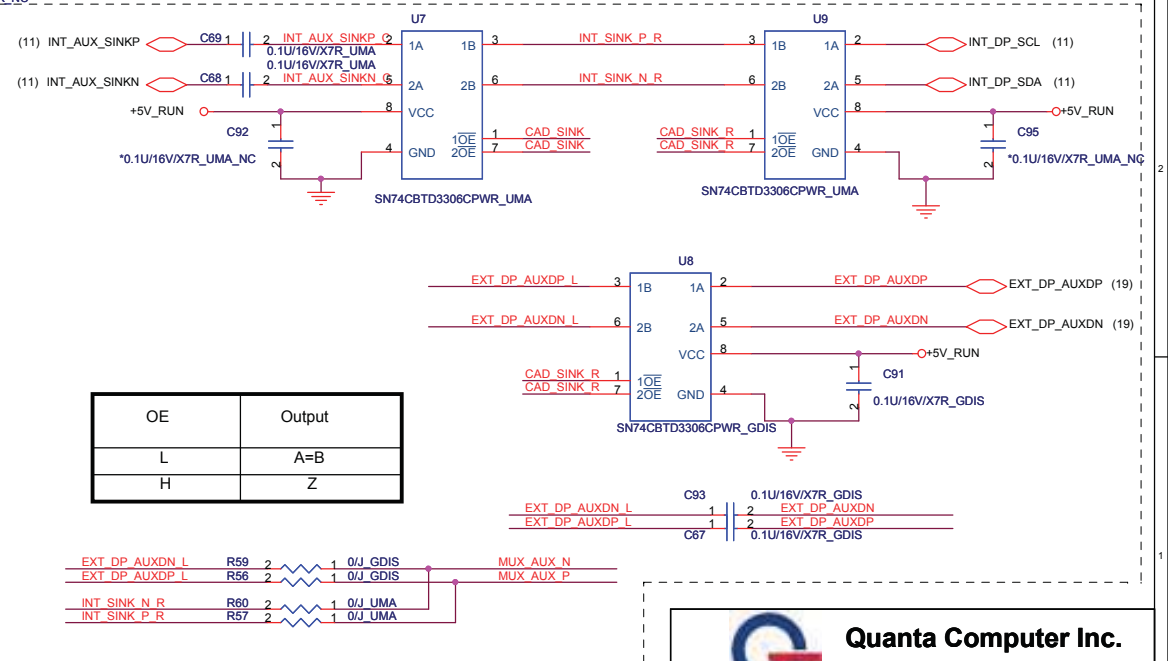
DISPLAY PORT Re-driver

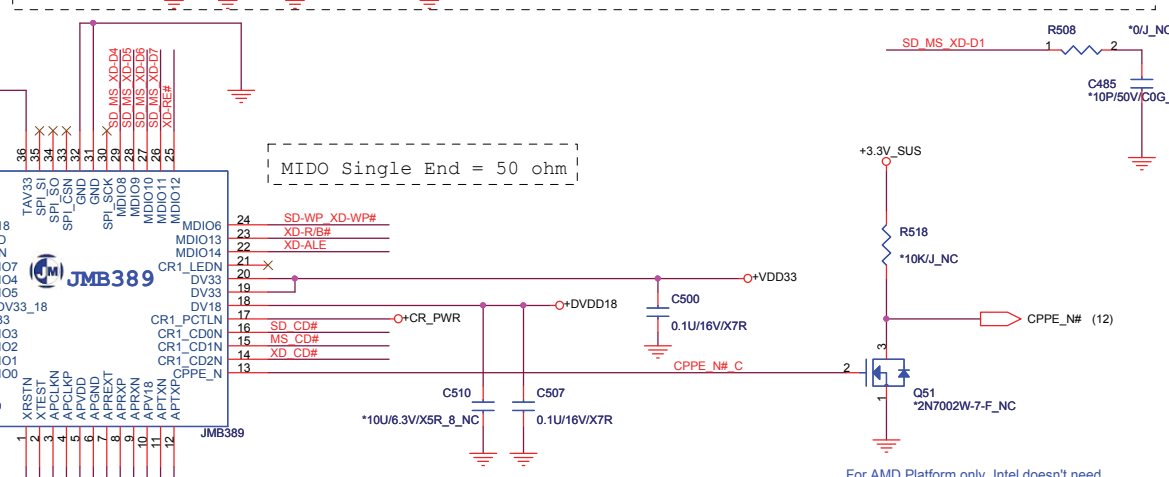
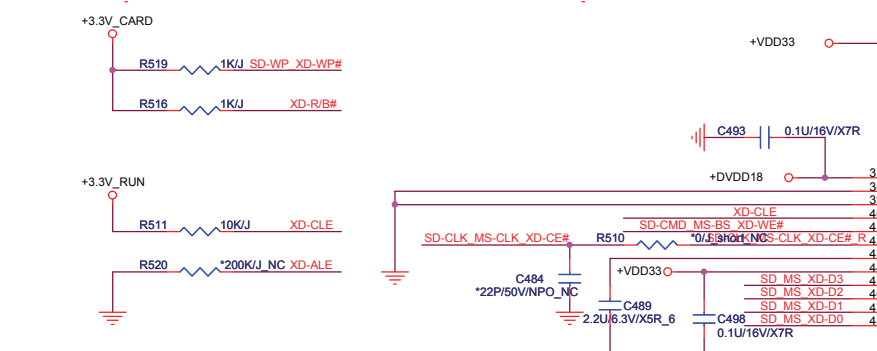
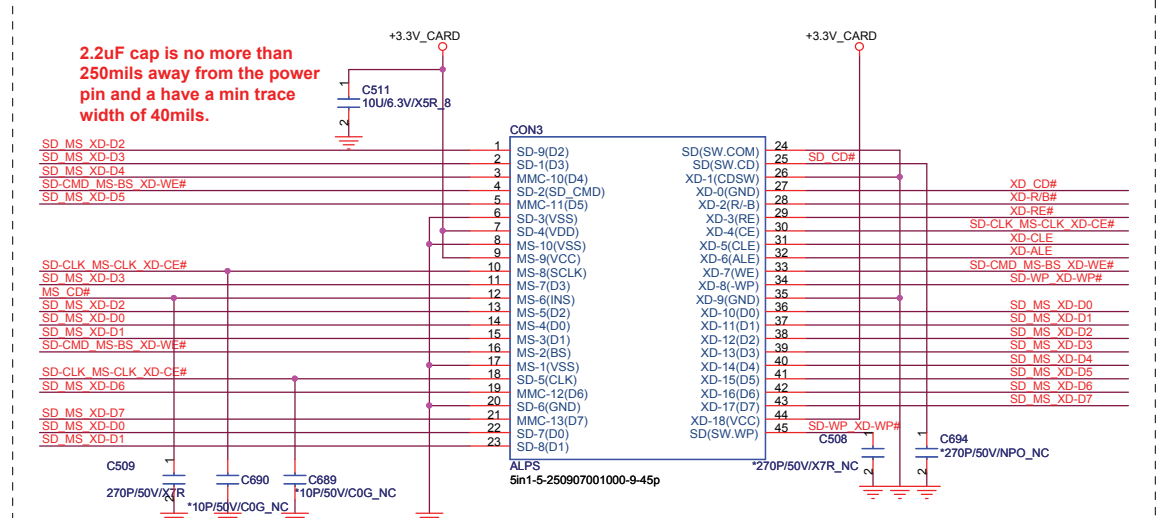
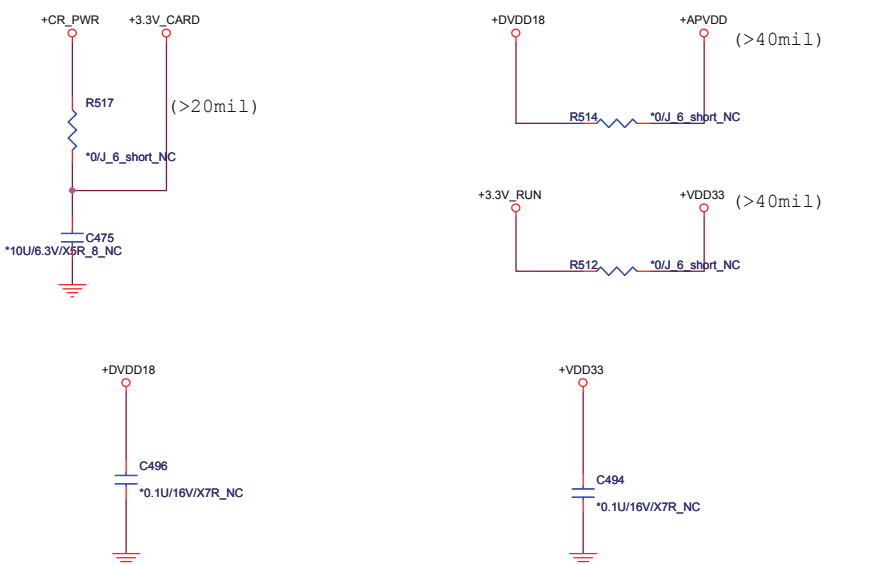


MINI DISPLAY PORT CONNECTOR



For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.



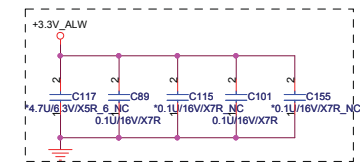


Needs close to Pin17: 12mil/<250mil
 Layout Note:
 Place this cap close to pin 18

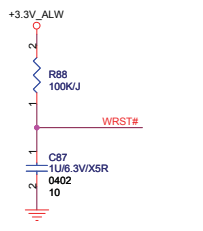
For AMD Platform only, Intel doesn't need to connect to PCH(Vendor)

Card Reader interface signal mapping

Pin	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD D0	MS D0	XD D0
MDIO01		SD D1	MS D1	XD D1
MDIO02		SD D2	MS D2	XD D2
MDIO03		SD D3	MS D3	XD D3
MDIO04		SD CMD	MS BS	XD WE#
MDIO05		SD CLK	MS CLR	XD CE#
MDIO06		SD WP		XD WP#
MDIO07				XD CLE
MDIO08		MMC D4	MS D4	XD D4
MDIO09		MMC D5	MS D5	XD D5
MDIO10		MMC D6	MS D6	XD D6
MDIO11		MMC D7	MS D7	XD D7
MDIO12				XD RE#
MDIO13				XD R/B#
MDIO14				XD ALE
CR1 LEDN		SD LED#	MS LED#	XD LED#
CR1 PCTLN		SD PWR#	MS PWR#	XD PWR#
CR1 CD0		SD CD#	MS CD#	XD CD#
CR1 CD1				
CR1 CD2				

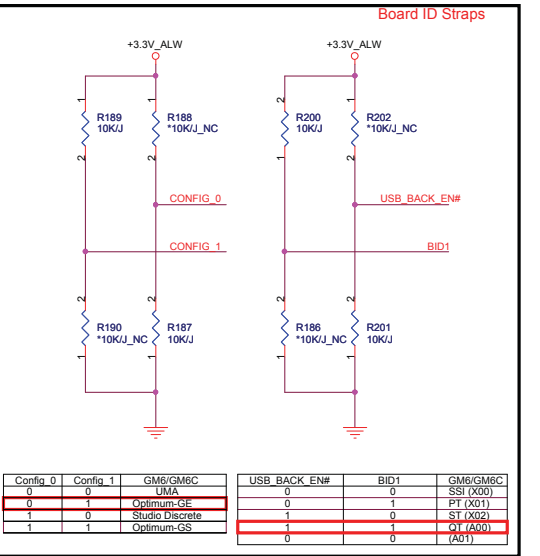
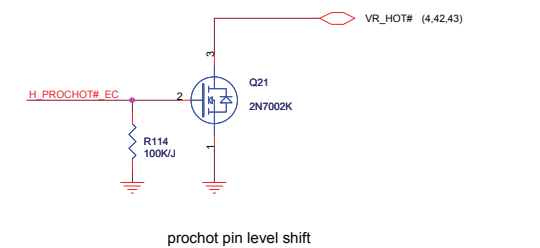
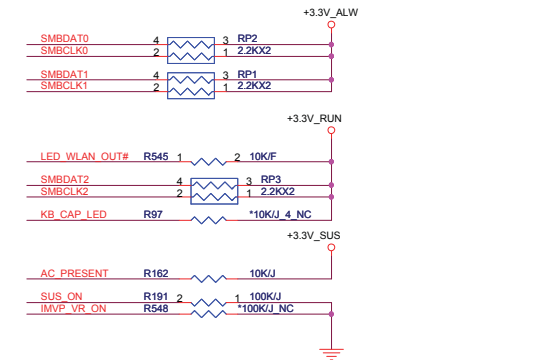
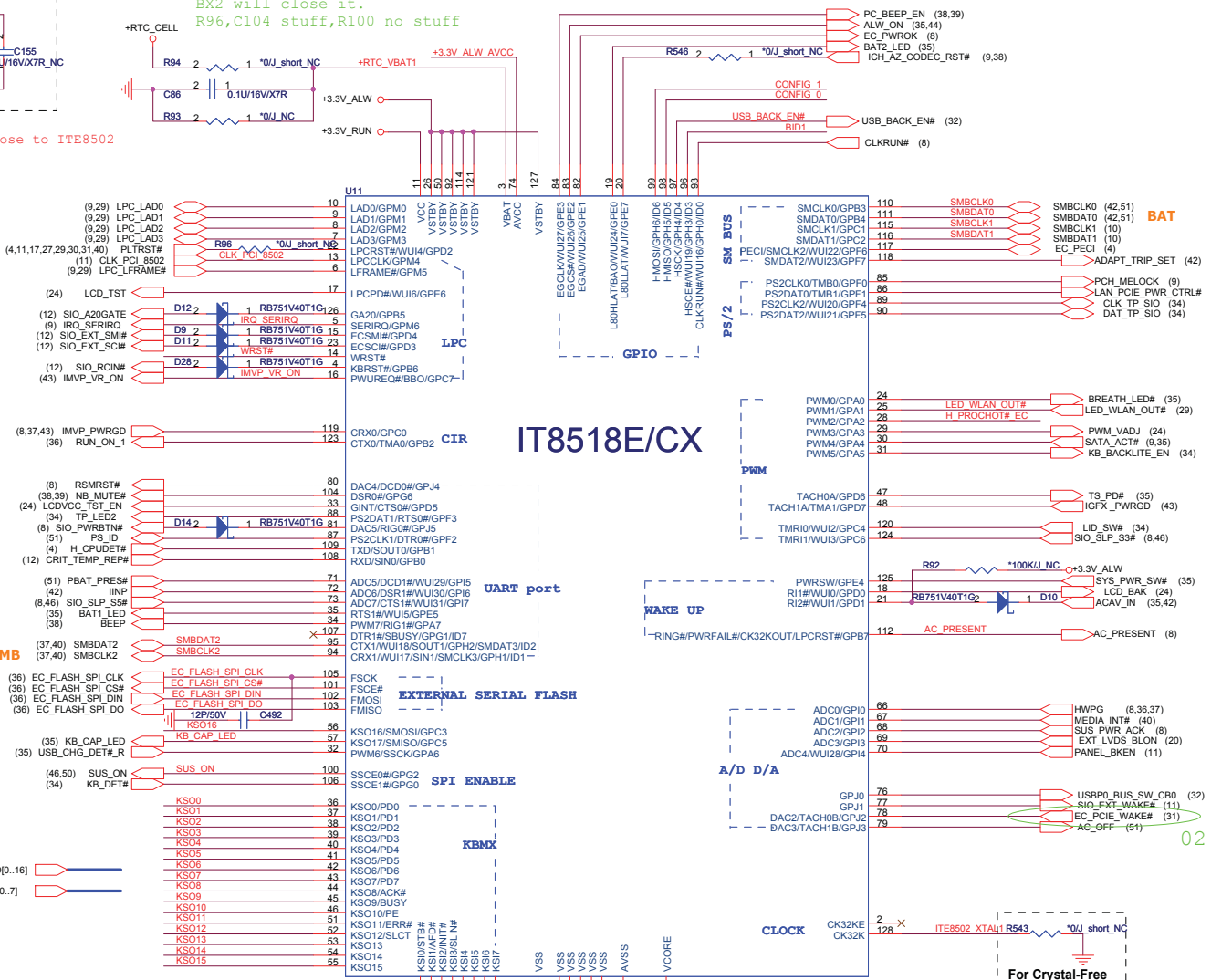


Layout Note: Place these caps close to ITE8502



Layout Note: Place PC169 close to ITE8502

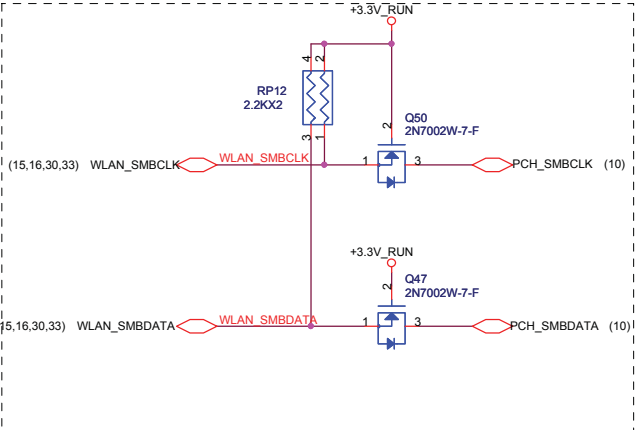
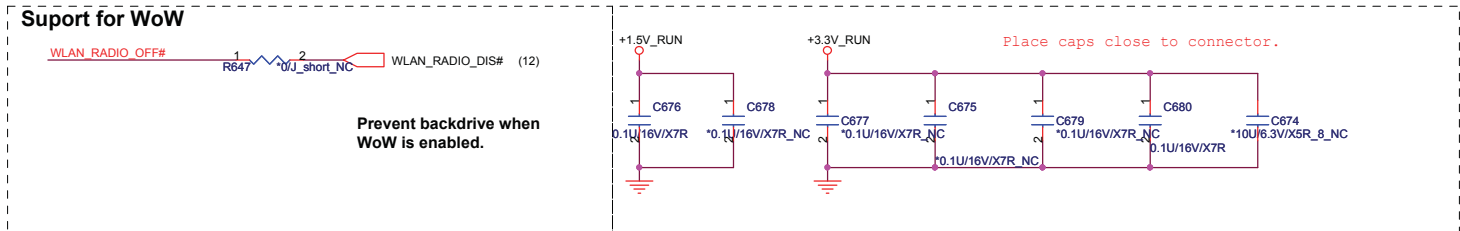
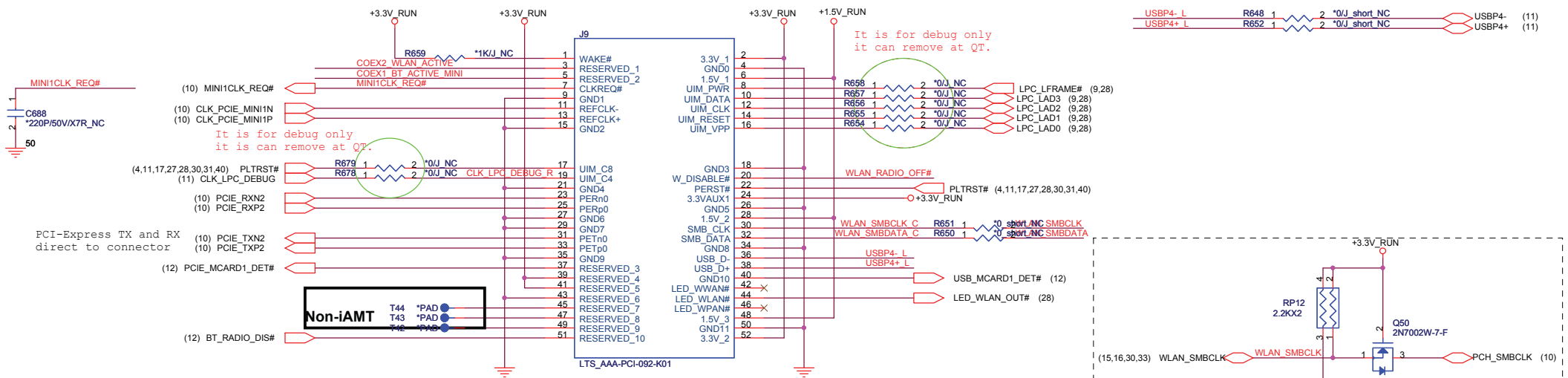
BX1 leakage issue workaround circuit
 R96, C104 no stuff, R100 stuff
 BX2 will close it.
 R96, C104 stuff, R100 no stuff



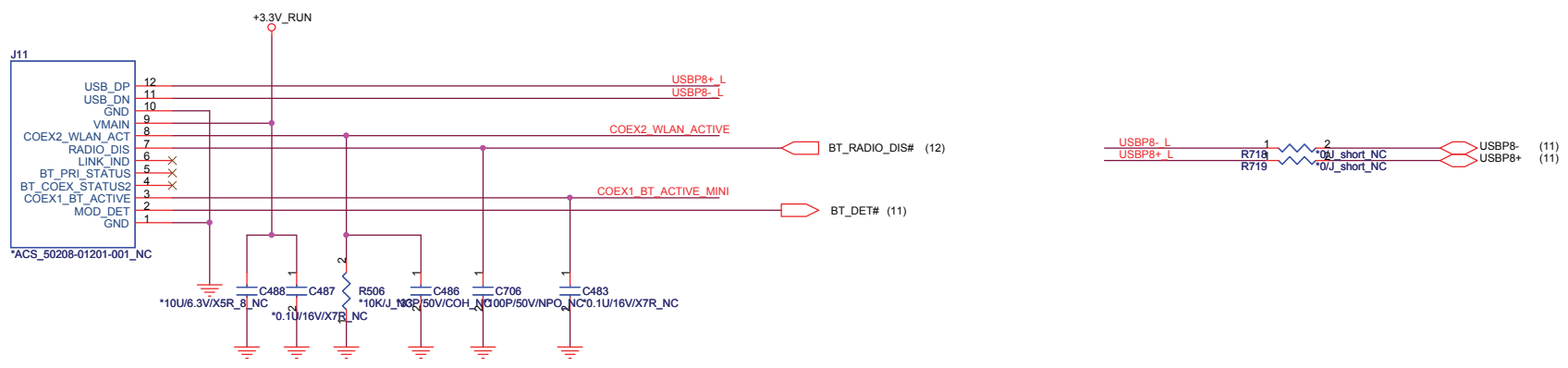
Config_0	Config_1	GM6/GM6C	USB_BACK_EN#	BID1	GM6/GM6C
0	0	UMA	0	0	SSI (X00)
0	0	Optimum-GS	0	1	PT (X01)
1	0	Studio-Discrete	1	0	ST (X02)
1	1	Optimum-GS	1	1	QT (A00)
0	0		0	0	(A01)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
SIO (ITE8518)
 Date: Friday, January 07, 2011 Sheet 28 of 59

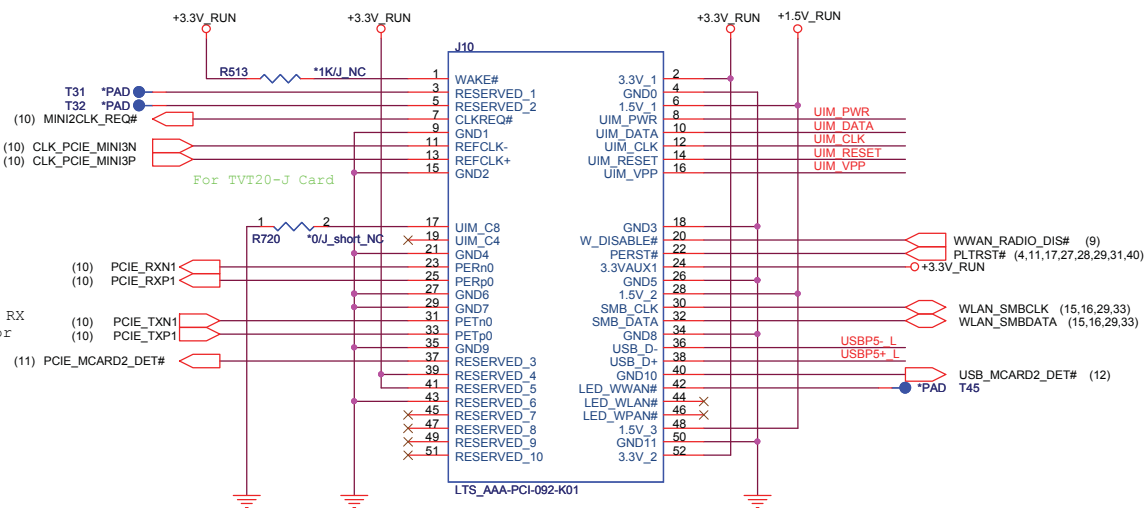
MiniCard WLAN connector



Support Dell BT375 (Little Stone) module (XPS) W TO B

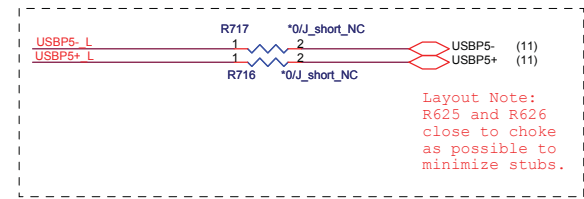


MiniCard WWAN connector

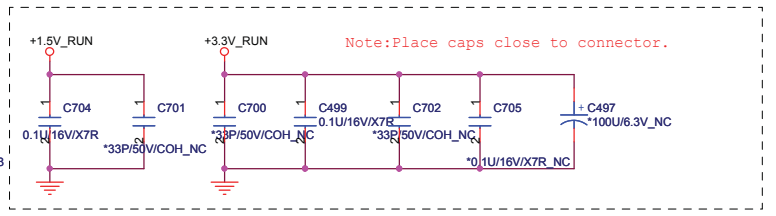
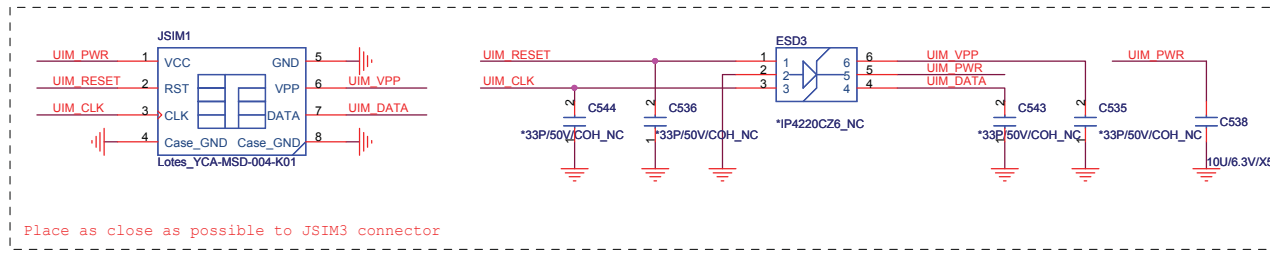


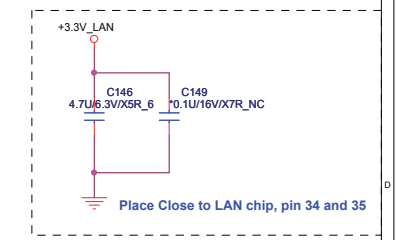
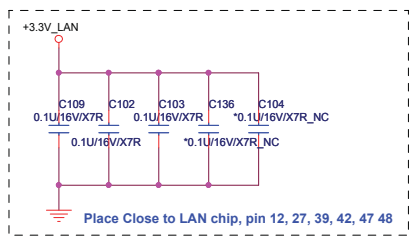
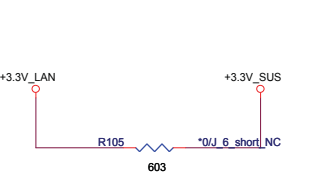
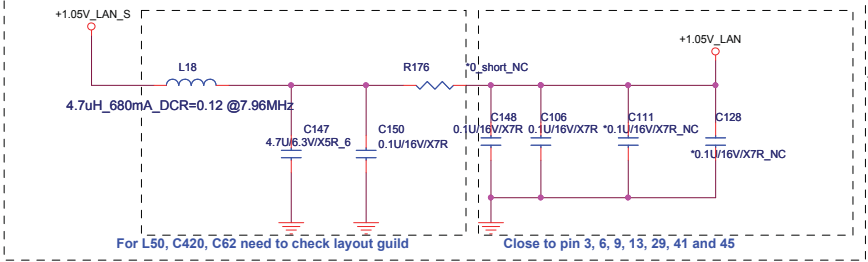
PCI-Express TX and RX direct to connector

For TVT20-J Card

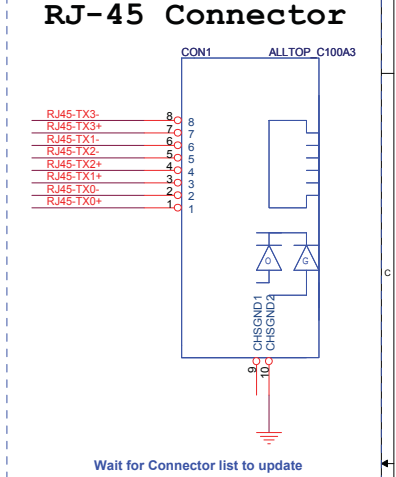
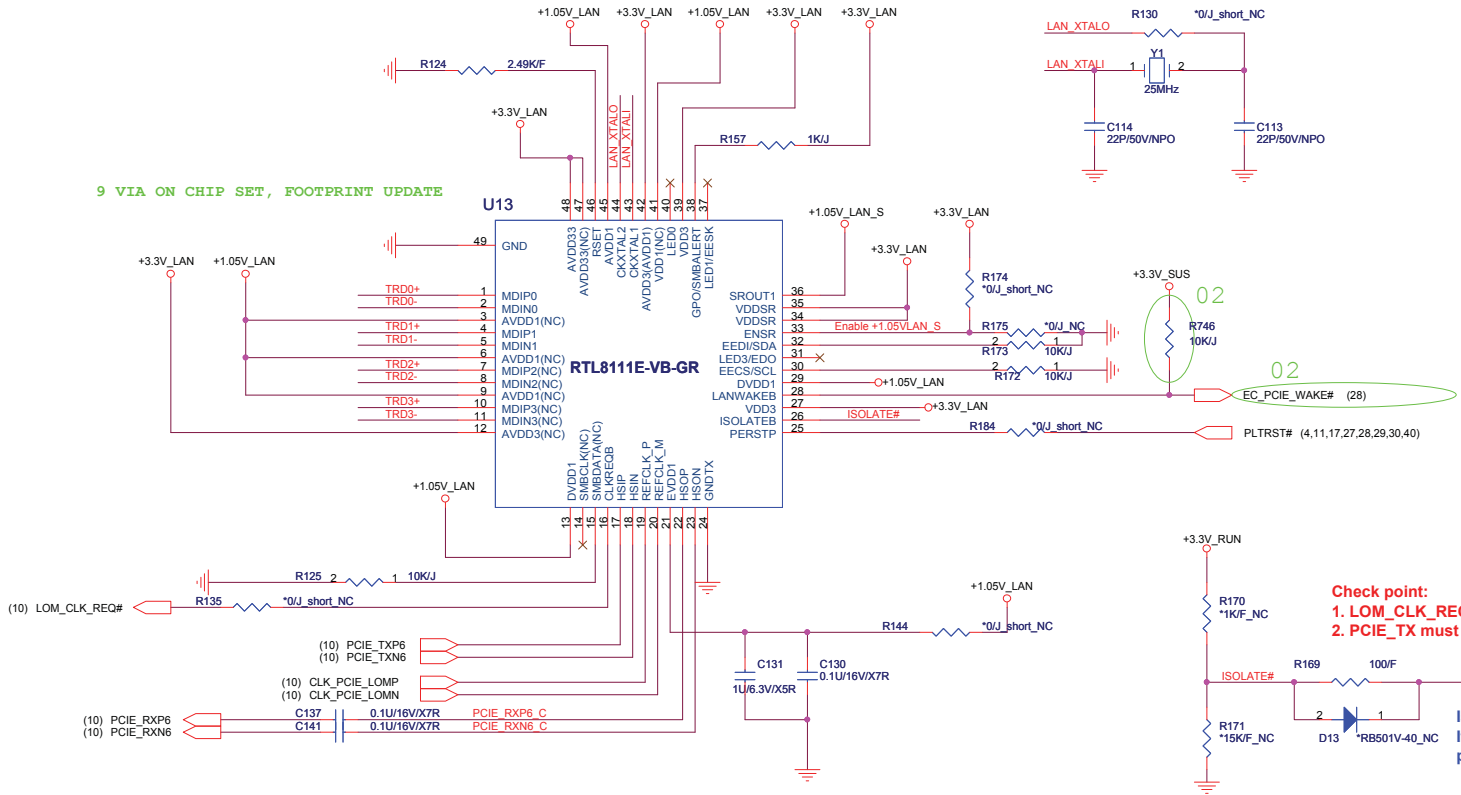


Layout Note:
R625 and R626 close to choke as possible to minimize stubs.





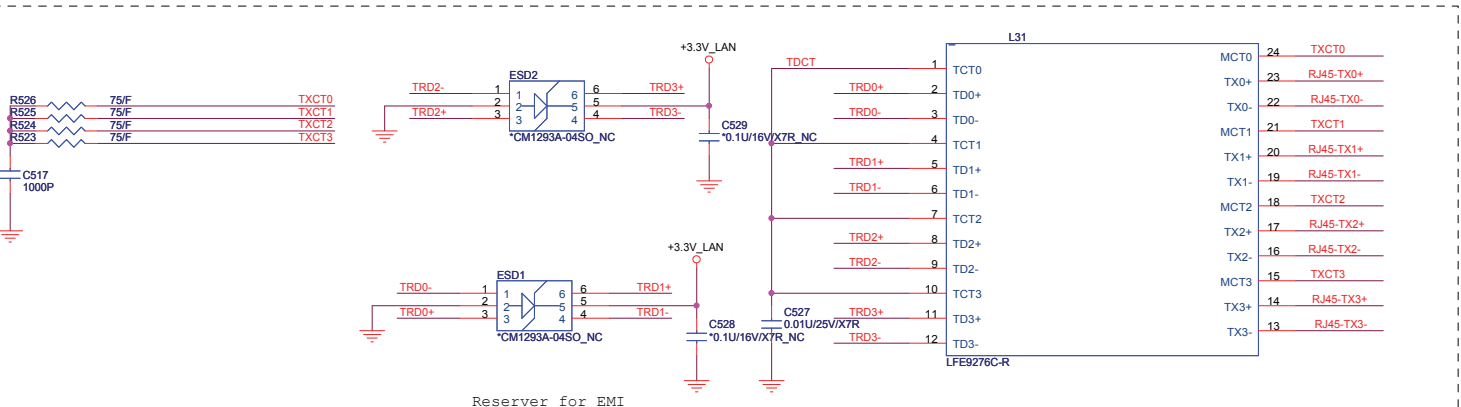
9 VIA ON CHIP SET, FOOTPRINT UPDATE



Wait for Connector list to update

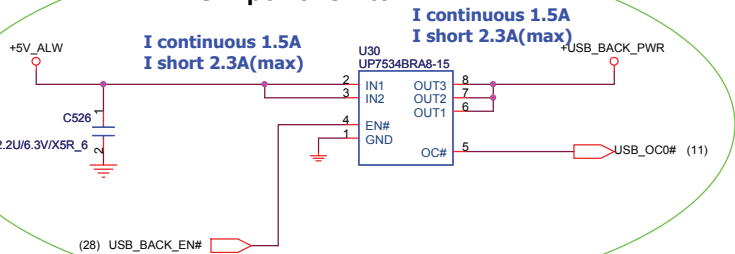
Check point:
 1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
 2. PCIE_TX must have AC cap at PCH side

Isolate# is for power saving.
 It needs to pull low when system state in S3, S4, and S5.
 pull high when system at S0 state

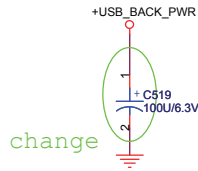


ESATA + USB Conn + Power Share

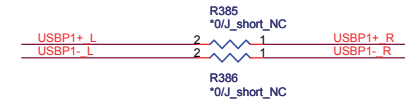
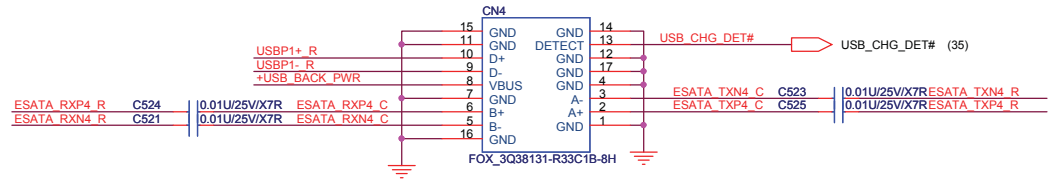
UPI power switch



USB_BACK_EN# needs to be low when system S3 and S5 for USB charge

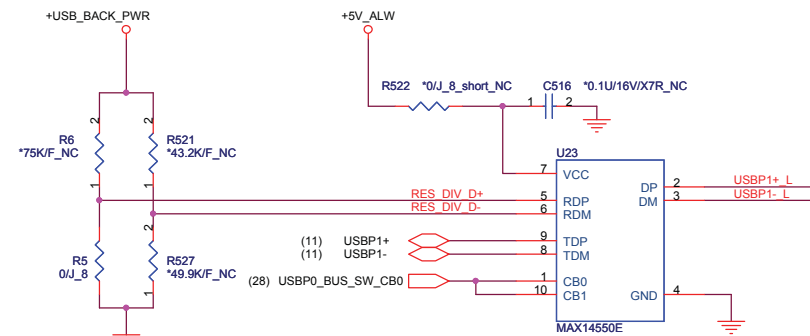
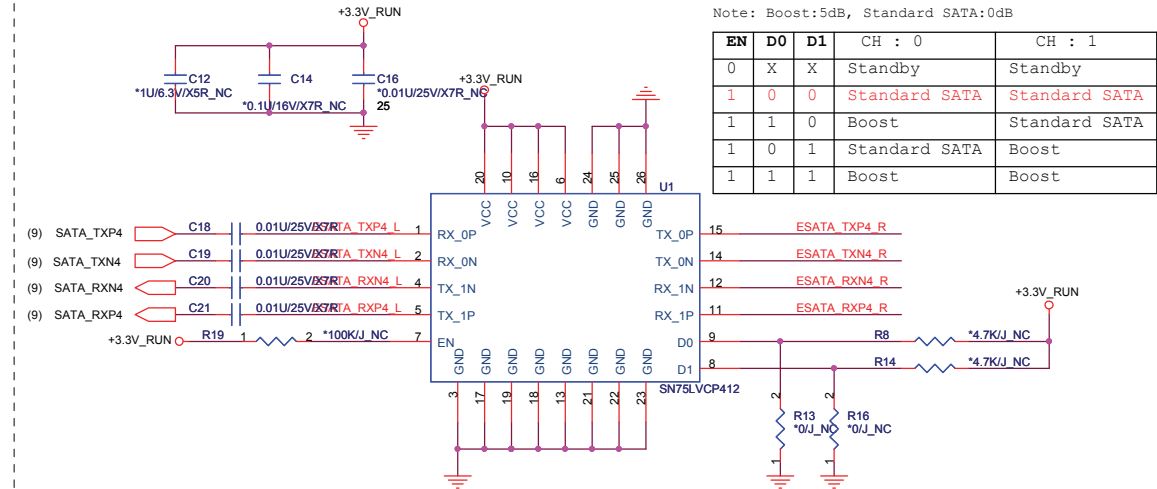


This pin connects to 3VALW ON POWER LOGIC



E-SATA Re-driver

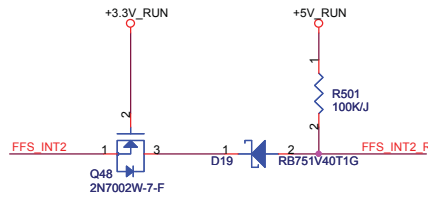
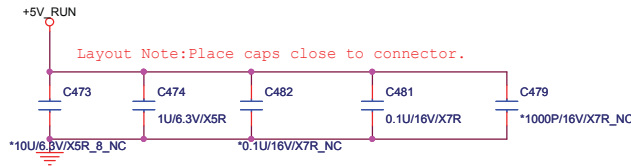
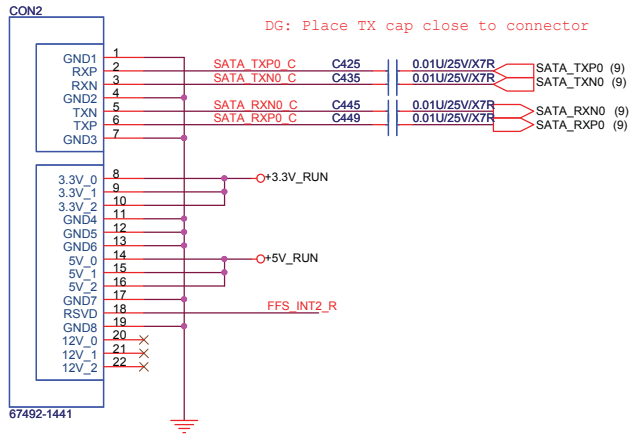
Layout Note: Please put those on the same side of MB PCB



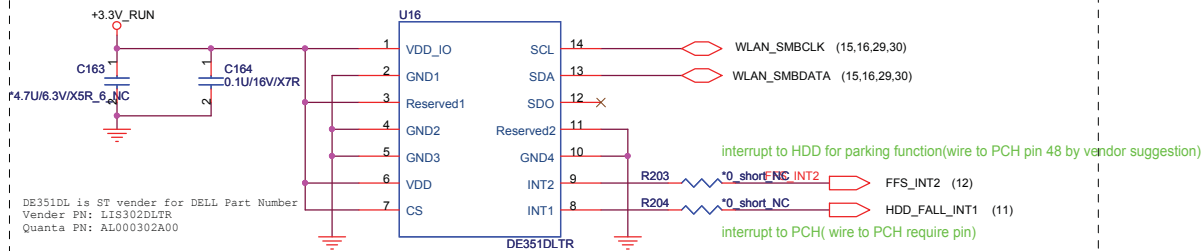
EC needs to drive CB0/CB1 pins to low when system S3/S5 and drive high when system S0.
 U49 PN and Footprint needs to double check
 R15 needs to be 49.9K_F if we use external resistors.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)		
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)		

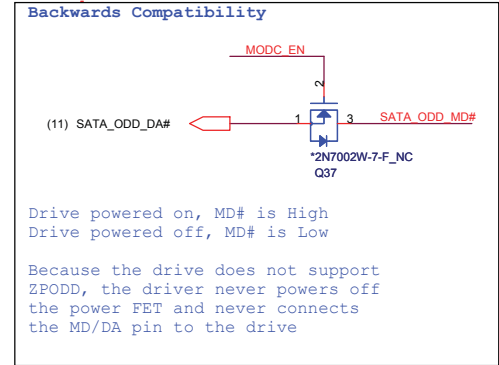
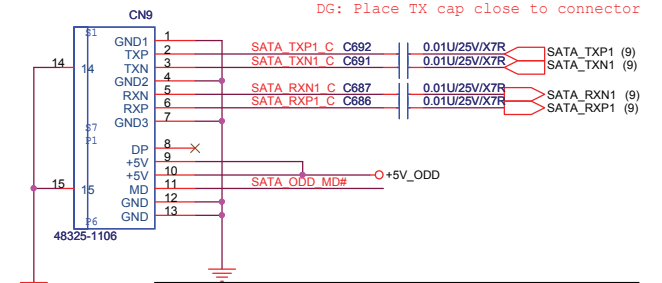
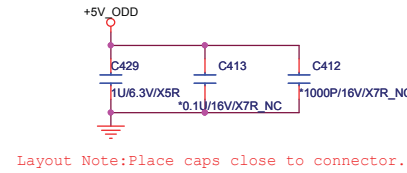
SATA Connector.



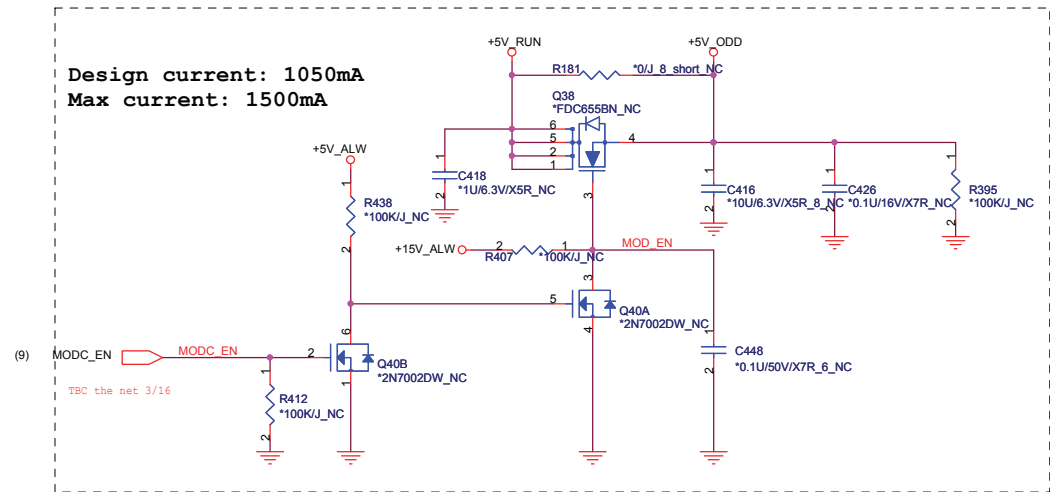
3-axis Fall Sensor (HDD data protector)



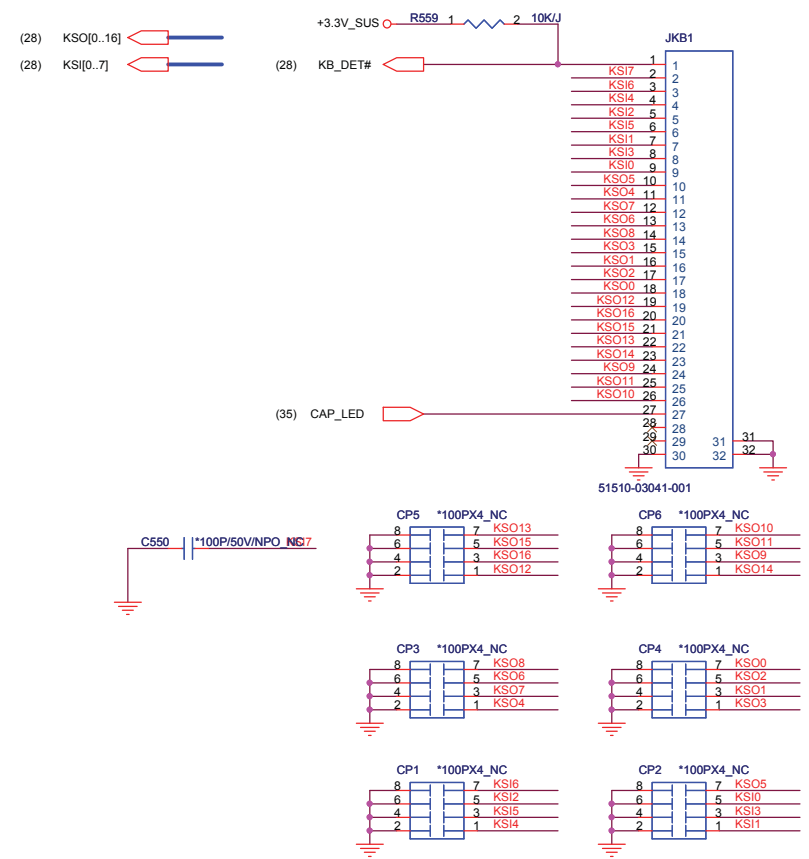
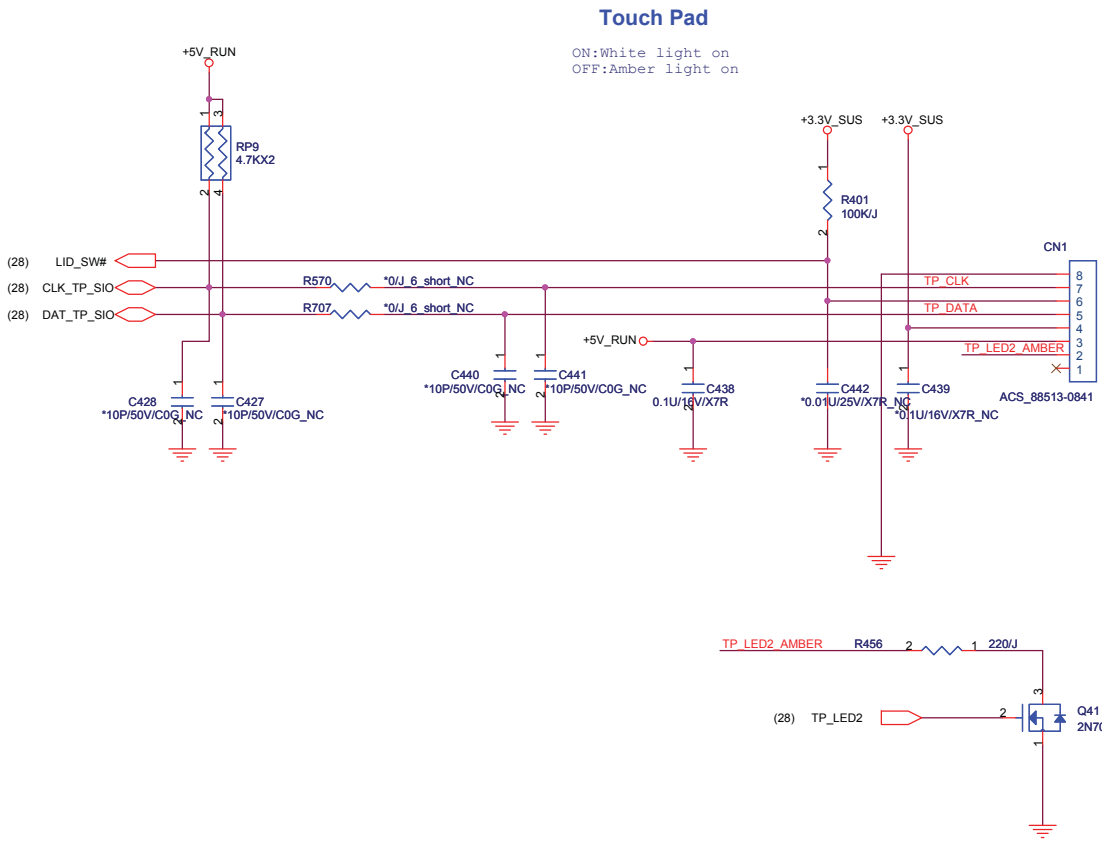
ODD Connector



Design current: 1050mA
Max current: 1500mA

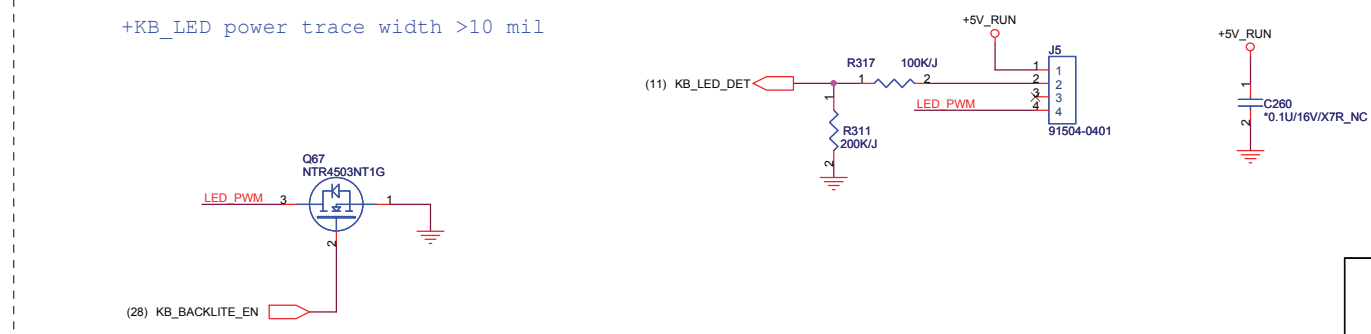


KEYBOARD CONNECTOR

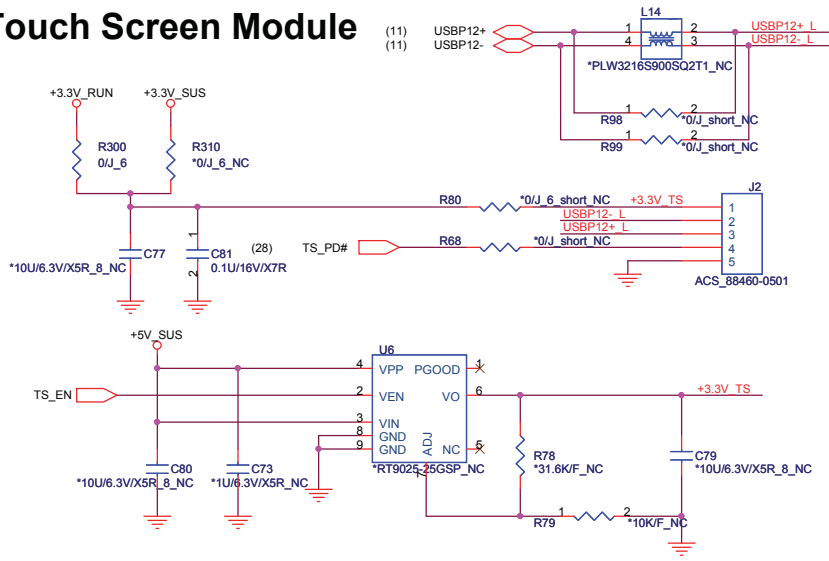


Layout Note: 100P CAPS CLOSE TO JKB3

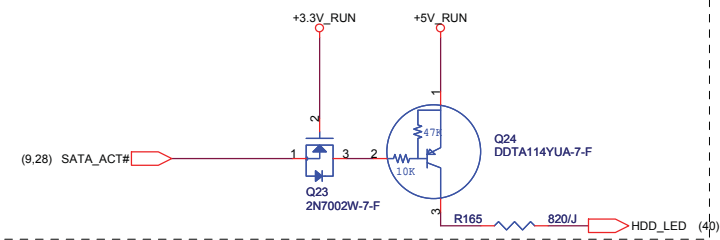
Key board illumination



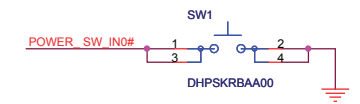
Touch Screen Module



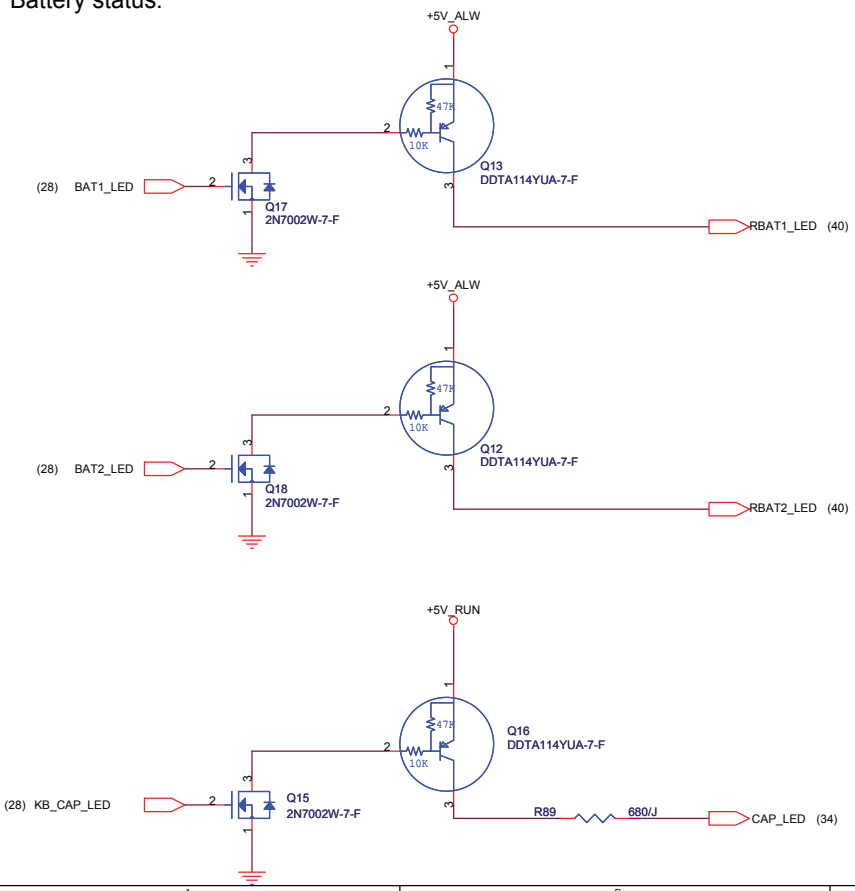
HDD activity LED.



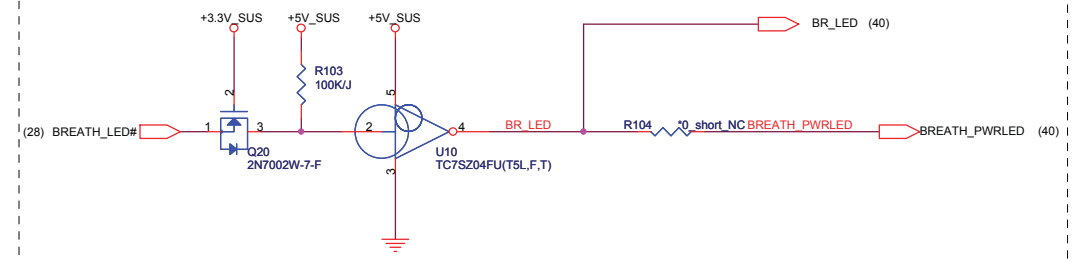
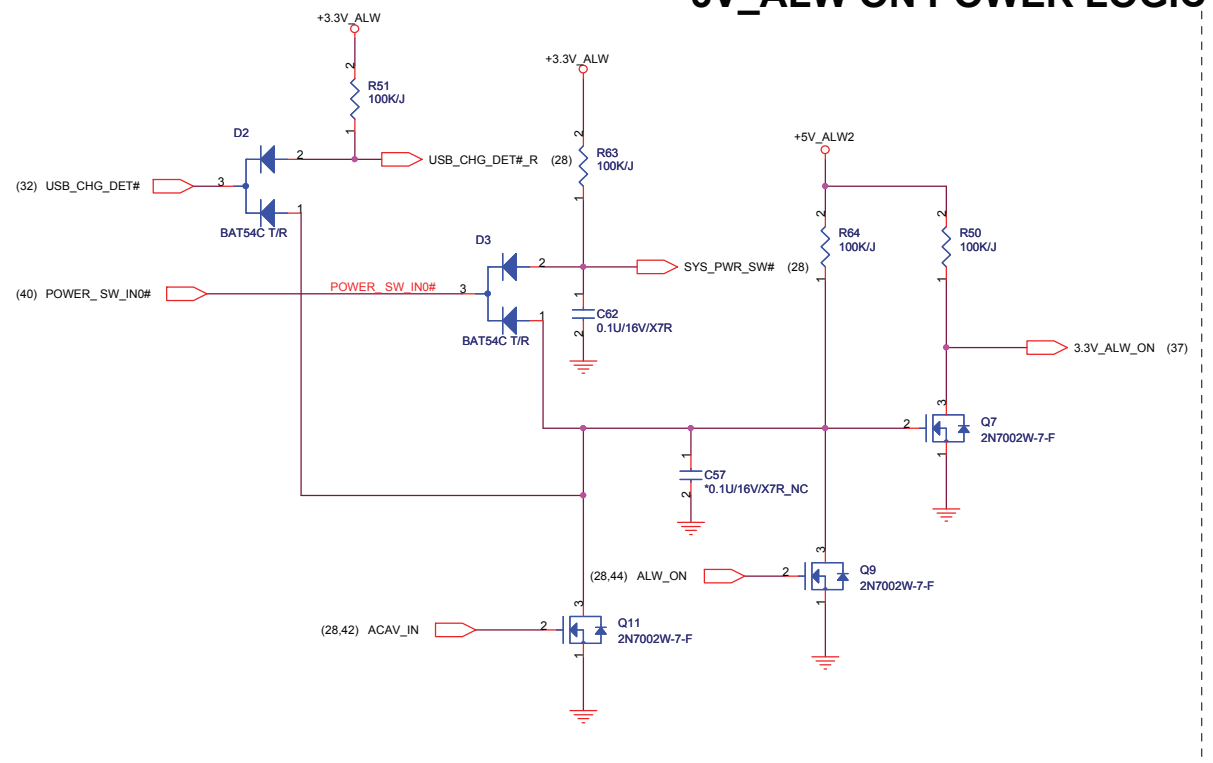
Power button for Engineer



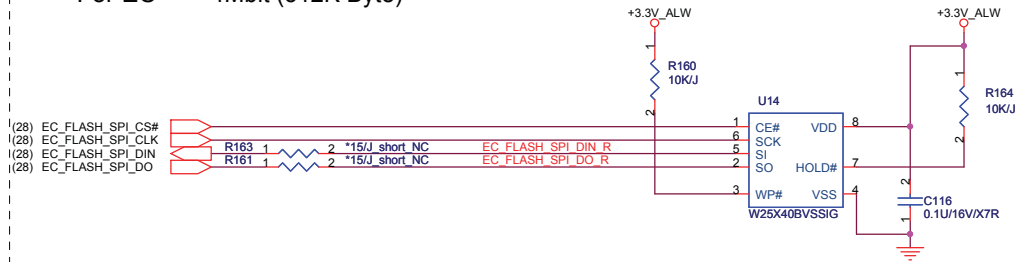
Battery status.



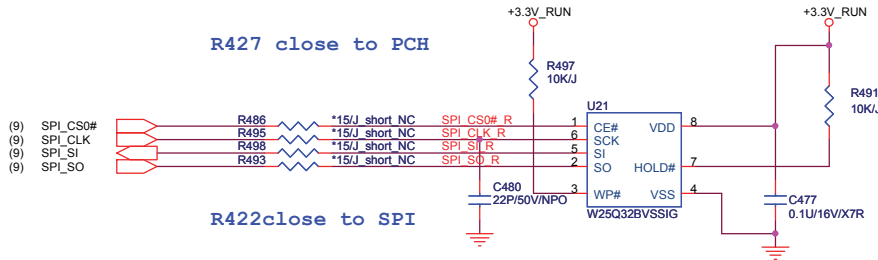
3V_ALW ON POWER LOGIC



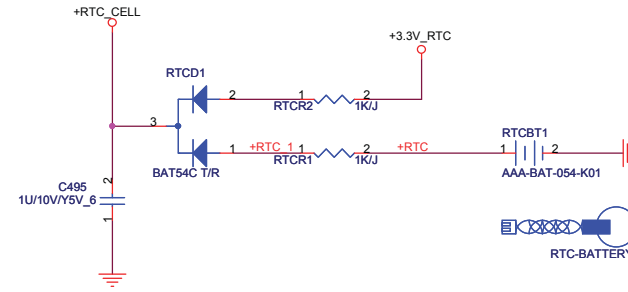
For EC 4Mbit (512K Byte)



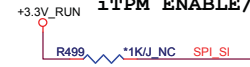
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE

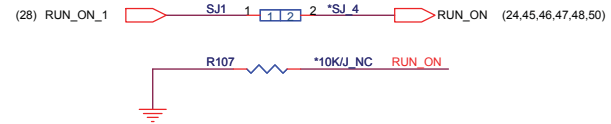
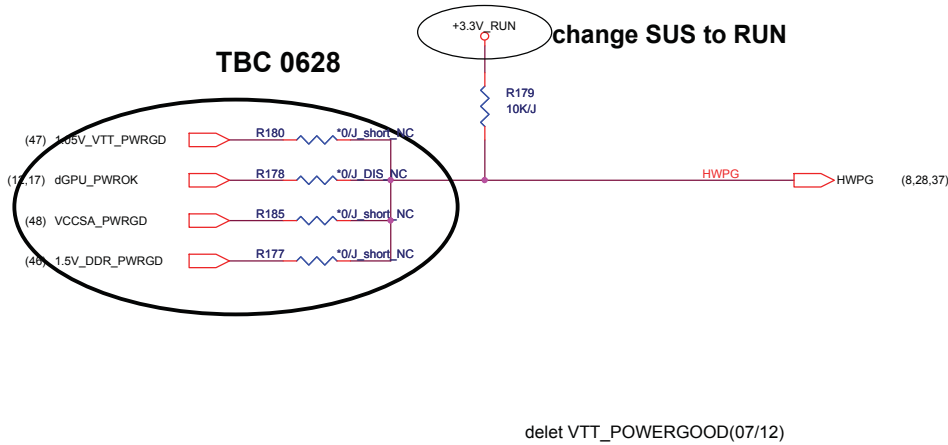


TPM Function	R428
Enable	Mount
Disable	NC (Default)

RESET CIRCUIT

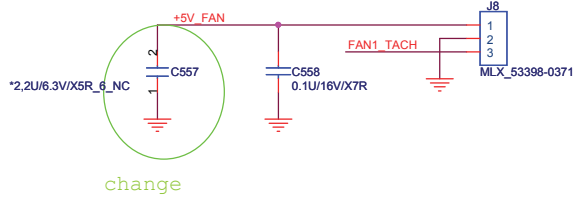
TBC 0628

change SUS to RUN

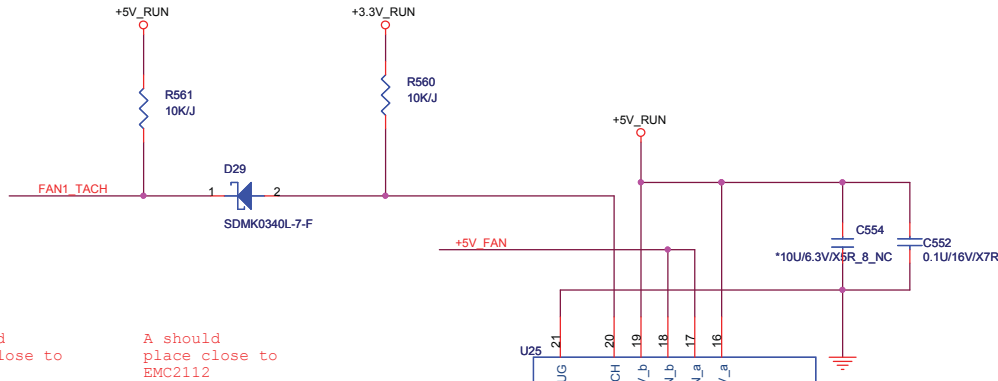


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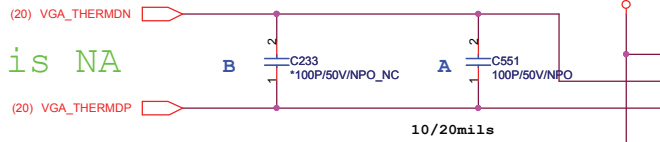
PROJECT : GM6C MLK DIS



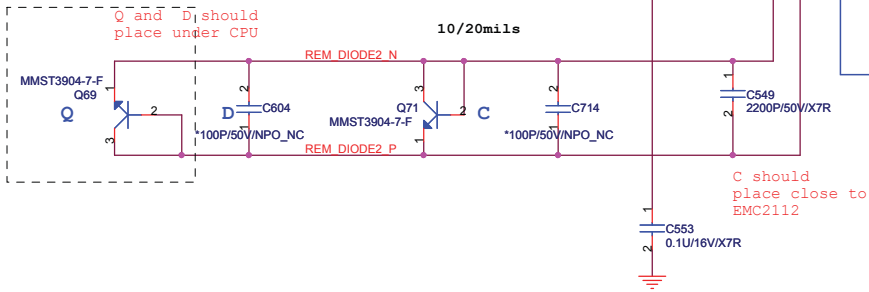
change



B should place close to GFX
A should place close to EMC2112

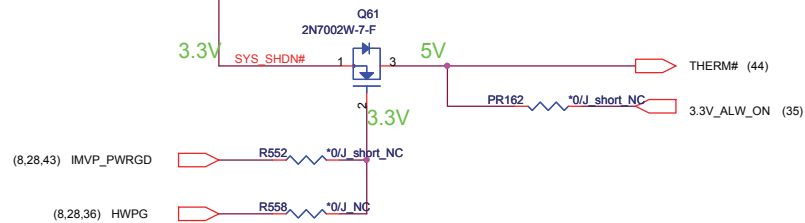


for UMA is NA



Q and D1 should place under CPU

C should place close to EMC2112

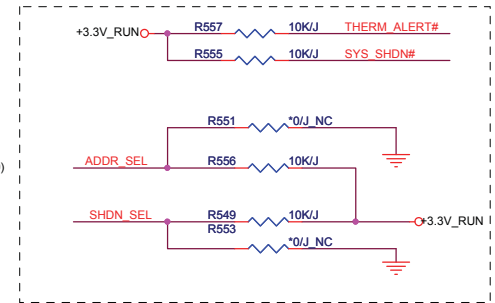


reserve HWPG only HW control (07/12)

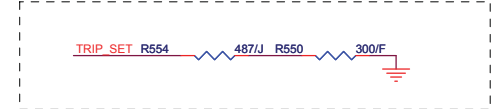
Need to check with BIOS

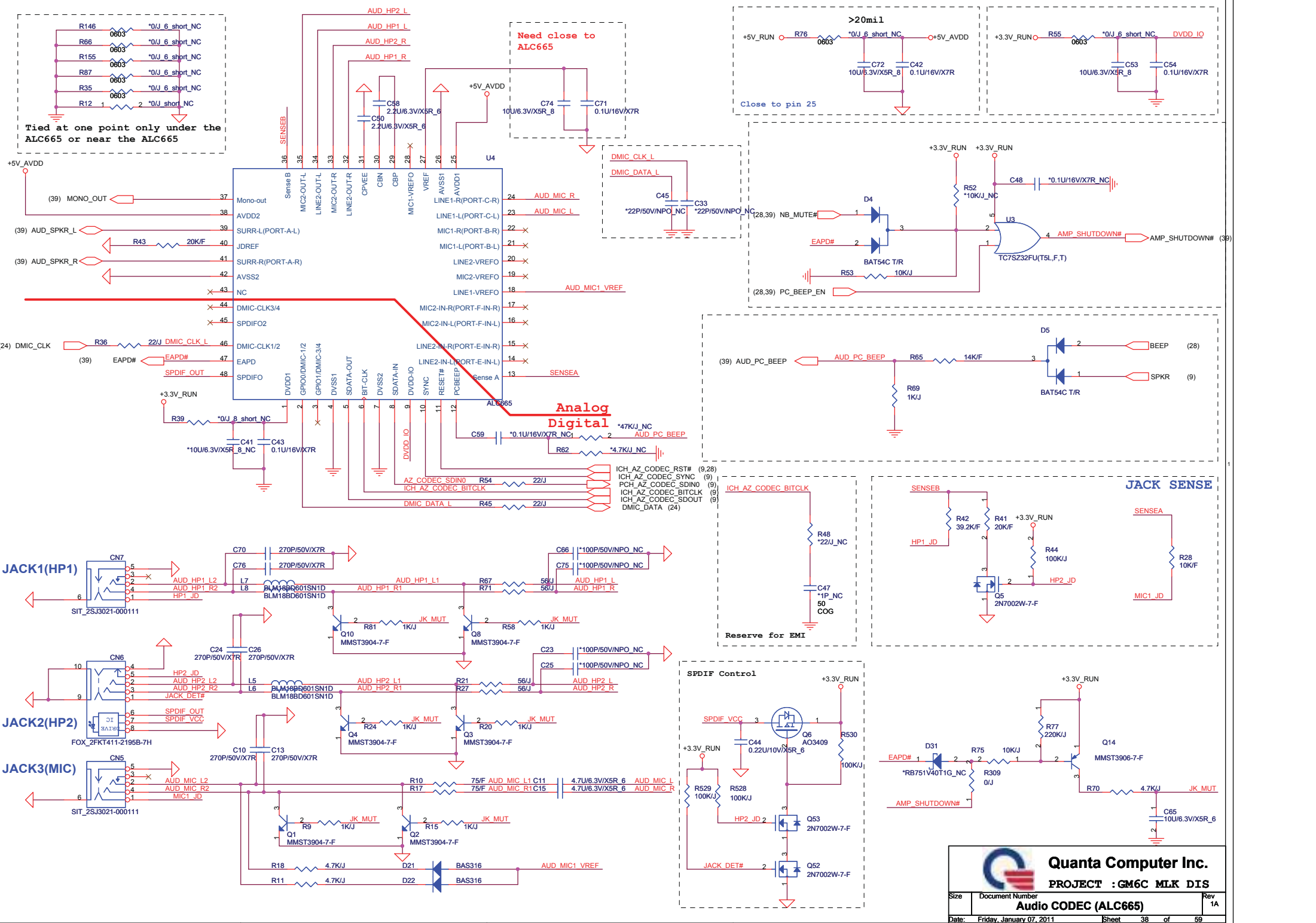
ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb

SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND: Intel Transistor Mode

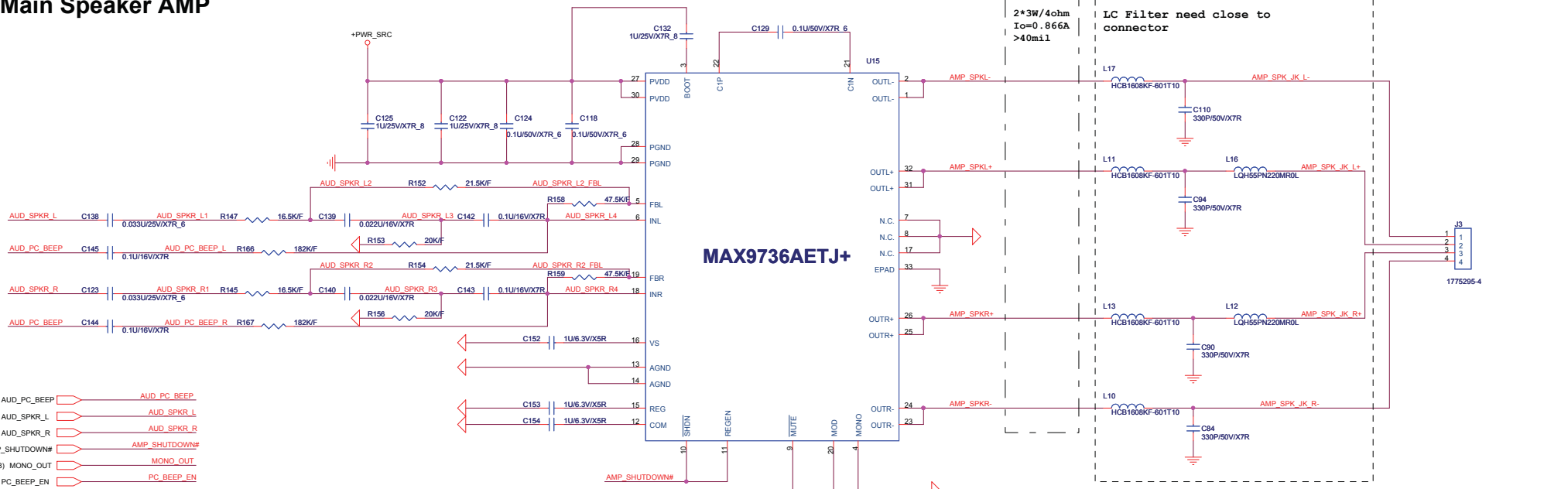


OTP 85 degree C

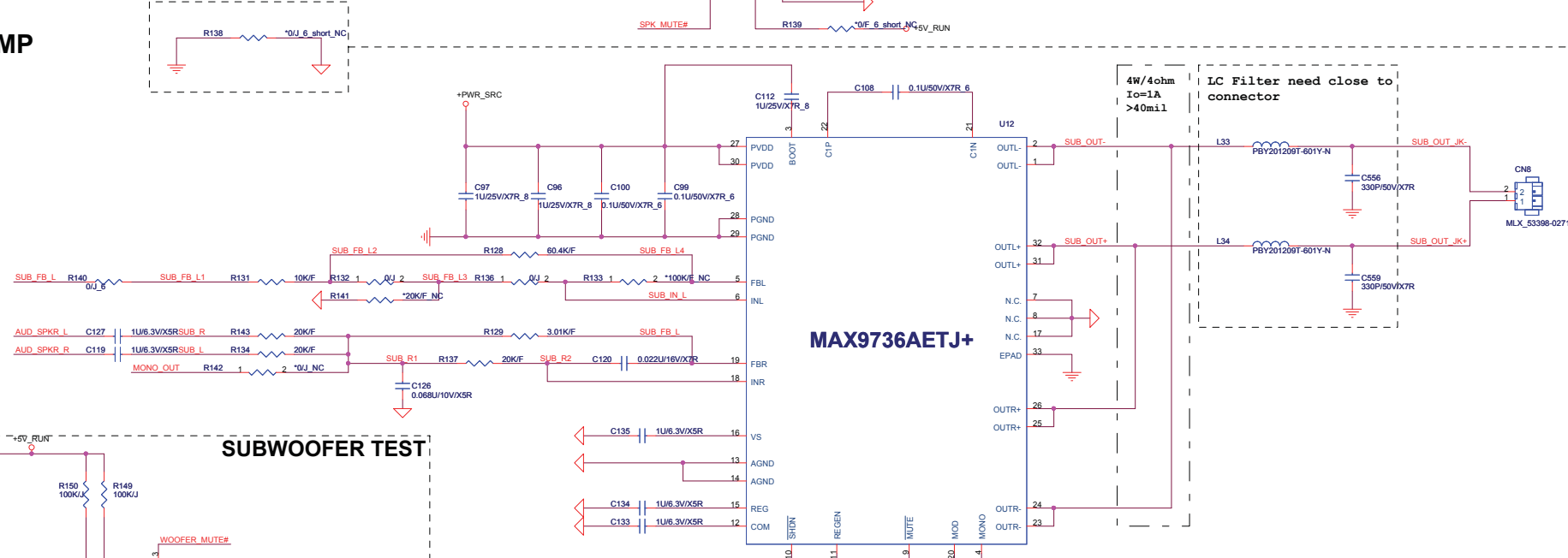




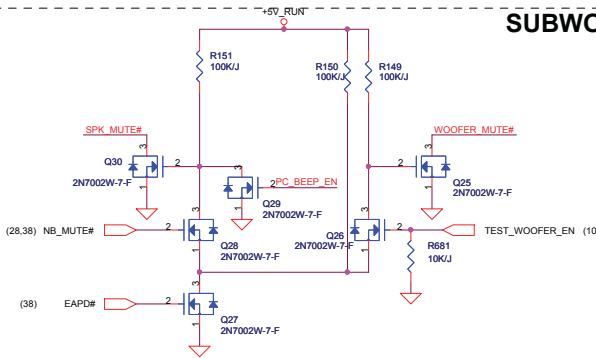
Main Speaker AMP



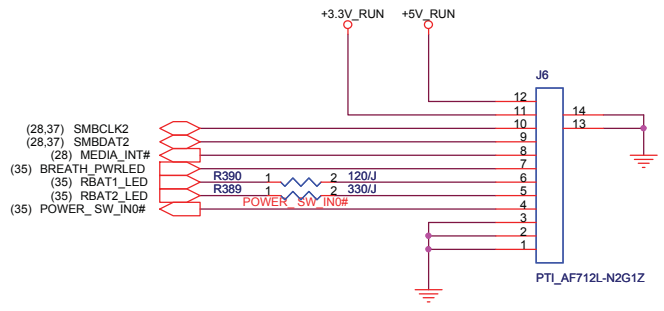
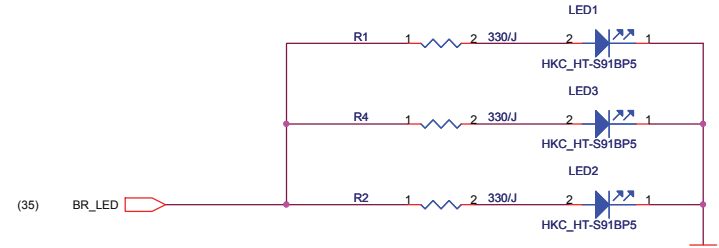
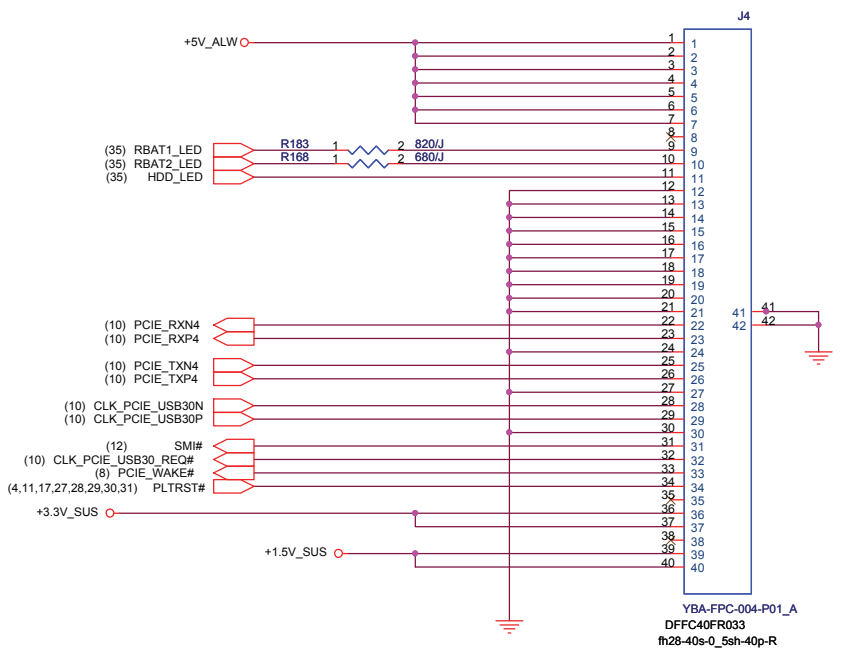
SUBWOOFER AMP



SUBWOOFER TEST

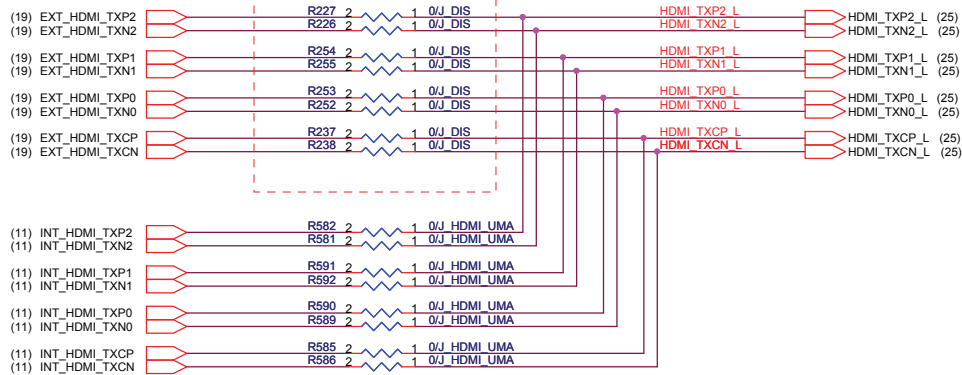


EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofers)
1	1	0	H(Test SPK)	L(Disable Woofers)
1	1	1	H	H

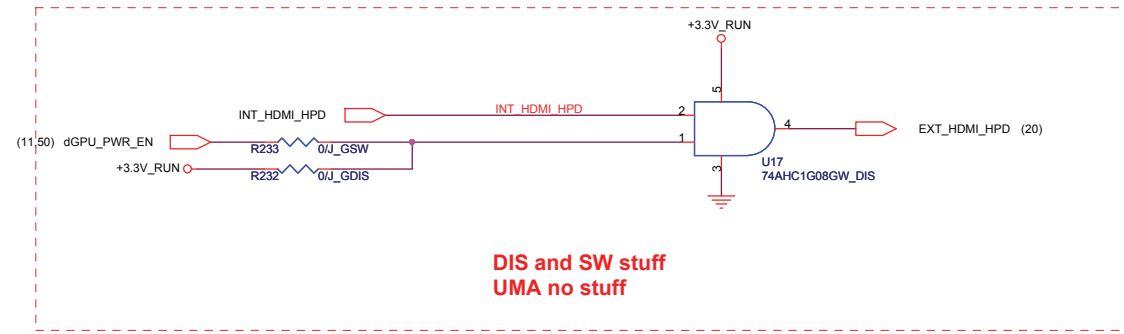
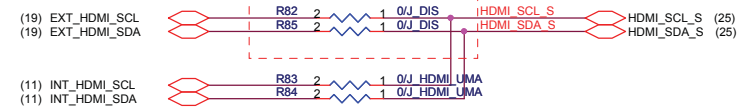


HDMI Switch

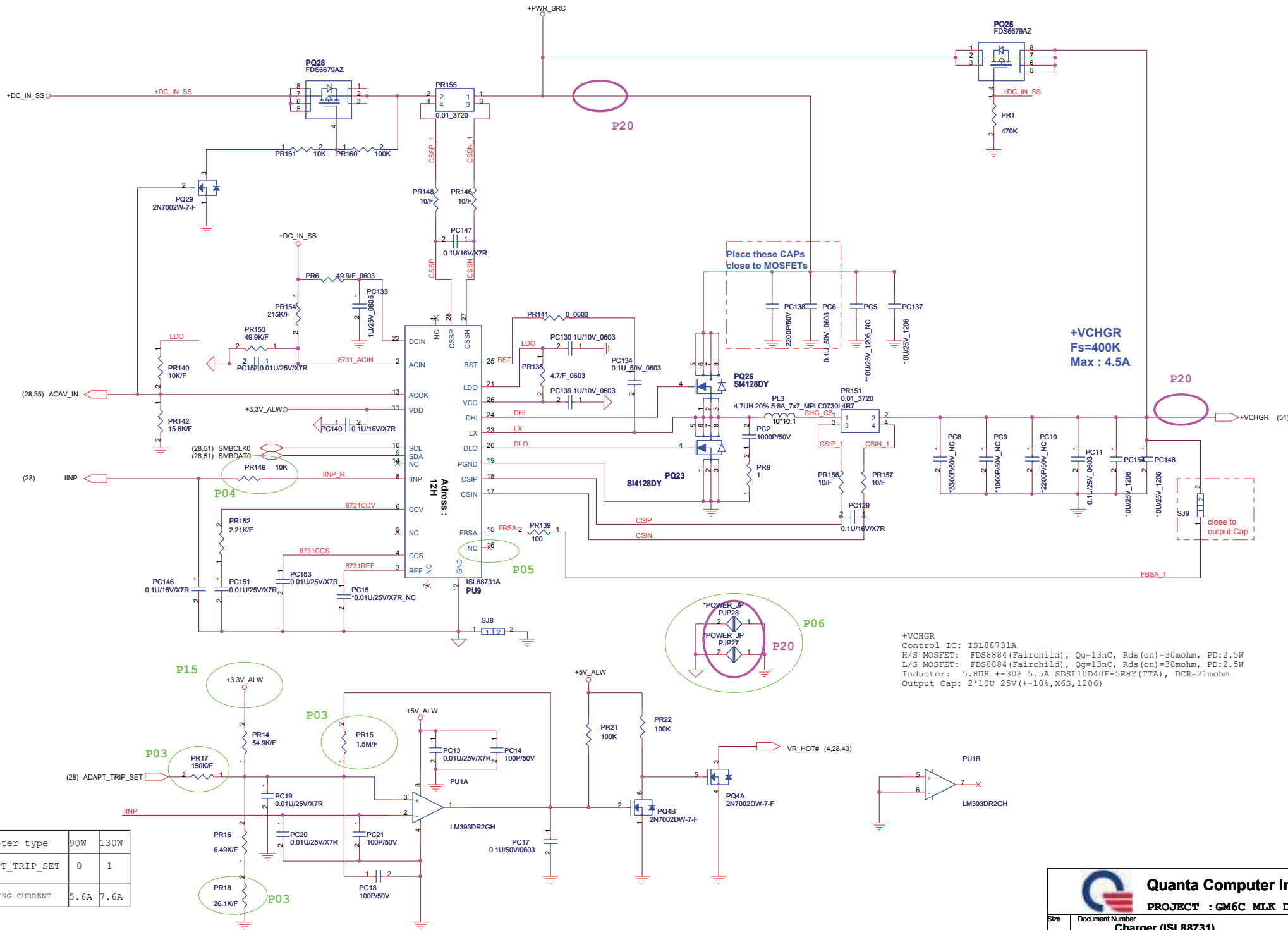
DIS and SW stuff
UMA no stuff



DIS and SW stuff
UMA no stuff

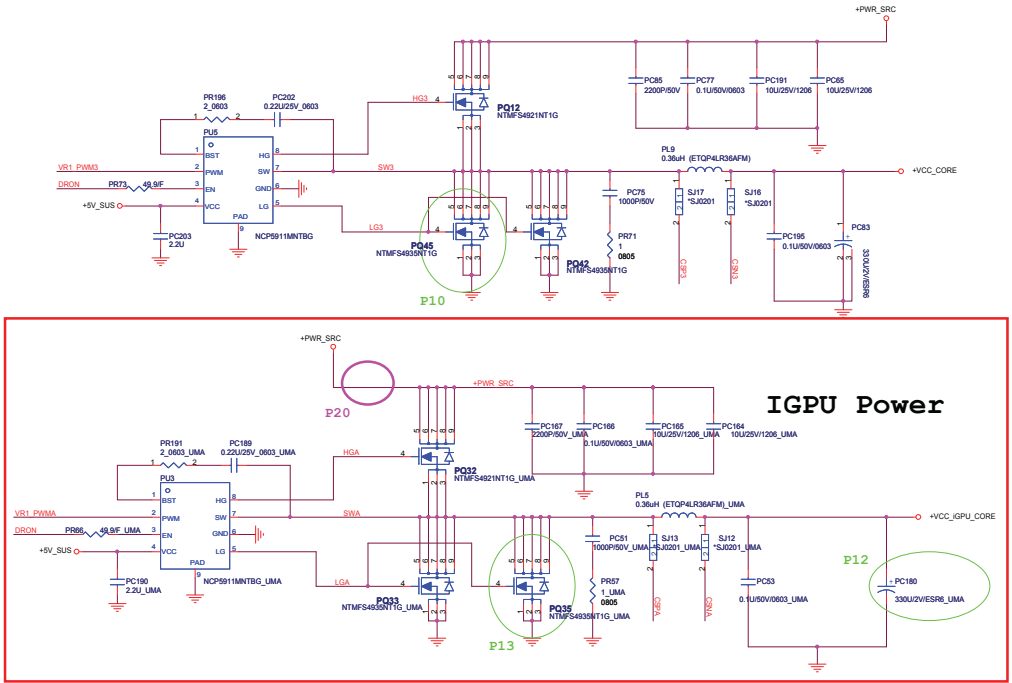
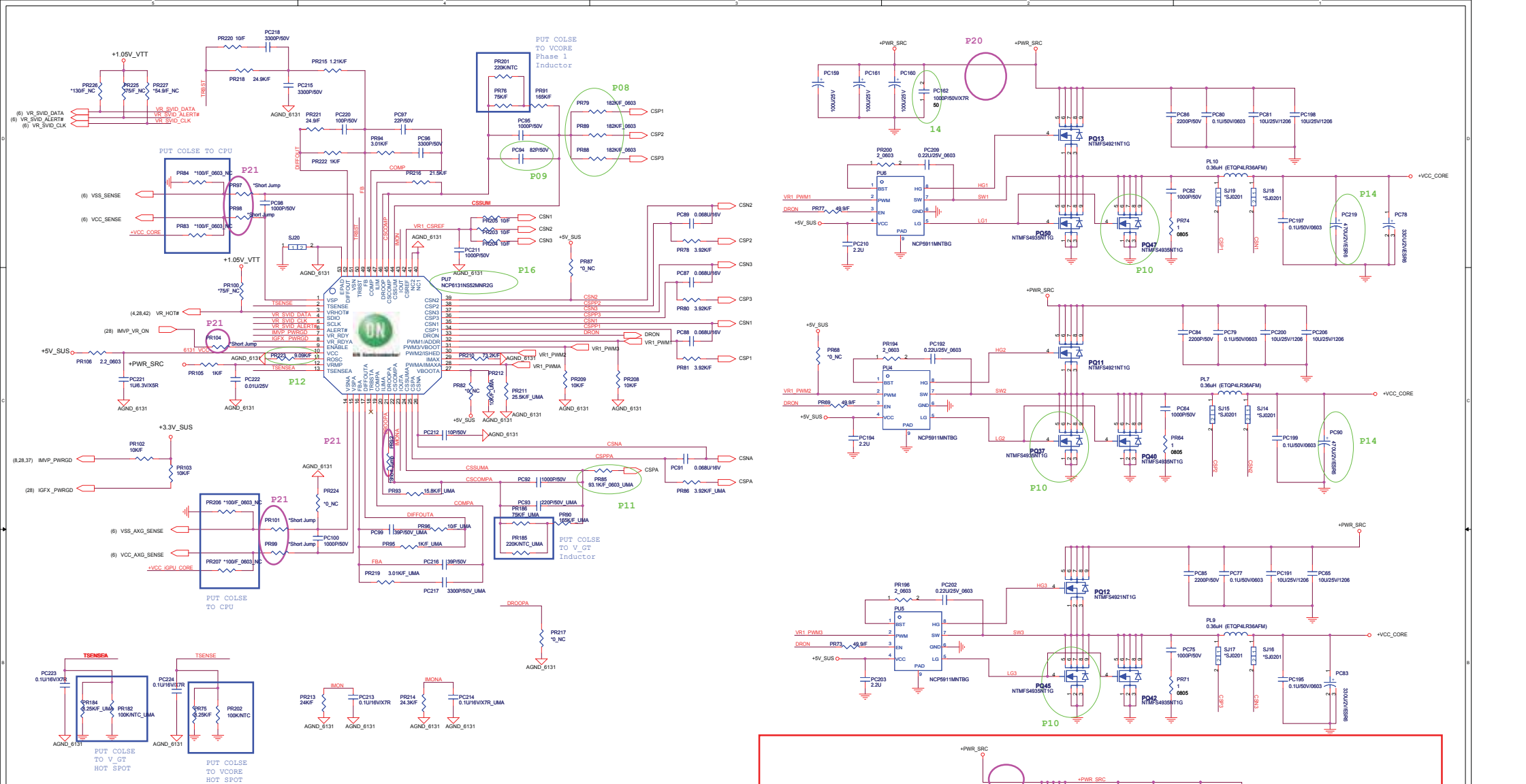


DIS and SW stuff
UMA no stuff



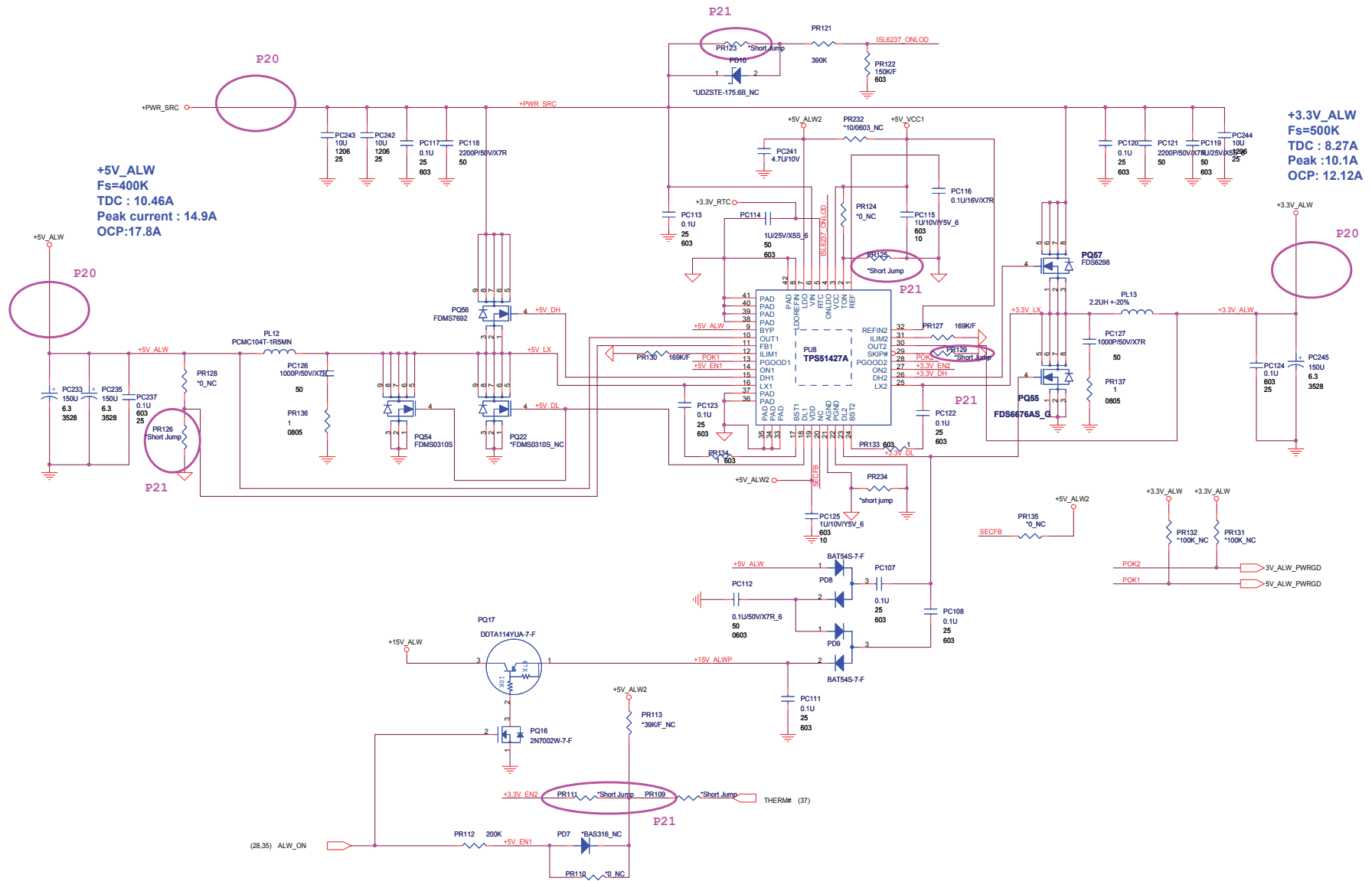
Adapter type	90W	130W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	5.6A	7.6A

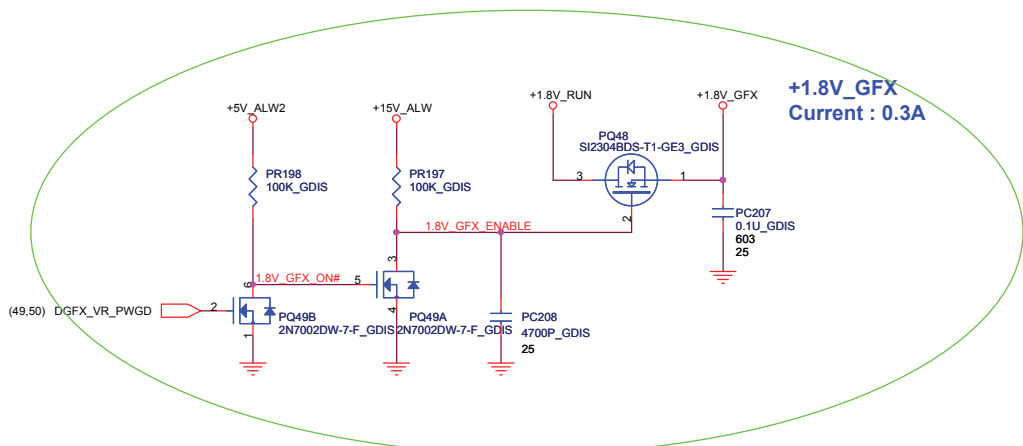
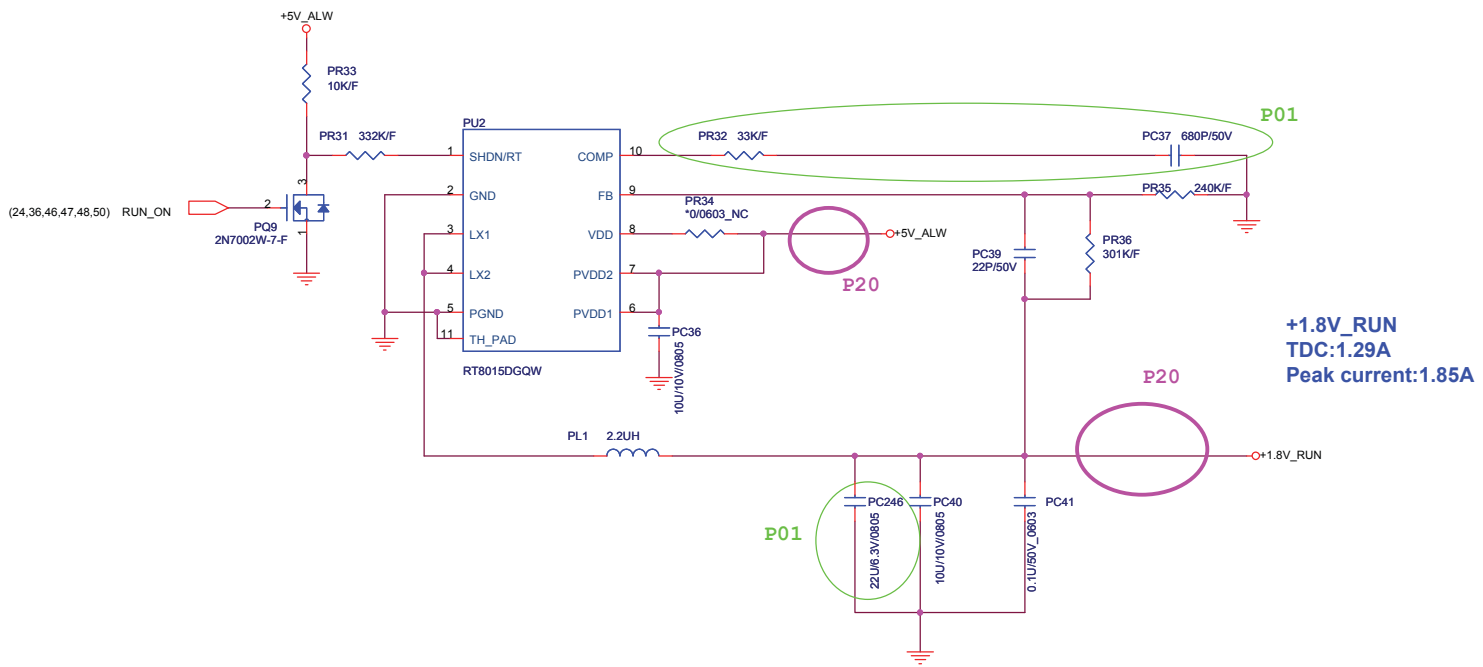
+VCHGR
Control IC: ISL88731A
H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD=2.5W
L/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD=2.5W
Inductor: 5.8uH +/-30% 5.5A SDSSL10D40F-5R8Y(TTA), DCR=21mohm
Output Cap: 2*10u 25V(+/-10%,X6S,1206)

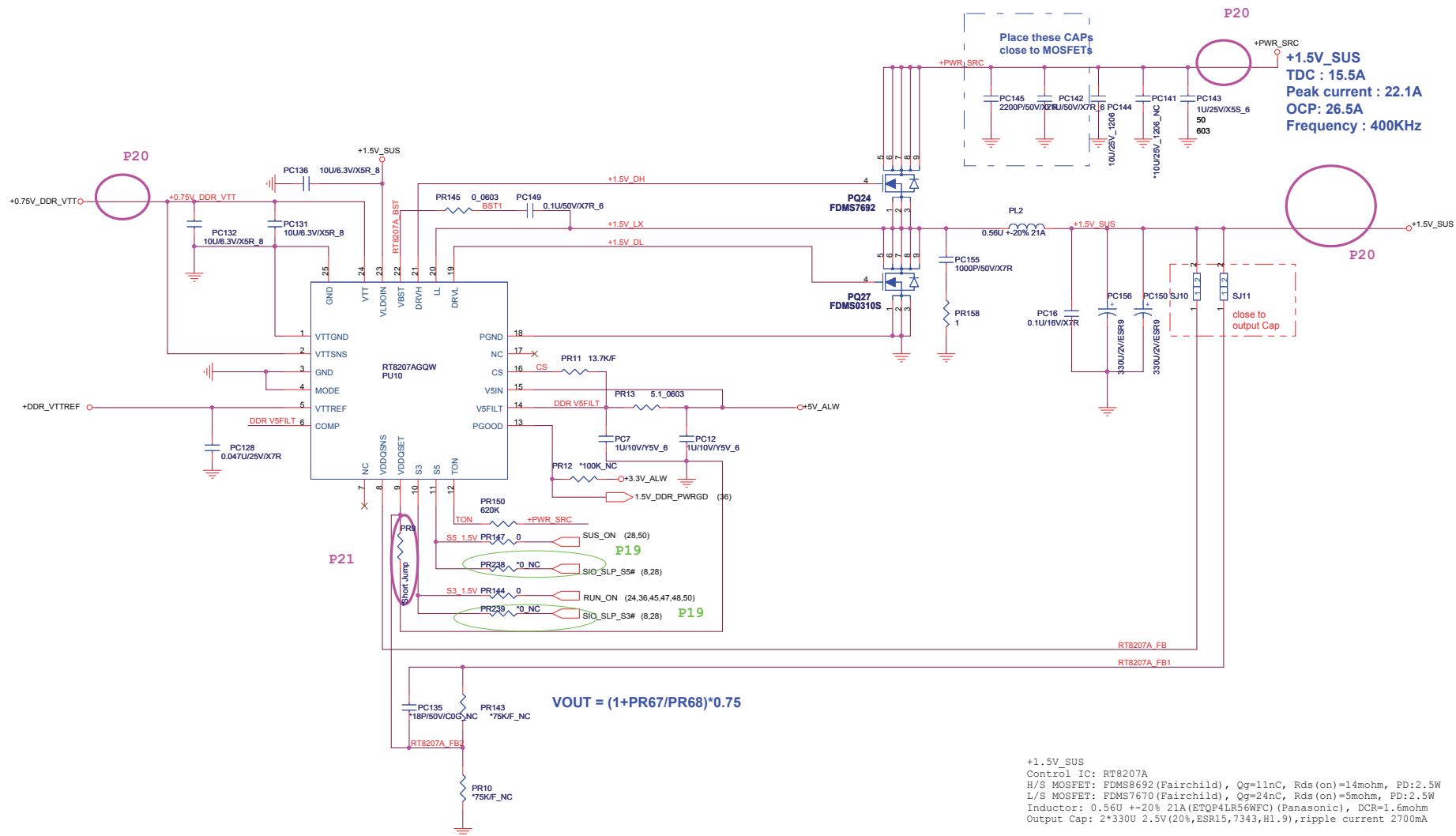


Reference	Discrete	UMA	Optimus
PR82	0(CS00002JB38)	NC	NC
PC91	0(CS00002JB38)	0.068U/16V(CH3683K1B09)	0.068U/16V(CH3683K1B09)
PC92	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PC1212	0(CS00002JB38)	10P/50V(CH01006JB08)	10P/50V(CH01006JB08)
PR217	0(CS00002JB38)	NC	NC
PC1216	0(CS00002JB38)	39P/50V(CH03906JB06)	39P/50V(CH03906JB06)
PC100	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PR224	0(CS00002JB38)	NC	NC
PR214	0(CS00002JB38)	24.3K/F(CS32432FB19)	24.3K/F(CS32432FB19)
PC223	0(CS00002JB38)	0.1U/10V(CH4102K1B03)	0.1U/10V(CH4102K1B03)

	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831







$$VOUT = (1 + PR67/PR68) * 0.75$$

+1.5V_SUS
 Control IC: RT8207A
 H/S MOSFET: FDMS7692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD=2.5W
 L/S MOSFET: FDMS7670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD=2.5W
 Inductor: 0.56uH +/-20% 21A (ETQP4LR56WPC) (Panasonic), DCR=1.6mohm
 Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

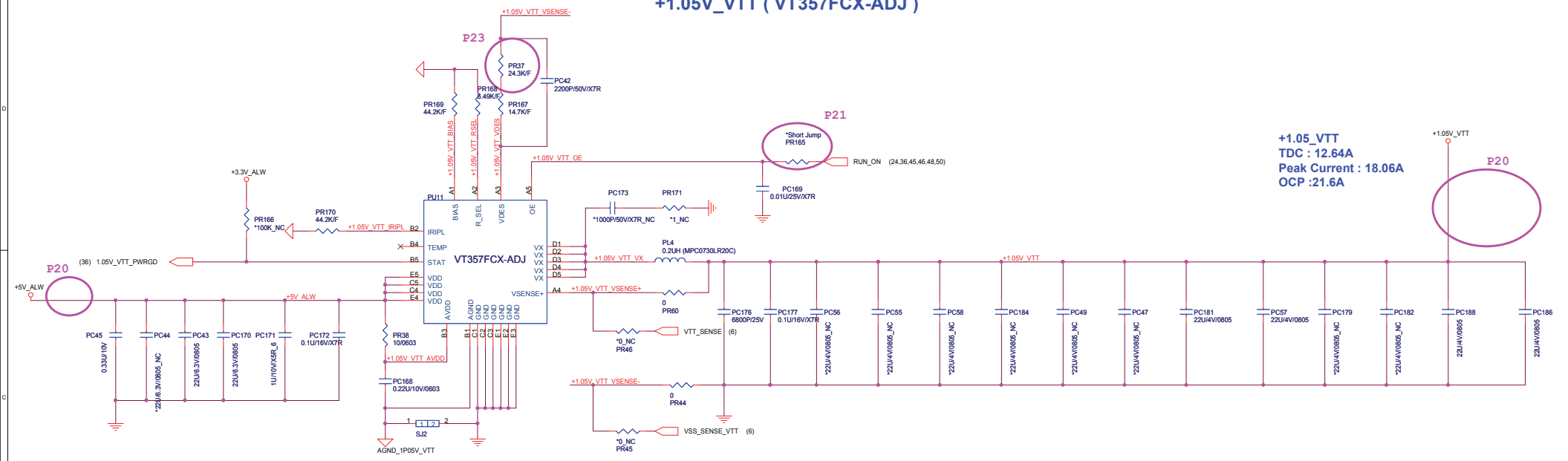
VDDQ output voltage selection

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

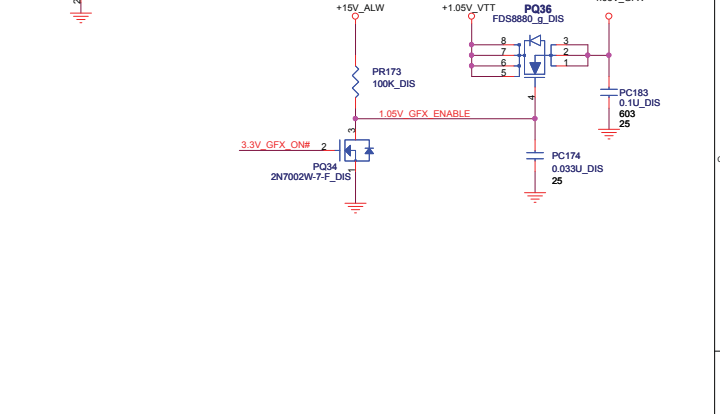
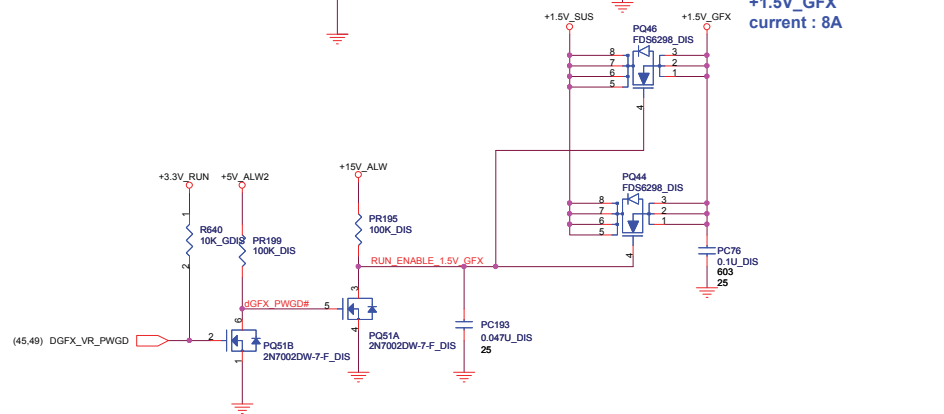
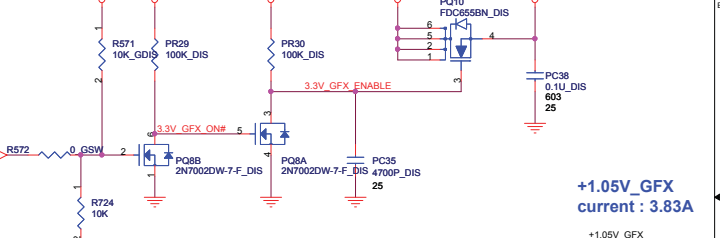
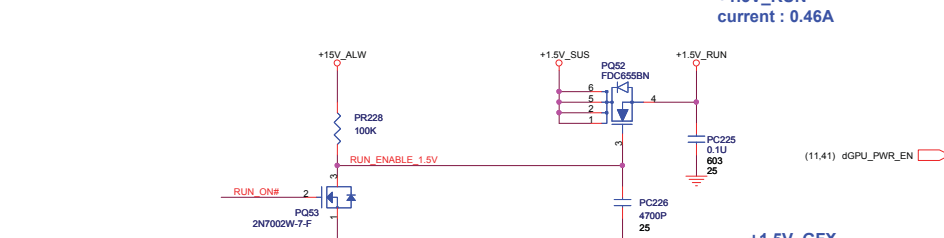
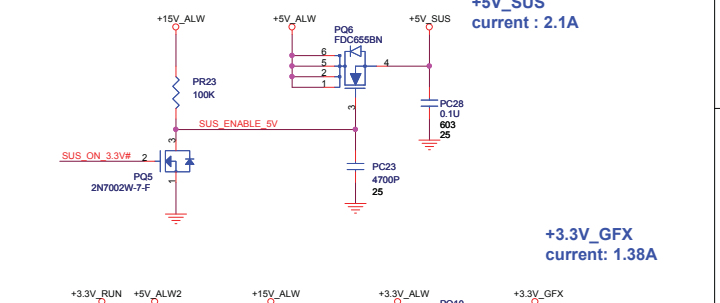
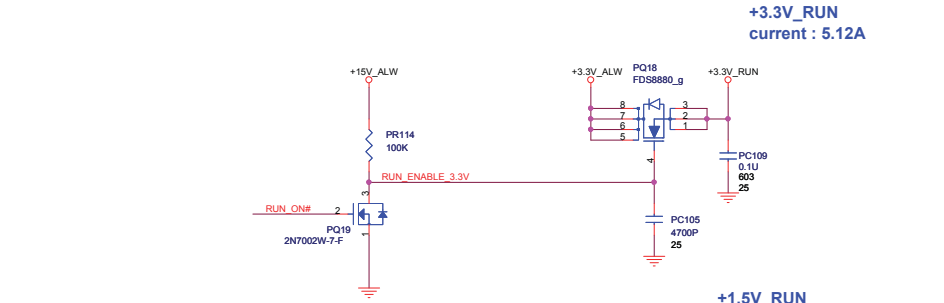
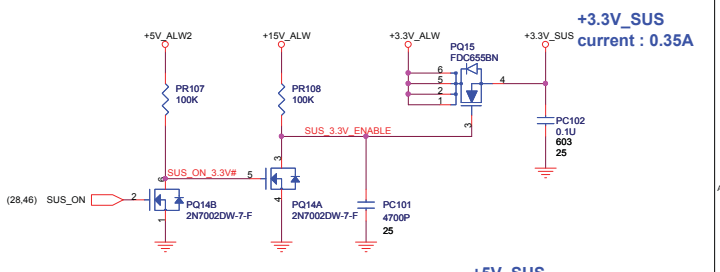
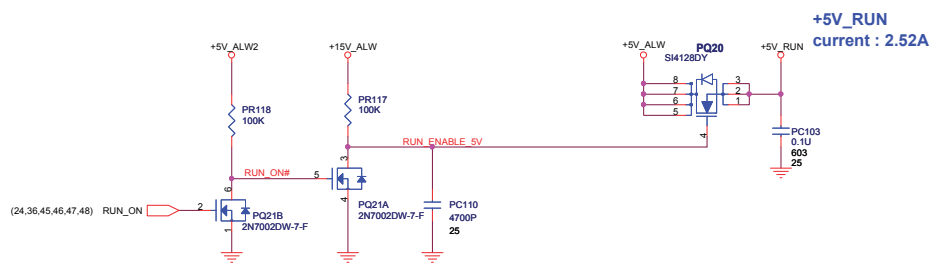
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

+1.05V_VTT (VT357FCX-ADJ)

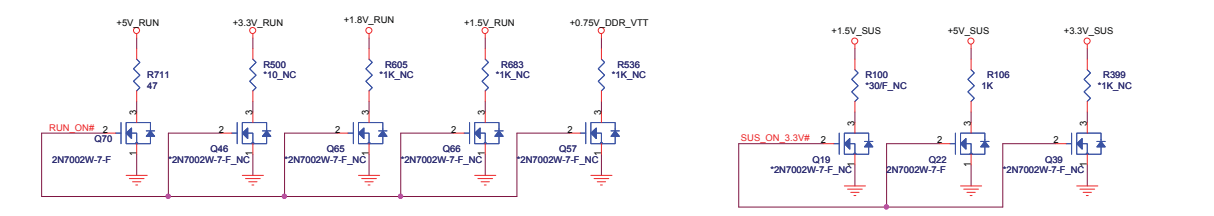


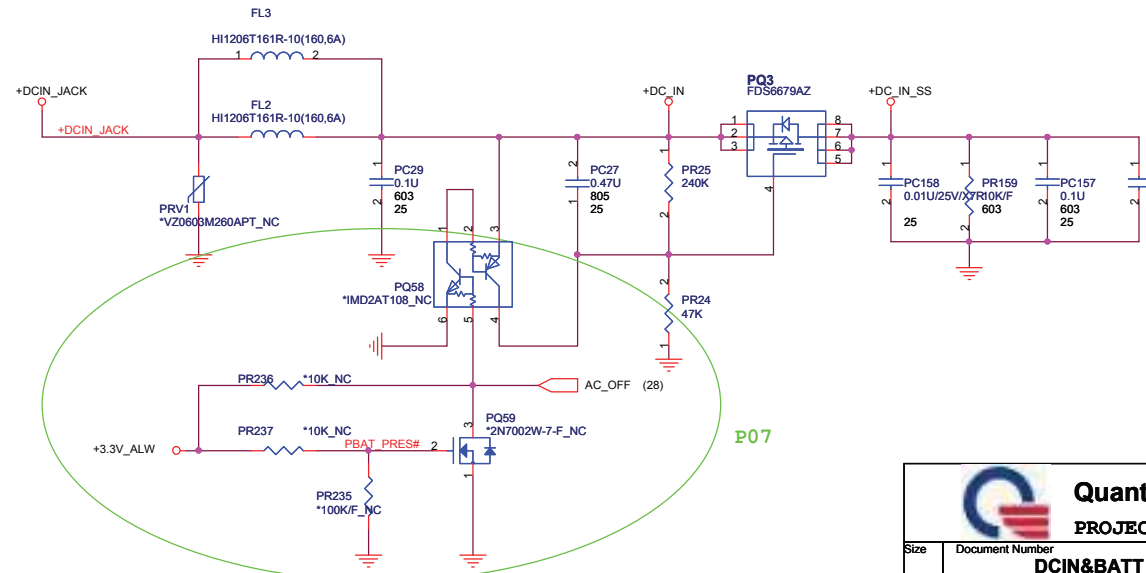
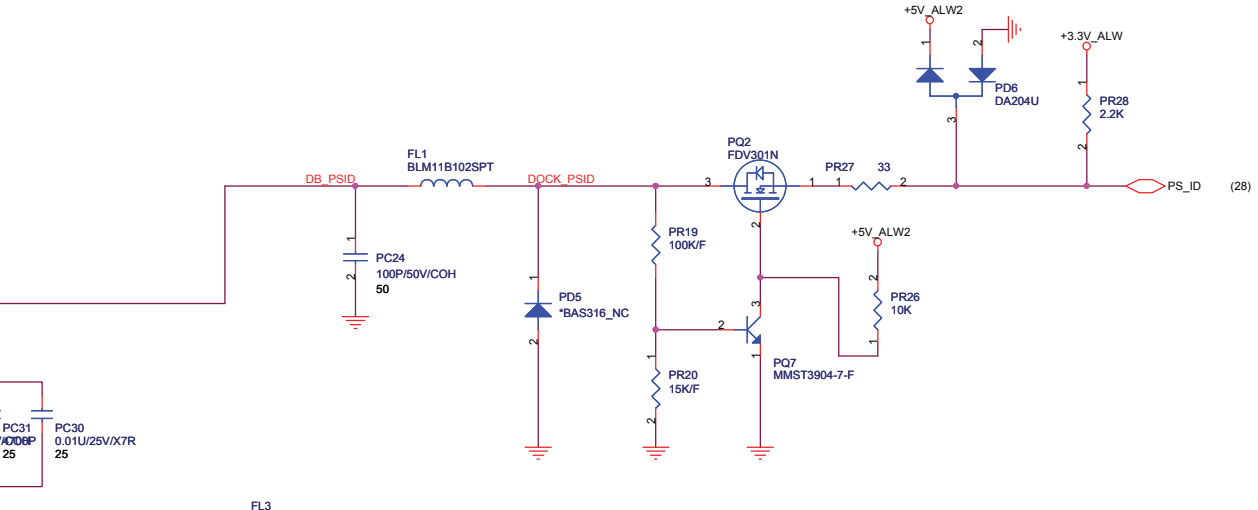
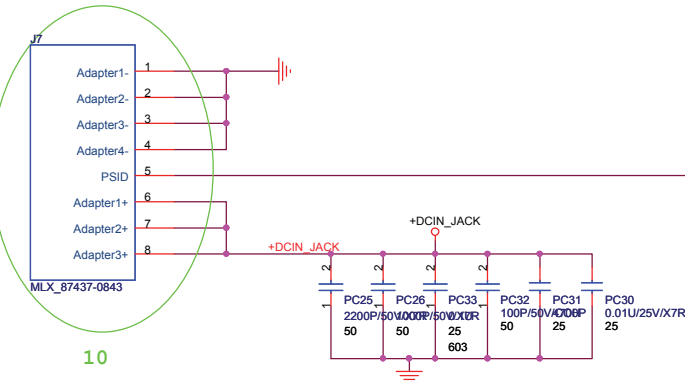
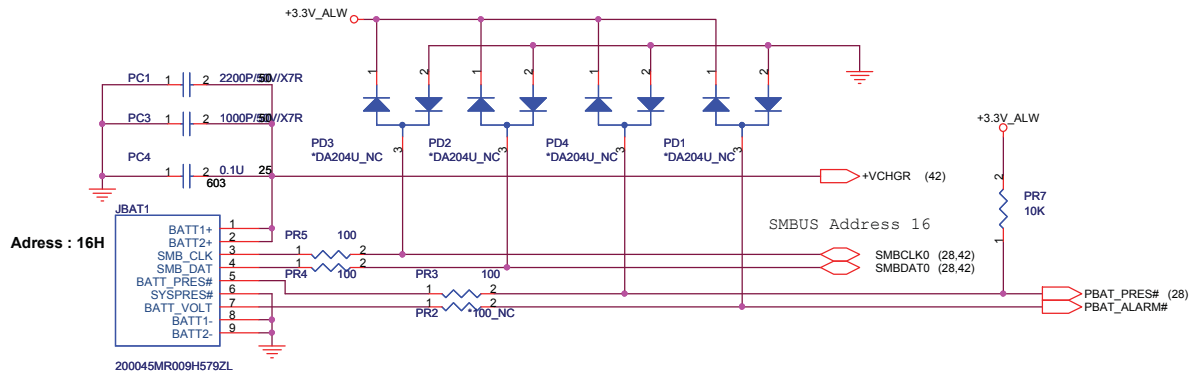
+1.05V_VTT
 TDC : 12.64A
 Peak Current : 18.06A
 OCP : 21.6A


Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE- as differential pair

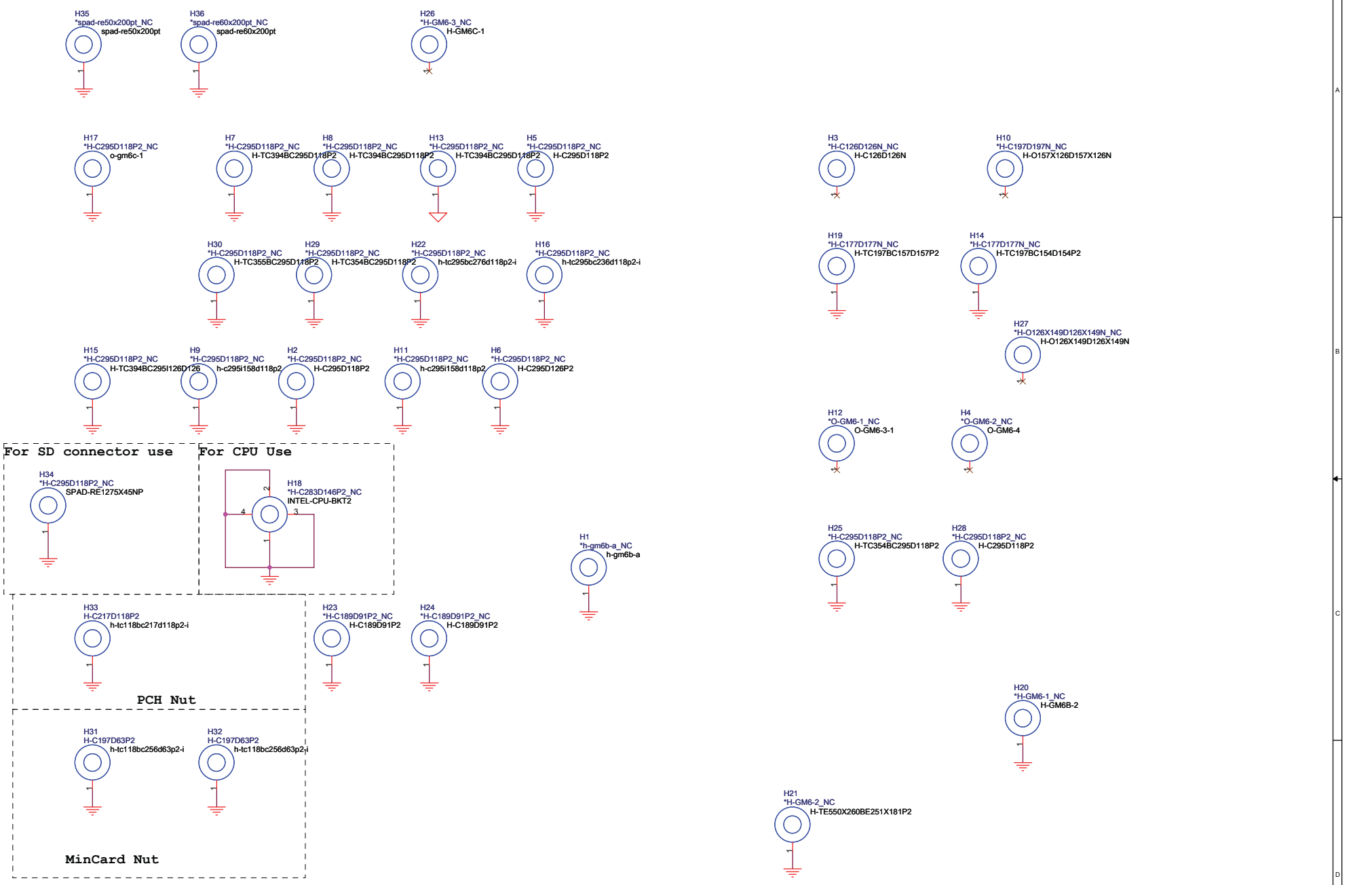


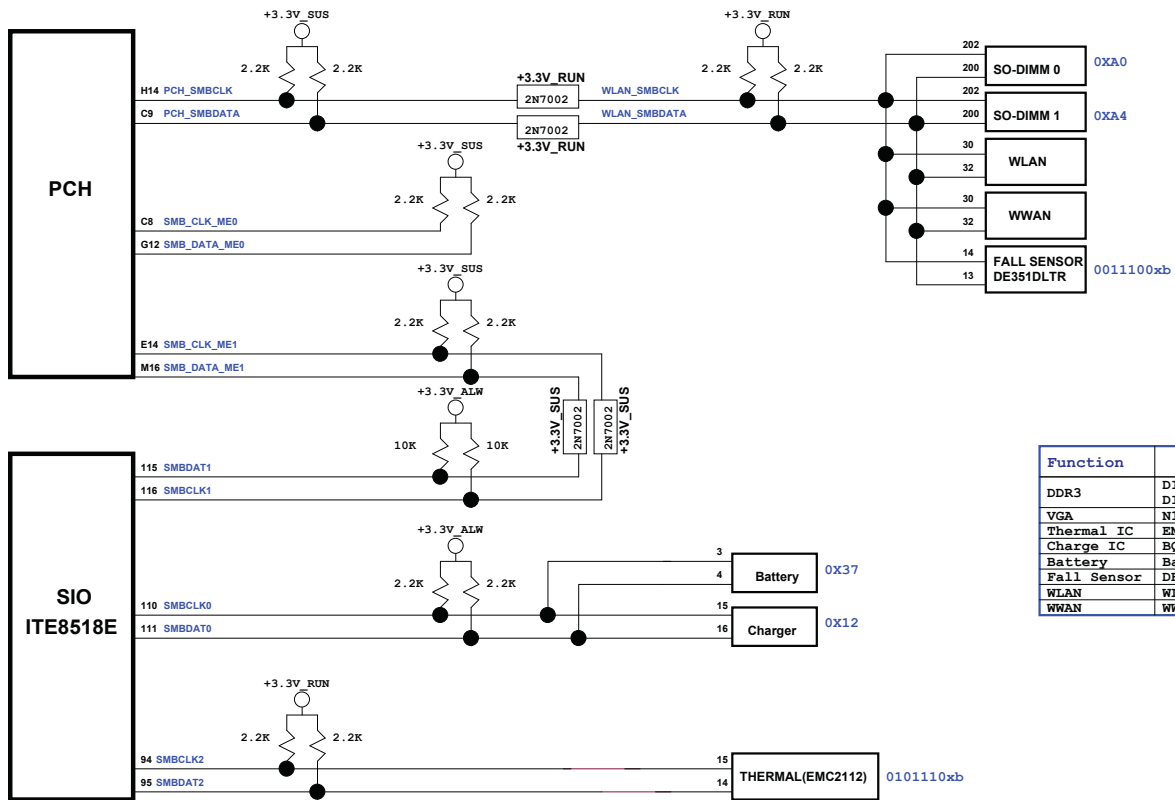
Reserve discharge path



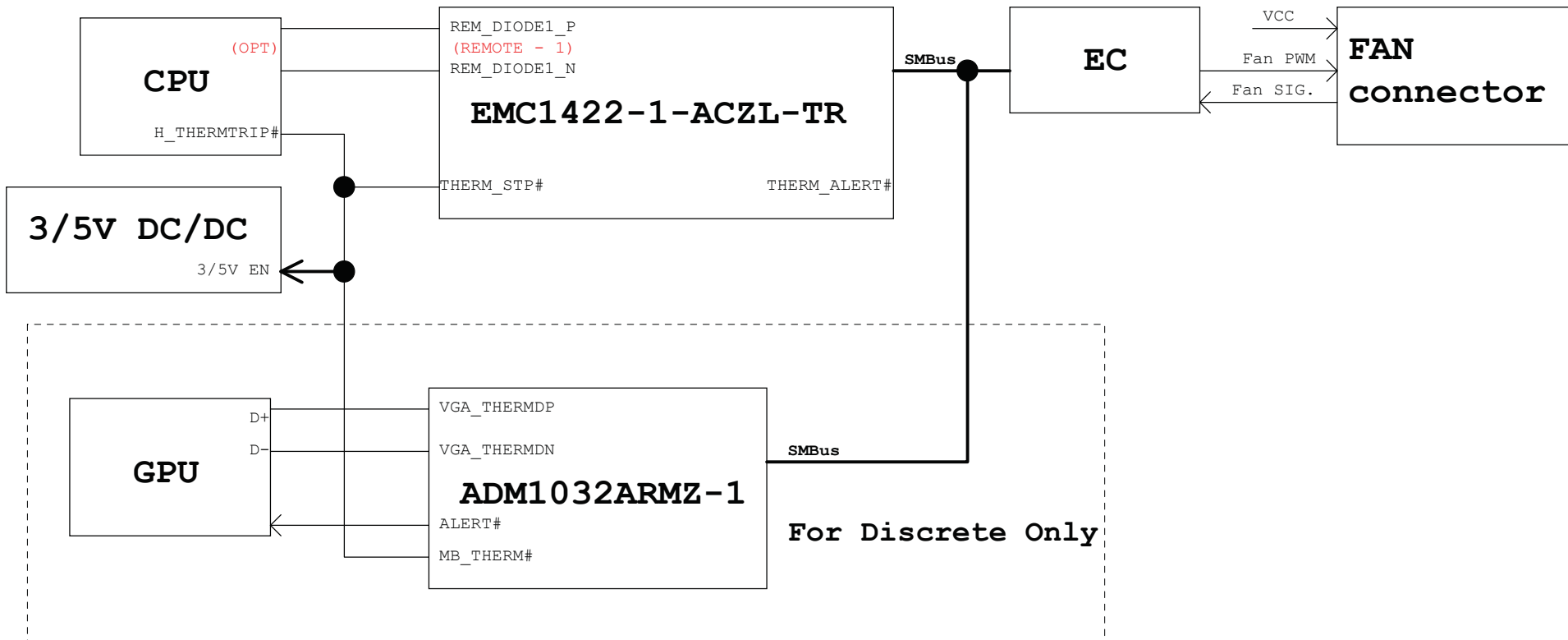



Quanta Computer Inc.
PROJECT : GM6C MLK DIS
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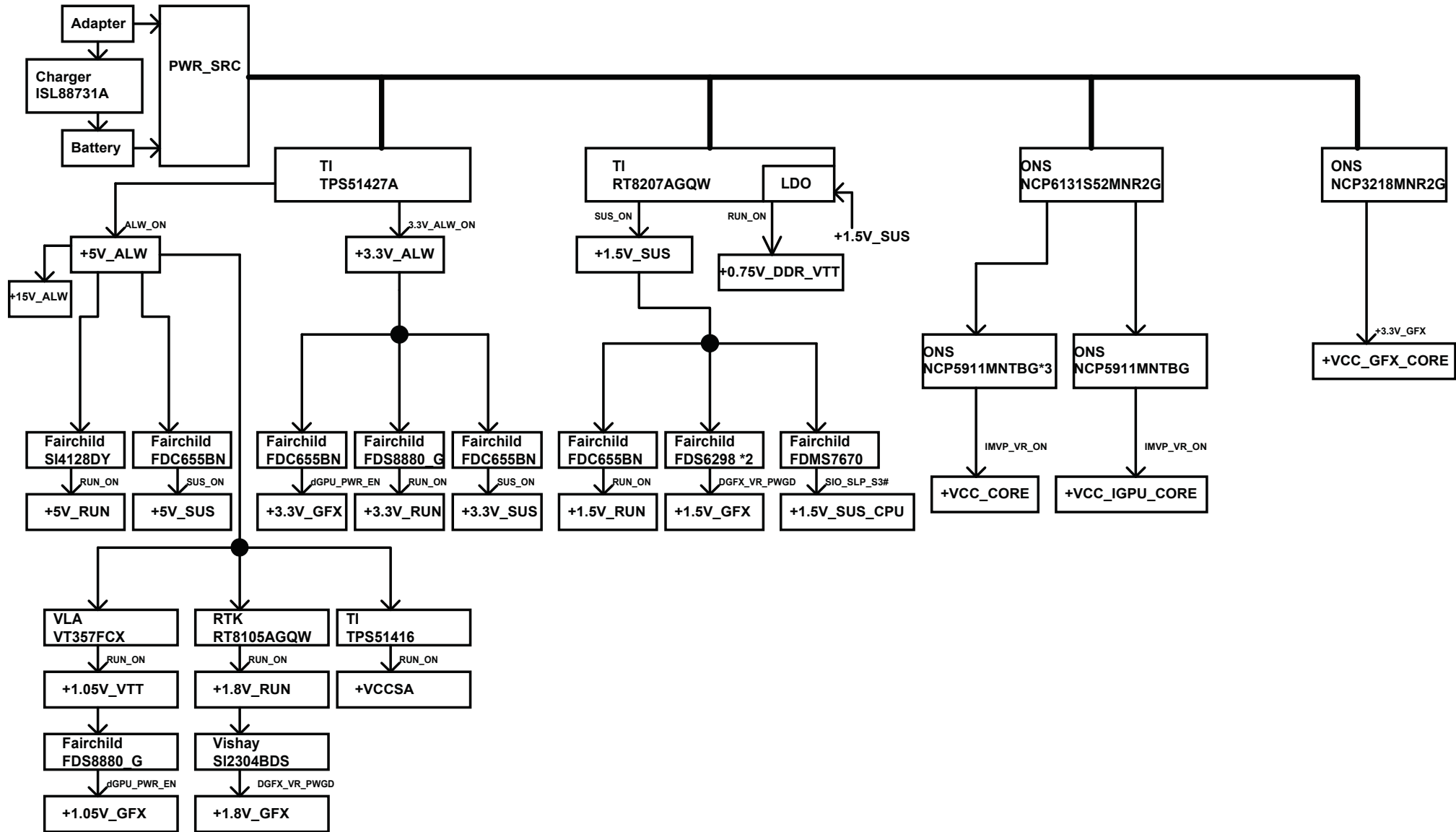




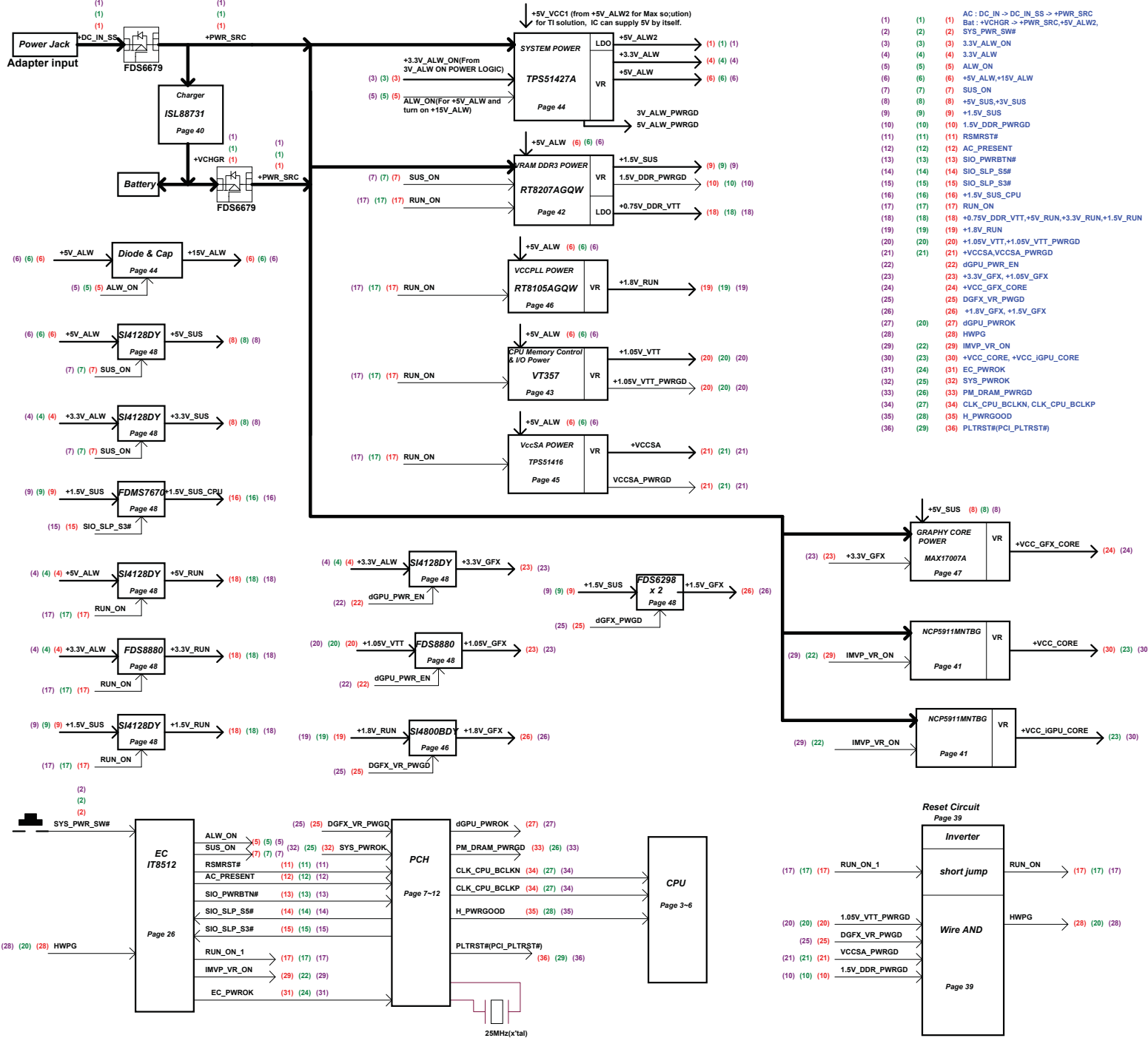
Function	IC	SMBus Address
DDR3	DIMM0	A0
	DIMM1	A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0x37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X



For Discrete Only

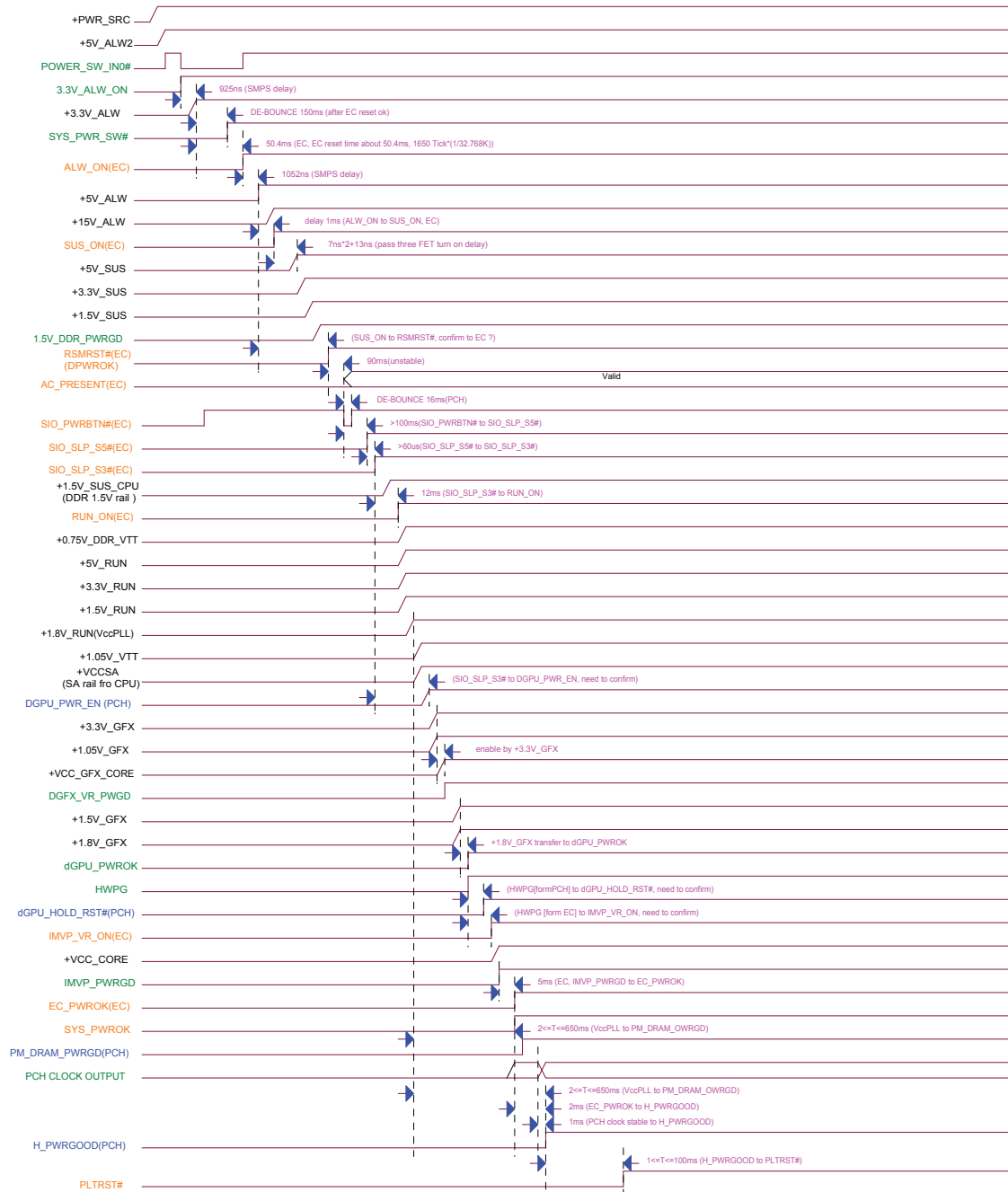


GM6C-MLK Power Design Block Diagram

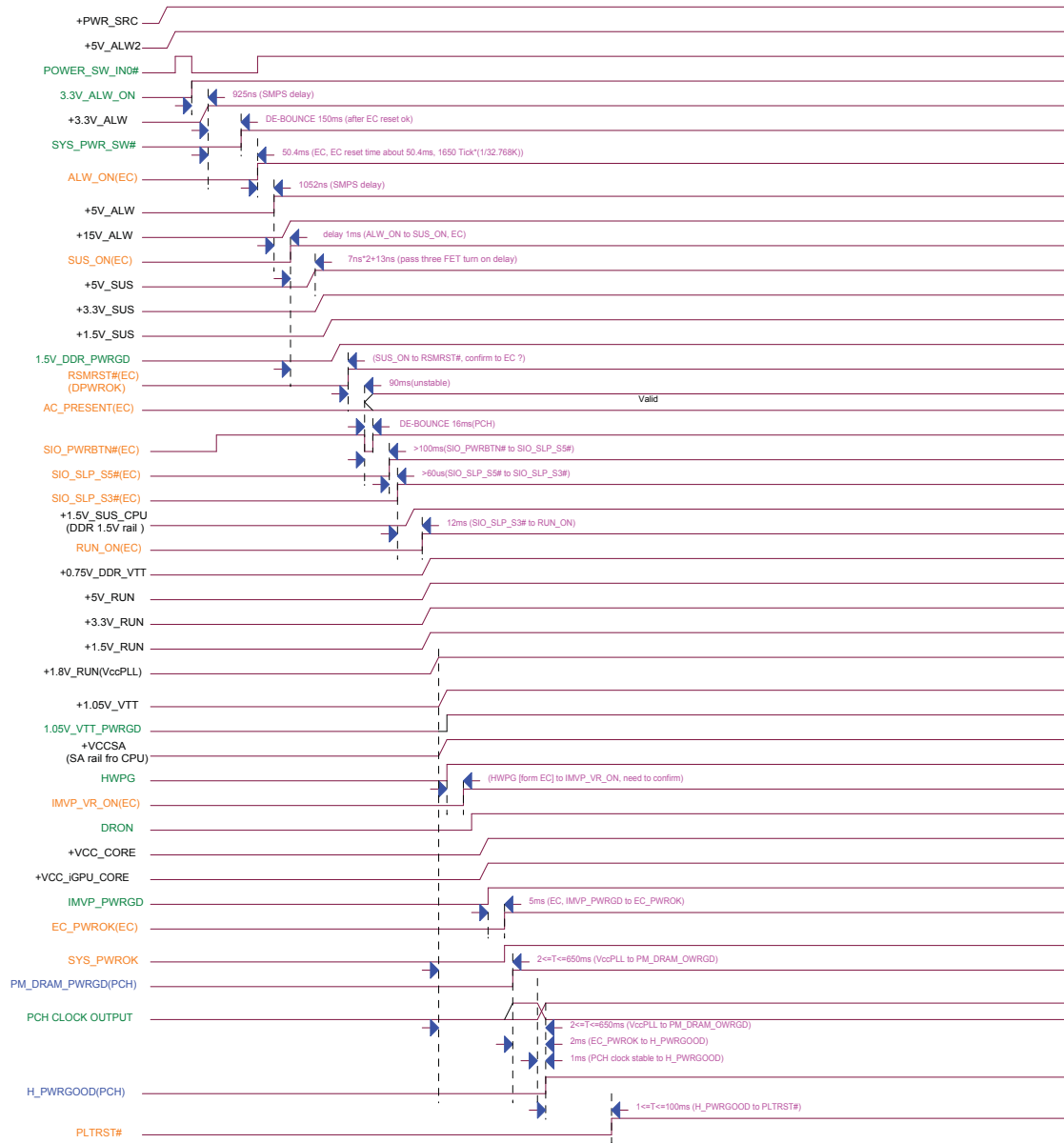


OPTIMUS	UMA	DIS
(1)	(1)	(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
(2)	(2)	(2) Bat : +VCHGR -> +PWR_SRC, +5V_ALW2, +3V_ALW_ON
(3)	(3)	(3) 3.3V_ALW_ON
(4)	(4)	(4) 3.3V_ALW
(5)	(5)	(5) ALW_ON
(6)	(6)	(6) +5V_ALW, +15V_ALW
(7)	(7)	(7) SUS_ON
(8)	(8)	(8) +5V_SUS, +3V_SUS
(9)	(9)	(9) +1.5V_SUS
(10)	(10)	(10) 1.5V_DDR_PWRGD
(11)	(11)	(11) RSMRST#
(12)	(12)	(12) AC_PRESENT
(13)	(13)	(13) SIO_PWRBTN#
(14)	(14)	(14) SIO_SLP_S#
(15)	(15)	(15) SIO_SLP_S3#
(16)	(16)	(16) +1.5V_SUS_CPU
(17)	(17)	(17) RUN_ON
(18)	(18)	(18) +0.75V_DDR_VTT, +5V_RUN, +3.3V_RUN, +1.5V_RUN
(19)	(19)	(19) +1.8V_RUN
(20)	(20)	(20) +1.05V_VTT, +1.05V_VTT_PWRGD
(21)	(21)	(21) +VCCSA, VCCSA_PWRGD
(22)	(22)	(22) dGPU_PWR_EN
(23)	(23)	(23) +3.3V_GFX, +1.05V_GFX
(24)	(24)	(24) +VCC_GFX_CORE
(25)	(25)	(25) DGFX_VR_PWGD
(26)	(26)	(26) +1.8V_GFX, +1.5V_GFX
(27)	(27)	(27) dGPU_PWRGOK
(28)	(28)	(28) HWPG
(29)	(29)	(29) IMVP_VR_ON
(30)	(30)	(30) +VCC_CORE, +VCC_IGPU_CORE
(31)	(31)	(31) EC_PWROK
(32)	(32)	(32) SYS_PWROK
(33)	(33)	(33) PM_DRAM_PWRGD
(34)	(34)	(34) CLK_CPU_BCLKN, CLK_CPU_BCLKP
(35)	(35)	(35) H_PWRGOOD
(36)	(36)	(36) PLTRST#(PCI_PLTRST#)

GM6C_MLK_DIS Power on Timing(BATTERY MODE)



GM6C_MLK_UMA Power on Timing(BATTERY MODE)



GM6C_MLK_OPTIMUS Power on Timing(BATTERY MODE)

