Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-04

REV : A00

```
DY :None Installed
UMA:UMA ONLY installed
DN15: ONLY FOR DN15 installed.
DQ15:ONLY FOR DQ15 installed.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
MUXLESS:MUXLESS solution installed.
OPTIMUS:OPTIMUS solution installed.
```

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 1 of 108

Block Diagram (Discrete/UMA co-lay)

Project code : 91.4IE01.001
PCB P/N : 10260-1
Revision : A00

##OnMainBoard

VRAM 1GB 88,89,90,91

1.N12P-GE-A1-GP(64Mx16b*8)
WKS P/N:72.51G63.H0U HYNIX
WKS P/N:72.41164.I0U SAMSUNG

DDR3 800MHz

Robson-XT& Seymour-XT& Whistler-LP& N12P-GE 15~25W 83.84,85,86,87

PCIe x 16 (Discrete only)

Intel CPU
Sandy Bridge
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 14
DDRIII Slot 1 1066/1333 15

ATI : Co-layout HDMI coming from UMA(default) & dGPU by reserving Resistor(0ohm) for optional selection.

NVidia : Co-layout HDMI coming from dGPU(Default) & UMA by reserving Resistor(0ohm) for optional selection.

FDIx4x2 (UMA only)
DMIx4

Discreet/UMA Co-lay

HDMI 51
LCD 49
CRT
Left Side: USB x 1
DCIN

HDMI
LVDS(Sigal Channel)
RGB CRT

CRT Board 82
Bluetooth 63
CAMERA 54
VOSTRO Finger Print 64

USB2.0 x 5

Intel PCH Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26

AZALIA

Internal Digital MIC
Azalia CODEC IDT 92HD87 29

2CH SPEAKER 58

SPI
Flash ROM 4MB 60

LPC Bus
LPC debug port 71

KBC NUVOTON NPCE795P 27

Touch PAD
Int. KB
Thermal P2800 28

D/A
A/D
Fan Control P2793 55

PCIE x 4
USB 2.0 x 3

I/O Board Connector 82

PCIE x 1
USB2.0 x 1
Mini-Card 802.11a/b/g

PCIE x 1
10/100/1000 NIC Realtek RTL8111E/8105E
RJ45 CONN

PCIE x 1
NEC USB3.0 UPD720200FA
USB3.0 X2 CONN

PCIE x 1,USB x 1
Mini-Card WWAN
SIM

HP1
MIC IN

SATAx1 / USB2.0x1
ESATA/USB/Powershare Combo 57

USB 2.0 x 1¡BPCIE X 1
USB 2.0 x 1
VOSTRO Express Card (On daughter board) 75

SATA x 2
CardReader Realtek RTS5138 32
SD/MMC+/MS/MS Pro/xD 74

HDD 56
ODD 56

SYSTEM LDO APL5916 48	
INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0

CPU DC/DC ISL95831HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC TPS51311 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 2 of 108

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-k[- 10-k[weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Card Reader
LANE2	Mini Card1(WLAN)
LANE3	Mini Card2(WWAN)
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	Express Card

SATA Table

SATA Pair	SATA Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 3 of 108

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

CPU1A — SANDY — 1 OF 9

DMI: 19 DMI_TXN[3:0] / 19 DMI_TXP[3:0] / 19 DMI_RXN[3:0] / 19 DMI_RXP[3:0]

FDI: 19 FDI_TXN[7:0] / 19 FDI_TXP[7:0] / 19 FDI_FSYNC0 / 19 FDI_FSYNC1 / 19 FDI_INT / 19 FDI_LSYNC0 / 19 FDI_LSYNC1

0719 Modify:
un-stuff R403 base on Intel James feedback list.

1D05V_VTT — R402 1 — 24D9R2F-L-GP — DP_COMP — R403 1 — 10KR2J-3-GP — eDP_HPD

DY

PEG_ICOMPI / PEG_ICOMPO / PEG_RCOMPO — PEG_IRCOMP_R — R401 1 — 24D9R2F-L-GP — 1D05V_VTT

PEG_RXN[0..15] — PEG_RXN[0..15] 83
PEG_RXP[0..15] — PEG_RXP[0..15] 83

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

PEG_TXN[0..15] — PEG_TXN[0..15] 83
PEG_TXP[0..15] — PEG_TXP[0..15] 83

M29	PEG_C_TXN15	C401	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN15
M32	PEG_C_TXN14	C402	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN14
M31	PEG_C_TXN13	C403	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN13
L32	PEG_C_TXN12	C404	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN12
L29	PEG_C_TXN11	C405	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN11
K31	PEG_C_TXN10	C406	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN10
K28	PEG_C_TXN9	C407	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN9
J30	PEG_C_TXN8	C408	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN8
J28	PEG_C_TXN7	C409	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN7
H29	PEG_C_TXN6	C410	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN6
G27	PEG_C_TXN5	C411	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN5
E29	PEG_C_TXN4	C412	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN4
F27	PEG_C_TXN3	C413	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN3
D28	PEG_C_TXN2	C414	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN2
F26	PEG_C_TXN1	C415	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN1
E25	PEG_C_TXN0	C416	MULTILESS	SCD22U10V2KX-1GP	PEG_TXN0
M28	PEG_C_TXP15	C417	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP15
M33	PEG_C_TXP14	C418	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP14
M30	PEG_C_TXP13	C419	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP13
L31	PEG_C_TXP12	C420	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP12
L28	PEG_C_TXP11	C421	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP11
K30	PEG_C_TXP10	C422	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP10
K27	PEG_C_TXP9	C423	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP9
J29	PEG_C_TXP8	C424	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP8
J27	PEG_C_TXP7	C425	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP7
H28	PEG_C_TXP6	C426	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP6
G28	PEG_C_TXP5	C427	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP5
E28	PEG_C_TXP4	C428	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP4
F28	PEG_C_TXP3	C429	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP3
D27	PEG_C_TXP2	C430	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP2
E26	PEG_C_TXP1	C431	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP1
D25	PEG_C_TXP0	C432	MULTILESS	SCD22U10V2KX-1GP	PEG_TXP0

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771
A00 0103 add 3rd foxcon CPU1 at XBuild batch run
3rd = 62.10055.321

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-k£[pull-Up resistor on the motherboard.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 4 of 108

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CPU1B — 2 OF 9 — SANDY

MISC: SNB_IVB#, SKTOCC#
THERMAL: CATERR#, PECI, PROCHOT#, THERMTRIP#
PWR MANAGEMENT: PM_SYNC, UNCOREPWRGOOD, SM_DRAMPWROK, RESET#
CLOCKS: BCLK, BCLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#
DDR3 MISC: SM_DRAMRST#, SM_RCOMP0, SM_RCOMP1, SM_RCOMP2
JTAG & BPM: PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO, DBR#, BPM#0–BPM#7

0625 Modify:
Add C502 47p 0402 on H_PROCHOT#.

1D05V_VTT — R501 62R2J-GP — H_PROCHOT# — C502 SC47P50V2JN-3GP
20100622 V1.2

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

18 H_SNB_IVB# → C26 SNB_IVB#
TPAD14-GP TP501 — SKTOCC#_R — AN34 SKTOCC#
TPAD14-GP TP502 — H_CATERR# — AL33 CATERR#
22,27 H_PECI — AN33 PECI
27,40,42 H_PROCHOT# — R513 56R2J-4-GP — H_PROCHOT#_R — AL32 PROCHOT#
22,36 H_THERMTRIP# — AN32 THERMTRIP#

19 H_PM_SYNC — AM34 PM_SYNC
A00 1229 EMI — EC505 MS04A03T2V2-GP-U
22,36 H_CPUPWRGD — R504 0R0402-PAD — AP33 UNCOREPWRGOOD
R503 10KR2J-3-GP
19,37 PM_DRAM_PWRGD — R505 0R2J-2-GP — V8 SM_DRAMPWROK
37 VDDPWRGOOD
18,27,71,75,82,83 PLT_RST# — R510 1K5R2F-2-GP — BUF_CPU_RST# — AR33 RESET#
R509 750R2F-GP
EC506 MS04A03T2V2-GP-U
C501 SC220P50V2KX-3GP
A00 1230 EMI

0623 Modify:
Reserved C501 220pF 0402 on BUF_CPU_RST#.

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771
3rd = 62.10055.321
A00 0103 add 3rd foxcon CPU1 at XBuild batch run

0617 Modify:
Joseph change RN501 to R512,R514 1K 0402 Resistor.

BCLK A28 → CLK_EXP_P 20
BCLK# A27 → CLK_EXP_N 20
DPLL_REF_SSCLK A16 — CLK_DP_P_R — R512 1K0R2J-1-GP
DPLL_REF_SSCLK# A15 — CLK_DP_N_R — R514 1K0R2J-1-GP — 1D05V_VTT

SM_DRAMRST# R8 — R502 4K99R2F-L-GP — SM_DRAMRST# 37

SM_RCOMP0 AK1 — SM_RCOMP_0 — R506 140R2F-GP
SM_RCOMP1 A5 — SM_RCOMP_1 — R507 25D5R2F-GP
SM_RCOMP2 A4 — SM_RCOMP_2 — R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# AP29 — XDP_PRDY# — TP511 TPAD14-GP
PREQ# AP27 — XDP_PREQ# — TP512 TPAD14-GP
TCK AR26 — XDP_TCLK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBRESET#

BPM#0 AT28 — XDP_BPM0 — TP503 TPAD14-GP
BPM#1 AR29 — XDP_BPM1 — TP504 TPAD14-GP
BPM#2 AR30 — XDP_BPM2 — TP505 TPAD14-GP
BPM#3 AT30 — XDP_BPM3 — TP506 TPAD14-GP
BPM#4 AP32 — XDP_BPM4 — TP507 TPAD14-GP
BPM#5 AR31 — XDP_BPM5 — TP508 TPAD14-GP
BPM#6 AT31 — XDP_BPM6 — TP509 TPAD14-GP
BPM#7 AR32 — XDP_BPM7 — TP510 TPAD14-GP

0630 Modify:
Removed XDP1101 connector related circuit by layout limitation.

0721 Modify:
SWAP RN501 pin1,2,3 base on swap report.

1D05V_VTT
RN501
XDP_TDO 1
XDP_TMS 2
XDP_TDI 3
XDP_TCLK 4
8 7 6 5
SRN51J-1-GP
XDP_TRST# — R511 51R2J-2-GP

3D3V_S0
19 XDP_DBRESET# — XDP_DBRESET# — R516 10KR2J-3-GP
0707 Modify:
Change R516 10K from 1K

0617 Modify:
Joseph Removed U501 Buffer reset to CPU circuit.

0719 Modify:
Add buffer for PLT_RST# based on Intel review.

Buffered reset to CPU
1D05V_VTT
3D3V_S0
R518 75R2J-1-GP
C503 SCD1U10V2KX-5GP
U501
IN B VCC
IN A
GND OUT Y
74VHC1G09DFT2G-GP
73.01G09.AAH
18,27,71,75,82,83 PLT_RST#
BUFO_CPU_RST# — R517 43R2J-GP — BUF_CPU_RST#
R515 0R2J-2-GP

XDP_TRST#
XDP_DBRESET#
SC1KP50V2KX-1GP — EC502
EC504 — SC1KP50V2KX-1GP

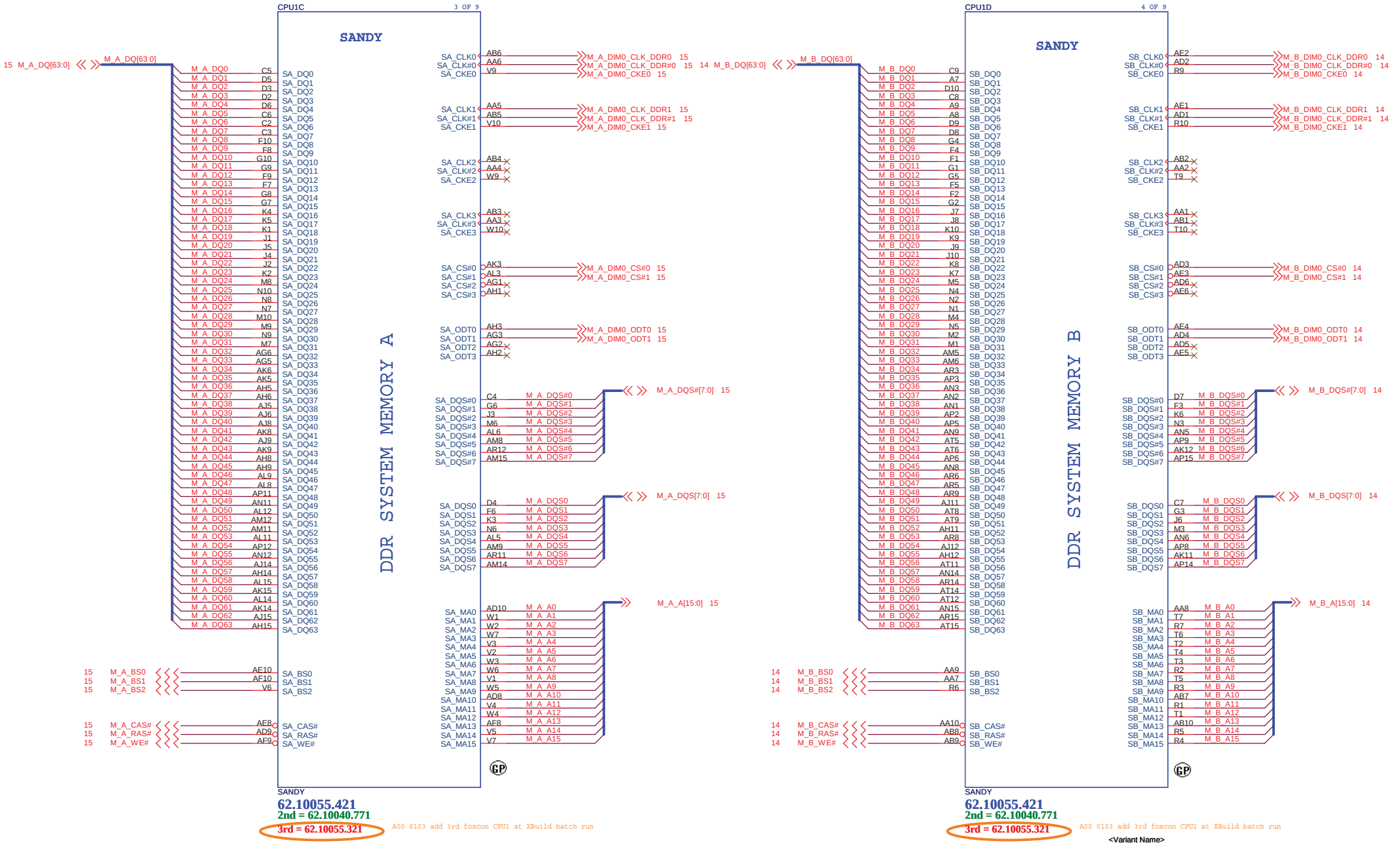
A00 1229 EMI

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THERMAL/CLOCK/PM)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 5 of 108

SSID = CPU

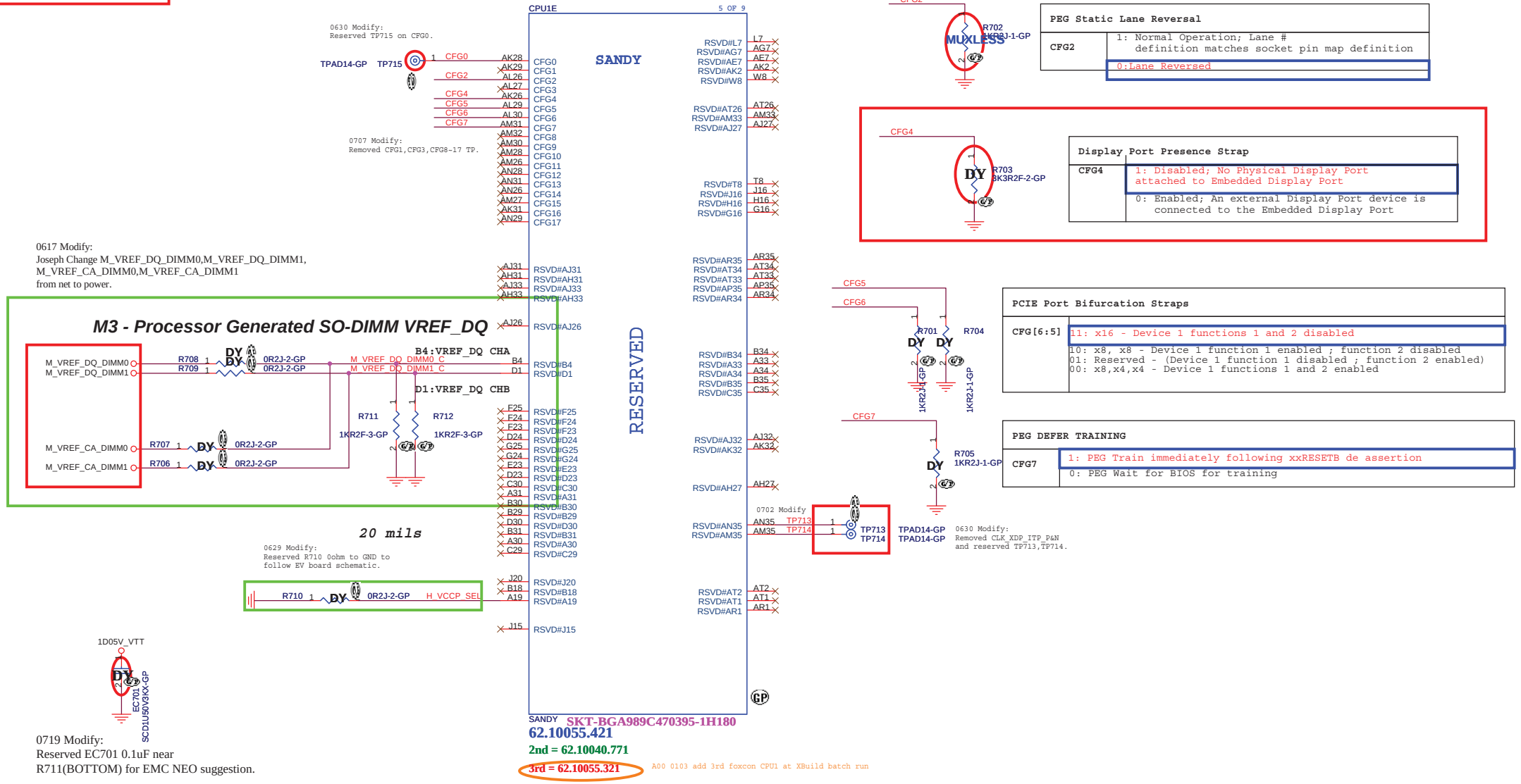


<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (DDR)	
Size A3	Document Number QUEEN 15	Rev A00
Date: Tuesday, January 04, 2011	Sheet 6 of 108	

SSID = CPU



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 7 of 108

SSID = CPU

POWER

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

CPU1F — SANDY — 6 OF 9

PEG AND DDR | CORE SUPPLY | SVID | SENSE LINES

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

PROCESSOR CORE POWER

53A

X02 1115

1115 X02 Modify:
Reserved C802~C804,C806,C807 10uF 0603
for power team fine tune Vcore quality.

VCC_CORE

SC10U6D3V5MX-2GP C802 C803 C804 C806 C807

0713 Modify:
Removed C802,C811 10uf 0603
cap base on layout limitation.

0819 De-cap DY — SC10U6D3V5KX-1GP C820 C819

0713 Modify:
Removed C818 10uf 0603 cap
base on layout limitation.

SC10U6D3V5MX-2GP C817

0726 Modify:
un-stuff C826.

SC10U6D3V5KX-1GP C816 C821 C825

SC22U6D3V5MX-2GP C826 C827

0721 Modify:
Removed C822,C823,C824

0819 De-cap

0721 Modify:
Removed C836.

SC22U6D3V5MX-L2GP C837

SC10U6D3V5KX-1GP C835 C834 C833 C832

SC22U6D3V5MX-2GP C831

0819 De-cap

0726 Modify:
un-stuff C837.

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

PROCESSOR VCCIO: 8.5A

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12

SC10U6D3V5MX-2GP C805 C808

SC10U6D3V5KX-1GP C809 C838 C839 C840 C841

0713 Modify:
Removed C810,C806,C807 10uf 0603 cap
base on layout limitation.

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

VCCIO: E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

0617 Modify:
Joseph Removed C812,
C813,C814

SC10U6D3V5KX-1GP C829 C830 C842 C843 C844 C845

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT R804 1 130R2F-1-GP

20100610 V1.0

0705 Modify:
Removed R805,R806, already PH closed PWM side.

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

VCC_CORE

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

SANDY

62.10055.421
2nd 62.10055.3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)
Size: Custom | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 8 of 108

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Edge
4 x 22 uF at Top Socket Cavity
2 x 22 uF at Bottom Socket Edge
4 x 22 uF at Bottom Socket Edge

0726 Modify:
un-stuff C906.

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

VCC_GFXCORE

0721 Modify:
Removed C903

PROCESSOR VAXG: 33A

C901 SC10U6D3V5KX-1GP
C902 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 DY SC10U6D3V5KX-1GP

0624 Modify:
Removed C918,C919 10uF 0603 for VCC_GFXCORE.

C908 SC4D7U6D3V3KX-GP
C920 DY SC10U6D3V3MX-GP
C921 DY SC10U6D3V3MX-GP

0713 Modify:
Removed C907 10uf 0603 cap.
0726 Modify:
stuff C908 10uF.

0818
De-cap

Removed DIS_ONLY Disable Resistor.
R904,R905,R901,R903

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C923 SC10U6D3V5KX-1GP
C922 SC1U10V2KX-1GP
C924 SC1U10V2KX-1GP

0617 Modify:
Joseph Removed TC902, TC903 330uF cap.

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

POWER

CPU1G — 7 OF 9

SANDY

GRAPHICS

SENSE LINES
VAXG_SENSE AK35
VSSAXG_SENSE AK34
VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

VREF
SM_VREF AL1
+V_SM_VREF_CNT
+V_SM_VREF_CNT 37

DDR3 -1.5V RAILS
VDDQ: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

SA RAIL
VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

MISC
VCCSA_SENSE H23
FC_C22 C22
VCCSA_VID1 C24

1.8V RAIL
VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17
VCCPLL: B6, A6, A2

SANDY
62.10055.421
2nd = 62.10040.771
3rd = 62.10055.321

A00 0103 add 3rd foxcon CPU1 at XBuild batch run

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U
20100609 V1.0

0719 Modify:
Add C907,C918,C919,C925 0402 0.1 uF stitching capacitors between 1D5V_S3 & 1D5V_S0 based on Intel's review

1D5V_S0

PROCESSOR VDDQ: 10A

C909 DY SC10U6D3V3MX-GP
C910 DY SC10U6D3V3MX-GP
C911 DY SC10U6D3V3MX-GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 SC10U6D3V5KX-1GP
TC901 ST330U2VDM-4-GP
C907 DY SCD1U10V2KX-5GP
C918 DY SCD1U10V2KX-5GP
C919 DY SCD1U10V2KX-5GP
C925 DY SCD1U10V2KX-5GP
1D5V_S3

79.33719.201
2nd = 77.C3371.13L

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 SC10U6D3V5KX-1GP
C915 SC10U6D3V5KX-1GP
C917 SC10U6D3V5KX-1GP
DY EC902 SCD1U50V3KX-GP

0617 Modify:
Joseph Removed TC902,TC903 330uF cap.
0719 Modify:
Reserved EC902 0.1uF near C917 for EMC NEO suggestion.

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0624 Modify:
Removed R902 10ohm closed CPU side.
0713 Modify:
Add R908 100ohm PH to 0D85V_S0.
0714 Modify:
Removed R908 PH.

VCCUSA_SENSE 48
H_FC_C22 48
VCCSA_SEL 48

RN901 SRN1KJ-7-GP
0714 Modify:
RN901 change to 1K PL from 10K base on Intel PDDG updated.

DCBATOUT
EC903 SCD1U50V3KX-GP

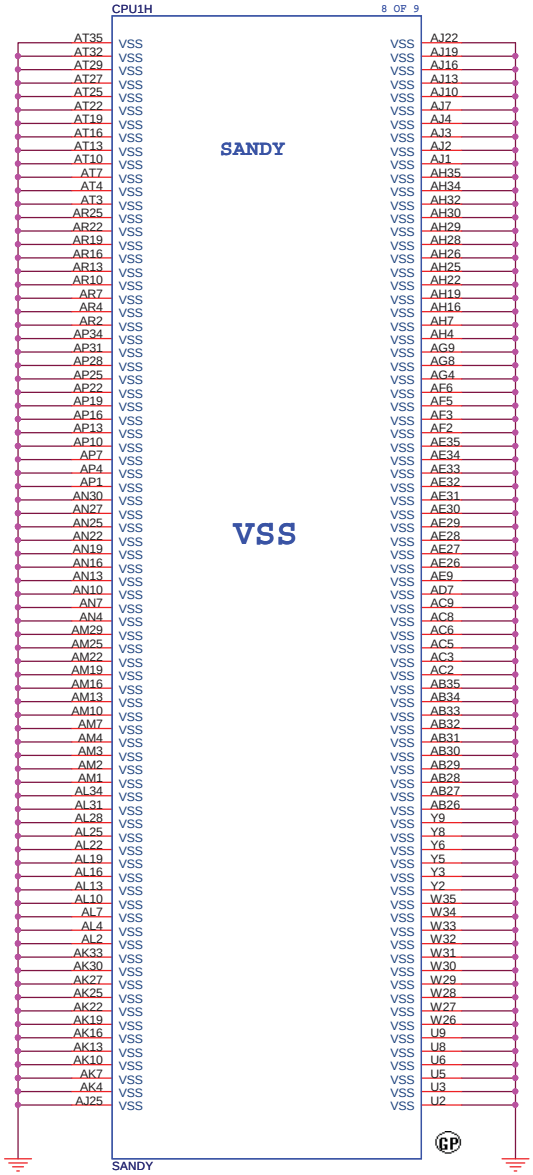
1122 X02 Modify:
stuff EC901 0.1uF from EMC Neo suggestion.

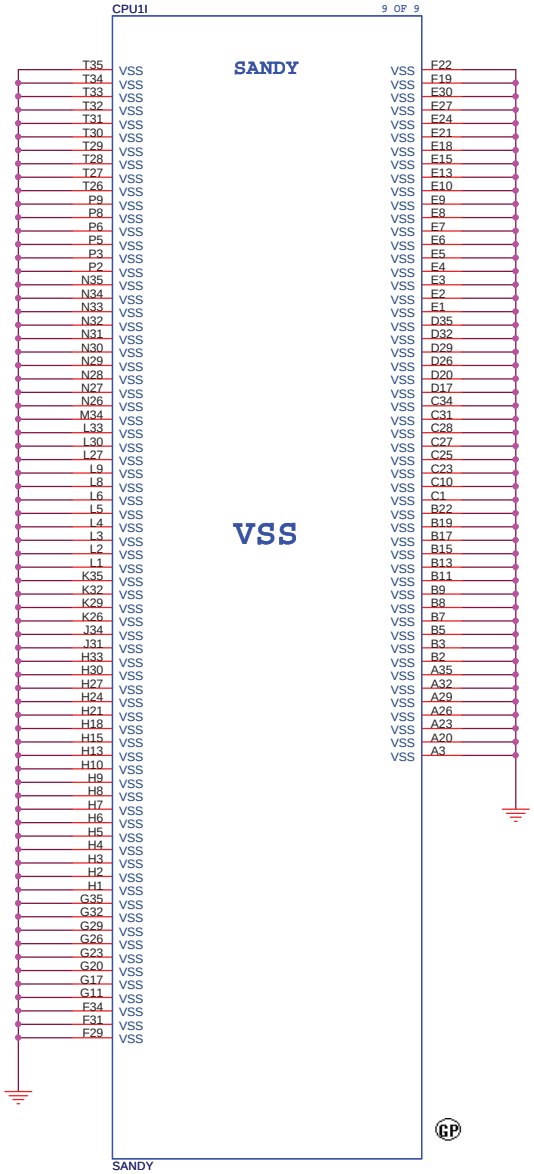
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 9 of 108

SSID = CPU





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 10 of 108

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 11 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 12 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 13 of 108

SSID = MEMORY

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1, M_VREF_CA_DIMM0,M_VREF_CA_DIMM1 from net to power.

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1, M_VREF_CA_DIMM0,M_VREF_CA_DIMM1 from net to power.

0707 Modify:
Change R1404,R1405 to 0ohm 0402 from short pad.

Place these caps close to VTT1 and VTT2.

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1, M_VREF_CA_DIMM0,M_VREF_CA_DIMM1 from net to power.

0624 Modify:
SWAP DM1 and DM2 location.

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

0617 Modify:
Joseph dummy C1401 default un-stuff.

Layout Note:
Place these Caps near SO-DIMMA.

1110 X02 Modify:
DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.

PART NUMBER	Height	TYPE
62.10017.P61	5.2mm	REVERSED
62.10017.N41(2nd)	5.2mm	REVERSED
62.10017.P41(3rd)	5.2mm	REVERSED
62.10024.E21(4th)	5.2mm	REVERSED

H =5.2mm

DDR3-204P-48-GP
62.10017.P61
2nd = 62.10017.N41
3rd = 62.10017.P41
4th = 62.10024.E21

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2
Size: Custom | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 14 of 108

SSID = MEMORY

0624 Modify:
SWAP DM1 and DM2 location.

DM1

20101220 R1501 R1502 for change to parallel resistor

RN1501
SRN10KJ-5-GP

A00

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

0707 Modify:
Change R1503,R1504 to 0ohm 0402 from short pad.

DDR_VREF_S3

R1504
0R0402-PAD-2-GP

M_VREF_CA_DIMM0

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0,M_VREF_CA_DIMM1
from net to power.

C1523 DY C1524 C1522

SCD1U10V2KX-5GP
SC2D2U10V3KX-1GP
SCD1U10V2KX-5GP

DDR_VREF_S3

R1503
0R0402-PAD-2-GP

M_VREF_DQ_DIMM0

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0,M_VREF_CA_DIMM1
from net to power.

C1515 DY C1516 C1517

SCD1U10V2KX-5GP
SC2D2U10V3KX-1GP
SCD1U10V2KX-5GP

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1518 C1519 DY C1520 C1521

SC1U6D3V2KX-GP

M_A_A[15:0] 6

M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6

6 M_A_DIM0_ODT0
6 M_A_DIM0_ODT1
M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

14,37 DDR3_DRAMRST#

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0,M_VREF_CA_DIMM1
from net to power.

0D75V_S0

H =9.2mm

DDR3-204P-42-GP

M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6

M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6

M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6

M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6

M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,79,82
PCH_SMBCLK 14,20,79,82

TS#_DIMM0_1 14

SA0_DIM0
SA1_DIM0

3D3V_S0

DY C1501 C1502

SCD1U10V2KX-5GP
SC2D2U10V3KX-1GP

1D5V_S3

SODIMM B DECOUPLING

DY C1503 DY C1504 C1505 C1506 DY C1507 DY C1508 DY C1509 DY C1510

SC10U10V5ZY-1GP
SC10U10V5ZY-1GP
SC22U6D3V5MX-2GP
SC10U6D3V5KX-1GP
SC10U6D3V5KX-1GP
SC10U10V5ZY-1GP
SC10U6D3V5KX-1GP
SC10U6D3V5KX-1GP

0818 De-cap

C1511 SC1U6D3V2KX-GP DY C1512 SCD1U10V2KX-5GP C1513 SCD01U50V2KX-1GP C1514 SCD01U50V2KX-1GP

0818 De-cap

Layout Note:
Place these Caps near SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q41	9.2mm	REVERSED
62.10017.N11(2nd)	9.2mm	REVERSED
62.10017.N61(3rd)	9.2mm	REVERSED
62.10024.D91(4th)	9.2mm	REVERSED

1110 X02 Modify:
DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.

62.10017.Q41
2nd = 62.10017.N11
3rd = 62.10017.N61
4th = 62.10024.D91

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: Custom | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 15 of 108

(Blanking)

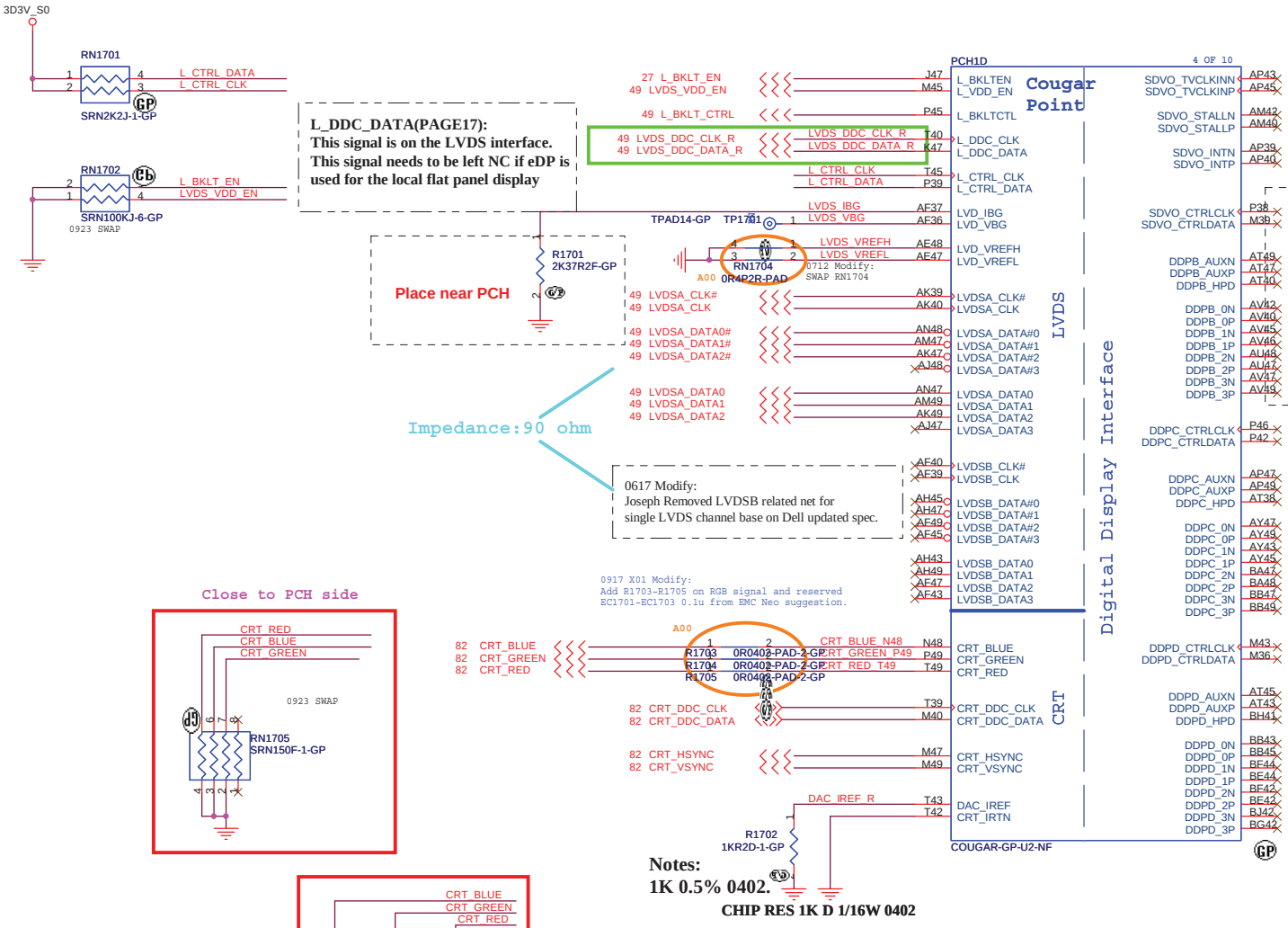
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 16 of 108



Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

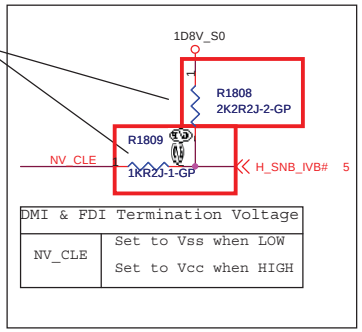
Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 17 of 108

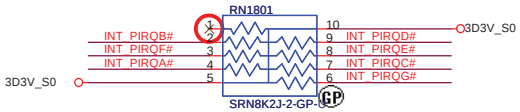
SSID = PCH

0719 Modify:
DF_TVS (NV_CLE) connect PROC_SELECT# (H_SNB_IVB#) with R1808 2.2K;Ó5% pull up resistor to PCH VCCPNAND rail and a R1809 1K;Ó5% series resistor base on Intel feedback.

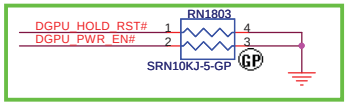


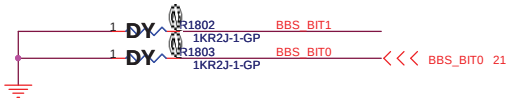
DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

0709 Modify:
Removed INT_PIRQH# on RN1801 pin1.

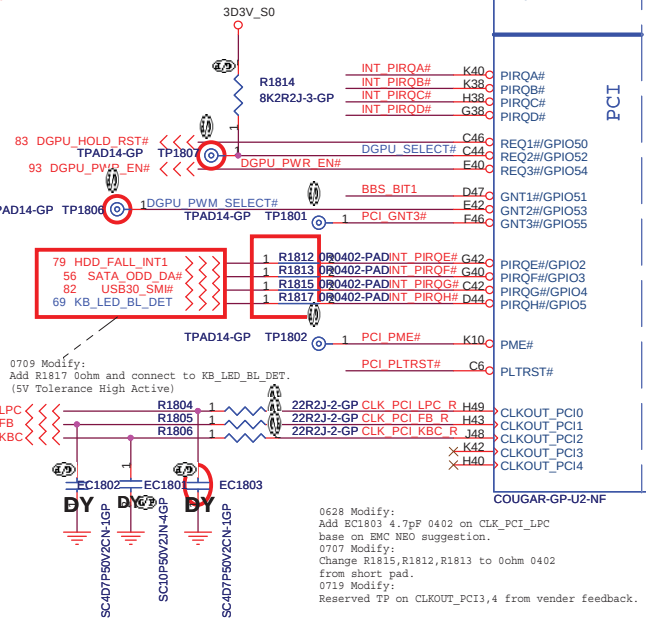


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



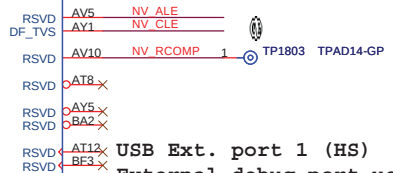


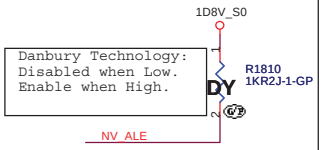
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



0709 Modify:
Add R1817 0ohm and connect to KB_LED_BL_DET.
(5V Tolerance High Active)

0628 Modify:
Add EC1803 4.7pF 0402 on CLK_PCI_LPC base on EMC NEO suggestion.
0707 Modify:
Change R1815,R1812,R1813 to 0ohm 0402 from short pad.
0719 Modify:
Reserved TP on CLKOUT_PCI3,4 from vender feedback.



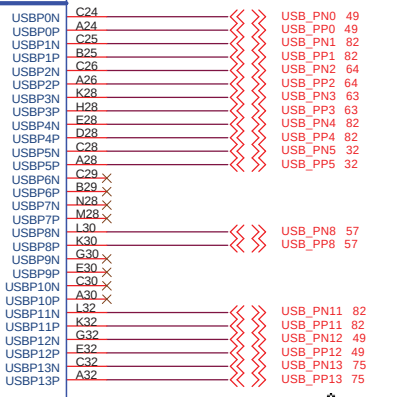


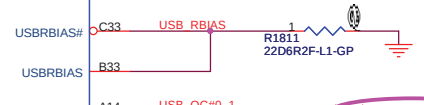
Danbury Technology:
Disabled when Low. Enable when High.

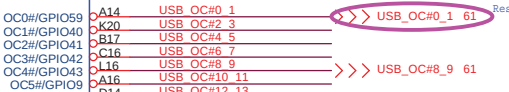
USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card







1120 X02 Modify:
Reserved USB_OC#0_1 connect from PCH GPIO59.

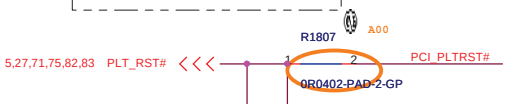
USB_OC#0_1 61
USB_OC#8_9 61

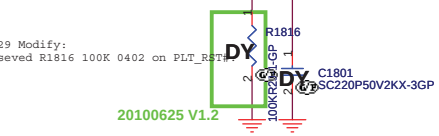
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

0617 Modify:
Joseph Remove PLT_RST AND gate logic IC U1801/C1802.



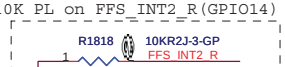


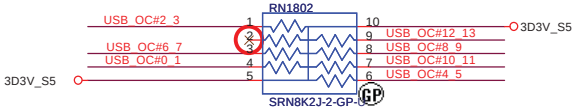
0629 Modify:
Reseved R1816 100K 0402 on PLT_RST#

20100625 V1.2

KBC CLK EMI

0908 X01 Modify:
Add R1818 10K_PL on FFS_INT2_R(GPIO14)





Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 18 of 108

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — Cougar Point — 3 OF 10

DMI: DMI_RXN[3:0], DMI_RXP[3:0], DMI_TXN[3:0], DMI_TXP[3:0]
FDI: FDI_TXN[7:0], FDI_TXP[7:0]

DMI_ZCOMP — R1901 49D9R2F-GP
DMI_IRCOMP — R1902 750R2F-GP
DMI2RBIAS — RBIAS_CPY

20100628 V1.3

0628 Modify:
Change R1904 to 100K 0402 from 10K and default stuff.
0629 Modify:
R1926 connect to SYS_PWROK.
0707 Modify:
Change R1903 change to 0ohm 0402 from short pad.

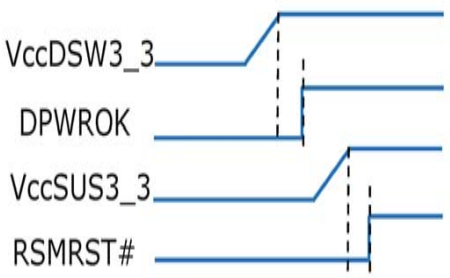
SUS_PWR_ACK — R1903 0R0402-PAD — SUSACK#
0707 Modify:
stuff R1925 and un-stuff R1905.
XDP_DBRESET# — R1925 0R0402-PAD — SYS_RESET#
3D3V_S0 — R1905 10KR2J-3-GP
SYS_PWROK — R1926 DY — SYS_PWROK
R1923 0R2J-2-GP
S0_PWR_GOOD — R1924 0R0402-PAD — PWROK
RUNPWROK — R1907 DY 0R2J-2-GP — R1906 0R0402-PAD — APWROK
PM_DRAM_PWRGD — DRAMPWROK
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms
PM_RSMRST# — RSMRST#
SUS_PWR_ACK — SUSWARN#/SUSPWRDNACK/GPIO30
PM_PWRBTN# — PWRBTN#
AC_PRESENT — ACPRESENT/GPIO31
BATLOW# — BATLOW#/GPIO72
PM_RI# — RI#

DSWVRMEN — A18 — DSWODVREN
DPWROK — F22 — PCH_DPWROK — R1910 0R0402-PAD PM_RSMRST# — R1911 10KR2J-3-GP DY — RTC_AUX_S5
WAKE# — B9 — PCH_WAKE# 27
CLKRUN#/GPIO32 — N3 — PM_CLKRUN# 27
SUS_STAT#/GPIO61 — G8 — PM_SUS_STAT# — TP1901 TPAD14-GP
SUSCLK/GPIO62 — N14 — SUS_CLK — R1913 0R0402-PAD — PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 — D10 — PM_SLP_S5# — TP1902 TPAD14-GP
SLP_S4# — H4 — PM_SLP_S4# 27,46,75
SLP_S3# — F4 — PM_SLP_S3# 27,36,37,47,75
SLP_A# — G10 — PM_SLP_A# — TP1903 TPAD14-GP
SLP_SUS# — G16 — PM_SLP_SUS# — TP1904 TPAD14-GP
PMSYNCH — AP14 — H_PM_SYNC — H_PM_SYNC 5
SLP_LAN#/GPIO29 — K14 — PM_SLP_LAN# — TP1905 TPAD14-GP

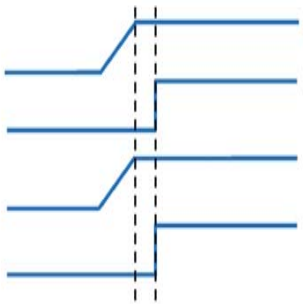
FDI_INT — AW16 — FDI_INT 4
FDI_FSYNC0 — AV12 — FDI_FSYNC0 4
FDI_FSYNC1 — BC10 — FDI_FSYNC1 4
FDI_LSYNC0 — AV14 — FDI_LSYNC0 4
FDI_LSYNC1 — BB10 — FDI_LSYNC1 4

COUGAR-GP-U2-NF

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as ¡¥no connect¡¦
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 DY 330KR2J-L1-GP

3D3V_S5 — RN1901 (0907 X01 SWAP RN1901) — SRN10KJ-6-GP
BATLOW# — PM_RI# — PCH_WAKE# — SUS_PWR_ACK

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

AC_PRESENT — R1909 100KR2J-1-GP
0920 X01 Modify:
move PCH_WAKE# to RN1901 pin4
Add R1909 PH on AC_PRESENT.
R1922 10KR2J-3-GP PM_PWRBTN#
R1920 10KR2J-3-GP PM_SLP_LAN#
DY DY

0621 Modify:
Joseph removed Q1901/R1909/R1916 3V_5V_POK and PM_RSMRST# related control circuit.

PM_RSMRST# — R1912 0R0402-PAD — RSMRST#_KBC 27

PCH_SUSCLK_KBC — EC1901 DY — SC4D7P50V2CN-1GP
0625 Modify:
Reserved EC1901 on PCH_SUSCLK_KBC for EMC NEO suggestion.

3D3V_S0 — PM_CLKRUN# — R1919 8K2R2J-3-GP

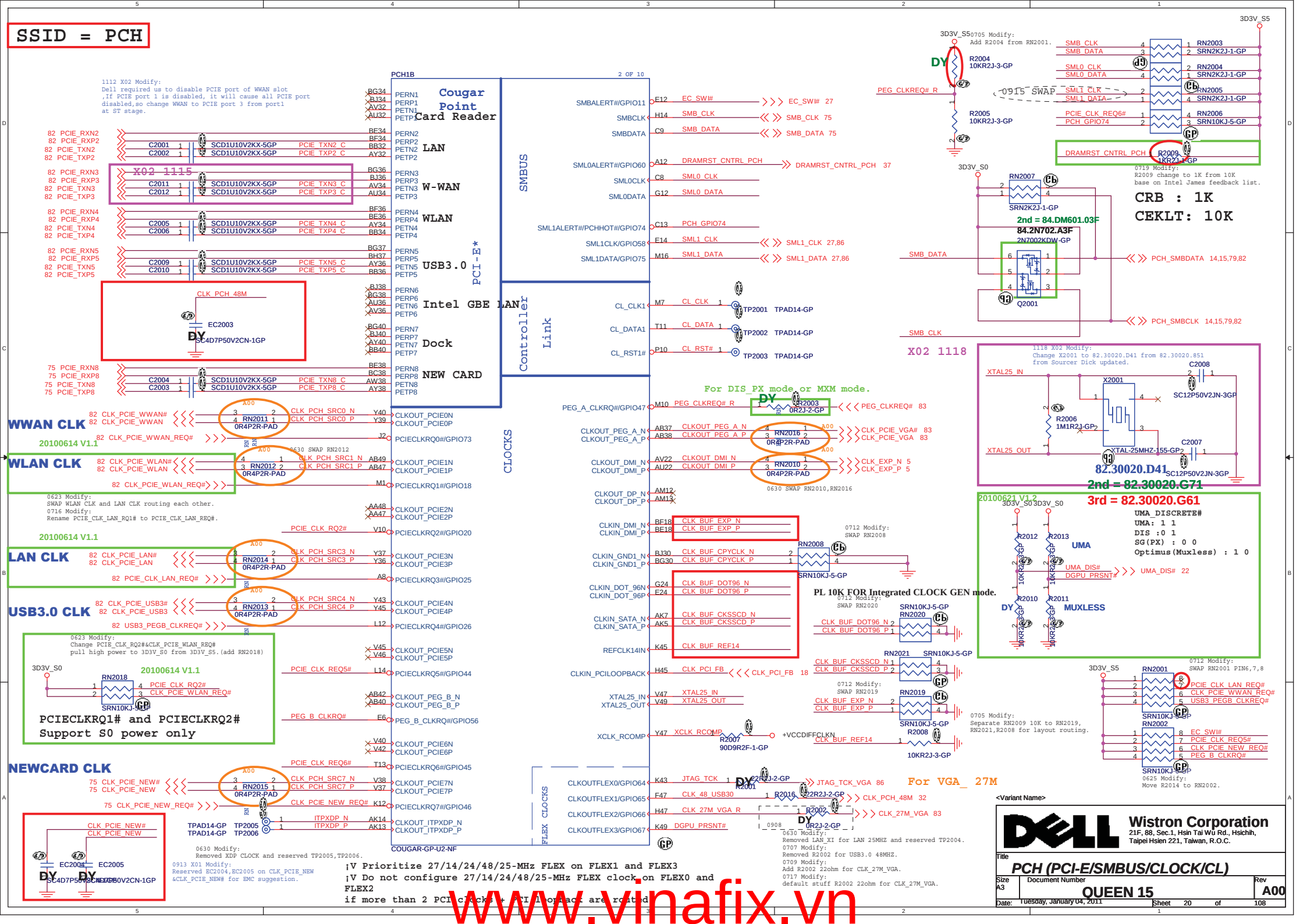
R1908 10KR2J-3-GP — PM_RSMRST#
0719 Modify:
Change R1908 to 10K ohm based on Intel review:
8.2K to 10K pull-down is recommended.

<Variant Name>

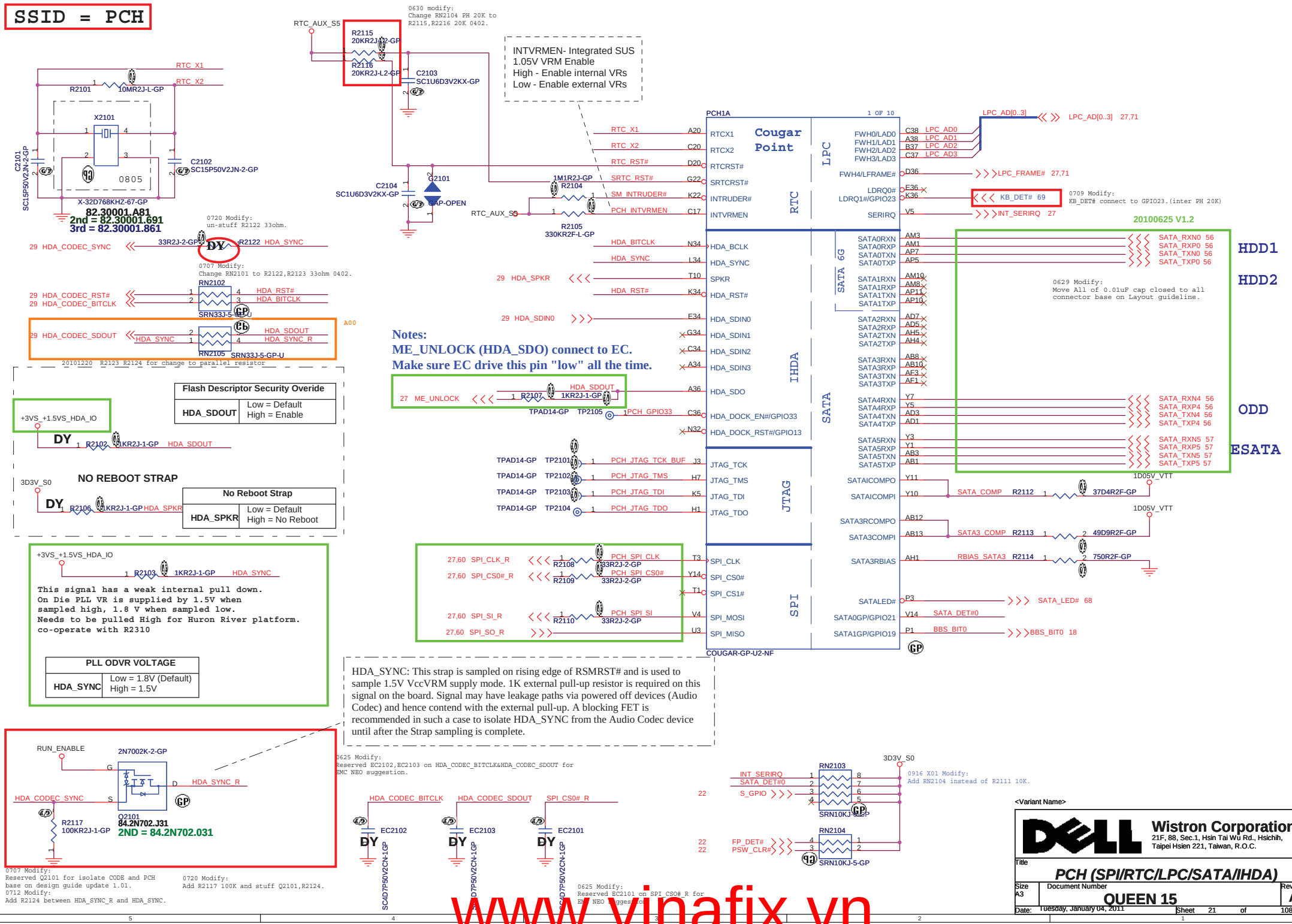
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 19 of 108

SSID = PCH



SSID = PCH



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 21 of 108

SSID = PCH

0719 Modify:
Change R2202 to 100K from 200K.

3D3V_S0 — R2202 — 100KR2J-1-GP — SATA_ODD_PRSNT#

0629 Modify:
20100625 V1.2

Note:
For PCH debug with XDP, need to NO STUFF R2218

	GSENSOR_ST	GSENSOR_ADI
R2205	DY	10K
R2206	100K	DY

0712 Modify: Stuff R2202 200K 0402 1%(ANNIE updated)
SWAP RN2203

3D3V_S0 — RN2203 — H_A20GATE — H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

1120 X02 Modify:
Rename PCH_GPIO12 to RTC_DET# on GPIO12.

0908 X01 Modify:
change FFS_INT2_R from PCH GPIO48 to GPIO14
Keep PCH_GPIO5 PH R2201,PCH_GPIO48 PH R2220

3D3V_S0 — R2220 — 10KR2J-3-GP — PCH_GPIO48

0720 Modify:
Removed DBC_EN on GPIO22.

0709 Modify:
Rename PCH_GPIO22 to DBC_EN.
Rename PCH_GPIO24 to 3G_EN.

0701 Modify:
Separate PCH_TEMP_ALERT# from RN2201 to R2222 10K base on layout limitation.

3D3V_S0 — R2222 — 10KR2J-3-GP — PCH_TEMP_ALERT#
R2223 — 10KR2J-3-GP — MFG_MODE

0701 Modify:
Separate MFG_MODE from RN2202 to R2223 10K base on layout limitation.

RN2201 — EC_SMI# — EC_SCI# — DGPU_HPD_INTR# — DBC_EN — SRN10KJ-5-GP
0923 SWAP

0916 X01 Modify:
Move EC_SCI#,DBC_EN to RN2201.
Move S_GPIO to RN2103.
Move PSW_CLR# to RN2104.

1118 X02 Modify:
Rename GFX_CRB_DET to GSENSOR_DET on GPIO39.

1118 X02 Modify:
Rename USB3_PWR_ON to PCH_GPIO57.
1120 X02 Modify:
Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57.

1120 X02 Modify:
Rename PCH_GPIO12 to RTC_DET# on GPIO12.

3D3V_S5 — RN2204 — RTC_DET# — USB2_CRT_ON# — SRN10KJ-5-GP
PCH_GPIO15 — R2201 — 1KR2J-1-GP
3G_EN — R2221 — 10KR2J-3-GP

20100625 V1.2

0629 Modify:
Add R2221 10K 0402 on PCH_GPIO24(ANNIE updated)
0709 Modify:
Rename PCH_GPIO24 to 3G_EN on R2221.

PCH1F — 6 OF 10 — Cougar Point — COUGAR-GP-U2-NF

GPIO:
- 21 S_GPIO — R2218 100R2J-2-GP — GPIO0 — T7
- 27 EC_SMI# — A42
- DGPU_HPD_INTR# — H36
- 27 EC_SCI# — E38
- ICC_EN# — C10
- 60 RTC_DET# — C4
- PCH_GPIO15 — G2
- 56 SATA_ODD_PRSNT# — R2213 0R0402-PAD — PCH_GPIO16 — U2
- 83,92,93 DGPU_PWROK — D40
- TPAD14-GP TP2210 — DBC_EN — T5
- 82 3G_EN — E8
- TPAD14-GP TP2203 — PCH_GPIO27 — E16
- PLL_ODVR_EN — P8
- PSW_CLR# — K1
- 21 FP_DET# — K4
- DMI_OVRVLTG — V8
- FDI_OVRVLTG — M5
- MFG_MODE — N2
- GSENSOR_DET — M3
- PCH_GPIO48 — V13
- PCH_TEMP_ALERT# — V3
- 61 USB2_CRT_ON# — D6

GAP-OPEN — G2201

GPIO: BMBUSY#/GPIO0, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, GPIO15, SATA4GP/GPIO16, TACH0/GPIO17, SCLOCK/GPIO22, GPIO24/MEM_LED, GPIO27, GPIO28, STP_PCI#/GPIO34, GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SATA5GP/GPIO49, GPIO57

CPU/MISC: TACH4/GPIO68, TACH5/GPIO69, TACH6/GPIO70, TACH7/GPIO71, A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#

- C40 — SATA_ODD_PWRGT 56
- B41 UMA_DIS# — UMA_DIS# 20
- C41 VRAM_SIZE1 — TP2204 TPAD14-GP
- A40 VRAM_SIZE2 — TP2205 TPAD14-GP
- P4 — H_A20GATE 27
- AU16 H_PECI_R — DY R2203 0R2J-2-GP — H_PECI 5,27
- P5 — H_RCIN# 27
- AY11 — H_CPUPWRGD 5,36
- AY10 PCH_THERMTRIP_R — R2204 390R2J-1-GP — H_THERMTRIP# 5,36
- T14 INIT3_3V# — TP2201 TPAD14-GP

TS_VSS1, TS_VSS2, TS_VSS3, TS_VSS4, NC_1 — AH8, AK11, AH10, AK10 TS_VSS — R2219 0R0402-PAD

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

0707 Modify:
Change R2219 change to 0ohm 0402 from short pad.

NCTF: NCTF_VSS#BG2, NCTF_VSS#BG48, NCTF_VSS#BH3, NCTF_VSS#BH47, NCTF_VSS#BJ4, NCTF_VSS#BJ44, NCTF_VSS#BJ45, NCTF_VSS#BJ46, NCTF_VSS#BJ5, NCTF_VSS#BJ6, NCTF_VSS#C2, NCTF_VSS#C48, NCTF_VSS#D1, NCTF_VSS#D49, NCTF_VSS#E1, NCTF_VSS#E49, NCTF_VSS#F1, NCTF_VSS#F49

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49; BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48; D1, D49, E1, E49, F1, F49

TPAD14-GP TP2206 — PCH_NCTF_1 — A4
0714 Modify:
Add TP2206~TP2209 on PCH NCTF pin.
TPAD14-GP TP2207 — PCH_NCTF_2 — BE1
TPAD14-GP TP2208 — PCH_NCTF_3 — BE49
TPAD14-GP TP2209 — PCH_NCTF_4 — BF49

3D3V_S0 — R2207 10KR2J-3-GP — DY — FDI_OVRVLTG
R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP — DY — DMI_OVRVLTG
R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

0705 Modify:
Removed R2214-R2217 10K 0402 on VRAM_SIZE1&2.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

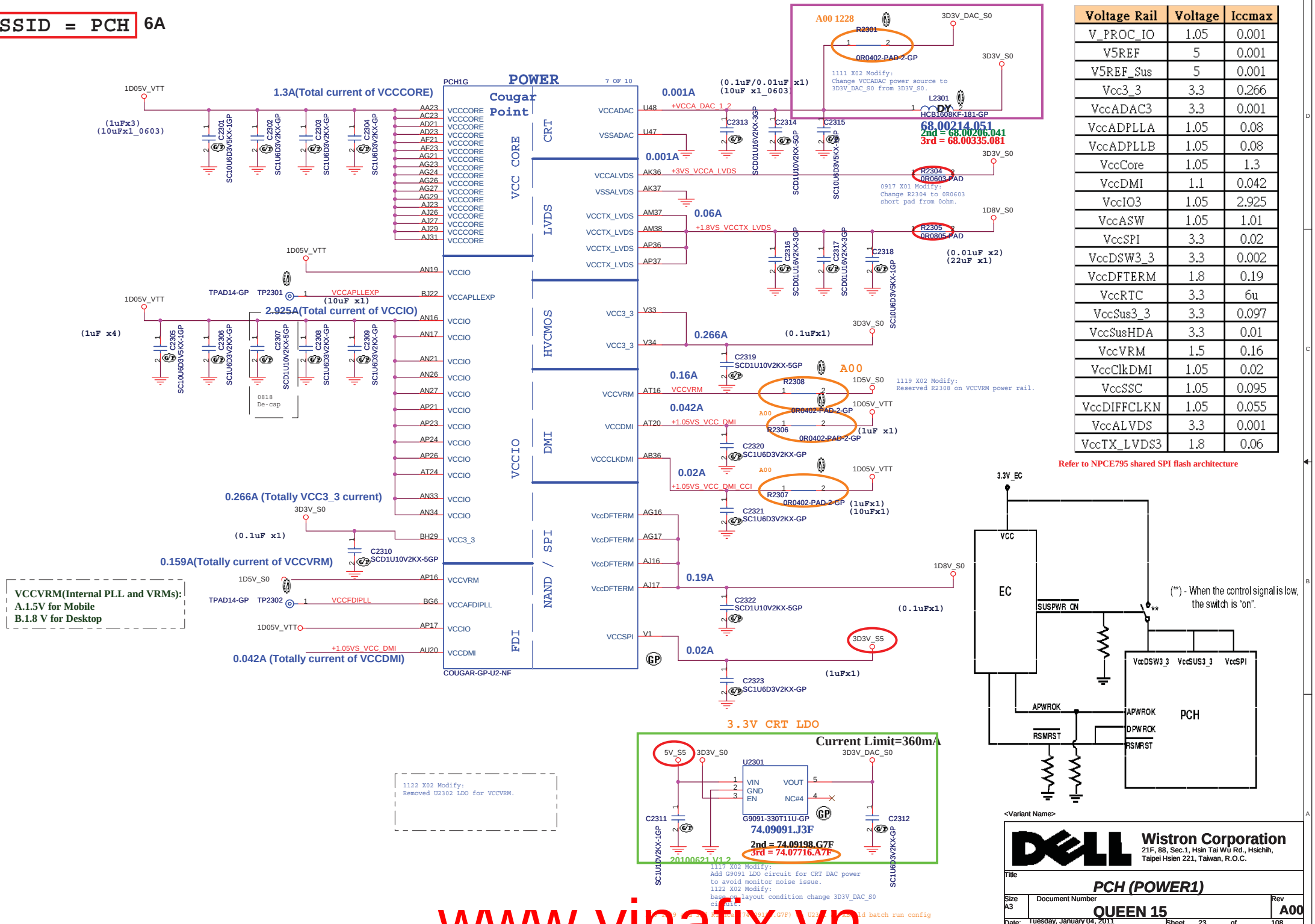
PLL_ODVR_EN — DY 1 R2212 1KR2J-1-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 22 of 108

SSID = PCH 6A



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 23 of 108

SSID = PCH

POWER

PCH1J

10 OF 10

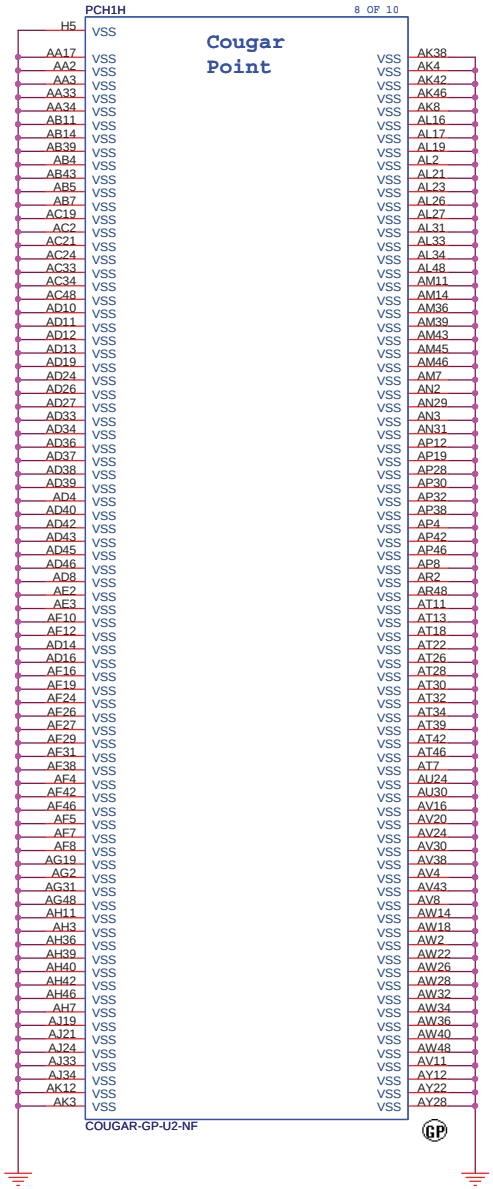
Cougar Point

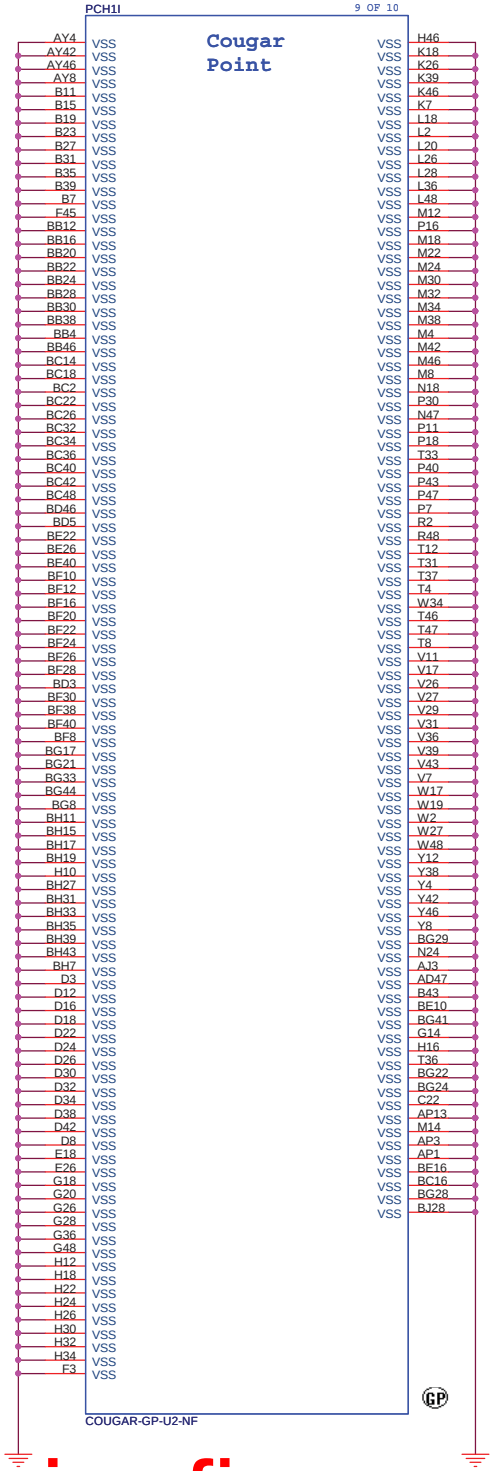
Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 24 of 108

SSID = PCH





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 25 of 108

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 26 of 108

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMA	100.0K	10.0K	3.0V
DQ15_ATI	100.0K	20.0K	2.75V
DQ15_NVIDIA	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K	2.24V
DN15_ATI	100.0K	64.9K	2.0V
DQ13_UMA	100.0K	76.8K	1.87V
DQ13_ATI	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.358V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V

215K=64.21535.6DL

NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.

Notes:
The total SPI interface signal between EC and PCH can¡¦t not exceed 6500mil. The mismatch between SPI signal must be within 500mil

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

C2712 Need very close to EC

Need very close to EC

NOTE:
Locate resistors R2736,R2719 and R2722 close to the NPCE795P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

ROSA Multi GPIO setting

EC_GPIO47 High Active

PSL SOLUTION

10mW SOLUTION

VBACKUP

PSL_IN1

PSL_OUT

EC GPIO standard PH/PL

MEDIA BUTTON CONTROL

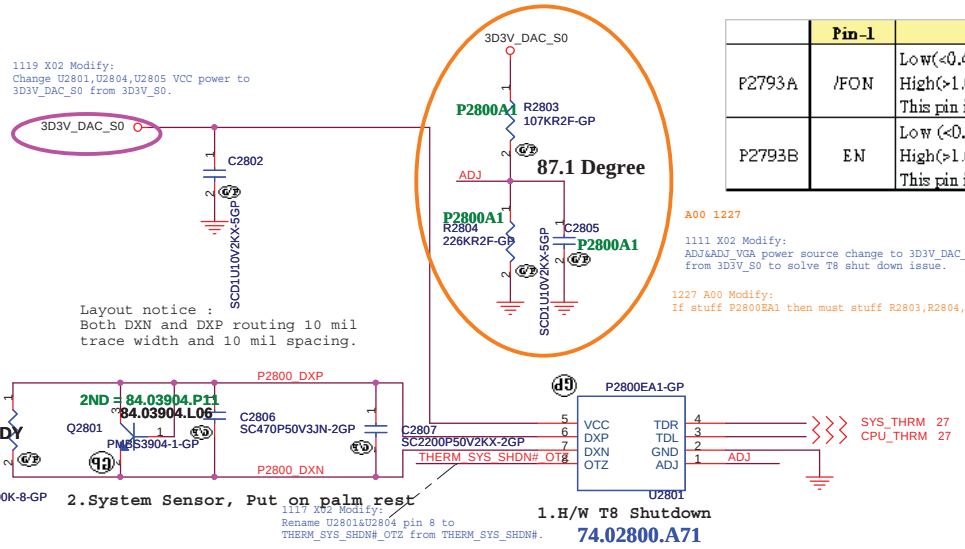
NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795
Size: A2 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 27 of 108

SSID = Thermal

Thermal sensor P2800



	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low (<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

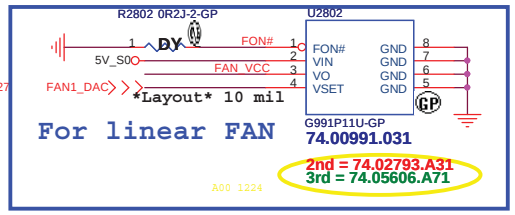
A00 1227

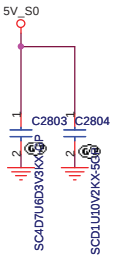
1111 X02 Modify:
ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.

1227 A00 Modify:
If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.

0705 Modify:
R2802 change to 0ohm 0402 from short pad and default un-stuff.

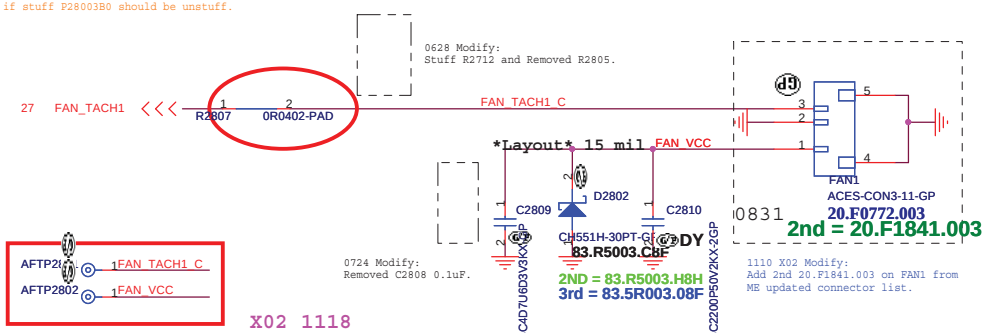
Fan controller P2793





0614 Modify:
Change FAN1 connector part number to 20.D0210.103 base on ME EMN and DXF.
0712 Modify:
Change FAN1 part number to 20.F1639.004 from 20.D0210.103 base on latest EMN and DXF.

0628 Modify:
Stuff R2712 and Removed R2805.



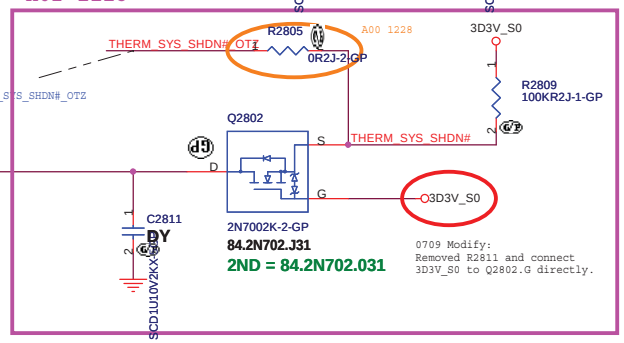
0724 Modify:
Removed C2808 0.1uF.

1110 X02 Modify:
Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.

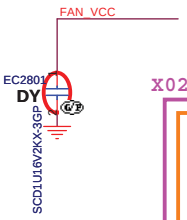
ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

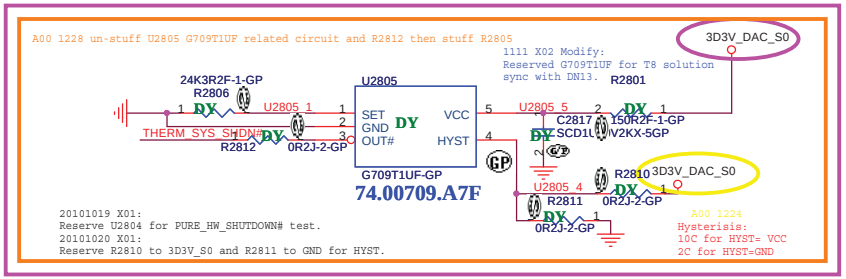
X02 1118



EMI/ESD



X02 1111



A00 1228 Cancel VGA Thermal sensor P2800 circuit

1111 X02 Modify:
ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 28 of 108

SSID = AUDIO

For EMI

AUD_DMIC_CLK
AUD_DMIC_IN0
EC2901
EC2902
SC22P50V2JN-4GP
SC22P50V2JN-4GP

1122 X02 Modify:
change R2920,R2921 to 22ohm from 0ohm and
stuff EC2901,EC2902 22p from EMC Neo updated.

Close to codec
AUD_DVDDCORE
C2901
SC10U6D3V5MX-3GP

27 AMP_MUTE#
AMP_MUTE#
+PVDD
+AVDD
AUD_SPK_R+
AUD_SPK_R-
AUD_SPK_L-
AUD_SPK_L+
AUD_SPK_R+ 58
AUD_SPK_R- 58
AUD_SPK_L- 58
AUD_SPK_L+ 58

+AVDD
C2905 SCD1U10V2KX-5GP
C2906 SC1U10V2KX-1GP
R2902 0R0603-PAD
5V_S0

+PVDD
C2908 SCD1U10V2KX-5GP
C2909 SC1U10V2KX-1GP
C2910 SC10U6D3V5MX-3GP
R2903 0R0603-PAD
R2904 0R0603-PAD
5V_S0

U2901
71.92H87.A03
92HD87B1A5NDGXTBX8-GP

THERMAL_PAD 41
EAPD 40
PVDD 39
PORTD_R 38
PORTD_-R 37
PVSS 36
PORTD_-L 35
PORTD_+L 34
PVDD 33
AVDD2 32
VREG/+2.5V 31
AUD_VREG

1 DVDD_LV
2 DMIC_CLK/GPIO_1
3 DMIC_0/GPIO_2
4 SDATA_OUT
5 BITCLK
6 SDATA_IN
7 DVDD
8 SYNC
9 RESET#
10 PCBEEP

30 CAP+
29 CAP-
28 V-
27 AVSS2
26 PORTB_R
25 PORTB_L
24 AVSS2
23 PORTA_R
22 PORTA_L
21 AVDD1

PUMP_CAPP
C2914 SC2D2U10V3KX-1GP
CLOSE TO CODEC
PUMP_CAPN
AUD_V_B
AUD_HP1_JACK_R
AUD_HP1_JACK_L
AUD_EXT_MIC_R
AUD_EXT_MIC_L
+AVDD

R2906 60D4R2F-GP
R2905 60D4R2F-GP
C2922 SC1U10V3KX-3GP
C2921 SC1U10V3KX-3GP
AUD_HP1_JACK_R2 82
AUD_HP1_JACK_L2 82
MIC_IN_R 82
MIC_IN_L 82
Put C2921 and C2922 close to codec

SENSE_A 11
SENSE_B 12
PORTF_L 13
PORTF_R 14
PORTC_R 15
PORTC_L 16
VREFFILT 17
CAP2 18
VREFOUT_A 19
VREFOUT_C 20

AUD_SENSE_A
AUD_SENSE_B
AUD_PC_BEEP
AUD_VREFFLT
AUD_CAP2
AUD_VREFOUT_B

3D3V_S0
Close to codec
C2903 SC1U6D3V2KX-GP
C2904 SCD1U10V2KX-5GP
C2902 SCD1U10V2KX-5GP

21 HDA_CODEC_SDOUT
21 HDA_CODEC_BITCLK
21 HDA_SDIN0
21 HDA_CODEC_SYNC
21 HDA_CODEC_RST#
R2901 33R2J-2-GP
HDA_CODEC_SDOUT
HDA_CODEC_BITCLK
HDA_CODEC_SDIN0
HDA_CODEC_SYNC
HDA_CODEC_RST#
AUD_PC_BEEP

0707 Modify:
updated U2901 part number from data base.

2010/06/30 Change to 92HD87 (71.92H87.A03)

A00
RN2902 SRN22J-7-GP
49 AUD_DMIC_IN0
49 AUD_DMIC_CLK
AUD_DMIC_IN0_R
AUD_DMIC_CLK_R
20101220 R2920 R2921 for change to parallel resistor

0707 Modify:
Change R2911,R2914,R2917 change
to 0ohm 0603 from short pad.
0726 Modify:
Removed all of AUD_AGND and R2911,R2914,R2917.

AUD_CAP2
AUD_VREFFLT
AUD_V_B
AUD_VREG
C2917 SC4D7U6D3V3KX-GP
C2918 SC10U6D3V5MX-3GP
C2915 SC10U6D3V5MX-3GP
C2916 SC1U6D3V2KX-GP
Close to codec

3D3V_S0
R2908 10KR2J-3-GP
AMP_MUTE#
AUD_VREFOUT_B
HDA_CODEC_BITCLK
C2923 SC1U10V2KX-1GP
DY C2907 SC4D7P50V2CN-1GP

AUD_PC_BEEP
C2912 SCD1U10V2KX-5GP SB_SPKR_R
C2913 SCD1U10V2KX-5GP KBC_BEEP_R
120KR2J-L-GP R2909
R2910 470KR2J-2-GP
From SB
HDA_SPKR 21
KBC_BEEP 27
From EC

AUD_PC_BEEP
Trace width>15 mils
G2901 DUMMY-C2

0719 Modify:
Move RN2901 to closed AUDIO CODEC from speaker connector.

MIC IN
AUD_VREFOUT_B
RN2901 SRN4K7J-8-GP
82 MIC_IN_L
82 MIC_IN_R

Azalia I/F EMI
HDA_CODEC_SDOUT
R2912 47R2J-2-GP
DY
PCH AZ CODEC SDOUT1
DY C2920 SCD1U10V2KX-5GP

+AVDD
R2915 2K49R2F-GP
AUD_SENSE_A
C2919 SC1000P50V3JN-GP-U
R2913 20KR2F-L
AUD_HP1_JD# 82
R2919 39K2R2F-L-GP
EXT_MIC_JD# 82
Close to Pin13

+AVDD
R2916 2K49R2F-GP
AUD_SENSE_B
R2918 20KR2F-L-GP
Close to Pin14

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD87B1
Size: A3
Document Number: QUEEN 15
Rev: A00
Date: Tuesday, January 04, 2011
Sheet 29 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*QUEEN 15*	*A00*

Date: Tuesday, January 04, 2011 Sheet 30 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

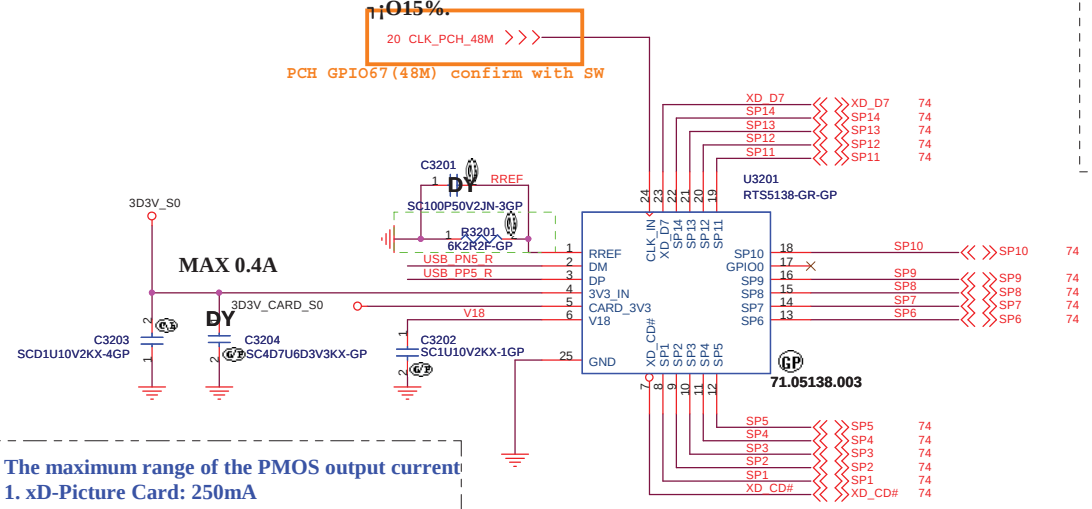
Title: *Reserved*

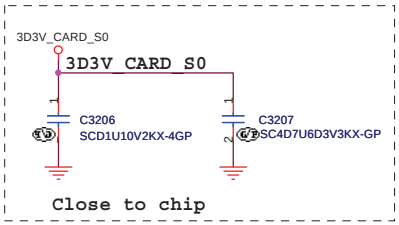
Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 31 of 108

SSID = SDIO

48MHz clock input trace of characteristic impedance (Zo) must be 50 ¡Ó15%.

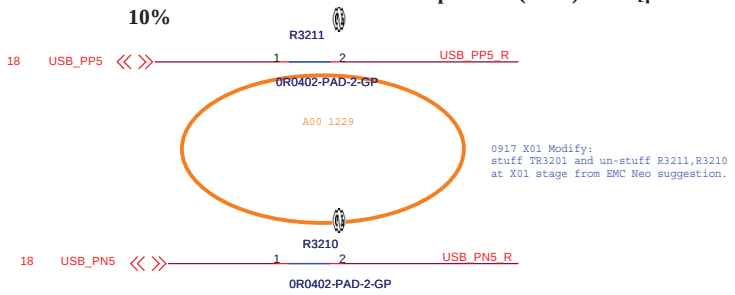




The maximum range of the PMOS output current
1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE
1.RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2.RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3.RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
Keep the trace routing lengths as short as possible.
4.RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5.RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7.It is recommended that use of ferrites bead on power trace.
8.Via size: Pad>=32 mils, Finished hole>=16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Zdiff) is 90£[¡Ó 10%



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 32 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 33 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*QUEEN 15*	*A00*

Date: Tuesday, January 04, 2011 Sheet 34 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

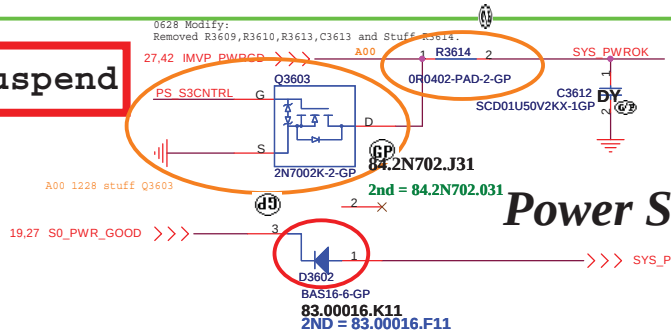
Title: *Reserved*

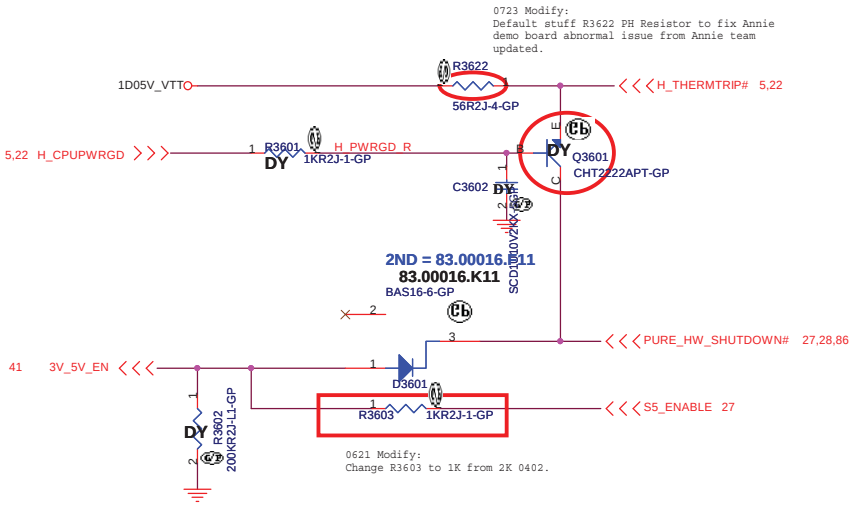
Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 35 of 108

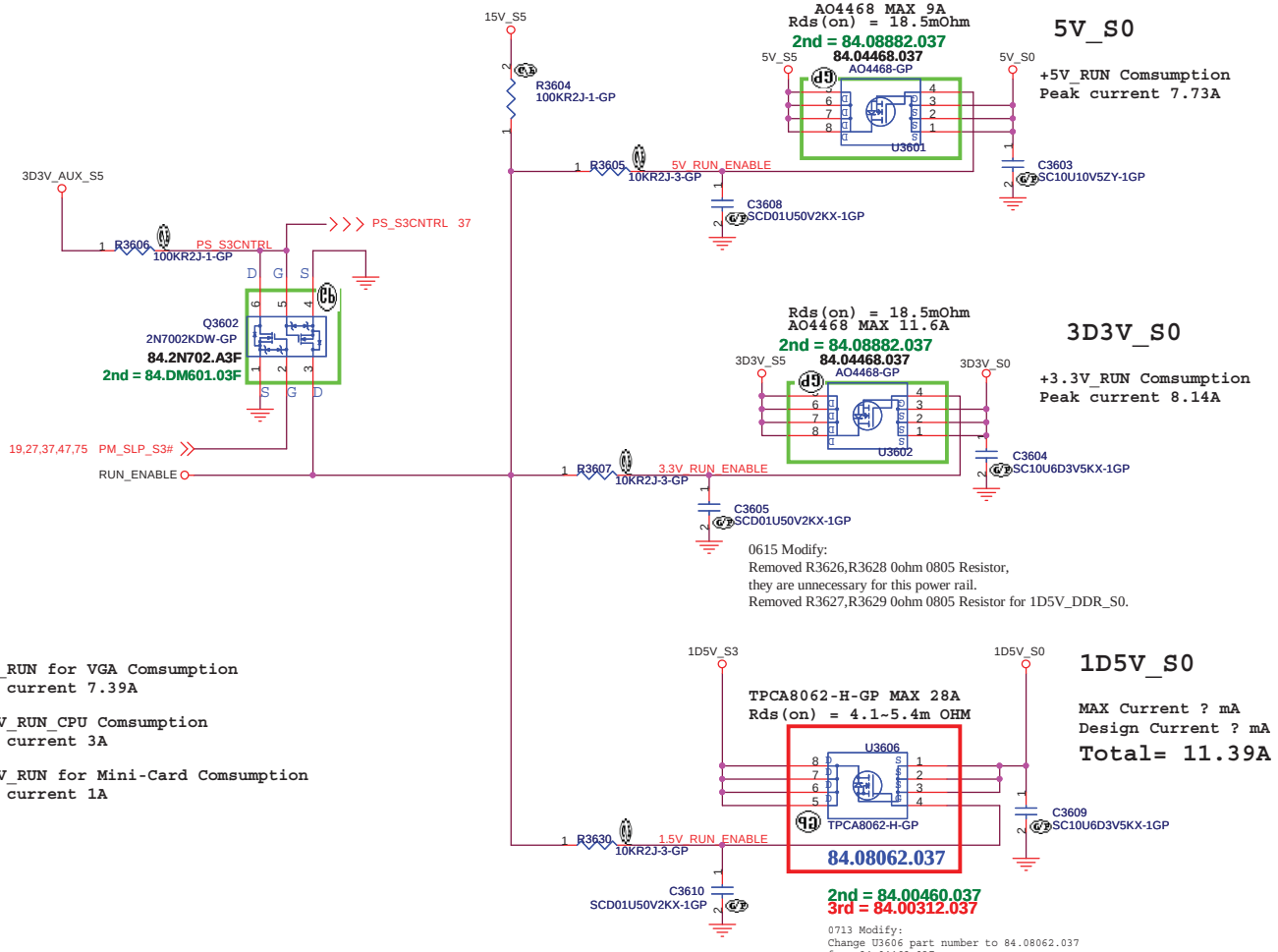
SSID = Reset.Suspend

Power Sequence





ROSA Run Power



0719 Modify:
Reserved EC3601 0.1uF near
C3604 for EMC NEO suggestion.

1.5V_RUN for VGA Comsumption
Peak current 7.39A

+1.5V_RUN_CPU Comsumption
Peak current 3A

+1.5V_RUN for Mini-Card Comsumption
Peak current 1A

<Core Design>

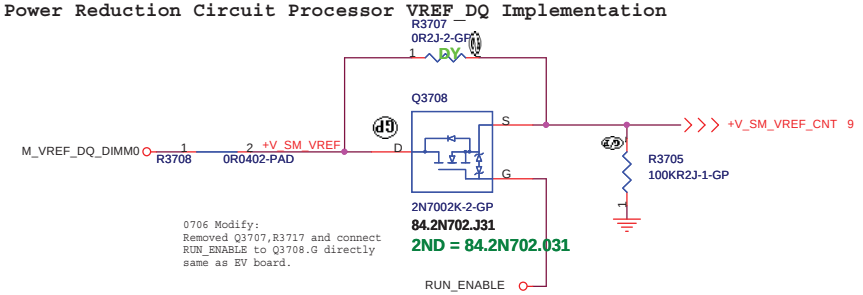
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	QUEEN 15	A00

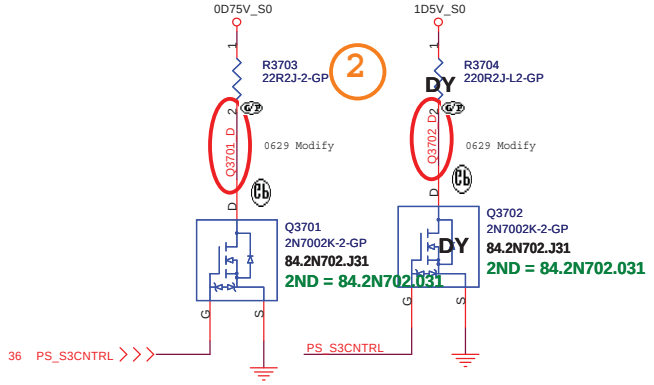
Date: Tuesday, January 04, 2011 Sheet 36 of 108

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



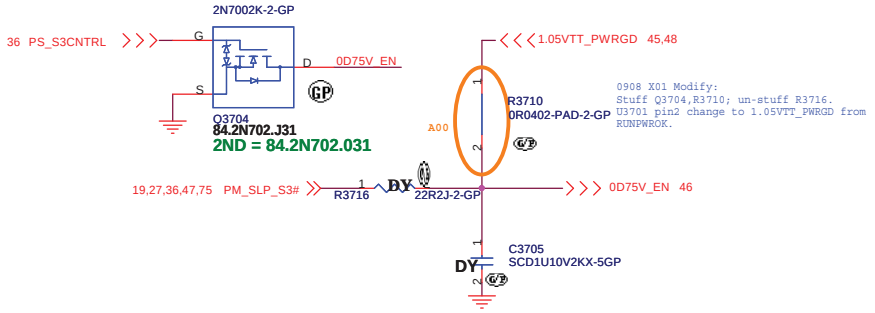
0706 Modify:
Removed Q3707,R3717 and connect RUN_ENABLE to Q3708.G directly same as EV board.

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



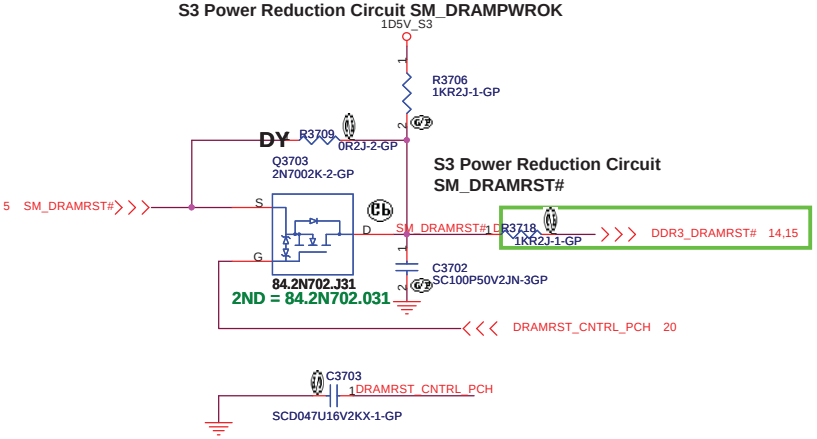
5 S3 Power Reduction X01 20091111

0730



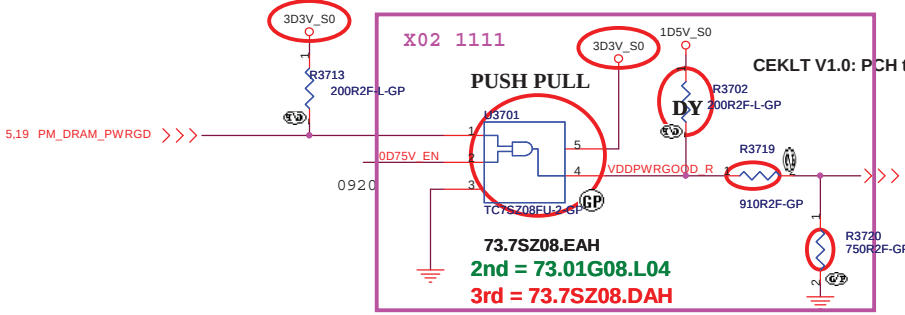
0908 X01 Modify:
Stuff Q3704,R3710; un-stuff R3716.
U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

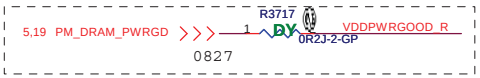


0709 Modify:
Change U3701 pin1,5 to 3D3V_S0 from 3D3V_S5.

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



1110 X02 Modify:
Change U3701 1st to 73.7SZ08.EAH;2nd to 73.01G08.L04;3rd to 73.7SZ08.DAH from Sourcer Eason updated.



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55¡Ó 200mV and the edge must be monotonic

0709 Modify:
U3701 change to OD type 73.01G09.AAH.
0723 Modify:
Change U3701 to push pull type 73.01G08.L04.
R3720 change to 910ohm 0402.
R3719 change to 750ohm 0402.
default un-stuff R3702.

DN15ATI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER
Size: A3
Document Number: QUEEN 15
Rev: A00
Date: Tuesday, January 04, 2011
Sheet 37 of 108

SSID = PWR.Support

(Blanking)

<Core Design>

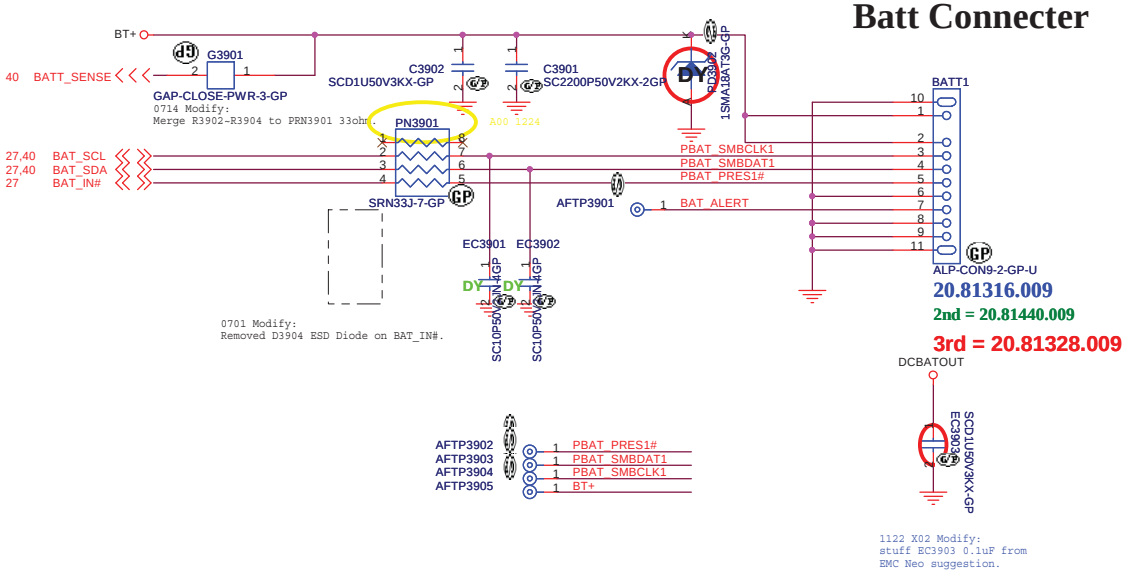
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

Size: A3 | Document Number: QUEEN 15 | Rev: A00

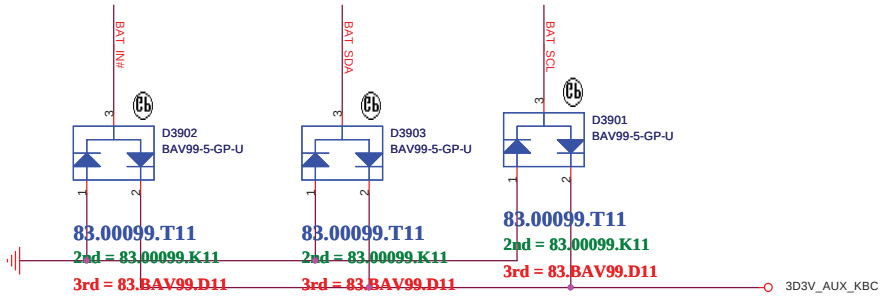
Date: Tuesday, January 04, 2011 | Sheet 38 of 108

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector

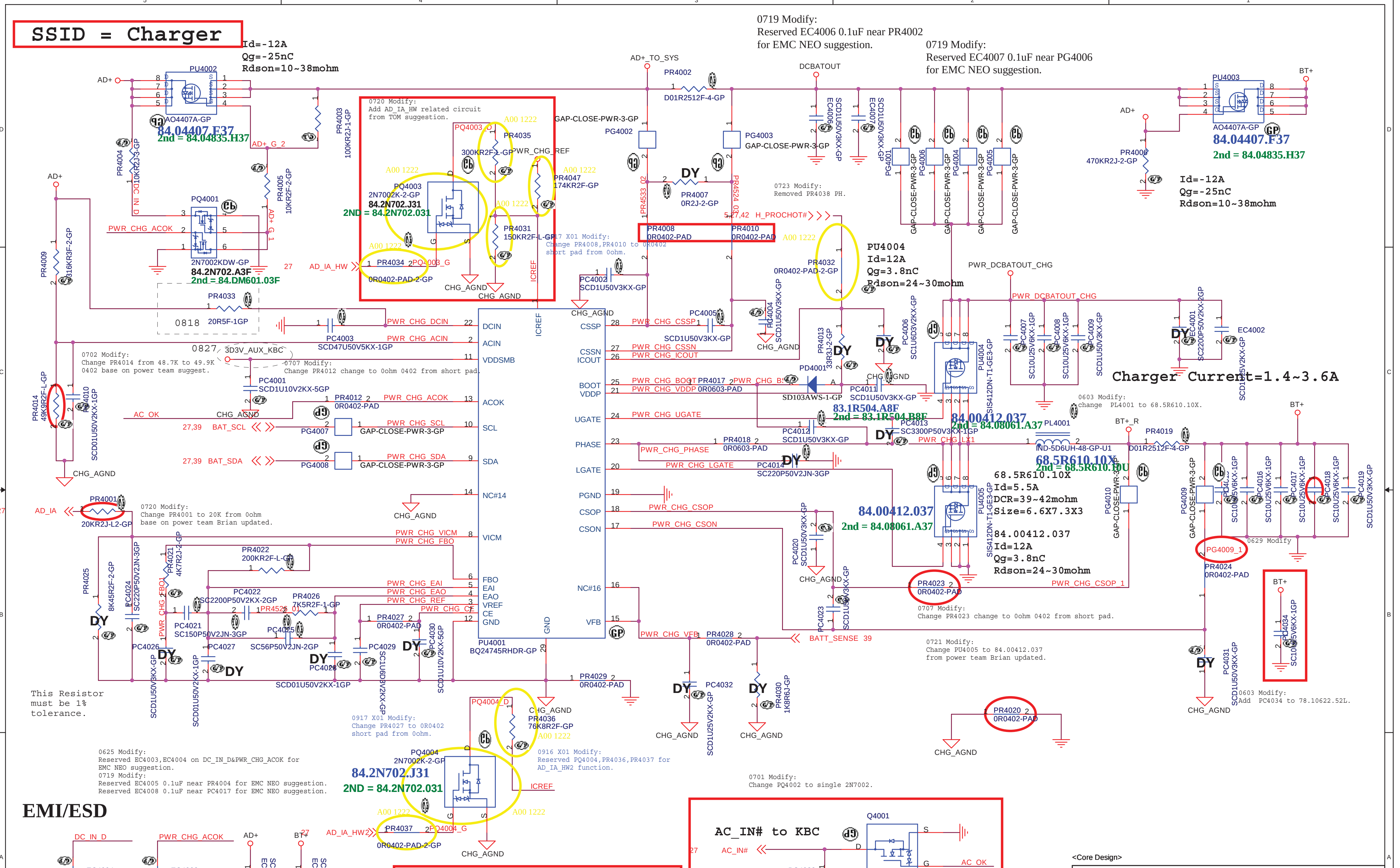


0930 X01 Modify:
Change D3901-D3903 main source to 83.00099.T11
for 83.BAV99.D11 shortage issue.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BATT CONN		
Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 39 of 108	

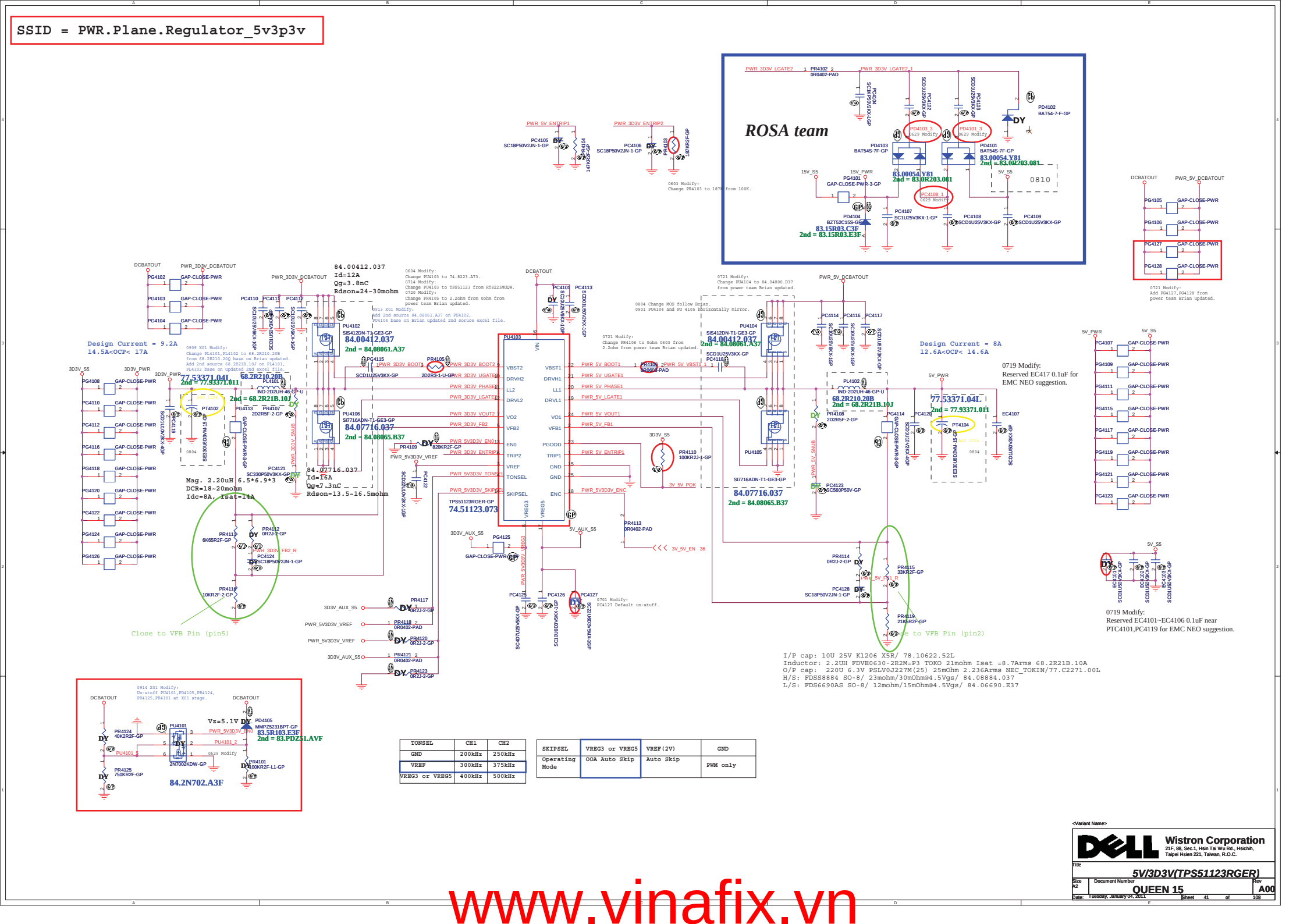


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CHARGER BQ24745		
Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 40 of 108	

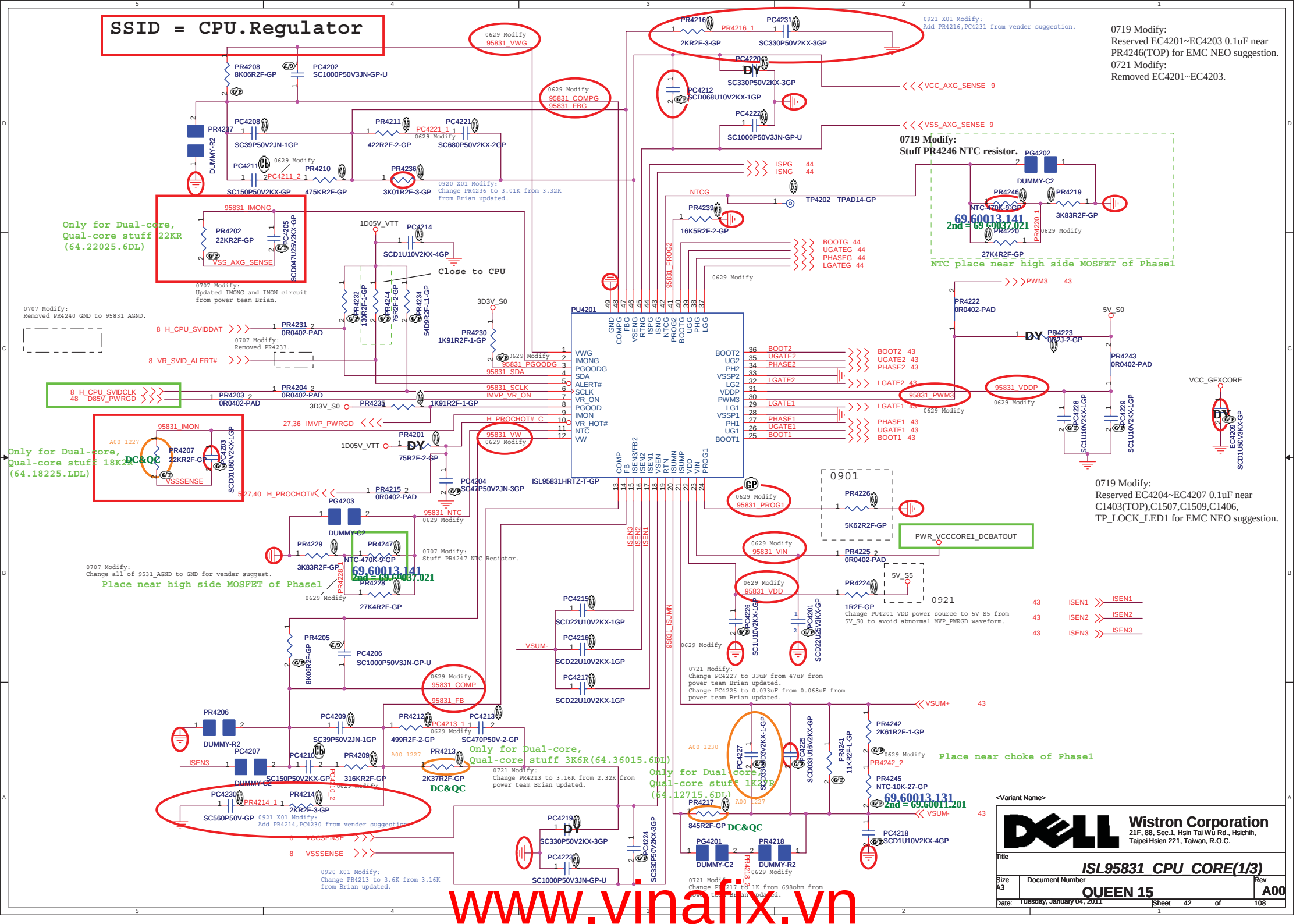
SSID = PWR.Plane.Regulator_5v3p3v



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: 5V/3D3V(TPS51123RGER)
Size: A2 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 41 of 108


SSID = CPU.Regulator
0719 Modify:
Reserved EC4201~EC4203 0.1uF near PR4246(TOP) for EMC NEO suggestion.
0721 Modify:
Removed EC4201~EC4203.
0719 Modify:
Reserved EC4204~EC4207 0.1uF near C1403(TOP),C1507,C1509,C1406, TP_LOCK_LED1 for EMC NEO suggestion.
0719 Modify:
Stuff PR4246 NTC resistor.
NTC place near high side MOSFET of Phase1
Place near high side MOSFET of Phase1
Place near choke of Phase1
Close to CPU
Only for Dual-core, Qual-core stuff 22KR (64.22025.6DL)
Only for Dual-core, Qual-core stuff 18K2R (64.18225.LDL)
Only for Dual-core, Qual-core stuff 3K6R(64.36015.6DL)
Only for Dual-core, Qual-core stuff 1K37R (64.12715.6DL)
ISL95831HRTZ-T-GP
PU4201
PWR_VCCCORE1_DCBATOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ISL95831_CPU_CORE(1/3)
QUEEN 15
Tuesday, January 04, 2011
www.vinafix.vn

84.00462.037
SIR462DP
Id=30A, Qg=8.8nC,
Rdson=7.9~10 mohm

0719 Modify:
Change PU4308 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.
0726 Modify:
Brian updatede PU4308 change to 84.00462.037.

80.3371V.A2L
330uF, 2.5V, B2
ESR=9m£[, Iripple=3.073A

68.R3610.20A
0.36uH, Idc=20A,
Isat=25A
DCR=1.4 +/-7% mohm

84.00460.037
SIR460DP
Id=40A,Qg=16.8nC,
Rdson=4.7~6.1mohm

Vcc_core
Iomax=53A
OCP>97.5A

0719 Modify:
Change PU4302 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.
0726 Modify:
Brian updatede PU4302 change to 84.00462.037.

84.00462.037
SIR462DP
Id=30A, Qg=8.8nC,
Rdson=7.9~10 mohm

84.00460.037
SIR460DP
Id=40A,Qg=16.8nC,
Rdson=4.7~6.1mohm

0719 Modify:
Change PU4305 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.
0726 Modify:
Brian updatede PU4305 change to 84.00462.037.

FOR NVIDIA VENTURA

0708 Modify:
PR4320 change to BIG SIZE footprint for CPU VENTURA.
0705 Modify:
R4346 change to PR4320 4m ohm sense Resistor from 3m ohm.

0705 Modify:
Removed R4347 sense Resistor base on VENTURA SPEC.

0705 Modify:
Add PR4321,PR4322,PC4319.

0702 Modify:
Change U4306 power source to 3D3V_VGA_S0 from 3D3V_S0.

0712 Modify:
Change VENTURA solution part number to 74.00900.079 from 74.00219.079.

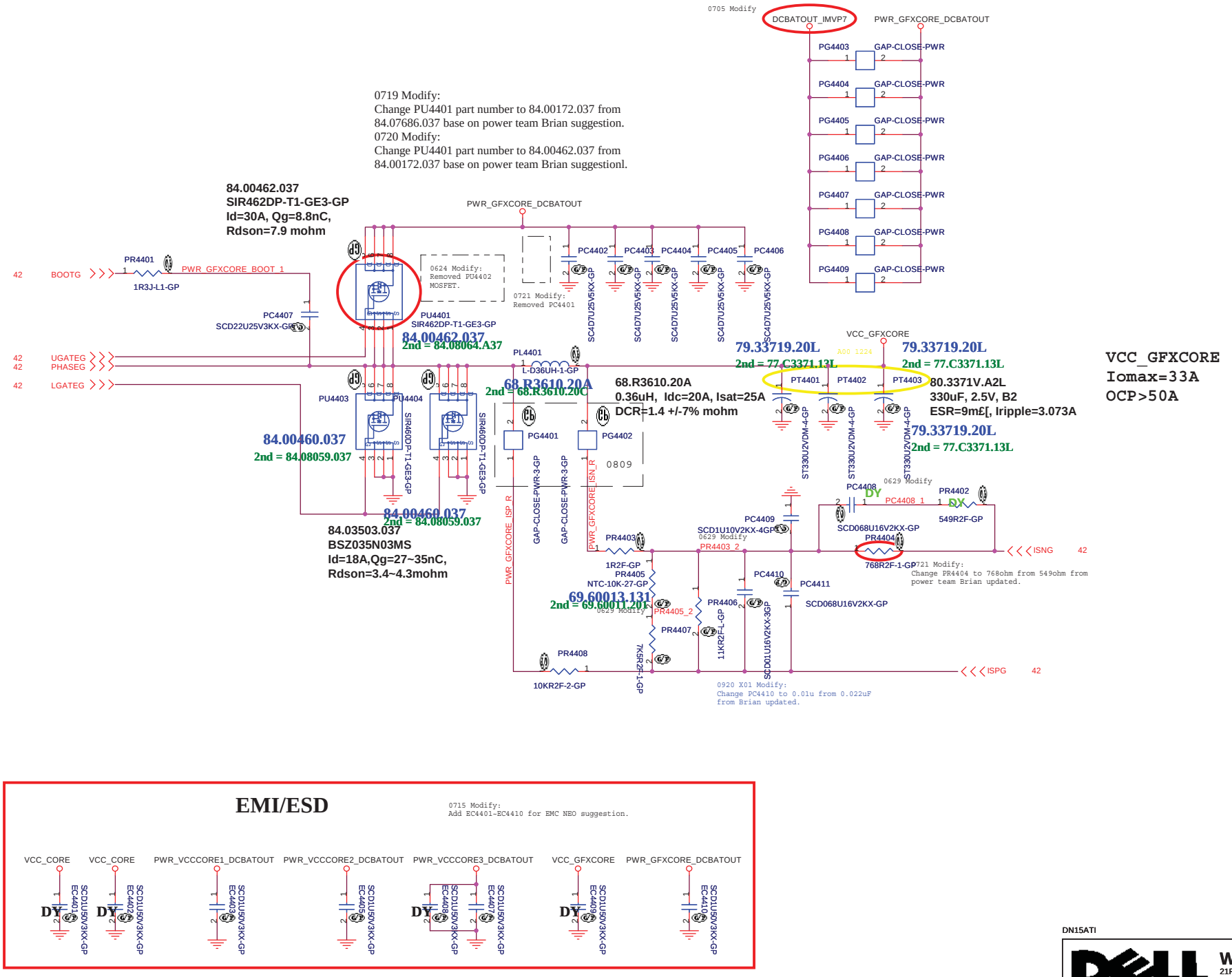
0719 Modify:
Reserved PTC4307 47uF.
0721 Modify:
Removed PTC4307.

Would be instead of INA219 by HPA00900

DN15ATI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95831_CPU_CORE (2 of 3)
Size: Custom | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 43 of 108



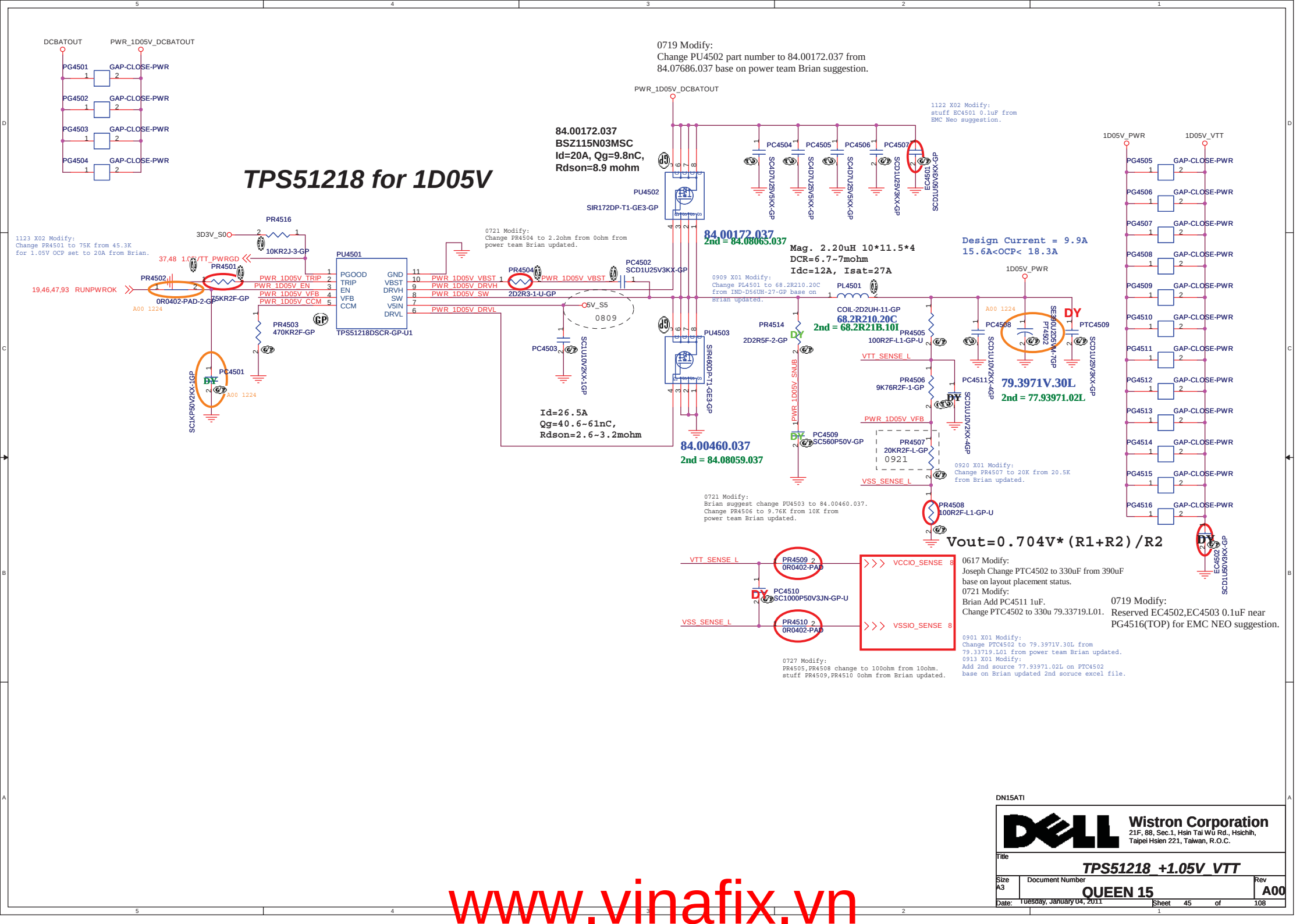
DN15ATI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95831_CPU_CORE(3/3)

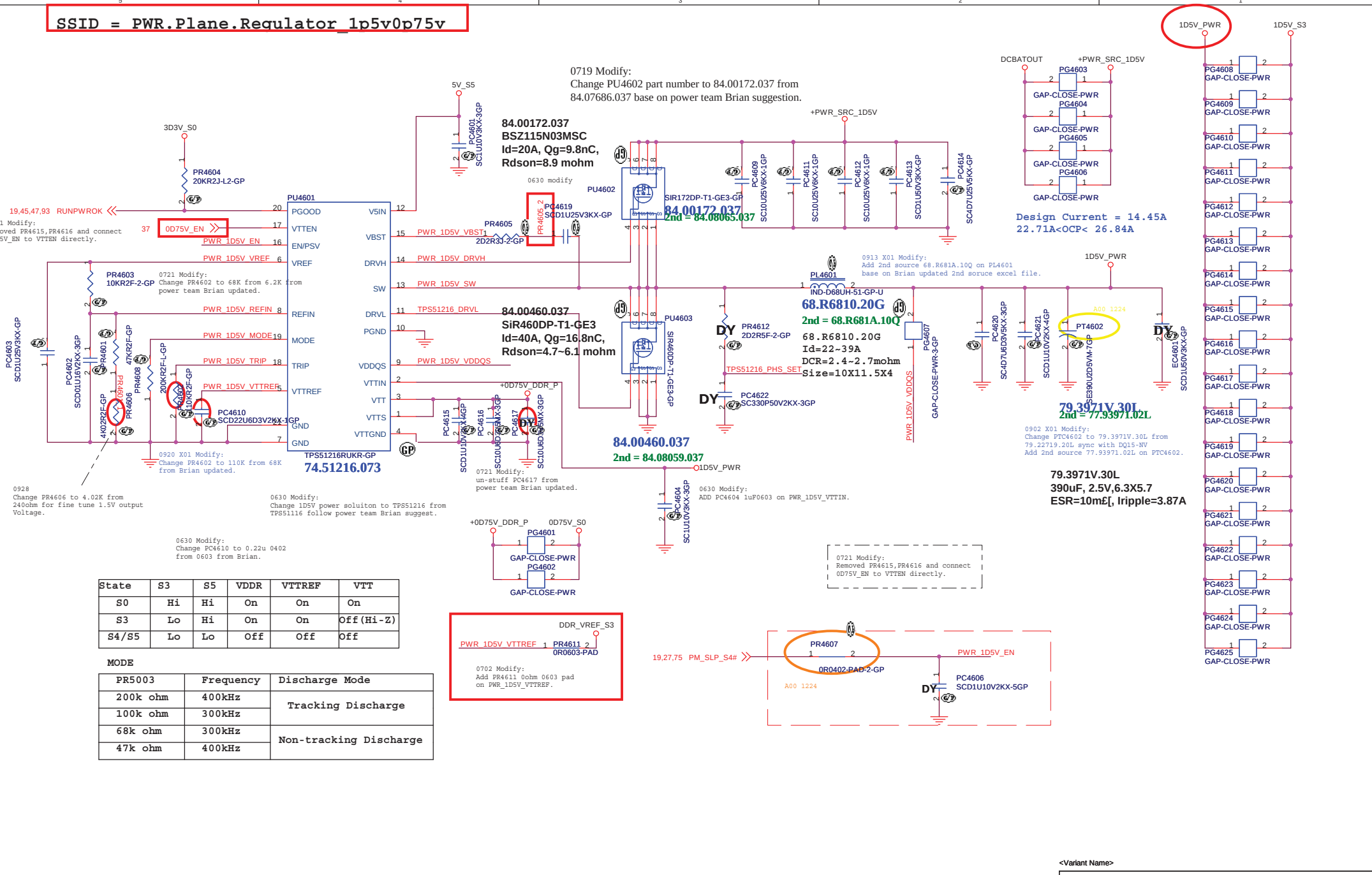
Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 44 of 108


TPS51218 for 1D05V
0719 Modify:
Change PU4502 part number to 84.00172.037 from
84.07686.037 base on power team Brian suggestion.
84.00172.037
BSZ115N03MSC
Id=20A, Qg=9.8nC,
Rdson=8.9 mohm
84.00172.037
2nd = 84.08065.037
Mag. 2.20uH 10*11.5*4
DCR=6.7~7mohm
Idc=12A, Isat=27A
Design Current = 9.9A
15.6A<OCP< 18.3A
84.00460.037
2nd = 84.08059.037
Id=26.5A
Qg=40.6~61nC,
Rdson=2.6~3.2mohm
68.2R210.20C
2nd = 68.2R21B.10I
79.3971V.30L
2nd = 77.93971.02L
Vout=0.704V*(R1+R2)/R2
0617 Modify:
Joseph Change PTC4502 to 330uF from 390uF
base on layout placement status.
0721 Modify:
Brian Add PC4511 1uF.
Change PTC4502 to 330u 79.33719.L01.
0719 Modify:
Reserved EC4502,EC4503 0.1uF near
PG4516(TOP) for EMC NEO suggestion.
DCBATOUT
PWR_1D05V_DCBATOUT
3D3V_S0
1D05V_PWR
1D05V_VTT
RUNPWROK
PU4501
PU4502
PU4503
PL4501
PR4501
PR4502
PR4503
PR4504
PR4505
PR4506
PR4507
PR4508
PR4509
PR4510
PR4514
PR4516
PC4501
PC4502
PC4503
PC4504
PC4505
PC4506
PC4507
PC4508
PC4509
PC4510
PC4511
PTC4509
EC4501
EC4502
TPS51218DSCR-GP-U1
SIR172DP-T1-GE3-GP
SIR460DP-T1-GE3-GP
COIL-2D2UH-11-GP
PWR_1D05V_TRIP
PWR_1D05V_EN
PWR_1D05V_VFB
PWR_1D05V_CCM
PWR_1D05V_VBST
PWR_1D05V_DRVH
PWR_1D05V_SW
PWR_1D05V_DRVL
VTT_SENSE_L
VSS_SENSE_L
PWR_1D05V_VFB
VCCIO_SENSE
VSSIO_SENSE
1PWR_1D05V_SNUB
0721 Modify:
Change PR4504 to 2.2ohm from 0ohm from
power team Brian updated.
0909 X01 Modify:
Change PL4501 to 68.2R210.20C
from IND-D56UH-27-GP base on
Brian updated.
1122 X02 Modify:
stuff EC4501 0.1uF from
EMC Neo suggestion.
1123 X02 Modify:
Change PR4501 to 75K from 45.3K
for 1.05V OCP set to 20A from Brian.
0721 Modify:
Brian suggest change PU4503 to 84.00460.037.
Change PR4506 to 9.76K from 10K from
power team Brian updated.
0920 X01 Modify:
Change PR4507 to 20K from 20.5K
from Brian updated.
0727 Modify:
PR4505,PR4508 change to 100ohm from 10ohm.
stuff PR4509,PR4510 0ohm from Brian updated.
0901 X01 Modify:
Change PTC4502 to 79.3971V.30L from
79.33719.L01 from power team Brian updated.
0913 X01 Modify:
Add 2nd source 77.93971.02L on PTC4502
base on Brian updated 2nd soruce excel file.
DN15ATI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51218_+1.05V_VTT
Size
A3
Document Number
QUEEN 15
Rev
A00
Date: Tuesday, January 04, 2011
Sheet 45 of 108
www.vinafix.vn

SSID = PWR.Plane.Regulator_1p5v0p75v

0719 Modify:
Change PU4602 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

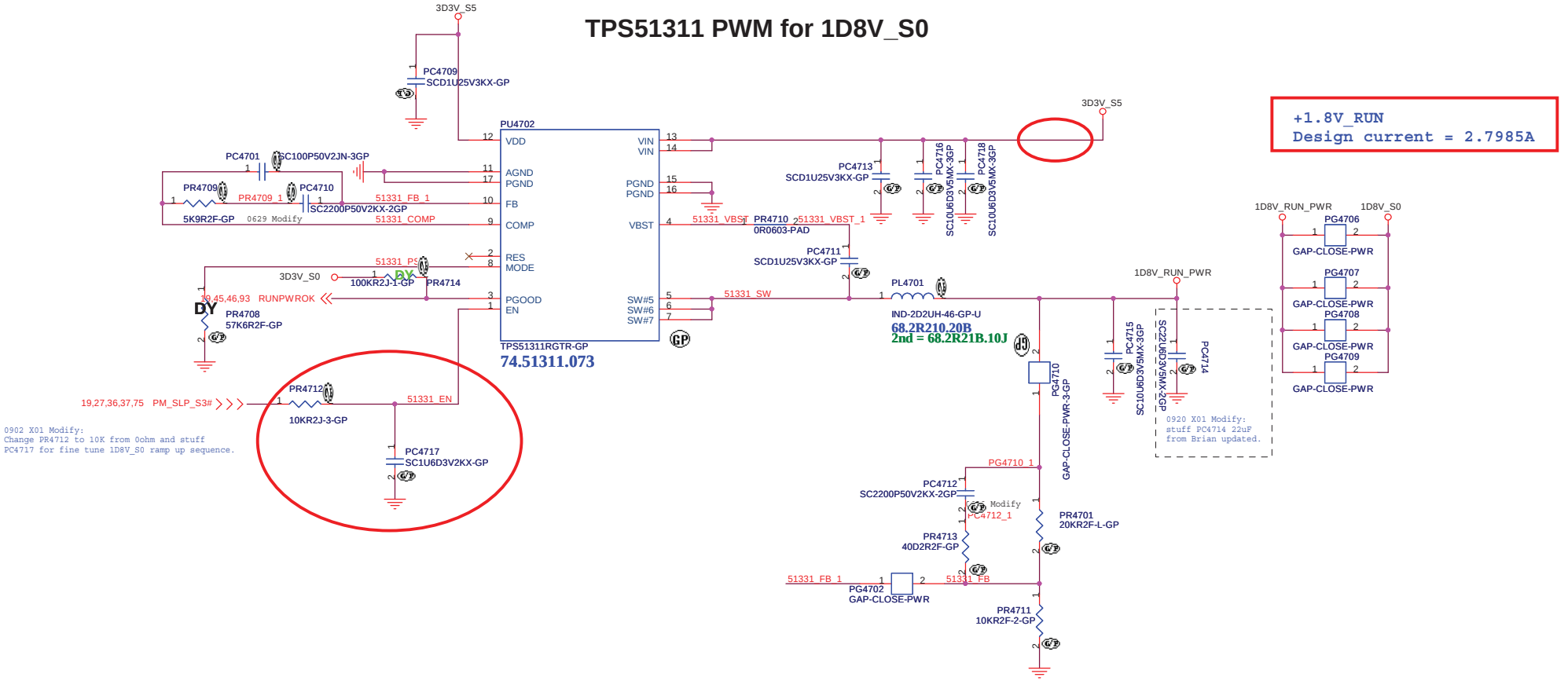
Title: TPS51116_+1.5V_SUS

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 46 of 108

SSID = PWR.Plane.Regulator_1D8V_S0

TPS51311 PWM for 1D8V_S0



DN15ATI Whistler

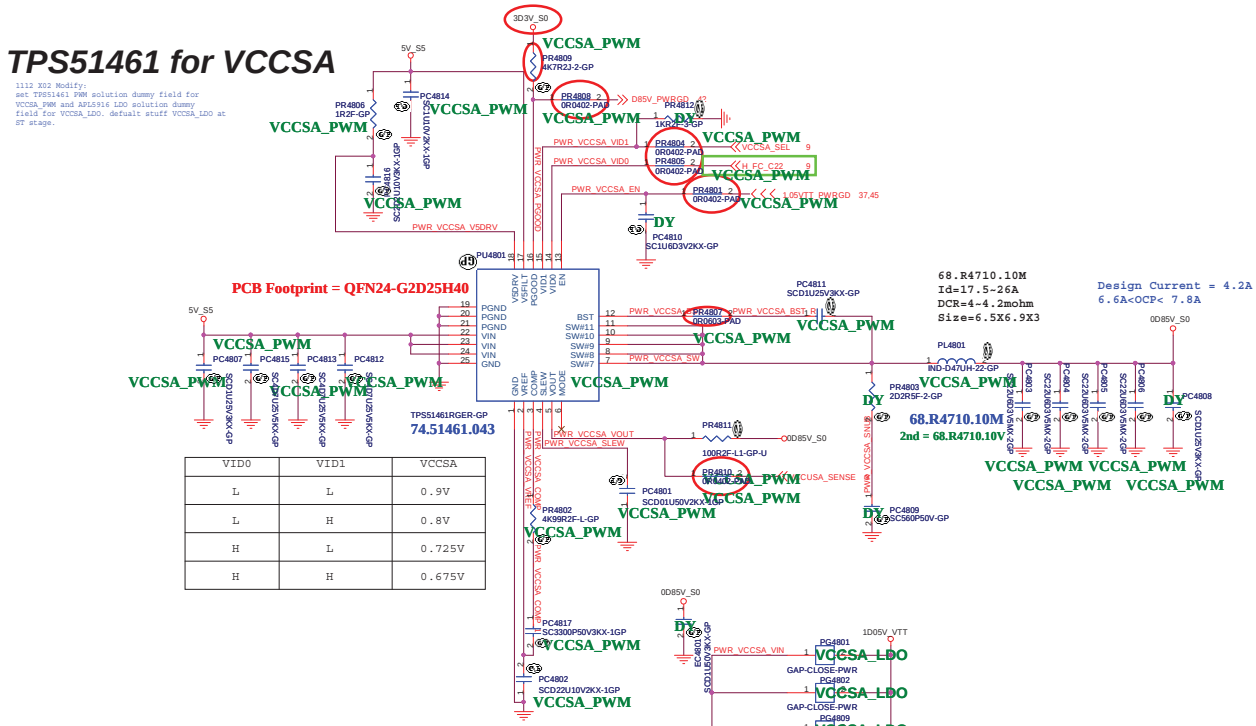
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51311 for 1D8V_S0

Size	Document Number	Rev
A3	QUEEN 15	A00

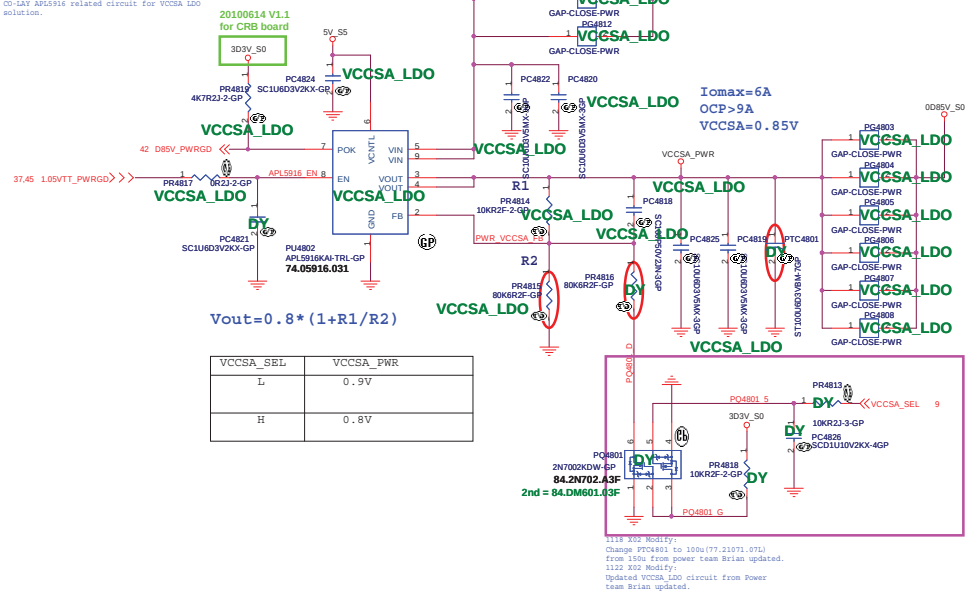
Date: Tuesday, January 04, 2011 Sheet 47 of 108

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

APL5916 for VCCSA



VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

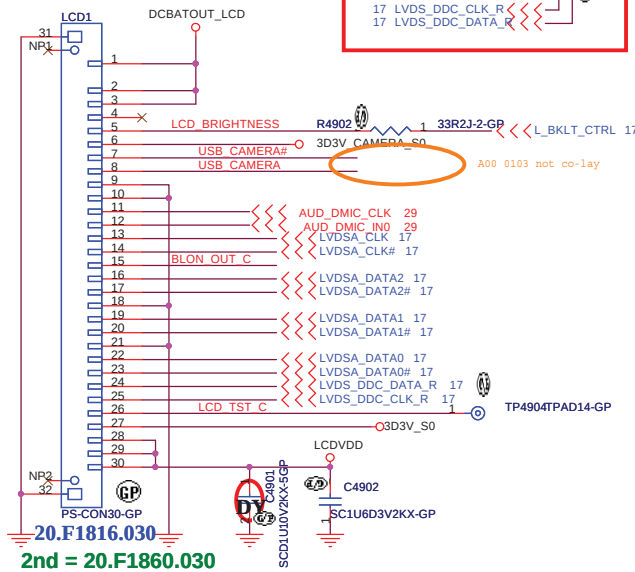
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

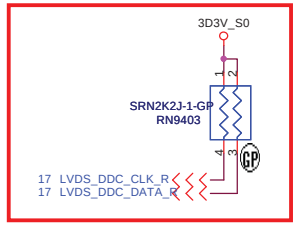
Title: TPS51461 VCCSA
Size: A2 | Document Number: QUEEN&NIRVANA 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 48 of 108

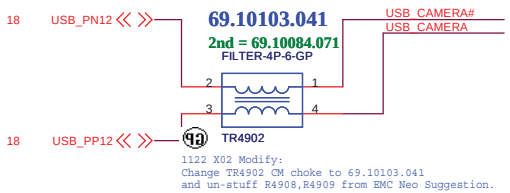
SSID = VIDEO

0909 X01 Modify:
Change LCD1 to 20.F1816.030 for 30pin
Re-assign LCD1 pin define base on Roy updated
cable pin define list.

LVDS CONNECTOR

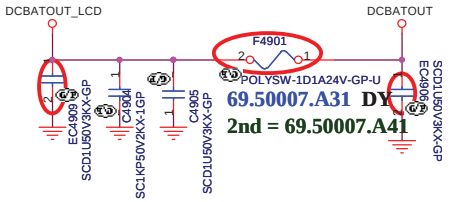


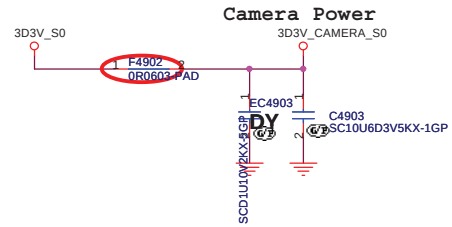




1122 X02 Modify:
Change TR4902 CM choke to 69.10103.041
and un-stuff R4908,R4909 from EMC Neo Suggestion.

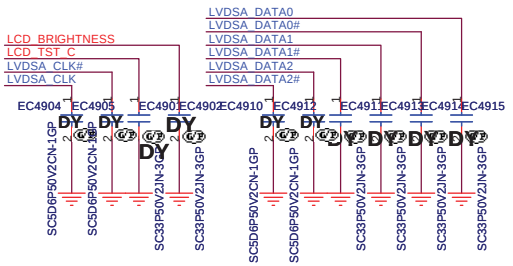
(MB Pin Define)	
MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	NC
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	BLON_OUT_C
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD





0913 X01 Modify:
Reserved EC4910-EC4915 on LVDS signal
for EMC suggestion.

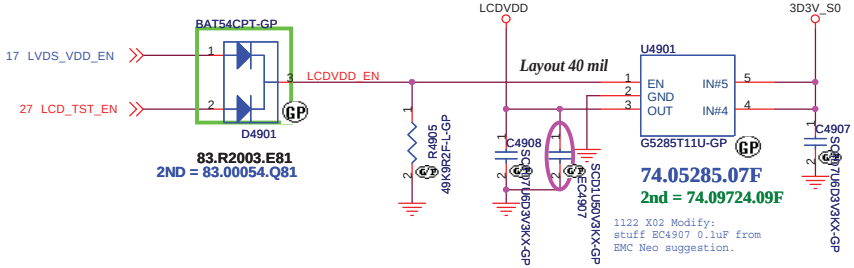
For EMI request
Close to LVDS connector



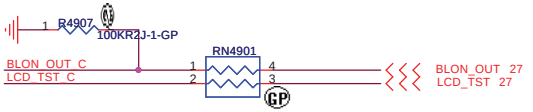
SSID = VIDEO

LCD POWER for ROSA

0902 X01 Modify:
Add 2nd source 74.09724.09F on
U4901 sync with Annie.



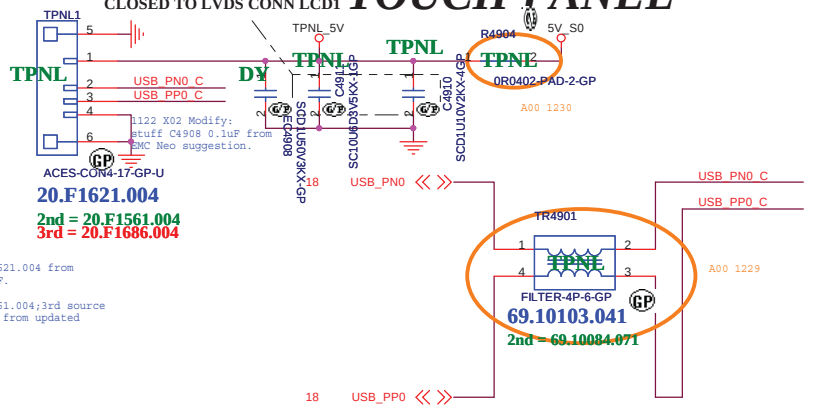
1122 X02 Modify:
stuff EC4907 0.1uF from
EMC Neo suggestion.



1122 X02 Modify:
Change RN4901 to 100ohm 4p from 8p
for improve layout place.

CLOSED TO LVDS CONN LCD1

TOUCH PANEL



1122 X02 Modify:
stuff C4908 0.1uF from
EMC Neo suggestion.

0916 X01 Modify:
Change TPNL1 to 20.F1621.004 from
Double updated EMN&DXF.
0917 X01 Modify:
Add 2nd source 20.F1561.004;3rd source
20.F1686.004 on TPNL1 from updated
connector list.

1122 X02 Modify:
Swap TR4901 pin4,3 and pin2,1 each other
base on Connie swap report.
Change TR4901 CM choke to 69.10103.041
and un-stuff R4911,R4912 from EMC Neo Suggestion.
Change R4911,R4912 to 0603 from 0402.

DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 49 of 108

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT Connector*

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 50 of 108

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

A00 1229

R5101 0R0402-PAD-2-GP: HDMI_CLK_R_C → HDMI_CLK_R_C_CON
R5106 0R0402-PAD-2-GP: HDMI_DATA1_R_C → HDMI_DATA1_R_C_CON
R5102 0R0402-PAD-2-GP: HDMI_CLK_R_C# → HDMI_CLK_R_C#_CON
R5105 0R0402-PAD-2-GP: HDMI_DATA1_R_C# → HDMI_DATA1_R_C#_CON
R5104 0R0402-PAD-2-GP: HDMI_DATA0_R_C → HDMI_DATA0_R_C_CON
R5108 0R0402-PAD-2-GP: HDMI_DATA2_R_C → HDMI_DATA2_R_C_CON
R5103 0R0402-PAD-2-GP: HDMI_DATA0_R_C# → HDMI_DATA0_R_C#_CON
R5107 0R0402-PAD-2-GP: HDMI_DATA2_R_C# → HDMI_DATA2_R_C#_CON

0913 X01 Modify:
Add R5101-R5108and reserved TR5101-TR5104
on all of HDMI differential pair for EMC suggestion.

HDMI_PLL_GND
R5123 0R2J-2-GP
Q5103 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
0806
3D3V_VGA_S0
R5113 100KR2J-1-GP DY

HDMI CONN

0721 Modify:
Change HDMI1 part number to 22.10296.271 from 22.10296.211 base on ME latest EMN and DXF.

0831 X01 Modify:
Change HDMI1 part number to 22.10296.311 from 22.10296.271 base on ME Double updated.
0910 X01 Modify:
Change HDMI1 part number to 22.10296.331 from 22.10296.311 base on ME Double updated.

HDMI1
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
SKT-HDMI23-2-GP-U1
22.10296.331
2nd = 22.10296.311

TPAD14-GP AFTP5101 1 DDC_DATA_HDMI

0716 Modify:
Add F5101 1A FUSE for DELL suggesiton.
0720 Modify:
Stuff F5101 FUSE from DELL suggestion.

5V_CRT_S0_R
A00 1223 HDMI leakage

X02 10.28

C5102 SCD1U10V2KX-5GP
3D3V_S0
R5112 10KR2J-3-GP
HDMI_IN# 27
HPD_HDMI_CON
Q5105 2N7002KDW-GP
GPU_HDMI_HPD 85
R5116 1KR2F-L-GP PEX_RST# 83,85,86
Q5102 PMBS3904-1-GP
0629 Modify
HDMI_HPD_B
R5111 1KR2F-L-GP
R5110 1MR2F-GP
84.03904.L06
2nd = 84.03904.P11
3rd = 84.03904.T11
HDMI_HPD_E
R5125 0R2F-N1-GP
HDMI_HPD_DET 85
R5117 10KR2J-3-GP DY

0629 Modify:
Utilize Q5104 2N7002 instead of PCA9509 Level shifter base on Intel DG recommand on HDMI DDC.

Close to HDMI Connector

85 HDMI_CLK# → HDMI_CLK# C5103 SCD1U10V2KX-5GP → HDMI_CLK_R_C#
85 HDMI_CLK → HDMI_CLK C5104 SCD1U10V2KX-5GP → HDMI_CLK_R_C
85 HDMI_DATA0# → HDMI_DATA0# C5105 SCD1U10V2KX-5GP → HDMI_DATA0_R_C#
85 HDMI_DATA0 → HDMI_DATA0 C5106 SCD1U10V2KX-5GP → HDMI_DATA0_R_C
85 HDMI_DATA1# → HDMI_DATA1# C5110 SCD1U10V2KX-5GP → HDMI_DATA1_R_C#
85 HDMI_DATA1 → HDMI_DATA1 C5107 SCD1U10V2KX-5GP → HDMI_DATA1_R_C
85 HDMI_DATA2# → HDMI_DATA2# C5108 SCD1U10V2KX-5GP → HDMI_DATA2_R_C#
85 HDMI_DATA2 → HDMI_DATA2 C5109 SCD1U10V2KX-5GP → HDMI_DATA2_R_C

RN5106 SRN470J-5-GP
0630 SWAP RN5106
RN5107 SRN470J-5-GP
0630 SWAP RN5107
0726 For NV
HDMI_PLL_GND

3D3V_VGA_S0 5V_S0
0927
R5114 0R0402-PAD-2-GP A00
R5115 0R2J-2-GP DY
RN5116 SRN2K2J-1-GP Optimus

0810
3D3V_VGA_S0
Q5104 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
85 GPU_HDMI_CLK → GPU_HDMI_CLK
85 GPU_HDMI_DATA → GPU_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI

5V_CRT_S0_R A00 1228
RN5101 SRN2K2J-1-GP
0923 SWAP

X02 1110

3D3V_S0
R5109 20KR2J-L2-GP DY
0714 Modify:
Stuff R5109 20K PH to 3D3V_S0.
HDMI_OE# → R5127 0R0402-PAD → HDMI_IN# 27
0707 Modify:
Add Q510_,R5109,R5127 for HDMI_IN# to KBC.
Q5101 2N7002K-2-GP DY
84.2N702.J31
2ND = 84.2N702.031
HPD_HDMI_CON

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: QUEEN 15
Rev: A00
Date: Tuesday, January 04, 2011
Sheet 51 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 52 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS Switch

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 53 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*QUEEN 15*	*A00*

Date: Tuesday, January 04, 2011 Sheet 54 of 108

SSID = User.Interface

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

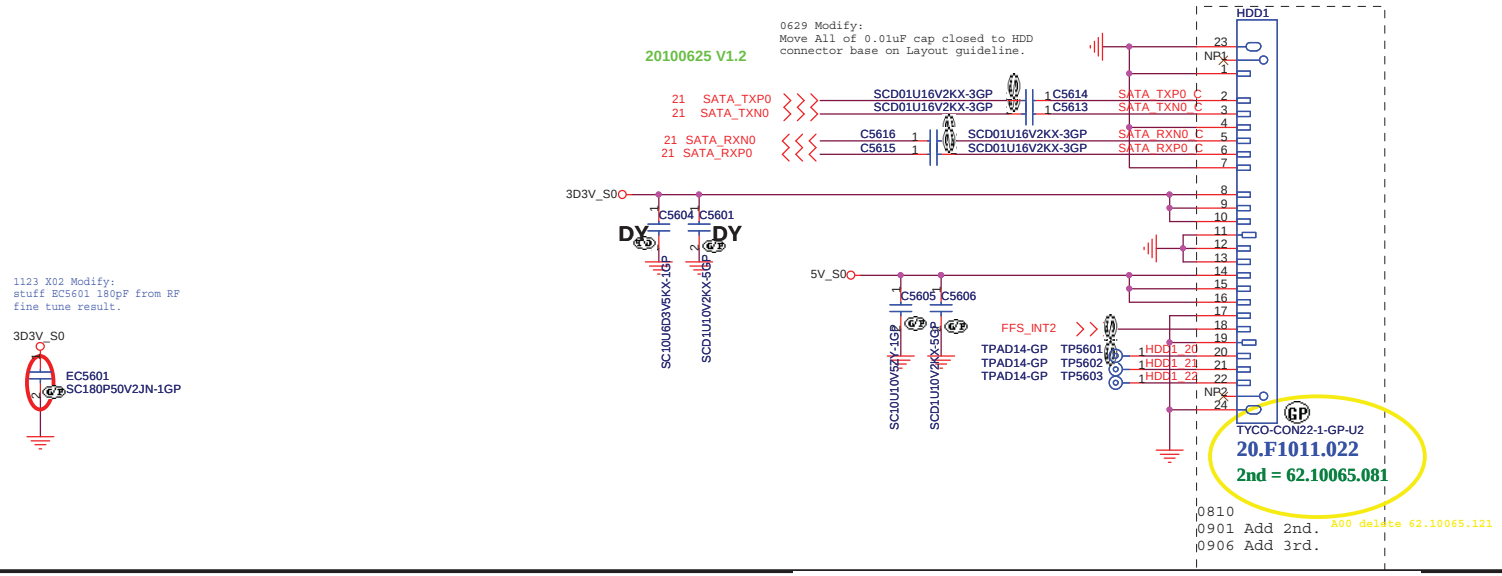
Title: ITP/Fan Connector

Size: A3 | Document Number: QUEEN 15 | Rev: A00

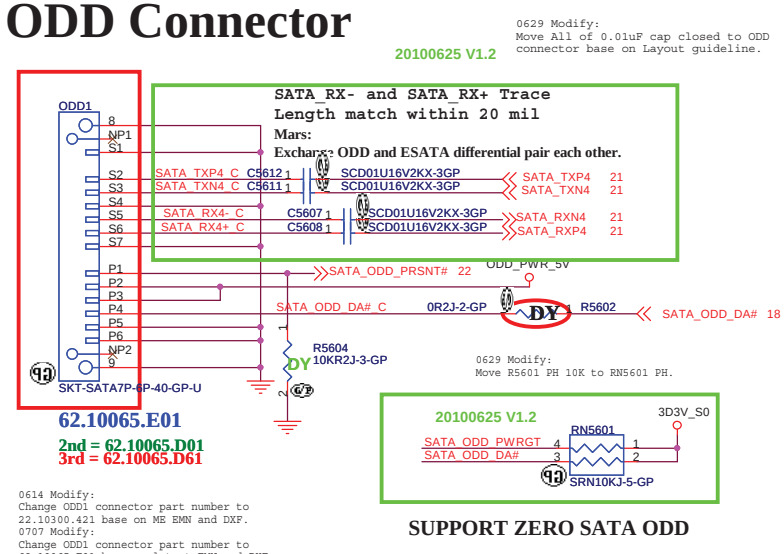
Date: Tuesday, January 04, 2011 | Sheet 55 of 108

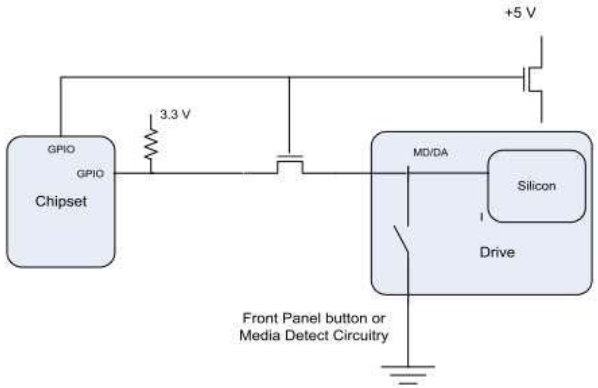
SSID = SATA

SATA HDD Connector

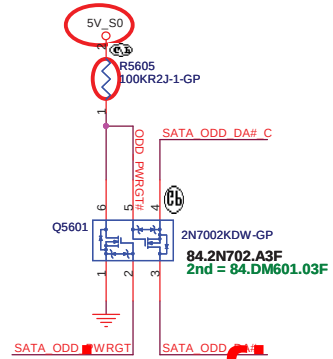


ODD Connector

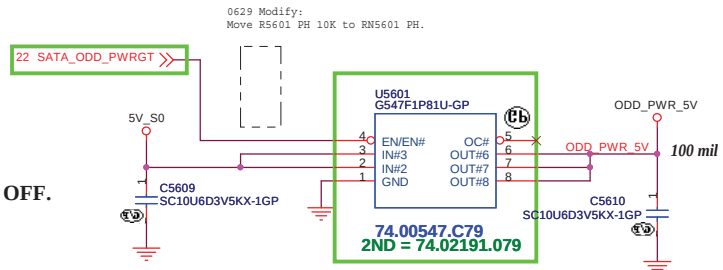




When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	QUEEN 15	A00

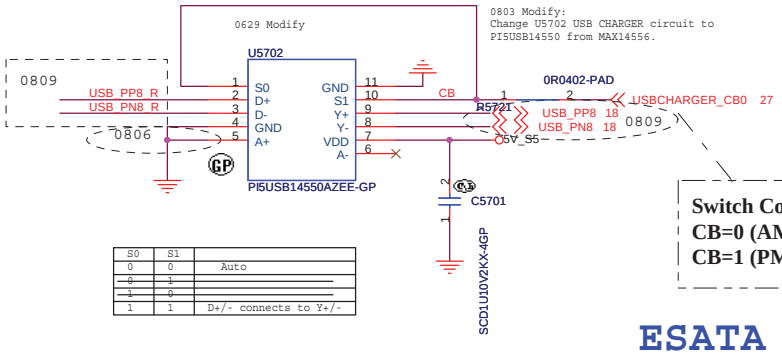
Date: Tuesday, January 04, 2011 Sheet 56 of 108

SSID = ESATA

USB CHARGER

0629 Modify

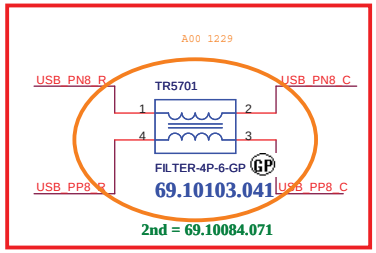
0803 Modify:
Change U5702 USB CHARGER circuit to
PI5USB14550 from MAX14556.



S0	S1	
0	0	Auto
0	1	
1	0	
1	1	D+/- connects to Y+/-

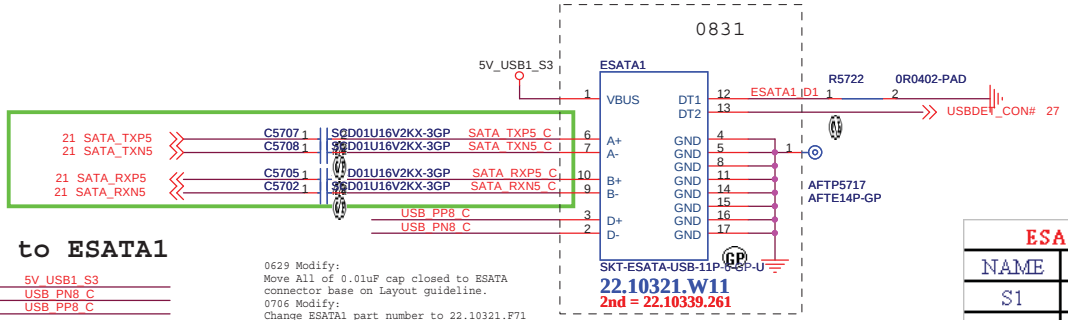
Switch Control Bit:
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

1122 X02 Modify:
Change TR5701CM choke to 69.10103.041
and un-stuff R5718,R5719 from EMC Neo Suggestion.
1123 X02 Modify:
Change R5718,R5719 to 0603 from 0402.

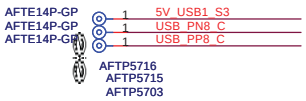


ESATA CONN

0831



close to ESATA1



0629 Modify:
Move All of 0.01uF cap closed to ESATA
connector base on Layout guideline.
0706 Modify:
Change ESATA1 part number to 22.10321.F71
base on latest EMN and DXF.
0713 Modify:
Add USBDET_CON# on ESATA1 pin15 for
USB temporary detect solution ESATA1 CONN
should be searched for detect type connector.
0719 Modify:
ME Double provide temporary foxconn ESATA conn
22.10290.141 for SSI stage function test.

E-SATA USB 2.0 Combo
CE/H=-0.16/2.83mm with detect function

ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

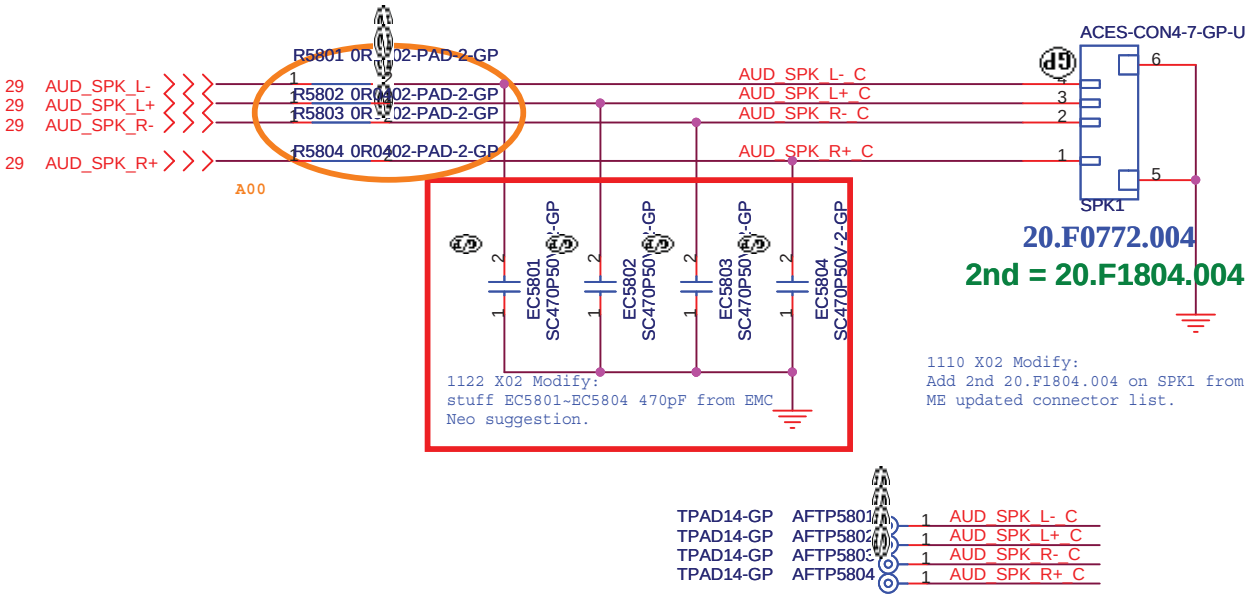
Title: ESATA

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 57 of 108

SSID = AUDIO

Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPEAKER CONN

Size	Document Number	Rev
A4	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 58 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

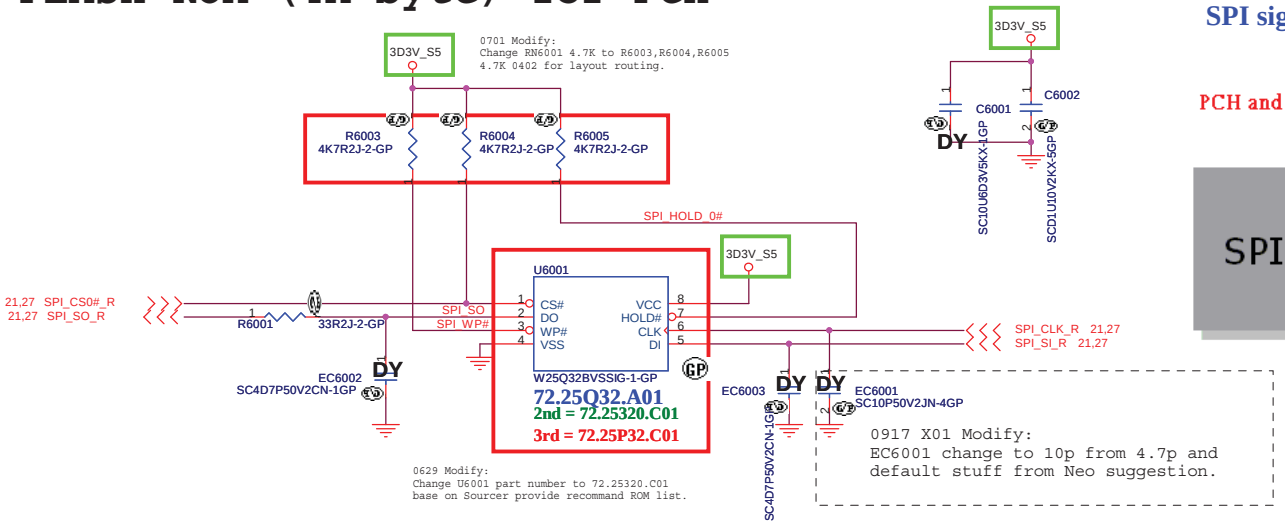
Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

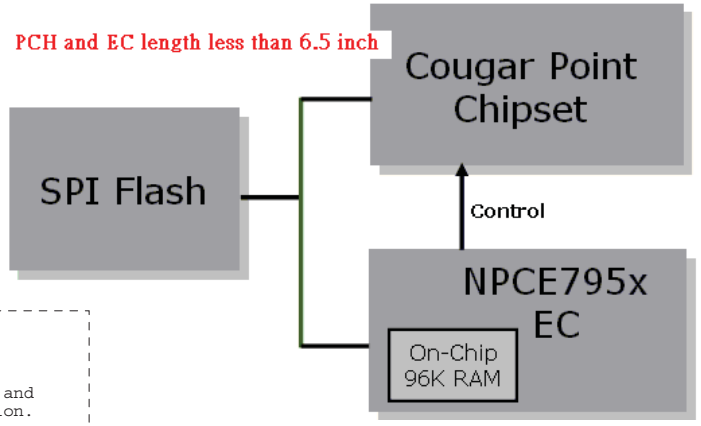
Date: Tuesday, January 04, 2011 | Sheet 59 of 108

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

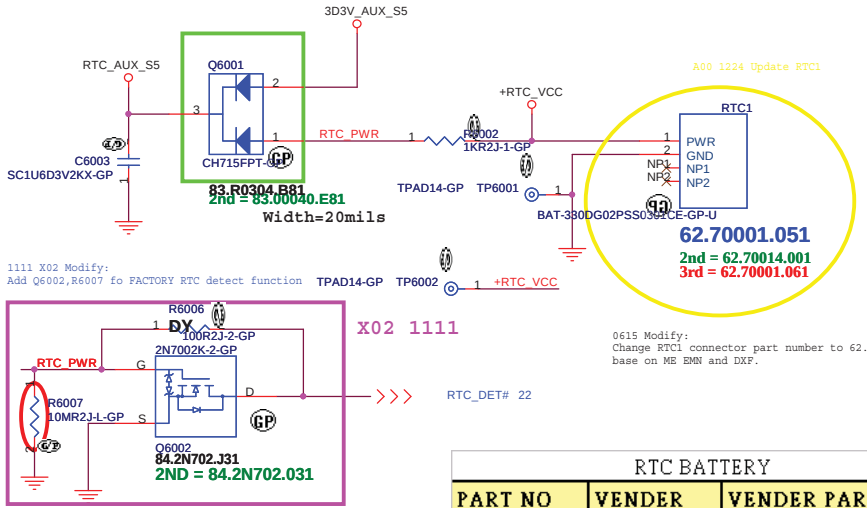
Notes:
The total SPI interface signal between EC and PCH can¡¦t not exceed 6500mil. The mismatch between SPI signal must be within 500mil

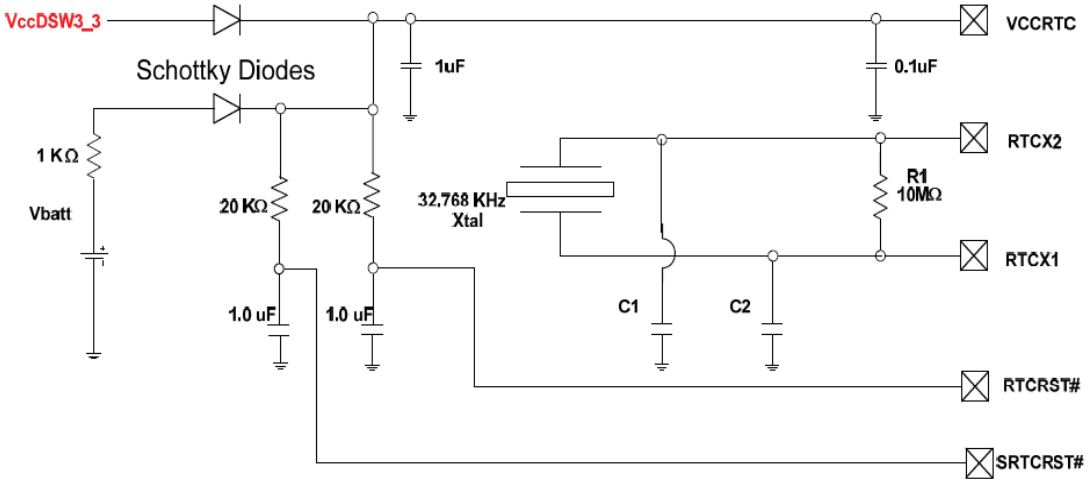




	Pirority	Wistron P/N	Manufacturer	Vendor P/N
X02	1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
	2	72.25320.C01	MXIC	MX25L3206EM2I-12G
X02	3	72.25P32.C01	Numonyx	M25PX32-VMW6F

SSID = RBATT





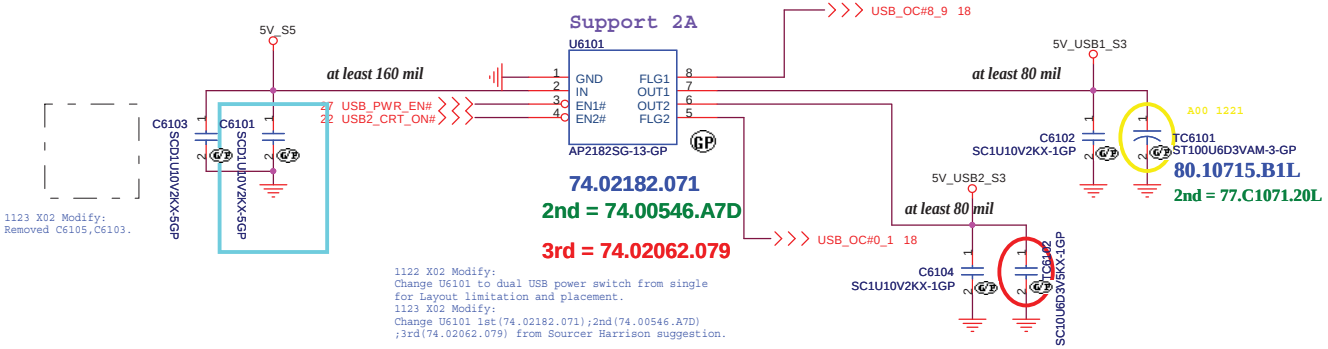
VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

RTC BATTERY		
PART NO	VENDER	VENDER PART NO.
23.20023.311	MITSUBISHI	CR2032 MITSUBISHI
23.20023.341	HENSHEN	CR-2032L/DBE
23.20068.001	KTS	BRBCR2032BX

<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: Flash/RTC
Size: A3
Document Number: QUEEN 15
Rev: A00
Date: Tuesday, January 04, 2011
Sheet 60 of 108

SSID = USB

CRT Board and COMBO USB Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size	Document Number: QUEEN&NIRVANA 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 61 of 108	

(Blanking)

<Core Design>

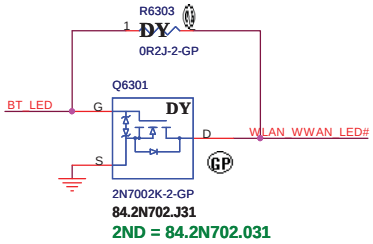
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

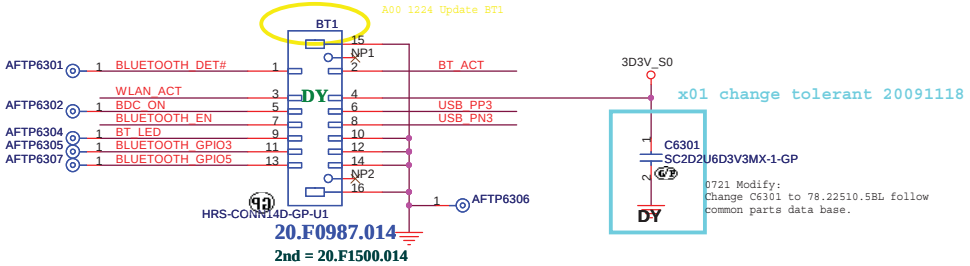
Size	Document Number	Rev
A3	*QUEEN 15*	*A00*

Date: Tuesday, January 04, 2011 Sheet 62 of 108

SSID = User.Interface

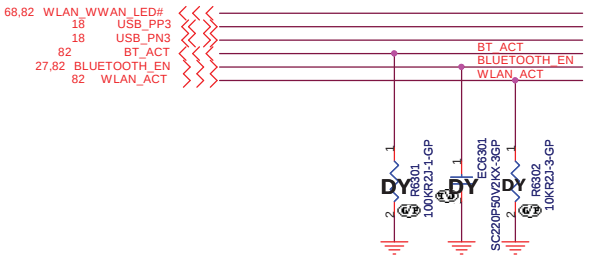


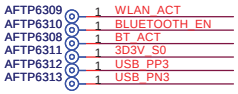
Bluetooth Module conn.



0722 Modify:
Add Q6301 and combine BT_LED to WLAN_WWAN_LED#.

0721 Modify:
Change C6301 to 78.22510.5BL follow common parts data base.





0709 Modify:
PM confirmed there is no stand-alone BT module, so DY BT1 connector, add BT enable signal and 5V_S5 power option on WLAN connector pin 51.
0712 Modify:
Stuff BT relatek component to verify function.

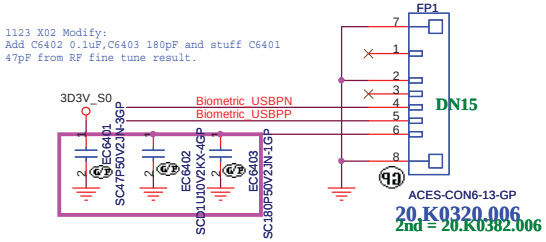
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

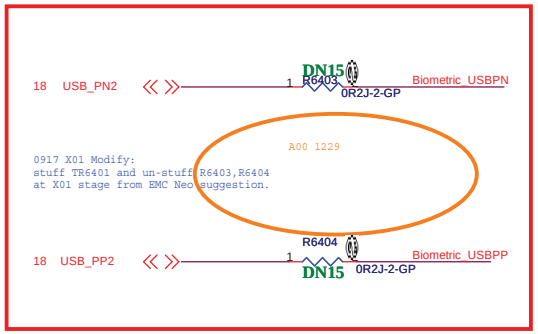
Title		
Bluetooth		
Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 63 of 108	

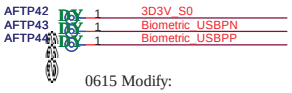
Finger Printer Connector

0707 Modify:
Add FP_DET# signal on FP1 pin1.
0715 Modify:
Add FP_DET# signal on FP1 pin1.
0806 Swap pin.
0810 Change to 4 pin.
0827 Change to 6 pin.



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0





0615 Modify:
Change FP1 connector part number to 20.K0320.004
base on ME EMN and DXF.
0630 Modify:
Change FP1 connector part number to 20.K0320.006
base on ME EMN and DXF.
0707 Modify:
Reassign Figer print pin define base on EXCEL FILE.
0713 Modify:
Reassign Figer print pin define base on EXCEL FILE.
Removed FP_DET# on FP1.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 64 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 65 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 66 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 67 of 108

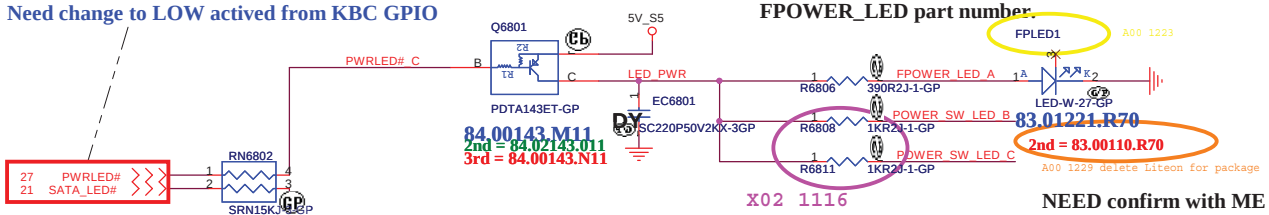
SSID = User.Interface

FRONT POWER LED

Need change to LOW actived from KBC GPIO

NEED confirm with ME actual FPOWER_LED part number.

0706 Modify:
Change FPOWER_LED part number to 83.01221.R70 base on latest EMN and DXF.



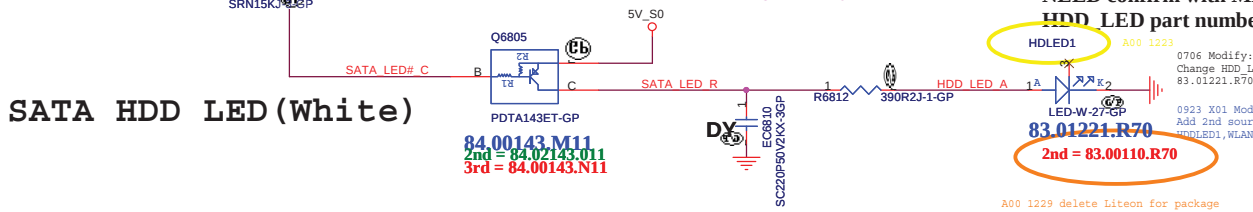
X02 1116

SATA HDD LED(White)

NEED confirm with ME actual HDD_LED part number.

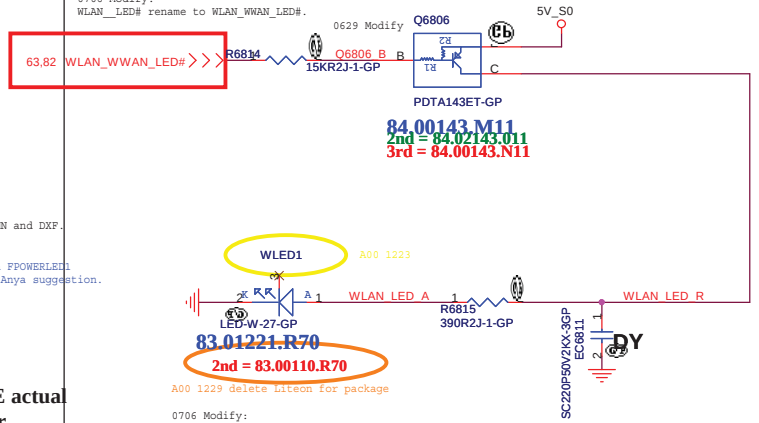
0706 Modify:
Change HDD_LED part number to 83.01221.R70 base on latest EMN and DXF.

0923 X01 Modify:
Add 2nd source 83.00110.J70 on FPOWERLED1
HDDLED1,WLANLED1 from Sourcer Anya suggestion.



WLAN_LED

0706 Modify:
WLAN_LED# rename to WLAN_WWAN_LED#.



0706 Modify:
Change WLAN_LED part number to 83.01221.R70 base on latest EMN and DXF.

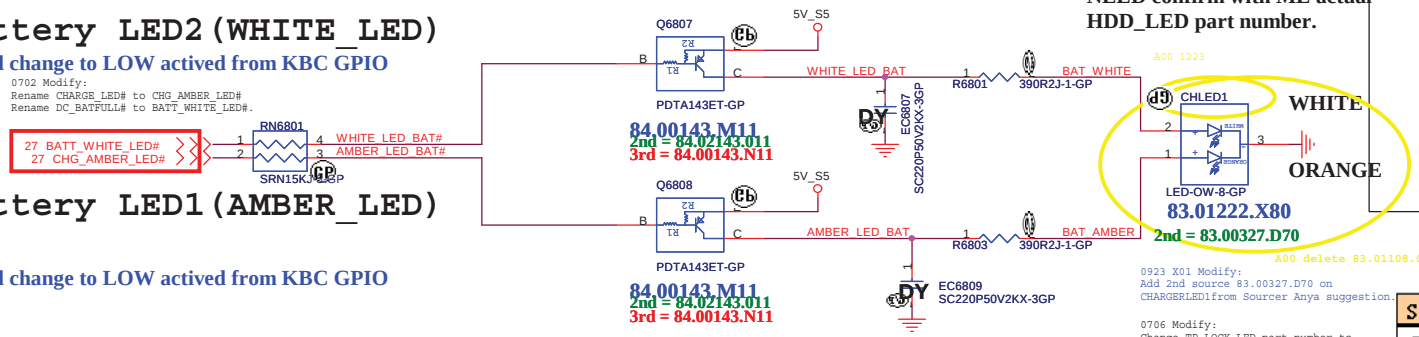
0923 X01 Modify:
Add 2nd source 83.00110.J70 on FPOWERLED1
HDDLED1,WLANLED1 from Sourcer Anya suggestion.

Battery LED2(WHITE_LED)

Need change to LOW actived from KBC GPIO

0702 Modify:
Rename CHARGE_LED# to CHG_AMBER_LED#
Rename DC_BATFULL# to BATT_WHITE_LED#.

NEED confirm with ME actual HDD_LED part number.



Battery LED1(AMBER_LED)

Need change to LOW actived from KBC GPIO

0923 X01 Modify:
Add 2nd source 83.00327.D70 on
CHARGERLED1from Sourcer Anya suggestion.

0706 Modify:
Change TP_LOCK_LED part number to 83.19217.J70 base on latest EMN and DXF.

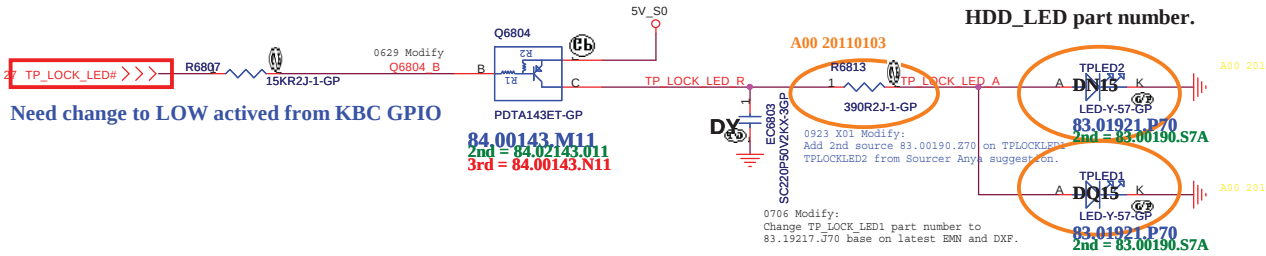
SKEW	ITEM1	ITEM2
DQ15	PWRBTN1	TP_LOCK_LED1
DN15	PWRBTN2	TP_LOCK_LED2

TPLOCK LED

Need change to LOW actived from KBC GPIO

NEED confirm with ME actual HDD_LED part number.

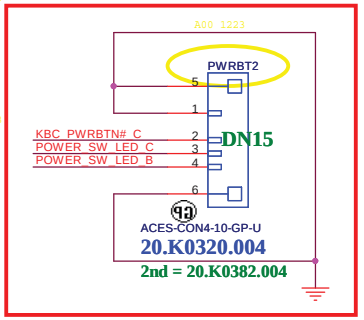
A00 20110103

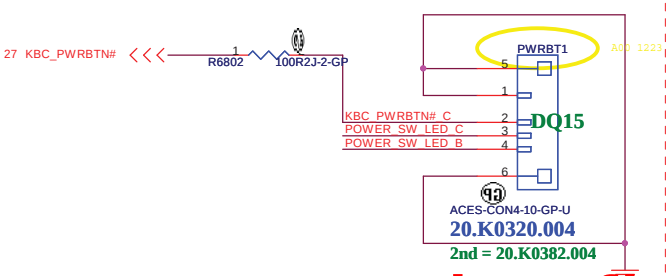


0923 X01 Modify:
Add 2nd source 83.00190.Z70 on TPLOCKLED1
TPLOCKLED2 from Sourcer Anya suggestion.

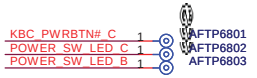
0706 Modify:
Change TP_LOCK_LED1 part number to 83.19217.J70 base on latest EMN and DXF.

0706 Modify:
Add PWRBTN2 for DQ15,PWRBTN1 FOR DN15.





0715 Modify:
Removed PWR_BTN_LED# control circuit base on Dell feedback.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

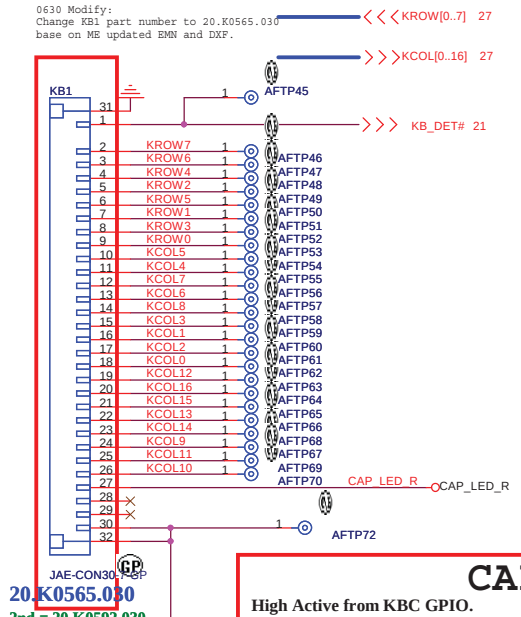
Title: LED Bard/Power Button

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 68 of 108

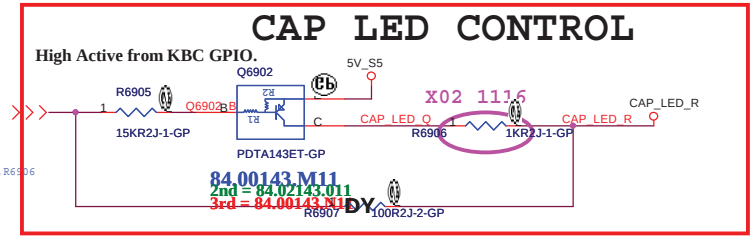
SSID = KBC

Internal KeyBoard Connector



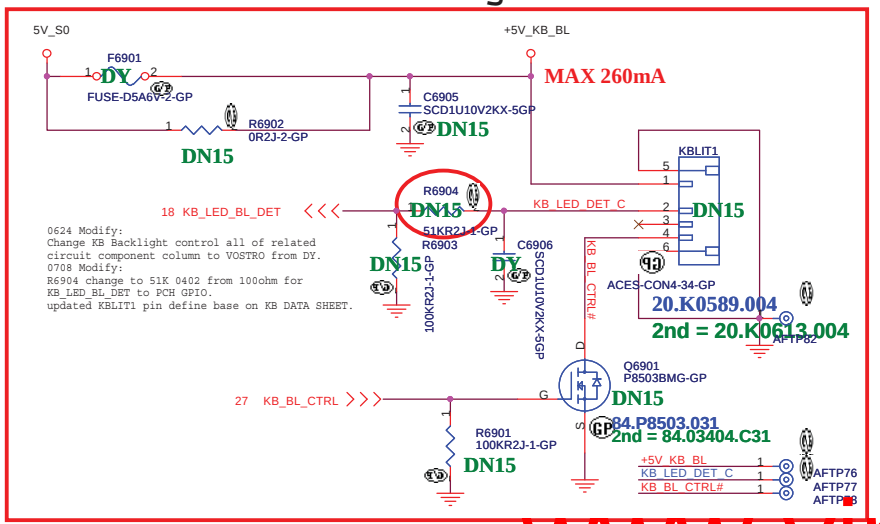
MB Pin	Description
1	Diag_Loop3 = GPIO_1 (TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	NC (reserved for Caps LK LED)
28	NC (reserved for Num LK LED)
29	NC (reserved for Scroll LK LED)
30	GND

CAP LED CONTROL



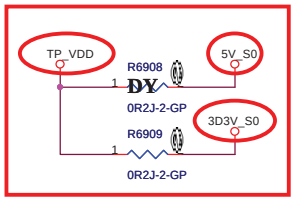
CAP_LED:(Default HIGH actived)
Connect to KB driving internal LED directly.(MAX 25mA)

KB Backlight Connector



SSID = Touch.Pad

0715 Modify:
Add R6908,R6909 for TPAD1 co-lay power option.

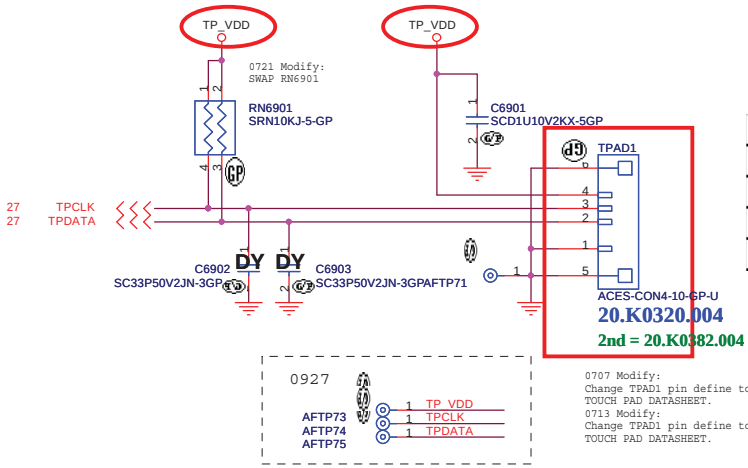


0624 Modify:
Removed TP LOCKED CONTROL combin
with KEYBOARD Function KEY.

0713 Modify:
Change TPAD1 power source to 3D3V_S0 from
5V_S0 base on DELL latest spec A02.

0630 Modify:
Change TPAD1 part number to 20.K0320.006
base on ME updated EMN&DXF.
0712 Modify:
Change TPAD1 part number to 20.K0320.004
from 20.K0320.006.

TouchPad Connector



MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

SKEW	OPTION1	OPTION2	PIN	Feature	REMARK
DQ13	C12S		30		S is mean small
DN13	C12S	C12SB	30/25	Backlight	SB is mean small with backlight
DN15	C12S	C12SB	30/25	Backlight	
DQ15	C12SN		30	KB_DET#,CAP LED	SN is mean small with numpad

MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

0901 X01 Modify:
Change KBLIT1 to 20.K0320.004 from
20.K0218.004 base on ME updated X01 DXF&EMN.
Re-assign KBLIT1 pin define sync with DQ15_NV.
0914 X01 Modify:
Add 2nd source 20.K0382.004 on KBLIT1
base on updated connector list.
0923 X01 Modify:
Change KBLIT1 part number to 20.K0589.004
and re-assign pin define base on Roy updated.

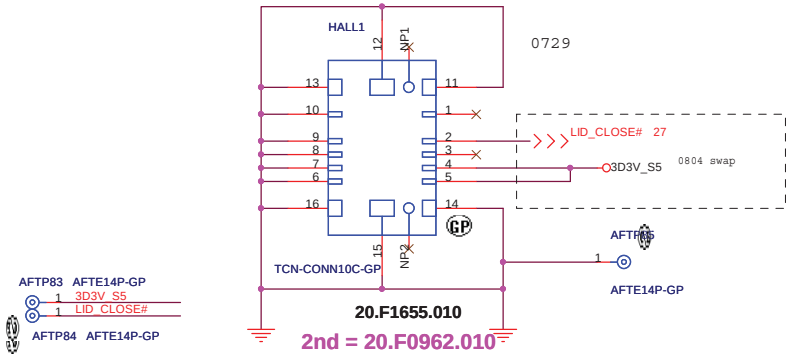
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 69 of 108



1110 X02 Modify:
Add 2nd 20.F0962.010 on HALL1 from
ME updated connector list.

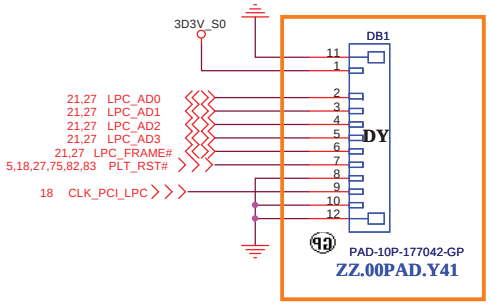
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Hall Sensor*

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 70 of 108



A00 1229 DB1 change to ZZ.00PAD.Y41(solder kmask type)
and keep un-stuffat X-Build stage

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector		
Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 71 of 108	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 72 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

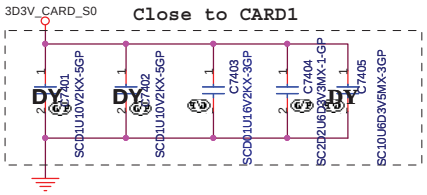
Title: *Reserved*

Size	Document Number	Rev
A3	*QUEEN 15*	*A00*

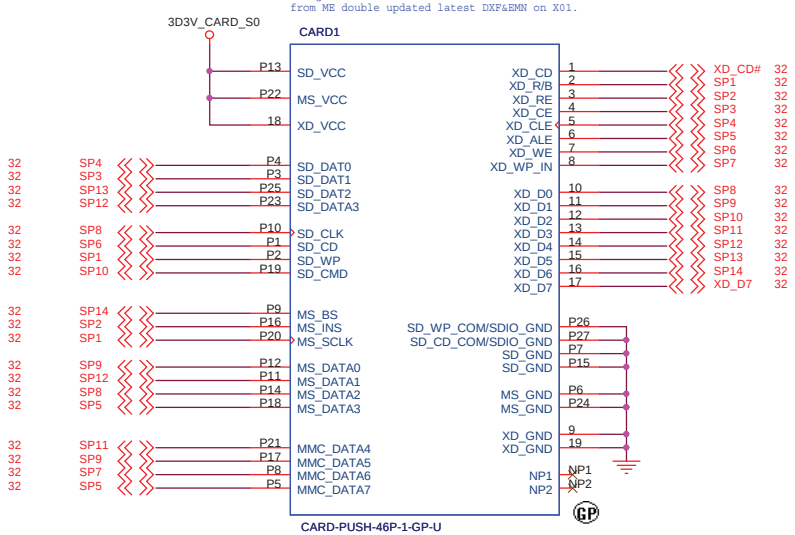
Date: Tuesday, January 04, 2011 Sheet 73 of 108

SSID = SDIO

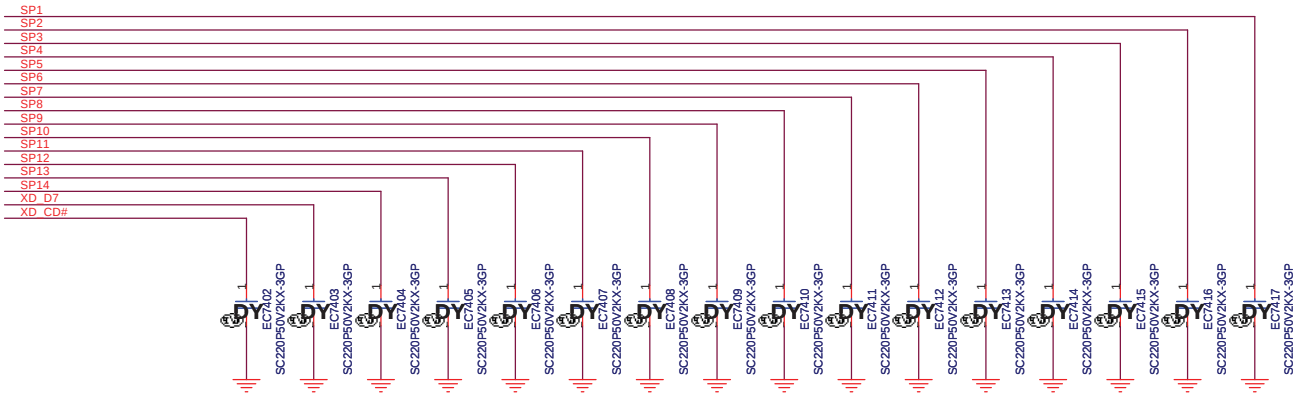
SD/XD/MS/MMC+ Card Reader



WITHOUT CARD	WP, CD, GND
CARD INSERTED WP−SW:LOCK	WP, CD, GND
CARD INSERTED WP−SW:UNLOCK	WP, CD, GND



For EMI Reserved



20.I0129.001			
PIN	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

<Core Design>

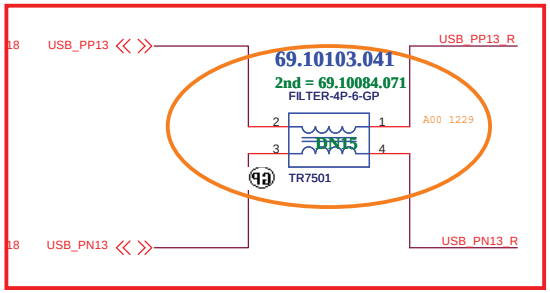
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

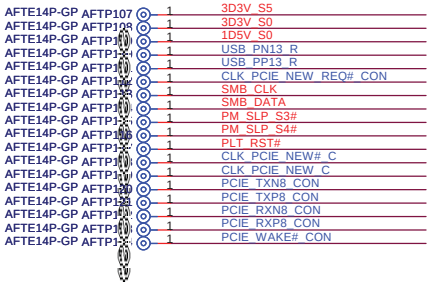
Title: SD/XD/MS/MMC Card CONN

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 74 of 108

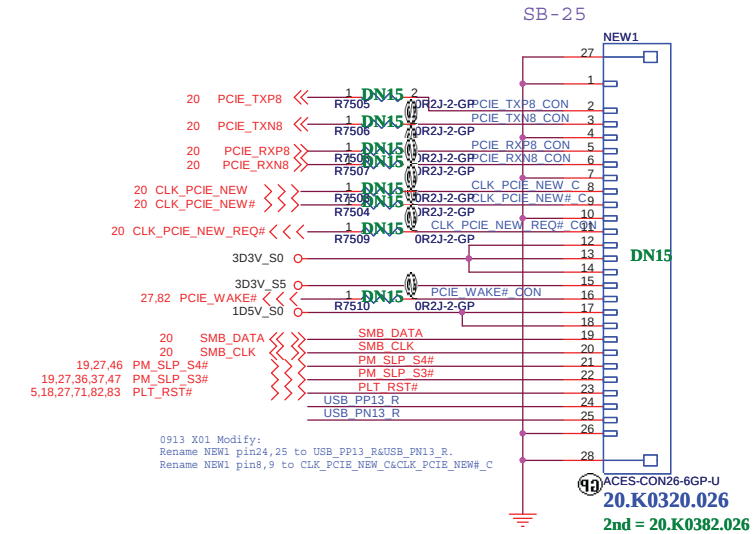
1122 X02 Modify:
Change TR7501 CM choke to 69.10103.041
and un-stuff R7501,R7502 from EMC Neo Suggestion.
Change R7501,R7502 to 0603 from 0402.





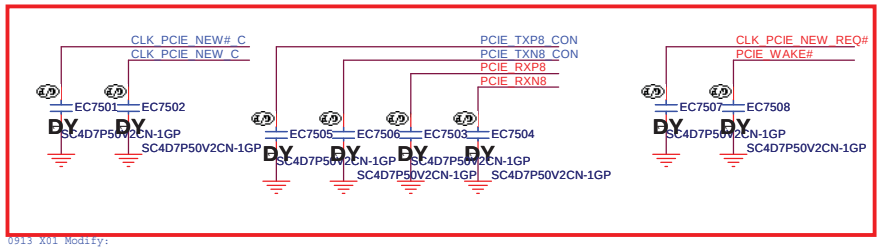
1D5V_S0_CARD Max. 650mA, Average 500mA.
3D3V_S0_CARD Max. 1300mA, Average 1000mA
3D3V_S5_CARDAUX Max. 275mA

0824 X01 Modify:
Due to our NEW1 change to Express card to bottom side so re-assign NEW1 pin define same as DQ15-NV.
0906 X01 Modify:
Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.



0913 X01 Modify:
Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R.
Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C

For EMI



0913 X01 Modify:
Add R7503,R7504 and reserved EC7501,EC7502 on
CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion.
0921 X01 Modify:
Add R7505~R7508 0ohm and reserved EC7503~EC7506
on PCIE_TX8&RX8 signal base on EMC Lance suggestion.
Add R7509,R7510 0ohm and reserved EC7507,EC7508
on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base
on EMC Lance suggestion.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Express Card

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 75 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 76 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 77 of 108

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

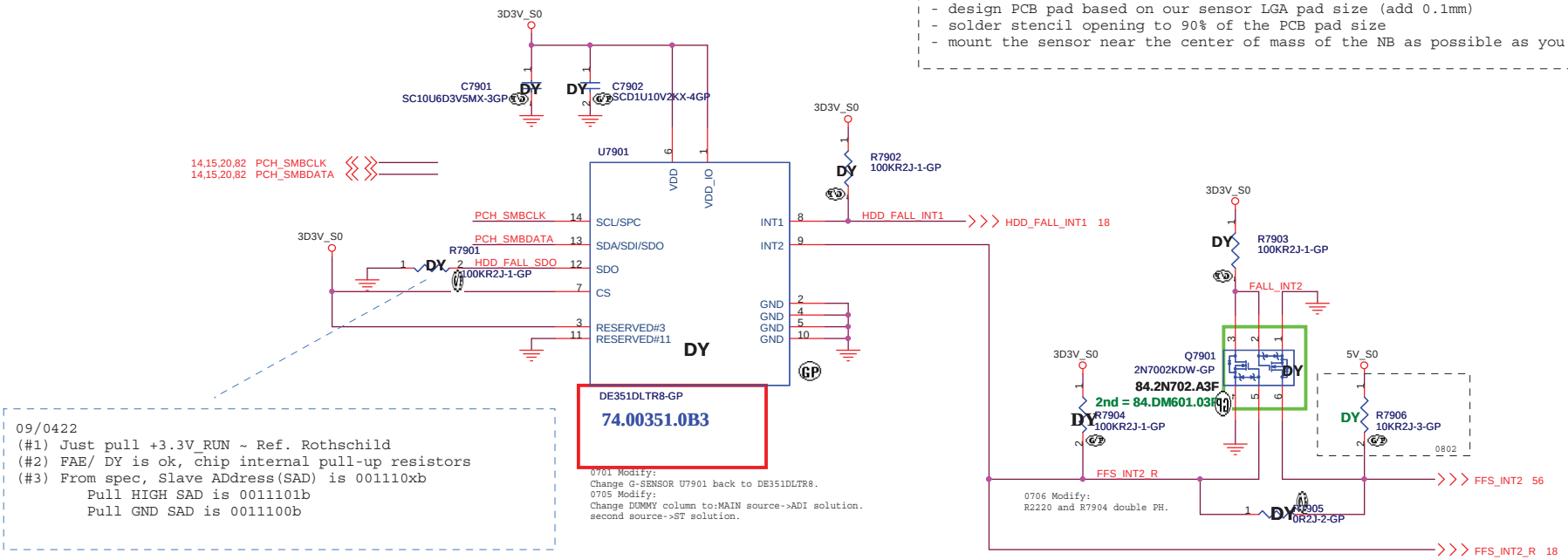
Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 78 of 108

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Free Fall Sensor		
Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 79 of 108	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 80 of 108

(Blanking)

<Core Design>

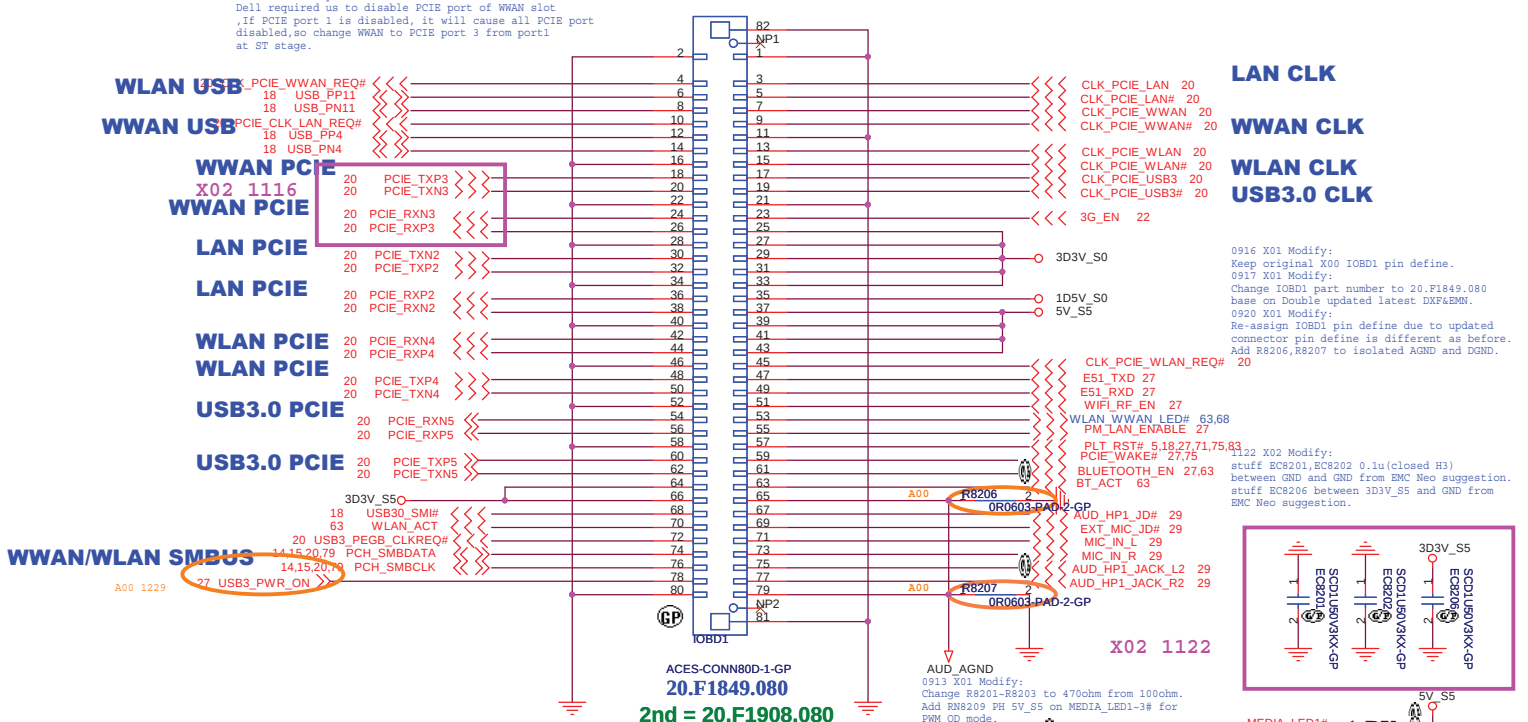
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *QUEEN 15* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 81 of 108

IO Board CONN 80 pin

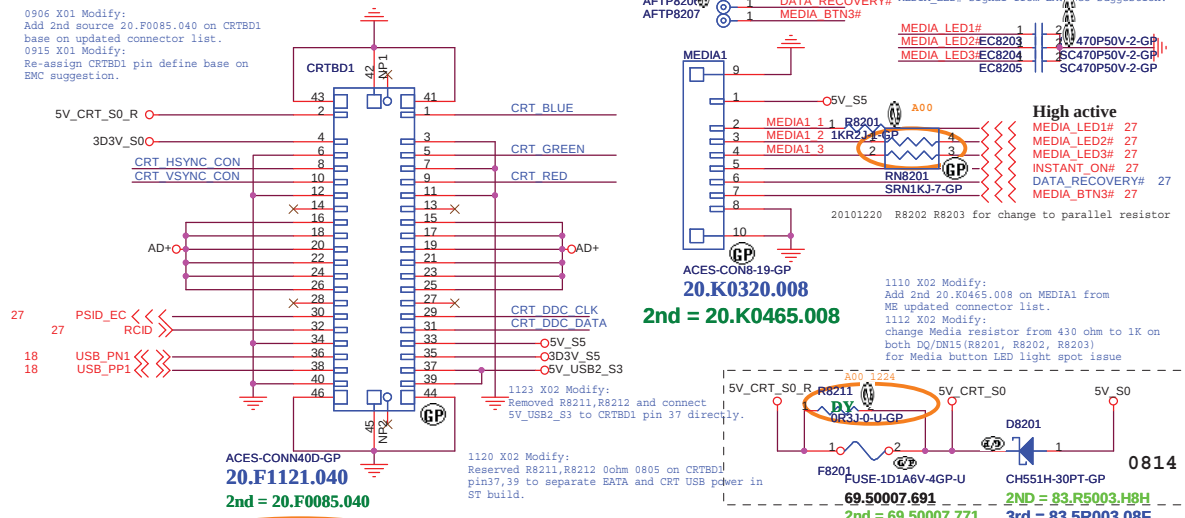


SIGNAL	PIN	PIN	SIGNAL
GND	80	79	GND
CLK_PCIE_WWAN_REQ#	78	77	CLK_PCIE_LAN
USB_PP11	76	75	CLK_PCIE_LAN#
USB_PN11	74	73	CLK_PCIE_WWAN
PCIE_CLK_LAN_REQ#	72	71	CLK_PCIE_WWAN#
USB_PP4	70	69	GND
USB_PN4	68	67	CLK_PCIE_WLAN
GND	66	65	CLK_PCIE_WLAN#
PCIE_TXP1	64	63	CLK_PCIE_USB3
PCIE_TXN1	62	61	CLK_PCIE_USB3#
GND	60	59	GND
PCIE_RXN1	58	57	3G_EN
PCIE_RXP1	56	55	3D3V_S0
GND	54	53	3D3V_S0
PCIE_TXN2	52	51	3D3V_S0
PCIE_TXP2	50	49	3D3V_S0
GND	48	47	3D3V_S0
PCIE_RXP2	46	45	1D5V_S0
PCIE_RXN2	44	43	5V_S5
GND	42	41	5V_S5
PCIE_RXN4	40	39	5V_S5
PCIE_RXP4	38	37	5V_S5
GND	36	35	CLK_PCIE_WLAN_REQ#
PCIE_TXP4	34	33	E51_TXD
PCIE_TXN4	32	31	E51_RXD
GND	30	29	WIFI_RF_EN
IOBD1_28	28	27	WLAN_WWAN_LED#
IOBD1_26	26	25	PM_LAN_ENABLE
GND	24	23	PLT_RST#
IOBD1_22	22	21	PCIE_WAKE#
IOBD1_20	20	19	BLUETOOTH_EN
3D3V_S5	18	17	BT_ACT
3D3V_S5	16	15	GND
IOBD1_14	14	13	AUD_HP1_JD#
WLAN_ACT	12	11	EXT_MIC_JD#
USB3_PEGB_CLKREQ#	10	9	MIC_IN_L
PCH_SMBDATA	8	7	MIC_IN_R
PCH_SMBCLK	6	5	AUD_HP1_JACK_L2
USB3_PWR_ON	4	3	AUD_HP1_JACK_R2
GND	2	1	GND

CRT Board Connector

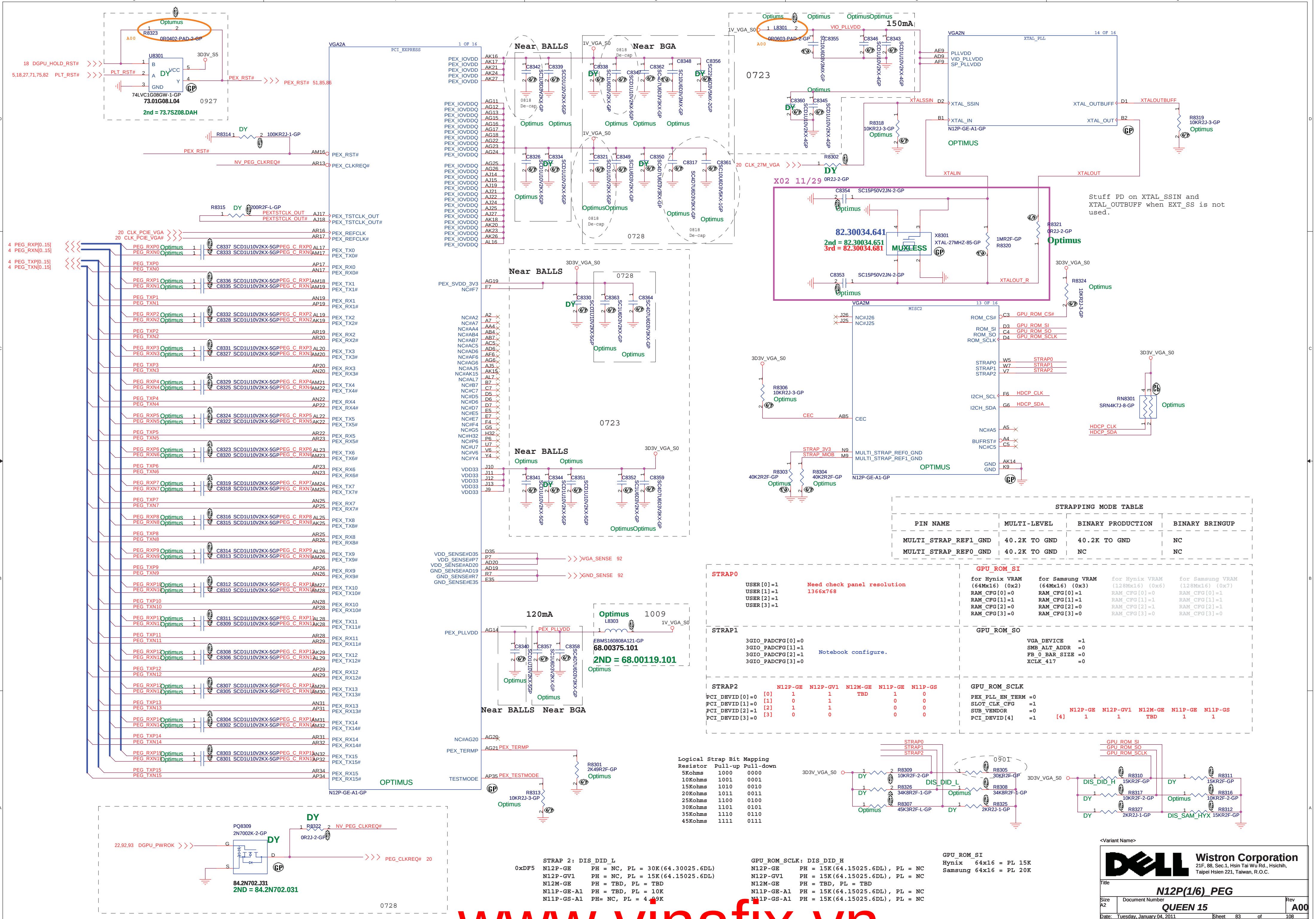
USB3.0 PCIE
USB3.0 PCIE

SIGNAL	PIN	PIN	SIGNAL
5V_CRT_S0_R	2	1	CRT_BLUE_R
3D3V_S0	4	3	GND
GND	6	5	CRT_GREEN_R
CRT_HSYNC_CON	8	7	GND
CRT_VSYNC_CON	10	9	CRT_RED_R
GND	12	11	GND
NC	14	13	NC
AD+	16	15	AD+
AD+	18	17	AD+
AD+	20	19	AD+
AD+	22	21	AD+
AD+	24	23	AD+
AD+	26	25	AD+
NC	28	27	NC
PSID_EC	30	29	DDCCLK
RCID	32	31	DDCDATA
GND	34	33	5V_S5
USB_PN1	36	35	3D3V_S5
USB_PP1	38	37	5V_USB1_S3
GND	40	39	5V_USB1_S3



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3 | Document Number: QUEEN 15 | Rev: A00
Date: Tuesday, January 04, 2011 | Sheet 82 of 108



STRAPPING MODE TABLE

PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF1_GND	40.2K TO GND	40.2K TO GND	NC
MULTI_STRAP_REF0_GND	40.2K TO GND	NC	NC

STRAP0

USER[0]=1
USER[1]=1
USER[2]=1
USER[3]=1

Need check panel resolution 1366x768

GPU_ROM_SI

for Hynix VRAM (64Mx16) (0x2)	for Samsung VRAM (64Mx16) (0x3)	for Hynix VRAM (128Mx16) (0x6)	for Samsung VRAM (128Mx16) (0x7)
RAM_CFG[0]=0	RAM_CFG[0]=1	RAM_CFG[0]=0	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=0	RAM_CFG[2]=1	RAM_CFG[2]=1
RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0

STRAP1

3GIO_PADCFG[0]=0
3GIO_PADCFG[1]=1
3GIO_PADCFG[2]=1
3GIO_PADCFG[3]=0

Notebook configure.

GPU_ROM_SO

VGA_DEVICE =1
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0

STRAP2

		N12P-GE	N12P-GV1	N12M-GE	N11P-GE	N11P-GS
PCI_DEVID[0]=0	[0]	1	1	TBD	1	0
PCI_DEVID[1]=0	[1]	0	1		0	0
PCI_DEVID[2]=1	[2]	1	1		0	0
PCI_DEVID[3]=0	[3]	0	0		1	0

GPU_ROM_SCLK

PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1

	N12P-GE	N12P-GV1	N12M-GE	N11P-GE	N11P-GS
[4]	1	1	TBD	1	1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

0xDF5 STRAP 2: DIS_DID_L
N12P-GE PH = NC, PL = 30K(64.30025.6DL)
N12P-GV1 PH = NC, PL = 15K(64.15025.6DL)
N12M-GE PH = TBD, PL = TBD
N11P-GE-A1 PH = TBD, PL = 10K
N11P-GS-A1 PH= NC, PL = 4.99K

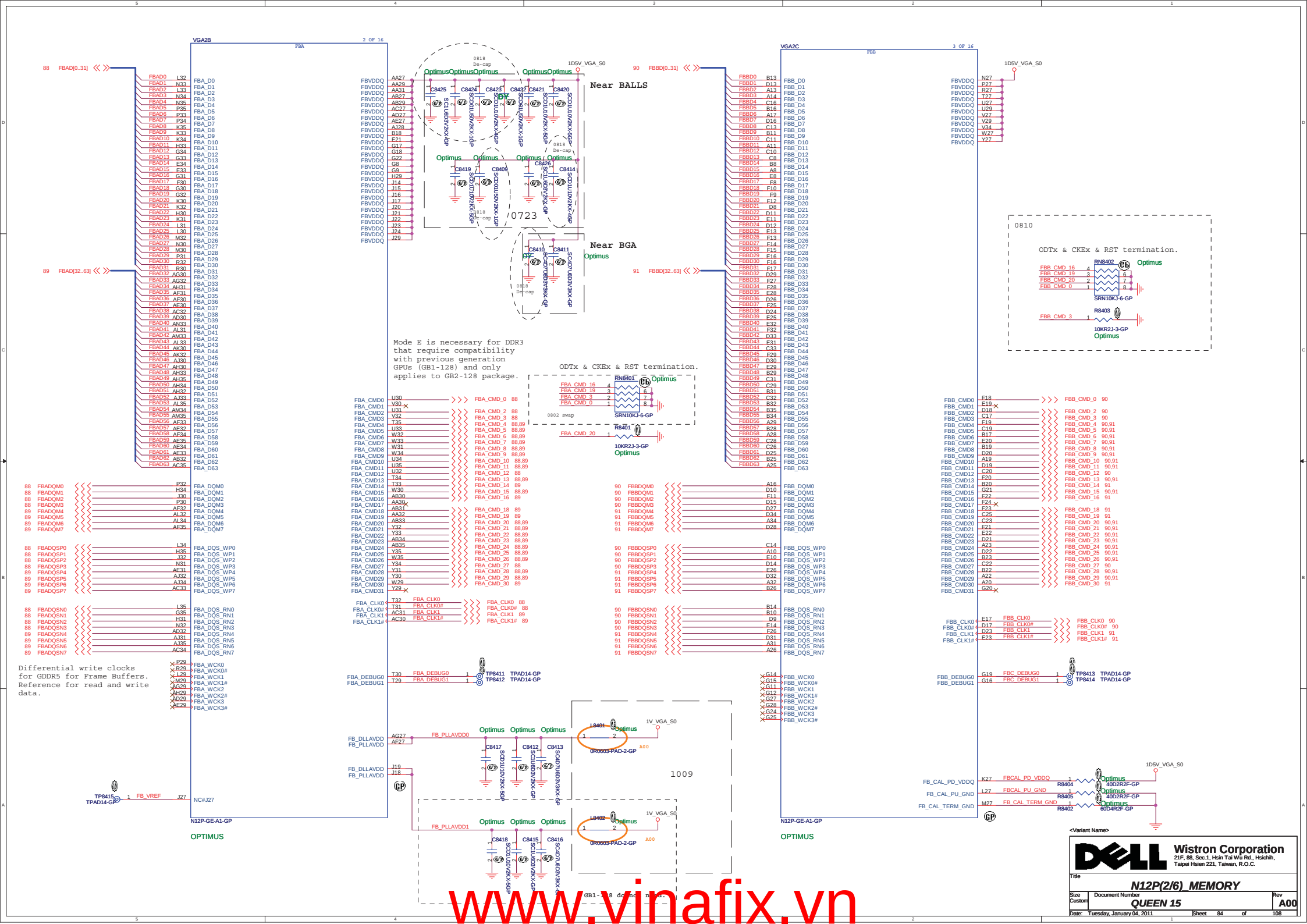
GPU_ROM_SCLK: DIS_DID_H
N12P-GE PH = 15K(64.15025.6DL), PL = NC
N12P-GV1 PH = 15K(64.15025.6DL), PL = NC
N12M-GE PH = TBD, PL = TBD
N11P-GE-A1 PH = 15K(64.15025.6DL), PL = NC
N11P-GS-A1 PH = 15K(64.15025.6DL), PL = NC

GPU_ROM_SI
Hynix 64x16 = PL 15K
Samsung 64x16 = PL 20K

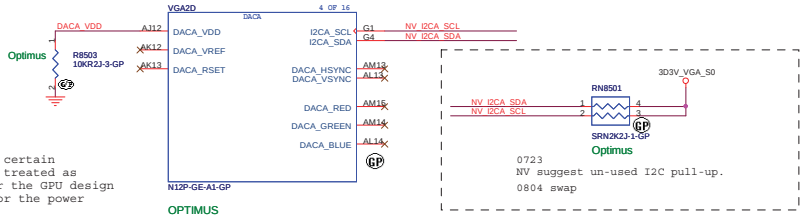
<Variant Name>

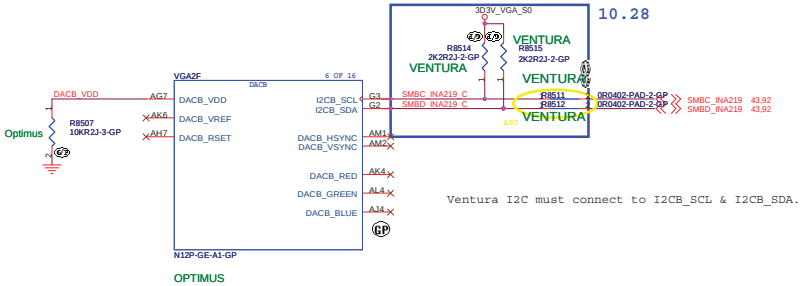
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P(1/6)_PEG
Size: A2 Document Number: QUEEN 15 Rev: A00
Date: Tuesday, January 04, 2011 Sheet 83 of 108


VGA2B
2 OF 16
FBA
VGA2C
3 OF 16
FBB
Near BALLS
Near BGA
0723
1009
0810
ODTx & CKEx & RST termination.
Mode E is necessary for DDR3 that require compatibility with previous generation GPUs (GB1-128) and only applies to GB2-128 package.
Differential write clocks for GDDR5 for Frame Buffers. Reference for read and write data.
N12P-GE-A1-GP
OPTIMUS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
N12P(2/6)_MEMORY
QUEEN 15
A00
Tuesday, January 04, 2011
84
108
www.vinafix.vn

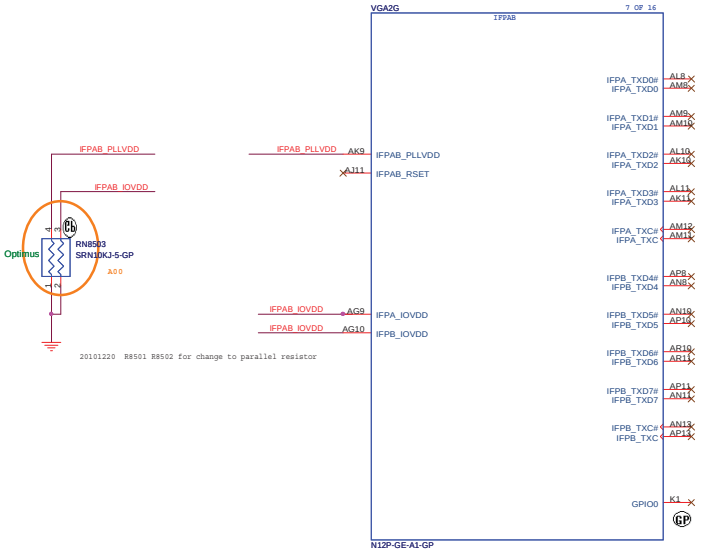
If a DAC interface is not required, it should be disabled by:
1. Adding a pull-down to the DACx_VDD with a 10 kilohm resistor to GND.
2. All other DAC I/O pins can be left floating.

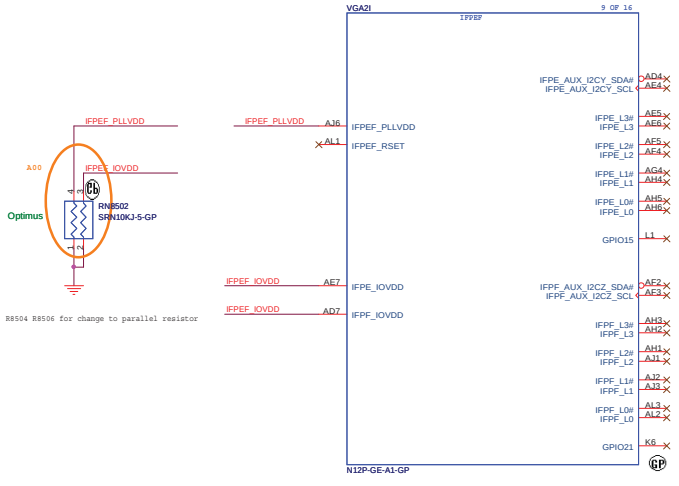


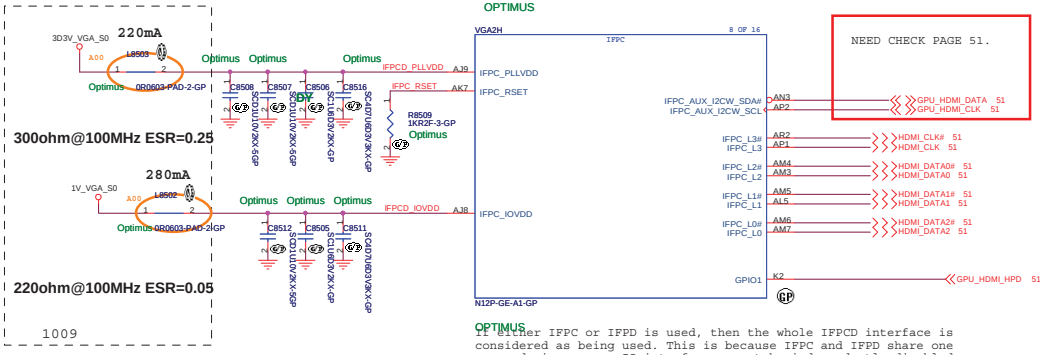


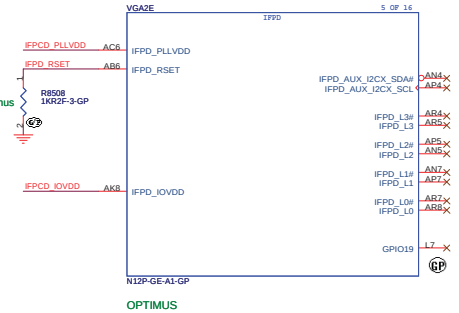
In Optimus mode the GPU does not drive certain interfaces. These interfaces should be treated as unused and appropriate terminations per the GPU design guide should be applied th the signal or the power supply block.

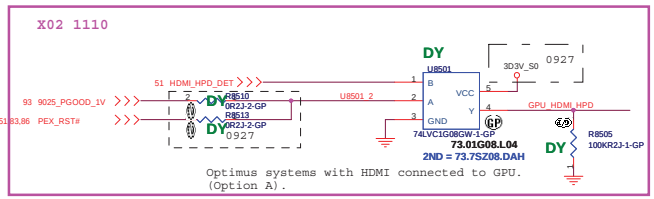
The following guidelines only apply to a fully unused IFP macro:
1. Pull down IFPxy_IOVDD with 10 kilohm resistor.
2. Pull down IFPxy_PLLVDD with 10 kilohm resistor.
3. The other IO pins can be NC; this includes unused data lines.



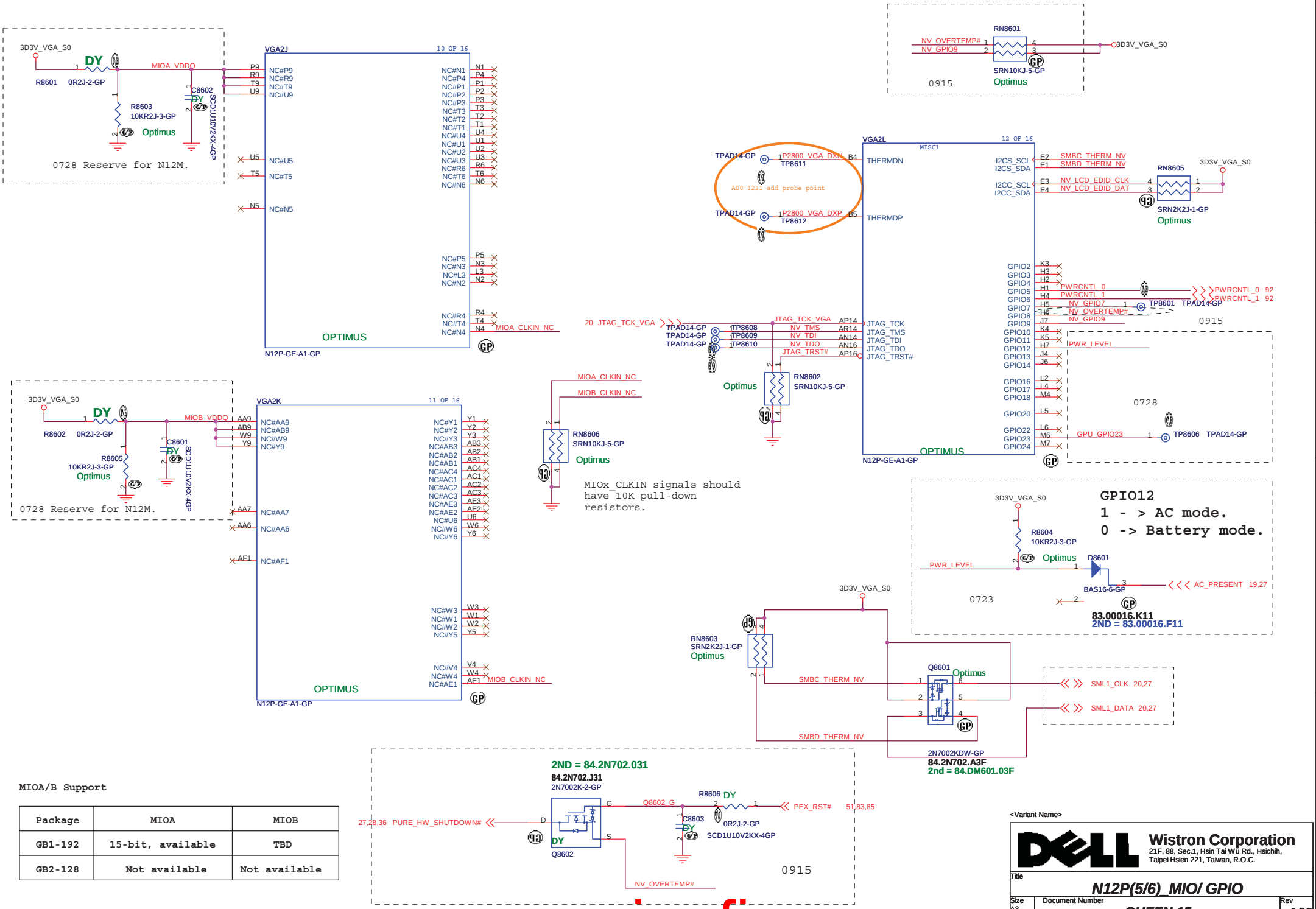








<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N12P(3/6) DAC
Size A2
Document Number QUEEN 15
Rev A00
Date: Tuesday, January 04, 2011
Sheet 85 of 108



MIOA/B Support

Package	MIOA	MIOB
GB1-192	15-bit, available	TBD
GB2-128	Not available	Not available

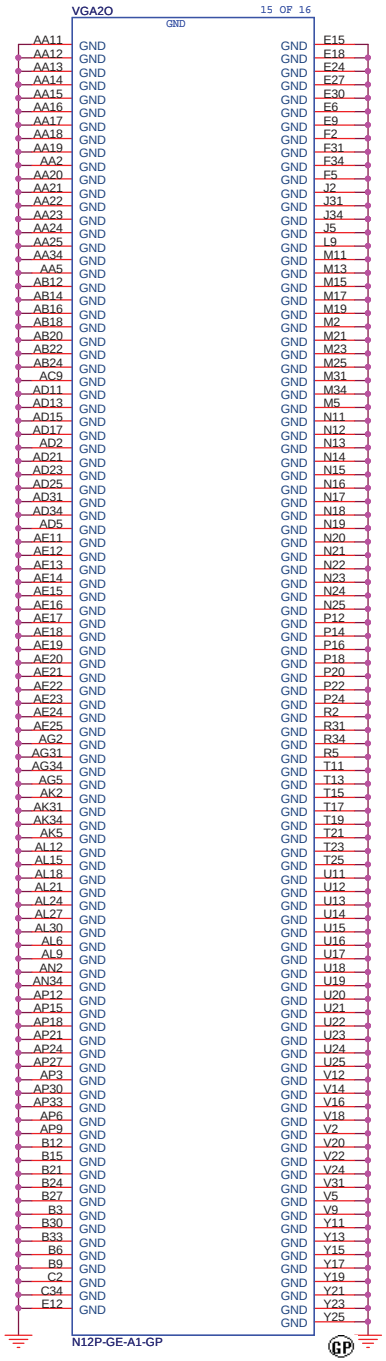
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

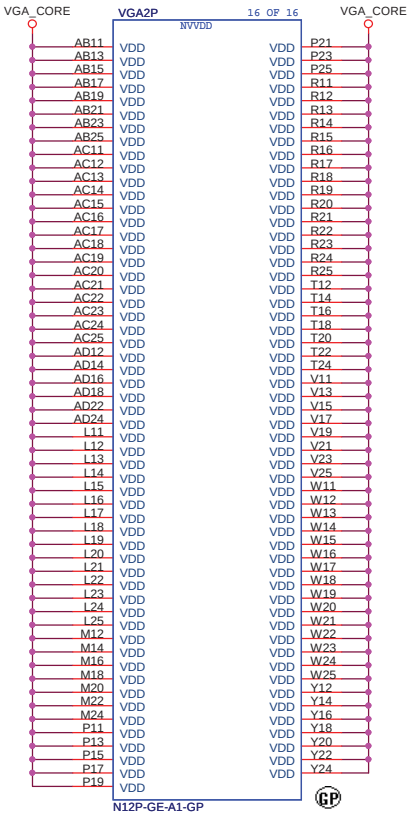
Title: N12P(5/6)_MIO/ GPIO

Size: A3 | Document Number: QUEEN 15 | Rev: A00

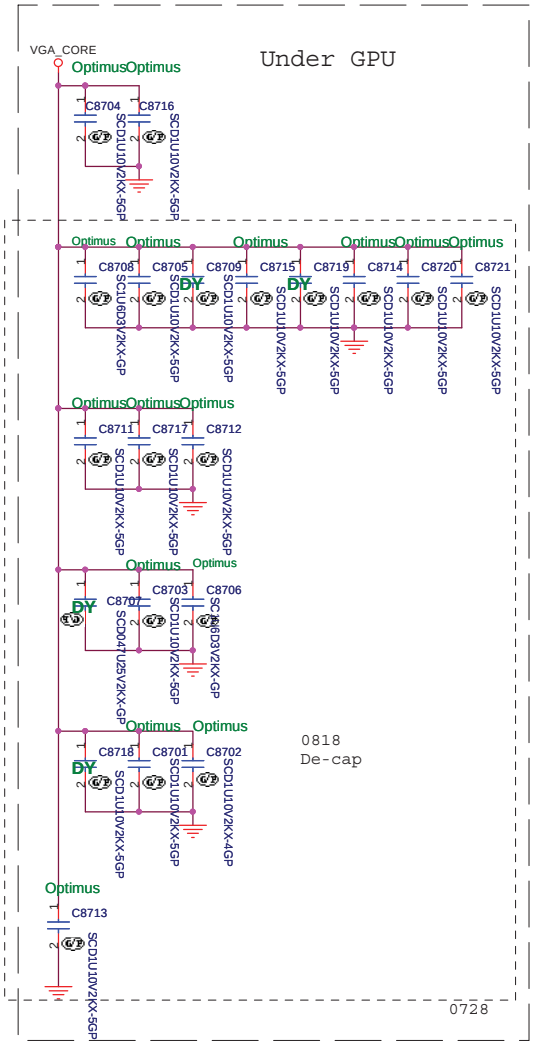
Date: Tuesday, January 04, 2011 | Sheet 86 of 108

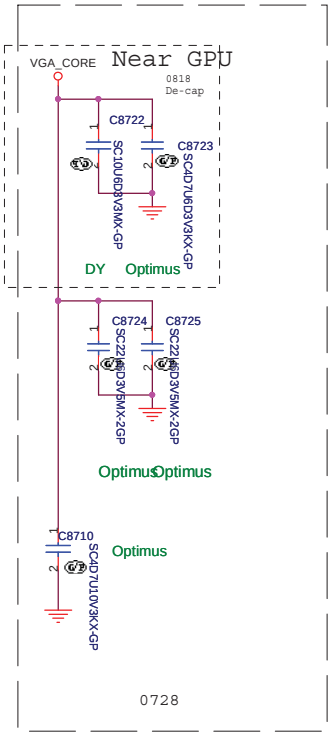


OPTIMUS



OPTIMUS





<Variant Name>

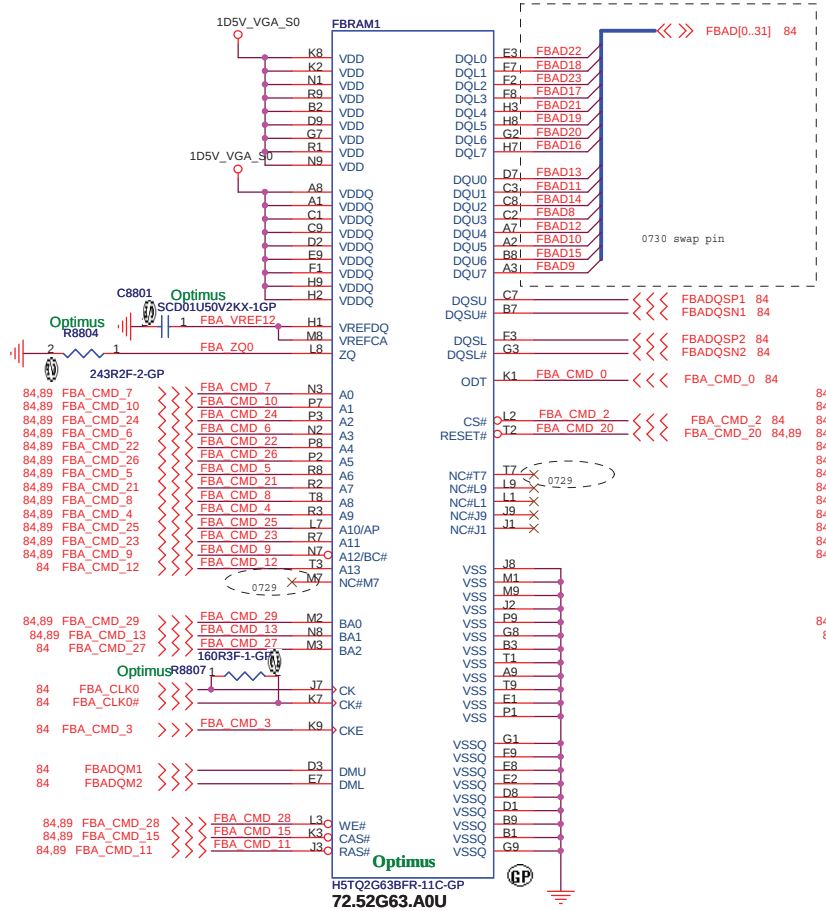
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

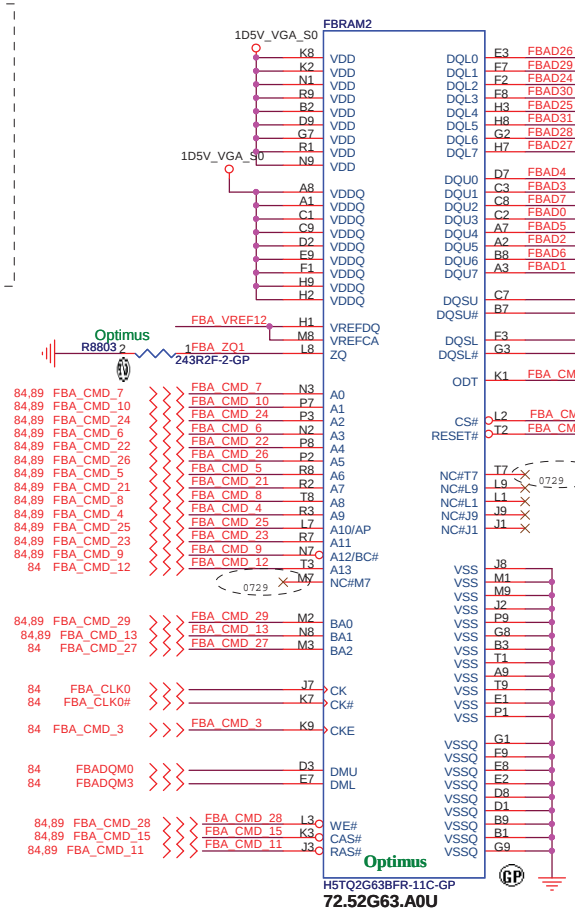
Title: N12P(6/6)_POWER

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 87 of 108

Frame Buffer Patition A Lower 32 bits.

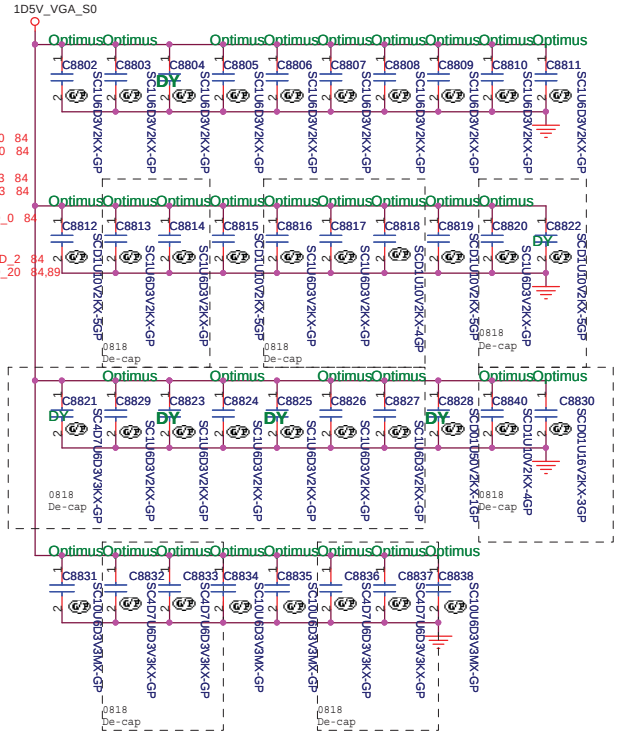




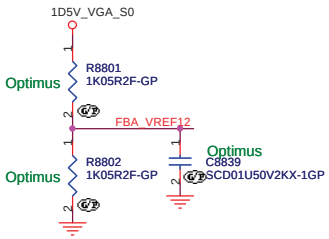
2nd = 72.41164.I0U

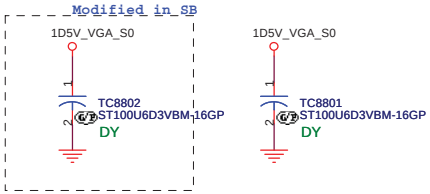
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133H48) from BGA96D0913H48



GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function 0..31	32..63
CMD25	CMD0	ODT	
CMD23	CMD1	CS1*	
CMD2	CMD2	CS0*	
CMD0	CMD3	CKE	
CMD10	CMD4	A9	A11
CMD26	CMD5	A6	A7
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	RAS*	RAS*
CMD18	CMD12	A13	A14
CMD9	CMD13	BA1	A3
CMD29	CMD14	A14	A13
CMD8	CMD15	CAS*	CAS*
CMD27	CMD16		CKE
CMD15	CMD17		CS1*
CMD11	CMD18		CS0*
CMD16	CMD19		ODT
CMD28	CMD20	RST	RST
CMD3	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A15
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD30	CMD30	A15	BA2





<Variant Name>

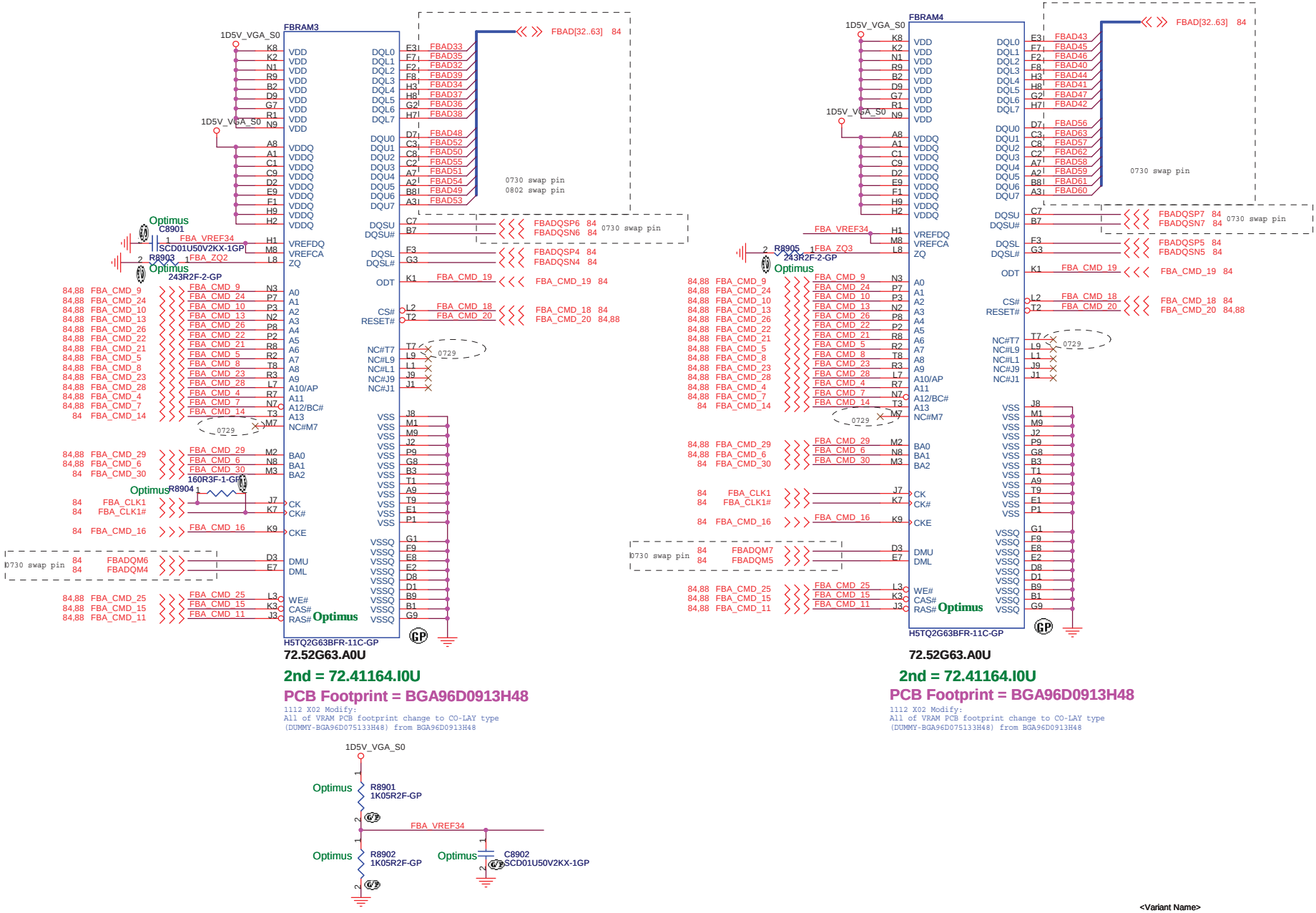
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(1/4)

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 88 of 108

Frame Buffer Patition A Upper 32 bits.



<Variant Name>

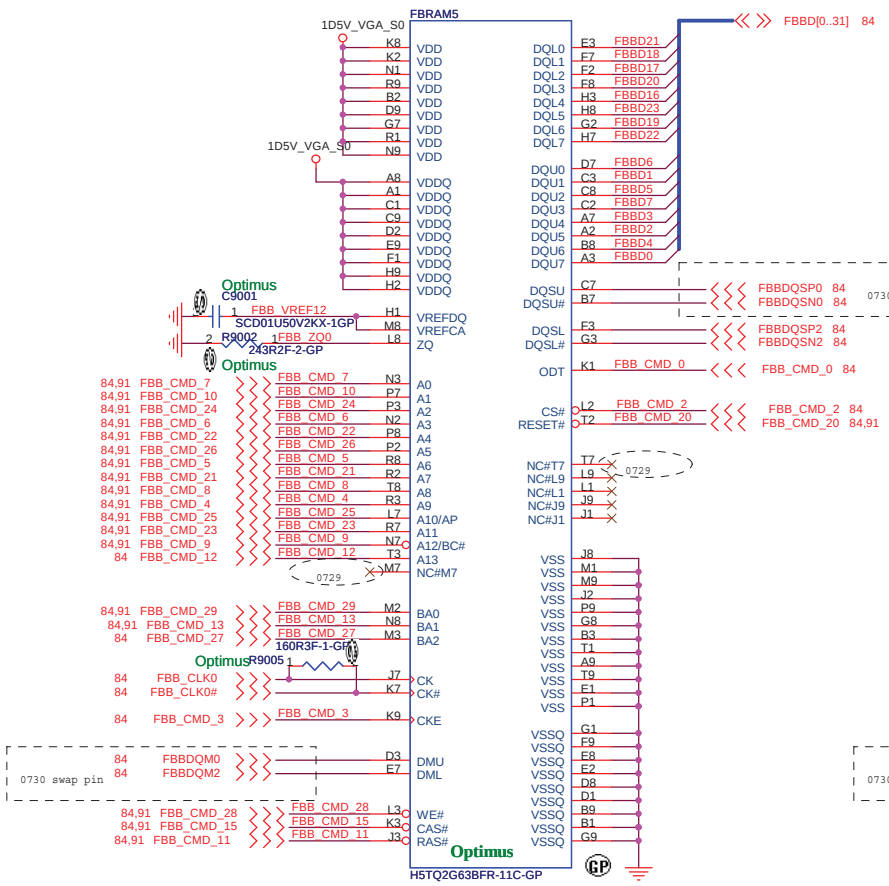
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(2/4)

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 89 of 108

Frame Buffer Patition B Lower 32 bits.

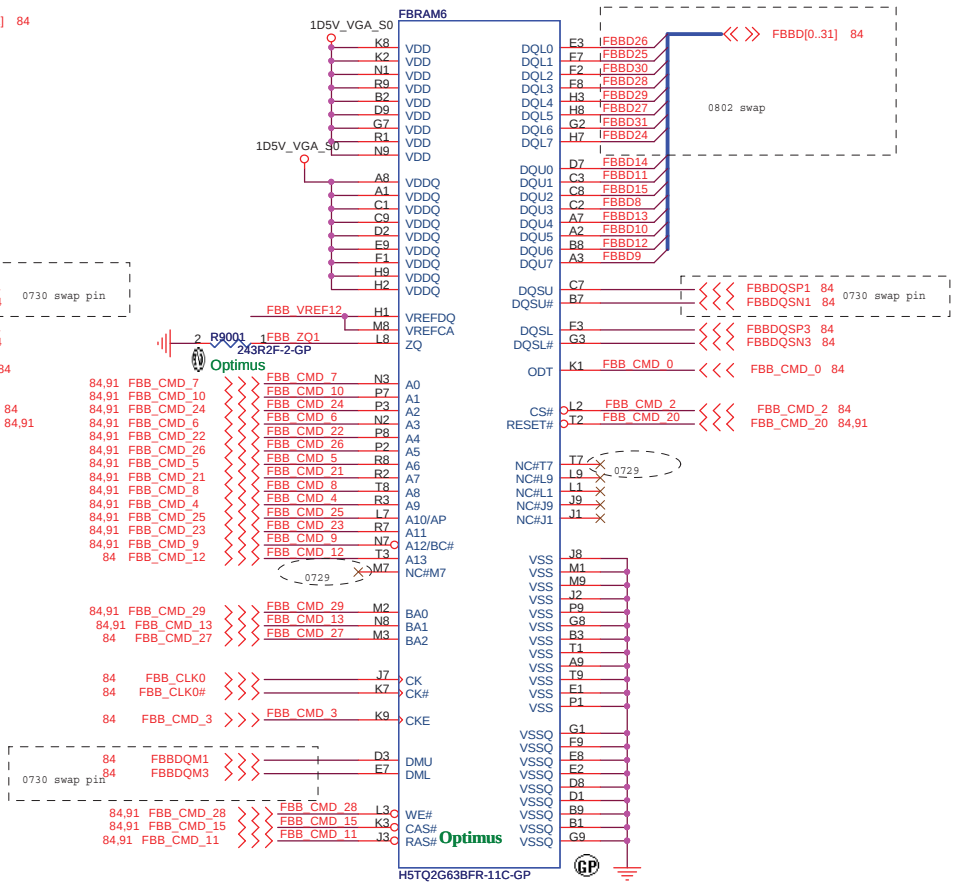


72.52G63.A0U

2nd = 72.41164.I0U

PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133H48) from BGA96D0913H48

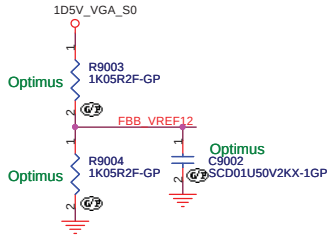


72.52G63.A0U

2nd = 72.41164.I0U

PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133H48) from BGA96D0913H48



<Variant Name>

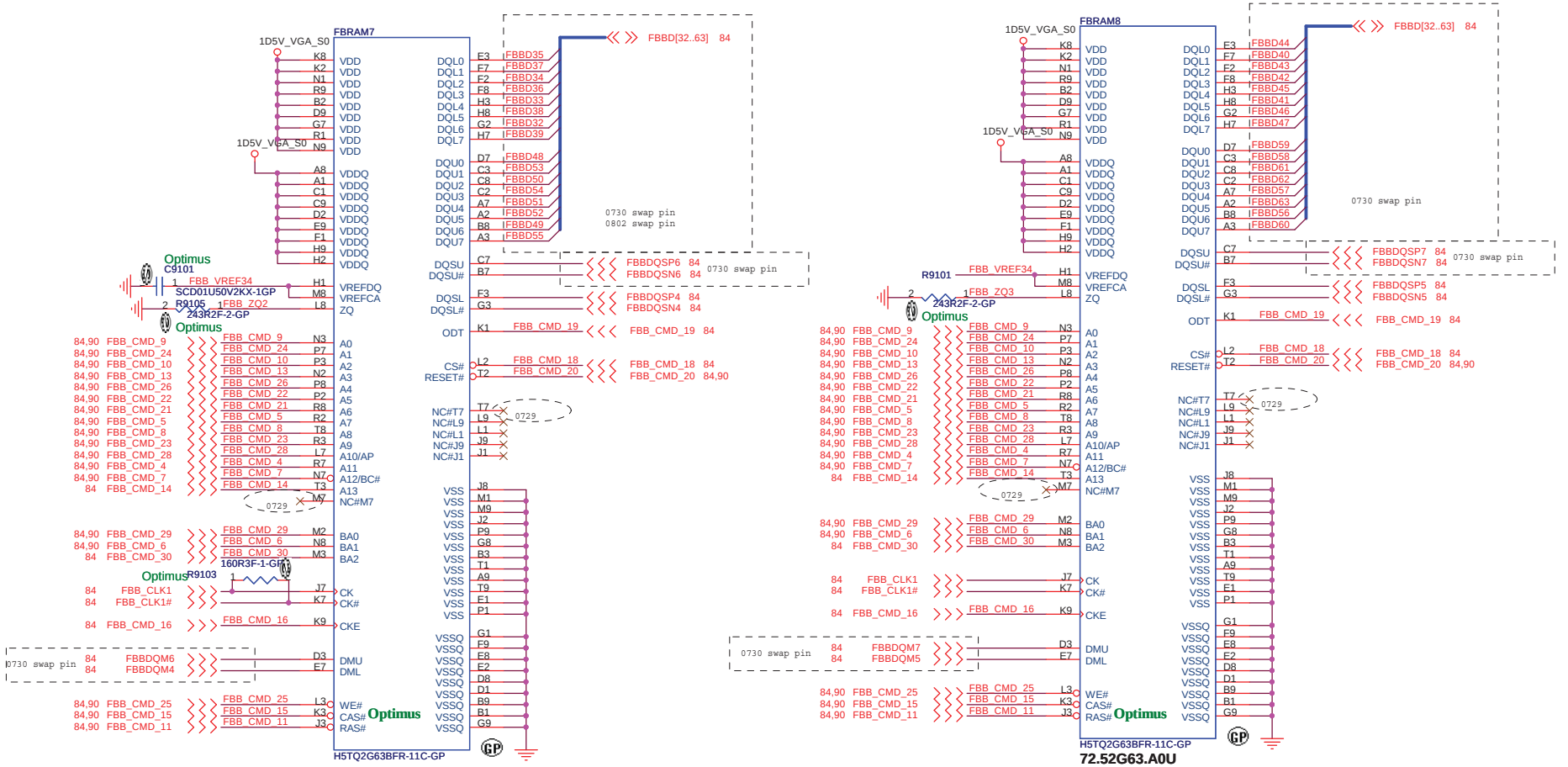
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(3/4)

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 90 of 108

Frame Buffer Patition B Upper 32 bits.



72.52G63.A0U

2nd = 72.41164.I0U

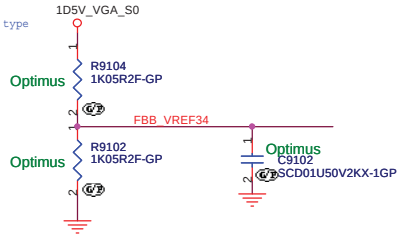
PCB Footprint = BGA96D0913H48

72.52G63.A0U

2nd = 72.41164.I0U

PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133H48) from BGA96D0913H48



1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133H48) from BGA96D0913H48

<Variant Name>

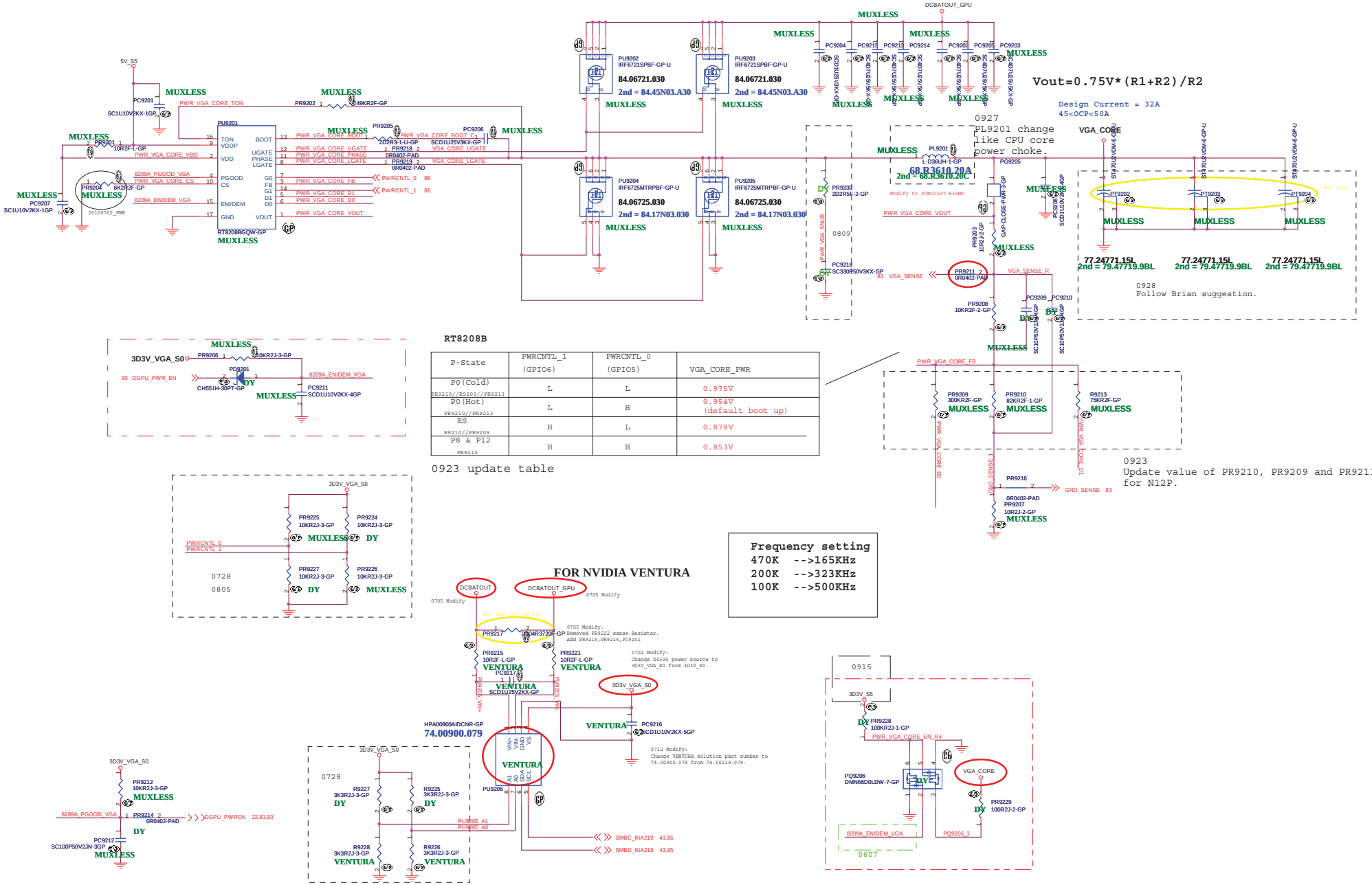
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(4/4)

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 91 of 108

SSID = PWR.Plane.Regulator_GFX



RT8208B

P-State	PWRCNTL_1 (GPIO6)	PWRCNTL_0 (GPIO5)	VGA_CORE_PWR
P0(Cold) PR9210//R9209//PR9213	L	L	0.975V
P0(Hot) PR9210//PR9213	L	H	0.954V (default boot up)
ES R9210//PR9209	H	L	0.878V
P8 & P12 PR9210	H	H	0.853V

0923 update table

0923
Update value of PR9210, PR9209 and PR9213 for N12P.

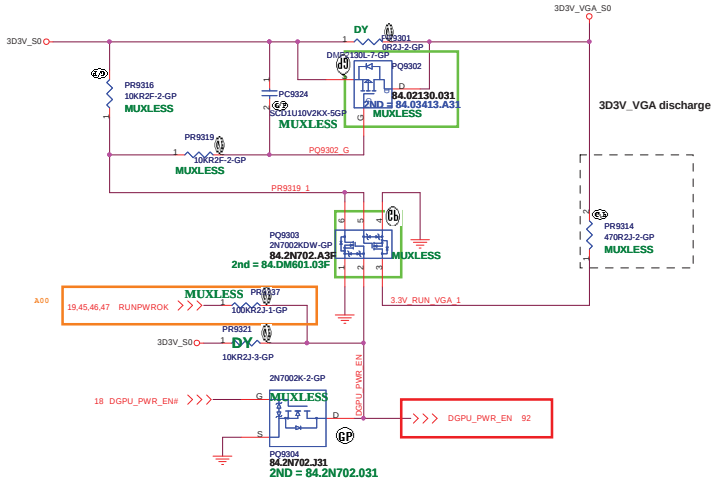
Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC_VGA CORE_RT8208A
Size: Document Number: QUEEN 15 Rev: A00
Date: Tuesday, January 04, 2011 Sheet 92 of 108

3D3V_S0 to 3D3V_VGA_S0 Transfer



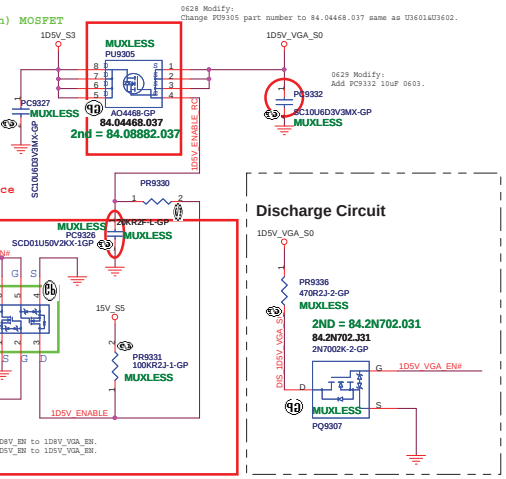
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

NV do not need 1.8V

1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm

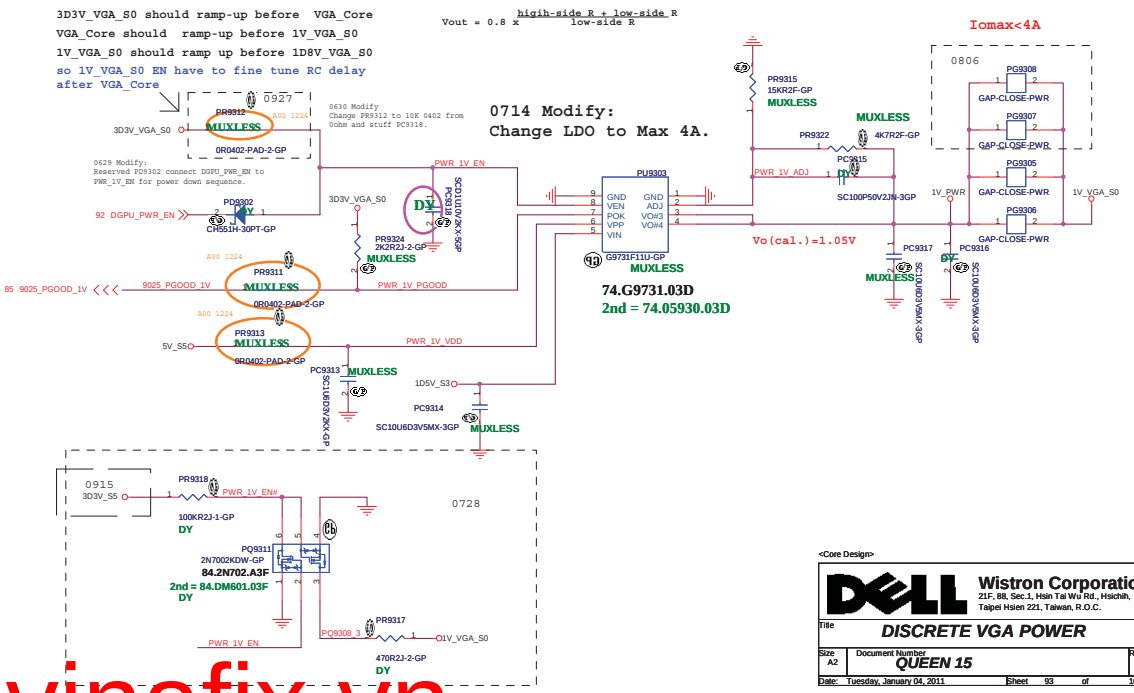


G9731F11U-GP for 1V_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

$$Vout = 0.8 \times \frac{\text{high-side R + low-side R}}{\text{low-side R}}$$

0714 Modify:
Change LDO to Max 4A.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 93 of 108

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 94 of 108

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT_Switch		
Size: A3	Document Number: QUEEN 15	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 95 of 108	

SSID = SDIO

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 96 of 108

H2
HOLE335R115-GP
ZZ.00PAD.D01
DY

H6
HOLE237R95-GP
ZZ.00PAD.921
DY

H9
HOLE335R115-GP
ZZ.00PAD.D01
DY

H10
HOLE335R115-GP
ZZ.00PAD.D01
DY

H3
HOLE256R126-GP
ZZ.00PAD.J01

H4
HOLE256R126-GP
ZZ.00PAD.J01

H11
HOLE256R126-GP
ZZ.00PAD.J01

H12
HOLE256R126-GP
ZZ.00PAD.J01

CPU Thermal module hole

HTML1
HOLE197R166-GP
DY

HTML2
HOLE197R166-GP
DY

HTML3
HOLE197R166-GP
DY

stand off

0721 Modify:
Removed SPR1

Check test point

0624 Modify:
Removed AFTP1,AFTP7~AFTP13.

H1
HT10X10BE10R32-D-5-GP
DY
ZZ.00PAD.J91

H5
HT10X10BE10R32-D-5-GP
DY
ZZ.00PAD.J91

H13
HT10X10BE10R32-D-5-GP
DY
ZZ.00PAD.J91

H7
HT10X10BE10R32-D-5-GP
DY
ZZ.00PAD.J91

H15
HT10X10BE10R32-D-5-GP
DY
ZZ.00PAD.J91

0901

RF CAP

0915 X01 Modify:
Reserved EC9701~EC9723 0.1uF for
RF suggestion.

1D5V_S3 EC9701 SCD1U50V3KX-GP DY
1D5V_S3 EC9702 SCD1U50V3KX-GP DY
5V_S0 EC9703 SCD1U50V3KX-GP DY
5V_S0 EC9704 SCD1U50V3KX-GP DY
3D3V_S5 EC9705 SCD1U50V3KX-GP DY
3D3V_S5 EC9706 SCD1U50V3KX-GP DY
3D3V_S5 EC9707 SCD1U50V3KX-GP DY
SC47P50V3JN-GP
5V_S5 EC9708 SCD1U50V3KX-GP DY
3D3V_S0 EC9709 SCD22U50V3ZY-1GP DY
DCBATOUT EC9710 SCD1U50V3KX-GP DY
5V_S5 EC9711 SCD1U50V3KX-GP DY

5V_S5 EC9724 SCD1U50V3KX-GP DY
DCBATOUT EC9723 SCD1U50V3KX-GP DY
1D05V_VTT EC9727 SCD1U50V3KX-GP DY
1D5V_S3 EC9731 SCD1U50V3KX-GP DY
DCBATOUT EC9728 SCD1U50V3KX-GP DY
3D3V_S0 EC9729 SC470P50V2-2-GP
3D3V_S0 EC9730 SC470P50V2-2-GP
5V_S0 EC9732 SCD1U50V3KX-GP DY
5V_S0 EC9733 SCD1U50V3KX-GP DY
3D3V_S5 EC9725 SCD1U50V3KX-GP DY
3D3V_S5 EC9726 SCD1U50V3KX-GP DY
3D3V_S0 EC9739 SC47P50V3JN-GP

3D3V_S0 EC9701 SCD1U10V2KX-4GP DY
EC9702 SCD1U10V2KX-4GP DY
1D8V_S0 EC9703 SCD1U10V2KX-4GP DY
DCBATOUT EC9704 SCD1U50V3KX-GP DY 1D8V_S0
DCBATOUT EC9705 SCD1U50V3KX-GP DY
EC9706 SCD1U50V3KX-GP DY
EC9707 SCD1U50V3KX-GP DY
EC9708 SCD1U50V3KX-GP DY
EC9709 SCD1U50V3KX-GP DY
EC9710 SCD1U50V3KX-GP DY
DCBATOUT EC9711 SCD1U50V3KX-GP DY 3D3V_S0
1D5V_S3 EC9712 SCD1U10V2KX-4GP DY
1D5V_S3 EC9713 SCD1U10V2KX-4GP DY
1D5V_S3 EC9714 SCD1U10V2KX-4GP DY
1D5V_S0 EC9715 SCD1U10V2KX-4GP DY

0802 For EMI/ESD.

GPU Thermal module hole

HHD1
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.401
3rd = 34.4CK01.501

HGPU1
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.401
3rd = 34.4CK01.501

HGPU2
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.401
3rd = 34.4CK01.501

HHD4
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.401
3rd = 34.4CK01.501

HBT1
STF237R117H123-GP
DY
34.4DM11.001
2nd = 34.4A902.001

0818

A00 0103 add 3rd LIDON(34.4CK01.501) on HDD1,HDD4,HGPU1,HGPU2 at XBuild [illegible] run

<Variant Name>

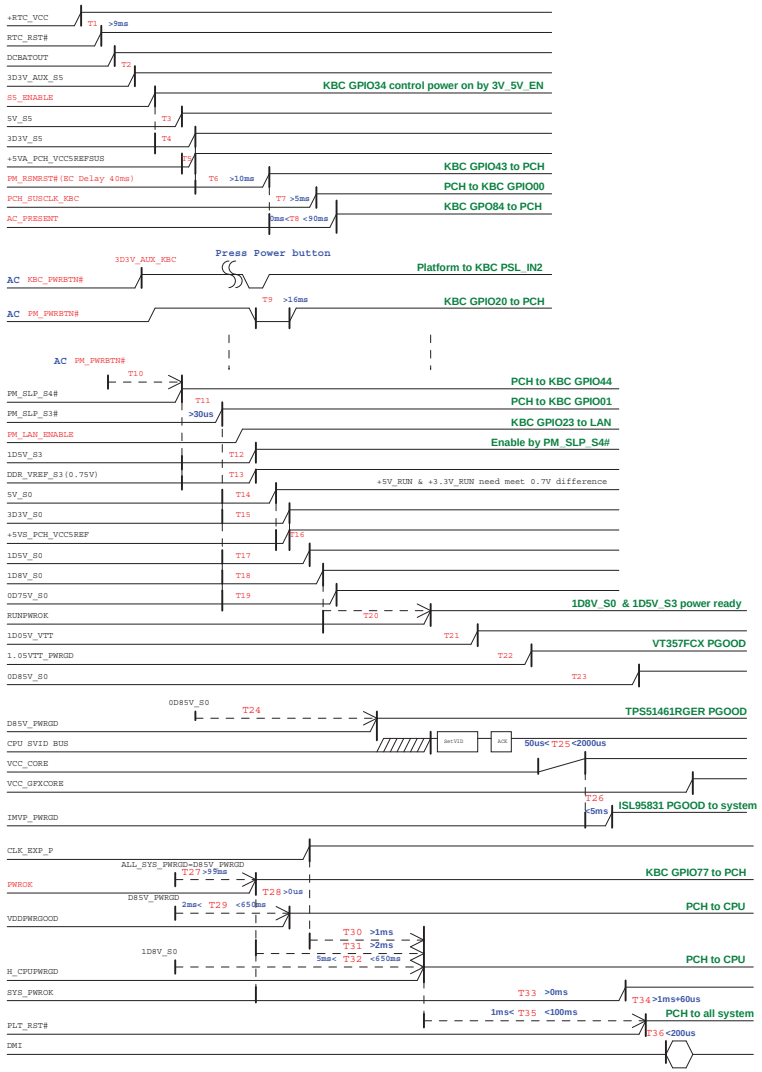
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: QUEEN 15
Rev: A00
Date: Tuesday, January 04, 2011
Sheet 97 of 108

Huron River Platform Power Sequence

(AC mode)

red word: KBC GPIO



Within logic high level and disable if it is less than the logic low level.

VGREF_DQG must be powered up before VccDmi3_1, or after VccDmi3_3 within 0.7 V. Also, VGREF_DQG must power down after VccDmi3_3, or before VccDmi3_1 within 0.7 V.

Not floating.

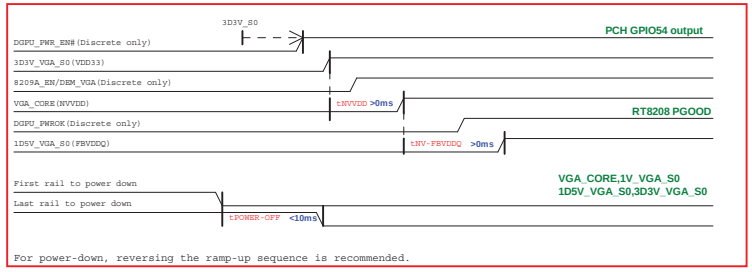
Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.

VGREF must be powered up before Vccl_A, or after Vccl_3 within 0.7 V. Also, VGREF must power down after Vccl_A, or before Vccl_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

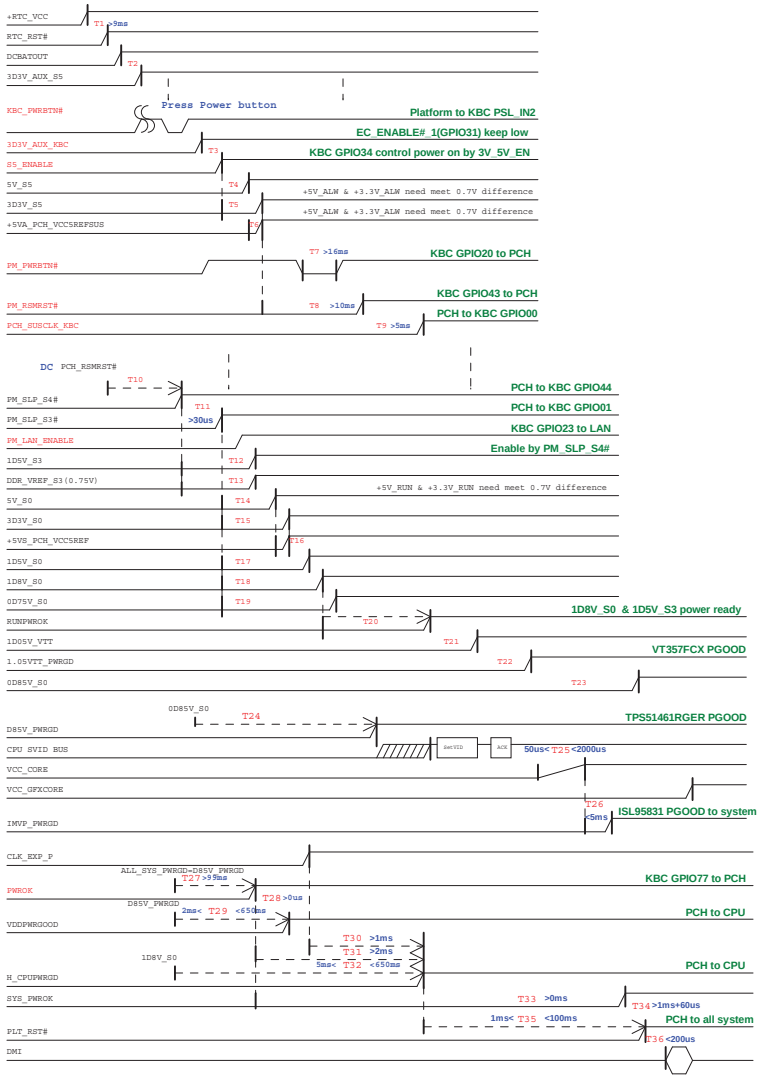
N12P-GE Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



Sense the power button status

VGREF must be powered up before VccDmi3_1, or after VccDmi3_3 within 0.7 V. Also, VGREF must power down after VccDmi3_3, or before VccDmi3_1 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

<Core Design>

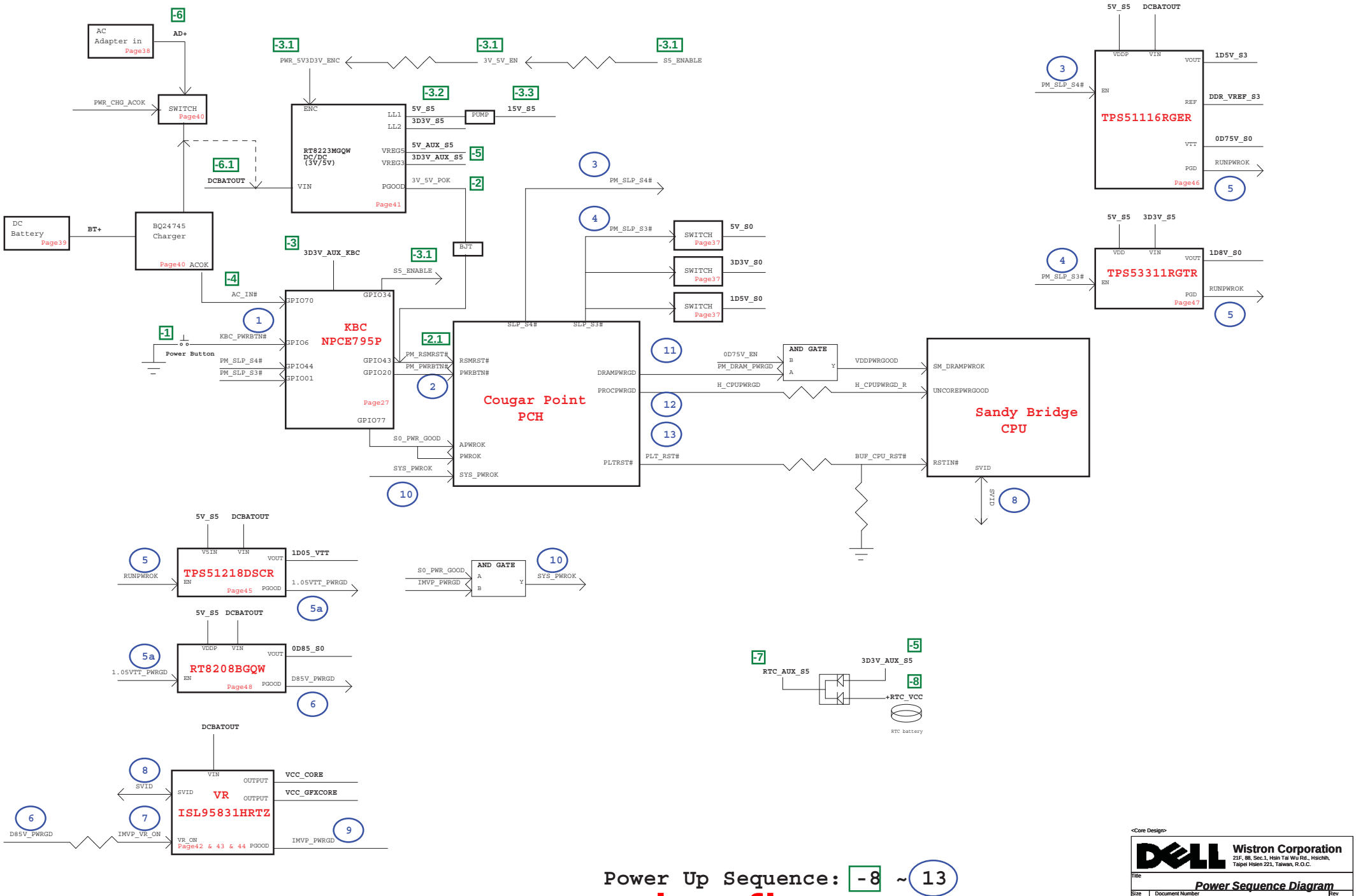
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size: A1 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 58 of 108

Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

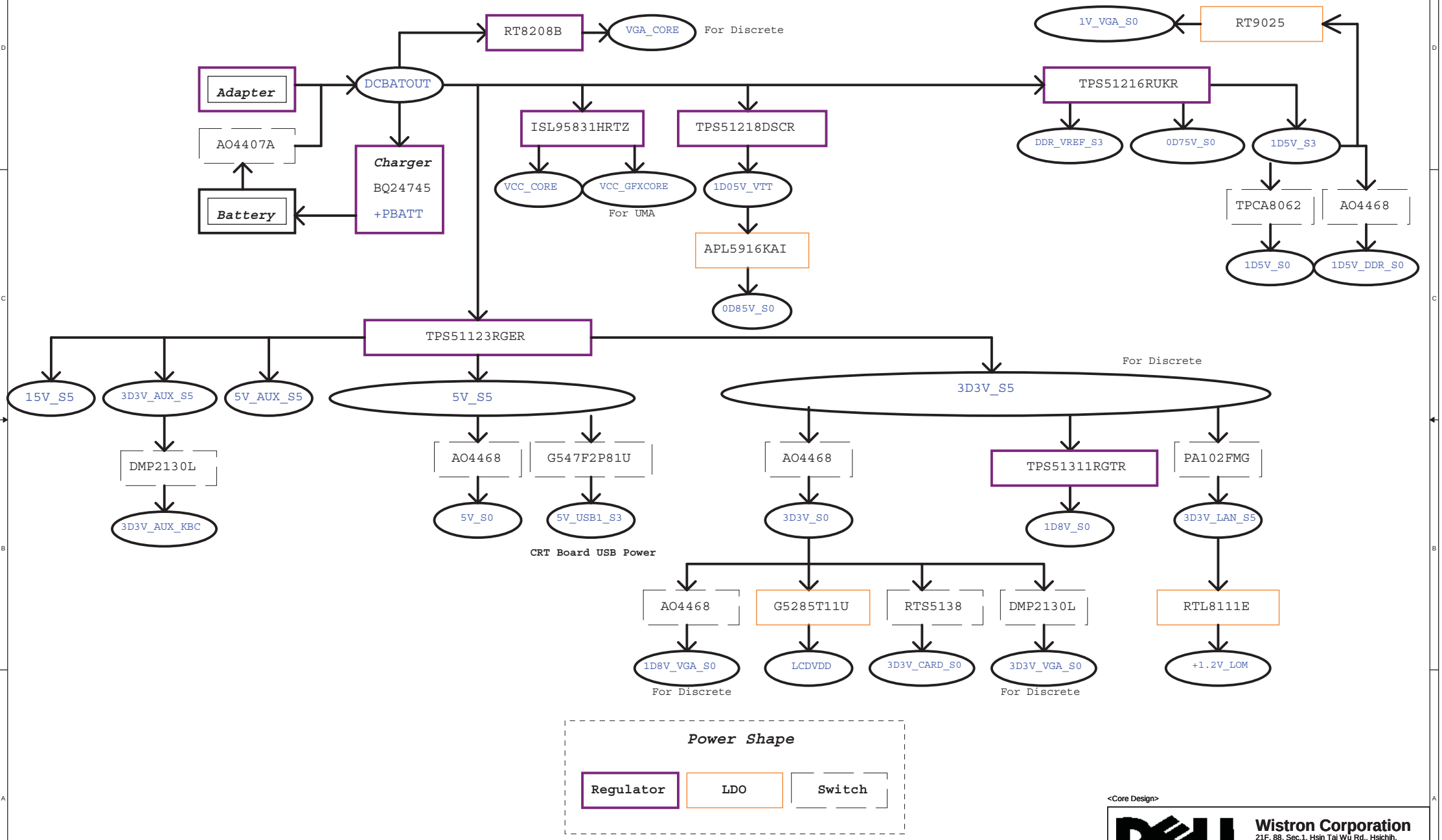
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Diagram

Size: A2 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 99 of 108



<Core Design>

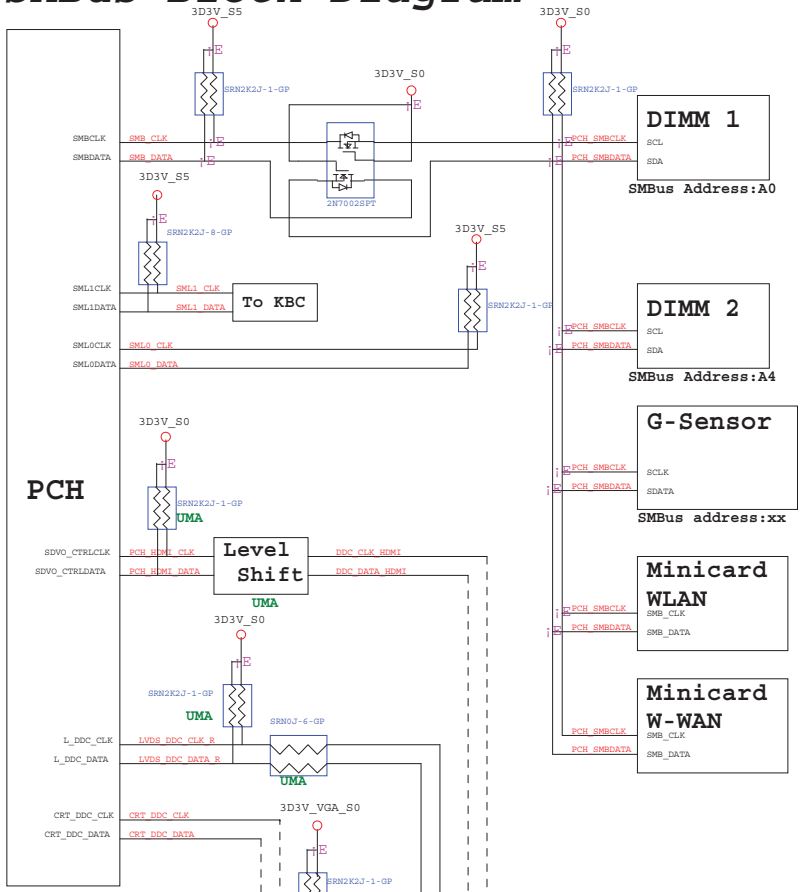
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

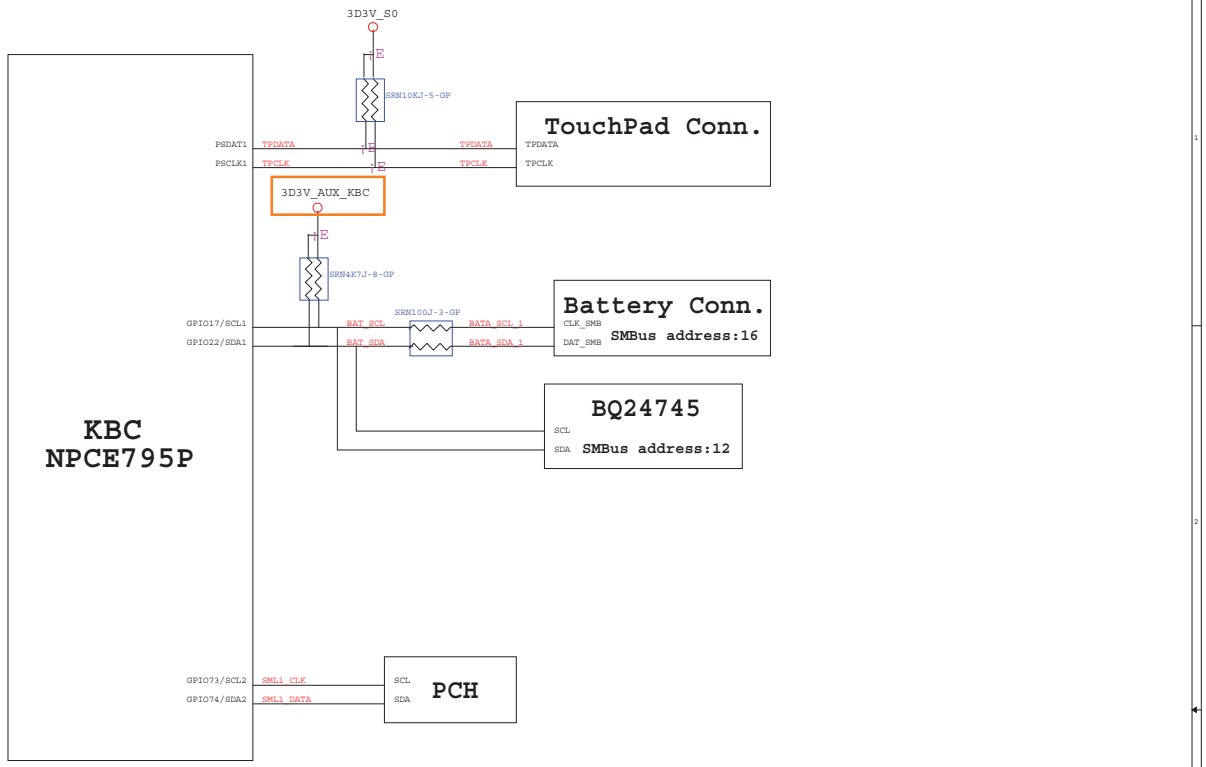
Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 100 of 108

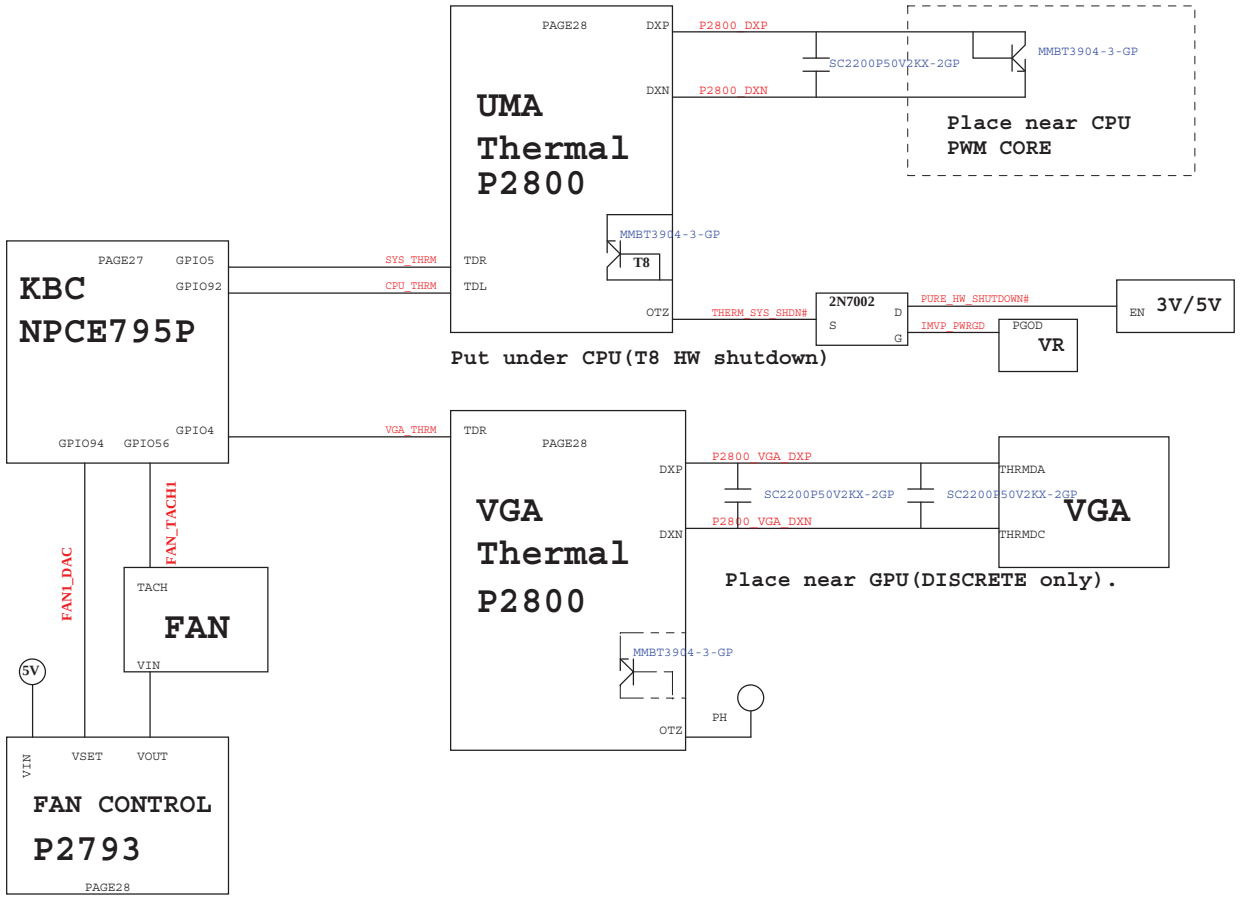
PCH SMBus Block Diagram



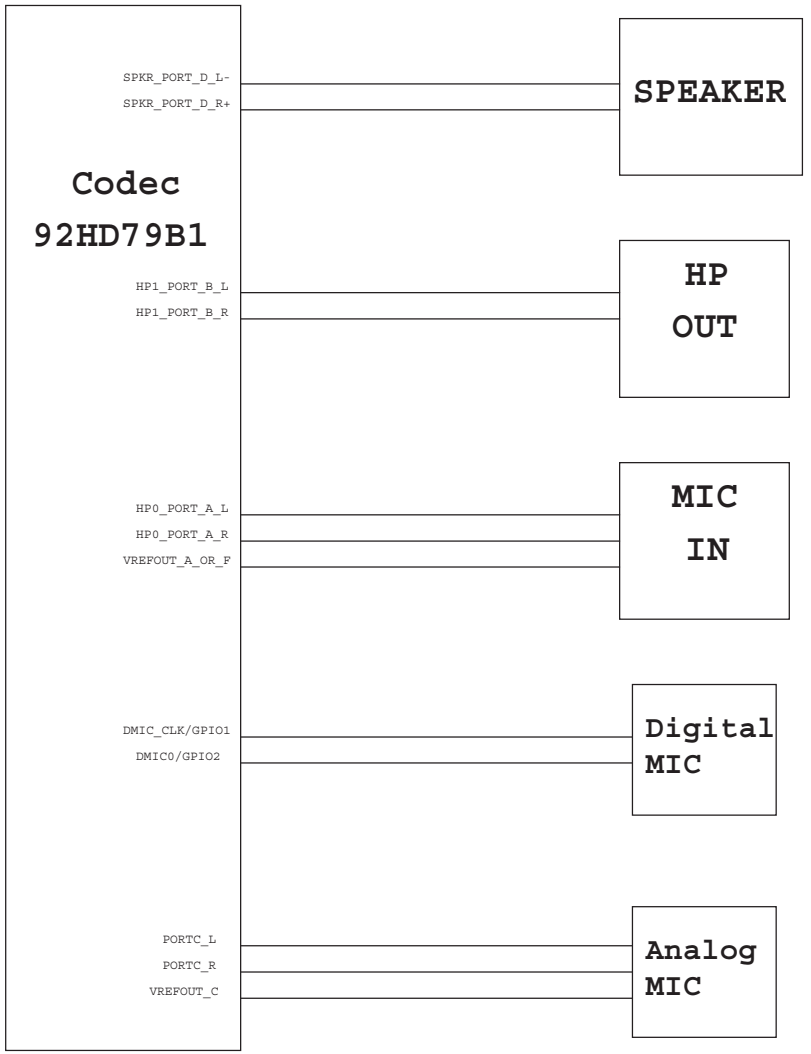
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 102 of 108

VERSION	DATA	PAGE	Change Iteam
X01	08/25	14	SWAP SA0_DM1 and SA1_DIM1 each other for DM2 can't boot up issue.
	08/29	28	Change U2802 Main source to 74.00991.031, 2nd 74.02793.A31,3rd 74.05606.071
	08/29	61	Add 2nd 77.C1071.20L on TC6101.
	08/29	64	Re-assign FP1 pin define.
	08/29	71	Un-stuff Debug port connector(DB1) on X01.
	08/29	37	Change U3701 pin2 to RUNPWROK from 0D75V_EN. Reserved R3717 0ohm between PM_DRAM_PWRGD and VDDPWRGOOD_R.
	08/29	37	Change R2724 to 20K 0402 from 10K for X01 stage.
	08/29	40	Change 3D3V_AUX_S5 to 3D3V_AUX_KBC to avoid leakage Voltage to 3D3V_AUX_KBC under DC mode.
	08/31	51	HDMI1 change to 22.10296.311 from 22.10296.271
	08/31	28	FAN1 change to 20.F0772.003 from 20.F1639.004
	08/31	57	E-SATA1 change to 22.10321.W11 from 22.10290.141
	09/01	41	PU4104 and PU 4105 horizontally mirror.
	09/01	83	R8305 Change to 30K ohm.
	09/01	97	H1, H5, H13, H7 and H15 change to ZZ.00PAD.J91 from ZZ.00PAD.D01.
	09/01	56	HDD1 add 2nd=62.10065.121.
	09/01	79	U7901 change main source to 74.00351.0B3.
	09/01	42	PR4226 change to 5.62K ohm.
	09/01	45	PTC4502 change to 79.3971V.30L.
	09/03	61	U6101 add 2nd=74.00547.079.
	09/03	49	U4901 add 2nd=74.09724.09F.
	09/03	40	PU4002 and PU4003 add 2nd=84.P1403.B37.
	09/03	24	L2401,L2402,L2403 add 2nd=68.10090.10B.
	09/03	27	DY C2713. Add C2722.
	09/03	47	Add PR4702
	09/03	22	Change FFS_INT2_R from PCH GPIO48 to GPIO15 Removed R2220 and change R2201 default pull up to pull down.
	09/06	20	X2001 add 3rd=82.30020.A31.
	09/06	56	U5601 add 2nd=74.02191.079.
	09/06	93	PU9303 add 2nd=74.05930.03D.
	09/06	37	U3701 add 2nd=73.7SZ08.DAH.
	09/06	23	Add 2nd and 3rd for L2301.
	09/06	23	R434 change name to PR9321. Add PC9324 and PR9319 for soft start.
	09/06	61	TC6101=80.10715.B1L, 2nd=77.C1071.21L, 3rd=77.C1071.20L.
	09/06	56	ODD1 add 2nd and 3rd source. HDD1 add 3rd source.
	09/06	49	LCD1 add 2nd source.
	09/06	69	TPAD1 add 2nd.

VERSION	DATA	PAGE	Change Iteam
X01	09/06	15	DM1 2nd=62.10017.Q31, 3rd=62.10017.K01.
	09/06	14	DM2 2nd=62.10017.P31, 3rd=62.10017.K11.
	09/07	68	Add 2nd source 20.K0343.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/07	69	Add 2nd source 20.K0343.004 on KBLIT1 base on updated connector list.
	09/07	82	Add 2nd source 20.F0085.040 on CRTBD1 base on updated connector list.
	09/07	64	Add 2nd source 20.K0382.006 on FP1 base on updated connector list.
	09/07	75	Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.
	09/07	4~10	Updated CPU1 footprint to SKT-BGA989C470395-1H180 from SKT-BGA989C470395-1H186 base on data base updated. Add 2nd source 62.10040.771 on CPU1 base on updated connector list.
	09/07	75	Change CARD1 to 20.I0129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.
	09/07	93	PQ9308 change name to PQ9311.
	09/07	ALL	Change all of single 2N7002 to 84.2N702.J31 from 84.2N702.D31 due to 84.2N702.D31 will EOL.
	09/07	28	Change U2801,U2803 to 74.02800.A71 from 74.02800.071 from vender updated parts. Change R2803&R2817 to 107K from 499K,R2804&R2818 to 226K from 102K base on updated ADJ Table.
	09/08	18, 22	Change FFS_INT2_R from PCH GPIO48 to GPIO14 Keep PCH_GPIO5 PH R2201,PCH_GPIO48 PH R2220. Add R1818.
	09/08	82	1.Rename IOBD1 pin20,22,26,28 to IOBD1_20,22,26,28 from PCIE_TXN5,PCIE_TXP5,PCIE_RXP5,PCIE_RXN5. 2.Add RN8207,RN8208 for optional USB3.0 PCIE or USB2.0 signal.
	09/08	18	Reserved USBP9~USBP10 to IOBD1 pin20,22,26,28.
	09/08	37	Stuff Q3704,R3710; un-stuff R3716. U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.
	09/08	20	DY R2002.
	09/08	47	Mount PC4710.
	09/08	98	Update N12P power sequence.
	09/09	82	R8201, R8202 and R8203 change to 62 ohm.
	09/10	45	Change PL4501 to 68.2R210.20C from IND-D56UH-27-GP base on Brian updated.
	09/10	41	Change PL4101,PL4102 to 68.2R210.20B from 68.2R210.20Q base on Brian updated.
	09/10	82	Rename IOBD1 pin14 to IOBD1_14 from USB30_SMI#. Add R8207 for USB20 USB_OC#10_11 Add R8206 for USB30 USB30_SMI# Add R8208 for USB20 USB signal. Add R8207 for USB30 PCIE signal.
	09/10	49	Add TPNL1 for touch panel solution 4pin connector. Change LCD1 to 20.F1816.030 for 30pin Re-assign LCD1 pin define base on Roy updated cable pin define list.
	09/10	51	Change HDMI1 part number to 22.10296.331 from 22.10296.311 base on ME Double updated.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 103 of 108

VERSION	DATA	PAGE	Change Iteam
X01	09/13	83	Change X8501 to 82.30034.641;2nd 82.30034.651;3rd 82.30034.681 from sourcer suggestion.
	09/13		Change KBLIT1, PWRBTN2 and TPAD1 2nd source from 20.K0343.004 to 20.K0382.004.
	09/13	47	Change 1.8V power solution.
	09/14	82	Change R8201~R8203 to 470ohm from 100ohm. Add RN8209 PH 5V_S5 on MEDIA_LED1~3# for PWM OD mode.
	09/14	40	Add 2nd source 84.04835.H37 on PU4002,PU4003 base on Brian updated 2nd source excel file.
	09/14	58	Change SPK1 to 20.F0772.004 from 20.F1647.004 from Double updated.
	09/14	51	Add R5101~R5108and reserved TR5101~TR5104 on all of HDMI differential pair for EMC suggestion. Rename HDMI1 CONN NET name.
	09/14	29	Add R2920,R2921 and reserved EC2901,EC2902 on AUD_DMIC_CLK &AUD_DMIC_IN0 for EMC suggestion.
	09/14	75	Add R7503,R7504 and reserved EC7501,EC7502 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion. Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R. Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C
	09/14	20	Reserved EC2004,EC2005 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion.
	09/14	49	Reserved EC4910~EC4915 on LVDS signal for EMC suggestion.
	09/15	58	Re-assign SPK1 pin define base on Roy updated excel file for 20.F0772.004
	09/15	51	Add 2nd source 22.10296.311 on HDMI1 from updated connector list.
	09/15	68	Add 2nd source 20.K0382.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	49	Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.
	09/15	28, 51,82	Add test point for WKS AFTE request.
	09/15	All	ADD 2nd source follow Power team suggestion.
	09/15	92, 93	Modify PR9318 and PR9228 power source from 3D3V_AUX_S5 to 3D3V_S5.
	09/15	86	Reserve Q8602, C8603 and R8606 for VGA over temp.
	09/15	20	RN2005 swap net.
	09/15	19	RN2005 swap net.
	09/15	48	Change PR4809 to 10K from 100K PH power source change to 3D3V_S0 from S5.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	97	Reserved EC9701~EC9723 0.1uF for RF suggestion.
	09/15	41	Un-stuff PU4101,PD4105,PR4124, PR4125,PR4101 at X01 stage for 5mW issue.
	09/15	69	un-stuff R6907 and stuff R6905,Q6902,R6906 for 5V drive CAP LED.
	09/17	82	Change IOBD1 part number to 20.F1849.080 base on Double updated latest DXF&EMN.
	09/17	49,57 32,64	stuff TR4901 and un-stuff R4911,R4912 at X01 stage from EMC Neo suggestion. stuff TR4902 and un-stuff R4908,R4909 at X01 stage from EMC Neo suggestion. stuff TR5701 and un-stuff R5718,R5719 at X01 stage from EMC Neo suggestion. stuff TR3201 and un-stuff R3211,R3210 at X01 stage from EMC Neo suggestion. stuff TR6401 and un-stuff R6403,R6404 at X01 stage from EMC Neo suggestion.
	09/17	20	Change RN2010~RN2016 to 33ohm from 0ohm from EMC Neo suggestion.
	09/17	37	Change R3710 to 100K from 0ohm to avoid impact 1.05VTT_PWRGD turn off sequence directly.
	09/17	17	Add R1703~R1705 on RGB signal and reserved EC1701~EC1703 0.1u from EMC Neo suggestion

VERSION	DATA	PAGE	Change Iteam
X01	09/17	40,41	Stuff EC4002 0.1uF from EMC Neo suggestion. Stuff EC4008 0.1uF from EMC Neo suggestion. Stuff EC4102,EC4103 0.1uF from EMC Neo suggestion. Stuff EC4107 0.1uF from EMC Neo suggestion. Stuff PC4119,PC4120 0.1uF from EMC Neo suggestion. Stuff EC4006,EC4007 0.1uF from EMC Neo suggestion.
	09/17	60,18	EC6001 change to 10p from 4.7p and default stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default stuff from Neo suggestion.
	09/17	44	default stuff EC4407,EC4405,EC4403,EC4410 base on EMC Neo suggestion.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	82	Change R8201~R8203 to 430ohm.
	09/17	48	Change PR4809 to 4.7K from 100K PH power source change to 3D3V_S0 from S5.
	09/17	40,27,83	Rename PCIE_RST# to AD_IA_HW2 on KBC GPIO50 for power Tom suggest. Reserved PQ4004,PR4036,PR4037 for AD_IA_HW2 function.
	09/17	68	Rename CHARGER_LED1 to CHARGERLED1. Rename FPOWER_LED1 to FPOWERLED1. Rename HDD_LED1 to HDDLED1. Rename TP_LOCK_LED1 to TPLOCKLED1. Rename TP_LOCK_LED2 to TPLOCKLED2. Rename WLAN_LED1 to WLANLED1
	09/17	21,22	Base on layout routing,Add RN2104 10K instead of R2111 10K. Move EC_SCI#,DBC_EN to RN2201. Move S_GPIO to RN2103. Move PSW_CLR# to RN2104.
	09/17	56	Change R5605 to 100K from 10K and PH to 5V_S0 from 3D3V_S0 to meet Vgs>2V turn on.
	09/17	56	Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.
	09/17	ALL	Change all of 0402 0ohm to 0R0402 short pad. PR4008,PR4010,PR4012,PR4020,PR4023,PR4024,PR4027,PR4028,PR4029,PR4225PR4102,PR4113,PR4118, PR4121,PR4203,PR4204,PR4215,PR4222,PR4231,PR4243,PR4301,PR4509,PR4510,PR4801,PR4804,PR4805, PR4808,PR4810,PR9211 F4902,PR4017,PR4018,PR4106,PR4611,PR4710,PR4807,R2304,R2403,R2406,R2409,R2702,R2902,R2903,R2904 R2305
	09/20	9	Add 2nd for TC901.
	09/20	83	Add 2nd for L8303.
	09/20	82	Add 2nd for LD8201.
	09/20	86	Add 2nd for Q8601.
	09/20	83	Add R8321. C8353 and C8354 change to 12pF.
	09/20	82	Redefine IOBD1.
	09/20	75	AFTP111 and AFTP110 connect to USB_PP13_R and USB_PN13_R.
	09/20	51	Change P/N of Q5102.
	09/21	42	Change PU4201 VDD power source to 5V_S5 from 5V_S0 to avoid abnormal MVP_PWRGD waveform.
	09/21	47	stuff PC4714 22uF from Brian updated.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 104 of 108

VERSION	DATA	PAGE	Change Iteam
X01	09/21	45	Change PR4507 to 20K from 20.5K from Brian updated.
	09/21	46	Change PR4602 to 110K from 68K from Brian updated.
	09/21	42	Change PR4217 to 1.27K from 1K from Brian updated. Change PR4213 to 3.6K from 3.16K from Brian updated. Change PR4236 to 3.01K from 3.32K from Brian updated.
	09/21	44	Change PC4410 to 0.01u from 0.022uF from Brian updated.
	09/21	39	Add 2nd 83.00099.K11;3rd 83.00099.T11 on D3901,D3902,D3903 from Sourcer Eden suggestion.
	09/21	39	Add 2nd 84.02143.011;3rd 84.00143.N11 on 6801,Q6804,Q6805,Q6806,Q6807,Q6808 from Sourcer Eden suggestion.
	09/21	43	Change PU4303,PU4306,PU4309 dummy field only for QC CPU stuff. Change PC4307,PC4316 dummy field only for QC CPU stuff. Add 2nd for PTC4306.
	09/21	41	PD4101, PD4103, PD4104 and PD4105 add 2nd source.
	09/21	69	Q6902 add 2nd source.
	09/21	40	PD4001 add 2nd source.
	09/21	19	move PCH_WAKE# to RN1901 pin4;Add R1909 PH 100K on AC_PRESENT.
	09/21	37	R3710 change to 0ohm. Remove R3701 and C3701.
	09/21	42	Add PR4214, PC4230, PR4216 and PC4231 from Brian updated.
	09/23	20	RN2016, RN2010, RN2011, RN2012, RN2014 and RN 2013 keep 0ohm.
	09/23	ALL	PR9216, R504, R1812,R1813,R1815,R1817, R1903, R1906,R1910,R1912,R1913,R1924,R1925, R2213,R2219, R2711,R2720,R2733,R2761, R2807,R2814, R3708, R5125, R5127, R5721, R5722.
	09/23	75	Add R7505~R7508 0ohm and reserved EC7503~EC7506 on PCIE_TX8&RX8 signal base on EMC Lance suggestion. Add R7509,R7510 0ohm and reserved EC7507,EC7508 on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base on EMC Lance suggestion.
	09/23	ALL	RN5101, RN2201, RN1702, RN1901, RN1705 swap pin.
	09/23	79	DUMMY G-SENSOR.
	09/23	92	Update value of PR9210, PR9209 and PR9213 for N12P.
	09/23	43	PR4320 change to 4 m ohm.
	09/23	68	Add 2nd source 83.00110.J70 on FPOWERLED1,HDDLED1,WLANLED1 from Sourcer Anya suggestion. Add 2nd source 83.00326.G70 on CHARGERLED1from Sourcer Anya suggestion. Add 2nd source 83.00190.Z70 on TPLOCKLED1,TPLOCKLED2 from Sourcer Anya suggestion.
	09/23	69	Change KBLIT1 part number to 20.K0589.004 and re-assign pin define base on Roy updated.
	09/23	42, 44	Add 2nd source 69.60011.201 on PR4405,PR4245 from Sourcer Kitty suggestion.
	09/23	42	Add 2nd source 69.60037.021 on PR4246,PR4247 from Sourcer Kitty suggestion.
	09/24	23	Add 2nd source 68.00214.211 on L2301 updated from DN13ATI.
	09/24	68, 69	Change R6806,R6808,R6811~R6813,R6801,R6803,R6815,R6906 to 390ohm from 1K to fine tune all of MB LED for 5mA spec.
	09/27	51	Reserve R5114 and R5115.
	09/27	85	Reserve R8510 and R8513.
	09/27	83	DY U8301, mount R8323.
	09/27	92	R9206 change to 10K, PC9211 mount 0.1u.
	09/27	93	R9312 change to 1K.

VERSION	DATA	PAGE	Change Iteam
X01	09/27	49, 57 32, 64	TR4901, TR4902, TR5701, TR3201 and TR6401 DY. Stuff 0 ohm.
	09/27	69	AFTP73 connect to TP_VDD.
	09/27	85	U8501 power change to 3D3V_S0.
	09/27	92	PL9201 change like CPU core power choke.
	09/28	83, 84	L8303, L8401, L8402, L8502 and L8503 follow NV DG spec.
	09/28	46	Change PR4606 to 4.02K from 240ohm for fine tune 1.5V output Voltage.
	09/28	92	PTC9202, PTC9203 and PTC9204 2nd=79.47719.9BL
	09/28	22	Change R2220 to 10K from 100K.
	09/28	60	EC6001 change to 10p from 4.7p and default un-stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default un-stuff from Neo suggestion
	09/28	27	Change R2710, R2739, R2724 and R2726 change to 1%.
	09/29	27	Default mount R2756, Dummy R2734.
	10/04	24	Add 2nd source 68.1001E.10N on L2401,L2402,L2403 from sourcer Renee Lee updated.
	10/07	43	PTC4306 cahnge second source to 79.47612.60L.
	10/09	85	Change L8503 to 68.00375.091,and add second source 68.00206.171
	10/09	85	Change L8502 to 68.00115.191,and add second source 68.00206.131
	10/09	84	Change L8401 and L8402 to 68.00115.181,and add second source 68.00206.341
	10/09	83	Change L8303 to 68.00375.101,and add second source 68.00119.101
	10/09	83	Change L8301 to 68.00115.161,and add second source 68.00206.111
	10/09	42	Change PR4217 to 64.84505.6DL for Dual-core OCP
	10/09	42	Change PR4213 to 64.23715.6DL for Dual-core loadline
	10/09	42	Change PR4207 to 64.22025.6DL for CPU(35W) Turbo setting
	10/09	42	Change PR4202 to 64.22025.6DL for GFX Turbo setting
	10/09	20,83	Dummy R2004 R2003 and PQ8309, stuff R2005
	10/19	28	Change R2817 from 107K to 124K (64.12435.6DL) for VGA temperature setting change
	10/25	84	Change R8402 from 40D2R to 60D4R (64.60R45.6DL) for meeting the spec
	10/25	14 15	Add DM1 and DM2 second source:62.10017.Q41 and 62.10017.P61
X02	10/25	85	Ventura SMBC_INA219_C and SMBD_INA219_C add 3.3V pull high schematic
	11/01	51 85	Change HDMI HPD schematic for cost down
	11/10	27	Change R2724 to 64.33025.6DL for PCB version change
	11/10	83	Change L8301 to 68.00115.181,and add second source 68.00206.341

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 105 of 108

VERSION	DATA	PAGE	Change Iteam
X02	11/11	14	DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.
	11/11	15	DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.
	11/11	60	U6001 1st change to 72.25Q32.A01; 2nd change to 72.25320.C01; 3rd change to 72.25P32.C01 on ST stage
	11/11	68	Change CHARGERLED1 2nd to 83.00327.D70 from Sourcer updated.
	11/11	37	Change U3701 1st to 73.7SZ08.EAH;2nd to 73.01G08.L04;3rd to 73.7SZ08.DAH from Sourcer Eason updated.
	11/11	69	Add 2nd 20.K0592.030 on KB1 from ME updated connector list.
	11/11	82	Add 2nd 20.K0465.008 on MEDIA1 from ME updated connector list.
	11/11	58	Add 2nd 20.F1804.004 on SPK1 from ME updated connector list.
	11/11	28	Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.
	11/11	70	Add 2nd 20.F0962.010 on HALL1 from ME updated connector list.
	11/11	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0.
	11/11	60	Add Q6002,R6007 fo FACTORY RTC detect function
	11/11	28	ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.
	11/11	28	Reserved G709T1UF for T8 solution sync with DN13.
	11/12	82	Change R8201, R8202, R8203 from 430 ohm to 1K ohm (63.10234.1DL) for soluting media board LED brightness is too light issue
	11/15	49	Add 2nd 20.F1860.030 on LCD1 from ME updated connector list.
	11/15	8	Reserved C802~C804,C806,C807 10uF 0603 for power team fine tune Vcore quality
	11/15	88 89 90 91	All of VRAM(VRAM1~VRAM8) PCB footprint change to CO-LAY type (DUMMY-BGA96D075133H48) from BGA96D0913H48 same as DW30.
	11/15	68 69	Change R6813, R6906 from 390 ohm to 1K ohm (63.10234.1DL) for soluting LED brightness is too light issue
	11/15	20	Dell required us to disable PCIE port of WWAN slot ,If PCIE port 1 is disabled, it will cause all PCIE port disabled,so change WWAN to PCIE port 3 from port1 at ST stage.
	11/16	97	Change HHD1 HDD4 HGPU1 HGPU2 2nd from 34.4CK01.201 to 34.4CK01.401 from ME update connector list
	11/16	68	Change R6808, R6811 from 390 ohm to 1K ohm (64.10234.1DL) for soluting LED brightness is too light issue
	11/16	28	stuff both G709T1UF and P2800 related circuit, add R2805 0ohm default un-stuff at ST stage.
	11/17	48	CO-LAY APL5916 related circuit for VCCSA LDO solution.
	11/18	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2301 and un-stuff L2301.
	11/18	28	Add R2805 0hm between THERM_SYS_SHDN#_OTZ and THERM_SYS_SHDN#. Add R2812 0ohm between THERM_SYS_SHDN# and U2805 pin3.

VERSION	DATA	PAGE	Change Iteam
X02	11/18	28	Rename U2801&U2804 pin 8 to THERM_SYS_SHDN#_OTZ from HERM_SYS_SHDN#.
	11/18	20	Change X2001 to 82.30020.D41 from 82.30020.851 from Sourcer Dick updated.
	11/18	23	Reserved R2308,R2309 on VCCVRM power rail.Reserved U2302 LDO circuit on VCCVRM power rail
	11/18	22 82	Rename USB3_PWR_ON to PCH_GPIO57. Add R8209,R8210 for PM_SLP_S4# and VGA_THRM to control USB3_PWR_ON
	11/18	48	Change PTC4801 to 100u(77.21071.07L) from 150u from power team Brian updated
	11/19	74	Add 2nd 20.I0135.001 on CARD1 from ME updated connector list.
	11/19	82	Add 2nd 20.F1908.080 on IOBD1 from ME updated connector list.
	11/20	3	Updated PCIE ROUTING
	11/20	28	Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2812, un-stuff R2805
	11/20	23	Reserved R2308 on VCCVRM power rail. Reserved U2302 LDO circuit on VCCVRM power rail.
	11/20	48	Set TPS51461 PWM solution dummy field for VCCSA_PWM and APL5916 LDO solution dummy field for VCCSA_LDO. defualt stuff VCCSA_LDO at ST stage
	11/20	22	Rename GFX_CRB_DET to GSENSOR_DET on GPIO39.
	11/20	60	Un-stuff R6007 10M.
	11/20	82	Reserved EC8201,EC8202 0.1u(closed H3) between AGND and GND from EMC Neo suggestion.
	11/20	82	Reserved EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/20	82	Add RN8205 base on HSYNC&VSYNC report
	11/20	61	Removed R6101 and connect USB_PWR_EN# to U6101 pin4 directly.
	11/20	22	Rename PCH_GPIO12 to RTC_DET# on GPIO12.
	11/20	61 22 18	Reserved U6102 USB POWER related circuit to separate EATA and CRT USB power in ST build. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/20	82	Reserved R8211,R8212 0ohm 0805 on CRTBD1 pin37,39 to separate EATA and CRT USB power in ST build.
	11/22	82	Swap RN8205 pin4,3 and pin2,1 each other base on Connie swap report.
	11/22	82	stuff EC8201,EC8202 0.1u(closed H3) between GND and GND from EMC Neo suggestion. stuff EC8206 between 3D3V_S5 and GND from EMC Neo suggestion.
	11/22	23	base on layout condition change 3D3V_DAC_S0 circuit. Stuff R2301 and un-stuff L2301.
	11/22	82	stuff EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/22	23	Removed U2302 LDO for VCCVRM.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: QUEEN 15 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 106 of 108

VERSION	DATA	PAGE	Change Iteam
X02	11/22	29	change R2920,R2921 to 22ohm from 0ohm and stuff EC2901,EC2902 22p from EMC Neo updated.
	11/22	61	Change U6101 to dual USB power switch from single for Layout limitation and placement. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/22	49	stuff C4908 0.1uF from EMC Neo suggestion.
	11/22	57	Change TR5701 to 69.10103.041 and un-stuff R5718,R5719 from EMC Neo Suggestion.
	11/22	49	Change TR4902 CM choke to 69.10103.041 and un-stuff R4908,R4909 from EMC Neo Suggestion.
	11/22	49	Swap TR4901 pin4,3 and pin2,1 each other base on Connie swap report. Change TR4901 CM choke to 69.10103.041 and un-stuff R4911,R4912 from EMC Neo Suggestion.
	11/22	75	Change TR7501 CM choke to 69.10103.041 and un-stuff R7501,R7502 from EMC Neo Suggestion.
	11/22	58	stuff EC5801~EC5804 470pF from EMC Neo suggestion.
	11/22	9 39 45 49	stuff EC901, EC3903, EC4501, EC4909, EC4907 0.1uF from EMC Neo suggestion.
	11/22	49	Change RN4901 to 100ohm 4p from 8p for improve layout place.
	11/22	48	Updated VCCSA_LDO circuit from Power team Brian updated.
	11/22	83 84 85	Change L8301 L8401 L8402 to 0 ohm resistor (63.00000.00L)
	11/22	60	stuff R6007 10M.
	11/23	49 57 75	SWAPTR4901 TR4902 TR5701 TR7501 pin1&4 and pin2&3 each other base on Connie swap report.
	11/23	60	Change U6101 1st(74.02182.071);2nd(74.00546.A7D);3rd(74.02062.079) from Sourcer Harrison suggestion.
	11/23	64	Add C6402 0.1uF,C6403 180pF and stuff C6401 47pF from RF fine tune result.
	11/23	57 49 75	Change R5718,R5719,R4908,R4909,4911,R4912,R7501,R7502 to 0ohm 0603 from 0402.
	11/23	56 97	stuff EC9739,EC9737,EC9735 47pF from RF fine tune result. stuff EC5601 180pF from RF fine tune result. Stuff EC9738 0.22uF closed EC9739 from RF fine tune result.
	11/23	97	stuff ECEC9729,EC9730 470pF from EMC Neo suggestion.
	11/23	45	Change PR4501 to 75K from 45.3K for 1.05V OCP set to 20A from Brian.
	11/23	82	Removed R8211,R8212 and connect 5V_USB2_S3 to CRTBD1 pin 37 directly.
	11/23	61	Removed C6105,C6103.
	11/23	69 70	Change AFTP 80 81 to AFTP 83 84; change AFTP 83 to AFTP82; change AFTP 82 to AFTP85.
	11/24	20	Add 2nd(82.30020.G71);3rd(82.30020.G61) on X2001 from Sourcer Dick updated.
	11/24	69	Add 2nd(20.K0613.004)on KBLIT1 from Karl updated.

VERSION	DATA	PAGE	Change Iteam
X02	11/24	57	Add 2nd(22.10339.261)on ESATA1 from Karl updated.
	11/24	28	un-stuff VGA P2800 related circuit from Niki confirmed.
	11/24	64	rename C6401,C6402,C6403 to EC6401,EC6402,EC6403
	11/24	22	Dummy R2206
	11/25	28	Dummy R2817 R2818 C2816
	11/25	69	Add 3rd(83.00110.R70) on FPOWERLED1,HDDLED1,WLANLED1 from Anya provide
	11/25	69	Add 3rd(83.00192.J70) on TPLOCKLED1 and TPLOCKLED2 from Anya provide.
	11/25	69	Add 3rd(83.01108.070) on CHARGERLED1 from Anya provide.
	11/26	43 92	Change PC9217 PC4319 to 0.1u 50V
	11/29	83	Change C8353 C8354 to 15PF ,R8320 stuff from vendor suggestion.
	11/29	36	Stuff D3602
	11/30	68	Change 2nd source to 83.00322.070 from 83.00110.J70
	11/30	85	Change L8502 L8503 to 0 ohm
	11/30	92	Stuff PR9237 DY PR9321
	12/01	8	Change C837,C826 to 22uF from 10uF and default stuff from Power Brian updated.
	12/01	8	Change C801~C807 and C817 10uF stuff at QC CONFIG from power Brian updated.
A00	12/21	ALL	Change 0402 pad(ZZ.00PAD.M11): R1404 R1405 R1503 R1504 R1703 R1704 R1705 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R2762 R3614 R3710 R5114 R5801 R5802 R5803 R5804 R8210 R8323 R8511 R8512
	12/21	82	Change 0603 pad(ZZ.00PAD.M21): R8206 R8207
	12/21	17 20	Change resistor pad(ZZ.0R04P.ZZZ): RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2015 RN2016
	12/21	83 84 85	Change L8301, L8401,L8402,L8502,L8503 to 0R0603 pad(ZZ.00PAD.M21)
	12/21	ALL	Change to Parallel resistor R1501 ,R1502; R2739 ,R2774;R8202 ,R8203;R8501 ,R8502;R8506 ,R8507;R2123 ,R2124
	12/21	82	RN8205 change to R8201, R8202
	12/21	93	PR9237 rename to PR9337
	12/21	56 61 68	Delete 77.C1071.21L(TC6101), delete 83.01108.070(CHARGERLED) , delete 62.10065.121(HDD1)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 107 of 108

VERSION	DATA	PAGE	Change Iteam
A00	12/22	27	R2724 change to 47K resistor for XBulid
	12/22	27	R2301 change to 0 resistor for CRT debug
	12/22	40	1.Change PR4032,PR4034,PR4037 to ZZ.00PAD.M11 2.Stuff PQ4003,PQ4004 3.Change PR4047 to 174K(64.17435.6DL) 4.Change PR4035 to 300K(64.30035.6DL) 5.Change PR4036 t0 76.8K(64.76825.6DL) 6.Change PR4031 to 150K(64.15035.6DL)
	12/23	68	1.FPOWERLED1 rename to FPLED1 2.HDDLED1 rename to HDLED1 3.CHARGERLED1 renamtpe to CHLED1 4.WLANLED1 rename to WLED1 5.TPLOCKLED2 rename to TPLED2 6.TPLOCKLED1 rename to TPLED1 7.PWRBTN1 rename to PWRBT1 8.PWRBTN2 rename to PWRBT2
	12/23	43	Delete PR4323,PR4324,PR4325; Stuff PR4320 for all BOM ,not co-lay Ventura
	12/23	92	Delete PR9220,PR9222,PR9223; Stuff PR9217 for all BOM ,not co-lay Ventura
	12/23	51	Change 5V_HDMI to 5V_CRT_S0_R for HDMI power leakage
	12/24	All	PRN3901 rename to PN3901 PTC9202~04 rename to PT9202~04 PTC4301~04 rename to PT4301~04 PTC4306 rename to PT4306 PTC4308~09 rename to PT4308~09 PTC4401~03 rename to PT4401~03 PTC4502 rename to PT4502 PTC4602 rename to PT4602 PTC4102 rename to PT4102 PTC4104 rename to PT4104
	12/24	28	Change U2802 3rdto 74.05606.A71 at X-Build batch run
	12/24	82	Change RN8205 to 66.22036.04L from 66.22036.040at X-Build stage
	12/24	82	Reserved R8211 0603 0ohm on F8201
	12/24	36	Reserved Q3603 2N702 on IMVP_PWRGD to fine tune glitch waveform when AC lose and DC lose.
	12/24	28	Change 3D3V_S0 to 3D3V_DAC_S0
	12/24	45 46 93	Change to short pad: PR4502,PR4607,PR9311,PR9312,PR9326. DUMMY PC4501
	12/27	28	If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.
	12/27	42	PR4207,PR4213,PR4217 DUMMY field set to DC&QC option
	12/28	51	Change 5V_HDMI to 5V_CRT_S0_R on RN5101
	12/28	28	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at XBuild

VERSION	DATA	PAGE	Change Iteam
A00	12/28	27	Change R2756, R2763, R2766 to short pad
	12/28	36	Stuff Q3603
	12/28	28 86	Cancel VGA Thermal sensor P2800 ciruit
	12/28	27 28 82	Change to VGA_THRM to USB3_PWR_ON
	12/28	23	Change R2301 to short pad
	12/29	51	Change HDMI resistor to short pad
	12/29	49,57,75	Delete USB DUMMY resistor for no-lay
	12/29	32	Change USB 0 resistor to short pad for no-lay
	12/29	5	Reserve EC502 ,EC504 for EMI suggestion,add DUMMY EC505 for EMI
	12/29	82	Delete PM_SLP_S4# line, directly link to USB3_PWR_ON
	12/29	23	Add 3rd Richtek(74.09198.G7F) on U2301 at XBuild batch run config
	12/29	68	Not use Liteon LED(83.00322.070) for package
	12/30	5	Add DUMMY diode EC506 for BUF_CPU_RST# as EMI suggestion
	12/30	42	PC4227 change to 78.33420.5FL as 78.33423.5FL obsoleted
	12/30	49	Change R4904 to short pad
	12/31	86	Add probe point for P2800_VGA_DXN/P2800_VGA_DXP
	01/03	68	Change TPLED1,2 1st to 83.01921.P70 ,2nd to 83.00190.S7A,3rd to 83.00191.H70; R6813 change to 390R from 1K same as DN13 LED part.
	01/03	49	Delete R4908, R4909 for USB_Camera not co-lay
	01/03	4~10	Add 3rd foxconn(62.10055.321) on CPU1 at X-Build batch run config
	01/03	82	Add 3rd T-conn(20.F1932.040) on CRTDB1at X-Build batch run config
	01/03	97	Add 3rd LIDON(34.4CK01.501) on HHD1,HHD4,HGPU1,HGPU2 at X-Build batch run config
	01/04	68	Delete 83.00191.H70 for TPLED1,2 as cost high
	01/04	49,57,75	Add 2nd TAI-TECH(69.10084.071) on TR4901,TR4902,TR5701,TR7501 at X-Build batch run config

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
A3	QUEEN 15	A00

Date: Tuesday, January 04, 2011 Sheet 108 of 108