Arsenal DJ1 Discrete Schematics Document

Arrandale

Intel PCH

2010-05-03

REV : A01

DY : Nopop Component
PARK : Pop when schematic is PARK-LP Component
M92 : Pop when schematic is M92-LP Component

DISCRETE PARK

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Title	Cover Page	
Size: A3	Document Number: Arsenal DJ1 Discrete	Rev: A01
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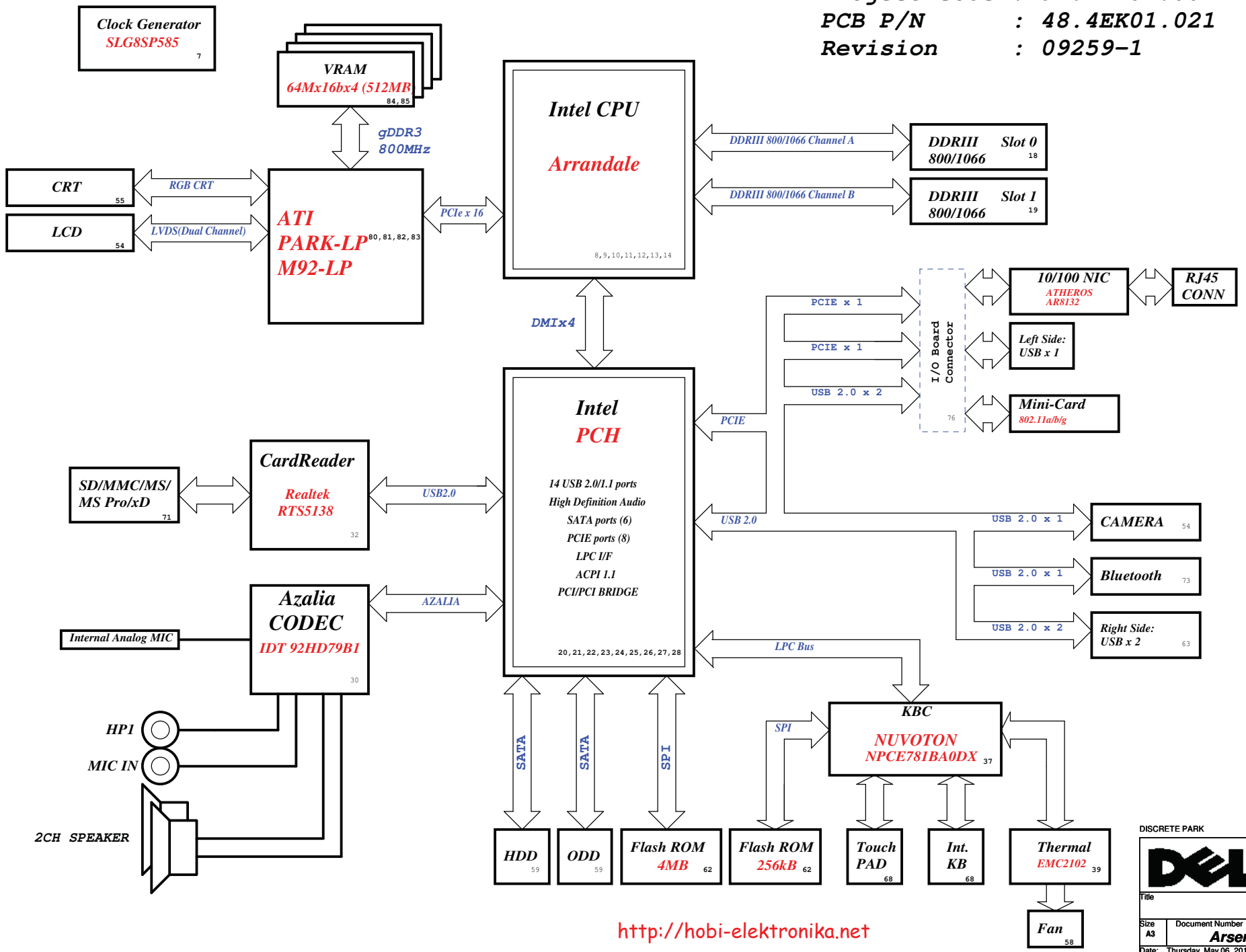
DJ1 Discrete Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK01.021
Revision : 09259-1



CPU DC/DC ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC APL5930KAI 88	
INPUTS	OUTPUTS
+1.5V_SUS	+1.1V_RUN

VGA RT8208BGQW 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_DELAY

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5 GND
L6: Bottom

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Title: Block Diagram

Size	Document Number	Rev
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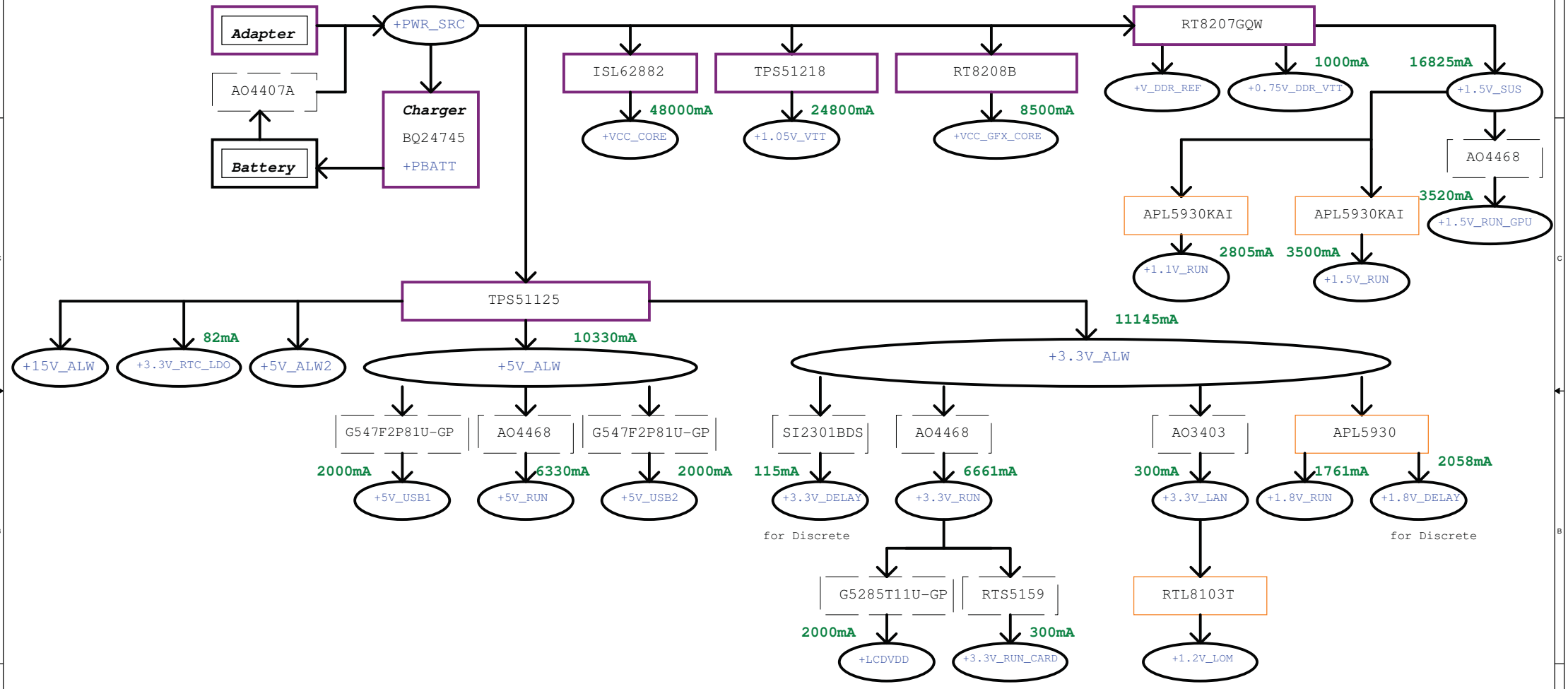

Power Shape

Regulator	LDO	Switch

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Title: *Power Block Diagram*

Size	Document Number	Rev
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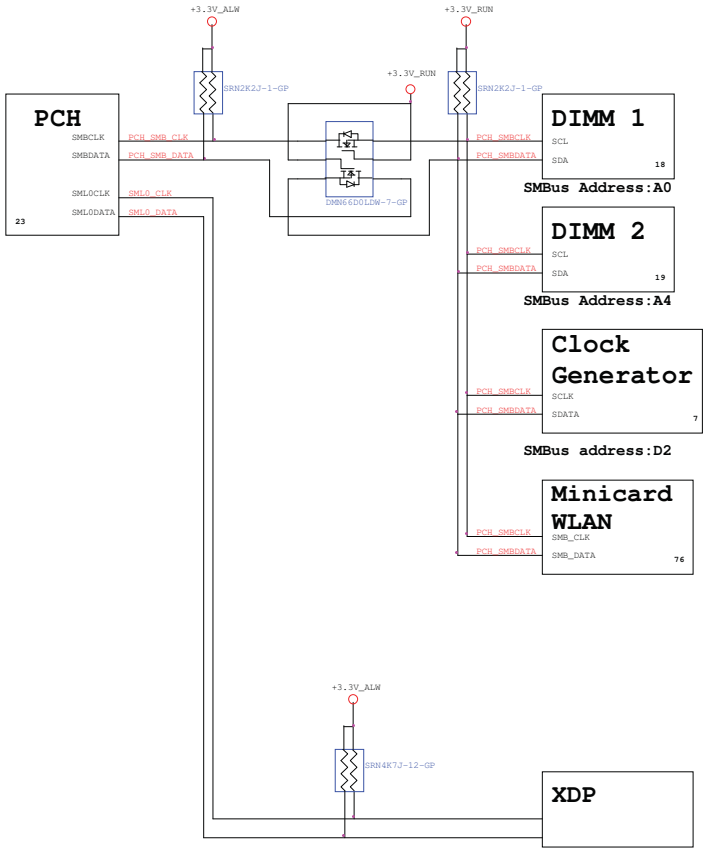
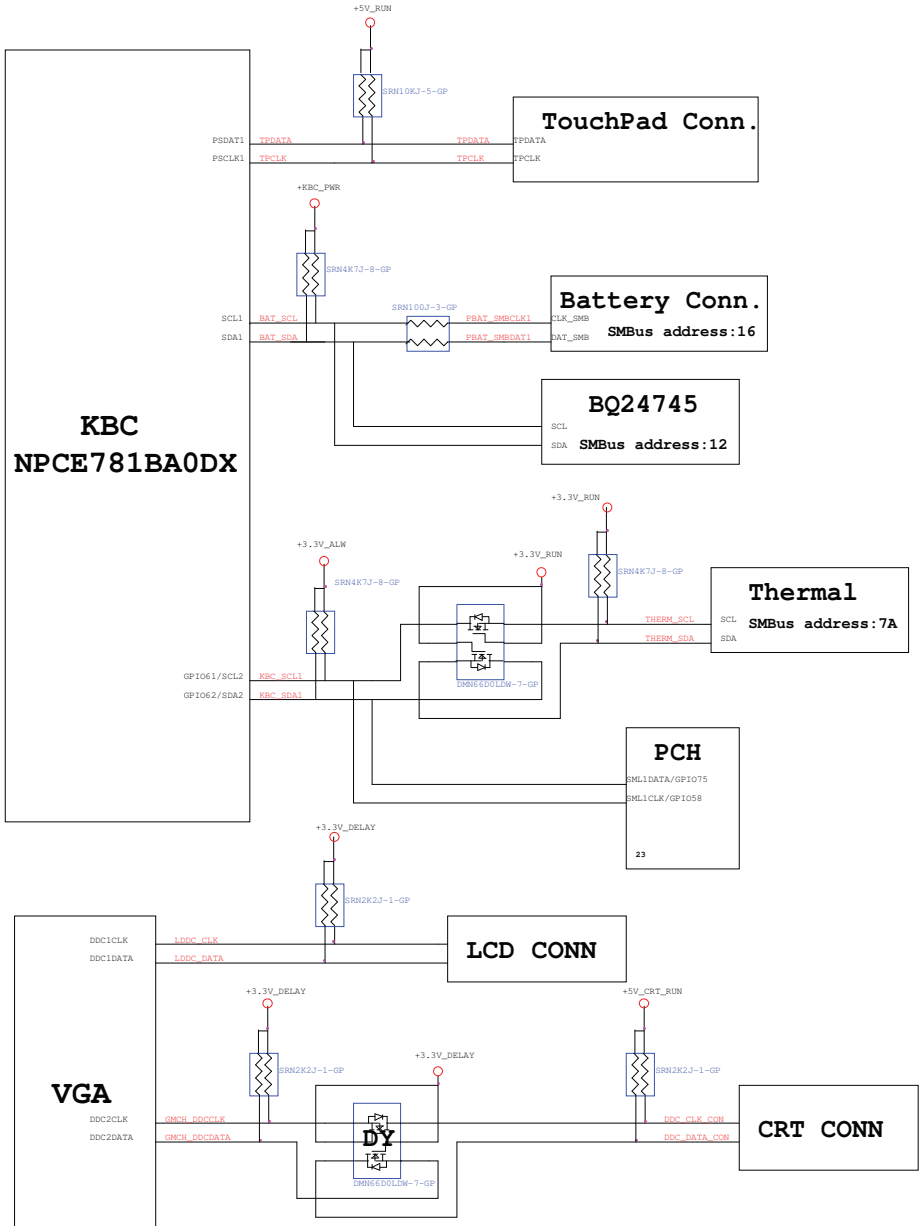
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Arsenal DJ1 Discrete	A01

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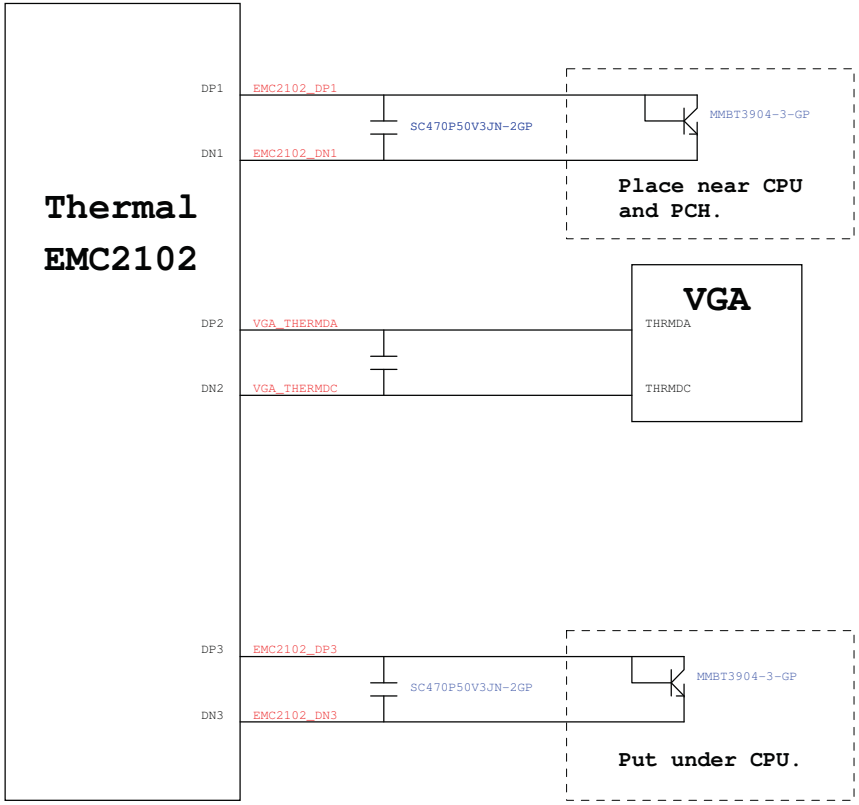
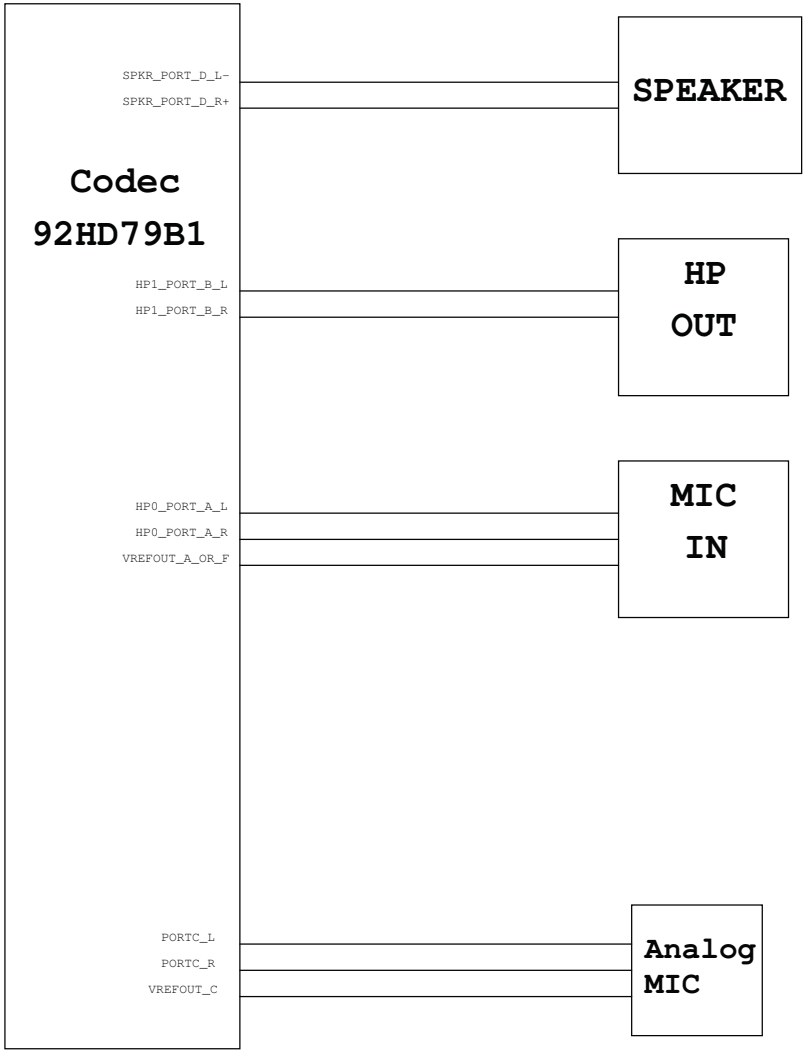
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

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Title: Table of Content

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: A01

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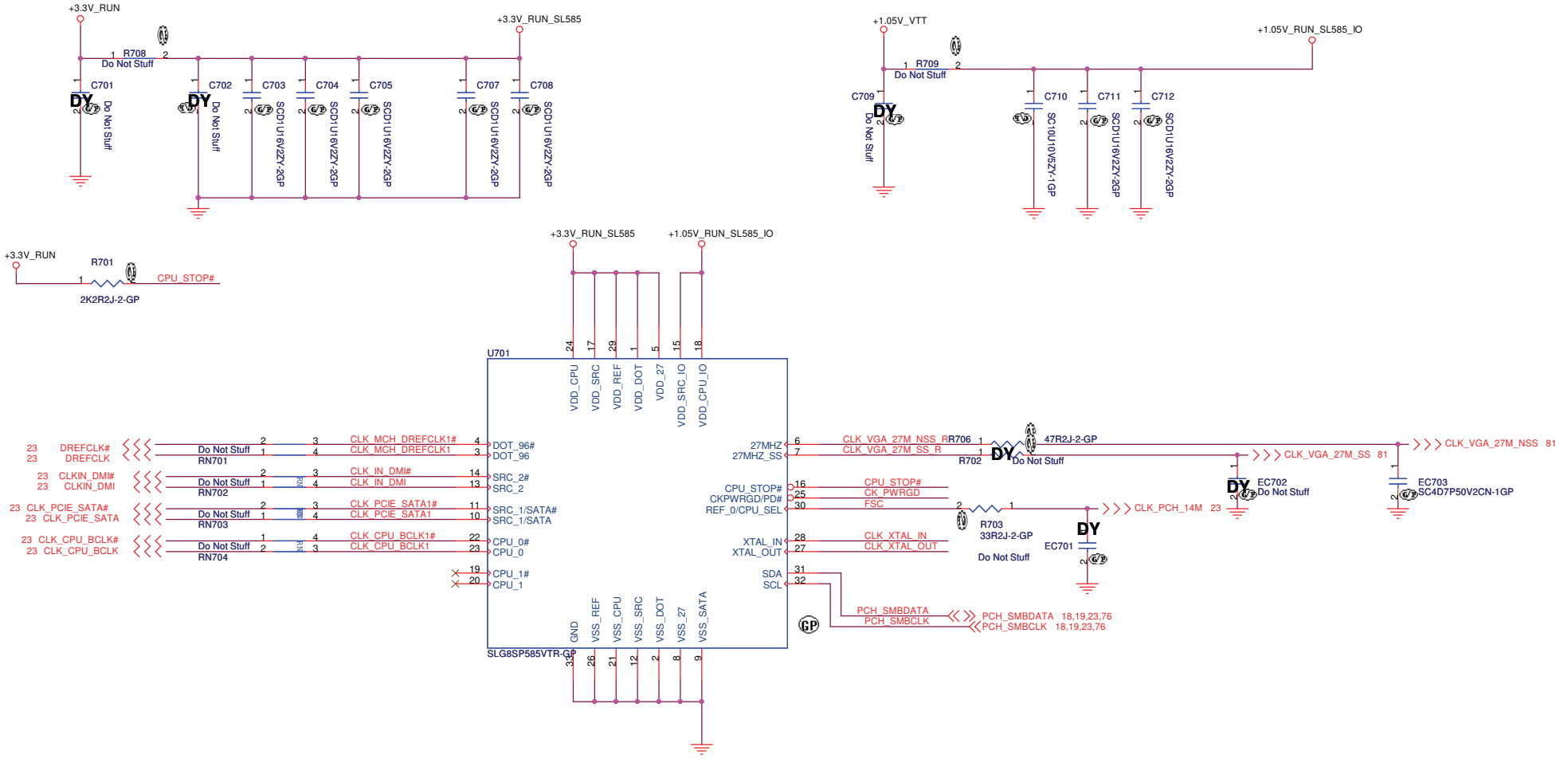
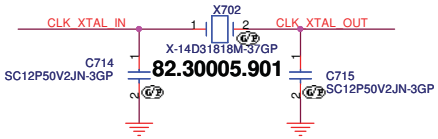
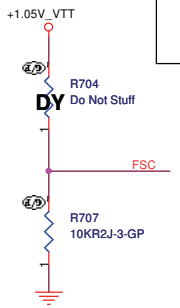
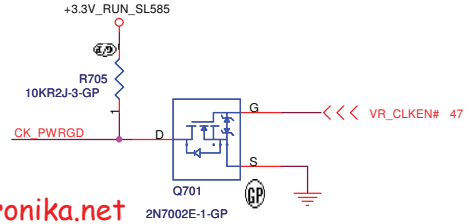
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz







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Title: Clock Generator SLG8SP585

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

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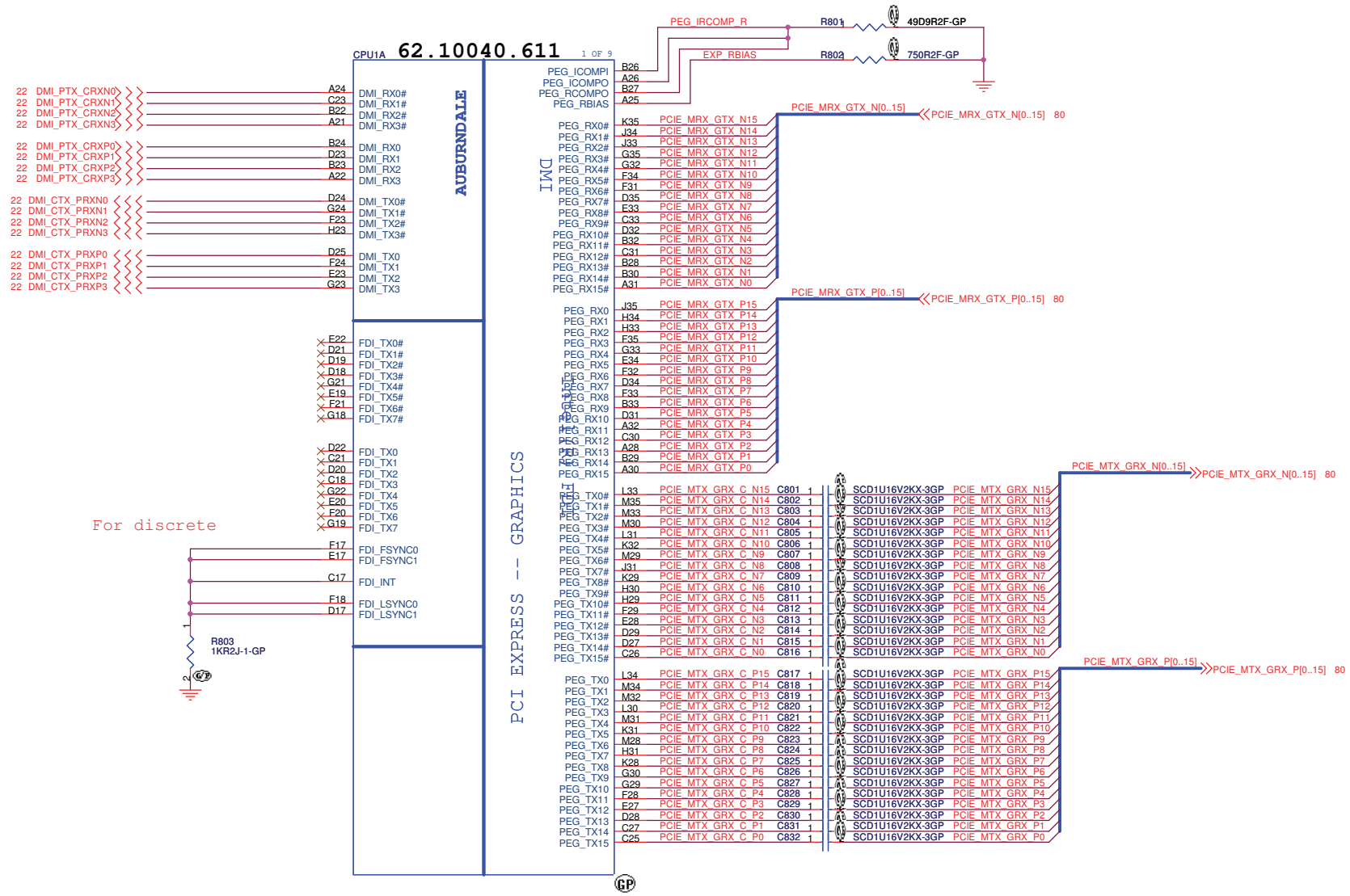
SSID = CPU



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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
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SSID = CPU

Processor Pullups

+1.05V_VTT

R902 1 49D9R2F-GP H_CATERR#

R933 1 68R2-GP H_PROCHOT#

R904 1 DY Do Not Stuff H_CPURST#

Processor Compensation Signals

R901 1 20R2F-GP H_COMP3

R903 1 20R2F-GP H_COMP2

R905 1 49D9R2F-GP H_COMP1

R906 1 49D9R2F-GP H_COMP0

Do Not Stuff TP901 1 SKTOCC#_R

H_CATERR#

CPU1B 2 OF 9

COMP3 AT23
COMP2 AT24
COMP1 G16
COMP0 AT26
SKTOCC# AH24
CATERR# AK14
PECI AT15
PROCHOT# AN26
THERMTRIP# AK15
RESET_OBS# AP26
PM_SYNC AL15
VCCPWRGOOD_1 AN14
VCCPWRGOOD_0 AN27
SM_DRAMPWROK AK13
VTTPWRGOOD AM15
TAPPWRGOOD AM26
RSTIN# AL14

25 H_PECI

47 H_PROCHOT#

25,37,42,81 H_THERMTRIP#

H_CPURST#

22 H_PM_SYNC

25,42 H_PWRGD — R908 Do Not Stuff — VCCPWRGOOD

22 PM_DRAM_PWRGD — R912 Do Not Stuff — VDDPWRGOOD_R

49 H_VTTPWRGD

H_PWRGD_XDP

21,37,70,76,80 PLT_RST# — R913 1K6R2F-GP — PLT_RST#_R — R915 750R2F-GP

AUBURNDALE MISC CLOCKS

BCLK A16 BCLK_CPU_P_R — RN901 — BCLK_CPU_P 25
BCLK# B16 BCLK_CPU_N_R — RN901 — BCLK_CPU_N 25
BCLK_ITP AR30 BCLK_ITP_P
BCLK_ITP# AT30 BCLK_ITP_N
PEG_CLK E16 PEG_CLK_R — RN903 — CLK_EXP_P 23
PEG_CLK# D16 PEG_CLK#_R — RN903 — CLK_EXP_N 23
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17

THERMAL DDR3 MISC

SM_DRAMRST# F6 SM_DRAMRST#
SM_RCOMP0 AL1 SM_RCOMP_0
SM_RCOMP1 AM1 SM_RCOMP_1
SM_RCOMP2 AN1 SM_RCOMP_2
PM_EXT_TS0# AN15 PM_EXTTS#0_C — PM_EXTTS#0 18
PM_EXT_TS1# AP15 PM_EXTTS#1_C — PM_EXTTS#1 19

Do Not Stuff RN906

+1.05V_VTT — RN905 — SRN10KJ-5-GP

DDR_RST_GATE 25

C915 SCD047U16V2ZY-1GP +1.5V_SUS

R934 1KR2J-1-GP

Q901 BSS138-7-F-GP

R935 DY Do Not Stuff

C903 SCD1U10V2KX-5GP

DDR3_DRAMRST# 18,19

A00 10.03.09

SM_DRAMRST# — R988 100KR2J-1-GP

PWR MANAGEMENT JTAG & BPM

PRDY# AT28 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
DBR# AN25 H_DBR#_R — R909 Do Not Stuff — XDP_DBRESET#

BPM0# AJ22 XDP_OBS0
BPM1# AK22 XDP_OBS1
BPM2# AK24 XDP_OBS2
BPM3# AJ24 XDP_OBS3
BPM4# AJ25 XDP_OBS4
BPM5# AH22 XDP_OBS5
BPM6# AK23 XDP_OBS6
BPM7# AH23 XDP_OBS7

DDR3 Compensation Signals

SM_RCOMP_0 R907 100R2F-L1-GP-U
SM_RCOMP_1 R910 24D9R2F-L-GP
SM_RCOMP_2 R911 130R2F-1-GP

XDP_TMS R914 DY Do Not Stuff
XDP_TDI_R R916 DY Do Not Stuff
XDP_PREQ# R917 DY Do Not Stuff
XDP_TCLK R918 DY Do Not Stuff
+1.05V_VTT

	R919	R920
S3 circuit	1.1k No Stuff	0.75k
Normal	1.27k	3k

+1.5V_RUN — R919 DY Do Not Stuff — VDDPWRGOOD_R — R937 750R2F-GP

+3.3V_ALW

A00 10.03.09

R2114 1 2 Do Not Stuff

U927 74LVC1G08GW-1-GP (B, A, GND, VCC, Y)

U927_B — VTT_PWRGD_R3 — R977 1K6R2F-GP

37,42,49 VTT_PWRGD

VDDPWRGOOD_R — R978 Do Not Stuff DY — VDDPWRGOOD_KBC 37

XDP1

XDP_PREQ# XDP_PRDY#
XDP_OBS0 XDP_OBS1
XDP_OBS2 XDP_OBS3
XDP_OBS4 XDP_OBS5
XDP_OBS6 XDP_OBS7
XDP_TCLK

DY Do Not Stuff

+1.05V_VTT

H_PWRGD — R927 DY Do Not Stuff
22 PM_PWRBTN#_R — R929 DY Do Not Stuff — H_CPUPWRGD_XDP — PM_PWRBTN#_XDP
H_PWRGD_XDP — R930 DY Do Not Stuff — PCIE_CLK_XDP_P

C902 DY Do Not Stuff

23 SML0_DATA
23 SML0_CLK

BCLK_ITP_P
BCLK_ITP_N

XDP_RST#_R — R931 DY Do Not Stuff — H_CPURST#

C901 DY Do Not Stuff — R928 51R2J-2-GP

XDP_DBRESET# 22

XDP_TDO

XDP_TRST#
XDP_TDI
XDP_TMS

XDP_RST#_R — R932 DY Do Not Stuff — PLT_RST# 21,37,70,76,80

JTAG MAPPING

XDP_TDI_R R921 DY Do Not Stuff — XDP_TDI
XDP_TDO_M R922 DY Do Not Stuff — XDP_TDO
R924 Do Not Stuff
XDP_TDI_M R925 DY Do Not Stuff
XDP_TDO_R R926 Do Not Stuff
XDP_TRST# — R923 51R2J-2-GP

Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

A00 10.03.25 change to ZZ.00PAD.Q81

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Title: CPU (THERMAL/CLOCK/PM)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

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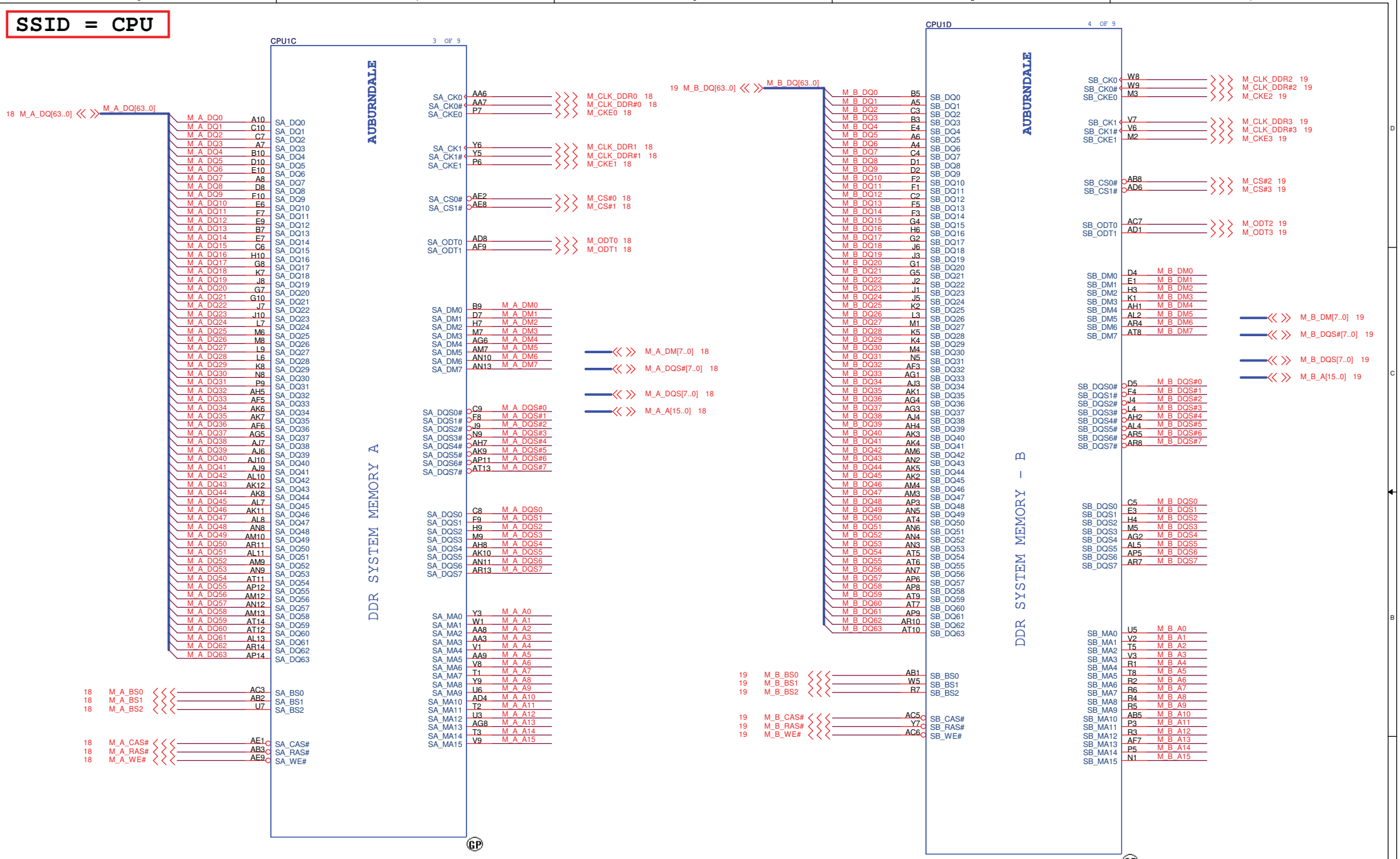
SSID = CPU



DISCRETE PA

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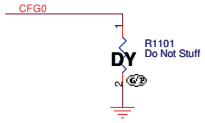
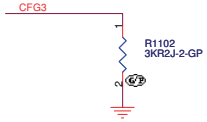
Title	CPU (DDR)
Size	
Document Number	Arsenal DJ1 Discrete
Rev	A01
Date: Thursday, May 06, 2010	Sheet 10 of 92

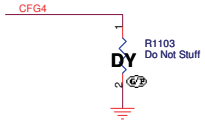
SSID = CPU



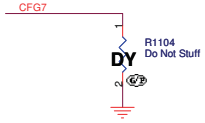
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



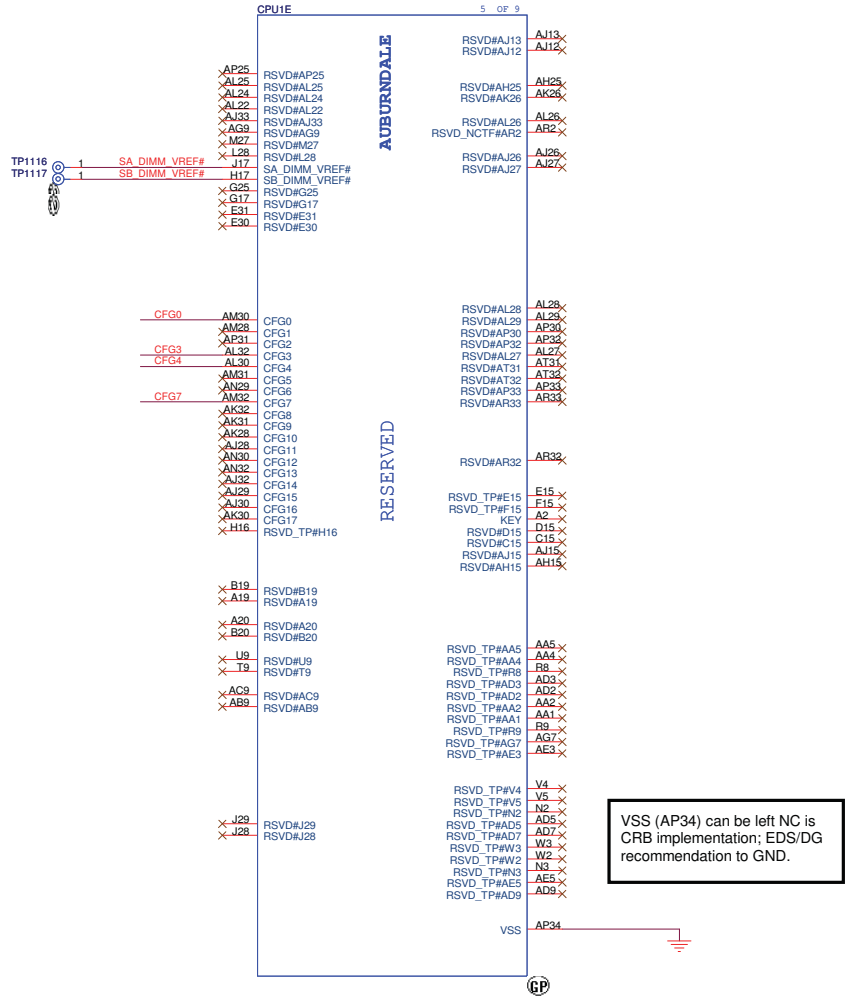
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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Title: CPU (RESERVED)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

A00 10.03.24

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

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Title: CPU (VCC_CORE)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

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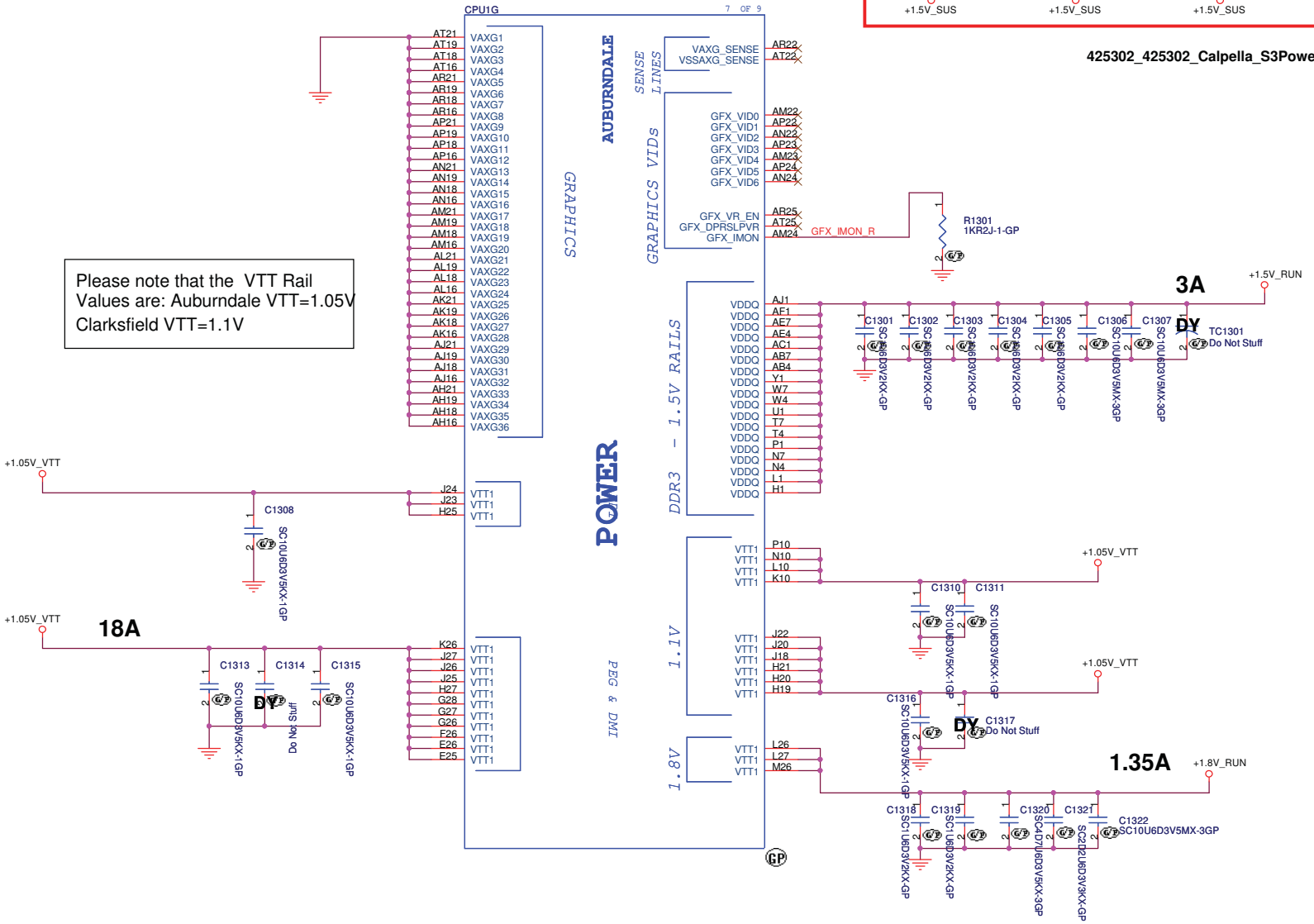
SSID = CPU



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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

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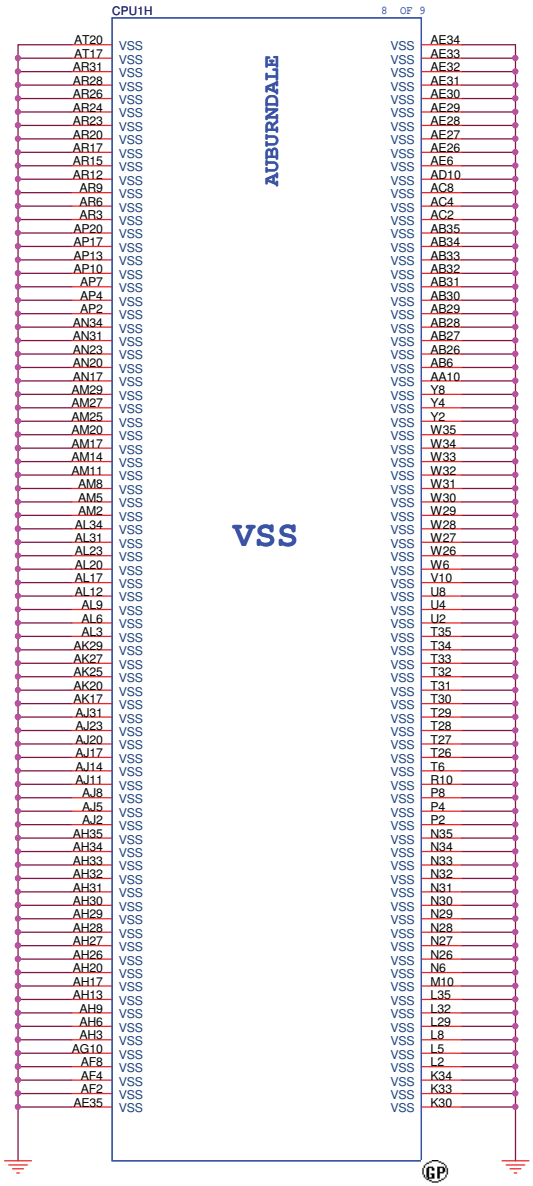
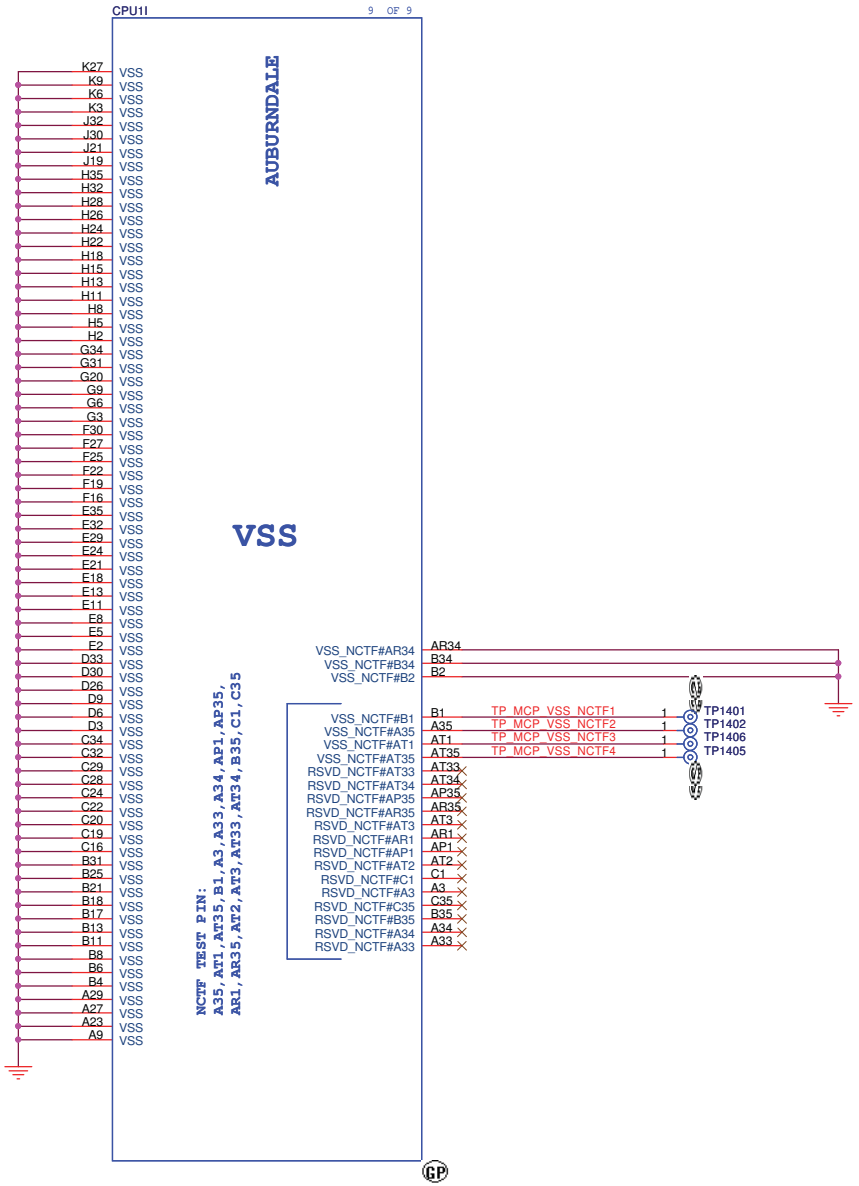
SSID = CPU





DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 14 of 92

(Blanking)

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *A01*

Date: Thursday, May 06, 2010 | Sheet 15 of 92

(Blanking)

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 16 of 92

(Blanking)

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Wistron Corporation
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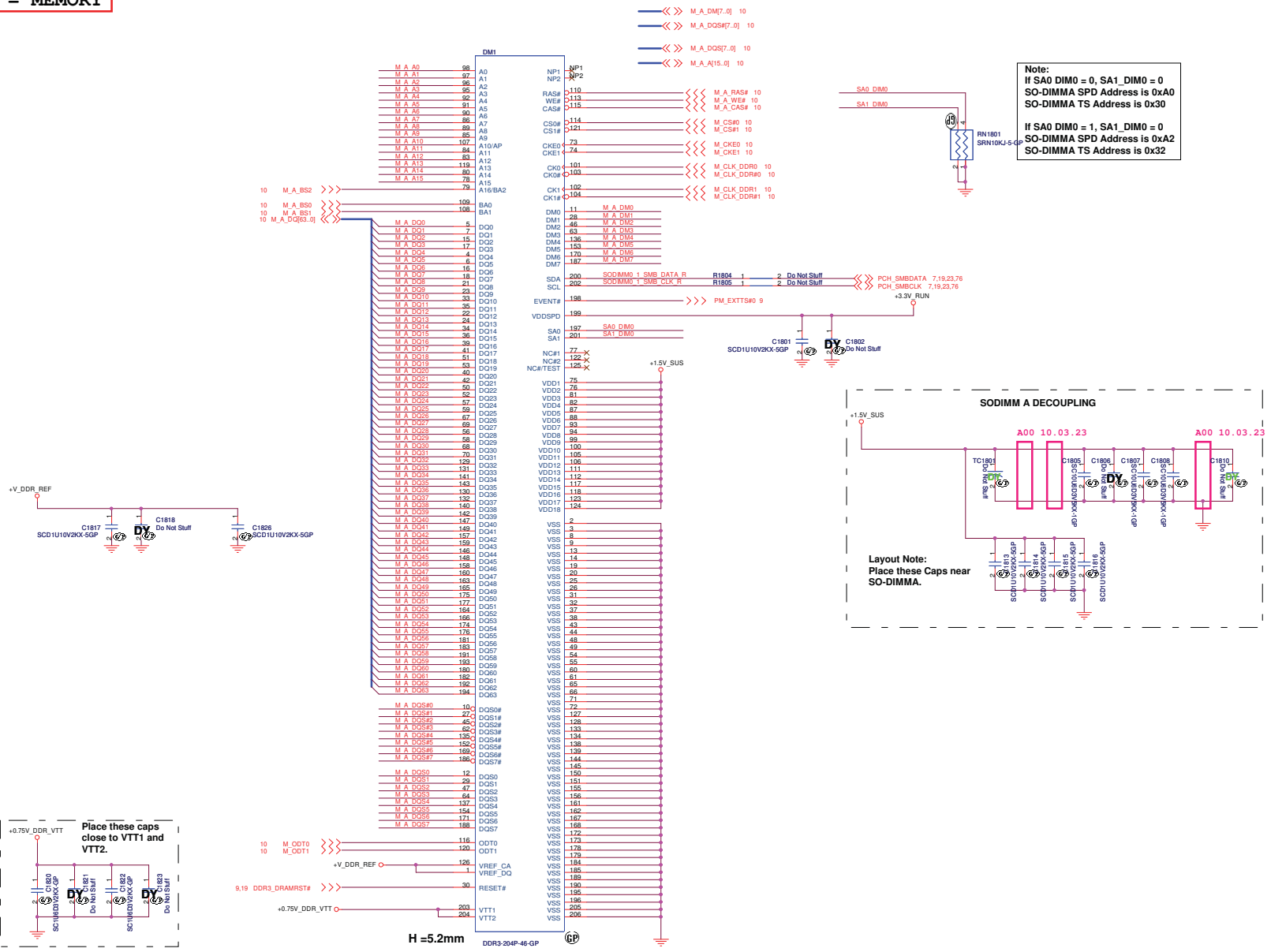
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 17 of 92

SSID = MEMORY



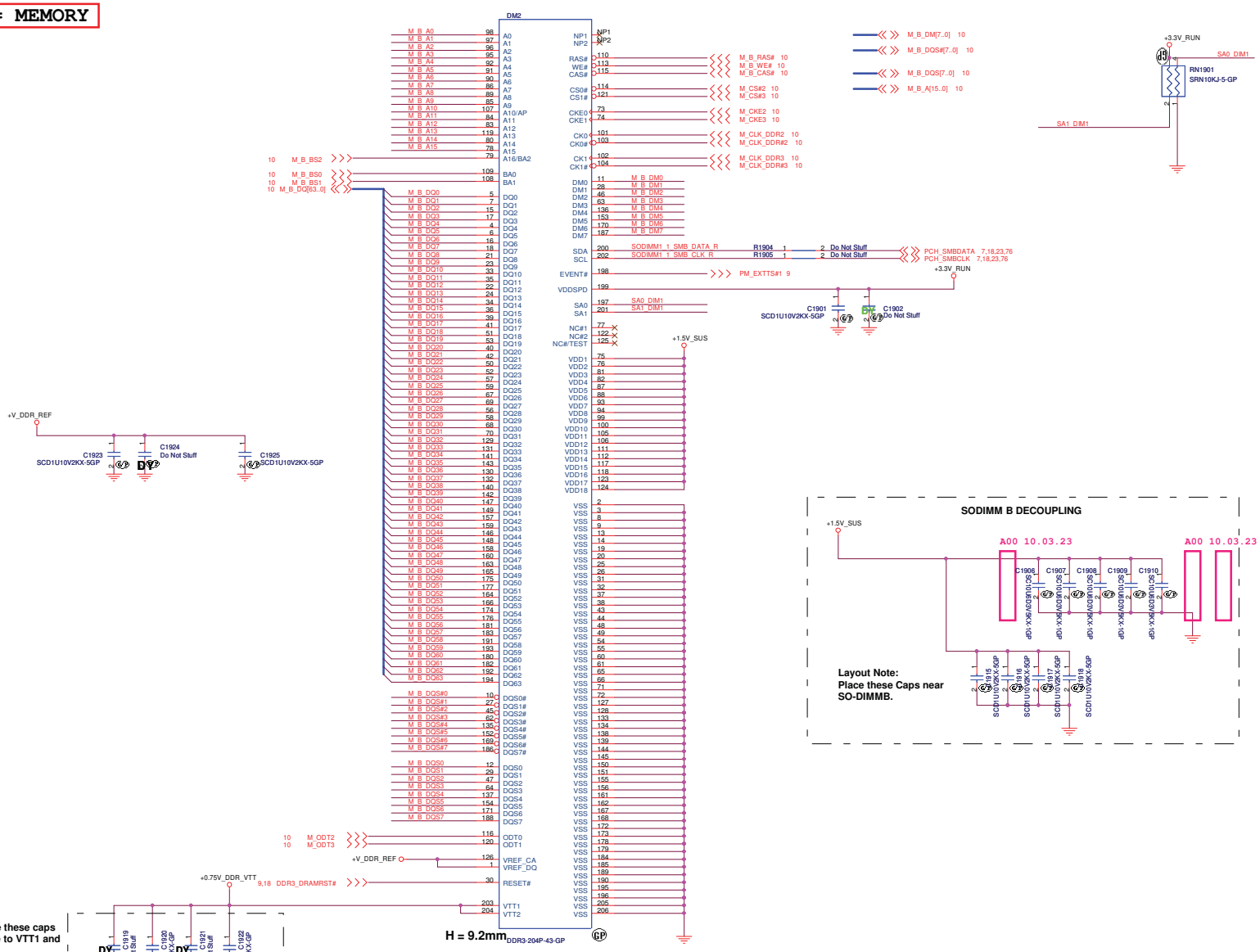
62.10017.P11

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DDR3-SODIMM1		
Size	Document Number	Rev
	Arsenal DJ1 Discrete	A01
Date: Thursday, May 06, 2010	Sheet 18 of 92	

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

DISCRETE PARK

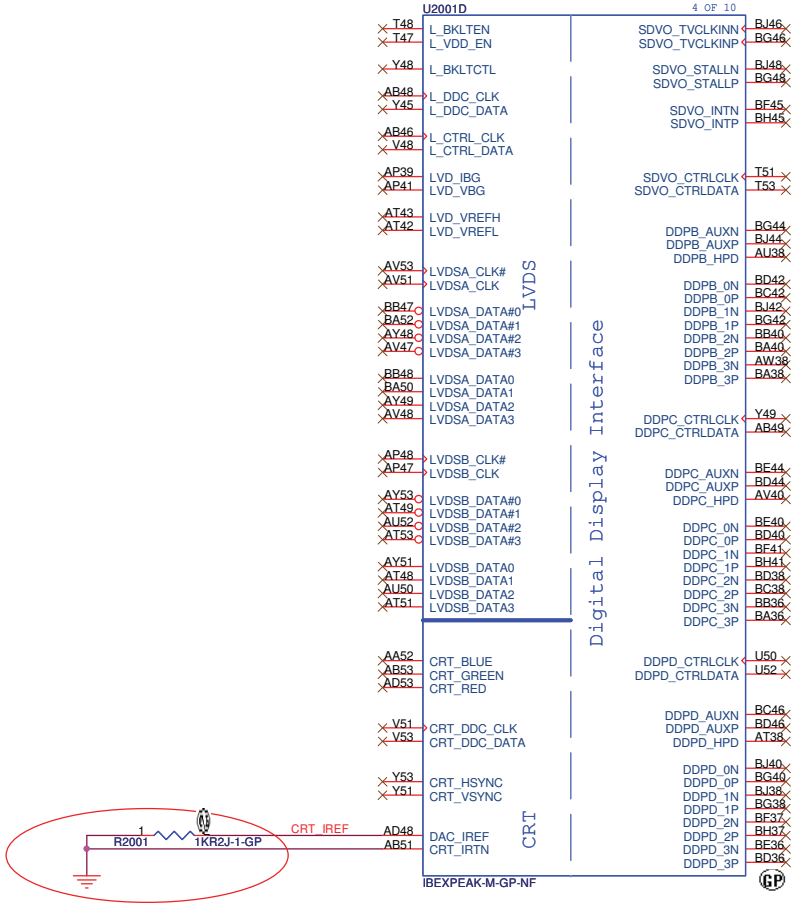
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
	Arsenal DJ1 Discrete	A01

Date: Thursday, May 06, 2010 Sheet 19 of 92

SSID = PCH



For discrete, DAC_IREF pull down through 1k ohm.
CRT_IRTN pull down to GND.

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 20 of 92

SSID = PCH

RN2101 SRN8K2J-2-GP-U
PCI_DEVSEL# PCI_IRDY# PCI_SERR# INT_PIRQC# → PCI_REQ2# INT_PIRQD# PCI_STOP# INT_PIRQA#
+3.3V_RUN

RN2102 SRN8K2J-2-GP-U
PCI_PERR# PCI_REQ0# PCI_REQ3# PCI_FRAME# → INT_PIRQB# PCI_PLOCK# PCI_REQ1# PCI_TRDY#
+3.3V_RUN

RN2103 SRN10KJ-7GP
+3.3V_RUN
INT_PIRQF# INT_PIRQH# INT_PIRQG# INT_PIRQE#

U2101 Do Not Stuff
+3.3V_RUN
9,37,70,76,80 PLT_RST# → PCI_PLTRST#
R2104 Do Not Stuff
C2101 Do Not Stuff

U2001E IBEXPEAK-M-GP-NF

BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

R2109 Do Not Stuff
PCI_GNT3#

RP2101 SRN10KJ-L3-GP
SMC_WAKE_SCI#_R, USB_OC#2_3, USB_OC#6_7, USB_OC#4_5 → +3.3V_ALW
USB_OC#0_1, USB_OC#8_9, USB_OC#12_13, USB_OC#10_11

Danbury Technology:
Disabled when Low.
Enable when High.

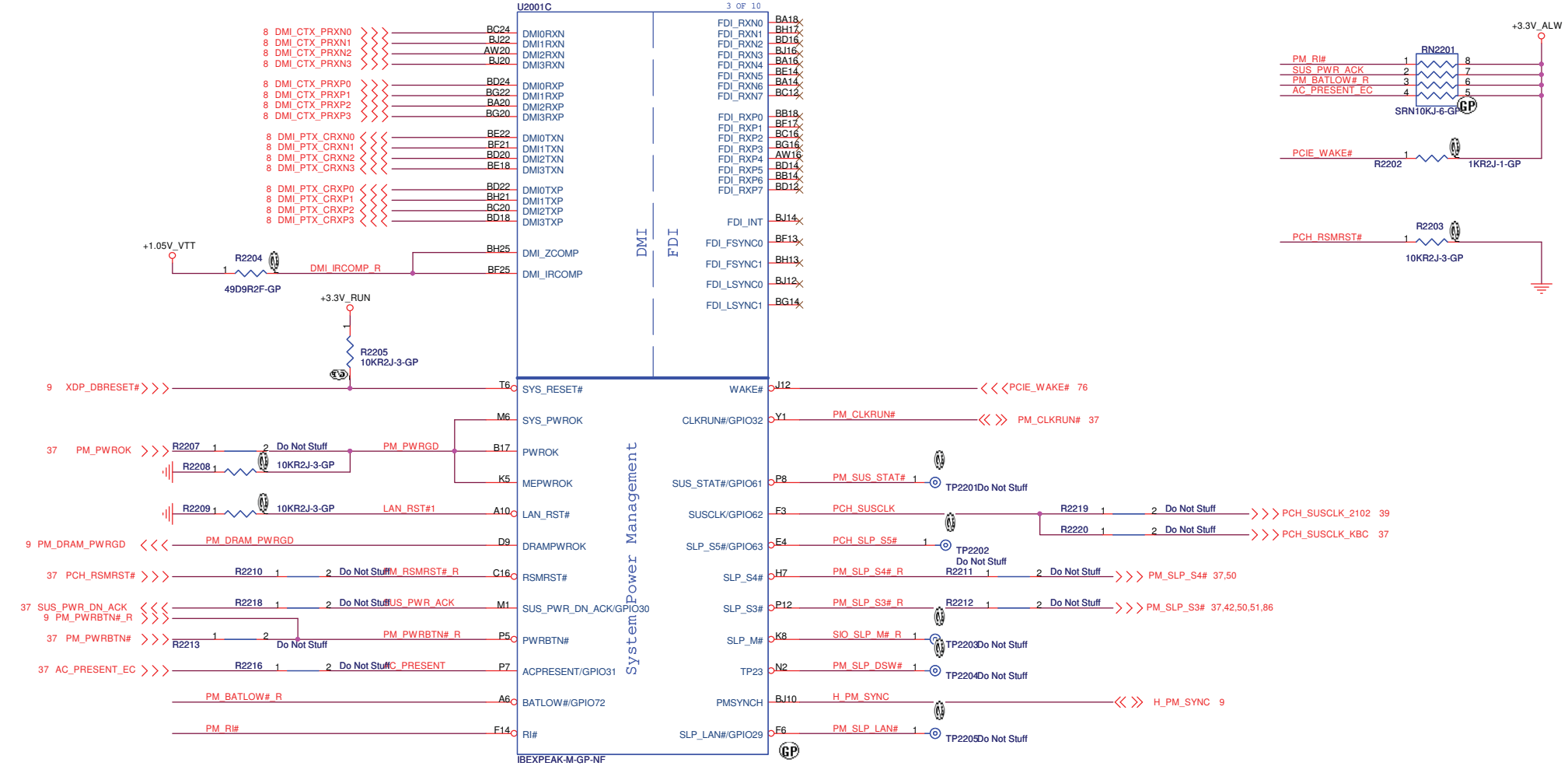
USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

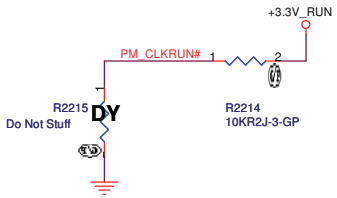
DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: | Document Number: Arsenal DJ1 Discrete | Rev: A01
Date: Thursday, May 06, 2010 | Sheet 21 of 92

SSID = PCH





Option to " Disable " clkrun.
Pulling it down will keep the clks running.

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size:
Document Number: Arsenal DJ1 Discrete
Rev: A01
Date: Thursday, May 06, 2010
Sheet 22 of 92

SSID = PCH

U2001B — 2 OF 10 — IBEXPEAK-M-GP-NF

PCI-E* / SMBus / Controller Link / PEG / From CLK BUFFER / Clock Flex

WLAN: PCIE_RXN2, PCIE_RXP2, PCIE_TXN2, PCIE_TXP2 — C2305 SCD1U10V2KX-5GP, C2306 SCD1U10V2KX-5GP — PCIE_C_TXN2, PCIE_C_TXP2

LAN: PCIE_RXN3, PCIE_RXP3, PCIE_TXN3, PCIE_TXP3 — C2303 SCD1U10V2KX-5GP, C2304 SCD1U10V2KX-5GP — PCIE_C_TXN3, PCIE_C_TXP3

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

A00 10.02.24

RN2309 Do Not Stuff: CLK_PCIE_MINI1#, CLK_PCIE_MINI1 — CLK_PCIE_MINI1R#, CLK_PCIE_MINI1R

MINI1_CLK_REQ#

RN2304 Do Not Stuff: CLK_PCIE_LAN#, CLK_PCIE_LAN — CLK_PCIE_LAN1#, CLK_PCIE_LAN1

R2305 10KR2J-3-GP

R2301 10KR2J-3-GP: SMBALERT#/GPIO11 — PCH_GPIO11 — +3.3V_ALW

R2302 10KR2J-3-GP: SMBCLK — PCH_SMB_CLK; SMBDATA — PCH_SMB_DATA; SML0ALERT#/GPIO60 — TPM_ID1 — +3.3V_ALW; SML0CLK — SML0_CLK — SML0_CLK 9; SML0DATA — SML0_DATA — SML0_DATA 9

R2303 10KR2J-3-GP: SML1ALERT#/GPIO74 — LPD_SPI_INTR# — +3.3V_ALW; SML1CLK/GPIO58 — KBC_SCL1 — KBC_SCL1 37; SML1DATA/GPIO75 — KBC_SDA1 — KBC_SDA1 37

CL_CLK1 — CL_CLK — TP2301 Do Not Stuff

CL_DATA1 — CL_DATA — TP2302 Do Not Stuff

CL_RST1# — CL_RST# — TP2303 Do Not Stuff

R2304 10KR2J-3-GP: PEG_A_CLKRQ#/GPIO47 — PEG_CLKREQ#

CLKOUT_PEG_A_N/P — CLK_PCIE_VGA#/CLK_PCIE_VGA — CLK_PCIE_VGA# 80, CLK_PCIE_VGA 80

CLKOUT_DMI_N/P — CLK_EXP_N/CLK_EXP_P — CLK_EXP_N 9, CLK_EXP_P 9

CLKOUT_DP_N/P/CLKOUT_BCLK1_N/P — AT1, AT3

CLKIN_DMI_N/P — CLKIN_DMI#/CLKIN_DMI — CLKIN_DMI# 7, CLKIN_DMI 7

CLKIN_BCLK_N/P — CLK_CPU_BCLK#/CLK_CPU_BCLK — CLK_CPU_BCLK# 7, CLK_CPU_BCLK 7

CLKIN_DOT_96N/P — DREFCLK#/DREFCLK — DREFCLK# 7, DREFCLK 7

CLKIN_SATA_N/P/CKSSCD_N/P — CLK_PCIE_SATA#/CLK_PCIE_SATA — CLK_PCIE_SATA# 7, CLK_PCIE_SATA 7

REFCLK14IN — CLK_PCH_14M — CLK_PCH_14M 7

CLKIN_PCILOOPBACK — CLK_PCI_FB — CLK_PCI_FB 21

XTAL25_IN/XTAL25_OUT — XTAL25_IN

XCLK_RCOMP — XCLK_RCOMP — R2306 90D9R2F-1-GP — +1.05V_VTT

CLKOUTFLEX0/GPIO64 — CLK_PCH_GPIO64 — TP2304 Do Not Stuff

CLKOUTFLEX1/GPIO65 — P43

CLKOUTFLEX2/GPIO66 — T42

CLKOUTFLEX3/GPIO67 — CLK48_GPIO — R2307 33R2J-2-GP — CLK_48M_CARD 32

PCIECLKRQ0#/GPIO73 — PCIE_CLK_RQ0#

PCIECLKRQ1#/GPIO18 — PCIE_CLK_RQ1#

PCIECLKRQ2#/GPIO20 — MINI1_CLK_REQ#

PCIECLKRQ3#/GPIO25 — PCIE_CLK_RQ3#

PCIECLKRQ4#/GPIO26 — PCIE_CLKRQ4#

PCIECLKRQ5#/GPIO44 — PCIE_CLK_RQ5#

PEG_B_CLKRQ#/GPIO56 — PEG_B_CLKRQ#

+3.3V_ALW — RN2301 SRN4K7J-12-GP — SML0_CLK, SML0_DATA, KBC_SCL1, KBC_SDA1

+3.3V_ALW — RN2302 SRN2K2J-1-GP — PCH_SMB_CLK, PCH_SMB_DATA

+3.3V_RUN — RN2303 SRN2K2J-1-GP

Q2301 MN66D0LDW-7-GP: PCH_SMB_DATA — PCH_SMBDATA 7,18,19,76; PCH_SMB_CLK — PCH_SMBCLK 7,18,19,76

XTAL25_IN — R2308 Do Not Stuff

+3.3V_ALW — RN2307 SRN10KJ-7GP: PCIE_CLK_RQ0#, PEG_B_CLKRQ#, PCIE_CLKRQ4#, PCIE_CLK_RQ5#

+3.3V_RUN — RN2308 SRN10KJ-5-GP: PCIE_CLK_RQ1#, MINI1_CLK_REQ#

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 23 of 92

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

82.30001.861

U2001A — 1 OF 10 — IBEXPEAK-M-GP-NF

HDD

ODD

DISCRETE PARK

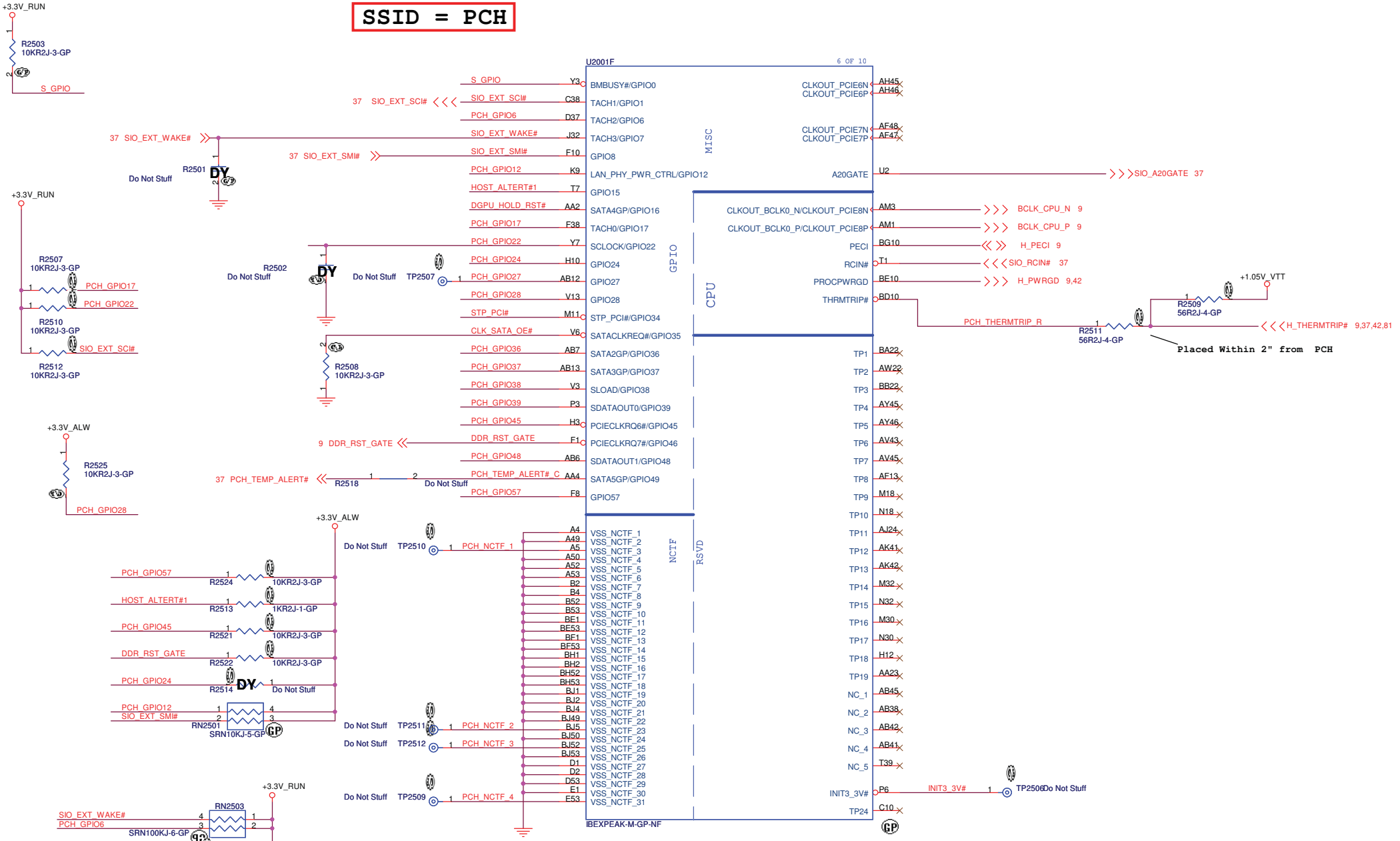
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 24 of 92

SSID = PCH



DISCRETE PARK

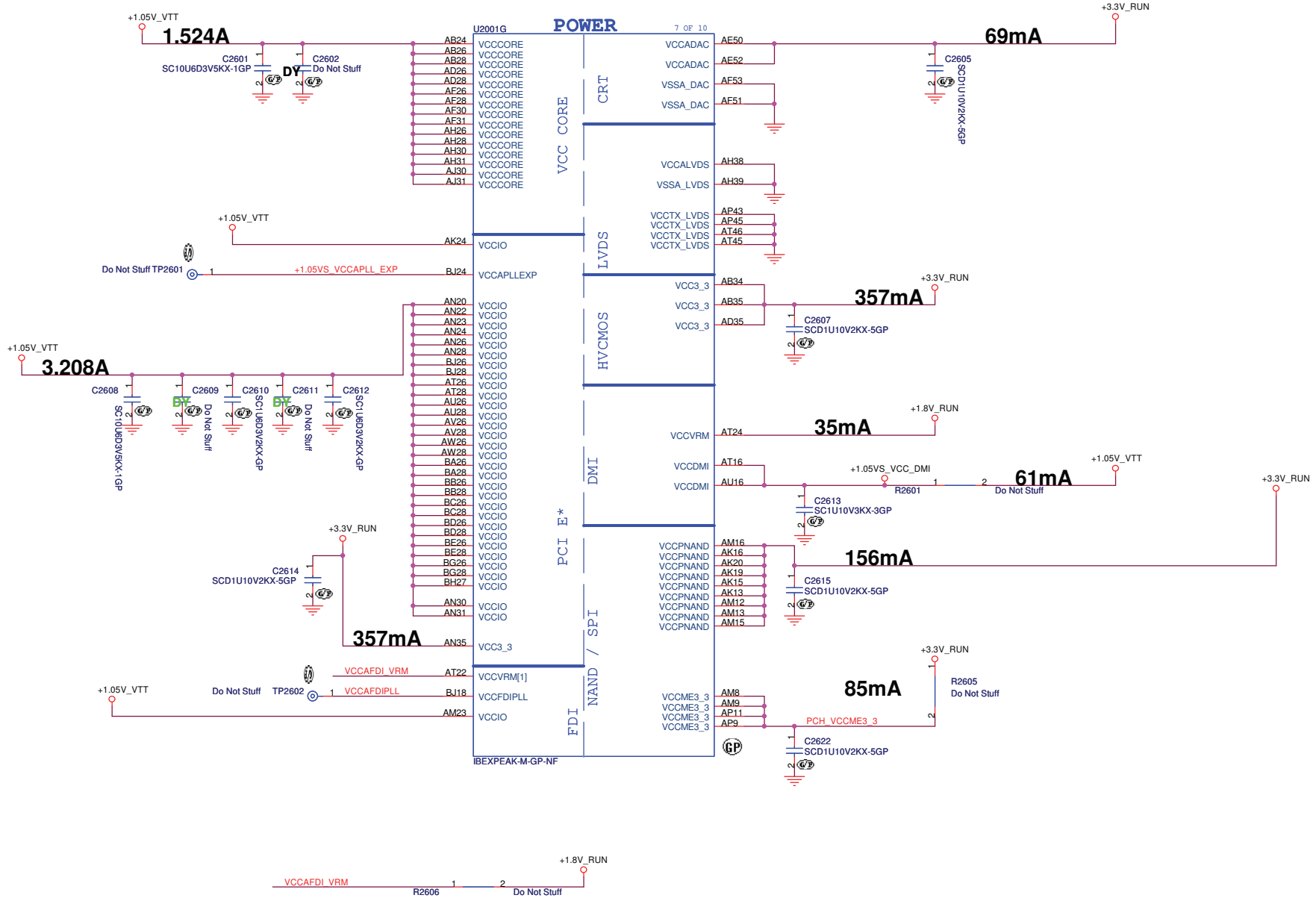
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
	Arsenal DJ1 Discrete	A01

Date: Thursday, May 06, 2010 Sheet 25 of 92

SSID = PCH



DISCRETE PARK

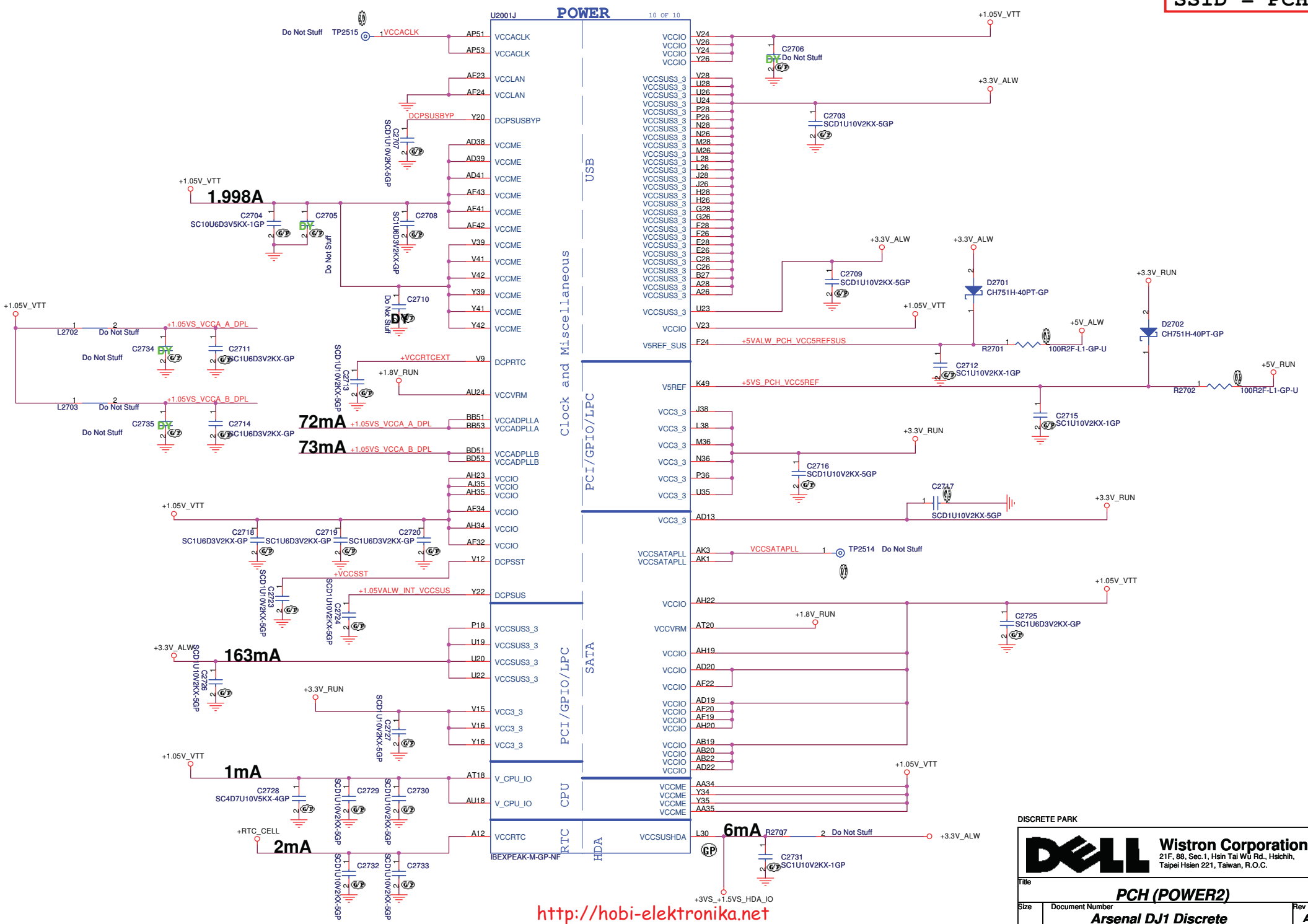
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 26 of 92

SSID = PCH



DISCRETE PARK

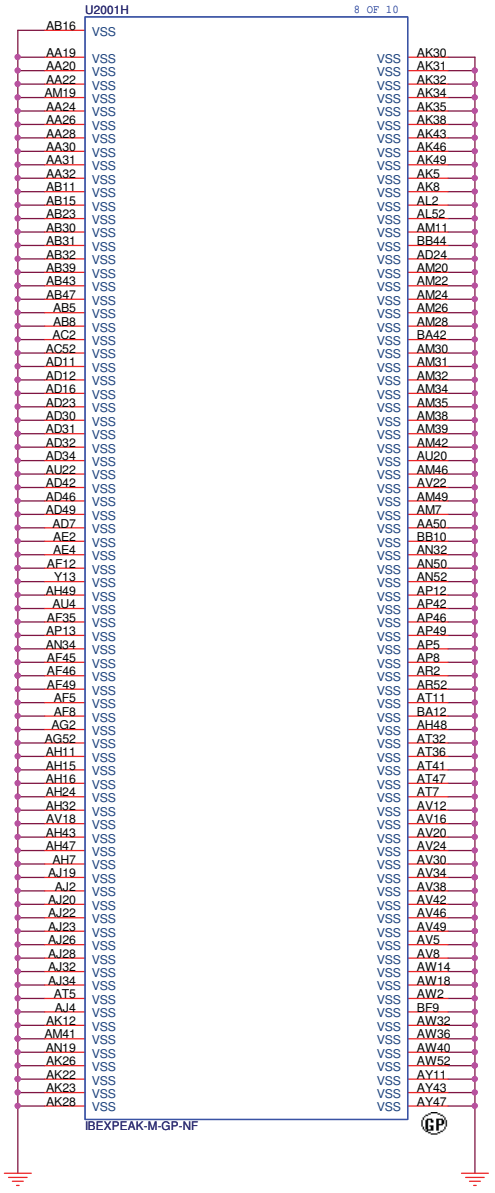
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

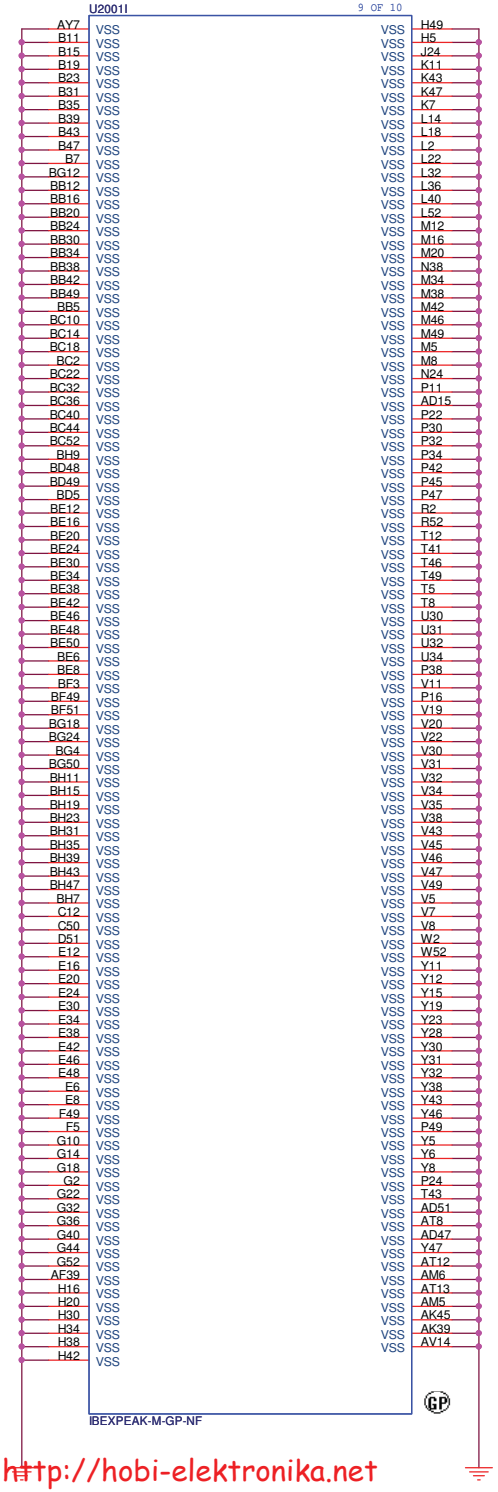
Title: PCH (POWER2)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 27 of 92

SSID = PCH





DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 28 of 92

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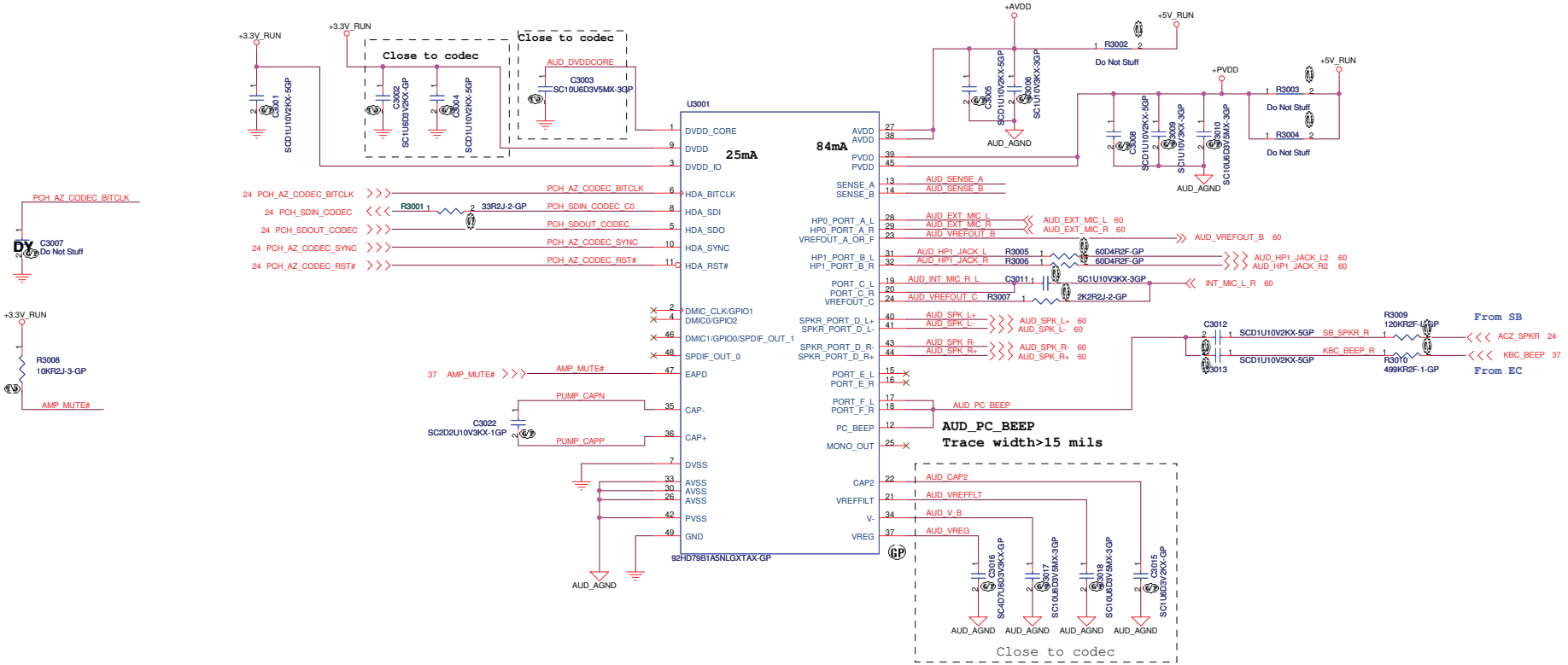
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

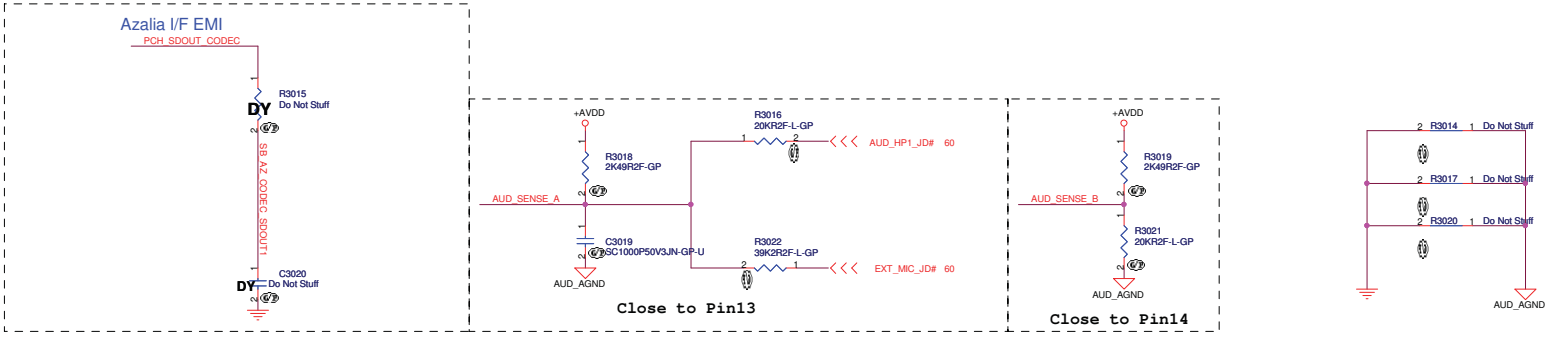
Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *A01*

Date: Thursday, May 06, 2010 | Sheet 29 of 92

SSID = AUDIO





DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec 92HD79B1**

Size: Custom | Document Number: **Arsenal DJ1 Discrete** | Rev: **A01**

Date: Thursday, May 06, 2010 | Sheet 30 of 92

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DISCRETE PARK

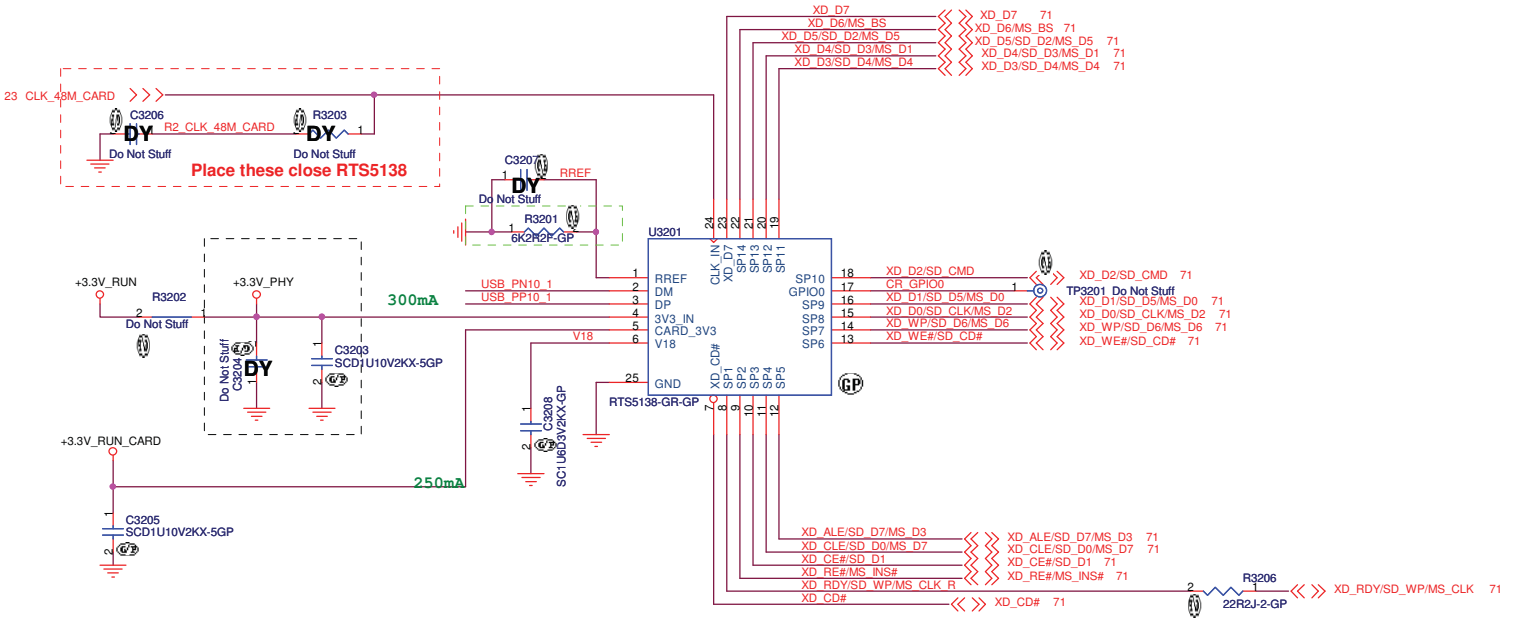
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

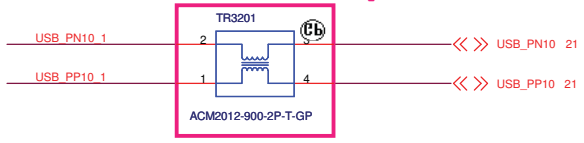
Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 31 of 92

SSID = SDIO



A00 10.03.09 EMI requirement



DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 32 of 92

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 36 of 92

CAP close to VCC-GND pin pair

SSID = KBC

A00 10.02.24

A00 10.03.22

U3701A

NPCE781BA0DX-GP

MB VERSION ID		
	VER1	VER0
X00	0	0
X01	0	1
X02	1	0
A00	1	1

KBC CLK
EMI

PH for DJ
Internal PL for DG

A00 10.02.24 GPU table

VGA STRAP option		
	GPIO24 (KBC_BIOS_ID)	GPIO05 (DISCRETE_ID)
UMA	0	Reserve
Madison,M96, M92 or PARK	1	Reserve

A00 10.03.15
POP when support RCID function

U3701B

NPCE781BA0DX-GP

A00 10.02.24

U3702

Q3702
PMBS3906-GP

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 37 of 92

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DISCRETE PARK

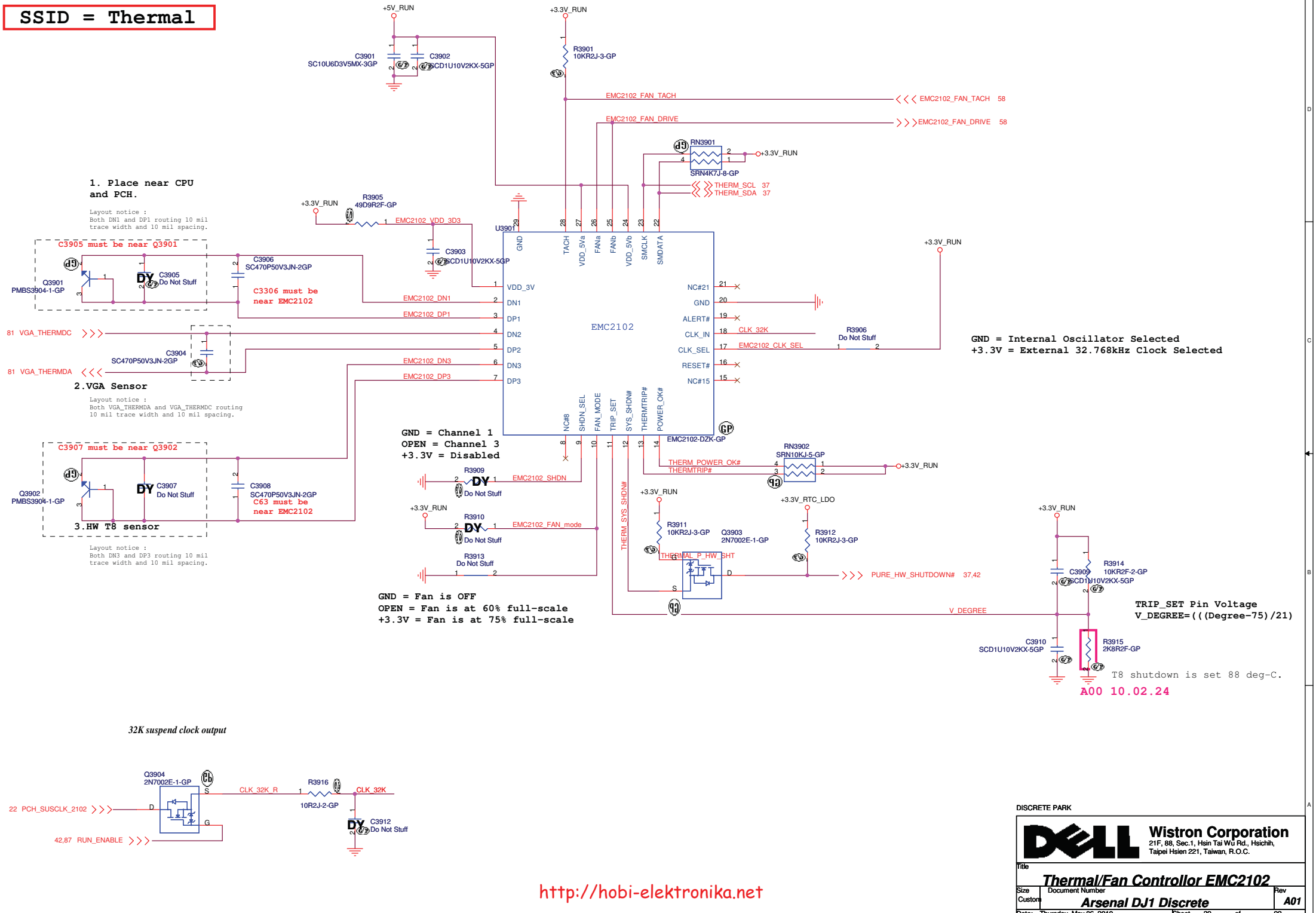
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *A01*

Date: Thursday, May 06, 2010 | Sheet 38 of 92

SSID = Thermal



http://hobi-elektronika.net

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 39 of 92

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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DISCRETE PARK

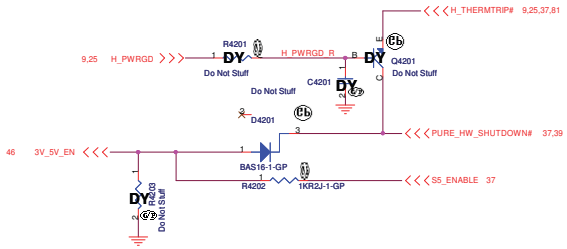
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *A01*

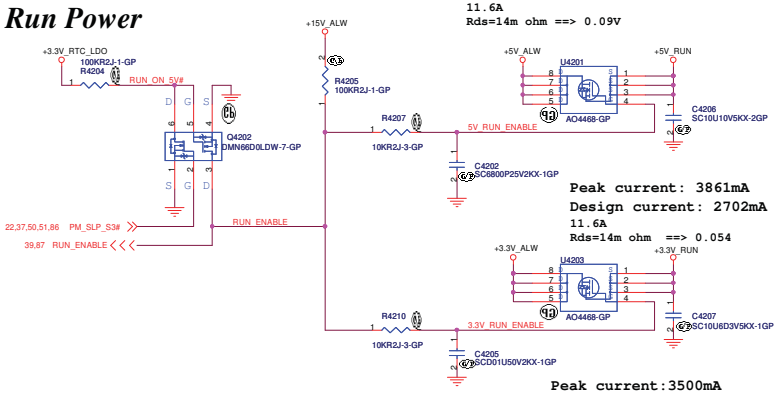
Date: Thursday, May 06, 2010 | Sheet 41 of 92

SSID = Reset.Suspend



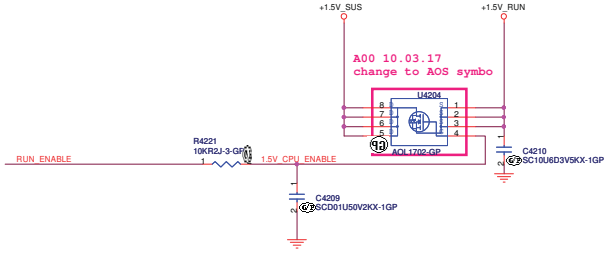
Run Power

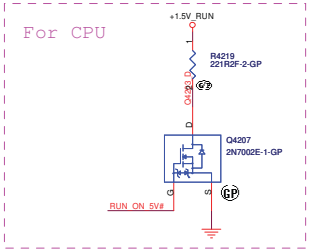
Peak current: 6370mA (HD:1100 ODD:2500)
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V



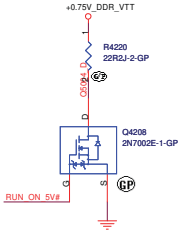
Peak current: 3861mA
Design current: 2702mA
11.6A
Rds=14m ohm ==> 0.054

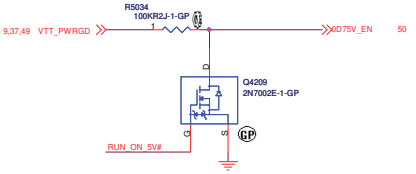
Peak current:3500mA
Design current: 2450mA
24.3A
Rds=4.7m ohm ==> 0.01645





425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7





DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A2	Arsenal DJ1 Discrete	A01

Date: Thursday, May 06, 2010 Sheet 42 of 92

(Blanking)

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 43 of 92

(Blanking)

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 44 of 92

(Blanking)

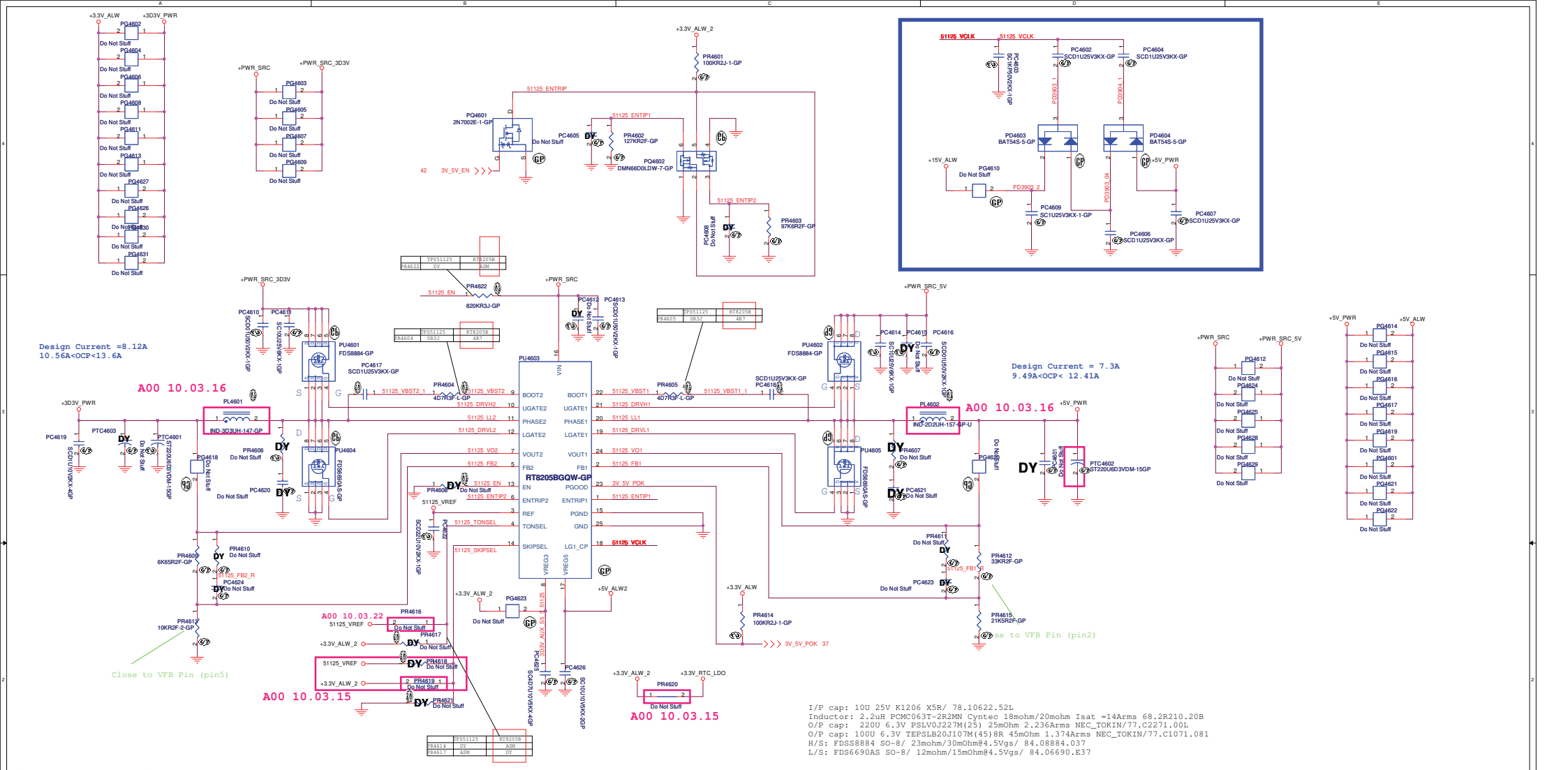
DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 45 of 92



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

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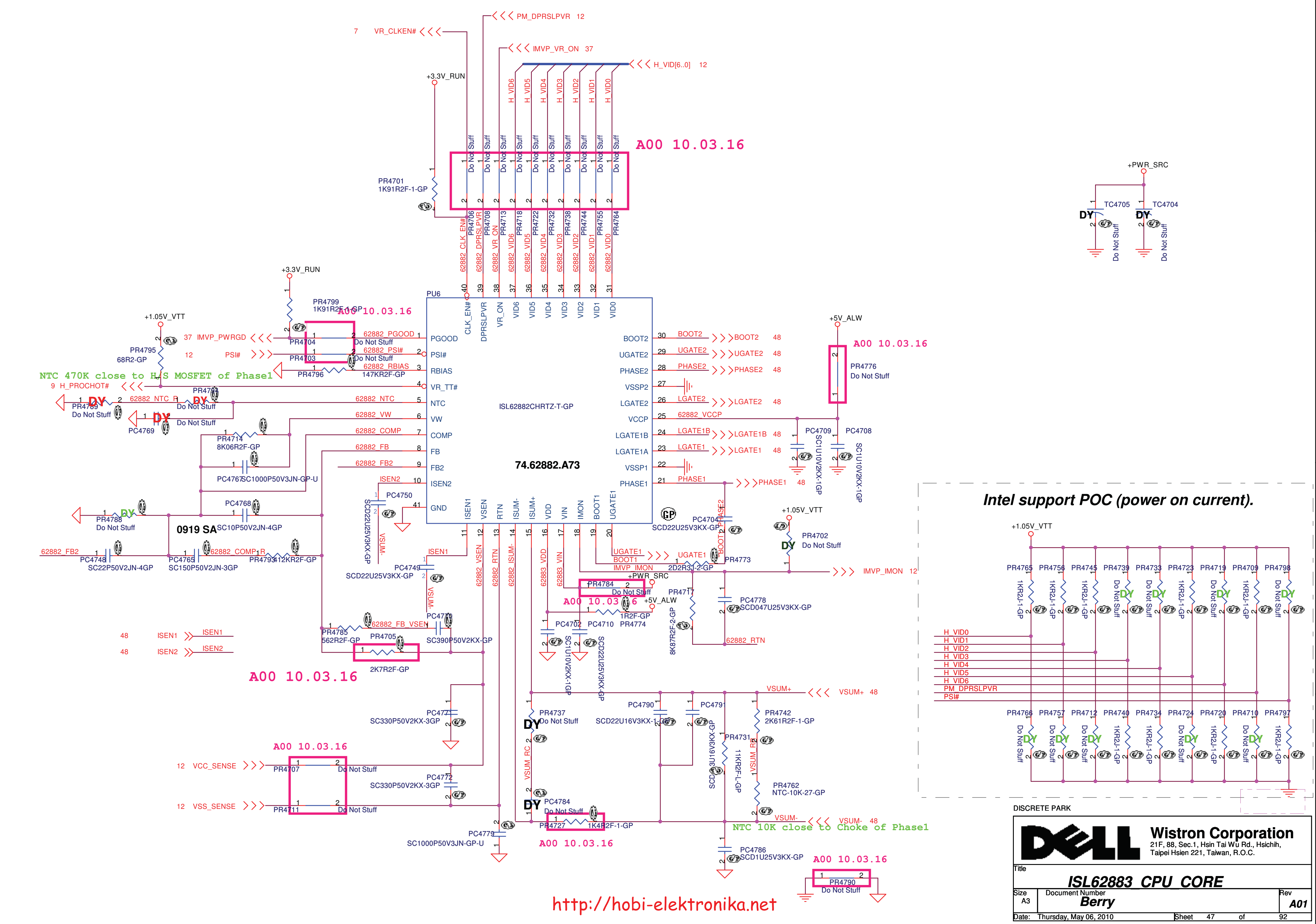
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 46 of 92



PM_DPRSLPVR 12
VR_CLKEN# 7
IMVP_VR_ON 37
H_VID[6..0] 12
+3.3V_RUN
A00 10.03.16
PR4701 1K91R2F-1-GP
PU6
ISL62882CHRTZ-T-GP
74.62882.A73
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
CLK_EN#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
PR4799 1K91R2F-1-GP
+1.05V_VTT
37 IMVP_PWRGD
12 PSI#
PR4795 68R2-GP
NTC 470K close to H/S MOSFET of Phase1
9 H_PROCHOT#
PR4714 8K06R2F-GP
PC4767 SC1000P50V3JN-GP-U
PC4768 SC10P50V2JN-4GP
0919 SA
62882_FB2
PC4748 SC22P50V2JN-4GP
PC4765 SC150P50V2JN-3GP
PR4793 12KR2F-GP
PR4796 147KR2F-GP
PR4785 562R2F-GP
PR4705 2K7R2F-GP
SC390P50V2KX-GP
48 ISEN1
48 ISEN2
A00 10.03.16
12 VCC_SENSE
12 VSS_SENSE
PR4707 Do Not Stuff
PR4711 Do Not Stuff
PC4771 SC330P50V2KX-3GP
PC4772 SC330P50V2KX-3GP
PC4779 SC1000P50V3JN-GP-U
PR4737 Do Not Stuff
PC4784 Do Not Stuff
PR4727 1K4R2F-1-GP
PC4790 SCD22U16V3KX-1-GP
PC4791
PR4731 11KR2F-L-GP
PR4742 2K61R2F-1-GP
PR4762 NTC-10K-27-GP
VSUM+ 48
VSUM- 48
NTC 10K close to Choke of Phase1
PC4786 SCD1U25V3KX-GP
PR4790 Do Not Stuff
+PWR_SRC
TC4705
TC4704
Do Not Stuff
+5V_ALW
PR4776 Do Not Stuff
PC4709 SC1U10V2KX-1GP
PC4708 SC1U10V2KX-1GP
PC4704 SCD22U25V3KX-GP
PR4702 Do Not Stuff
PR4773 2D2R3J-2-GP
IMVP_IMON 12
PR4784 Do Not Stuff
PR4774 1R2F-GP
PR4717 8K87R2F-2-GP
PC4778 SCD047U25V3KX-GP
PC4702 SC1U10V2KX-1GP
PC4710 SCD22U25V3KX-GP
PC4750 SCD22U25V3KX-GP
PC4749 SCD22U25V3KX-GP
Intel support POC (power on current).
PR4765 PR4756 PR4745 PR4739 PR4733 PR4723 PR4719 PR4709 PR4798
PR4766 PR4757 PR4712 PR4740 PR4734 PR4724 PR4720 PR4710 PR4797
1KR2J-1-GP
H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6 PM_DPRSLPVR PSI#
DY
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DISCRETE PARK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62883_CPU_CORE
Size A3
Document Number Berry
Rev A01
Date: Thursday, May 06, 2010
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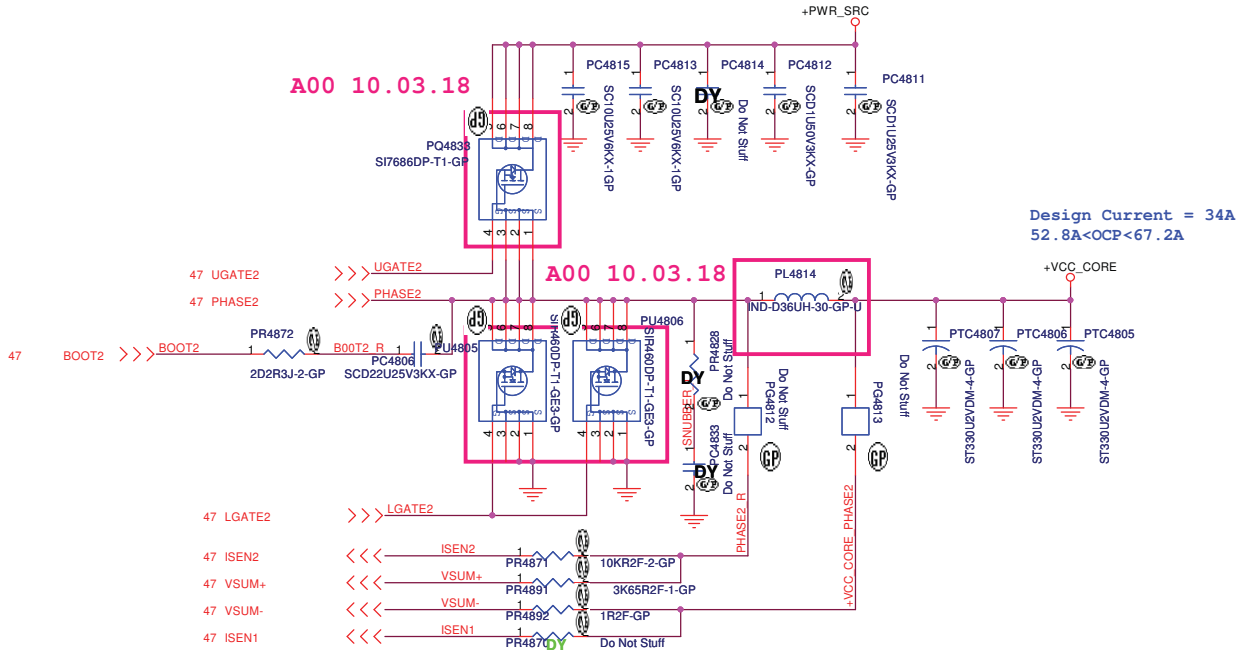

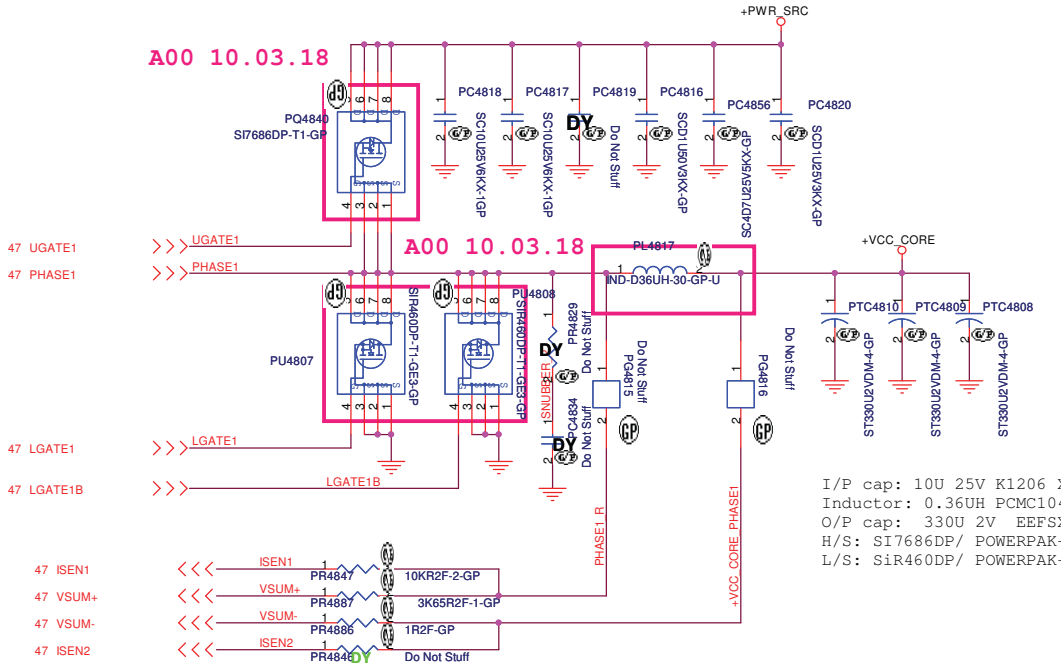

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

DISCRETE PARK

Wistron Corporation
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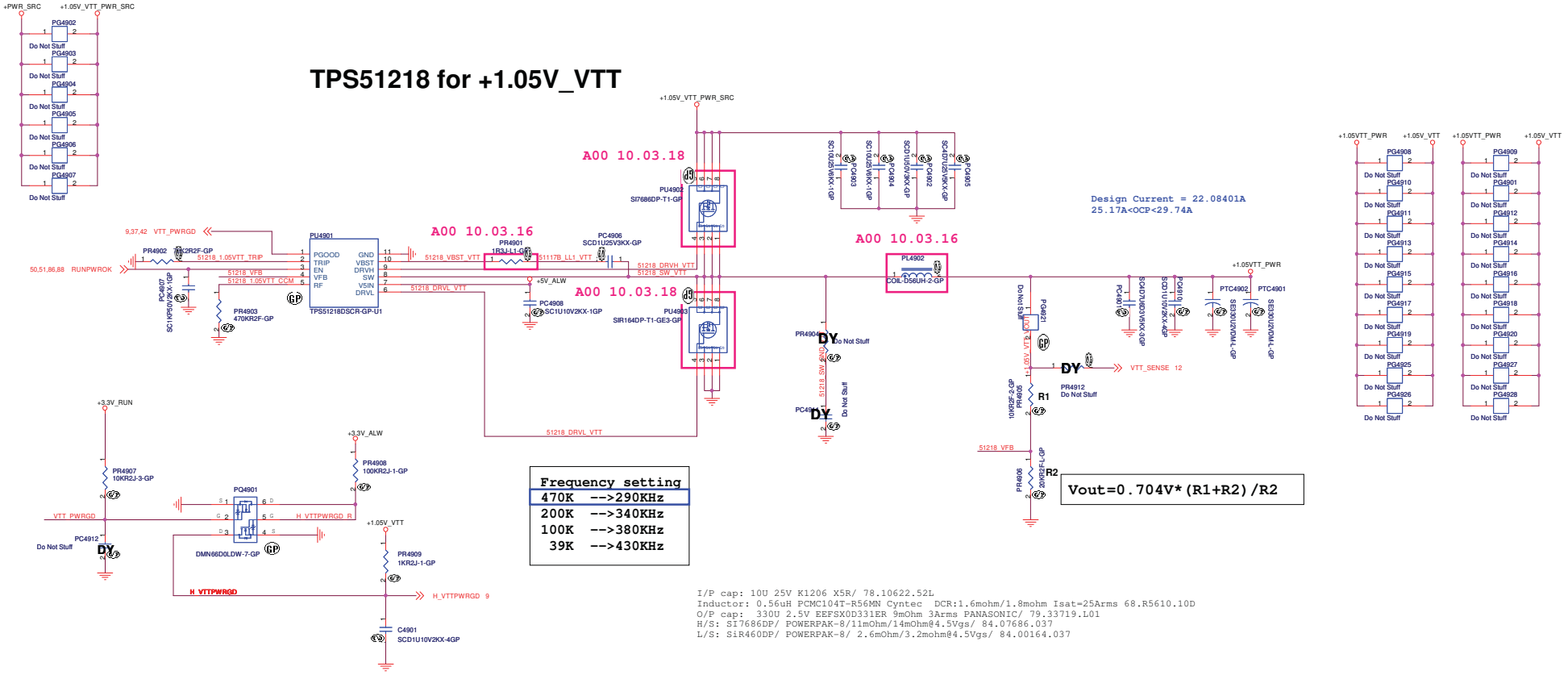
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size	Document Number	Rev
A3	Berry	A01

Date: Thursday, May 06, 2010 Sheet 48 of 92

TPS51218 for +1.05V_VTT



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

DISCRETE PARK

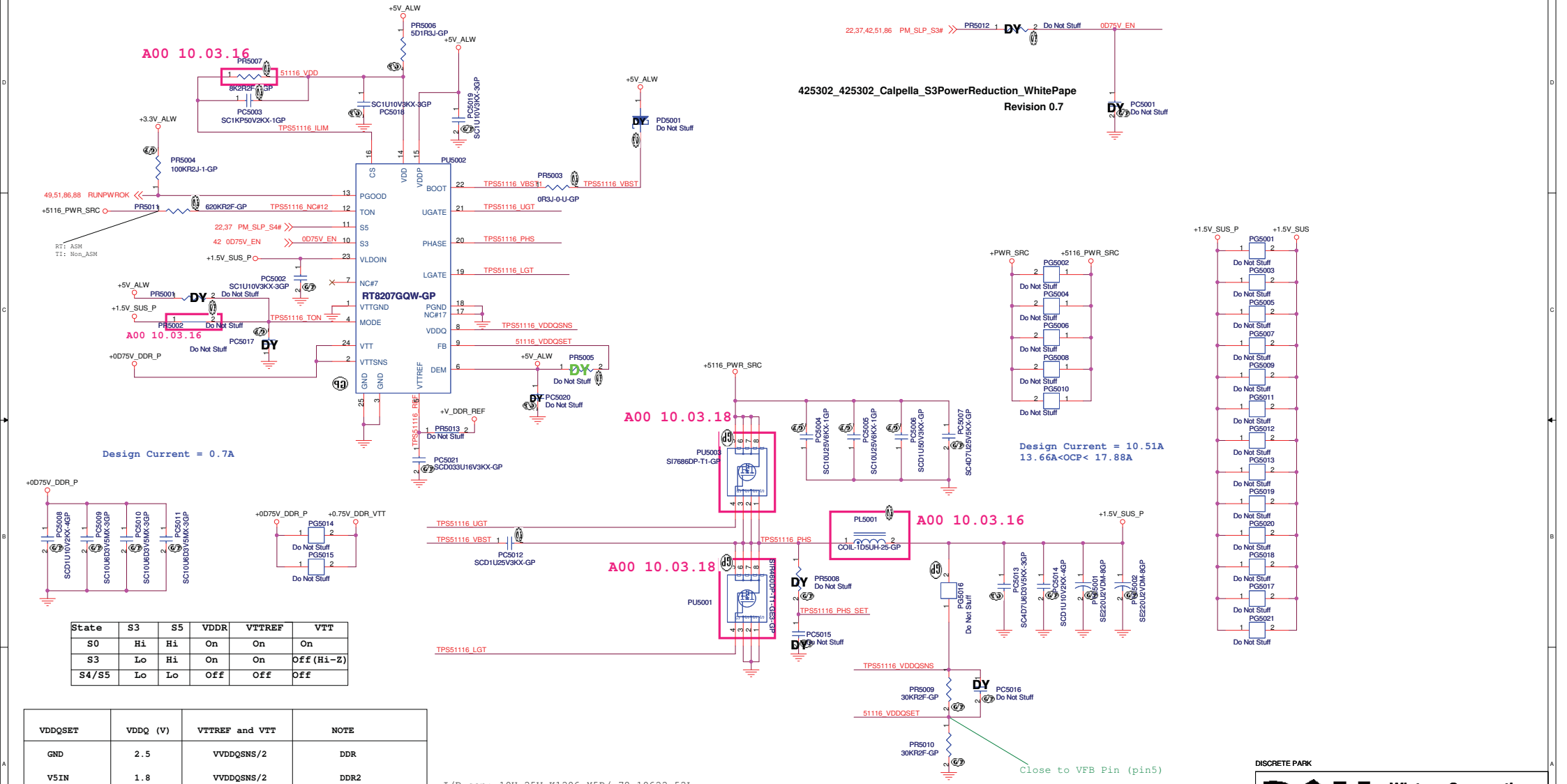
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V VTT

Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 49 of 92

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5uH PCMC104T-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

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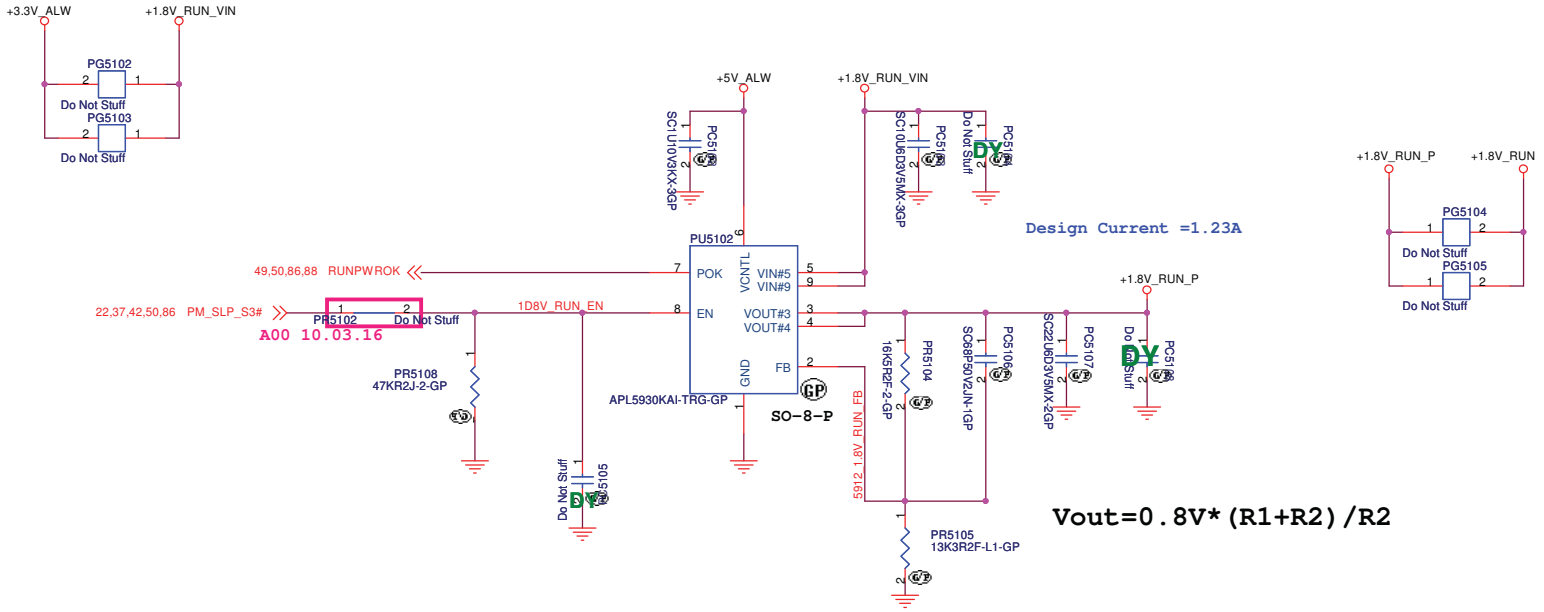
Title: TPS51116_+1.5V_SUS
Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: A01
Date: Thursday, May 06, 2010 | Sheet 50 of 92

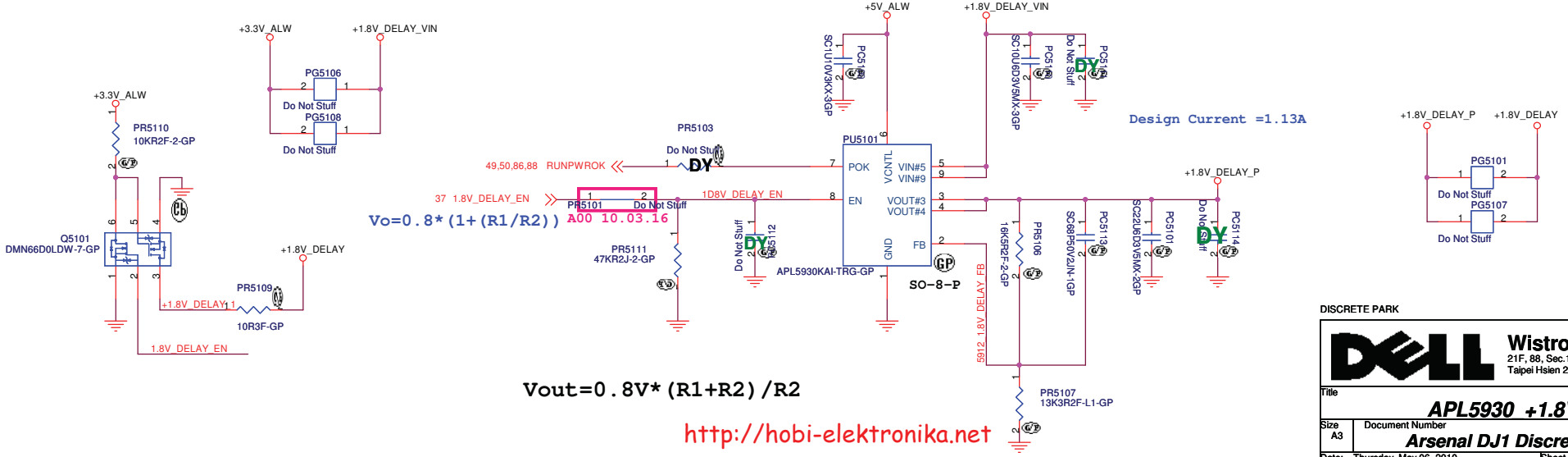
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_DELAY



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930 +1.8V_RUN

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

Date: Thursday, May 06, 2010 Sheet 51 of 92

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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DISCRETE PARK

Wistron Corporation
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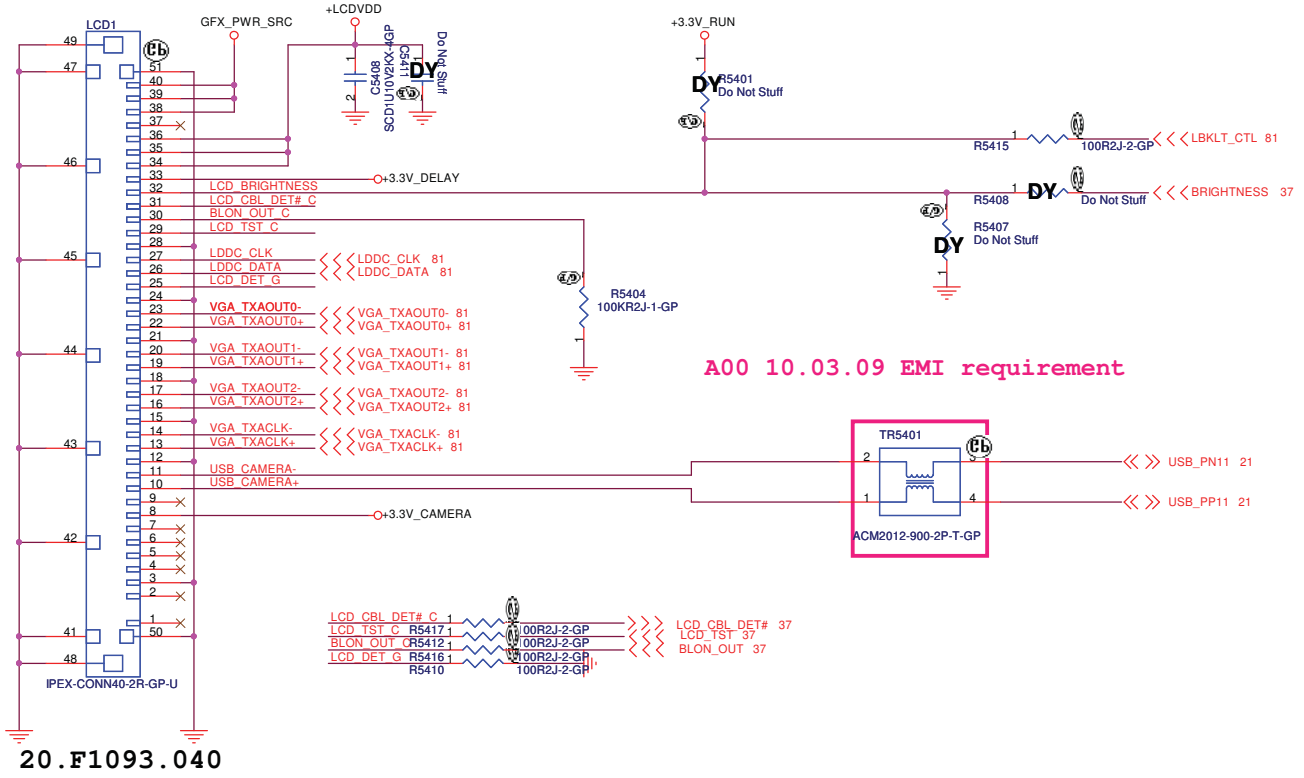
Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 53 of 92

SSID = VIDEO

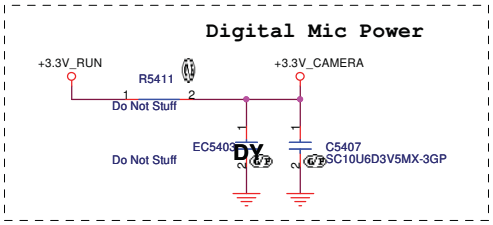
LVDS CONNECTOR



A00 10.03.09 EMI requirement

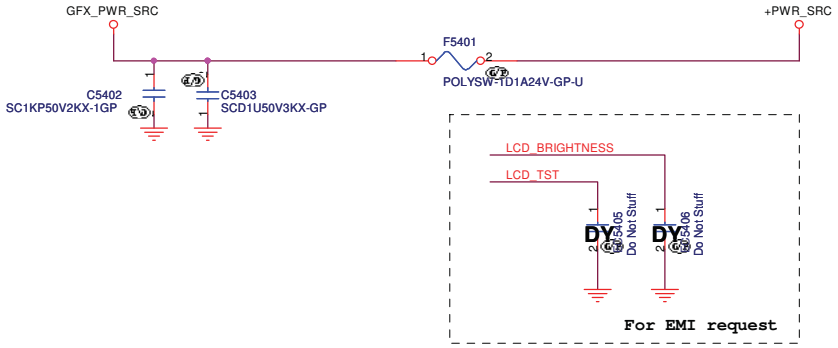
20.F1093.040

Digital Mic Power



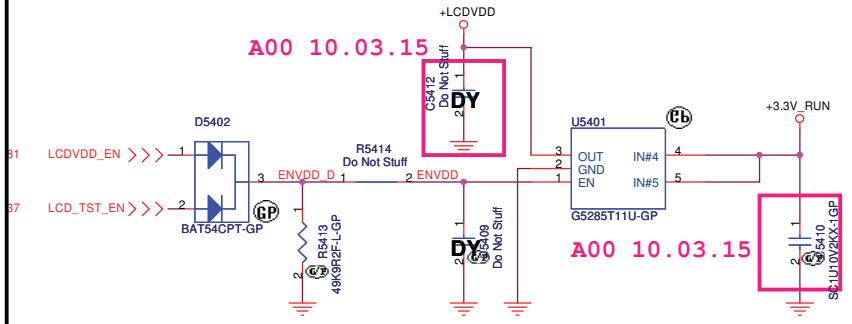
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



DISCRETE PARK

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

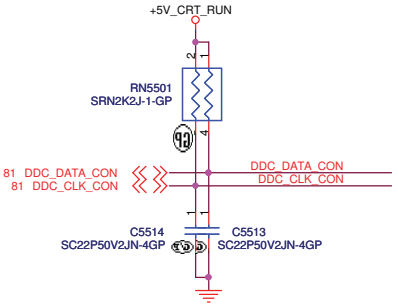
Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

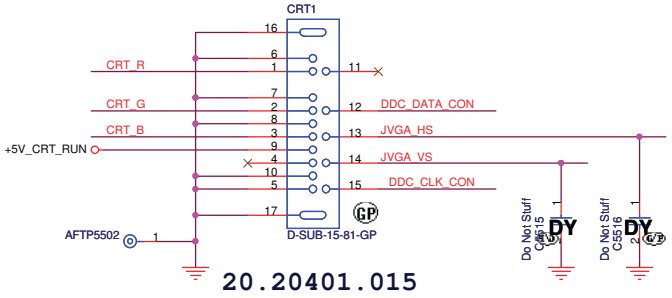
Date: Thursday, May 06, 2010 Sheet 54 of 92

SSID = VIDEO

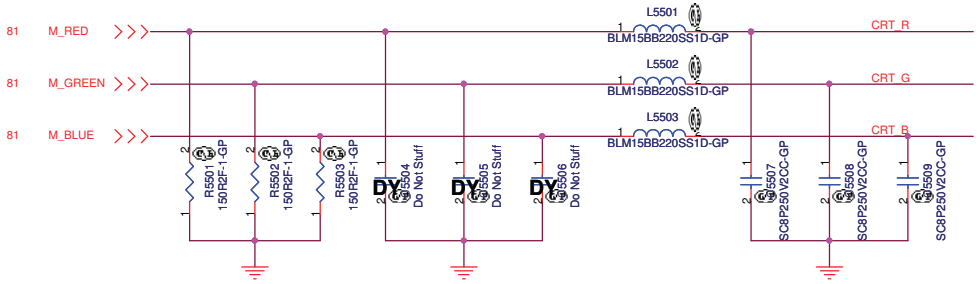
Layout Note:

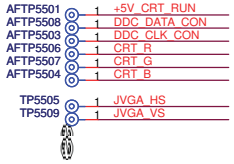
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



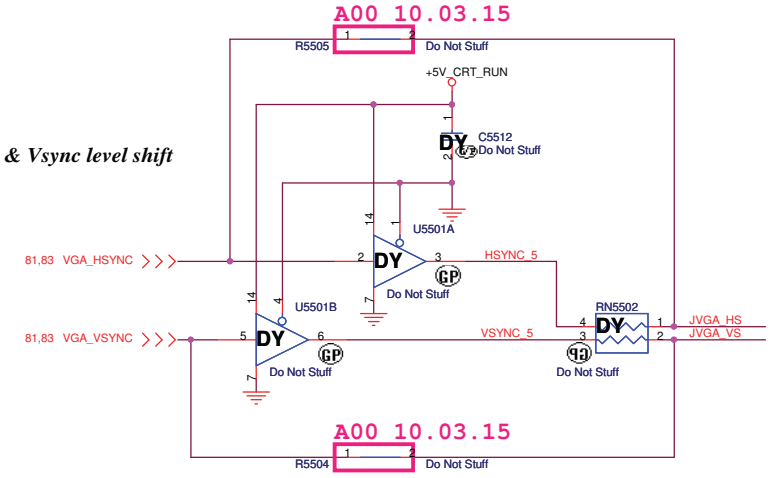


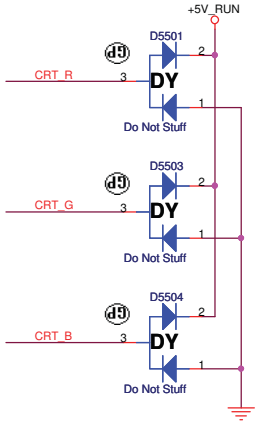
20.20401.015

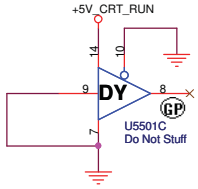


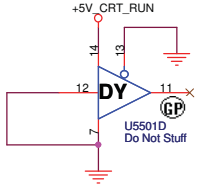


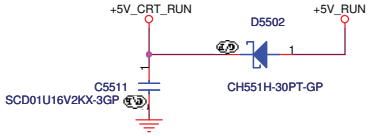
Hsync & Vsync level shift











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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size | Document Number: Arsenal DJ1 Discrete | Rev: A01

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

Date: Thursday, May 06, 2010 Sheet 56 of 92

(Blanking)

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

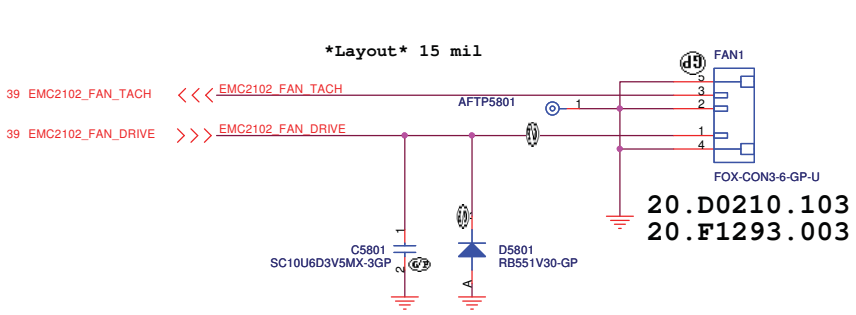
Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

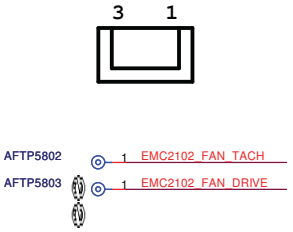
Date: Thursday, May 06, 2010 Sheet 57 of 92

SSID = User.Interface

SSID = Thermal

Fan Connector





DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: A01

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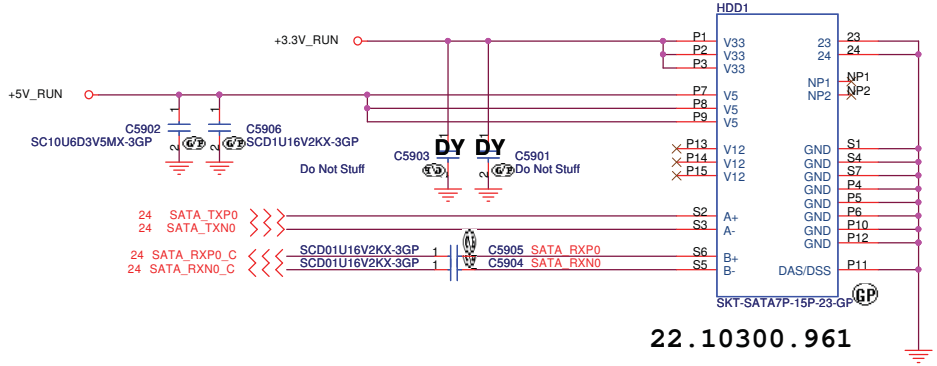
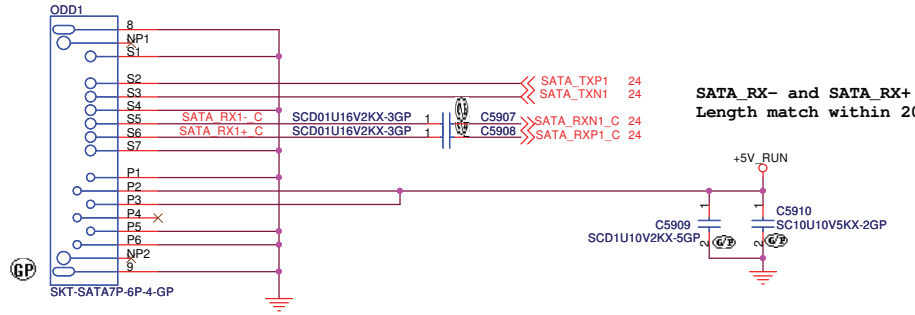
SSID = SATA

SATA HDD Connector



22.10300.961

ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

22.10300.811
22.10300.471

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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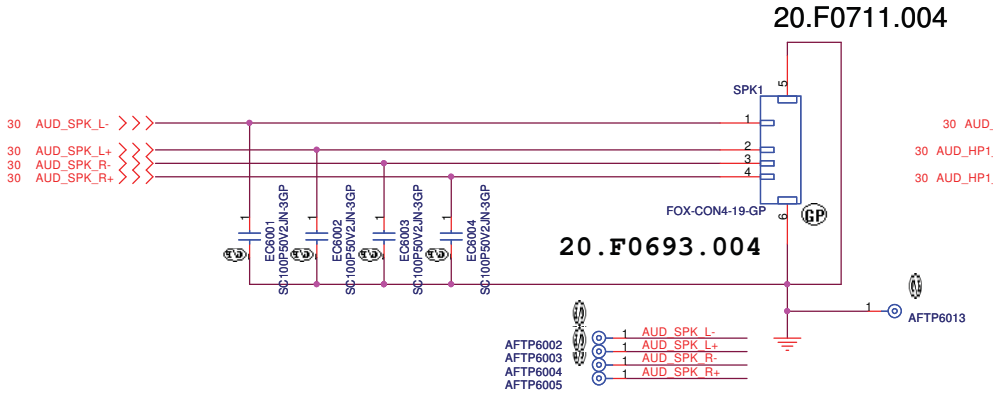
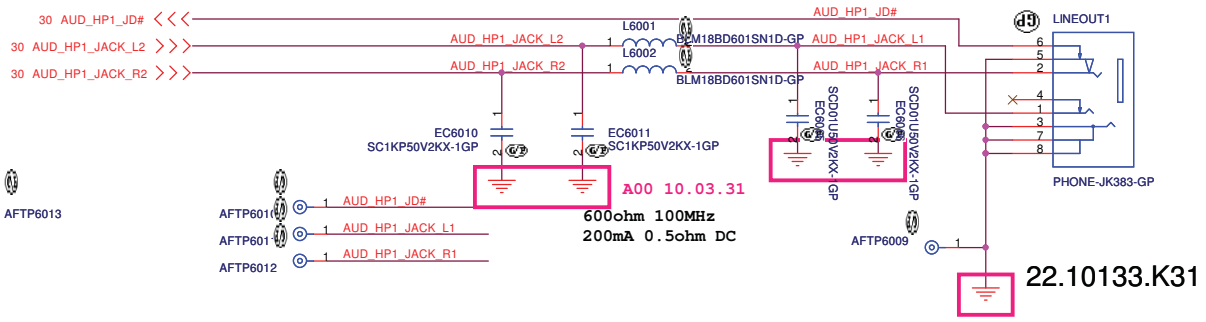
SSID = AUDIO

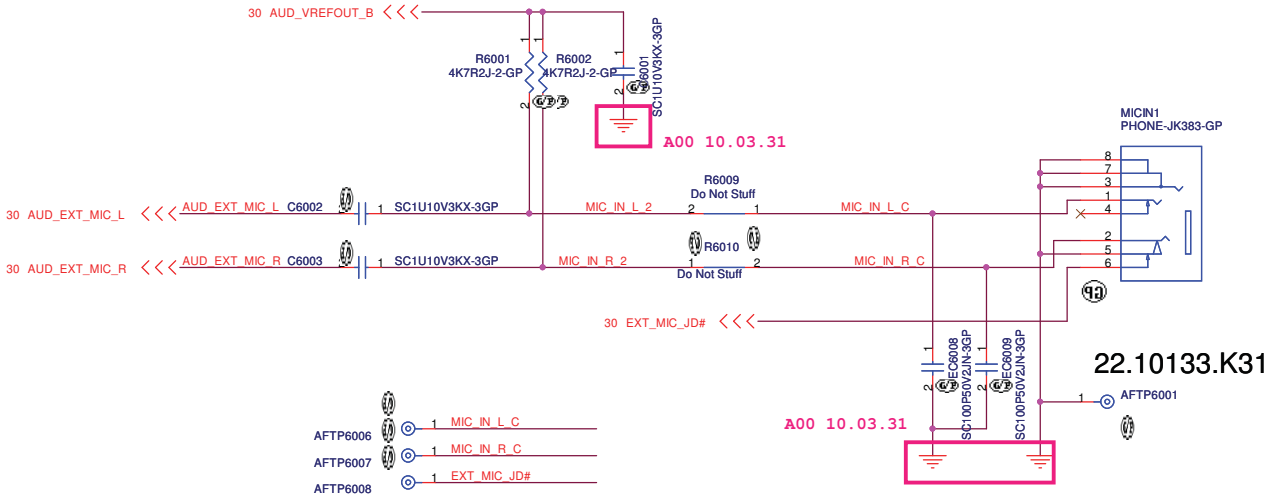
Speaker Connector



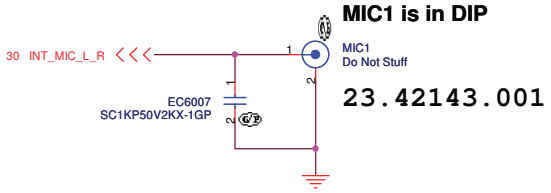
LINE1 OUT



MIC IN



Internal Microphone



DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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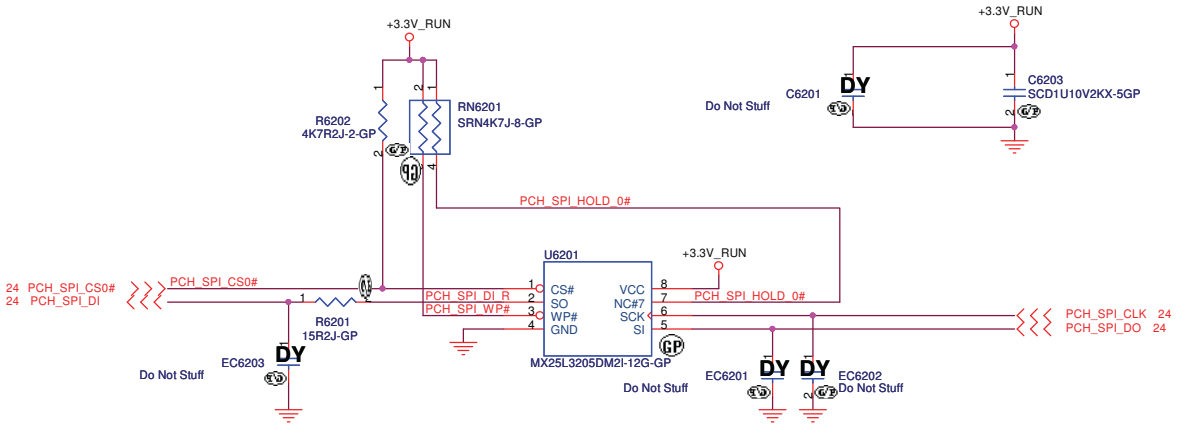
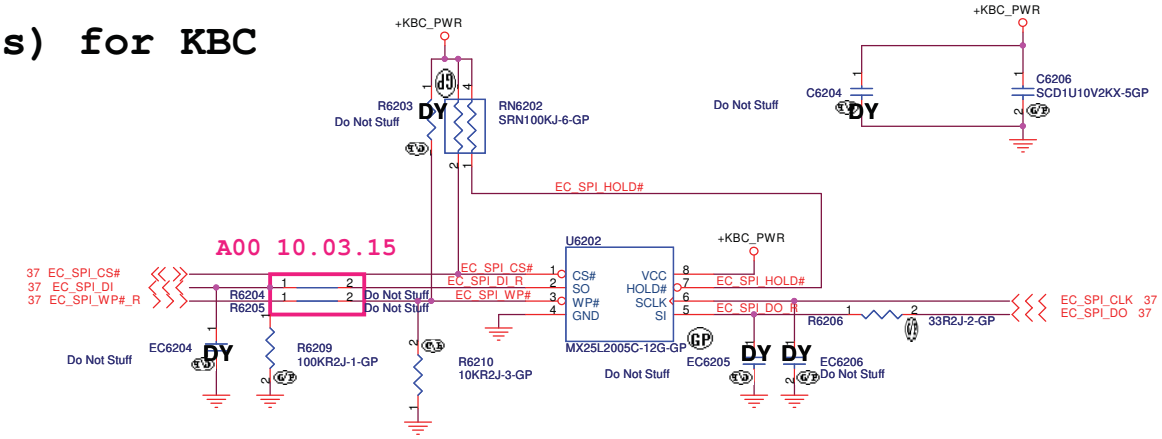
SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

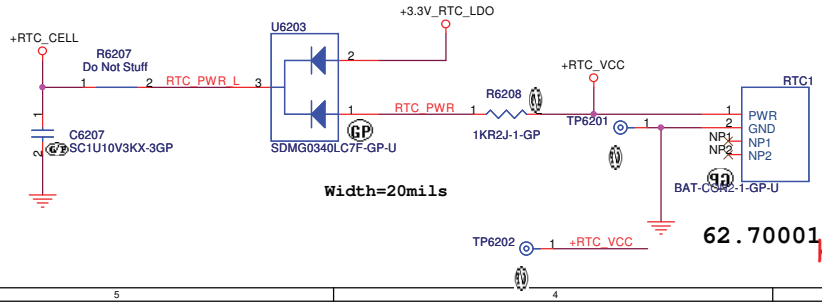


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



62.70001.011

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: A01

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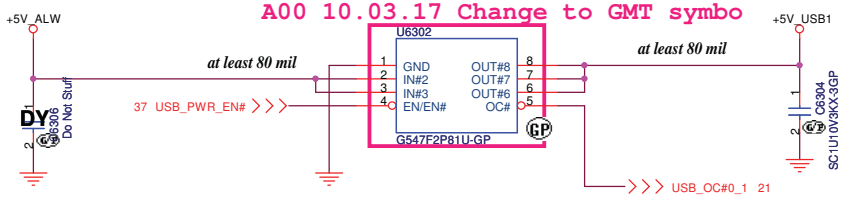
SSID = USB

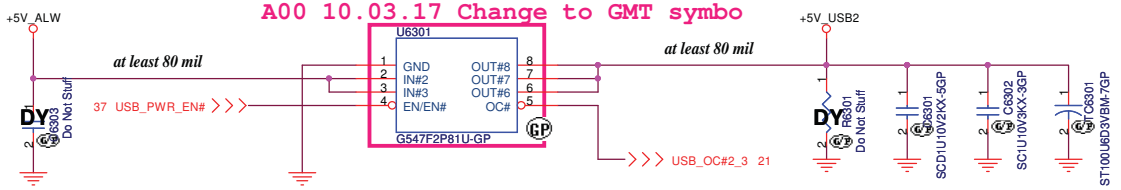
IO Board USB Power

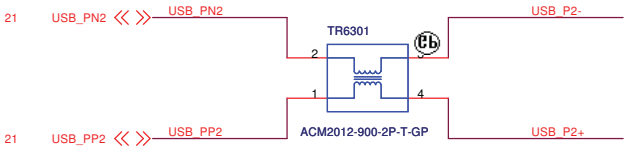
A00 10.03.17 Change to GMT symbo

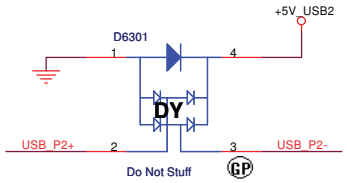


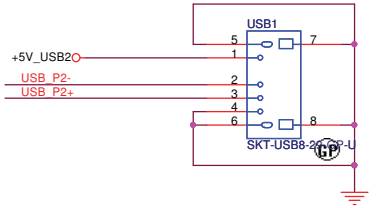
Right USB Power

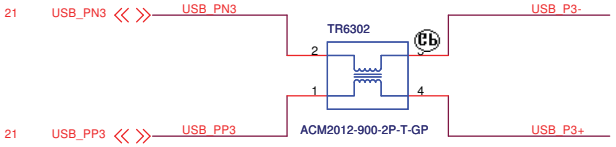
A00 10.03.17 Change to GMT symbo

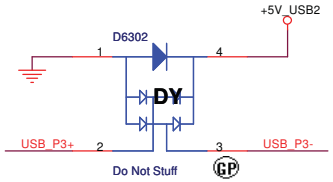


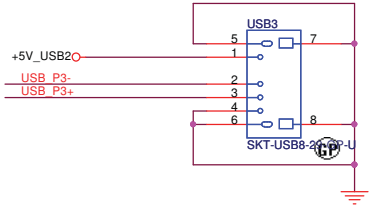












22.10254.451

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB		
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *A01*

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

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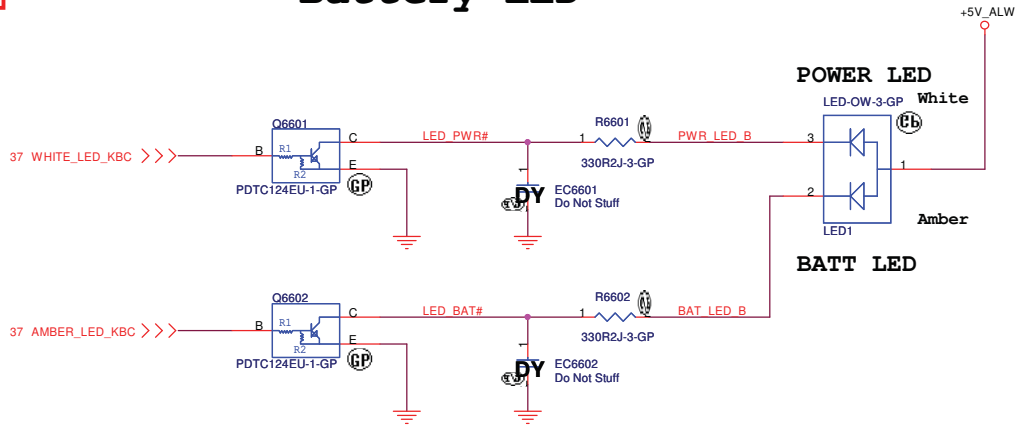
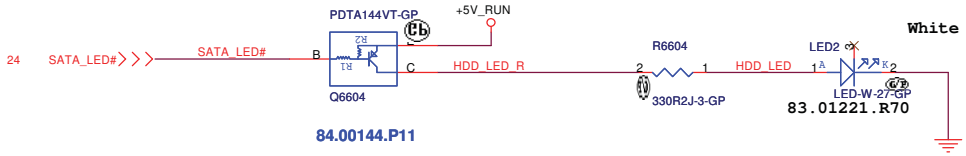
SSID = User.Interface

Battery LED



83.00326.G70
83.01222.K70

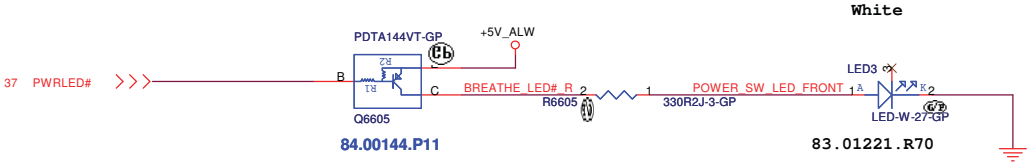
HDD LED



84.00144.P11

83.01221.R70

BREATHE PWR LED (Front)



84.00144.P11

83.01221.R70

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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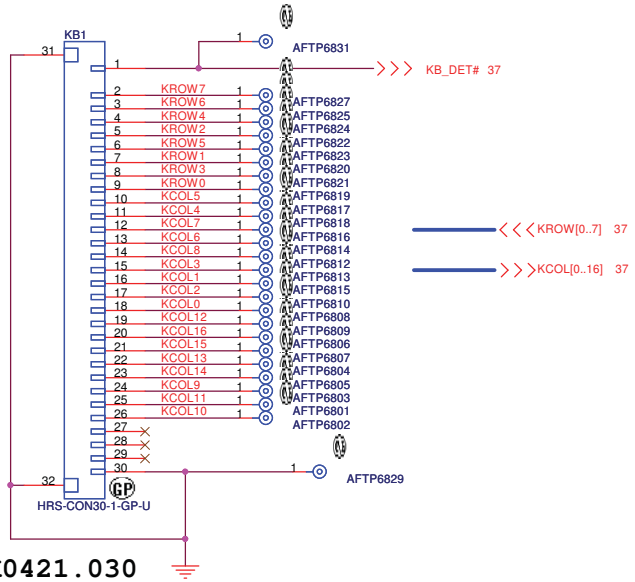
SSID = KBC

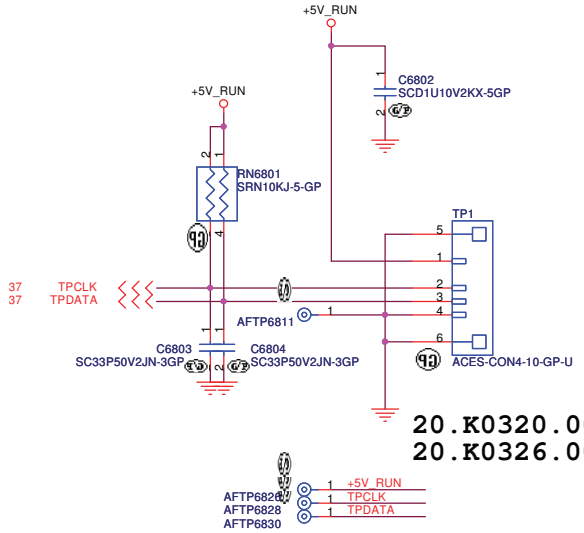
Internal KeyBoard Connector



Main 20.K0421.030
20.K0259.030

SSID = Touch.Pad

TouchPad Connector



20.K0320.004
20.K0326.004

DISCRETE PARK

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

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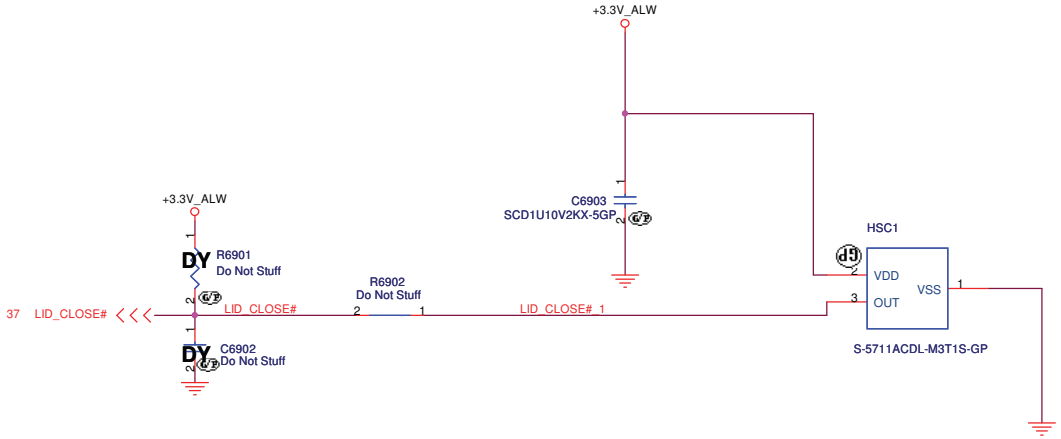

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

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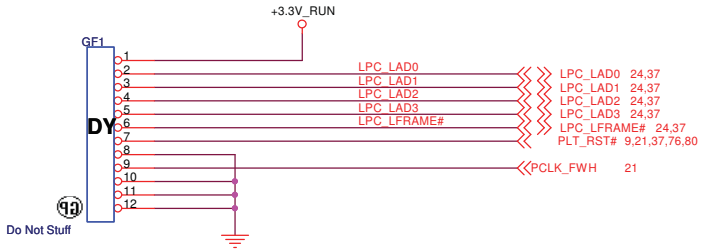

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Arsenal DJ1 Discrete*	*A01*

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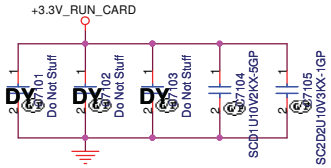
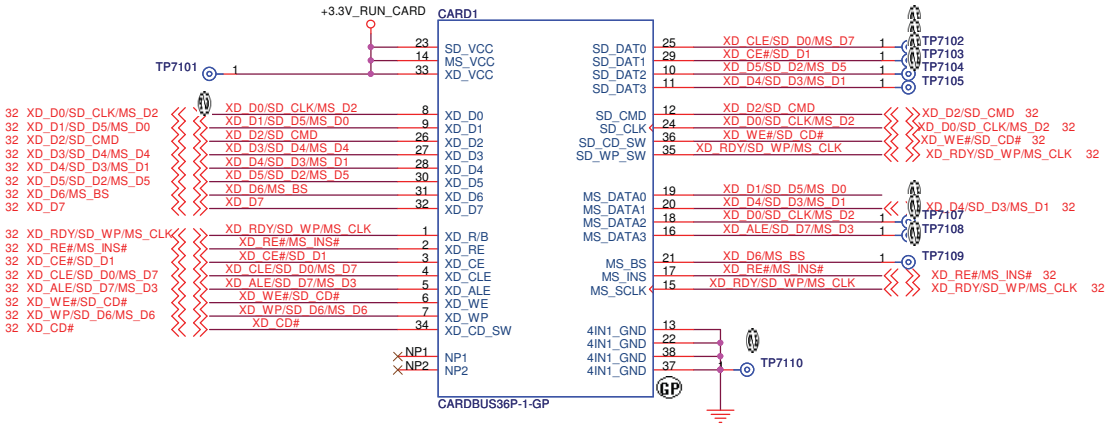
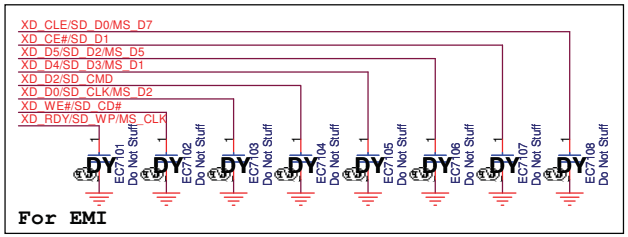
SSID = SDIO

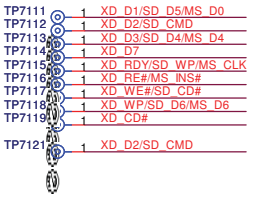
SD/XD/MS Card Reader





20.I0109.001
20.I0081.011





http://hobi-elektronika.net

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

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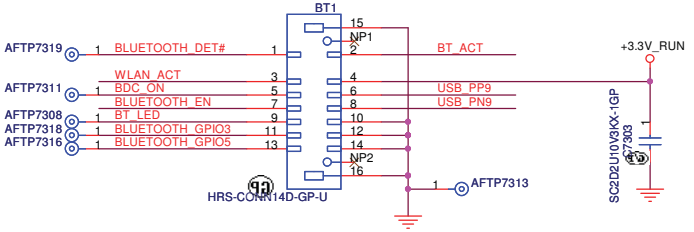
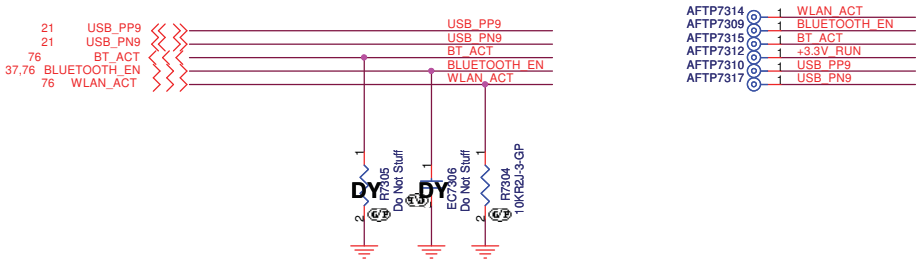
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014



DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

Size	Document Number	Rev
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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A3	*Arsenal DJ1 Discrete*	*A01*

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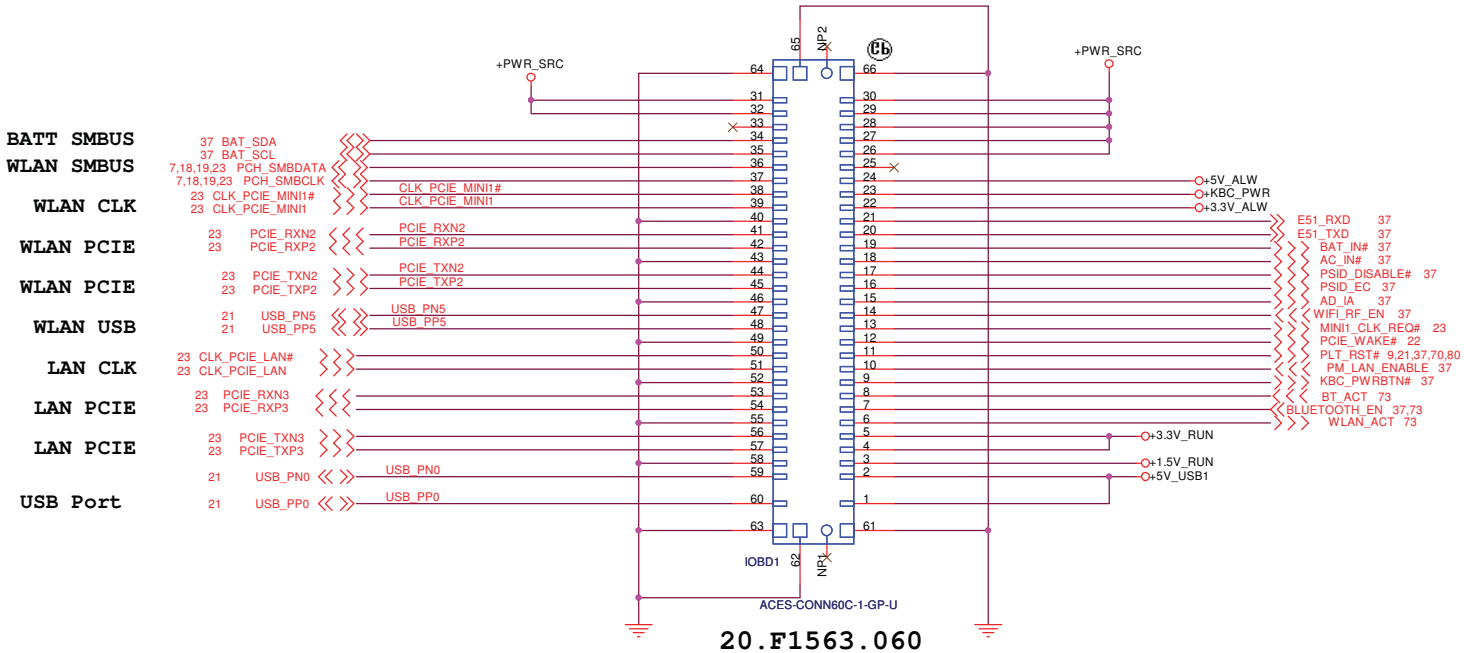
SSID = PWR.Support



20.F1563.060

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Arsenal DJ1 Discrete* | Rev: *A01*

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DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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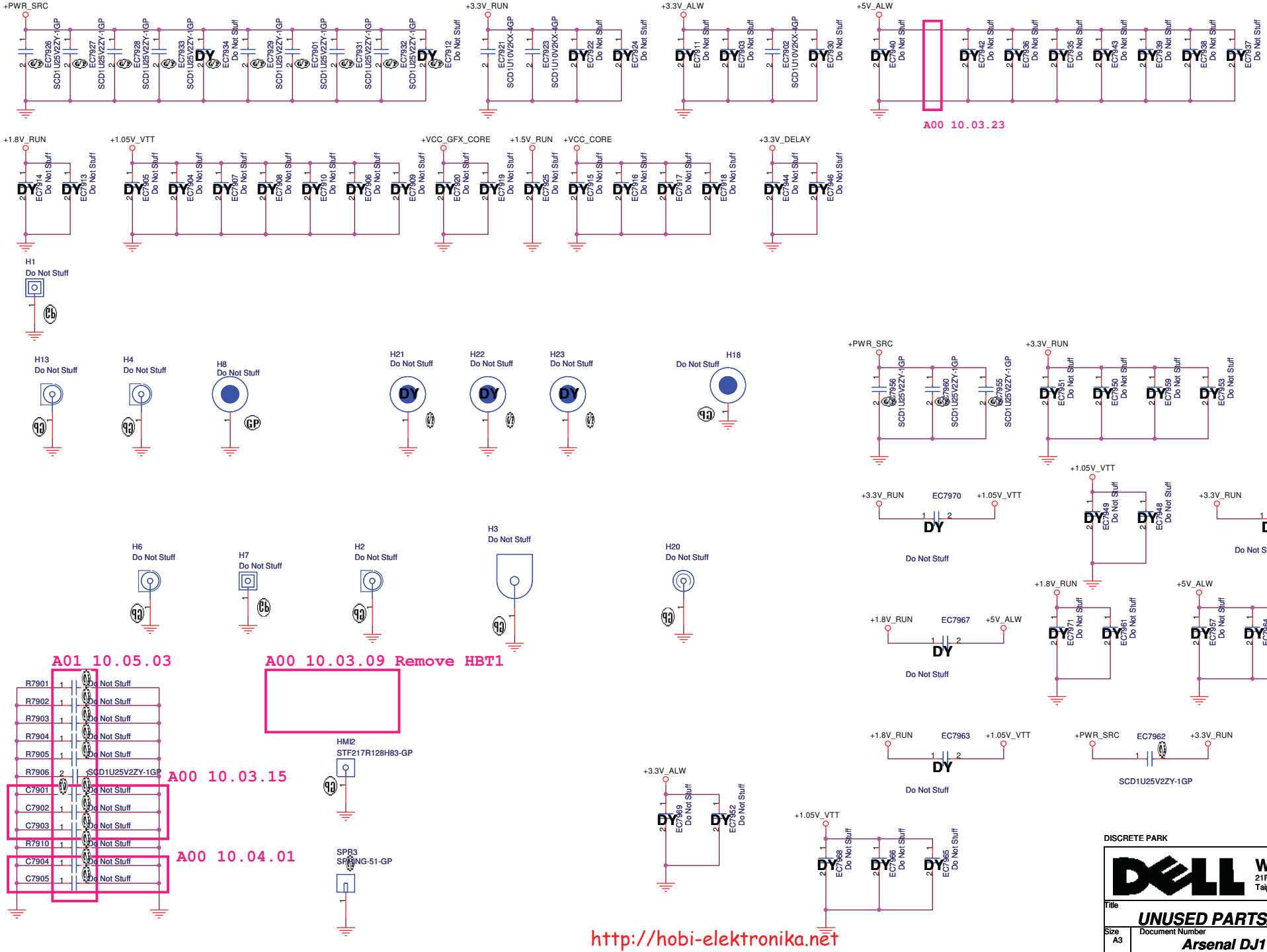

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

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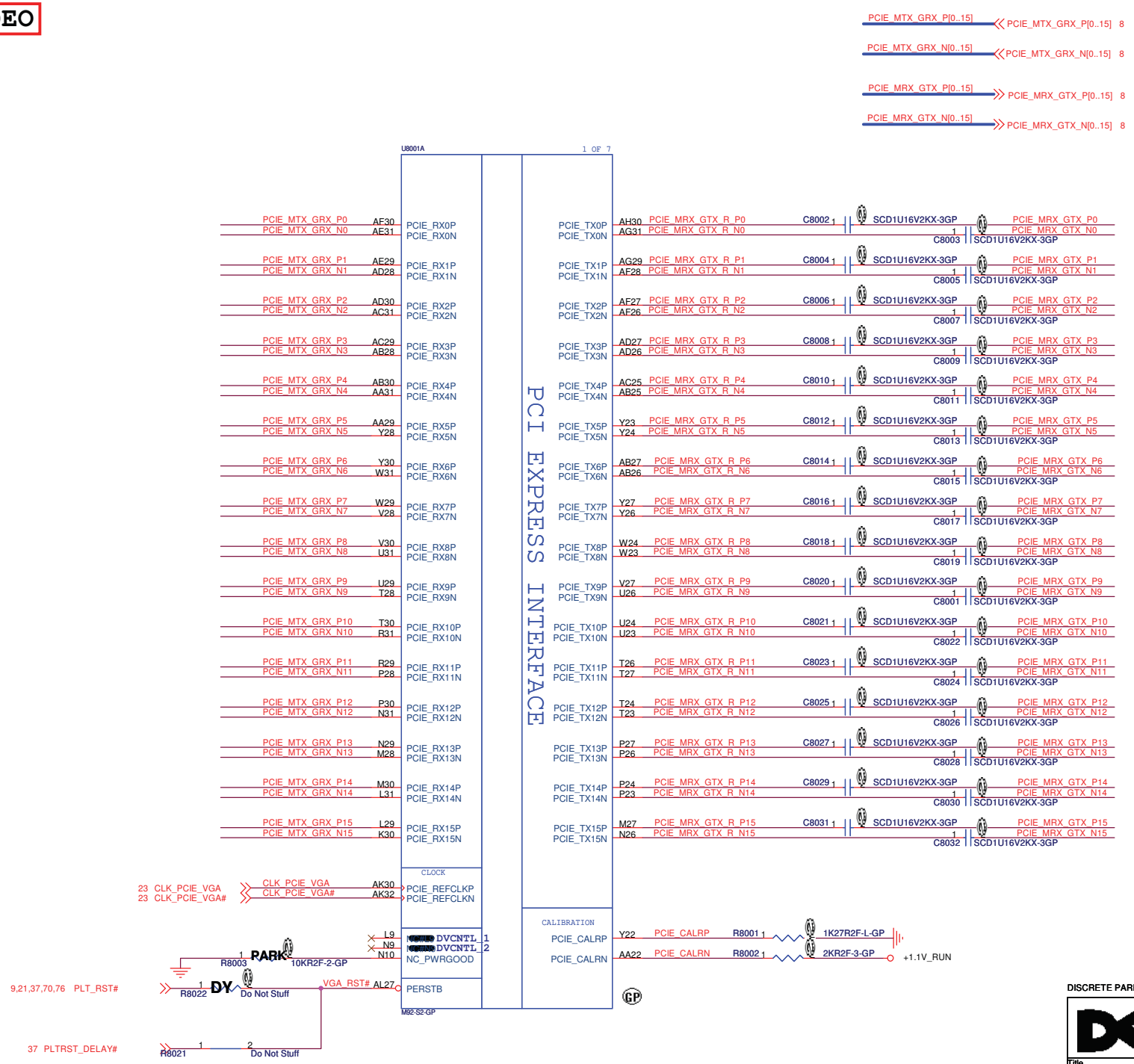
SSID = VIDEO



DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA PCIE(1/4)

Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A01

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SSID = VIDEO

M92/ PARK switch

X01change tolerant 10/01/15

X01 M92/ PARK switch

SIGNALS	Normal mode	Debug mode
JTAG_TESTEN	0	1
JTAG_TRSTB	0	1
JTAG_TCK	NC	1
JTAG_TMS	1	1

DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA LVDS/TV/CRT(2/4)

Size: C | Document Number: Arsenal DJ1 Discrete | Rev: A01

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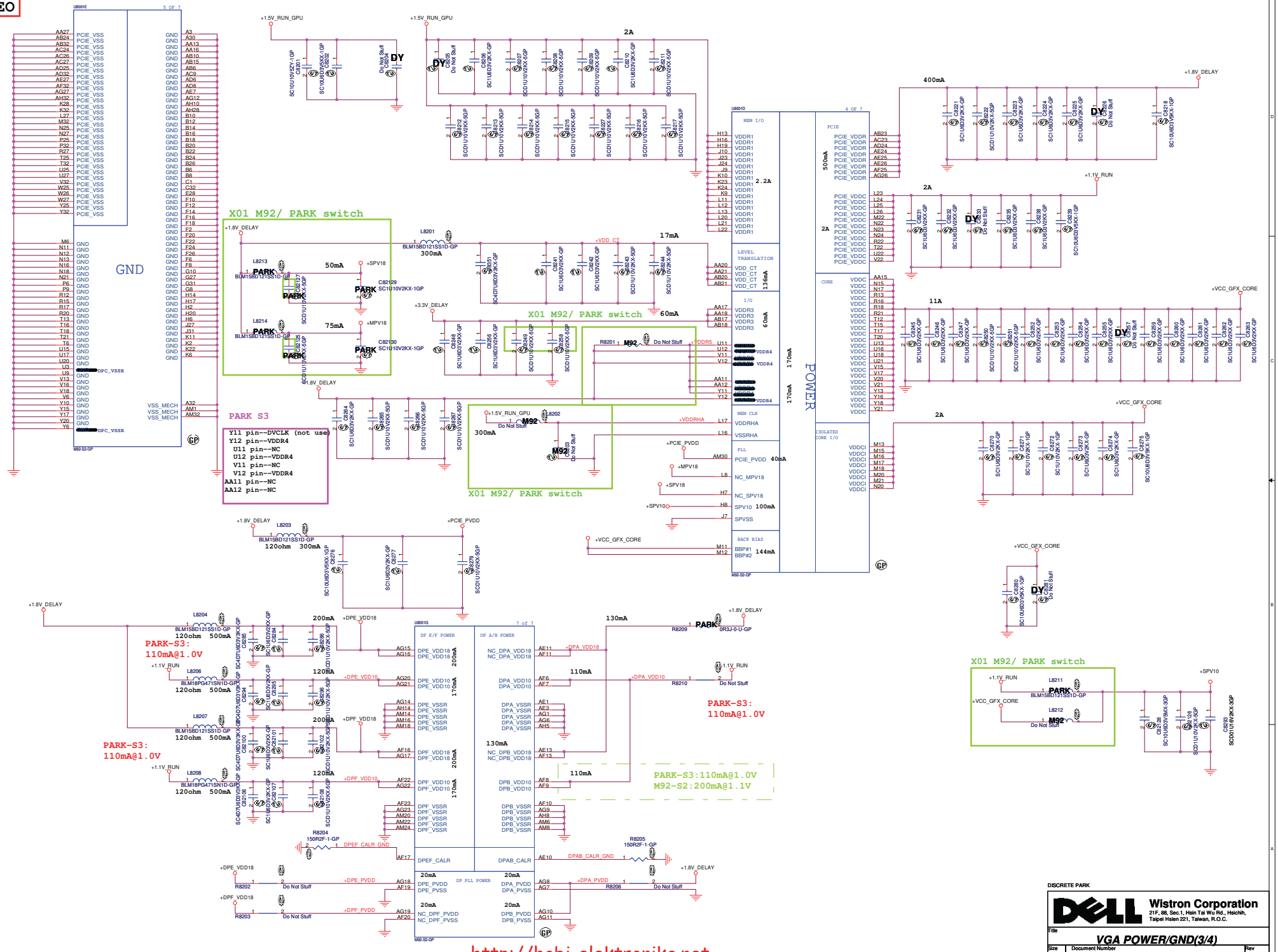
SSID = VIDEO



DISCRETE PARK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA POWER/GND(3/4)

Size: A2 | Document Number: Arsenal DJ1 Discrete | Rev: A01

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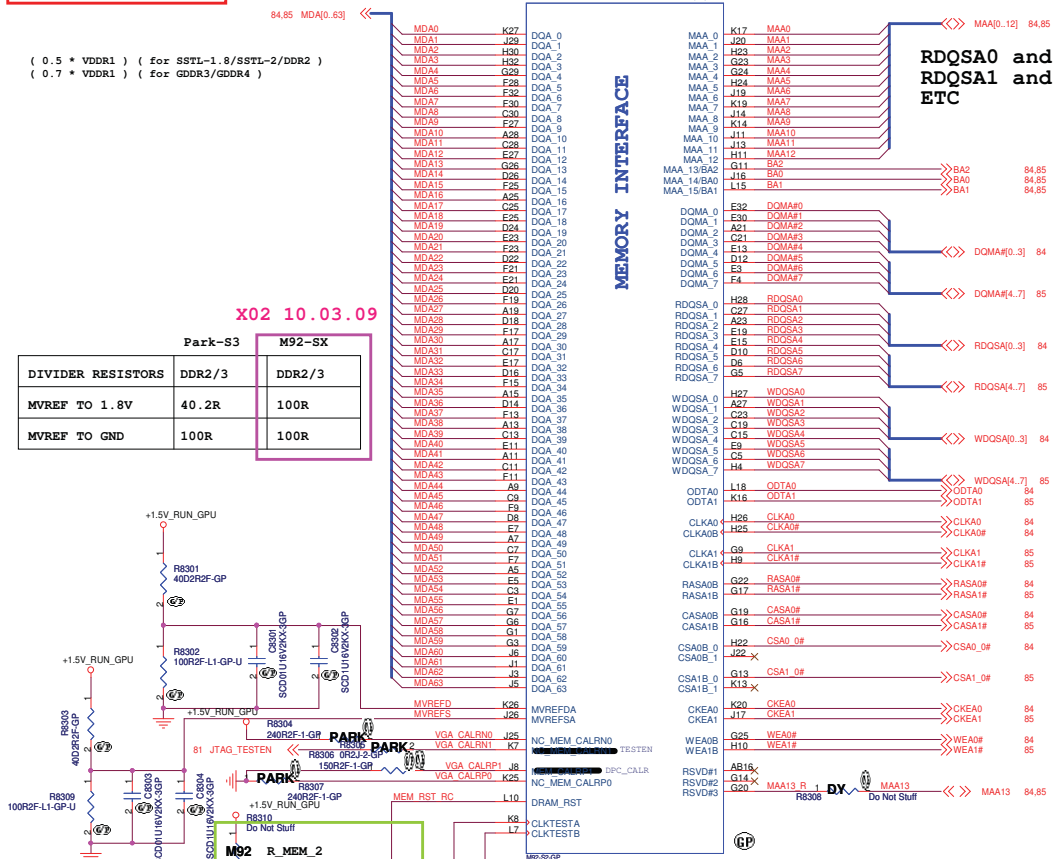
SSID = VIDEO

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

X02 10.03.09

	Park-S3	M92-SX
DIVIDER RESISTORS	DDR2/3	DDR2/3
MVREF TO 1.8V	40.2R	100R
MVREF TO GND	100R	100R



Designator	For M9X-S2	For Park-S3
R_MEM_1	DNI	10K
R_MEM_2	OR/Short	51R
R_MEM_3	2.2K	DNI
C_MEM	2.2nF	68pF

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(2,0) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 00 - gDDR3 64Mx16 Hynix 01 - gDDR3 64Mx16 Samsung V 10 - gDDR3 128Mx16 Hynix 11 - gDDR3 128Mx16 Samsung

DISCRETE PARK

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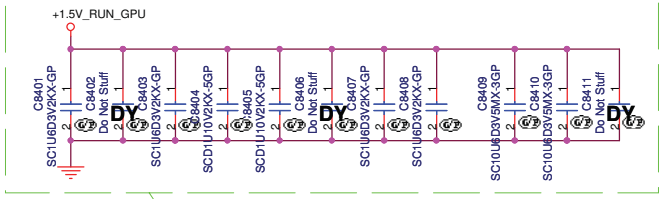
Taipei Hsien 221, Taiwan, R.O.C.

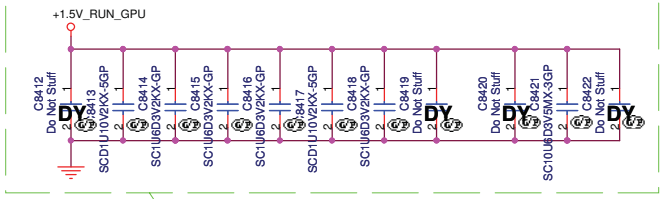
Title: VGA MEMORY/STRAPS(4/4)
Size: C | Document Number: Arsenal DJ1 Discrete | Rev: A01
Date: Thursday, May 06, 2010 | Sheet 83 of 92

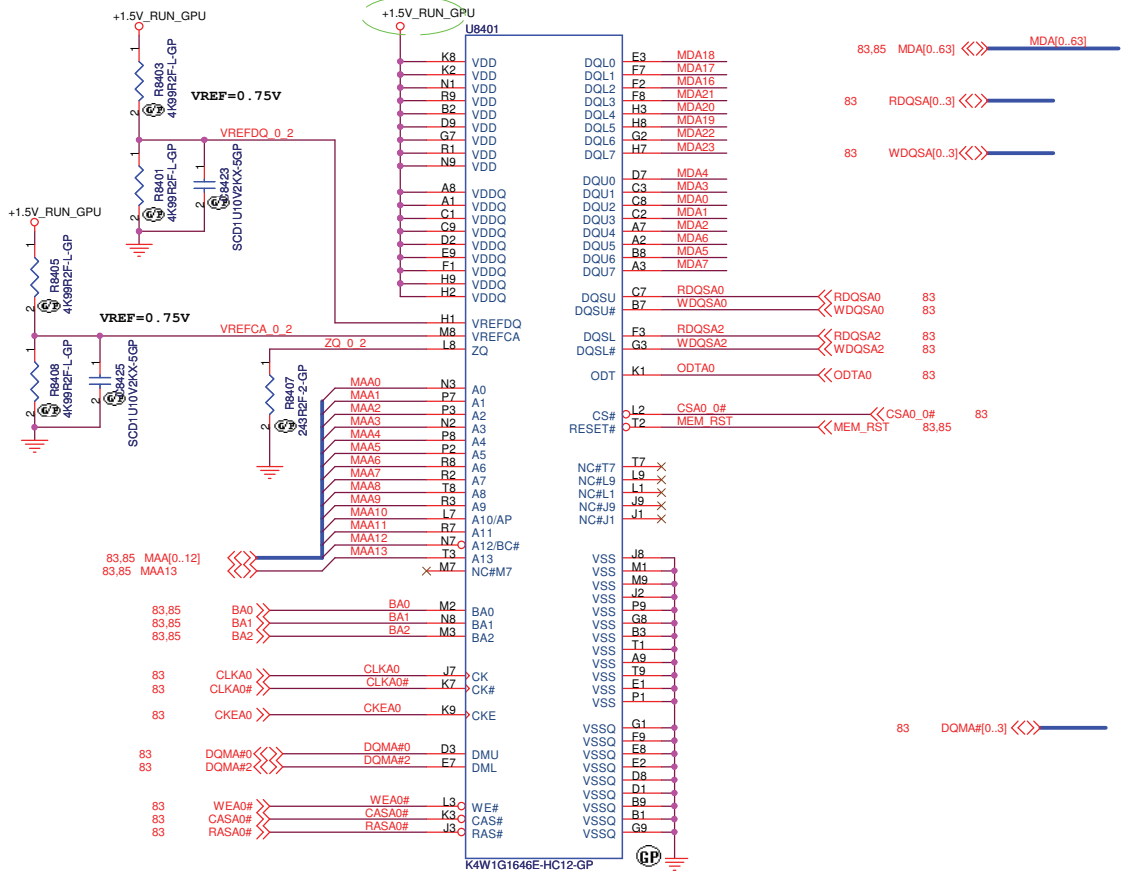
SSID = VIDEO

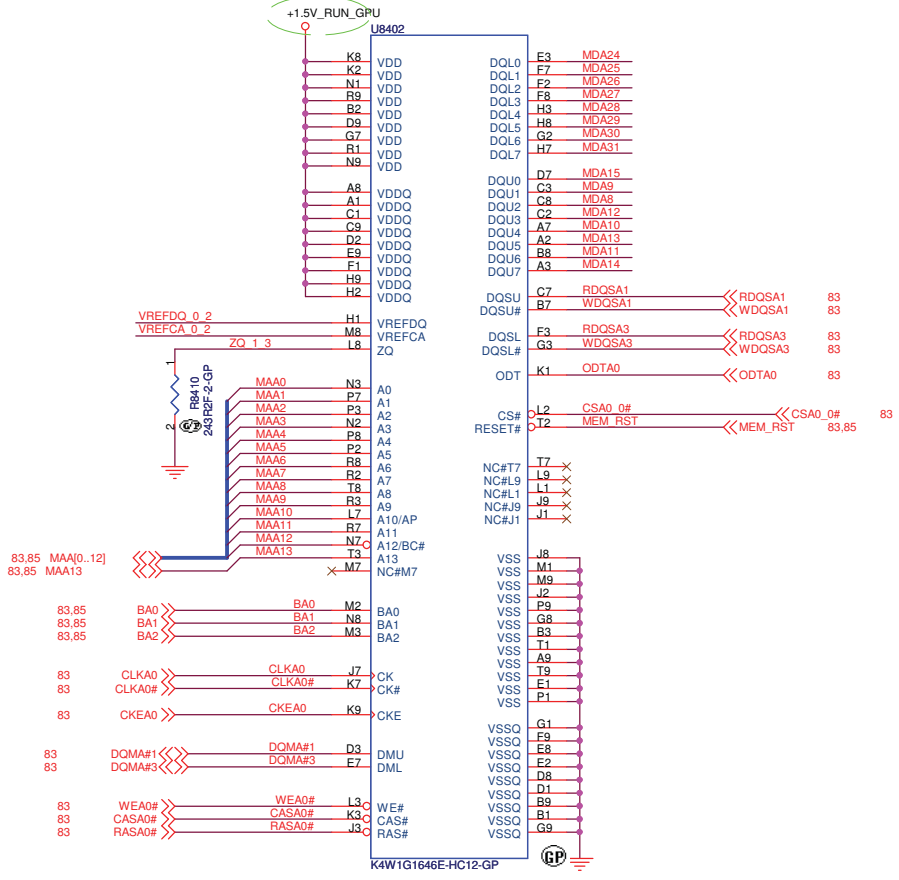
Place blow decouping caps close VDD pin.

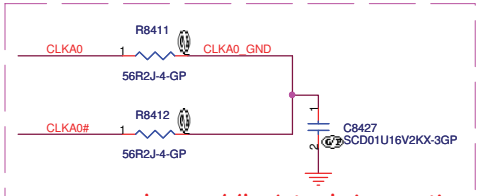


Place blow decouping caps close VDD pin.









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Taipei Hsien 221, Taiwan, R.O.C.

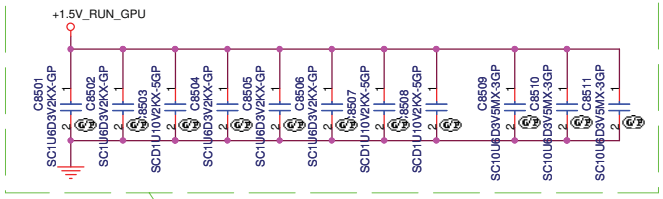
Title: GPU-VRAM (1/2)

Size	Document Number	Rev
Custom	Arsenal DJ1 Discrete	A01

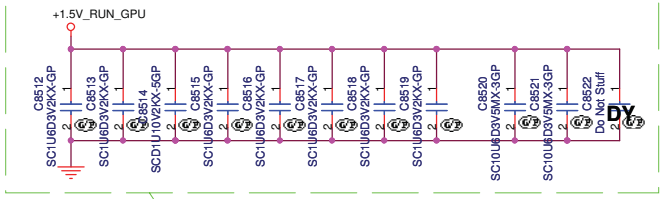
Date: Thursday, May 06, 2010 Sheet 84 of 92

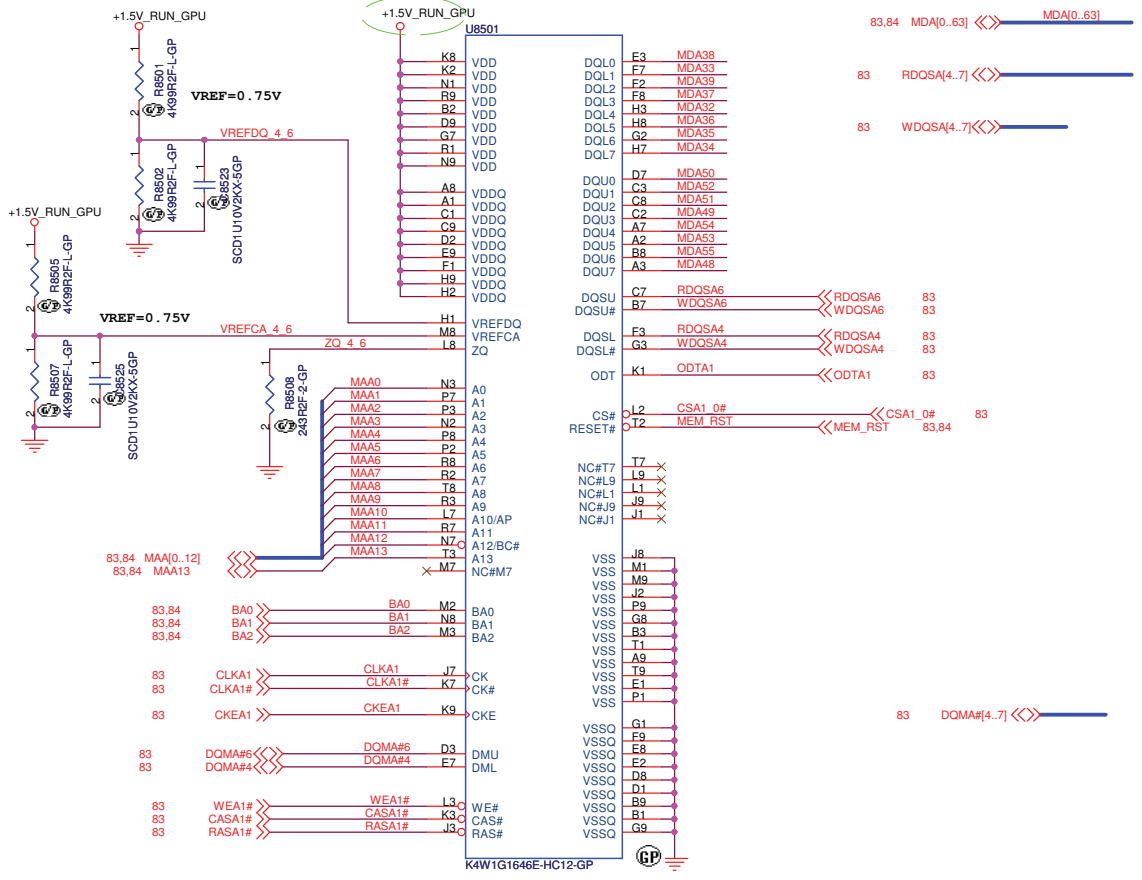
SSID = VIDEO

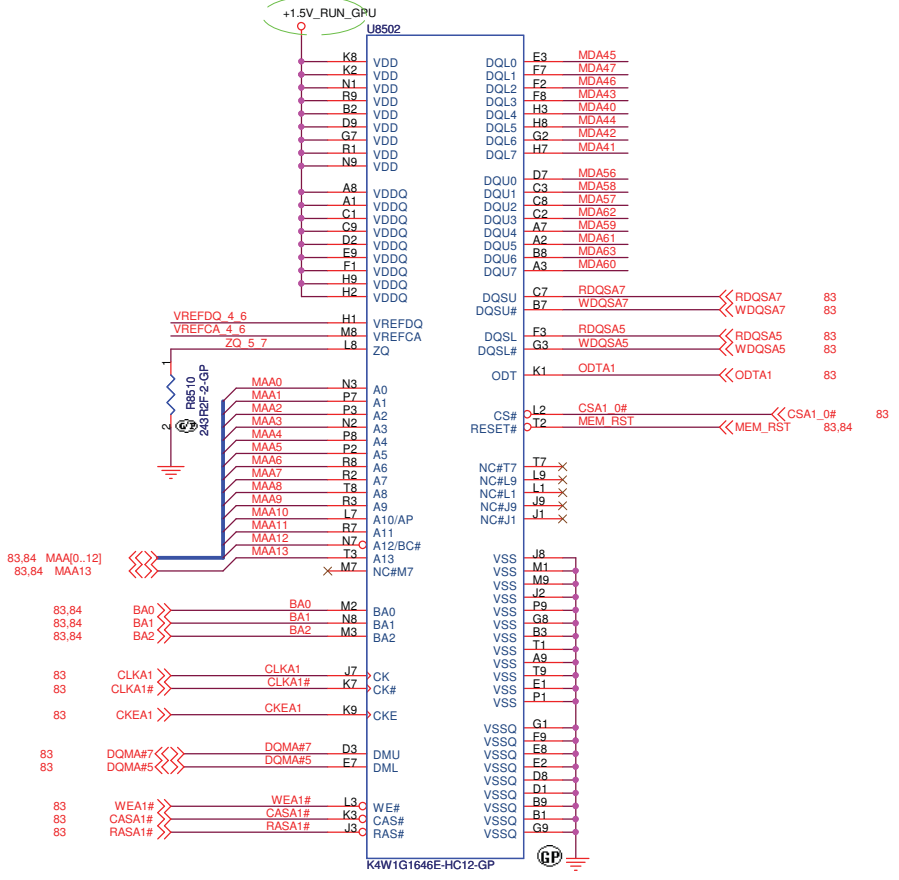
Place blow decouping caps close VDD pin.

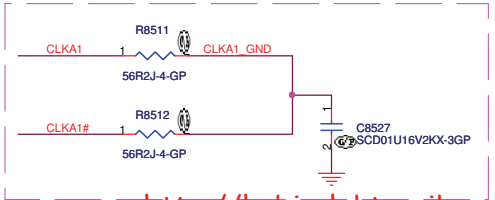


Place blow decouping caps close VDD pin.









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Wistron Corporation
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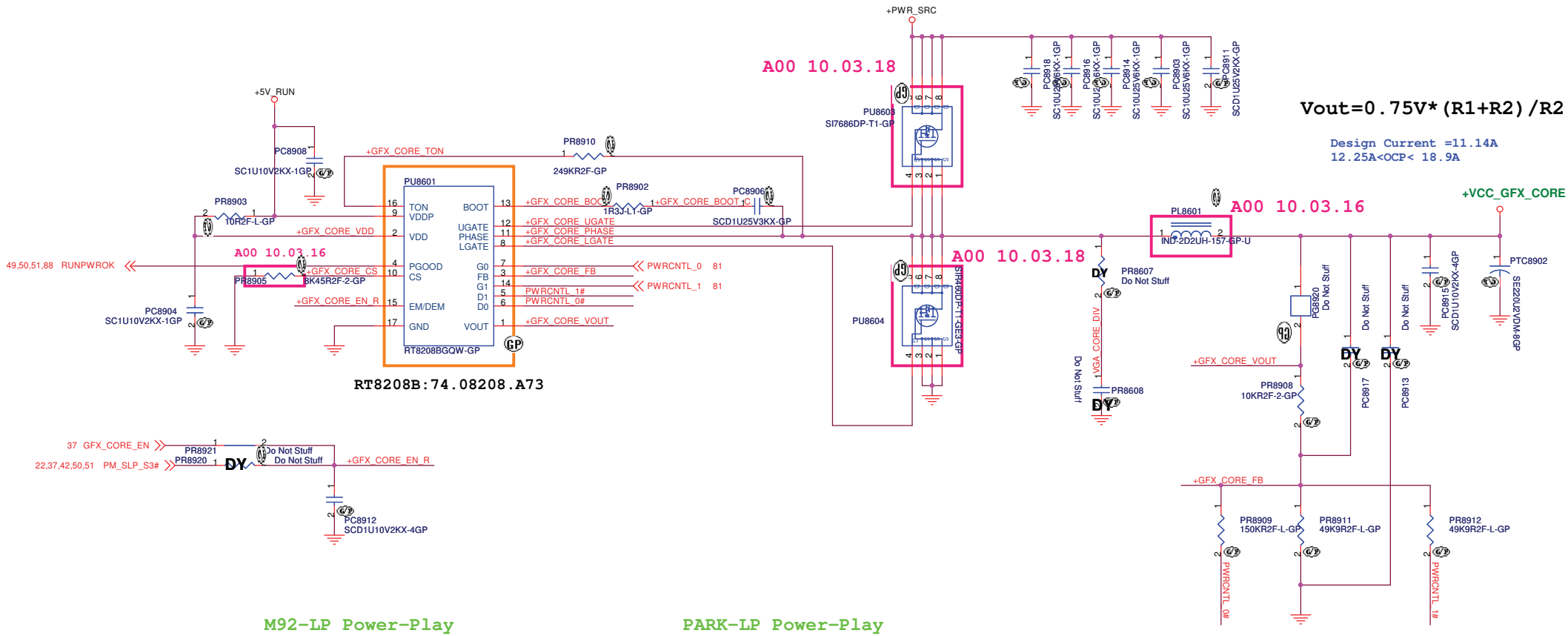
Title: GPU-VRAM (2/2)

Size: Custom | Document Number: Arsenal DJ1 Discrete | Rev: A01

Date: Thursday, May 06, 2010 | Sheet 85 of 92

SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



M92-LP Power-Play

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

PARK-LP Power-Play

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec DCR:18mohm/201mohm Isat=14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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Title: RT8208B_+VGA_CORE
Size: A3
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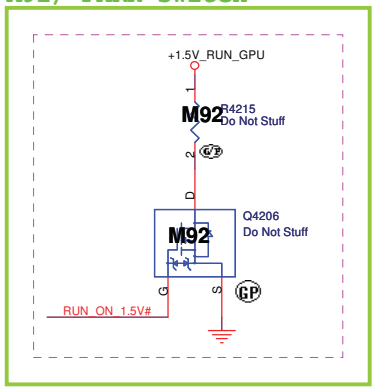
M92/ PARK switch

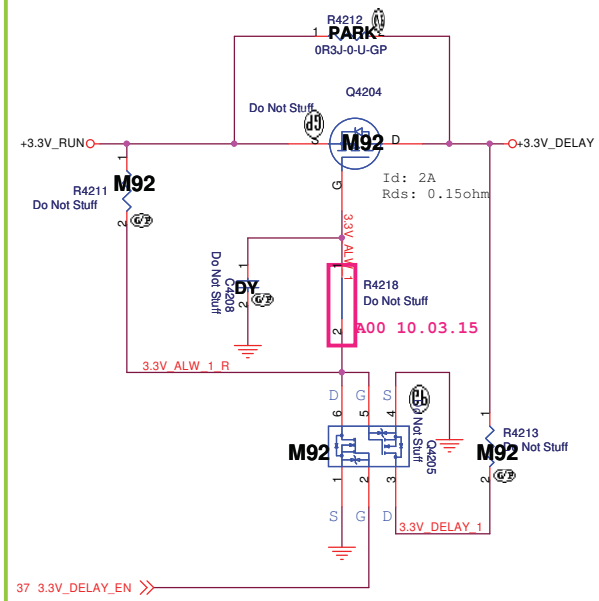


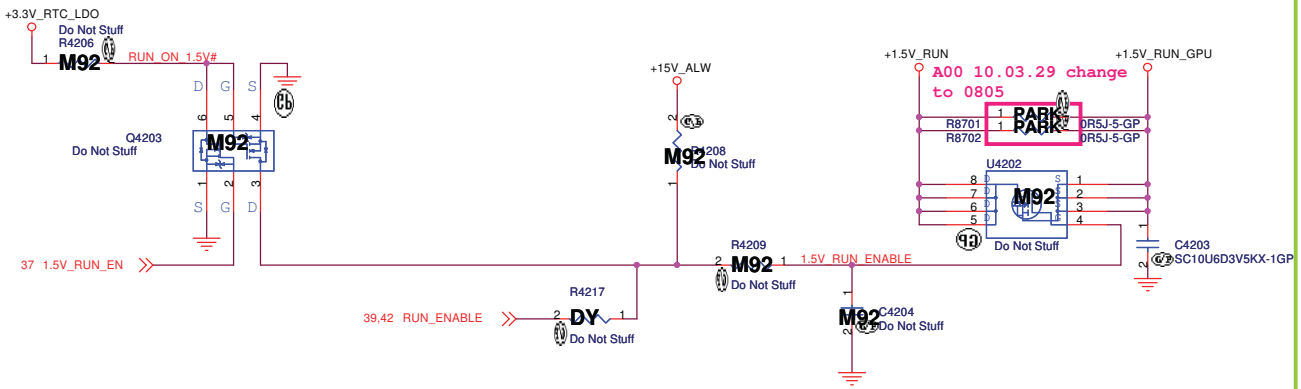
Peak current: 2805mA
Design current: 1963.5mA

M92/ PARK switch

Peak current:3520mA
Design current: 2464mA
11.6A
Rds=14m ohm ==> 0.04928

For Discrete +1.5V_RUN





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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane +1.05V_GFX

Size	Document Number	Rev
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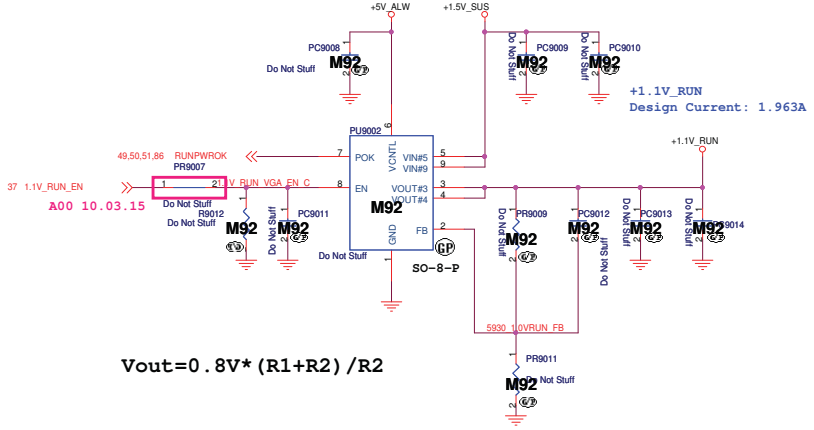
APL5930KAI for +1.1V_RUN



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Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930_+1.1V_RUN	
Size: C	Document Number: Arsenal DJ1 Discrete	Rev: A01
Date: Thursday, May 06, 2010	Sheet 88 of 92	

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	47	2010/01/04	Wistron	CPU core power was two phase	Remove PC4766	
2	81 82 83	2010/01/04	Wistron	M92/ PARK switch	ADD RN8102,R8104,R8105,R8201,L8202,L8212,C8203 R8310,R8311,R8312 Connect Ball L17 to +1.5V_RUN_GPUand Ball L16 to GND	X01 X01
3	81	2010/01/04	ATI	Modify Park to Normal mode	PD R8132 to GND	X01
4	87	2010/01/04	Wistron	Derect connect +1.5V_RUN to +1.5V_RUN_GPU.	Change +1.5V_SUS power rail to +1.5V_RUN ADD R8701,R8702 NOPOP U4202,C4203,C4204,R4209,R4208 Q4203,R4215,Q4206	X01
5	80 81 82 83 84	2010/01/04	Wistron	BOM Control	PARK:POP R8003,RN8102,R8104,R8105,C8134,C8135,C8136 C8128,C8129,C8130,L8108,L8109,C8131,C8132,C8133 L8107,C82127,C82129,C82125,C82130,L8213,L8214 R8209,L8211,R8313,C8306,C8307,R8332,R8333,R8308 ,R8304,R8305,R8307,R4212 M92:POP R82011,C8203,L8202,L8212,R8310,R8311,R8312 R4211,R4213,Q4204,Q4205	X01
6	37 62	2010/01/05	Wistron	Improve BIOS data loss issue.	ADD U3702 circuit POP R6210 NOPOP R6203	X01
7	87 88	2010/01/05	Wistron	M92/Park Co-lay to use 1.1V_RUN LDO.	ADD PU9002 LDO circuit Remove U8703 MOSFET circuit	X01
8	59	2010/01/06	Wistron	Suyin ODD connect PT build SMT issue	Change to 22.10300.811	X01
9	7 46 60 79 86	2010/01/06	Wistron	EMI requirement	Pop EC7932,EC7960,EC7933,EC7928,EC7931,EC7929,EC7901 ,EC7926,PC8911,PC4610,EC7927,EC7962,EC7955,PC4616, EC7956,EC7923,EC7921,EC7902,PC4619,EC6001,EC6002, EC6003,EC6004,EC703	X01
10	62	2010/01/07	Wistron	Change RTC battery connect drawing from Coxoc to Foxconn by SMT issue	Change to 62.70001.011	X01
11	24	2010/01/07	Wistron	Schematic could not PD this pin	Packege ball name:AY3 NC	X01
12	39	2010/02/24	Wistron	T8 shutdown is set 88 deg-C.	Change R3915 to 64.28015.6DL	A00
13	37	2010/02/24	Wistron	Change MB VERSION ID and GPU table	POP R3723,R3722 NOPOP R3725 Remove R3724,R3727	A00
14	37	2010/02/24	Wistron	Power bottom delay issue	NOPOP Reset IC U3702	A00

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Title: Change History

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev
15	32 54	2010/03/09	Wistron	EMI requirement	ADD TR3201,TR5401	A00
16	79	2010/03/09	Wistron	ME requirement	Remove HBT1	A00
17	09	2010/03/09	Wistron	S3 Power Reduction requirement	POP U927,R2114,R977 NOPOP R978	A00
18	09	2010/03/09	Wistron	DDR3_DRAMRST# drop issue	ADD C903	A00
19	79	2010/03/09	Wistron	Change page83 DIVIDER RESISTORS table		A00
20	37	2010/03/15	Wistron	Support RCID function schematic when pop Q3706	ADD Q3706	A00
21	46	2010/03/15	Wistron	Operation Mode Select to Diode Emulation Mode	POP PR4619 NOPOP PR4618	A00
22	79	2010/03/15 2010/05/03	Wistron	EMI requirement	Reserve Pad C7901,C7902,C7903	A00
23	54	2010/03/15	Wistron	LCD VDD power	ADD C5412 ,change C5410 from 0.1uf to 1uf	A00
24	46 47 50 88	2010/03/16	Wistron	Change 0 ohm to short pad	R2114,R4218,PR4620,PR4616,PR4619,PR4706, PR4708, PR4713, PR4718, PR4722,PR4732, PR4738, PR4744, PR4755, PR4764, PR4704,PR4703, PR4707, PR4711, PR4784,PR4790, PR4784,PR4776,PR5002,PR9007,R3751	A00
25	47 49 50 89	2010/03/16	Wistron	change to 2.7Kohm for CPU_CORE load/line setting change to 1.4Kohm for CPU_CORE OCP setting. change to 1ohm for boost resister. change to 73.2Kohm for 1.05V OCP setting. change to 8.2Kohm for 1.5V OCP setting. change to 8.45Kohm for VGA_CORE OCP setting.	PR4705 change to 2.7Kohm PR4727 change to 1.4Kohm PR4901 change to 1ohm PR4902 change to 73.2Kohm PR5007 change to 8.2Kohm . PR8905 change to 8.45Kohm	A00
26	46 48 49 50 86	2010/03/16	Wistron	Power requirement	Change PL4814,PL4817 from 68.R3610.10M to 68.R3610.10T Change PL4602 from 68.2R21B.10A to 68.2R210.20Q Change PL8601 from 68.2R210.20B to 68.2R210.20Q Change PL4601 from 68.3R31A.10W to 68.3R310.20I Change PTC4602 from 77.23371.12L to 77.C2271.00L Change from 68.R5610.10D to 68.R5610.20I Change PL5001 from 68.1R510.10J to 68.1R510.20I	A00
27	63	2010/03/17	Wistron	USB Enable pin signal issue remove UPI vendor	Change U6302,U6301 to GMT symbo	A00
28	42	2010/03/17	Wistron	Change symbo from VISHAY to AOL	Modify U4204	A00
29	48 49 50	2010/03/18	Wistron	Power requirement	Change PQ4840 PQ4833 PU4902 PU5003 from 84.07686.A37 to 84.07686.037	A00
30	12 18 19	2010/03/24	Wistron	PSE issue,Layout routing	Remove C1219,C1211,C1803,C1804, C1809,C1905,C1911,C1912	A00
31	09	2010/03/25	Wistron	XDP1 change to ZZ.00PAD.Q81		

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Title: Change History

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: A01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
32	79	2010/05/03	Wistron	EMI requirement	POP C7901,C7902,C7903,C7904,C7905,R7901,R7902,R7903, R7904,R7905,R7906,R7910	A01

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Title: Change History

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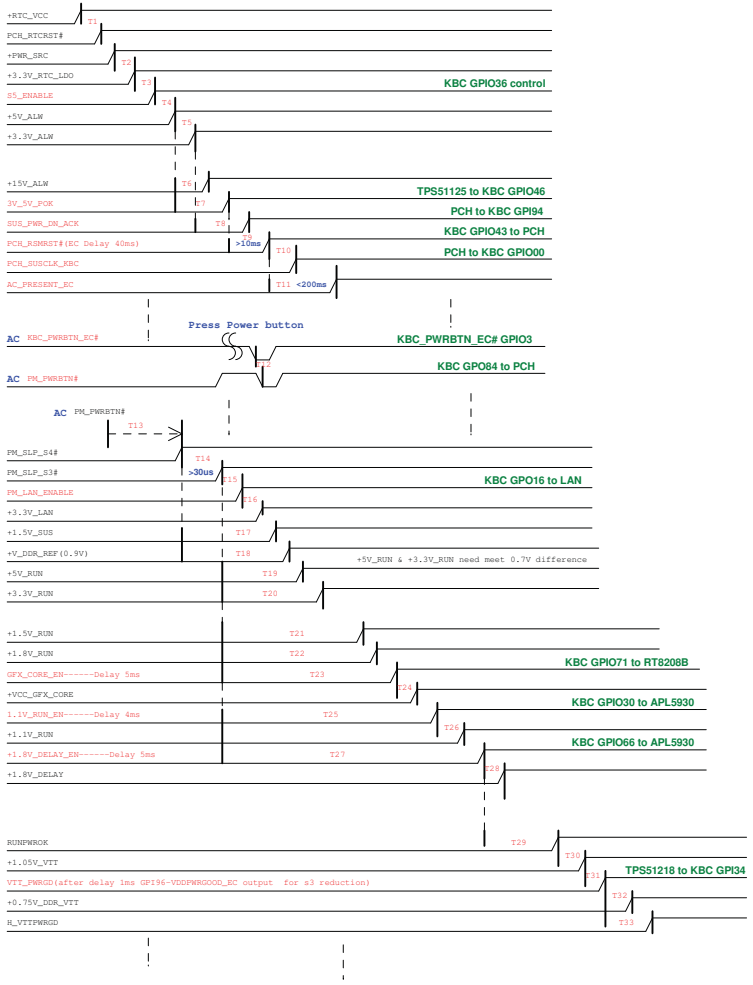
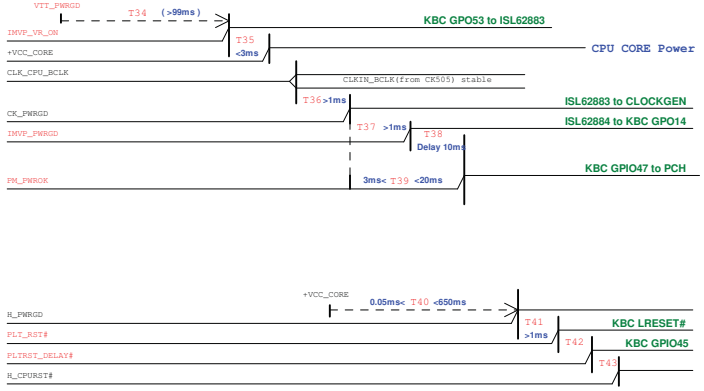
DJ1 Calpella Discrete-Power Up Sequence

(AC mode)

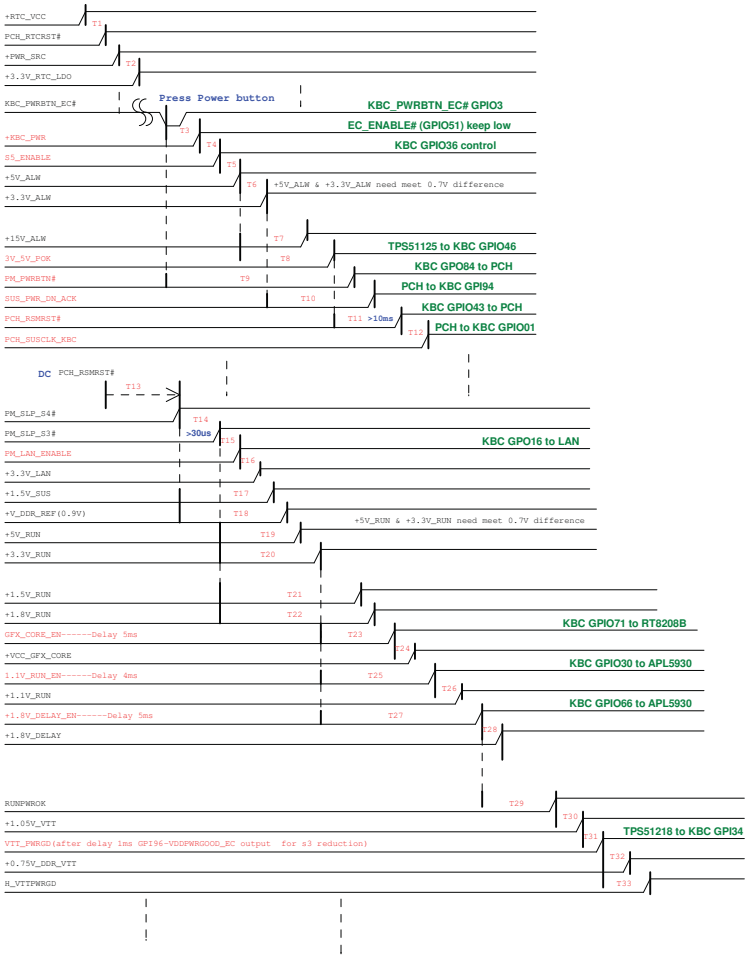
red word: KBC GPIO

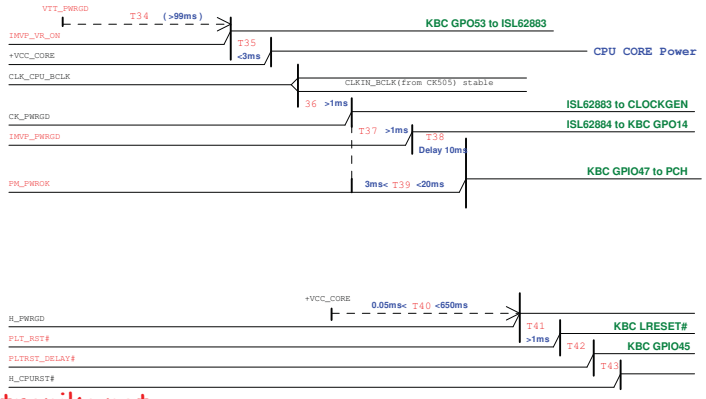




(DC mode)

red word: KBC GPIO





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Title: Power Sequence

Size	Document Number	Rev
A1	DJ1 Calpella Discrete	A01

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