

Essentials Oak 14 Schematic

Chief River

2012-09-05

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

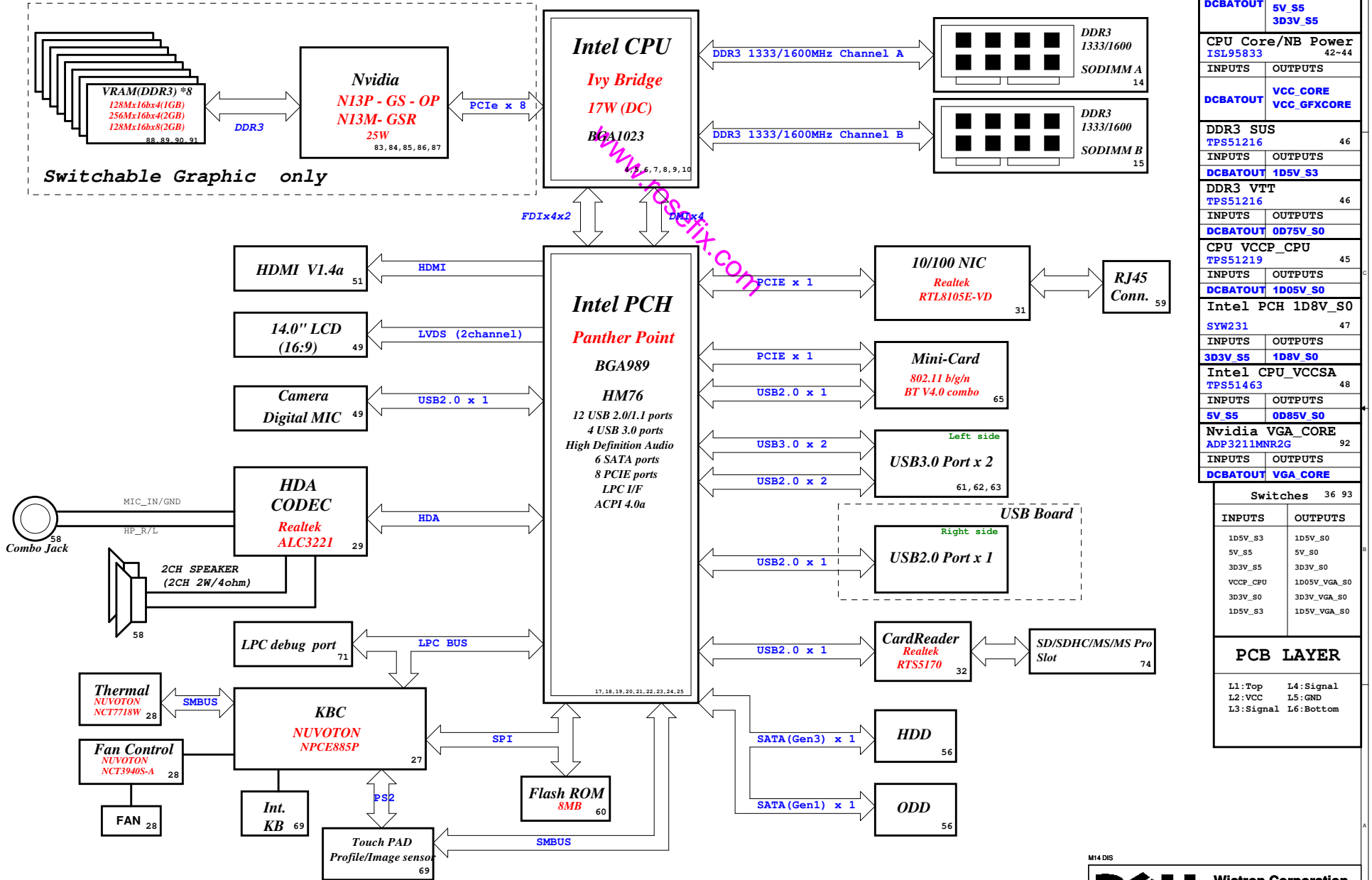
M14 DIS



Title		
Cover Page		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date:	Wednesday, September 05, 2012	Sheet 1 of 105

Project code: 91.4WT01.001
 91.4XP01.001
 PCB P/N : 12204
 Revision: A00

Oak14 Block Diagram



CHARGER		40
BQ24727		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		41
TPS51225		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core/NB Power		42-44
ISL95833		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE VCC_GFXCORE	
DDR3 SUS		46
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3	
DDR3 VTT		46
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	0D75V_S0	
CPU VCCP_CPU		45
TPS51219		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
Intel PCH 1D8V_S0		
SYW231		47
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S0	
Intel CPU VCCSA		48
TPS51463		
INPUTS	OUTPUTS	
5V_S5	0D85V_S0	
Nvidia VGA_CORE		92
ADP3211MNR2G		
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	
Switches		36 93
INPUTS	OUTPUTS	
1D5V_S3	1D5V_S0	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
VCCP_CPU	1D05V_VGA_S0	
3D3V_S0	3D3V_VGA_S0	
1D5V_S3	1D5V_VGA_S0	
PCB LAYER		
L1:Top	L4:Signal	
L2:VCC	L5:GND	
L3:Signal	L6:Bottom	

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kohms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kohms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kohms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kohms ±5% pull-up resistor to PCH_VccDFTERM.
SATA1GP/ GPIO19	Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Panther Point require SPI flash connected directly to the Panther Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of PWROK will halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug. This signal has a 20k internal pull down resistor.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform. Note: HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase. Refer to the example circuits provided in the latest Chief River platform design guide.
GPIO15	Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality.
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected. When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7k resistor to ensure proper strap setting when used as the chipset test interface. Refer to the latest platform debug design guide and platform design guide for more details. NOTE: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft strap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping Chief River Schematic Checklist Revision 1.5

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kohms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	1
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort 0: Enabled - An external Display Port device is connected to the Embedded Display Port pull-down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	PCIe Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

Sandy Bridge + Ivy Bridge Compatibility Requirements Chief River Schematic Checklist Revision 1.5

Pin Name	Configuration	Schematic Notes
DDR3 VREF	Sandy Bridge + Ivy Bridge Ivy Bridge	DDR3 VREF M1 and M3 Guidelines are required. Note: The M3 traces are routed to the Sandy Bridge Processor reserved pins. No change.
PROC_SELECT# & DF_TVS	Sandy Bridge + Ivy Bridge Ivy Bridge	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1k±5% series resistor. PROC_SELECT# also needs a 2.2k±5% pull up resistor to PCH VccDFTERM rail. No change.
VCCIO VR Implementation	Sandy Bridge + Ivy Bridge Ivy Bridge	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a requirement for a separate VCCIO VR for Sandy Bridge + Ivy Bridge compatibility. No change.
VCCSA_SEL connection to VCCSA_VID[1:0] lines	Sandy Bridge + Ivy Bridge Ivy Bridge	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller. No change.
Layout Requirement on PCI Express Gen3	Sandy Bridge + Ivy Bridge Ivy Bridge	The total motherboard length for a pair of consecutive PCI Express Tx lanes be length matched within 100 mils (2.54 mm) No change.
GT Core VR Implementation	Sandy Bridge + Ivy Bridge Ivy Bridge	Depending on the PDDG specifications, some IVB GT2 SKUs may require a new VR controller and 2 phase VCC GT core VR. No change.
Processor PCI Express Graphics Guidelines	Sandy Bridge + Ivy Bridge (PCIe Gen3): Ivy Bridge	To support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 180 - 265 nF. No change.

Power Plane

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
IV_S0 IVS0_S0 IVS0_S1 IVS0_S2 IVS0_VTT IVS0_VS0 IVS0_VS1 IVS0_VS2 IVS0_VS3 IVS0_VS4 IVS0_VS5 IVS0_VS6 IVS0_VS7 IVS0_VS8 IVS0_VS9 IVS0_VS10 IVS0_VS11 IVS0_VS12 IVS0_VS13 IVS0_VS14 IVS0_VS15	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.75V 0.33V to 1.35V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
IV_USBK_S3 IVS3_S3 IVS3_PREF_S3	5V 1.5V 0.75V	S3	
IV_CSBADOUT IVS5_S5 IVS5_AUX_S5 IVS5_S5 IVS5_AUX_S5	6V-14.1V 6V-14.1V 5V 3.3V 3.3V	All S states	AC Brick Mode only
IVS17_LAN_S5	3.3V	WOL_EN	Legacy WOL
IVS0_AUX_S0C	3.3V	DSW_Sx	ON for supporting Deep Sleep states
IVS0_AUX_S5	3.3V	G1_Sx	Powered by Li Coin Cell in G1 and +V3ALM in Sx

PCIe Routing

LANE1	X
LANE2	X
LANE3	Mini Card1 (WLAN)
LANE4	x
LANE5	X
LANE6	Onboard LAN
LANE7	X
LANE8	X


USB Table

Pair	Device
0	USB3.0 port1
1	USB3.0 port2, with Debug Port
2	USB2.0 port3
3	X
4	X
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	X
9	X
10	CARD READER
11	Mini Card (WLAN)
12	X
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

M14 DS



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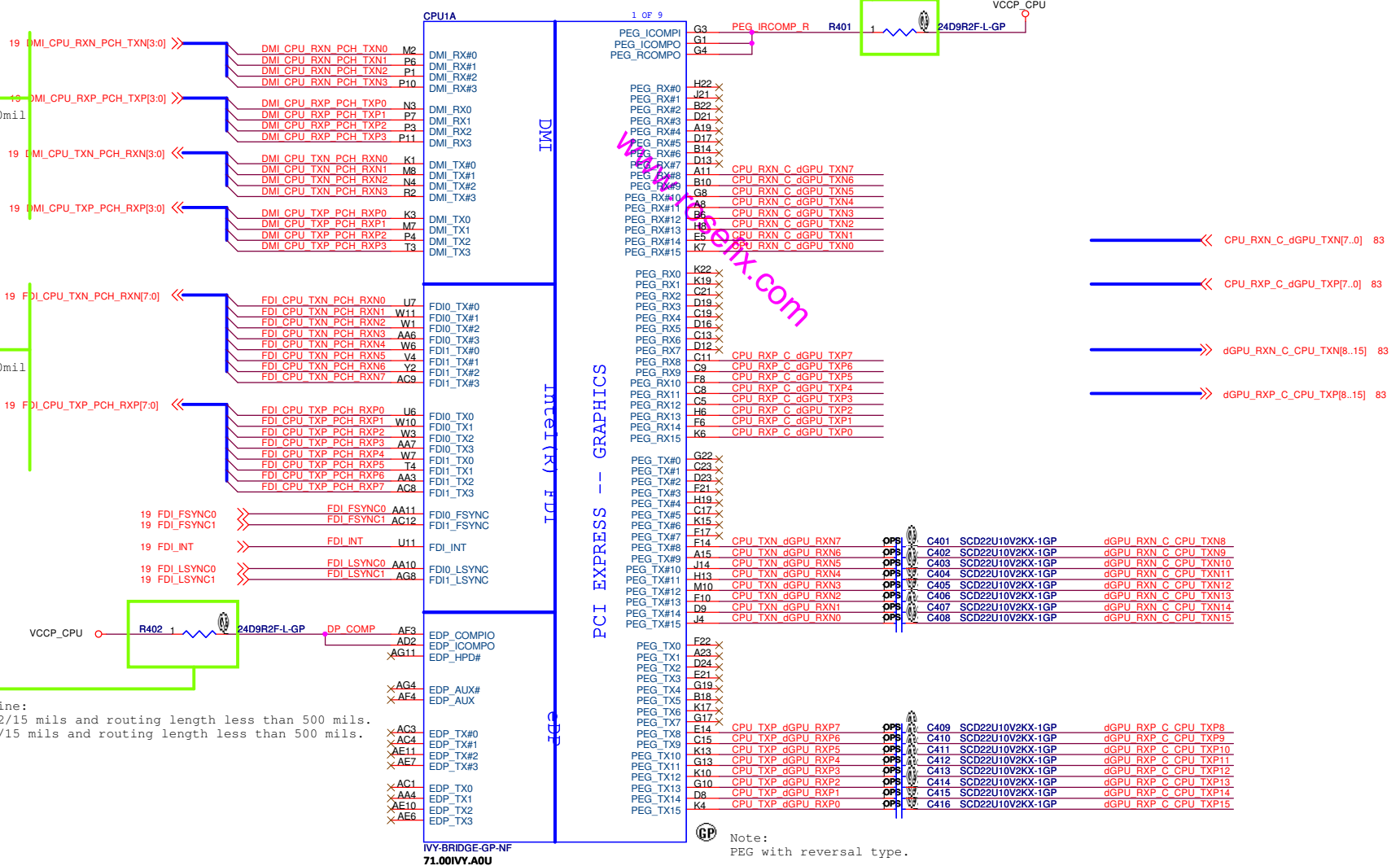
SSID = CPU

Layout Note:
DMI trace length 2000-8000mil

Layout Note:
FDI trace length 2000-6500mil

Layout Note:
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
PEG with reversal type.

M14 DIS

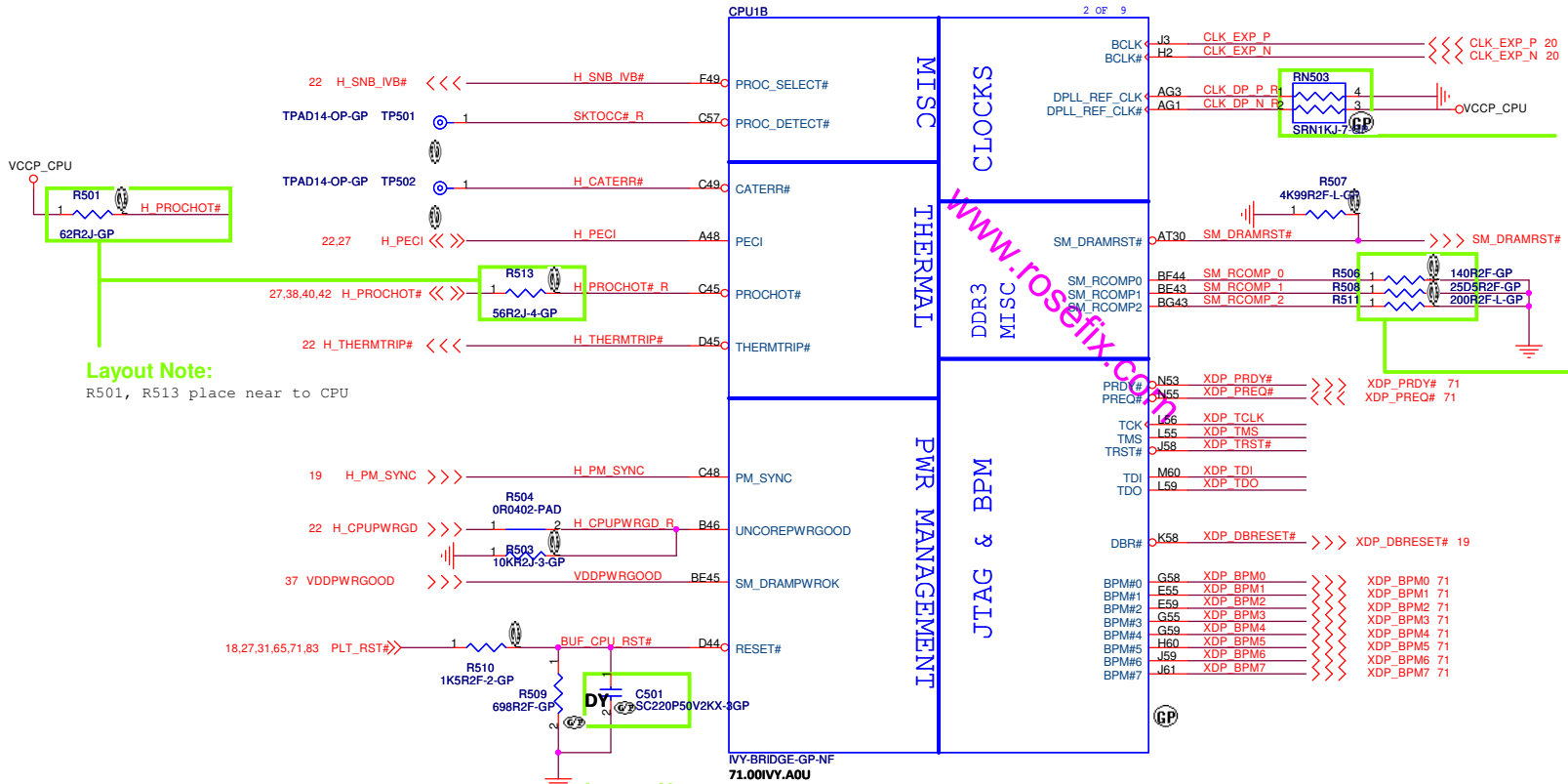
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(PCIE/DMI/FDI)**

Size: AS Document Number: **OAK14 Chief River DIS** Rev: **A00**

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SSID = CPU

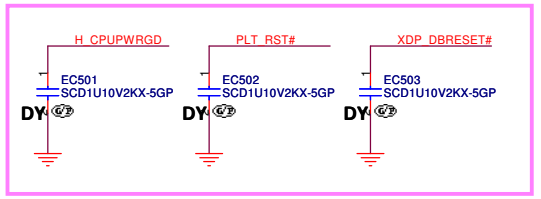
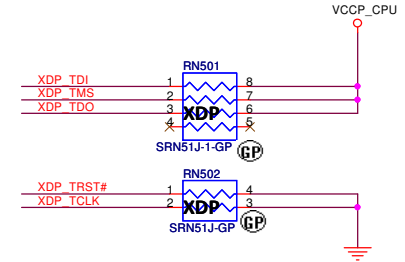


Layout Note: Checking the connector pin's LAYOUT

Layout Note: R501, R513 place near to CPU

Layout Note: Signal Routing Guideline: SM_RCOMP keep routing length less than 500 mils. Trace width = 15mil

Layout Note: C501 place near to CPU



reserve for EMI Request

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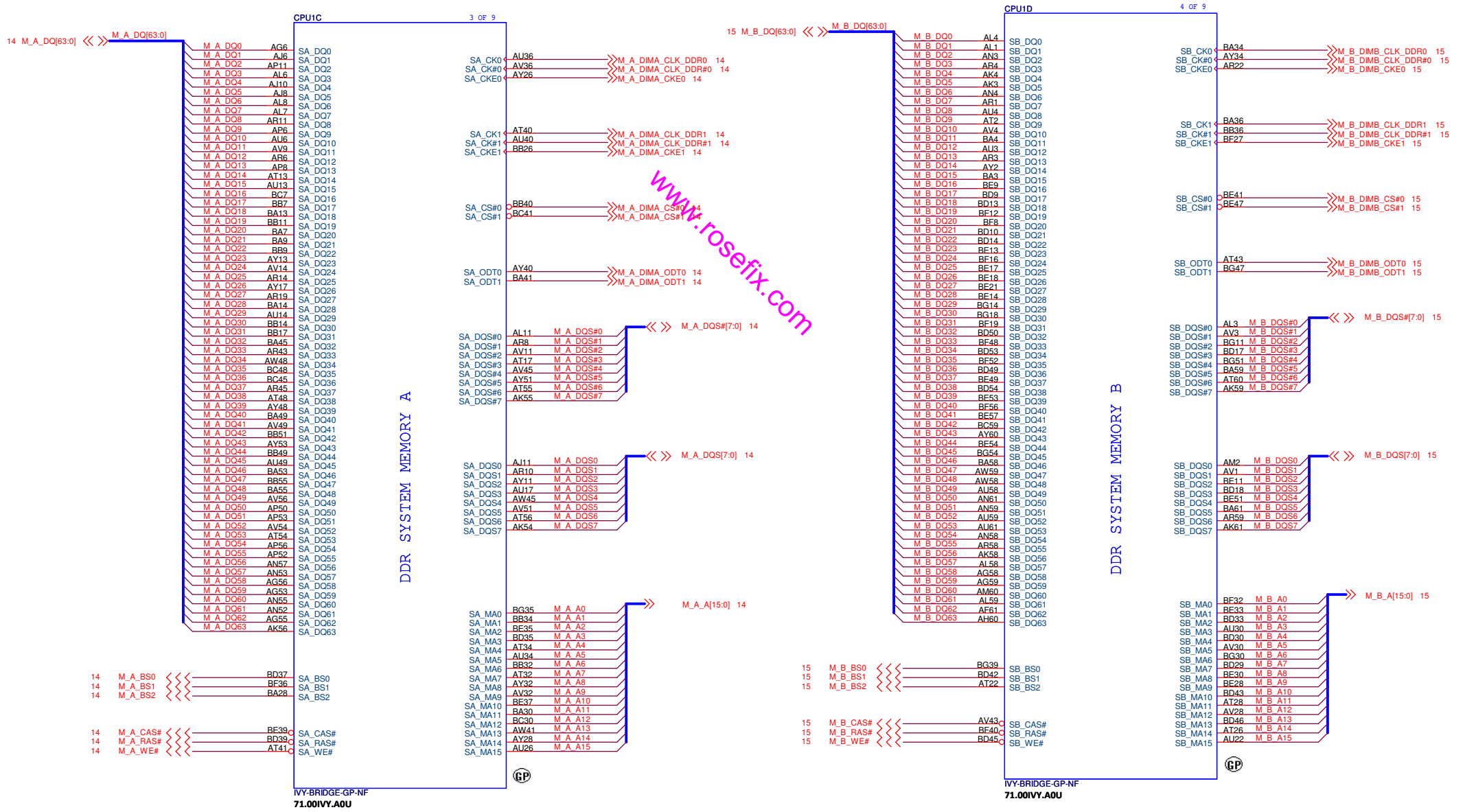
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Title: **CPU(THERMAL/CLOCK/PM)**

Size: A3 Document Number: **OAK14 Chief River DIS** Rev: **A00**

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SSID = CPU



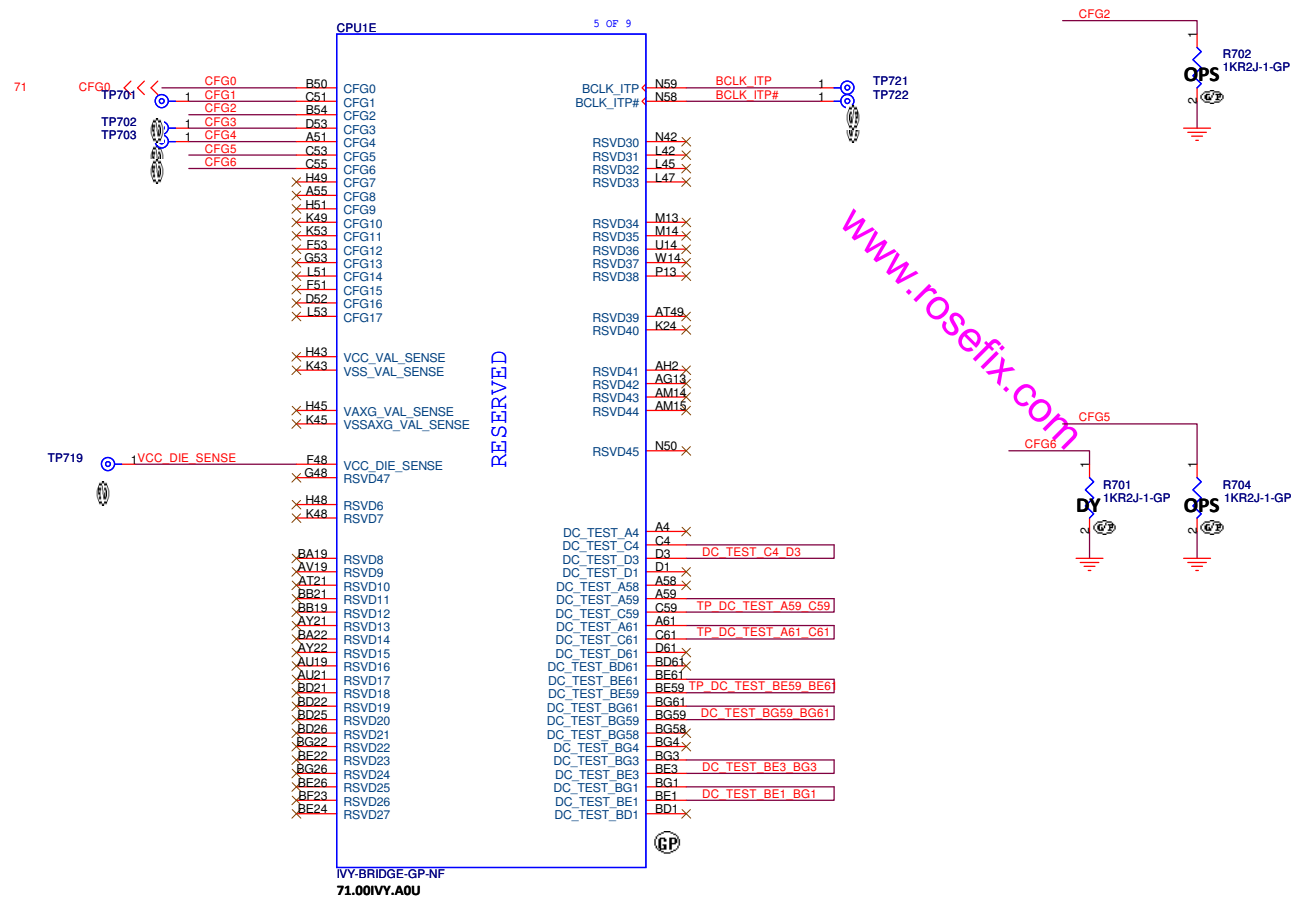
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Title: **CPU (DDR)**

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SSID = CPU



PEG Static Lane Reversal

CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
--------	--

Display Port Presence Strap

CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
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PCIe Port Bifurcation Straps

CFG[6:5]	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express
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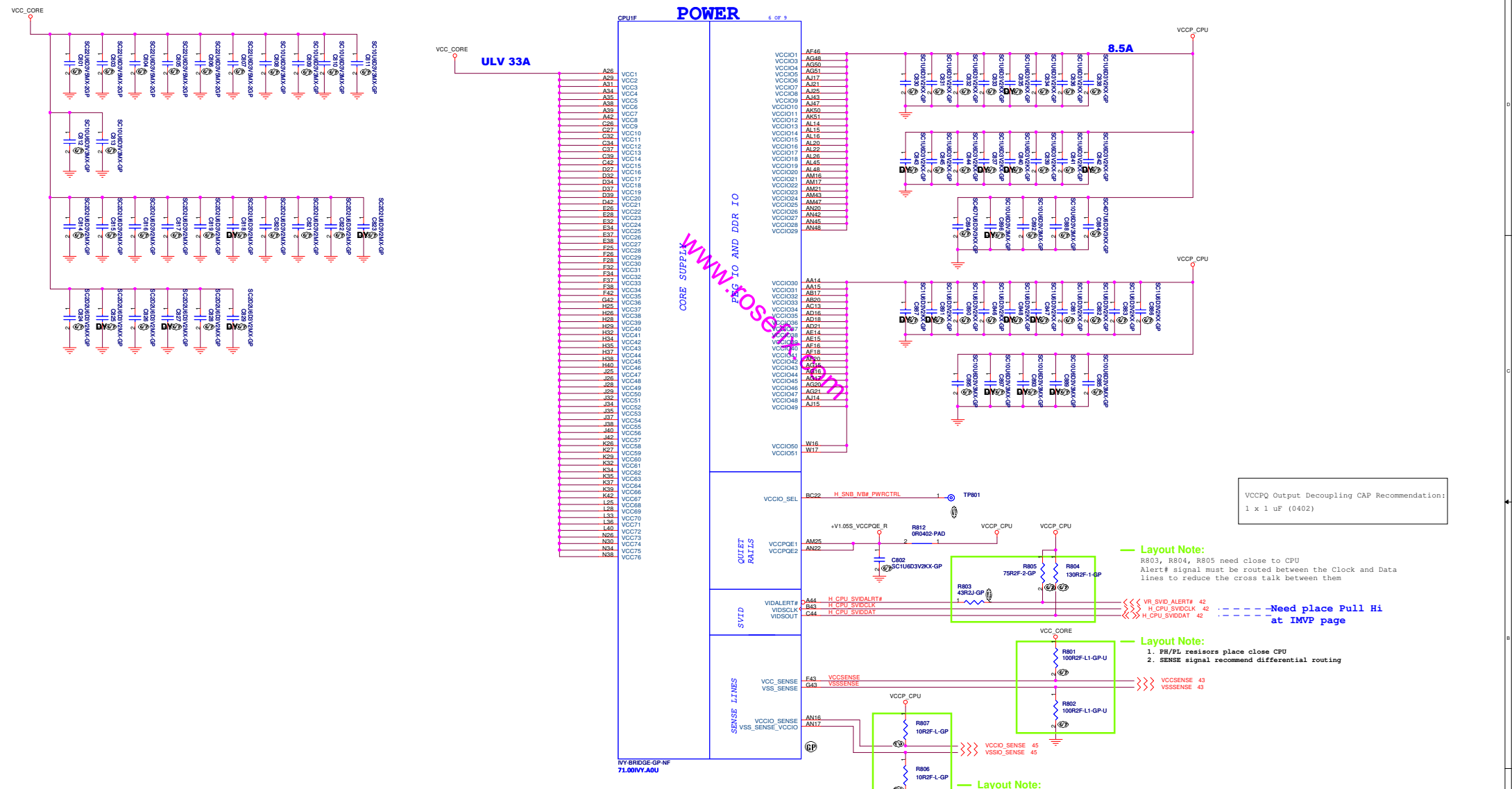
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Title: **CPU (RESERVED)**

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VCCPO Output Decoupling CAP Recommendation:
1 x 1 uF (0402)

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

--- Need place Pull Hi at IMVP page

Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

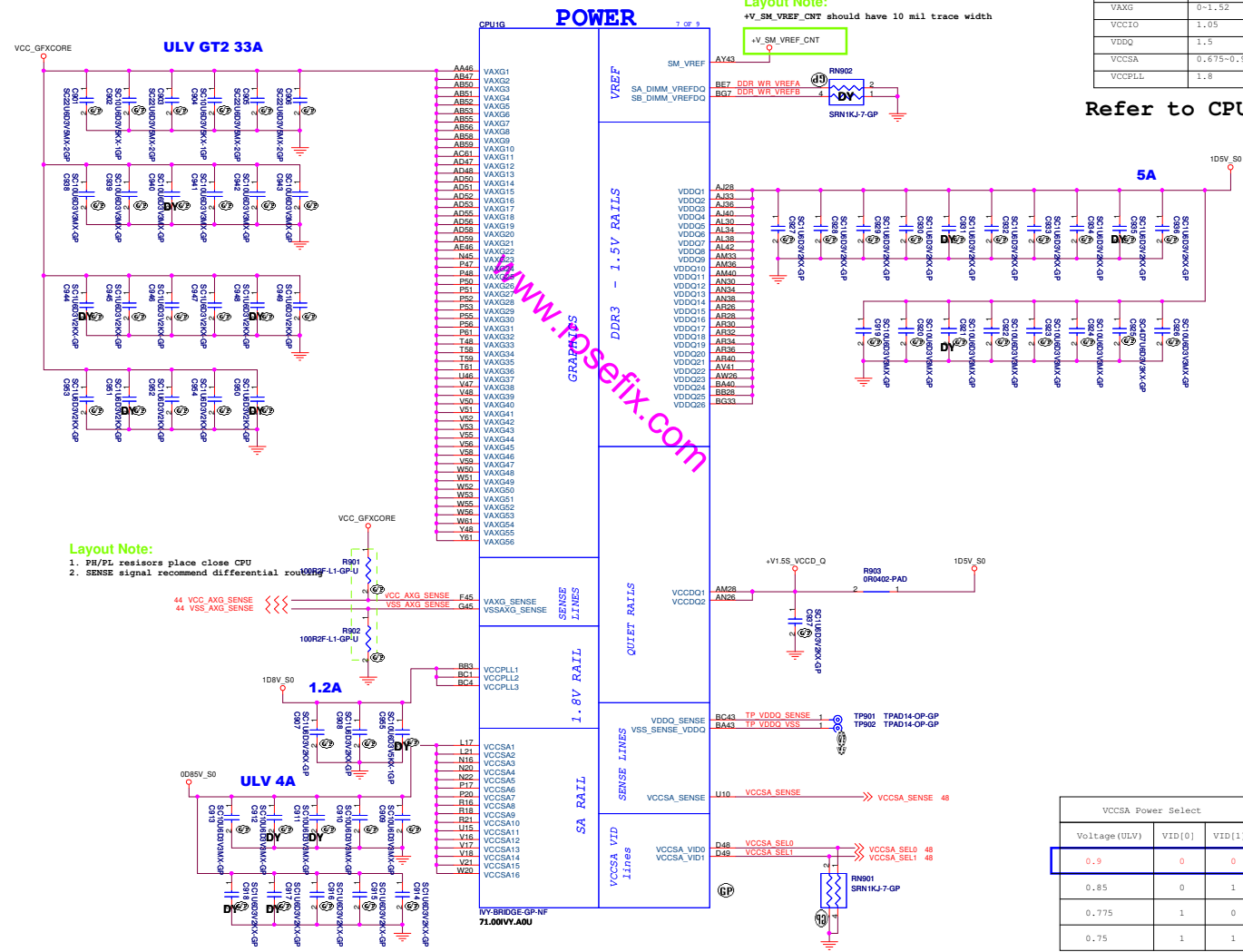
Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Voltage Rail	Voltage (V)	Iccmax (A)
VCC_CORE	0.9-1.52	33
VAXG	0-1.52	29 (gr2)
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.675-0.9	4
VCCPLL	1.8	1.2

Refer to CPU EDS V.1.7.5

Voltage Rail	Voltage (V)	Iccmax (A)
VCC_CORE	0.3-1.52	33
VAXG	0-1.52	29 (GT2)
VCCIO	1.05	8.5
VDDO	1.5	5
VCCSA	0.675-0.9	3
VCCPLL	1.8	1.2

Refer to CPU EDS V2.0



Layout Note:
 1. FB/TL resistors place close CPU
 2. SENSE signal recommend differential routing

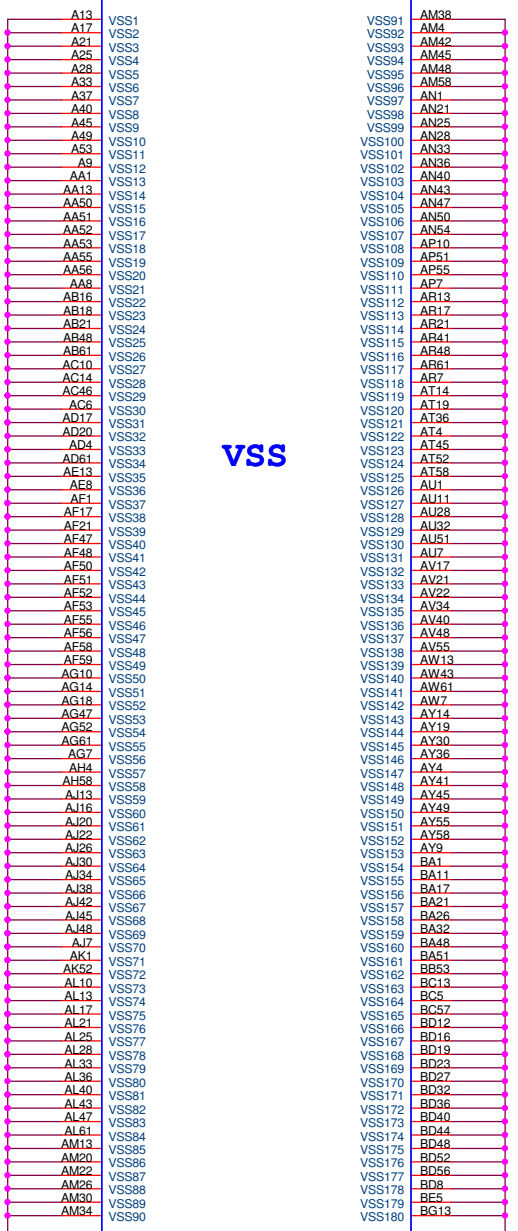
Layout Note:
 +V_SM_VREF_CWT should have 10 mil trace width

Voltage (ULV)	VID[0]	VID[1]
0.9	0	0
0.85	0	1
0.775	1	0
0.75	1	1

- CPU I/O**
- VAXG1-VAXG56
 - VCCPLL1-VCCPLL3
 - VCCSA1-VCCSA16
 - VDDO_SENSE
 - VSS_SENSE_VDDO
 - VCCSA_VID
 - VCCSA_VID1

SSID = CPU

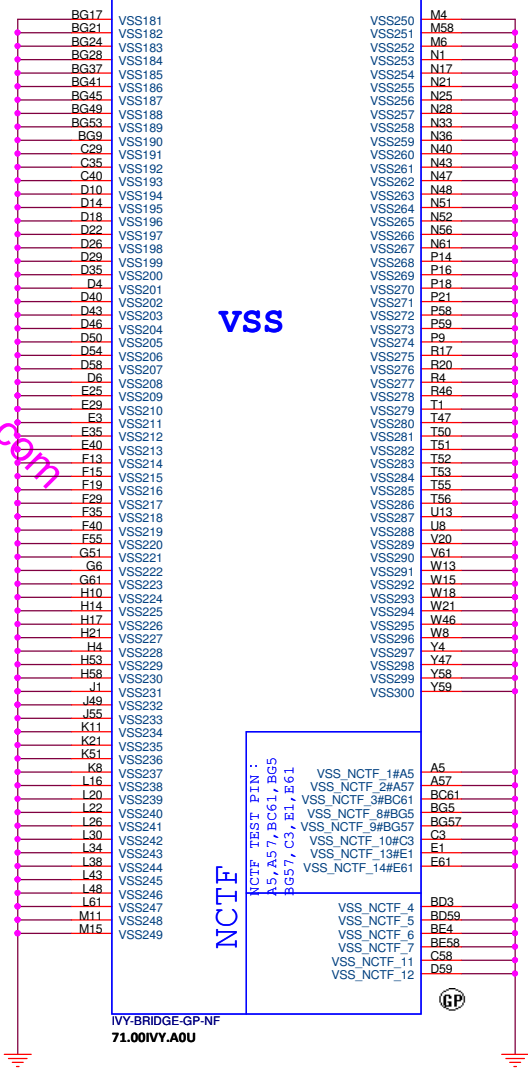
CPU1H 8 OF 9



IVY-BRIDGE-GP-NF
71.00IVY.A0U



CPU1I 9 OF 9



IVY-BRIDGE-GP-NF
71.00IVY.A0U

NCTF TEST PIN :
A5, A57, BC61, BG5
BG57, C3, E1, E61
VSS_NCTF_1#A5
VSS_NCTF_2#A57
VSS_NCTF_3#BC61
VSS_NCTF_9#BG5
VSS_NCTF_9#BC57
VSS_NCTF_10#C3
VSS_NCTF_13#E1
VSS_NCTF_14#E61
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_11
VSS_NCTF_12



M14 DIS



Title CPU (VSS)		
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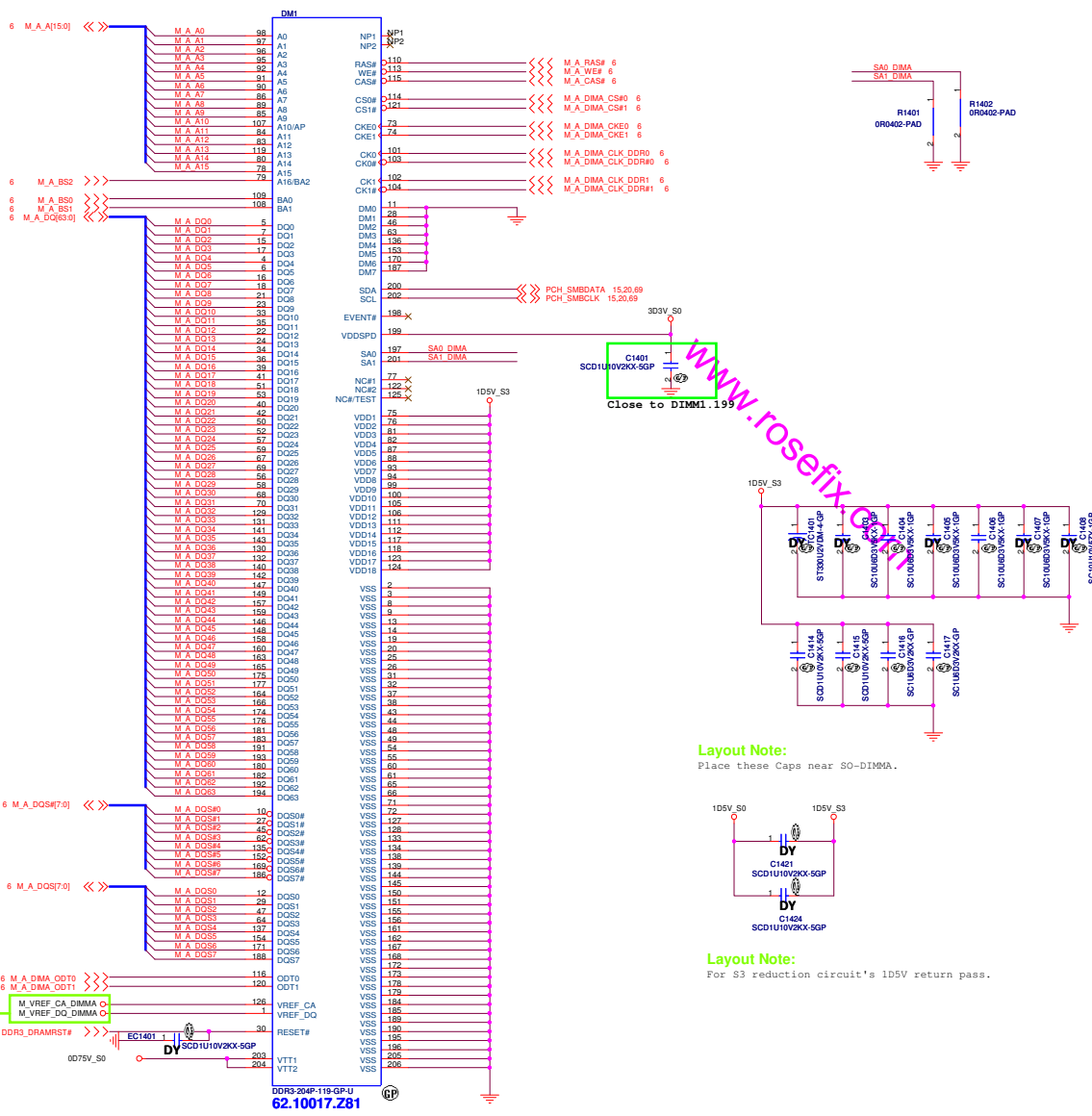
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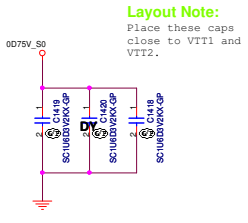
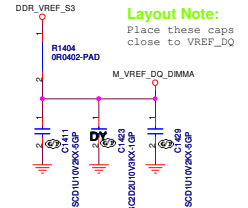
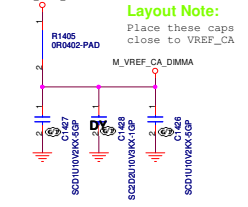
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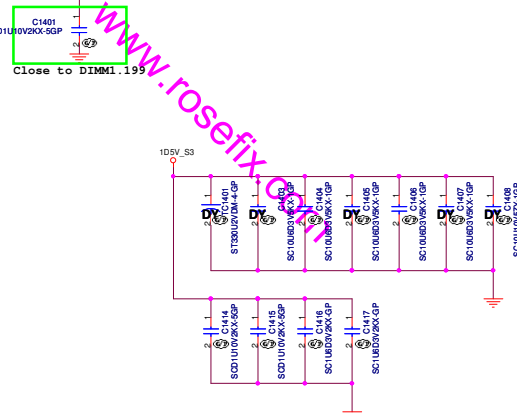
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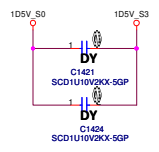
Note:
SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0x40
SO-DIMMA TS Address is 0x30



Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

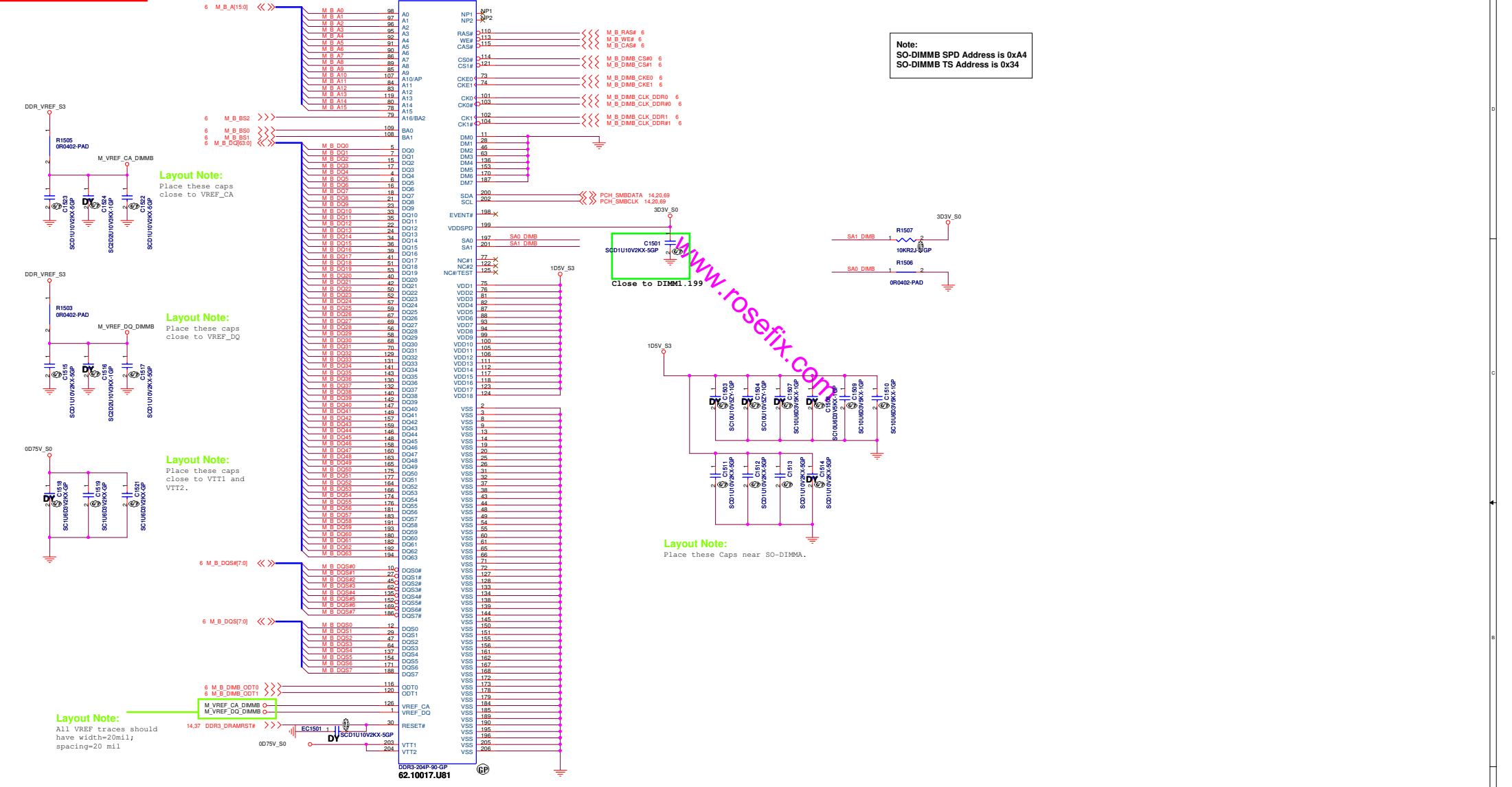


Layout Note:
Place these Caps near S0-DIMMA.



Layout Note:
For S3 reduction circuit's 1D5V return pass.

SSID = MEMORY



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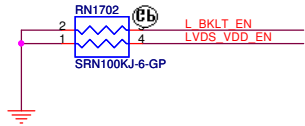
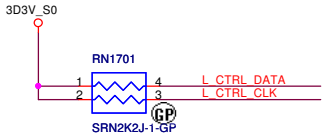
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M14 DIS



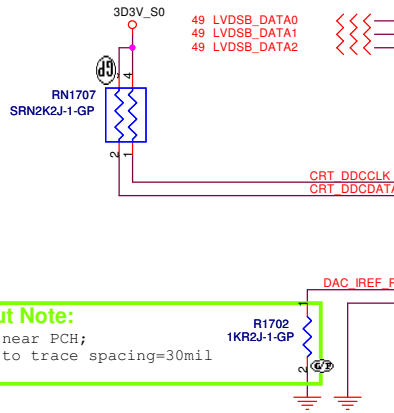
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SSID = PCH

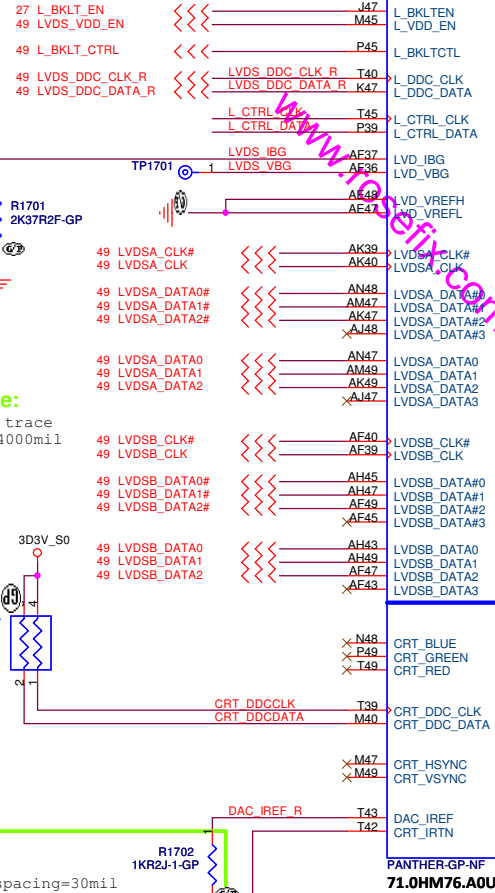


Layout Note:
Place near PCH;
trace to trace spacing=20mil

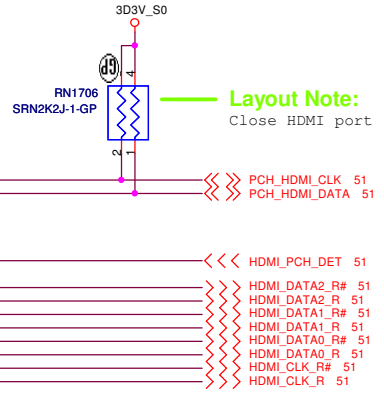
Layout Note:
LVDS signal trace
length max 4000mil



Layout Note:
Place near PCH;
trace to trace spacing=30mil



Digital Display Interface



Layout Note:
Close HDMI port

Layout Note:
HDMI trace length to DC CAP. max 10000mil

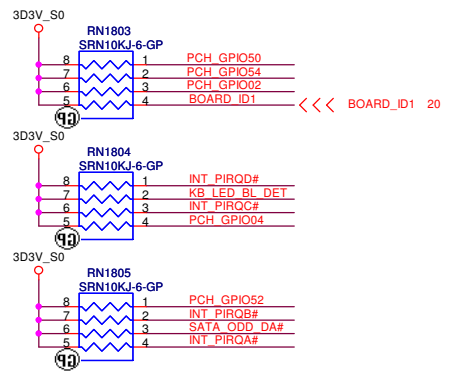
M14 DIS

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**

Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 17	of 105

SSID = PCH



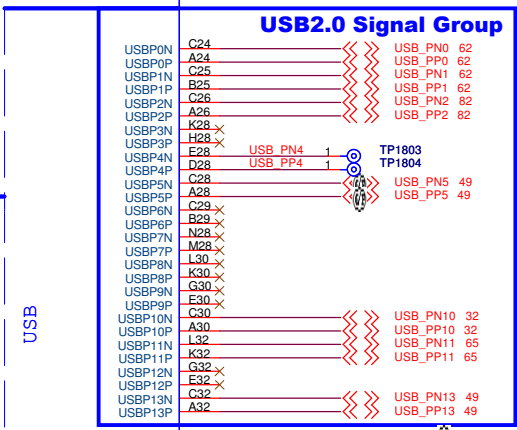
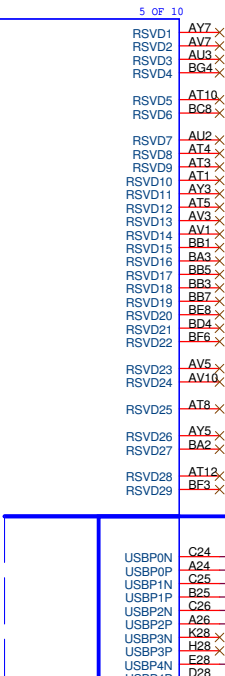
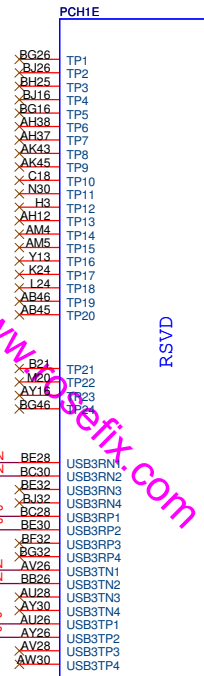
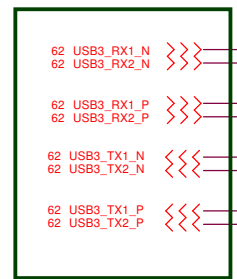
USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

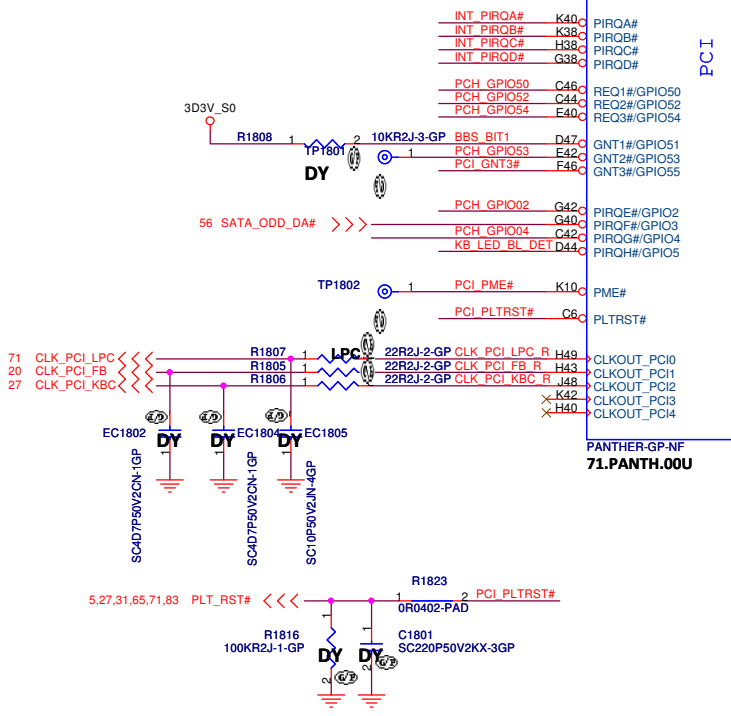
Layout Note:
Trace Length :
PCH ~9000mil~~Cap~~1000mil~~CONN



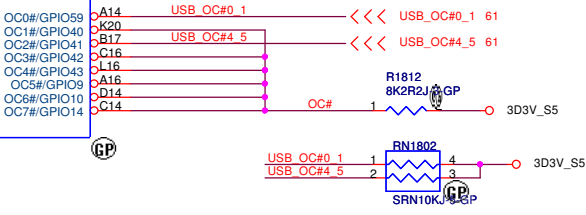
USB Table

Pair	Device
0	USB3.0 port2
1	USB3.0 port1, with Debug Port
2	USB2.0 port3
3	NC
4	NC
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	NC
9	NC
10	Card reader
11	WLAN
12	NC
13	CAMERA

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.



Layout Note:
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil



M14 DIS

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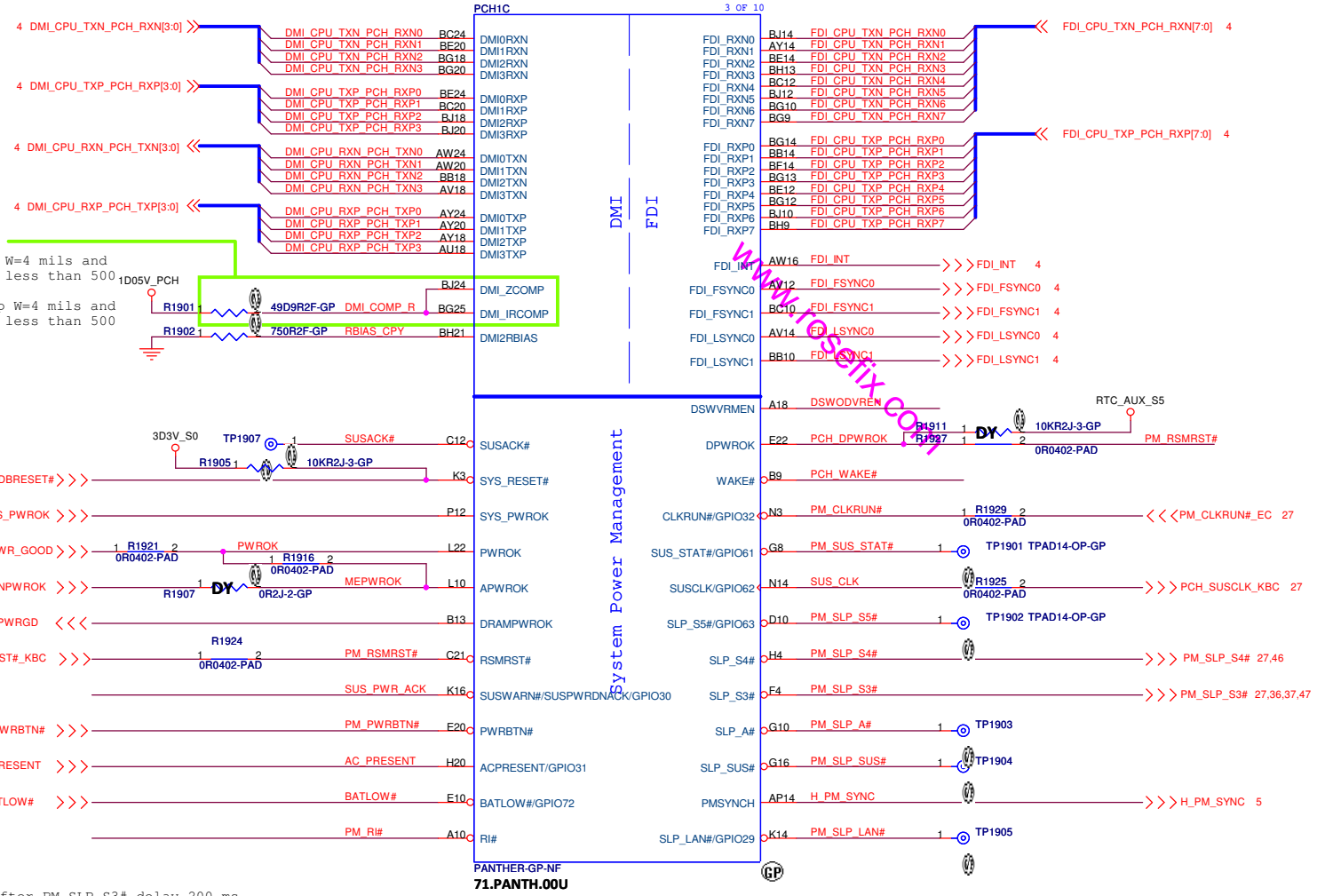
Title: **PCH (PCI/USB/NVRAM)**

Size A3 Document Number: **DNE40 14 CR DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 18 of 105

SSID = PCH

Layout Note:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

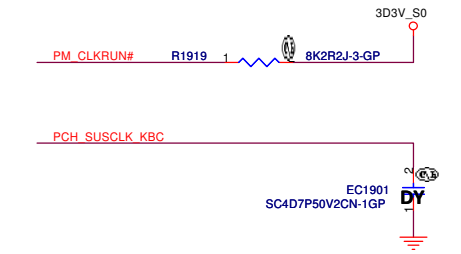


DSWODVREN - On Die DSW VR Enable

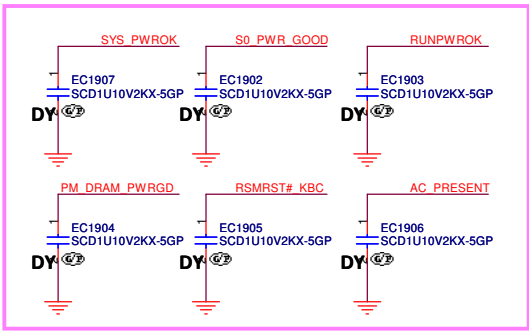
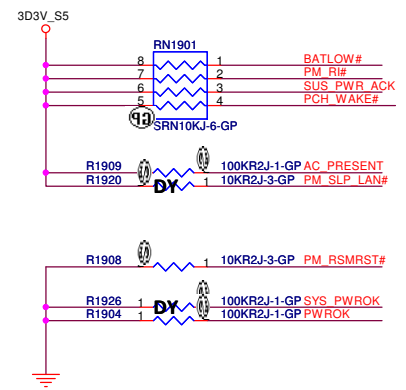
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5

DSWODVREN R1917 10K R1911 10KR2J-3-GP R1927 10KR2J-3-GP



Sequence:
 S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



reserve for EMI Request

M14 DIS

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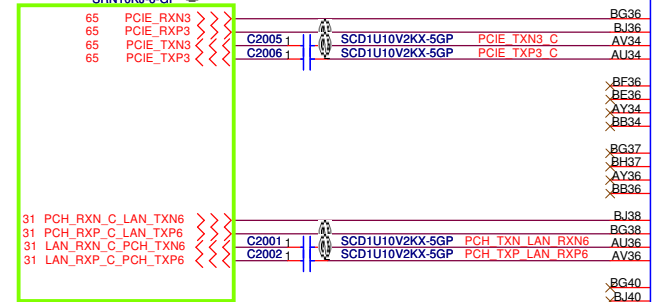
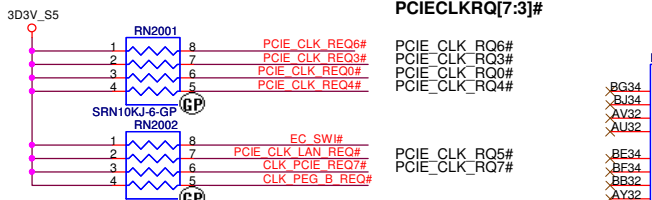
Title: **PCH (DM I/FDI/PM)**

Size A3 Document Number: **DNE40 14 CR DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 19 of 105

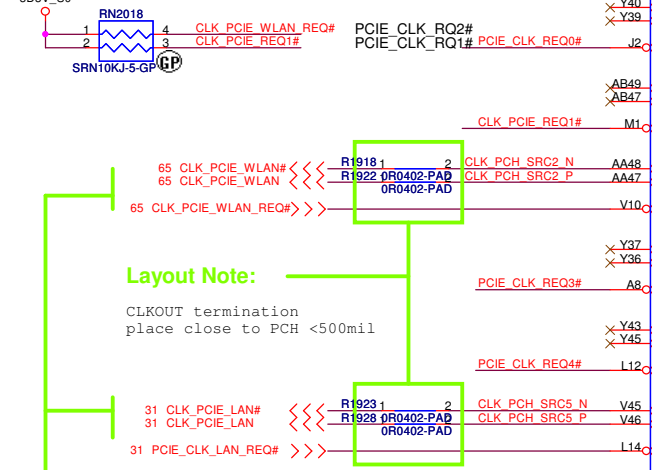
SSID = PCH

S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#



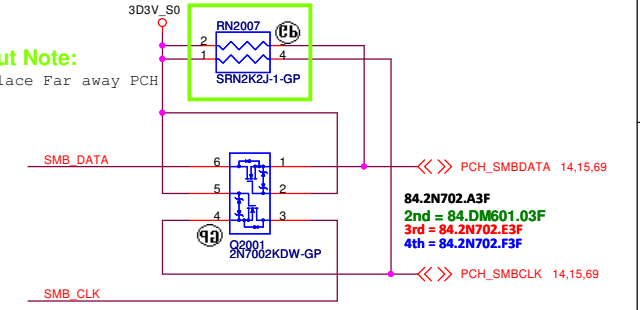
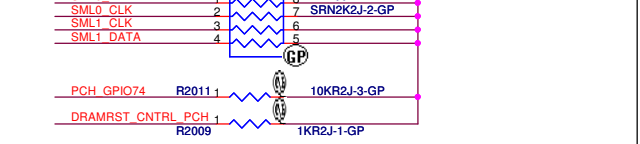
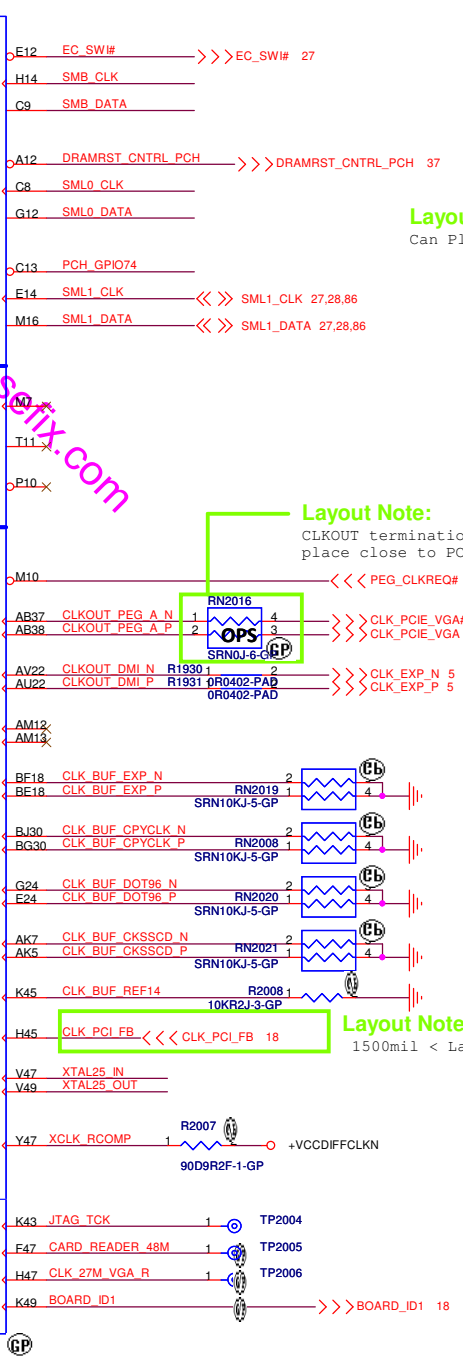
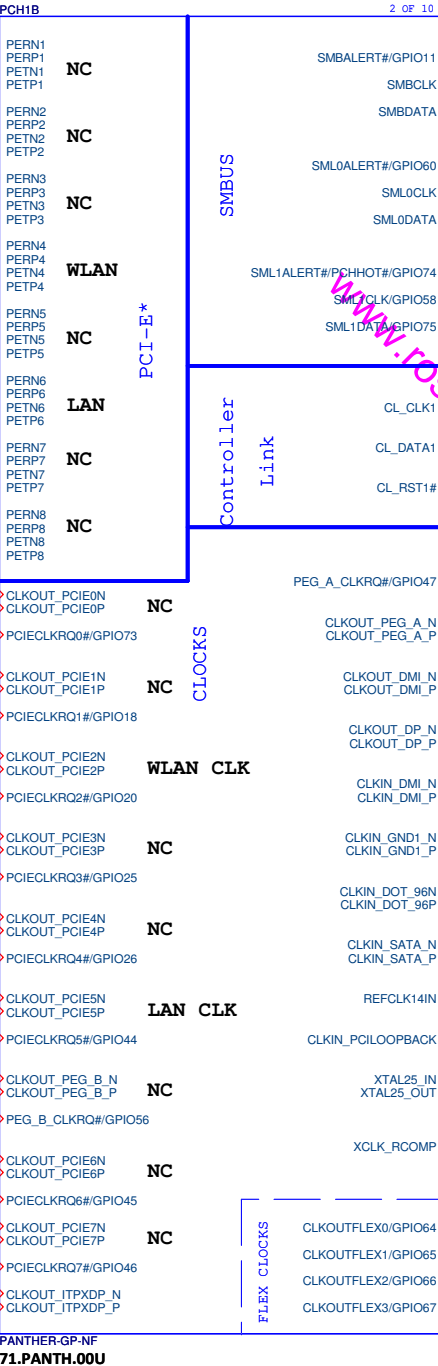
Layout Note:
Layout trace < 14000mil

S0 power rail CLKREQ#:
PCIECLKRQ[2:1]#



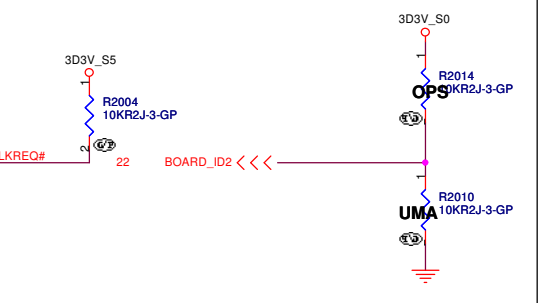
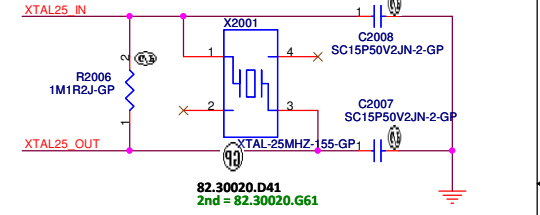
Layout Note:
CLKOUT termination place close to PCH < 500mil

Layout Note:
Layout trace < 14000mil



Layout Note:
Can Place Far away PCH

Layout Note:
CLKOUT termination place close to PCH < 500mil

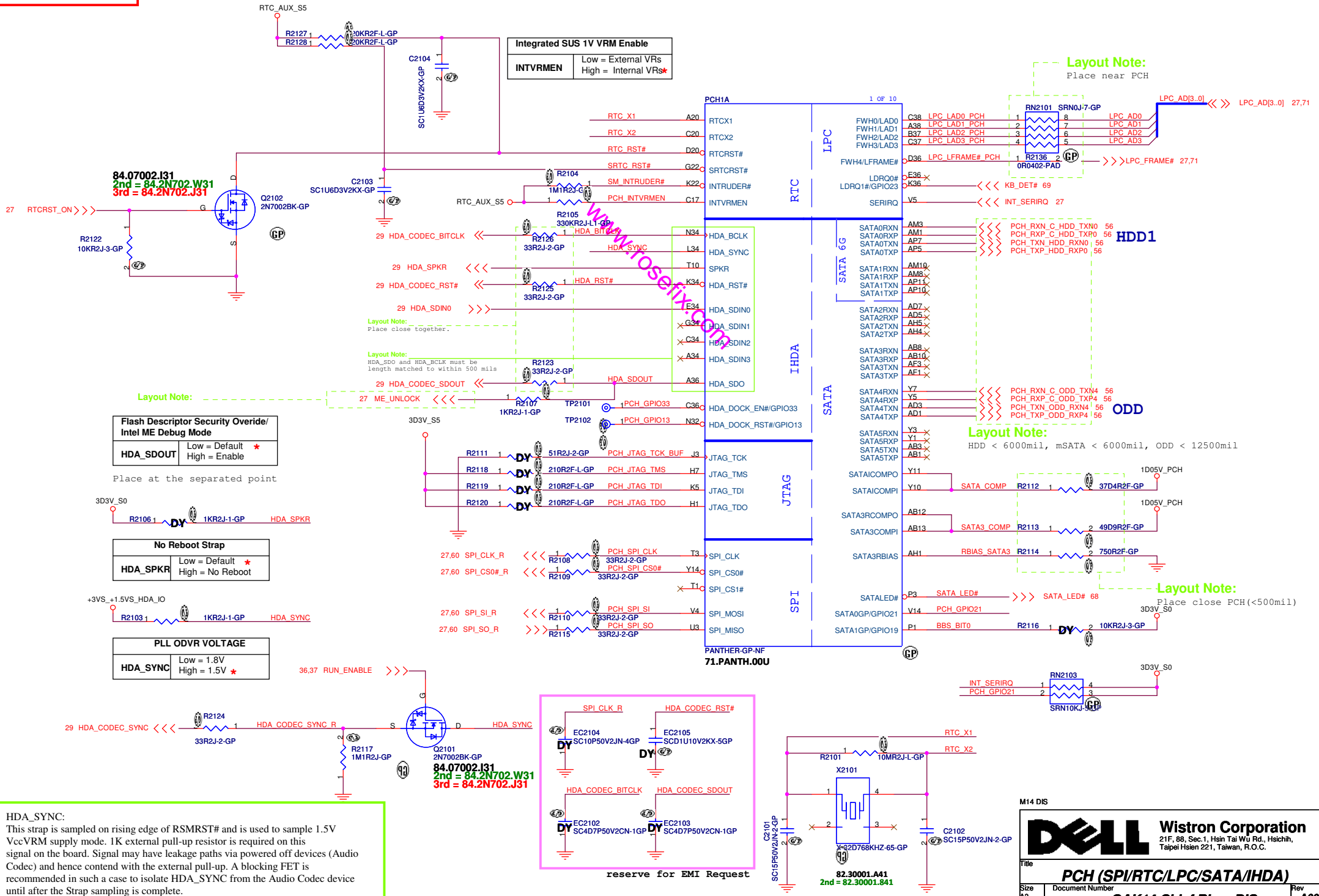


BIOS UMA/DIS Strap pin

	BOARD_ID1	BOARD_ID2
EN (AMB)	0	0
DIS	0	1
UMA	1	0
Optimus (NV)	1	1

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SSID = PCH



Integrated SUS 1V VRM Enable

INTVRMEN	Low = External VRs
	High = Internal VRs*

Layout Note:
Place near PCH

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

Flash Descriptor Security Override/ Intel ME Debug Mode

HDA_SDOOUT	Low = Default *
	High = Enable

Place at the separated point

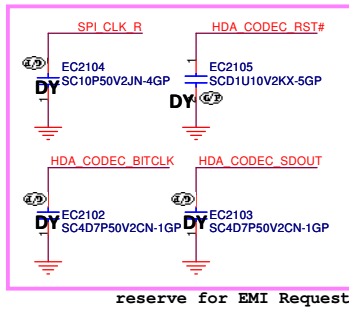
No Reboot Strap

HDA_SPKR	Low = Default *
	High = No Reboot

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V
	High = 1.5V *

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via required off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



Layout Note:
HDD < 6000mil, mSATA < 6000mil, ODD < 12500mil

Layout Note:
Place close PCH (<500mil)

M14 DIS

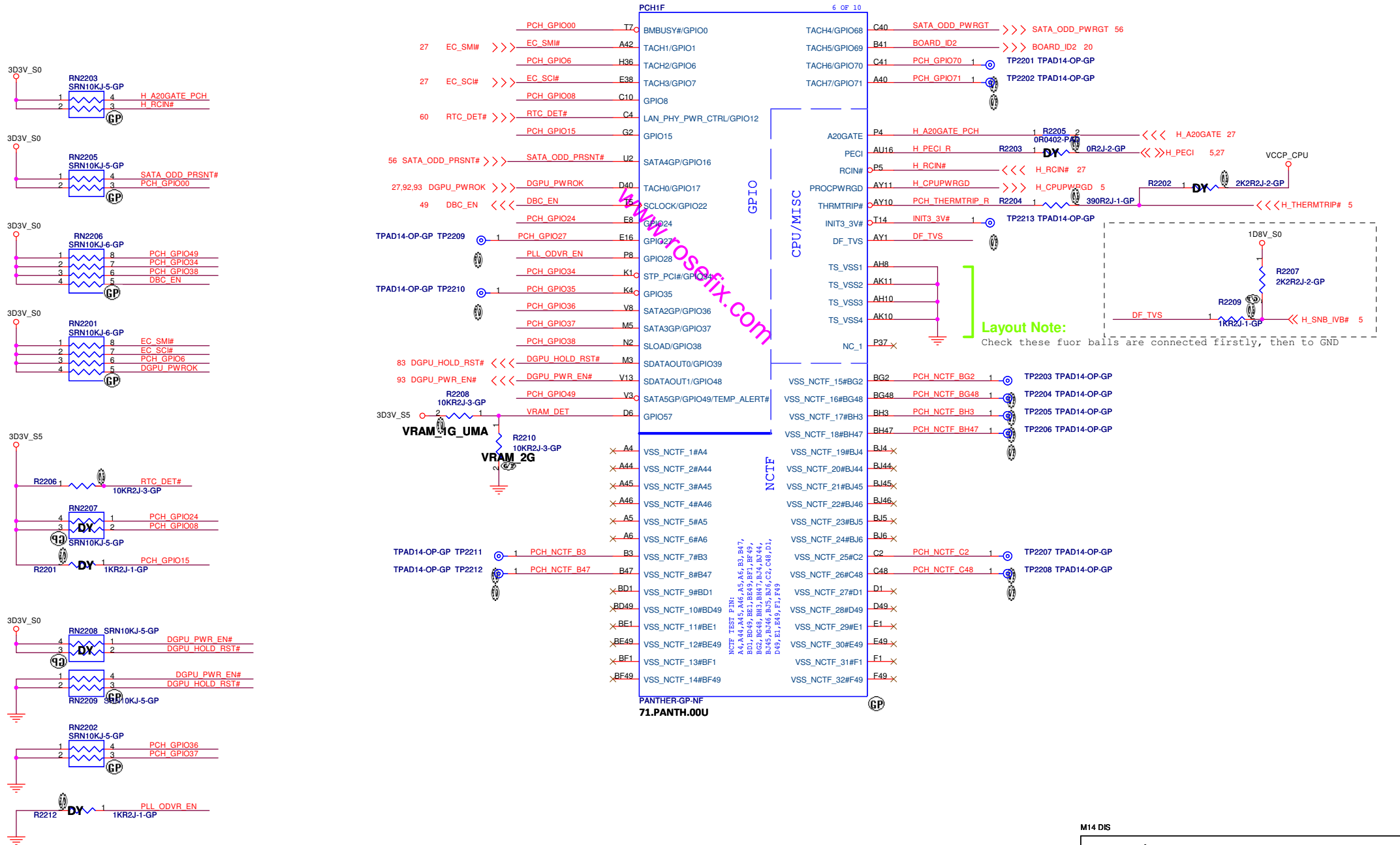
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Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00

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SSID = PCH



PLL ON DIE VR ENABLE	
GPI028 (PLL_ODVR_EN)	Weakly internal pull up 20k. High - Enable LOW - Disable

M14 DIS

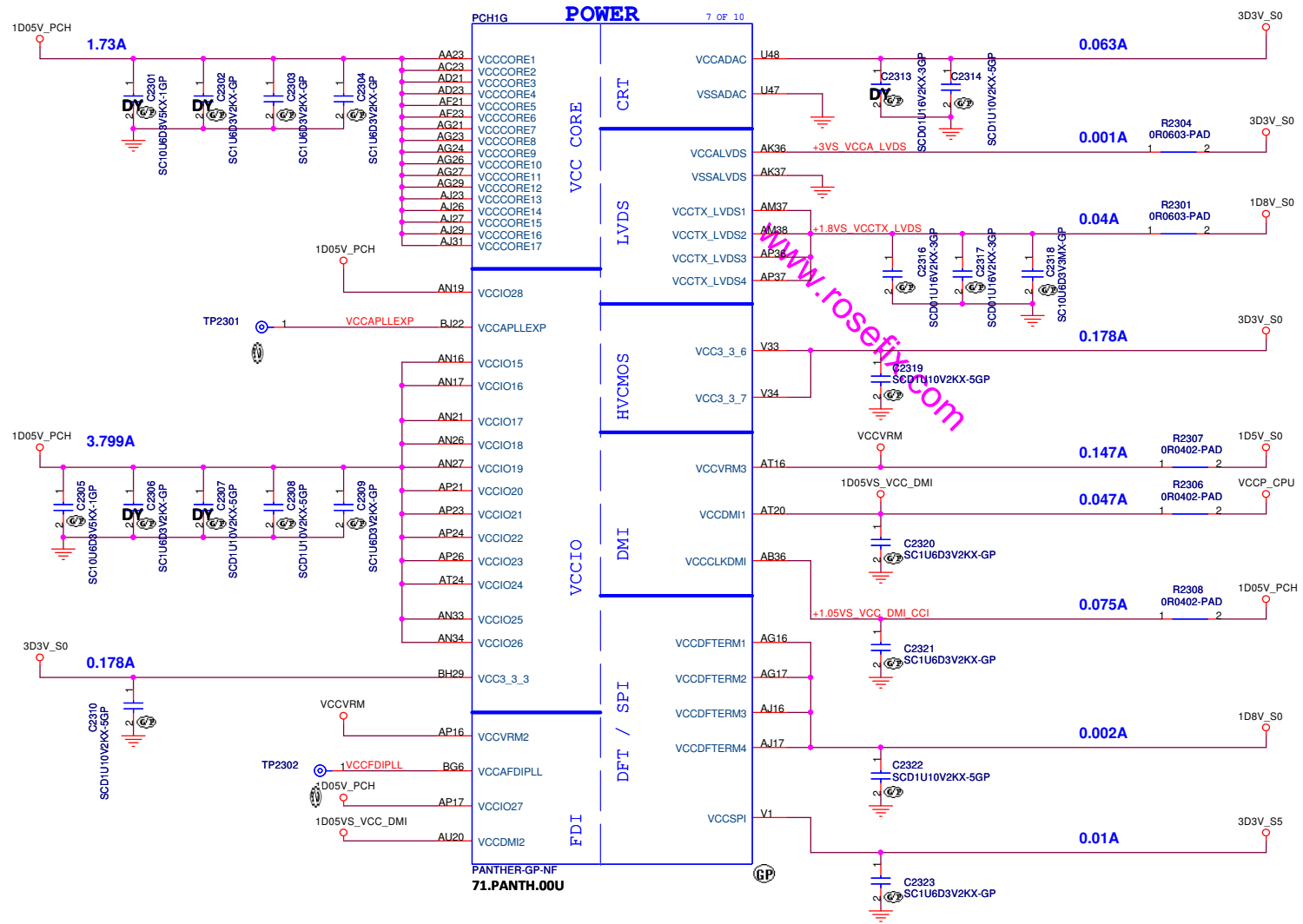
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Title: **PCH (GPIO/CPU)**

Size A3 Document Number: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 22 of 105

SSID = PCH



Voltage Rail	Voltage (V)	Iccmax (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.1.8

check

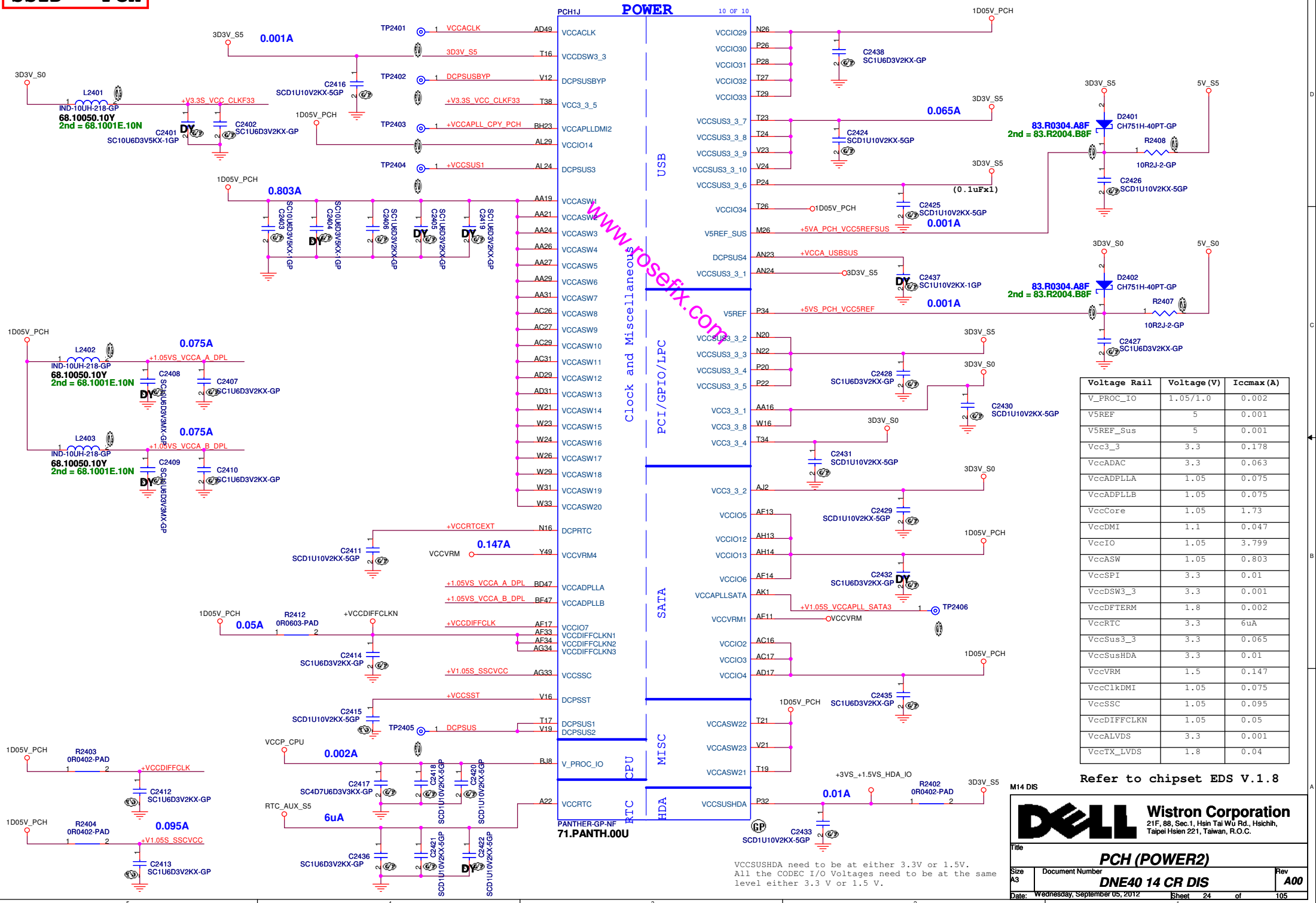
M14 DIS

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Title: **PCH (POWER1)**

Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 23	of 105

SSID = PCH



Voltage Rail	Voltage (V)	Iccmax (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.1.8



Title			PCH (POWER2)		
Size	Document Number				Rev
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VCCSUSHDA need to be at either 3.3V or 1.5V.
All the CODEC I/O Voltages need to be at the same level either 3.3 V or 1.5 V.

SSID = PCH

PCH1H 8 OF 10

H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK9
AB11	VSS6	VSS85	AL16
AB14	VSS7	VSS86	AL17
AB39	VSS8	VSS87	AL19
AB4	VSS9	VSS88	AL2
AB43	VSS10	VSS89	AL21
AB5	VSS11	VSS90	AL23
AB7	VSS12	VSS91	AL26
AC19	VSS13	VSS92	AL27
AC2	VSS14	VSS93	AL31
AC21	VSS15	VSS94	AL33
AC24	VSS16	VSS95	AL34
AC33	VSS17	VSS96	AL48
AC34	VSS18	VSS97	AM11
AC48	VSS19	VSS98	AM14
AD10	VSS20	VSS99	AM36
AD11	VSS21	VSS100	AM39
AD12	VSS22	VSS101	AM43
AD13	VSS23	VSS102	AM45
AD19	VSS24	VSS103	AM46
AD24	VSS25	VSS104	AM7
AD26	VSS26	VSS105	AN2
AD27	VSS27	VSS106	AN29
AD33	VSS28	VSS107	AN3
AD34	VSS29	VSS108	AN31
AD36	VSS30	VSS109	AP12
AD37	VSS31	VSS110	AP19
AD38	VSS32	VSS111	AP28
AD39	VSS33	VSS112	AP30
AD4	VSS34	VSS113	AP32
AD40	VSS35	VSS114	AP38
AD42	VSS36	VSS115	AP4
AD43	VSS37	VSS116	AP42
AD45	VSS38	VSS117	AP46
AD46	VSS39	VSS118	AP8
AD8	VSS40	VSS119	AR2
AE2	VSS41	VSS120	AR48
AE3	VSS42	VSS121	AT11
AE10	VSS43	VSS122	AT13
AE12	VSS44	VSS123	AT18
AD14	VSS45	VSS124	AT22
AD16	VSS46	VSS125	AT26
AF16	VSS47	VSS126	AT28
AF19	VSS48	VSS127	AT30
AF24	VSS49	VSS128	AT32
AF26	VSS50	VSS129	AT34
AF27	VSS51	VSS130	AT39
AF29	VSS52	VSS131	AT42
AF31	VSS53	VSS132	AT46
AF38	VSS54	VSS133	AT7
AF4	VSS55	VSS134	AU24
AF42	VSS56	VSS135	AU30
AF46	VSS57	VSS136	AV16
AF5	VSS58	VSS137	AV20
AF7	VSS59	VSS138	AV24
AF8	VSS60	VSS139	AV30
AG19	VSS61	VSS140	AV38
AG2	VSS62	VSS141	AV4
AG31	VSS63	VSS142	AV43
AG48	VSS64	VSS143	AV8
AH11	VSS65	VSS144	AW14
AH3	VSS66	VSS145	AW18
AH36	VSS67	VSS146	AW2
AH39	VSS68	VSS147	AW22
AH40	VSS69	VSS148	AW26
AH42	VSS70	VSS149	AW28
AH46	VSS71	VSS150	AW32
AH7	VSS72	VSS151	AW34
AJ19	VSS73	VSS152	AW36
AJ21	VSS74	VSS153	AW40
AJ24	VSS75	VSS154	AW48
AJ33	VSS76	VSS155	AV11
AJ34	VSS77	VSS156	AY12
AK12	VSS78	VSS157	AY22
AK3	VSS79	VSS158	AY28

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PCH1I 9 OF 10

AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K32
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L20
B31	VSS168	VSS268	L26
B35	VSS169	VSS269	L28
B39	VSS170	VSS270	L36
B7	VSS171	VSS271	L48
F45	VSS172	VSS272	M12
BB12	VSS173	VSS273	P16
BB16	VSS174	VSS274	M18
BB20	VSS175	VSS275	M22
BB22	VSS176	VSS276	M24
BB24	VSS177	VSS277	M30
BB28	VSS178	VSS278	M32
BB30	VSS179	VSS279	M34
BB38	VSS180	VSS280	M38
BB4	VSS181	VSS281	M4
BB46	VSS182	VSS282	M42
BC14	VSS183	VSS283	M46
BC18	VSS184	VSS284	M8
BC2	VSS185	VSS285	N18
BC22	VSS186	VSS286	P30
BC26	VSS187	VSS287	P32
BC32	VSS188	VSS288	N47
BC34	VSS189	VSS289	P18
BC36	VSS190	VSS290	T33
BC40	VSS191	VSS291	P40
BC42	VSS192	VSS292	P43
BC48	VSS193	VSS293	P47
BD46	VSS194	VSS294	P7
BD5	VSS195	VSS295	R2
BE22	VSS196	VSS296	R48
BE26	VSS197	VSS297	T12
BE40	VSS198	VSS298	T31
BF10	VSS199	VSS299	T37
BF12	VSS200	VSS300	T4
BF16	VSS201	VSS301	W34
BF20	VSS202	VSS302	T46
BF22	VSS203	VSS303	T47
BF24	VSS204	VSS304	T8
BF26	VSS205	VSS305	V11
BF28	VSS206	VSS306	V17
BF3	VSS207	VSS307	V26
BF30	VSS208	VSS308	V27
BF38	VSS209	VSS309	V29
BF40	VSS210	VSS309	V31
BF8	VSS211	VSS310	V36
BG17	VSS212	VSS311	V39
BG21	VSS213	VSS312	V43
BG33	VSS214	VSS313	V7
BG44	VSS215	VSS314	W17
BG8	VSS216	VSS315	W19
BH11	VSS217	VSS316	W2
BH15	VSS218	VSS317	W27
BH17	VSS219	VSS318	W48
BH19	VSS220	VSS319	W48
H10	VSS221	VSS320	Y12
BH27	VSS222	VSS321	Y38
BH31	VSS223	VSS322	Y4
BH33	VSS224	VSS323	Y42
BH35	VSS225	VSS324	Y46
BH39	VSS226	VSS325	Y8
BH43	VSS227	VSS326	BG29
D3	VSS228	VSS327	N24
D12	VSS229	VSS328	N24
D16	VSS230	VSS329	AJ3
D18	VSS231	VSS330	AD47
D22	VSS232	VSS331	B43
D24	VSS233	VSS332	BE10
D26	VSS234	VSS333	BG41
D30	VSS235	VSS334	BG14
D32	VSS236	VSS335	G14
D34	VSS237	VSS336	H16
D38	VSS238	VSS337	T36
D42	VSS239	VSS338	BG22
D4	VSS240	VSS339	BG24
E18	VSS241	VSS340	C22
E26	VSS242	VSS341	AP13
G18	VSS243	VSS342	M14
G20	VSS244	VSS343	AF3
G26	VSS245	VSS344	AP1
G28	VSS246	VSS345	BE16
G36	VSS247	VSS346	BC16
G48	VSS248	VSS347	BG28
H12	VSS249	VSS348	BG28
H18	VSS250	VSS349	VSS351
H22	VSS251	VSS350	VSS352
H24	VSS252	VSS351	BJ28
H26	VSS253	VSS352	
H30	VSS254		
H32	VSS255		
H34	VSS256		
F3	VSS257		
	VSS258		

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71.PANTH.00U



M14 DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
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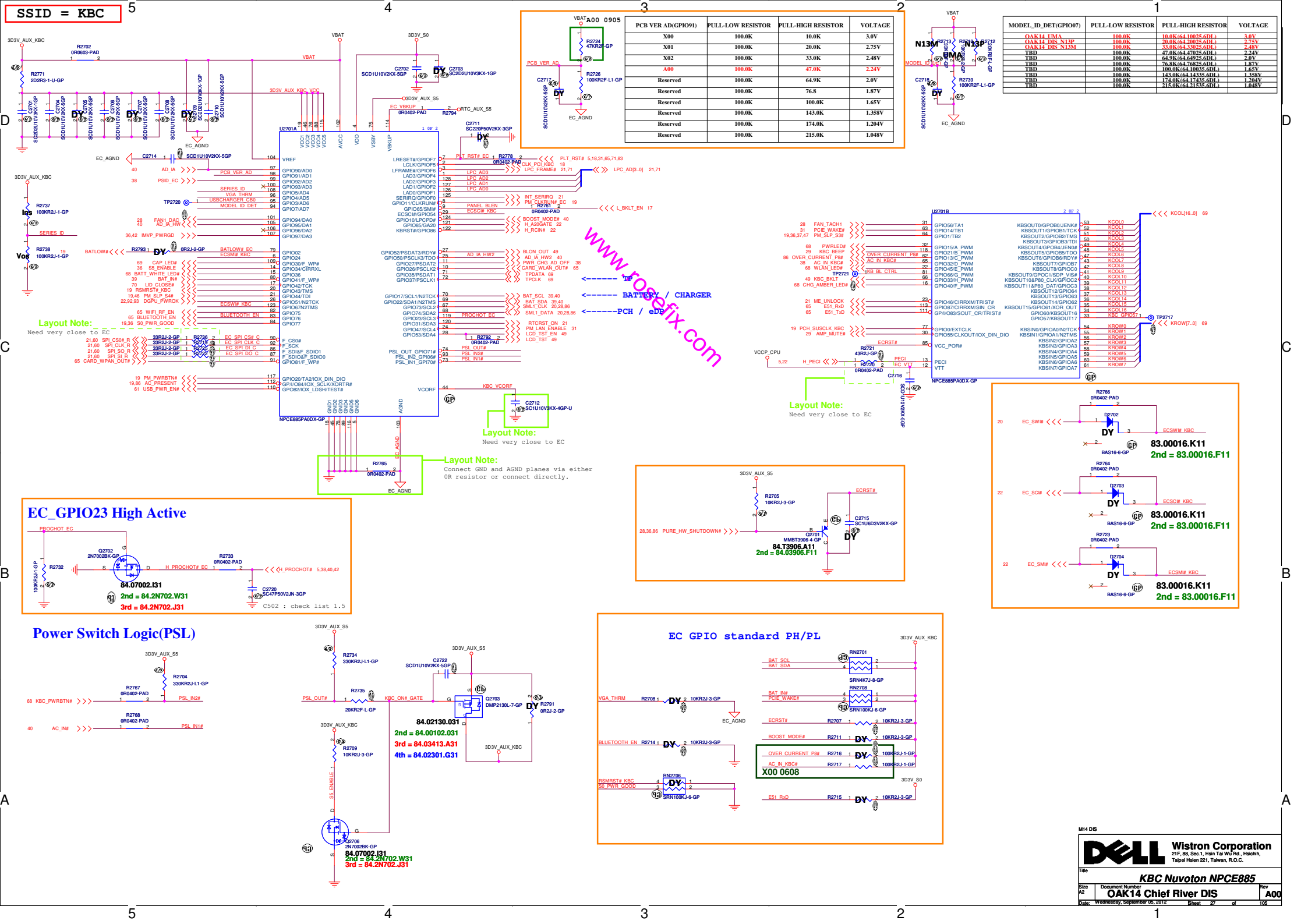
Date: Wednesday, September 05, 2012 Sheet 25 of 105

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M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
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A3	OAK14 Chief River DIS	A00
Date:	Wednesday, September 05, 2012	Sheet 26 of 105



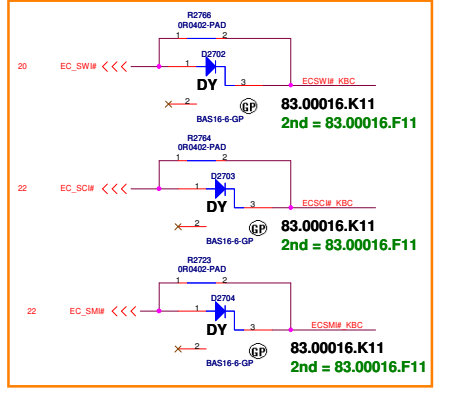
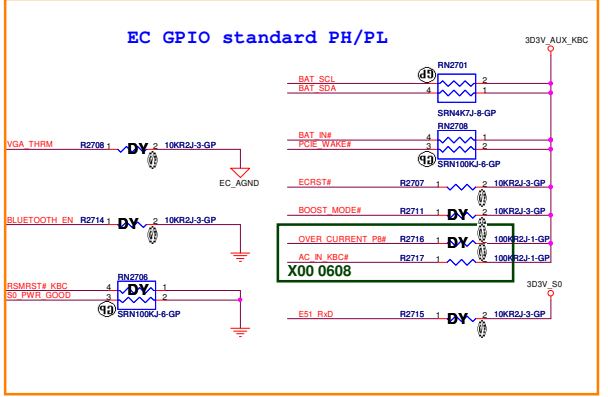
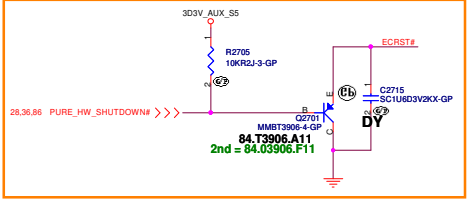
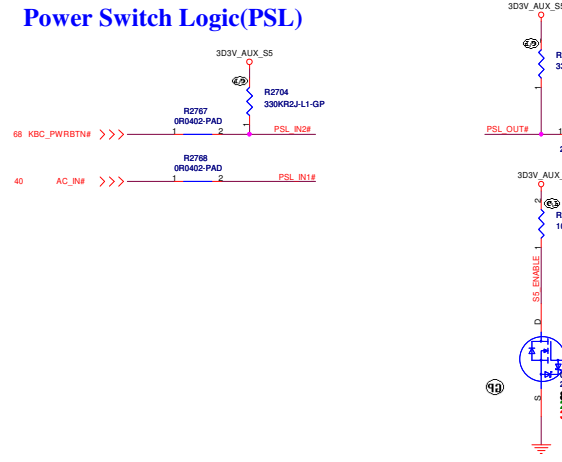
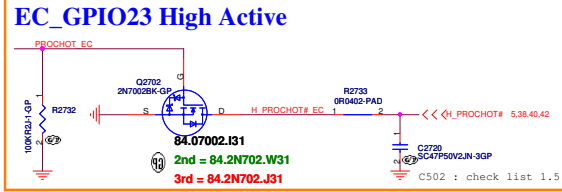
PCB VER AD(GPIO#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO#07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
OAK14_LINA	100.0K	100.0K(64.10035.GDI.)	3.0V
OAK14_DIS_N13M	100.0K	20.0K(64.20035.GDI.)	2.75V
OAK14_DIS_N13M	100.0K	33.0K(64.33035.GDI.)	2.48V
TBD	100.0K	47.0K(64.47035.GDI.)	2.24V
TBD	100.0K	64.9K(64.64935.GDI.)	2.0V
TBD	100.0K	76.8K(64.76835.GDI.)	1.87V
TBD	100.0K	100.0K(64.10035.GDI.)	1.65V
TBD	100.0K	143.0K(64.14335.GDI.)	1.358V
TBD	100.0K	174.0K(64.17435.GDI.)	1.204V
TBD	100.0K	215.0K(64.21535.GDI.)	1.048V

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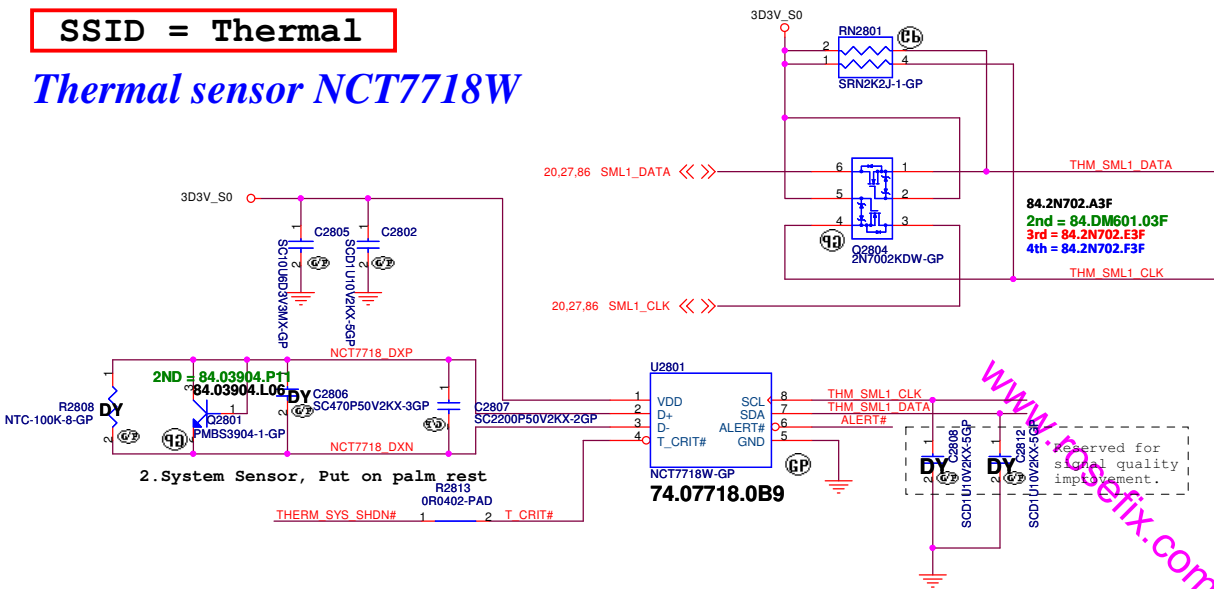
BATTERY / CHARGER

PCH / eDP



SSID = Thermal

Thermal sensor NCT7718W

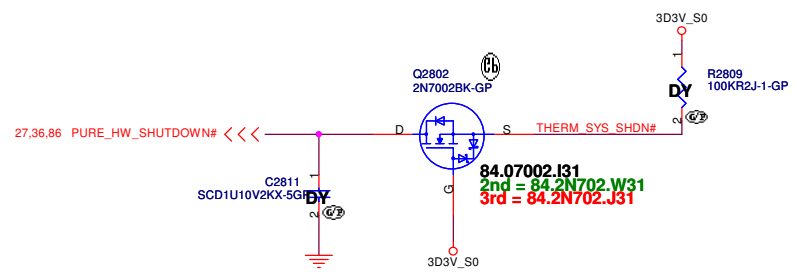


ALERT# /T CRIT# Pull-up Resistor

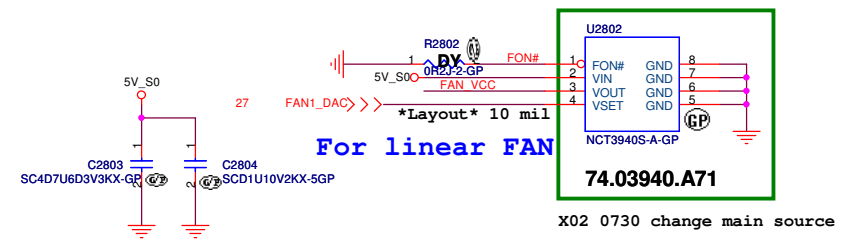
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	82°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

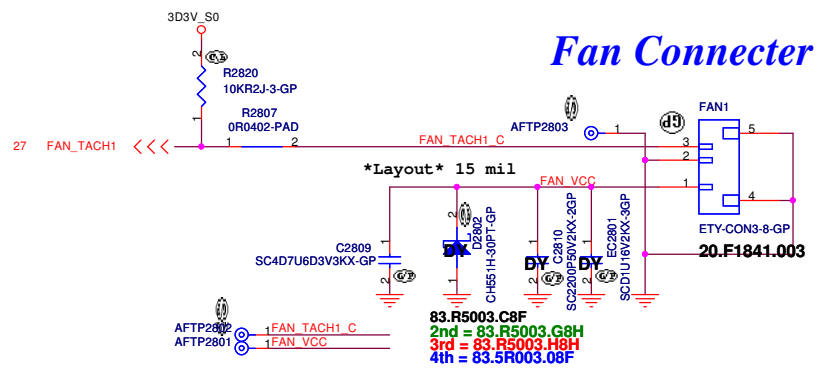
Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing, and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W



Fan controller NCT3940S-A



Fan Connector



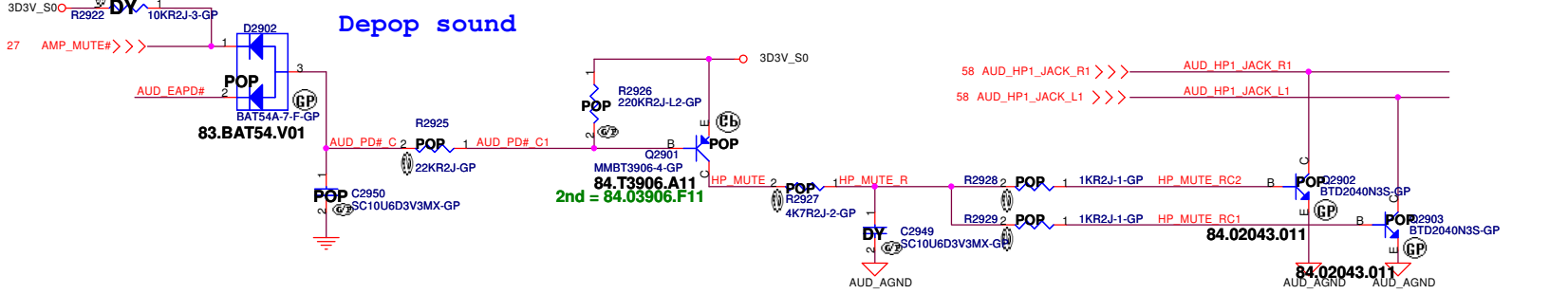
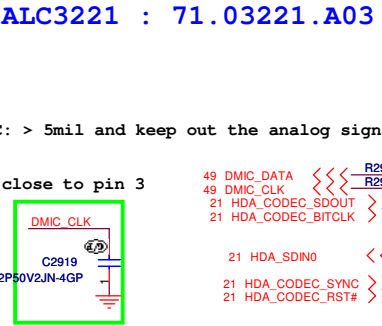
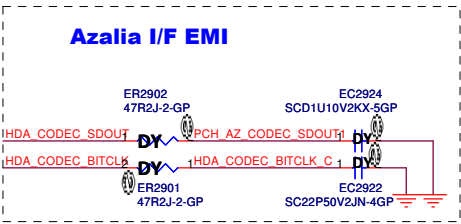
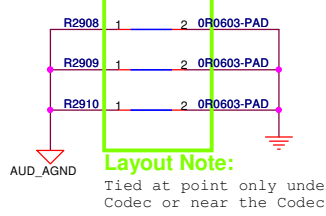
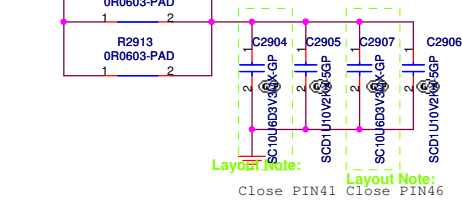
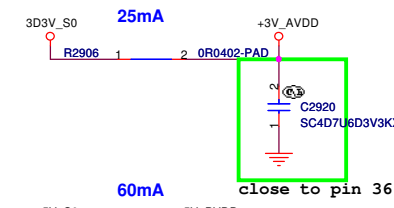
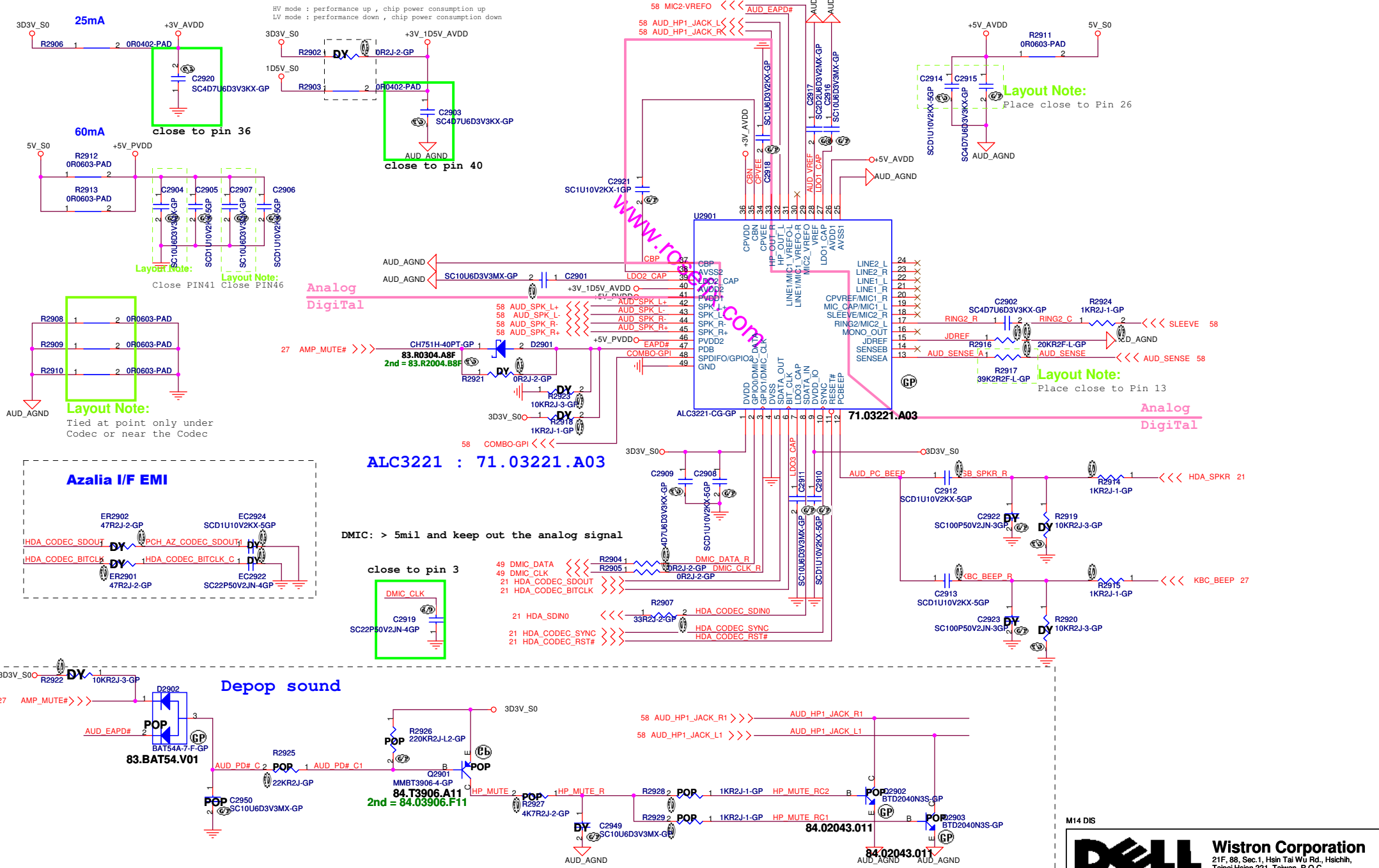
M14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal NCT7718W/Fan Controller P2793**

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SSID = AUDIO



W14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC3221**

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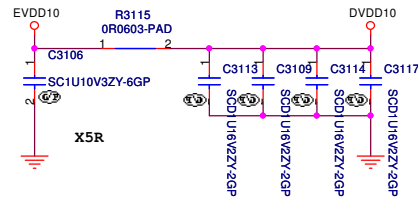
(Blanking)

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M14 DIS

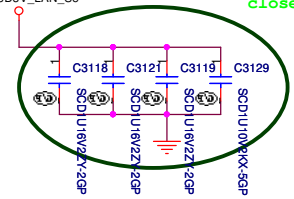
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012		Sheet 30 of 105

LAN CHIP

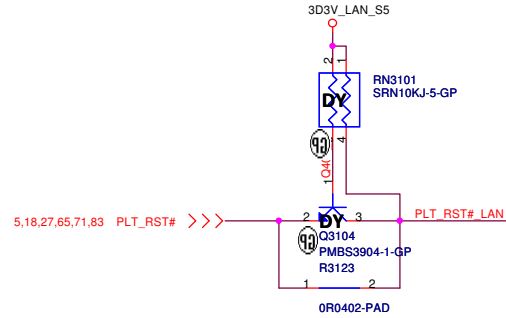
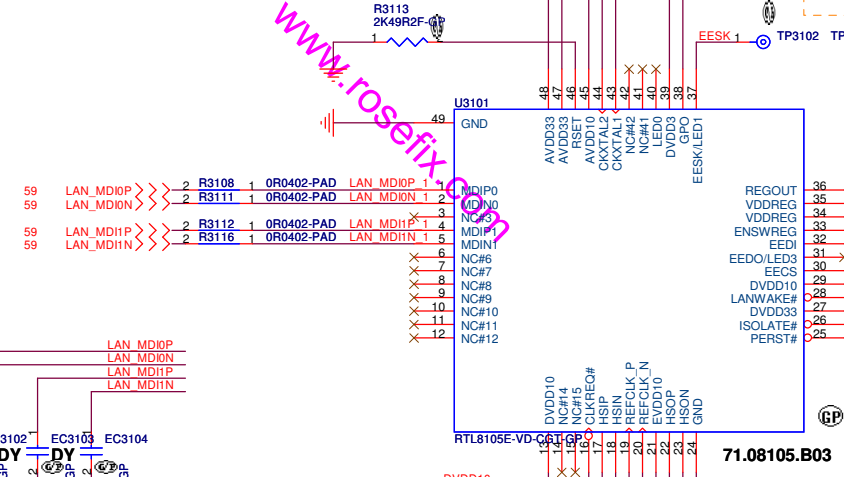


1ms < +3D3V_LAN_S5 Rising time (10%~90%) <100ms

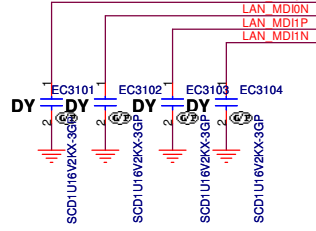
40 mils



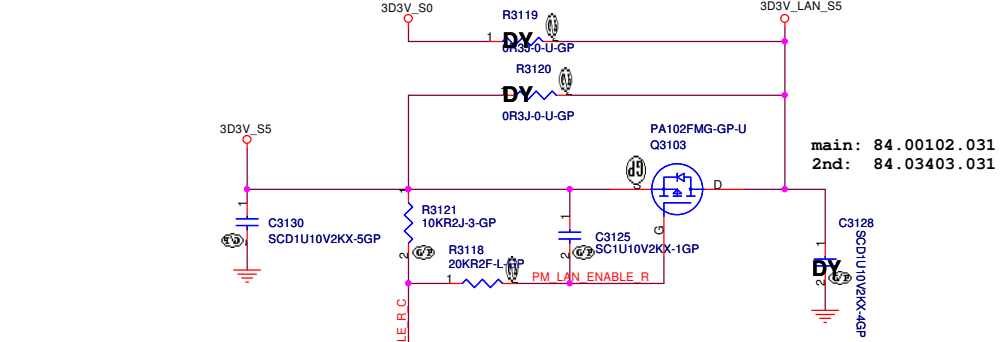
close to pin 27 39 47 48



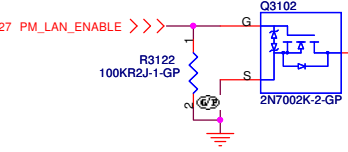
5,18,27,65,71,83 PLT_RST# >>>



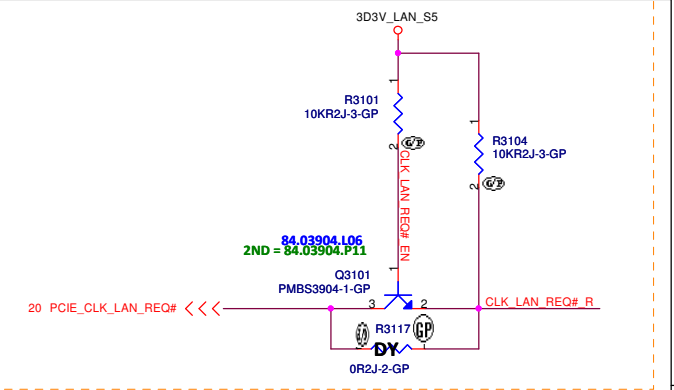
251mA



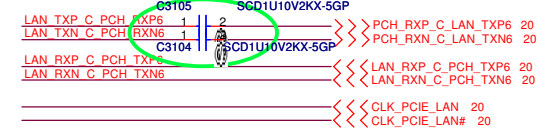
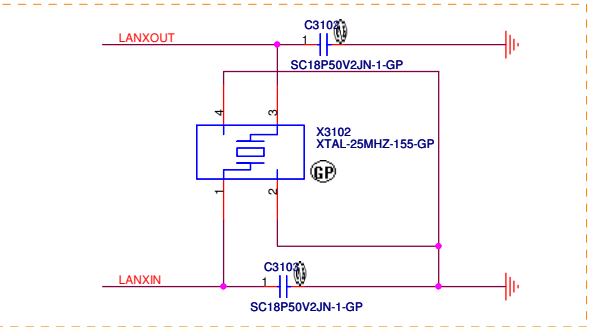
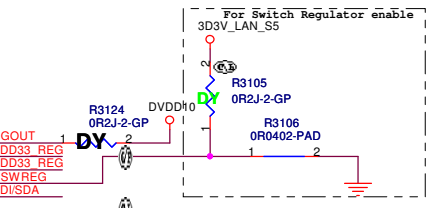
main: 84.00102.031
2nd: 84.03403.031



27 PM_LAN_ENABLE >>>



20 PCIE_CLK_LAN_REQ# <<<



LAN_TXP_C_PCH_TXP6 >>> PCH_RXN_C_LAN_TXN6 20
LAN_TXN_C_PCH_RXN6 >>> PCH_RXN_C_LAN_TXN6 20
LAN_RXP_C_PCH_TXP6 >>> LAN_RXN_C_PCH_TXN6 20
LAN_RXN_C_PCH_RXN6 >>> LAN_RXN_C_PCH_TXN6 20
CLK_PCIE_LAN 20
CLK_PCIE_LAN# 20

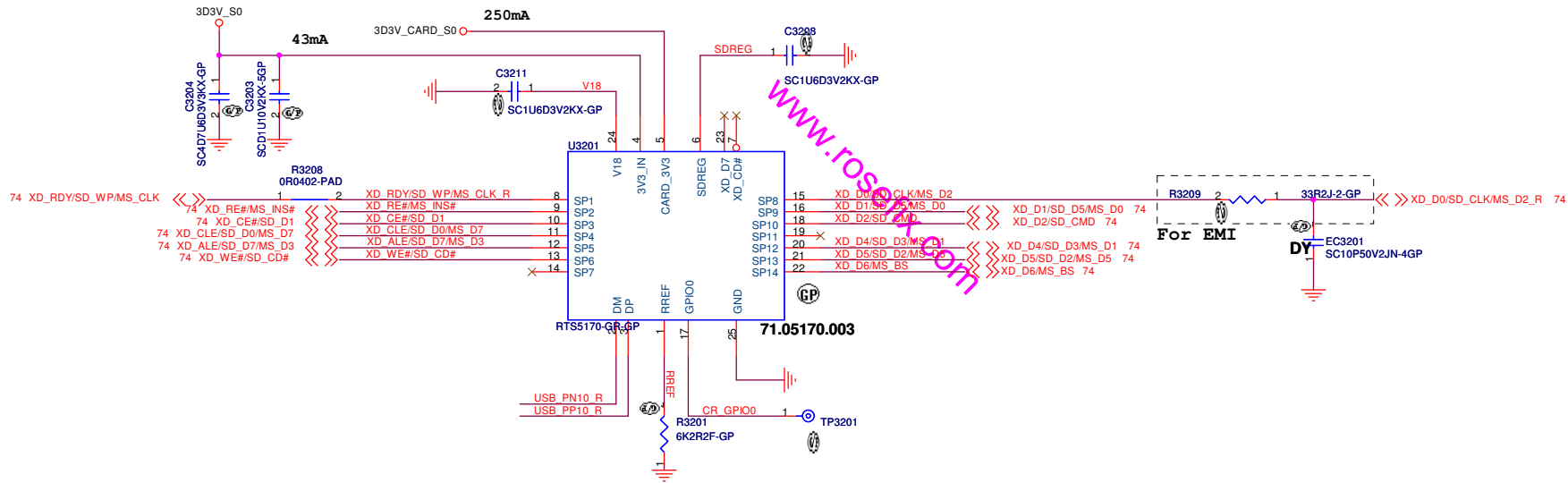
M14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

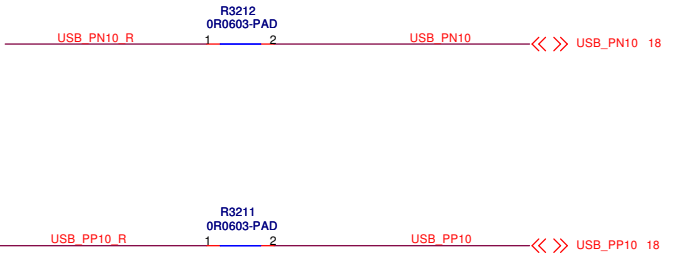
Title: **LOM**

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SSID = SDIO



Close U3201



M14 DIS

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader-RTS5170**

Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
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M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012		Sheet 33 of 105

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(Blanking)

M14 DIS



Title		
Reserved		
Size	Document Number	Rev
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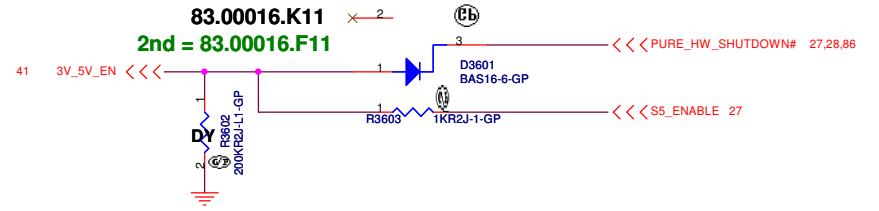
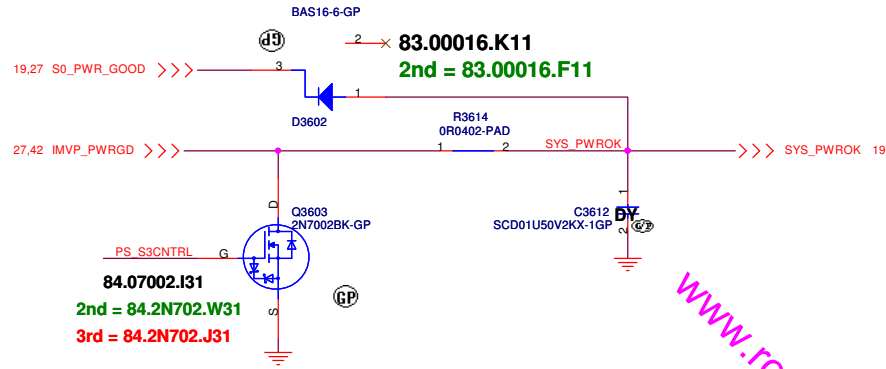
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M14 DIS

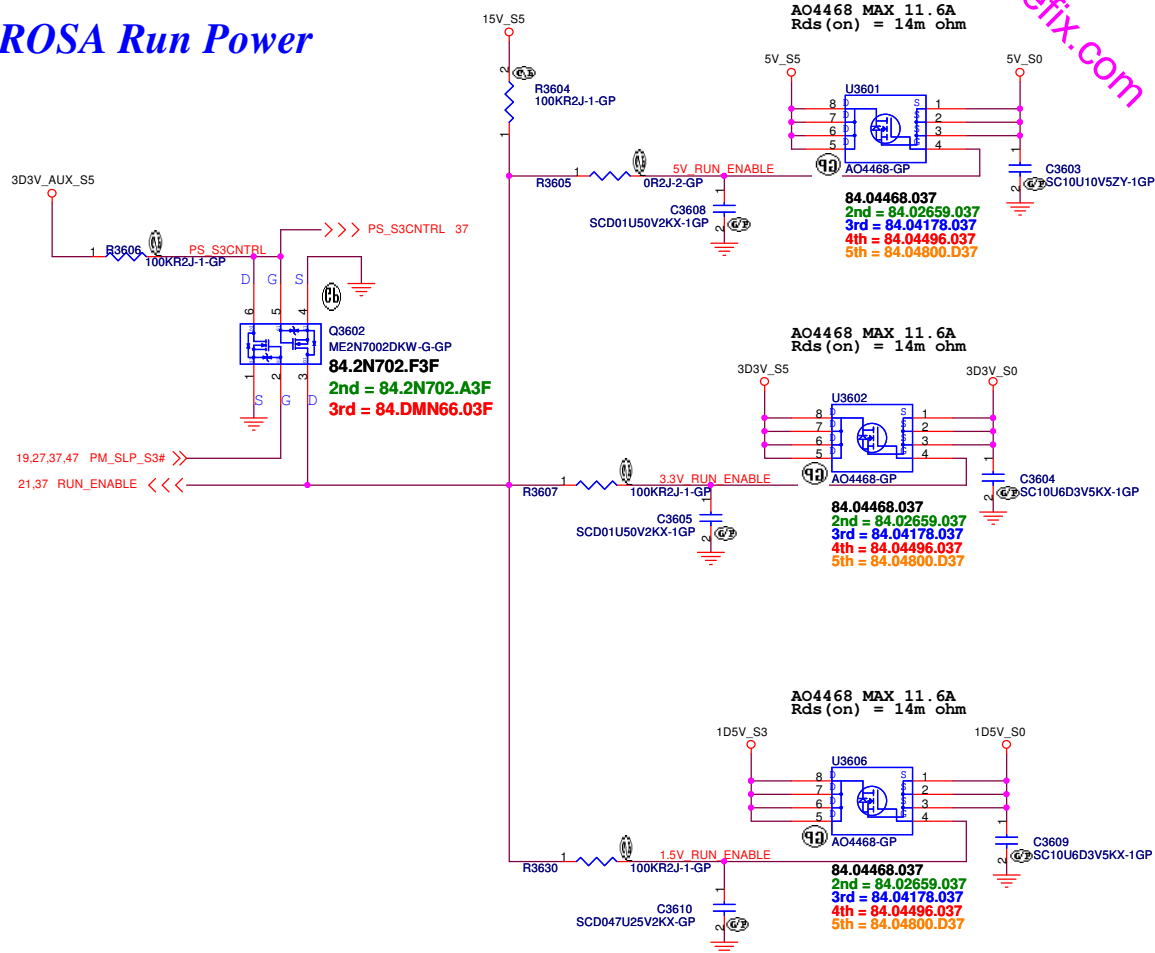


Title		
Reserved		
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A3	OAK14 Chief River DIS	A00
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SSID = Reset.Suspend



ROSA Run Power

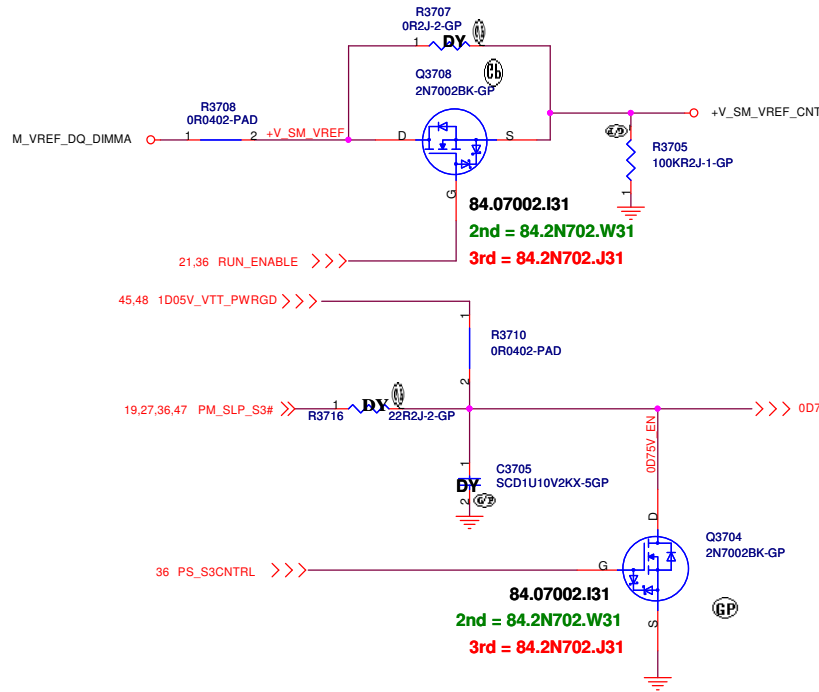


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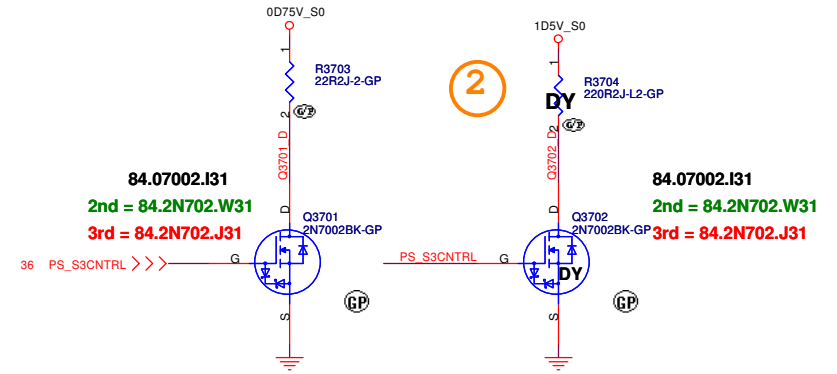
M14 DIS

		Wistron Corporation
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Power Plane Enable		
Size A3	Document Number	Rev
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**Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation**

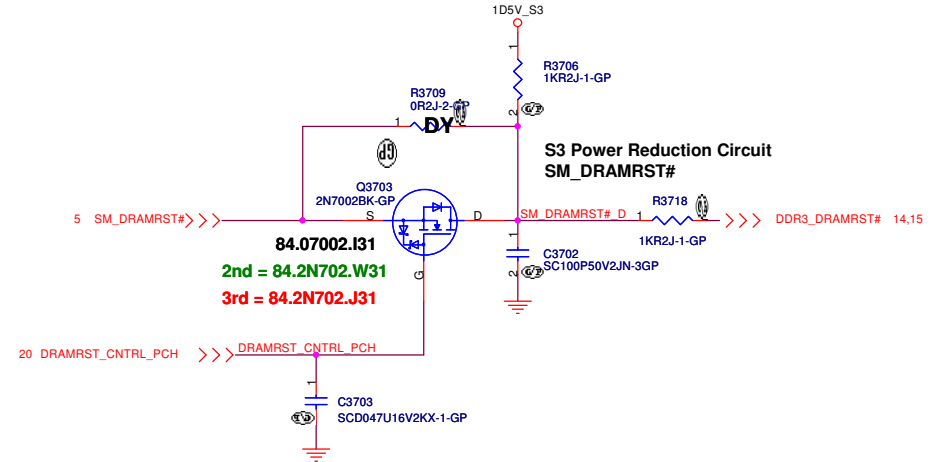


**Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK**

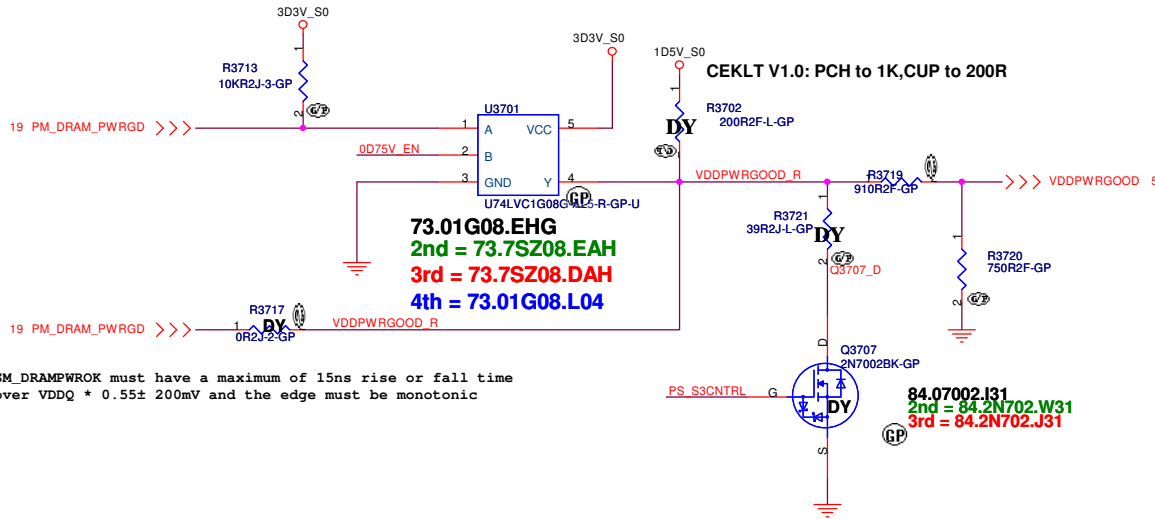


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**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



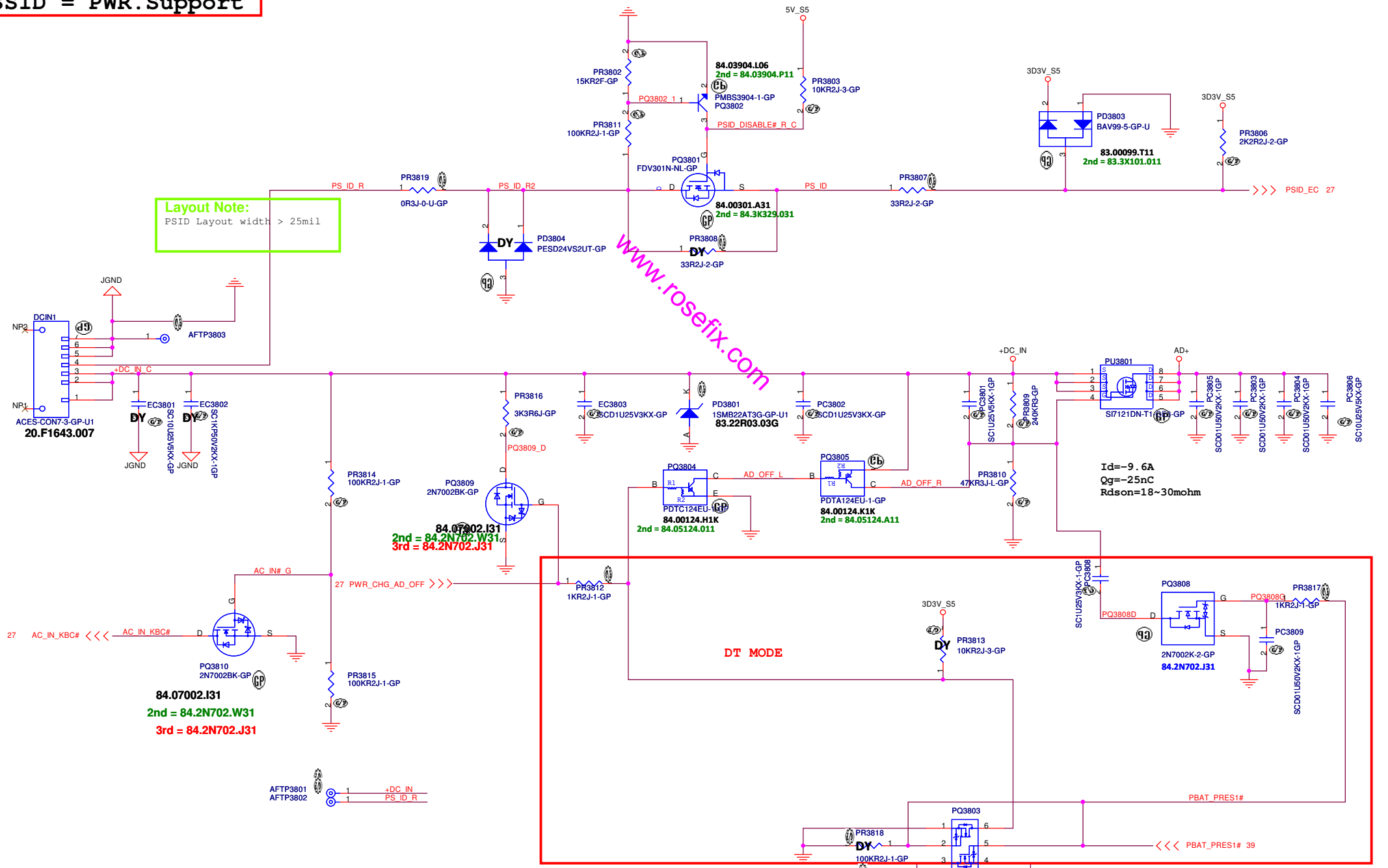
SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

M14 DIS

DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
S3 Reduction Circuit			
Size	Document Number	Rev	
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SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil



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$I_d = -9.6A$
 $Q_g = -25nC$
 $R_{dson} = 18 \sim 30m\Omega$

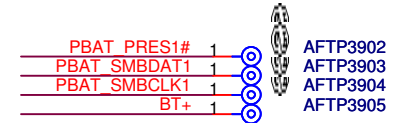
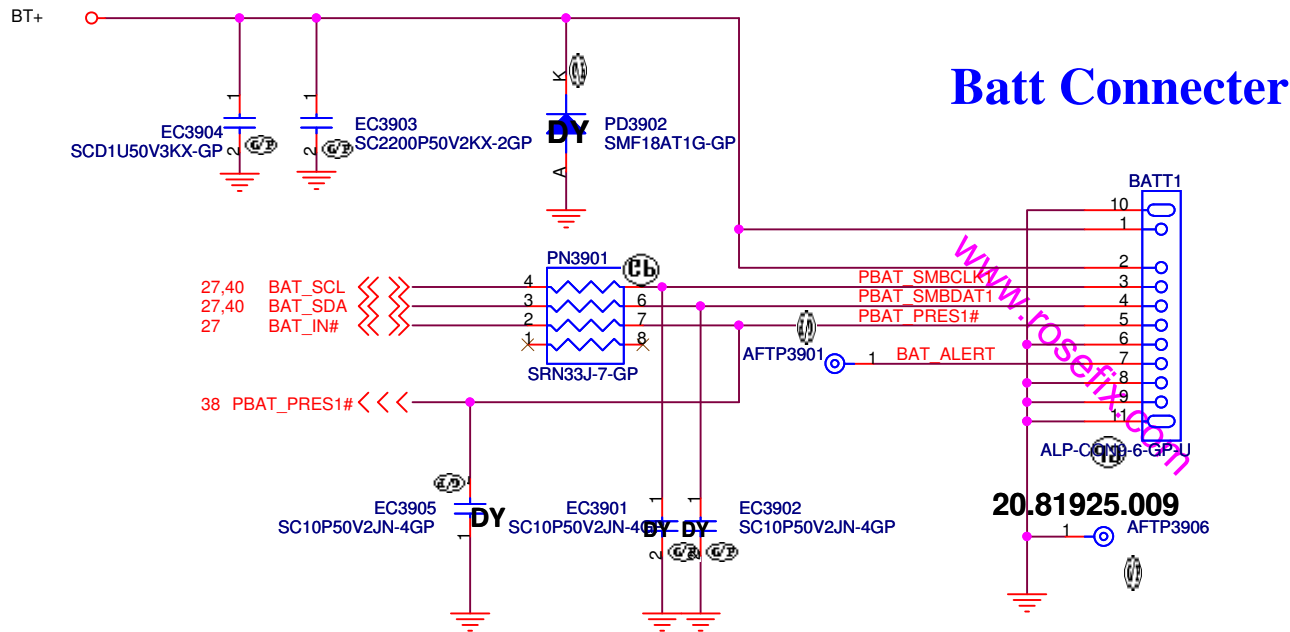
M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN**

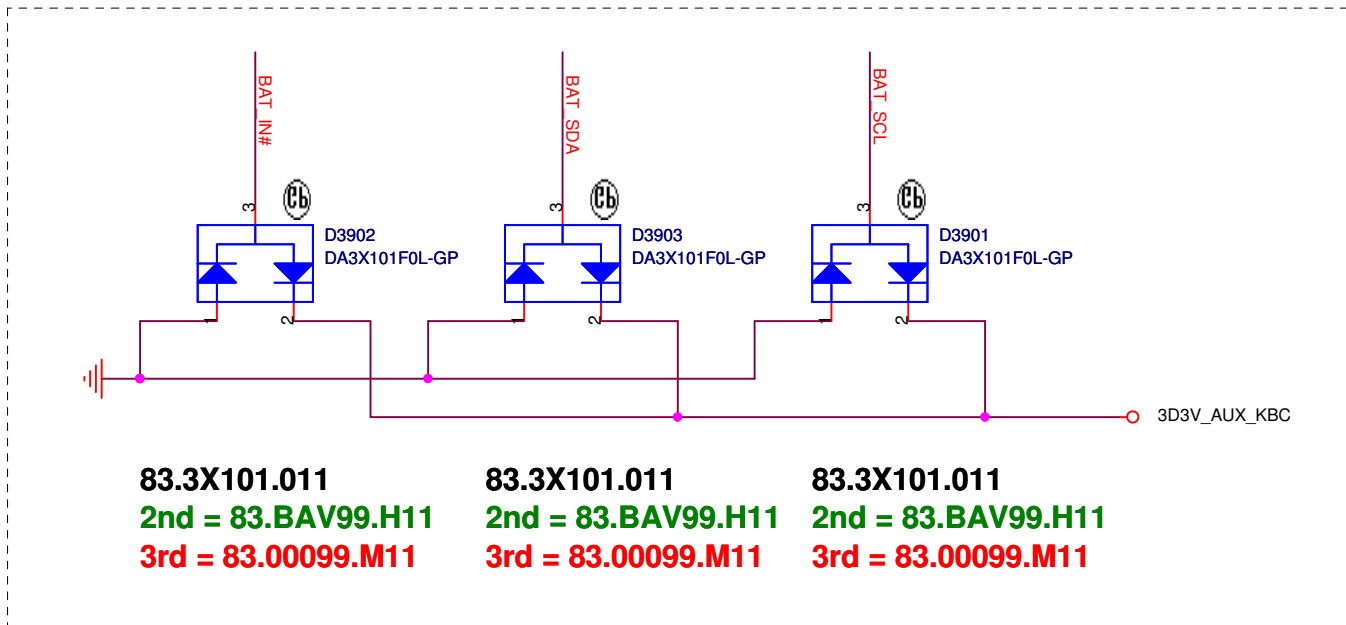
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
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SSID = PWR. Support



Batt Connector

Placement: Close to Batt Connector

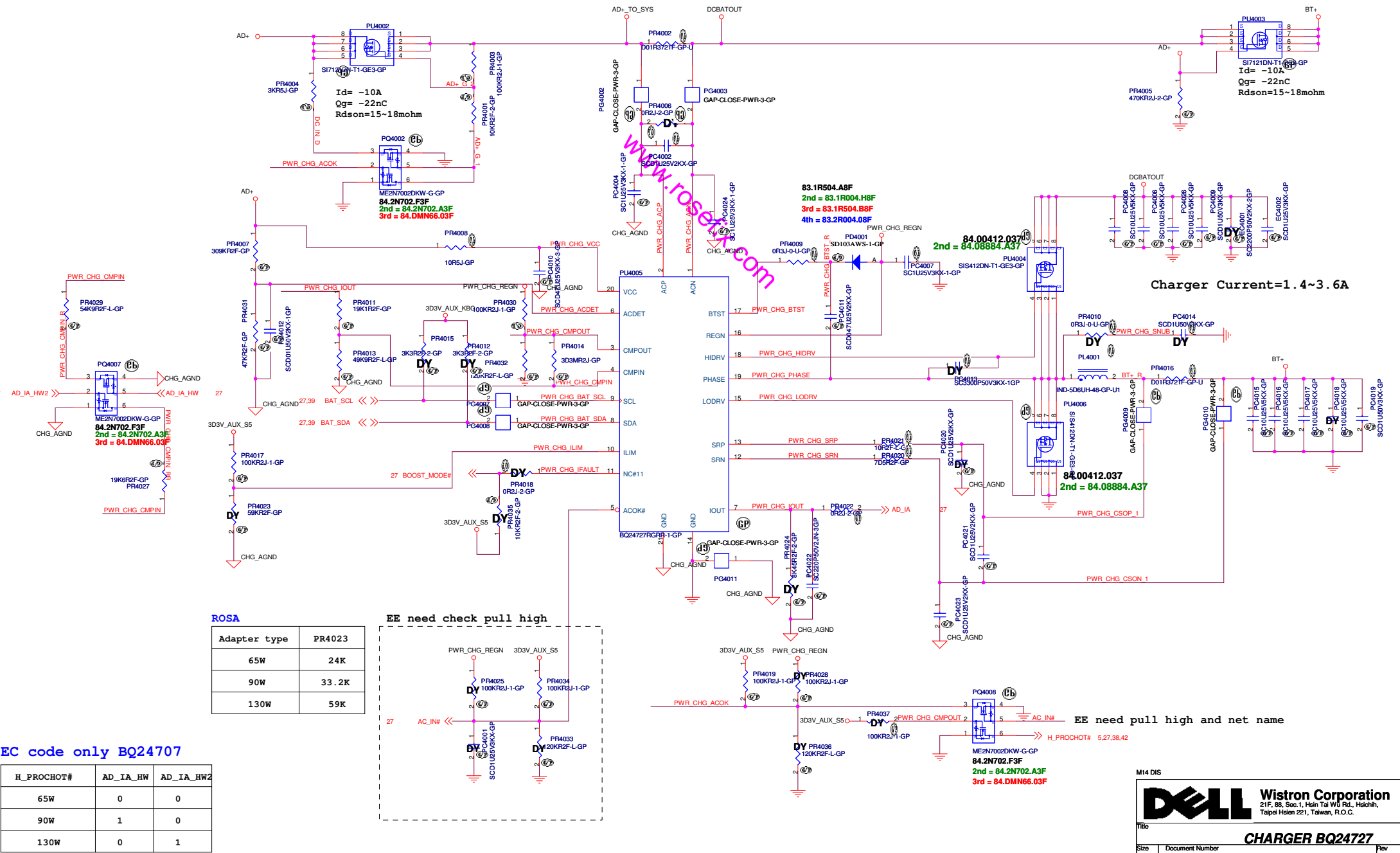


83.3X101.011	83.3X101.011	83.3X101.011
2nd = 83.BAV99.H11	2nd = 83.BAV99.H11	2nd = 83.BAV99.H11
3rd = 83.00099.M11	3rd = 83.00099.M11	3rd = 83.00099.M11

M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title: BATT CONN	
Size: A4	Document Number: OAK14 Chief River DIS	Rev: A00	
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SSID = Charger

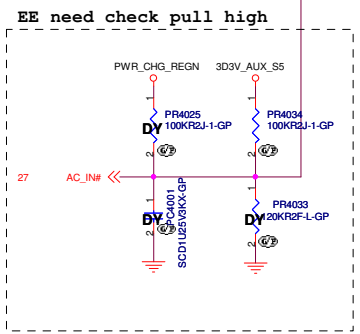


EC code only BQ24707

H_PROCHOT#	AD_IA_HW2	AD_IA_HW1
65W	0	0
90W	1	0
130W	0	1

ROSA

Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K



M14 DIS

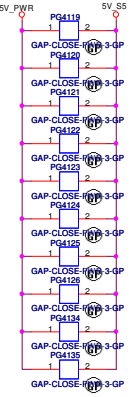
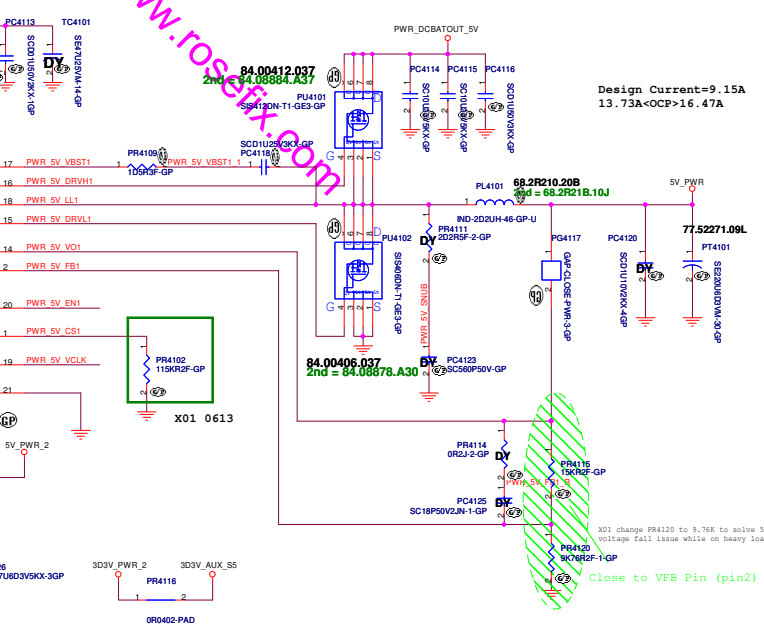
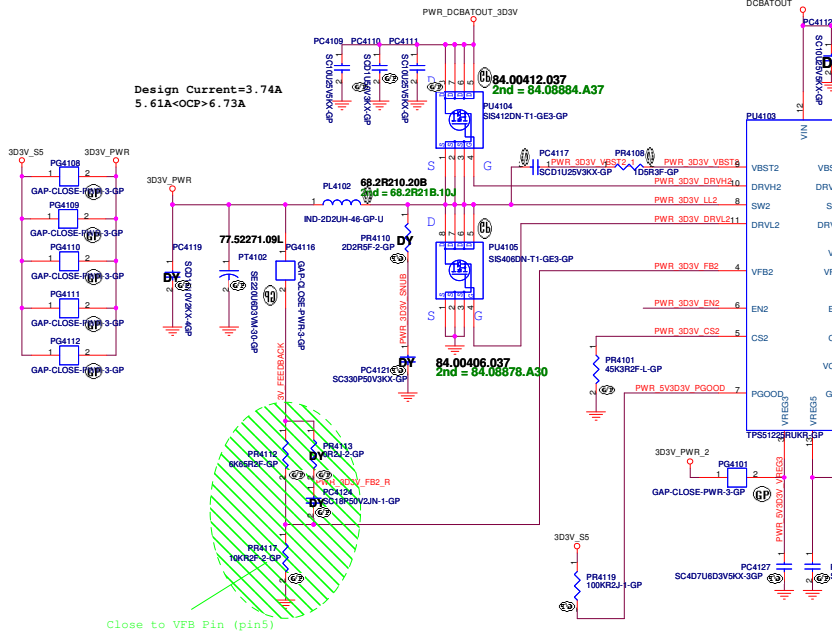
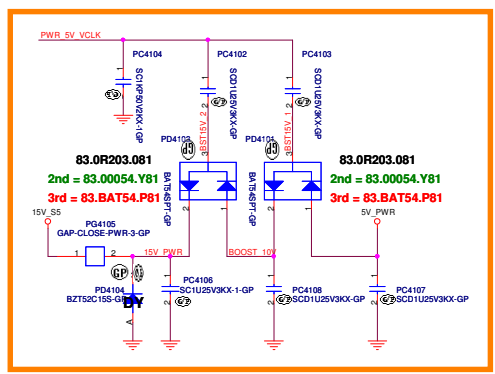
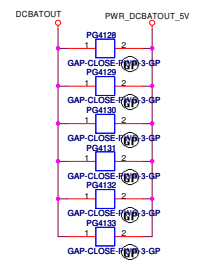
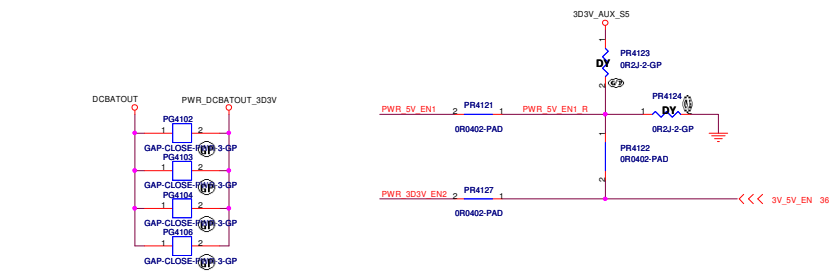
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wd Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **CHARGER BQ24727**

Size: Custom Document Number: **DNE40 14 CR DIS** Rev: **A00**

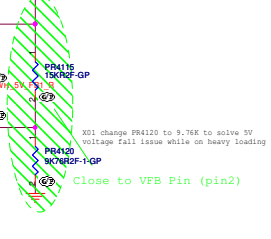
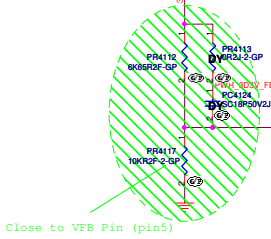
Date: Wednesday, September 05, 2012 Sheet 40 of 105

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=3.74A
5.61A<OCP>6.73A

Design Current=9.15A
13.73A<OCP>16.47A

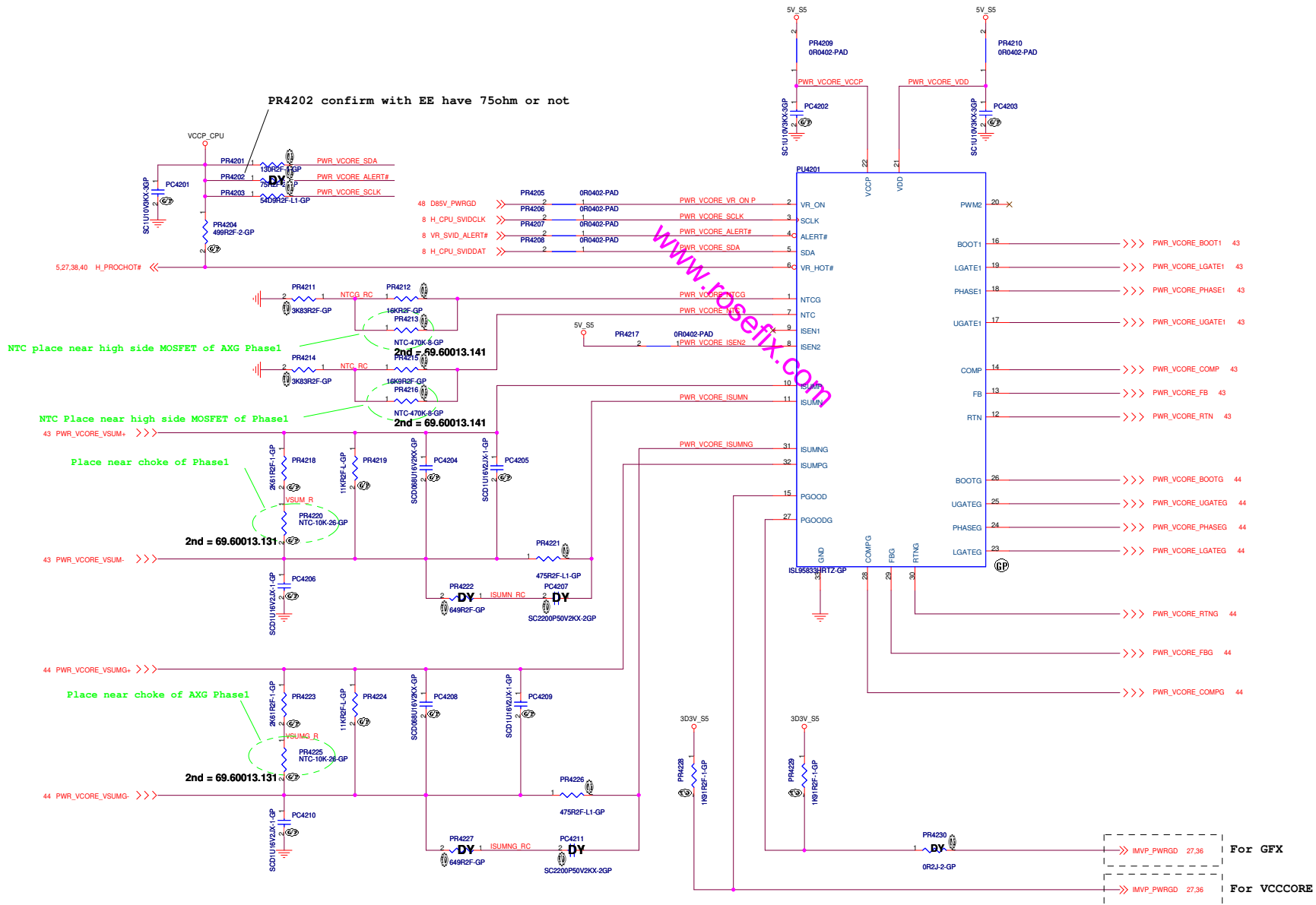


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mohm / 77.52271.09L
R/S: S1S412DN-T1-GE3 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: S1S406DN-T1-GE3 / 11.5mohm/14.5mohm@4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mohm / 77.52271.09L
R/S: S1S412DN-T1-GE3 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: S1S406DN-T1-GE3 / 11.5mohm/14.5mohm@4.5Vgs / 84.00406.037

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SSID = CPU.Regulator

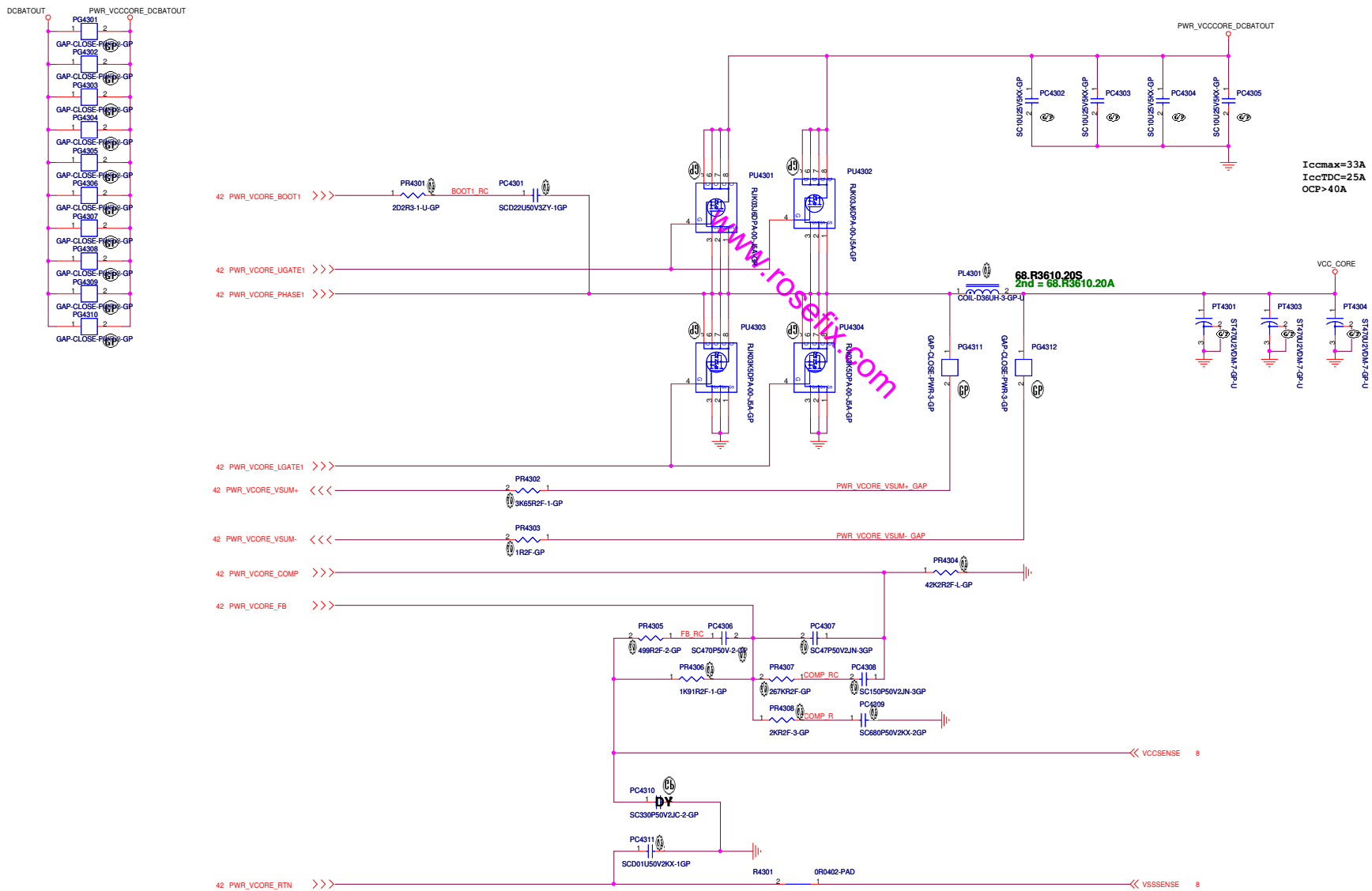


M14 DIS

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **ISL95833 CPU CORE(1/3)**
 Size C Document Number OAK14 Chief River DIS Rev A00

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Iccmax=33A
IccTDC=25A
OCP>40A

68.R3610.20S
2nd = 68.R3610.20A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
 O/P cap: CHIP CAP EL 470U 2V 7.3*4.3 ESR=0.0045 3.8Arms Panasonic/79.47719.9BL
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K5DPA-00#J5A / 3mohm/3.9mOhm@4.5Vgs/ 84.00035.037

M14 DIS

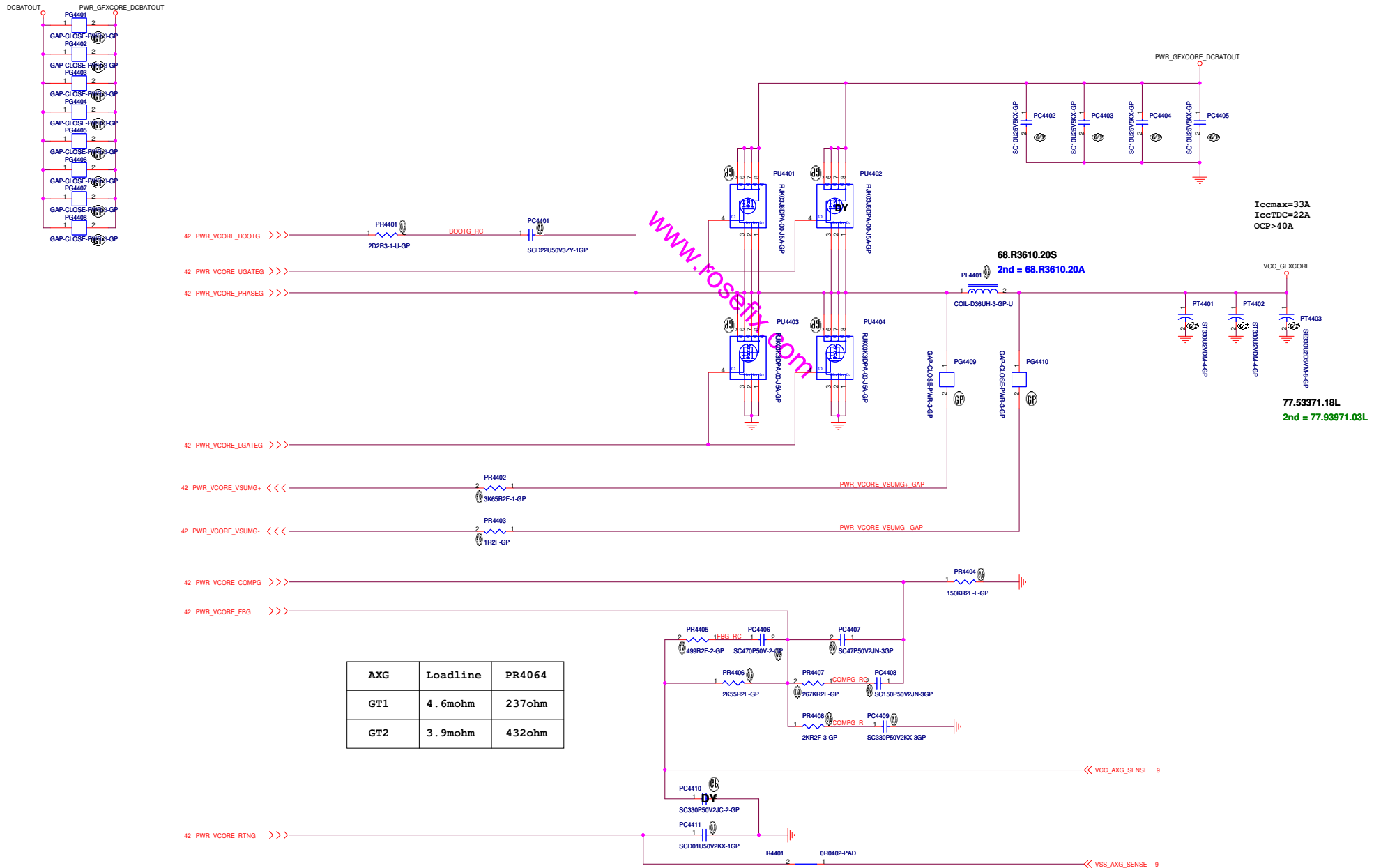
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95833 CPU CORE(2/3)**

Size	Document Number	Rev
C	OAK14 Chief River DIS	A00

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SSID = CPU.Regulator



Iccmax=33A
IccTDC=22A
OCP>40A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
 O/P cap: CHIP CAP 330U 2V BFPX0D331XE 3.5Arms Panasonic/79.33719.20L
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

M14 DIS

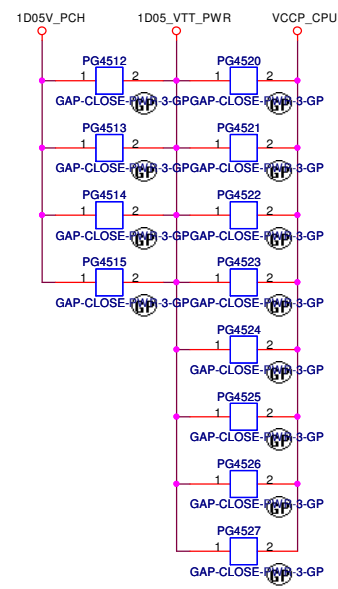
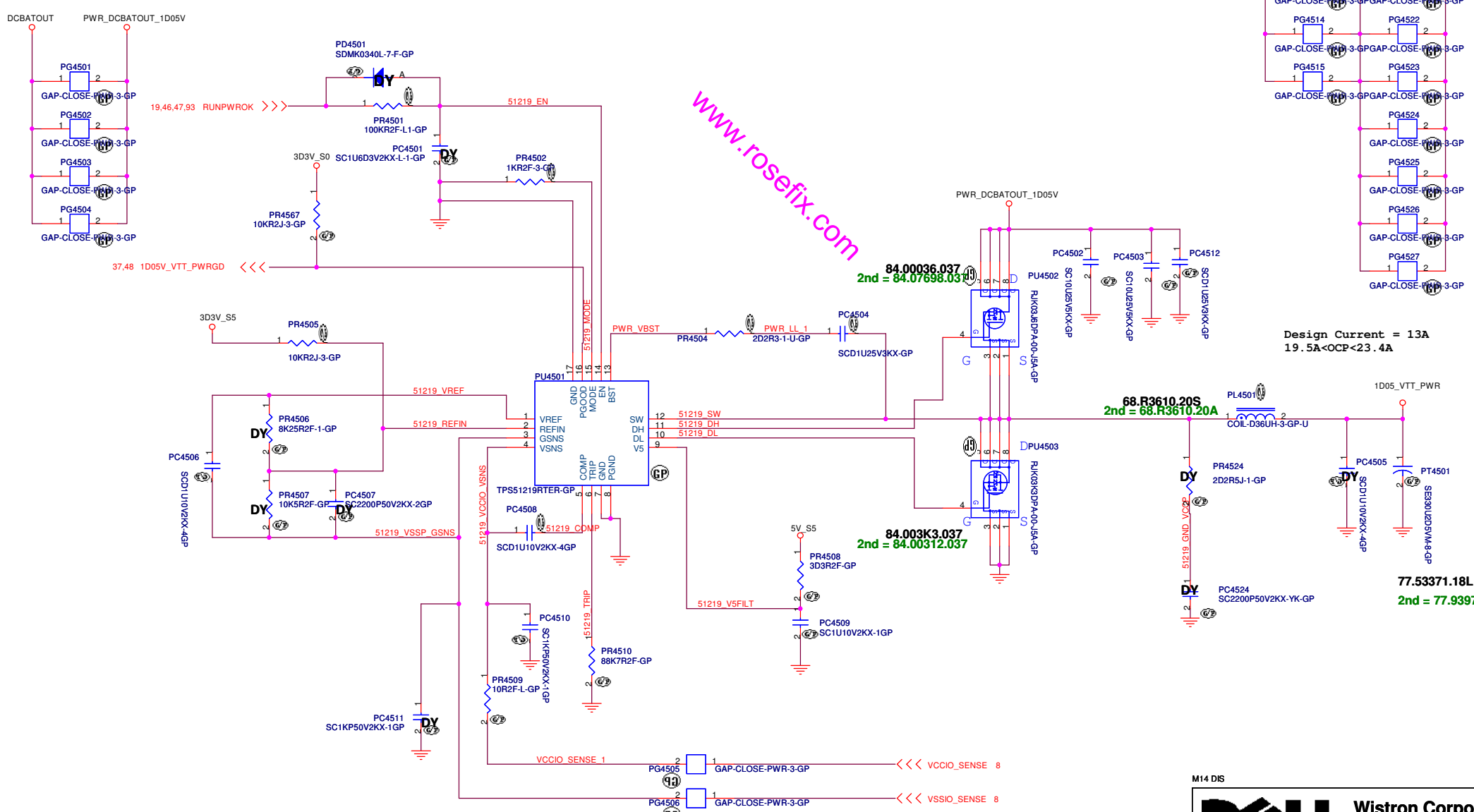
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95833 CPU CORE(3/3)**

Size: C Document Number: OAK14 Chief River DIS Rev: A00

Date: Wednesday, September 05, 2012 Sheet: 44 of 105

TPS51219 for 1D05V_VTT



Design Current = 13A
19.5A < OCP < 23.4A

84.00036.037
2nd = 84.07698.037

84.003K3.037
2nd = 84.00312.037

68.R3610.20S
2nd = 68.R3610.20A

77.53371.18L
2nd = 77.93971.03L

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

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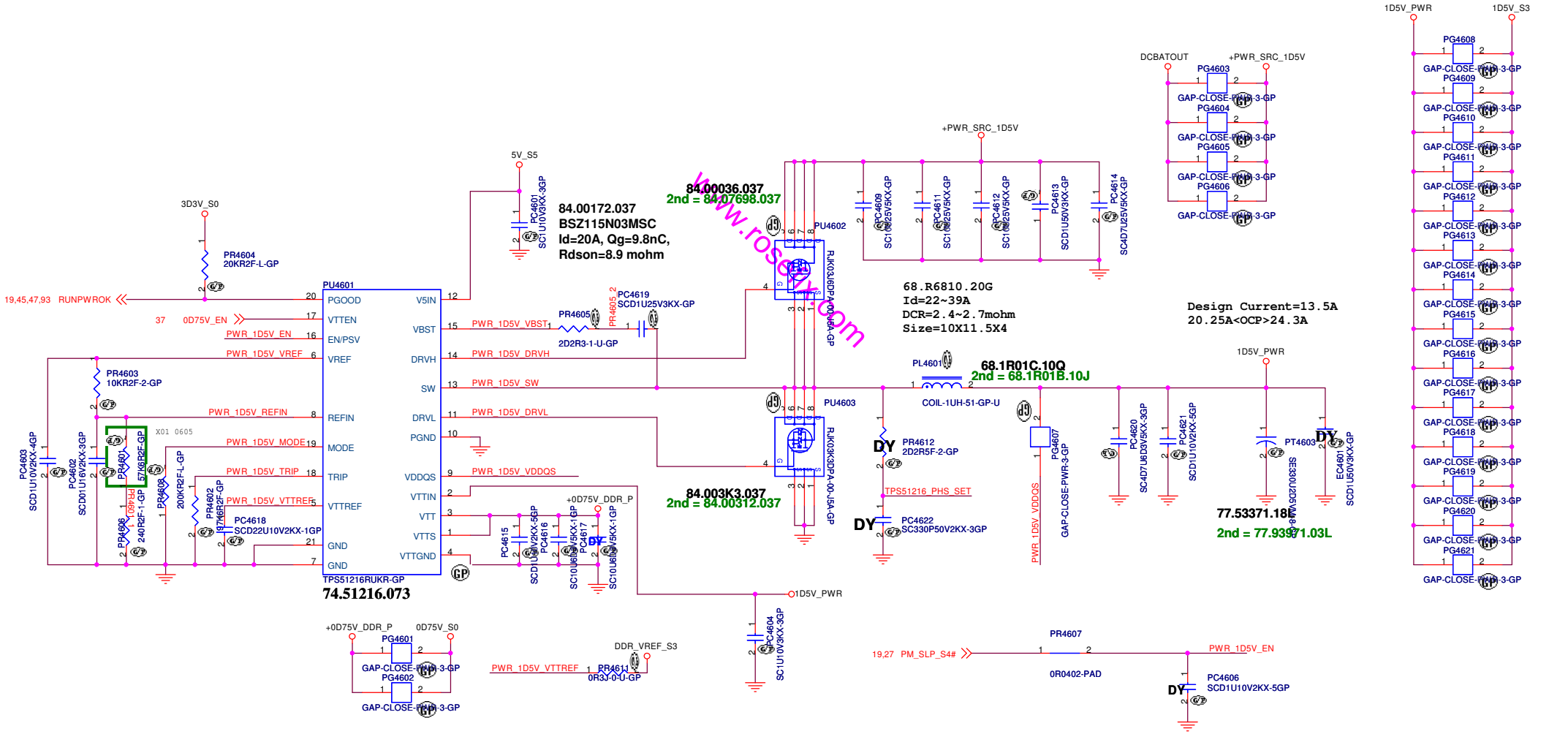
M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51219 1D05V_VTT**

Size A3	Document Number DNE40 14 CR DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 45	of 105

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

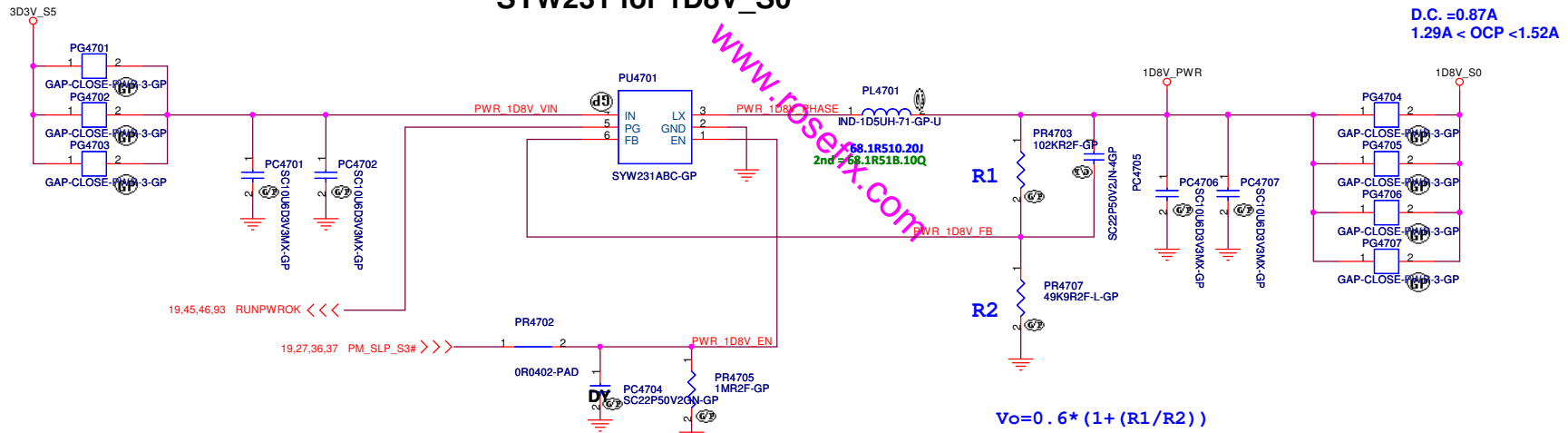
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10J
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

M14 DIS



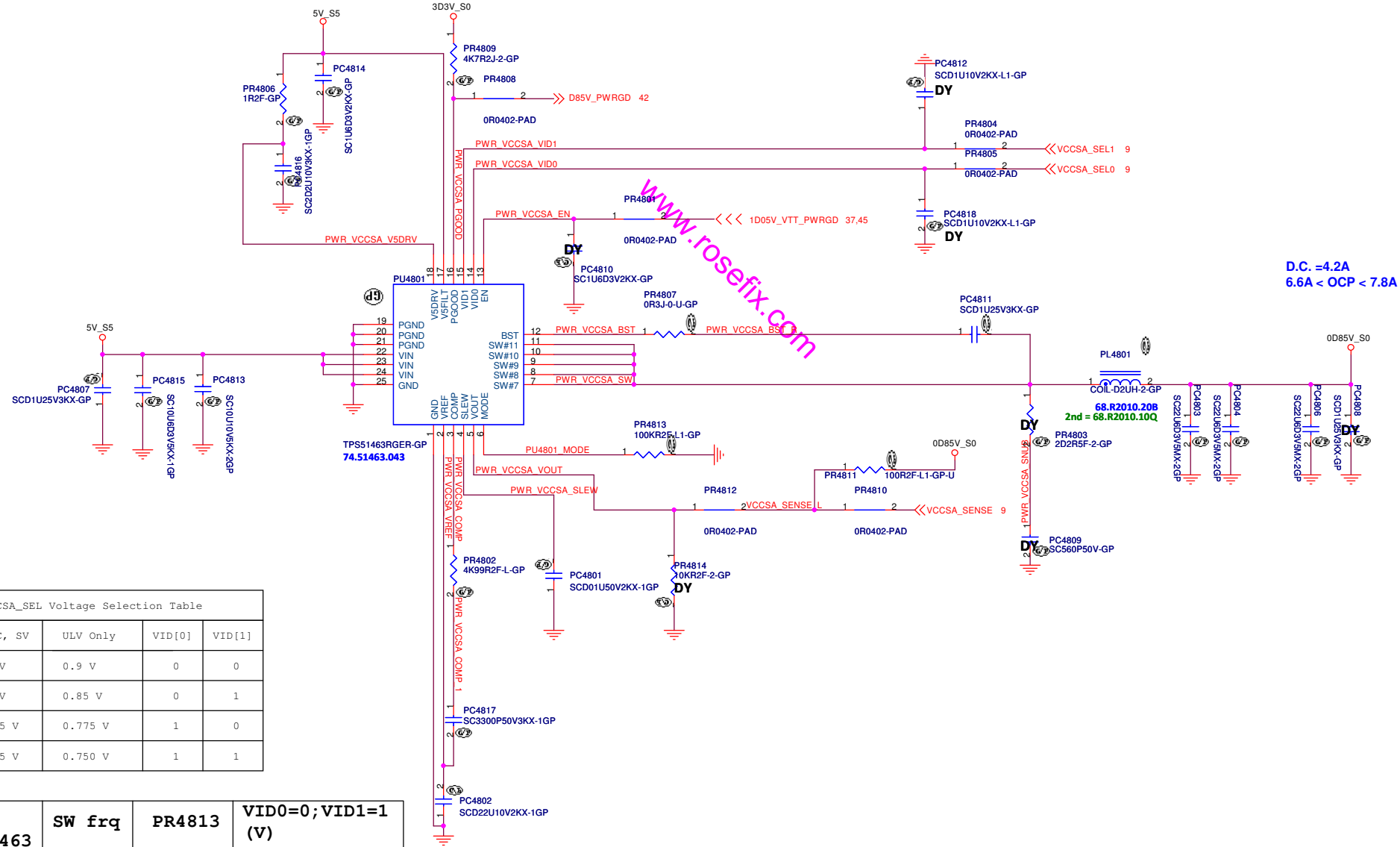
Title TPS51216 +1.5V SUS		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
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SYW231 for 1D8V_S0



M14 DIS

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SYW231 1D8V S0			
Size	Document Number	Rev	
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D.C. =4.2A
6.6A < OCP < 7.8A

XE, QC, SV	ULV Only	VID[0]	VID[1]
0.9 V	0.9 V	0	0
0.8 V	0.85 V	0	1
0.725 V	0.775 V	1	0
0.675 V	0.750 V	1	1

TPS51463 for ULV	SW frq	PR4813	VID0=0; VID1=1 (V)
	700KHz	100K	0.85
	1MHz	Open	0.85

M14 DIS

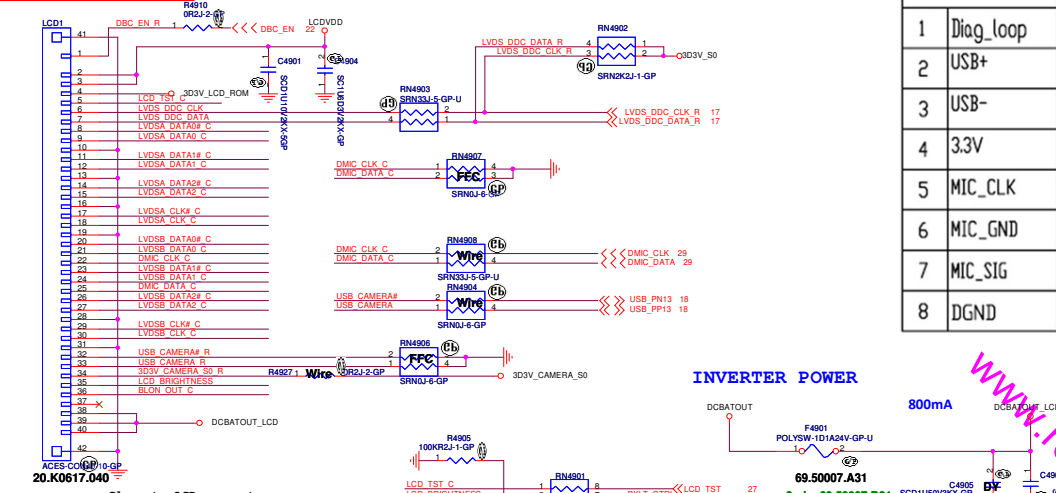
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51463 VCCSA**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00

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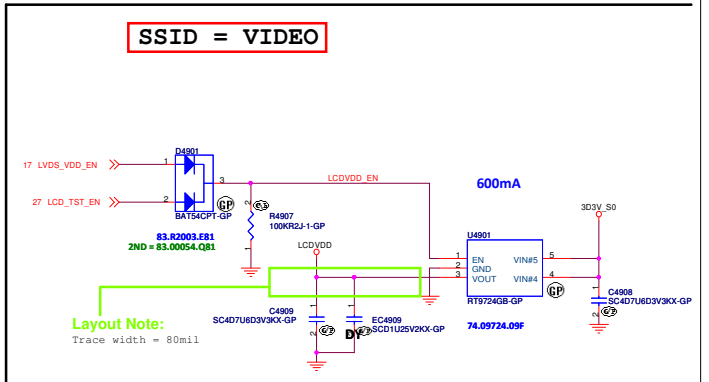
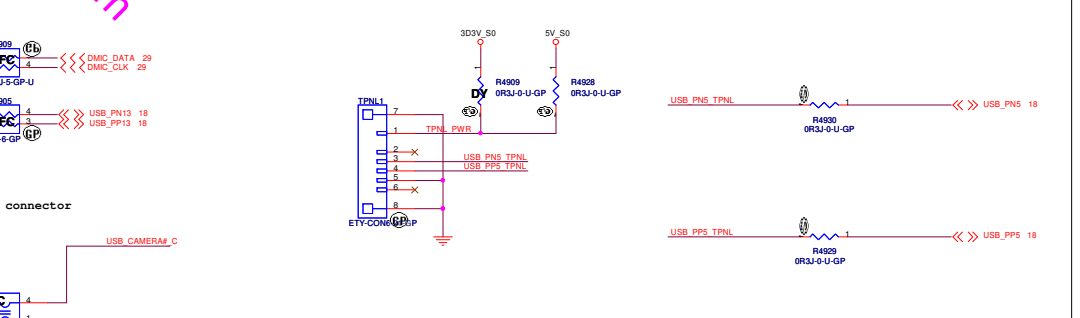
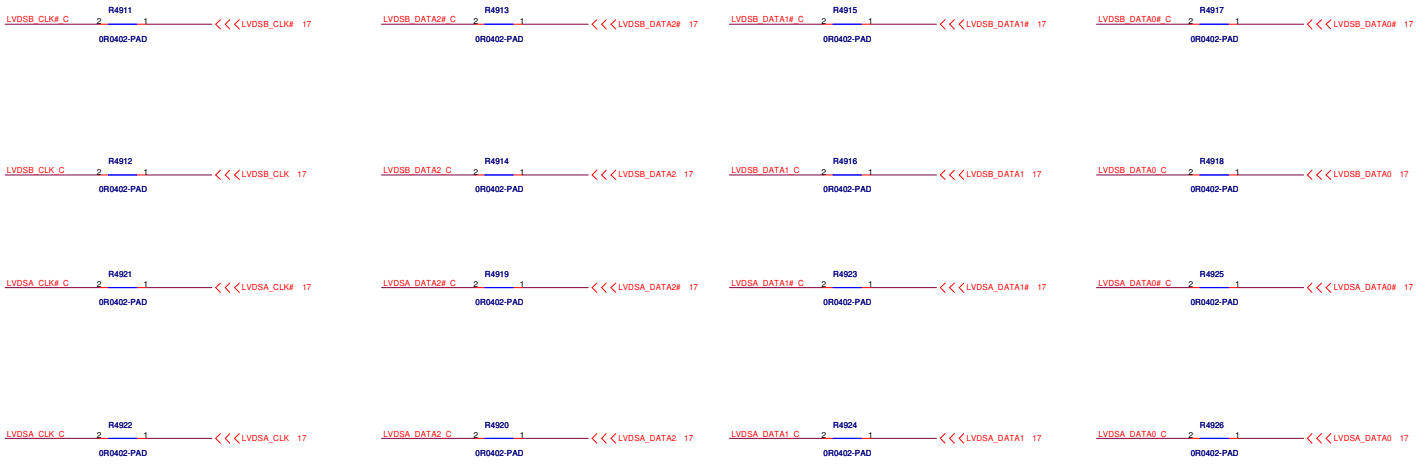
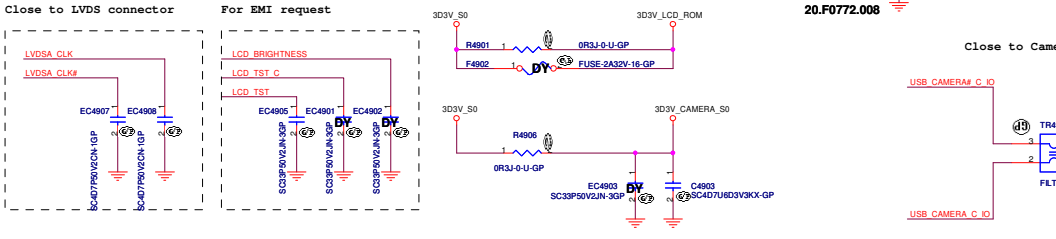
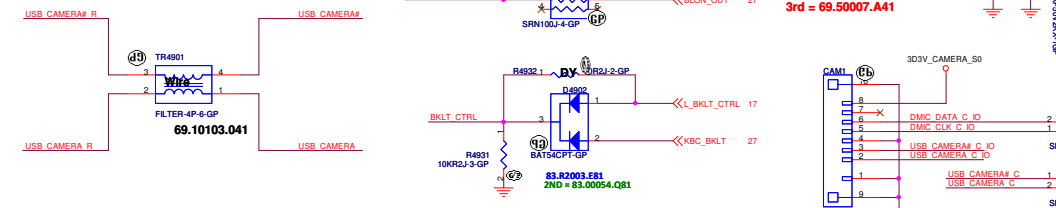
SSID = VIDEO



CN Table	
1	Diag_loop
2	USB+
3	USB-
4	3.3V
5	MIC_CLK
6	MIC_GND
7	MIC_SIG
8	DGND

MB Connector	是否接線	Wire (40 PIN)	FFC(40 PIN)
Pin 10	GND	Y	Pin 10(GND 實體線)
Pin 13	GND	Y	Pin 13(GND 實體線)
Pin 16	GND	Y	Pin 16 (GND實體線)
Pin 19	GND	Y	Camera Module Pin 6 DMIC_GND(實體線)
Pin 22	GND	Y	Camera Module Pin 5 AUD_DMIC_CLK
Pin 25	GND	Y	Camera Module Pin 7 AUD_DMIC_IN0
Pin 28	GND	Y	Camera Module Pin 8 CCD_GND(實體線)
Pin 31	GND	Y	Pin 31 (實體線)
Pin 32	GND	Y	Camera Module Pin 3 USB_CAMERA#
Pin 33	GND	Y	Camera Module Pin 2 USB_CAMERA
Pin 34	3D3V_CAMERA_S0	Y	Camera Module Pin 4 3D3V_CAMERA_S0

PIN	MB Connector	是否接線	PIN	Camera Module Conn
1	DGND	Y	8	DGND
2	USB_CAMERA_C (USB+)	Y	2	USB_CAMERA_C (USB+)
3	USB_CAMERA#_C (USB-)	Y	3	USB_CAMERA#_C (USB-)
4	DMIC_GND	Y	6	DMIC_GND
5	DMIC_CLK_C	Y	5	DMIC_CLK_C
6	DMIC_DATA_C	Y	7	DMIC_DATA_C
7	NC	N	1	NC
8	3D3V_CAMERA_S0	Y	4	3D3V_CAMERA_S0



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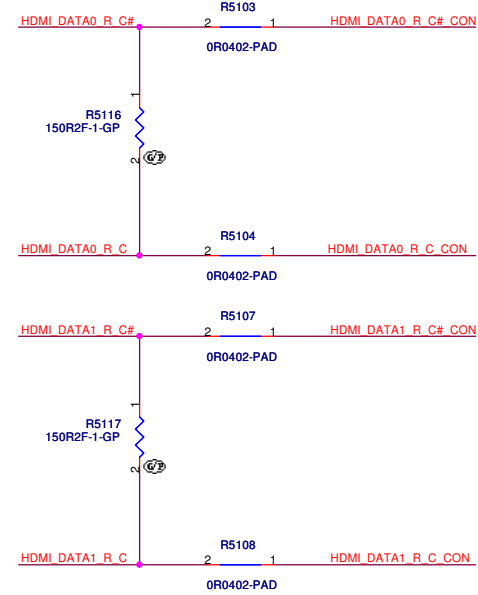
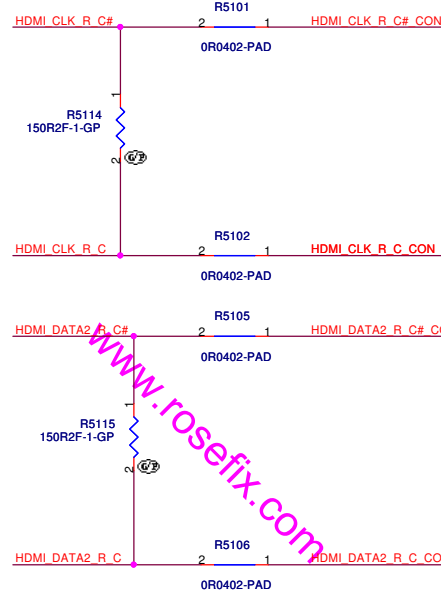
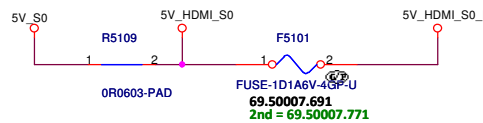
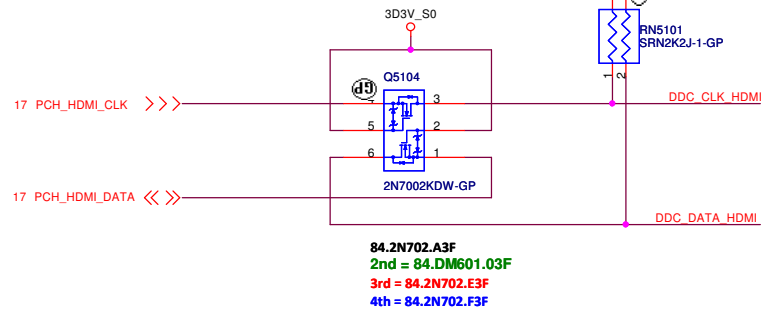
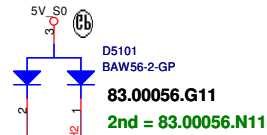
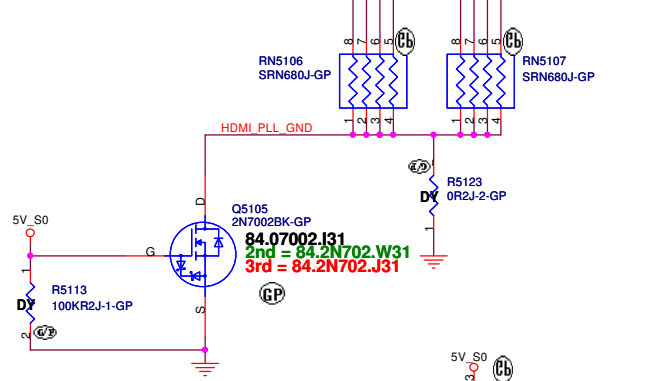
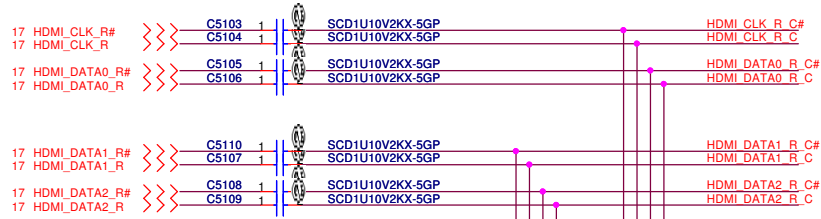
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M14 DIS

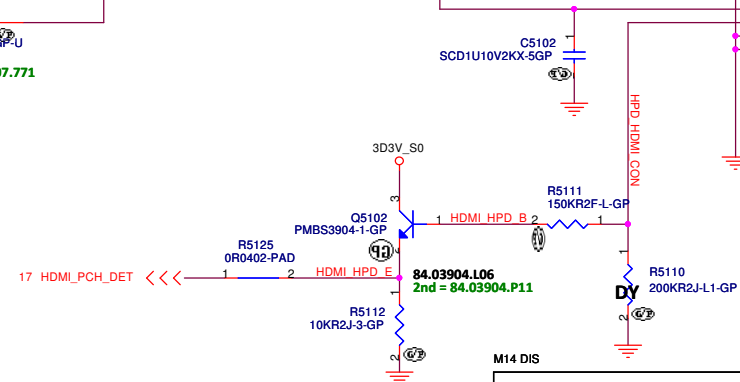
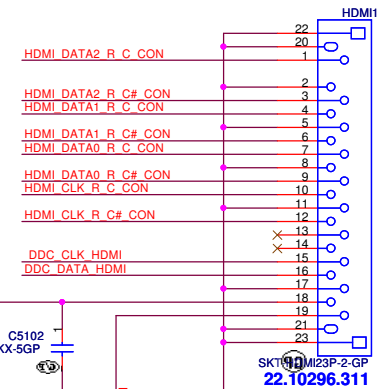
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Title					
CRT Connector					
Size	Document Number				Rev
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SSID = VIDEO

HDMI Level Shifter



HDMI CONN



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title HDMI Level Shifter/Connector	
Size A3	Document Number OAK14 Chief River DIS	Rev A00	
Date: Wednesday, September 05, 2012	Sheet 51	of 105	

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M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
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M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 53 of 105

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M14 DIS

	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
---	--

Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		
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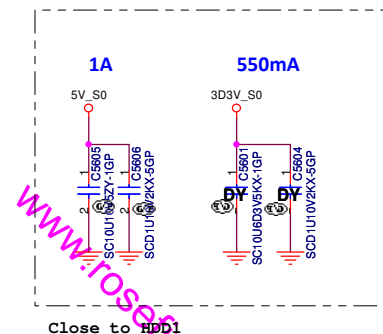
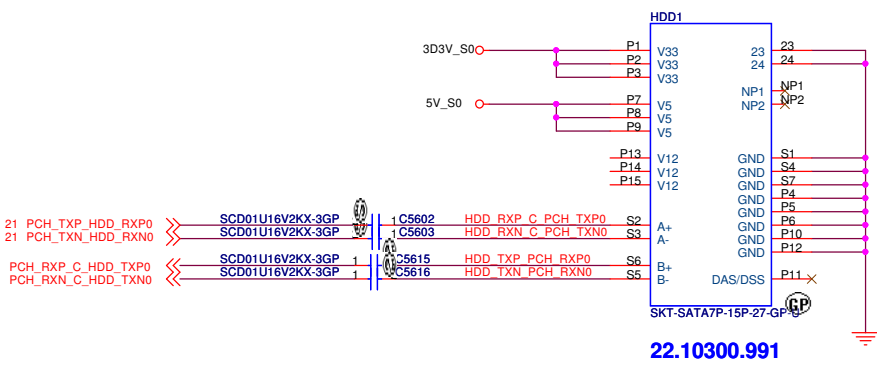
SSID = User.Interface

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(Blanking)

M14 DIS

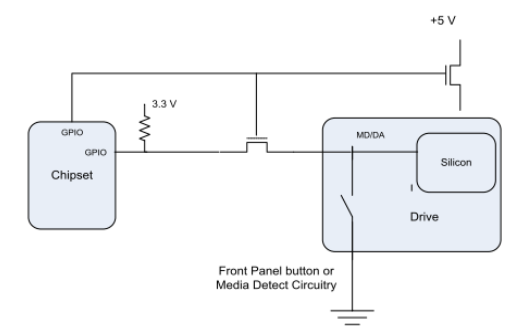
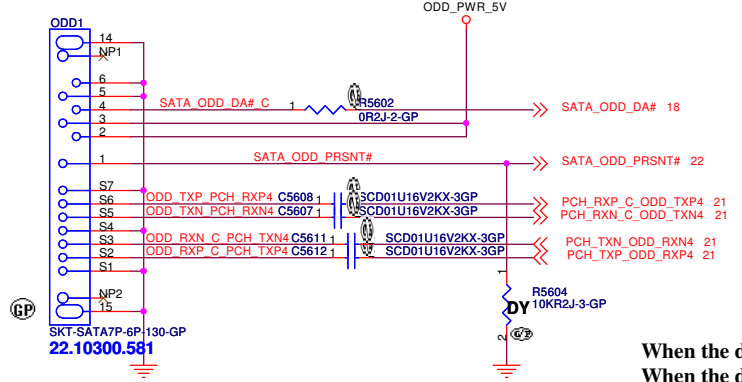
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Title		
ITP/Fan Connector		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
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SATA HDD Connector

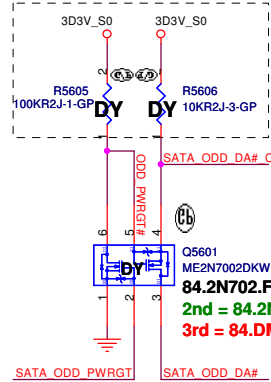


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ODD Connector

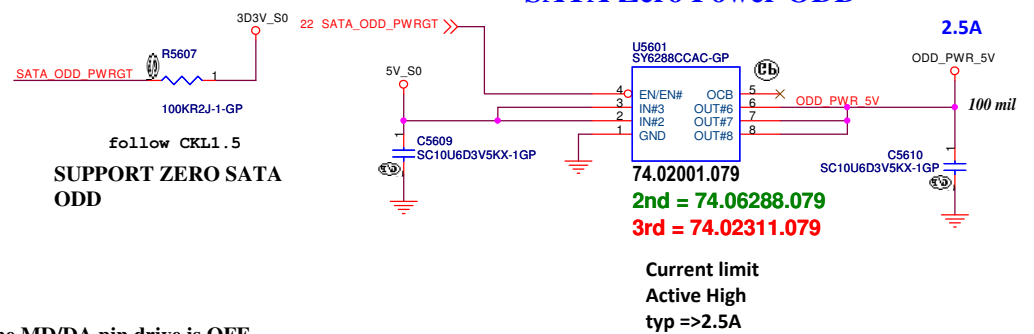


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
 When the drive is powered off, the FET to the MD/DA pin is ON



A00-0408 Add R5606 to pull high 3.3V_S0
 Change pull high to 3.3V_S0
 A00-0415 Dummy R5606

SATA Zero Power ODD



SSID = ESATA

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M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		ESATA
Size A3	Document Number OAK14 Chief River DIS	Rev A00
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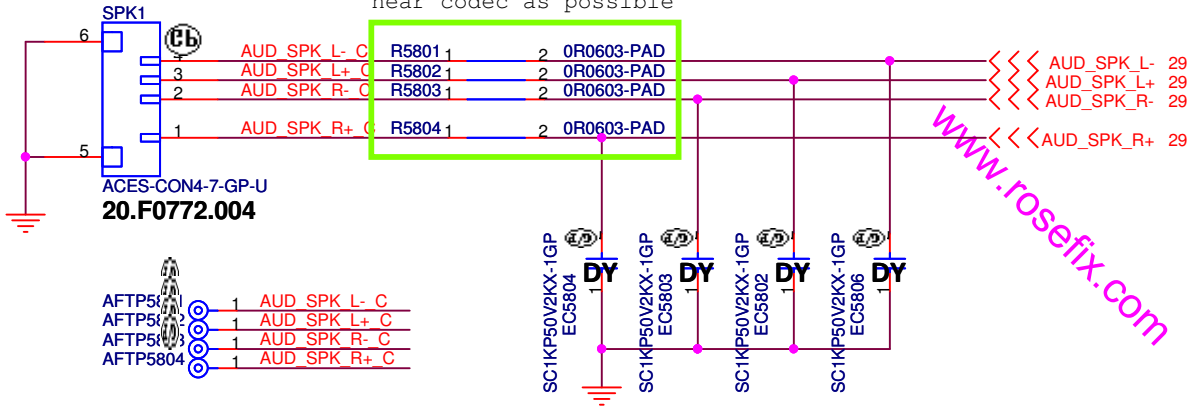
SSID = AUDIO

Speaker

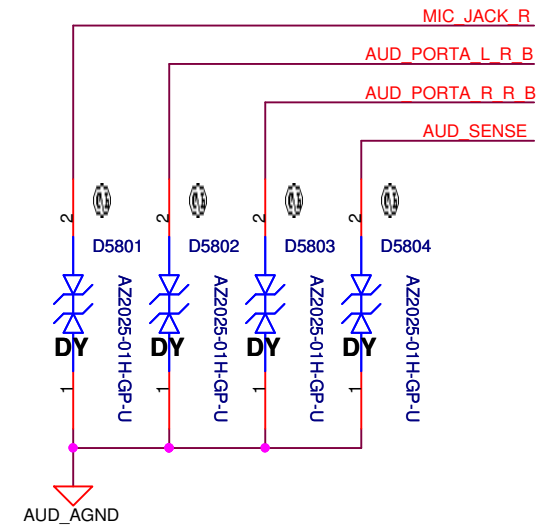
Layout Note:

trace width=30mil

R5801~R5804 and EC5804~EC5806 near codec as possible

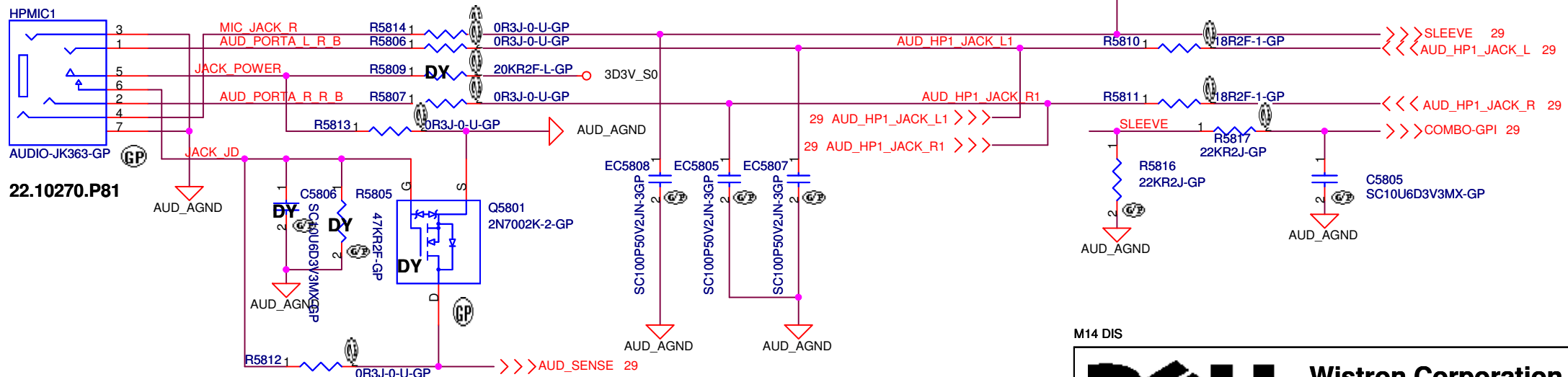


X01 0605



Combo Jack

change to 22.10270.P81, but symble not change



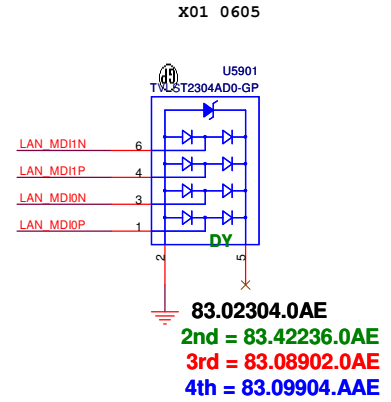
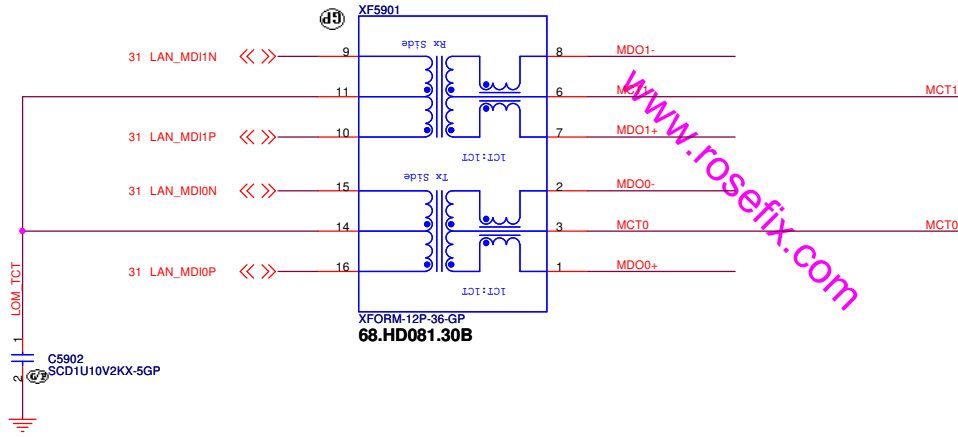
M14 DIS



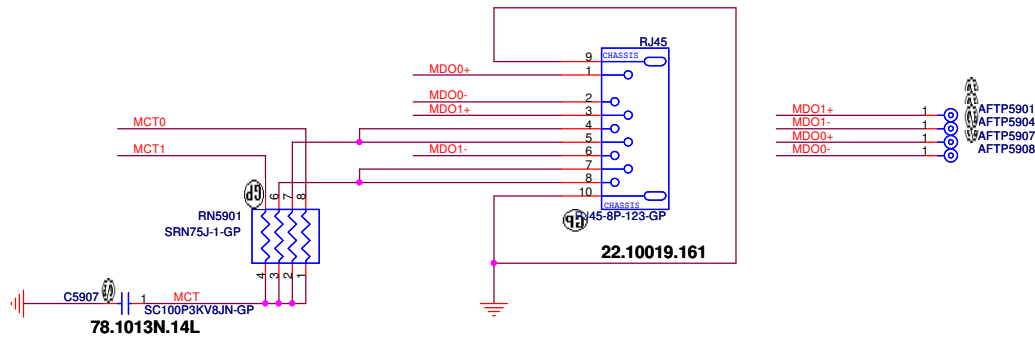
Title Speaker/HPMIC CONN		
Size A4	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012 Sheet 58 of 105		

SSID = LOM

LAN TransFormer



RJ45



<Core Design>

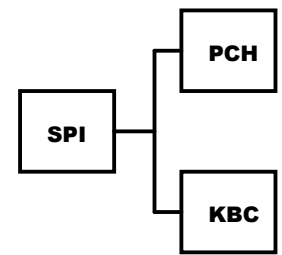
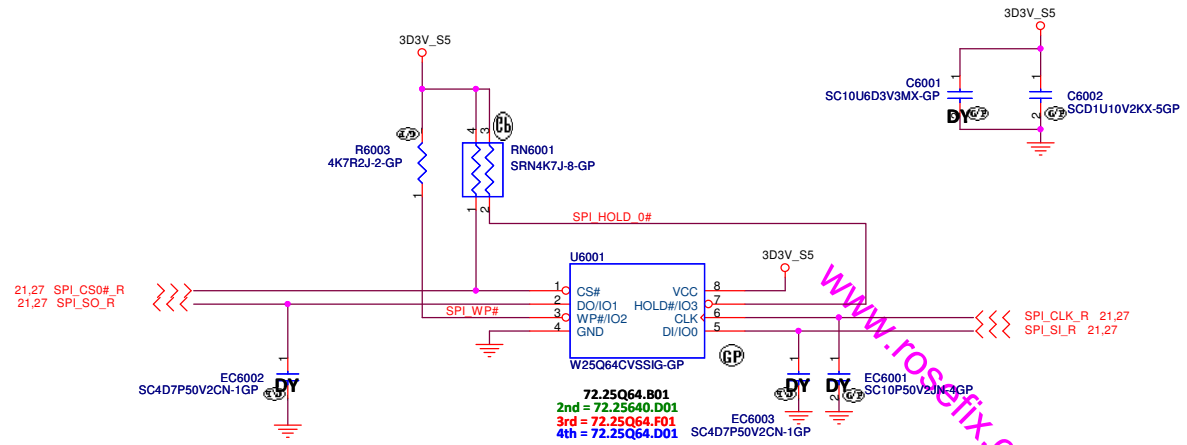
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **XFOM&RJ45**

Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012		Sheet 59 of 105

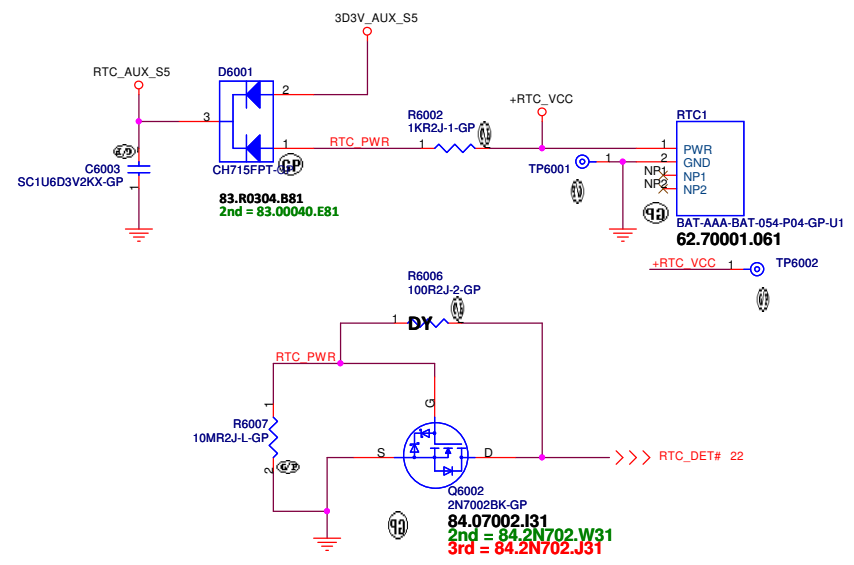
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



Layout Note:
 KBC---10"---PCH
 KBC---1.5"~6.5"---SPI
 PCH---0.5"~6.5"---SPI

SSID = RBATT

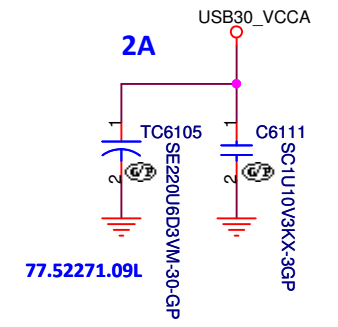
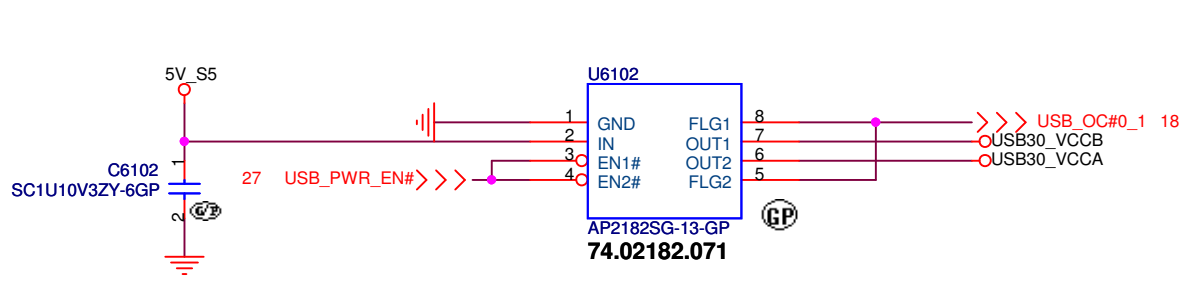


M14 DIS

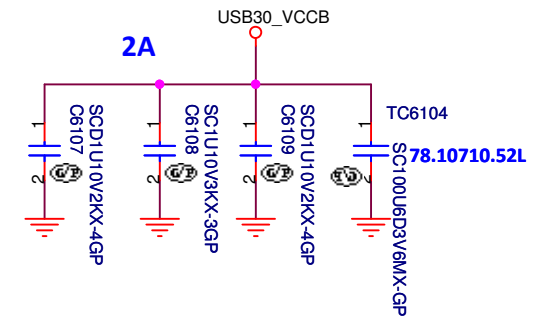
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00
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USB3.0 Port1

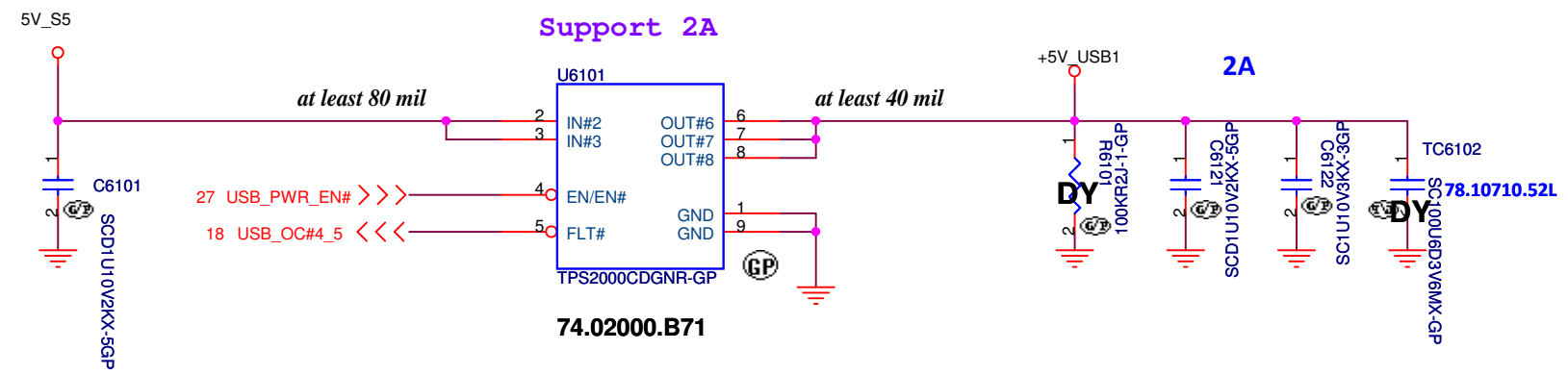


USB3.0 Port2


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Right USB Power x1

Support 2A

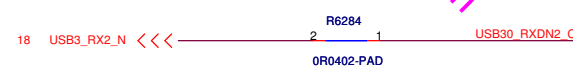
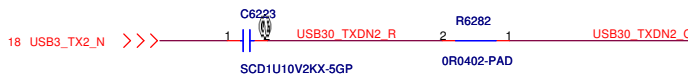
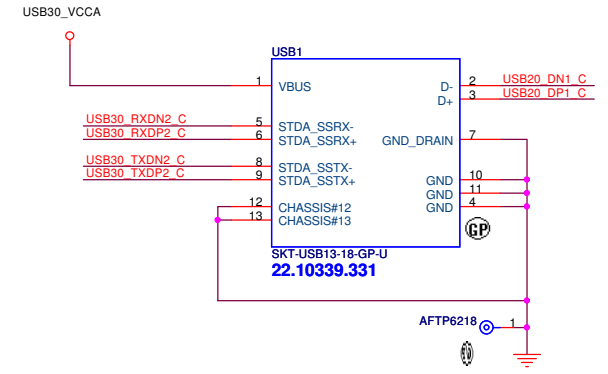
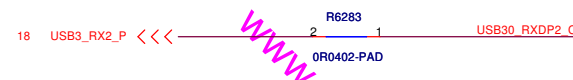
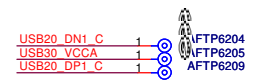
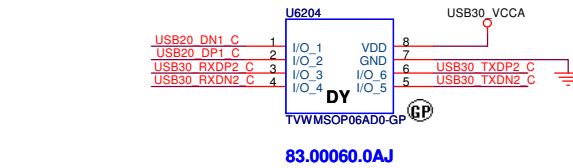
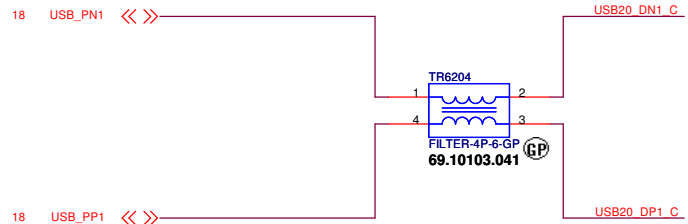


M14 DIS

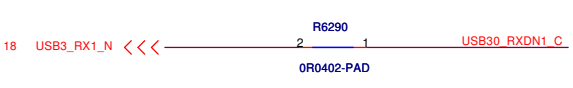
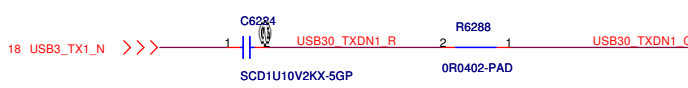
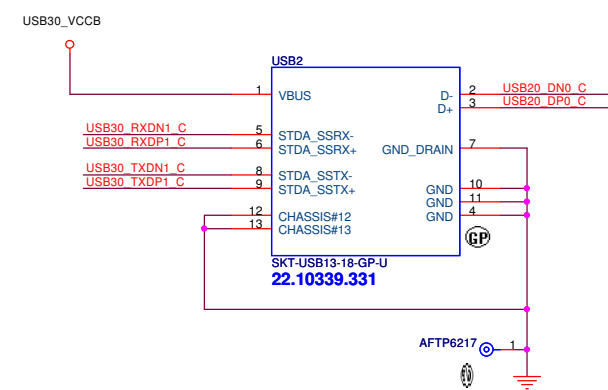
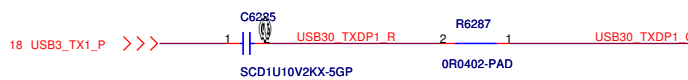
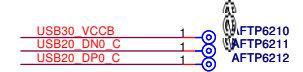
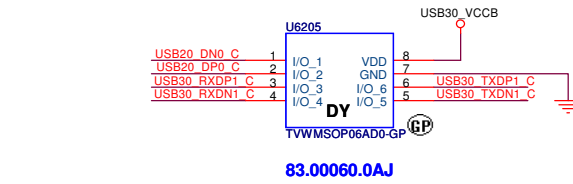
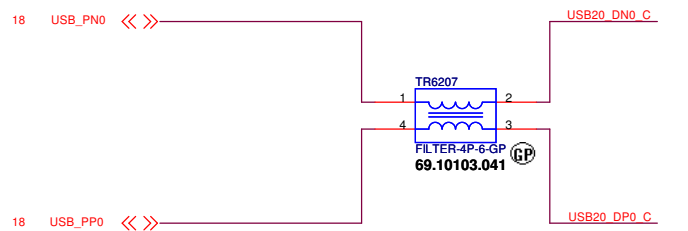
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <p style="text-align: center;">USB Power SW</p>	
Size	Document Number	Rev	
OAK14 Chief River DIS		A00	
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SSID = USB

USB3.0 Port1



USB3.0 Port2



M14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0**


Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012		
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SSID = USB

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M14 DIS

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Title		
USB3.0 PORT		
Size	Document Number	Rev
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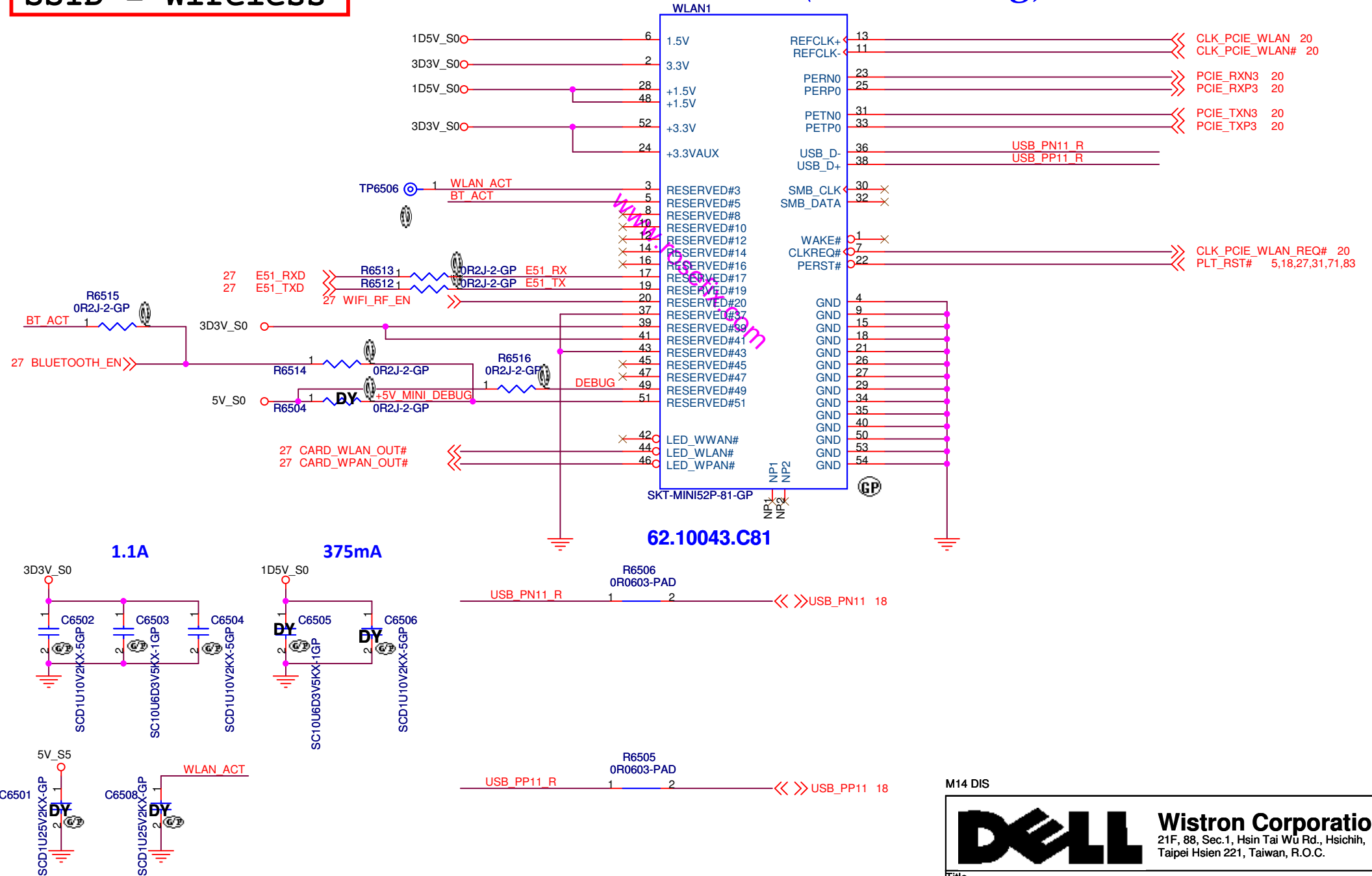
M14 DIS



Title		
RESERVED		
Size	Document Number	Rev
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SSID = Wireless

Mini Card Connector(802.11a/b/g)



M14 DIS



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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title MINICARD(WLAN)/ITP CONN		
Size A4	Document Number OAK14 Chief River DIS	Rev A00
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M14 DIS



Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		
Sheet 66 of 105		1

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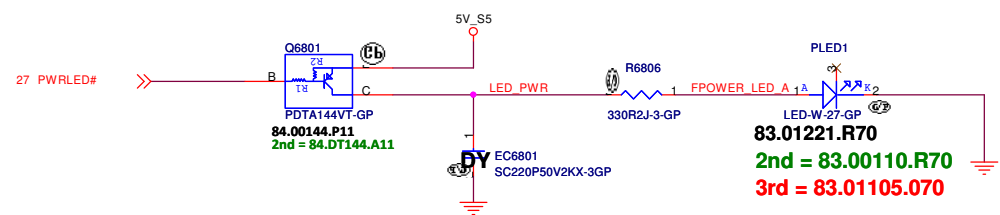
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M14 DIS

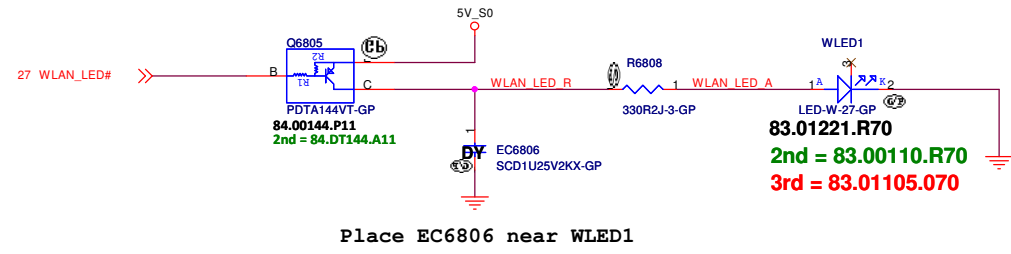
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
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SSID = User.Interface

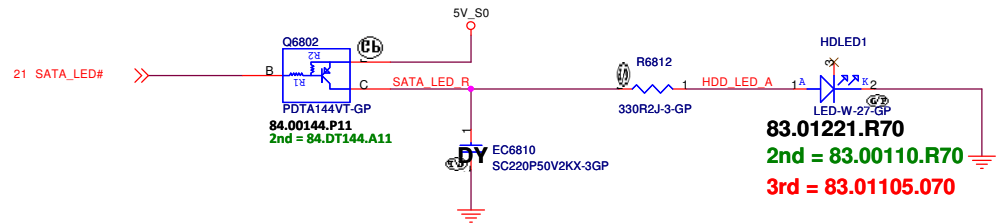
FRONT POWER LED
Low actived from KBC GPIO



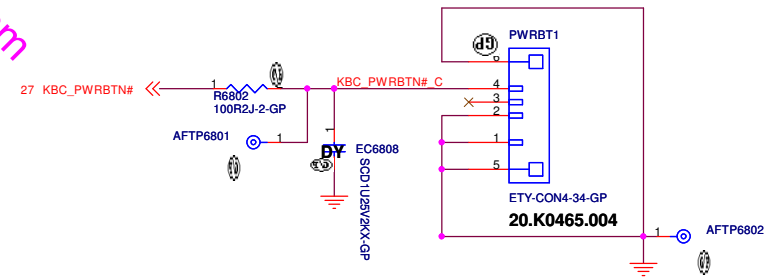
Wireless LED
Low actived from KBC GPIO



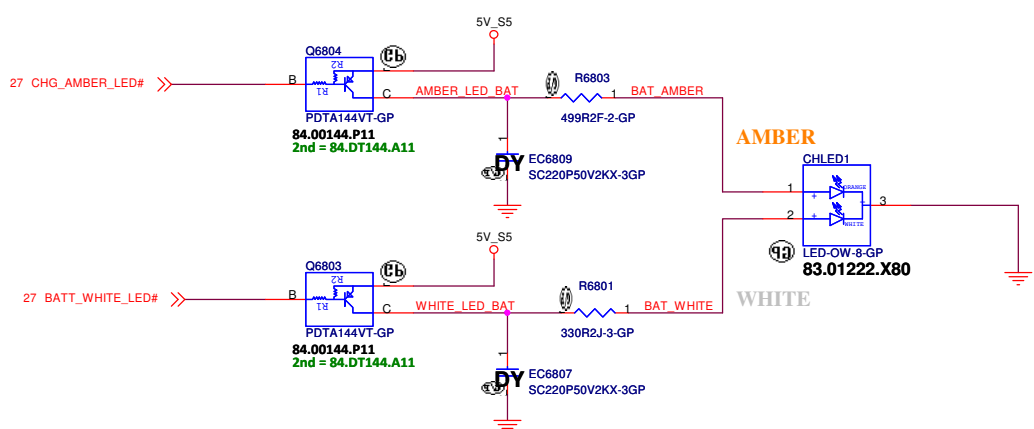
SATA HDD LED (White)
Low actived from PCH GPIO



Power button



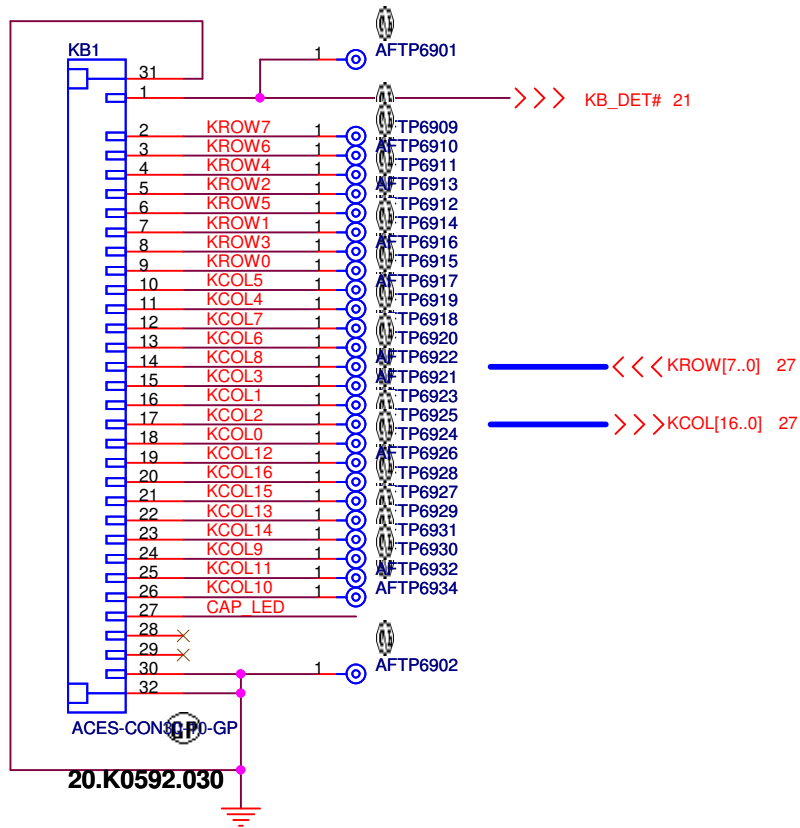
Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

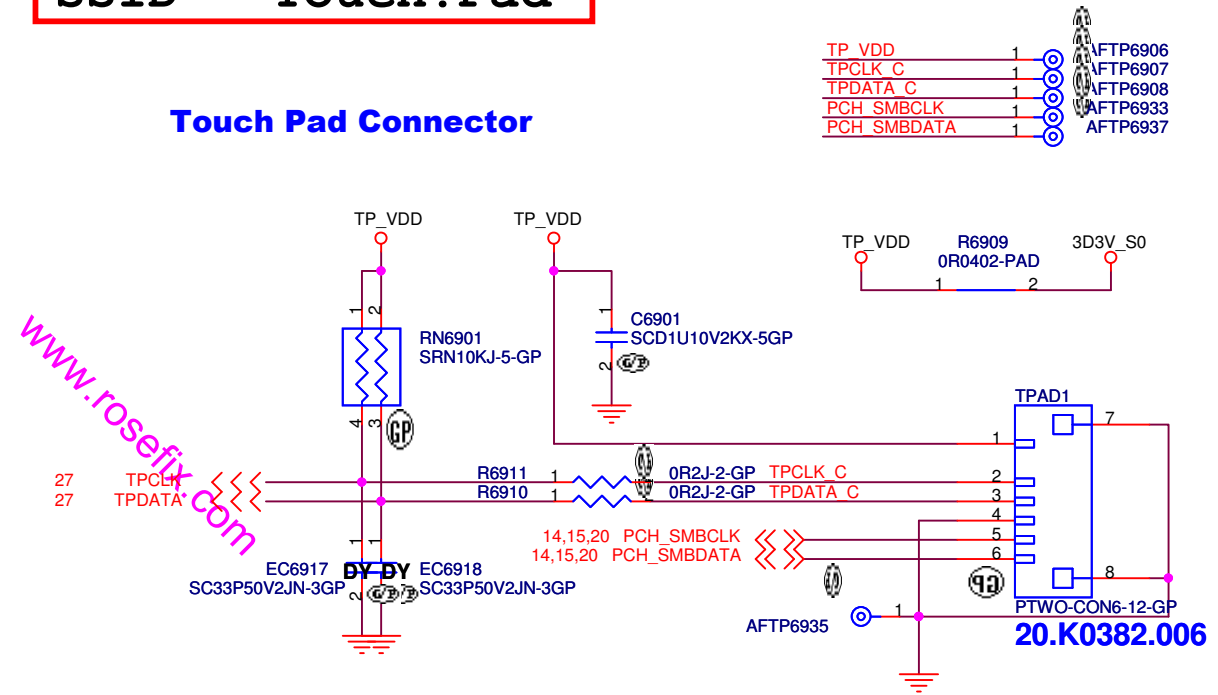
SSID = KBC

Internal Keyboard Connector



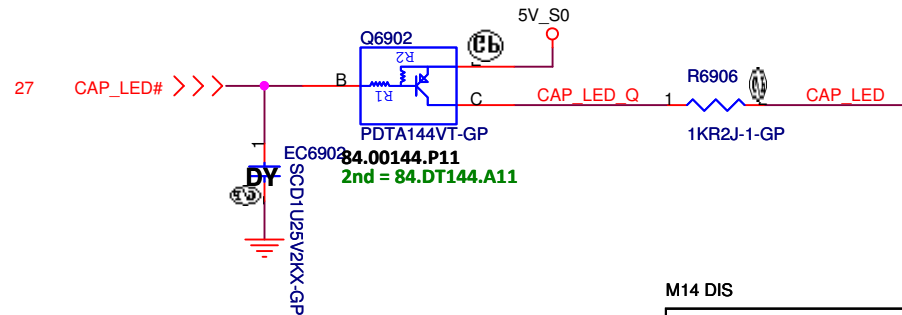
SSID = Touch.Pad

Touch Pad Connector



CAP LED Control

LOW acted from KBC GPIO



M14 DIS



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Title

Key Board/Touch Pad

Size

Document Number

OAK14 Chief River DIS

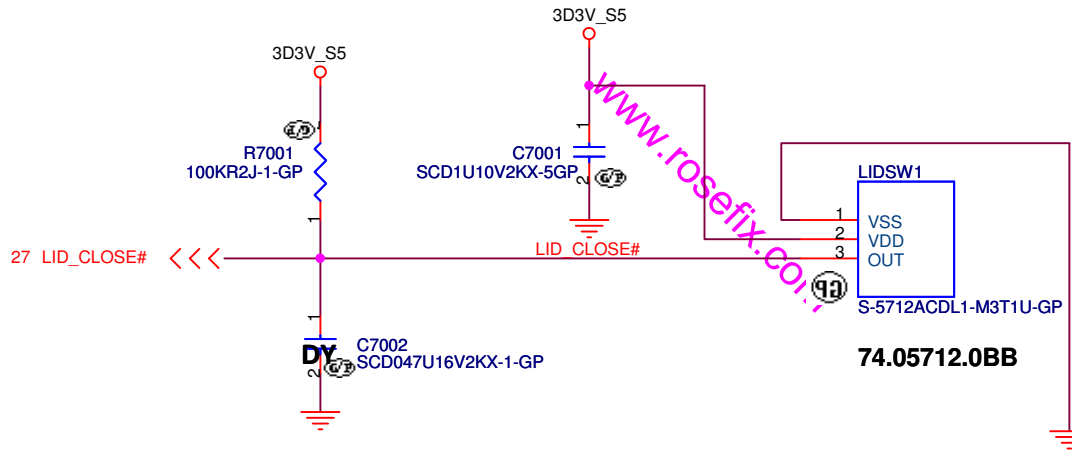
Rev

A00


Date: Wednesday, September 05, 2012

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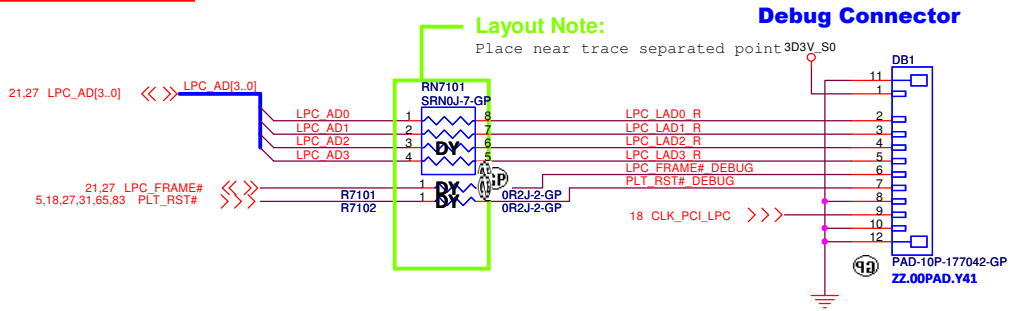
SSID = User.Interface



M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Hall Sensor		
Size A4	Document Number OAK14 Chief River DIS	Rev A00
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SSID = DEBUG PORT



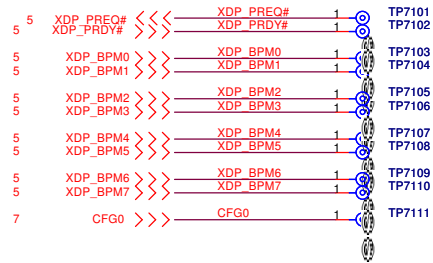
Layout Note:

Place near trace separated point 3D3V_S0

Debug Connector

SSID = CPU

CPU XDP



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M14 DIS

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Dubug connector			
Size: A3	Document Number: OAK14 Chief River DIS		Rev: A00
Date: Wednesday, September 05, 2012		Sheet: 71	of: 105

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M14 DIS

	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 72 of 105

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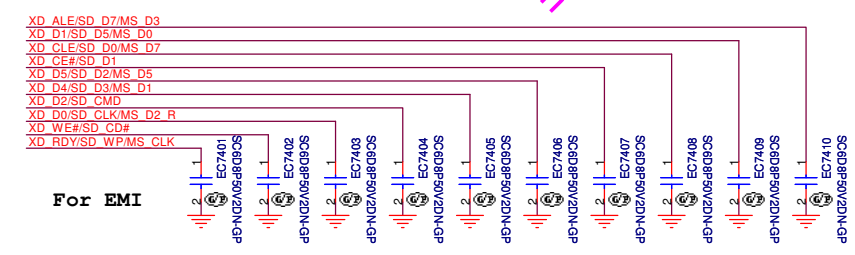
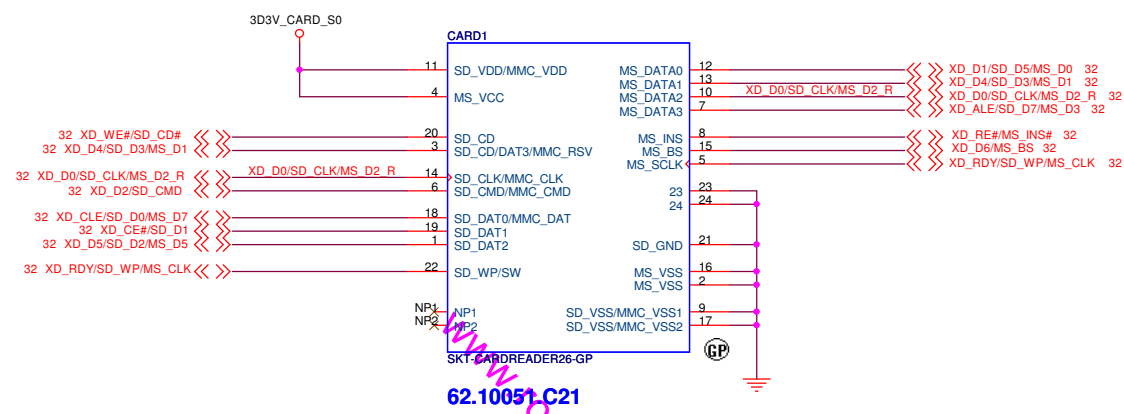
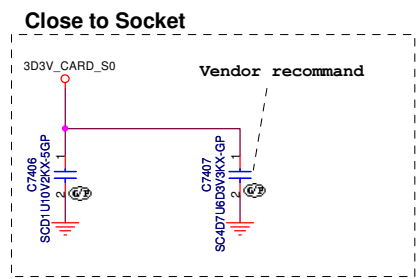
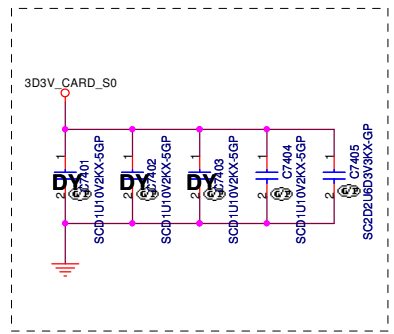
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M14 DIS

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Title		
Reserved		
Size	Document Number	Rev
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SSID = SDIO



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Title			
Express Card			
Size	Document Number	Rev	
A3	OAK14 Chief River DIS	A00	
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M14 DIS

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Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
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M14 DIS



Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		
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M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Free Fall Sensor		
Size	Document Number	Rev
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M14 DIS

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Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
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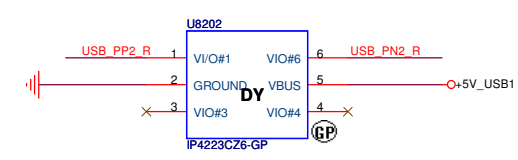
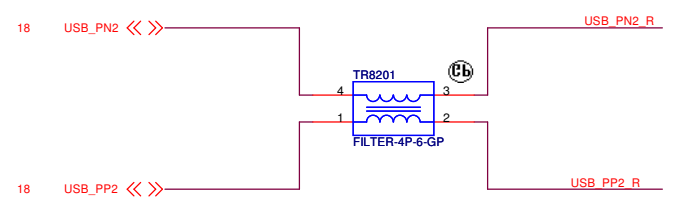
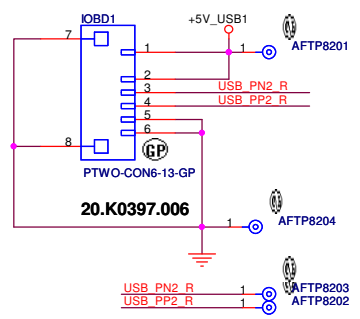
M14 DIS

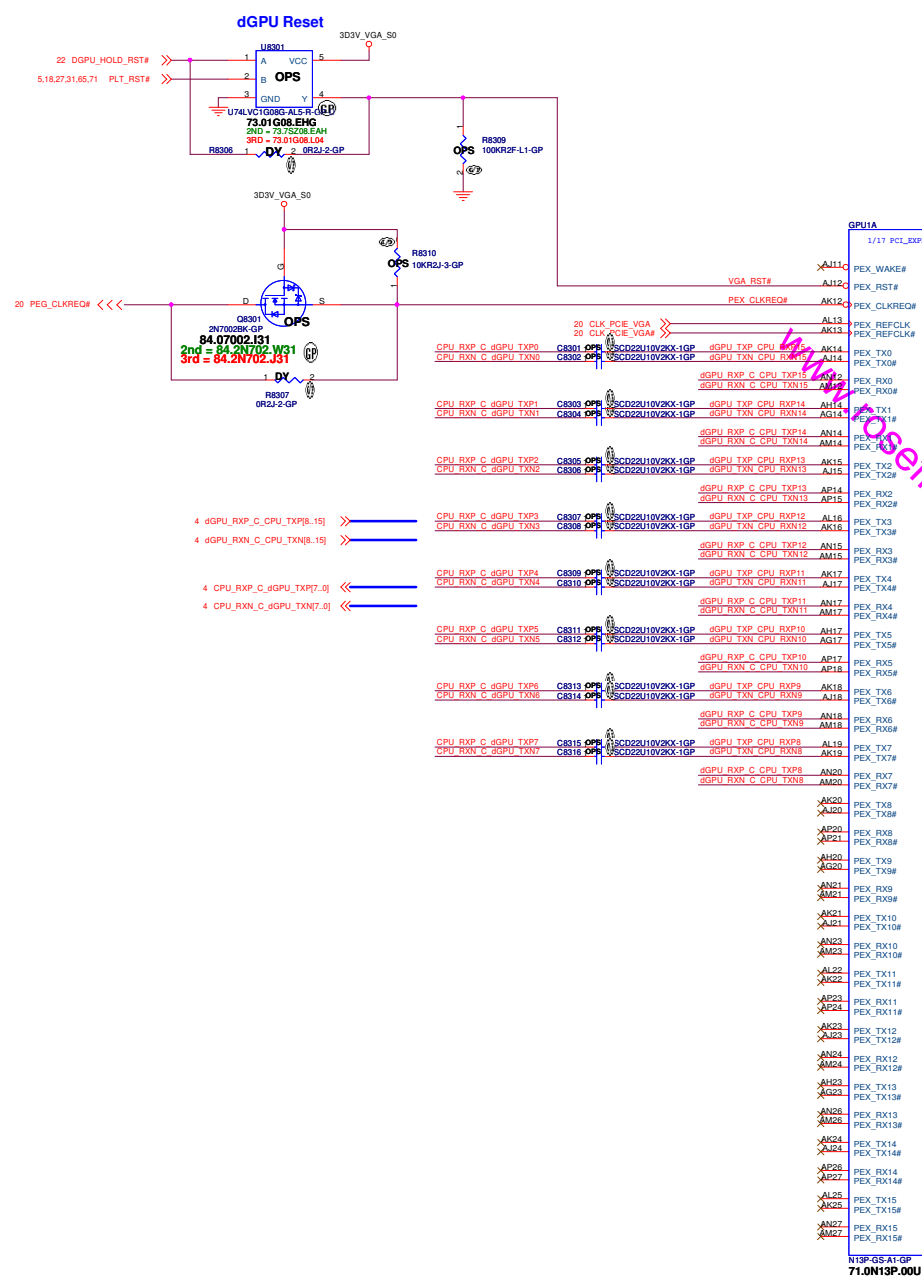


Title		
Reserved		
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A3	OAK14 Chief River DIS	A00
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SSID = User.Interface

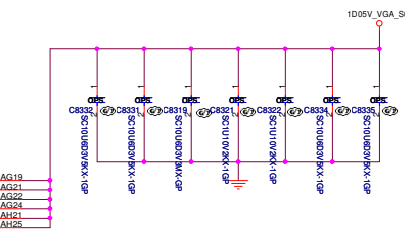
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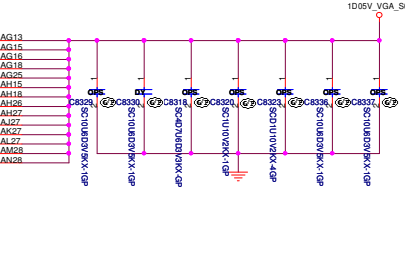


GPUA	1/17 PCI_EXPRESS
PEX_WAKE#	AJ11
PEX_RST#	AJ12
PEX_CLKREQ#	AK12
PEX_REFCLK#	AK13
PEX_REFCLK#	AK13
PEX_TX0	AK14
PEX_TX0#	AJ14
PEX_RX0	AM12
PEX_RX0#	AM12
PEX_TX1	AH14
PEX_TX1#	AJ14
PEX_RX1	AM14
PEX_RX1#	AM14
PEX_TX2	AH15
PEX_TX2#	AJ15
PEX_RX2	AM15
PEX_RX2#	AM15
PEX_TX3	AK16
PEX_TX3#	AK16
PEX_RX3	AM16
PEX_RX3#	AM16
PEX_TX4	AH17
PEX_TX4#	AJ17
PEX_RX4	AM17
PEX_RX4#	AM17
PEX_TX5	AH17
PEX_TX5#	AG17
PEX_RX5	AM17
PEX_RX5#	AM17
PEX_TX6	AH18
PEX_TX6#	AJ18
PEX_RX6	AM18
PEX_RX6#	AM18
PEX_TX7	AH19
PEX_TX7#	AJ19
PEX_RX7	AM19
PEX_RX7#	AM19
PEX_TX8	AK20
PEX_TX8#	AK20
PEX_RX8	AM20
PEX_RX8#	AM20
PEX_TX9	AH20
PEX_TX9#	AJ20
PEX_RX9	AM20
PEX_RX9#	AM20
PEX_TX10	AH21
PEX_TX10#	AJ21
PEX_RX10	AM21
PEX_RX10#	AM21
PEX_TX11	AH22
PEX_TX11#	AJ22
PEX_RX11	AM22
PEX_RX11#	AM22
PEX_TX12	AH23
PEX_TX12#	AJ23
PEX_RX12	AM23
PEX_RX12#	AM23
PEX_TX13	AH24
PEX_TX13#	AJ24
PEX_RX13	AM24
PEX_RX13#	AM24
PEX_TX14	AH25
PEX_TX14#	AJ25
PEX_RX14	AM25
PEX_RX14#	AM25
PEX_TX15	AH26
PEX_TX15#	AJ26
PEX_RX15	AM26
PEX_RX15#	AM26
PEX_TX16	AH27
PEX_TX16#	AJ27
PEX_RX16	AM27
PEX_RX16#	AM27
PEX_TX17	AH27
PEX_TX17#	AJ27
PEX_RX17	AM27
PEX_RX17#	AM27
PEX_TX18	AH28
PEX_TX18#	AJ28
PEX_RX18	AM28
PEX_RX18#	AM28
PEX_TX19	AH29
PEX_TX19#	AJ29
PEX_RX19	AM29
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PEX_TX20	AH30
PEX_TX20#	AJ30
PEX_RX20	AM30
PEX_RX20#	AM30

GPU



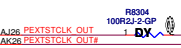
1.05V +/- 5%
1.97A



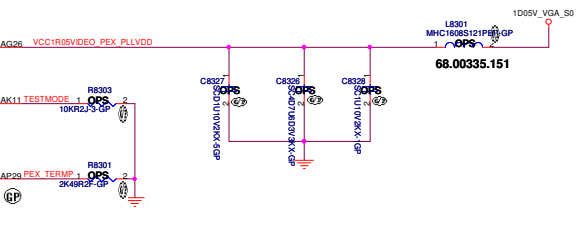
3.3V +/- 5%
22mA

X7R, Under GPU.

POWER IC

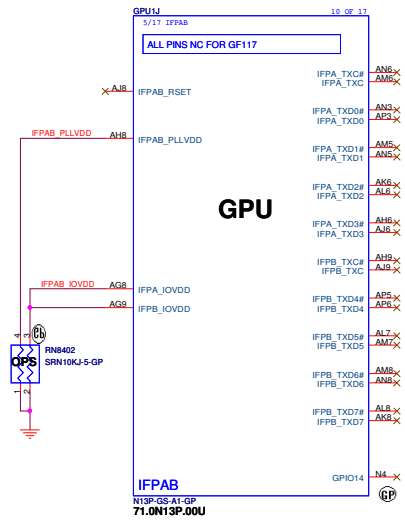


1.05V +/- 3%
130mA

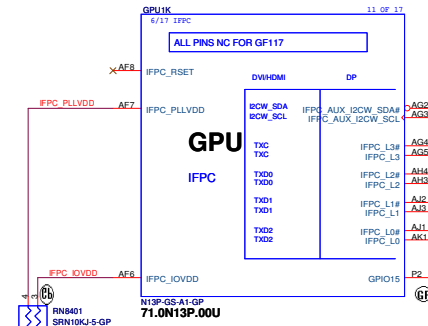


68.00335.151

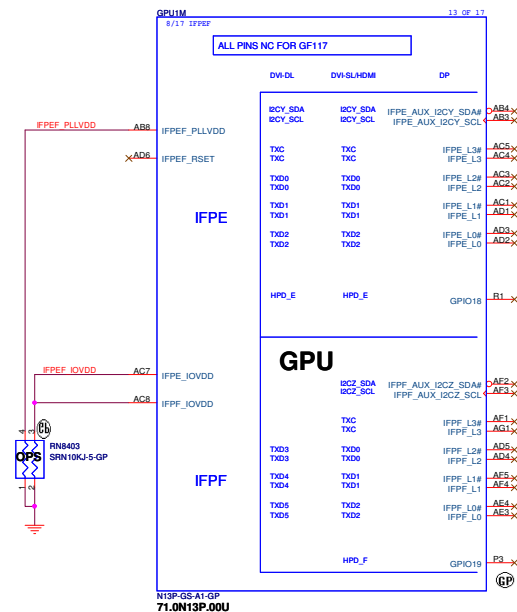
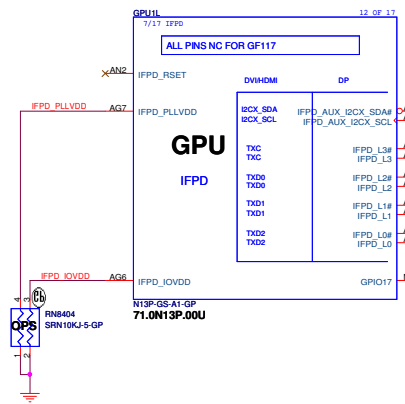
LVDS Interface

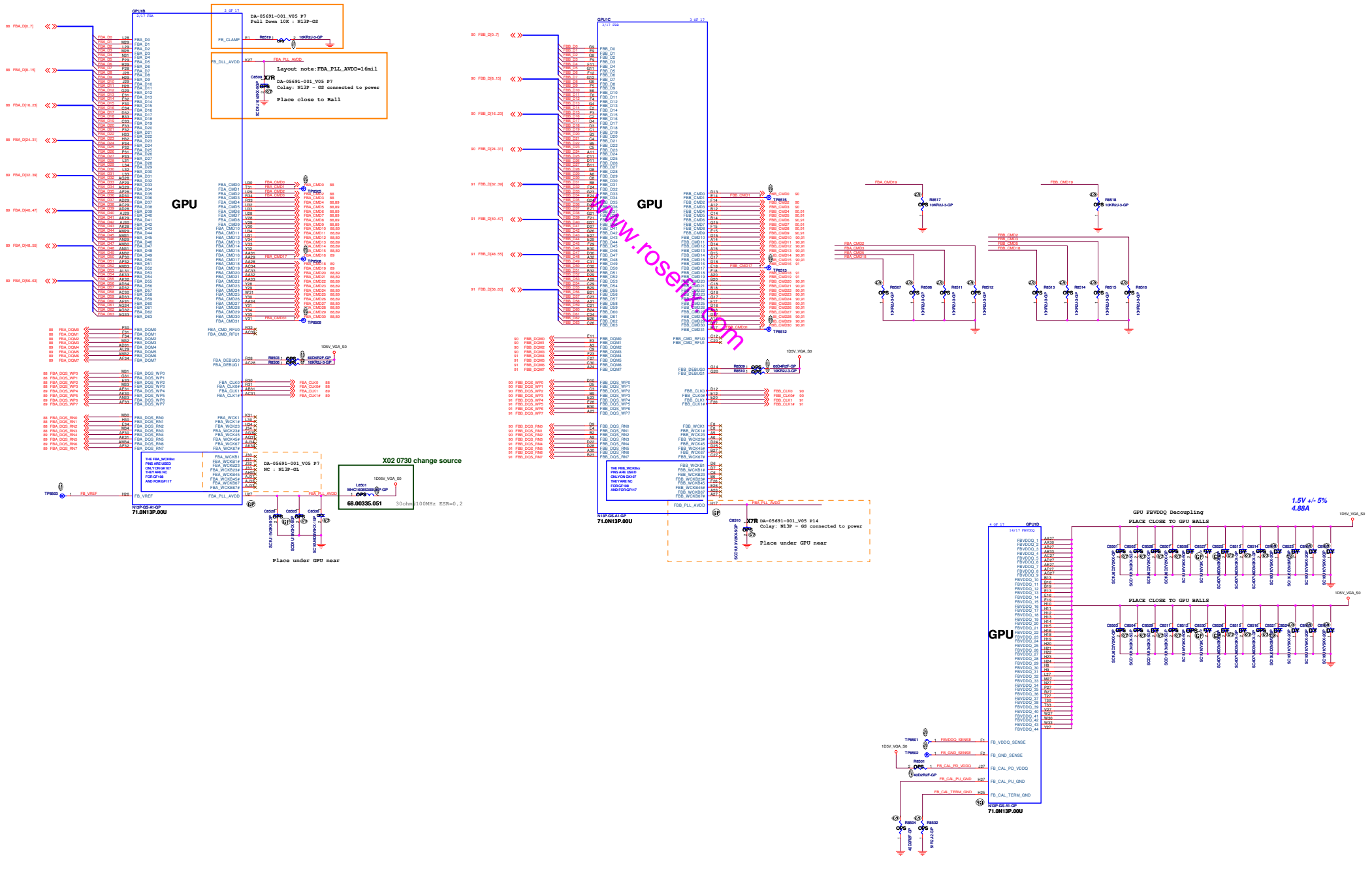


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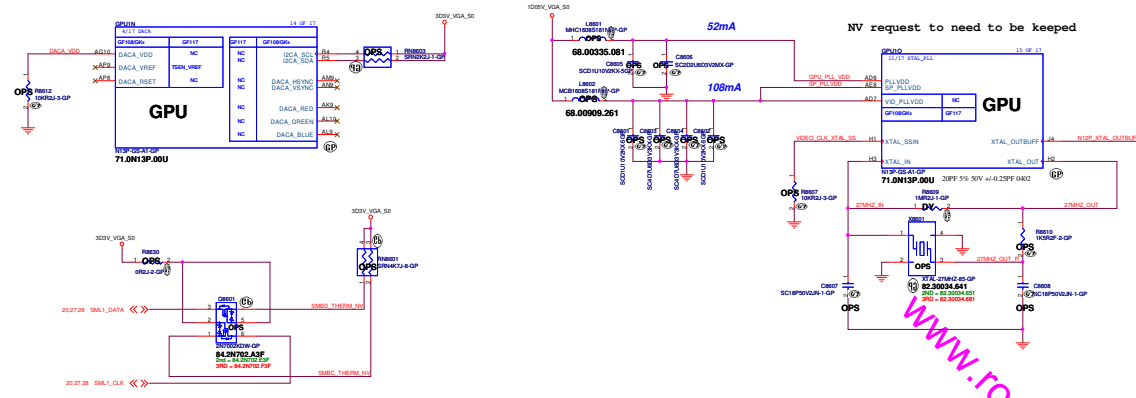


HDMI Interface





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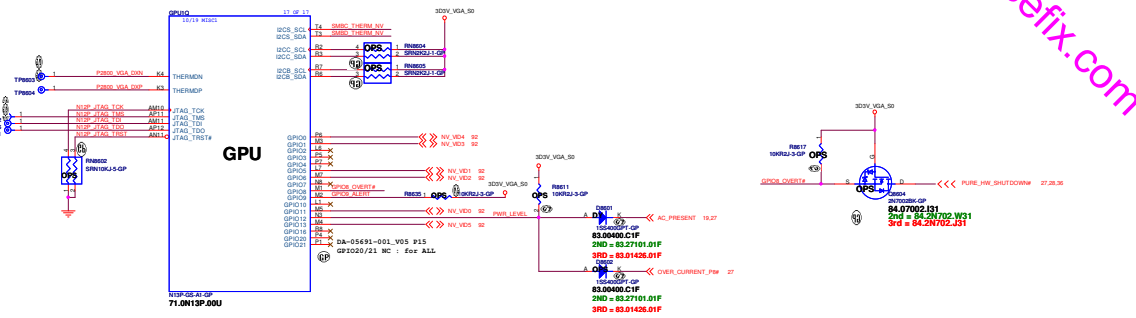
N13P-GS1

Strap Pin Name	Logical strapping name bit#	Logical strapping name bit#	Logical strapping name bit#	Logical strapping name bit#
ROM_SCLK	PCL_DEVID[1]	SUB_VENDOR	PCL_DEVID[5]	PEX_PEN_TER_M
ROM_SI	RAMCFG[1]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[1]	USER[2]	USER[1]	USER[0]
STRAP1	0	0	0	0
STRAP2	0	0	0	0
STRAP3	0	0	0	0
STRAP4	0	0	0	0

10K ohm pull-up
45K ohm pull-up
5K ohm pull-down
5K ohm pull-down
45K ohm pull-down

Part Reference	Part Number	Value	PCB Footprint
R8621(DIS_ROM SI)	64.20025.6DL	20K R2F-L-GP	R402H16
R8621	64.19025.6DL	15K R2F-L-GP	R402H16
R8621	64.34825.6DL	34K R2F-L-GP	R402H16
R8621	64.45325.6DL	45K R2F-L-GP	R402H16
R8621	64.30125.6DL	30K R2F-L-GP	R402H16
R8621	64.24925.6DL	24K R2F-L-GP	R402H16

GPU	N13P-GS
STRAP 0	PULL UP 45.3K
STRAP 1	PULL DOWN 4.99K
STRAP 2	PULL DOWN 15K
STRAP 3	PULL DOWN 4.99K
STRAP 4	PULL DOWN 45.3K
ROM_SO	PULL UP 10K
ROM_SCLK	PULL UP 4.99K
VRAM	ROM_SI pin
128M*16 DDR3 Samsung	Pull down 24.9K ohm
K4W2G1646E-BC11	
128M*16 DDR3 Hynix	Pull down 30K ohm
H5TQ2G63DFR-11C	

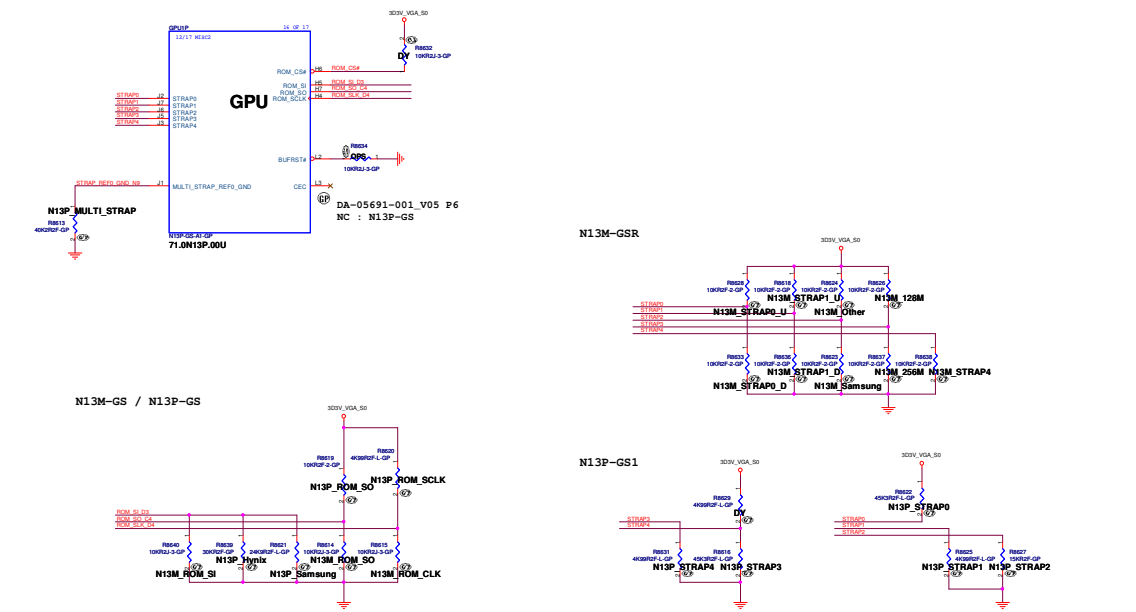


N13M-GSR

Table 4. Binary Strap Mode Mapping

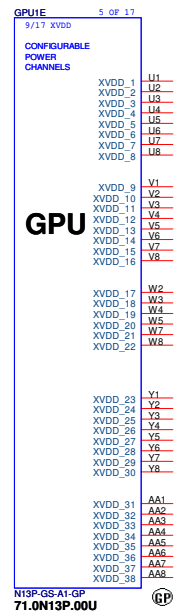
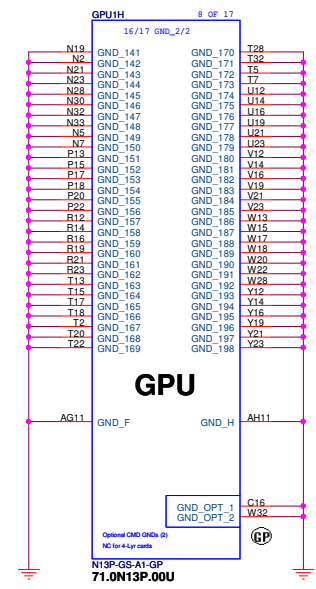
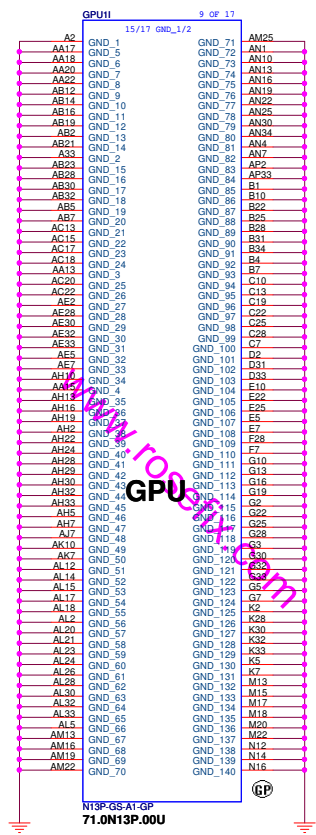
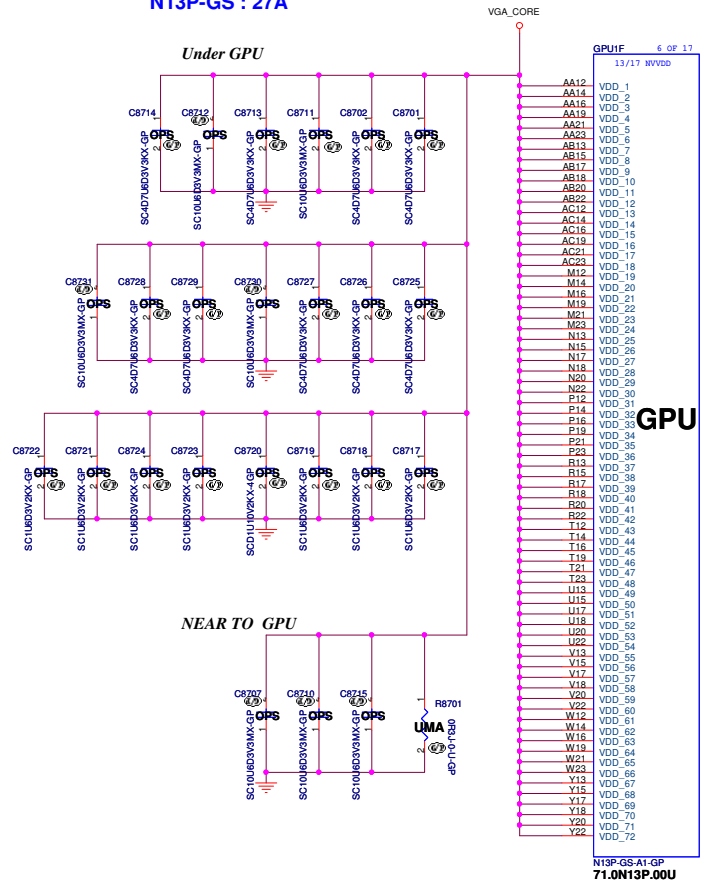
Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCI_MAX_SPEED	10k Ω	Pull-down to GND

GPU	N13M-GS	STRAP 0	STRAP 1	STRAP 2	STRAP 3	
STRAP 4	PULL DOWN 10K					
ROM_SCLK	PULL DOWN 10K					
ROM_SO	PULL DOWN 10K					
ROM_SI	PULL DOWN 10K					
VRAM	STRAP 0	STRAP 1	STRAP 2	STRAP 3		
128M*16 DDR3 Samsung	PULL UP 10K	PULL UP 10K	PULL DOWN 10K	PULL UP 10K	0xB	
128M*16 DDR3 Hynix	PULL DOWN 10K	PULL DOWN 10K	PULL UP 10K	PULL UP 10K	0xC	
256M*16 DDR3 Samsung	PULL UP 10K	PULL DOWN 10K	PULL DOWN 10K	PULL DOWN 10K	0x1	
256M*16 DDR3 Micron	PULL UP 10K	PULL DOWN 10K	PULL UP 10K	PULL DOWN 10K	0x5	

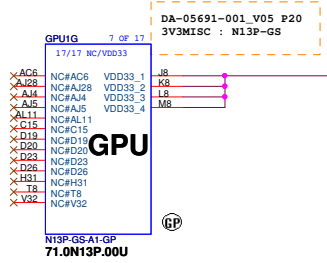


4/9 update GPU strapping

N13P-GS : 27A



XVDD_1~38
NC : N13P-GL



M14 DIS

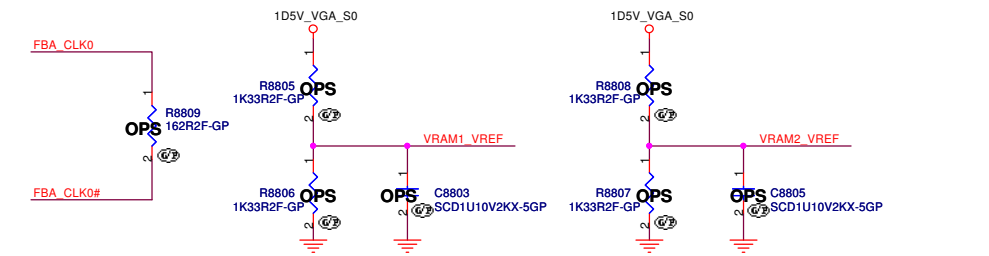
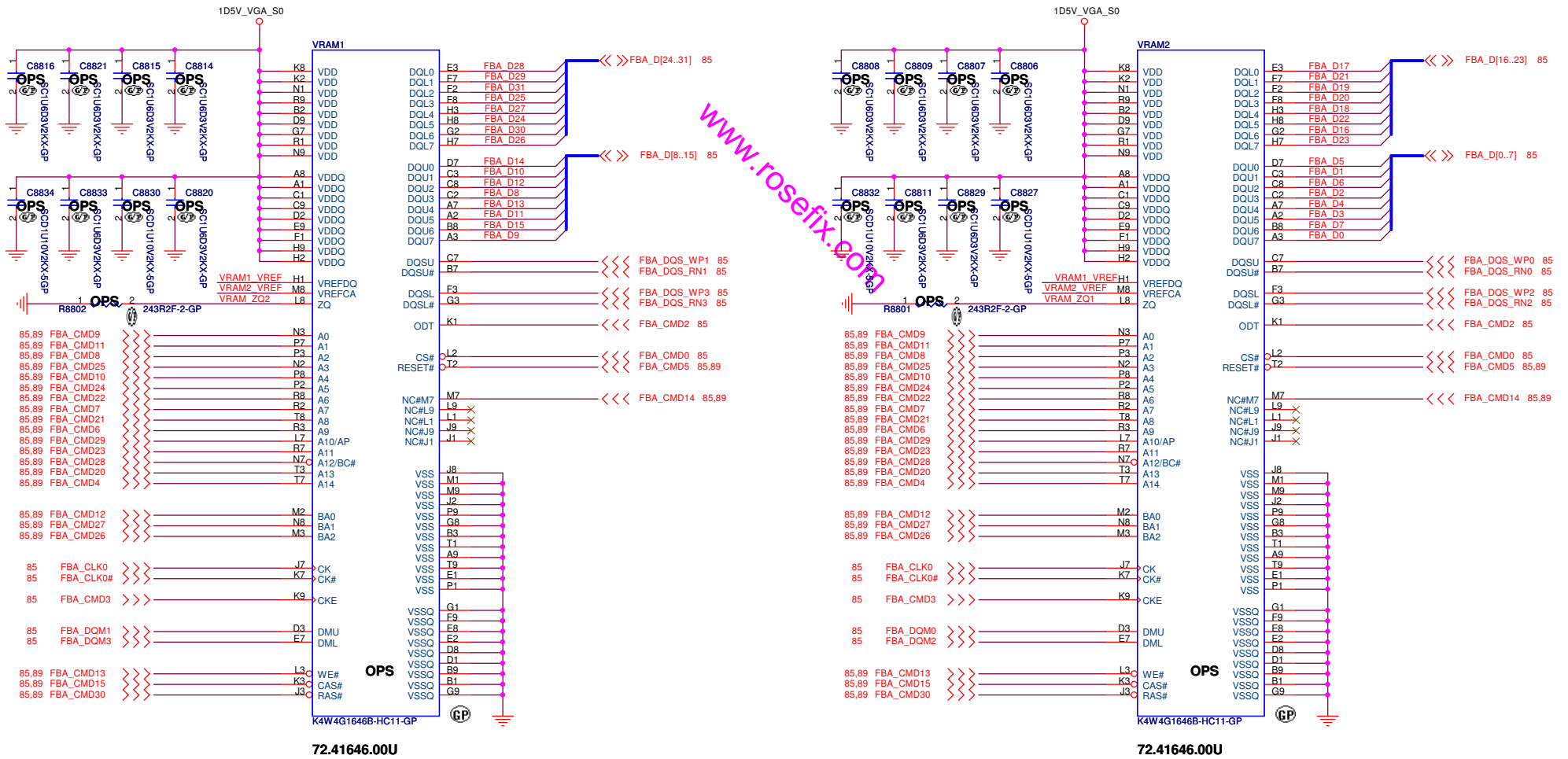
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU DPPWR/GND(5/5)**

Size: Document Number
Customer: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 1 Sheet 87 of 105

Frame Buffer Partition A-Lower Half



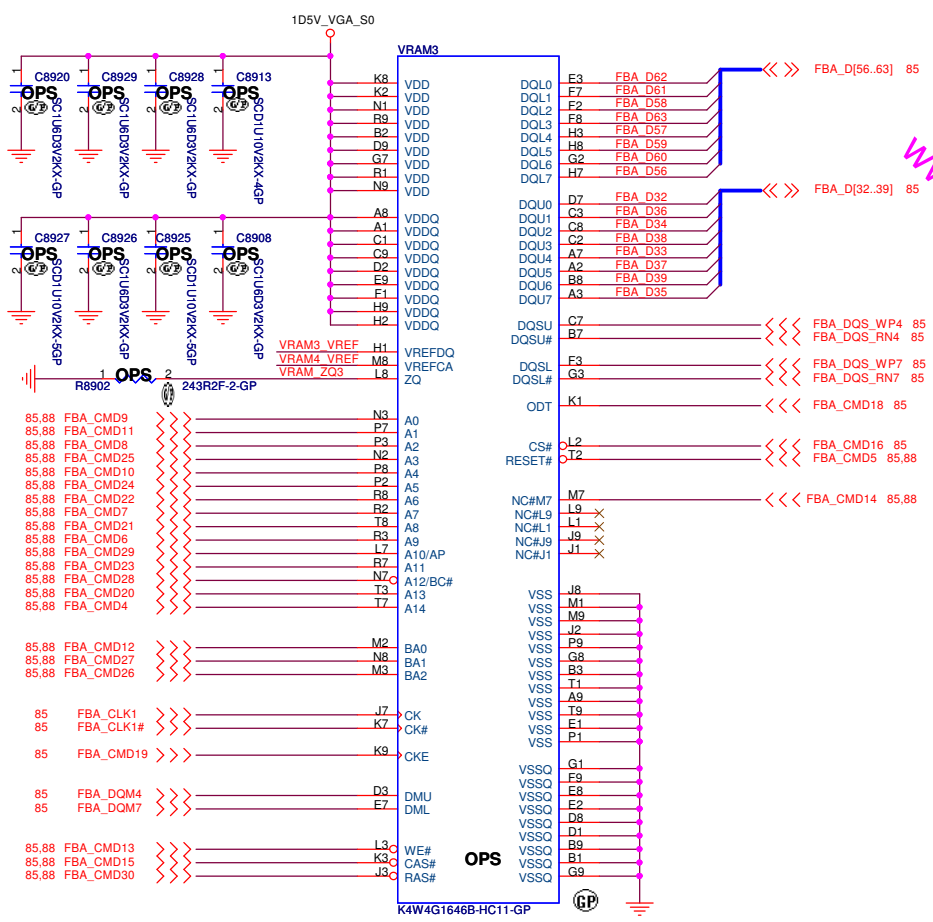
M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

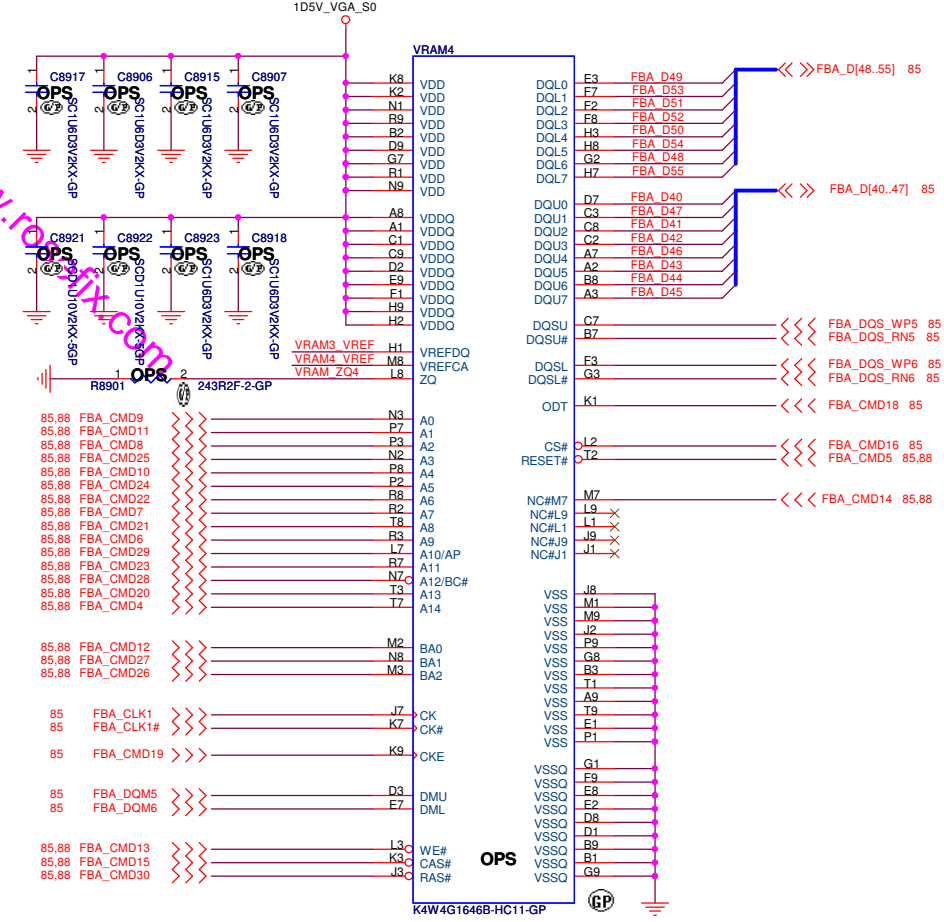
Title: **GPU-VRAM1,2 (1/4)**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 88	of 105

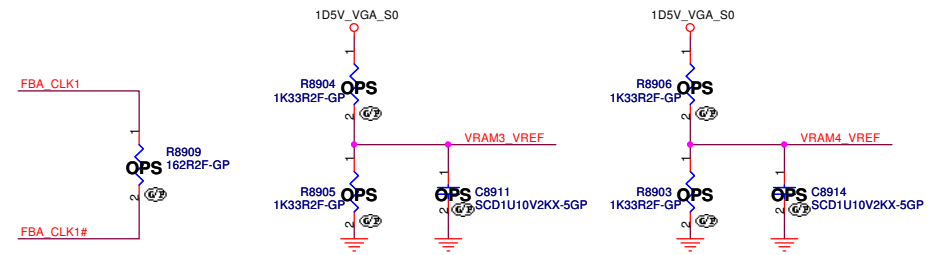
Frame Buffer Partition A-Upper Half



72.41646.00U



72.41646.00U



M14 DIS

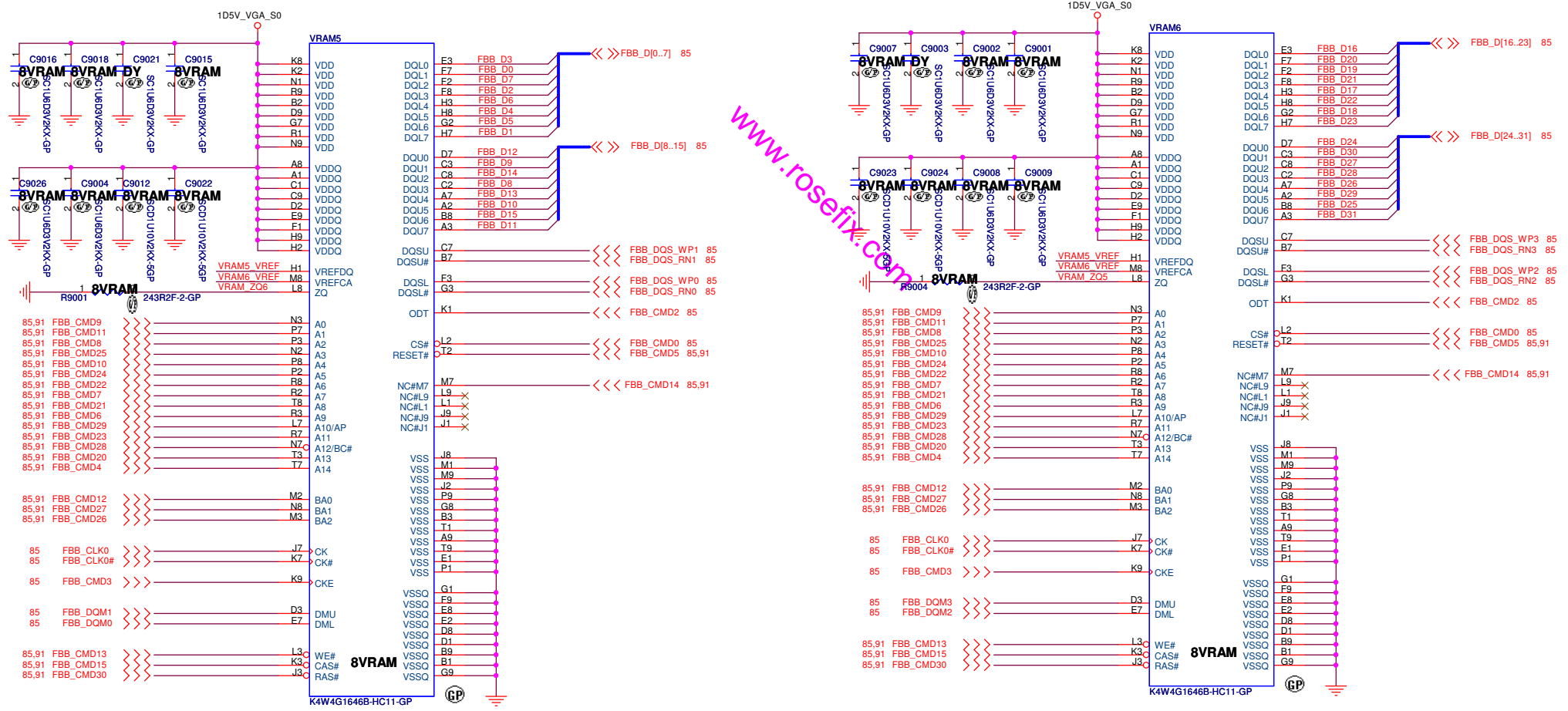
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM3,4 (2/4)**

Size A3, Document Number: **OAK14 Chief River DIS**, Rev: **A00**

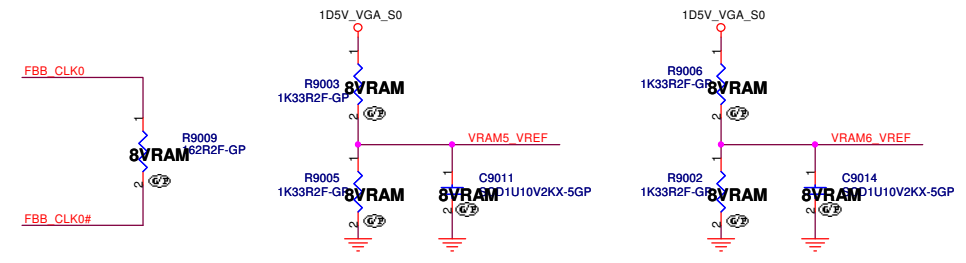
Date: Wednesday, September 05, 2012, Sheet 89 of 105

Frame Buffer Partition B-Lower Half



72.41646.00U

72.41646.00U

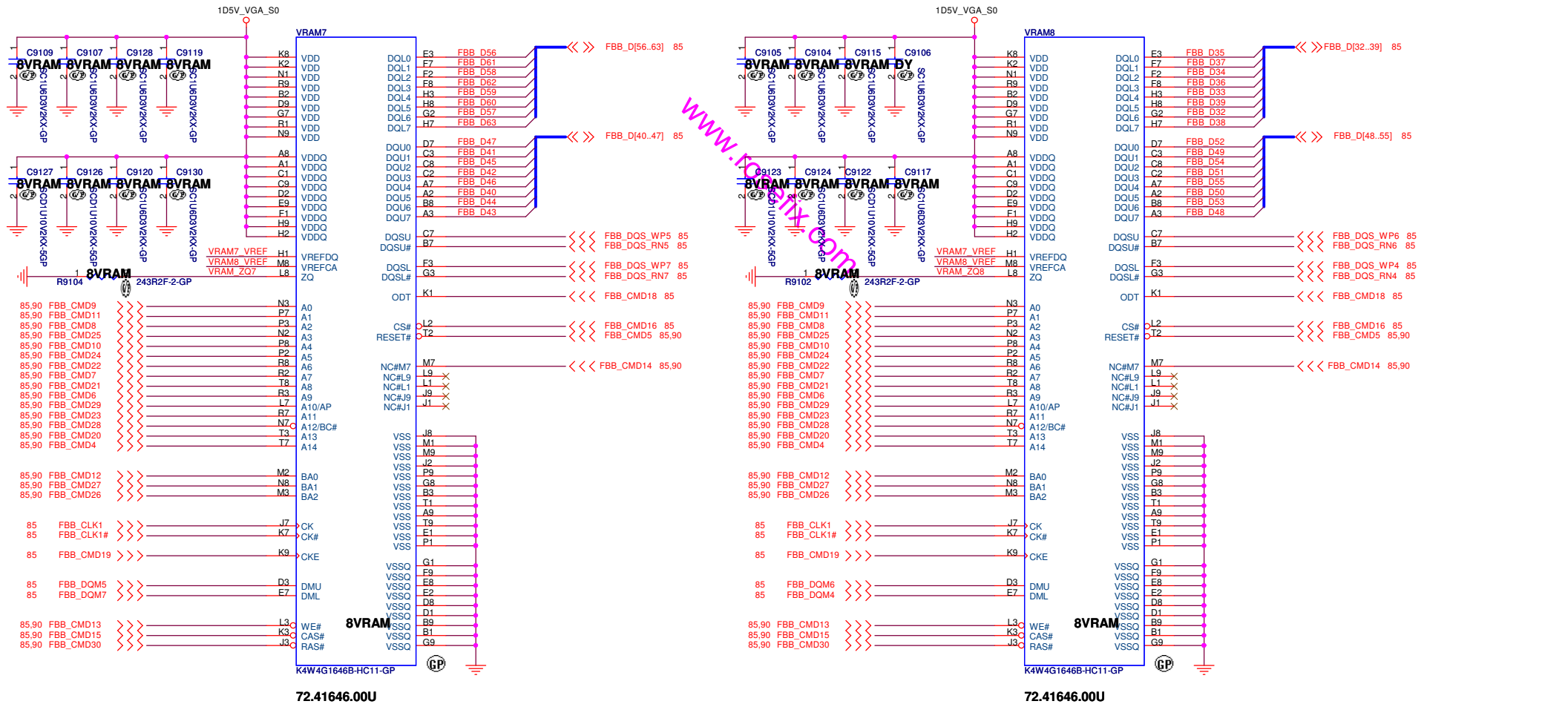


M14 DIS



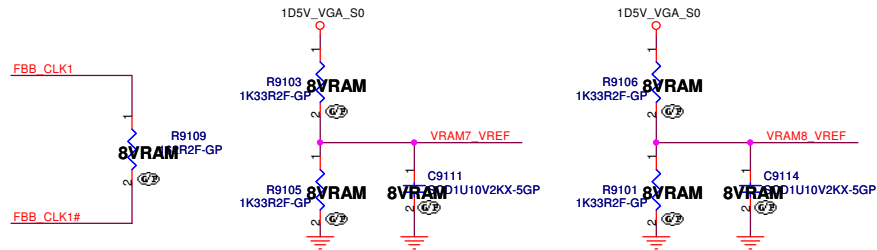
Title GPU-VRAM5,6 (3/4)		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date Wednesday, September 05, 2012	Sheet 90	of 105

Frame Buffer Partition B-Upper Half



72.41646.00U

72.41646.00U



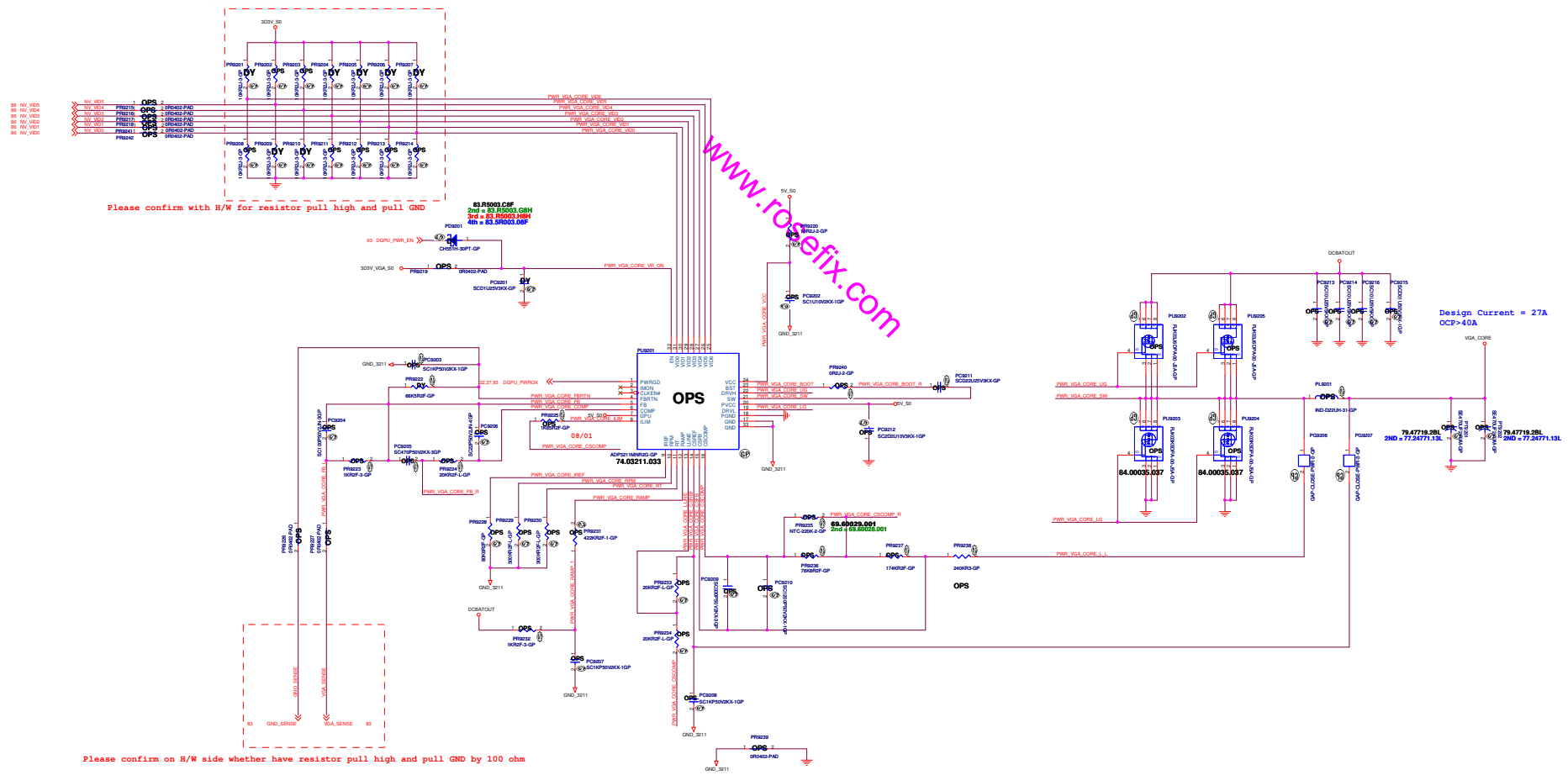
M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

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V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0



I/P cap: 100 25V K0805 X5R/ 78.10622.511
 Inductor: CHIP COIL 0.3R0H POWR1047-83R0H 1.05mohm/ Isat -60A rms68.R3610.200
 O/P cap: CHIP CAP 470UF 2V EEP30D471X/ 3.5Ams Panasonic/79.47719.28L
 R/S: RUMK3K50PA-00475A / 10mohm/13mOhm±4.5Vpp/ 84.00036.037
 L/S: RUMK3K50PA-00475A / 3mohm/3.5mOhm±4.5Vpp/ 84.00031.037

M14 018

DELL Wistron Corporation
 P.O. Box 1, Hsin-Tai Wu, Taipei, Taiwan, R.O.C.

ADP3211 +VGA CORE

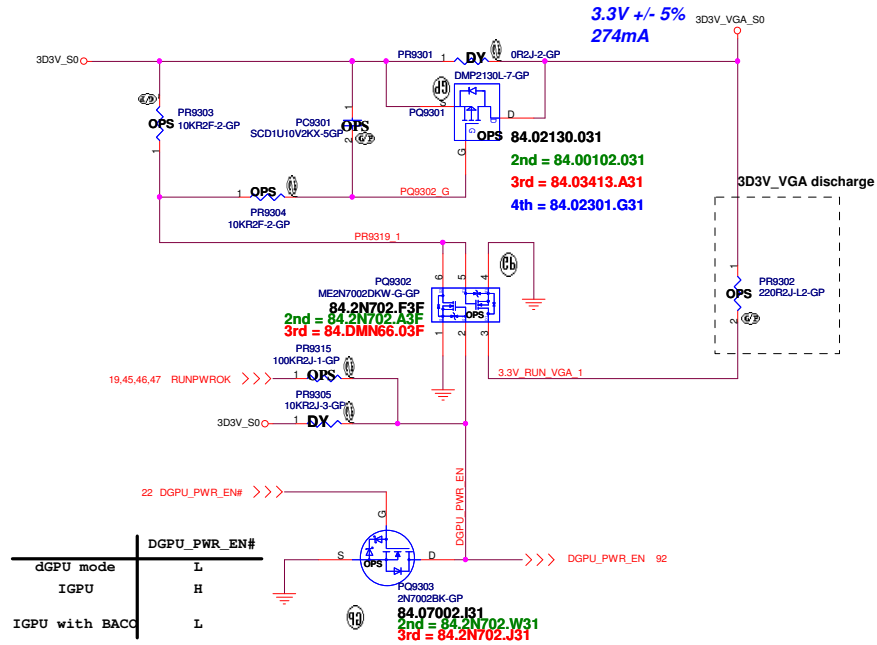
Rev: 1.0

Q1: **DNE40 14 CR DIS**

Rev: 1.0

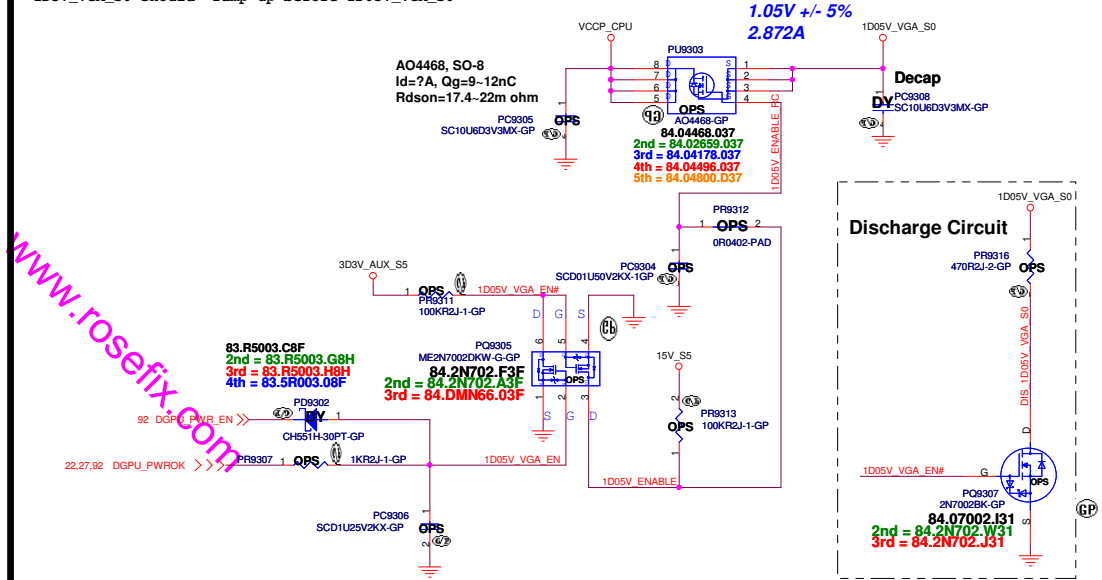
Date: Wednesday, September 05, 2012 Sheet: 02 of 100

3D3V_VGA_S0

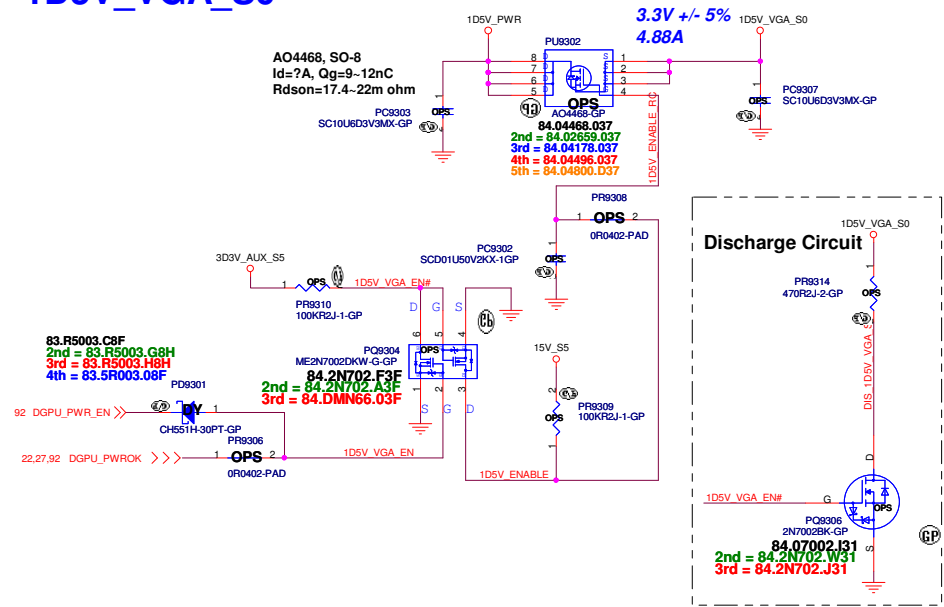


1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D05V_VGA_S0
1D05V_VGA_S0 should ramp-up before 1D05V_VGA_S0



1D5V_VGA_S0



NV do not need 1.8V

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M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LVDS Switch			
Size	Document Number	Rev	
A3	OAK14 Chief River DIS	A00	
Date:	Wednesday, September 05, 2012	Sheet	94 of 105

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M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Switch			
Size	Document Number	Rev	
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SSID = SDIO

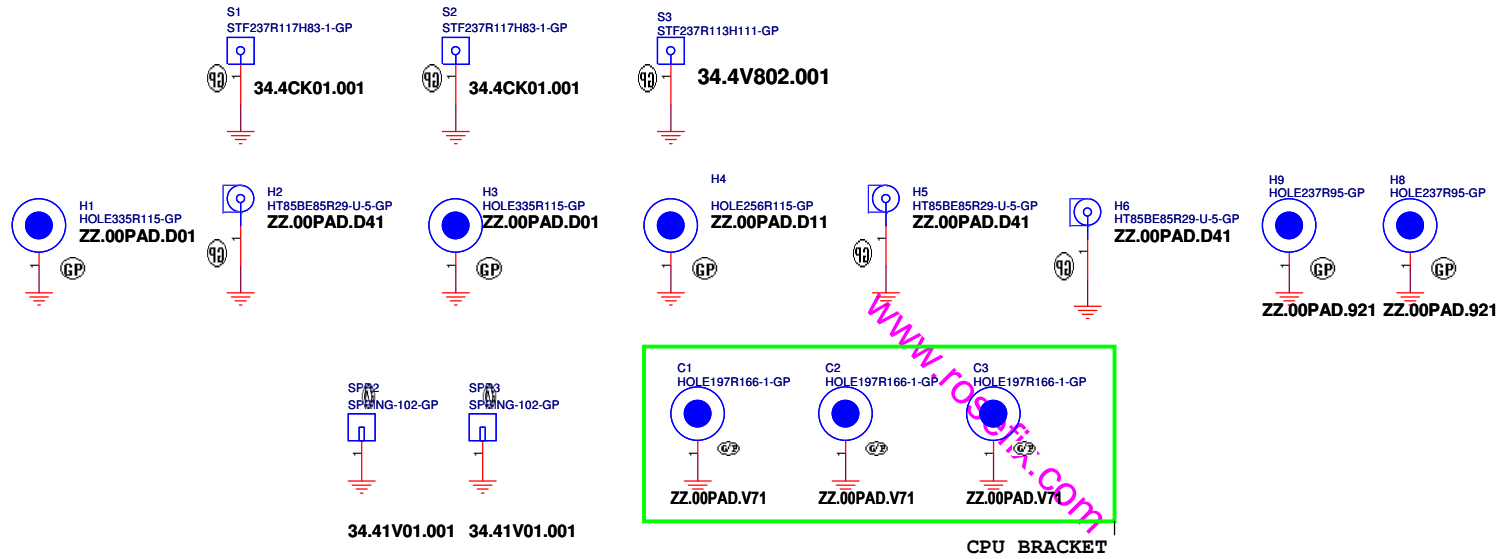
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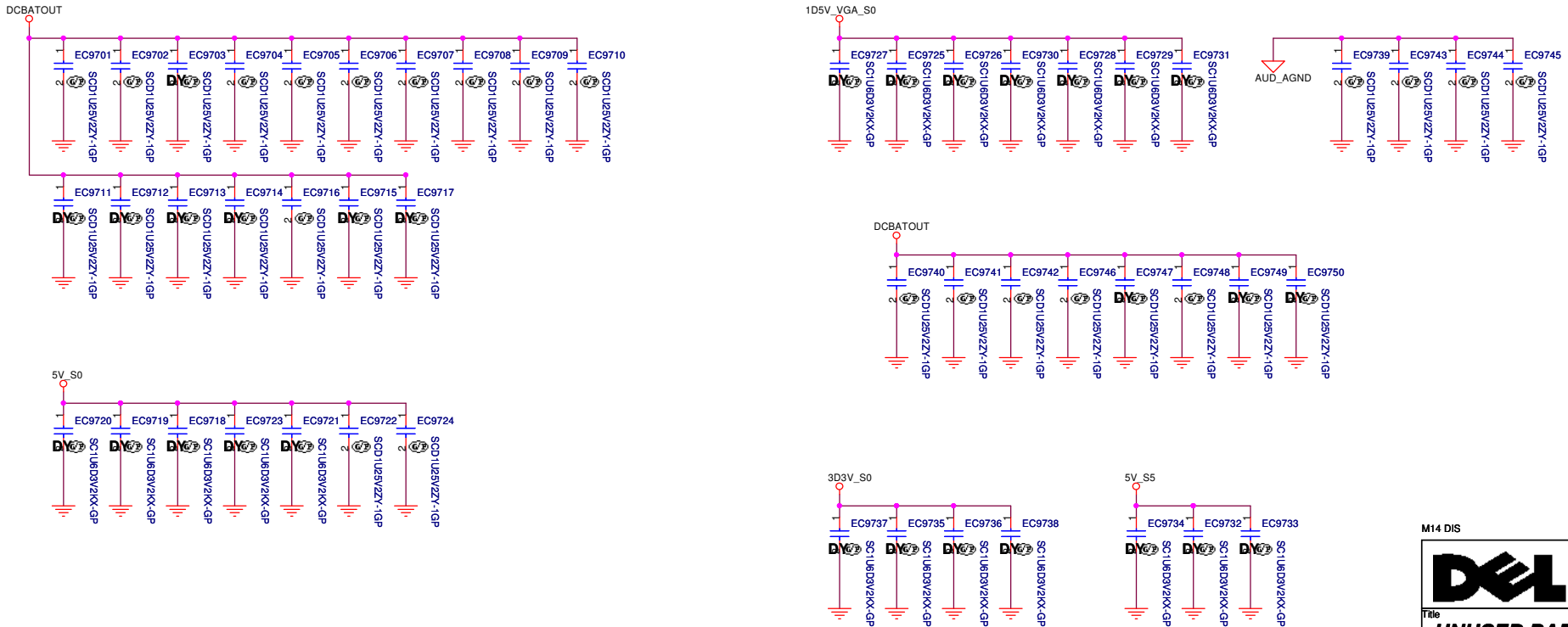
M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
TOUCH PANEL		
Size	Document Number	Rev
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SSID = Mechanical



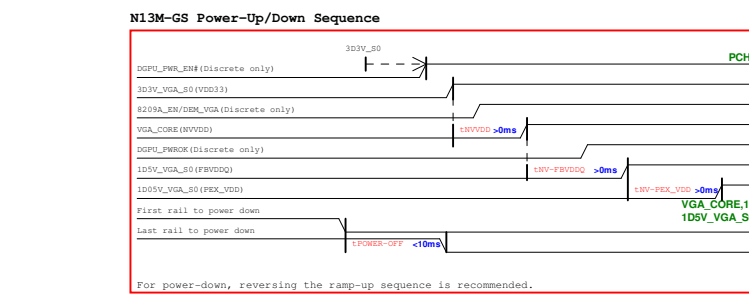
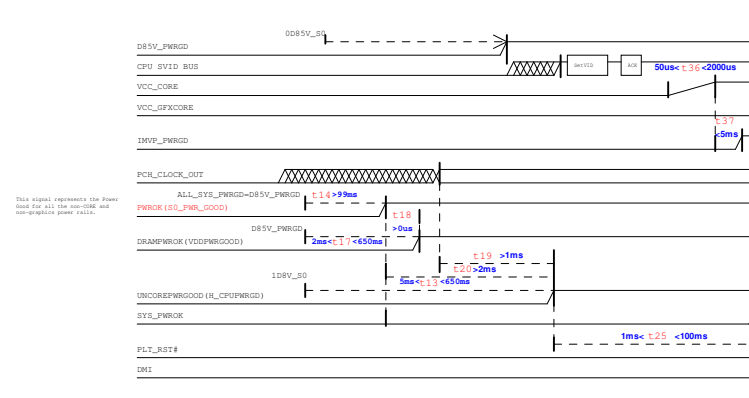
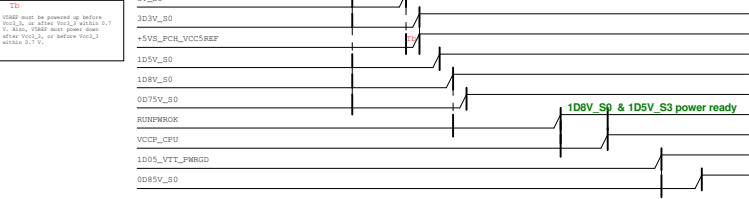
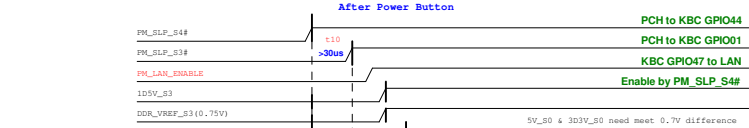
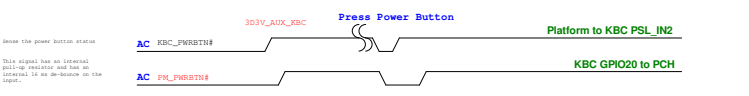
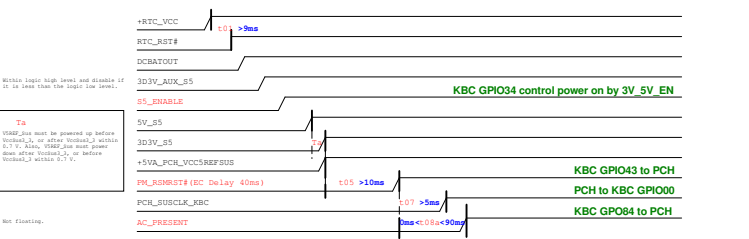
SSID = EMI



Chief River Platform Power Sequence

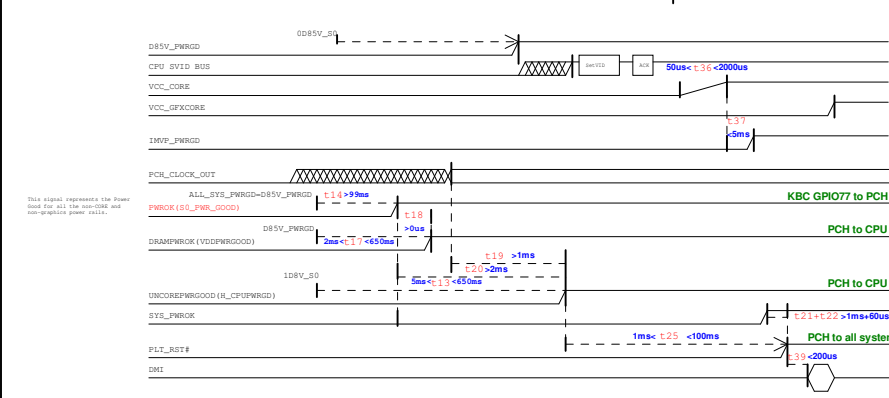
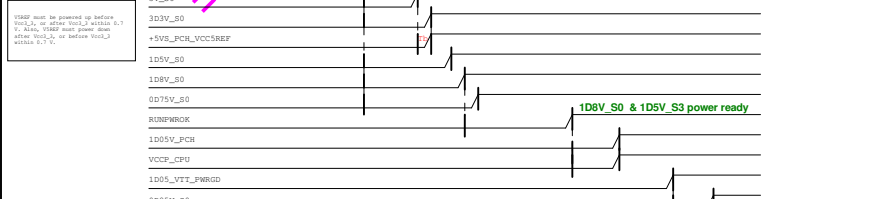
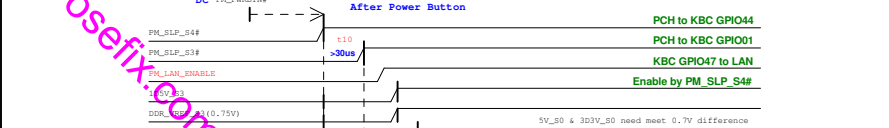
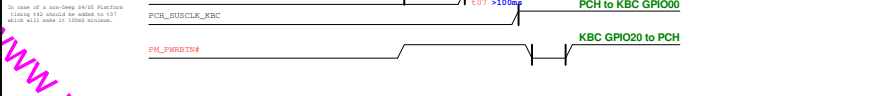
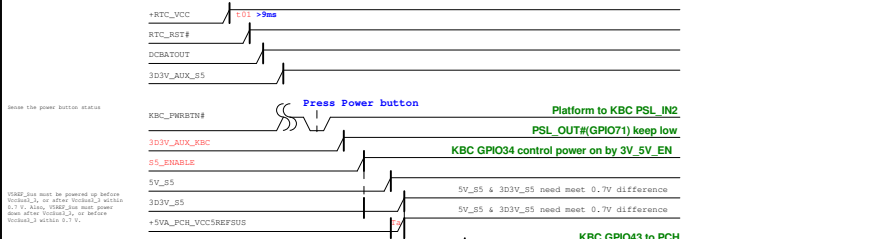
(AC mode)

Red Words: Controlled by EC GPIO



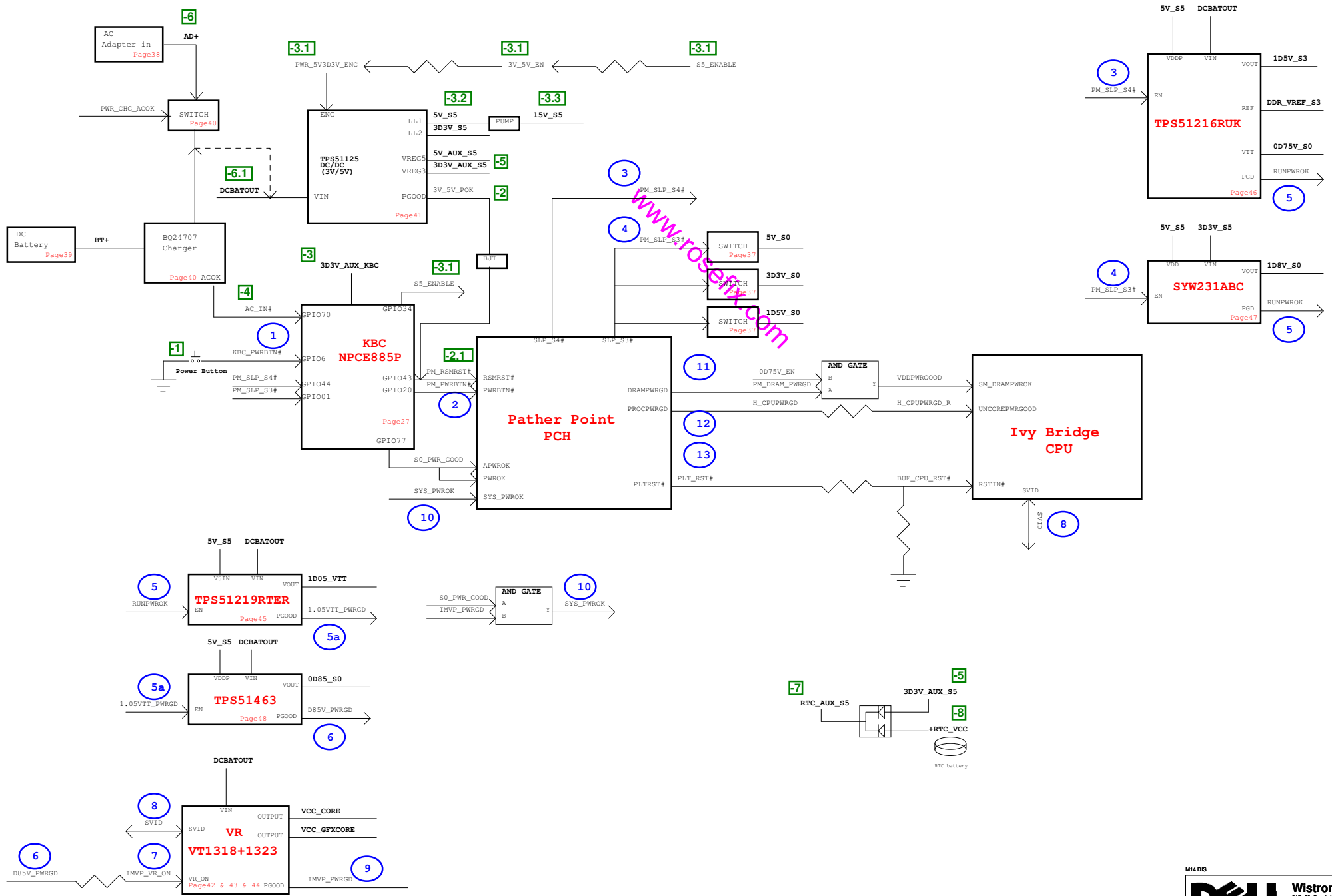
(DC mode)

Red Words: Controlled by EC GPIO

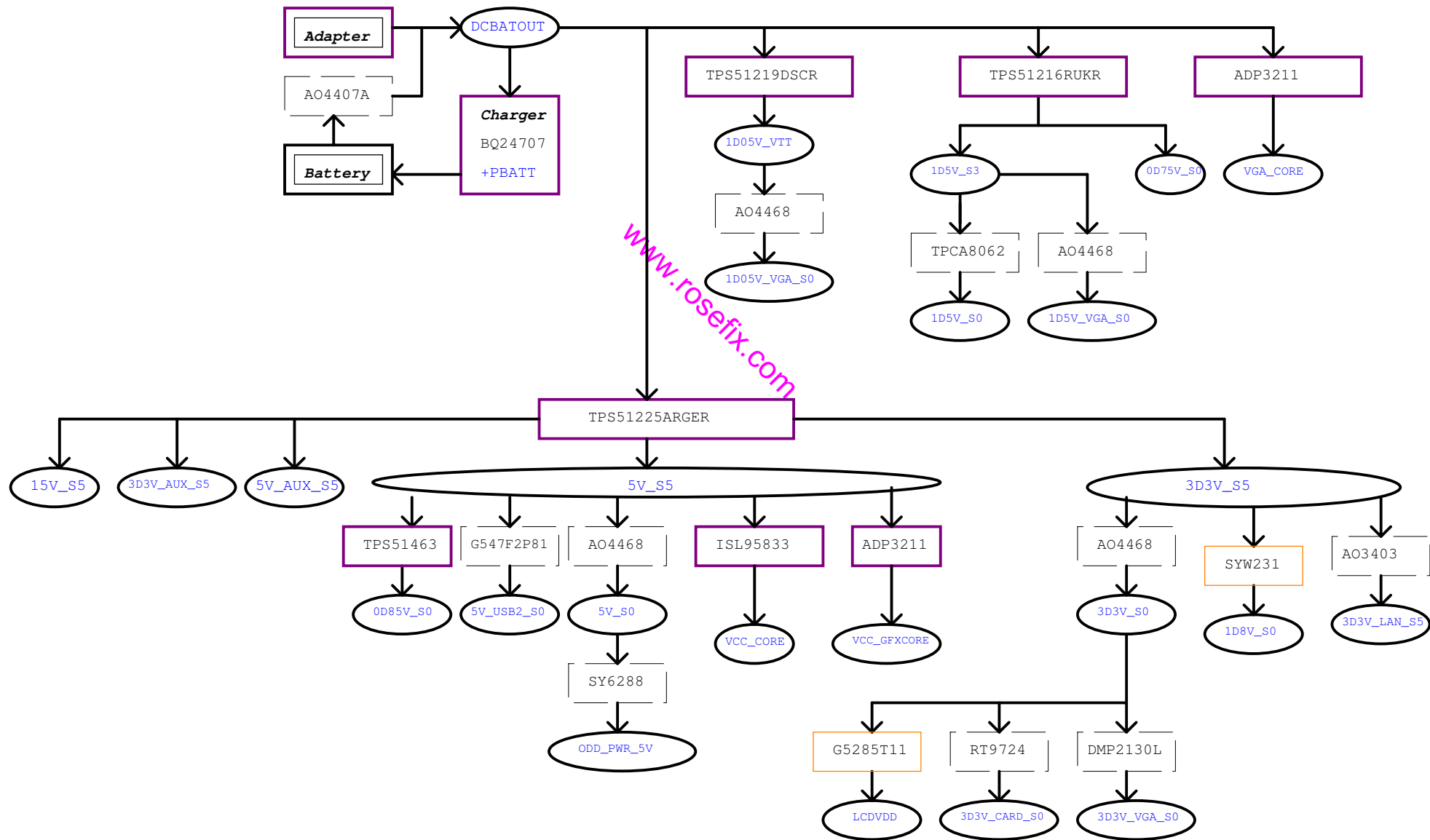


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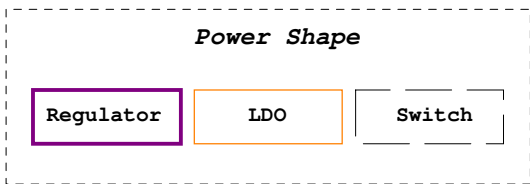
OAK14 Chief River POWER UP SEQUENCE DIAGRAM



Power Up Sequence: [-8] ~ [13]



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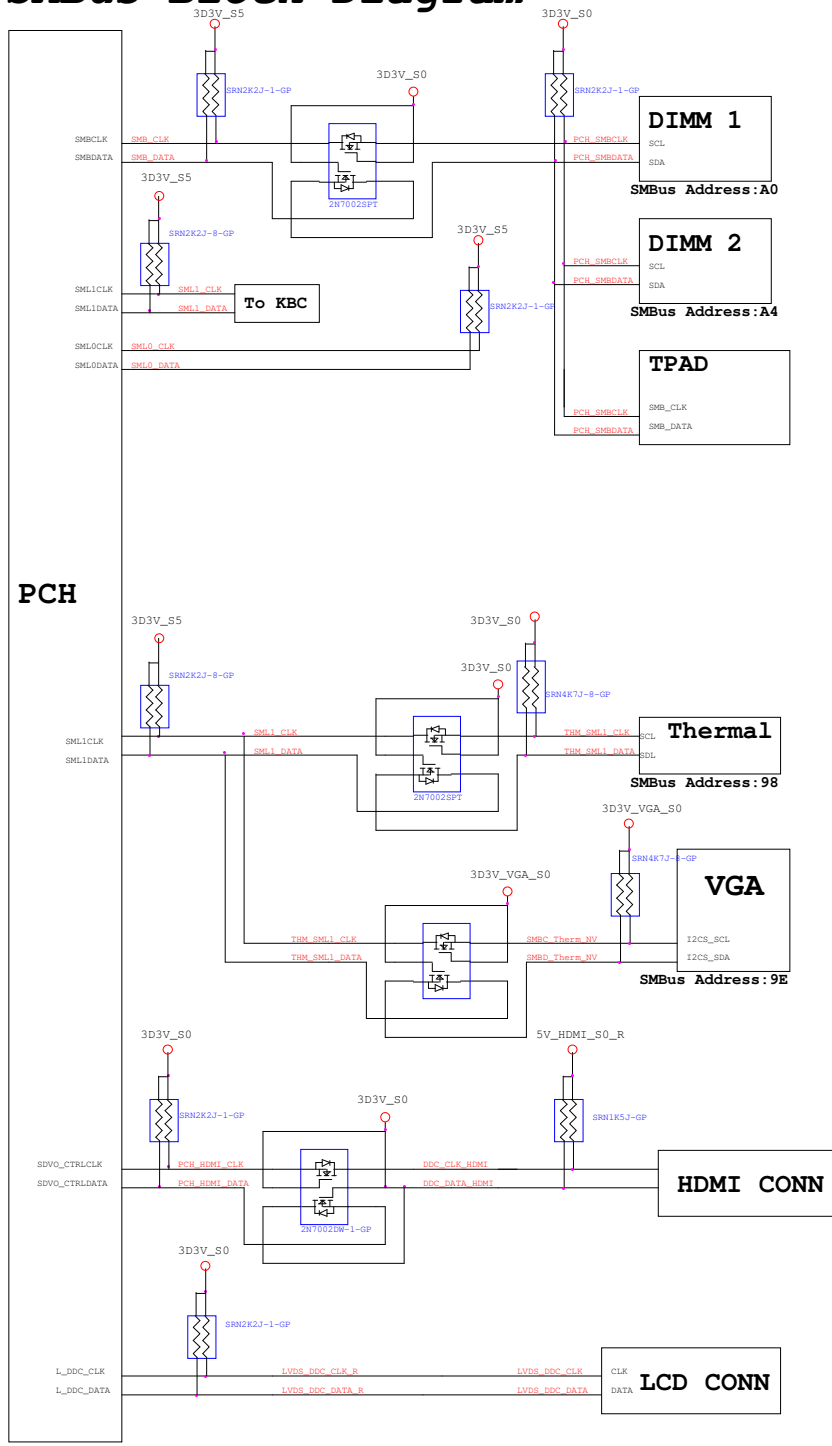
M14 DIS

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

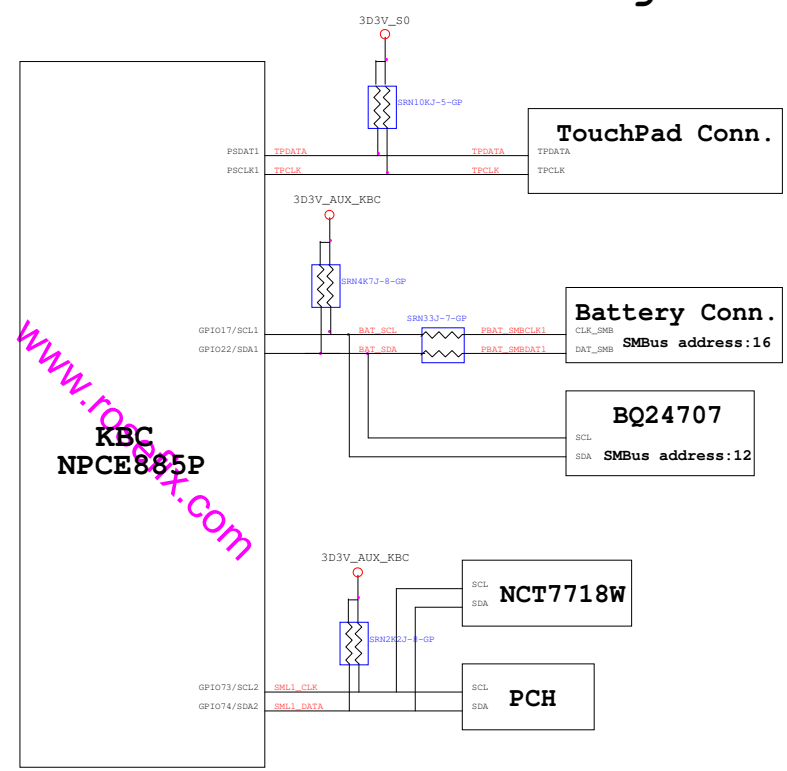
Title: **Power Block Diagram**

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PCH SMBus Block Diagram

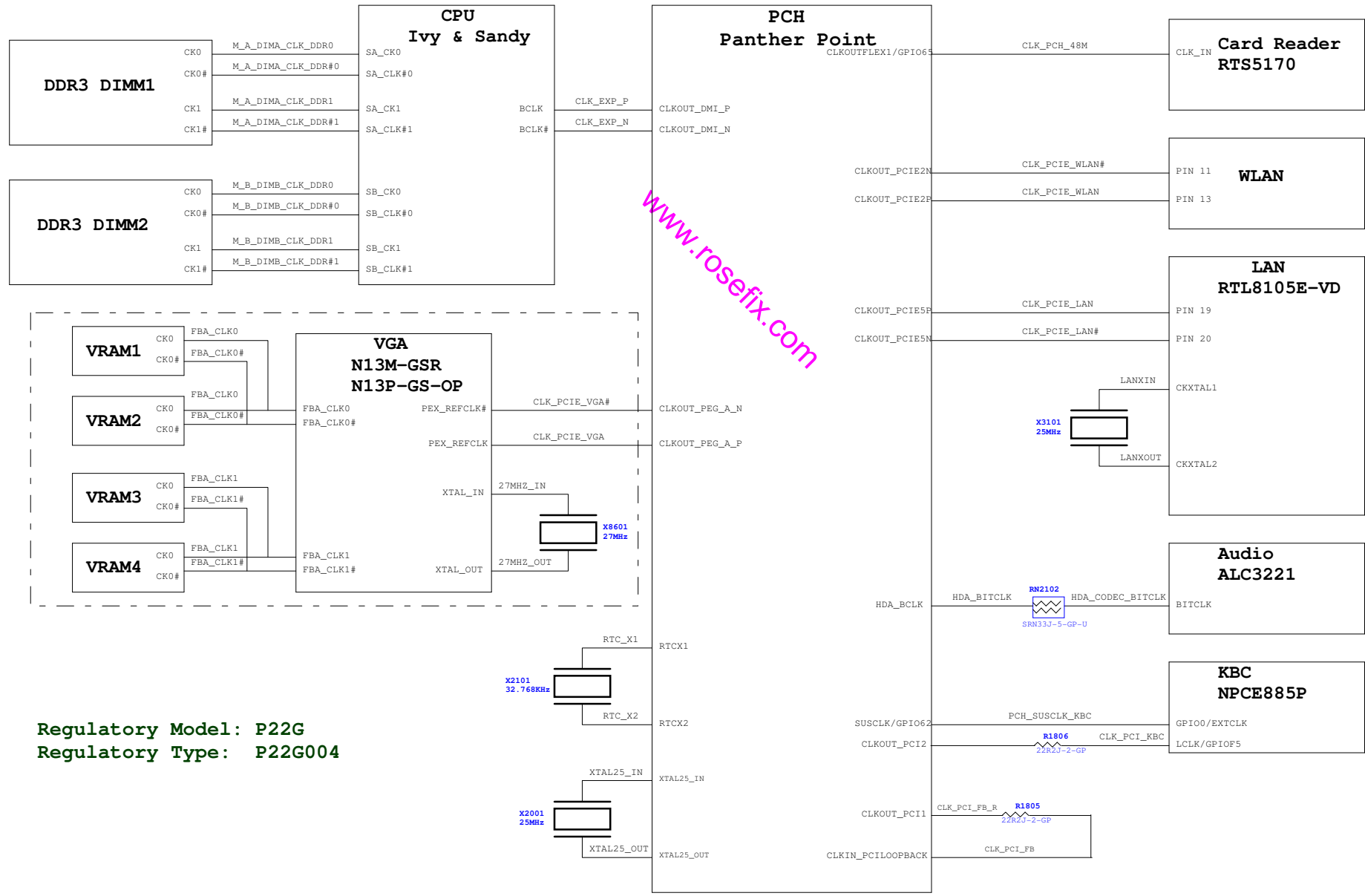


KBC SMBus Block Diagram



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KBC NPCE885P

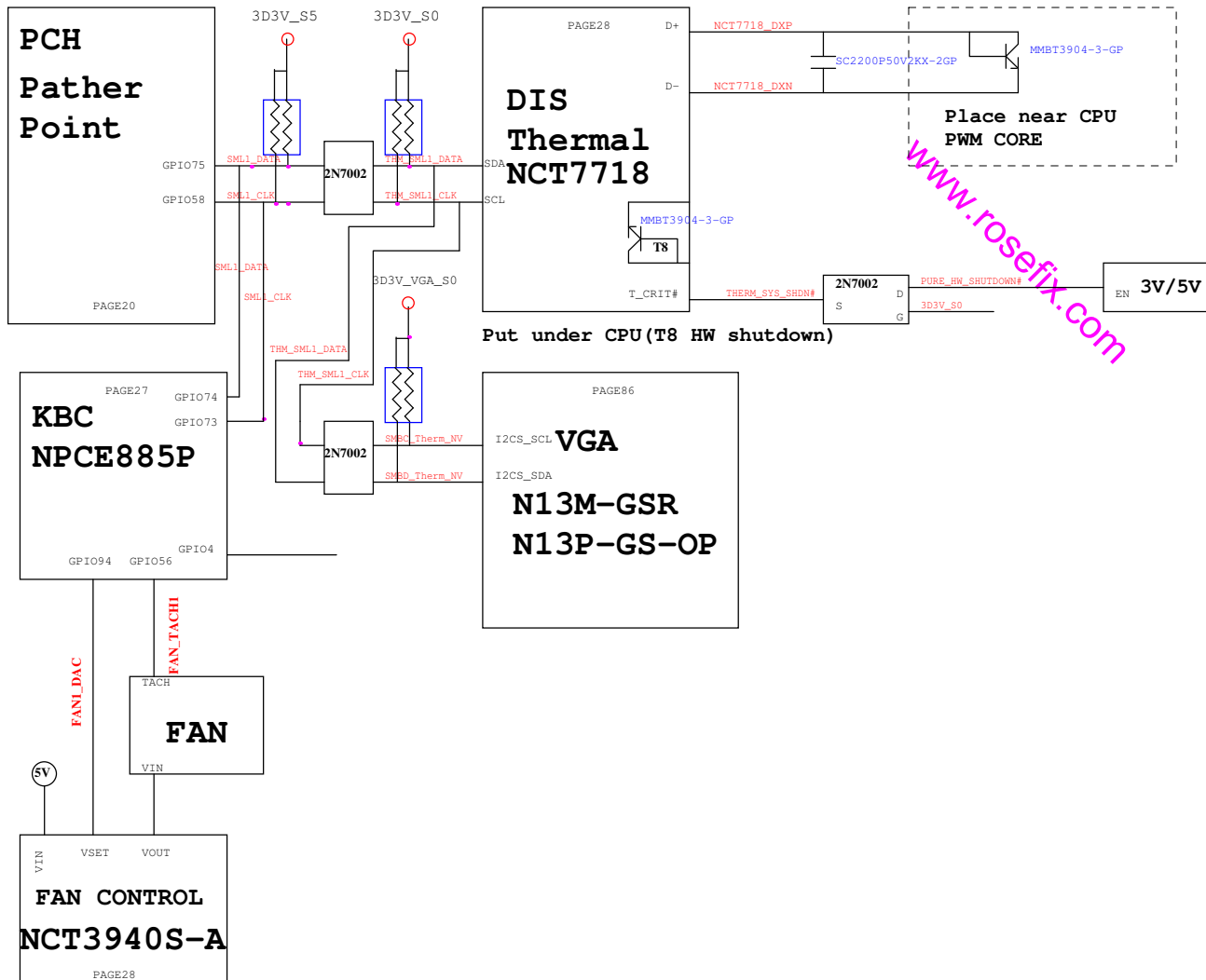
OAK14 DIS CLK Block Diagram



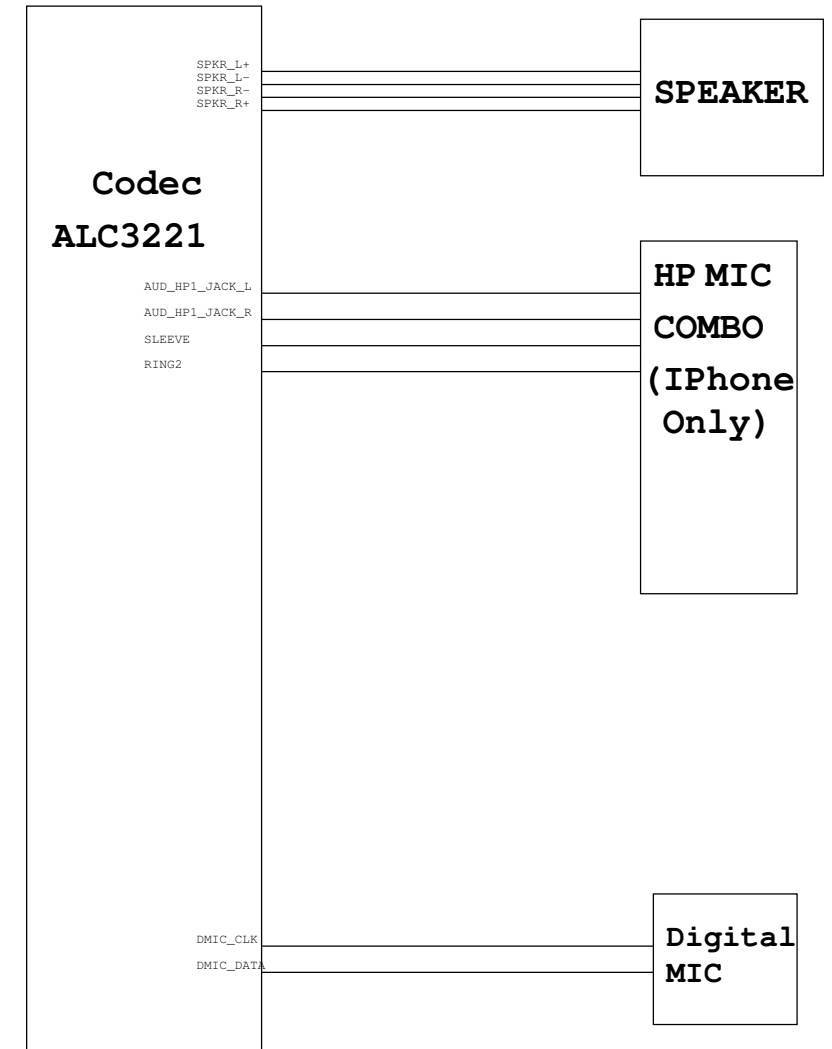
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Regulatory Model: P22G
Regulatory Type: P22G004

Thermal Block Diagram



Audio Block Diagram



M14 DIS

Version	Date	PAGE	Description of Required Change
X01	5/10	P38	Dummy R3818 R3813 for DT Mode
X01	5/10	P20	Change CLK_PCIE_WLAN_REQ# PU from 3D3V_S5 to 3D3V_S0 & change port 3 to port 2(non AOAC)
X01	5/10	P86	Dummy R8613 (for N13M-GS1 strappin)
X01	5/28		Update connector list(5/28) for X01
X01	5/30	P49	Add TPNL1 (USB20 port#3)
X01	5/30	P29	Add delay circuit for Audio Jack JD pin
X01	5/30	P59	Change RJ45 Conn
X01	6/1	P38	Stuff PQ3801 PR3814 PR3815 for DT mode
X01	6/1	P37	Change R3713 to 10k for sequence timing
X01	6/1	P31	Change R3118 to 20k for sequence timing
X01	6/1	P69	Add KBL1 and keyboard backlight function
X01	6/1	P27	Change PCB version from X00 to X01
X01	6/5	P46	Fine tune the level of 1d5v_vga_s0: PR4601 (47K -> 57.6K)
X01	6/5	P58	Add TVS at combo JACK & RJ45 for EMI request
X01	6/5	P18	Move the KB_LED_BL_DET from GPIO5 to GPIO4
X01	6/11		Implement EMI change request 6/11
X01	6/11	P27	Delete RN2702 , DY R2716, Stuff R2717 For DT Mode
X01	6/11	P21	Add VRAM detect circuit at PCH_GPIO57
X01	6/11	P51	Change D5101 to 83.00056.G11 for lower internal cap
X01	6/12	P18	Move USB2.0 from port4# to port2#
X01	6/12	P49	Modify CAMERA1 to CAM1
X01	6/13	P61	Separate the USB3.0 PWR to USB30_VCCA & USB30_VCCB
X01	6/14	P49	Add LCD Back Light control circuit from KBC GPIO33
X01	6/14	P40	implement Power team request item
X01	6/15	P31	Change C3102=C3103=18pf for Xtal vendor request
X01	6/15	P62	Modify cap value for USB30_VCCA & USB30_VCCB
X01	6/18	P69	DY the Keyboard back light parts, add R6916 for PU
X01	6/18	P61	Change TC6102 & TC6104 to 78.10710.52L; TC6103 to 79.10710.60L
X01	6/18	P20	Move WLAN from PCIE 4# to PCIE 3#
X01	6/18	P51	implement EMI team request item (6/15)
X01	6/18	P69	Remove R6916 Stuff R6912
X01	6/18	P69	Change Q6801~Q6805 & Q6902 to 84.00144.P11

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