BLOCK DIAGRAM

FAN /THERMAL
EMC2103-2
Page32

Note :DP means Display Port Interface

Note :DDR3 1.35V support 1066~1333 MHz
DDR3 1.5V support 1066~1600 MHz

DDR III
SO-DIMM 0
SO-DIMM 1
Memory size MAX is 16GB per channel

Dual Channel
1333/1600 MHz

DDR SYSTEM MEMORY

AMD
Support 45W/ 35W TDP
Socket FS1-Llano
APU (CPU + GPU)
uPGA 722 pin

DP0/TXPN[0:3]
DP2/PCI-E 0_3
GPP PCIEX1
GPP PCIEX1
DP4_DP5/PCI-E 8_11
UMI
DP1/TXPN[0:3]

DP0 → ANX3110 → LVDS → LVDS
DP to LVDS

DP2 → HDMI

PCI-Express Gen2
5GT/s
PCIE X8
ATI GPU
Seymour XT M2
VRAM
512M/1G
X'TAL
27.0MHz

RealTek
RTL8105
Page31
PCIEx1
GPP PCIE0
2.5GT/s
PCI-Express Gen1
X'TAL
25MHz
Transformer
RJ45

PCI-Express Gen1
2.5GT/s
PCIEx1
GPP PCIE1
Mini Card
Wlan/WiFi
USB 2.0

X4 UMI interface
2.5GT/s
UMI
DP1

AMD
FCH
Hudson-M3
SATA Gen3
SATA Gen3
SATA Gen2
USB2.0
USB3.0/2.0
RTC
PCI-E
FCBGA 656 pin
HDA
LPC
SPI
LPC

DP to VGA
VGA
VGA

HDD (SATA)
ODD (SATA)
SATA0
SATA1
6Gbit/s
6Gbit/s

eSATA/USB Port x 1
SATA3
3Gbit/s
USB 2.0
USB 2.0

USB 3.0/2.0 Combo X1
Reserved
USB 3.0/2.0

X'TAL
32.768KHz

USB 2.0 X3
USB 2.0

Azalia (HDA bus)

Bluetooth
USB 2.0

CCD
USB 2.0

CardReader
RTS5139
USB 2.0

7-IN-1 Card read
CONN

Audio CODEC
RTL ALC269Q-VB6-GR
Page29

SPI ROM

EC
(ITE 8518E)
X'TAL
32.768KHz

HP Jack
MIC Jack
SPK
DMIC

SPI ROM
Touch Pad
Keyboard

Discharge	Page37
Charge	Page38
DDR3/0.75V (RT8207)	Page39
3V/5V (RT8206)	Page40
1.1V/+1.0V_GPU	Page41
+1.2V_VDDPR/+2.5	Page42
VDD/+VDDNB_CORE	Page43
GFX_CORE (OZ8117)	Page44
+1.8V_GPU (HPA00835RTER)	Page45

PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	System Block Diagram	1A

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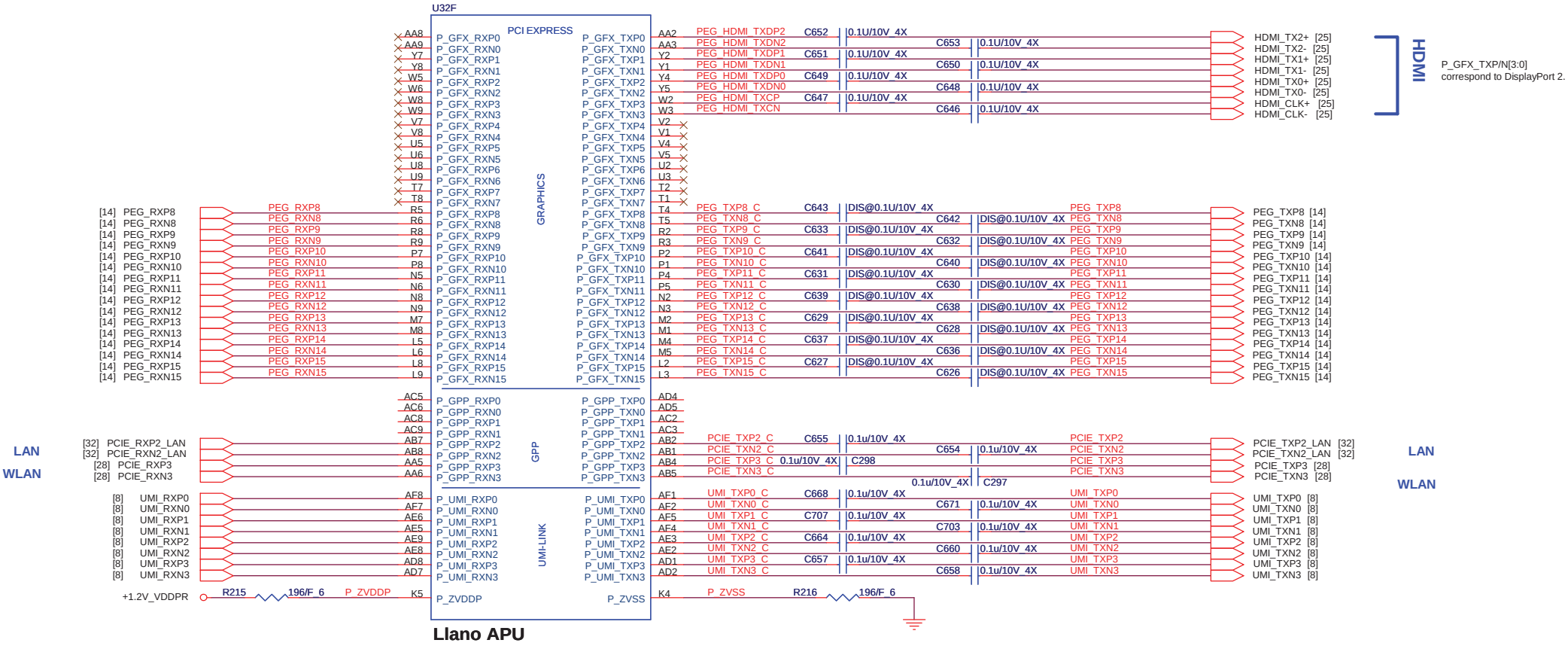
[4,5,9,23,38,43] +1.2V_VDDPR

02



Size	Document Number	Rev
	Llano PCIE/UMI/GPP	1A
Date: Thursday, April 28, 2011	Sheet 2 of 49	

PROJECT : KL6B/C

Quanta Computer Inc.

[4,5,6,9,10,12,13,37,38,40,42] +1.5V_SUS

U32A

MEMORY CHANNEL A

[12] M_A_A[15:0]

M_A_A0 U20
M_A_A1 R20
M_A_A2 R21
M_A_A3 P22
M_A_A4 P21
M_A_A5 N24
M_A_A6 N23
M_A_A7 N20
M_A_A8 N21
M_A_A9 M21
M_A_A10 U23
M_A_A11 M22
M_A_A12 L24
M_A_A13 AA25
M_A_A14 L21
M_A_A15 L20

[12] M_A_BS#[2..0]

M_A_BS#0 U24
M_A_BS#1 U21
M_A_BS#2 L23

[12] M_A_DM[7..0]

M_A_DM0 E14
M_A_DM1 J17
M_A_DM2 E21
M_A_DM3 F25
M_A_DM4 AD27
M_A_DM5 AC23
M_A_DM6 AD19
M_A_DM7 AC15

[12] M_A_DQSP0 G14
[12] M_A_DQSN0 H14
[12] M_A_DQSP1 G18
[12] M_A_DQSN1 H18
[12] M_A_DQSP2 J21
[12] M_A_DQSN2 H21
[12] M_A_DQSP3 E27
[12] M_A_DQSN3 E26
[12] M_A_DQSP4 AE26
[12] M_A_DQSN4 AD26
[12] M_A_DQSP5 AB22
[12] M_A_DQSN5 AA22
[12] M_A_DQSP6 AB18
[12] M_A_DQSN6 AA18
[12] M_A_DQSP7 AA14
[12] M_A_DQSN7 AA15

[12] M_A_CLKP0 T21
[12] M_A_CLKN0 T22
[12] M_A_CLKP1 R23
[12] M_A_CLKN1 R24

[12] M_A_CKE0 H28
[12] M_A_CKE1 H27

[12] M_A_ODT0 Y25
[12] M_A_ODT1 AA27

[12] M_A_CS#0 V22
[12] M_A_CS#1 AA26

[12] M_A_RAS# V21
[12] M_A_CAS# W24
[12] M_A_WE# W23

[12] M_A_RST# H25

[12] M_A_EVENT# T24

+M_VREF W20

+1.5V_SUS R303 39.2/F_4 +M_ZVDDIO W21

Place close to APU within 1"

MA_ADD0 MA_ADD1 MA_ADD2 MA_ADD3 MA_ADD4 MA_ADD5 MA_ADD6 MA_ADD7 MA_ADD8 MA_ADD9 MA_ADD10 MA_ADD11 MA_ADD12 MA_ADD13 MA_ADD14 MA_ADD15
MA_BANK0 MA_BANK1 MA_BANK2
MA_DM0 MA_DM1 MA_DM2 MA_DM3 MA_DM4 MA_DM5 MA_DM6 MA_DM7
MA_DQS_H0 MA_DQS_L0 MA_DQS_H1 MA_DQS_L1 MA_DQS_H2 MA_DQS_L2 MA_DQS_H3 MA_DQS_L3 MA_DQS_H4 MA_DQS_L4 MA_DQS_H5 MA_DQS_L5 MA_DQS_H6 MA_DQS_L6 MA_DQS_H7 MA_DQS_L7
MA_CLK_H0 MA_CLK_L0 MA_CLK_H1 MA_CLK_L1
MA_CKE0 MA_CKE1
MA_ODT0 MA_ODT1
MA_CS_L0 MA_CS_L1
MA_RAS_L MA_CAS_L MA_WE_L
MA_RESET_L MA_EVENT_L
M_VREF
M_ZVDDIO

MA_DATA0 MA_DATA1 MA_DATA2 MA_DATA3 MA_DATA4 MA_DATA5 MA_DATA6 MA_DATA7 MA_DATA8 MA_DATA9 MA_DATA10 MA_DATA11 MA_DATA12 MA_DATA13 MA_DATA14 MA_DATA15 MA_DATA16 MA_DATA17 MA_DATA18 MA_DATA19 MA_DATA20 MA_DATA21 MA_DATA22 MA_DATA23 MA_DATA24 MA_DATA25 MA_DATA26 MA_DATA27 MA_DATA28 MA_DATA29 MA_DATA30 MA_DATA31 MA_DATA32 MA_DATA33 MA_DATA34 MA_DATA35 MA_DATA36 MA_DATA37 MA_DATA38 MA_DATA39 MA_DATA40 MA_DATA41 MA_DATA42 MA_DATA43 MA_DATA44 MA_DATA45 MA_DATA46 MA_DATA47 MA_DATA48 MA_DATA49 MA_DATA50 MA_DATA51 MA_DATA52 MA_DATA53 MA_DATA54 MA_DATA55 MA_DATA56 MA_DATA57 MA_DATA58 MA_DATA59 MA_DATA60 MA_DATA61 MA_DATA62 MA_DATA63

M_A_DQ[0..63] [12]

M_A_DQ0 E13
M_A_DQ1 J13
M_A_DQ2 H15
M_A_DQ3 J15
M_A_DQ4 H13
M_A_DQ5 F13
M_A_DQ6 F15
M_A_DQ7 E15
M_A_DQ8 H17
M_A_DQ9 F17
M_A_DQ10 E19
M_A_DQ11 J19
M_A_DQ12 G16
M_A_DQ13 H16
M_A_DQ14 H19
M_A_DQ15 F19
M_A_DQ16 H20
M_A_DQ17 F21
M_A_DQ18 J23
M_A_DQ19 H23
M_A_DQ20 G20
M_A_DQ21 E20
M_A_DQ22 G22
M_A_DQ23 H22
M_A_DQ24 G24
M_A_DQ25 E25
M_A_DQ26 G27
M_A_DQ27 G26
M_A_DQ28 F23
M_A_DQ29 H24
M_A_DQ30 E28
M_A_DQ31 F27
M_A_DQ32 AB28
M_A_DQ33 AC27
M_A_DQ34 AD25
M_A_DQ35 AA24
M_A_DQ36 AE28
M_A_DQ37 AD28
M_A_DQ38 AB26
M_A_DQ39 AC25
M_A_DQ40 Y23
M_A_DQ41 AA23
M_A_DQ42 Y21
M_A_DQ43 AA20
M_A_DQ44 AB24
M_A_DQ45 AD24
M_A_DQ46 AA21
M_A_DQ47 AC21
M_A_DQ48 AA19
M_A_DQ49 AC19
M_A_DQ50 AC17
M_A_DQ51 AA17
M_A_DQ52 AB20
M_A_DQ53 Y19
M_A_DQ54 AD18
M_A_DQ55 AD17
M_A_DQ56 AA16
M_A_DQ57 Y15
M_A_DQ58 AA13
M_A_DQ59 AC13
M_A_DQ60 Y17
M_A_DQ61 AB16
M_A_DQ62 AB14
M_A_DQ63 Y13

Llano APU

Soldermask openings for all bottom side vias/TPs under FS1

U32B

MEMORY CHANNEL B

[13] M_B_A[15:0]

M_B_A0 T27
M_B_A1 P24
M_B_A2 P25
M_B_A3 N27
M_B_A4 N26
M_B_A5 M28
M_B_A6 M27
M_B_A7 M24
M_B_A8 M25
M_B_A9 L26
M_B_A10 U26
M_B_A11 L27
M_B_A12 K27
M_B_A13 W26
M_B_A14 K25
M_B_A15 K24

[13] M_B_BS#[2..0]

M_B_BS#0 U27
M_B_BS#1 T28
M_B_BS#2 K28

[13] M_B_DM[7..0]

M_B_DM0 D14
M_B_DM1 A18
M_B_DM2 A22
M_B_DM3 C25
M_B_DM4 AE25
M_B_DM5 AG22
M_B_DM6 AH18
M_B_DM7 AD14

[13] M_B_DQSP0 C15
[13] M_B_DQSN0 B15
[13] M_B_DQSP1 E18
[13] M_B_DQSN1 D18
[13] M_B_DQSP2 E22
[13] M_B_DQSN2 D22
[13] M_B_DQSP3 B26
[13] M_B_DQSN3 A26
[13] M_B_DQSP4 AG24
[13] M_B_DQSN4 AG25
[13] M_B_DQSP5 AG21
[13] M_B_DQSN5 AF21
[13] M_B_DQSP6 AG17
[13] M_B_DQSN6 AG18
[13] M_B_DQSP7 AH14
[13] M_B_DQSN7 AG14

[13] M_B_CLKP0 R26
[13] M_B_CLKN0 R27
[13] M_B_CLKP1 P27
[13] M_B_CLKN1 P28

[13] M_B_CKE0 J26
[13] M_B_CKE1 J27

[13] M_B_ODT0 W27
[13] M_B_ODT1 Y28

[13] M_B_CS#0 V25
[13] M_B_CS#1 Y27

[13] M_B_RAS# V24
[13] M_B_CAS# V27
[13] M_B_WE# V28

[13] M_B_RST# J25

[13] M_B_EVENT# T25

+1.5V_SUS

R355 1K/F_4

MB_ADD0 MB_ADD1 MB_ADD2 MB_ADD3 MB_ADD4 MB_ADD5 MB_ADD6 MB_ADD7 MB_ADD8 MB_ADD9 MB_ADD10 MB_ADD11 MB_ADD12 MB_ADD13 MB_ADD14 MB_ADD15
MB_BANK0 MB_BANK1 MB_BANK2
MB_DM0 MB_DM1 MB_DM2 MB_DM3 MB_DM4 MB_DM5 MB_DM6 MB_DM7
MB_DQS_H0 MB_DQS_L0 MB_DQS_H1 MB_DQS_L1 MB_DQS_H2 MB_DQS_L2 MB_DQS_H3 MB_DQS_L3 MB_DQS_H4 MB_DQS_L4 MB_DQS_H5 MB_DQS_L5 MB_DQS_H6 MB_DQS_L6 MB_DQS_H7 MB_DQS_L7
MB_CLK_H0 MB_CLK_L0 MB_CLK_H1 MB_CLK_L1
MB_CKE0 MB_CKE1
MB_ODT0 MB_ODT1
MB_CS_L0 MB_CS_L1
MB_RAS_L MB_CAS_L MB_WE_L
MB_RESET_L MB_EVENT_L

MB_DATA0 MB_DATA1 MB_DATA2 MB_DATA3 MB_DATA4 MB_DATA5 MB_DATA6 MB_DATA7 MB_DATA8 MB_DATA9 MB_DATA10 MB_DATA11 MB_DATA12 MB_DATA13 MB_DATA14 MB_DATA15 MB_DATA16 MB_DATA17 MB_DATA18 MB_DATA19 MB_DATA20 MB_DATA21 MB_DATA22 MB_DATA23 MB_DATA24 MB_DATA25 MB_DATA26 MB_DATA27 MB_DATA28 MB_DATA29 MB_DATA30 MB_DATA31 MB_DATA32 MB_DATA33 MB_DATA34 MB_DATA35 MB_DATA36 MB_DATA37 MB_DATA38 MB_DATA39 MB_DATA40 MB_DATA41 MB_DATA42 MB_DATA43 MB_DATA44 MB_DATA45 MB_DATA46 MB_DATA47 MB_DATA48 MB_DATA49 MB_DATA50 MB_DATA51 MB_DATA52 MB_DATA53 MB_DATA54 MB_DATA55 MB_DATA56 MB_DATA57 MB_DATA58 MB_DATA59 MB_DATA60 MB_DATA61 MB_DATA62 MB_DATA63

M_B_DQ[0..63] [13]

M_B_DQ0 A14
M_B_DQ1 B14
M_B_DQ2 D16
M_B_DQ3 E16
M_B_DQ4 B13
M_B_DQ5 C13
M_B_DQ6 B16
M_B_DQ7 A16
M_B_DQ8 C17
M_B_DQ9 B18
M_B_DQ10 B20
M_B_DQ11 A20
M_B_DQ12 E17
M_B_DQ13 B17
M_B_DQ14 B19
M_B_DQ15 C19
M_B_DQ16 C21
M_B_DQ17 B22
M_B_DQ18 C23
M_B_DQ19 A24
M_B_DQ20 D20
M_B_DQ21 B21
M_B_DQ22 F23
M_B_DQ23 B23
M_B_DQ24 E24
M_B_DQ25 B25
M_B_DQ26 B27
M_B_DQ27 D28
M_B_DQ28 B24
M_B_DQ29 D24
M_B_DQ30 D26
M_B_DQ31 C27
M_B_DQ32 AG26
M_B_DQ33 AH26
M_B_DQ34 AF23
M_B_DQ35 AG23
M_B_DQ36 AG27
M_B_DQ37 AF27
M_B_DQ38 AH24
M_B_DQ39 AE24
M_B_DQ40 AE22
M_B_DQ41 AH22
M_B_DQ42 AE20
M_B_DQ43 AH20
M_B_DQ44 AD23
M_B_DQ45 AD22
M_B_DQ46 AD21
M_B_DQ47 AD20
M_B_DQ48 AF19
M_B_DQ49 AE18
M_B_DQ50 AE16
M_B_DQ51 AH16
M_B_DQ52 AG20
M_B_DQ53 AG19
M_B_DQ54 AF17
M_B_DQ55 AD16
M_B_DQ56 AG15
M_B_DQ57 AD15
M_B_DQ58 AG13
M_B_DQ59 AD13
M_B_DQ60 AG16
M_B_DQ61 AF15
M_B_DQ62 AE14
M_B_DQ63 AF13

Llano APU

+1.5V_SUS

+M_VREF

R349 1K/F_4

R348 1K/F_4

C416 1000P/50V_4X

C417 0.1u/10V_4X

PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	Llano DDR3 MEM I/F	1A
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DP0 to LVDS

DP1 to Hudson-M3 VGA output

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

These TP near the APU

Llano APU

B_EC_05

EC_A_01

Remove APU_TEST6

LVDS

VGA

HDMI

PROJECT : KL6B/C

Quanta Computer Inc.

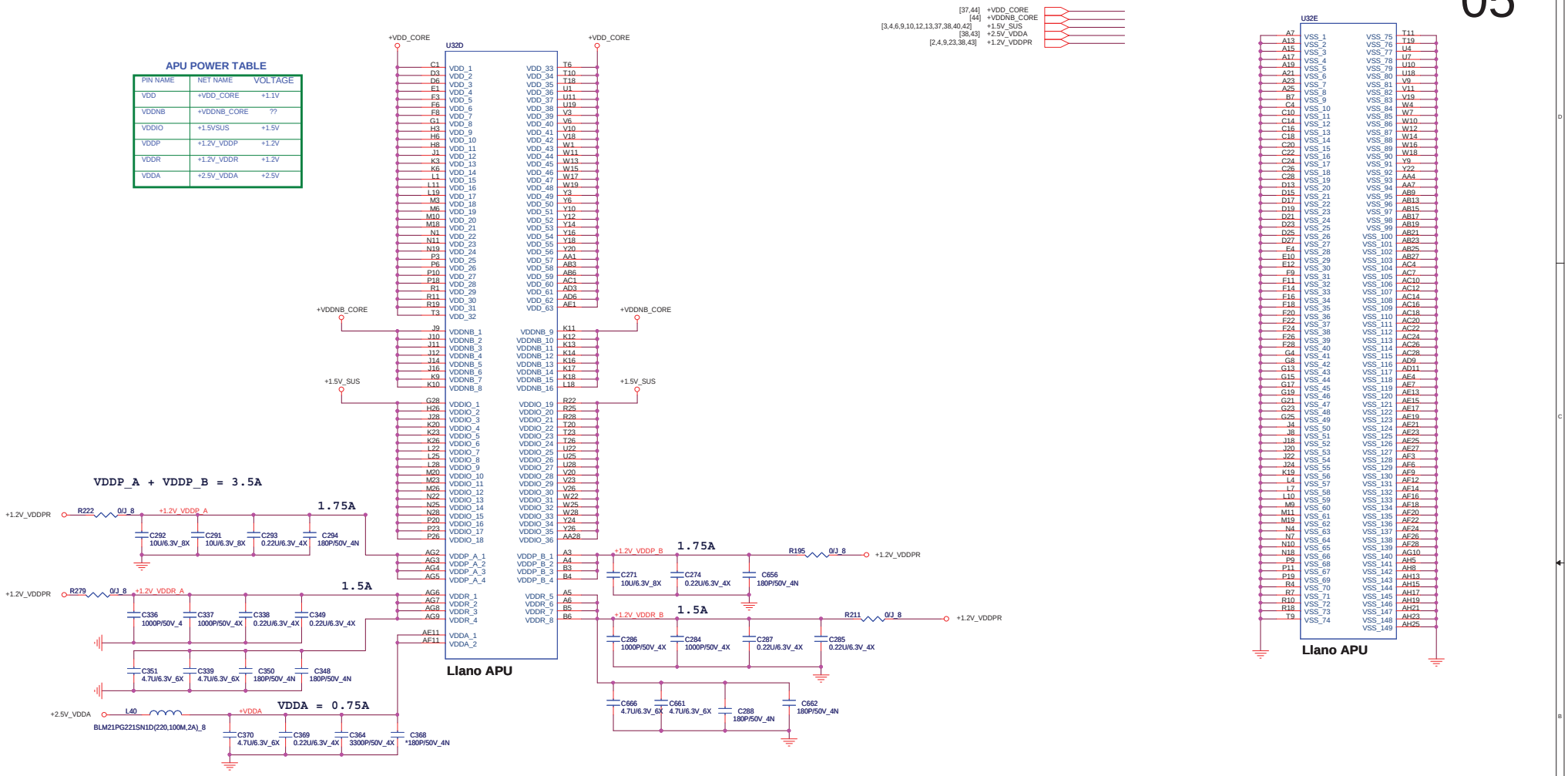
Llano Display/Misc

Size | Document Number | Rev 1A

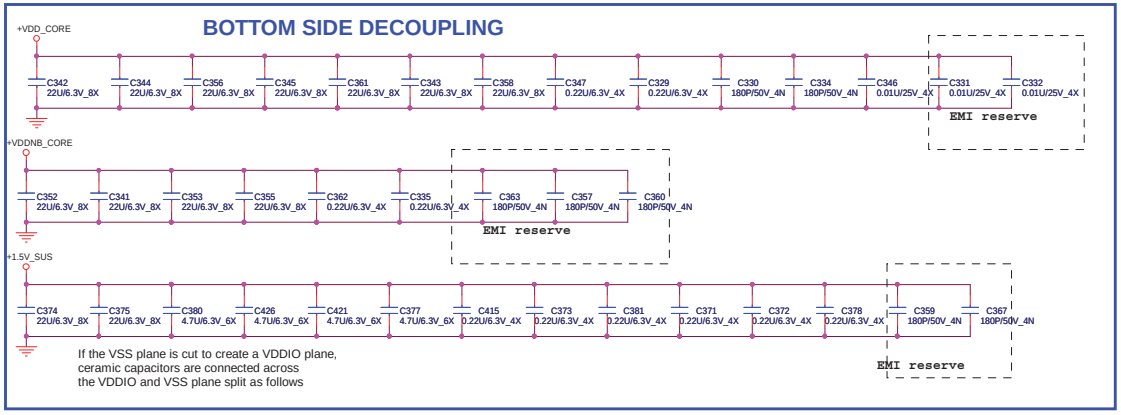
Date: Thursday, April 28, 2011 | Sheet 4 of 49

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



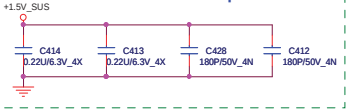
BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	Llano POWER/GND	1A

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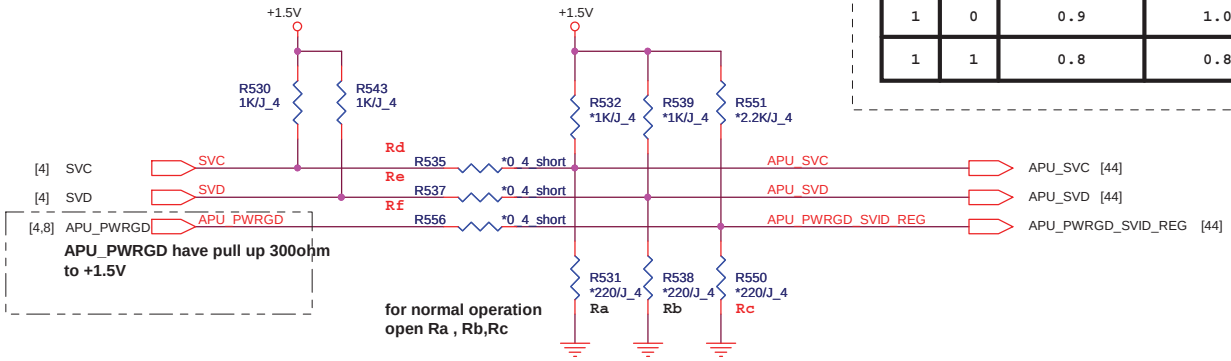
VID Override Circuit

		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



HDT+ Connector

Debug only

[4,8,9,23,25,28,29,42] +1.5V
[3,4,5,9,10,12,13,37,38,40,42] +1.5V_SUS

PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	Llano DEBUG&OTHER	1A
Date: Thursday, April 28, 2011	Sheet 6 of 49	

NC,no install by default

remove pull hi
(chip internal
have pull hi)

R526 *2.2K/J_4 FCH_TEST0
R524 *2.2K/J_4 FCH_TEST1
R517 *2.2K/J_4 FCH_TEST2

R513 2.2K/J_4 SMB_RUN_CLK
R514 2.2K/J_4 SMB_RUN_DAT
R295 *1K/J_4 SYS_RST#
G1 *SHORT_PAD

R518 *10K/J_4 VGA_PD
R529 10K/J_4 SCL1
R536 10K/J_4 SDA1
R574 10K/J_4 SCL2
R575 10K/J_4 SDA2
R582 10K/J_4 SCL3_LV
R581 10K/J_4 SDA3_LV

VGA_PD for power control

EC_A_15
R546 4.7K/J_4 APU_THERMTRIP#
R553 10K/J_4 USB_OC1#
R525 10K/J_4 USB_OC0#
R259 10K/J_4 USB_OC2#
R534 10K/J_4 USB_OC6#

R325 4.7K/J_4 ODD_PRSNT#
R540 *10K/J_4 EC_EXT_SCI#
R308 *10K/J_4 EC_EXT_SMI#

R288 10K/J_4 PCIE_WAKE#
R294 2.2K/J_4 DNBSWON#

Note:LLB#, WAKE# and PWR_BTN need pull up to 3.3V_S5+ only if S5+ mode is supported

R163 *22K/J_4
C207 2.2U/6.3V_6X
R164 0/J_4
R165 *20K/J_4
Q21 *DISR@2N7002E
[36] RSMRST#_EC
RSMRST_GATE# from EC
RSMRST#
RSMRST_GATE#

U15A
HUDSON-M2
Part 4 of 5
Hudson-M3

T124 SLP_S3#
T121 SLP_S5#
[36] SLP_S3#
[36] SLP_S5#
[36] DNBSWON#
[11] FCH_PWRGD
DNBSWON#
FCH_PWRGD
T76 T80 T123
FCH_TEST0
FCH_TEST1
FCH_TEST2
T120
[36] EC_A20GATE
[36] EC_KBRST#
[36] EC_EXT_SCI#
[36] EC_EXT_SMI#
T78
SYS_RST#
R287 *0_4 short
[28,32] PCIE_WAKE#
T122
R545 *0_4 short APU_THERMTRIP#
R176 10K/F_4 WD_PWRGD
[4] APU_THERMTRIP#
+3VO
RSMRST#
12/15 add
[31] BT_ON#
[32] PCIE_CLKREQ_LAN#
[35] CCD_ON#
R468 *0_4 short
B_EC_08
B_EC_01
T77
R169 *0_4 short
[30] SPKR
[12,13] SMB_RUN_CLK
[12,13] SMB_RUN_DAT
SMB_RUN_CLK
SMB_RUN_DAT
SCL1
SDA1
T65
[28] PCIE_CLKREQ_WLAN#
[24] LCD_BK_OFF
[10] VGA_PD
R521 *0_4 short GEVENT#7
[9] SPI_HOLD#
[15] FCH_PCIE_PEG_CLKREQ#
R506 *0/J_4

[31] USB_OC6#
[36] AC_PRESENT
[29,36] ODD_MDDA#
[29] ODD_PRSNT#
[29] USB_OC2#
[31] USB_OC1#
[31] USB_OC0#
R533 R256 R317 R258 R552 R528 *0_4 short
T11
T1

HD audio
interface is
+3V_S5 voltage
R237 *10K/F_4 ACZ_BCLK_R
ACZ_SDOUT_R
R241 R240 R249 R252 *10K/F_4
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2_R
ACZ_SDIN3_R
ACZ_SYNC_R
ACZ_RST#_R

T125 T127

For B stage, for password.
G3 *SHORT_PAD
R313 *10K/J_4
KSO_5

T93 T84 T89 T91 T88 T128 T130 T133 T86 T131 T94 T90 T81 T92 T85 T87 T83
KSO_0 KSO_1 KSO_2 KSO_3 KSO_4 KSO_5 KSO_6 KSO_7 KSO_8 KSO_9 KSO_10 KSO_11 KSO_12 KSO_13 KSO_14 KSO_15 KSO_16 KSO_17

Provided test points from checklist

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
GPIO
USB 2.0

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB MISC
USB 1.1

USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
USB 3.0

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

[4,6,8,9,10,11,12,13,19,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V
[4,8,10,24,29,32,34,35,36,38,39,40,41,43,46] +3VPCU
[9,10,11,28,35,38] +3V_S5
[10] +FCH_VDD_11_SSUSB_S

R321 11.8K/F_6
Note: USB P/N pairs with trace lengths up to 10"

USB#1 Daughter Board
USB#2 Right
Card Reader
USB 3.0 x1
Blue Tooth
WLAN
CCD
ESATA
USB 3.0 x1

EC_A_10

R315 R314 USB3@1K/F_4
+FCH_VDD_11_SSUSB_S
If USB 3.0 not implemented, left unconected

SMB_LV_CLK [4]
SMB_LV_DAT [4]
EC_PWM2 [11]
No need for GPIO200
USB_BUS_SW2
USB_BUS_SW3
T82
T134
INTEL_BT_OFF# [28]

Note: USB 3.0 1:1 MAP to USB2.0 PORT As Below:

SSUSB0+USB10	USB3.0 PORT 0
SSUSB1+USB11	USB3.0 PORT 1
SSUSB2+USB12	USB3.0 HEADER
SSUSB3+USB13	EXPRESSCARD

To Azalia

ACZ_SDOUT_R R231 33/J_4 ACZ_SDOUT [30]
ACZ_SYNC_R R212 33/J_4 ACZ_SYNC [30]
ACZ_BCLK_R R236 33/J_4 ACZ_BITCLK [30]
C307 *22P/50V_4N
ACZ_RST#_R R201 33/J_4 ACZ_RST# [30]
ACZ_SDIN0 ACZ_SDIN0 [30]

PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	Hudson-M3 GPIO/USB/AZ/RGMII	1A
Date: Thursday, April 28, 2011	Sheet 7 of 49	

HUDSON-M2

Part 1 of 5

U15E

Hudson-M3

RTC Circuitry(RTC)

RTC_BAT(RTC SOCKET-2032)

Card Reader

Note: CLK_FCH_SRCP/N is 100MHZ SSC (Pop RP9 if use external CLK gen)

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_PCIE_VGAP/N is 100MHZ SSC

Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable

Note: For external CLK gen mode, depop RP10/RP11/RP12/RP13/RP14/RP15/RP16

NOTE: The 0R serial resistor on FCH CLK pair must share Pad with the serial resistor close to EXT CLOCK GEN

RP12, PR18~RP23 need close to connect node

ALL CLOCK TEST POINT PLACE CLOSE TO DEVICE SIDE

PLACE C181~C188 CLOSE TO U5

APU_PCIE_RST# is for APU PCIE devices reset

FCH_GPP	DEVICE	CLKREQ#
GFX_CLK MXM3.0(via x16 slot)		CLK_REQG#
0	EXPRESS	0
1	PE0	1
2	PE2	2
3	LAN	3
4	PE1	4
5	X1DT	5
6	NA	NA
7	USB3.0	7
8	1394	8

INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).

PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	Hudson-M2 ACPI/PCI/CLOCK	1A

Date: Thursday, April 28, 2011 Sheet 8 of 49

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON-M2/M3

SATA PORTS DISTRIBUTION:
0, 2.5 INCH DISK DRIVER
1, SATA ODD
2, 2.5 INCH DISK DRIVER
3, eSATA
4-7, NOT USED

SATA HDD/SSD

SATA ODD

ESATA#1

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

U15B

HUDSON-M2 Part 2 of 5

Hudson-M3

WINBOND(4M): AKE391P0N00
MAX(4M): AKE39FP0Z02
Socket: DFHS08FS023

SPI Flash Socket

R place close to PCH

Change +1.5V_RUN to +1.5v

CRT Hot-plug

Integrated Clock Mode:
Leave unconnected.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU VGA SKU	H L					
Reserve		H L				
Reserve			H L			
Reserve				H L		
Reserve					H L	
Reserve						H L

PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	Hudson-M2 SATA/HWM/SPI	1A

Date: Thursday, April 28, 2011 Sheet 9 of 49

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

HUDSON-M2 Part 3 of 5

HUDSON-M2 Part 5 of 5

S5 plus mode

S5_3.3--3.3v standby power

S5_1.1V--1.1V standby power

CKVDD_1.1V--Internal clock Generator I/O power

PCIE_VDDR--PCIE I/O power

AVDD_SATA--SATA phy power

Checklist request one 1uF capacitor

C7490,C7447 0.1uF to Oohm for M2 FCH

32 mA Max

233 mA Max

PROJECT : KL6B/C

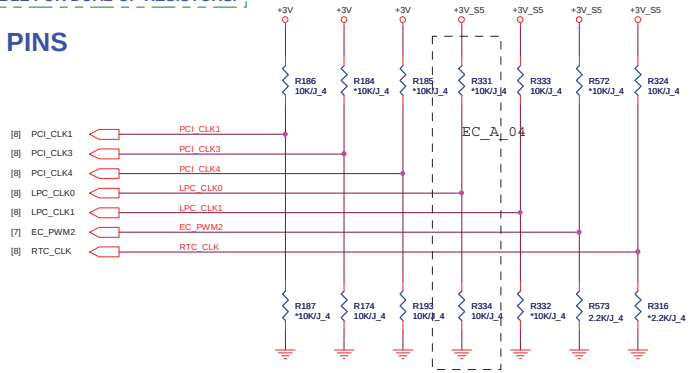
Quanta Computer Inc.

Size | Document Number: Hudson-M2 POWER/GND | Rev: 1A

Date: Thursday, April 28, 2011 | Sheet 10 of 49

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

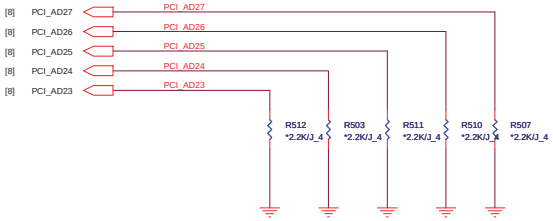


REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

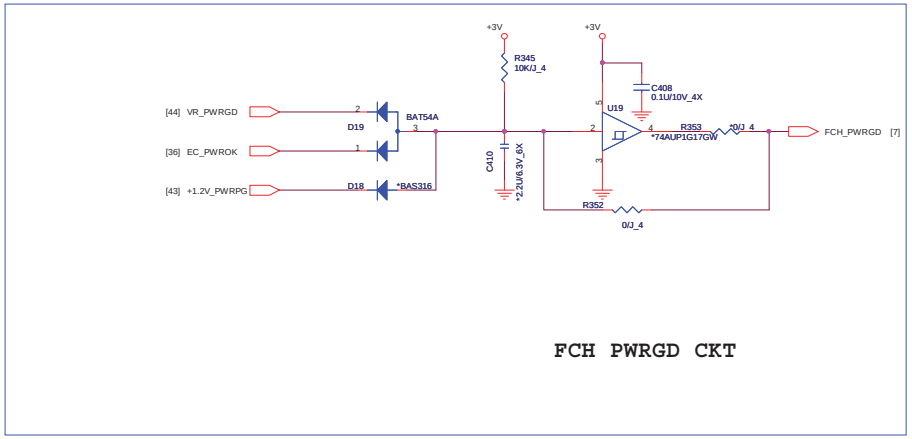
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

[4,6,7,8,9,10,12,13,19,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V
[7,9,10,28,35,38] +3V_S5

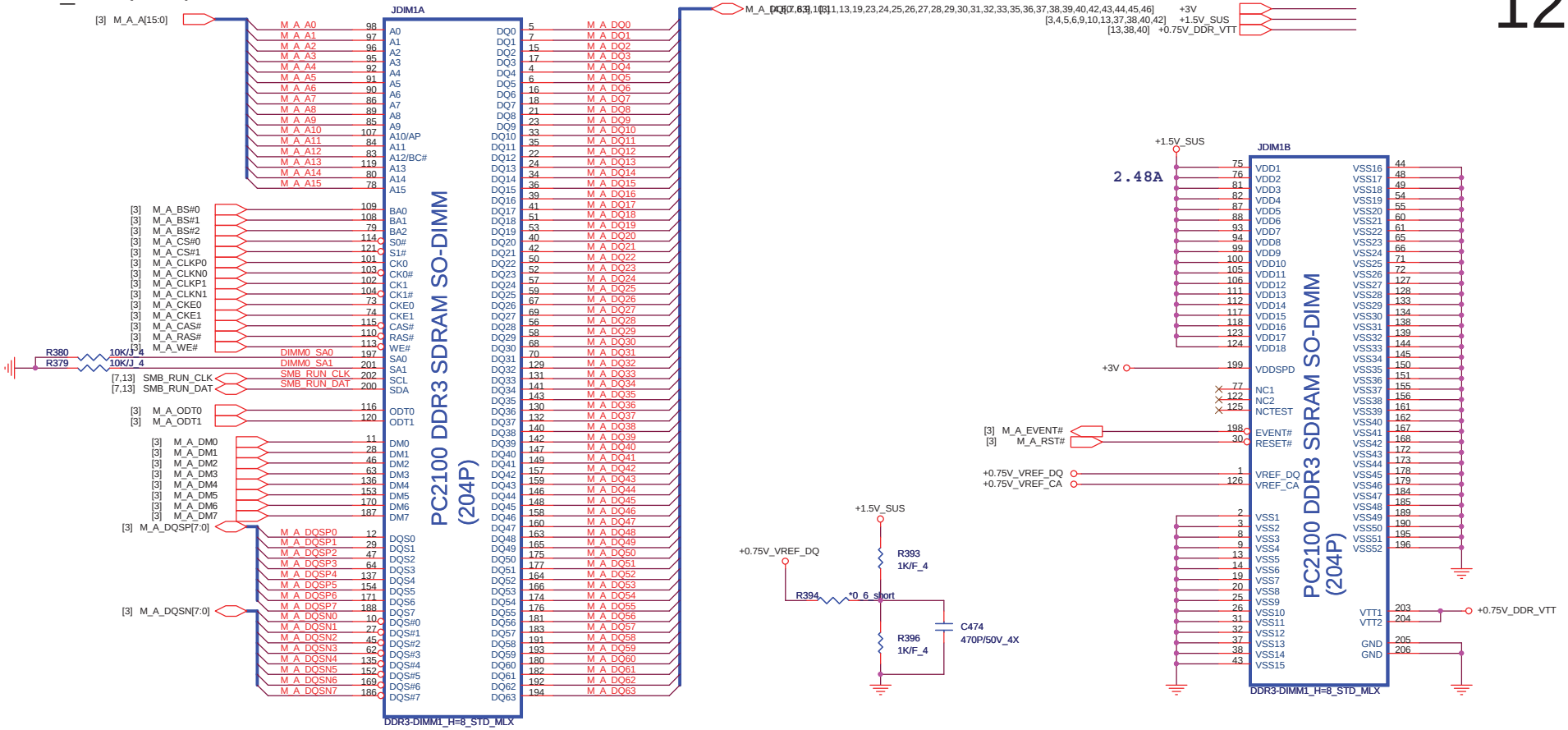


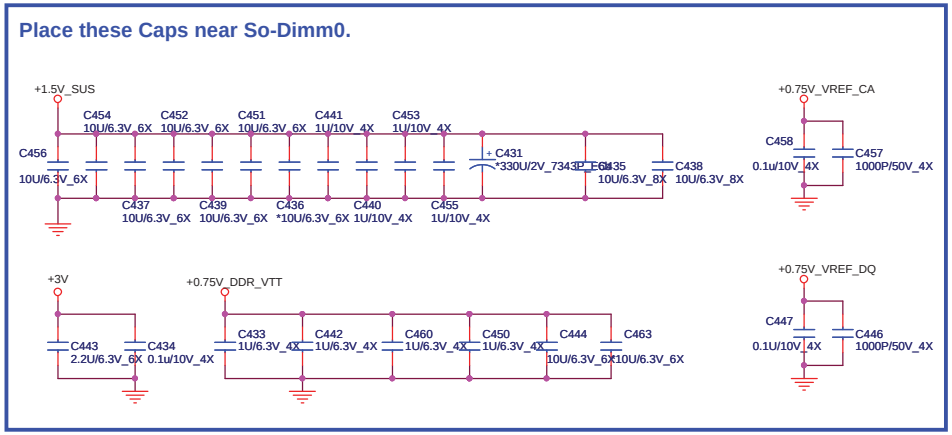
FCH PWRGD CKT

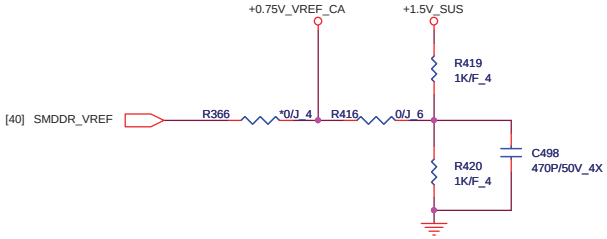
PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	Hudson-M2 STRAP/PWRGD	1A

Date: Thursday, April 28, 2011 Sheet 11 of 49



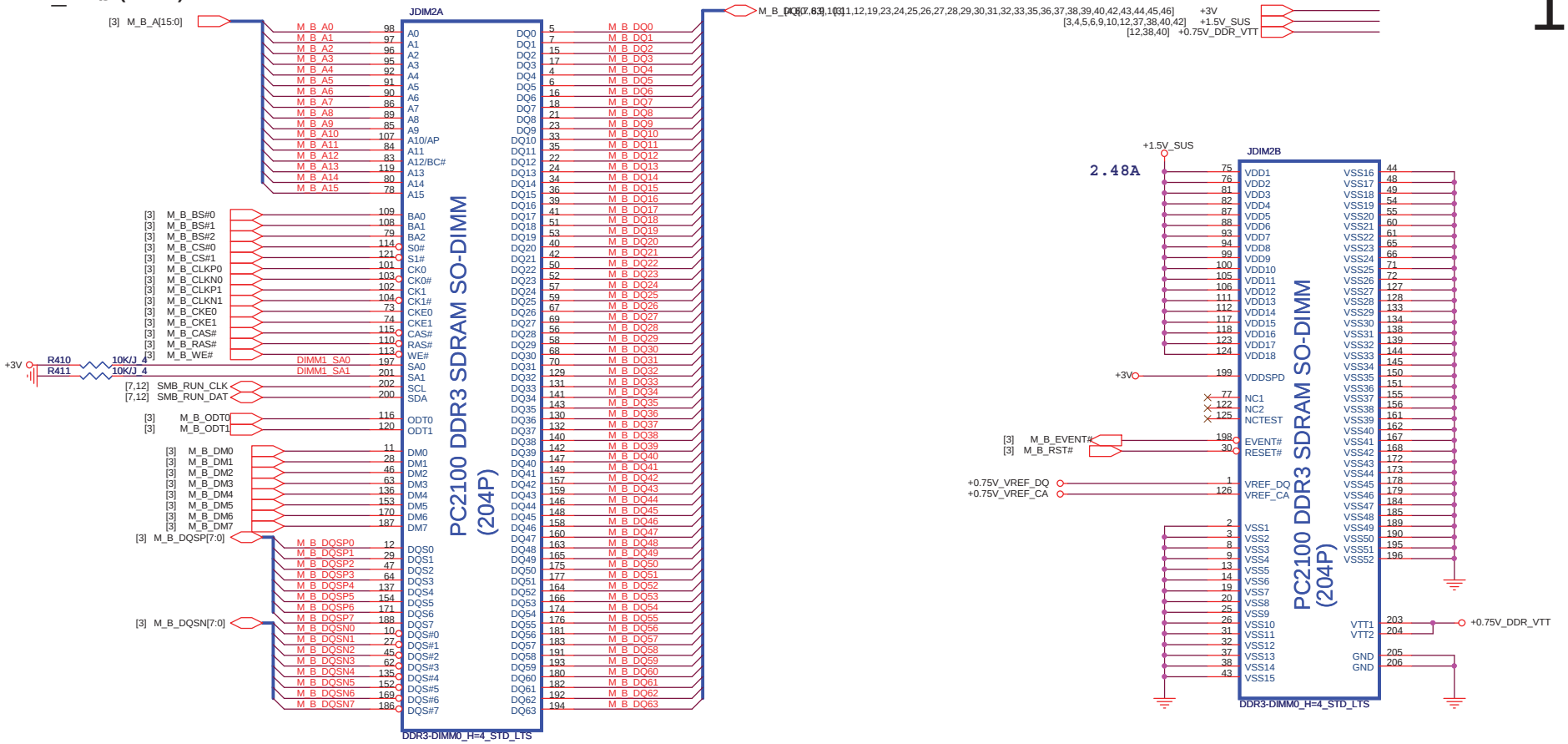


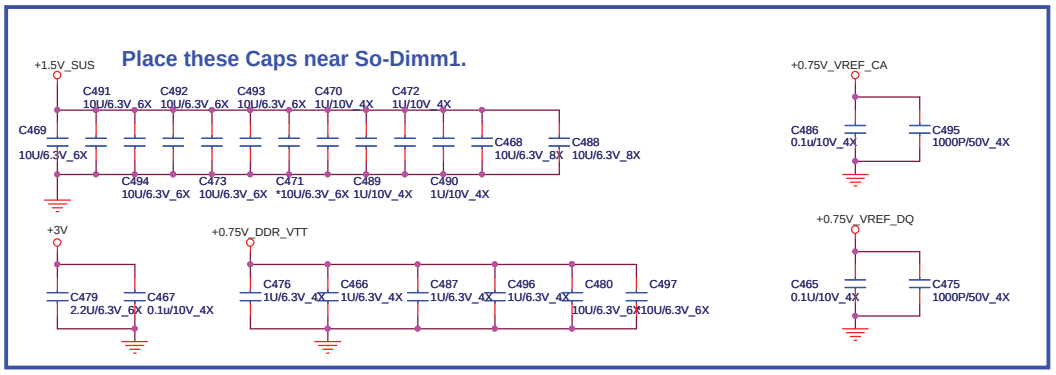


PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Thursday, April 28, 2011	Sheet 12 of 49	





PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

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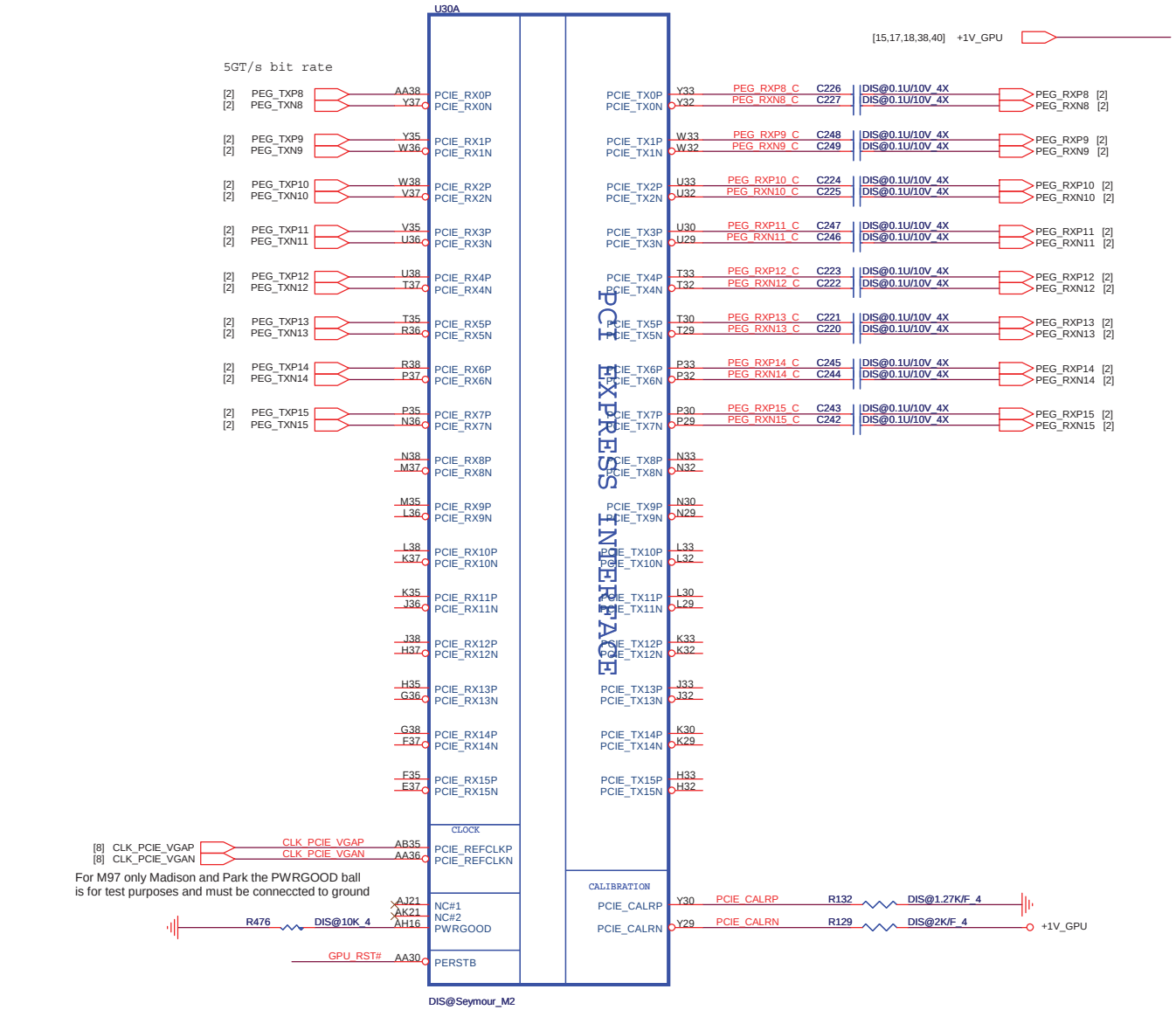
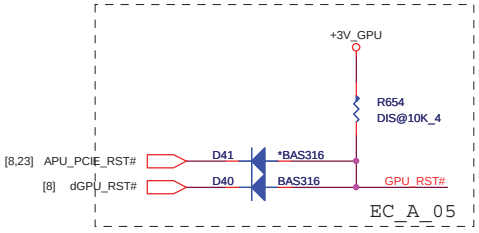
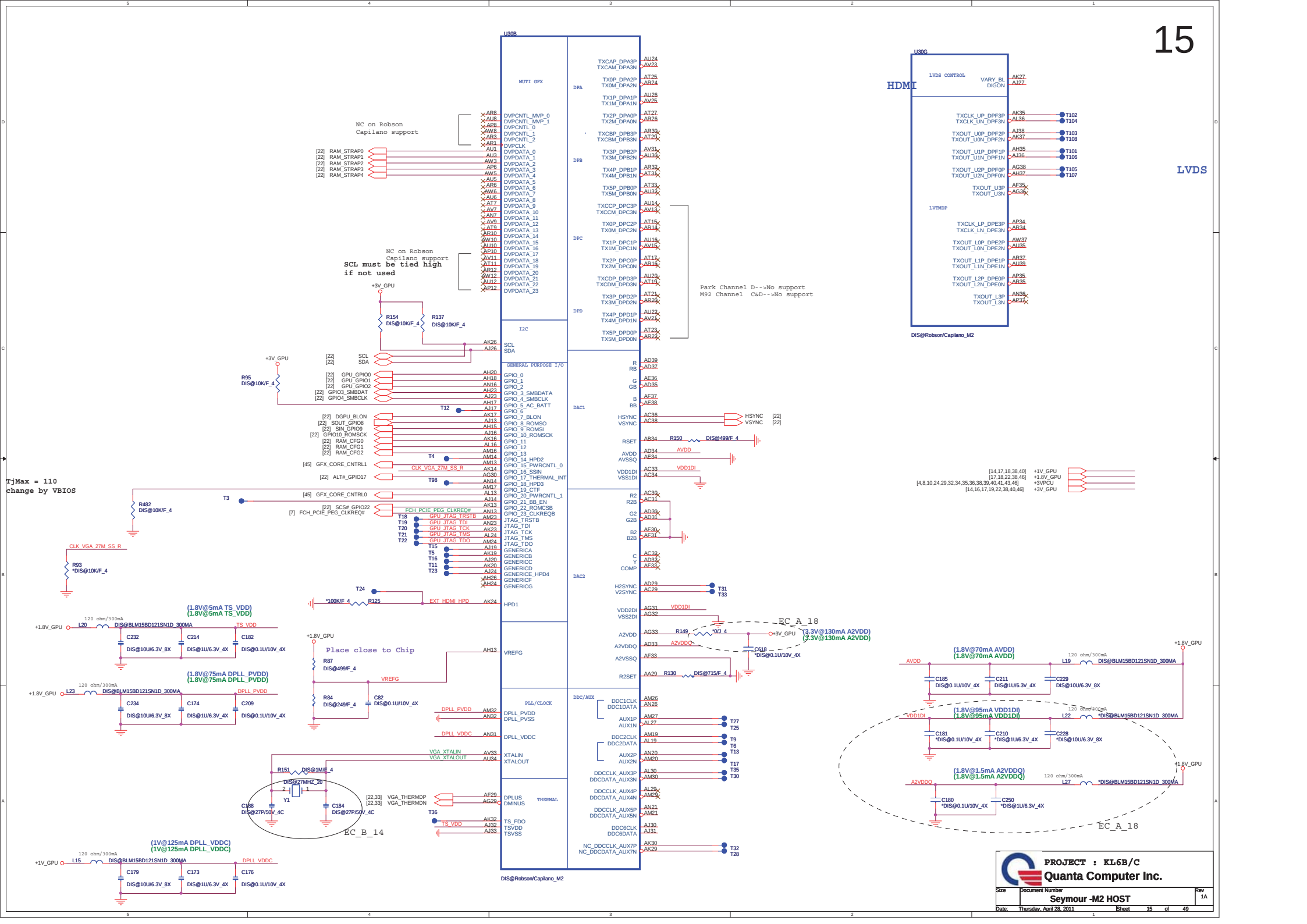




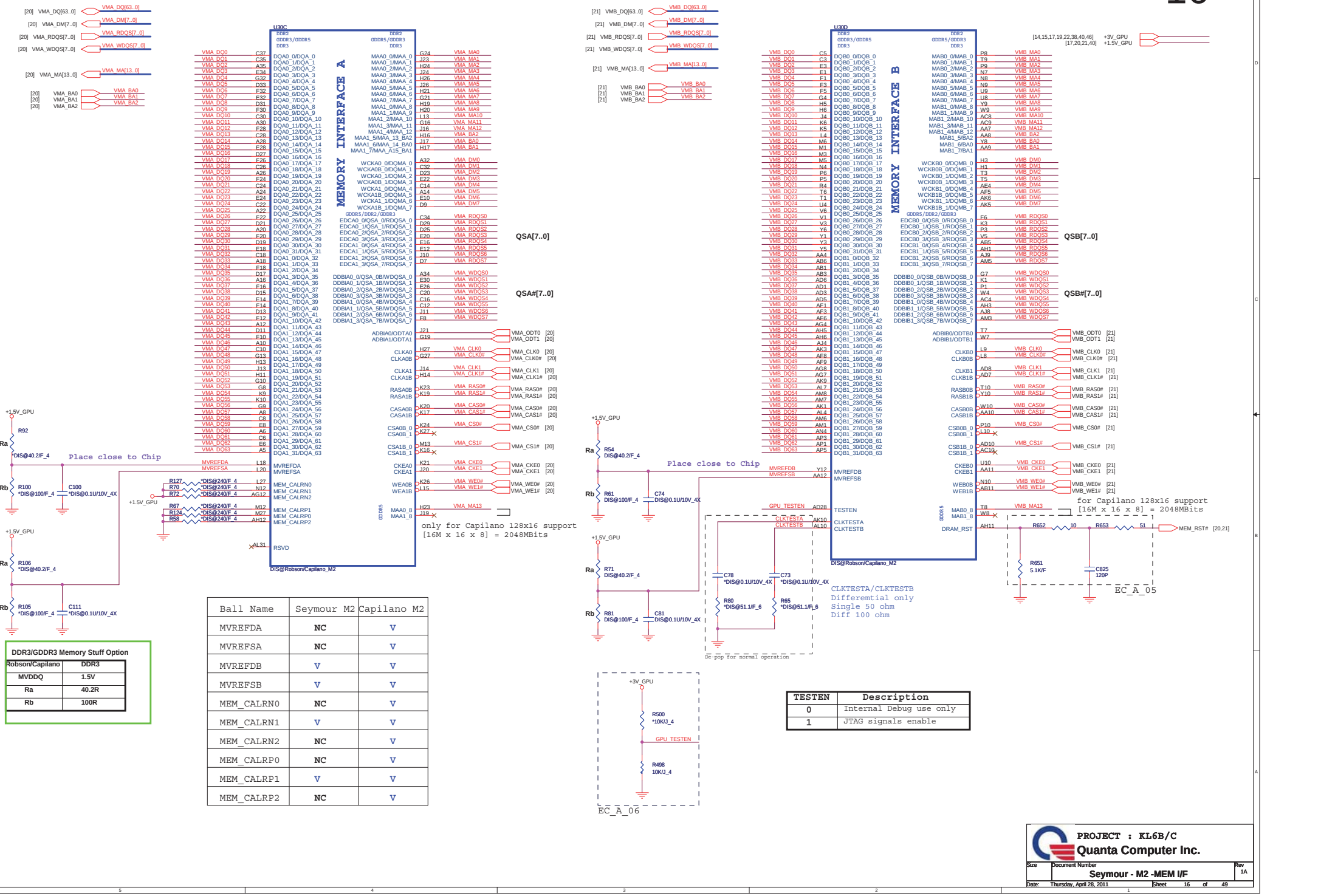
PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	Seymour_M2 PCIE	1A
Date: Thursday, April 28, 2011	Sheet 14 of 49	


U30B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
PLL/CLOCK
DDC/AUX
THERMAL
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
NC on Robson
Capilano support
SCL must be tied high
if not used
Park Channel D-->No support
M92 Channel C&D-->No support
DIS@Robson/Capilano_M2
U30G
HDMI
LVDS
LVDS CONTROL
LVTMDP
DIS@Robson/Capilano_M2
TjMax = 110
change by VBIOS
Place close to Chip
EC_A_18
EC_B_14
PROJECT : KL6B/C
Quanta Computer Inc.
Seymour -M2 HOST
Size
Document Number
Rev
1A
Date: Thursday, April 28, 2011
Sheet 15 of 49

Seymour M2 use Memory Group B only



Ball Name	Seymour M2	Capilano M2
MVREFDA	NC	V
MVREFSA	NC	V
MVREFDB	V	V
MVREFSB	V	V
MEM_CALRN0	NC	V
MEM_CALRN1	V	V
MEM_CALRN2	NC	V
MEM_CALRP0	NC	V
MEM_CALRP1	V	V
MEM_CALRP2	NC	V

DDR3/GDDR3 Memory Stuff Option

Robson/Capilano	DDR3
MVDDQ	1.5V
Ra	40.2R
Rb	100R

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	Seymour - M2 -MEM I/F	1A

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Robson PRO
Capilano LP

U30E

MEM I/O

POWER

PCIE

CORE

I/O

LEVEL TRANSLATION

PLL

VOLTAGE SENSE

ISOLATED CORE I/O

GND

(1.5V@2.8A PEAK VDDR1 with MEMORY)
(1.5V@3.4A PEAK VDDR1 W/O MEMORY)

(1.8V@400mA PCIE_VDDR)
(1.8V@400mA PCIE_VDDR)

(1V@2A PCIE_VDDC)
(1V@1.1A PCIE_VDDC)

120ohm, 2A

(30A or more)

(VDDCI + VDDC)@0.95V/8.5A PEAK
(VDDCI + VDDC)@1V/27.6A PEAK

(1.8V@17mA VDD_CT)
(1.8V@17mA VDD_CT)

(3.3V@60mA VDDR3)
(3.3V@60mA VDDR3)

(1.8V@170mA VDDR4)
(1.8V@170mA VDDR4)

(1.8V@40mA PCIE_PVDD)
(1.8V@75mA PCIE_PVDD)

(1.8V@75mA MPV18)
(1.8V@150mA MPV18)

(1.8V@50mA SPV18)
(1.8V@50mA SPV18)

(1V@100mA SPV10)
(1V@100mA SPV10)

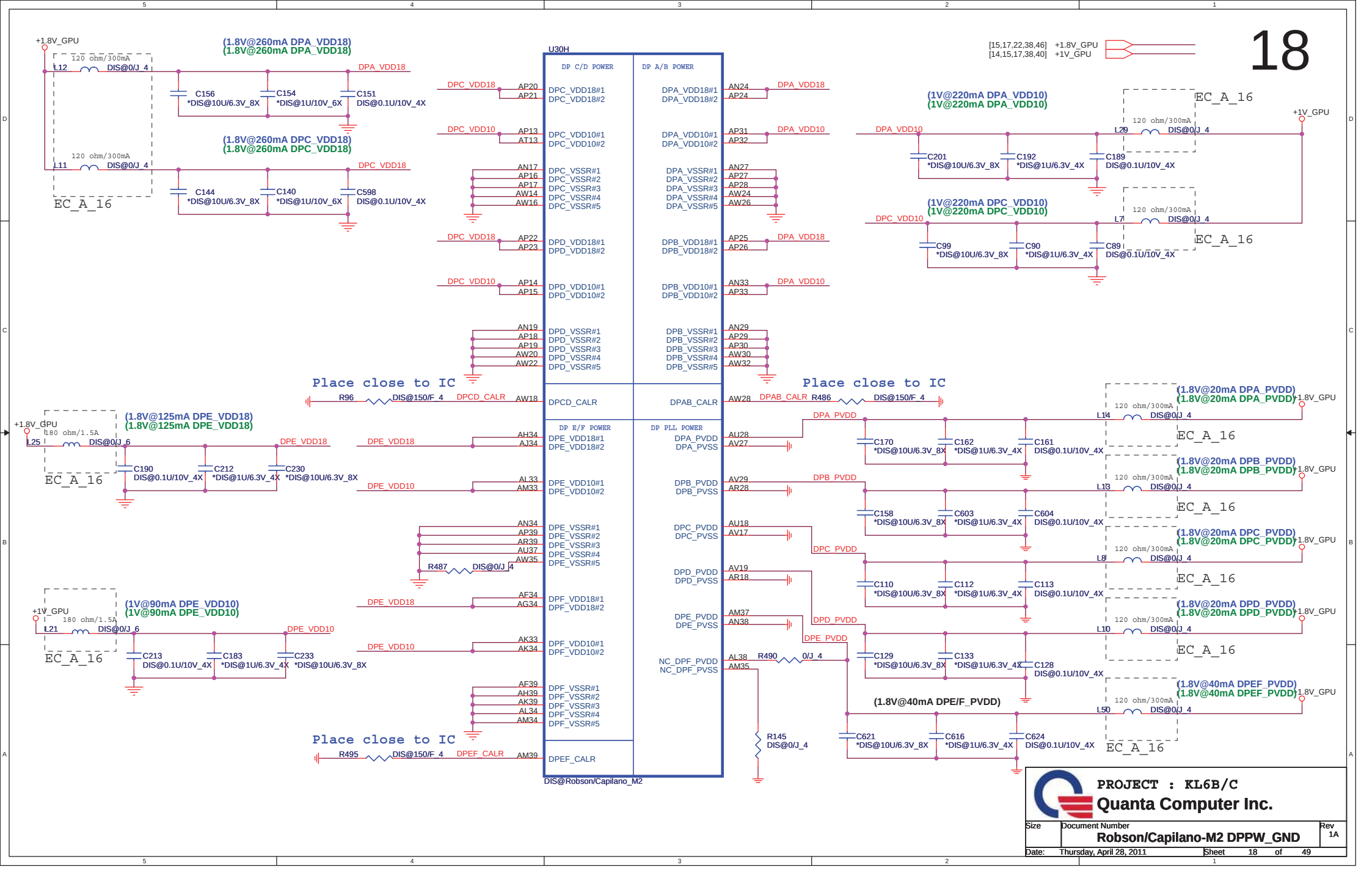
VGPU_VCC_SENSE and VGPU_VSS_SENSE need route as differetial pair

Robson had BACO support and Capilano didn't .
If not used, can be disconnected. (AL21 pin)

PX_EN = LOW, turn on
PX_EN = HIGH, turn off

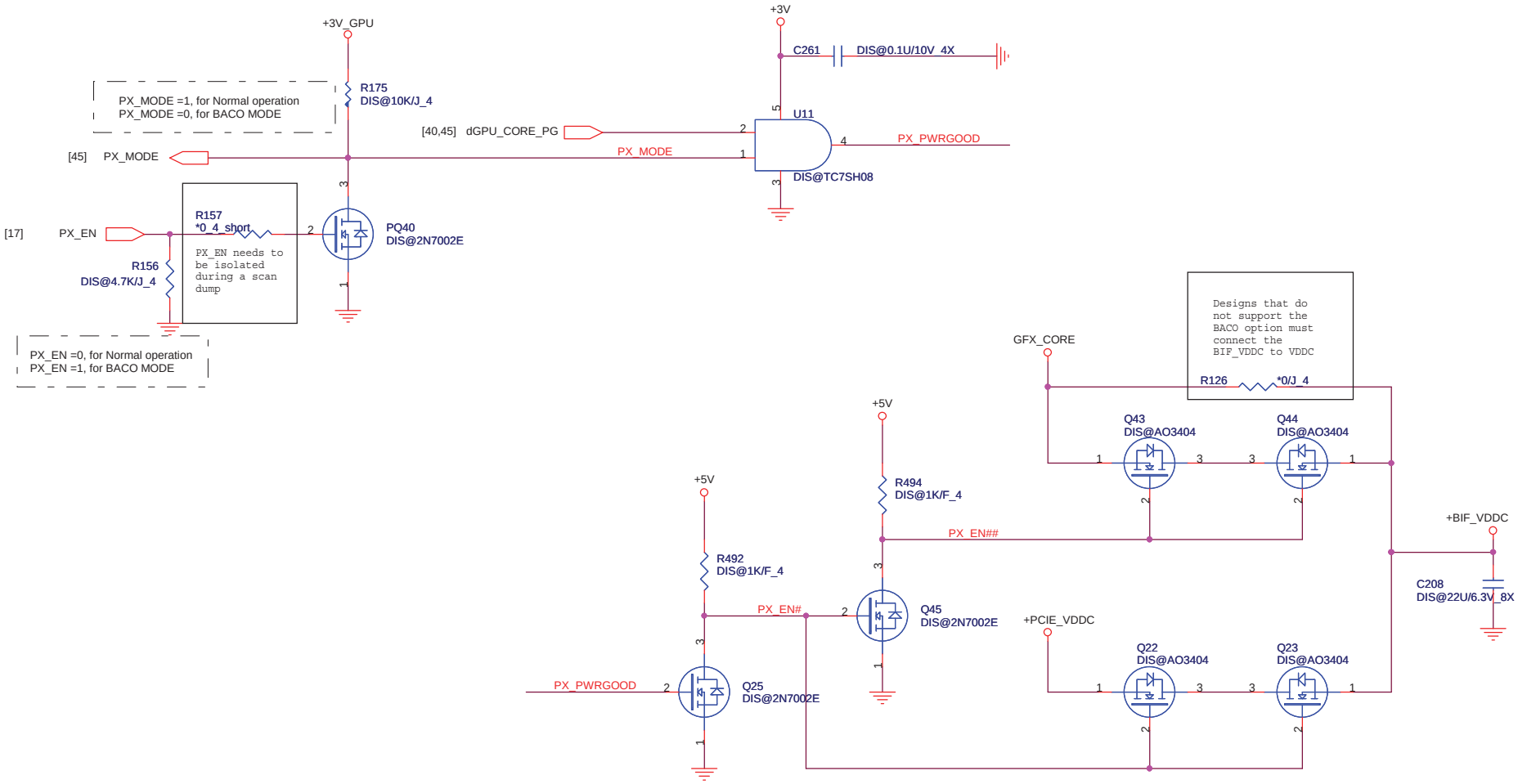
DIS@Robson/Capilano_M2

PROJECT :	KL6B/C
Quanta Computer Inc.	
Size	Document Number: Seymour -M2 PWR_GND
Rev	1A
Date: Thursday, April 28, 2011	Sheet 17 of 49



PROJECT : KL6B/C			
Quanta Computer Inc.			
Size	Document Number		Rev
	Robson/Capilano-M2 DPPW_GND		1A
Date: Thursday, April 28, 2011		Sheet 18 of 49	

[4,6,7,8,9,10,11,12,13,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V
[9,23,25,26,29,30,33,34,35,36,37,38,39,44] +5V
[17] +PCIE_VDDC
[14,15,16,17,22,38,40,46] +3V_GPU
[17,37,45] GFX_CORE



PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	Seymour -M2 BACO	1A
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CHANNEL A: 512MB DDR3 (64M*16*4pcs)

[16] VMA_DQ[63..0] — VMA_DQ[63..0]
[16] VMA_DM[7..0] — VMA_DM[7..0]
[16] VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
[16] VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]
[16] VMA_MA[13..0] — VMA_MA[13..0]

[16,17,21,40] +1.5V_GPU

U7 — TOP Left
U31 — BOT Left
U4 — BOT Right
U29 — TOP Right

100-BALL SDRAM DDR3
*DIS@VRAM_DDR3

Group-A0 VREF

+1.5V_GPU
R128 *DIS@4.99K/F_4 — VREFC_VMA1 — R131 *DIS@4.99K/F_4 — C175 *DIS@0.1U/10V_4X
R114 *DIS@4.99K/F_4 — VREFD_VMA1 — R121 *DIS@4.99K/F_4 — C137 *DIS@0.1U/10V_4X
R481 *DIS@4.99K/F_4 — VREFC_VMA2 — R483 *DIS@4.99K/F_4 — C595 *DIS@0.1U/10V_4X
R489 *DIS@4.99K/F_4 — VREFD_VMA2 — R488 *DIS@4.99K/F_4 — C609 *DIS@0.1U/10V_4X

Group-A1 VREF

+1.5V_GPU
R104 *DIS@4.99K/F_4 — VREFC_VMA3 — R103 *DIS@4.99K/F_4 — C108 *DIS@0.1U/10V_4X
R68 *DIS@4.99K/F_4 — VREFD_VMA3 — R69 *DIS@4.99K/F_4 — C71 *DIS@0.1U/10V_4X
R480 *DIS@4.99K/F_4 — VREFC_VMA4 — R477 *DIS@4.99K/F_4 — C592 *DIS@0.1U/10V_4X
R478 *DIS@4.99K/F_4 — VREFD_VMA4 — R479 *DIS@4.99K/F_4 — C593 *DIS@0.1U/10V_4X

MEM_A0 CLK

VMA_CLK0 — VMA_CLK0#
R136 *DIS@56.2/F_4 — R144 *DIS@56.2/F_4 — C191 *DIS@0.01U/25V_4X

Put close to VRAM

Group-A0 decoupling CAP

+1.5V_GPU
C163 C202 C198 C612 C143 C611 C602 C605 *DIS@1U/6.3V_4X
C132 C607 C608 C215 C236 C206 C615 C610 *DIS@1U/6.3V_4X

Group-A1 decoupling CAP

+1.5V_GPU
C620 C600 C219 C599 C134 C597 C586 C588 *DIS@1U/6.3V_4X
C591 C596 C594 C606 C585 C587 C584 C590 *DIS@1U/6.3V_4X
C41 C97 C106 C56 C239 *DIS@10U/6.3V_8X

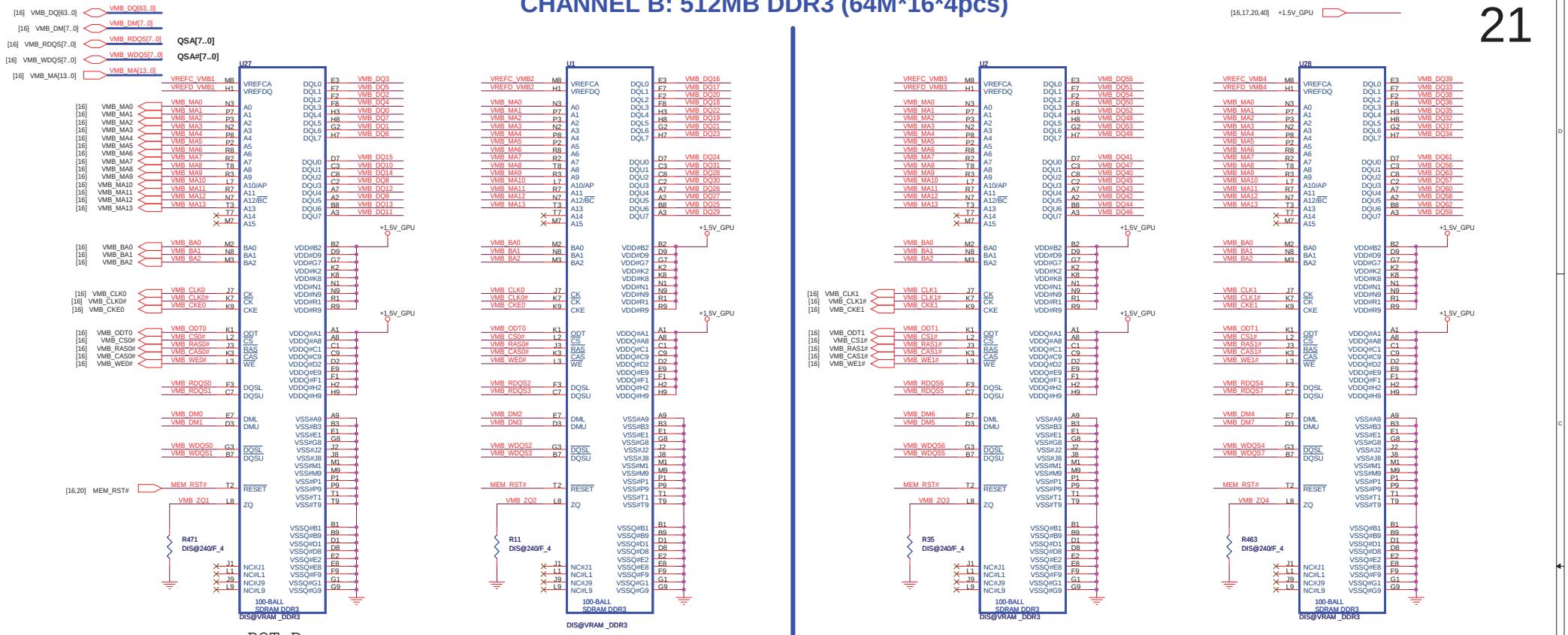
MEM_A1 CLK

VMA_CLK1 — VMA_CLK1#
R59 *DIS@56.2/F_4 — R53 *DIS@56.2/F_4 — C58 *DIS@0.01U/25V_4X

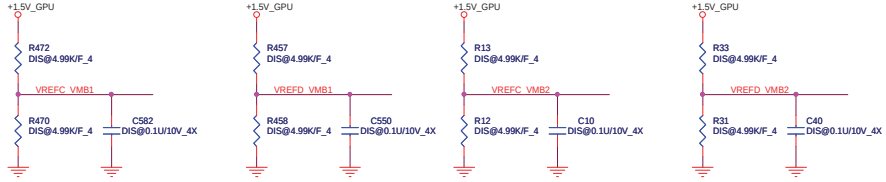
Put close to VRAM

PROJECT : KL6B/C
Quanta Computer Inc.
Size | Document Number: VRAM_A: DDR3-64M*16*4PCS | Rev 1A
Date: Thursday, April 28, 2011 | Sheet 20 of 49

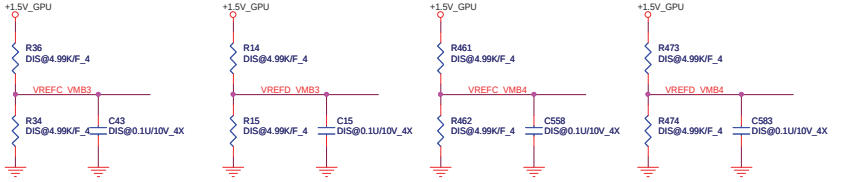
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



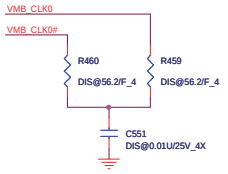
Group-B0 VREF



Group-B1 VREF

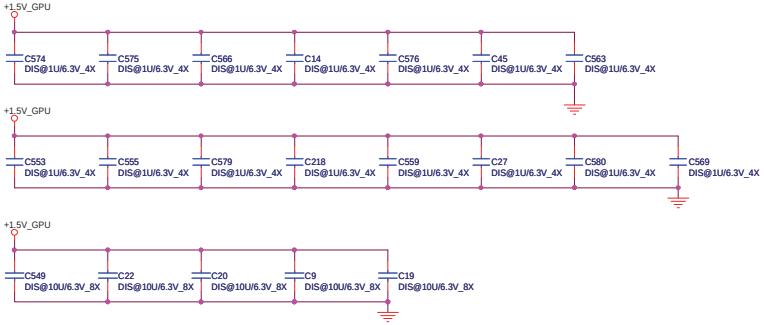


MEM_B0 CLK

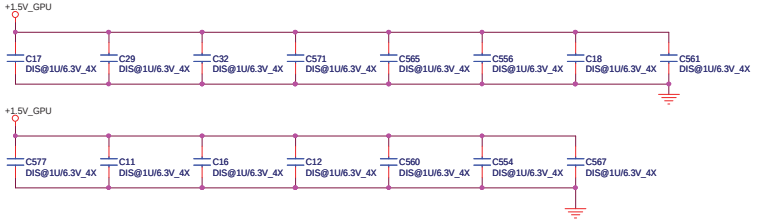


Put close to VRAM

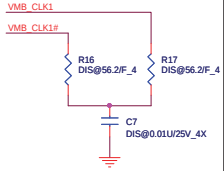
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



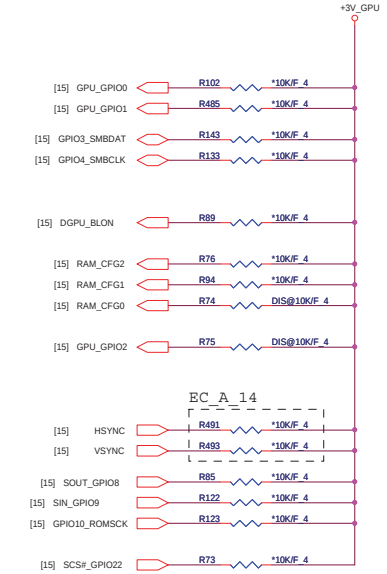
Put close to VRAM

PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	1A
Date: Thursday, April 28, 2011	Sheet 21 of 49	

PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
HSYNC	VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

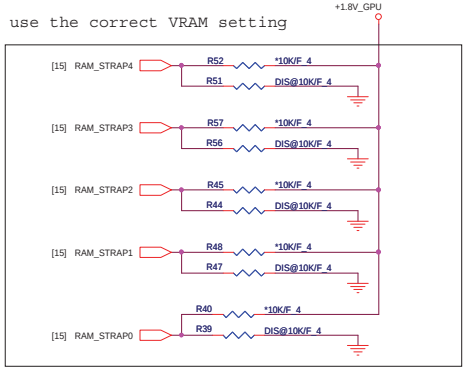
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	1	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

[15,17,18,38,46] +1.8V_GPU
[14,15,16,17,19,38,40,46] +3V_GPU

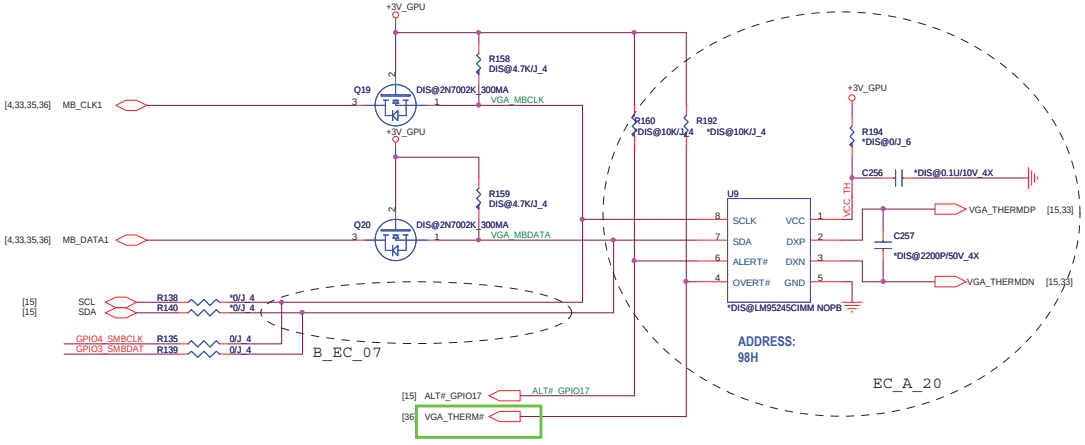
VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	0	1	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-1Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	0	1	1	0	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-1Gb)	1GB	0	0	0	1	0	1

Make sure to use the correct VRAM setting



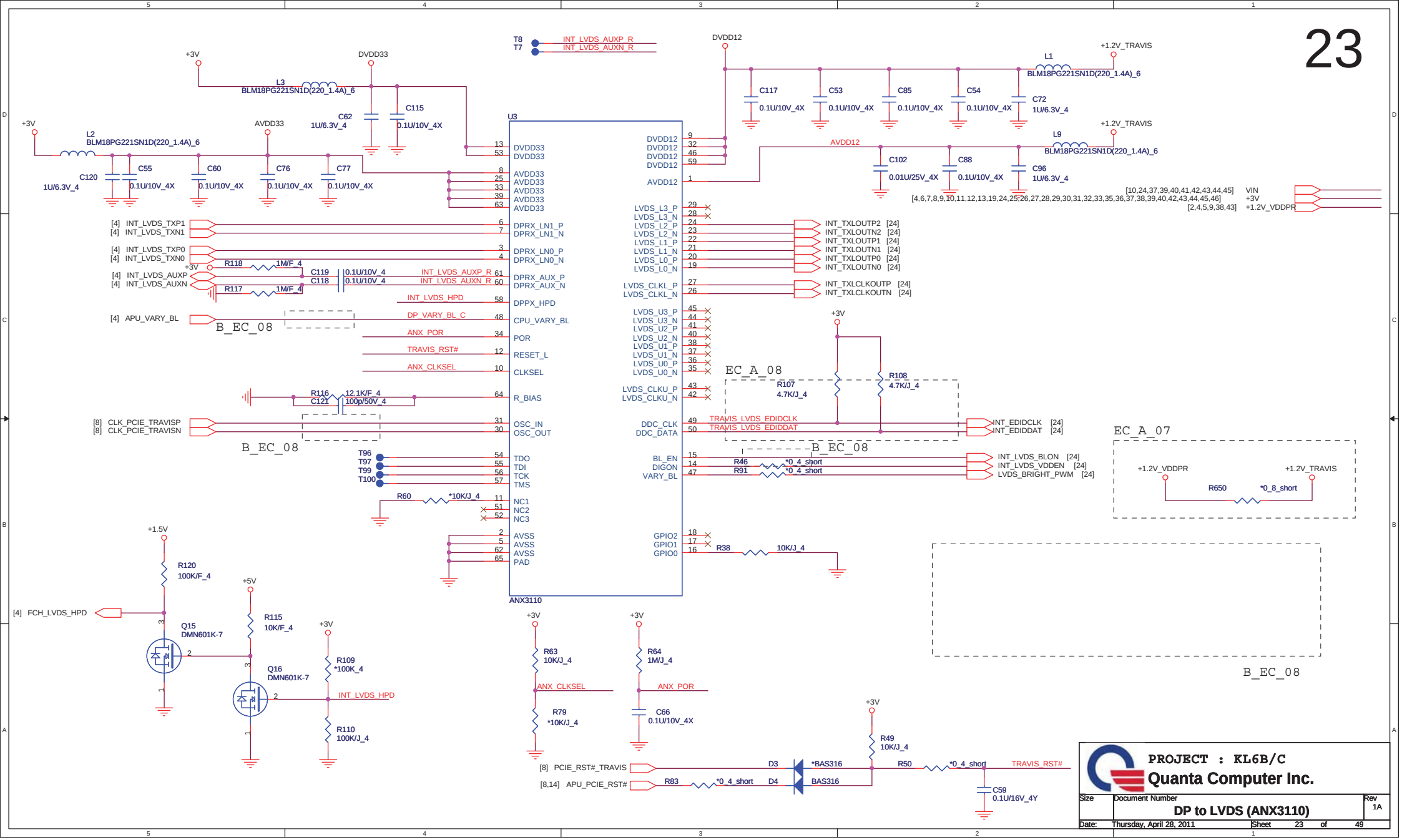
Thermal Sensor



PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	Memory strip/Thermal/HDCP	1A

Date: Thursday, April 28, 2011 Sheet 22 of 49



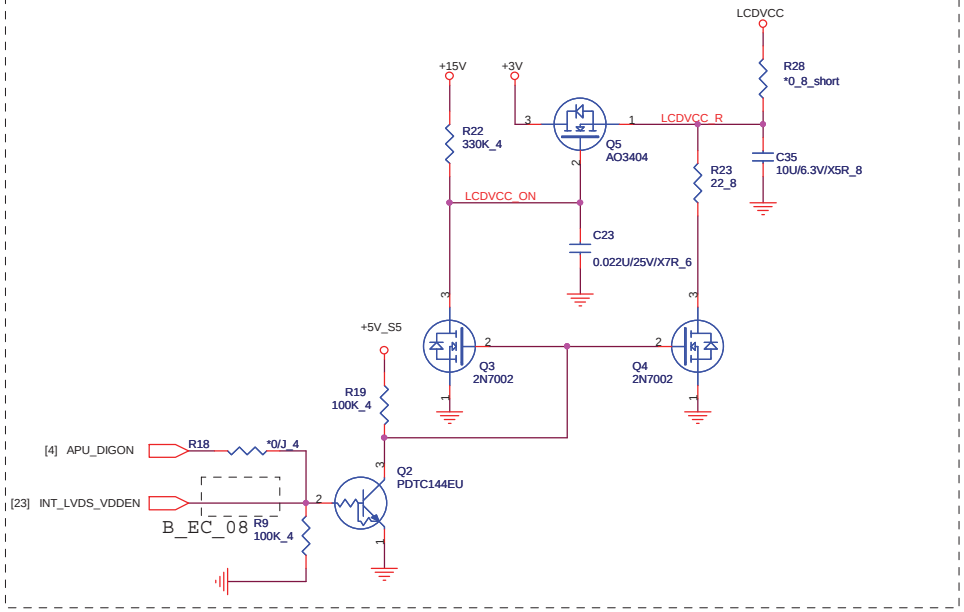
PROJECT : KL6B/C

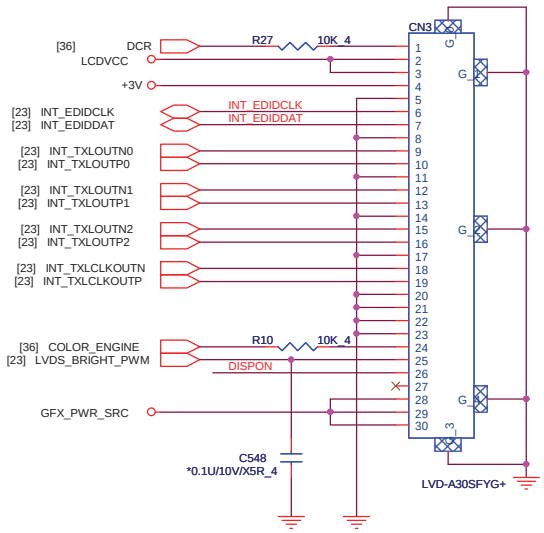
Quanta Computer Inc.

Size	Document Number	Rev
	DP to LVDS (ANX3110)	1A
Date: Thursday, April 28, 2011	Sheet 23 of 49	

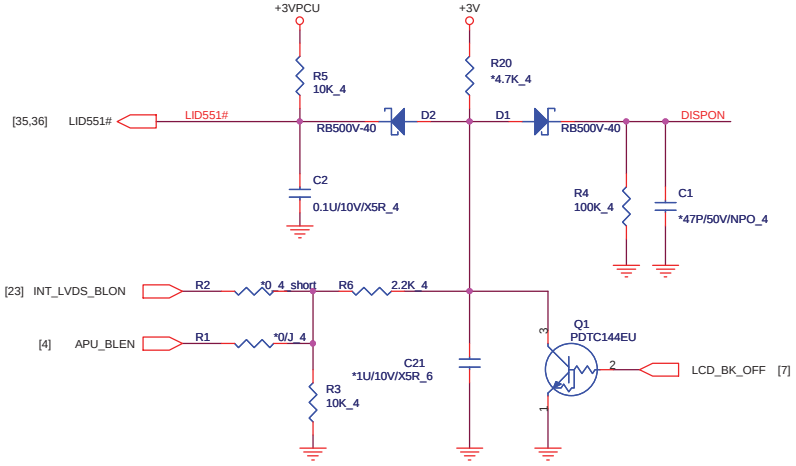
[4,6,7,8,9,10,11,12,13,19,23,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V
[29,31,35,38,40,41,42,46] +15V
[4,8,10,29,32,34,35,36,38,39,40,41,43,46] +3VPCU
[10,37,39,40,41,42,43,44,45] VIN

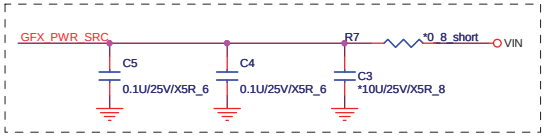
LCDVCC

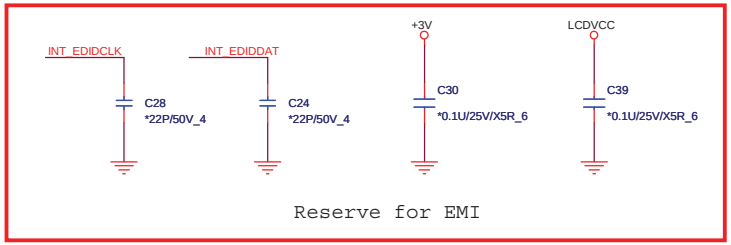




back light



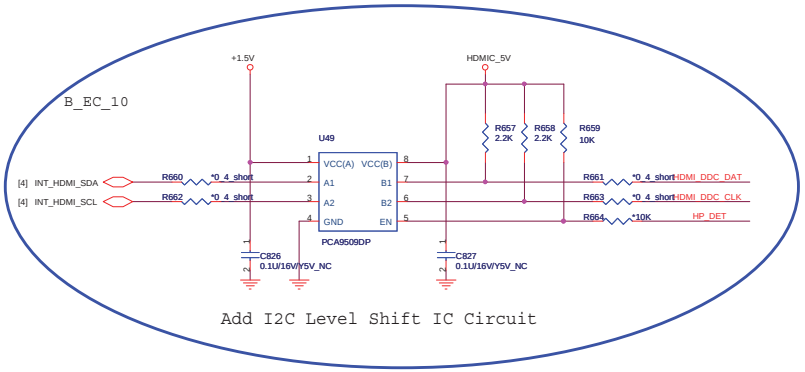




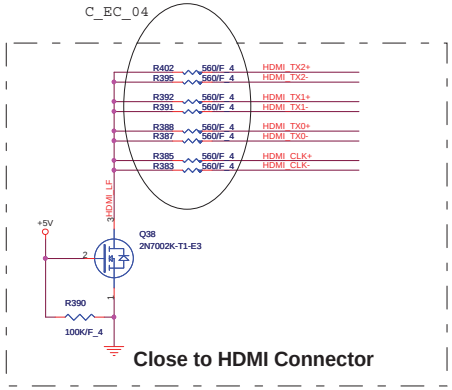
PROJECT : KL6B/C
Quanta Computer Inc.

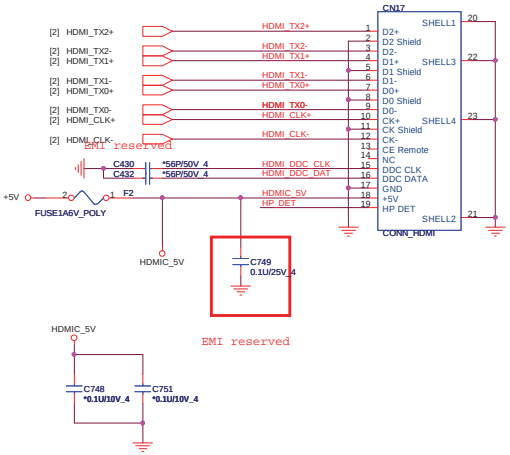
Size	Document Number	Rev
Custom	LCD CONN	1A

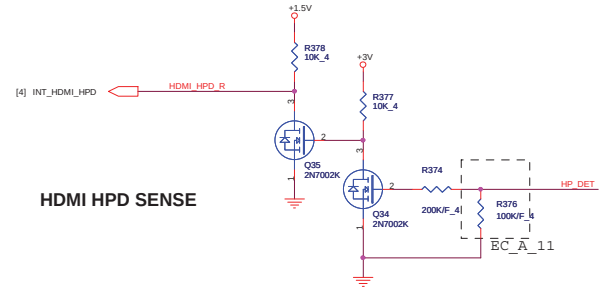
Date: Thursday, April 28, 2011 Sheet 24 of 49

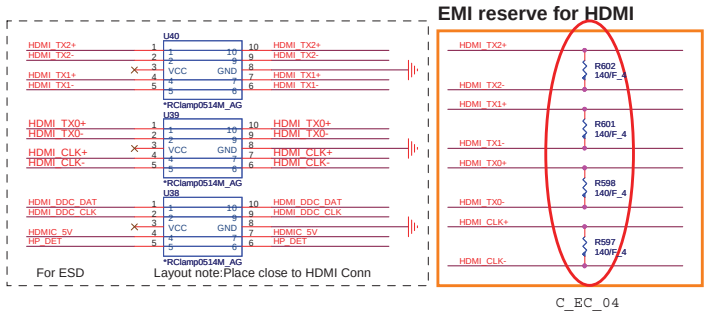


[9,19,23,26,29,30,33,34,35,36,37,38,39,44] +5V
[4,6,7,8,9,10,11,12,13,19,23,24,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V









PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

Date: Thursday, April 28, 2011 Sheet 25 of 49

Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

[9] INT_CRT_RED
[9] INT_CRT_GRE
[9] INT_CRT_BLU
L38 BLM18BA470SN1
L36 BLM18BA470SN1
L33 BLM18BA470SN1
CRT_R1
CRT_G1
CRT_B1
R262 150/F_4
R253 150/F_4
R246 150/F_4
C327 5.6P/50V/COG_4
C324 5.6P/50V/COG_4
C320 5.6P/50V/COG_4
C315 5.6P/50V/COG_4
C323 5.6P/50V/COG_4
C333 5.6P/50V/COG_4
TP7
CRT_VCC
D29 RB500V-40
C692 0.1U/10V/X5R_4
+5V
F1 FUSE1A6V_POLY
CRT_VCC_R
C303 0.1U/10V/X5R_4
CN13 CRT_CONN

+5V
[9] INT_CRT_VSYNC
[9] INT_CRT_HSYNC
U13 AHCT1G125DCH
U14 AHCT1G125DCH
VGAVSYNC_R
VGAHSYNC_R
C318 0.1U/10V/X5R_4
R219 10_4
R232 10_4
Place near
U37,U38 < 200 mil
CRTVSYNC1
CRTHSYNC1
C308 *10P/50V/COG_4
C282 *10P/50V/COG_4
L30 HB-1T1608-121JT
L32 HB-1T1608-121JT
CRTVSYNC
CRTHSYNC
C309 10P/50V/COG_4
C281 10P/50V/COG_4
Place near CN5002 connector
< 200 mil

ESD PROTECTION
D17 *TVSS5VESPT CRT_R1
D16 *TVSS5VESPT CRT_G1
D14 *TVSS5VESPT CRT_B1
D11 *TVSS5VESPT CRTVSYNC
D12 *TVSS5VESPT CRTHSYNC
D28 *TVSS5VESPT DDCCLK
D30 *TVSS5VESPT DDCDAT

+3V
R527 2.2K_4
R505 2.2K_4
CRT_VCC
R520 4.7K_4
R509 4.7K_4
[9] INT_DDCCLK
[9] INT_DDCDAT
Q46 2N7002K-T1-E3
Q47 2N7002K-T1-E3
DDCCLK
DDCDAT
C685 *10P/50V/COG_4
C665 *10P/50V/COG_4

PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CONN	1A
Date: Thursday, April 28, 2011	Sheet 26 of 49	

Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

Note:

SD/MMC	MS	XD
SP1 SD_D7		XD_RDY
SP2 SD_D6		XD_RE#
SP3 SD_D5		XD_CE#
SP4 SD_D4		XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15 SD_WP		XD_D7

For RTS5139

SD,MS 4bit only

change to 0ohm

[8] CLK_48M_CARD — R633 0/J_4 — XI — Y6 *12MHZ 30ppm — XO — R639 *270K_4 — C813 *5.6P/50V_4 — C816 *5.6P/50V_4

R635 *10K_4 +3V

C815 *1U/6.3V/X5R_4 CARD_RST#

C820 1U/6.3V/X5R_4

R647 6.19K/F_4 RREF

U48 **RTS5139-GR**

RREF DV18 NC RST# XTLO XTLI/CLK_IN CLK_MODE[0] GPIO MS_INS# SD_CD# SP15 SP14

[7] USBP7- — 1 DM

[7] USBP7+ — 2 DP

3 NC, 4 NC, 5 NC, 6 NC, 7 NC, 8 GND, 9 NC, 10 NC

11 3V3_IN — 3V3_IN

12 Card_3V3

+3V — R646 *0_8_short — 3V3_IN — C821 10U/6.3V/X5R_6 — C822 0.1U/10V/X5R_4 — VCC_XD — C818 0.1U/10V/X5R_4

SP13 36, SP12 35, SP11 34, SP10 33, SP9 32, SP8 31, SP7 30, SP6 29, SP5 28

CLK_MODE[1] 27 — R624 *10K_4 — DV33_18

GND 26

SD_D2 25 — SD_D2_R — R622 *0_4_short — SD_D2

XD_CD# 13, DV33_18 14, GND 15, SP1 16, SP2 17, SP3 18, SP4 19, SD_D1 20, SD_D0 21, SD_CLK 22, SD_CMD 23, SD_D3 24

XD_CD# — DV33_18 — SP1 — SP2 — SP3 — SP4 — SD_D1_R — SD_D0_R — SD_CLK_R — SD_CMD_R — SD_D3_R

R638 *0_4_short — R636 *0_4_short — R634 33/1_4 — R627 *0_4_short — R623 *0_4_short

SD_D1 — SD_D0 — SD_CLK — SD_CMD — SD_D3

C814 *4.7U/6.3V/X5R_6 — C795 0.1U/10V/X5R_4

+3V — R640 10K_4

XD_CD# — RB500V-40 — D37

SD_CD# — RB500V-40 — D39

MS_CD# — RB500V-40 — D38

[36] CARDREADER_DET# — C823 EGA-0402

[36] CARDREADER_RST# — RB500V-40 — D36 — CARD_RST#

B-05
D-03

7 IN1 CARD CONN XD,MMC/SD,MS/MSP

CN10

XD_RDY 1 (2)XD-R/B

XD_RE# 2 (3)XD-RE

XD_CE# 3 (4)XD-CE

XD_CLE 4 (5)XD-CLE

XD_ALE 5 (6)XD-ALE

XD_WE# 6 (7)XD-WE

XD_WP# 7 (8)XD-WP

XD_D0 8 (10)XD-D0

XD_D1 9 (11)XD-D1

SD_D2 10 (9)SD-DAT2

SD_D3 11 (1)SD-DAT3

SD_CMD 12 (2)SD-CMD

13 4IN1-GND1

14 (9)MS-VCC

MS_CLK 15 (8)MS-SCLK

MS_D3 16 (7)MS-DATA3

MS_CD# 17 (6)MS-INS

MS_D2 18 (5)MS-DATA2

MS_D0 19 (4)MS-DATA0

20 (3)MS-DATA1 — MS_D1

21 (2)MS-BS — MS_BS

22 4IN1-GND2

23 (4)SD-VCC

SD_CLK 24 (5)SD-CLK

SD_D0 25 (7)SD-DAT0

XD_D2 26 (12)XD-D2

XD_D3 27 (13)XD-D3

XD_D4 28 (14)XD-D4

SD_D1 29 (8)SD-DAT1

XD_D5 30 (15)XD-D5

XD_D6 31 (16)XD-D6

XD_D7 32 (17)XD-D7

33 (18)XD-VCC

XD_CD# 34 (19)XD-CD-SW

SD_WP 35 SD-WP-SW

SD_CD# 36 SD-CD-SW

SHIELD1-GND 37, SHIELD2-GND 38, SHIELD3-GND 41, SHIELD4-GND 42

R015-212-LM

C767 *33P/25V_4 — VCC_XD — C768 0.1U/10V/X5R_4 — C771 *10U/6.3V/X5R_6

VCC_XD — C769 0.1U/10V/X5R_4

VCC_XD — C770 0.1U/10V/X5R_4

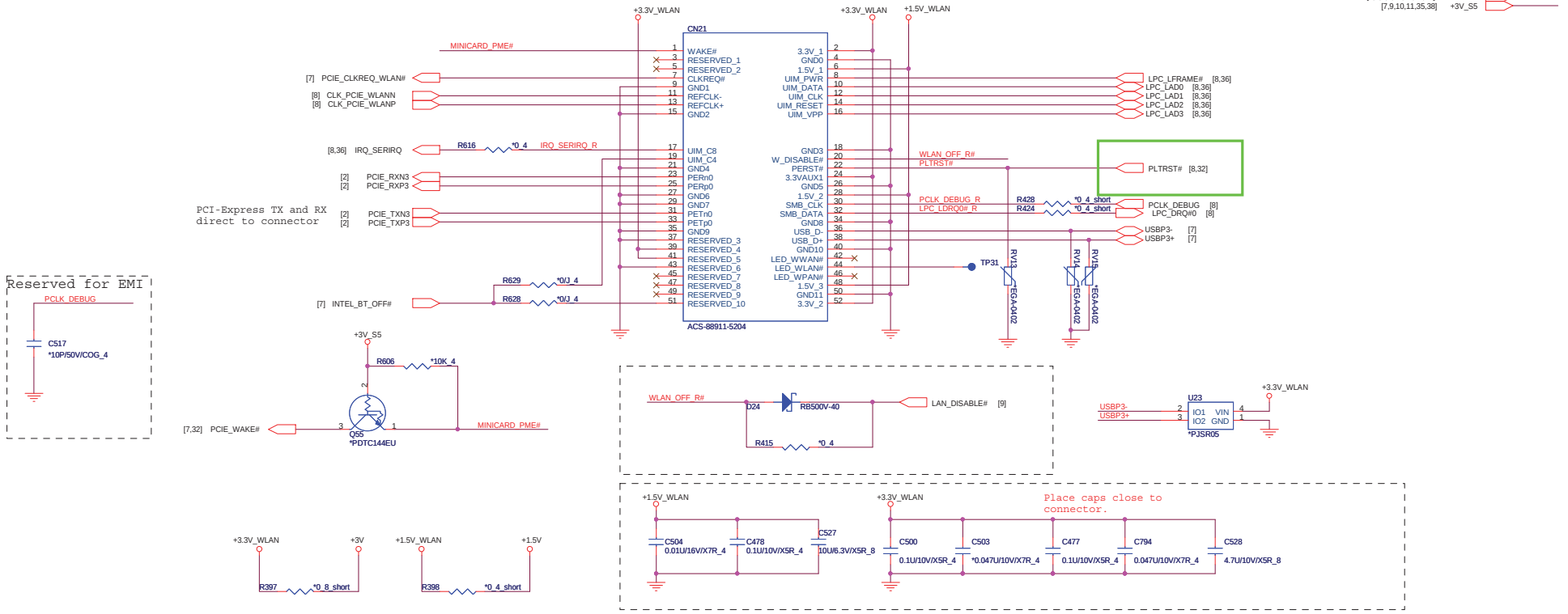
PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A

Date: Thursday, April 28, 2011 Sheet 27 of 49

MiniCard WLAN connector



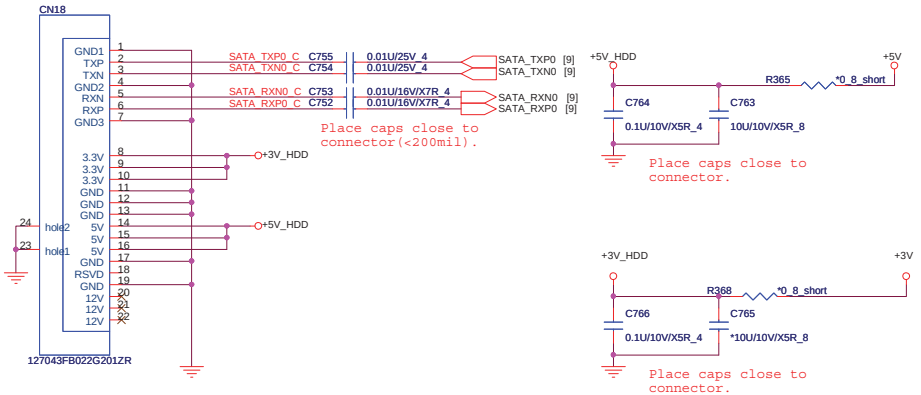
PROJECT : KL6B/C

Quanta Computer Inc.

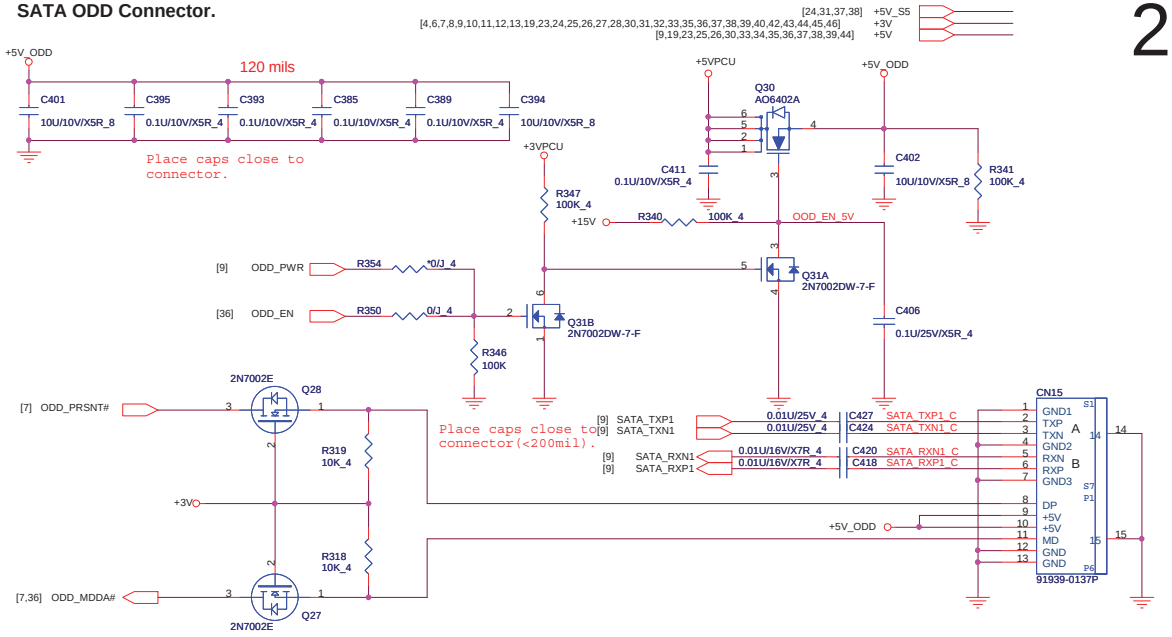
Size	Document Number	Rev
Custom	MINI-Card WLAN	1A

Date: Thursday, April 28, 2011 Sheet 28 of 49

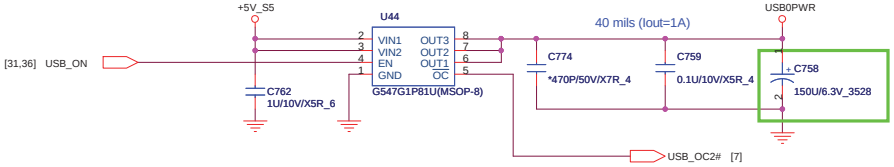
SATA HDD Connector.

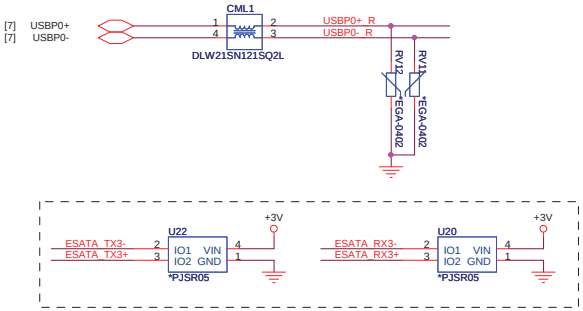


SATA ODD Connector.

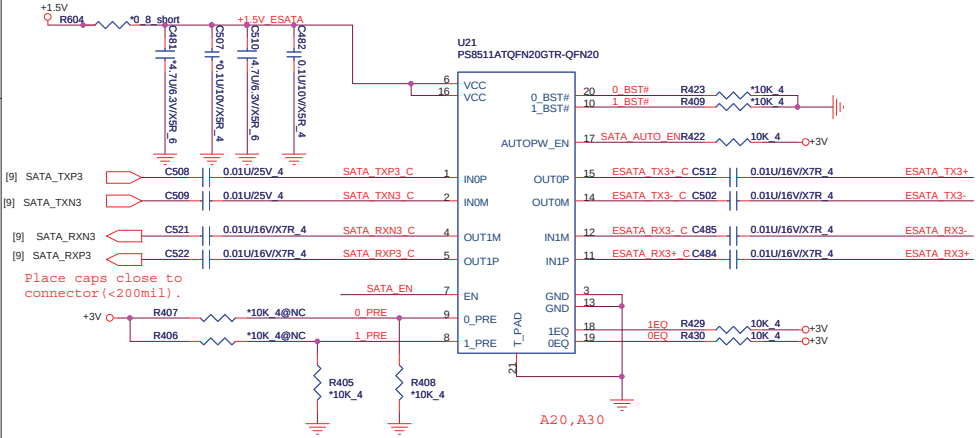


USB + E-SATA





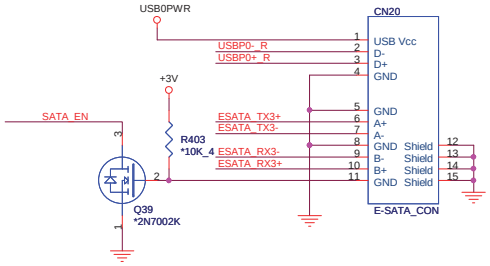
E-SATA RE-DRIVER



All straps of PS8511A have int. PL 150Kohm.

EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

USB 0



PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

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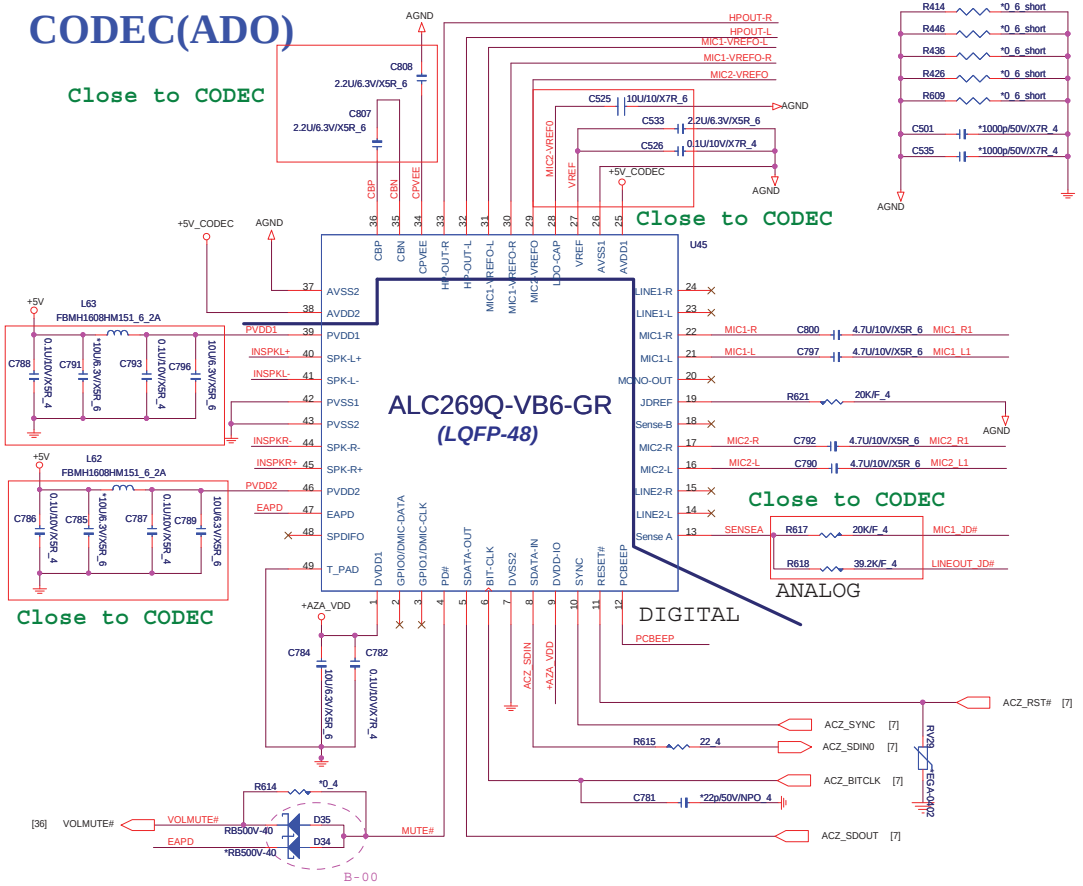
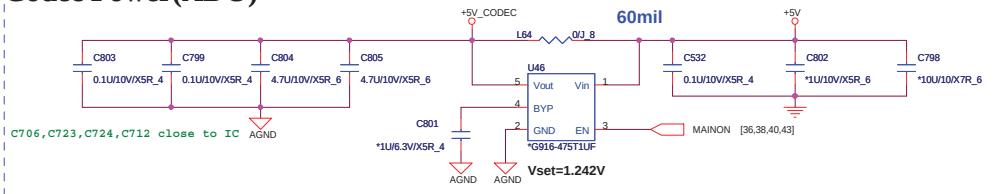
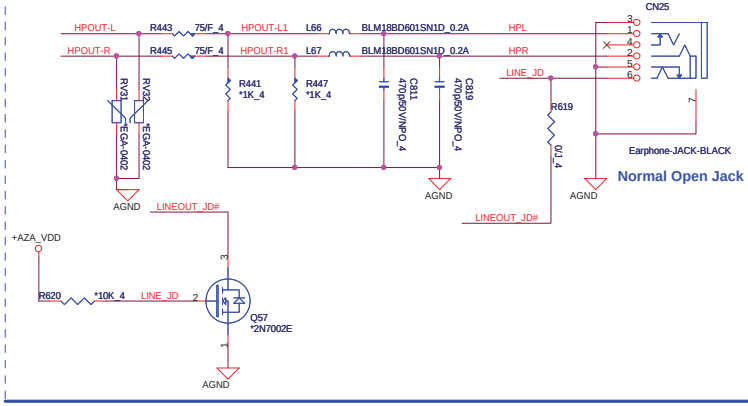
CODEC(ADO)



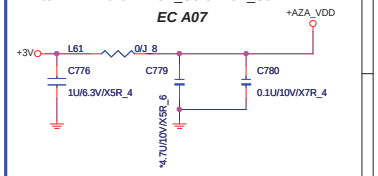
Codec Power(ADO)



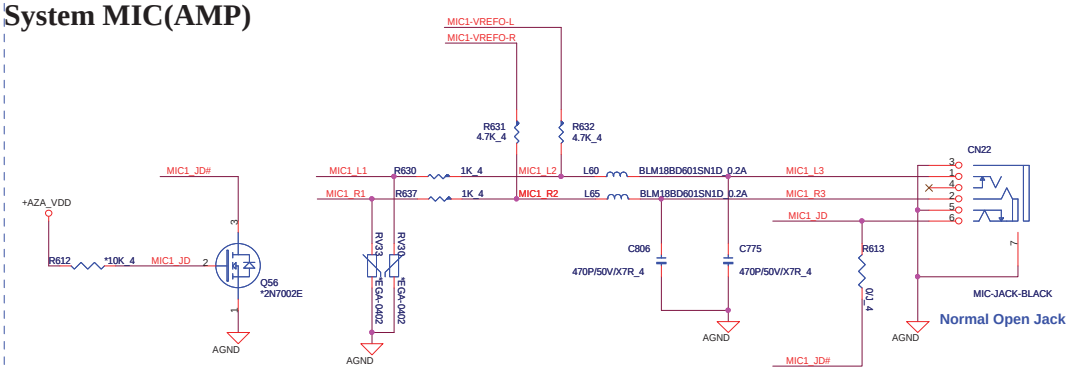
Earphone(AMP)



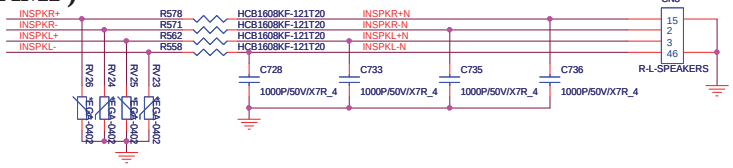
HDA Power(ADO)



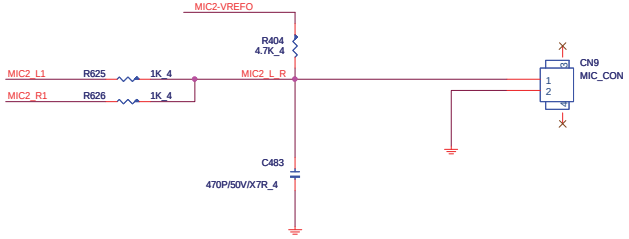
System MIC(AMP)



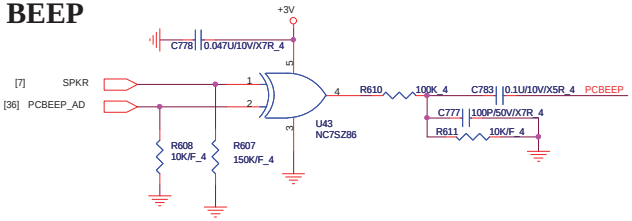
Speaker(AMP)



INTERNAL MIC



PC BEEP



PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A

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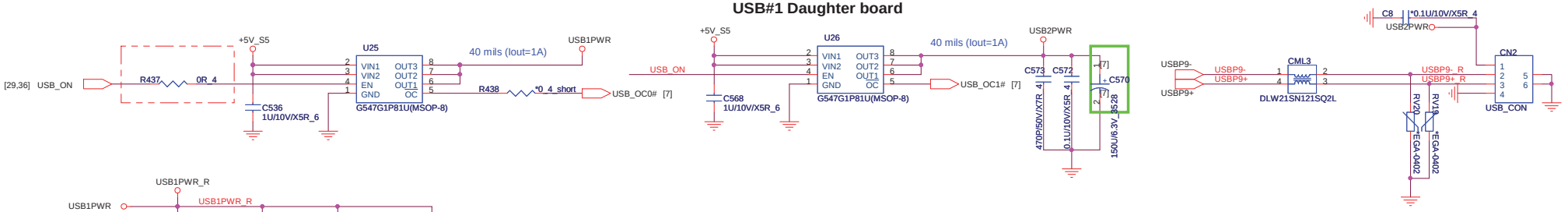
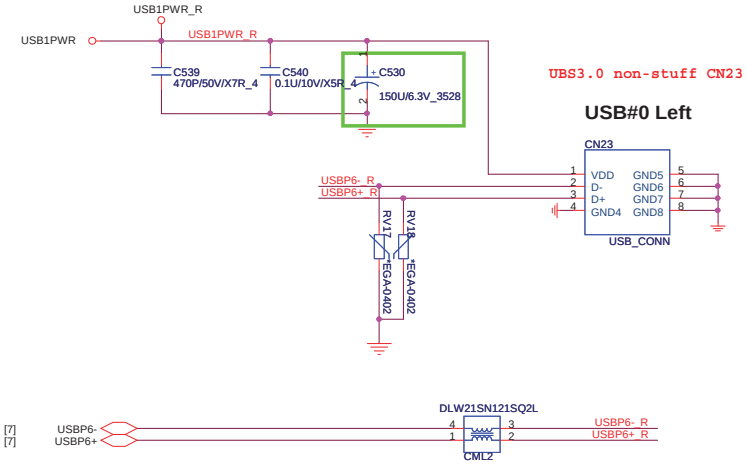
[24,29,37,38] +5V_S5
[4,6,7,8,9,10,11,12,13,19,23,24,25,26,27,28,29,30,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V
[24,29,35,38,40,41,42,46] +15V

USB2.0*3

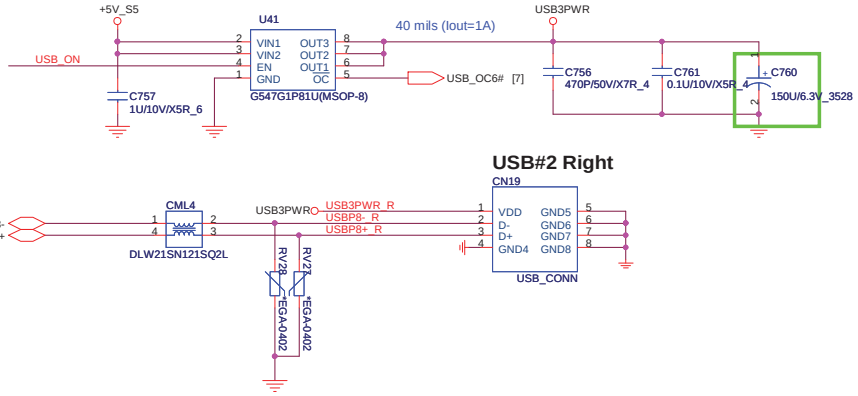
USB#1 Daughter board



USB#0 Left



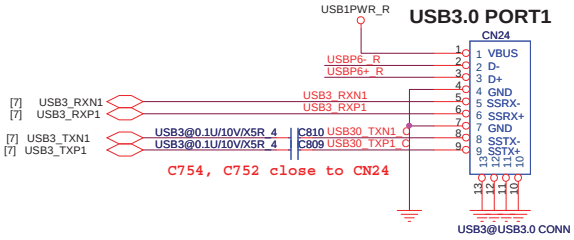
USB#3 Right



USB#2 Right

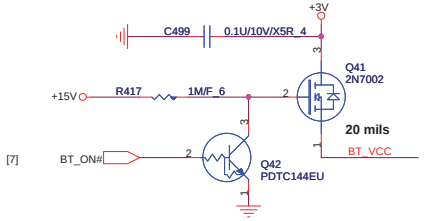
REAR USB PORT X1

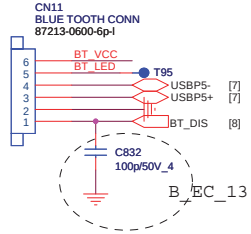
USB3.0 PORT1



SUY USB3.0: DFHS09FR063

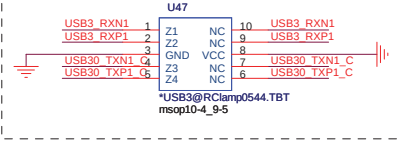
BLUETOOTH





B_EC_13

ESD



PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
	BT/USB2.0X3/USB3.0X1	1A

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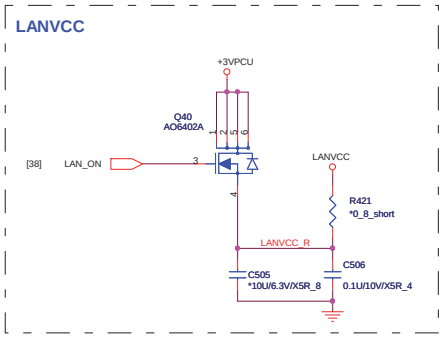
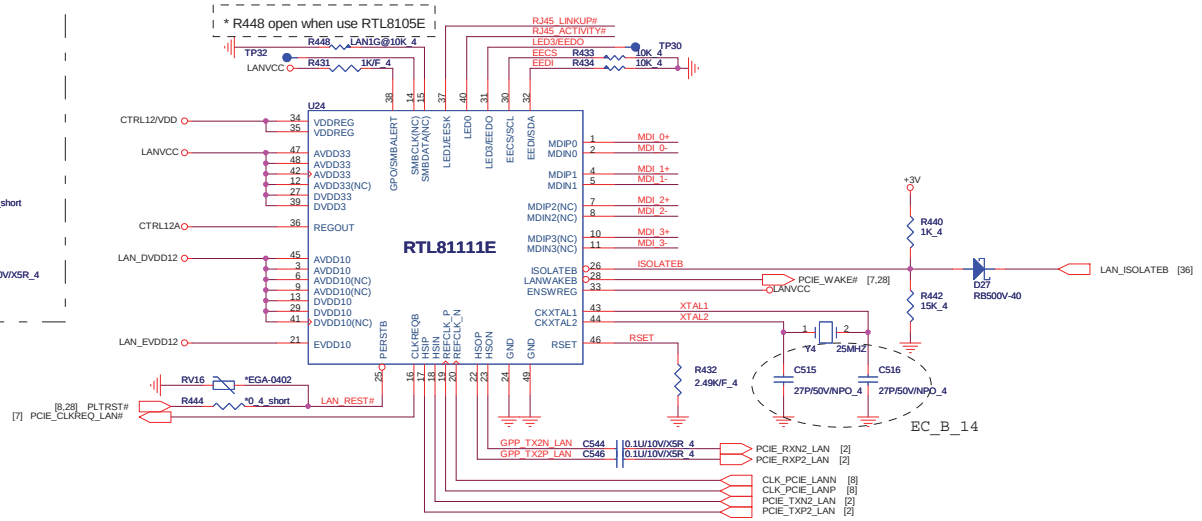
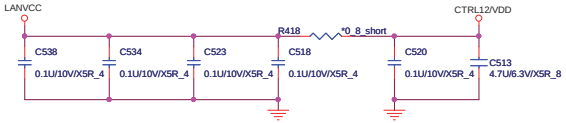
LANVCC



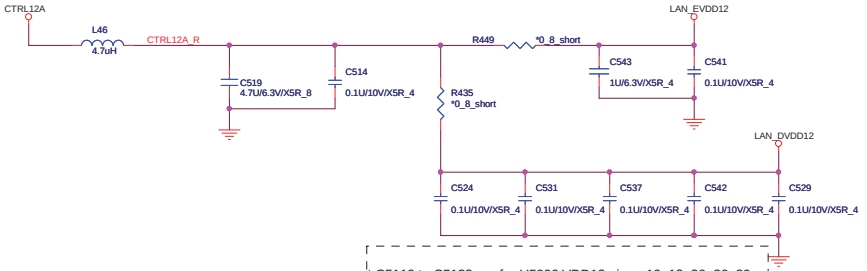




* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

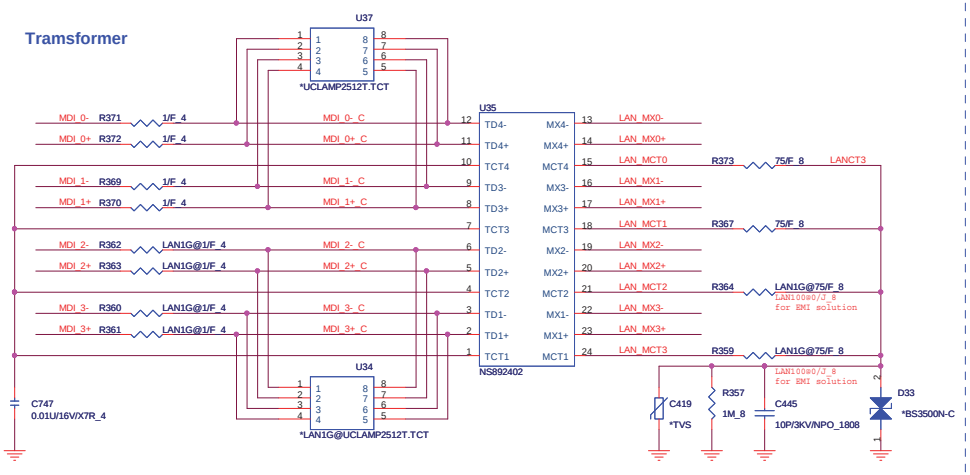
* C476 and C472 are for U24 LAN_EVDD12 pin 21.



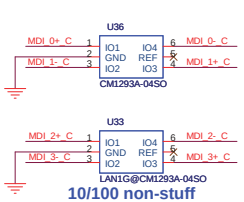
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Layout:All termination signal should have 20 mil trace

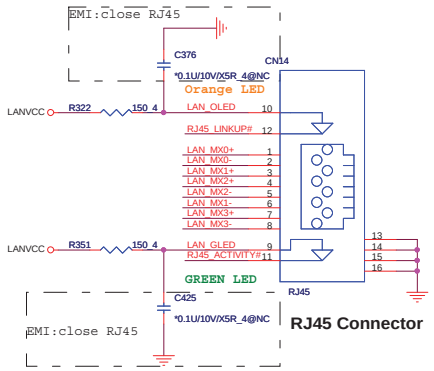
Tramsformer



RJ45 Connector



10/100 non-stuff



RJ45 Connector

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Quanta Computer Inc.

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Custom	RTL8111EL-VB	1A
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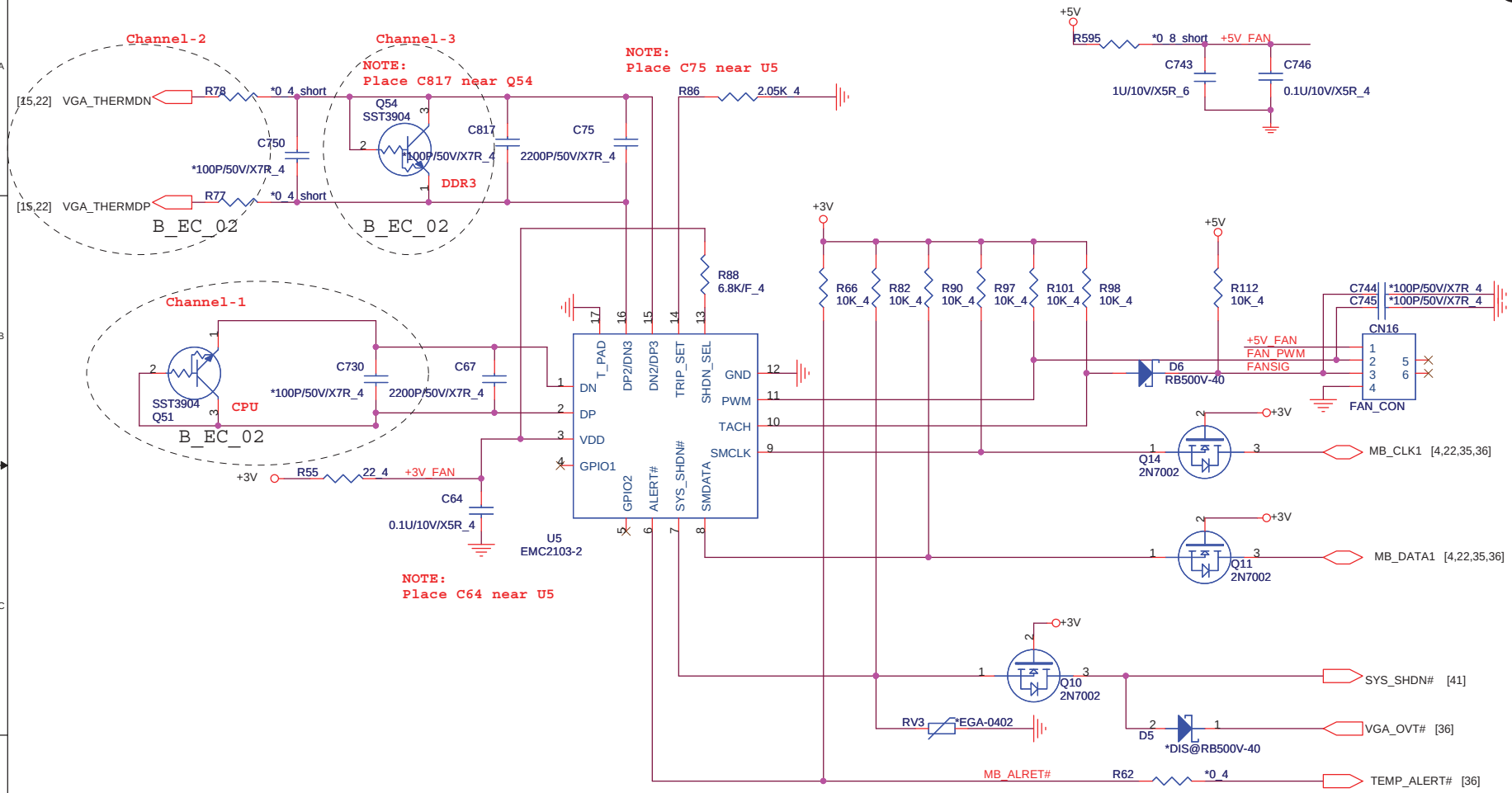
FAN CONTROL

[4,6,7,8,9,10,11,12,13,19,23,24,25,26,27,28,29,30,31,32,35,36,37,38,39,40,42,43,44,45,46] +3V
[9,19,23,25,26,29,30,34,35,36,37,38,39,44] +5V

33



PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A
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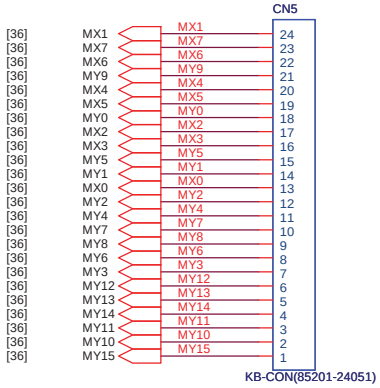
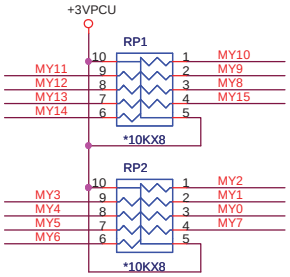
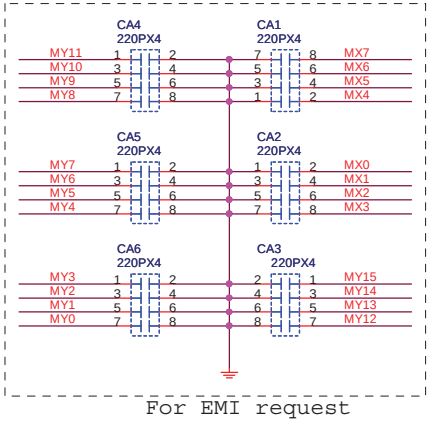
KEYBOARD

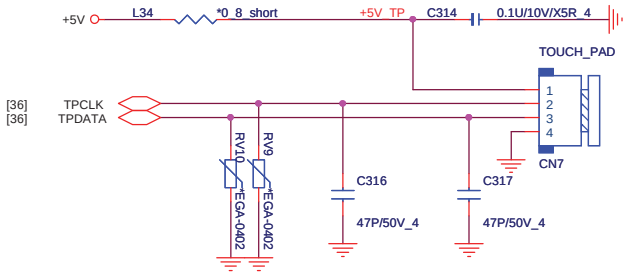
[9,19,23,25,26,29,30,33,35,36,37,38,39,44] +5V
[4,8,10,24,29,32,35,36,38,39,40,41,43,46] +3VPCU







Touch pad



PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B, T/P	1A
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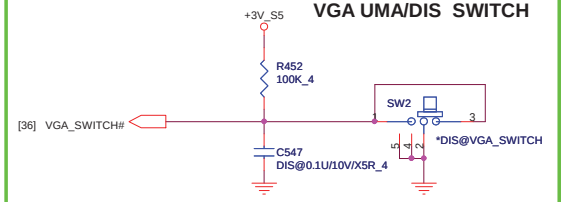
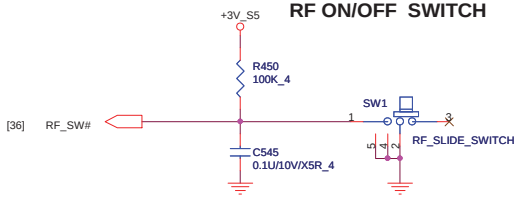
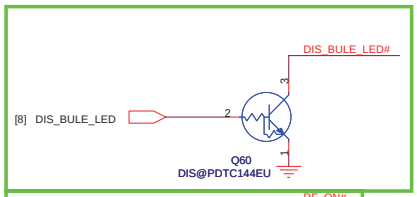
[7,9,10,11,28,38] +3V_S5
[4,6,7,8,9,10,11,12,13,19,23,24,25,26,27,28,29,30,31,32,33,36,37,38,39,40,42,43,44,45,46] +3V

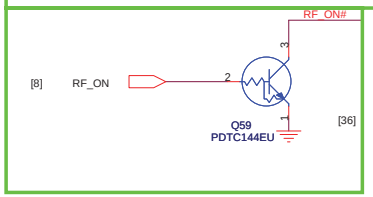
VGA UMA/DIS SWITCH

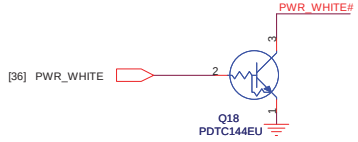


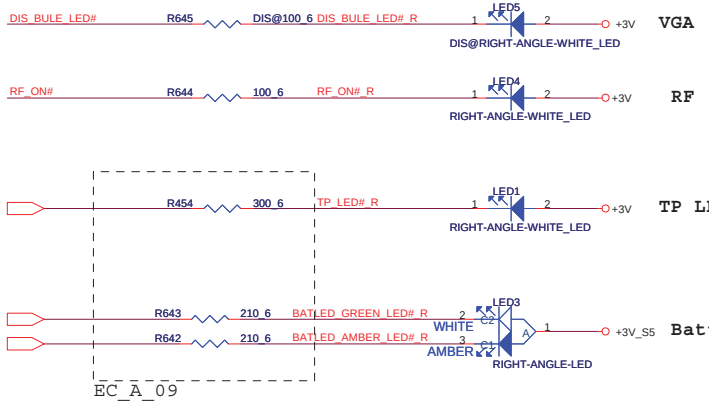
RF ON/OFF SWITCH

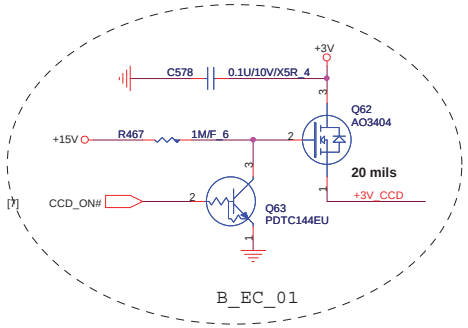




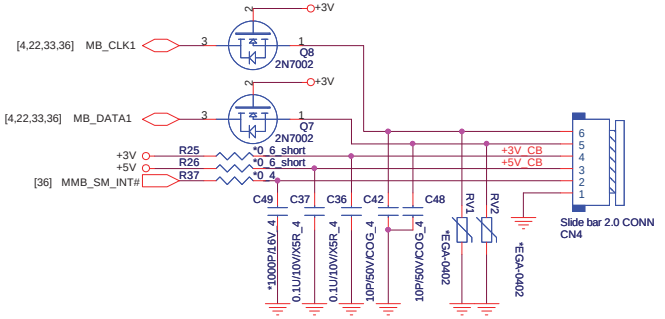




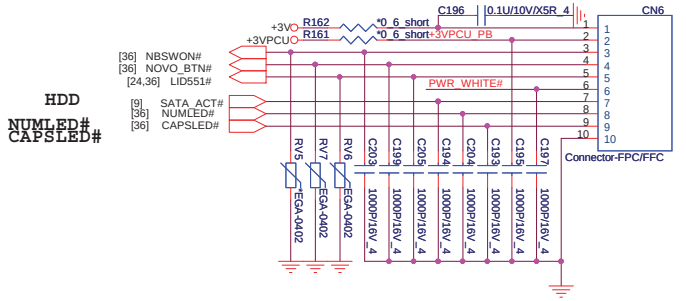




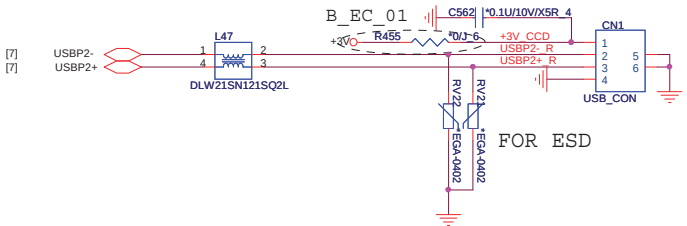
CAPACITANNCE BUTTON BOARD



POWER BOARD



CCD BOARD



PROJECT : KL6B/C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	B TO B CON/LED	1A
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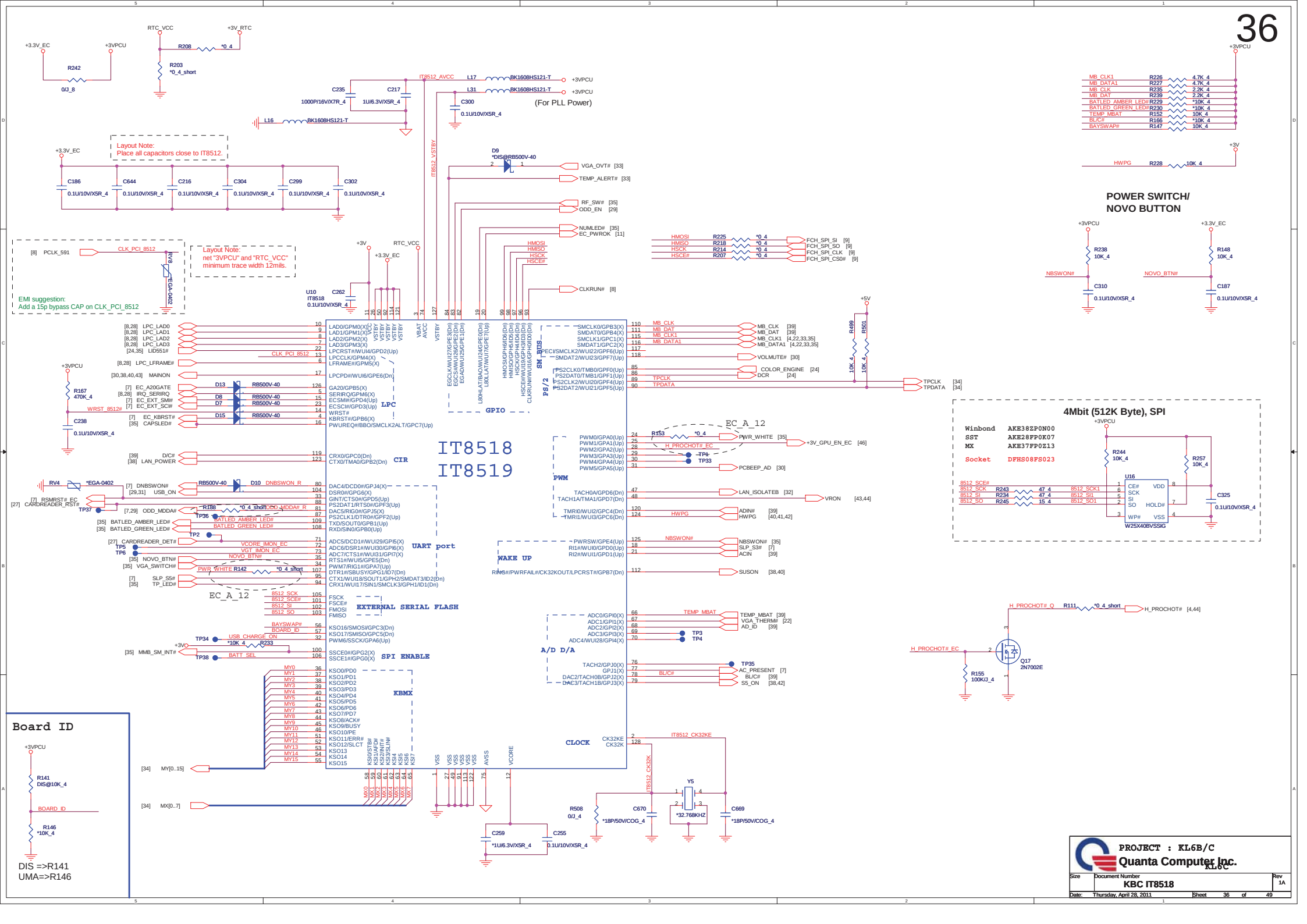
IT8518
IT8519
Board ID
DIS =>R141
UMA=>R146
EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
(For PLL Power)
POWER SWITCH/
NOVO BUTTON
4Mbit (512K Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
Socket DFHS08FS023
W25X40BVSSIG
LPC
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
PS/2
SMBUS
PROJECT : KL6B/C
Quanta Computer Inc.
KL6C
KBC IT8518
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Screw for ME

WLAN

HOLE21 H-TC217BC142D102P2

HOLE22 H-TC217BC75I75D35P2

SMT NUT H=4/7mm

VGA

HOLE18 DIS@H-TC5_5BC4I3D3P2

HOLE20 DIS@H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

CPU BKT

HOLE9 *C142D102N

HOLE17 AGND *HG-TC276BC315D106P2

HOLE13 *HG-TC276BC315D106P2

HOLE12 *HG-TC276BC315D106P2

HOLE11 *HG-TC276BC315D106P2

HOLE16 *HG-TC276BC315D106P2

HOLE7 *HG-TC276BC315D106P2

HOLE4 *HG-TC276BC315D106P2

HOLE6 *HG-TC276BC315D106P2

HOLE3 *H-TC276BC315D106P2

HOLE2 *H-TC276BC315D106P2

HOLE1 *H-TC276BC315D106P2

HOLE10 *H-BS236X150D59PB

HOLE8 *H-BC197D59PB

HOLE14 *Spad-re1010x45np

HOLE23 *Spad-re1010x45np

HOLE15 *spad-kl6-2np

HOLE5 *spad-re160x774np

EMI suggestion

VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	+5V	+1.5V_SUS	+1.5V_SUS	+1.5V_SUS	+1.5V_SUS	+1.1V_DUAL
C422	C772	C6	C462	C812	C564	C464	C461	C47	C33	C828	C829	C830	C831	C448
0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/10V/X5R_4	*100P/25V/X7R_4	*100P/25V/X7R_4	*100P/25V/X7R_4	*100P/25V/X7R_4	0.1U/25V/X5R_4

4/22 change

B-08

ESD suggestion

+5V_S5 / +3V

SC20 0.1U/10V/X5R_4
SC44 0.1U/10V/X5R_4
SC19 0.1U/10V/X5R_4
SC7 0.1U/10V/X5R_4
SC25 0.1U/10V/X5R_4

VIN / +1.5V_SUS / +3V

SC29 0.1U/25V/X5R_4
SC11 0.1U/25V/X5R_4
SC13 0.1U/25V/X5R_4
SC4 0.1U/25V/X5R_4
SC2 0.1U/25V/X5R_4
SC28 0.1U/25V/X5R_4
SC38 0.1U/25V/X5R_4
SC22 *0.1U/25V/X5R_4
SC27 0.1U/25V/X5R_4
SC14 0.1U/25V/X5R_4

SC12 0.1U/10V/X5R_4
SC34 0.1U/10V/X5R_4
SC37 0.1U/10V/X5R_4
SC36 0.1U/10V/X5R_4
SC33 *0.1U/10V/X5R_4
SC35 0.1U/10V/X5R_4
SC32 *0.1U/10V/X5R_4
SC46 0.1U/10V/X5R_4
SC8 0.1U/10V/X5R_4
SC10 0.1U/10V/X5R_4
SC23 0.1U/10V/X5R_4
SC31 0.1U/10V/X5R_4

VIN / +3V

SC9 0.1U/25V/X5R_4
SC16 0.1U/25V/X5R_4
SC18 0.1U/25V/X5R_4
SC21 0.1U/25V/X5R_4
SC43 *0.1U/25V/X5R_4
SC3 0.1U/25V/X5R_4

+5V / +5V_S5

SC45 *0.1U/10V/X5R_4
SC49 *0.1U/10V/X5R_4
SC42 0.1U/10V/X5R_4
SC24 0.1U/10V/X5R_4
SC26 0.1U/10V/X5R_4

HDMIC_5V

SC41 0.1U/10V/X5R_4

GFX_CORE / VIN

SC30 0.1U/25V/X5R_4
SC1 *0.1U/25V/X5R_4

+VDD_CORE / VIN

SC5 *0.1U/25V/X5R_4
SC6 0.1U/25V/X5R_4

+5V_S5 / +1.5V_SUS

SC47 0.1U/10V/X5R_4

VIN / +5V

SC48 *0.1U/25V/X5R_4

SC17 *0.1U/10V/X5R_4
SC15 *0.1U/10V/X5R_4
SC39 *0.1U/10V/X5R_4
SC40 *0.1U/10V/X5R_4

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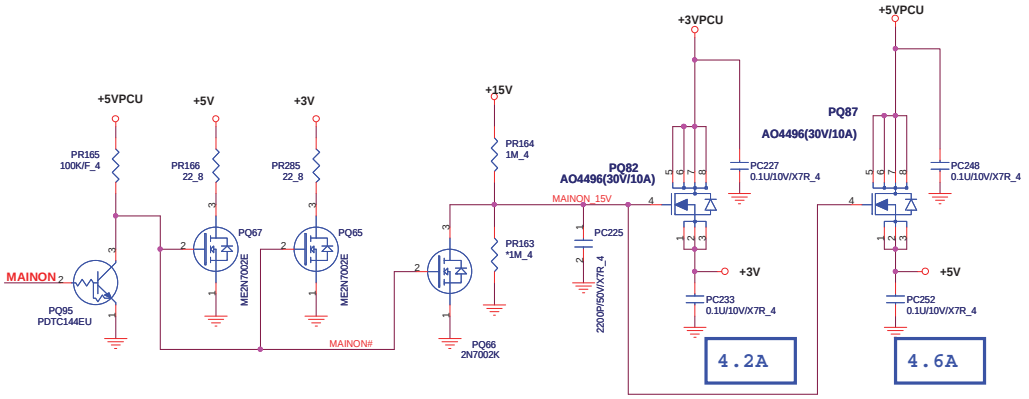
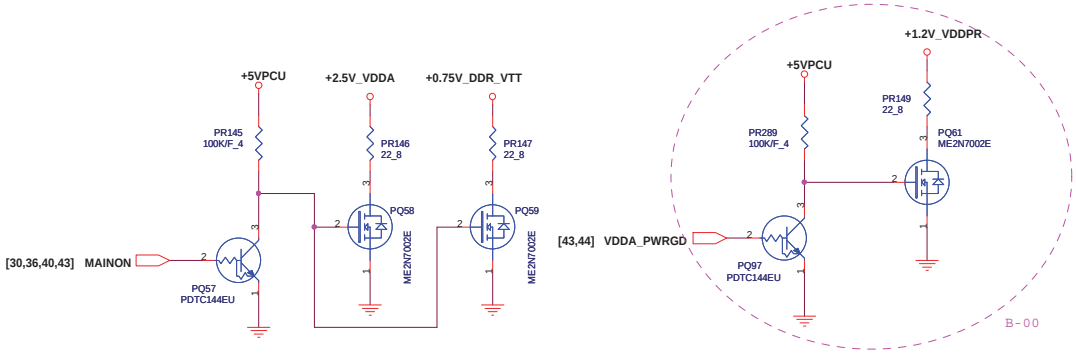
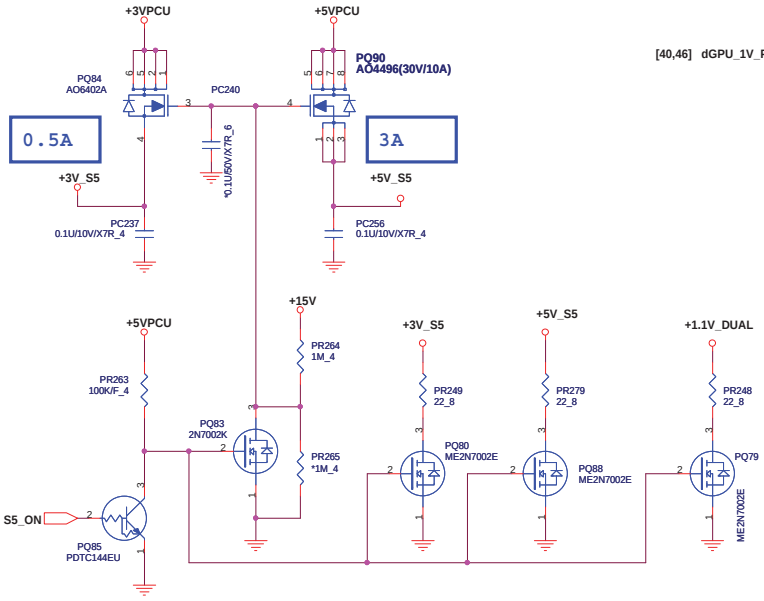
DISCHARGE

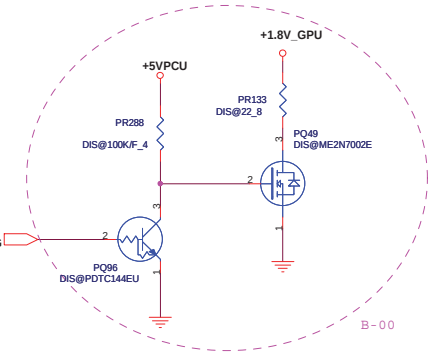
+3V, +5V,+1.5V



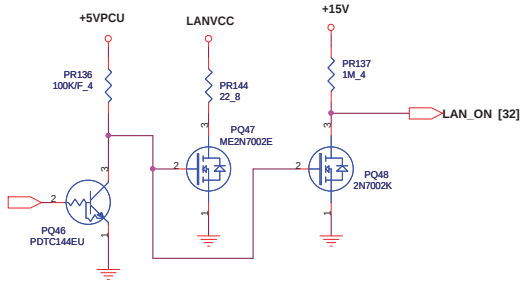


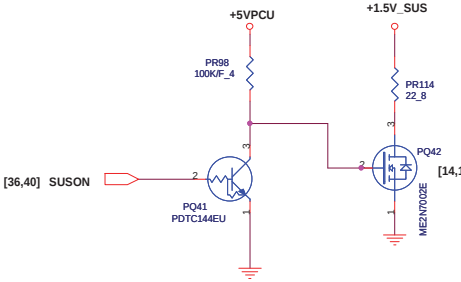
3V_S5,5V_S5

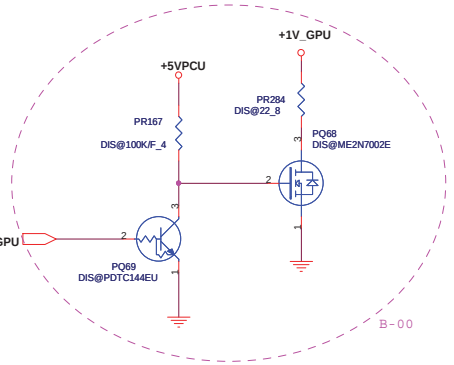




LANVCC







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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

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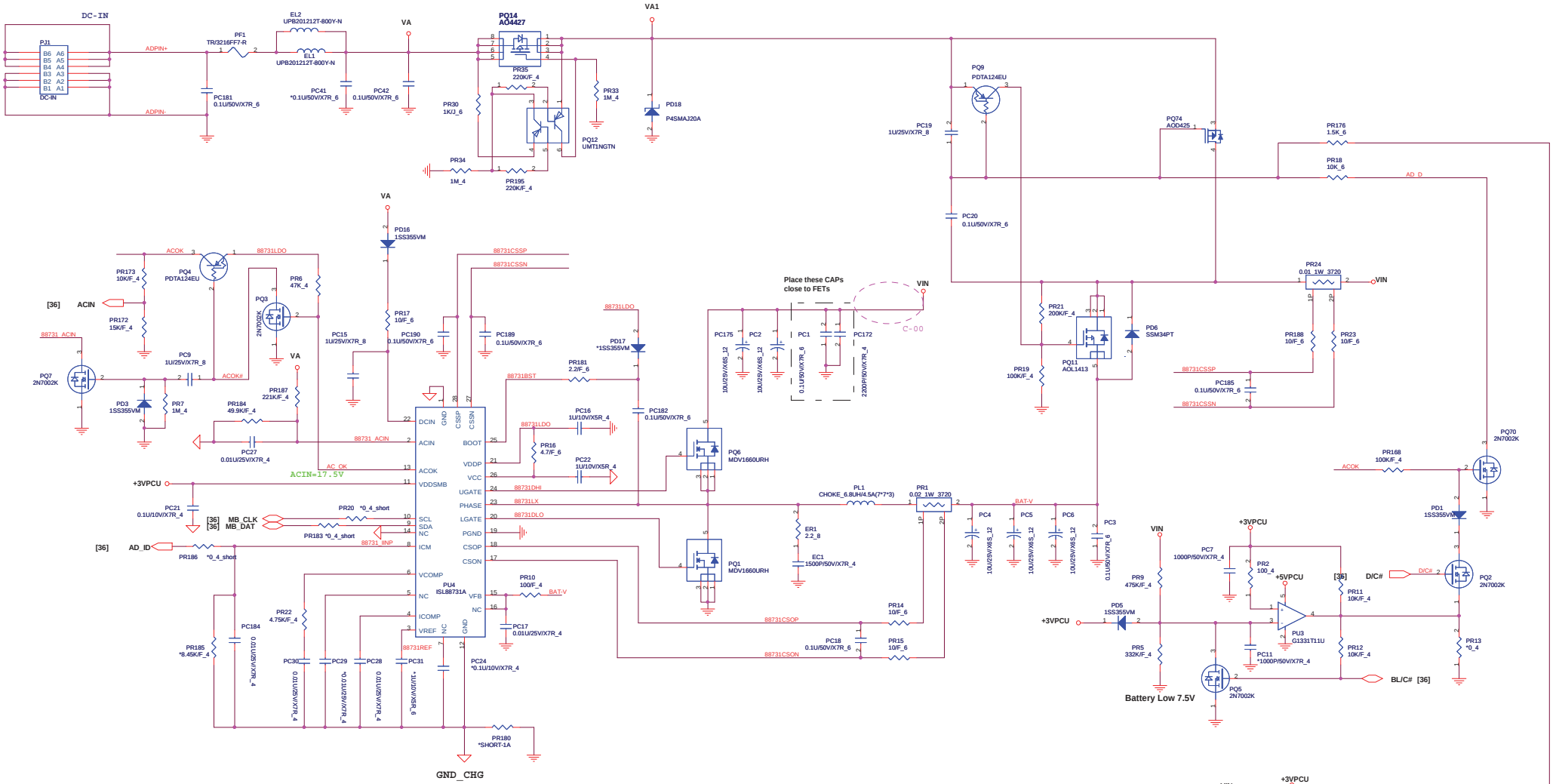

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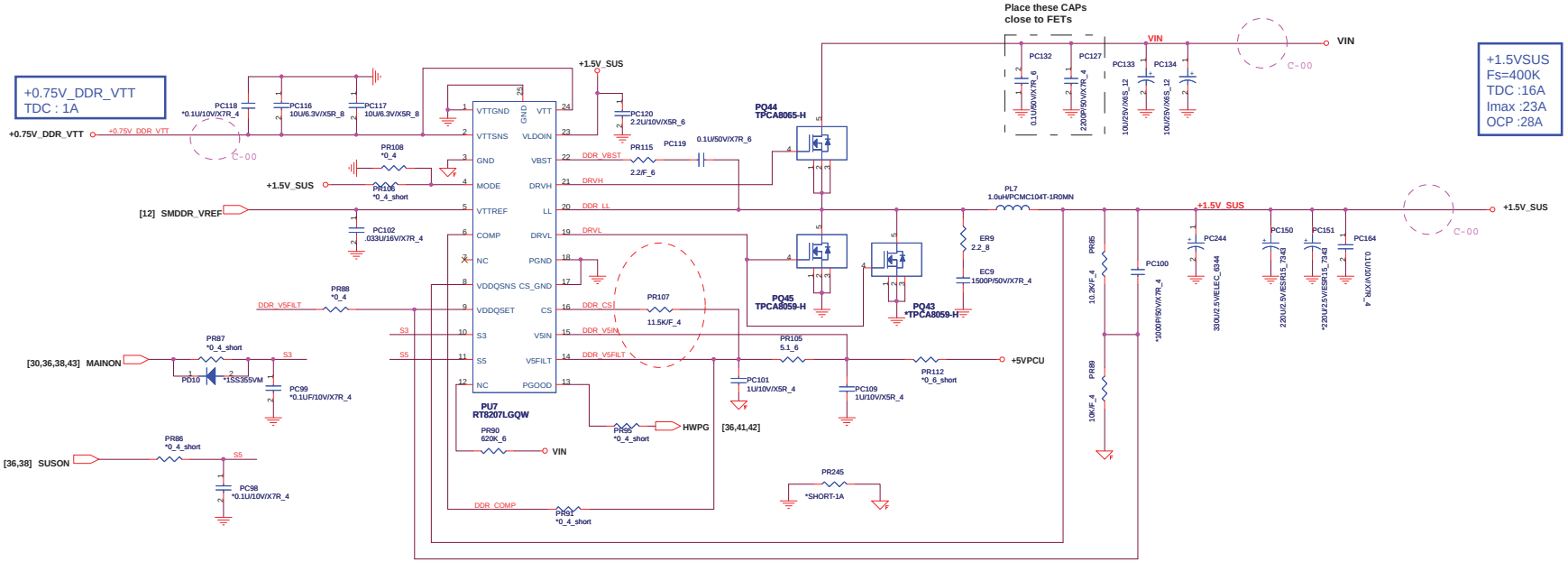
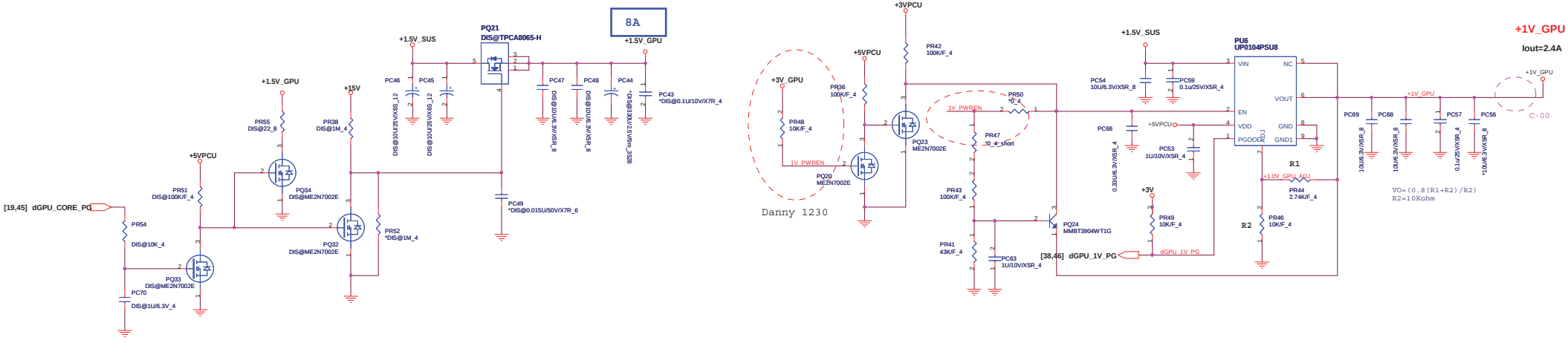
Quanta Computer Inc.

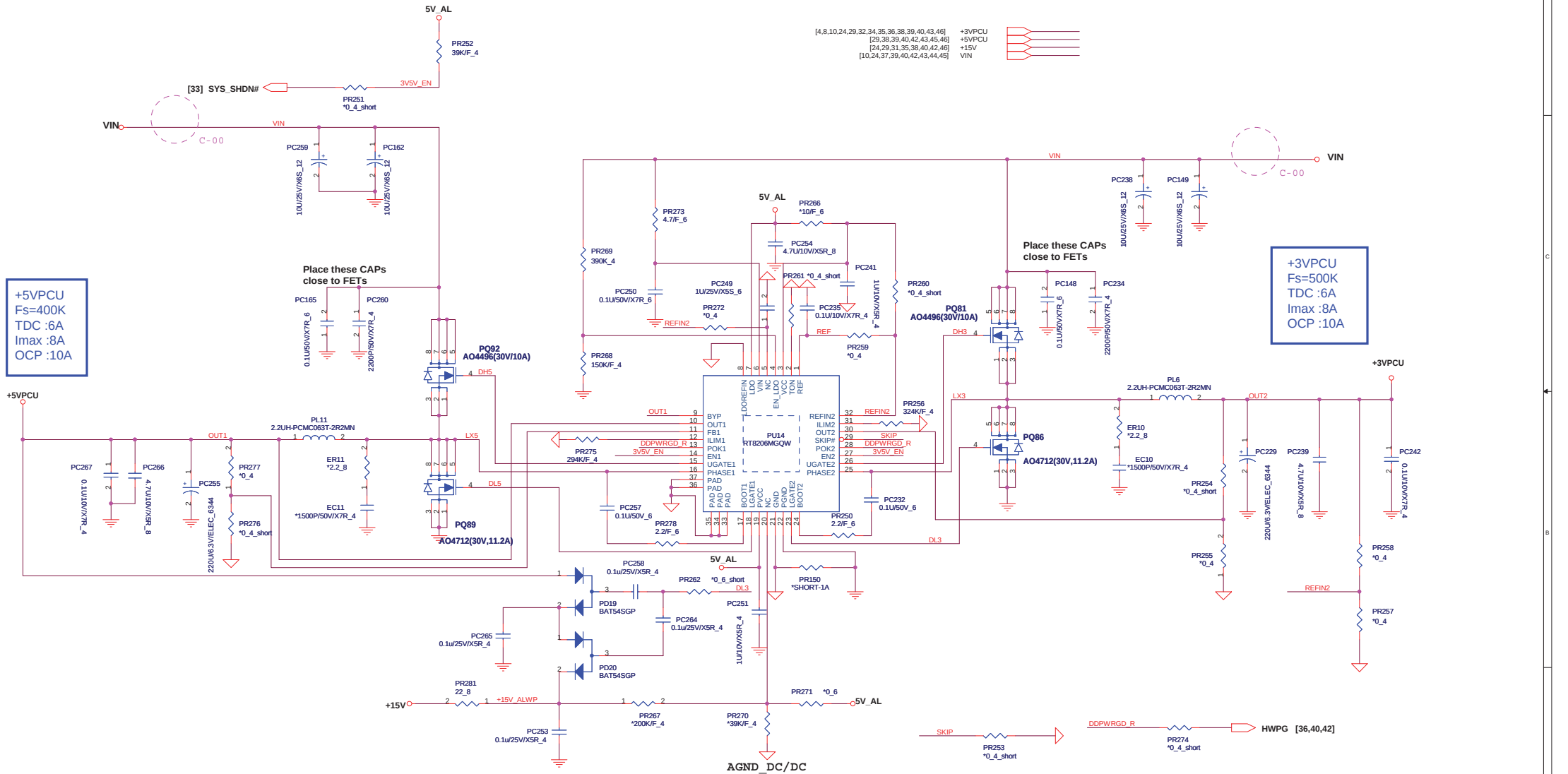
Size	Document Number	Rev
Custom	Charger (ISL88731A)	1A

Date: Thursday, April 28, 2011 Sheet 39 of 49

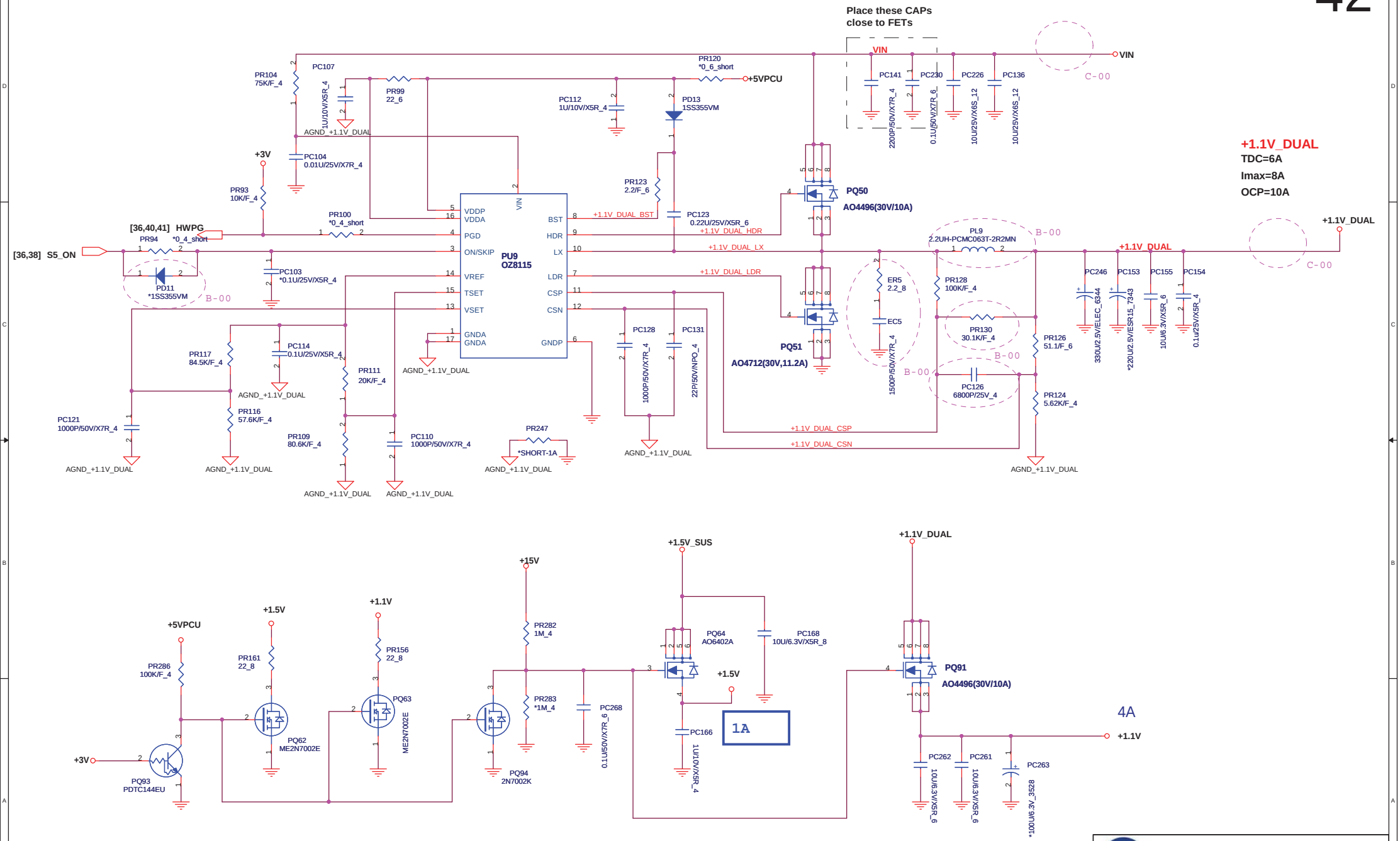




PROJECT : KL6B/C			
Quanta Computer Inc.			
Size: Custom	Document Number: DDR3/0.75V(RT8207LGQW)		Rev: 1A
Date: Thursday, April 28, 2011	Sheet 40 of 49		



PROJECT :	KL6B/C
Quanta Computer Inc.	
Size: Custom	Document Number: 3V/5V (RT8206MGQW)
Rev: 1A	
Date: Thursday, April 28, 2011	Sheet 41 of 49


Place these CAPs
close to FETs
VIN
+1.1V_DUAL
TDC=6A
Imax=8A
OCP=10A
PU9
OZ8115
PQ50
AO4496(30V/10A)
PQ51
AO4712(30V,11.2A)
PL9
2.2UH-PCMC063T-2R2MN
[36,40,41] HWPG
[36,38] S5_ON
+5VPCU
+3V
+1.5V_DUAL_BST
+1.1V_DUAL_HDR
+1.1V_DUAL_LX
+1.1V_DUAL_LDR
+1.1V_DUAL_CSP
+1.1V_DUAL_CSN
AGND_+1.1V_DUAL
+1.5V_SUS
+15V
+1.5V
+1.1V
PQ62
ME2N7002E
PQ63
ME2N7002E
PQ64
AO6402A
PQ91
AO4496(30V/10A)
PQ93
PDTC144EU
PQ94
2N7002K
1A
4A
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Quanta Computer Inc.
+1.1V_DUAL/+1.0V_GPU
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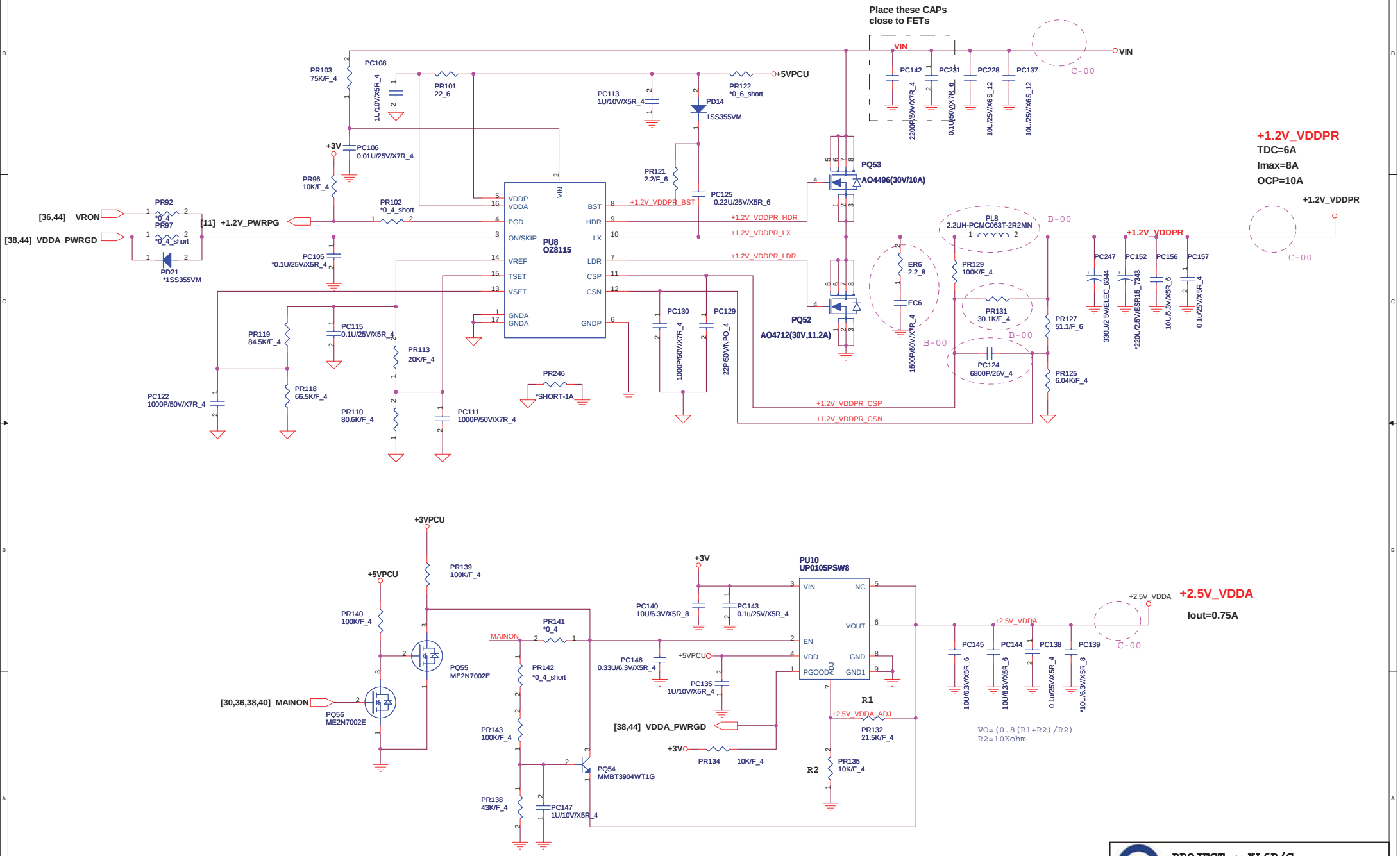

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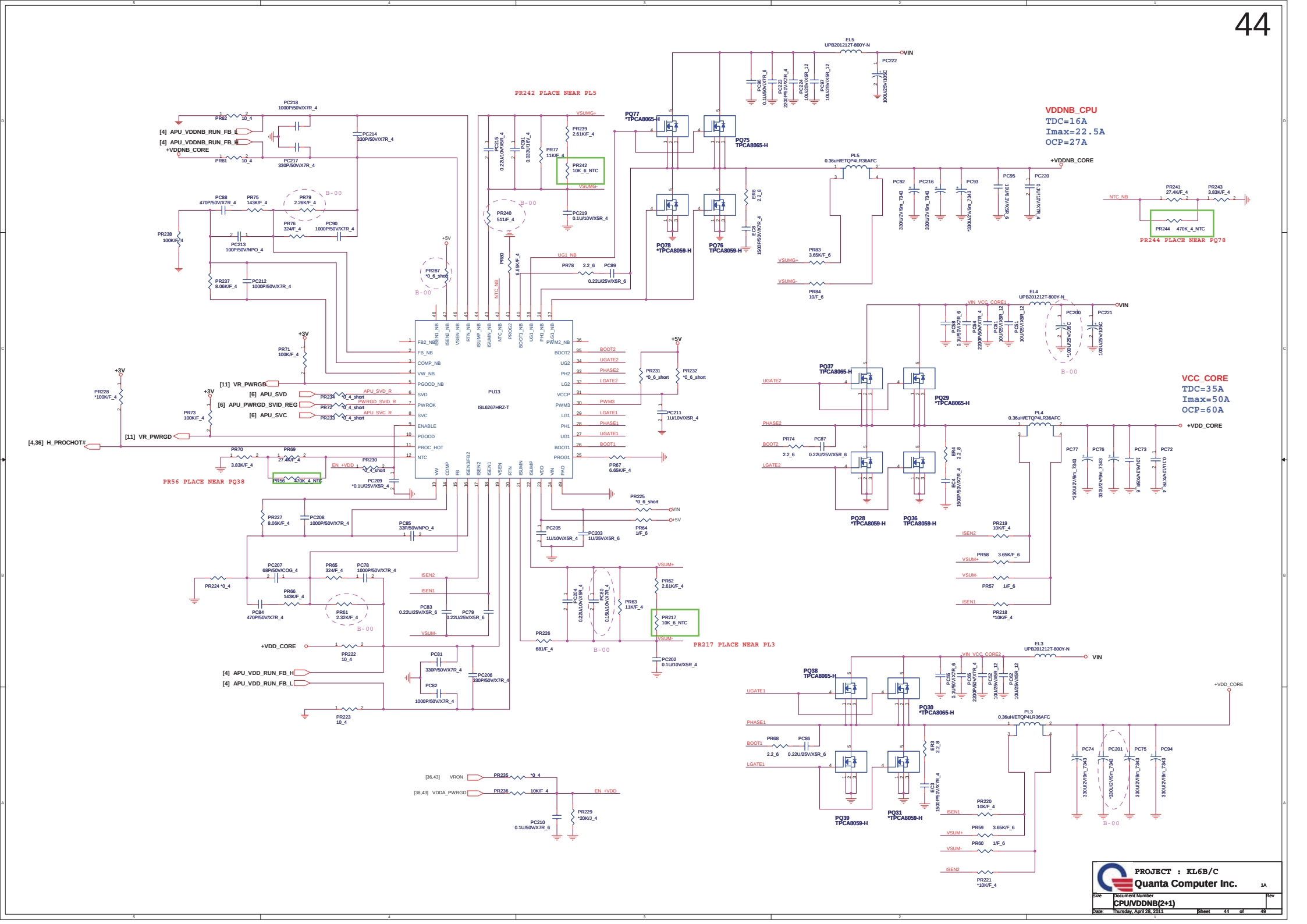
Size	Document Number	Rev
	+1.2V_VDDPR (OZ8115)/+2.5V_VDDA	1A
Date: Thursday, April 28, 2011	Sheet 43 of 49	



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Quanta Computer Inc.			1A
Size	Document Number		Rev
	CPU/VDDNB(2+1)		
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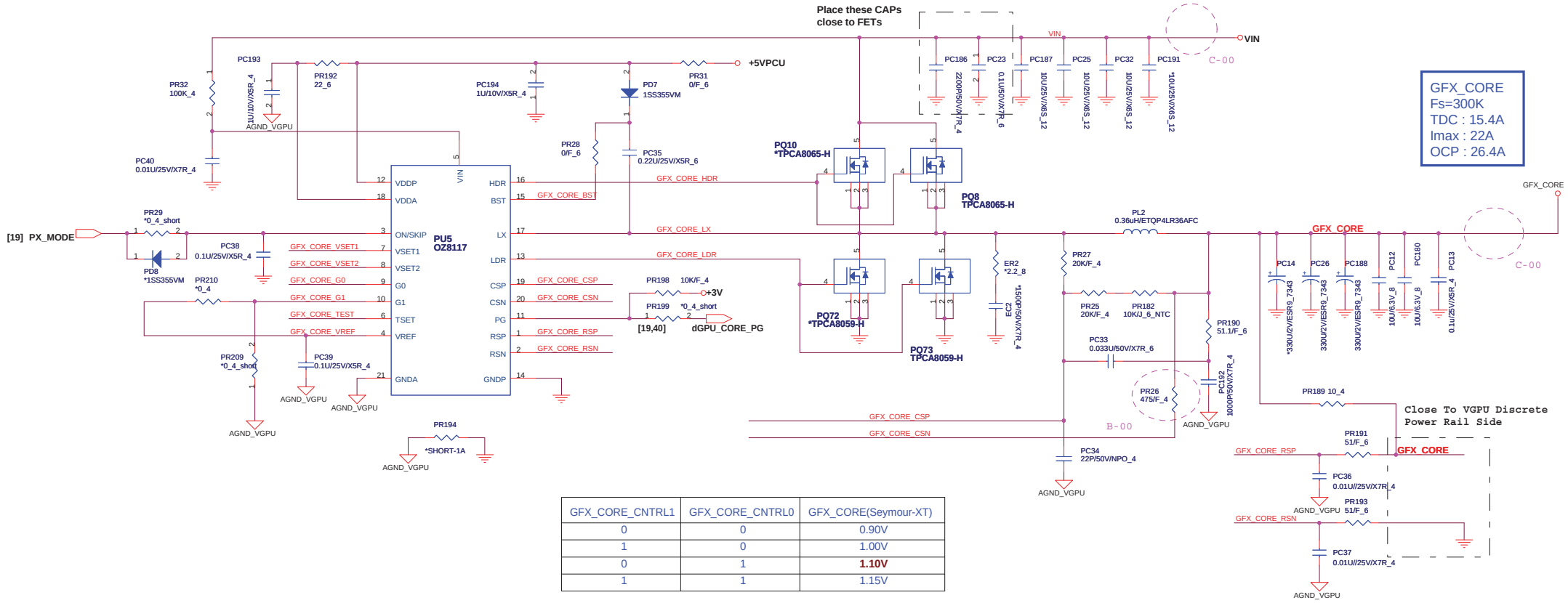
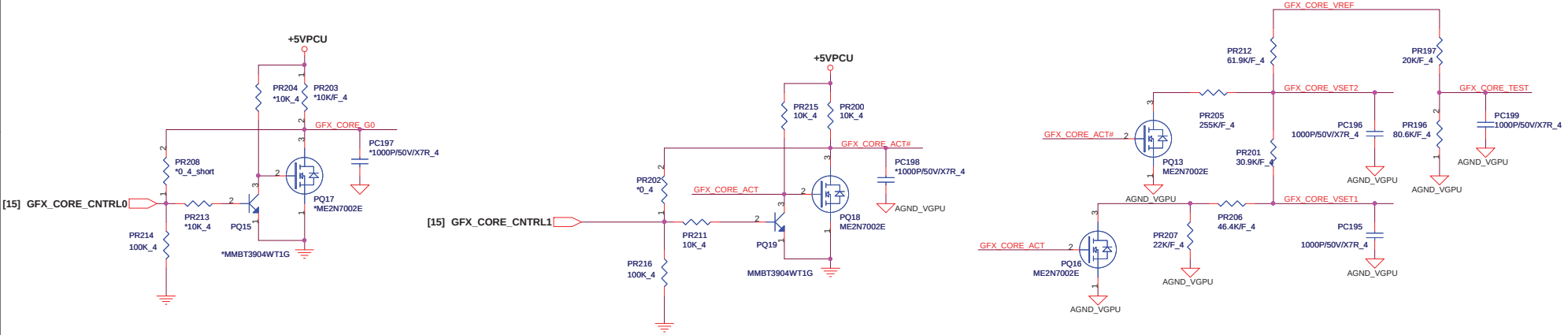


GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	GFX_CORE(Seymour-XT)
0	0	0.90V
1	0	1.00V
0	1	**1.10V**
1	1	1.15V



Quanta Computer Inc.	PROJECT : KL6B/C	
Size	Document Number: GFX_CORE (OZ8117)	Rev: 1A
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+1.8V_GPU [15,17,18,22,38]
+3VPCU [4,8,10,24,29,32,34,35,36,38,39,40,41,43]
+5VPCU [29,38,39,40,41,42,43,45]
GFX_CORE [17,19,37,45]
+1V_GPU [14,15,17,18,38,40]
+3V_GPU [14,15,16,17,19,22,38,40]
+15V [24,29,31,35,38,40,41,42]

+1.8V_GPU
TDC : 1.9A

+3VPCU
C-00
PC169 10U/6.3V_8
PC171 10U/6.3V_8
PC170 0.1U/10V_4
PR162 22_6
+3VPCU_+1.8V_GPU
PC167 1U/10V/X5R_4
AGND_+1.8V_GPU
[38,40] dGPU_1V_PG
PR159 *0_4_short
PC163 *0.01U/50V/X7R_4
PR151 57.6K/F_4
AGND_+1.8V_GPU

PU11 TPS51311RGTR
VIN VIN VDD RES AGND EN MODE
SW SW SW VBST FB COMP PGOOD PGND
AGND AGND AGND AGND AGND AGND PGND

PL10 1UH/11A-PCMD063T-1R0MN
PR153 0_6
PC158 0.1U/25V_4
ER7 *2.2_8
EC7 *1500P/50V/X7R_4
+1.8V_GPU_FB
PR152 1.43K/F_4
PC160 2200P/50V/X7R_4
PR158 47/F_4
PC161 3300P/50V/X7R_4
PC159 100P/25V_4
PR155 2K/F_4
PR160 1K/F_4
AGND_+1.8V_GPU
PR157 *0_4_short
PR154 10K/J_4
+3V
PR280 *SHORT-1A
dGPU_1.8V_PG [8]

+1.8V_GPU
C-00
PC236 0.1U/10V_4
PC245 10U/6.3V_8
PC243 10U/6.3V_8

0.06A

+3V_GPU
PR37 DIS@22_8
PQ22 DIS@ME2N7002E
+15V
PR40 DIS@1M_4
PQ27 DIS@ME2N7002E
PR39 *DIS@1M_4
+3V
PQ26 DIS@AO6402A
PC71 DIS@10U/25V/X6S_12
PC67 DIS@10U/6.3V/X5R_8
PC50 *DIS@0.1U/10V/X7R_4
PC60 *DIS@0.015U/50V/X7R_6
+3V_GPU

+5VPCU
PR53 DIS@100K/F_4
[8] dGPU_PWREN
PD9 *DIS@1SS355VM
[36] +3V_GPU_EN_EC
PQ35 DIS@ME2N7002E

B-00

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V (TPS51311RGTR)	1A
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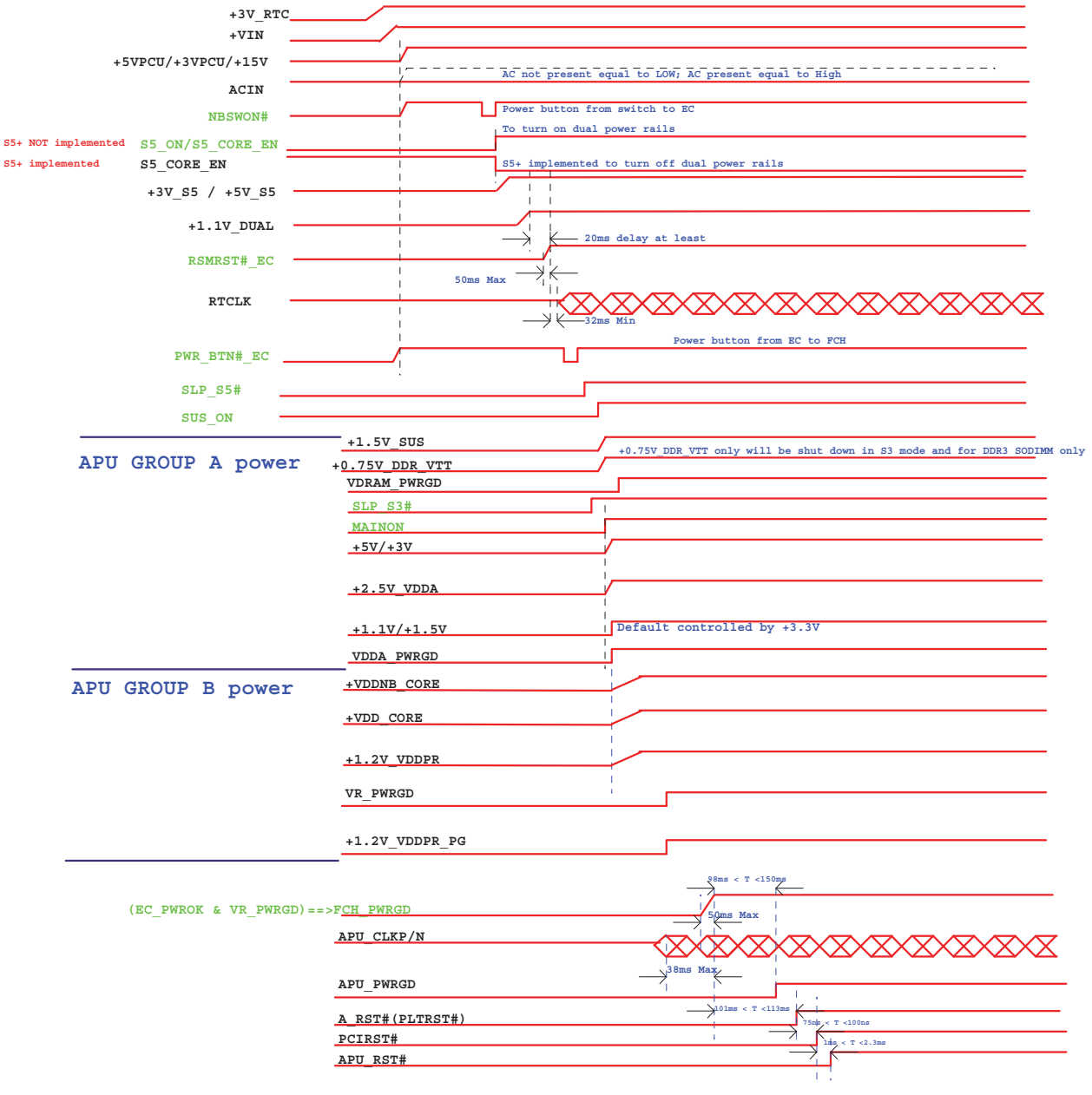
Z475 Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:
1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Robson-Pro M2/Capilano-LP M2 package Power-on sequence

All power rails reach nominal within 20ms

1 => +3V_GPU
2 => +VGPU_CORE/+1V_GPU
3 => +VGPU_CORE PWRGD to enable +1.5V_GPU
4.=> +1V_GPU PWRGD to enable +1.8V_GPU

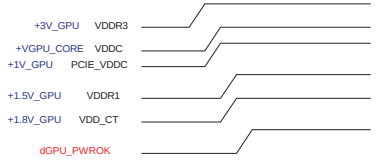
NOTE

1.EC (EC_PWR_EN) or FCH (PE_GPIO1) to turn on +3V_GPU

2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU
(+1V_GPU will ramp up before +VGPU_CORE)

3.+VGPU_CORE PWRGD to enable +1.5V_GPU

3.+1V_GPU PWRGD to enable +1.8V_GPU



TRAVIS_L ANX3110 power sequecne

1.+3V must lead +1.2V_TRAVIS

NOTE: EC output TRAVIS_EN# after receive +1.2V_VDDPR_PG

2.+1.2V_TRAVIS must lead TRAVIS_RST#

NOTE: FCH must output PCIE_RST#_TRAVIS or APU_PCIE_RST# after +1.2V_TRAVIS ready

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Size | Document Number | Rev 1A
POWER SEQUENCE
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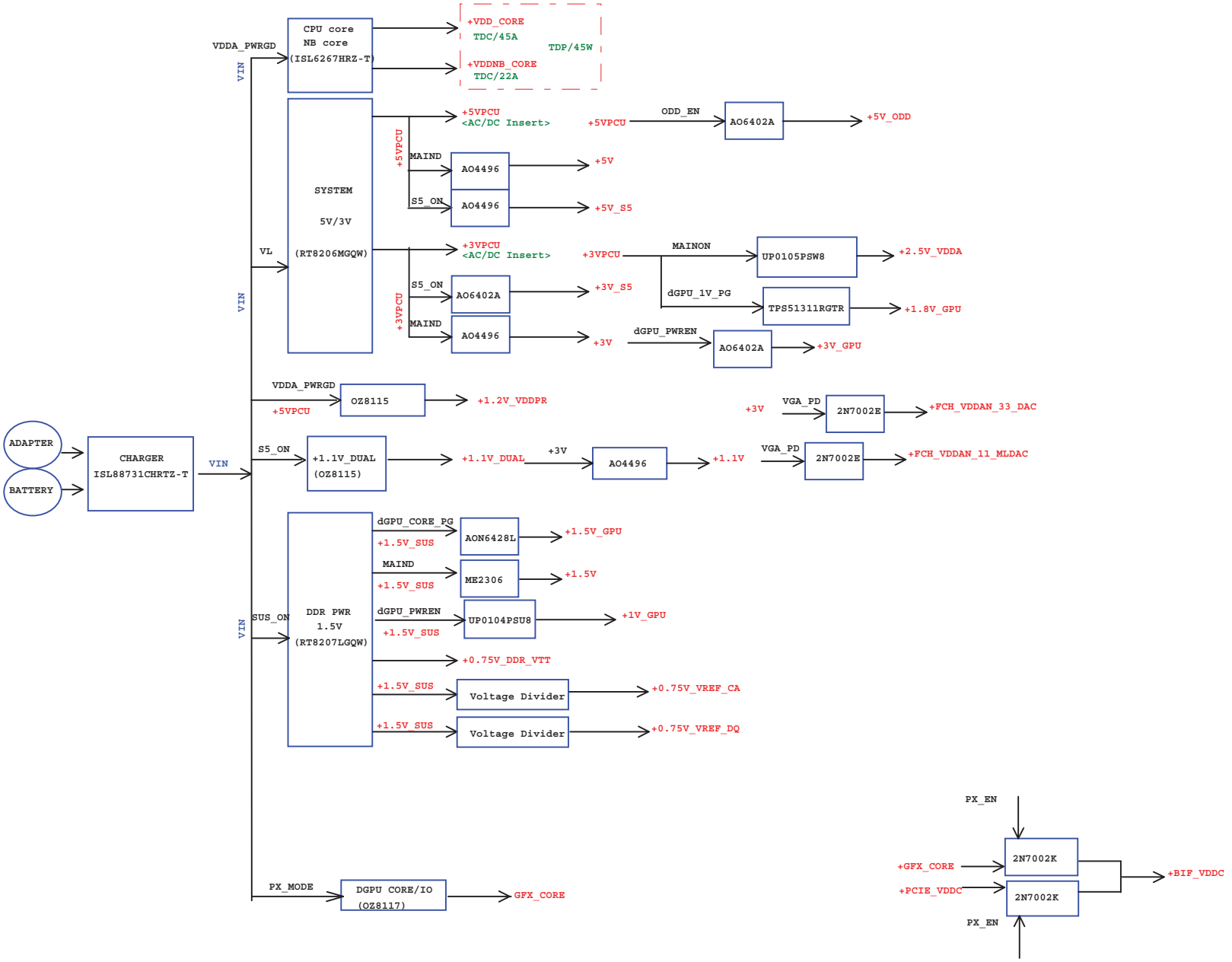

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Quanta Computer Inc.
Size
Document Number
Power Tree
Rev
1A
Date: Thursday, April 28, 2011
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KL6C / Z475 Schematic EE EC Tracking list

EC #	Page	CMVC #	Description	Date	Part Affected
A-01	4		Add level shifter design for LVDS PWM signal	0208	
A-02	4		Sys_pwrok pull high from 10K to 100K	0208	
A-03	9		Design issue need to swap SPI SI/SO signal	0208	
A-04	11		Disable Strap pin (EC disable) for CRT no function issue	0208	
A-05	14		DGPU reset change design to be controlled by GPIO only	0208	
A-06	16		Disable DGPU JTAG DEBUG MODE	0208	
A-07	23		Remove Travis IC power switch schematic for cost down	0208	
A-08	23		Desgin issue need to swap LVDS EDID signal	0208	
A-09	35		Change Resistor vaule to adjust the brighness of LED	0208	
A-10	7		Change USB port for USB2.0 & CardReader to USB.(Disable Hub3)	0208	
A-11	25		Change PU resistor value from 100ohm to 100kohm	0208	
A-12	36		Change EC pin to default PL to aviod PWR LED light one time as DC-IN	0208	
A-13	25		I2C level shift IC change to stuff.	0211	
A-14	22		no need to enable HDMI audio function in DGPU	0216	
A-15	7		Add Thermal trip PU resistor	0216	
A-16	18		Remove bead & cap for cost down	0218	
A-17	35		Add R188 ODD_MDDA# to connect to EC	0224	
A-18	35		Remove VGA SW2(ATI can't support HW swithch)	0224	
A-19	22		Remove VGA External thermal IC	0224	
SIV					
B-01	35		Add CCD P_SW on/off (Add C578, Q62, R467, Q63, R468 ; Del R455)	0306	
B-02	33		Connect to VGA Therm_Die use Channel 1.Del Q58(WLAN) to for CPU used.	0306	
			Add: R78, R77 ; Del: Q58		
B-03	9		Change U17 VDD to +3V_S5	0306	
B-04	9		ADD SPI_HOLD# GPIO control, reserve R469	0306	
B-05	4		ADD SM_LV_CLK & SM_LV_DAT to connect FCH; Reserve R496 & R497	0306	
B-06	9		AUXCAL change to power rail for VGA Power Down Feature	0306	
B-07	22		ADD MOSFET for VGA SMBUS; ADD Q19, Q20, R158, R159	0306	
B-08	23		Del R8 ,R177,R99, R41,R42,R43 for remove LVDS reserve schematic	0307	
B-09	25		Delete R389,R401,D20,D21,D22,D23,Q36,Q37 cost reduce fail	0316	
B-10	25		Add R657,R658,R659,R660,R661,R662,R663,R664,C826,C827,U49	0316	
			2nd source verify	0316	
B-11			EMI solution	0316	
			POP R602,R601,R598,R597 120ohm	0316	
			POP CML3,CML4,CML2,CML1,L47	0316	
			Remove R464,R456,R599,R600,R451,R453,R412,R413,R465,R466 0ohm	0316	
			POP C408,C422,C749	0316	
			POP C391,C392	0316	
			Reserve C828,C829,C830,C831	0316	
B-12	06		POP R655,R656 Remove U18,R337,R330 Internal notice update	0317	
			Change Q61 PN:BA05L060000 Internal notice update	0317	
			Remove C207	0317	
B-13	34		CN5 Modify footprint to 85208-24071-24p-l	0317	
B-13	31		Add C832 for EMI solution	0318	
B-14			Change C515 & C516 to 27pF to fine tune timing	0321	
			Change C387 & C386 to 27pF to fine tune timing	0321	
			Change C188 & C184 to 27pF to fine tune timing	0321	
			Change C365 & C366 to 27pF to fine tune timing	0321	
SVT					
C-01	04		Change R541,R547 to *0_4_short	0418	
	06		Change R535,R537,R545 to *0_4_short	0418	
			Delete U18,R655,R656,R337,R330; J1,R587,R336,R323,R305,R580,R577	0418	
	07		Change R468,R287,R545,R169, R521,R533,R256,R317,R258,R552,R528 to *0_4_short	0418	
	08		Change R200,R183 to *0_4_short; Change R427 to *0_6_short	0418	

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Quanta Computer Inc.

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Custom	EC Tracking Record A	1A

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KL6C / Z475 Schematic EE EC Tracking list

EC #	Page	CMVC #	Description	Date	Part Affected
C-01	09		Change R263,R254,R247 to *0_4_short	0418	
	19		Change R157 to *0_4_short	0418	
	23		Change R83,R50,R46,R91 to *0_4_short; change R650 to *0_8_short	0418	
	24		Change R2 to *0_4_short; Change R7,R28 to *0_8_short	0418	
	25		Change R660,R661,R662,R663 to *0_4_short	0418	
			Delete U42,R603,R605, R381,R382,R384,R386,R399,R400; C375, C377,C448,C449,C459	0418	
	28		Change R398,R424,R428 to *0_4_short	0418	
			Change R397 to *0_8_short	0418	
	29		Change CML1 footprint to "choke-wcm2012-4p"	0418	
			Delete R412,R413; Change R365,R3698,R604 to *0_8_short	0418	
	31		Change R438 to *0_4_short	0418	
			Change CML2,CML3,CML4 footprint to "choke-wcm2012-4p"	0418	
			Delete R451,R453,R599,R600,R456,R464	0418	
	32		Change R444 to *0_4_short; Change R418,R421,R435,R449 to *0_8_short	0418	
	33		Change R77,R78 to *0_4_short; Change R595 to *0_8_short	0418	
	34		Change L34 to *0_8_short	0418	
	35		Change L47 footprint to "choke-wcm2012-4p"	0418	
			Delete R465,R466; Change R161,R162 to *0_6_short	0418	
	36		Change R111,R142,R188,R203 to *0_4_short	0418	
	27		Change R646 to *0_8_short	0418	
	12		Change R394 to *0_6_short	0418	
C-02	31		change U47 Pin8 design	0422	
	37		Add C448 (0.1u CAP) for EMI solution	0422	
C-03	4		delete APU debug funciton, R570, R579,R583,R584,R596	0425	
	34		Mount CA1,CA2,CA3,CA4,CA5,CA6 for EMI solution	0426	
	35		Change Q62 PN to BAM34040001	0426	
	10		Change Q29,Q32 PN to BAM34040001	0426	
C-04	25		Change value of R601,R602,R597,R598 to 140 ohm for HDMI issue	0428	
			Change value of R383,R385,R387,R388,R391,R392,R395,R402 to 560 ohm for HDMI issue	0428	

PROJECT : KL6B/C

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC Tracking Record B	1A

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