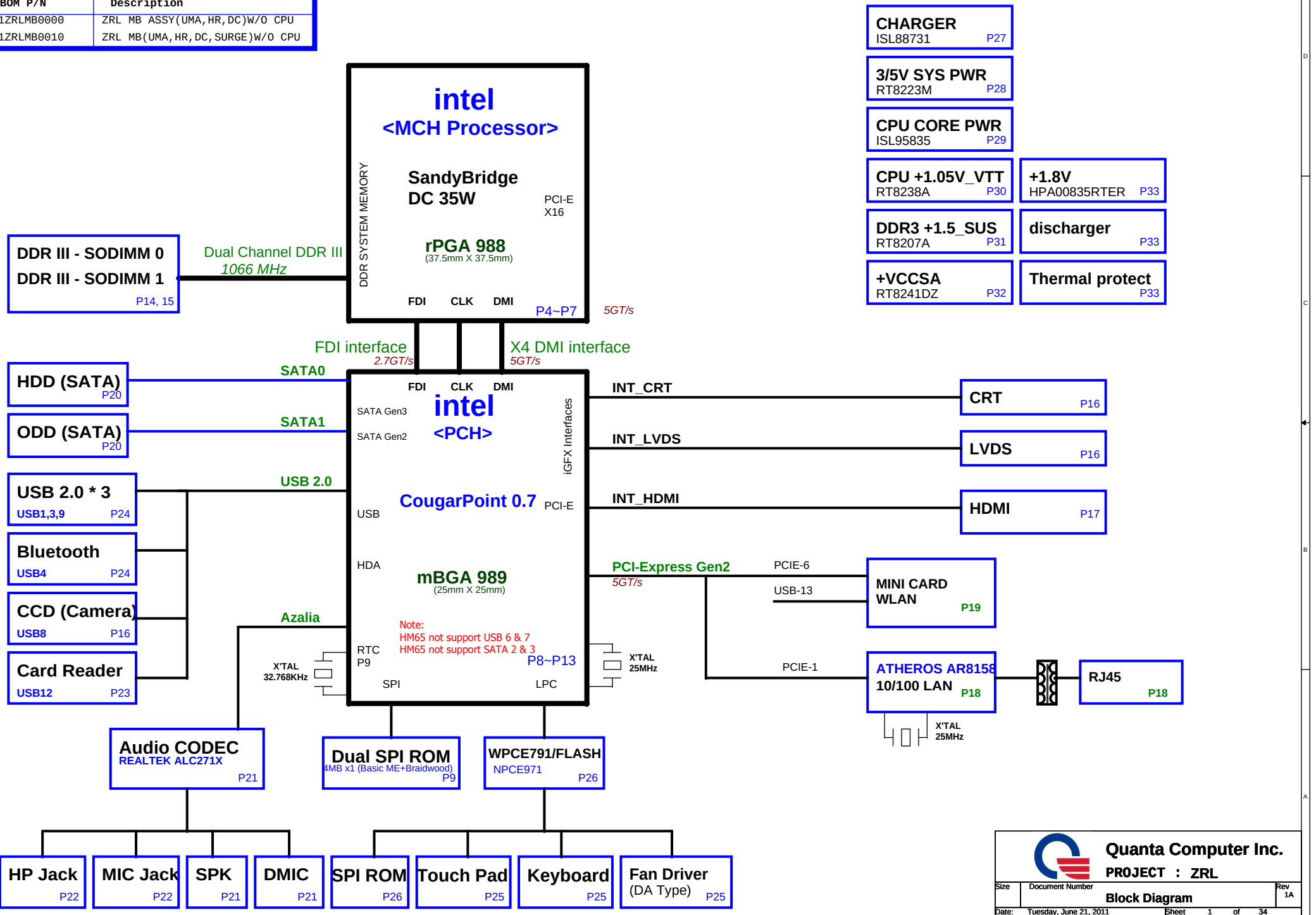
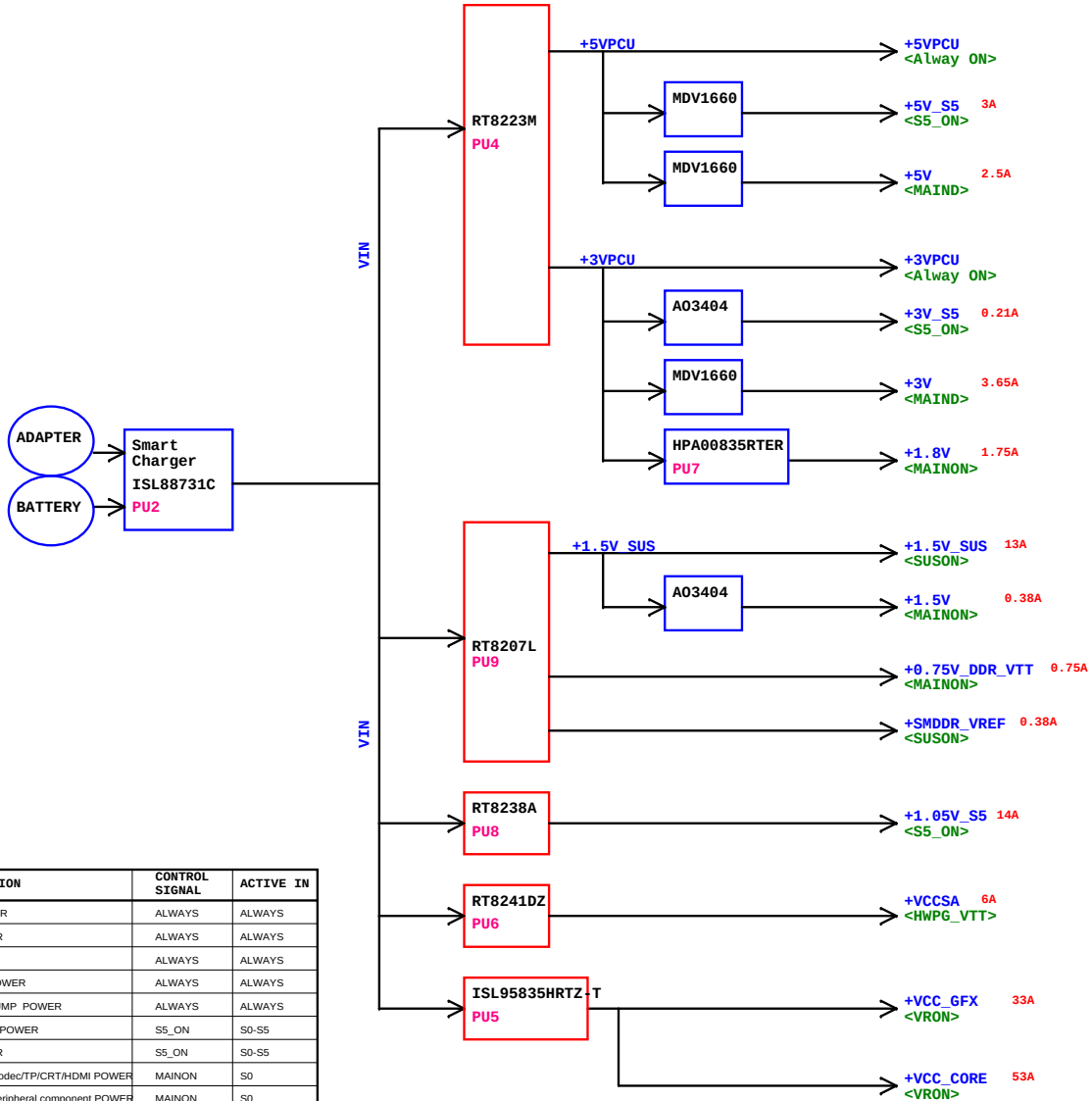
ZRL BLOCK DIAGRAM

VER : 1A	
BOM P/N	**Description**
31ZRLMB0000	ZRL MB ASSY(UMA,HR,DC)W/O CPU
31ZRLMB0010	ZRL MB(UMA,HR,DC,SURGE)W/O CPU



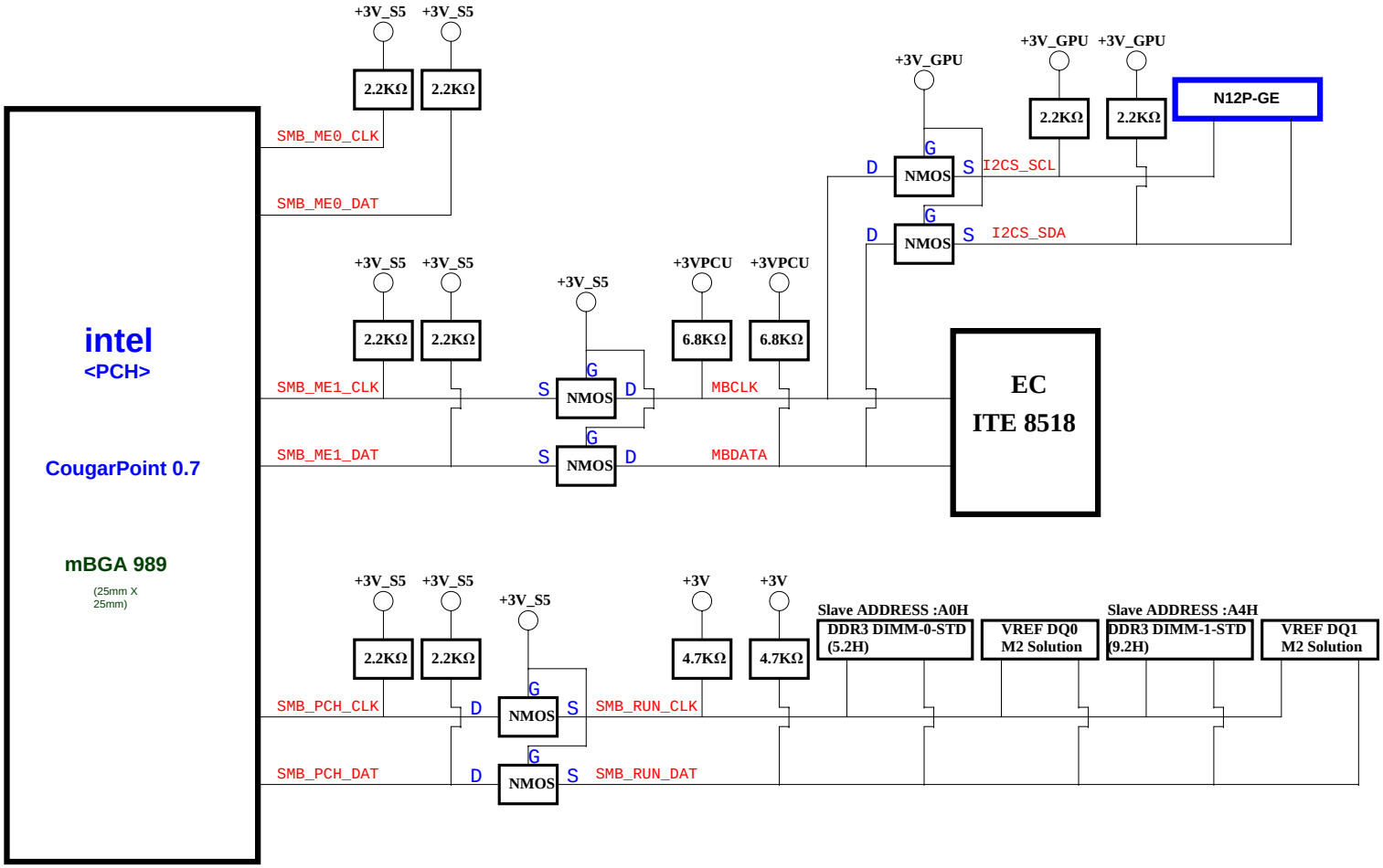
Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	Block Diagram		1A
Date: Tuesday, June 21, 2011		Sheet 1 of 34	

ZRL power tree



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable



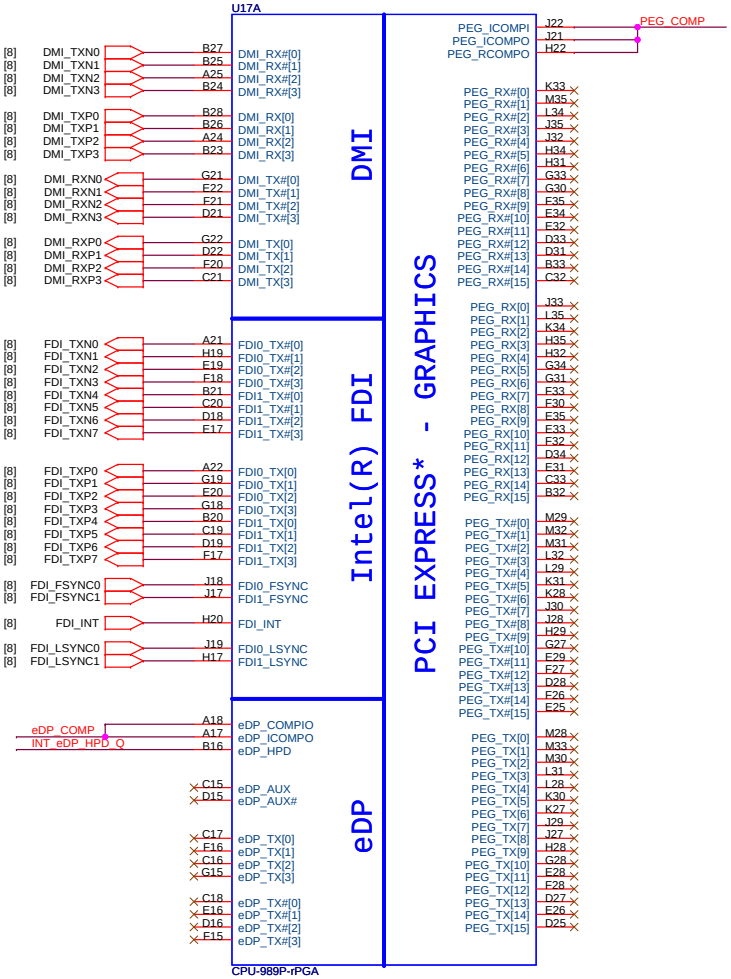
Quanta Computer Inc.
PROJECT : ZRL

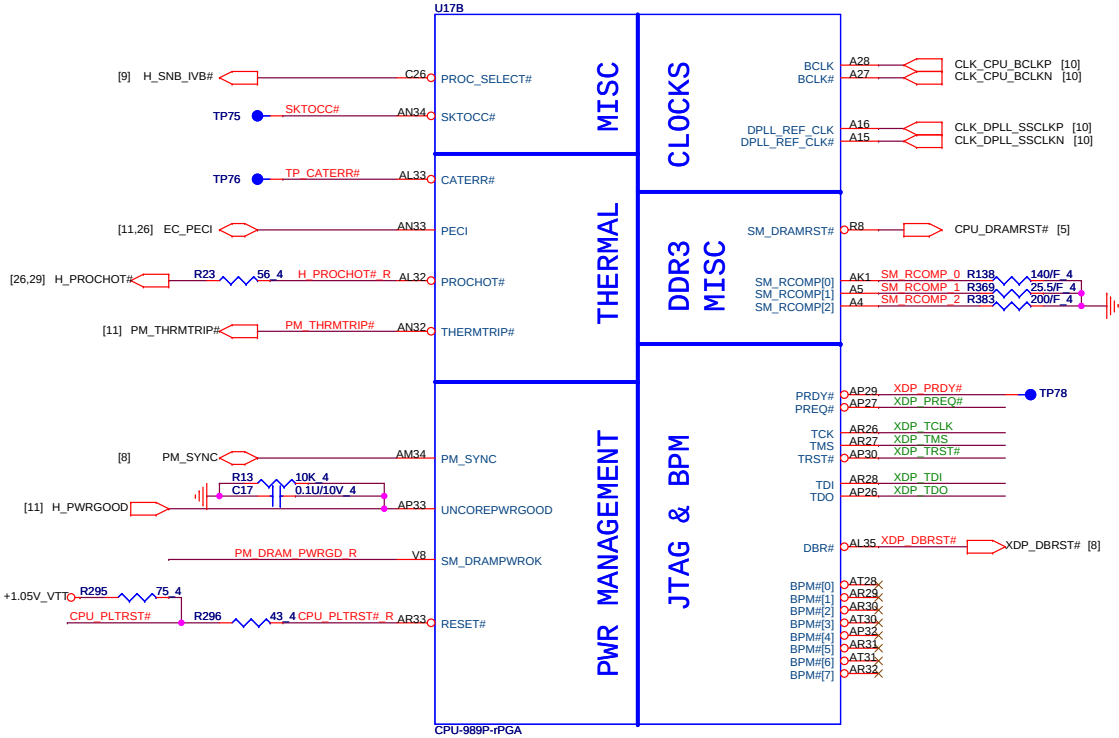
Size	Document Number	Rev
	SMBus Address	1A
Date: Tuesday, June 21, 2011	Sheet 3 of 34	

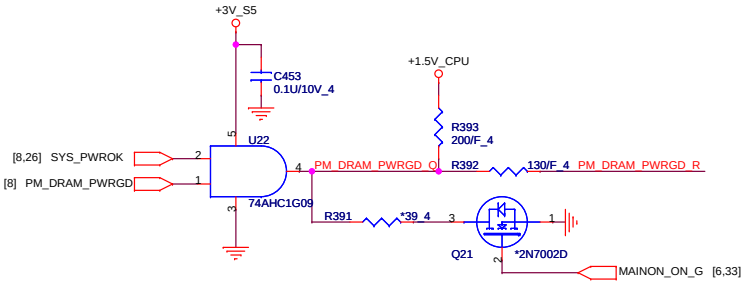
Sandy Bridge Processor (DMI,PEG,FDI)

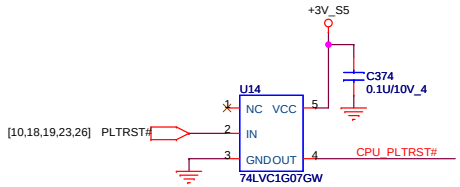
Sandy Bridge Processor (CLK,MISC,JTAG)

04

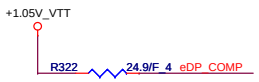




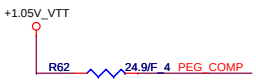




DP & PEG Compensation



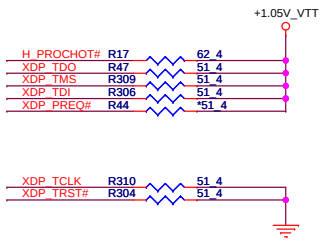
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

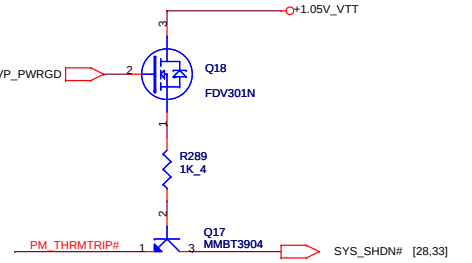


PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)





eDP Hot-plug

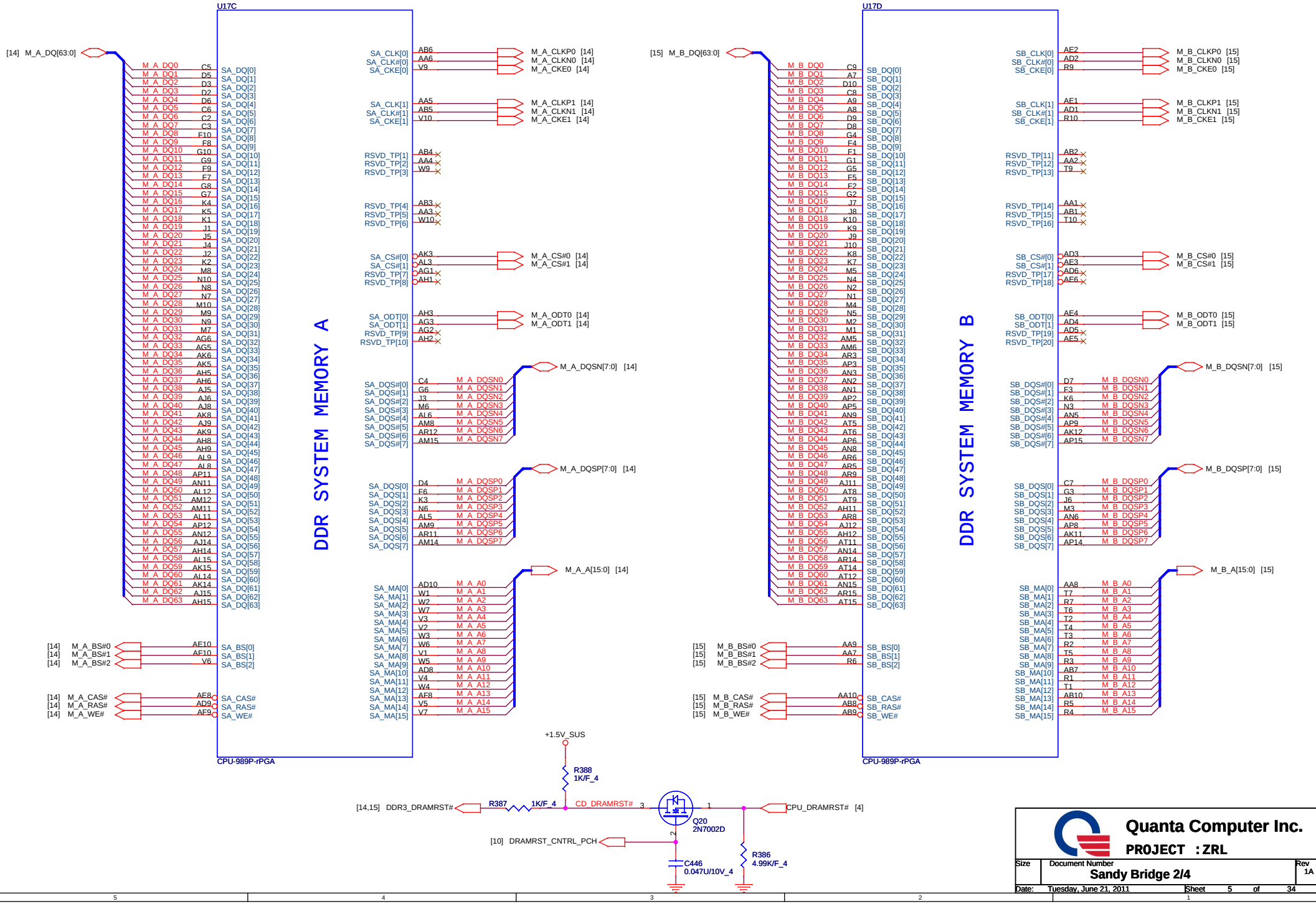
Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Sandy Bridge 1/4	1A
Date: Tuesday, June 21, 2011	Sheet 4 of 34	

Sandy Bridge Processor (DDR3)

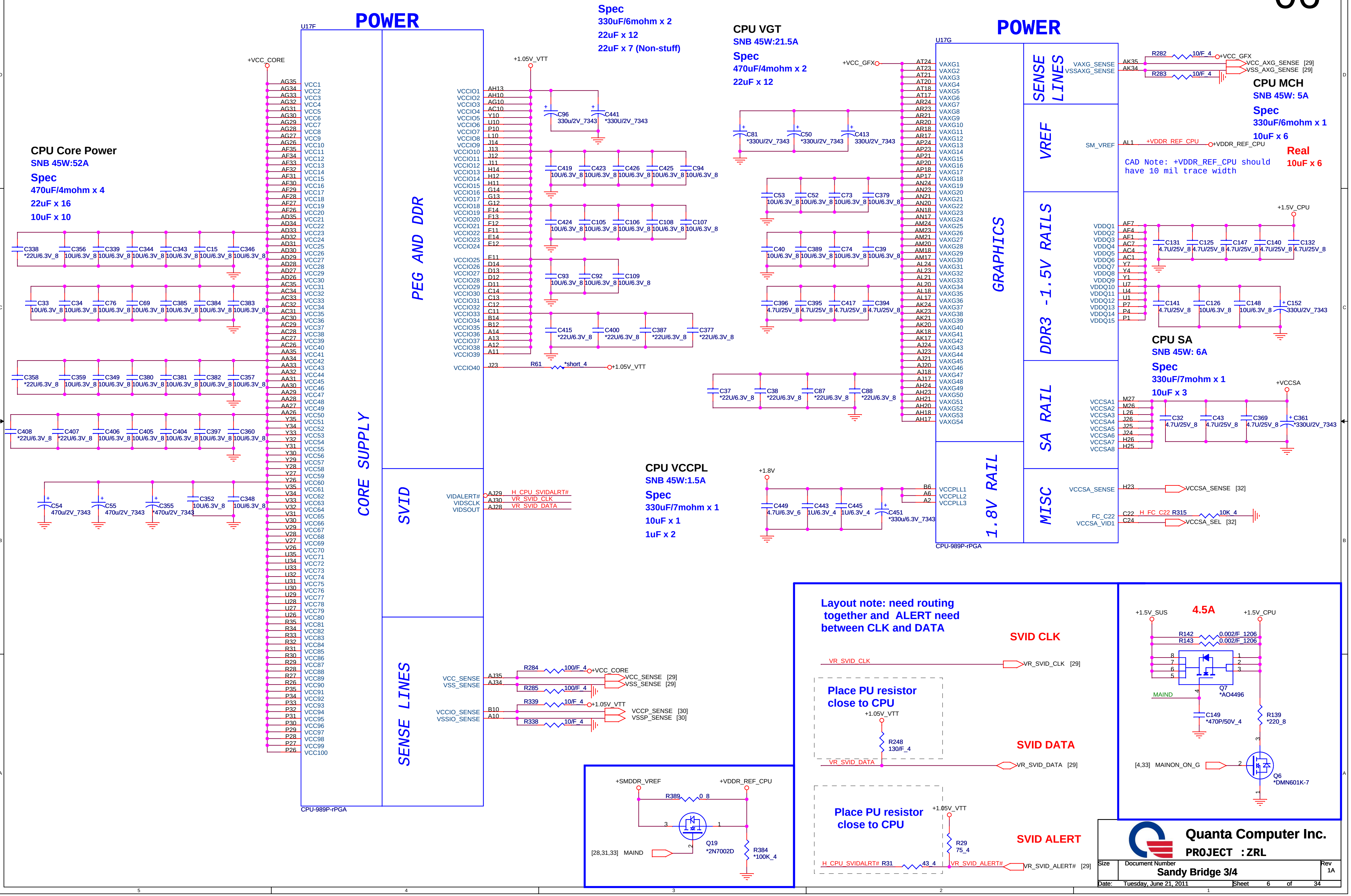
05



Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number: Sandy Bridge 2/4		Rev: 1A
Date: Tuesday, June 21, 2011		Sheet 5 of 34	

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

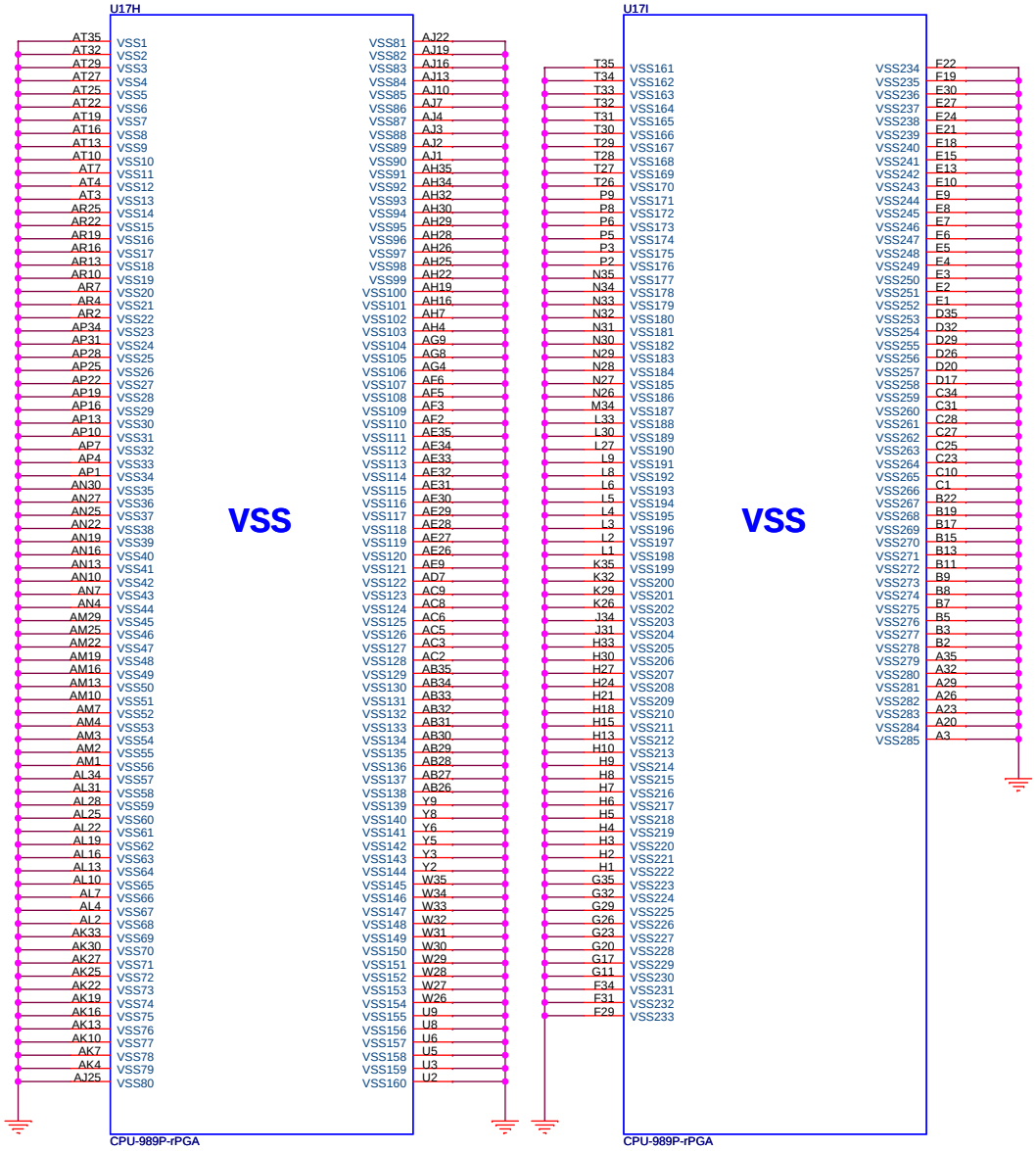

CPU VTT
SNB 45W:8.5A
Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)
U17F
POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
+VCC_CORE
+1.05V_VTT
CPU Core Power
SNB 45W:52A
Spec
470uF/4mohm x 4
22uF x 16
10uF x 10
CPU-989P-rPGA
CPU VGT
SNB 45W:21.5A
Spec
470uF/4mohm x 2
22uF x 12
U17G
POWER
SENSE LINES
VREF
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
+VCC_GFX
VCC_AXG_SENSE [29]
VSS_AXG_SENSE [29]
CPU MCH
SNB 45W: 5A
Spec
330uF/6mohm x 1
10uF x 6
Real
10uF x 6
+VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
+1.5V_CPU
CPU SA
SNB 45W: 6A
Spec
330uF/7mohm x 1
10uF x 3
+VCCSA
VCCSA_SENSE [32]
VCCSA_SEL [32]
CPU VCCPL
SNB 45W:1.5A
Spec
330uF/7mohm x 1
10uF x 1
1uF x 2
+1.8V
H_CPU_SVIDALRT#
VR_SVID_CLK
VR_SVID_DATA
VCC_SENSE [29]
VSS_SENSE [29]
VCCP_SENSE [30]
VSSP_SENSE [30]
+SMDDR_VREF
+VDDR_REF_CPU
[28,31,33] MAIND
Q19
*2N7002D
R384
*100K_4
Layout note: need routing together and ALERT need between CLK and DATA
SVID CLK
VR_SVID_CLK [29]
Place PU resistor close to CPU
+1.05V_VTT
R248
130/F_4
SVID DATA
VR_SVID_DATA [29]
Place PU resistor close to CPU
R29
75_4
SVID ALERT
R31 43_4
VR_SVID_ALERT# [29]
+1.5V_SUS
4.5A
+1.5V_CPU
R142 0.002/F_1206
R143 0.002/F_1206
Q7
*AO4496
MAIND
C149
*470P/50V_4
R139
*220_8
[4,33] MAINON_ON_G
Q6
*DMN601K-7

Quanta Computer Inc.

PROJECT : ZRL

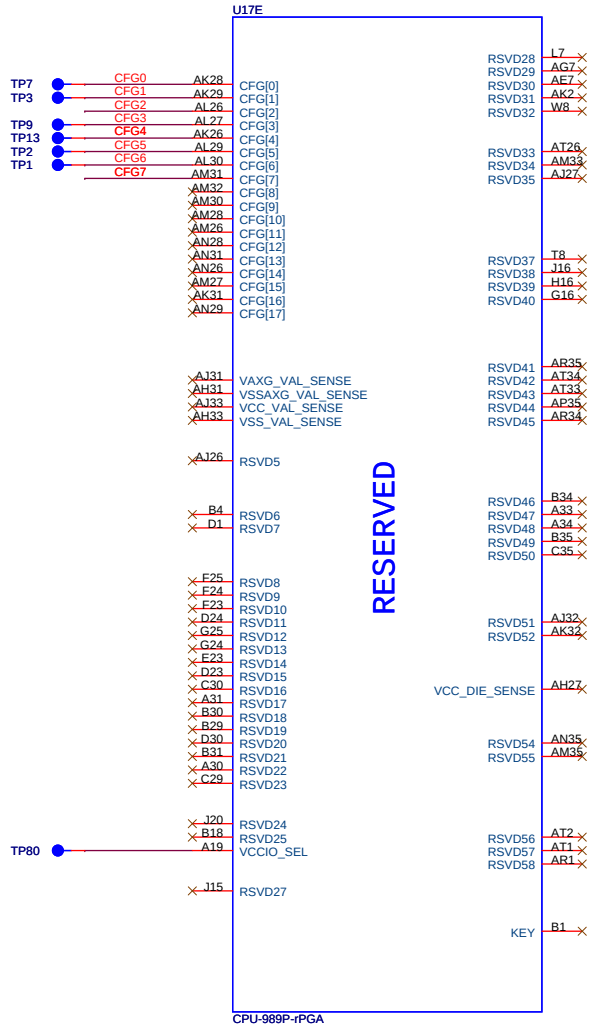
Size	Document Number	Rev
	Sandy Bridge 3/4	1A
Date: Tuesday, June 21, 2011	Sheet 6 of 34	

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

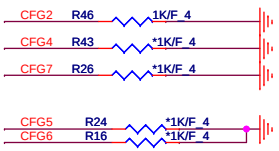
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



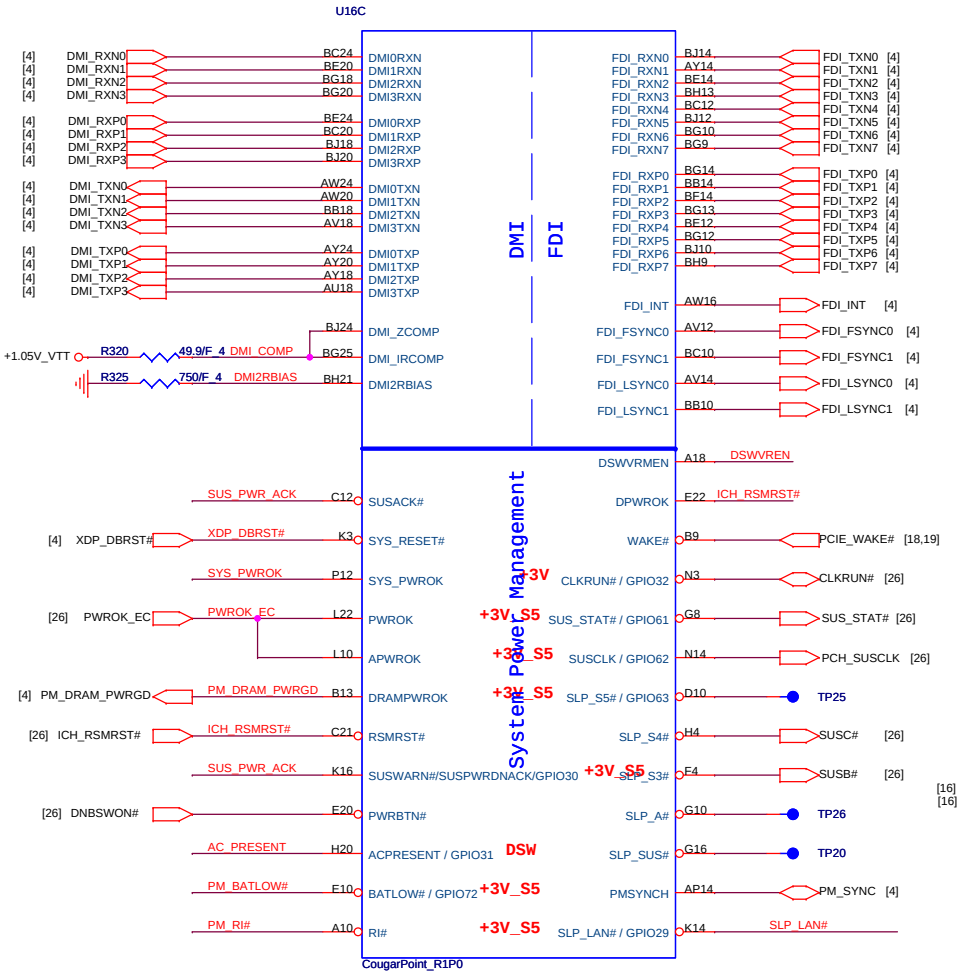
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

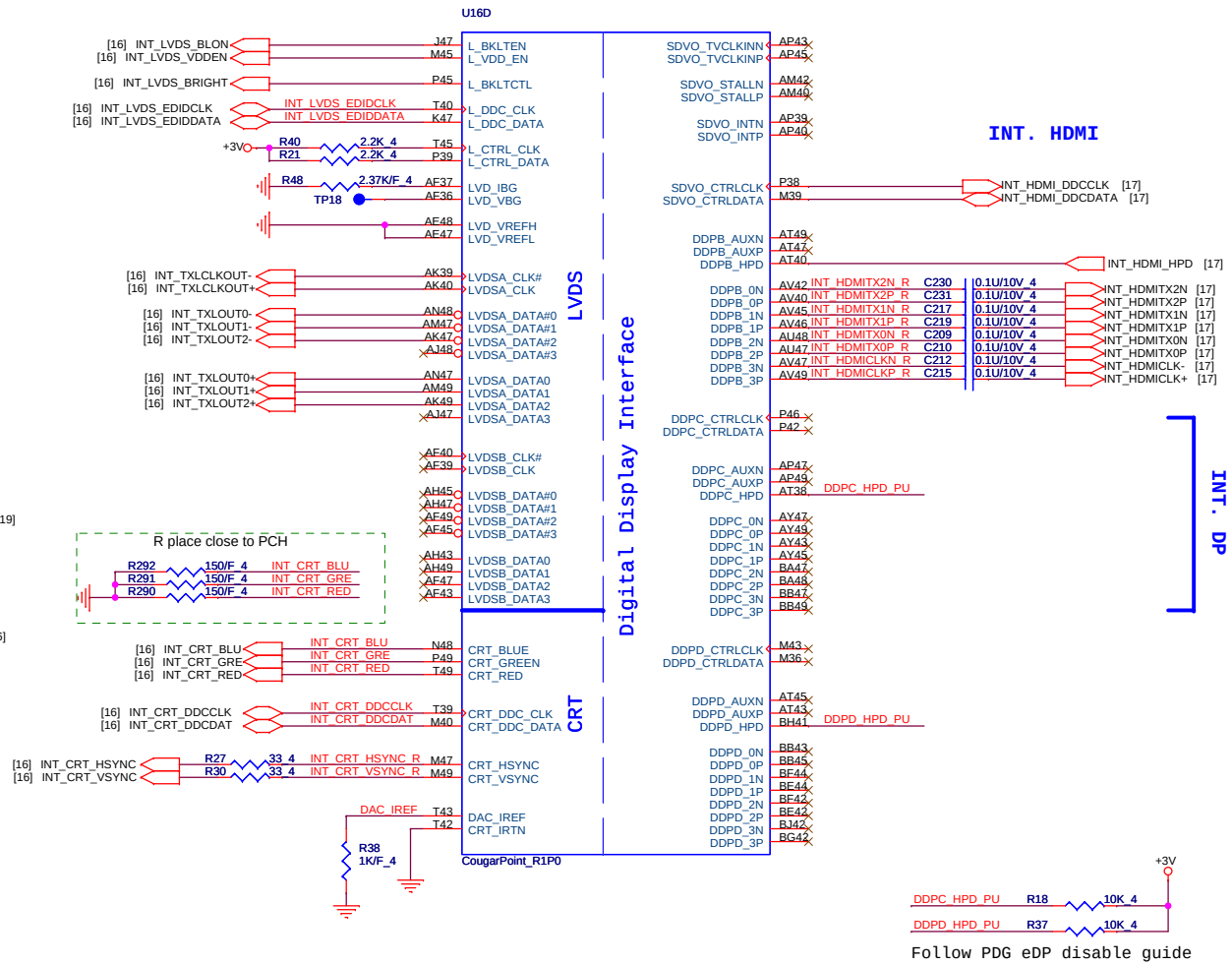
Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date: Tuesday, June 21, 2011	Sheet 7 of 34	

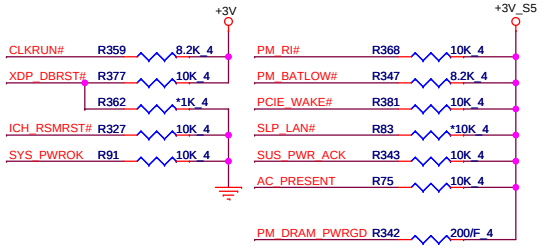
Cougar Point (DMI,FDI,PM)



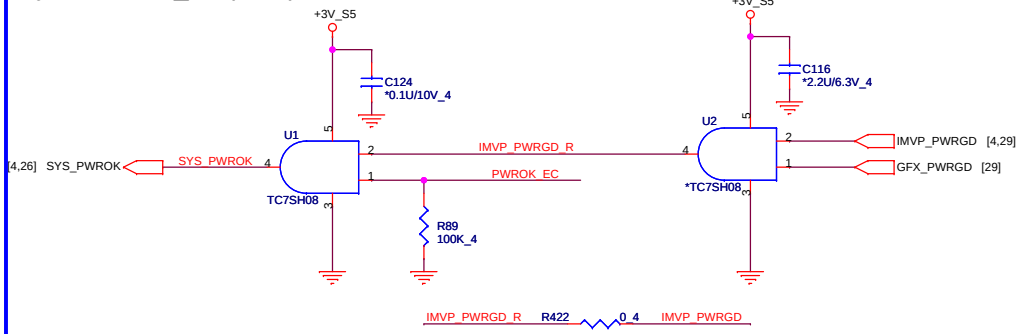
Cougar Point (LVDS,DDI)

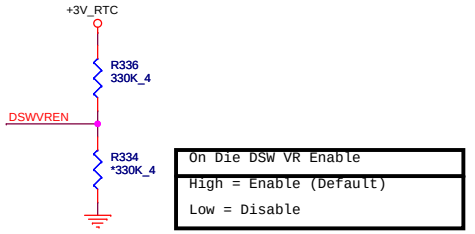


PCH Pull-high/low(CLG)



System PWR_OK(CLG)

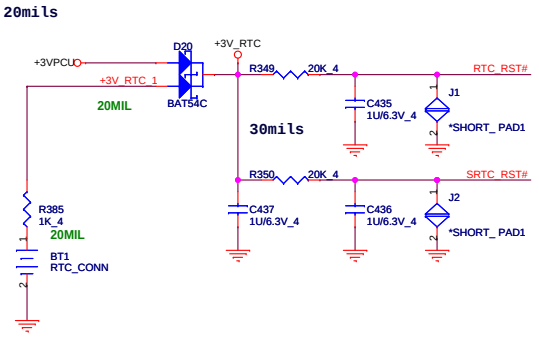




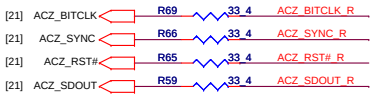
Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	Cougar Point 1/6	1A
Date: Tuesday, June 21, 2011	Sheet 8 of 34	

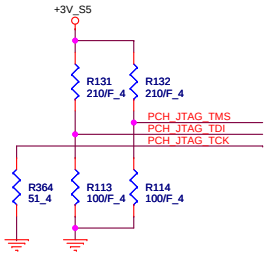
RTC Circuitry(RTC)



HDA Bus(CLG)

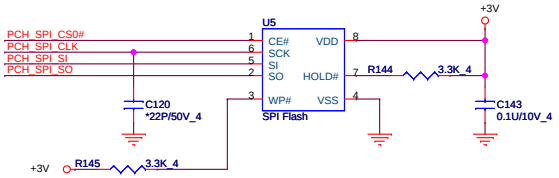


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

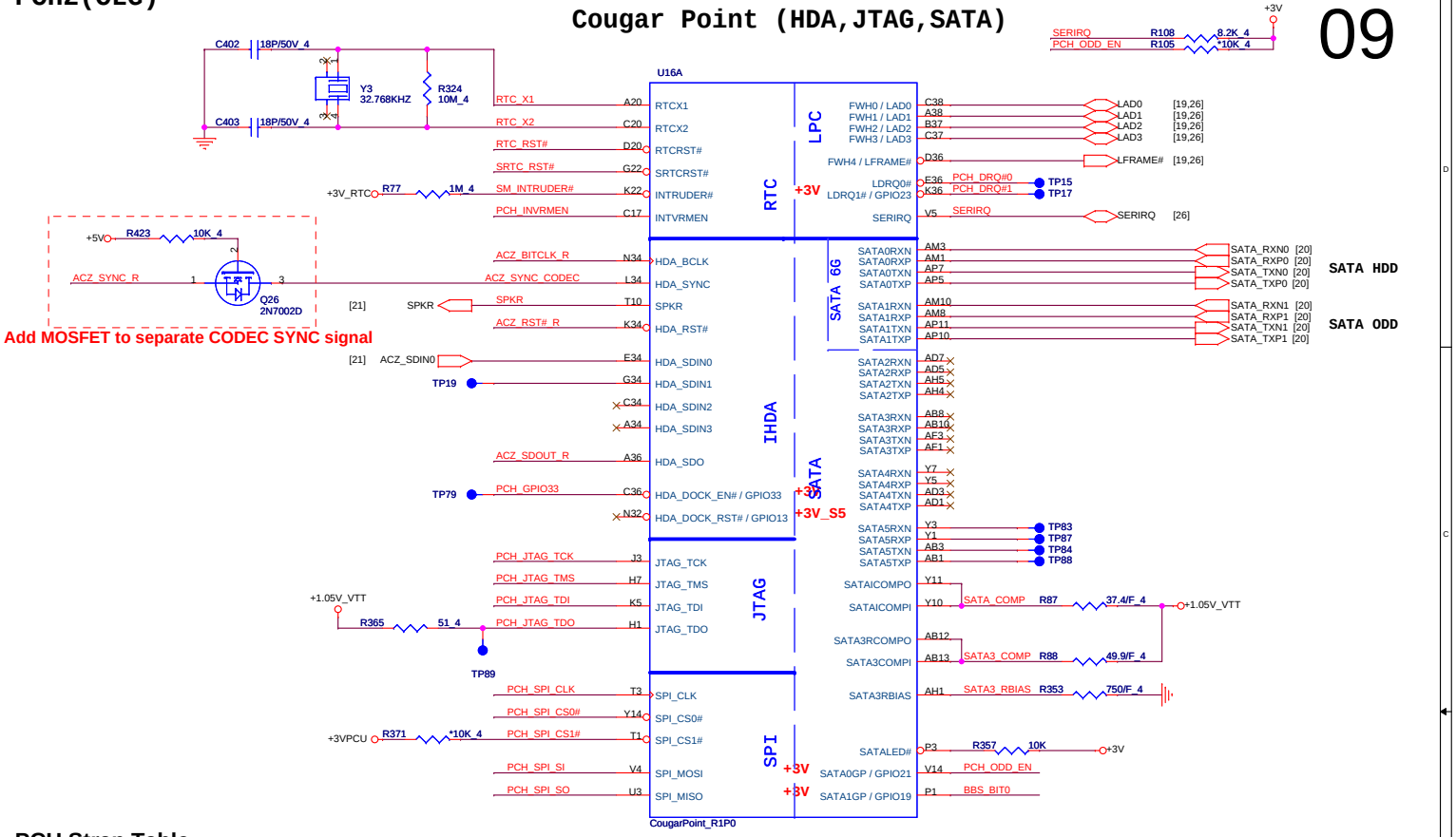
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



PCH2(CLG)

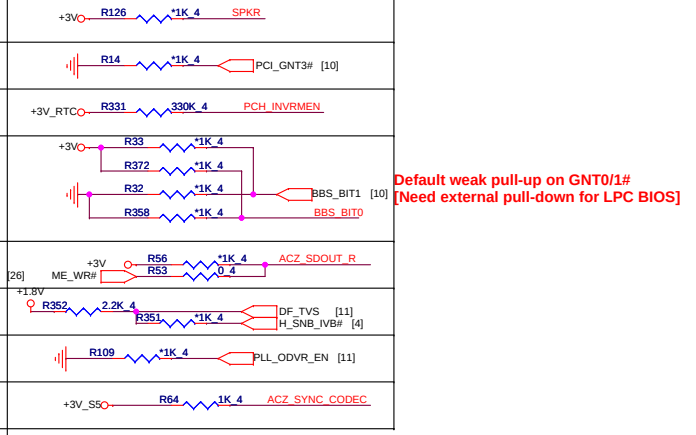
Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



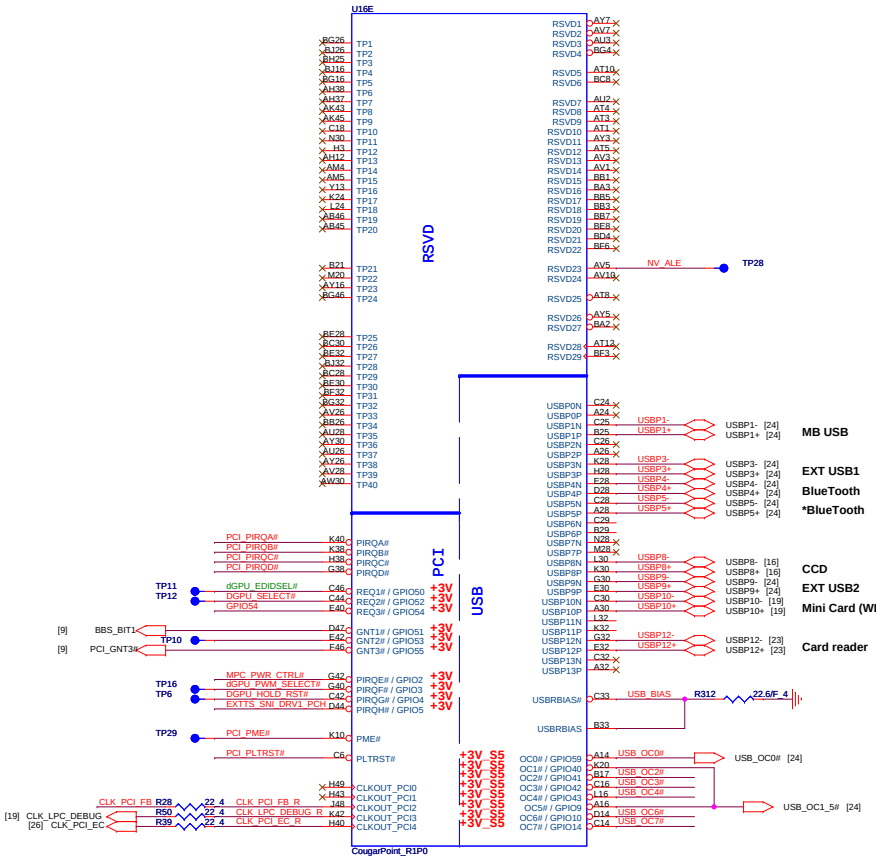
Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Cougar Point 2/6	1A

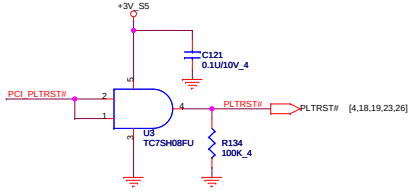
Date: Tuesday, June 21, 2011 Sheet 9 of 34

Cougar Point-M (PCI,USB,NVRAM)

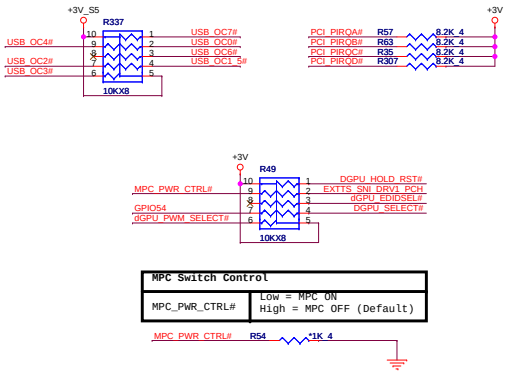


Cougar Point-M (PCI-E,SMBUS,CLK)

PLTRST#(CLG)

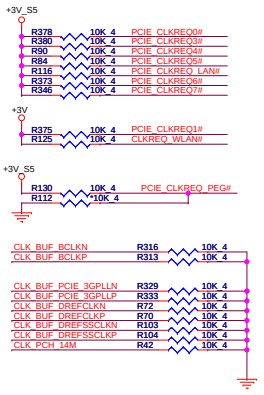


PCI/USBOC# Pull-up(CLG)



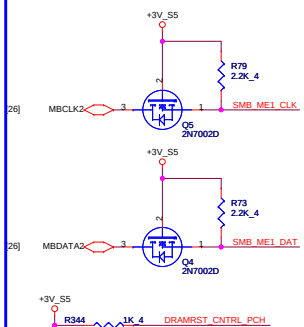
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)

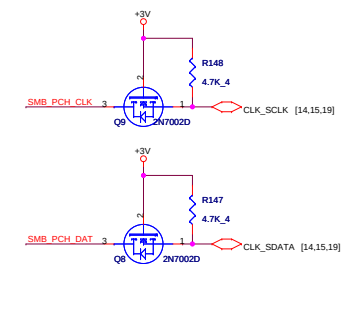


CLOCK TERMINATION for FCIM

SMBus/Pull-up(CLG)



SMBus(PCH)



Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	Cougar Point 3/6	1A
Date: Tuesday, June 21, 2011	Sheet 10 of 34	

Cougar Point (GPIO,VSS_NCTF,RSVD)

U16F

GPIO

S_GPIO	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40	dGPU_PWR_CTRL#
[26] EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41	R298 1.5K/F_4
BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41	R302 1.5K/F_4 +3V
[26] EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40	R303 1.5K/F_4
TP86	C10	GPIO8	+3V_S5				
SMIB#	C4	LAN_PHY_PWR_CTRL / GPIO12		+3V_S5			
PCH_GPIO15	G2	GPIO15	+3V_S5				
check VR_ON GPIO SKU_ID0	U2	SATA4GP / GPIO16	+3V				
TP4 dGPU_PWROK	D40	TACH0 / GPIO17	+3V				
BIOS_REC	T5	SCLOCK / GPIO22	+3V				
CR_WAKER#	E8	GPIO24 / MEM_LED	+3V_S5				
GPIO27	E16	GPIO27	DSW				
[9] PLL_ODVR_EN	P8	GPIO28	+3V_S5				
Need Check STP_PCI#	K1	STP_PCI# / GPIO34	+3V				
TP27 dGPU_VRON	K4	GPIO35	+3V				
TP30 DMI_OVRVLTG	V8	SATA2GP / GPIO36	+3V				
FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V				
MFG_MODE	N2	SLOAD / GPIO38	+3V				
BOARD_ID0	M3	SDATAOUT0 / GPIO39	+3V				
TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V				
[10,25] SML1ALERT# R354 *short_4 CRIT_TEMP_REP#	V3	SATA5GP / GPIO49	+3V				
BOARD_ID2	D6	GPIO57	+3V_S5				

CPU/MISC

A20GATE	P4	EC_A20GATE	EC_A20GATE [26]
PECI	AU16	R102 *0_4	EC_PECI [4,26]
RCIN#	P5	EC_RCIN#	EC_RCIN# [26]
PROCPWRGD	AY11	TP23	H_PWRGOOD [4]
THRMTRIP#	AY10	PCH_THRMTRIP# R101 390_4	PM_THRMTRIP# [4]
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS [9]
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

GPIO27:
Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

R353??

	dGPU_PWR_CTRL# (GPIO68)	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R124 10K_4 +3V
R107 *0_4

PCH_GPIO15 R379 1K_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO

S_GPIO R111 1K/F_4 +3V
R95 *100_4

MFG-TEST

MFG_MODE R374 10K_4 +3V
R360 *0_4

GPIO Pull-up/Pull-down(CLG)

+3V_S5
CR_WAKER# R348 10K/F_4
SMIB# R366 10K_4
PLL_ODVR_EN R127 *10K_4

+3V
EC_EXT_SMI# R299 10K_4
EC_EXT_SCI# R34 10K_4
STP_PCI# R363 *10K_4
EC_A20GATE R96 10K_4
EC_RCIN# R93 10K_4
CRIT_TEMP_REP# R355 10K_4
dGPU_PWROK R36 *10K_4
GPIO27 R80 *10K_4

+3V
R297 10K_4 dGPU_PWR_CTRL#
R305 *100K_4

+3V
R15 *10K_4 SKU_ID1 [10]
R22 10K_4

+3V
R370 *10K_4 SKU_ID0
R356 10K_4

+3V
R361 *10K_4 BOARD_ID0 R376 10K_4
R300 10K_4 BOARD_ID1 R301 *10K_4
R115 10K_4 BOARD_ID2 R133 *10K_4

FDI_OVRVLTG R129 *10K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R94 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

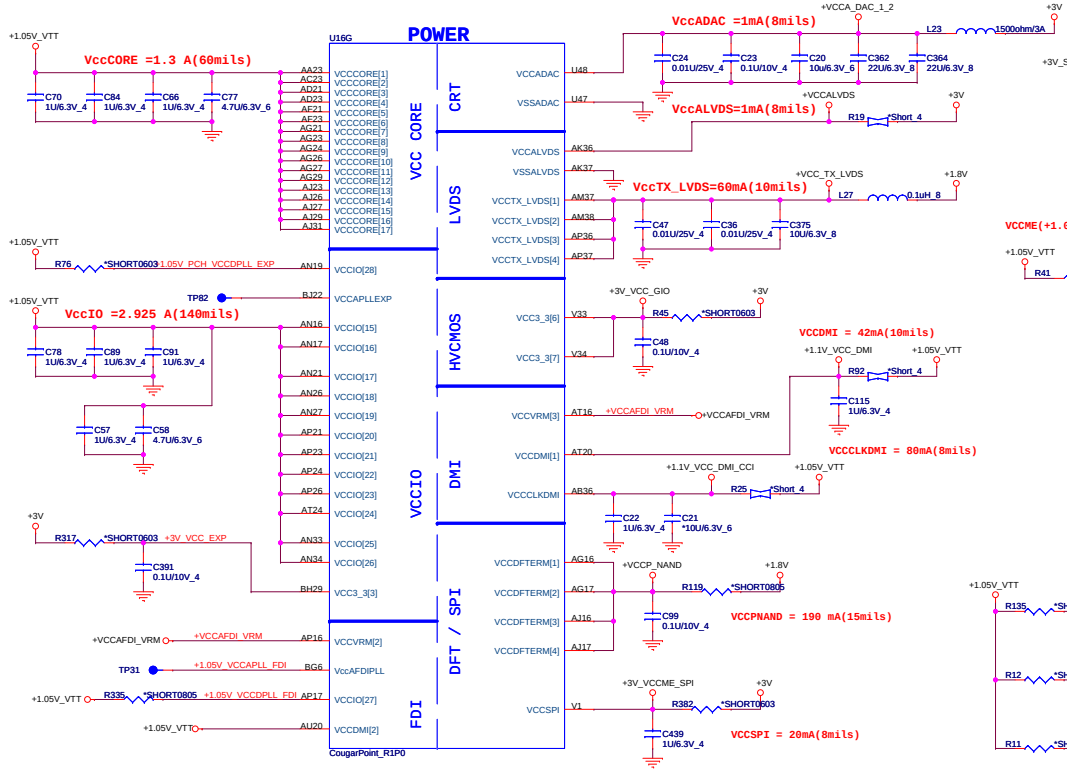
BIOS_REC R128 10K_4 +3V
R110 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

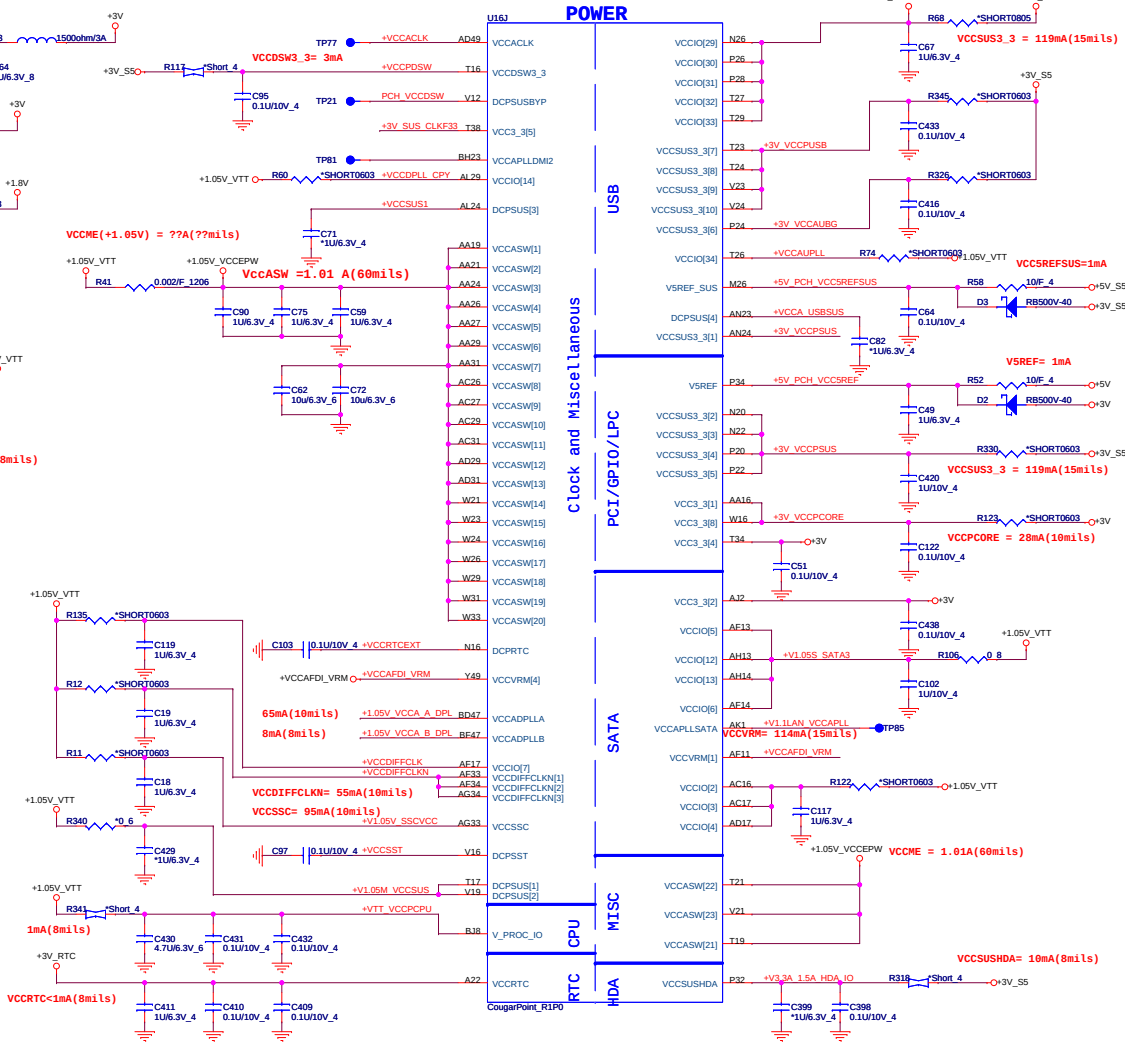
Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	Cougar Point 4/6	1A
Date: Tuesday, June 21, 2011	Sheet 11 of 34	

COUGAR POINT (POWER)

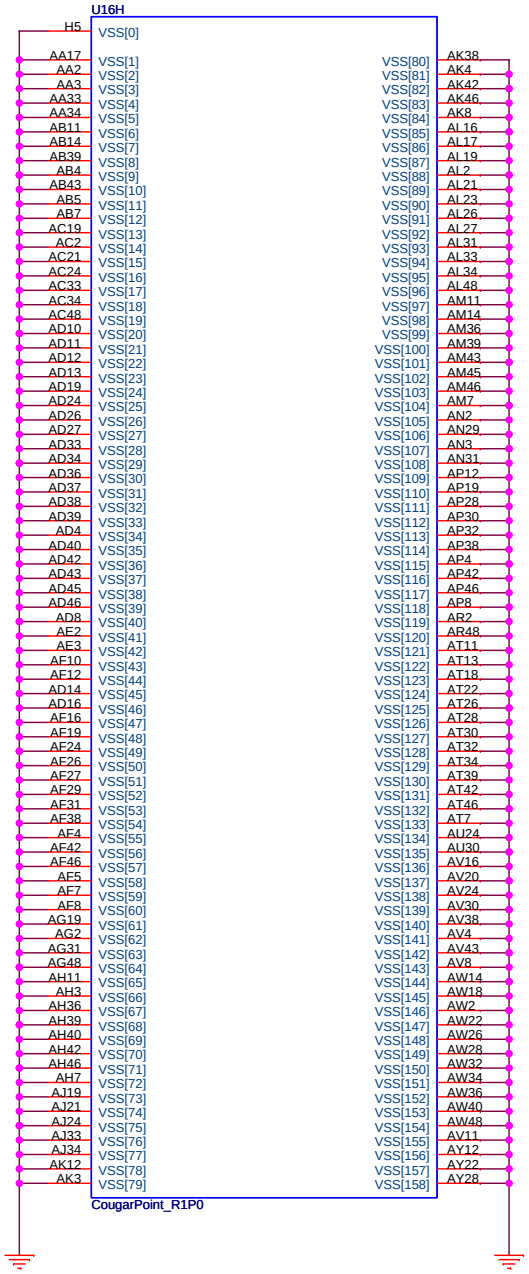


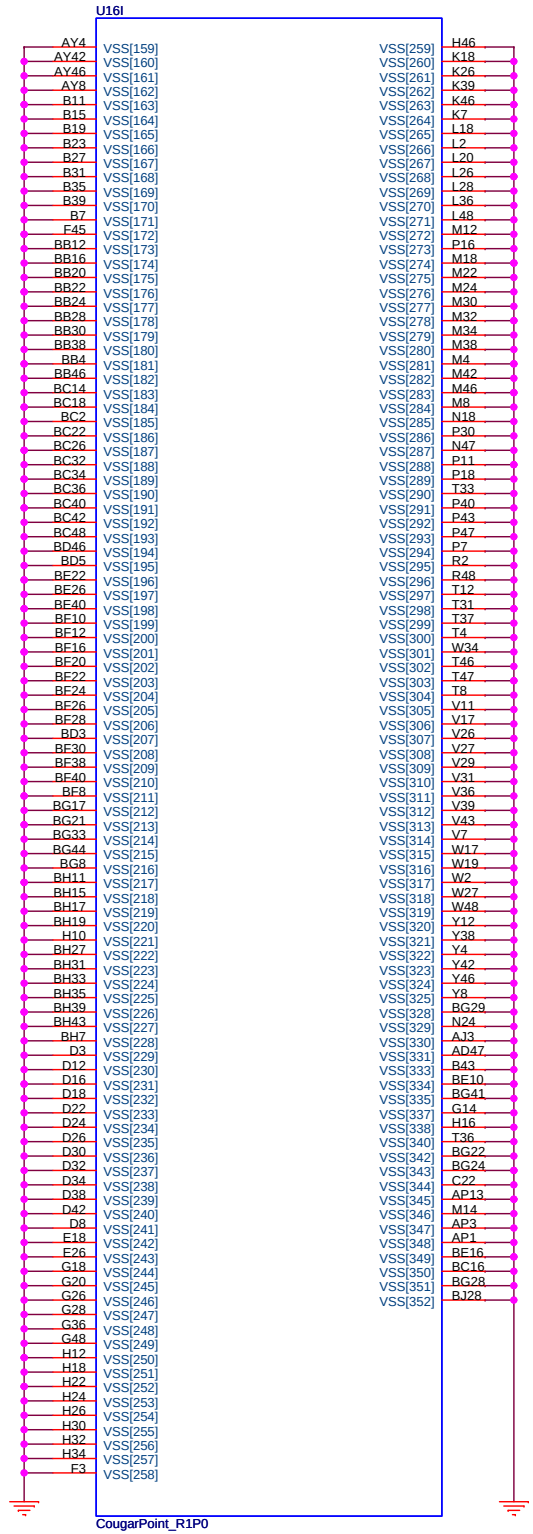
Cougar Point-M (POWER)



PCH6(CLG)

IBEX PEAK-M (GND)





Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Cougar Point 6/6	1A
Date: Tuesday, June 21, 2011	Sheet 13 of 34	

DDR RVS 4H

[5] M_A_A[15:0]

JDIM2A

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

[5] M_A_BS#0 109 BA0
[5] M_A_BS#1 108 BA1
[5] M_A_BS#2 79 BA2
[5] M_A_CS#0 114 S0#
[5] M_A_CS#1 121 S1#
[5] M_A_CLKP0 101 CK0
[5] M_A_CLKN0 103 CK0#
[5] M_A_CLKP1 102 CK1
[5] M_A_CLKN1 104 CK1#
[5] M_A_CKE0 73 CKE0
[5] M_A_CKE1 74 CKE1
[5] M_A_CAS# 115 CAS#
[5] M_A_RAS# 110 RAS#
[5] M_A_WE# 113 WE#

R183 10K_4
R182 10K_4
DIMM0_SA0 197 SA0
DIMM0_SA1 201 SA1
[10,15,19] CLK_SCLK 202 SCL
[10,15,19] CLK_SDATA 200 SDA

[5] M_A_ODT0 116 ODT0
[5] M_A_ODT1 120 ODT1

02/23 Remove 0ohm to GND

11 DM0
28 DM1
46 DM2
63 DM3
136 DM4
153 DM5
170 DM6
187 DM7

[5] M_A_DQSP[7:0]

M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

[5] M_A_DQSN[7:0]

M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

DQ0 5 M_A_DQ5
DQ1 7 M_A_DQ4
DQ2 15 M_A_DQ6
DQ3 17 M_A_DQ7
DQ4 4 M_A_DQ0
DQ5 6 M_A_DQ1
DQ6 16 M_A_DQ2
DQ7 18 M_A_DQ3
DQ8 21 M_A_DQ12
DQ9 23 M_A_DQ13
DQ10 33 M_A_DQ14
DQ11 35 M_A_DQ15
DQ12 22 M_A_DQ8
DQ13 24 M_A_DQ9
DQ14 34 M_A_DQ10
DQ15 36 M_A_DQ11
DQ16 39 M_A_DQ20
DQ17 41 M_A_DQ21
DQ18 51 M_A_DQ23
DQ19 53 M_A_DQ22
DQ20 40 M_A_DQ17
DQ21 42 M_A_DQ16
DQ22 50 M_A_DQ19
DQ23 52 M_A_DQ18
DQ24 57 M_A_DQ25
DQ25 59 M_A_DQ24
DQ26 67 M_A_DQ27
DQ27 69 M_A_DQ31
DQ28 56 M_A_DQ28
DQ29 58 M_A_DQ29
DQ30 68 M_A_DQ26
DQ31 70 M_A_DQ30
DQ32 129 M_A_DQ33
DQ33 131 M_A_DQ37
DQ34 141 M_A_DQ34
DQ35 143 M_A_DQ38
DQ36 130 M_A_DQ32
DQ37 132 M_A_DQ36
DQ38 140 M_A_DQ39
DQ39 142 M_A_DQ35
DQ40 147 M_A_DQ44
DQ41 149 M_A_DQ40
DQ42 157 M_A_DQ43
DQ43 159 M_A_DQ42
DQ44 146 M_A_DQ45
DQ45 148 M_A_DQ41
DQ46 158 M_A_DQ46
DQ47 160 M_A_DQ47
DQ48 163 M_A_DQ53
DQ49 165 M_A_DQ52
DQ50 175 M_A_DQ54
DQ51 177 M_A_DQ55
DQ52 164 M_A_DQ48
DQ53 166 M_A_DQ49
DQ54 174 M_A_DQ51
DQ55 176 M_A_DQ50
DQ56 181 M_A_DQ61
DQ57 183 M_A_DQ60
DQ58 191 M_A_DQ62
DQ59 193 M_A_DQ63
DQ60 180 M_A_DQ56
DQ61 182 M_A_DQ57
DQ62 192 M_A_DQ59
DQ63 194 M_A_DQ58

DDR3-DIMM0_H=4_RVS_LTS

M_A_DQ[63:0] [5]

+1.5V_SUS

2.48A

JDIM2B

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V VDDSPD 199

NC1 77
NC2 122
NCTEST 125

+3V R173 10K_4
[5,15] DDR3_DRAMRST# DDR3_DRAMRST# EVENT# 198 RESET# 30

SMDDR_VREF_DQ0_M1 SMDDR_VREF_DQ0_M1
+SMDDR_VREF_DIMM VREF_DQ 1 VREF_CA 126

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +0.75V_DDR_VTT
VTT2 204

GND 205
GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_RVS_LTS

CAD Note: All VREF traces should have 10 mil trace width

DDR3_DRAMRST#
C197
0.1u/10V_4

VREF DQ0 M1 Solution

+1.5V_SUS
R178 1K/F_4
SMDDR_VREF_DQ0_M1
R177 1K/F_4

+1.5V_SUS
R176 10K/F_4
+SMDDR_VREF_DIMM
R175 10K/F_4
C221 470P/50V_4

Place these Caps near So-Dimm0.

+1.5V_SUS

C164 4.7U/6.3V_6
C222 4.7U/6.3V_6
C223 4.7U/6.3V_6
C169 4.7U/6.3V_6
C173 4.7U/6.3V_6
C184 4.7U/6.3V_6
C214 *10U/6.3V_6
C218 1U/10V_4
C224 1U/10V_4
C202 1U/10V_4
C163 1U/10V_4
C241 *330U/2V_7343
C165 4.7U/25V_8
C228 4.7U/25V_8

+3V
C211 2.2U/6.3V_6
C213 0.1u/10V_4

+0.75V_DDR_VTT
C204 1U/6.3V_4
C200 1U/6.3V_4
C196 1u/6.3V_4
C194 1U/6.3V_4
C208 4.7U/6.3V_6
C205 *10U/6.3V_6

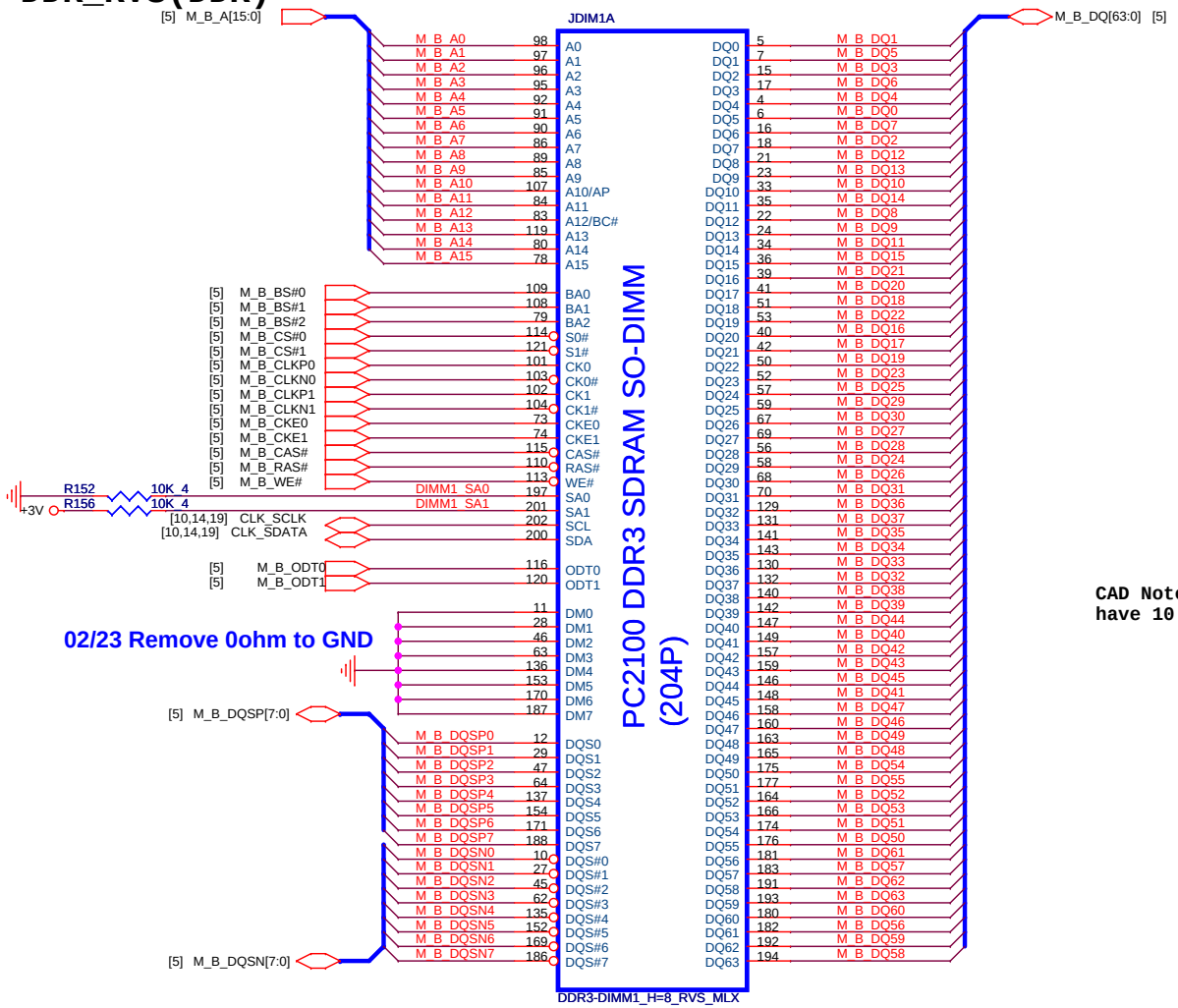
+SMDDR_VREF_DIMM
C220 0.1u/10V_4
C225 2.2U/6.3V_6

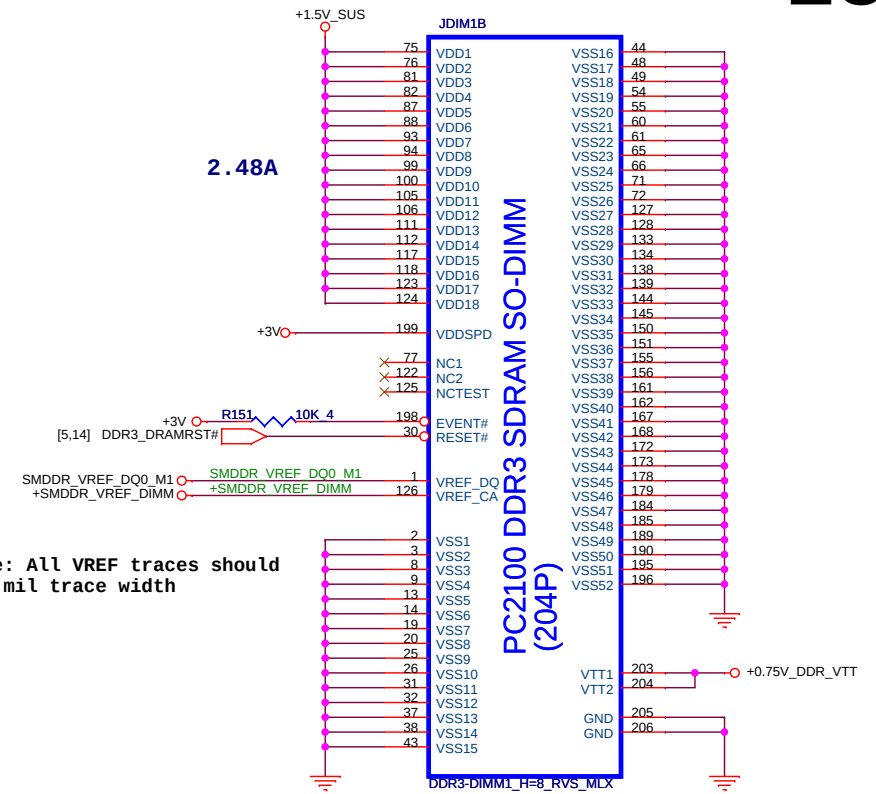
SMDDR_VREF_DQ0_M1
C226 0.1u/10V_4
C227 2.2U/6.3V_6

Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Tuesday, June 21, 2011	Sheet 14 of 34	

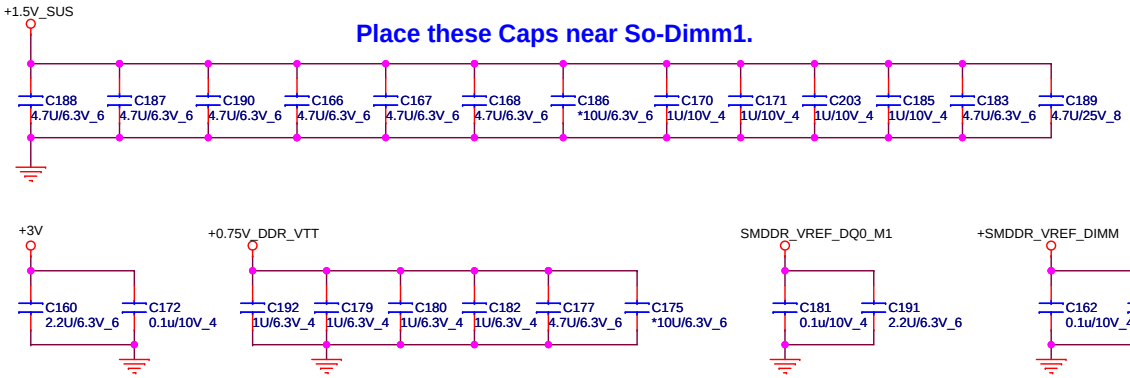
DDR_RVS(DDR)





CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm1.



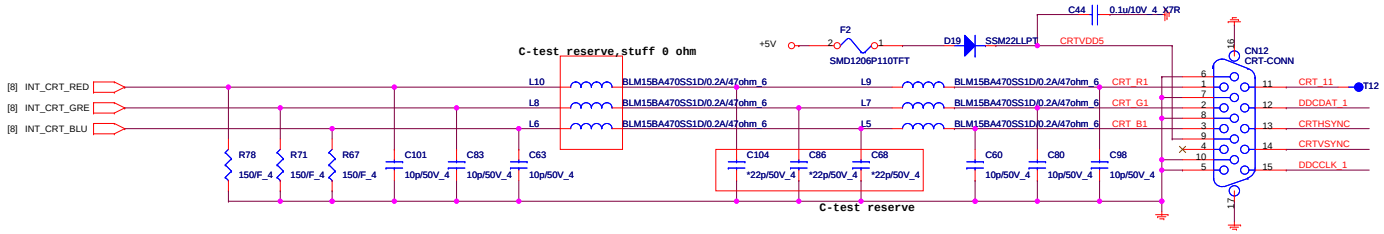
Quanta Computer Inc.

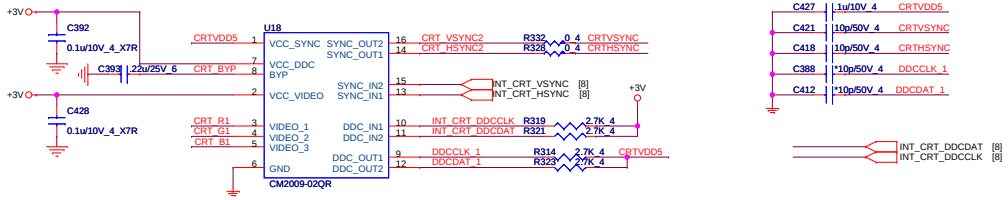
PROJECT : ZRL

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

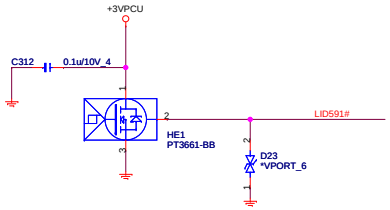
Date: Tuesday, June 21, 2011 Sheet 15 of 34

CRT

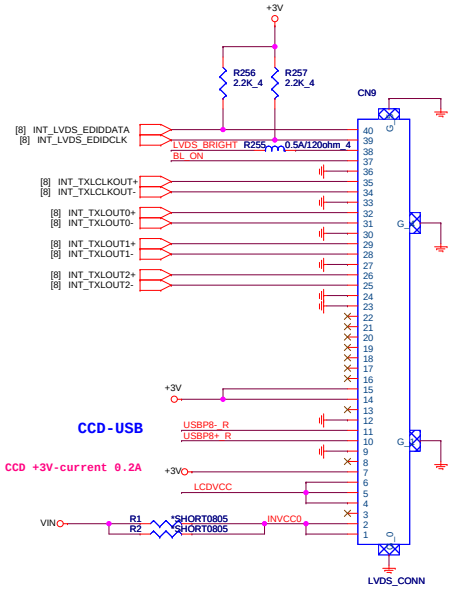


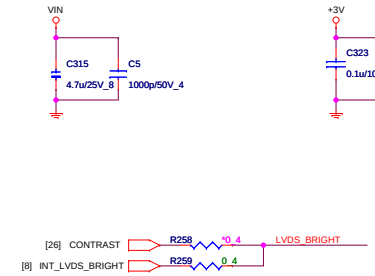


Lid Switch (Hall sensor)

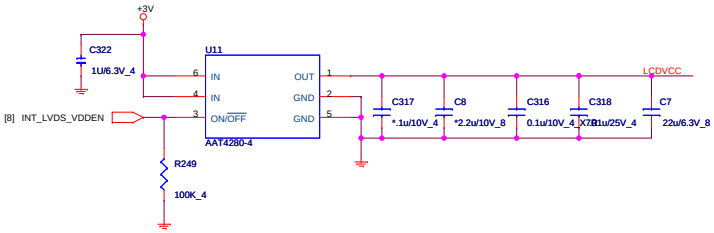


LVDS

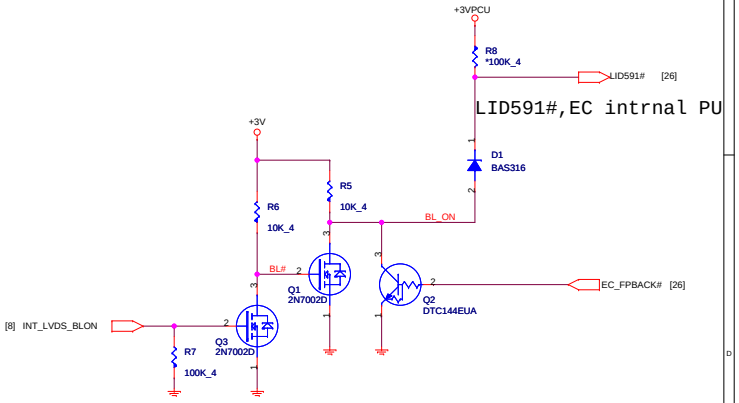




LCD Power

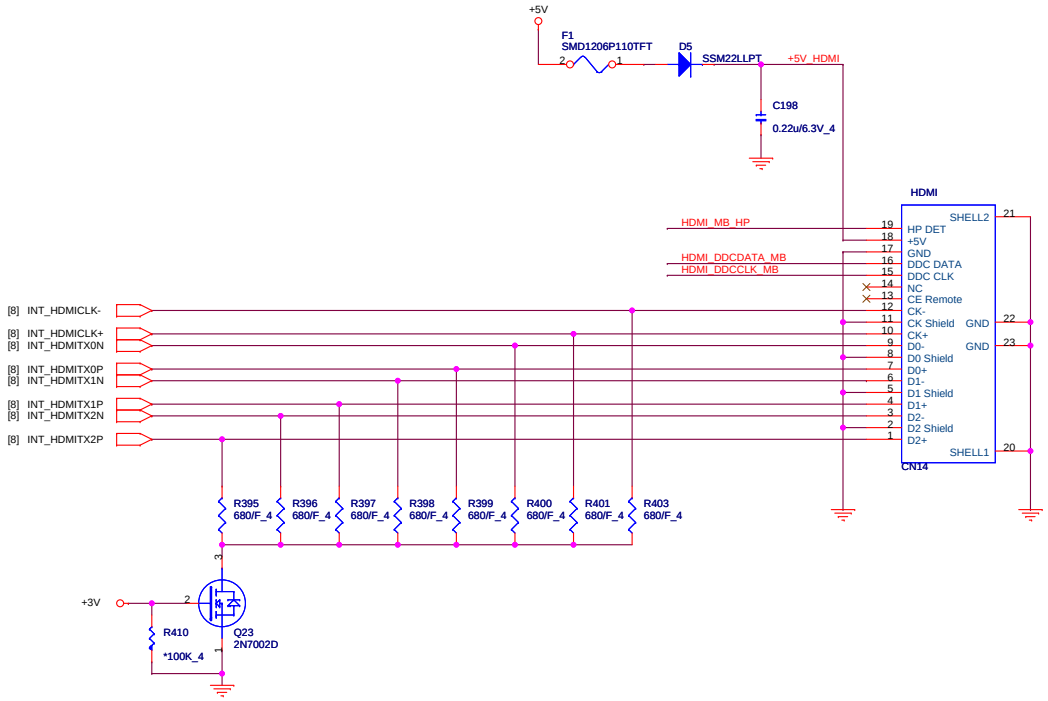


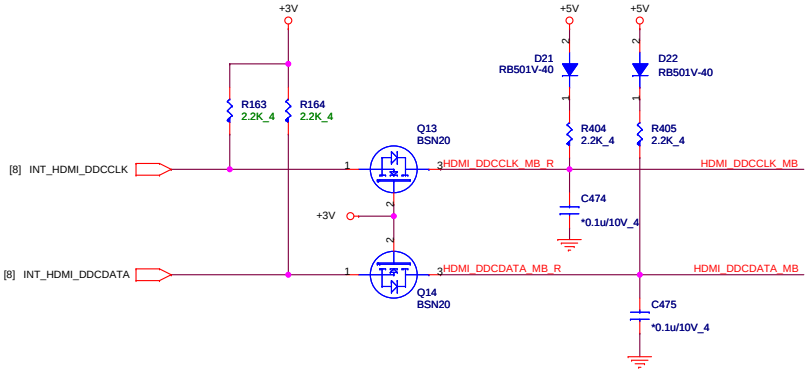
Backlight Control



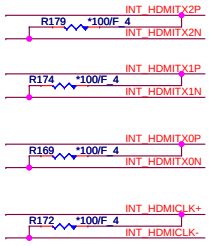
Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number	CRT/LVDS/CAMERA/LID	Rev 1A
Date: Tuesday, June 21, 2011		Sheet 16 of 34	

HDMI

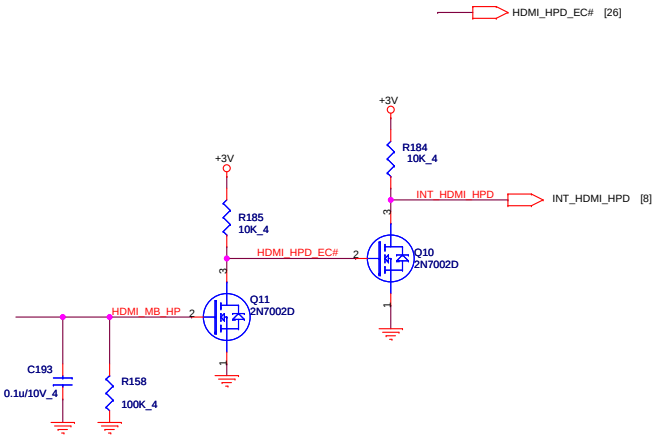




EMI



HDMI-detect



Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number	Rev
	HDMI (PS8101)	1A
Date: Tuesday, June 21, 2011	Sheet 17 of 34	

LAN

<BOM note>
If center tap power come from internal switch regulator=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO=>Stuff 52LDO@

76.1mA ; 30mil <Layout note> Close to Pin2

Power Sequence:
VDD33 to PERSTn >= 100ms

U4 — AR8158 4X4mm 32Pin QFN — AR8158-BL1A-RL

1	LX	17	CLKREQn
2	VDD33	18	SMCLK
3	PERSTn	19	SMDATA
4	WAKEn	20	TESTMODE
5	VDDCT_REG	21	NC
6	VDDCT	22	TX_N
7	AVDDL_REG	23	TX_P
8	XTLO	24	AVDDL
9	XTLI	25	REFCLK_N
10	AVDDH_REG	26	REFCLK_P
11	RBIAS	27	AVDDL
12	TRXP0	28	RX_P
13	TRXN0	29	RX_N
14	TRXP1	30	DVDDL_REG
15	TRXN1	31	LED[0]
16	LED[2]	32	LED[1]
		33	GND1
		34–42	GND2–GND10

PU in CLK Gen.

<Layout note> Close to LAN Chip 1nF reserved for EMI

+3V_S5	2	+1.1V regulator output (For all the analog 1.1V supply pins)
+1.1V analog power	24/27	+2.7V regulator output
		+1.1V regulator output (For all the digital 1.1V supply pins)
		+1.8V regulator output (For VDDCT when LDO mode)
+1.7V analog power	6	+1.7V Switching regulator (For VDDCT when switching mode)
	1	+1.7V Switching regulator (For VDDCT when switching mode)

ATHEROS AR8158

TRANSFORMER

U21 — NS0014 LF_Bothhand 10/100 type

L11 CX8EG601000: 0.5A/600ohm_6

main CY640P31Z08
2'nd CY003100Z06

1nF reserved for EMI

RJ45 Connector

CN13 — RJ45

Active LED Pin:
Non-overclocking=>active high

LINK LED Pin:
SWR mode=>active low
LDO mode=>active high

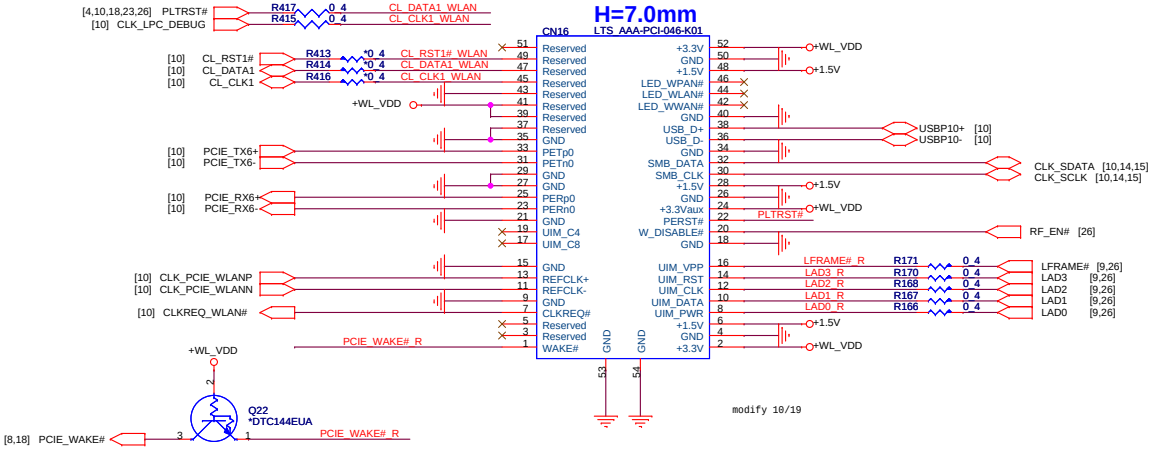
Quanta Computer Inc.	
PROJECT : ZRL	
Size	Document Number: LAN AR8158L
Rev	1A
Date:	Tuesday, June 21, 2011
Sheet	18 of 34

MINI-CARD WLAN

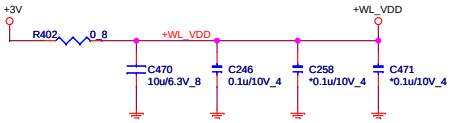
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

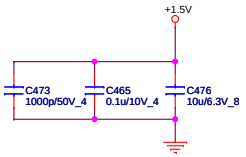
Debug

H=7.0mm

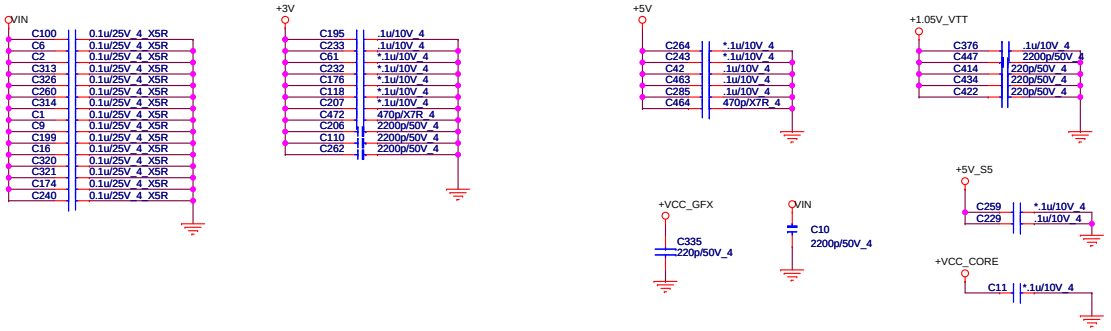


Debug



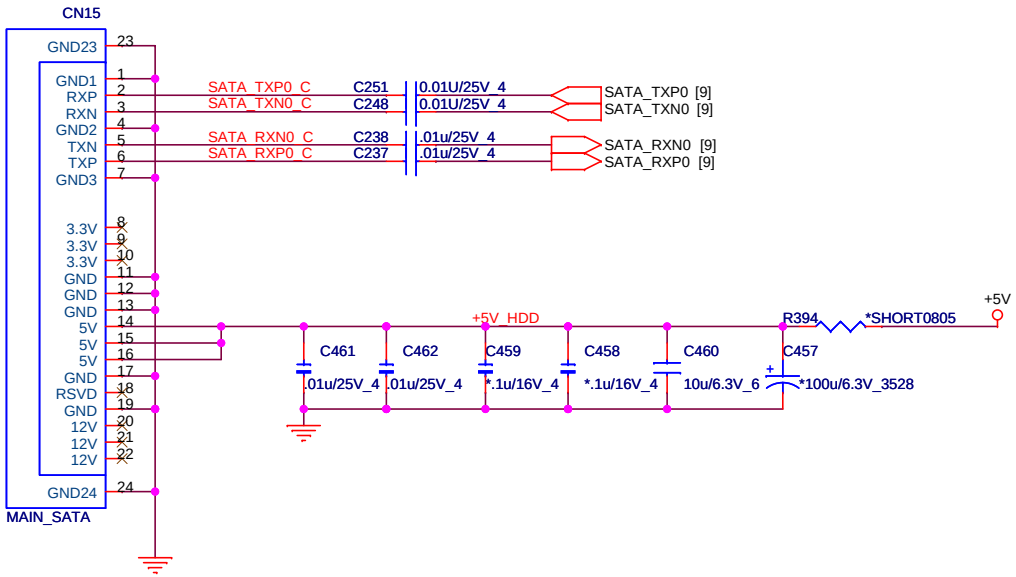


EE RETURN-PATH CAPACITORS

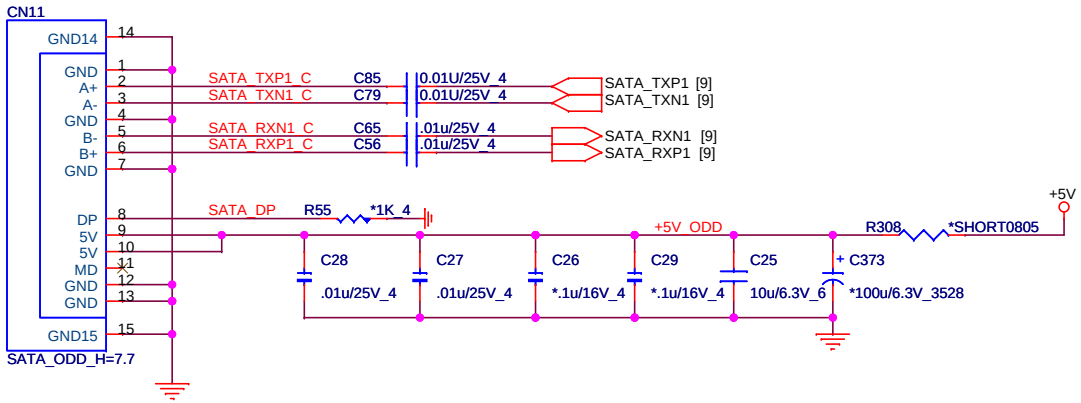


Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Tuesday, June 21, 2011	Sheet 19 of 34	

MAIN SATA HDD



ODD (SATA)

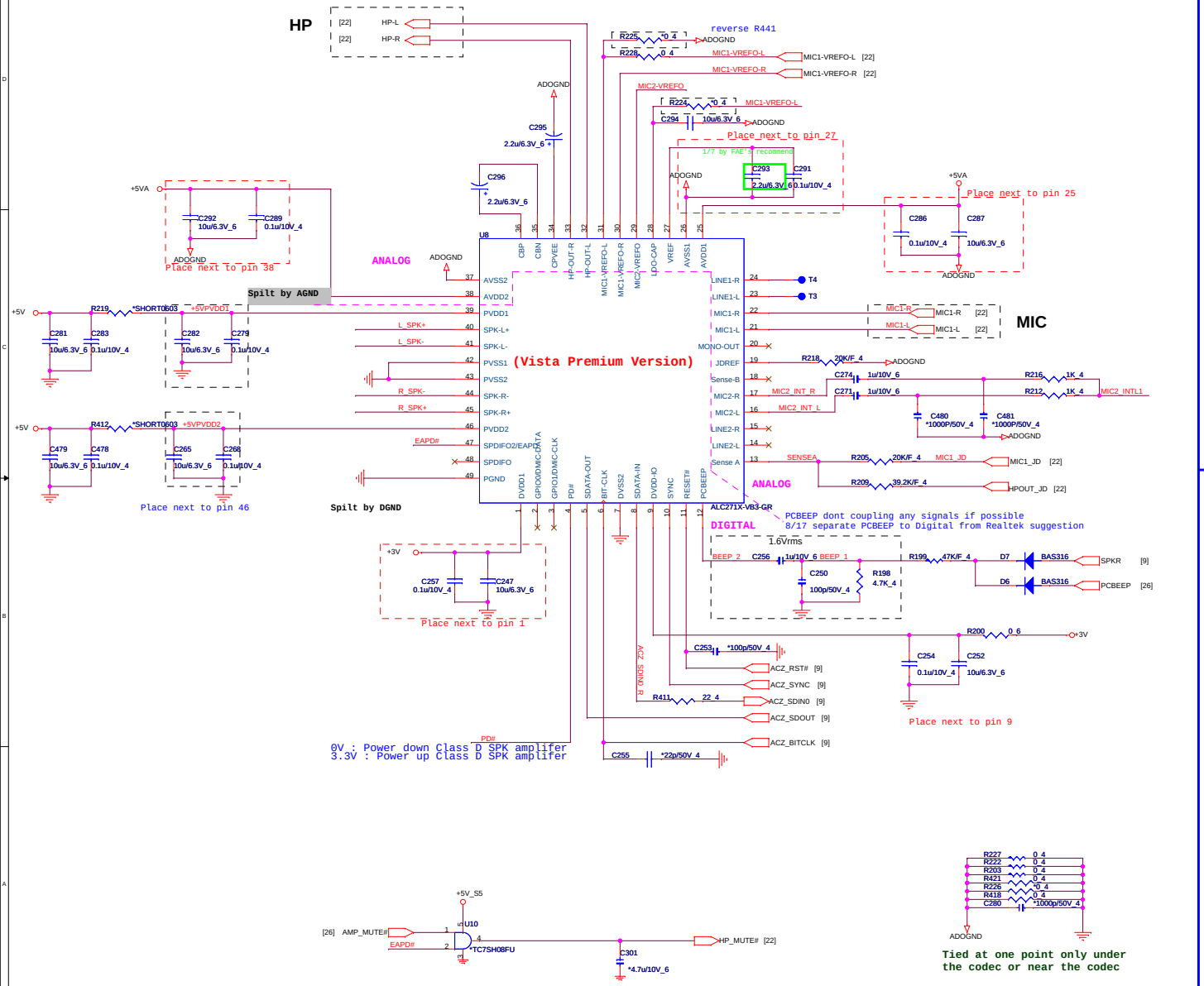


Quanta Computer Inc.

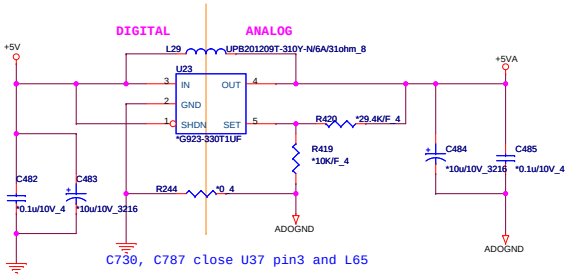
PROJECT : ZRL

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date: Tuesday, June 21, 2011	Sheet 20 of 34	

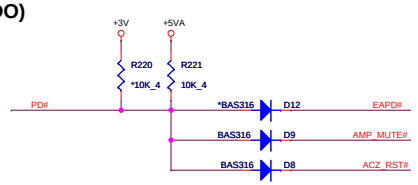
Codec



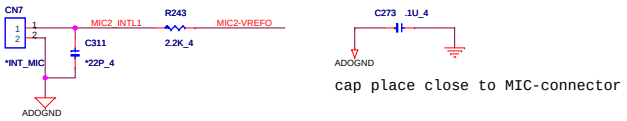
Power



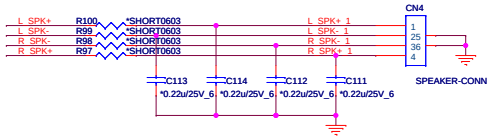
Mute(ADO)



Internal MIC

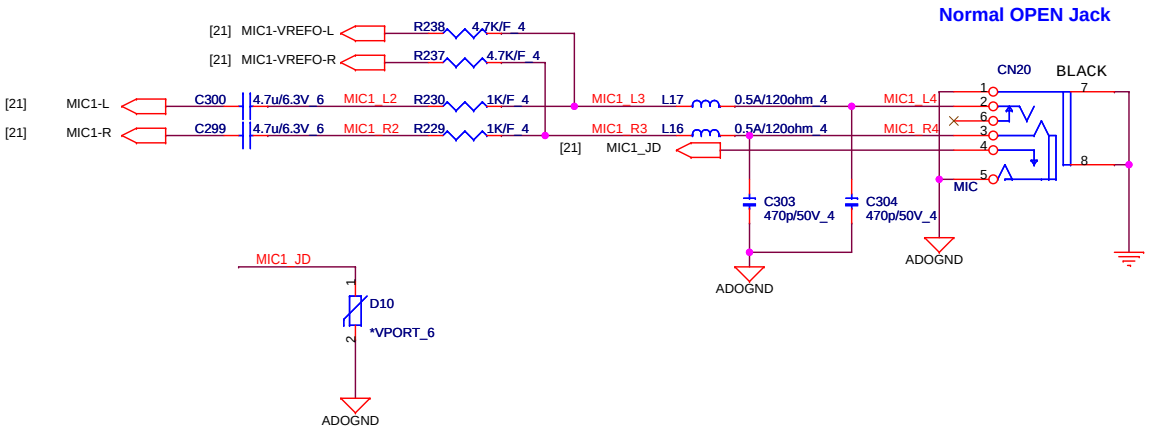


Internal Speaker

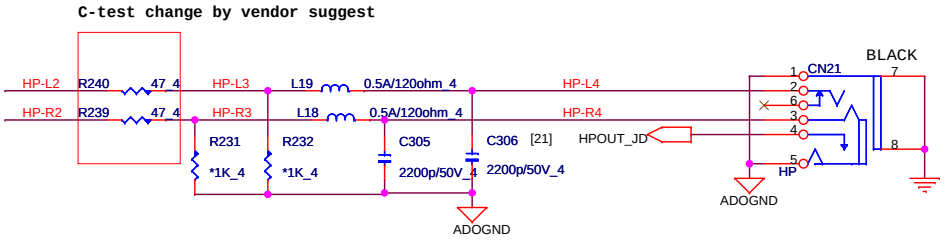


Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number: REALTEK ALC271X	Rev: 1A
Date: Tuesday, June 21, 2011	Sheet 21 of 34	

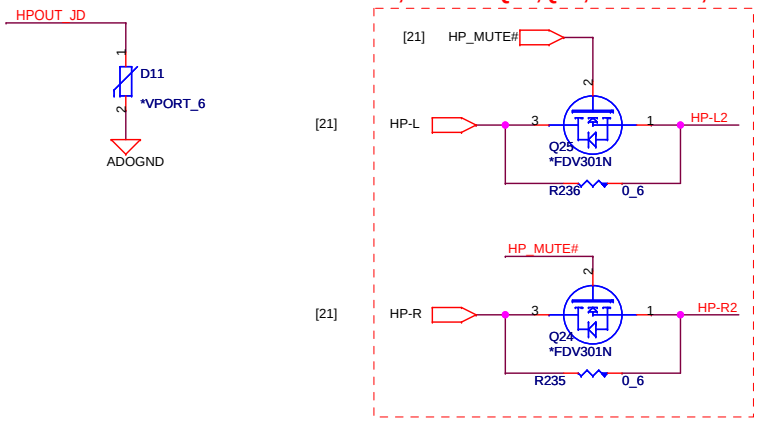
MIC



HP



C-test , remove Q25,Q24, stuff R236,R235 fix POPO sound



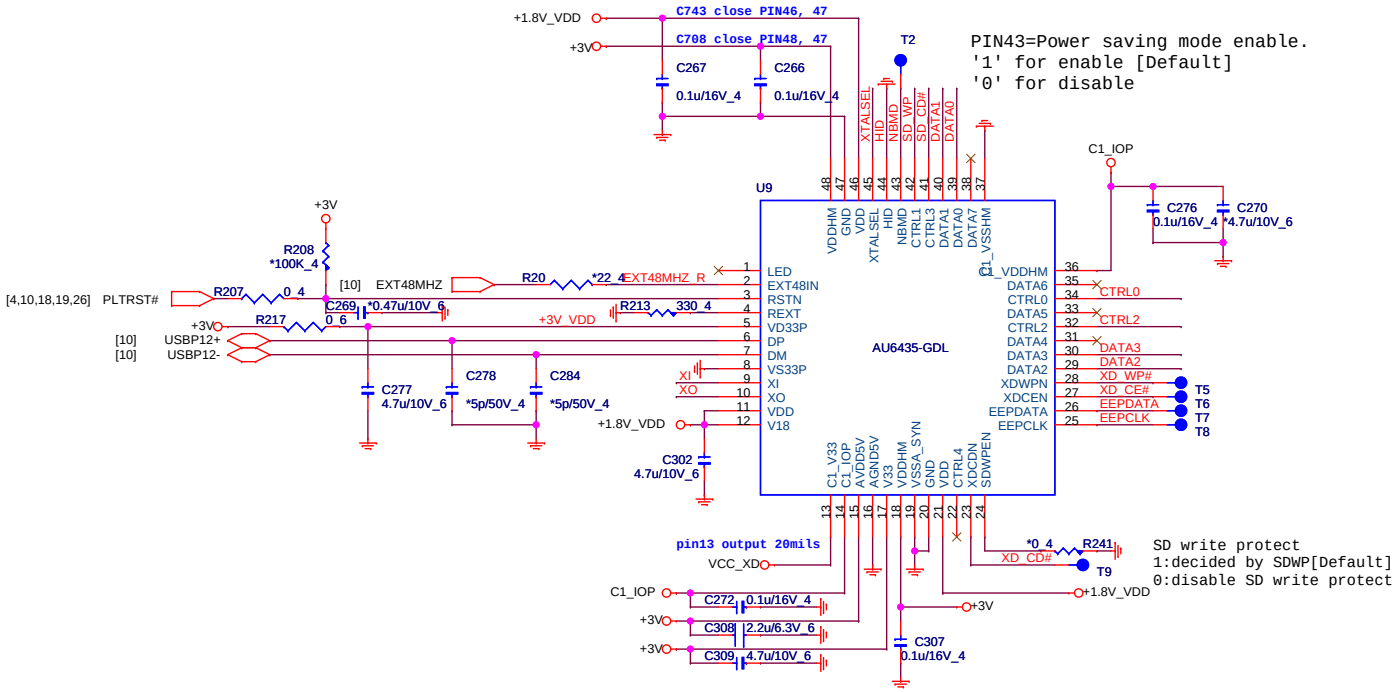
Quanta Computer Inc.

PROJECT : ZRL

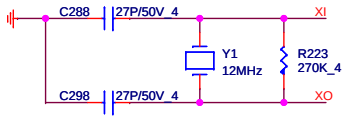
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A

Date: Tuesday, June 21, 2011 Sheet 22 of 34

4 in 1 CARD READER IC (SD,MMC,xD,MS)

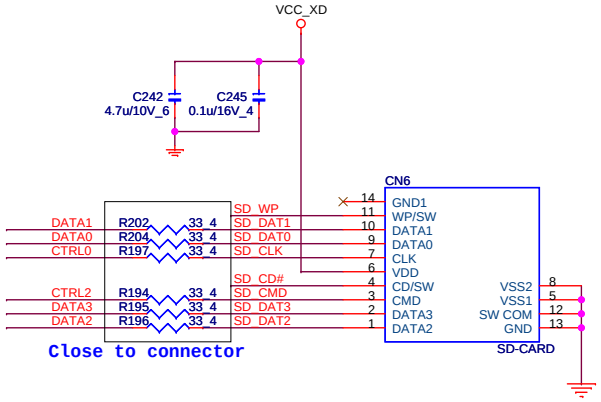


CTRL0, CRTL 1 trace length shorter ,
and surround with GND.

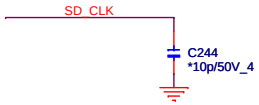


PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

2 IN 1 CARD READER CONN (SD/MMC)



CLK Shorter than 1200 mil is good.

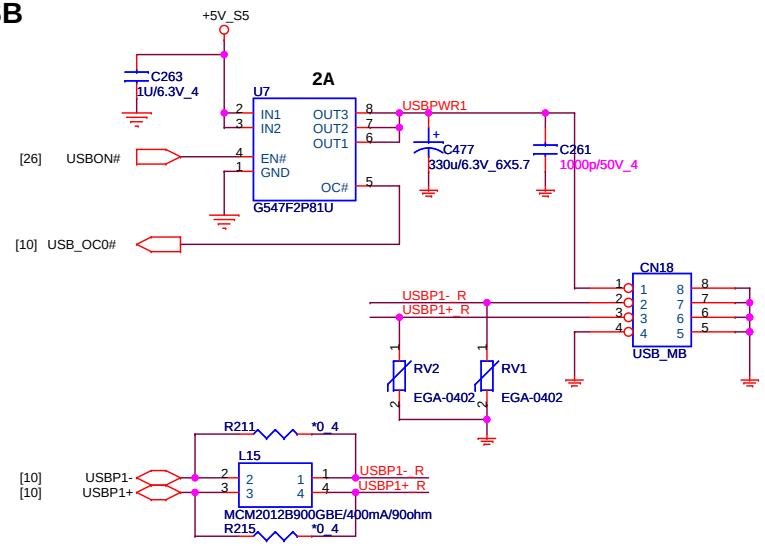


Main	DFHS11FR011
Second	DFHS11FR033

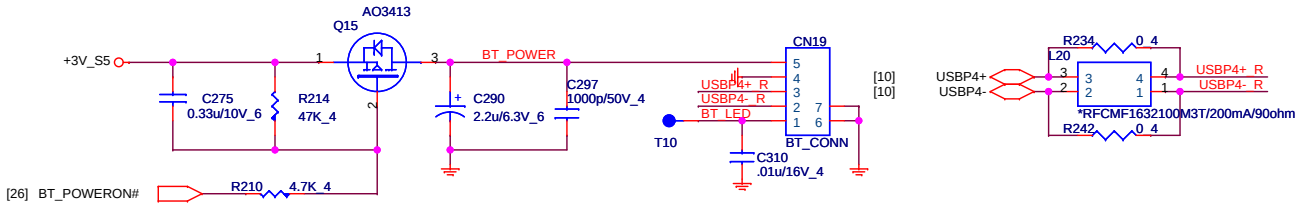
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date: Tuesday, June 21, 2011	Sheet 23 of 43	

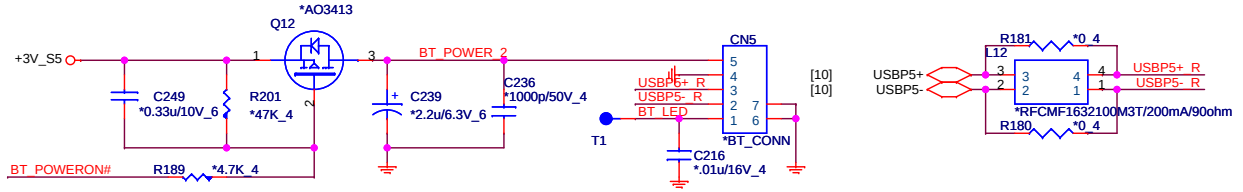
USB



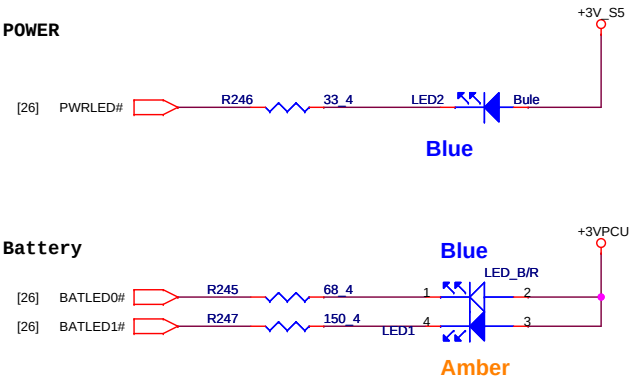
BT



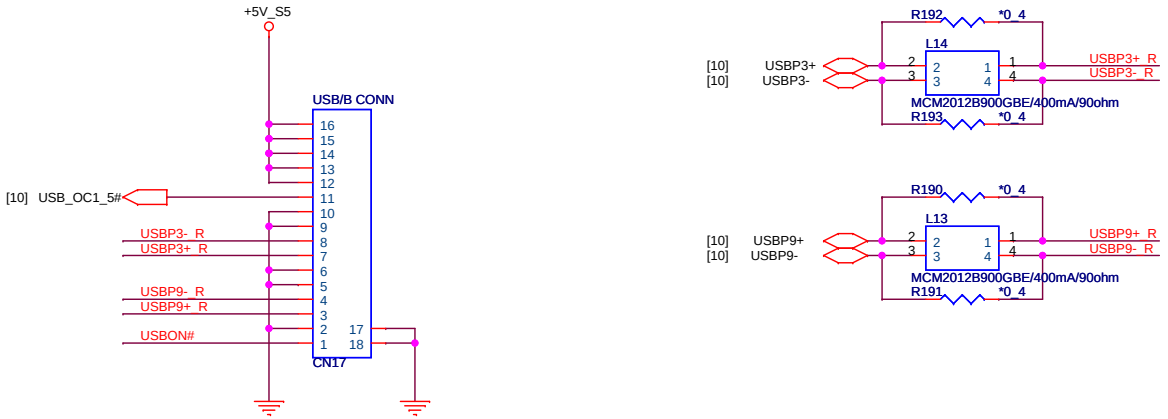
*BT



LED



USB/B



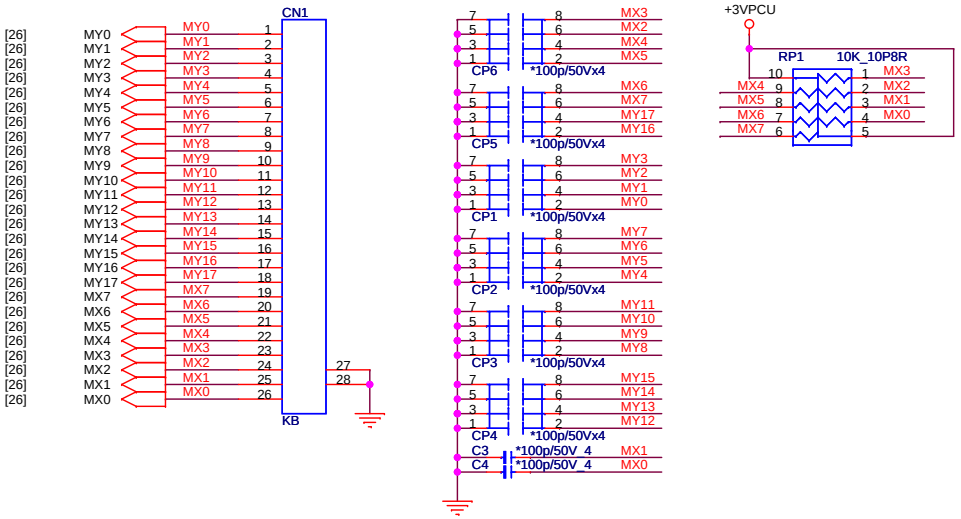
Quanta Computer Inc.

PROJECT : ZRL

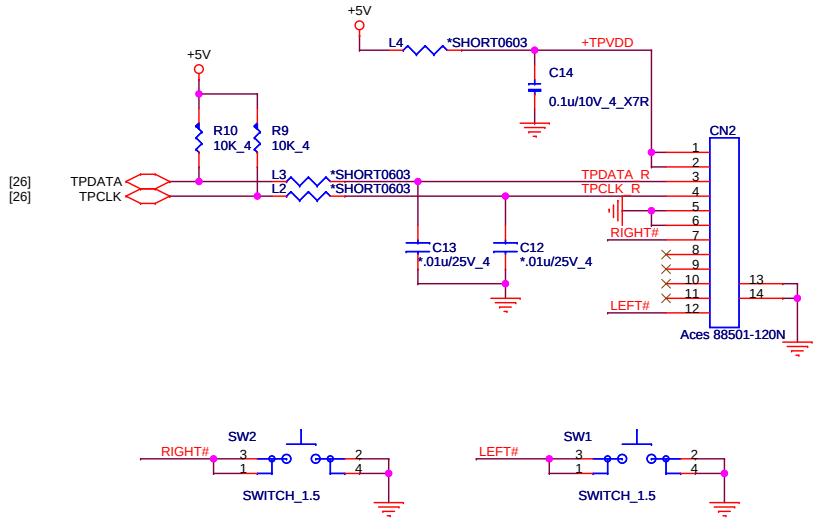
Size	Document Number	Rev
	USB/ BT	1A

Date: Tuesday, June 21, 2011 Sheet 24 of 34

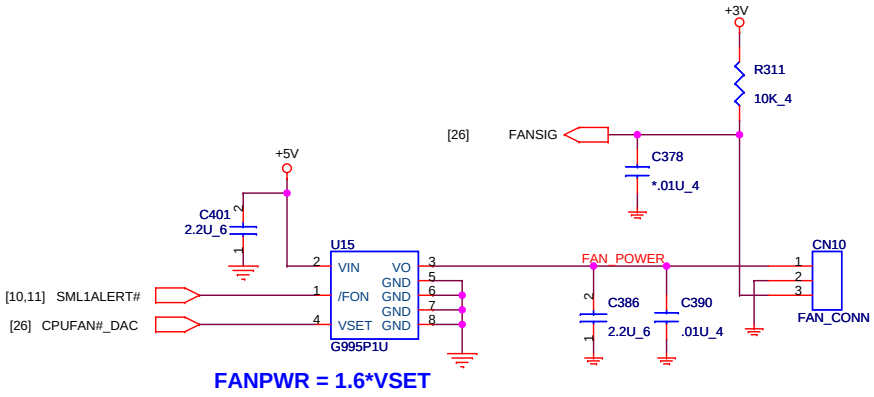
K/B



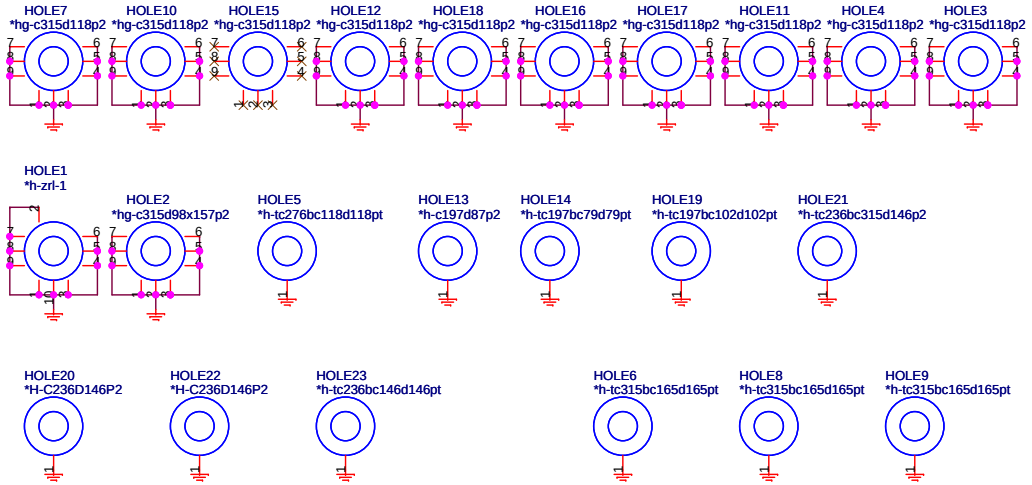
TP



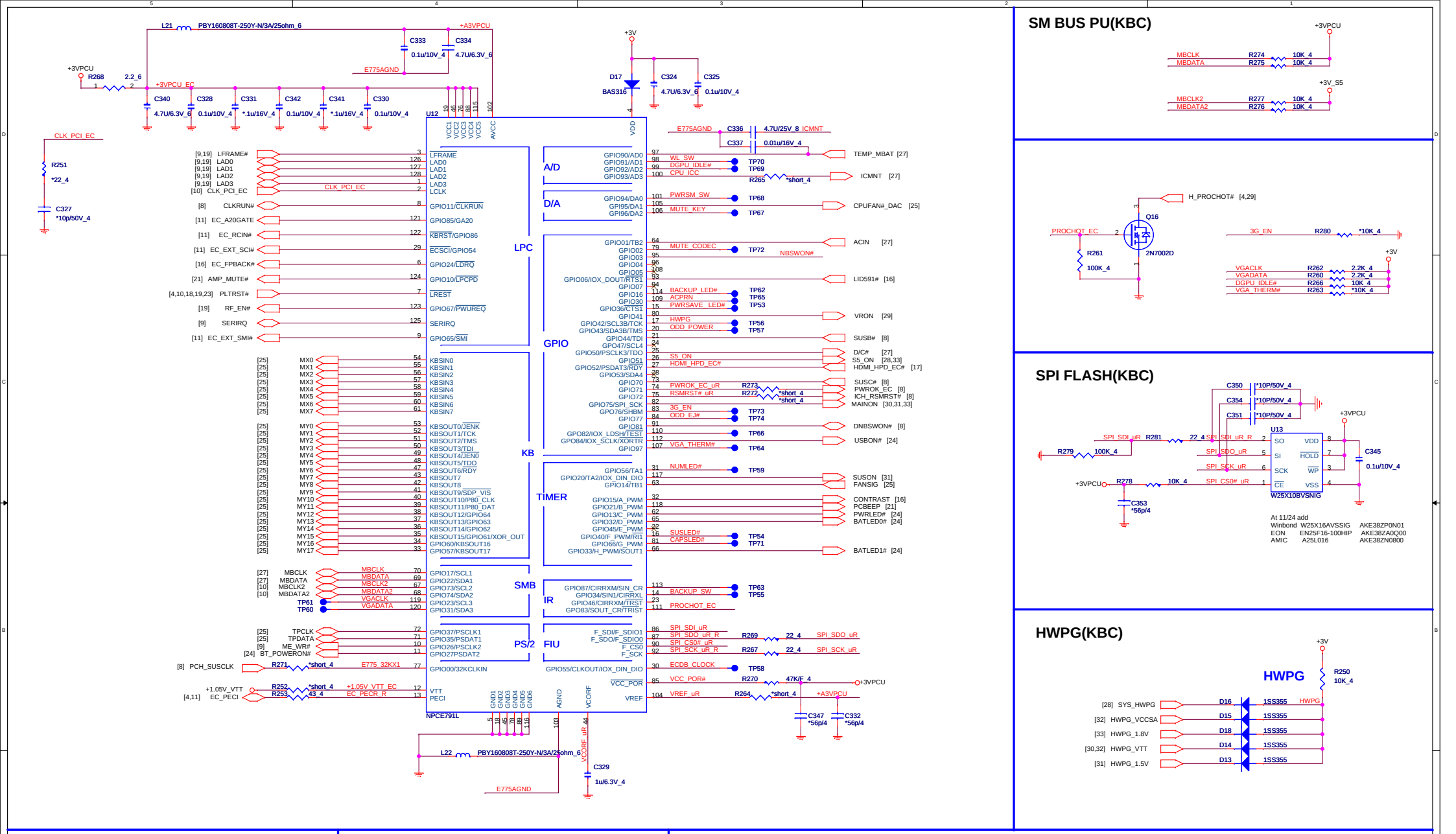
CPU FAN



HOLE



Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number: KB/FAN/TP+FP	Rev: 1A
Date: Tuesday, June 21, 2011	Sheet 25 of 34	



SM BUS PU(KBC)

SPI FLASH(KBC)

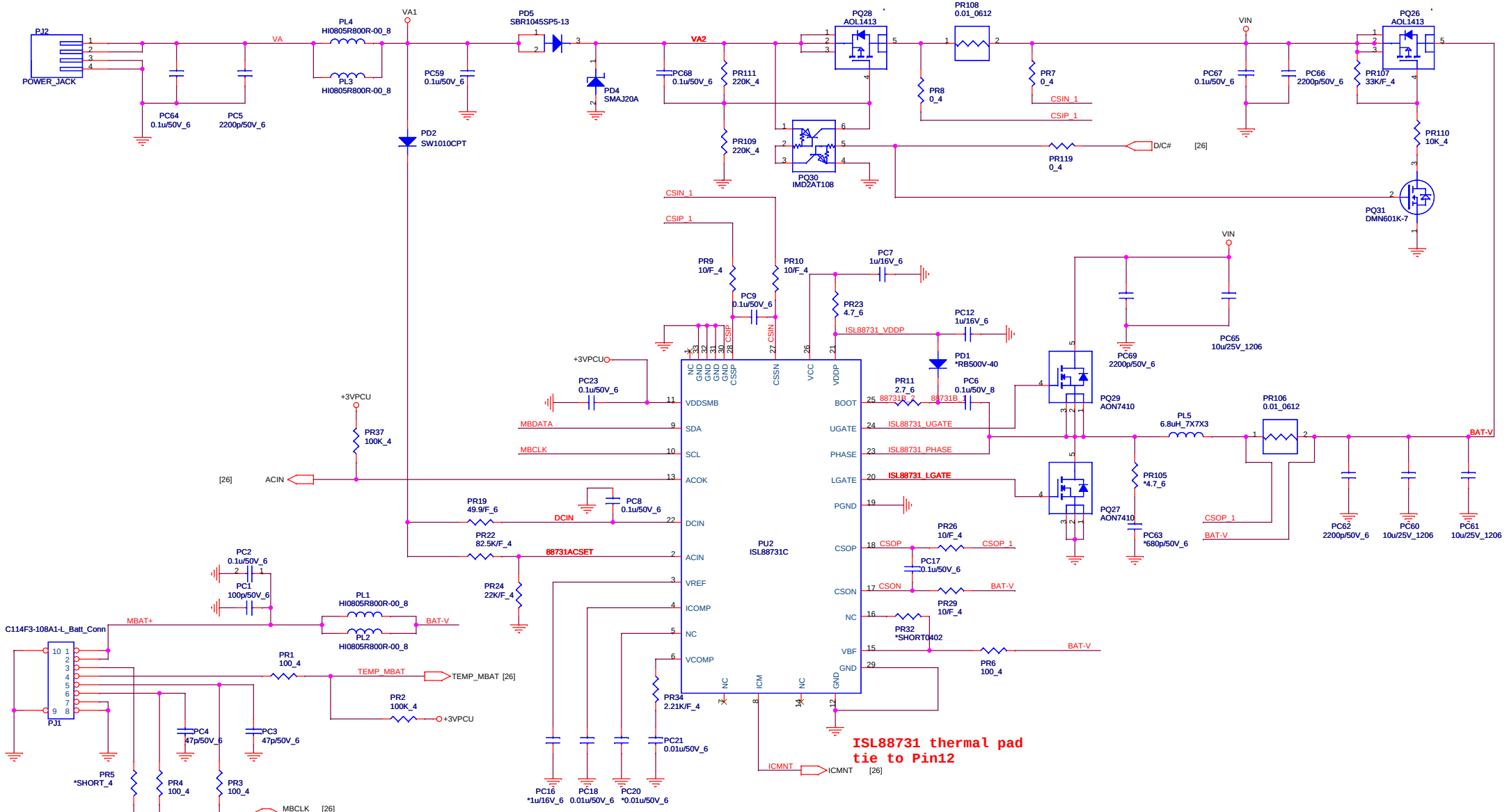
HWPG(KBC)

POWER-ON Switch(KBC)

PWR/B

Power sequence

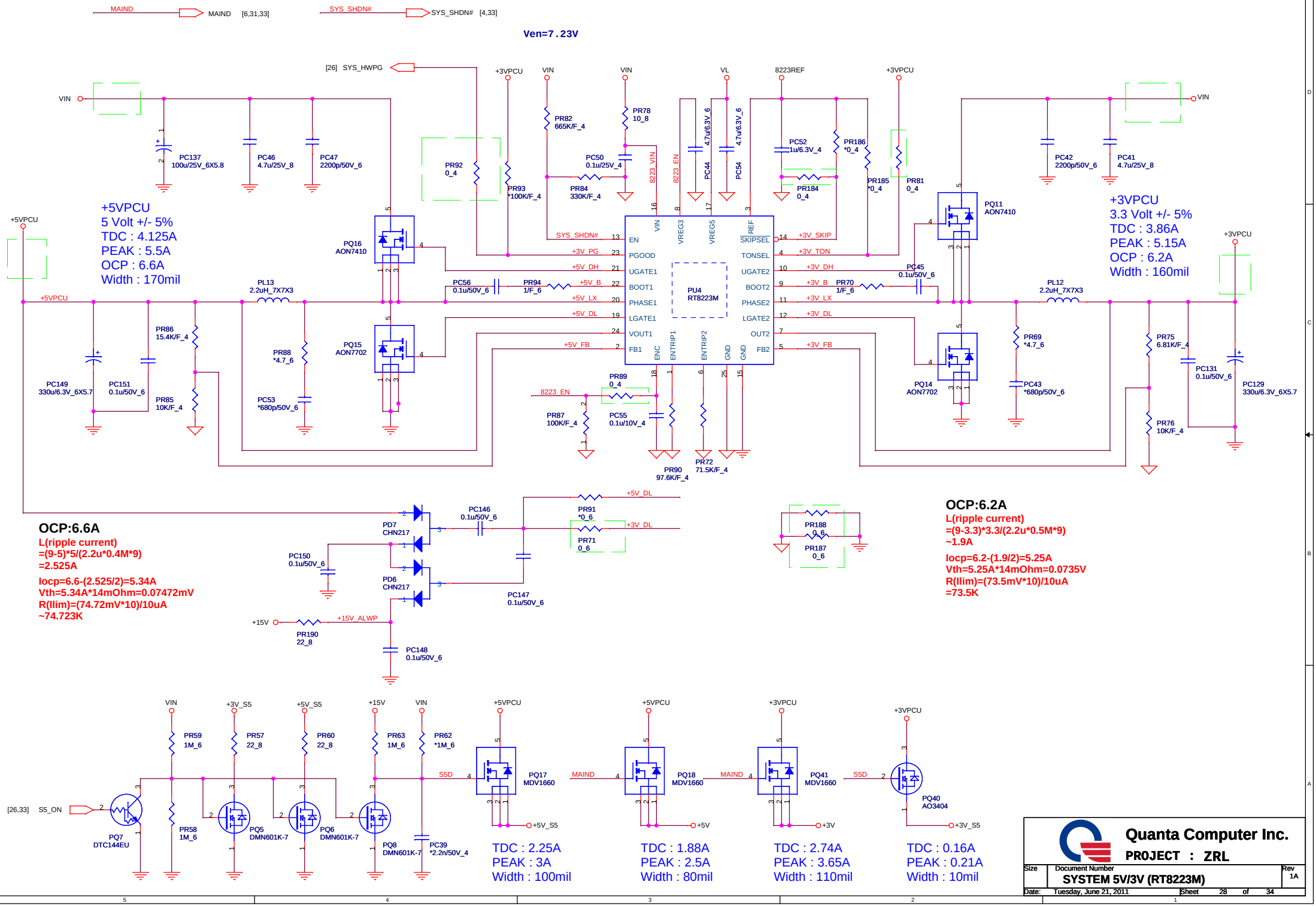
Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	WPCE791 & FLASH		1A
Date: Tuesday, June 21, 2011		Sheet 26 of 34	

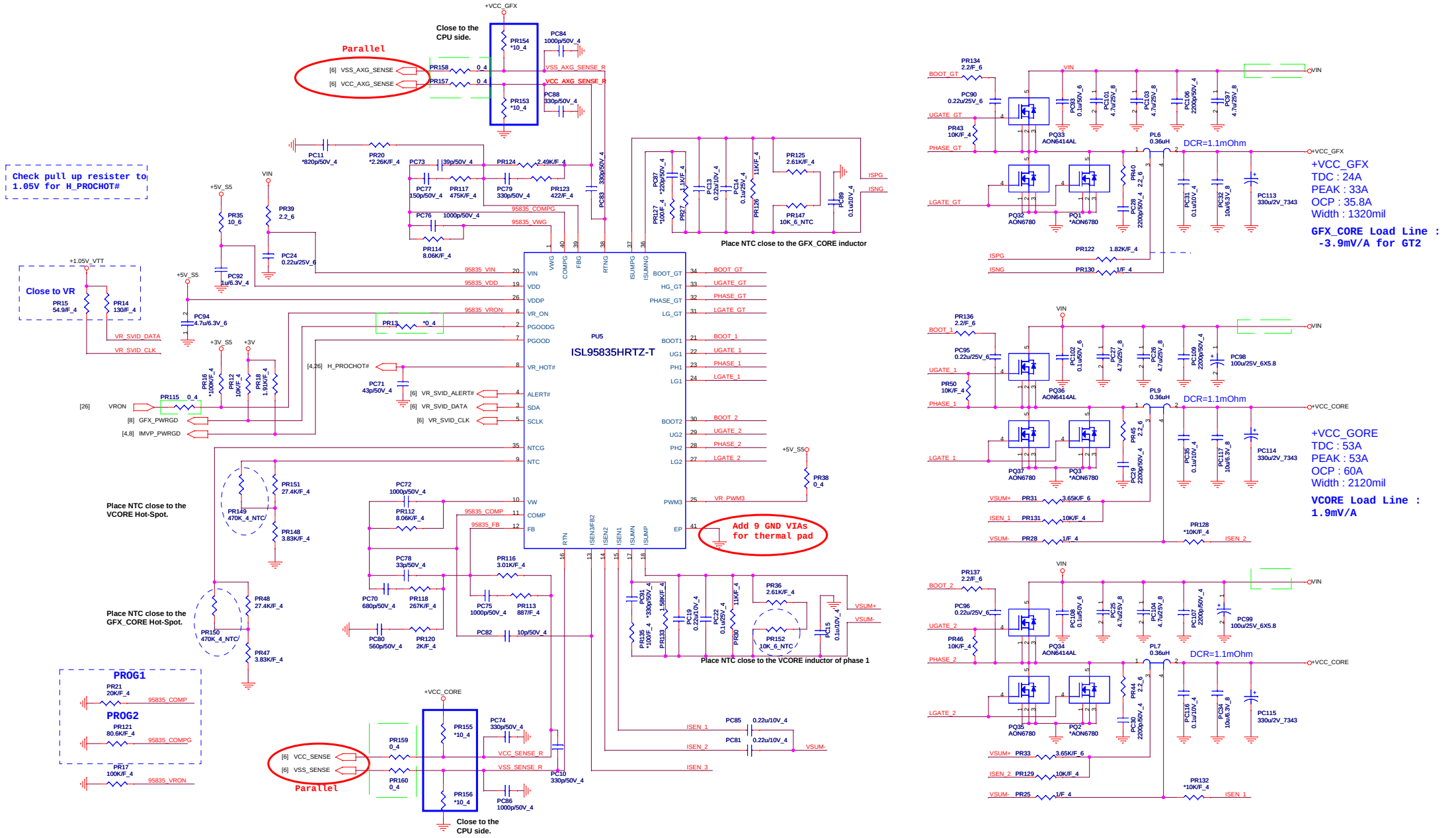


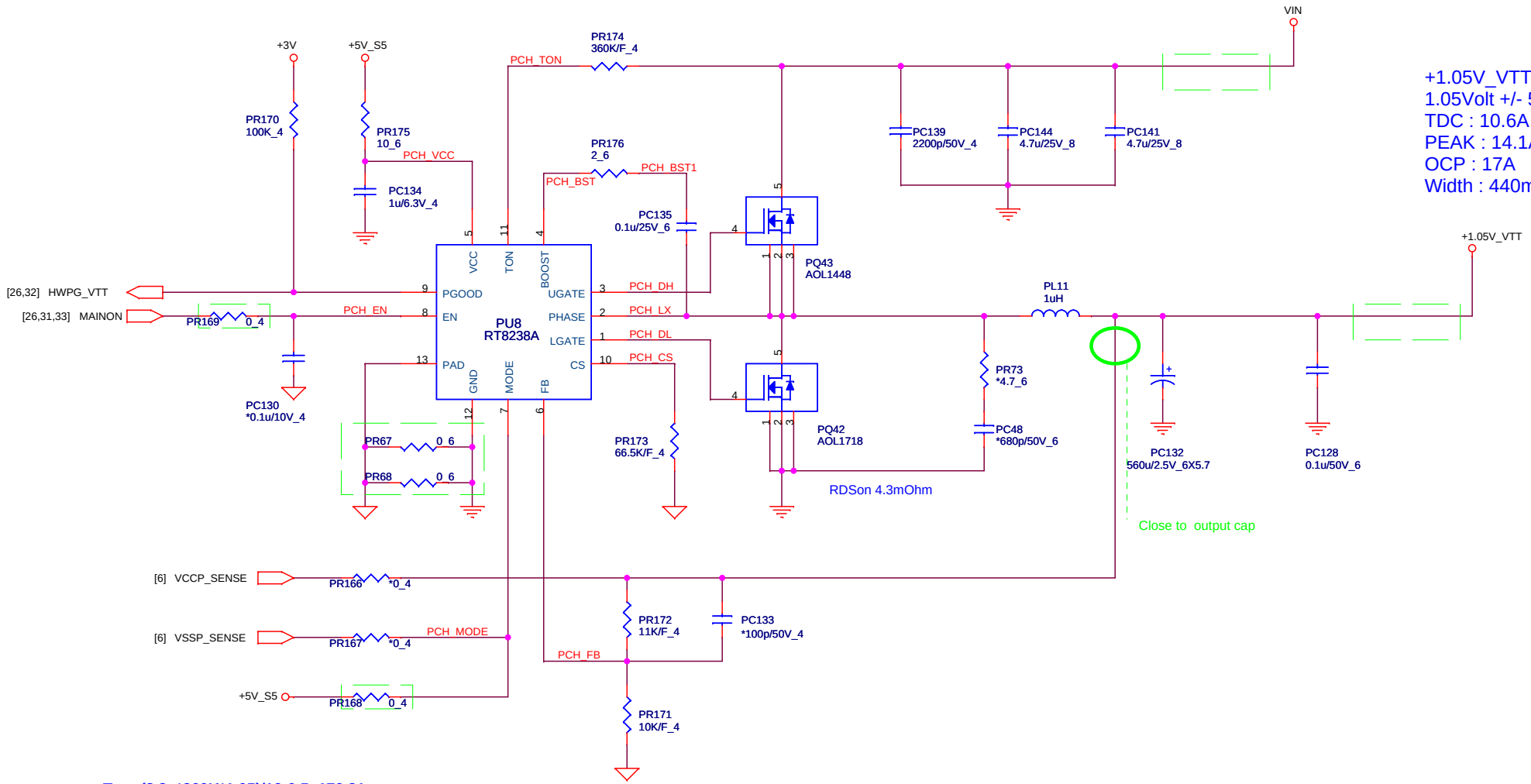
Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Charger(ISL88731A)	1A
Date: Tuesday, June 21, 2011	Sheet 27 of 34	


MAIND
MAIND [6,31,33]
SYS_SHDN#
SYS_SHDN# [4,33]
Ven=7.23V
[26] SYS_HWPG
+5VPCU
5 Volt +/- 5%
TDC : 4.125A
PEAK : 5.5A
OCP : 6.6A
Width : 170mil
+3VPCU
3.3 Volt +/- 5%
TDC : 3.86A
PEAK : 5.15A
OCP : 6.2A
Width : 160mil
PU4
RT8223M
OCP:6.6A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=6.6-(2.525/2)=5.34A
Vth=5.34A*14mOhm=0.07472mV
R(Ilim)=(74.72mV*10)/10uA
~74.723K
OCP:6.2A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6.2-(1.9/2)=5.25A
Vth=5.25A*14mOhm=0.0735V
R(Ilim)=(73.5mV*10)/10uA
=73.5K
[26,33] S5_ON
TDC : 2.25A
PEAK : 3A
Width : 100mil
TDC : 1.88A
PEAK : 2.5A
Width : 80mil
TDC : 2.74A
PEAK : 3.65A
Width : 110mil
TDC : 0.16A
PEAK : 0.21A
Width : 10mil
Quanta Computer Inc.
PROJECT : ZRL
Size
Document Number
SYSTEM 5V/3V (RT8223M)
Rev
1A
Date: Tuesday, June 21, 2011
Sheet 28 of 34


Check pull up resister to 1.05V for H_PROCHOT#
Close to VR
Close to the CPU side.
Parallel
Place NTC close to the GFX_CORE inductor
Place NTC close to the VCORE Hot-Spot.
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE inductor of phase 1
Add 9 GND VIAs for thermal pad
PU5
ISL95835HRTZ-T
PROG1
PROG2
Close to the CPU side.
Parallel
+VCC_GFX
TDC : 24A
PEAK : 33A
OCP : 35.8A
Width : 1320mil
GFX_CORE Load Line : -3.9mV/A for GT2
+VCC_GORE
TDC : 53A
PEAK : 53A
OCP : 60A
Width : 2120mil
VCORE Load Line : 1.9mV/A
DCR=1.1mOhm
Quanta Computer Inc.
PROJECT : ZRL
+VCC_CORE & +VCC_GFX (ISL95835)
Tuesday, June 21, 2011
Sheet 29 of 34



Quanta Computer Inc.

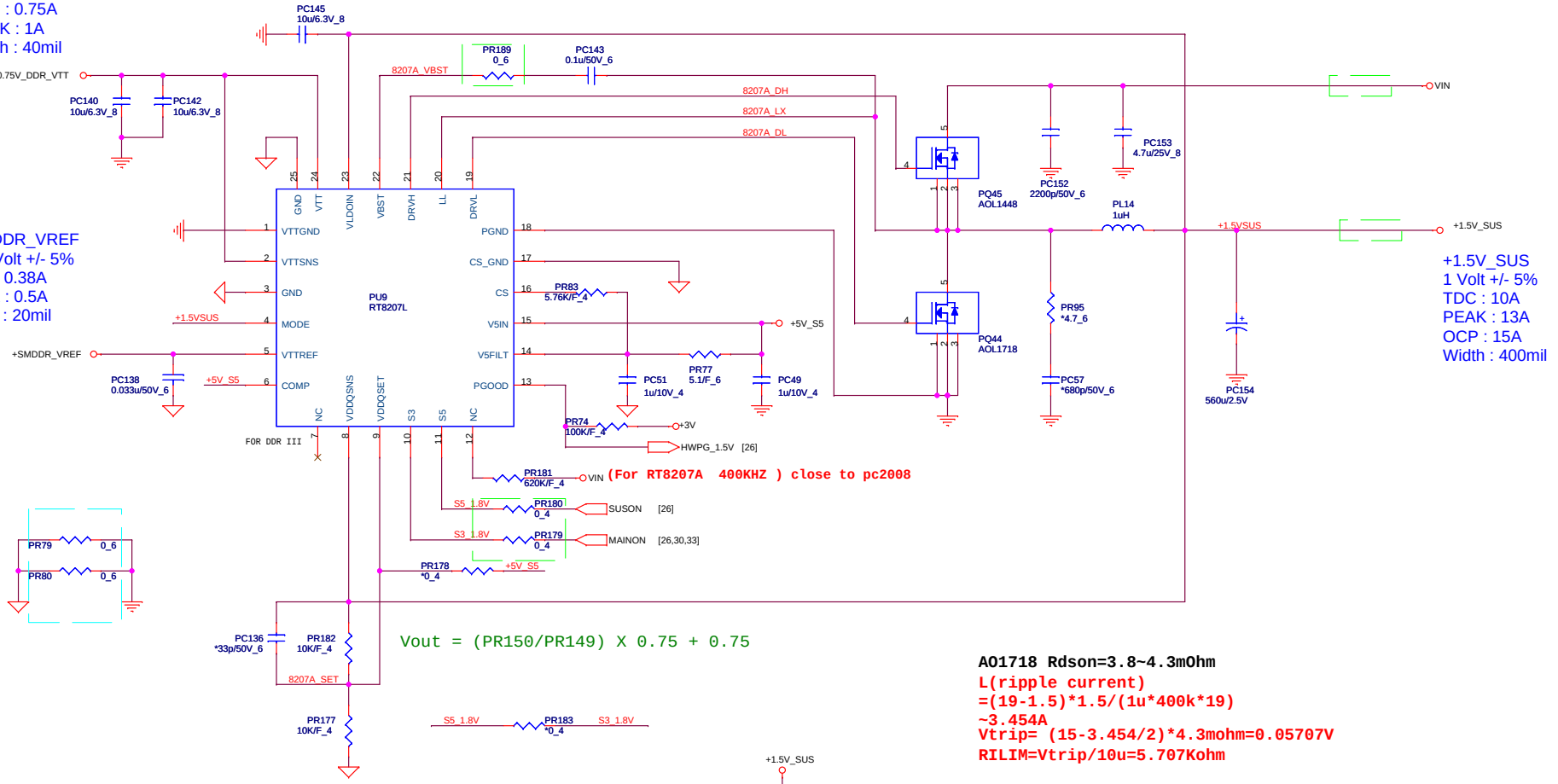
PROJECT : ZRL

Size	Document Number	Rev
	+PCH&VTT (RT8238A)	1A

Date: Tuesday, June 21, 2011 Sheet 30 of 34

+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil



+1.5V_SUS
1 Volt +/- 5%
TDC : 10A
PEAK : 13A
OCP : 15A
Width : 400mil

+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRL

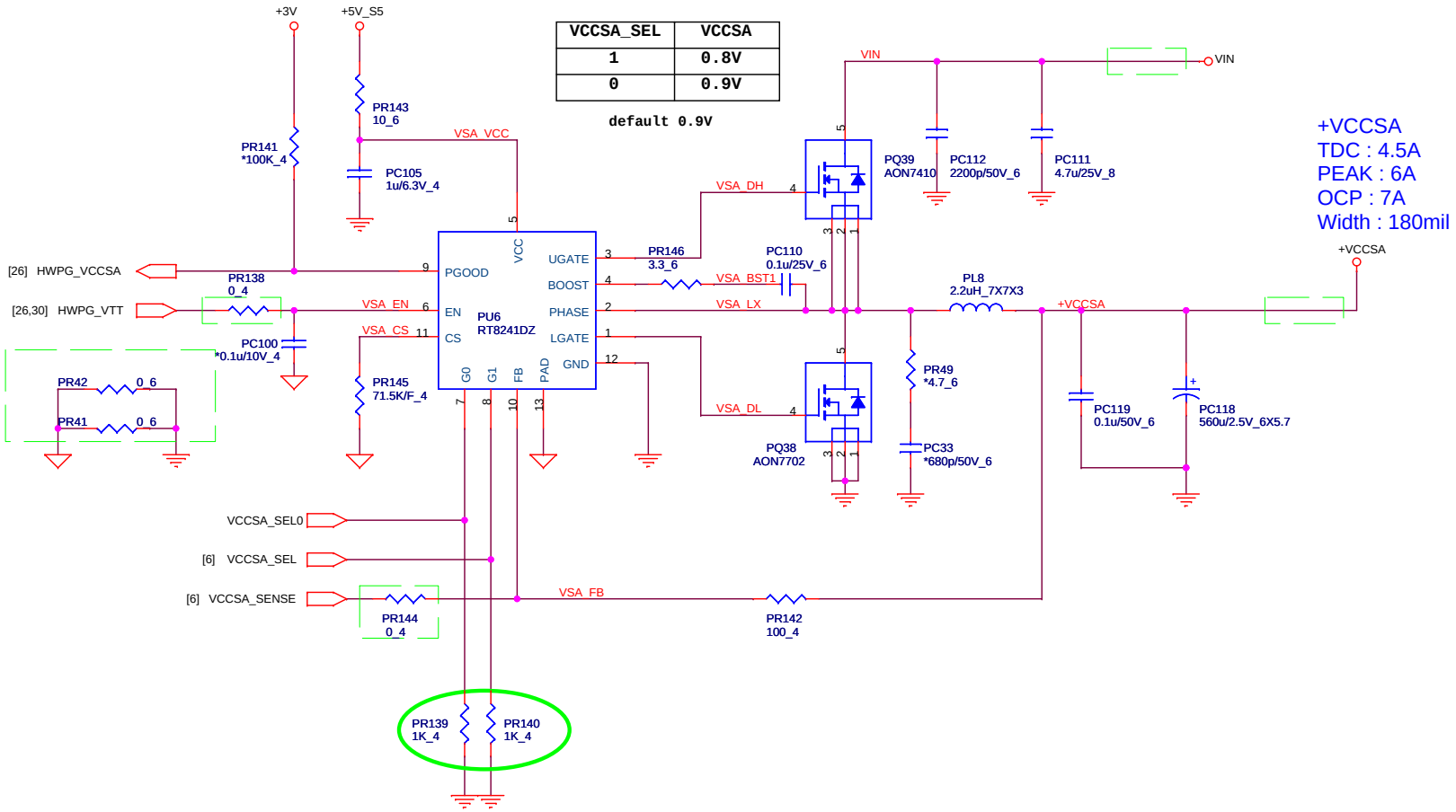
Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A

Date: Tuesday, June 21, 2011 Sheet 31 of 34

G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

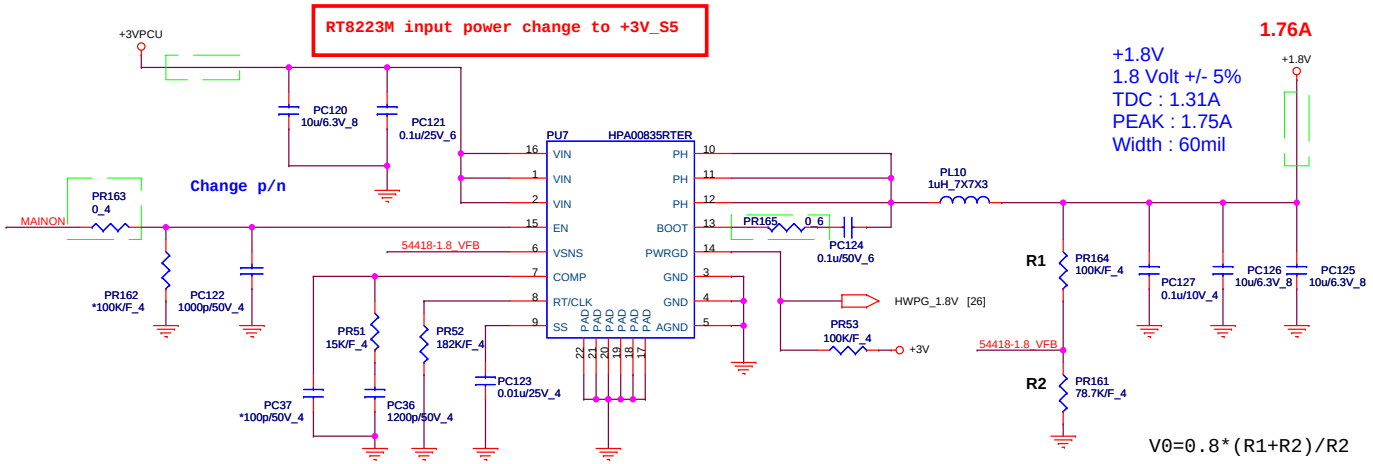


+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

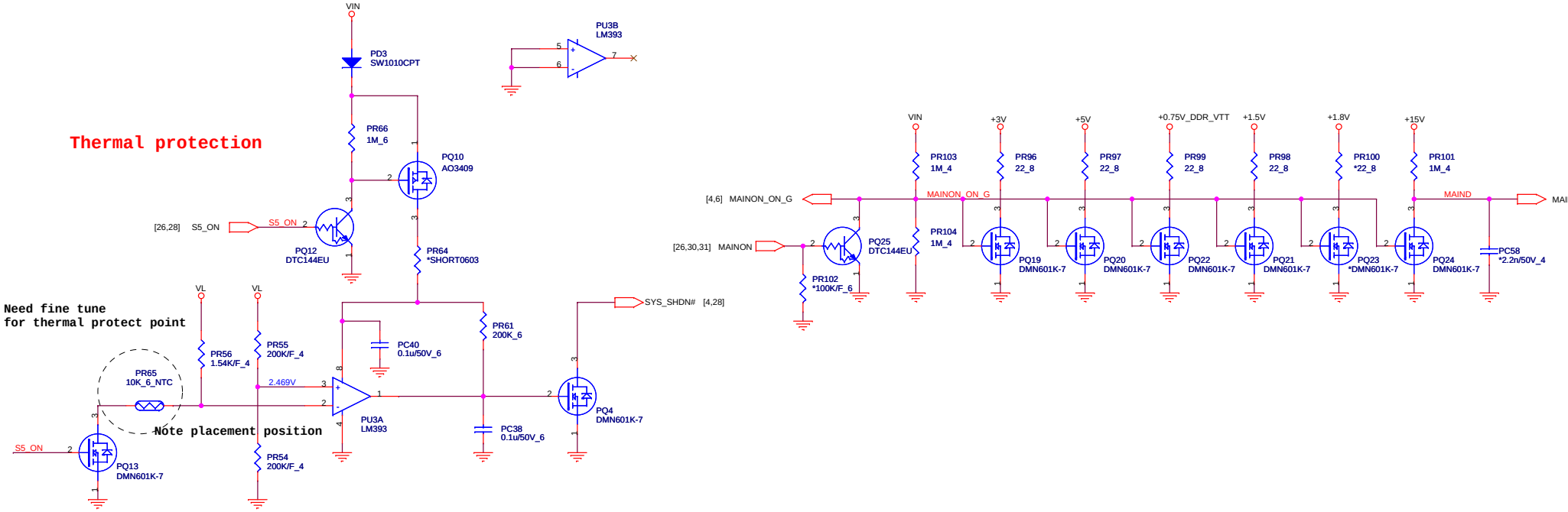
OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	+VCCSA	1A
Date: Tuesday, June 21, 2011	Sheet 32 of 34	



For EC control thermal protection (output 3.3V)



Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Discharge/1.8V)	1A

Date: Tuesday, June 21, 2011 Sheet 33 of 34

1 7/7 modify

CHANGE LIST

Model	date	CHANGE LIST
ZRL	5/18	page16 : L6,L8,L10 change to 0ohm C104,C86,C68 remove for monitor issue L5,L7,L9 change to 0603 package
		page 8 : add R422 for GFX_PWRGD
		page 27 :PQ26,PQ28 change footprint
		page 17 :Remove U6 HDMI level shift
		page 9 :add Q26,R423 to separate CODEC SYNC signal
		page 22 :change R239,R240 to 47 ohm by realtek
	5/25	page 29 : change PR133 to 1.58K, PR124 to 2.49K ,PC22,PC14 to 0.1u
		page 22 : remove Q25,Q24, stuff R236,R235 fix POPO sound
	6/9	page 24 : change R246 to 33ohm,R245 to 68ohm, R247 to 150ohm for LED brightness.
	2A	

MODEL	ZRL	
	FROM	To
	X	1A
	X	1A
	X	1A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A

Quanta Computer Inc.
PROJECT : ZRL

Size | Document Number: Change list2 | Rev 1A
Date: Tuesday, June 21, 2011 | Sheet 34 of 34

DOC NO.	PROJECT MODEL :	ZRL	APPROVED BY:	Spruce Wu	DATE:
	PART NUMBER:	31ZRLMB0000	DRAWING BY:	Ronnie Liu	REVISON: