


LCFC Confidential

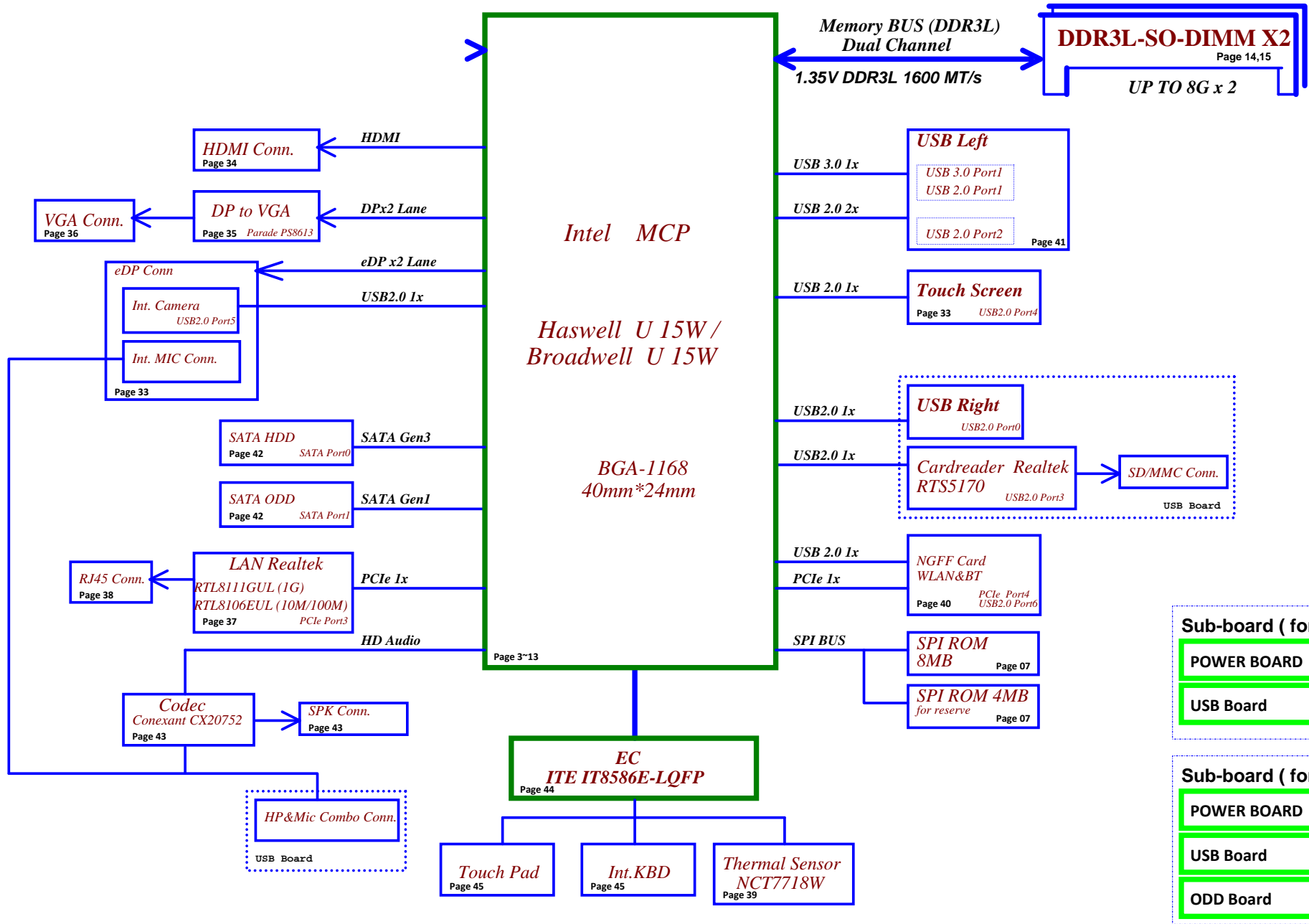
ACLU1/2 UMA M/B Schematics Document

Intel Haswell/Broadwell U-Processor

2013-12-05

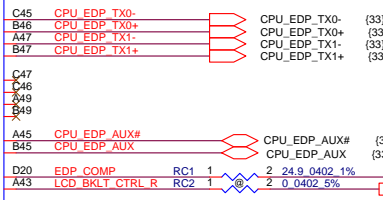
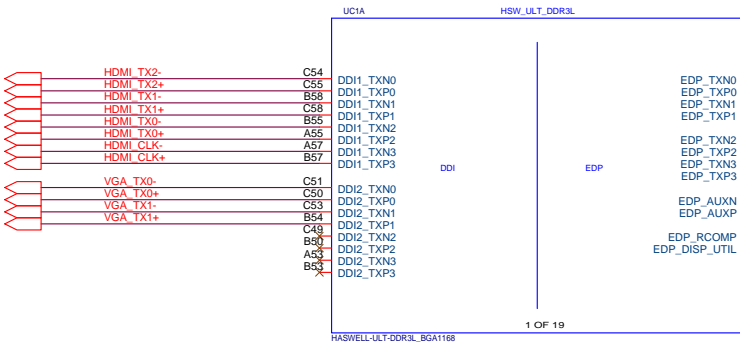
REV:1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page		
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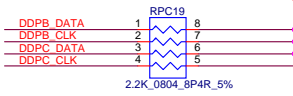
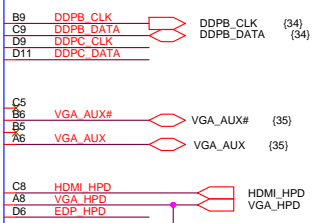
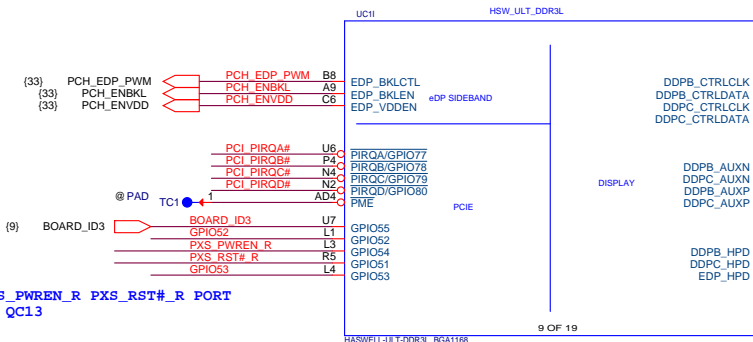


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HDMI D2
HDMI D1
HDMI D0
HDMI CLK
DP TO VGA Converter



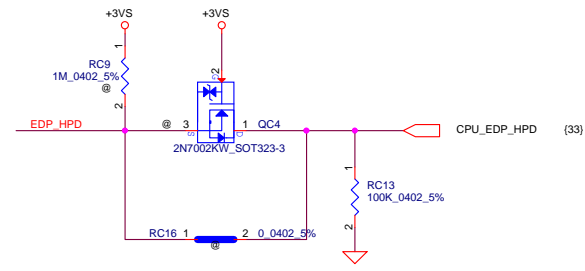
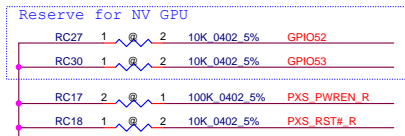
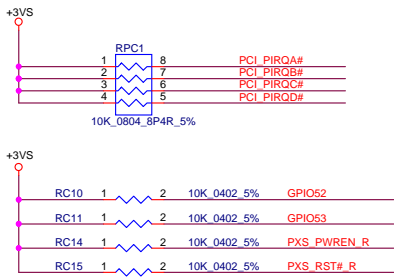
+VCCIOA_OUT +VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil



DDPx_CTRLDATA
The signal has a weak internal pull-down.
* H Port is detected.
L Port is not detected.

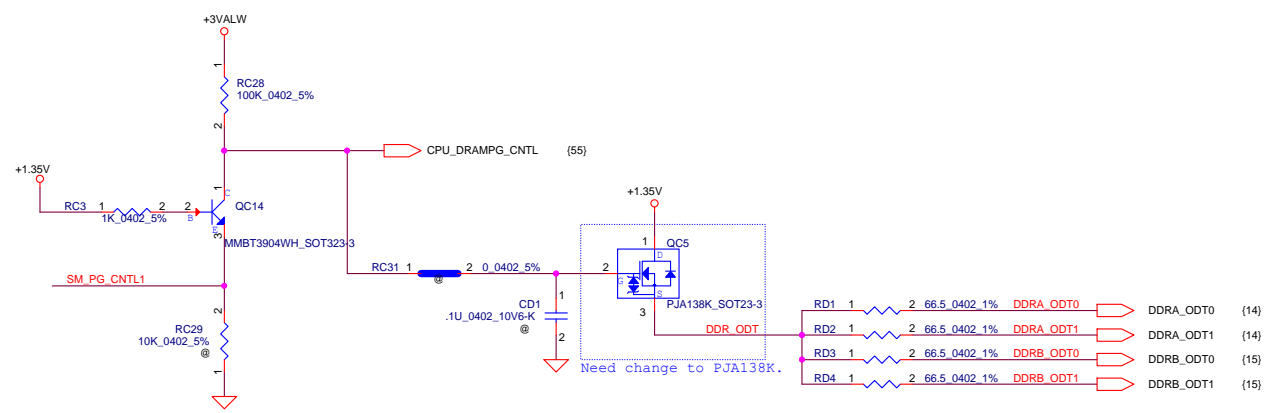
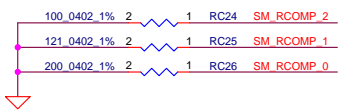
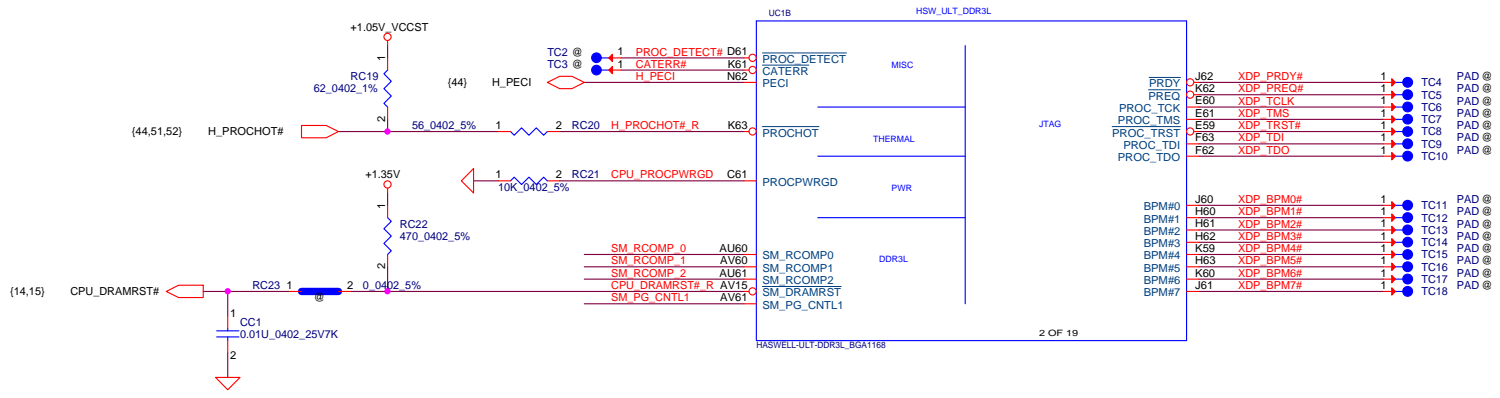
ACLU2: delete PXS_PWREN_R PXS_RST#_R PORT
and RC7 RC8 RC170 QC13

After confirm with vendor, HPD has internal pull-down ~100K at PS8613, just reserve in case.
RC37 can be removed next phase if no issue.

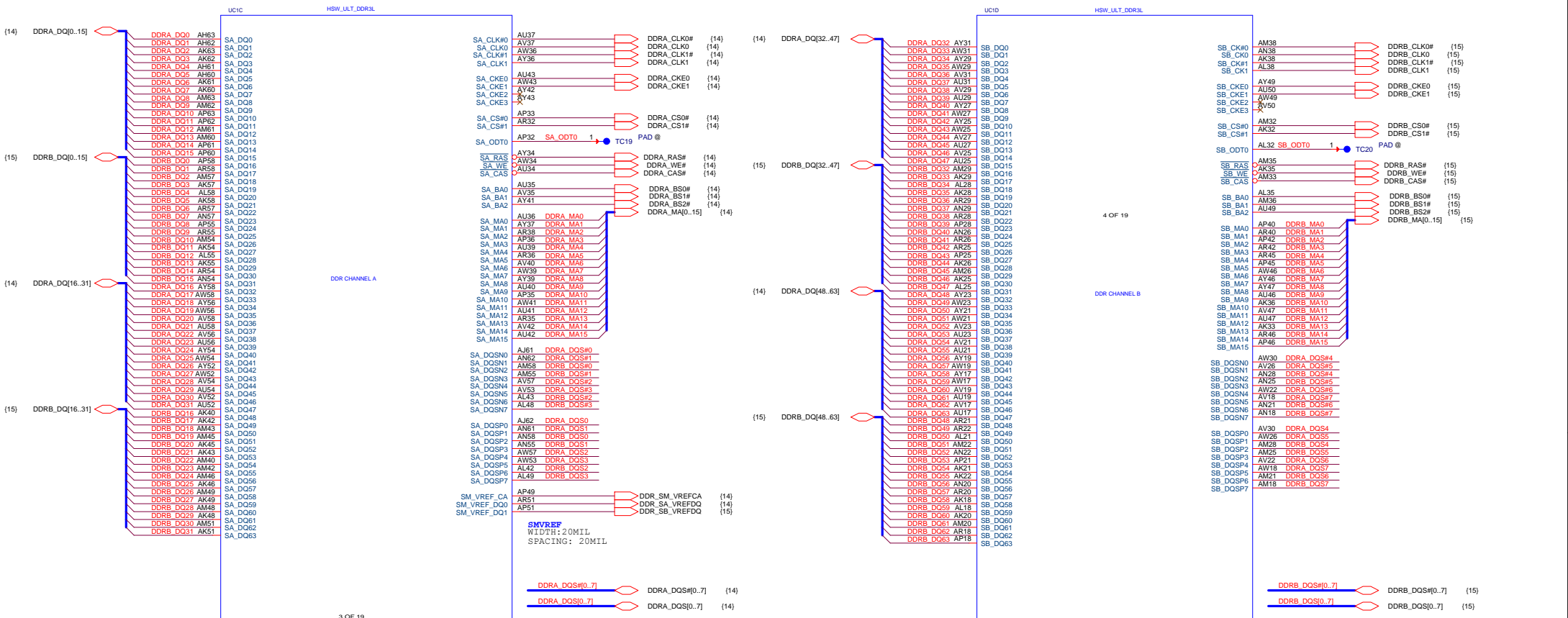


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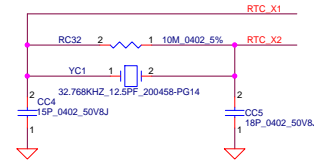
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Size	Document Number	Rev	1.0
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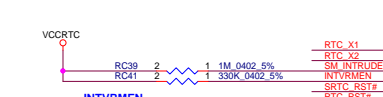
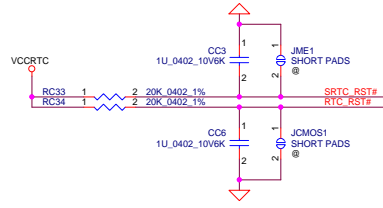
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size	Custom
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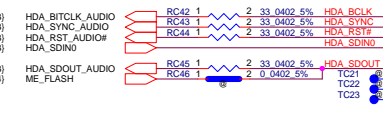
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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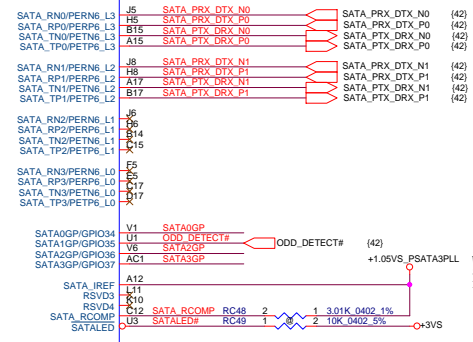
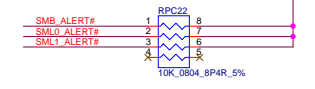
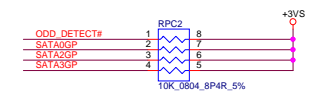
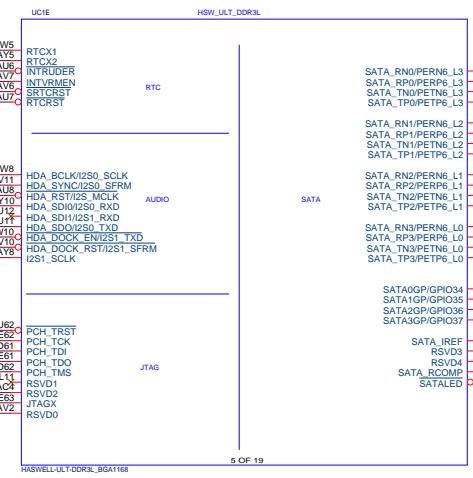
CRYSTAL
 1. Space 15mil
 2. No trace under crystal
 3. Place on opposite side of MCP for temp influence



INTVRMEN
 * H Integrated VRM enable (Default)
 L Integrated VRM disable
 (INTVRMEN should always be pull high.)

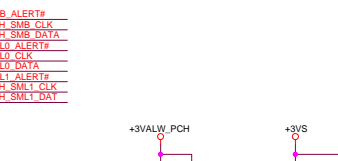
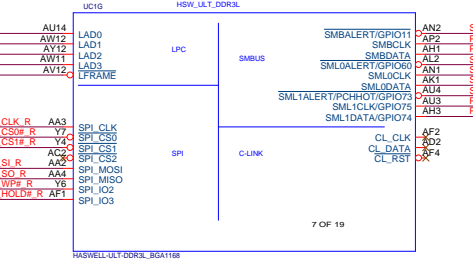
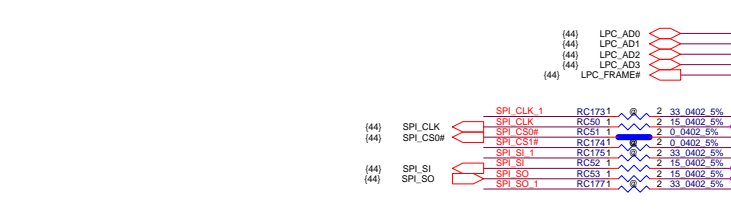


HDA_SDO This signal has a weak internal pull-down.
 * 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

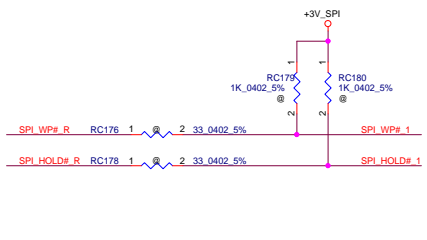
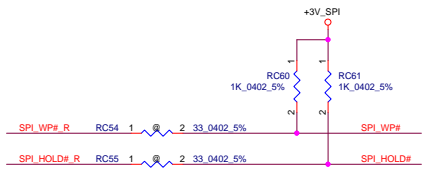


HDD
 ODD

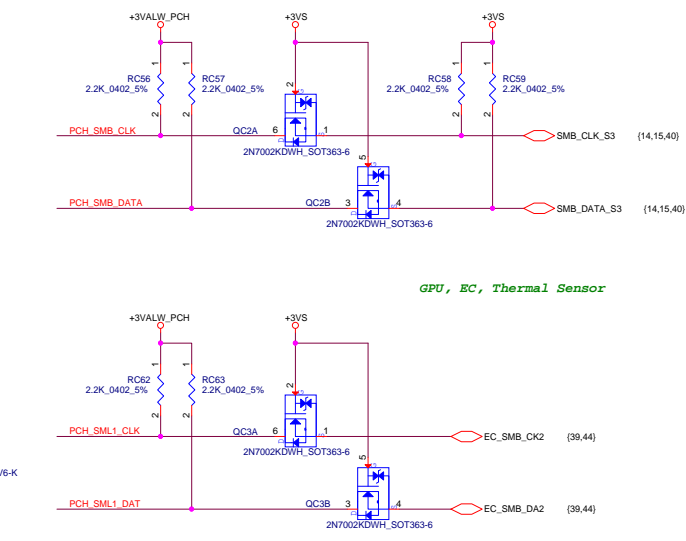
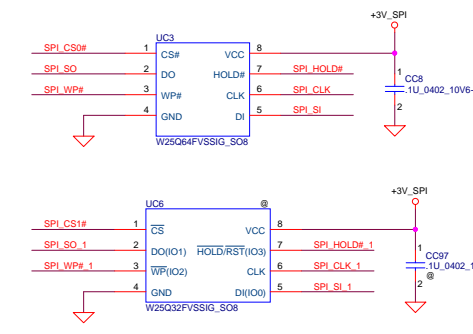
IREF6RCOMP
 Width: 12-15mil
 Space: 12mil
 Length: 500mil



DIMM1, DIMM2, NGFF

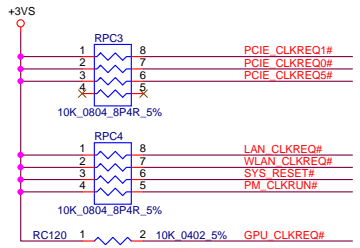


+3V SPI
 1. If support DS3, connect to +3VS and don't support EC mirror code;
 * 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

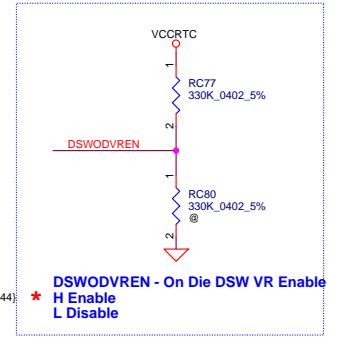
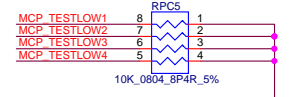
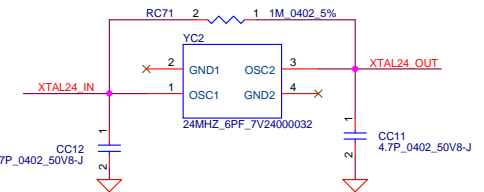
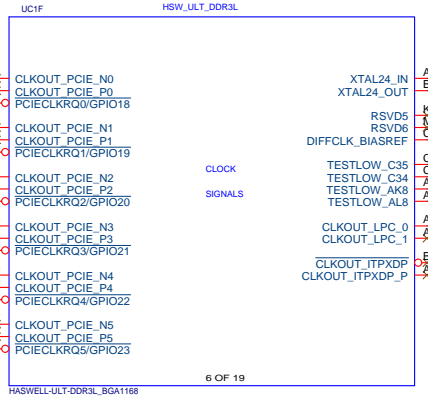
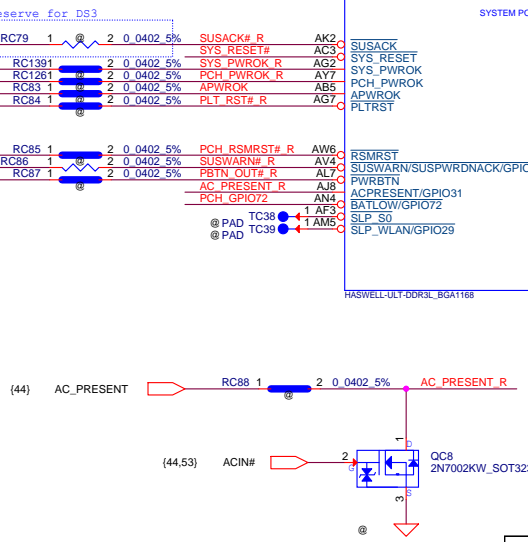
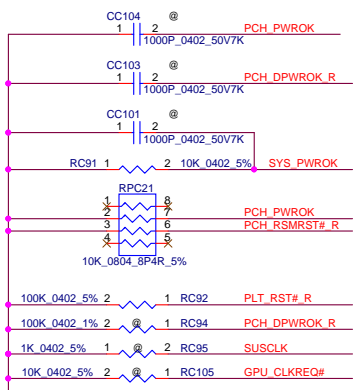
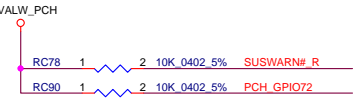
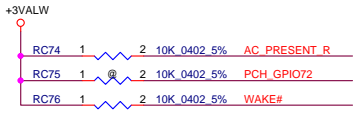


GPU, EC, Thermal Sensor

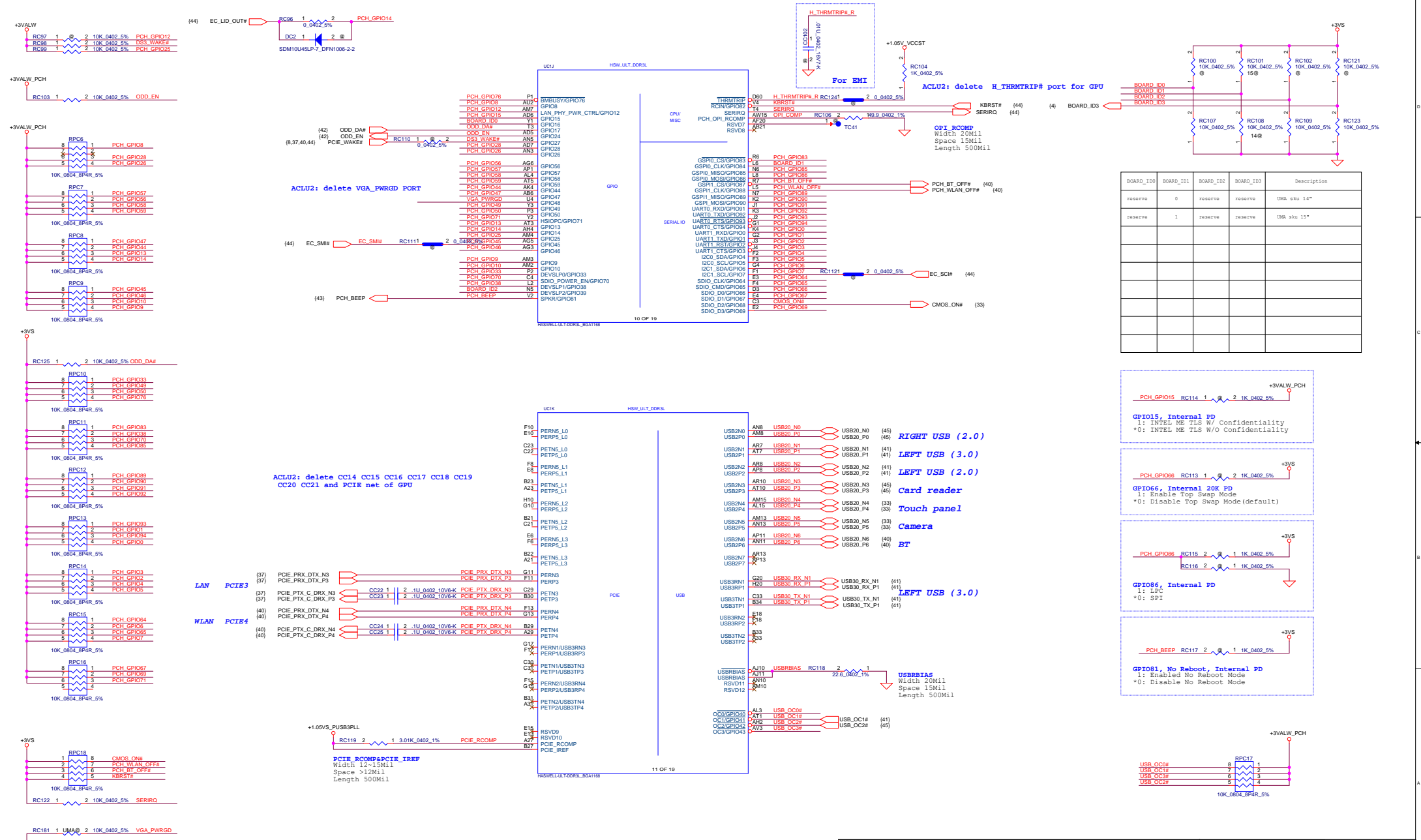
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PCIE CLK2 LAN (37) CLK_PCIE_LAN#
 (37) CLK_PCIE_LAN LAN_CLKREQ#
PCIE CLK3 WLAN (40) CLK_PCIE_WLAN#
 (40) CLK_PCIE_WLAN WLAN_CLKREQ#
PCIE CLK4 GPU (40) CLK_PCIE_WLAN#
 (40) CLK_PCIE_WLAN WLAN_CLKREQ#



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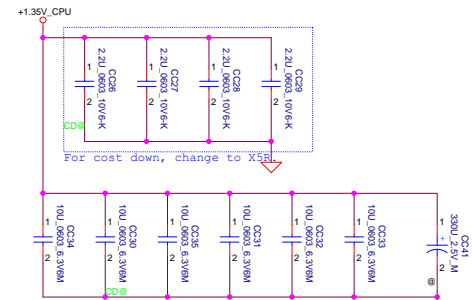
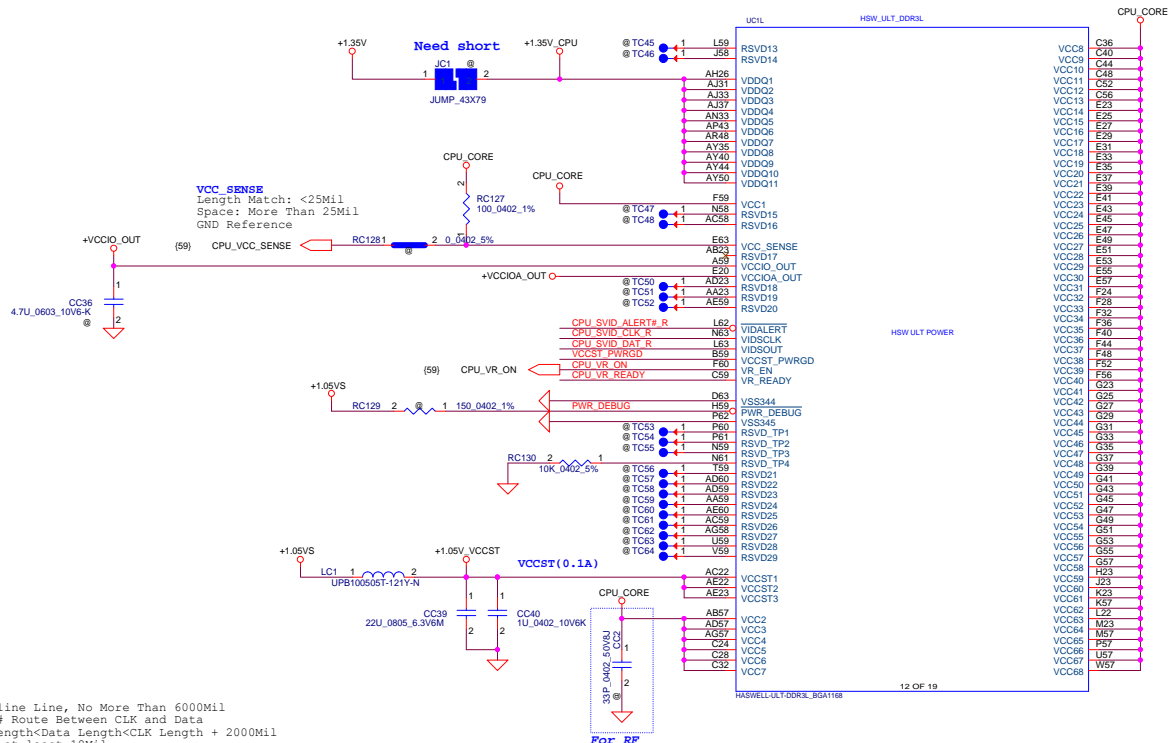
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description
reserve	0	reserve	reserve	UDA sku 14"
reserve	1	reserve	reserve	UDA sku 15"

GPIO15, Internal PD
 *0: INTEL ME TLS W/ Confidentiality
 *1: INTEL ME TLS W/O Confidentiality

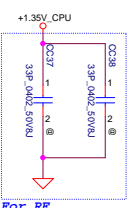
GPIO66, Internal 20K PD
 *1: Enable Top Swap Mode
 *0: Disable Top Swap Mode (default)

GPIO86, Internal PD
 *1: LFC
 *0: SPI

GPIO81, No Reboot, Internal PD
 *1: Enabled No Reboot Mode
 *0: Disable No Reboot Mode

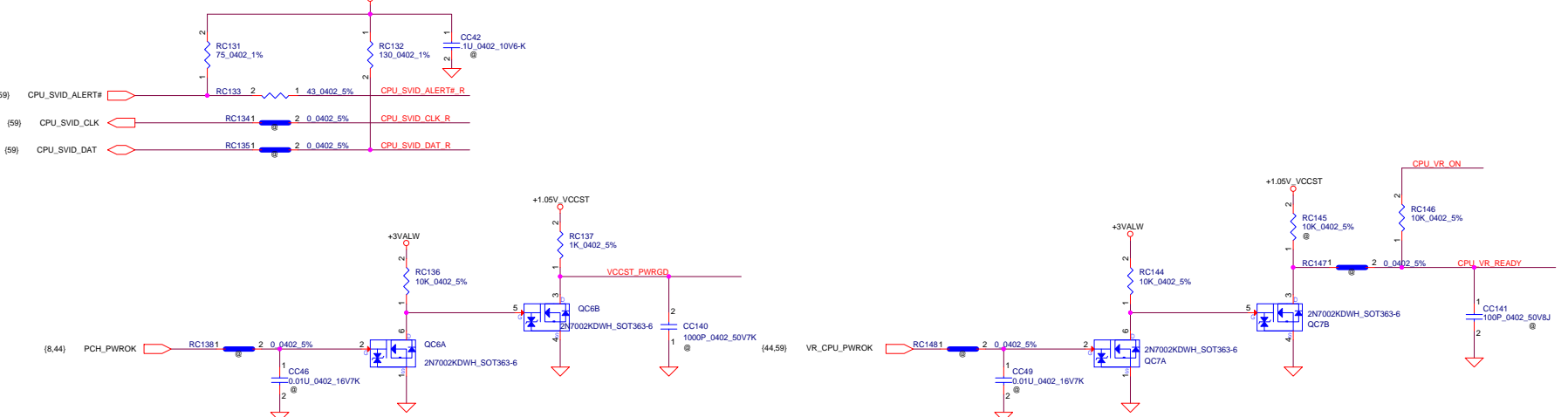


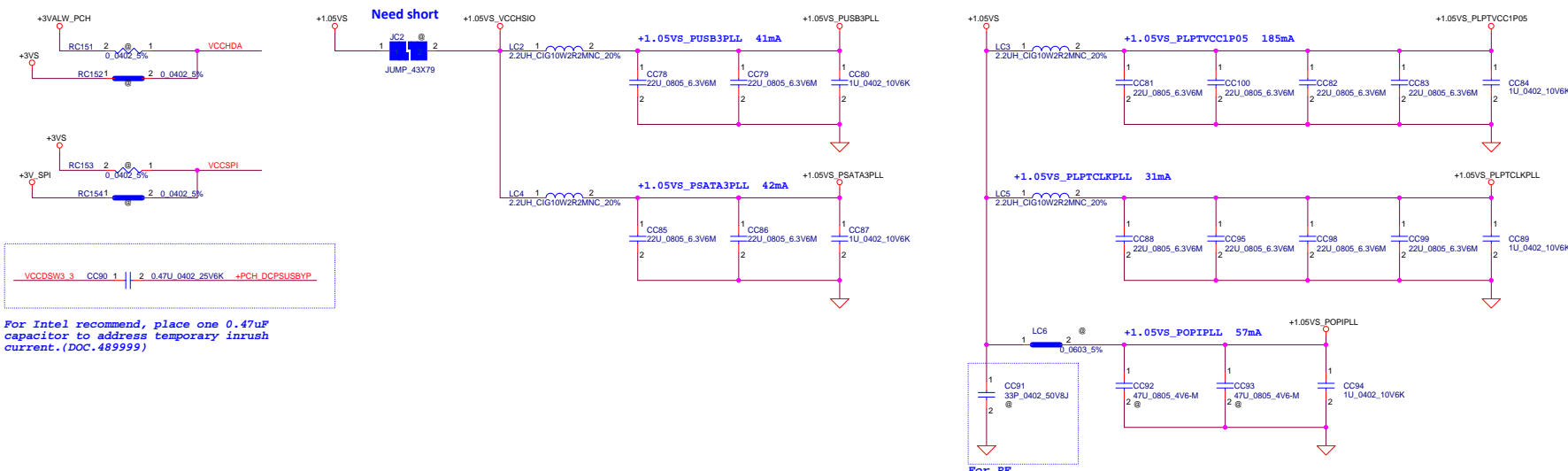
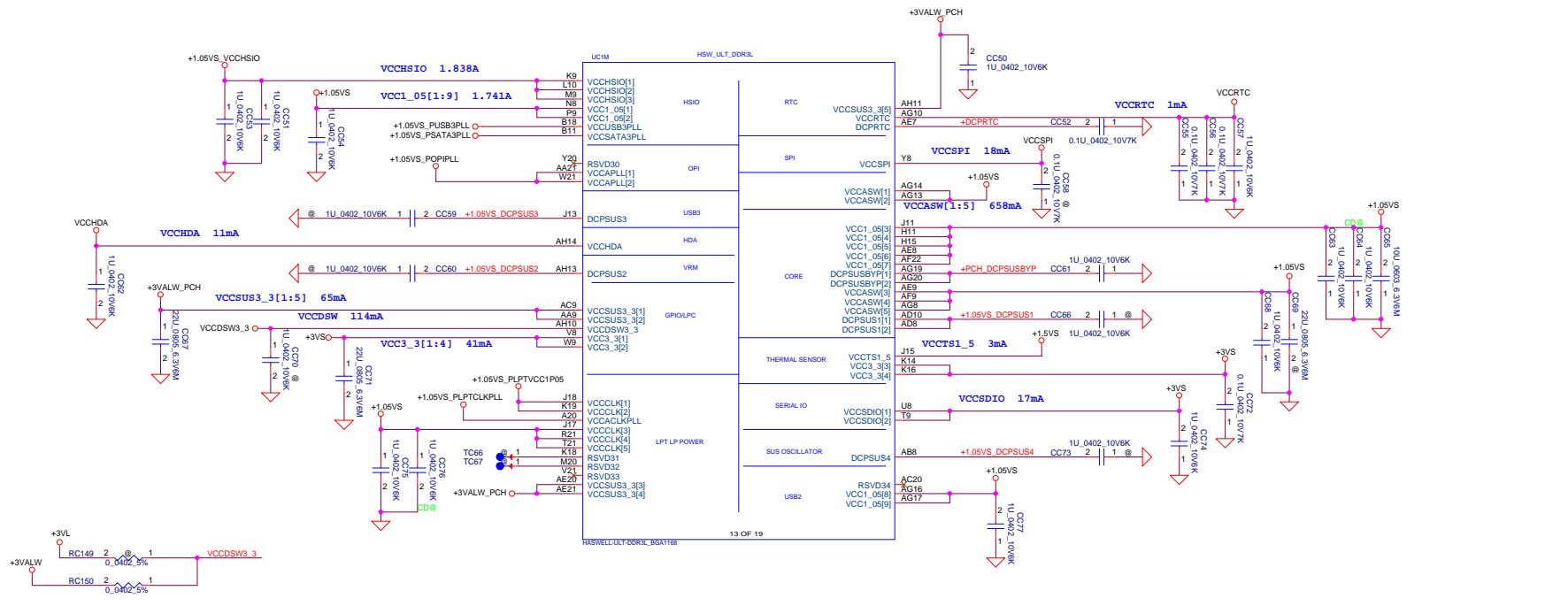
1.35V CPU (1.4A)
 HW 4PCS 2.2UF CAP Mounted
 HW 6PCS 10UF CAP Mounted
 PWR 2PCS 470U Near VR Output



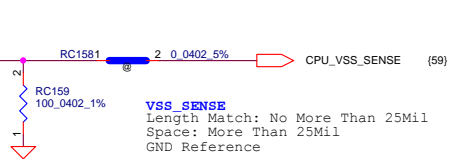
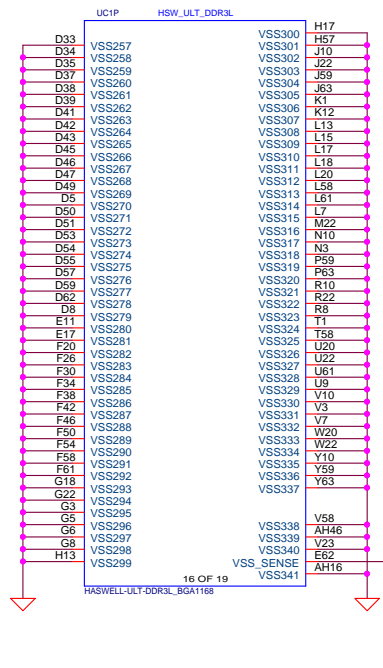
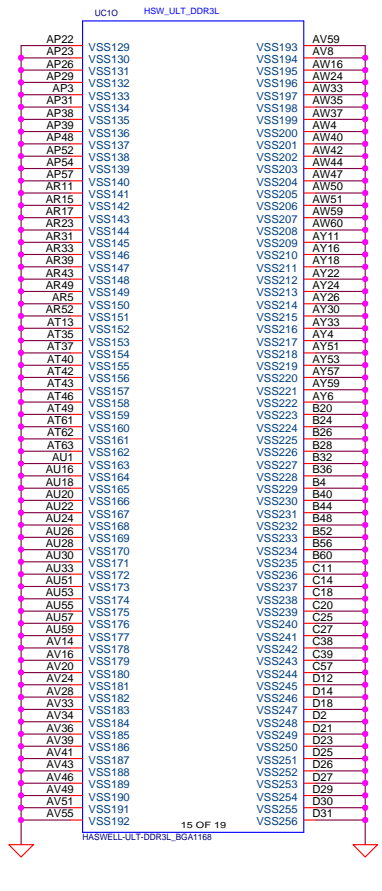
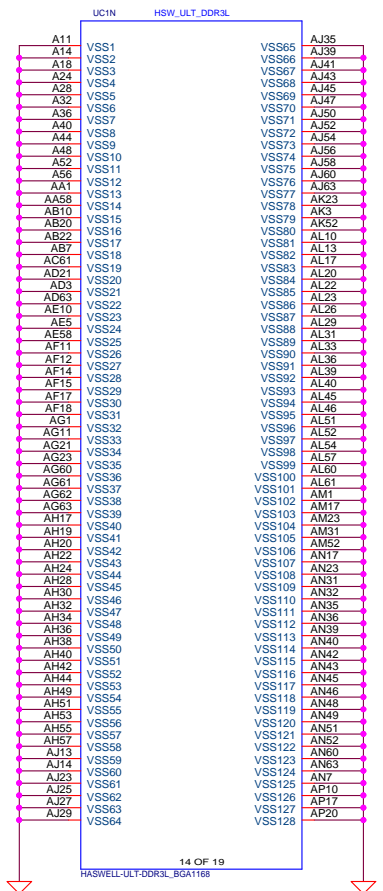
For RF

SVID
 1, Stripline Line, No More Than 6000Mil
 2, Alert# Route Between CLK and Data
 3, CLK Length < Data Length < CLK Length + 2000Mil
 4, Space at least 18Mil

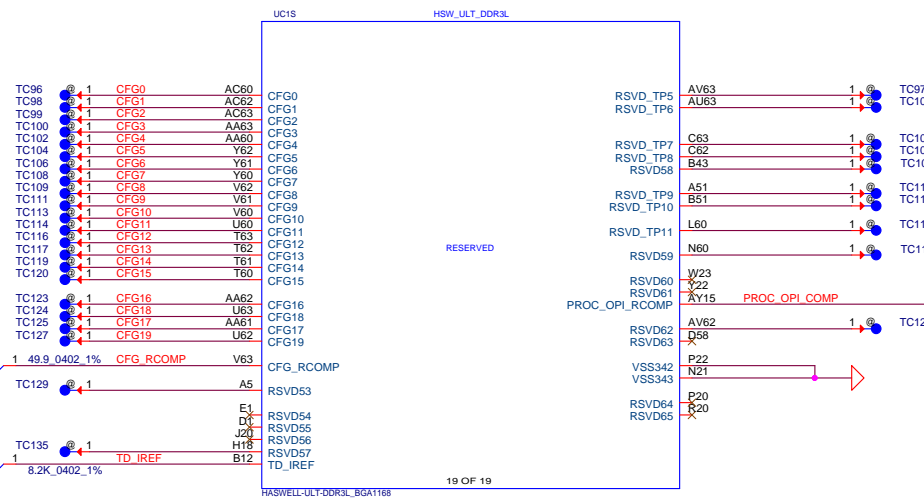
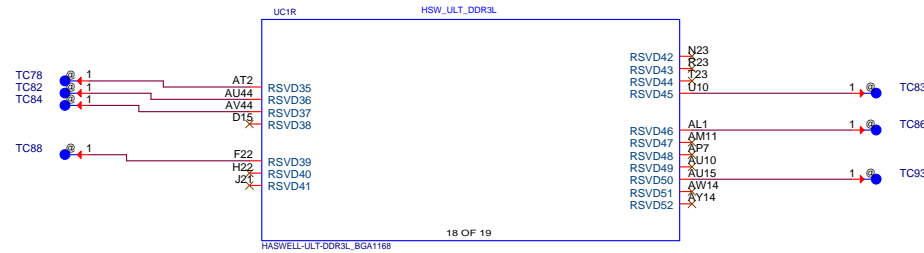
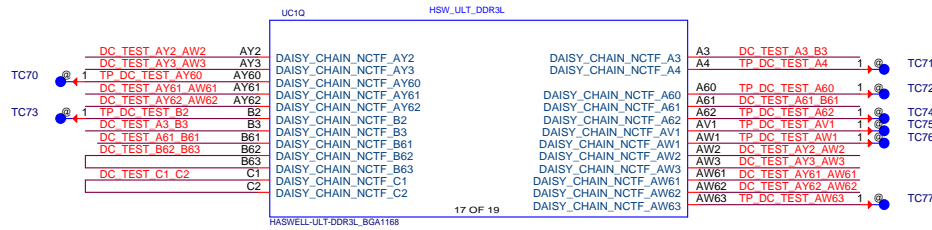




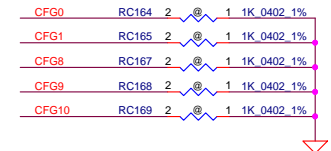
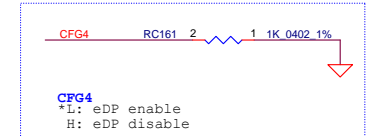
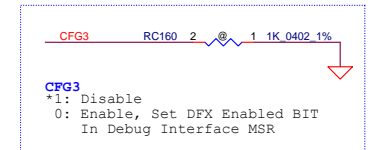
For Intel recommend, place one 0.47uF capacitor to address temporary inrush current. (DOC.489999)



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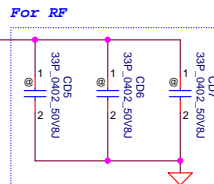
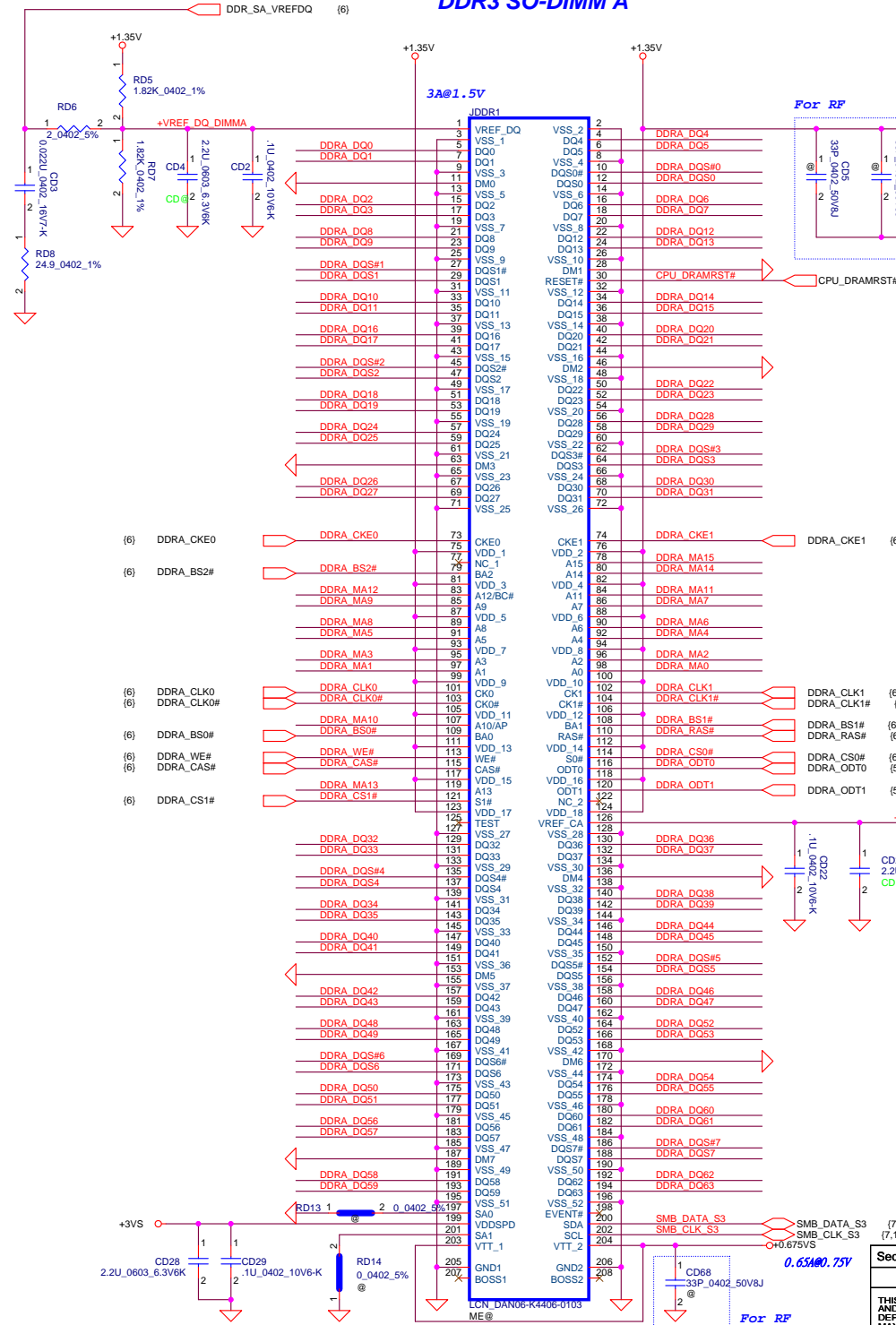
CFG_RCOMP&TD_IREF
Width 20Mil
Space 15Mil
Length 500Mil



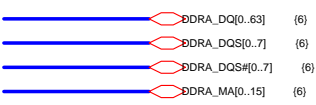
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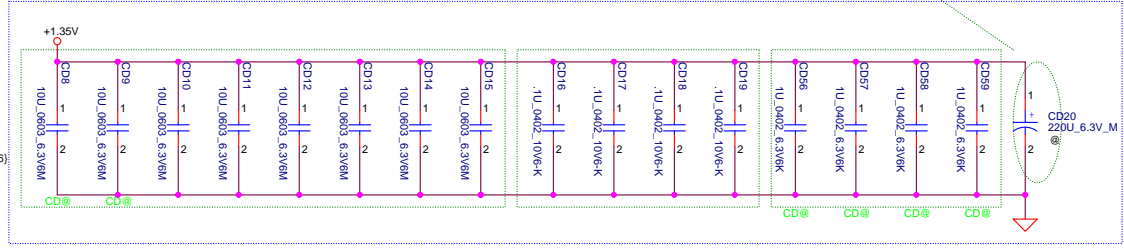
DDR3 SO-DIMM A



Layout Note:
Place near DIMM



OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF00002Y0J)
(10uF_0603_6.3V)*8
(1U_0402_6.3V)*4
(.1U_0402_10V6-K)*4

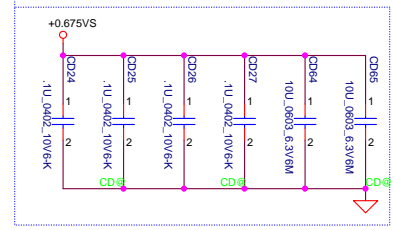


Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

Trace width:20 mils
Space:20mils

Layout Note:
Place near DIMM

(10U_0603_6.3V)*2
(.1U_0402_10V)*4

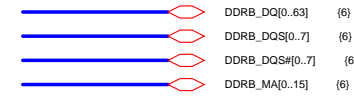


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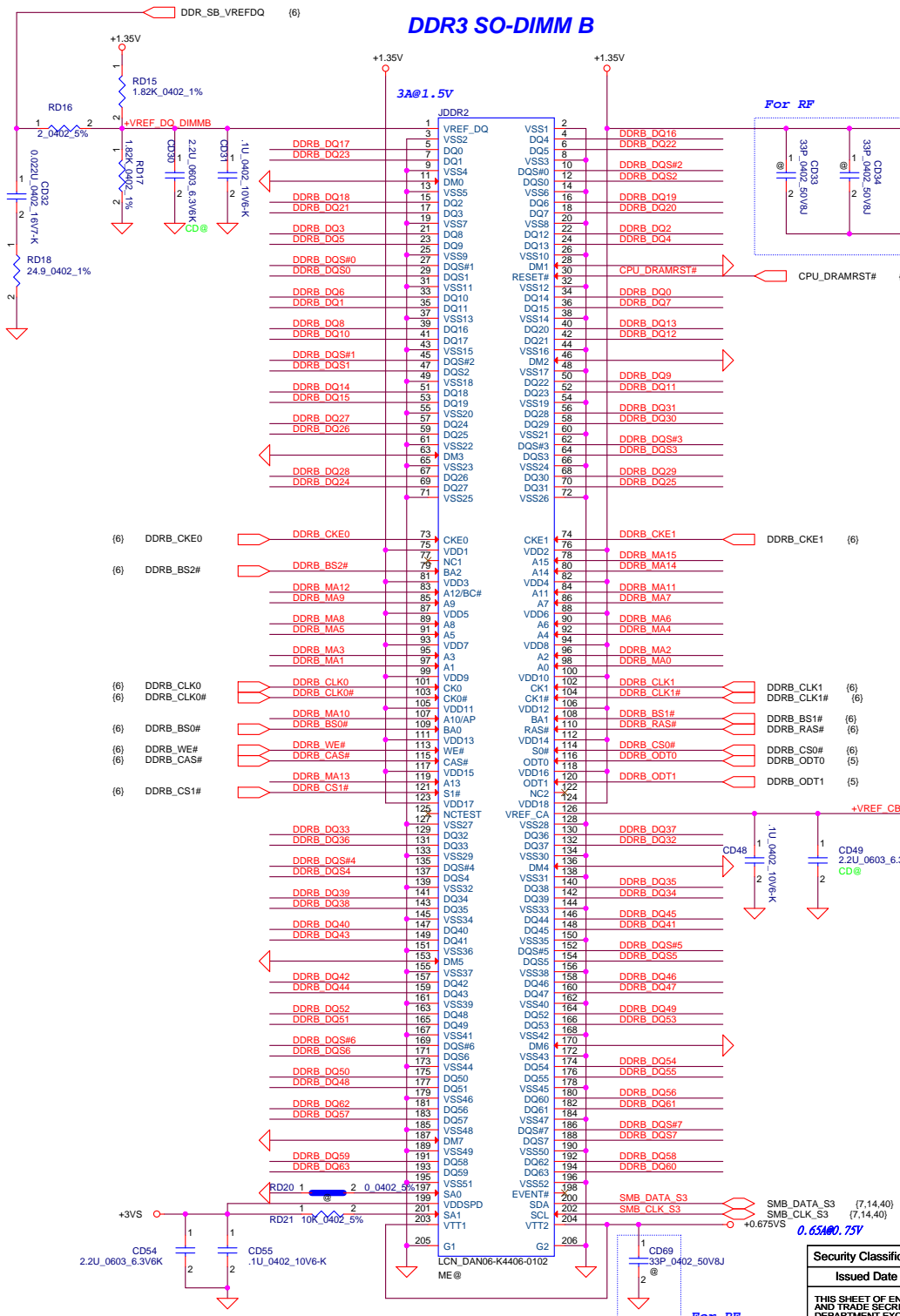
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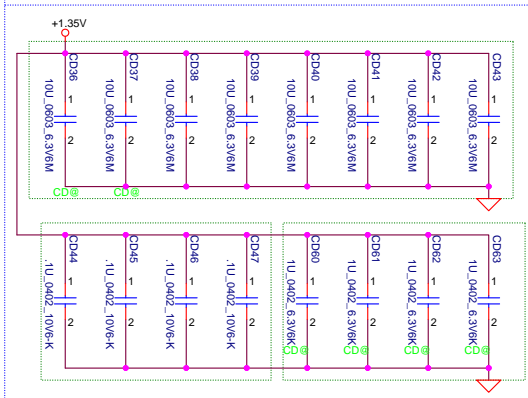


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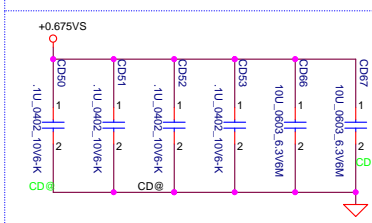
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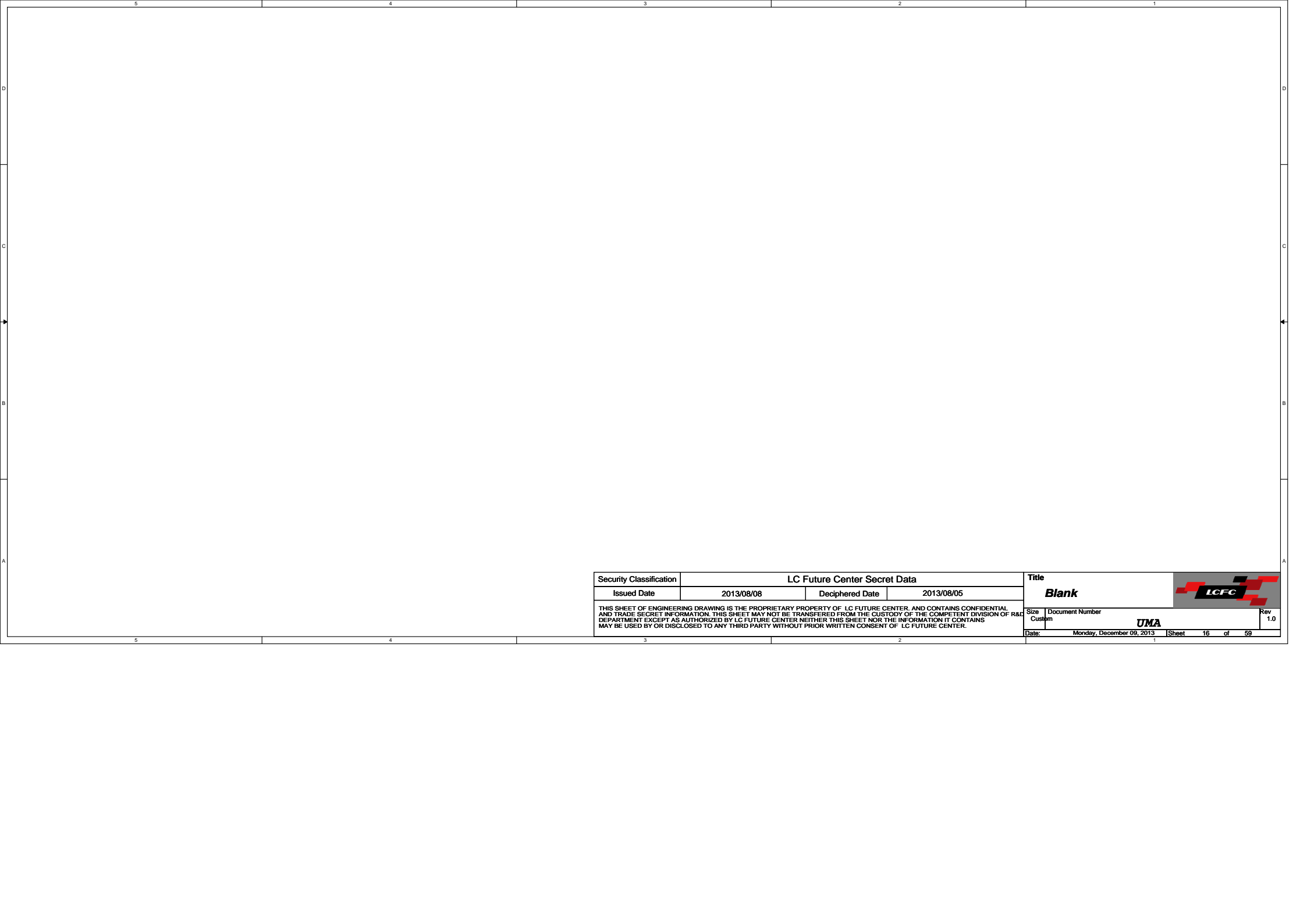
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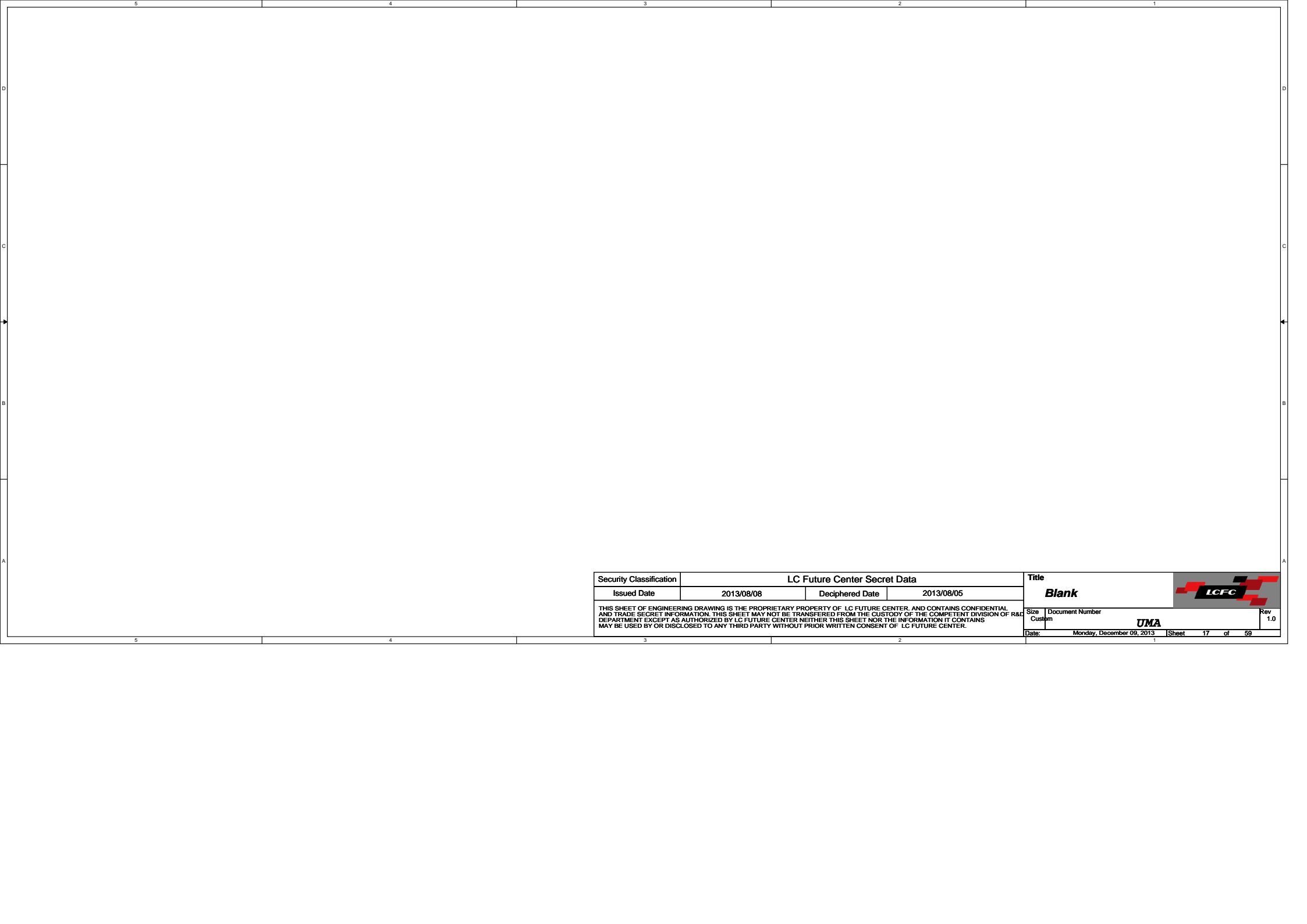



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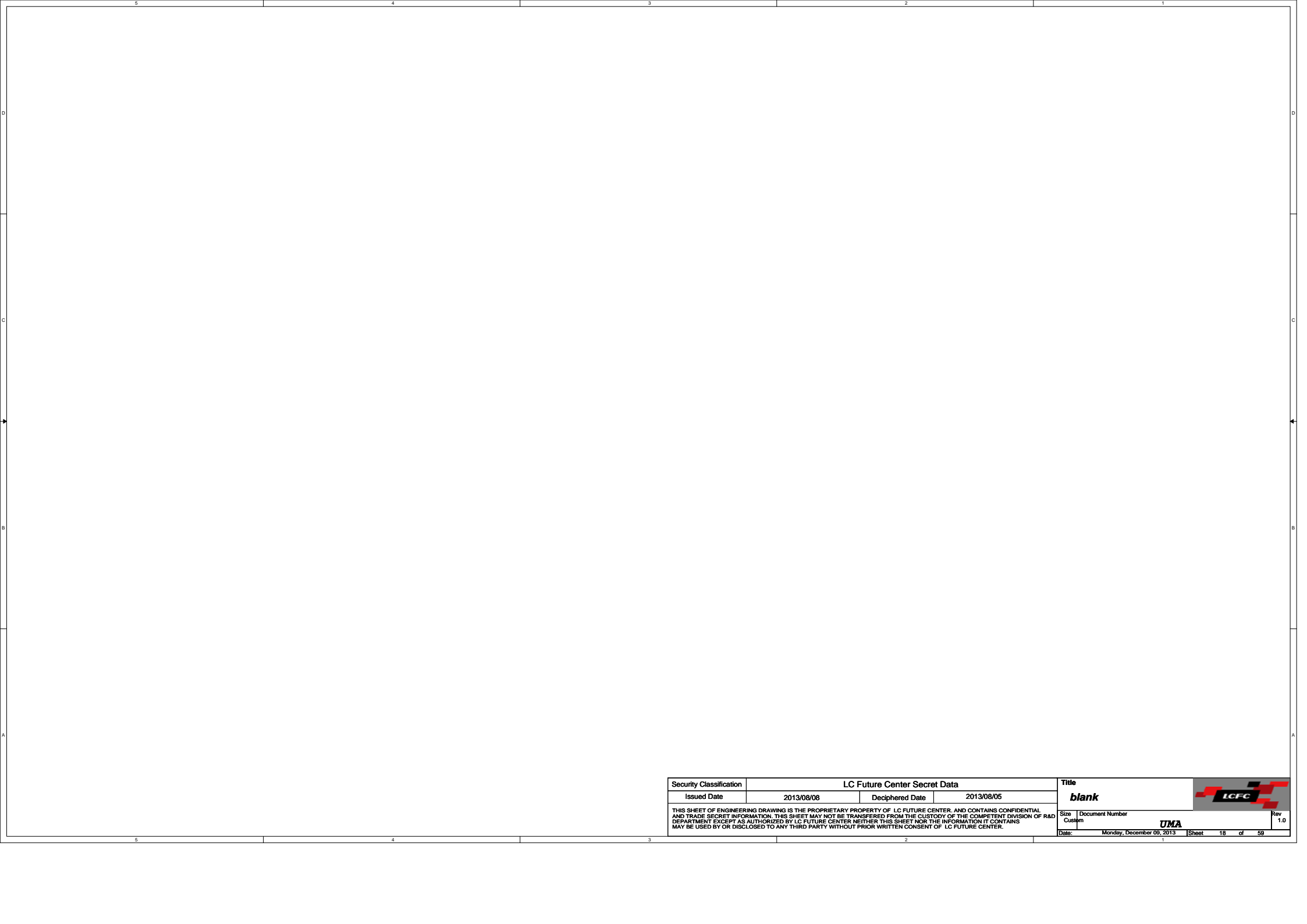
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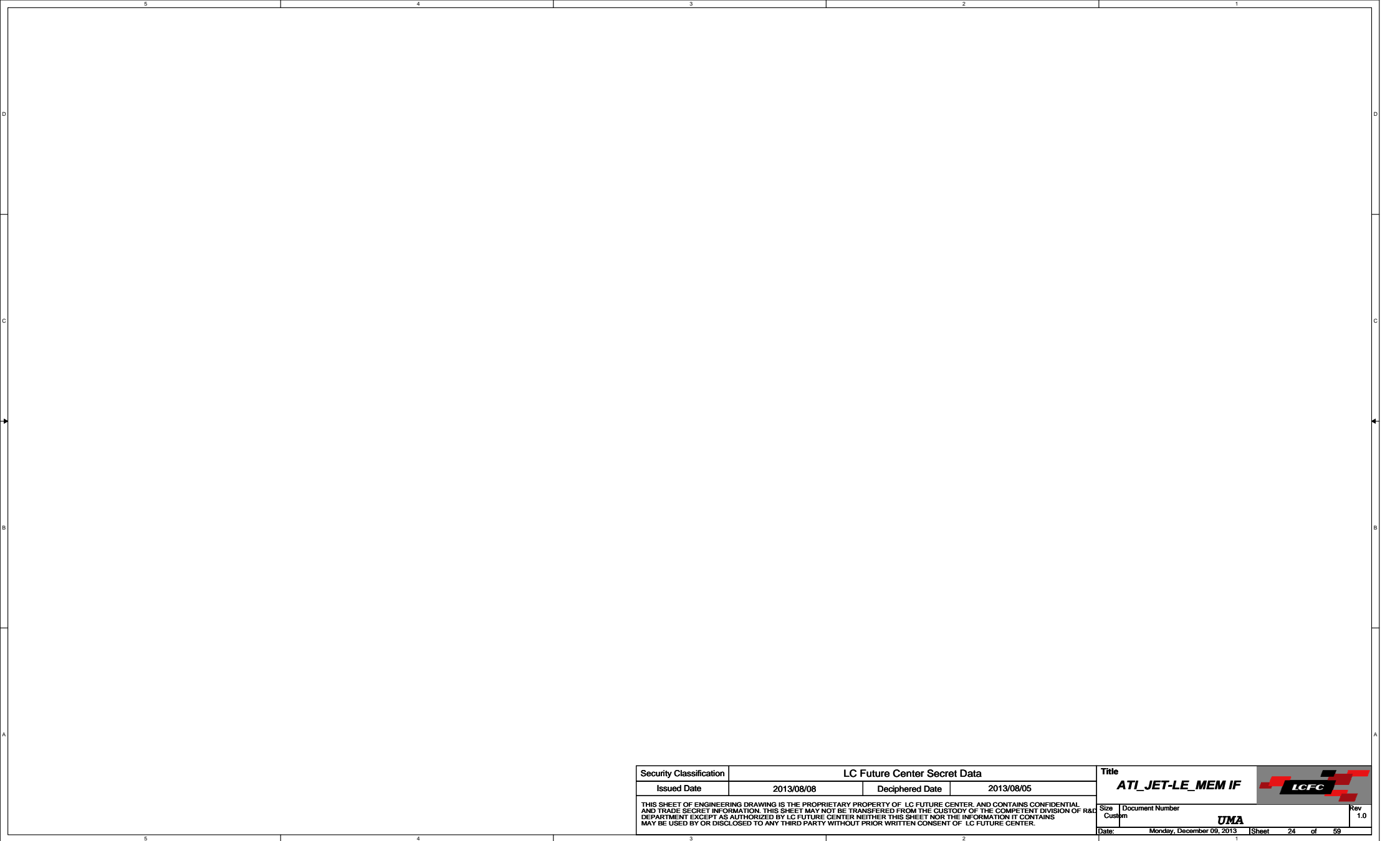
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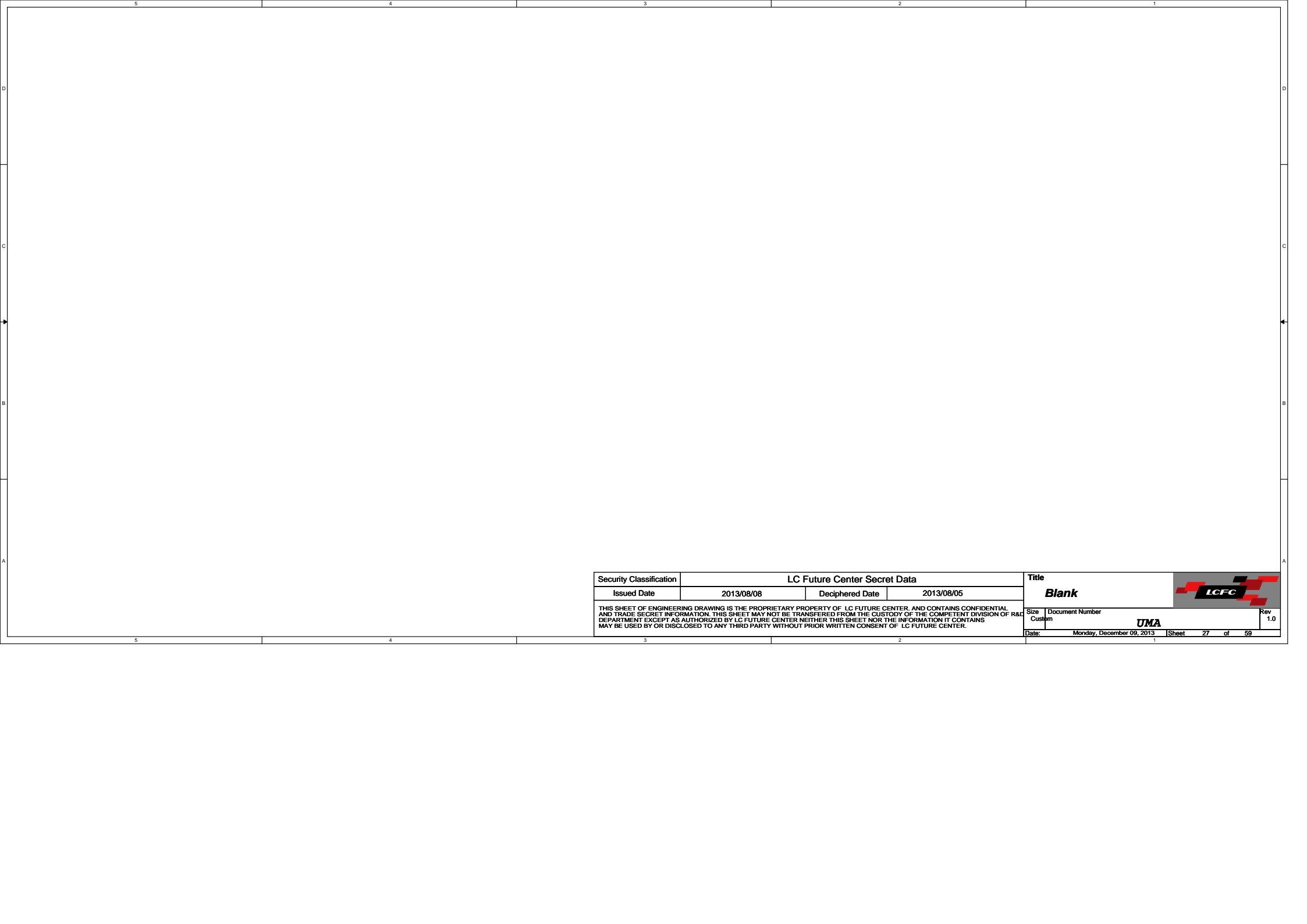
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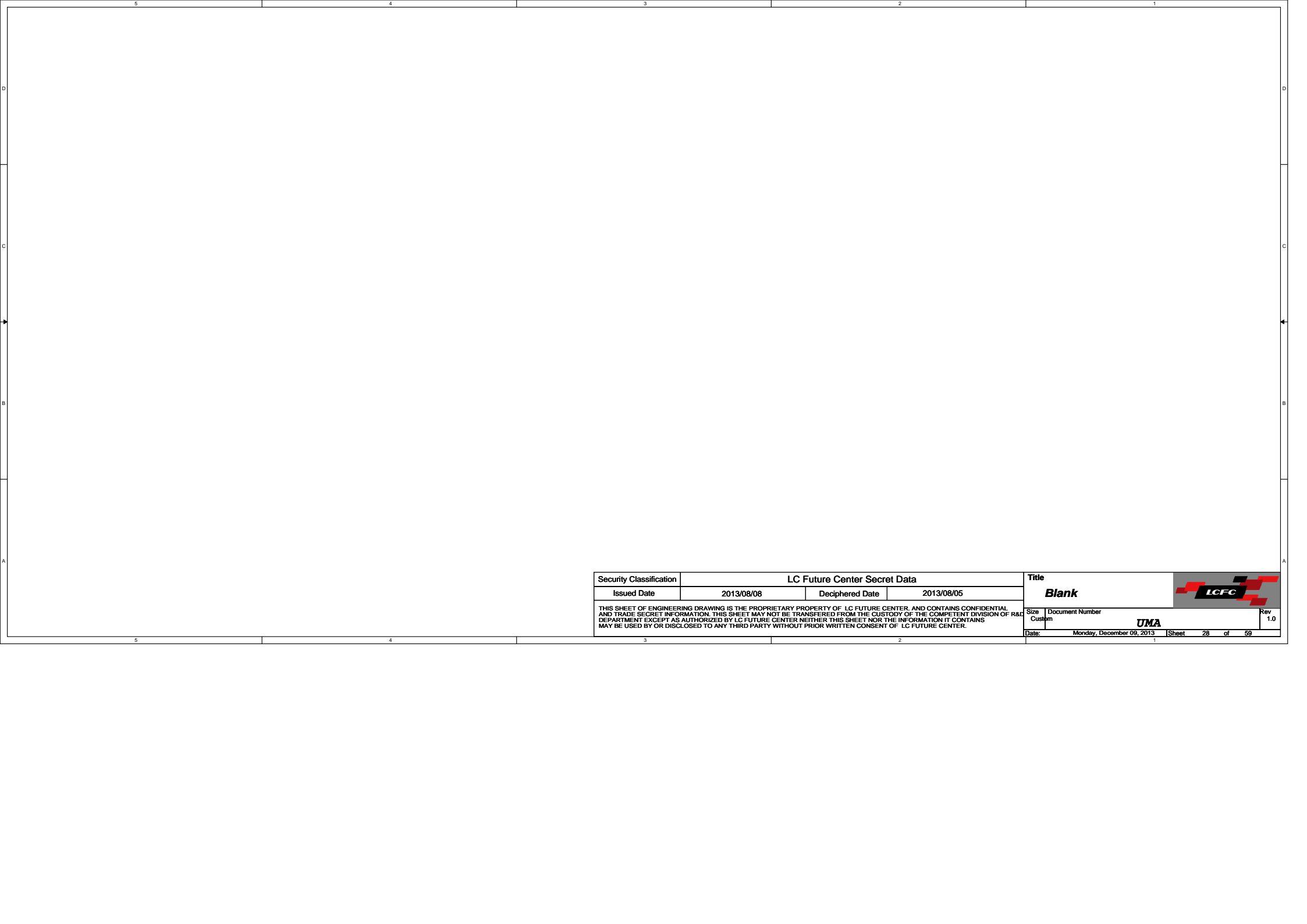
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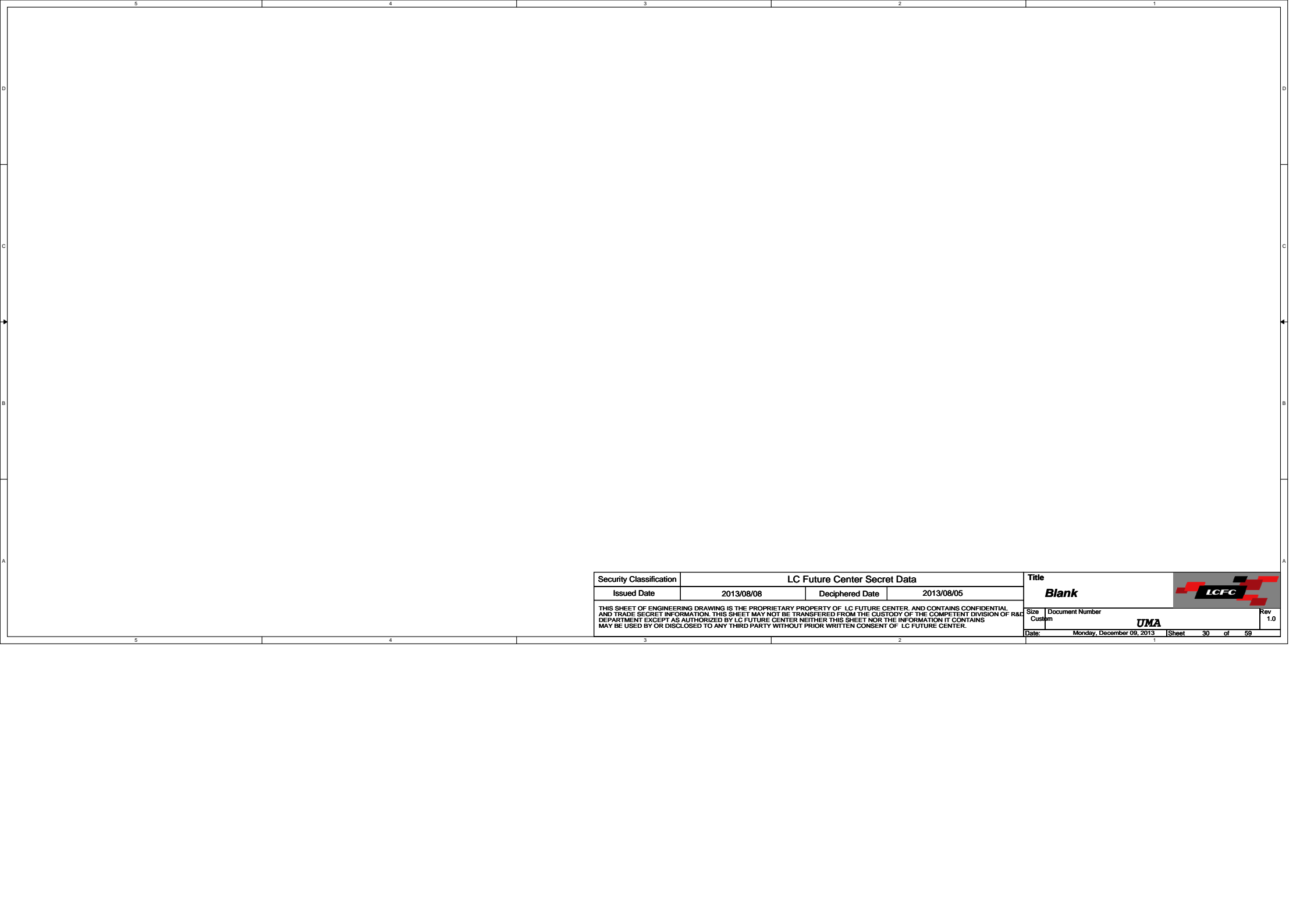
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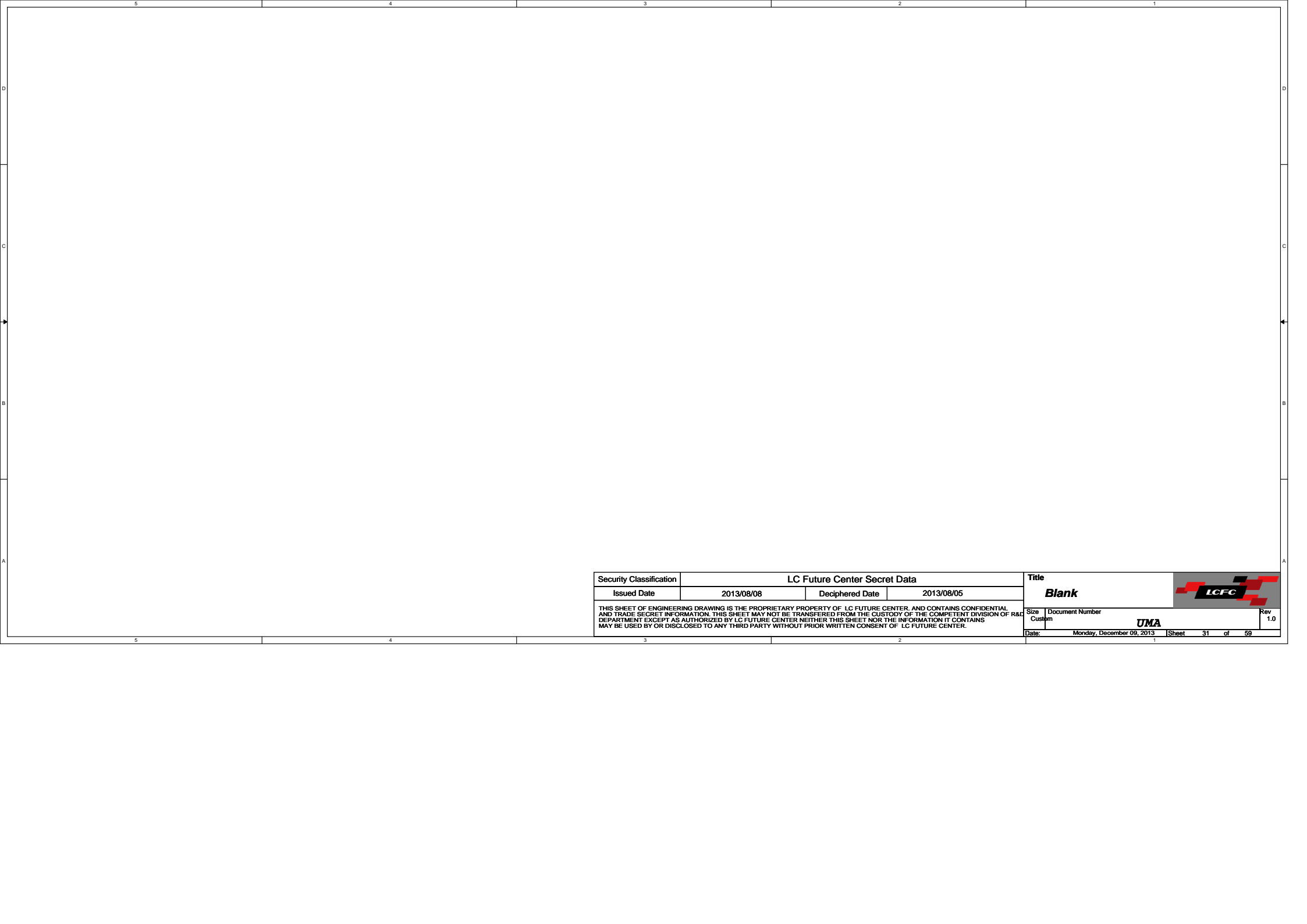
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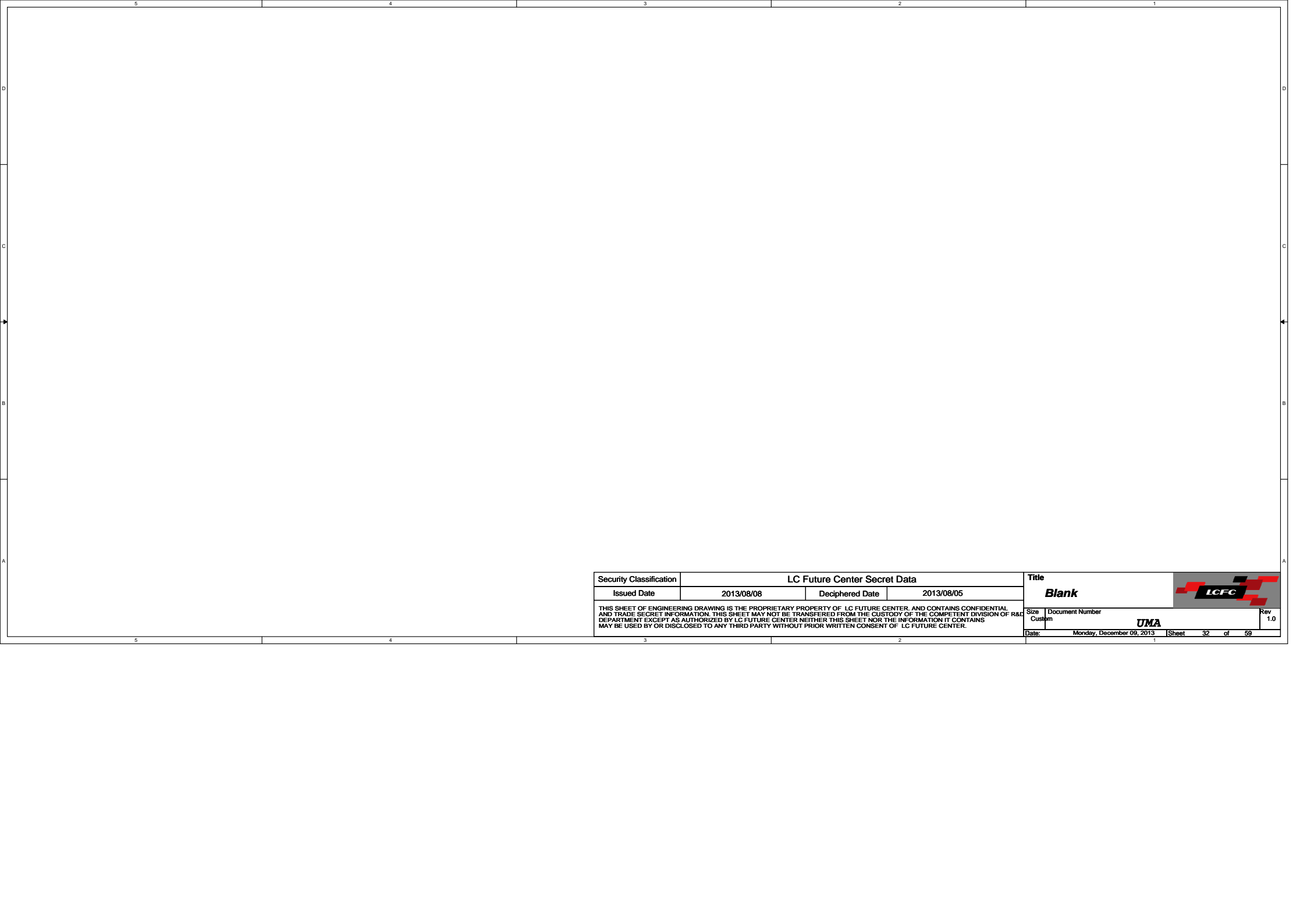
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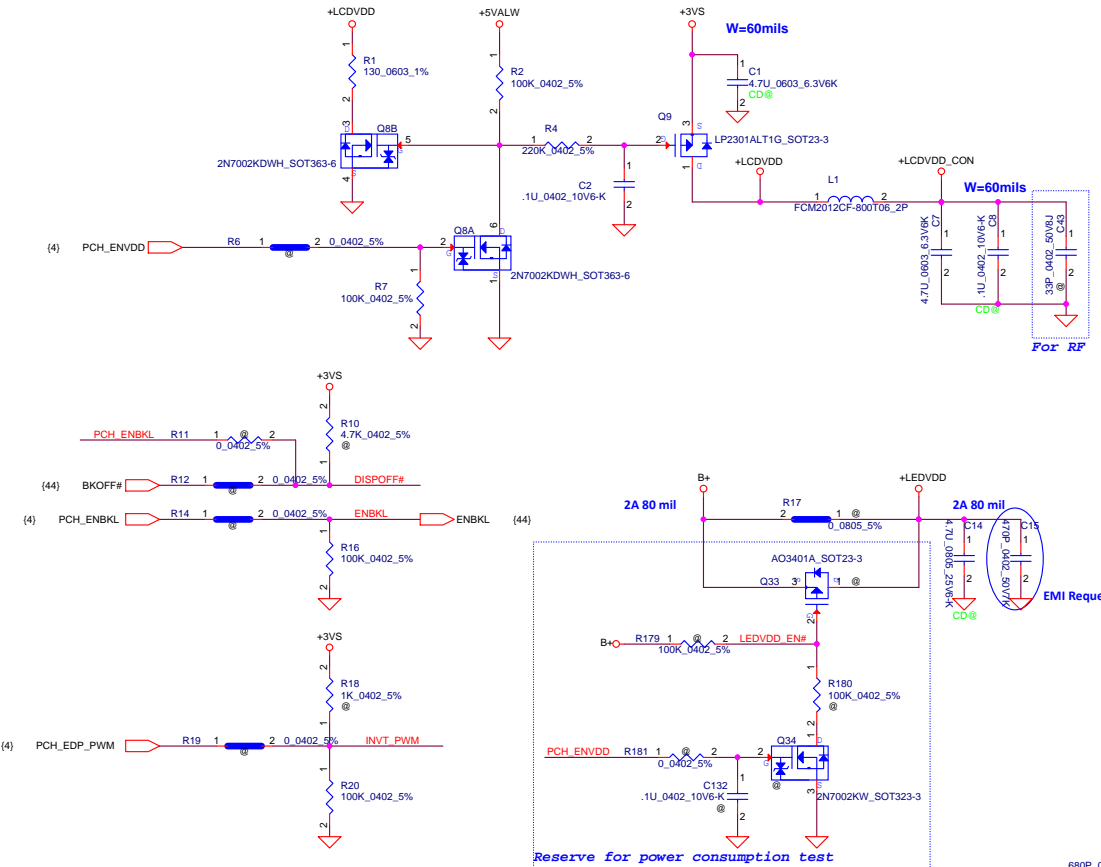
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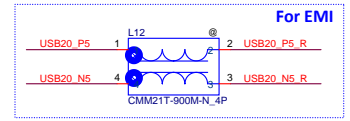
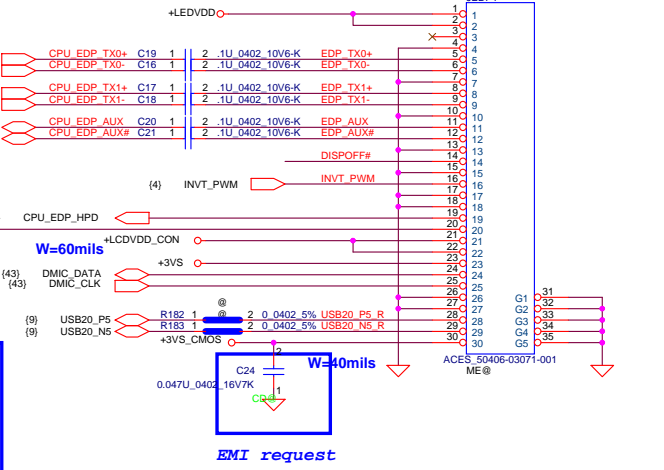
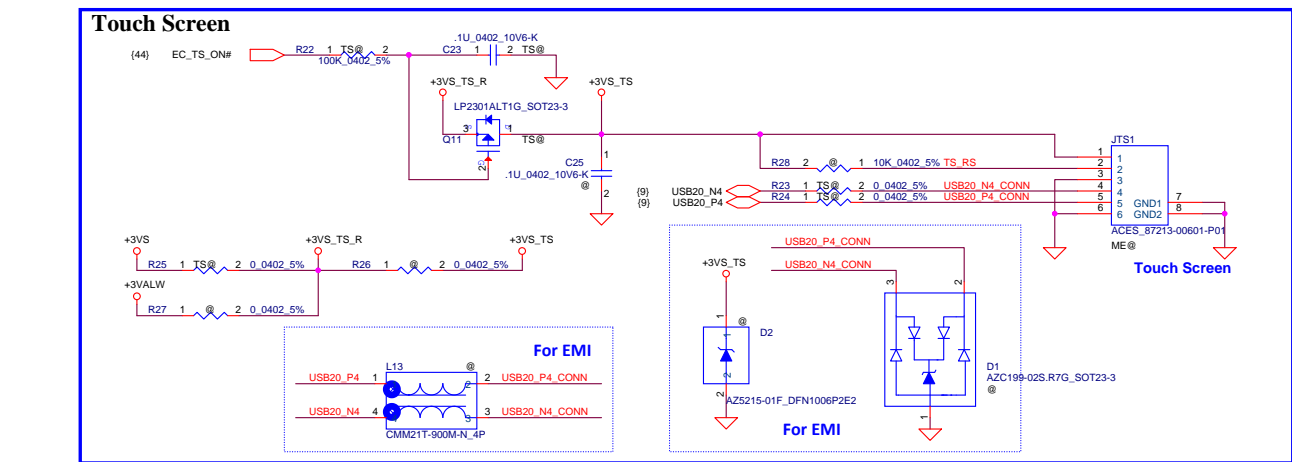
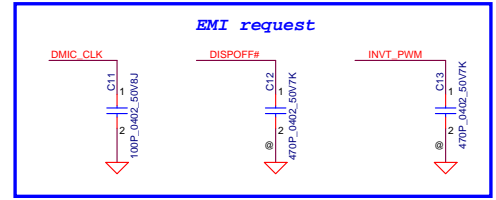
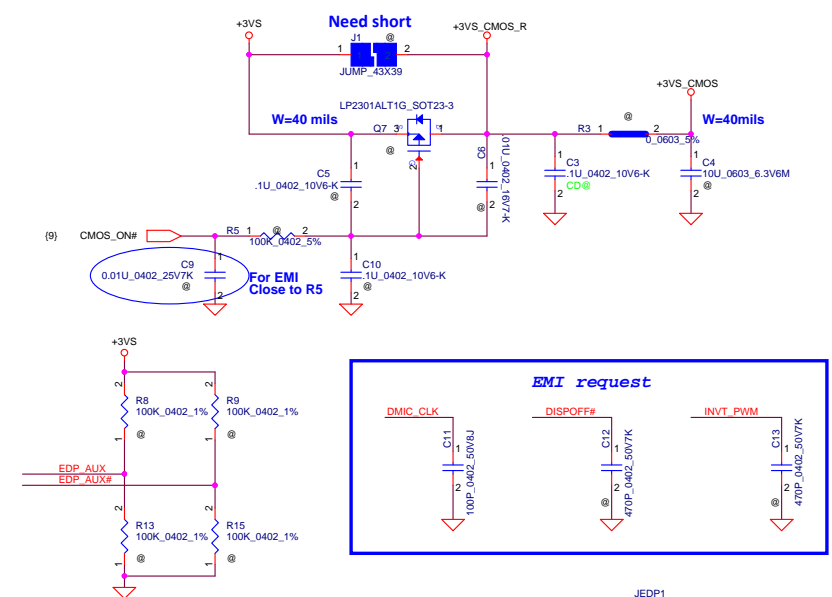
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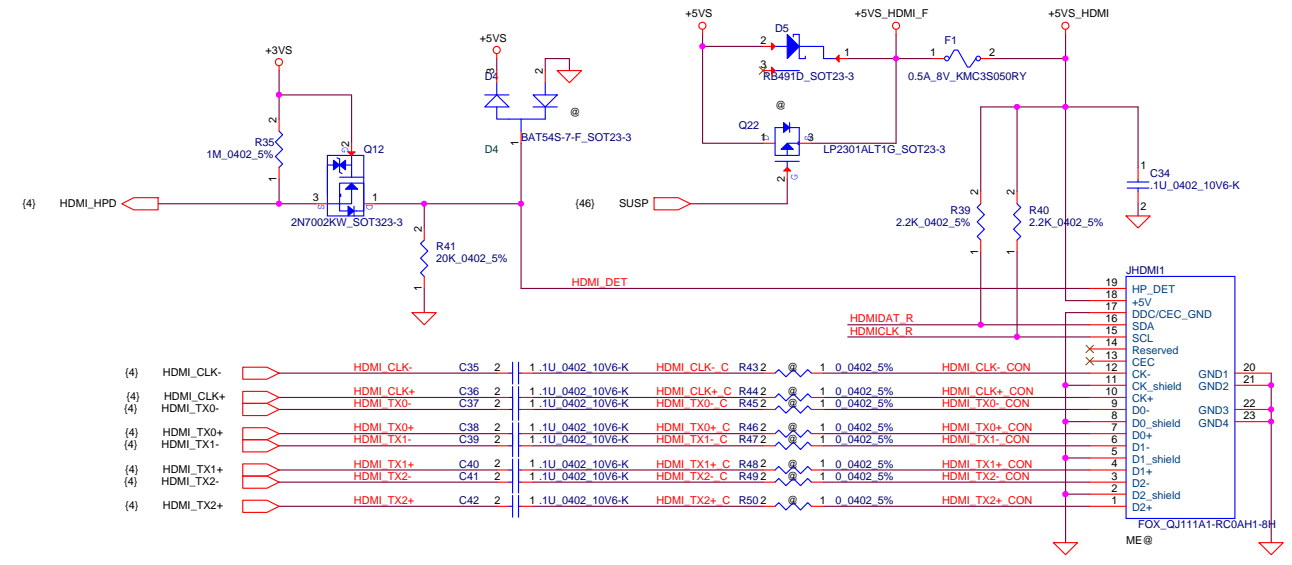
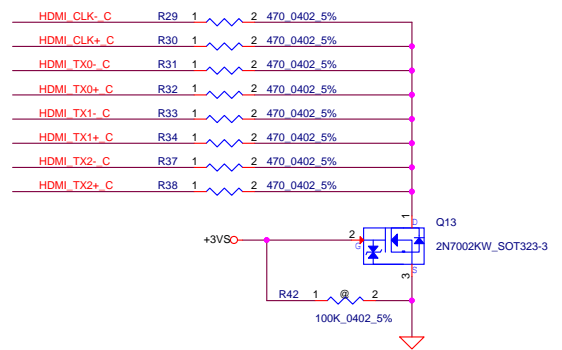
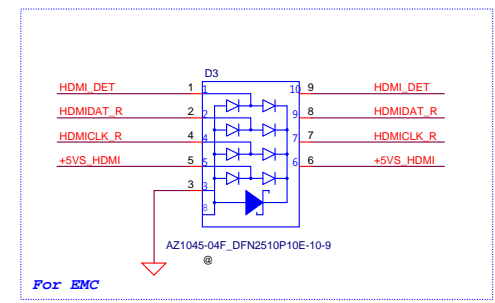
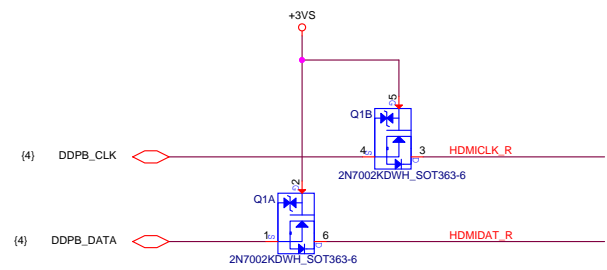
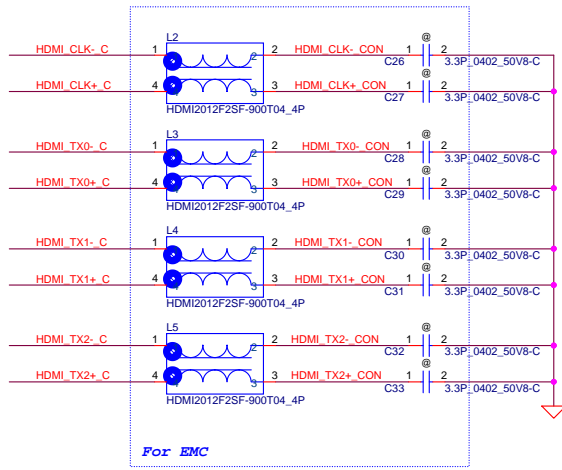
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LCD POWER CIRCUIT

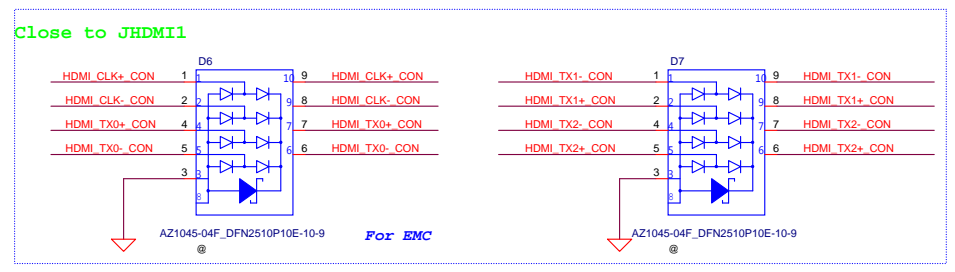


CMOS Camera



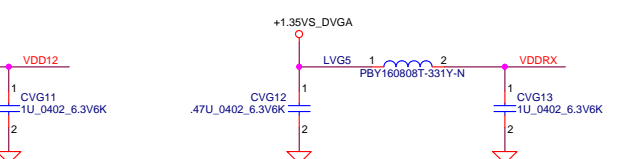
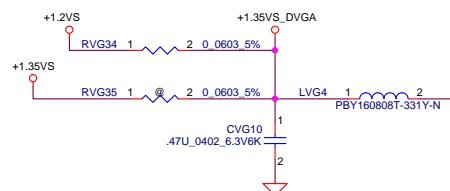
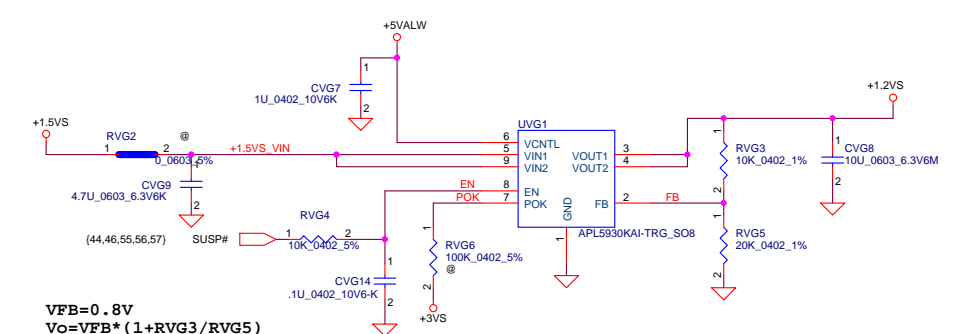
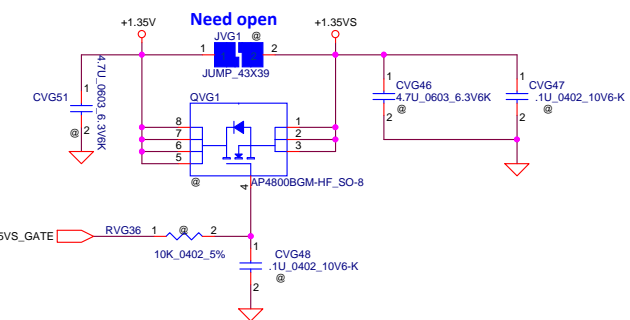
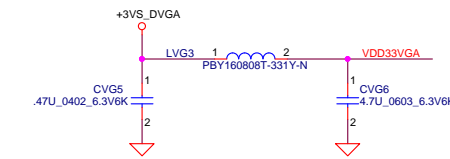
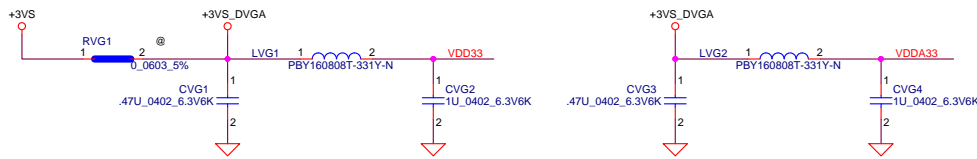


(4)	HDMI_CLK-	HDMI_CLK-	C35	2	1.1U_0402_10V6-K	HDMI_CLK- C	R43	2	1.0	0.402_5%	HDMI_CLK- CON	
(4)	HDMI_CLK+	HDMI_CLK+	C36	2	1.1U_0402_10V6-K	HDMI_CLK+ C	R44	2	1.0	0.402_5%	HDMI_CLK+ CON	
(4)	HDMI_TX0-	HDMI_TX0-	C37	2	1.1U_0402_10V6-K	HDMI_TX0- C	R45	2	1.0	0.402_5%	HDMI_TX0- CON	
(4)	HDMI_TX0+	HDMI_TX0+	C38	2	1.1U_0402_10V6-K	HDMI_TX0+ C	R46	2	1.0	0.402_5%	HDMI_TX0+ CON	
(4)	HDMI_TX1-	HDMI_TX1-	C39	2	1.1U_0402_10V6-K	HDMI_TX1- C	R47	2	1.0	0.402_5%	HDMI_TX1- CON	
(4)	HDMI_TX1+	HDMI_TX1+	C40	2	1.1U_0402_10V6-K	HDMI_TX1+ C	R48	2	1.0	0.402_5%	HDMI_TX1+ CON	
(4)	HDMI_TX2-	HDMI_TX2-	C41	2	1.1U_0402_10V6-K	HDMI_TX2- C	R49	2	1.0	0.402_5%	HDMI_TX2- CON	
(4)	HDMI_TX2+	HDMI_TX2+	C42	2	1.1U_0402_10V6-K	HDMI_TX2+ C	R50	2	1.0	0.402_5%	HDMI_TX2+ CON	



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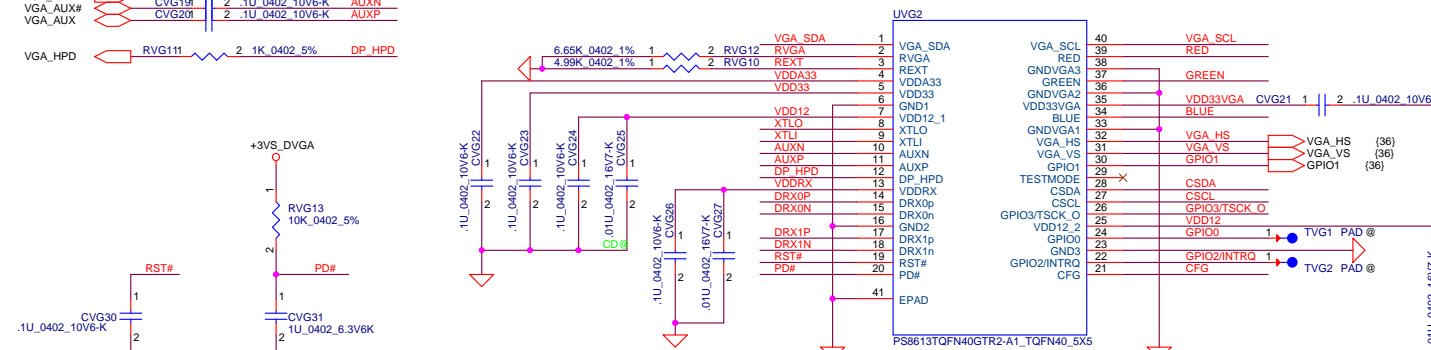
Title	
HDMI_CONN	
Size	Document Number
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Sheet	34 of 59
Rev	1.0



VFB=0.8V
 $V_o = VFB * (1 + RVG3 / RVG5)$
 OCP:Min 4A

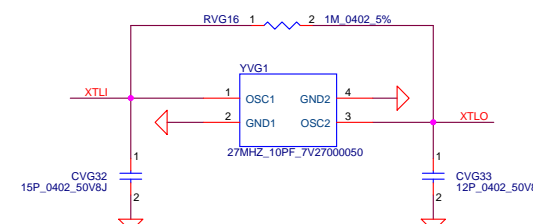
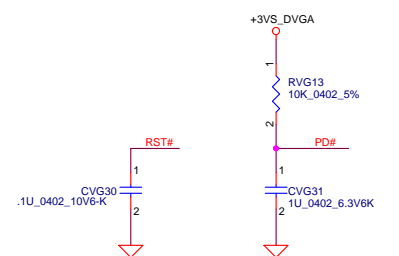
- (4) VGA_TX0- CVG151 2 .1U_0402_10V6-K DRX0N
- (4) VGA_TX0+ CVG152 2 .1U_0402_10V6-K DRX0P
- (4) VGA_TX1- CVG171 2 .1U_0402_10V6-K DRX1N
- (4) VGA_TX1+ CVG172 2 .1U_0402_10V6-K DRX1P
- (4) VGA_AUX# CVG191 2 .1U_0402_10V6-K AUXN
- (4) VGA_AUX CVG201 2 .1U_0402_10V6-K AUXP

- (4) VGA_HP# RVG111 2 1K_0402_5% DP_HP#



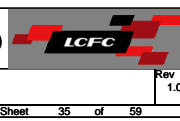
Initial code loading selection, internal pull down ~80kΩ:
 L: Loading initial code from internal MTP ROM
 H: No initial code loading, external I2C control is expected

I2C address, 3-state inputs:
 L: 0x50h ~ 0x6Fh
 M: 0x90h ~ 0xAfh
 H: 0x30h ~ 0x4Fh

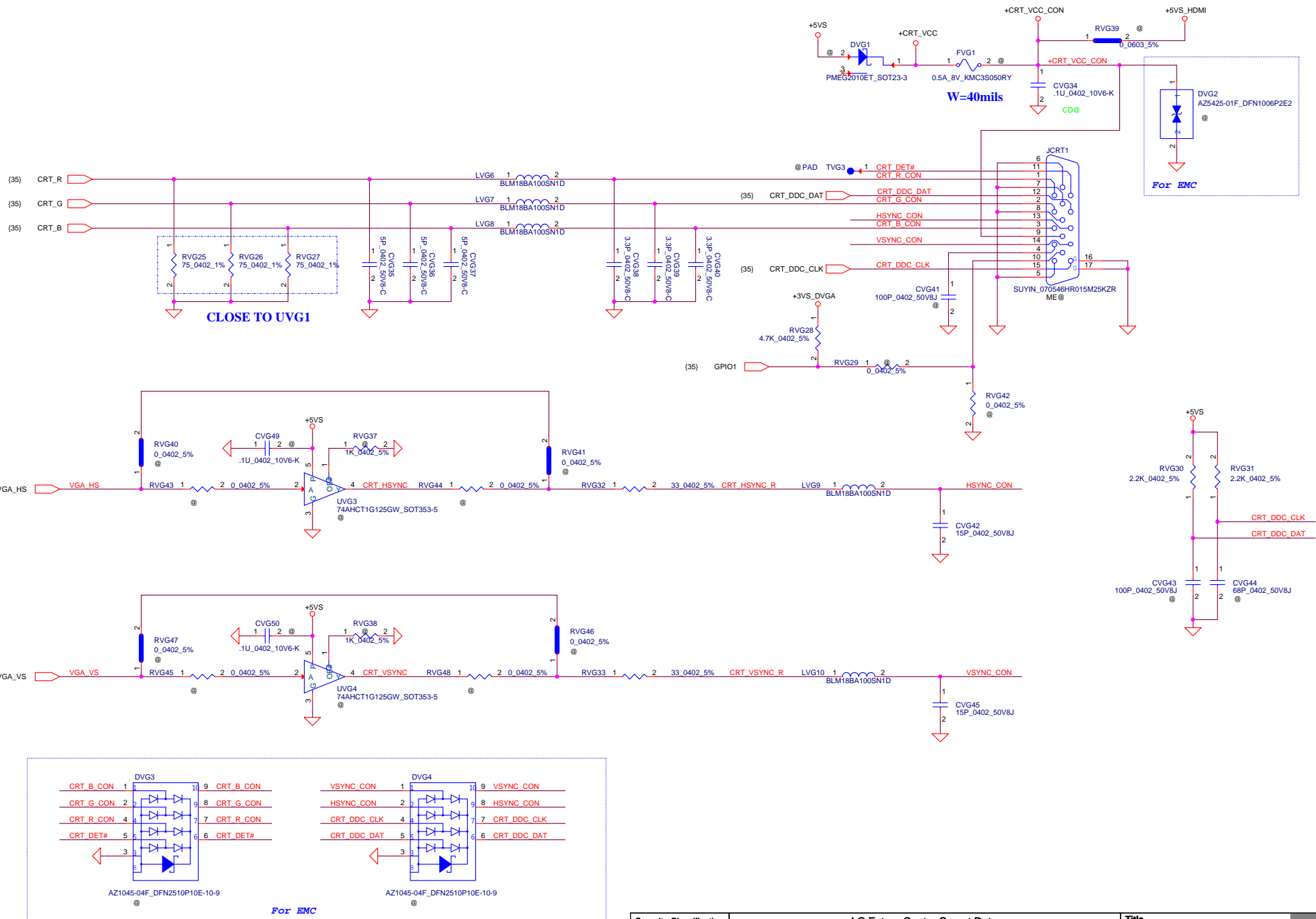


- RED RVG17 1 2 10_0402_5% CRT_R (36)
- GREEN RVG18 1 2 10_0402_5% CRT_G (36)
- BLUE RVG20 1 2 10_0402_5% CRT_B (36)
- VGA_SCL RVG231 2 0_0402_5% CRT_DDC_CLK (36)
- VGA_SDA RVG241 2 0_0402_5% CRT_DDC_DAT (36)

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CRT Connector



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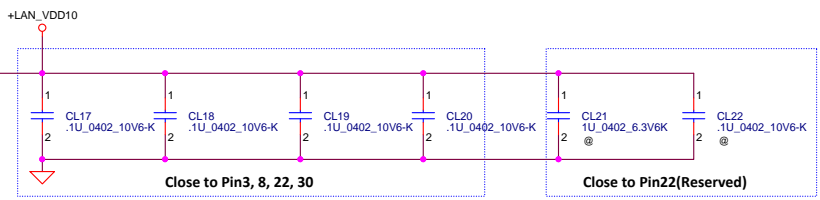
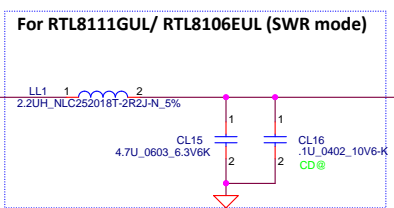
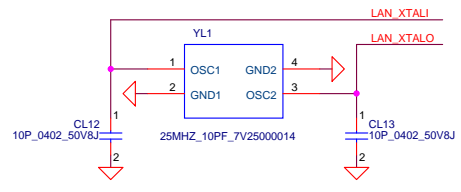
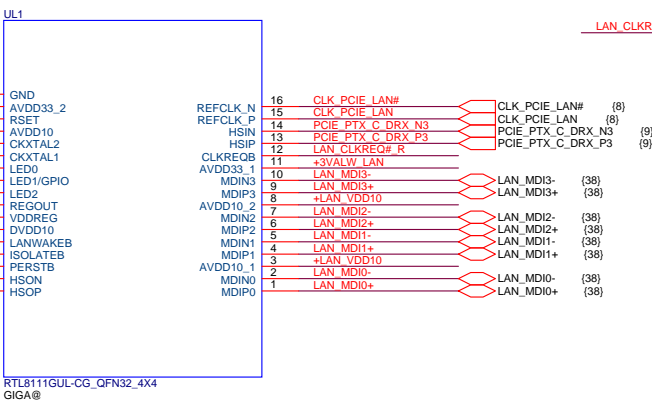
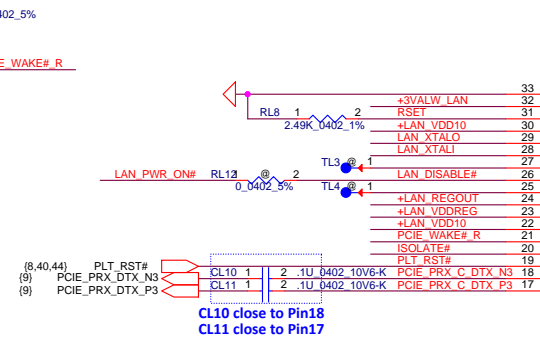
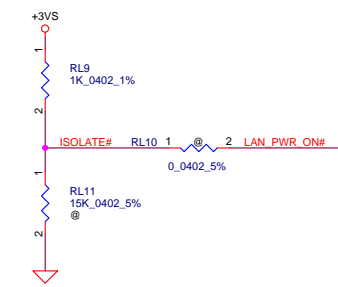
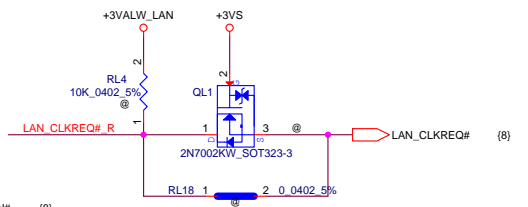
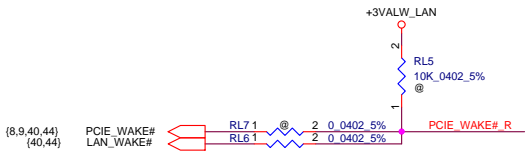
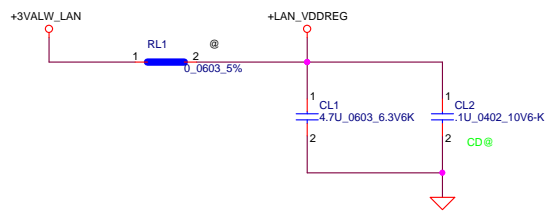
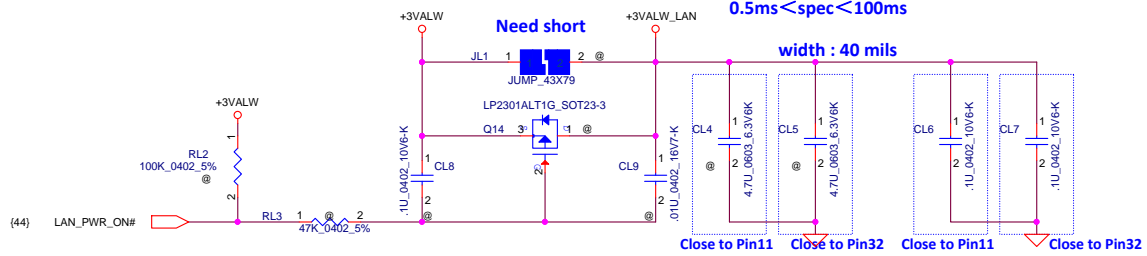
Title		Rev	
CRT		1.0	
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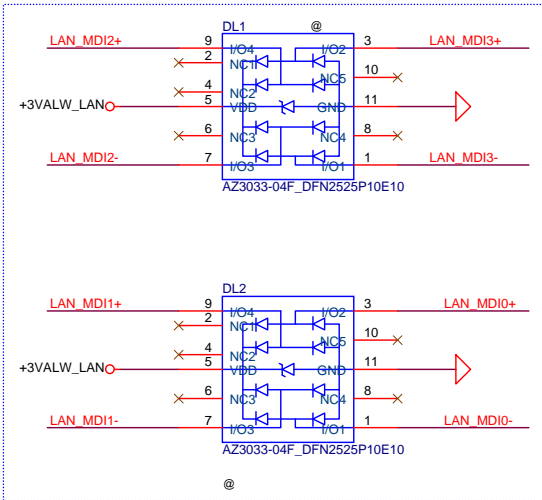
+3VALW TO +3VALW_LAN

**+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100ms**

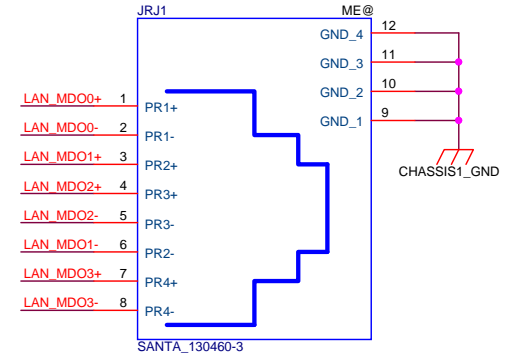
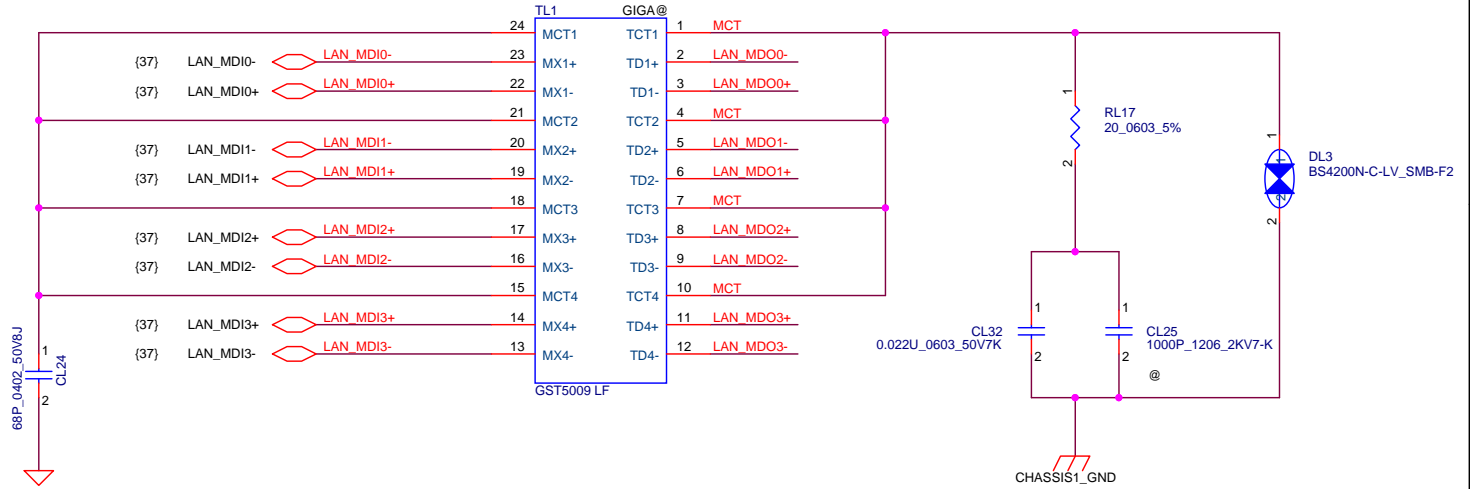
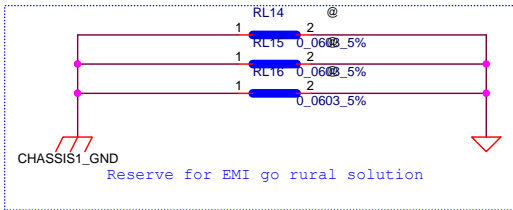


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DL1/DL2
1'S PN:SC300003M00

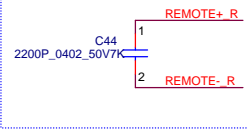


Place Close to TL1

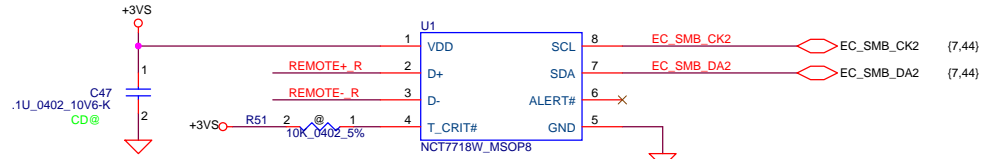


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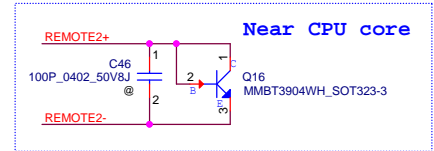
Close to U1



SMSC thermal sensor placed near DIMM



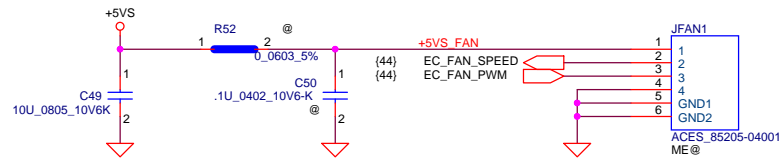
Address 1001_100xb



REMOTE2+ R176 1 @ 2 0.0402_5% REMOTE+_R
 REMOTE2- R177 1 @ 2 0.0402_5% REMOTE-_R

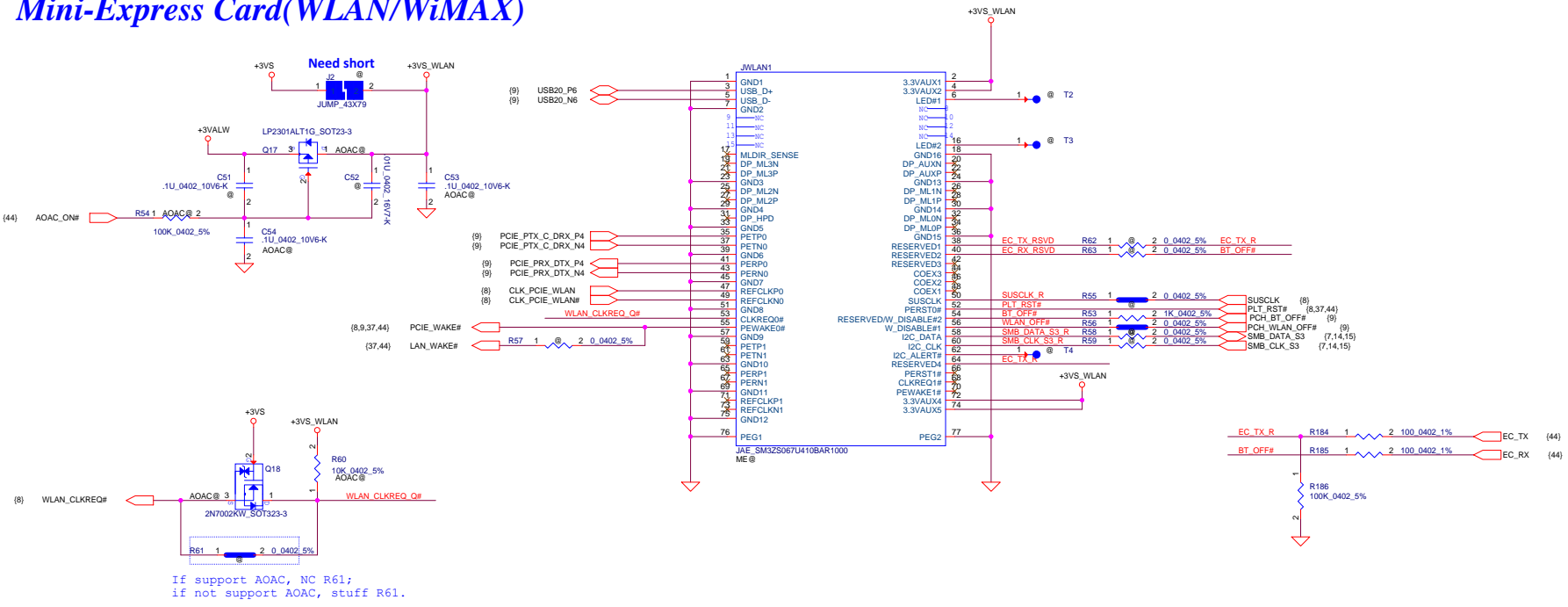
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
 Trace width/space:10/10 mil
 Trace length:<8"

FAN Conn

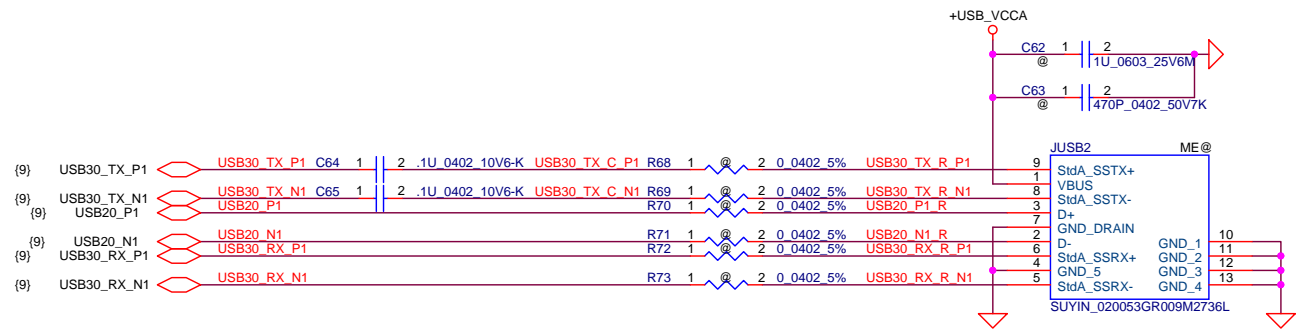
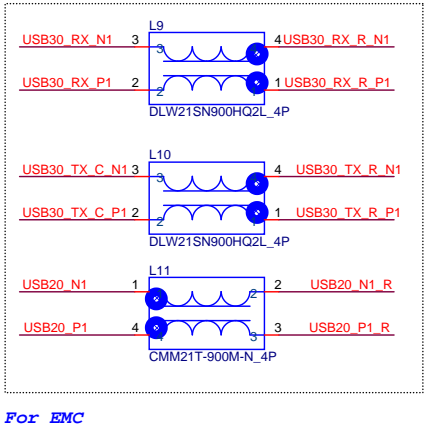
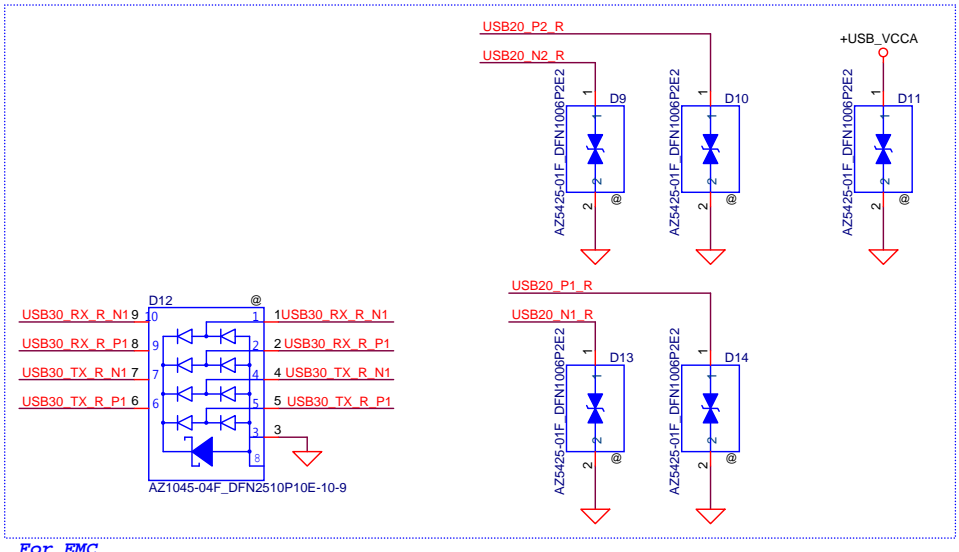
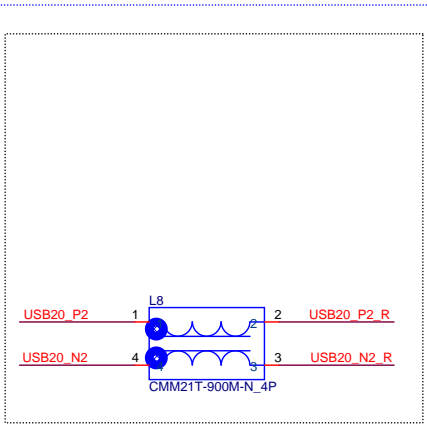
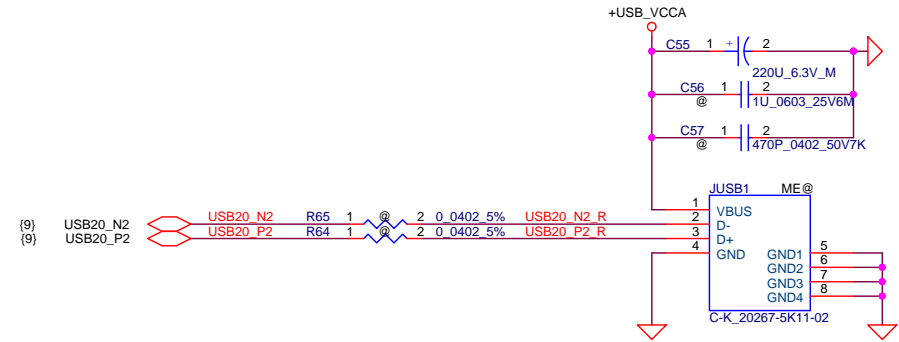
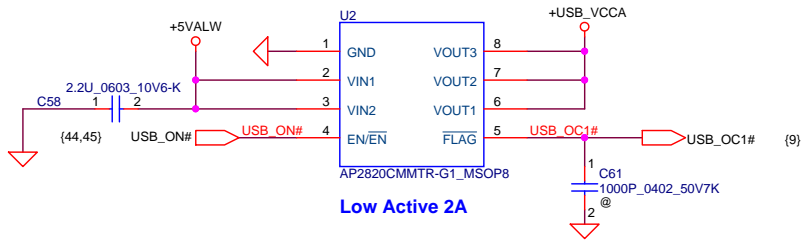


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Mini-Express Card(WLAN/WiMAX)

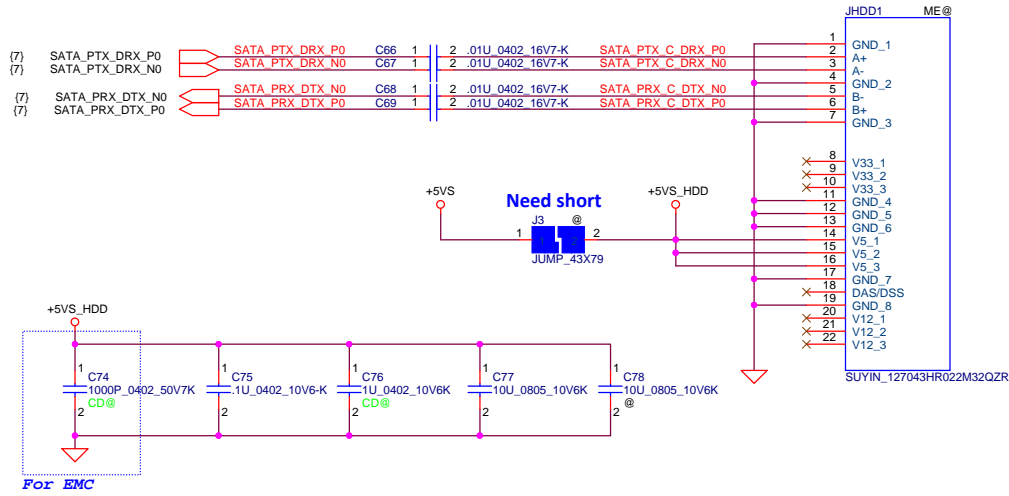


LEFT SIDE USB3.0 PORT X2

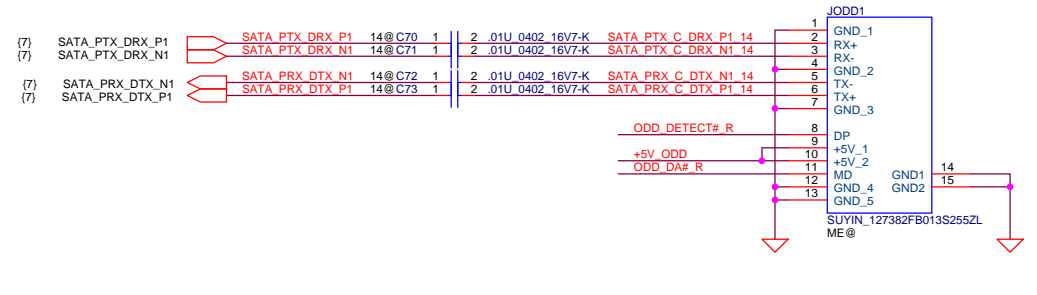


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Issued Date				2013/08/08		Deciphered Date		2013/08/05		USB2.0/USB3.0 PORT (LEFT)					
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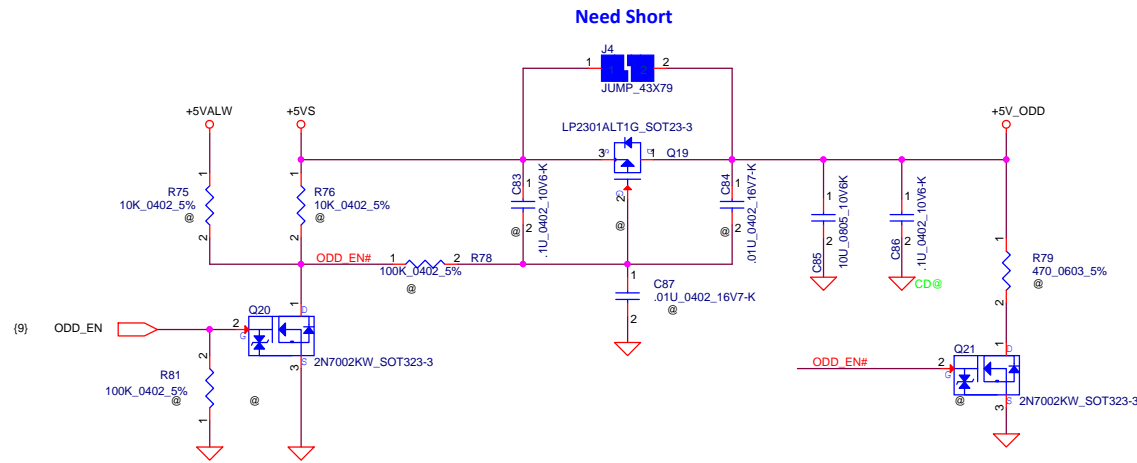
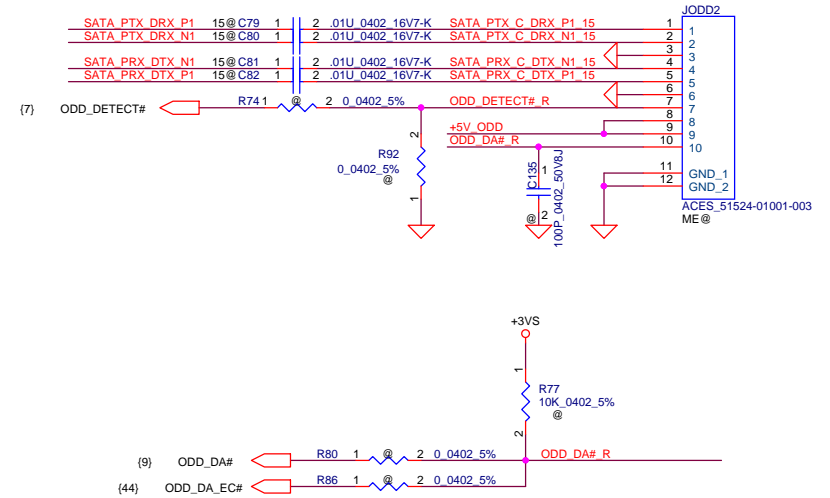
SATA HDD Conn.



FOR 14" SATA ODD Conn.

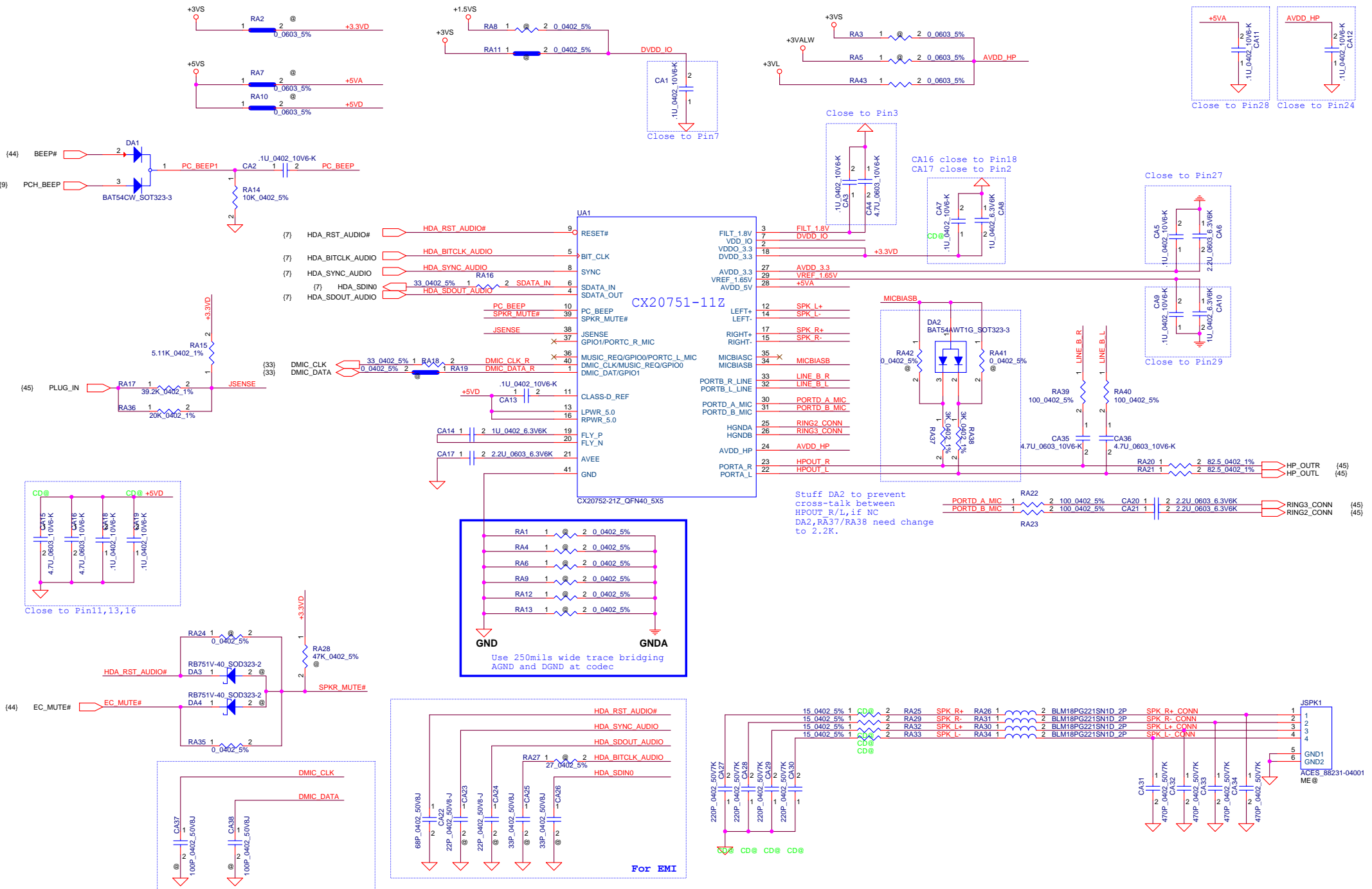


FOR 15" SATA ODD FFC Conn



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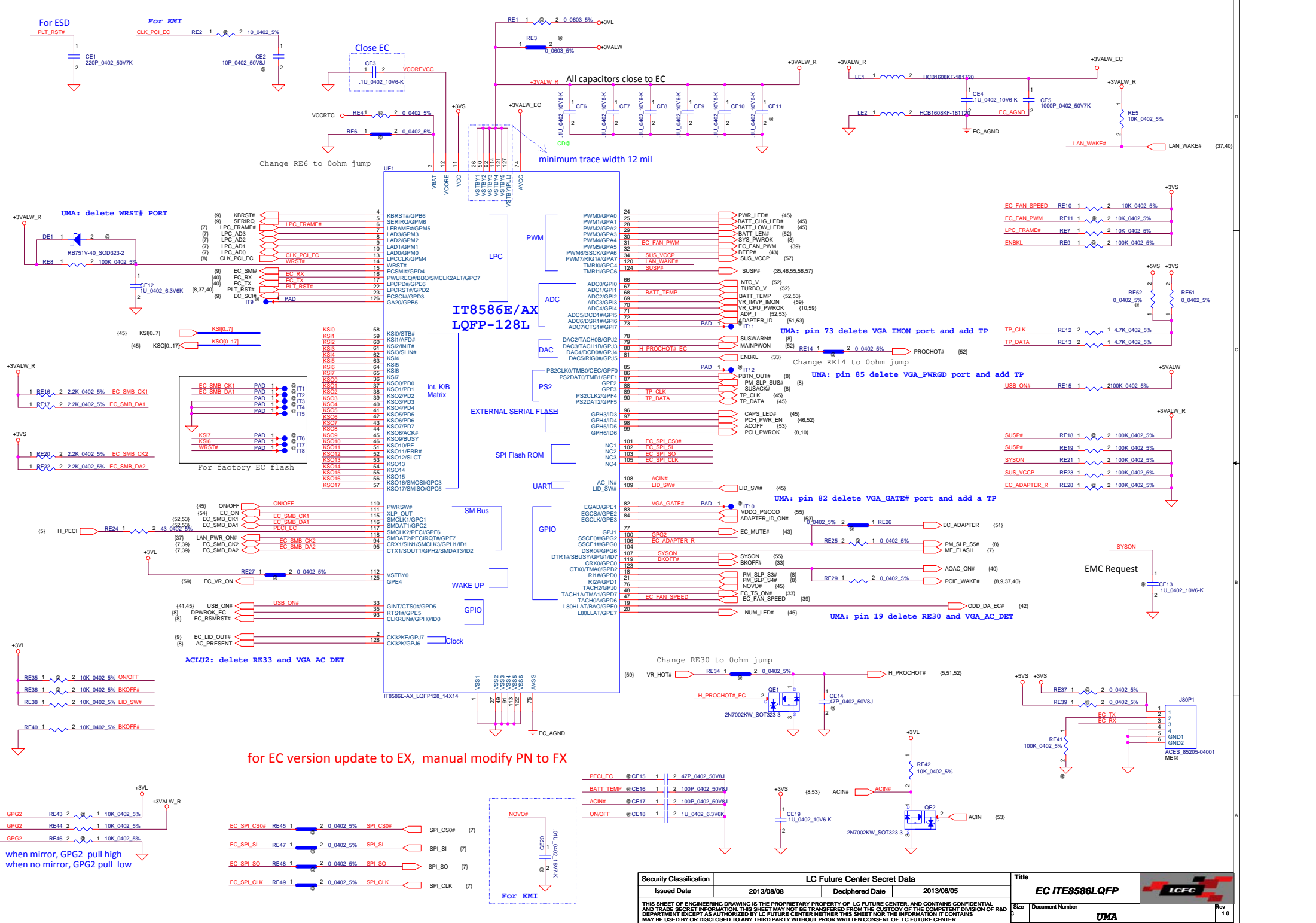
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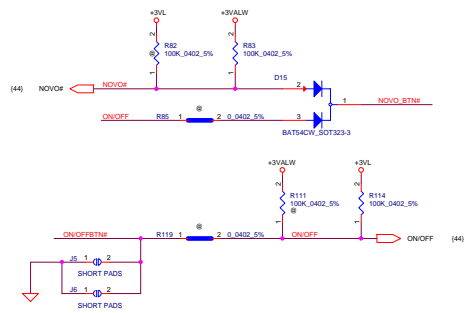
Title		Codec_CX20752	
Document Number	UMA	Rev	1.0
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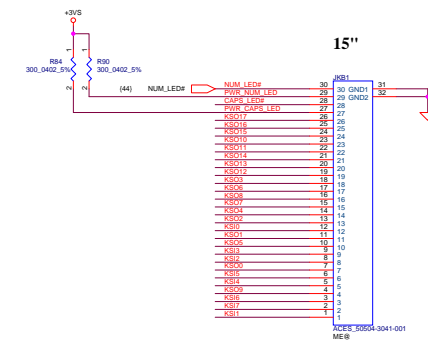
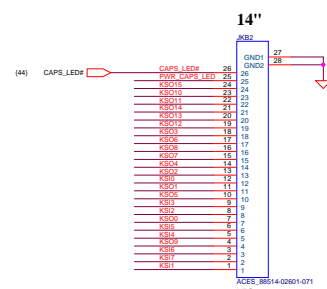
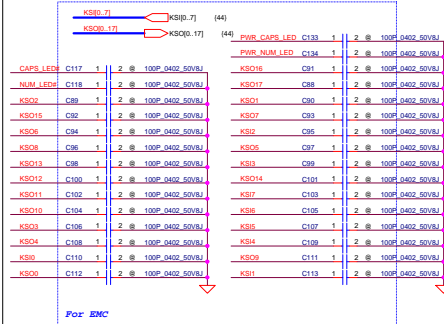
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	EC ITE8586LQFP	
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ON/OFF switch

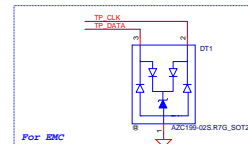
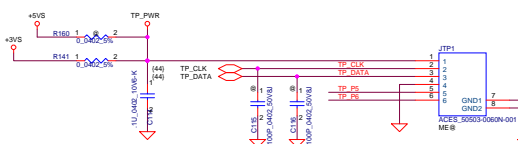


TP/B Connector

K/B Connector

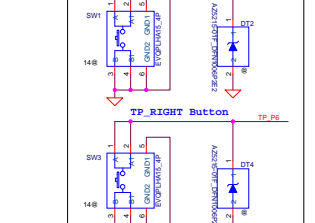


	14"	15"
KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS15_14	KS10_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS10_14	KS03_15
KB_13	KS02_14	KS02_15
KB_14	KS04_14	KS01_15
KB_15	KS07_14	KS01_15
KB_16	KS08_14	KS01_14
KB_17	KS06_14	KS01_15
KB_18	KS03_14	KS01_15
KB_19	KS02_14	KS01_15
KB_20	KS01_14	KS01_15
KB_21	KS01_14	KB_LED_PWR_15
KB_22	KS01_14	CAPS_LED#_15
KB_23	KS01_14	VDD_15
KB_24	KS01_14	NUM_LED#_15

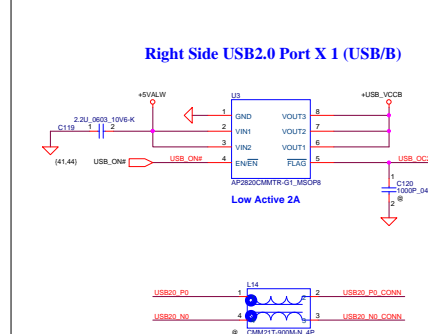
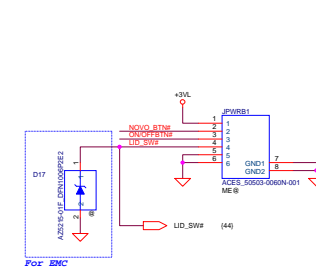


For 14"

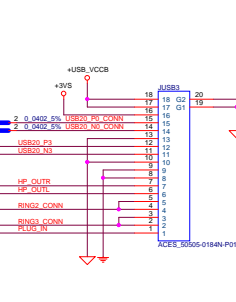
1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R



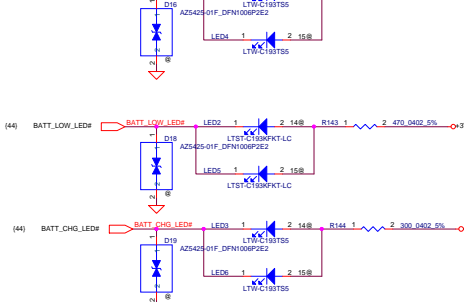
PWR/B Connector



USB I/O Connector

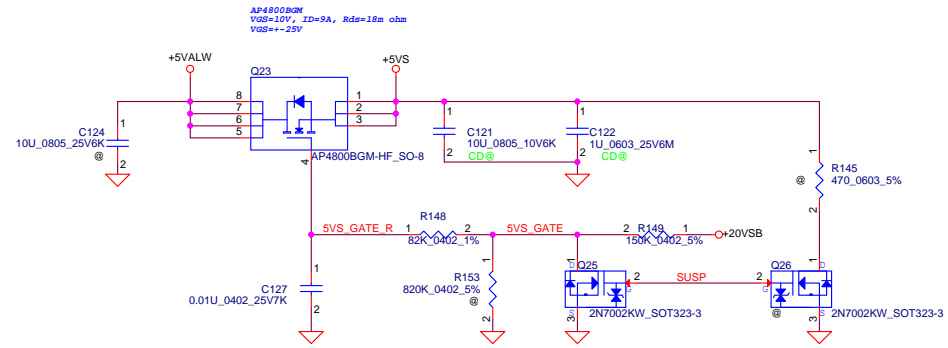


LED

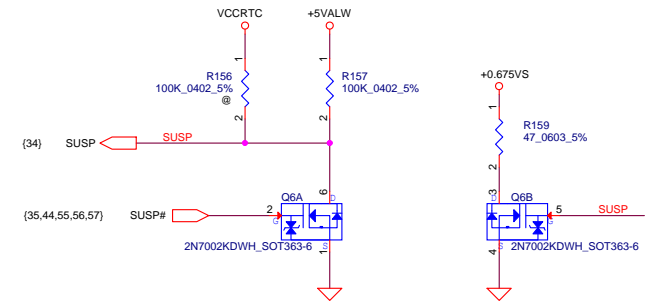
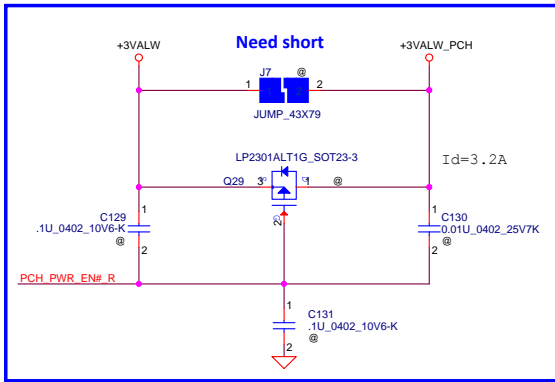
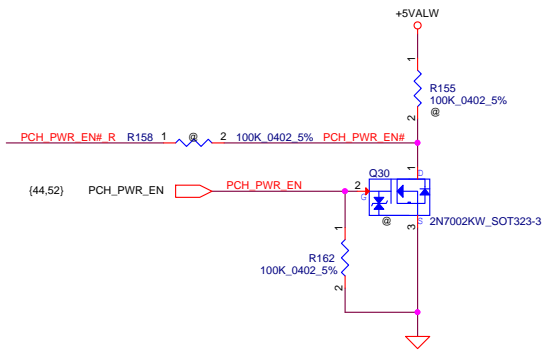
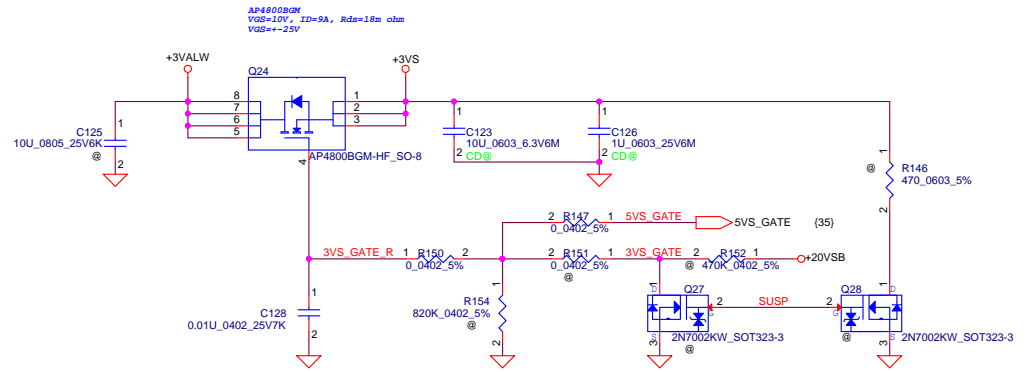


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Size	Document Number	Rev	
Count	U7MA	1.0	
Date	Monday, December 09, 2013	19:58	45 of 69

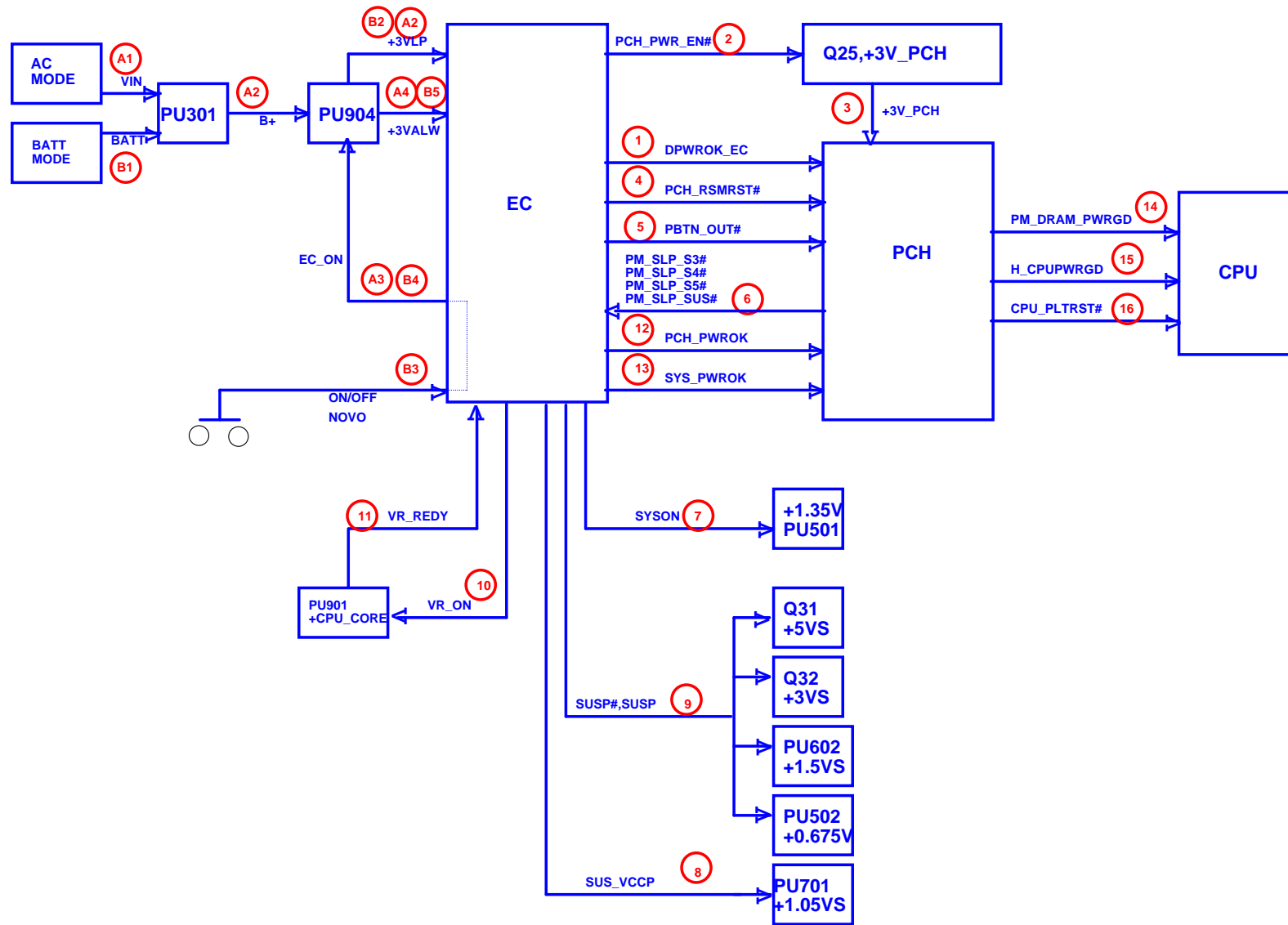
+5VALW to +5VS



+3VALW to +3VS



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Title	Power sequence Block	
Size	Document Number	Rev
Custom	UMA	1.0
Date:	Monday, December 09, 2013	Sheet 47 of 59

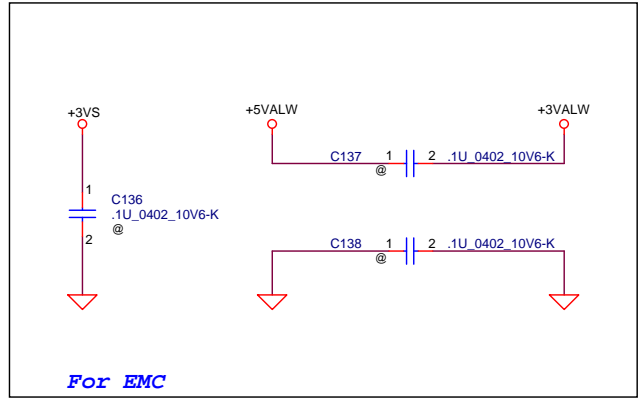
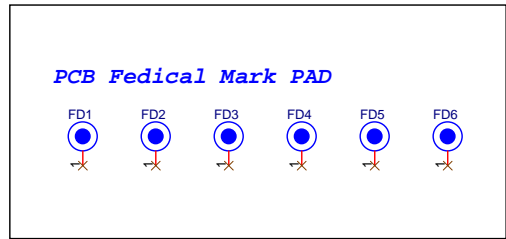
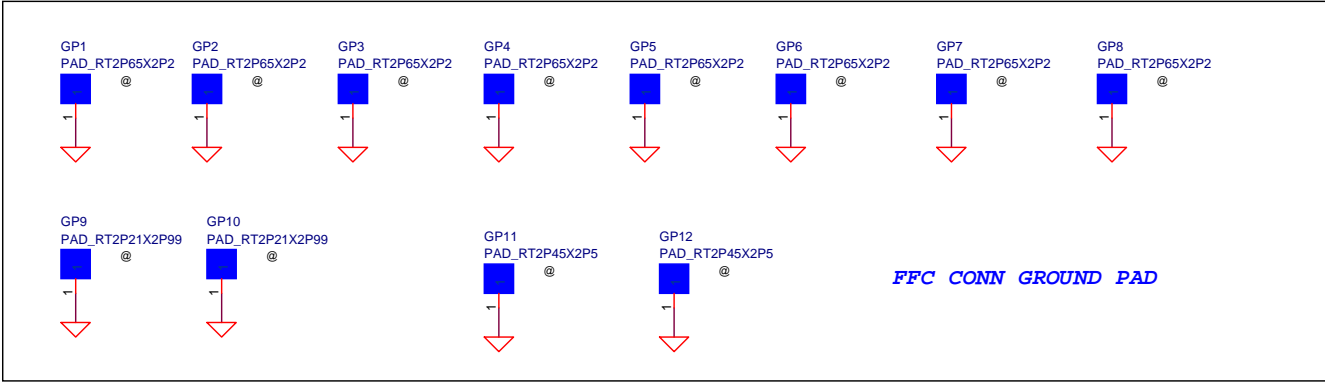
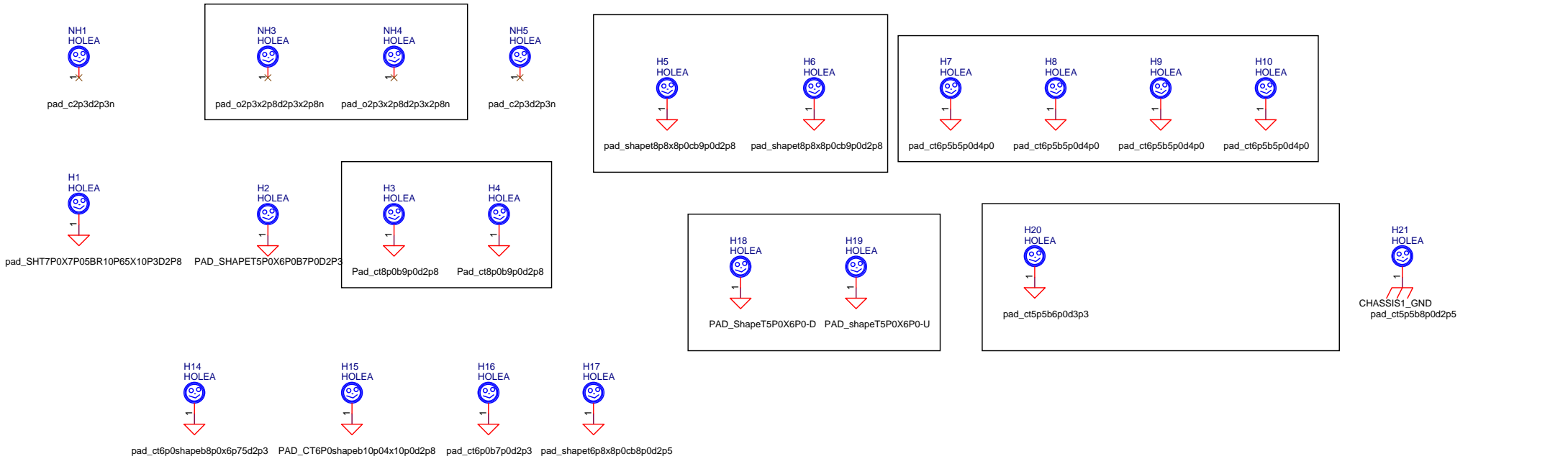


Board ID

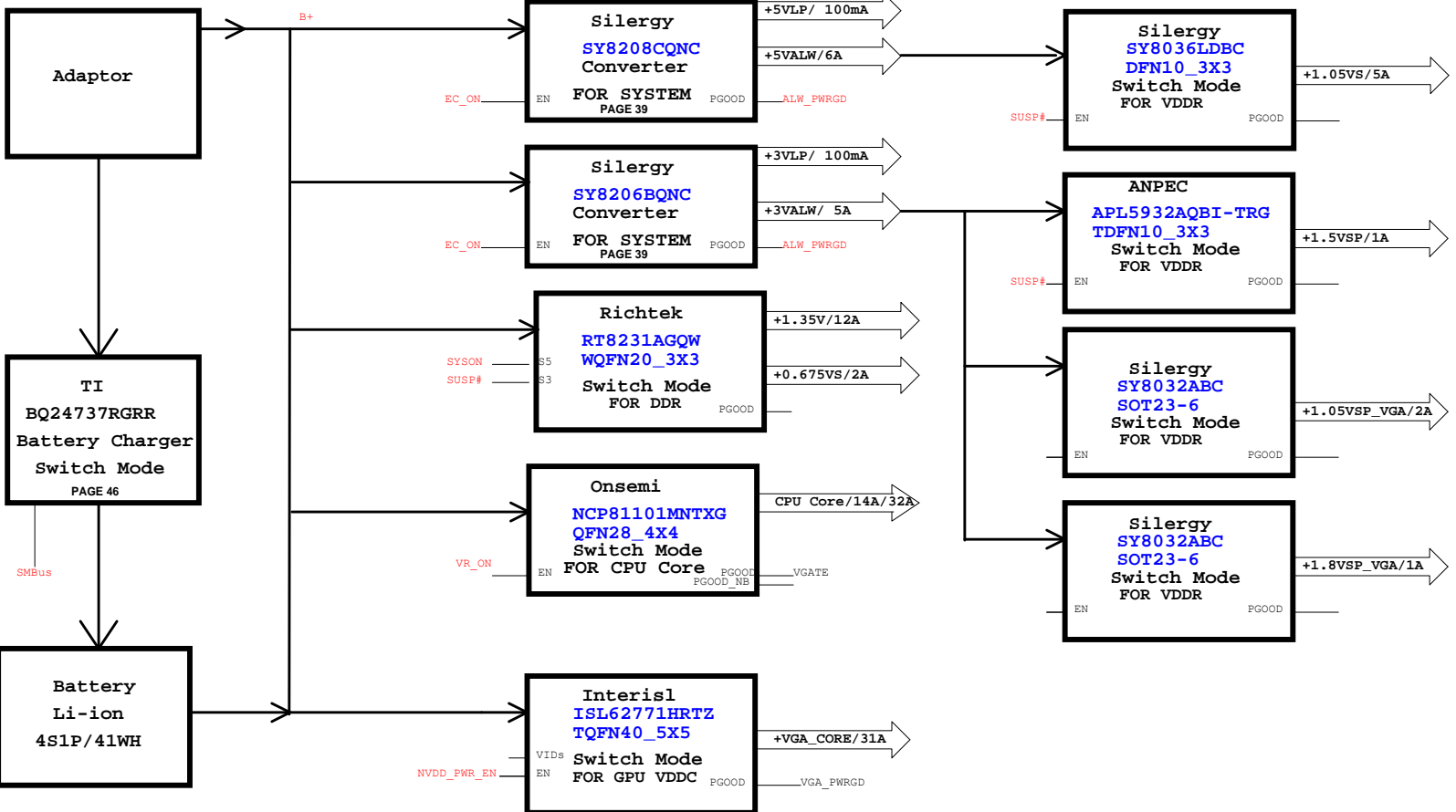
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	0	BDW + Jet-LE sku	RC107,RC108,RC109,RC123
0	0	1	0	BDW + Topaz-XT sku	RC107,RC108,RC102,RC123
0	1	0	0	BDW + N15V-GM sku	RC107,RC101,RC109,RC123
0	1	1	0	BDW + N15S-GT sku	RC107,RC101,RC102,RC123
* 1	0	0	0	HSW + Jet-LE sku	RC100,RC108,RC109,RC123
1	0	1	0	HSW + Topaz-XT sku	RC100,RC108,RC102,RC123
1	1	0	0	HSW + N15V-GM sku	RC100,RC101,RC109,RC123
1	1	1	0	HSW + N15S-GT sku	RC100,RC101,RC102,RC123
0	0	0	1	BDW + UMA sku	RC107,RC108,RC109,RC123
1	0	0	1	HSW + UMA sku	RC100,RC108,RC109,RC123

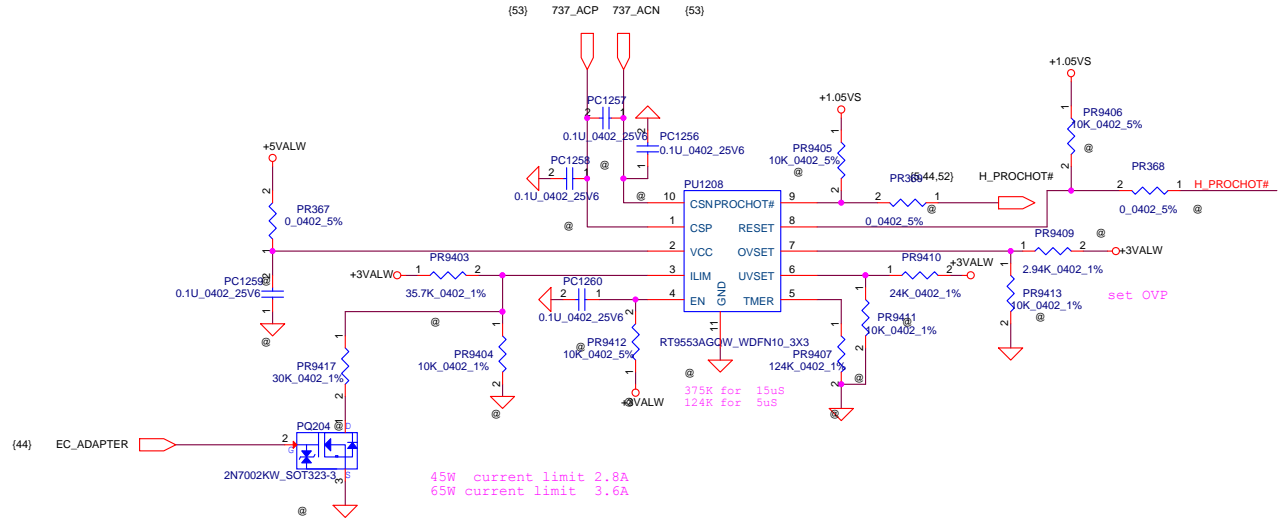
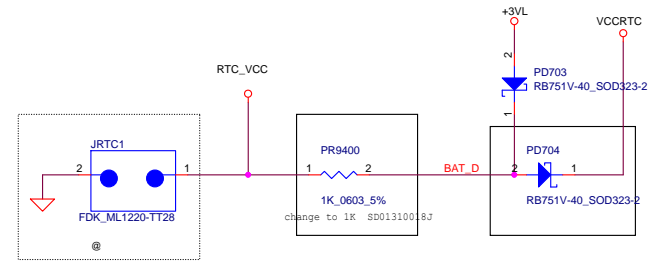
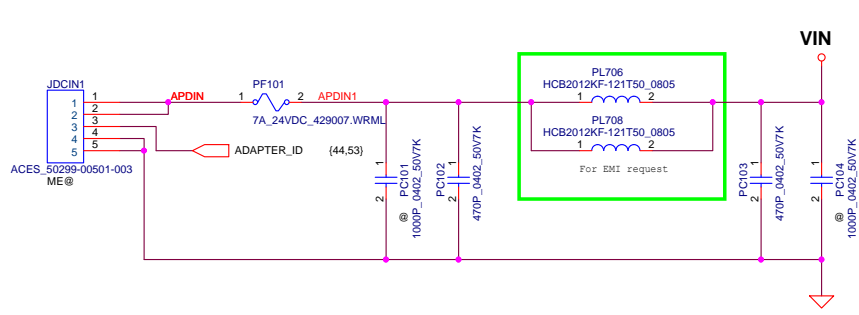
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Virtual symbol	
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				Date:	Monday, December 09, 2013	Sheet 49 of 59

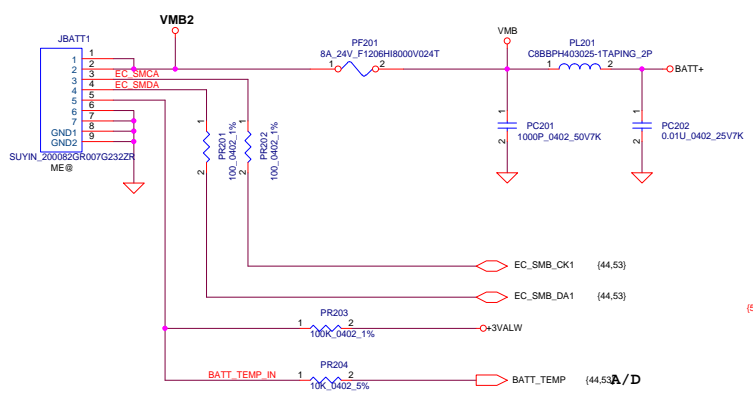




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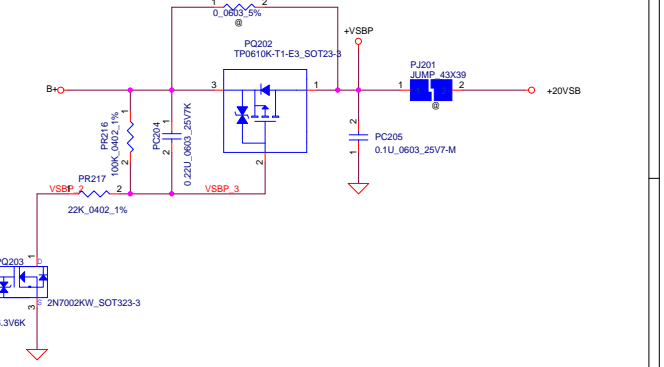
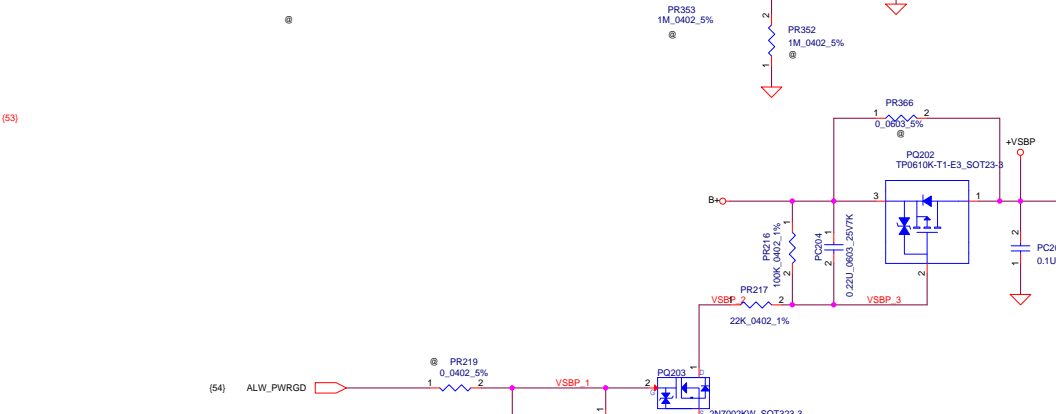
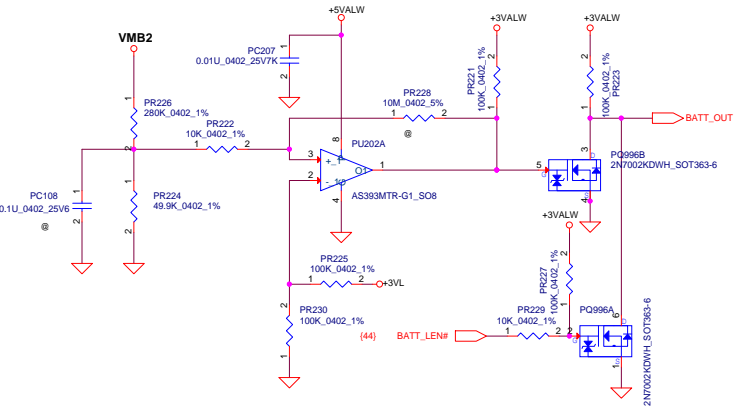
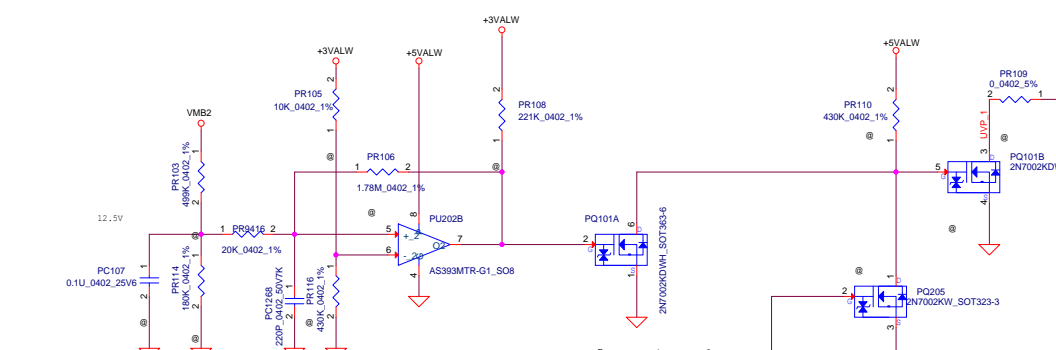
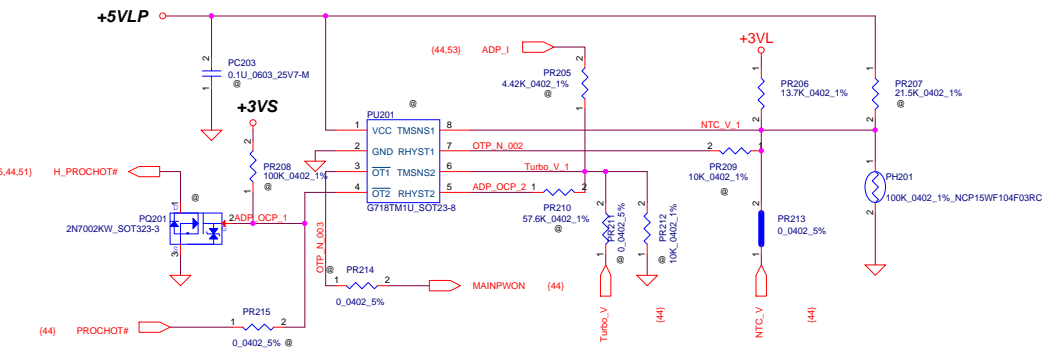
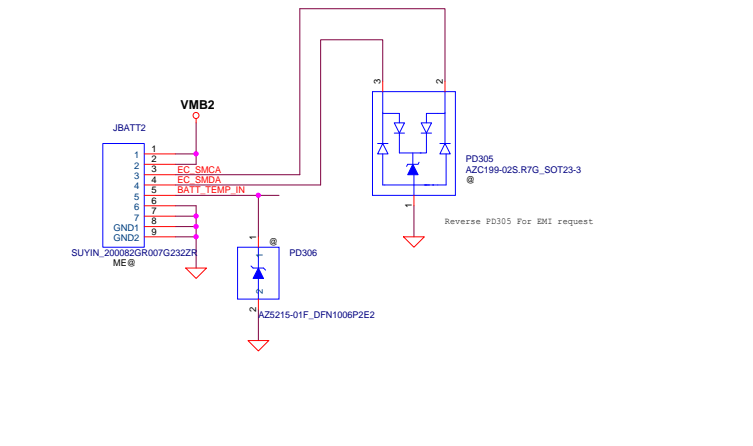
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Size	Custom
Document Number	UMA
Date:	Monday, December 09, 2013
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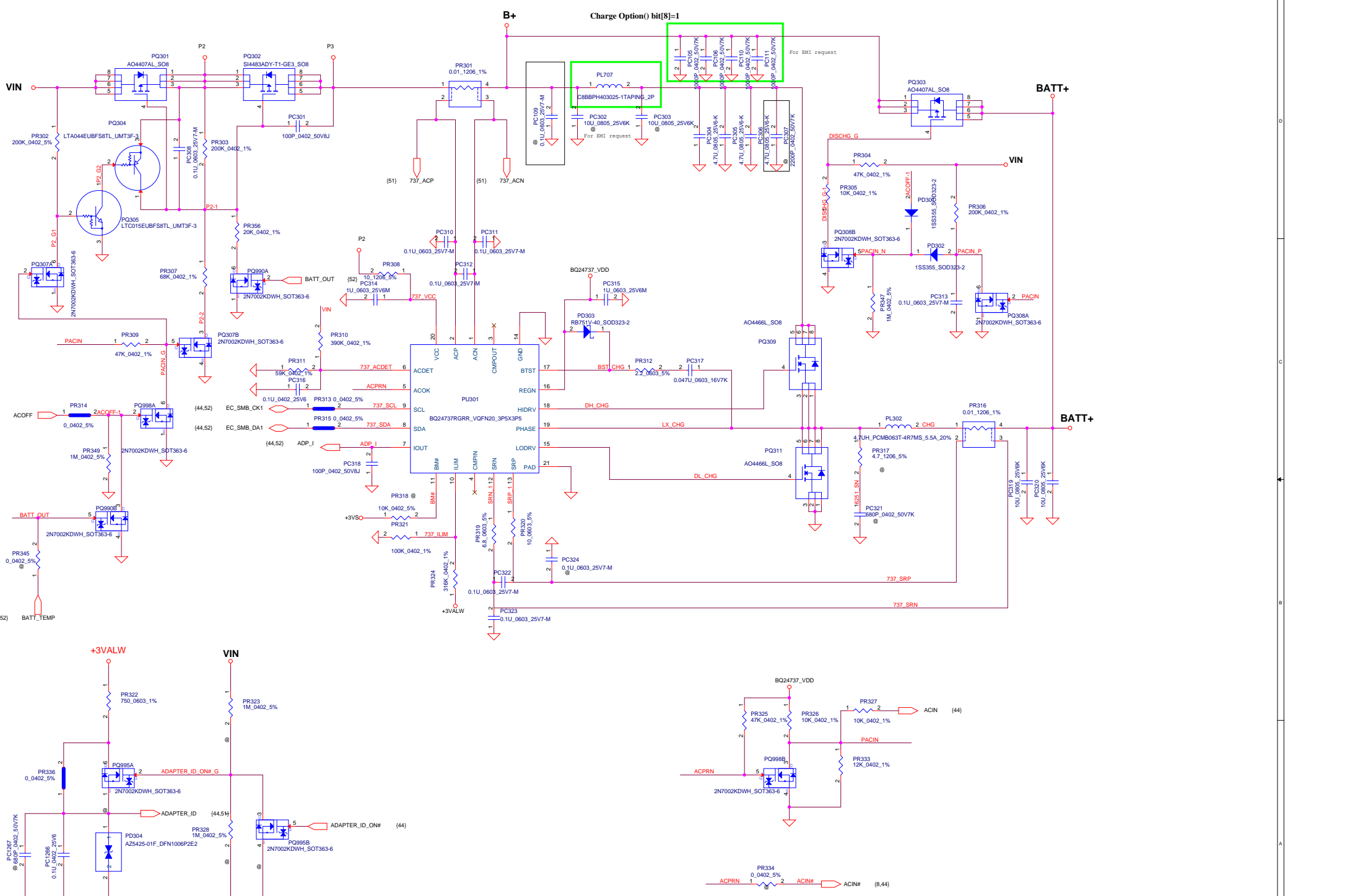


PH201 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C

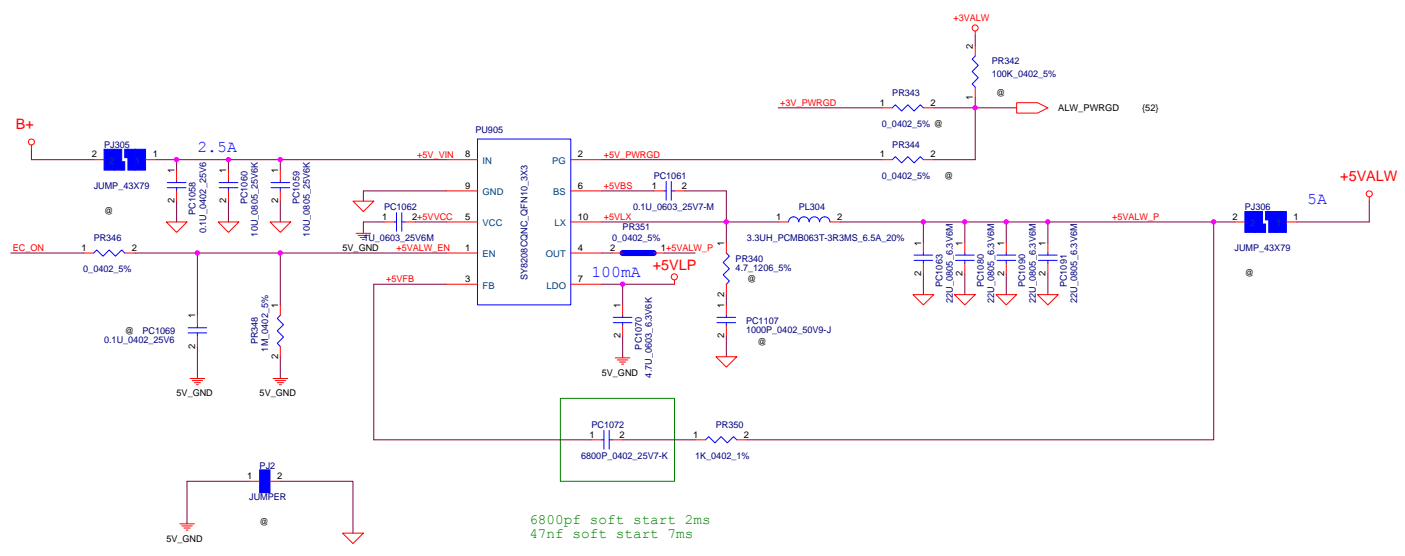
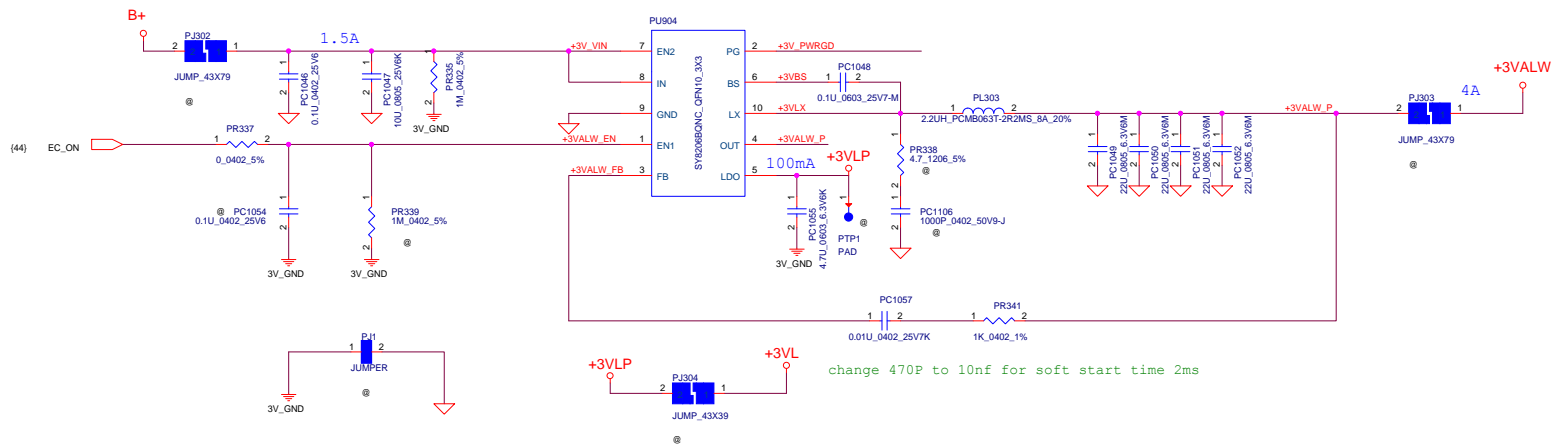
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



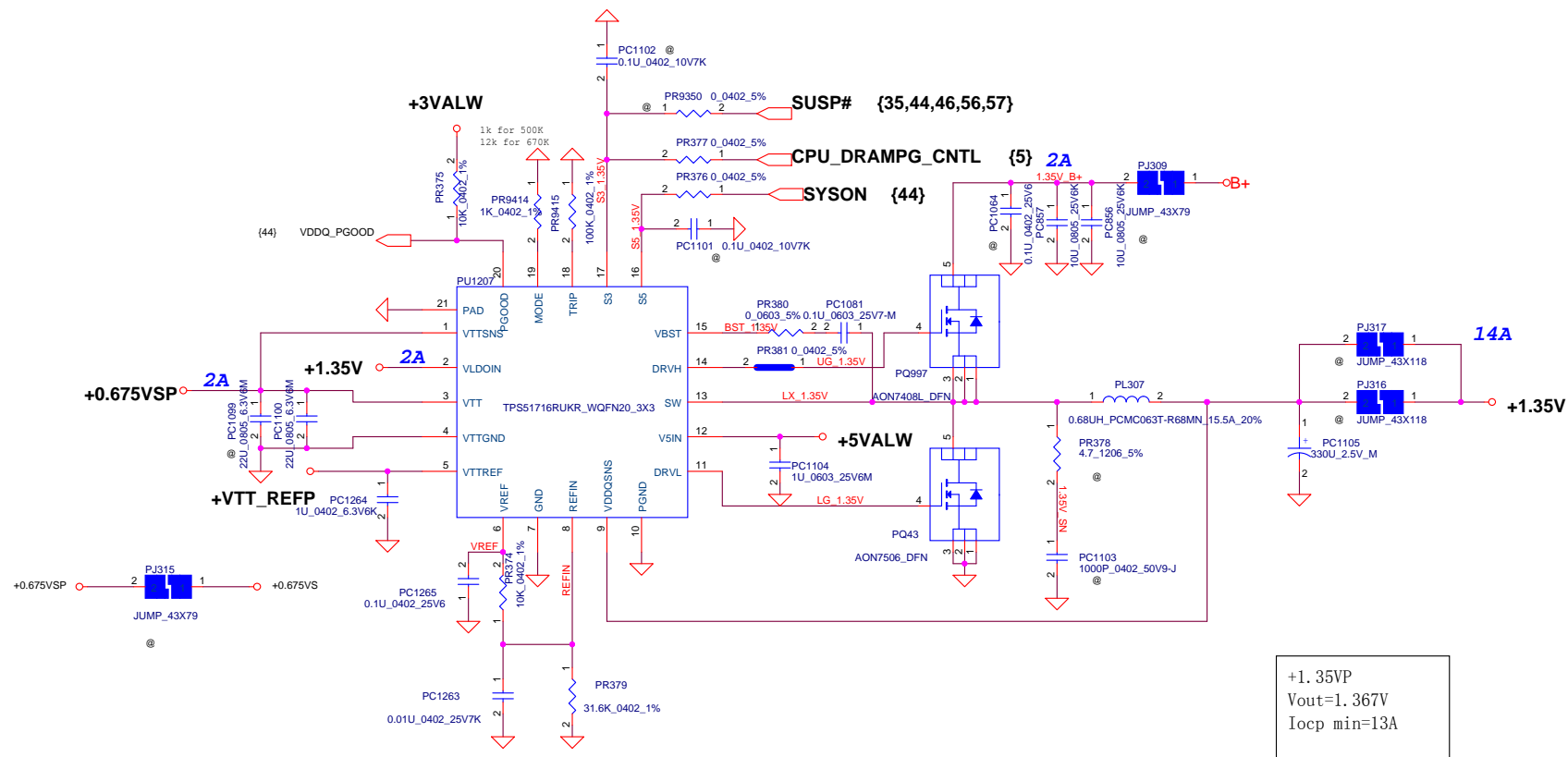
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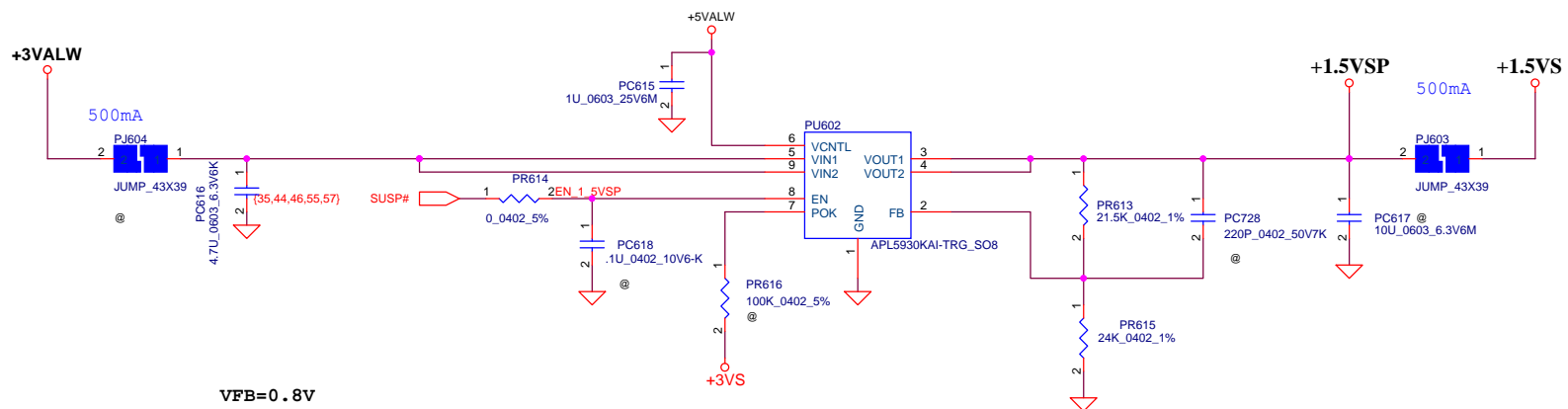


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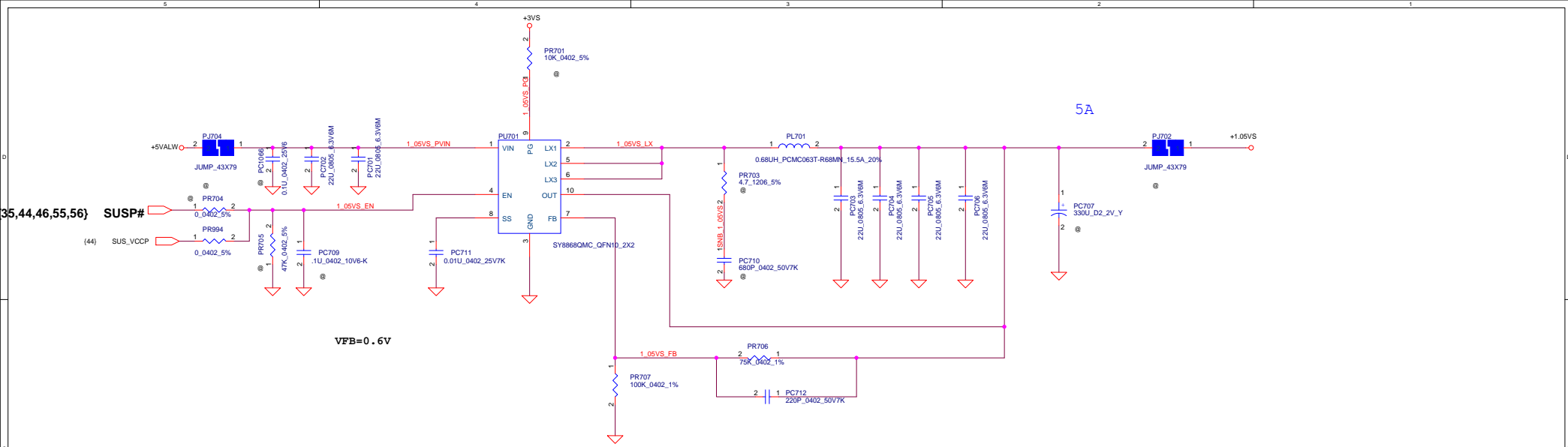
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1.35VS/+0.675VS		
Size	Document Number	Rev
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VFB=0.8V

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Title		
+1.35VS_VGA/+1.5VS		
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35,44,46,55,56}

SUSP#

(44) SUS_VCCP

VFB = 0.6V



5A

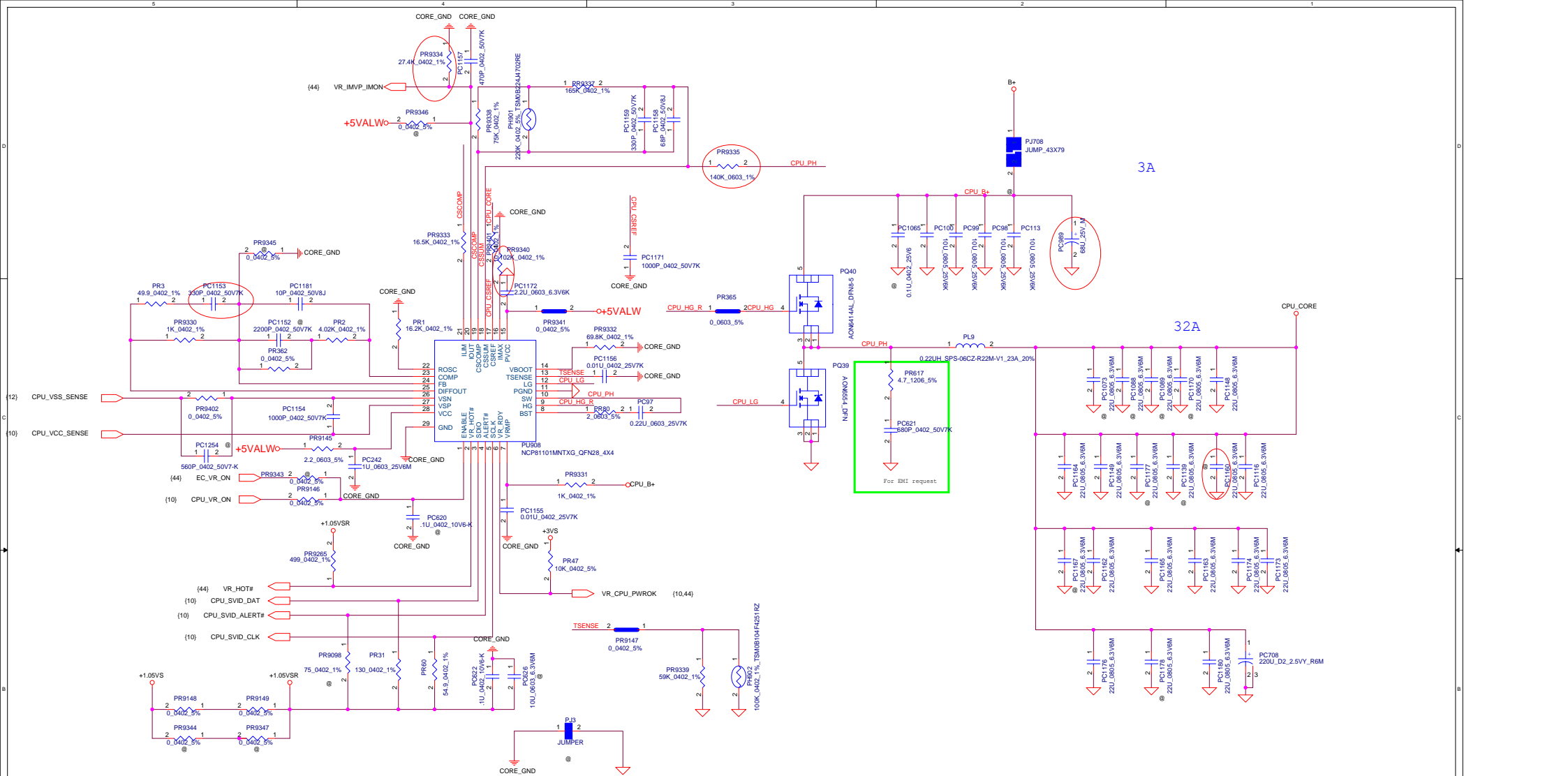
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+1.05VS/+1.05VS_VGA

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