

Compal Confidential

ULC AMD M/B LA-A996P DIS Schematics Document

AMD APU Beema/Kabini FT3 + ATI SUN LE + DDR3

Project Code : ZSO51

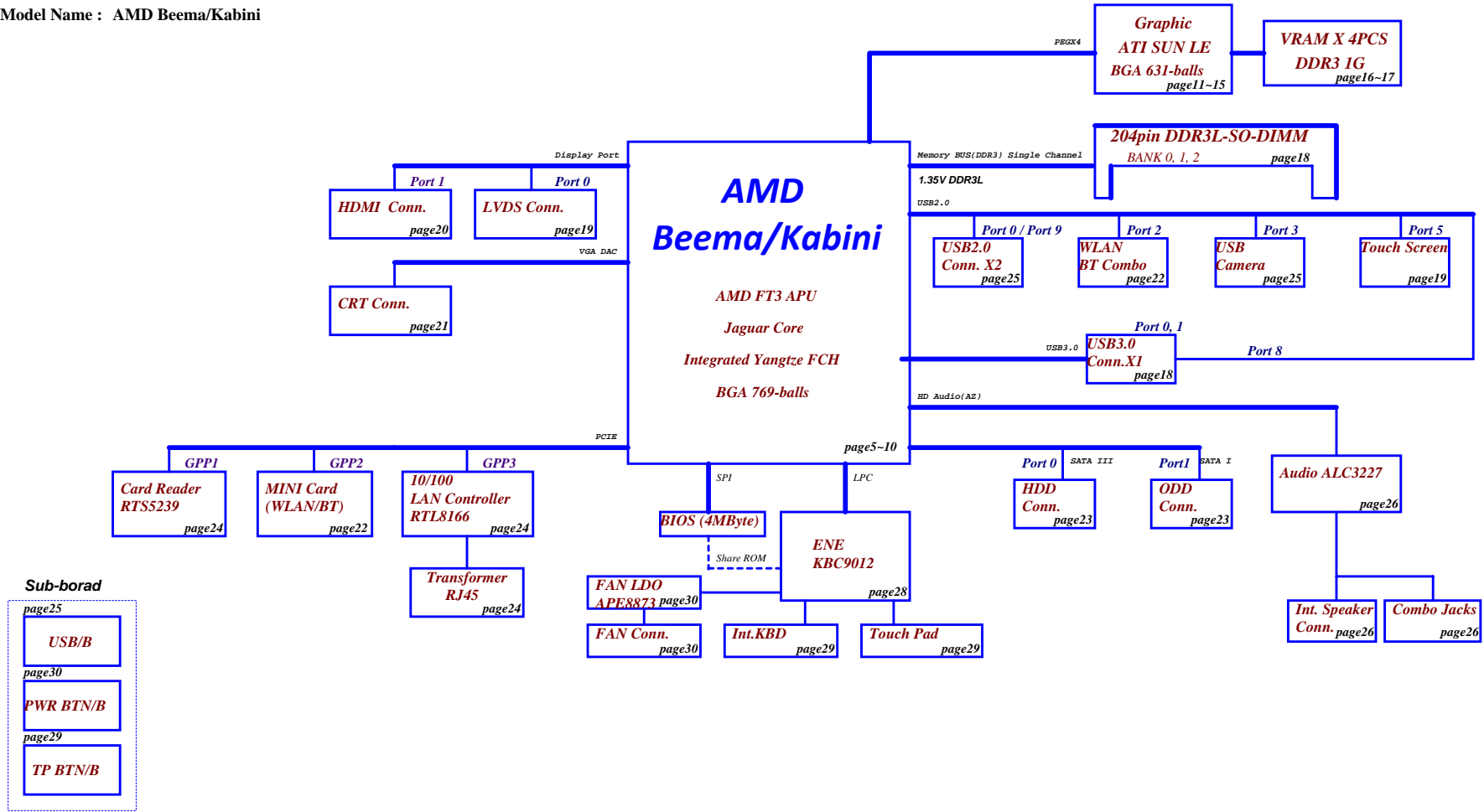
2014/02/08

PV Rev. 4.0

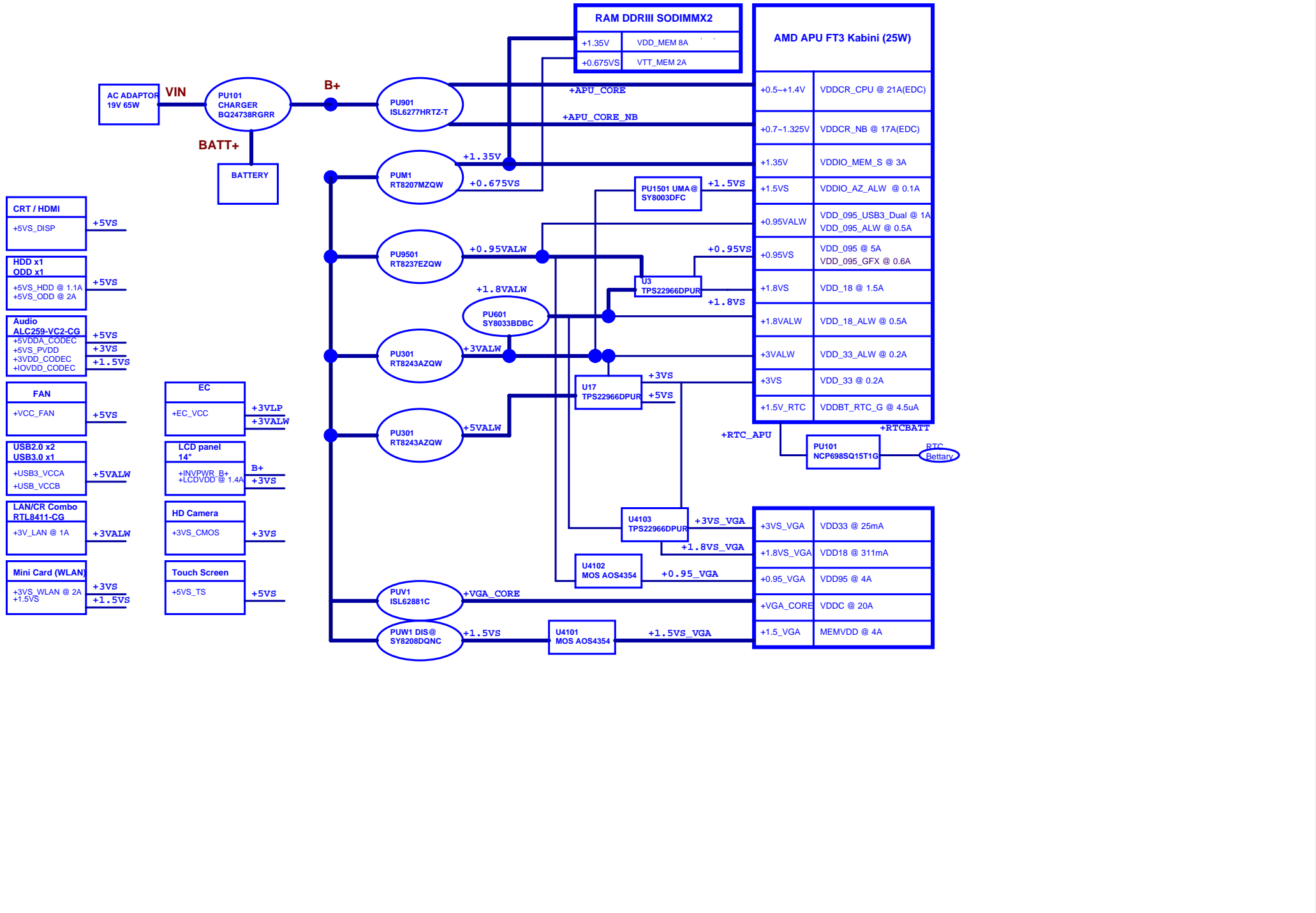
Security Classification	Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	COVER PAGE
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Model Name : AMD Beema/Kabini



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				BLOCK DIAGRAMS
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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power			

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF



A4-6300
Part Number = SA00007OP20
S IC A32 A4-6300 AM6300TJ44JB



E2-6200
Part Number = SA00007OQ20
S IC A32 E2-6200 EM6200TJ44JB 1.5G BGA



E1-6050
Part Number = SA00007IQ50
S IC A32 E1-6050 ZM1332M2J2370 1.35G BGA



A8-6410 15W
Part Number = SA00007TQ20
AM6410TJ44JB



A4-6210 R3 15W
Part Number = SA00007RA60
AM6210TJ44JB



E2-6110 R2 15W
Part Number = SA00007RB60
EM6110TJ44JB



E1-6010 R2 10
Part Number = SA00007RC60
EM6010IUJ23JB



A8-6410 15W
Part Number = SA00007TQ10
AM6410TJ44JB



A4-6210 R1 15W
Part Number = SA00007RA40
AM6210TJ44JB



E2-6110 R2 15W
Part Number = SA00007RB40
EM6110TJ44JB



E1-6010 R2 10
Part Number = SA00007RC40
EM6010IUJ23JB



PCB
Part Number = DAZ14000203
PCB LA-A996P REV4.0 MIB



E1-2100
Part Number = SA00006QX10
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A4-5000
Part Number = SA00006R410
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



E2-3800
Part Number = SA00007BX20
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A6-5200
Part Number = SA00006R350
S IC KABINI AM5200AJ44HM 2G BGA769P APU



HDMI
Part Number = RO0000003HM
PCB 102 LA-A996P REV0 MIB 2



E1-2100
Part Number = SA00006QX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A4-5000
Part Number = SA00006R460
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



E2-3800
Part Number = SA00007BX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P

SMBus List

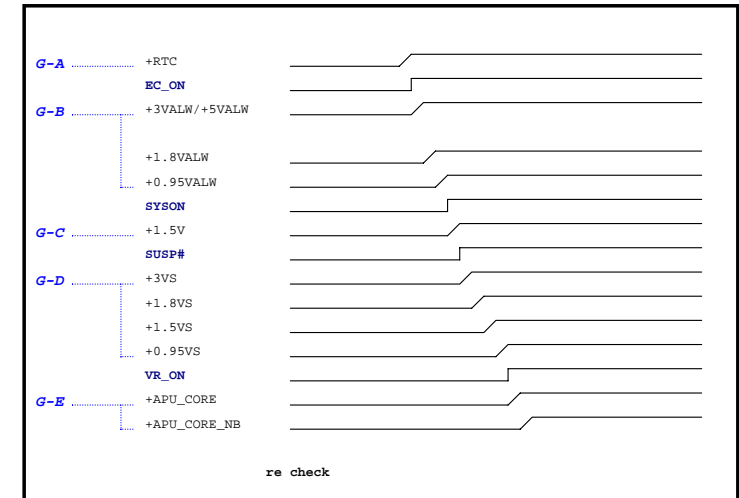
EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

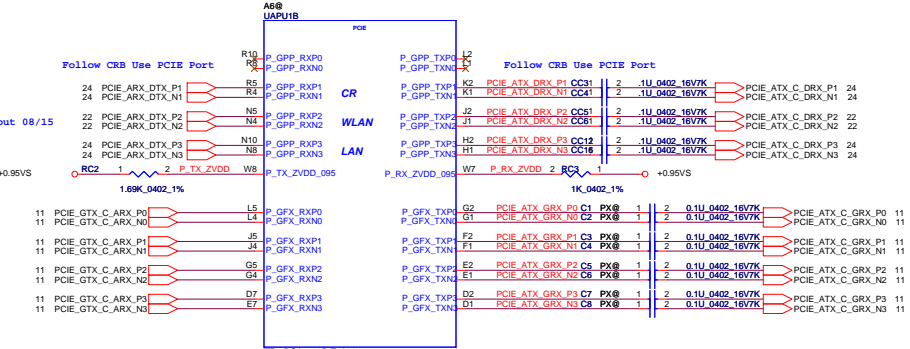
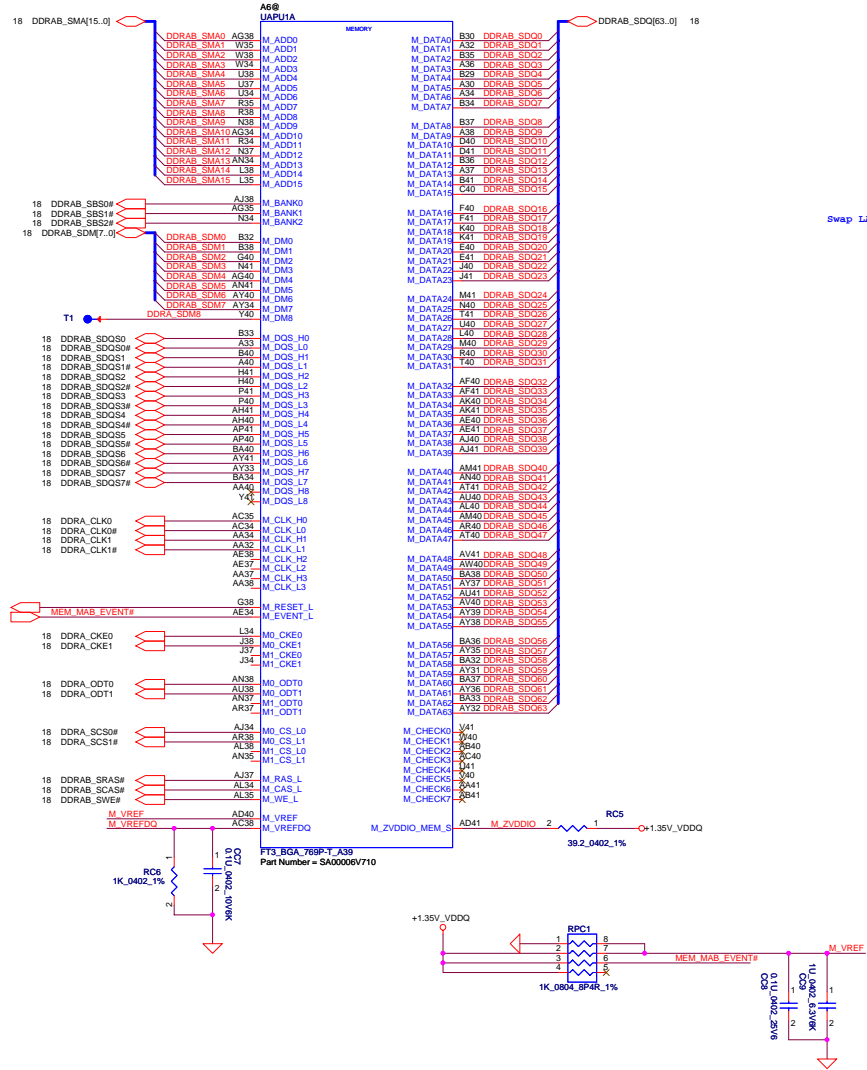
APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM2	1010 000Xb	A0H			
DDR DIMM1	1010 001Xb	A2H			
Mini Card (DNI)					

BOM Structure Table

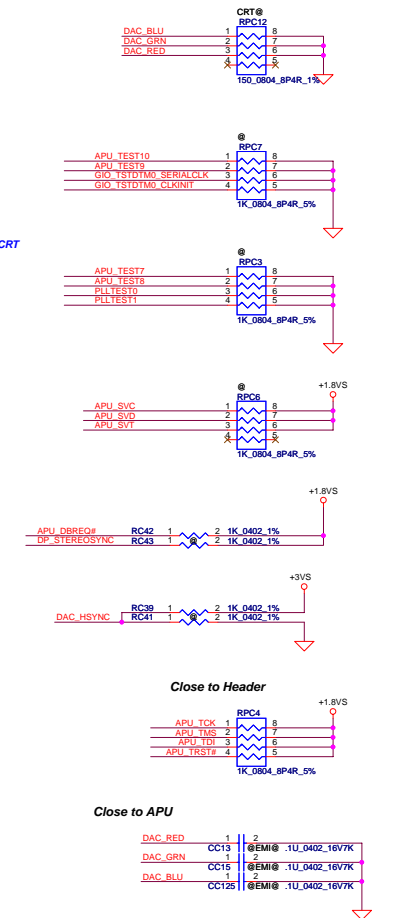
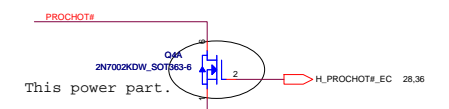
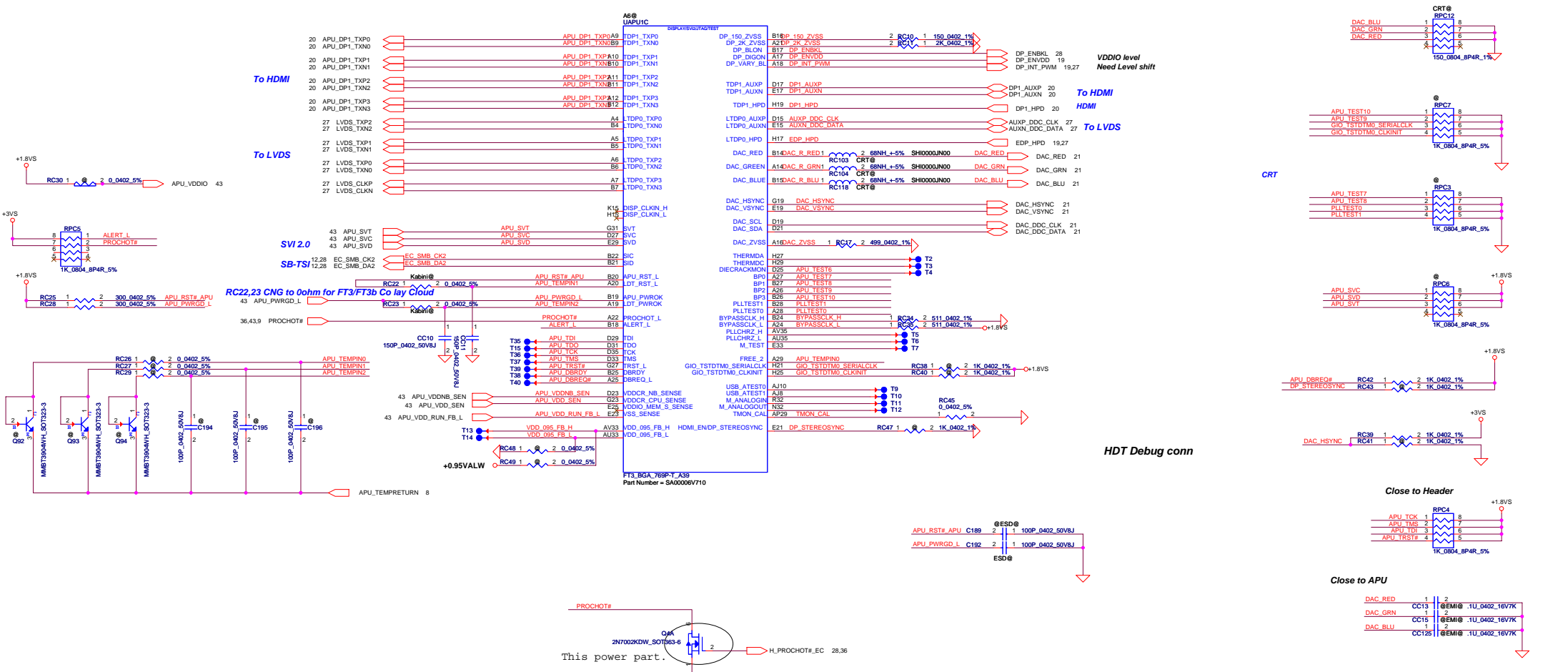
BOM Structure	BTO Item
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD Unpop component
PX@	GPU SUN LE Componet
8166@	10/100 LAN
8151@	Giga LAN
UMA@	UMA Componet
display@	display Componet
EDP@	EDP Componet
KLVDs@	Kabini LVDS Componet
BLVDs@	Beema LVDS Componet
Kabini@	Kabini Componet
Beema@	Beema Componet
LVDS@	LVDS Componet

APU POWER SEQUENCE

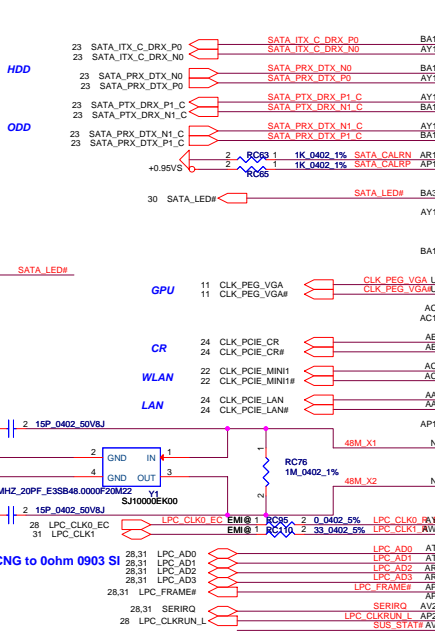




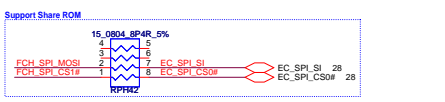
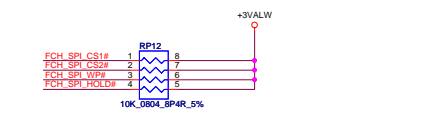
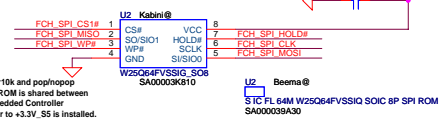
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Title			LA-USB LPC SPI
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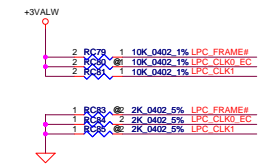
4MB SPI ROM & Non-share ROM.

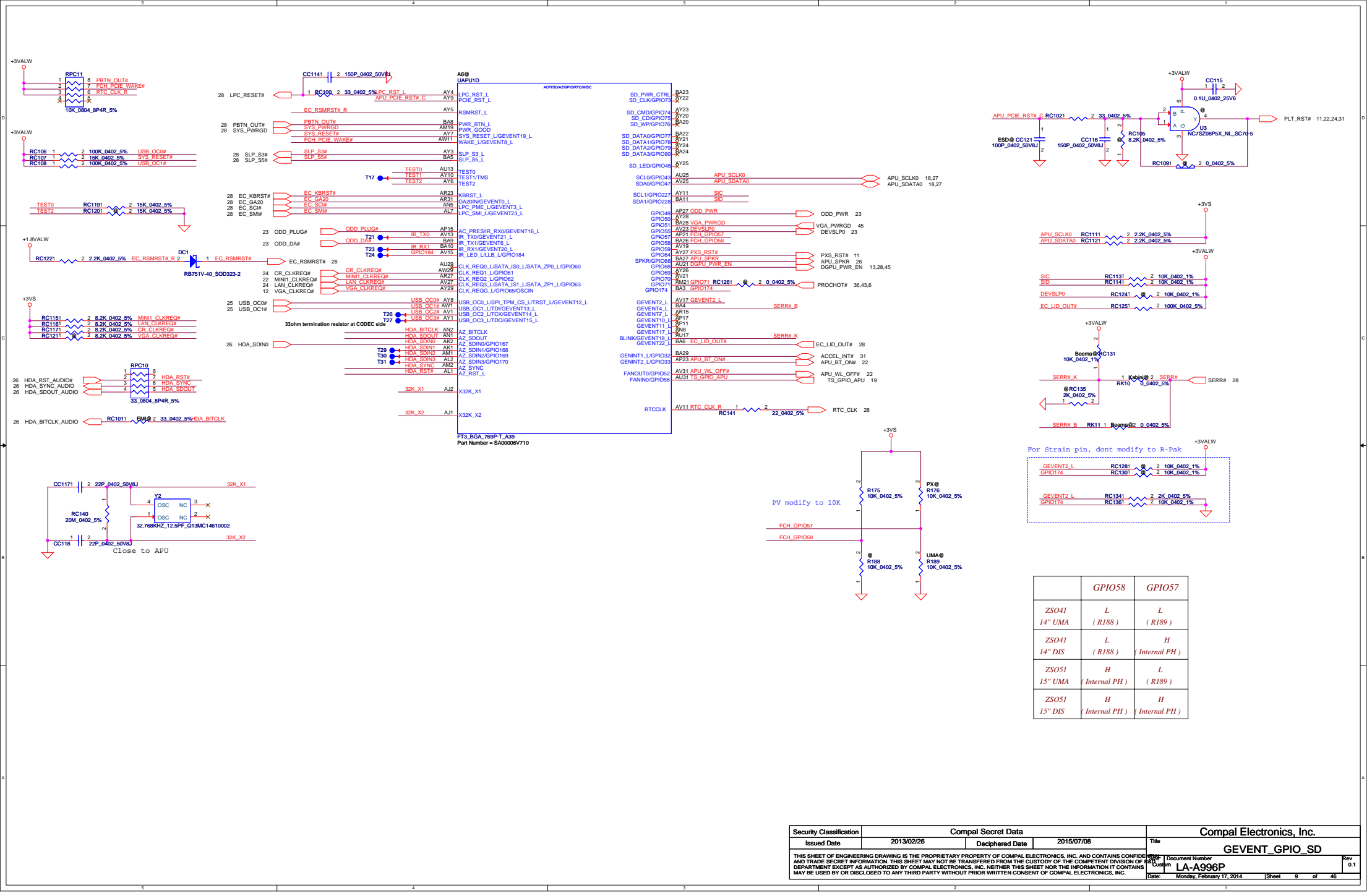


RC78, RC82 CNG to 0ohm 0903 SI

STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION





FT3_BGA_789P-T_A39
Part Number = SA00006V710

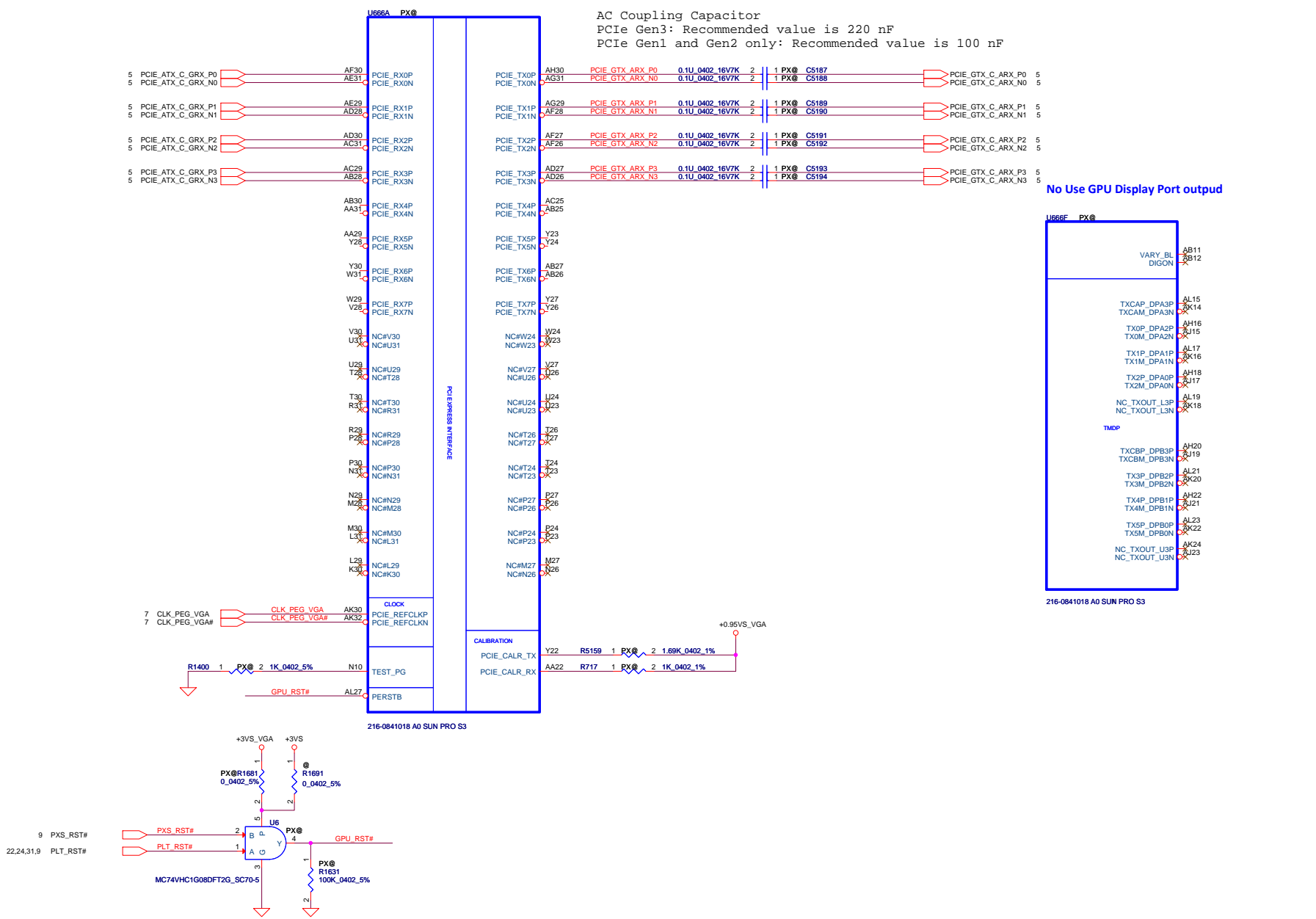
	GPI058	GPI057
ZS041	L	L
14" UMA	(R188)	(R189)
ZS041	L	H
14" DIS	(R188)	Internal PH
ZS051	H	L
15" UMA	(Internal PH)	(R189)
ZS051	H	H
15" DIS	(Internal PH)	Internal PH

Panel ENBKL

Panel ENVDD

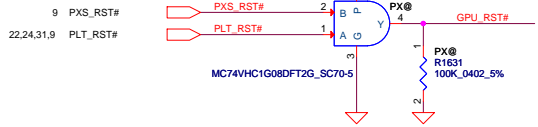
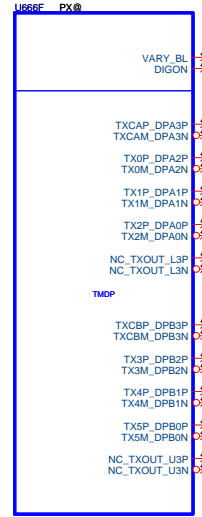
Panel PWM

Security Classification	Compal Secret Data			Title	Level Shifter
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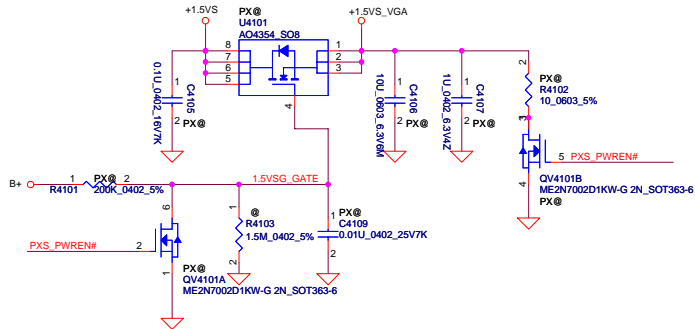
AC Coupling Capacitor
 PCIe Gen3: Recommended value is 220 nF
 PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No GPU Display Port output



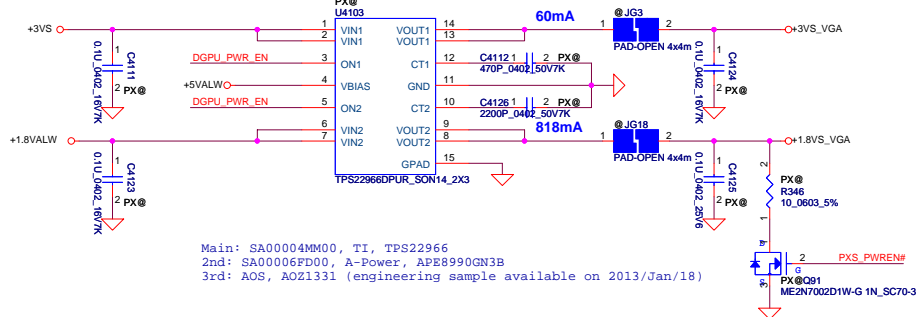
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN_PCIE/DP
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+1.5VS to +1.5VS_VGA (2.096A)



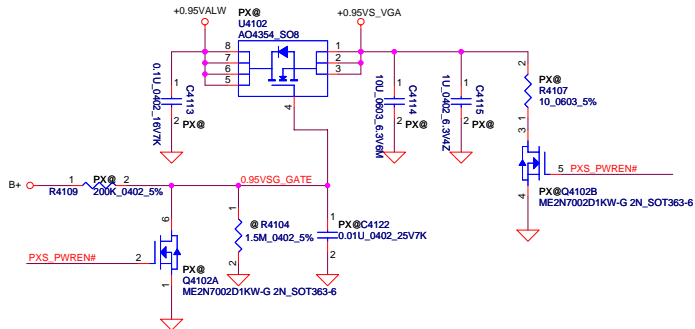
+3VS to +3VS_VGA (25mA)
+1.8VALW to +1.8VS_VGA (311mA)

+1.8VS_VGA 必須比 +VGA_CORE晚起來

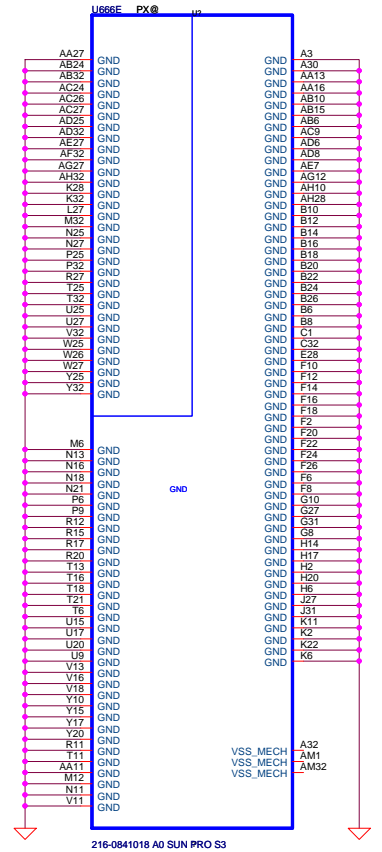
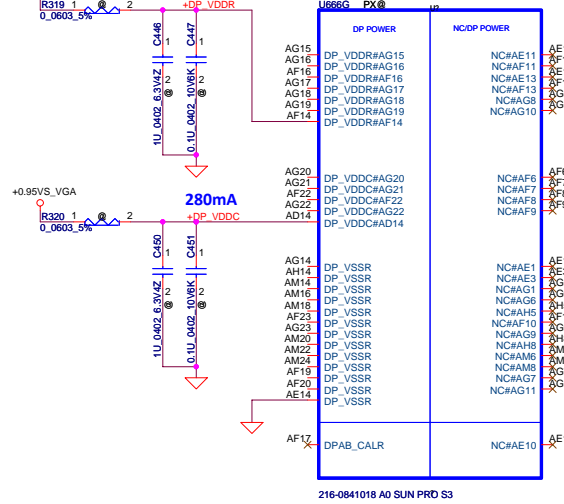


Main: SA00004MM00, TI, TPS22966
 2nd: SA00006FD00, A-Power, APE8990GN3B
 3rd: AOS, A021331 (engineering sample available on 2013/Jan/18)

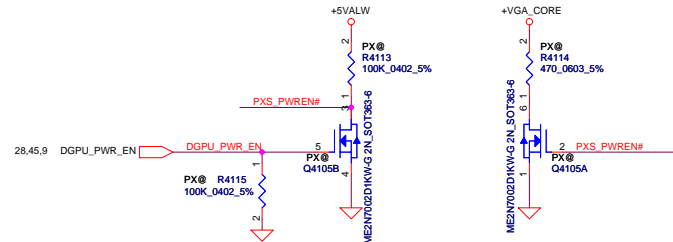
+0.95VALW to +0.95VSG (4.016A)



370mA (HDMI)
188mA (Display Port)
 No Use GPU Display Port output



+0.95VALW to +0.95VSG (4.016A)



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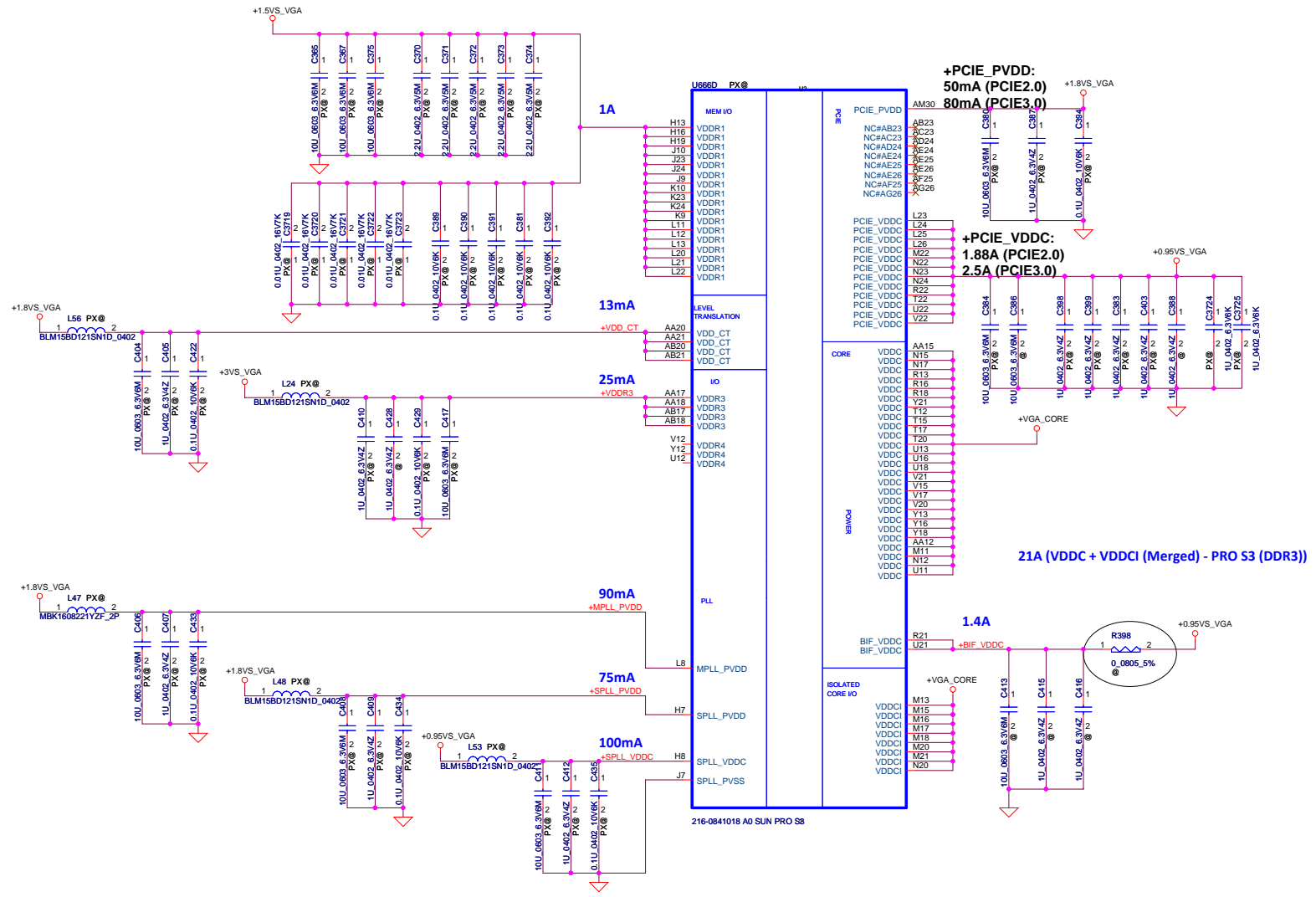
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

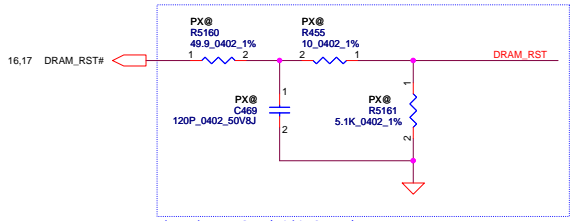
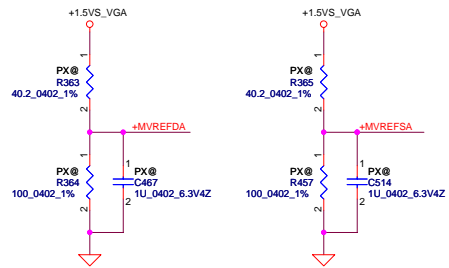
+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

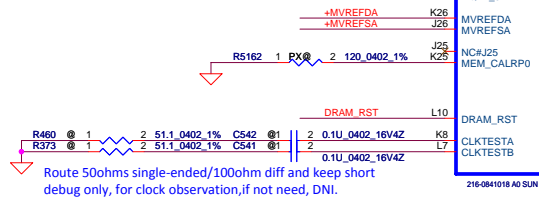
+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)



- 16.17 M_DA[63..0] M_DA[63..0]
- 16.17 M_MA[15..0] M_MA[15..0]
- 16.17 M_DOM[7..0] M_DOM[7..0]
- 16.17 M_DQS[7..0] M_DQS[7..0]
- 16.17 M_DQS# [7..0] M_DQS#[7..0]



Place close to GPU (within 25mm)
and place component close to each other

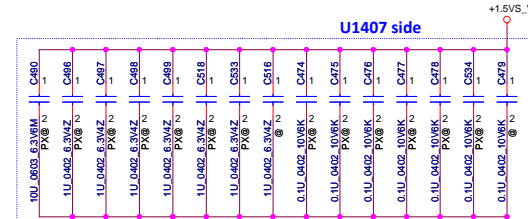
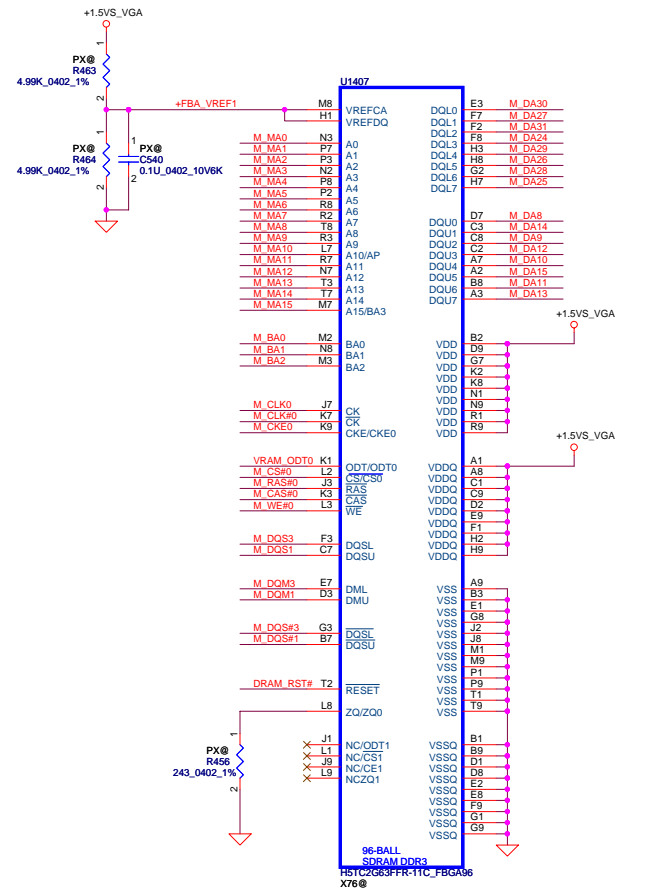
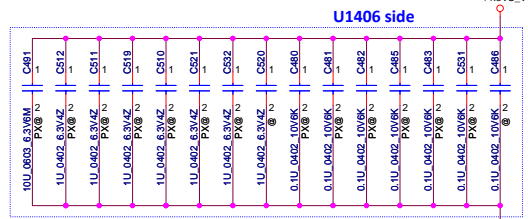
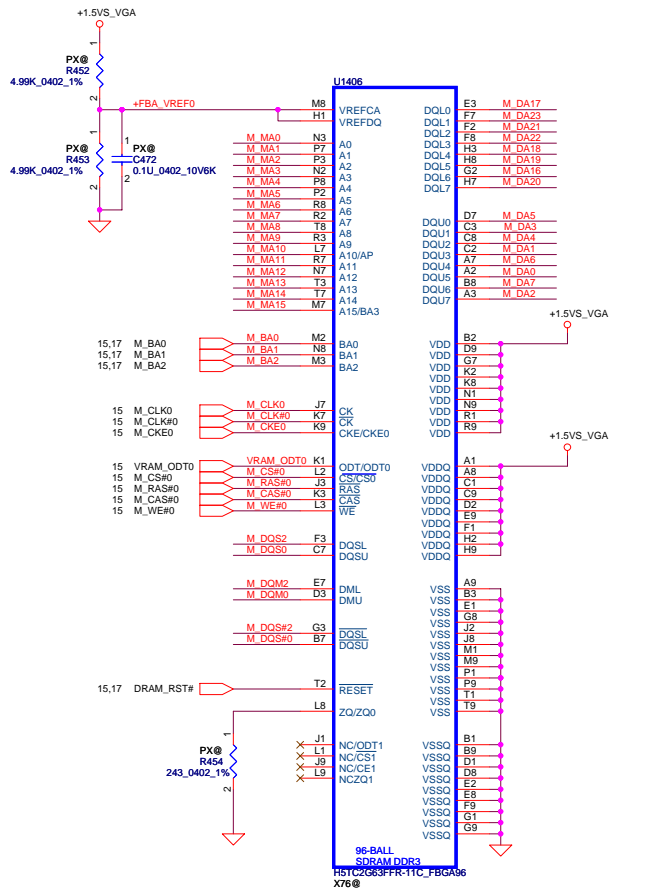


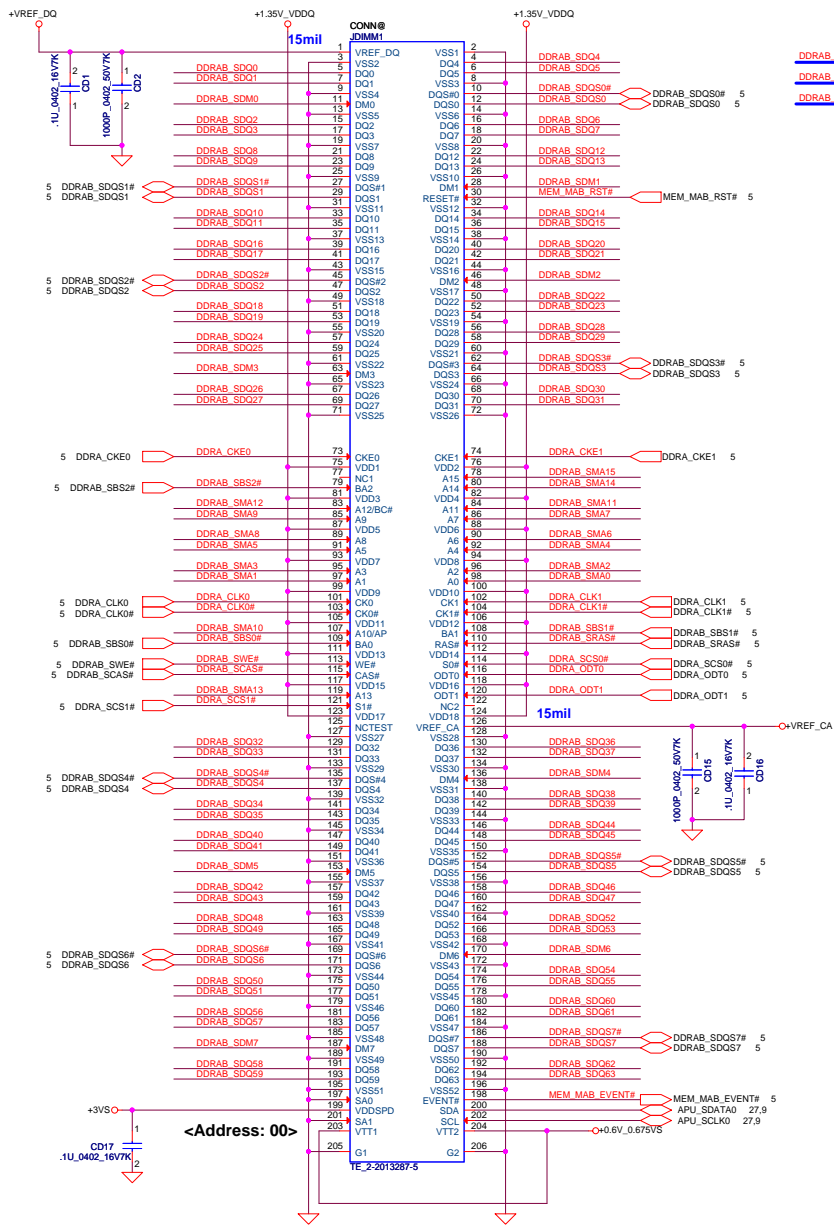
Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation, if not need, DNI.

PX@ U886C		IP	
M_DA0	K27	DDA0_0	M_MAO
M_DA1	J29	DDA0_1	M_MA1
M_DA2	H33	DDA0_2	H23
M_DA3	H32	DDA0_3	M_MA3
M_DA4	G29	DDA0_4	G24
M_DA5	F28	DDA0_5	H24
M_DA6	F32	DDA0_6	J19
M_DA7	F30	DDA0_7	K19
M_DA8	C30	DDA0_8	C20
M_DA9	F27	DDA0_9	L17
M_DA10	A28	DDA0_10	J14
M_DA11	C28	DDA0_11	K14
M_DA12	E27	DDA0_12	J11
M_DA13	G26	DDA0_13	J13
M_DA14	D26	DDA0_14	H11
M_DA15	F25	DDA0_15	G11
M_DA16	A25	DDA0_16	J16
M_DA17	C25	DDA0_17	L15
M_DA18	E25	DDA0_18	G14
M_DA19	D24	DDA0_19	L16
M_DA20	E23	DDA0_20	K
M_DA21	F23	DDA0_21	E32
M_DA22	D22	DDA0_22	E30
M_DA23	F21	DDA0_23	A21
M_DA24	E21	DDA0_24	C21
M_DA25	D20	DDA0_25	E13
M_DA26	F19	DDA0_26	D12
M_DA27	A19	DDA0_27	E3
M_DA28	D18	DDA0_28	F4
M_DA29	F17	DDA0_29	H28
M_DA30	A17	DDA0_30	C27
M_DA31	C17	DDA0_31	A23
M_DA32	D16	DDA0_32	E19
M_DA33	D16	DDA0_33	E15
M_DA34	F15	DDA0_34	D10
M_DA35	A15	DDA0_35	D6
M_DA36	D14	DDA0_36	G5
M_DA37	F13	DDA0_37	H27
M_DA38	A13	DDA0_38	A27
M_DA39	C13	DDA0_39	C23
M_DA40	E11	DDA0_40	C19
M_DA41	A11	DDA0_41	C15
M_DA42	C11	DDA0_42	E9
M_DA43	F11	DDA0_43	C5
M_DA44	A9	DDA0_44	H4
M_DA45	C9	DDA0_45	L18
M_DA46	F9	DDA0_46	K16
M_DA47	D8	DDA0_47	H26
M_DA48	E7	DDA0_48	H25
M_DA49	A7	DDA0_49	G9
M_DA50	C7	DDA0_50	H9
M_DA51	F7	DDA0_51	G22
M_DA52	A5	DDA0_52	G17
M_DA53	E5	DDA0_53	G19
M_DA54	C3	DDA0_54	G16
M_DA55	E1	DDA0_55	H22
M_DA56	G7	DDA0_56	K22
M_DA57	G6	DDA0_57	G13
M_DA58	G1	DDA0_58	K13
M_DA59	G3	DDA0_59	H26
M_DA60	J6	DDA0_60	H25
M_DA61	J1	DDA0_61	G9
M_DA62	J8	DDA0_62	H9
M_DA63	J5	DDA0_63	G22
M_DA64	J5	DDA0_64	G17
M_DA65	J5	DDA0_65	G19
M_DA66	J5	DDA0_66	G16
M_DA67	J5	DDA0_67	H22
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Memory Partition A - Lower 32 bits

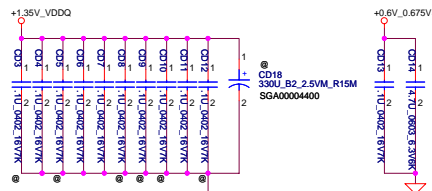
- 15,17 M_DA[63..0] \rightarrow M_DA[63..0]
- 15,17 M_MA[15..0] \rightarrow M_MA[15..0]
- 15,17 M_DQM[7..0] \rightarrow M_DQM[7..0]
- 15,17 M_DQS[7..0] \rightarrow M_DQS[7..0]
- 15,17 M_DQS#7..0] \rightarrow M_DQS#7..0]





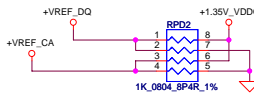
- DDRAB_SDQ[0..63] 5
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- DDRAB_SMA[0..15] 5

+1.35V_VDDQ/+0.675VS OF DIMM1



0.1UX10

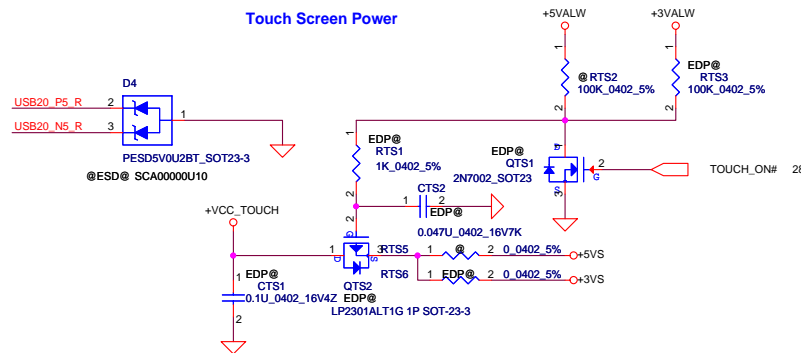
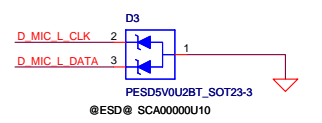
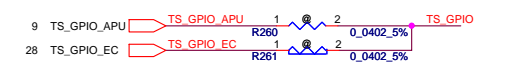
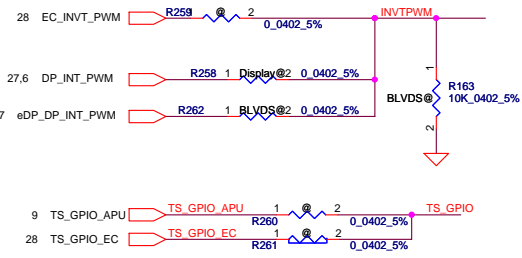
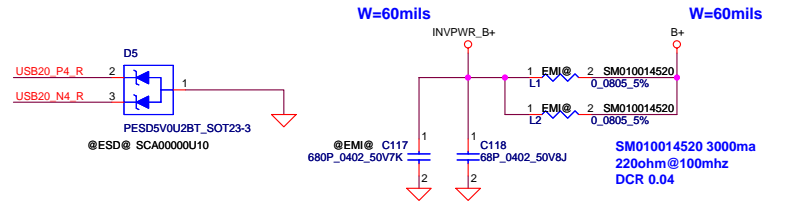
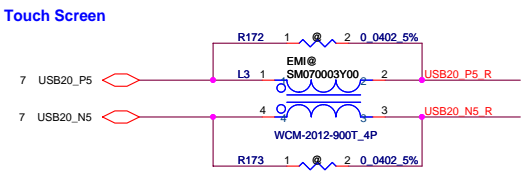
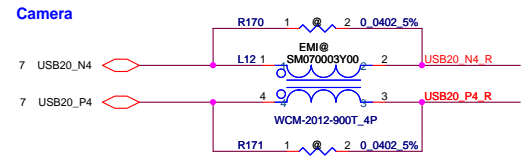
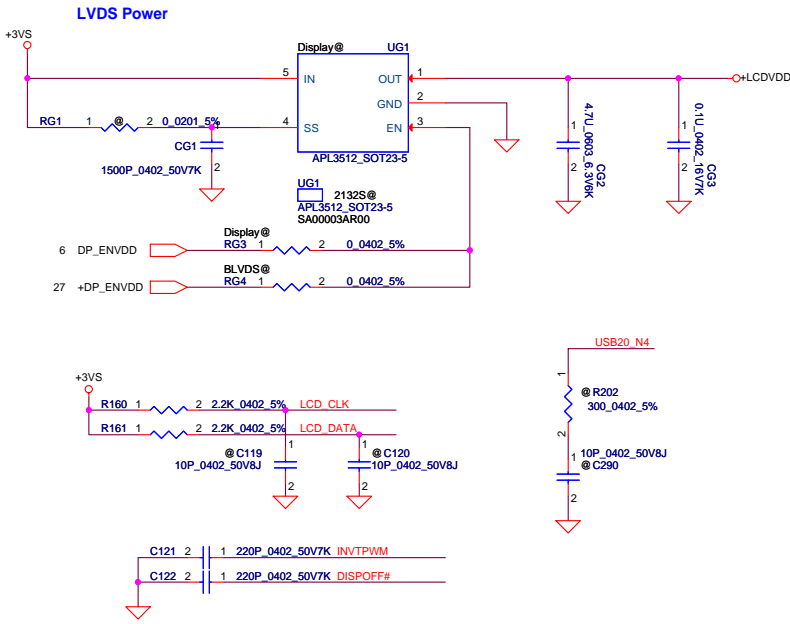
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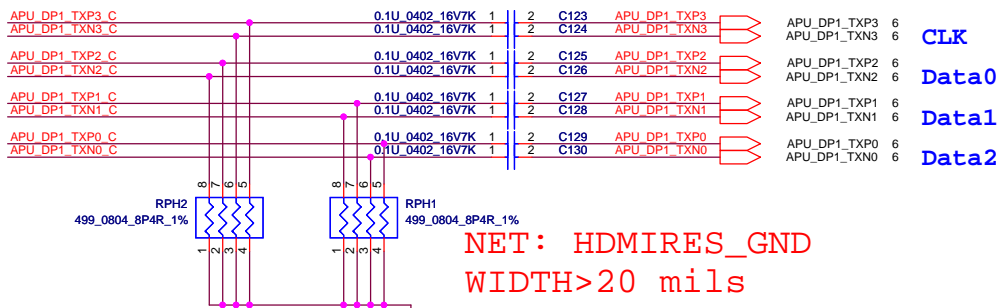
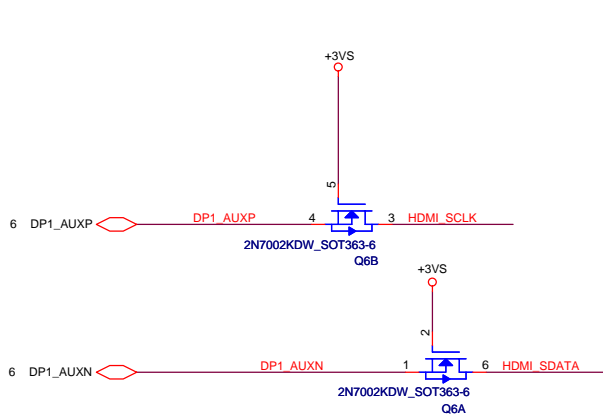
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						Document Number	
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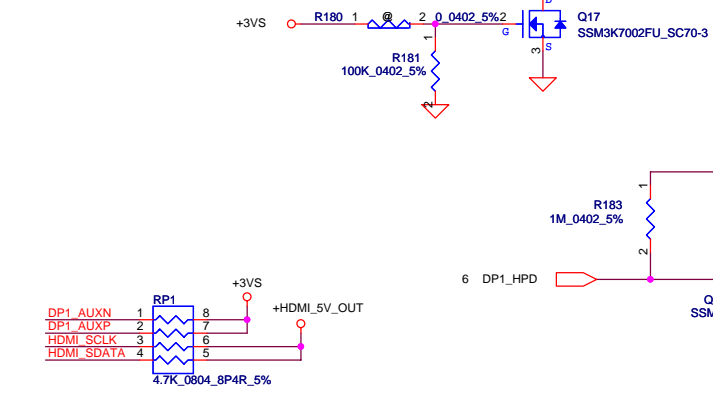
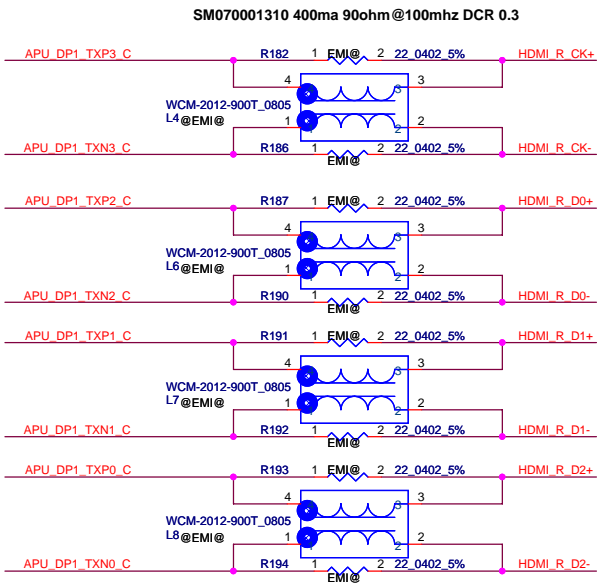
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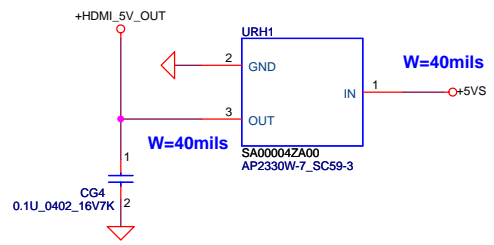
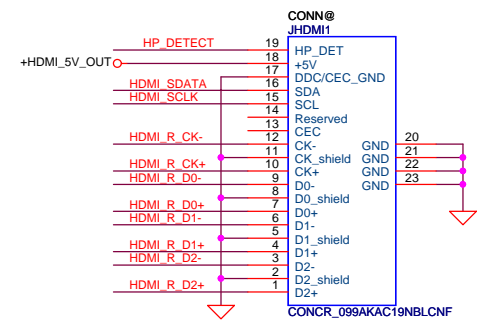
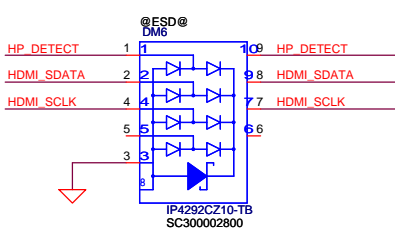
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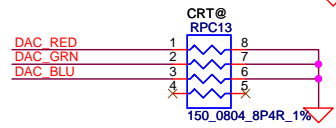
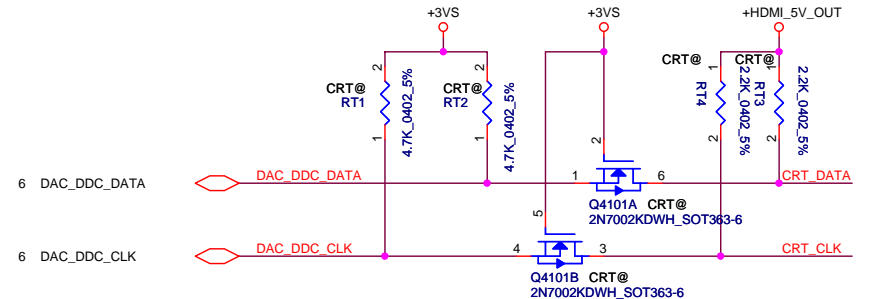
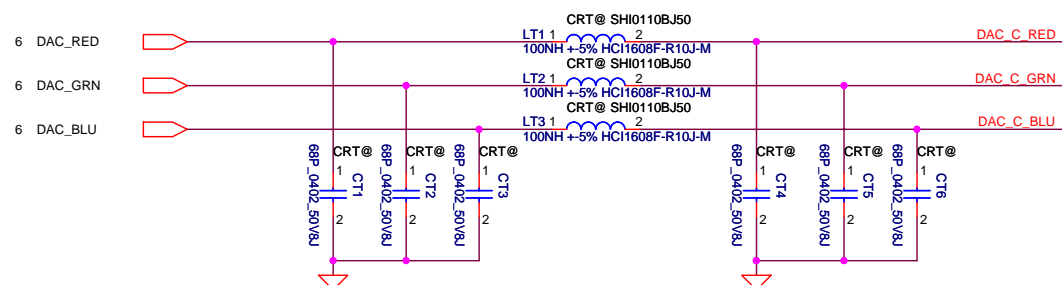
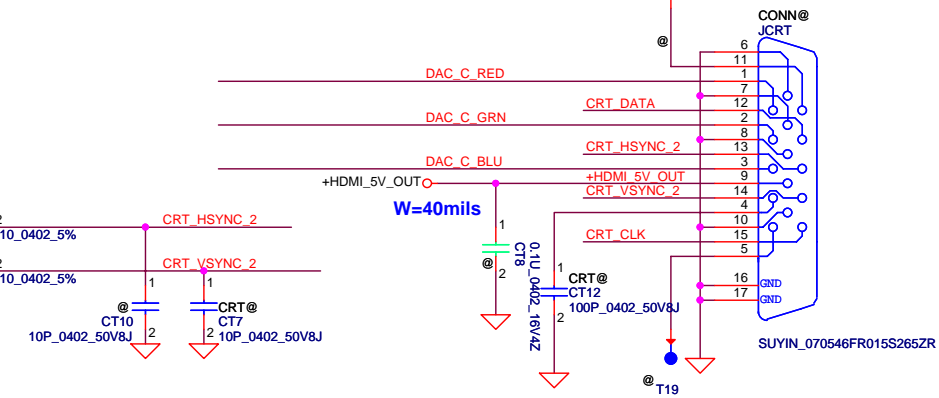
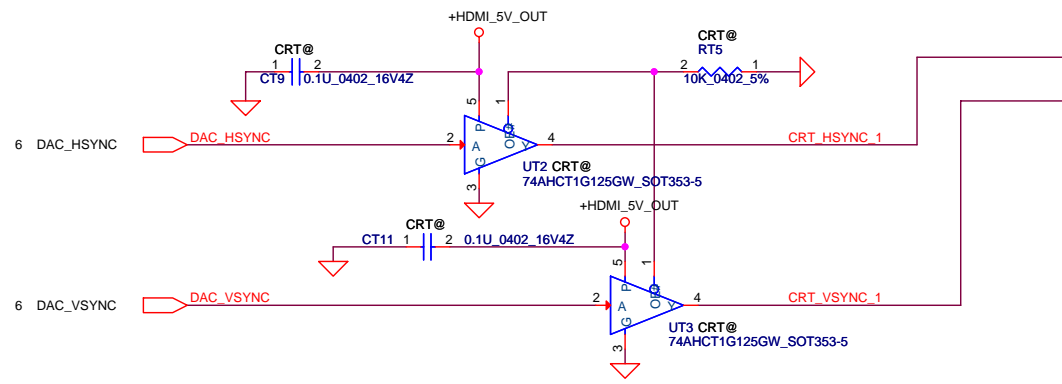
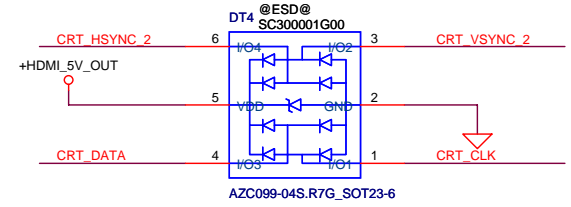
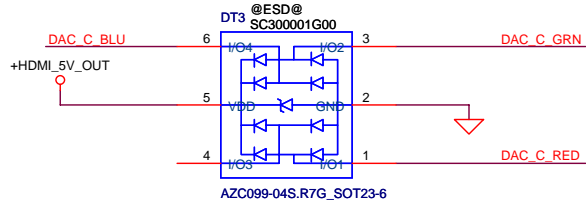


8/20 change HDMI Conn HDMI Conn.

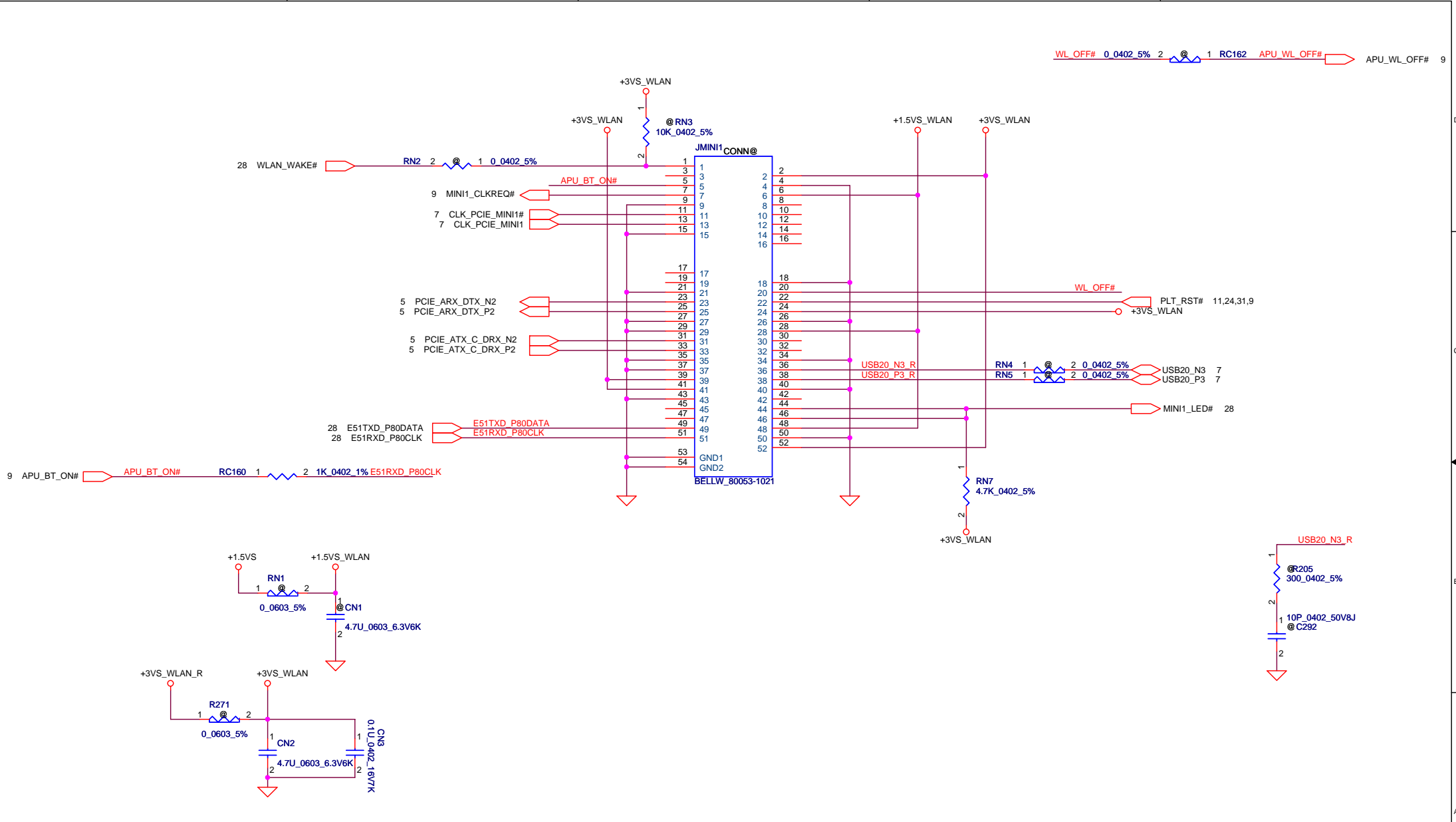


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CRT share HDMI Power

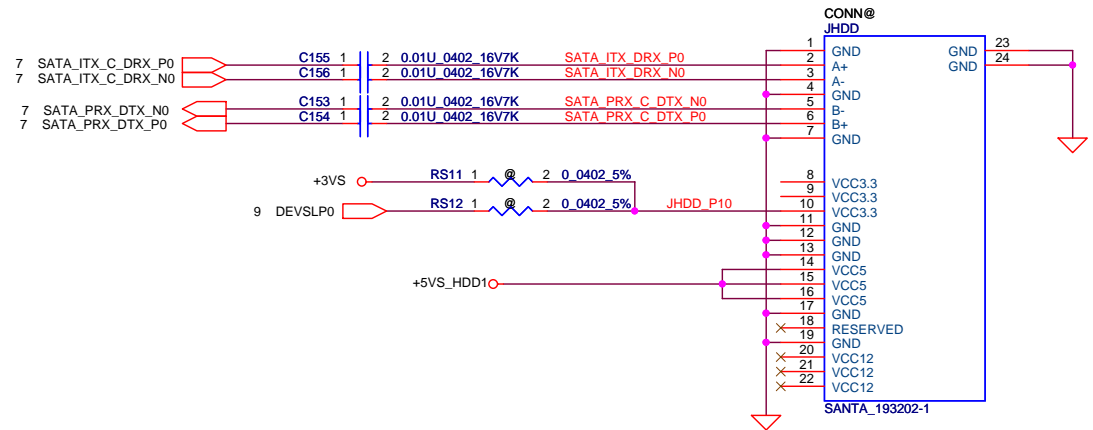
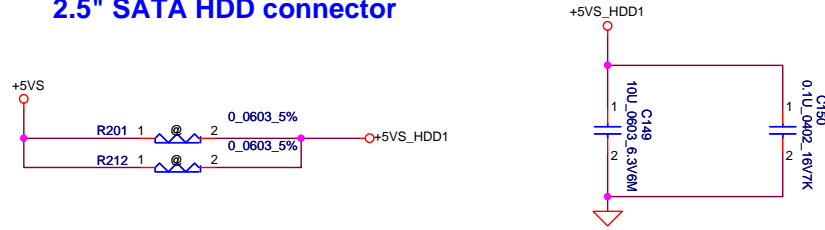


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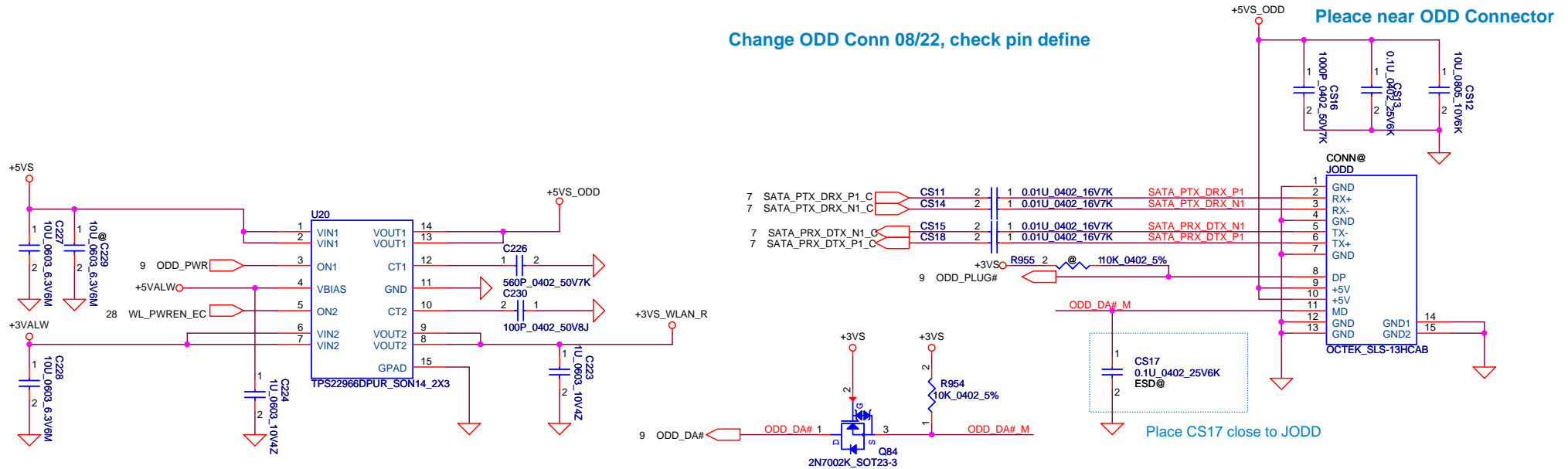


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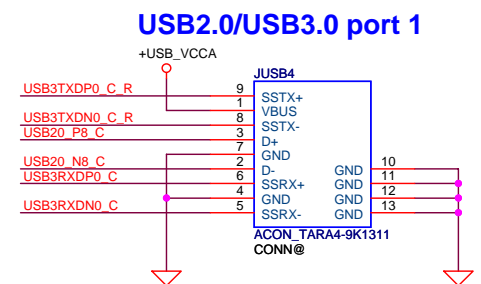
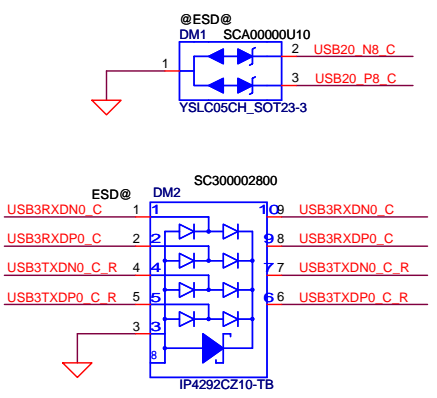
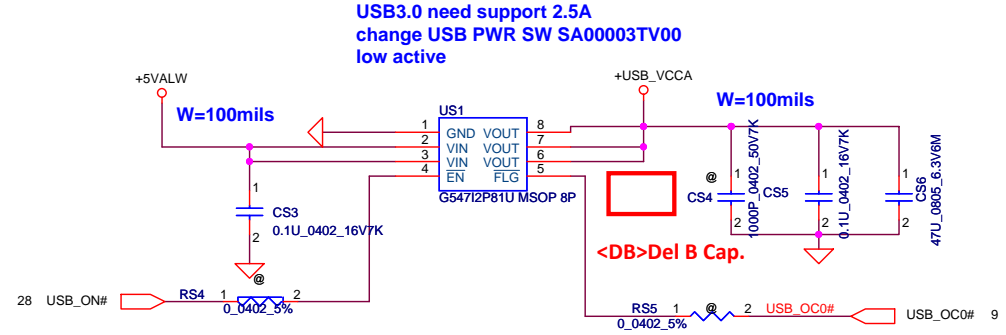
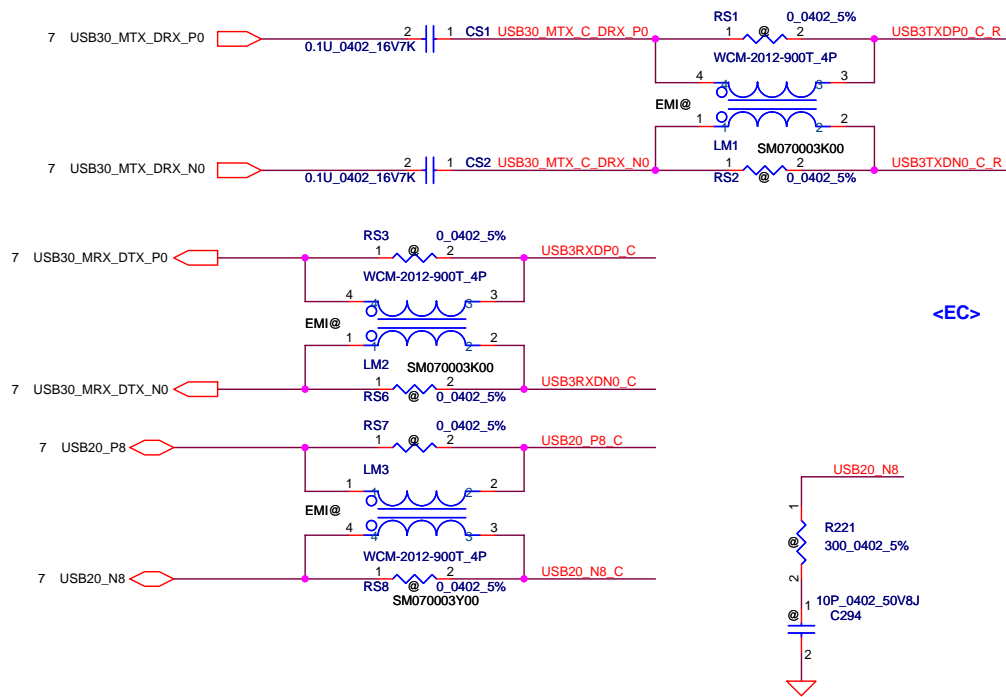
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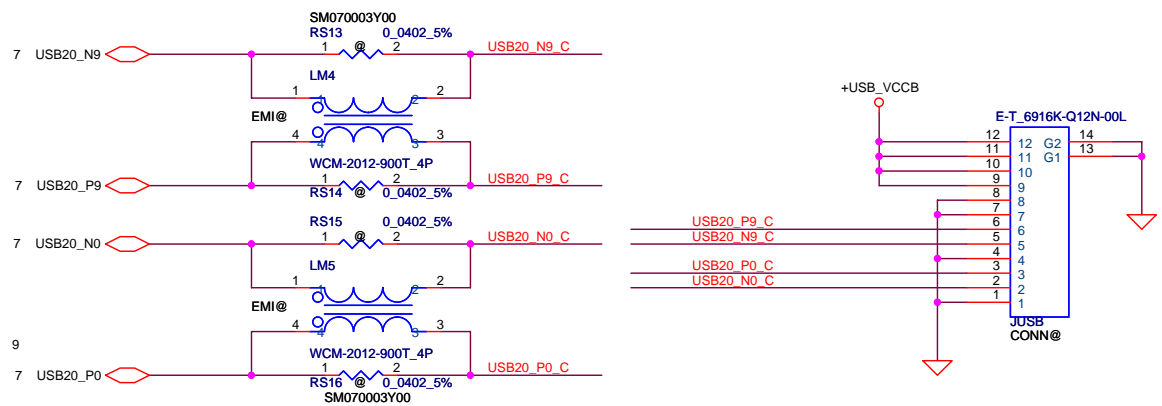
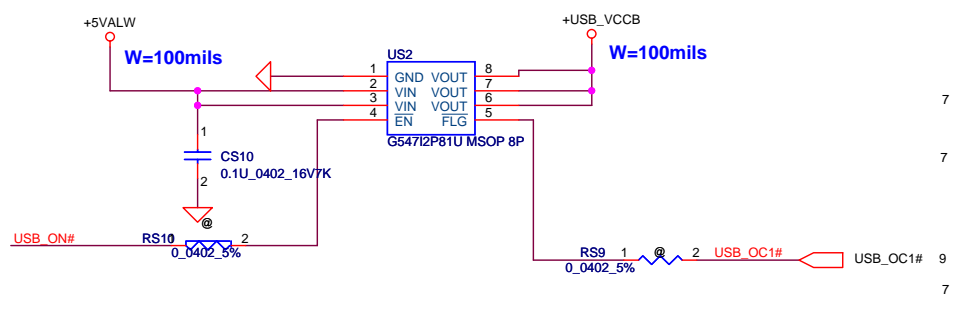
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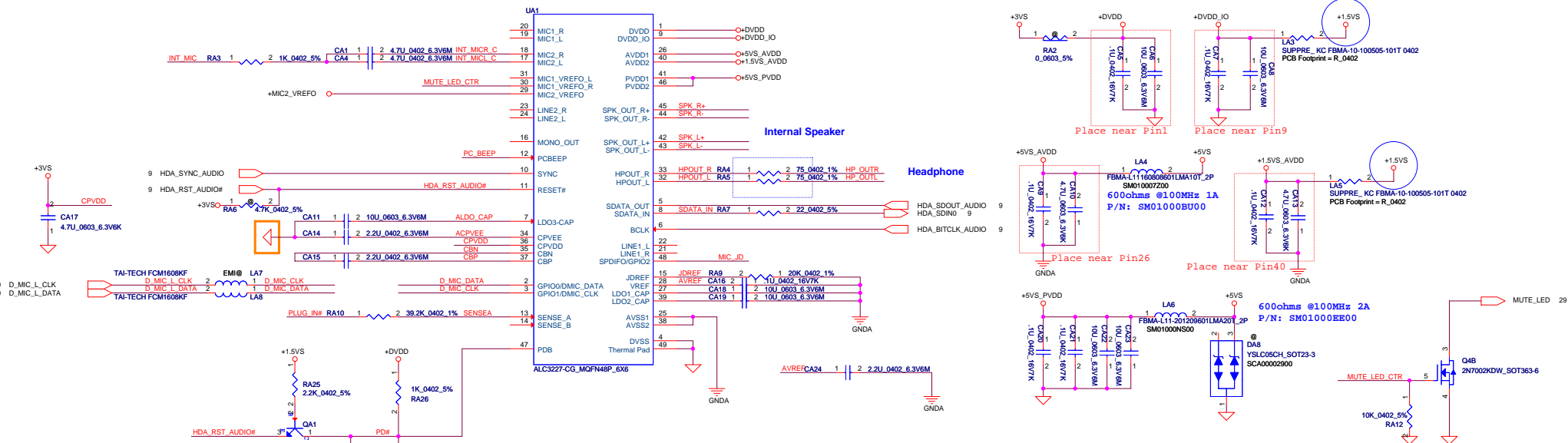
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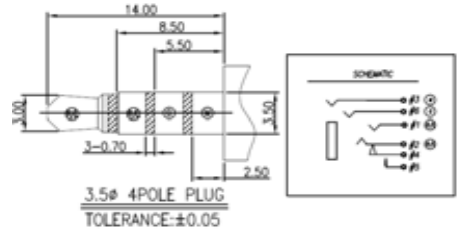
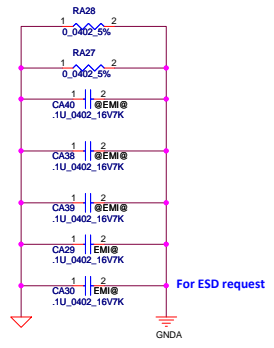
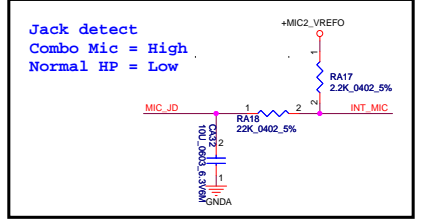
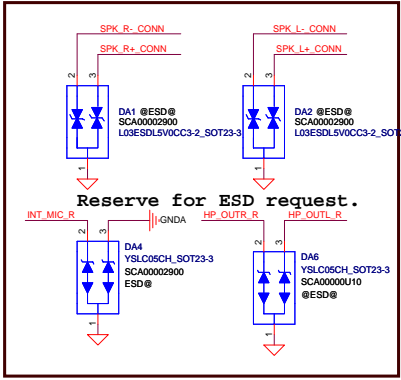
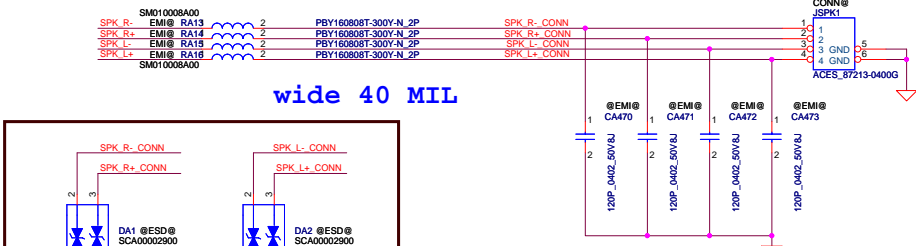
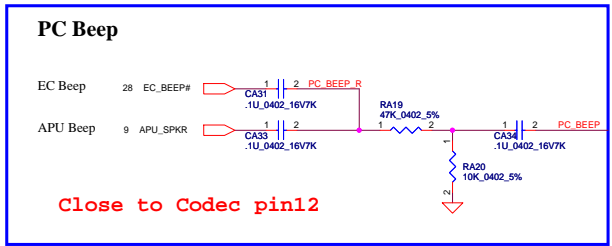
USB2.0 port x 2



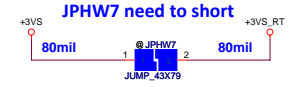
Security Classification		Compal Secret Data		Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	USB 3.0/2.0 conn	
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				LA-A996P	0.1
Date: Friday, February 21, 2014				Sheet	25 of 46



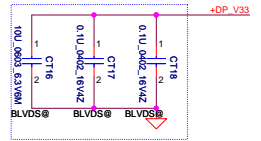
Power down (PD#) power stage for save power
 0V: Power down power stage
 3.3V: Power up power stage



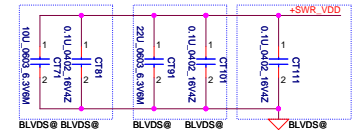
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2013/01/04	Deciphered Date	2015/01/04	AUDIO ALC259-VC2-CG			
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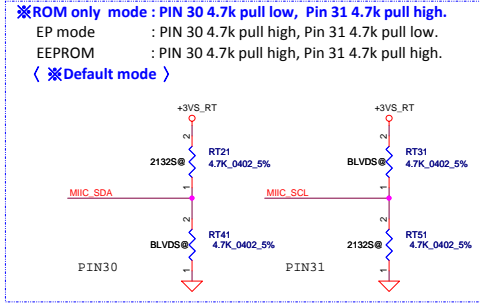
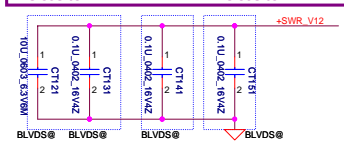
Layout note
Close to Pin3



Layout note
Close to LT5 Close to Pin18 Close to Pin13

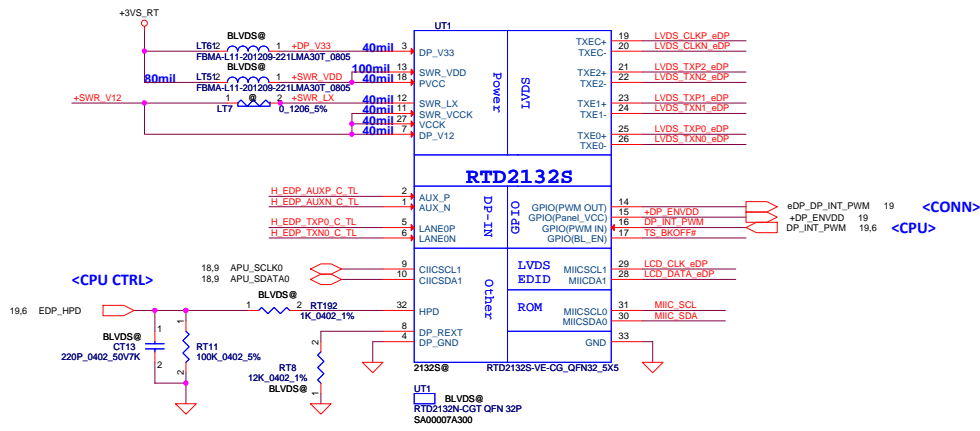


Layout note
Close to Pin11 Pin27 Close to Pin7

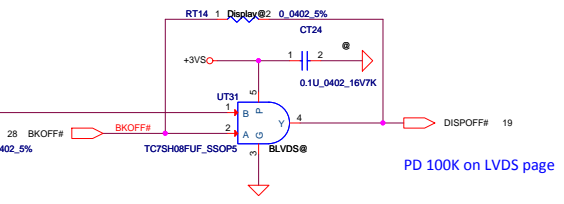


	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

※ If use 2132N, please select LDO mode as default.



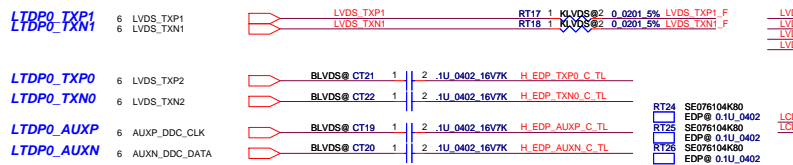
Layout note
Close to Pin8



PD 100k on LVDS page



<CPU>



RP40 Close CPU

RT24~27 Close JLVDS conn

LTPDO_TXP2	RT33	1	Display@2	0.0402 5%	LVDS_TXP2_K	RT24	1	KLVDSE@2	0.0402 5%	LVDS_TXP2_F
LVDS_TXN2	RT34	1	Display@2	0.0402 5%	LVDS_TXN2_K	RT25	1	KLVDSE@2	0.0402 5%	LVDS_TXP2_F
AUXP_DDC_CLK	RT35	1	Display@2	0.0402 5%	AUXP_DDC_CLK_K	RT26	1	KLVDSE@2	0.0402 5%	LCD_CLK
AUXN_DDC_DATA	RT36	1	Display@2	0.0402 5%	AUXN_DDC_DATA_K	RT27	1	KLVDSE@2	0.0402 5%	LCD_DATA

	display@	EDP@	KLVDSE@	BLVDSE@	Kabini@	Beema@
Kabini LVDS	V		V		V	
Kabini EDP	V	V			V	
Beema LVDS				V		V
Beema EDP	V	V				V

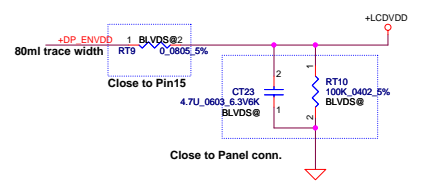
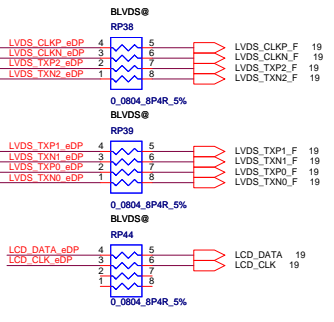
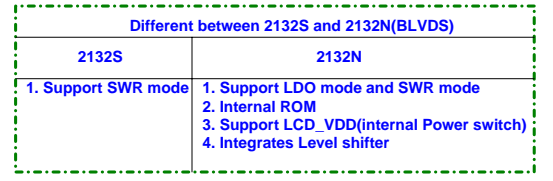


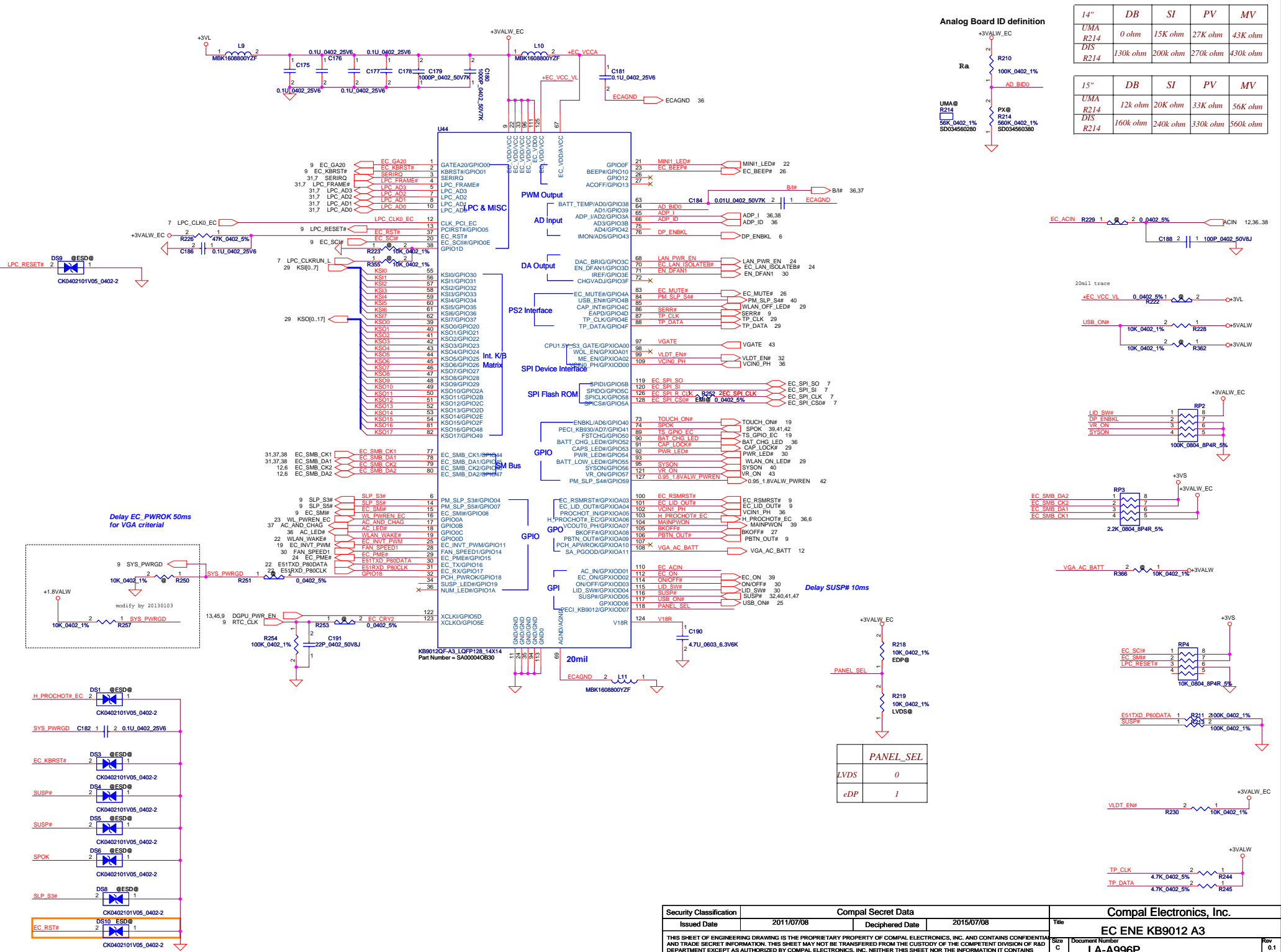
	PIN15
2132S	TL_ENVDD
BLVDS	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
BLVDS	1.5-3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform





Analog Board ID definition

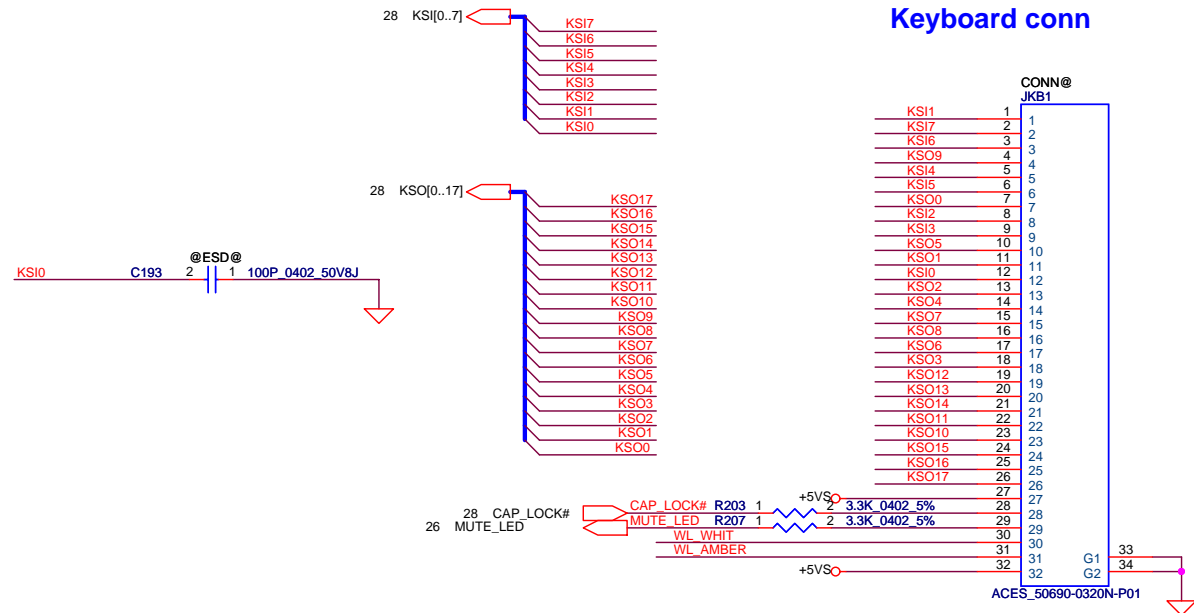
14"	DB	SI	PV	MV
UMA	0 ohm	15K ohm	27K ohm	43K ohm
R214	130k ohm	200k ohm	270k ohm	430k ohm

15"	DB	SI	PV	MV
UMA	12k ohm	20K ohm	33k ohm	56k ohm
R214	160k ohm	240k ohm	330k ohm	560k ohm

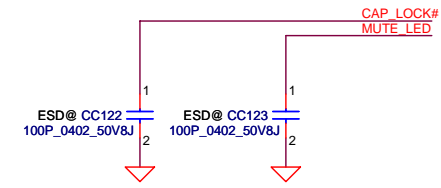
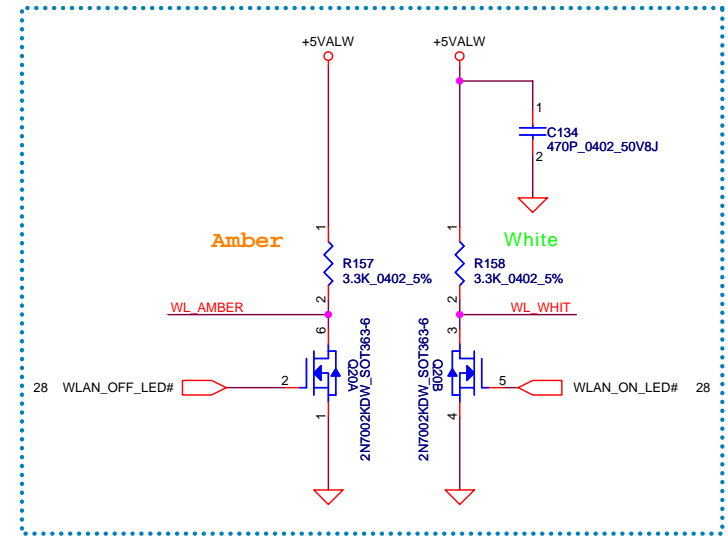
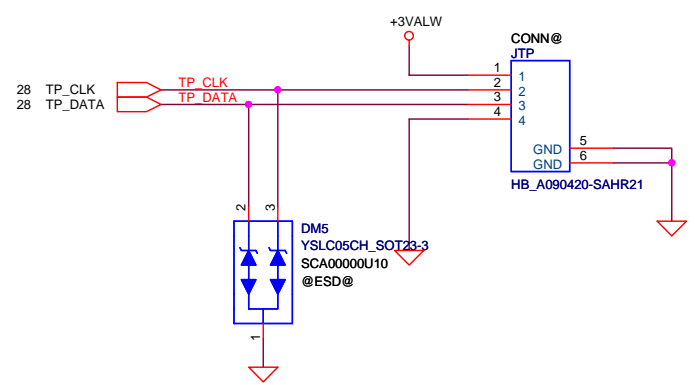
PANEL_SEL	
LVDS	0
eDP	1

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Issued Date	2011/07/08	Deciphered Date	2015/07/08	EC ENE KB9012 A3	
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Date	Wednesday, March 26, 2014	Sheet	28	of	46

Keyboard conn

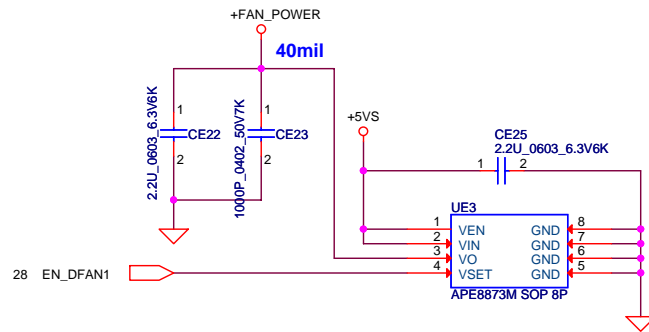
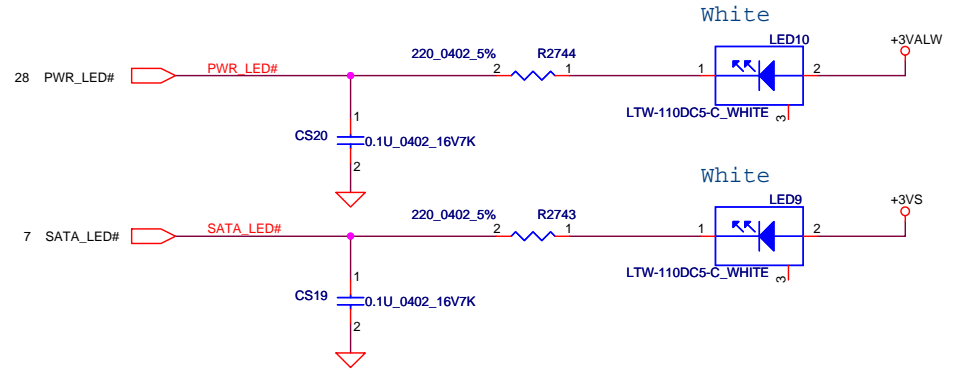
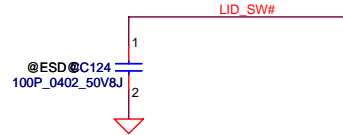
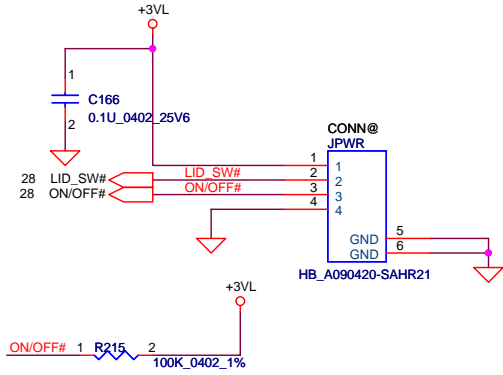


Touch pad conn

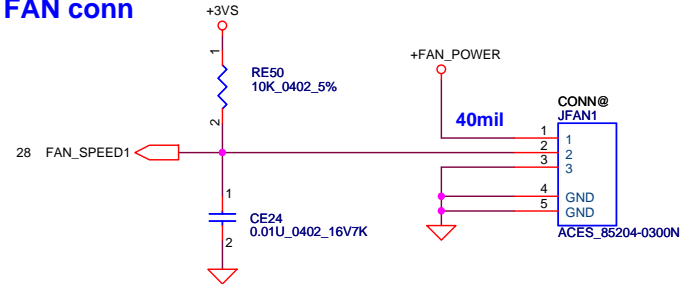


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Date: Monday, February 17, 2014								Sheet 29 of 46		Document Number LA-A996P	

Power Button Connector

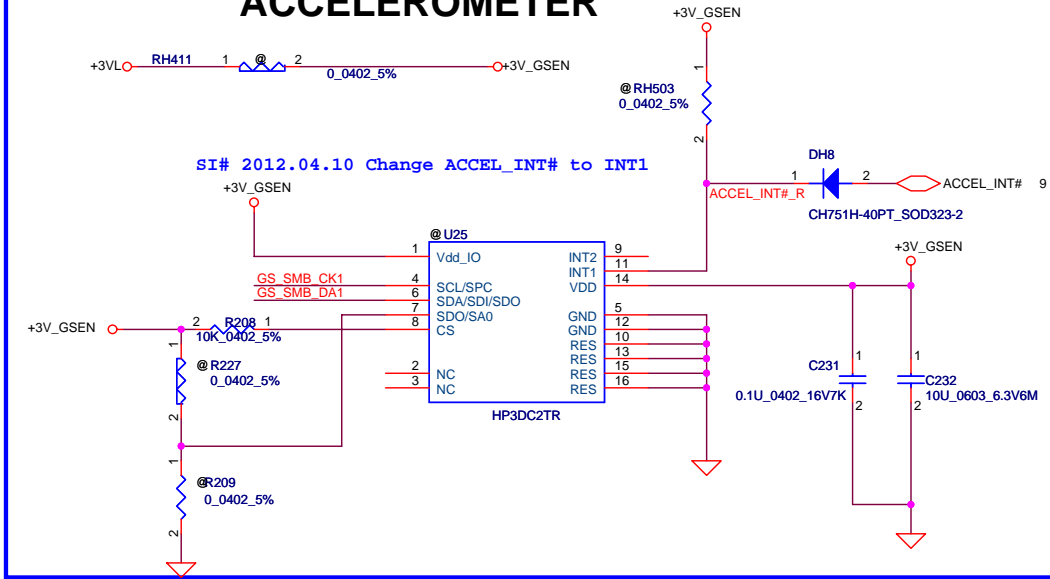


FAN conn



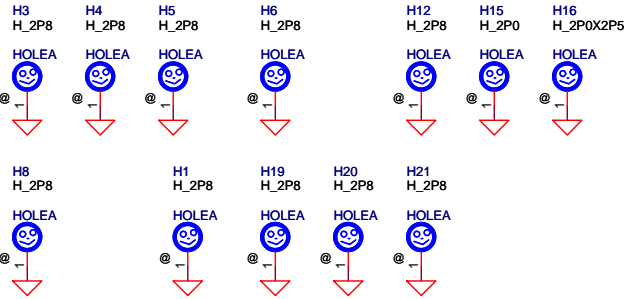
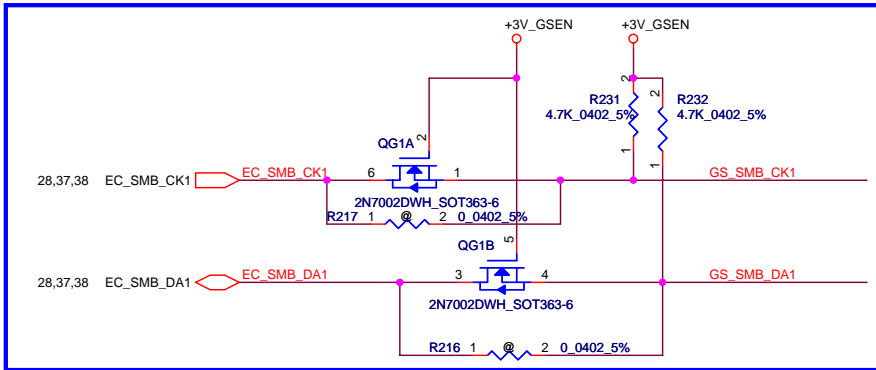
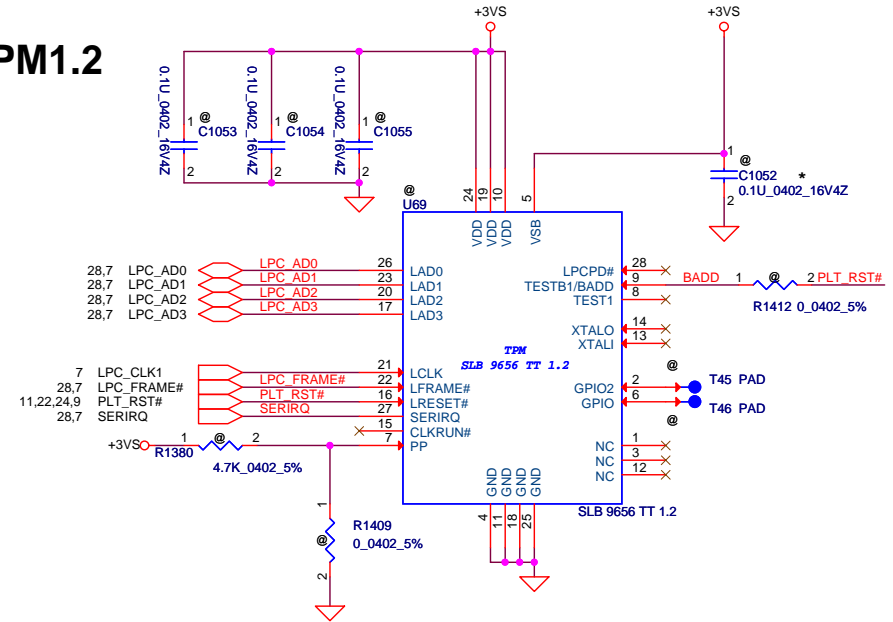
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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ACCELEROMETER

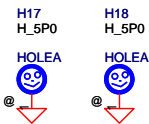


Add TPM Circuit in PV Phase

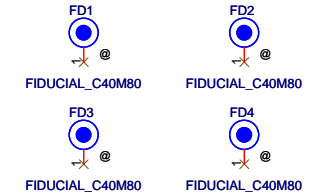
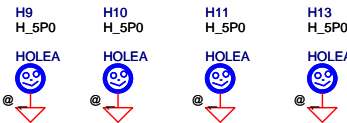
TPM1.2



VGA

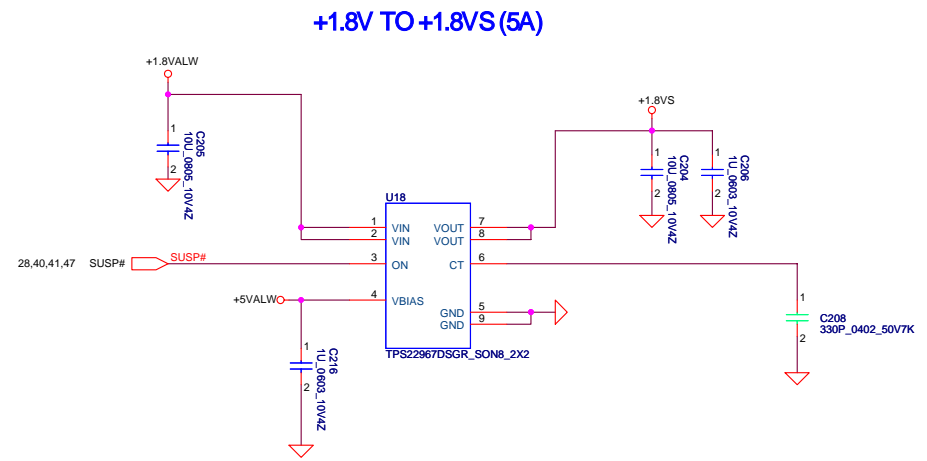
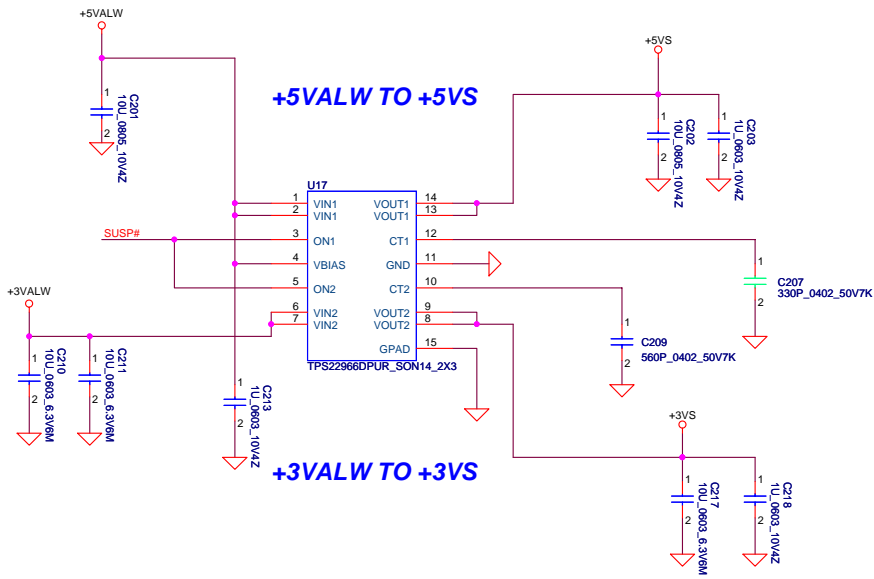


CPU

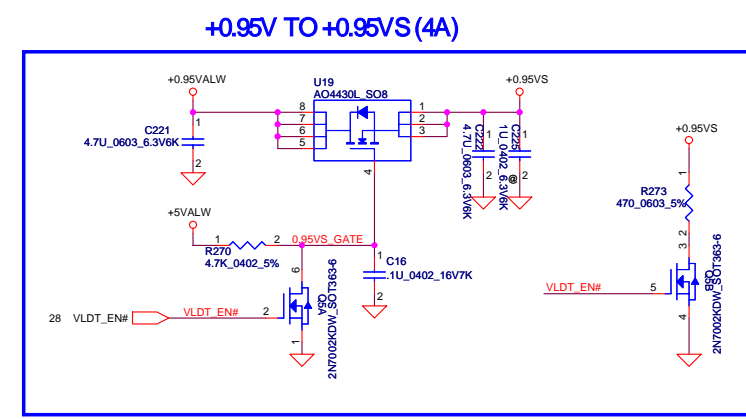


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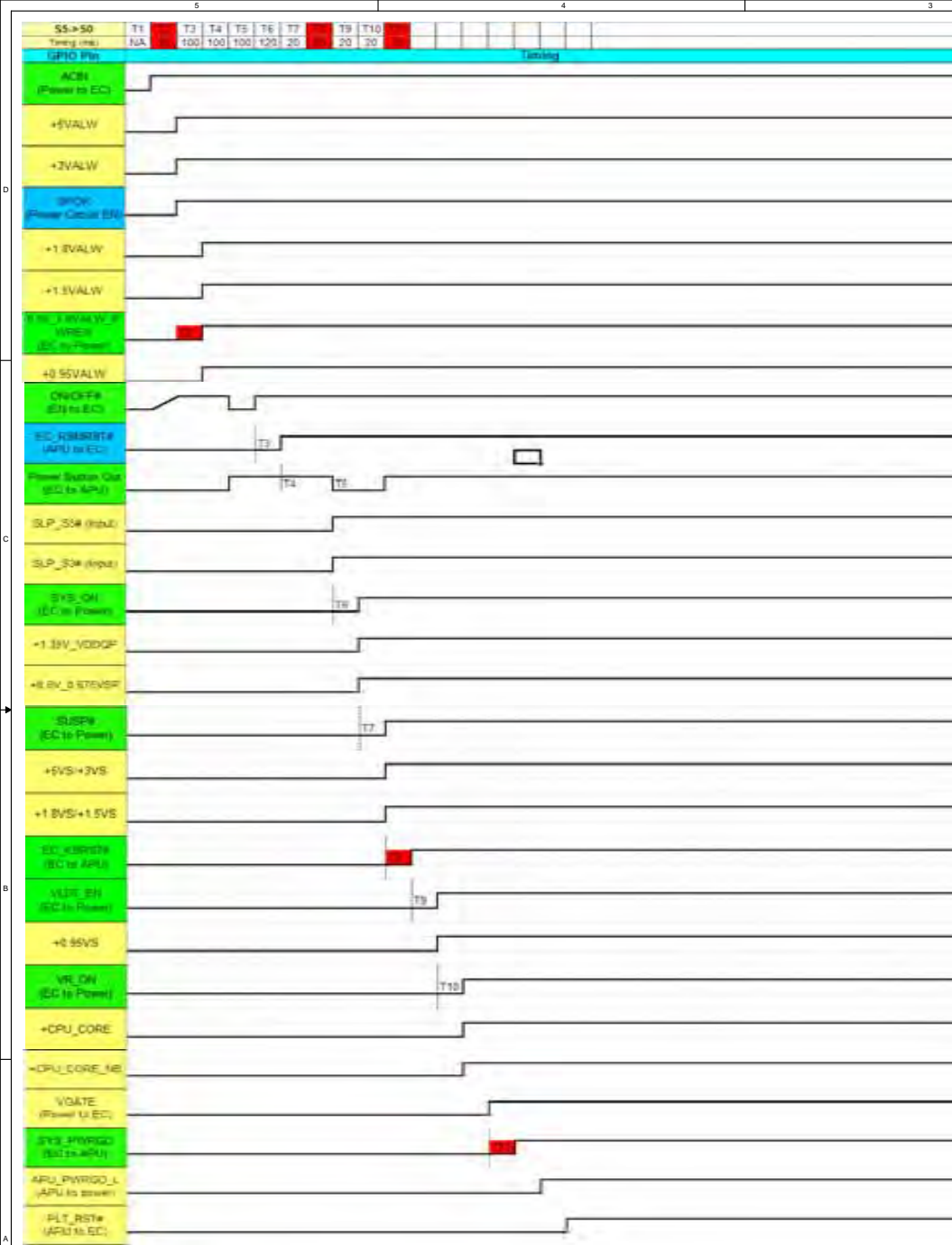
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Size			LED/Screw hole
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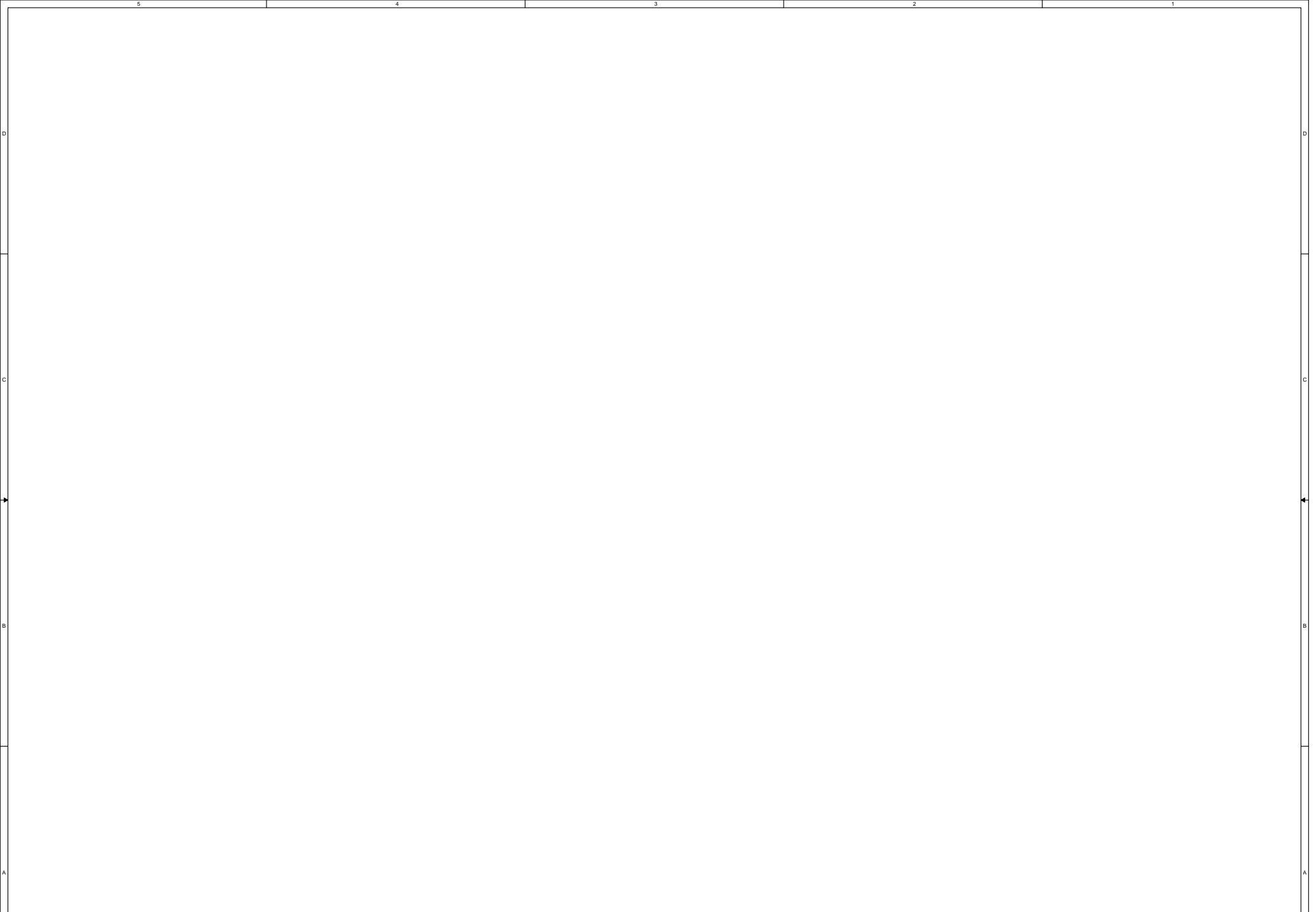
+1.5V TO +1.5VS (2A)



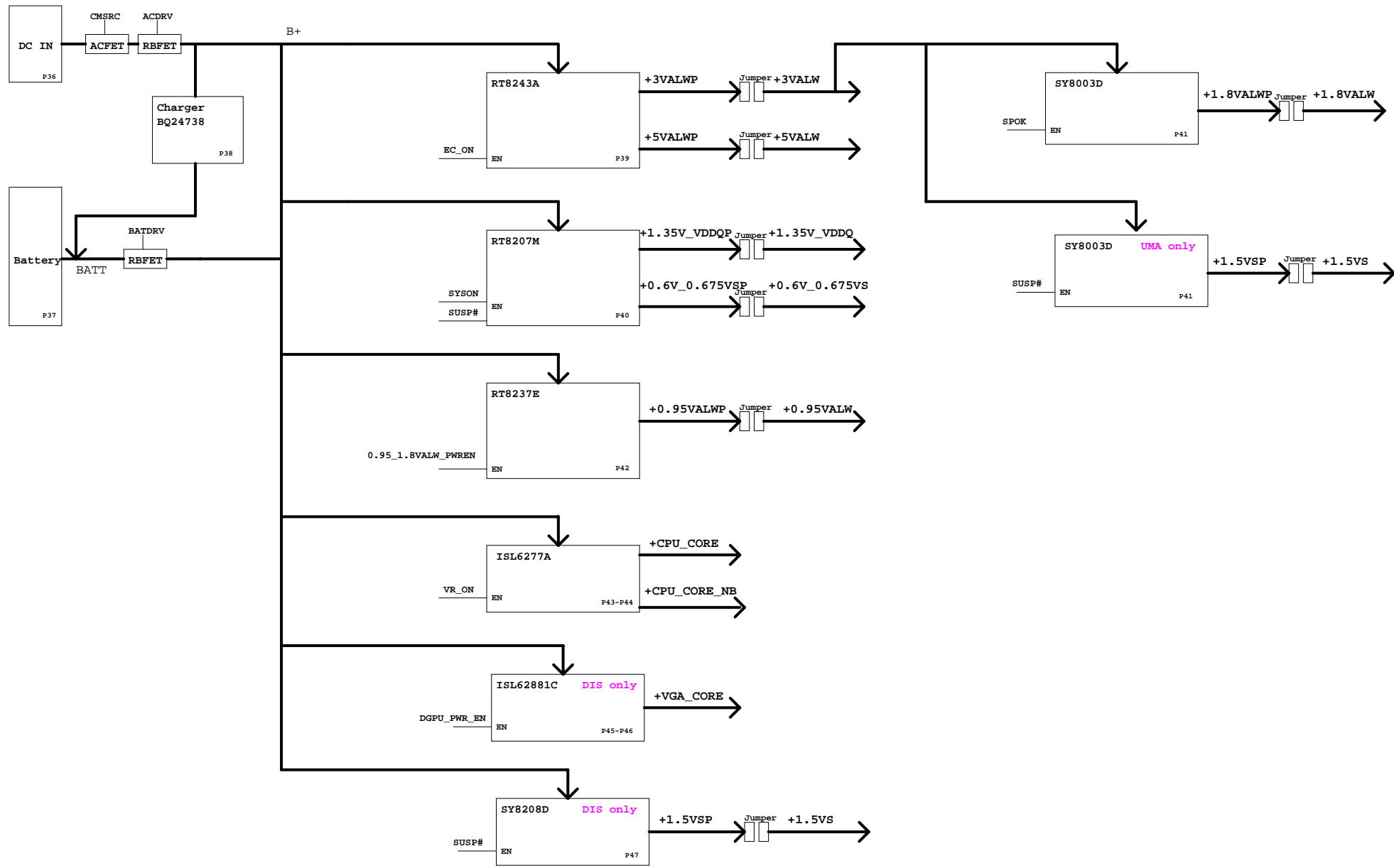
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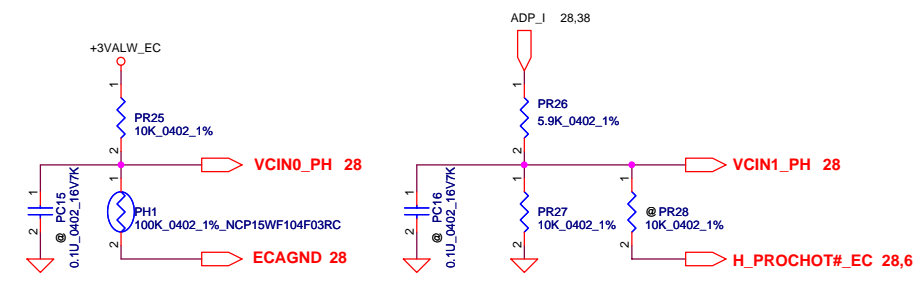
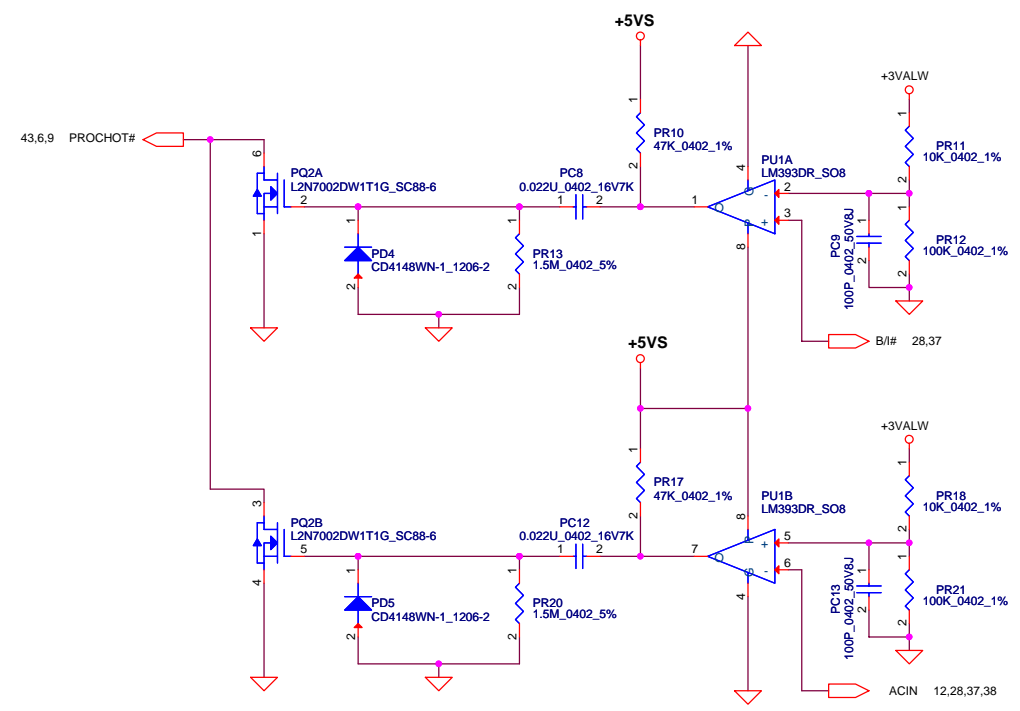
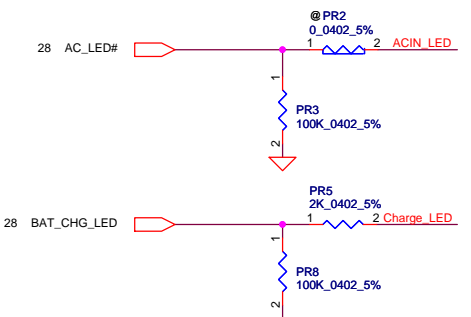
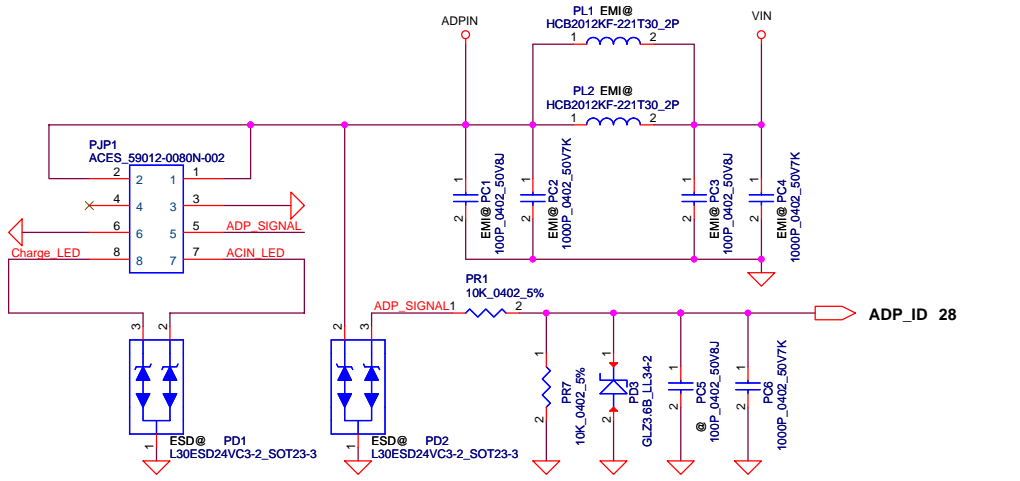
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	Power sequence
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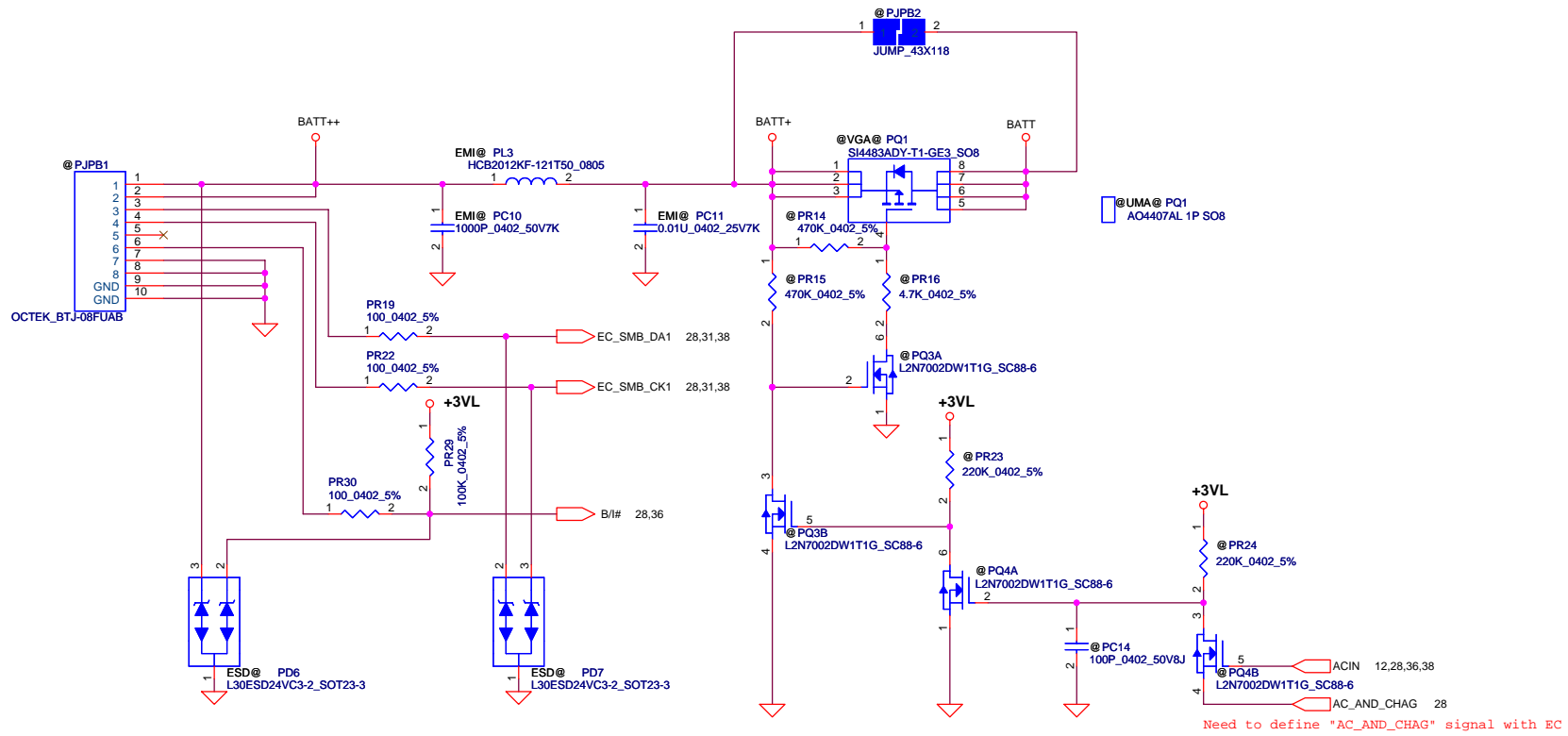
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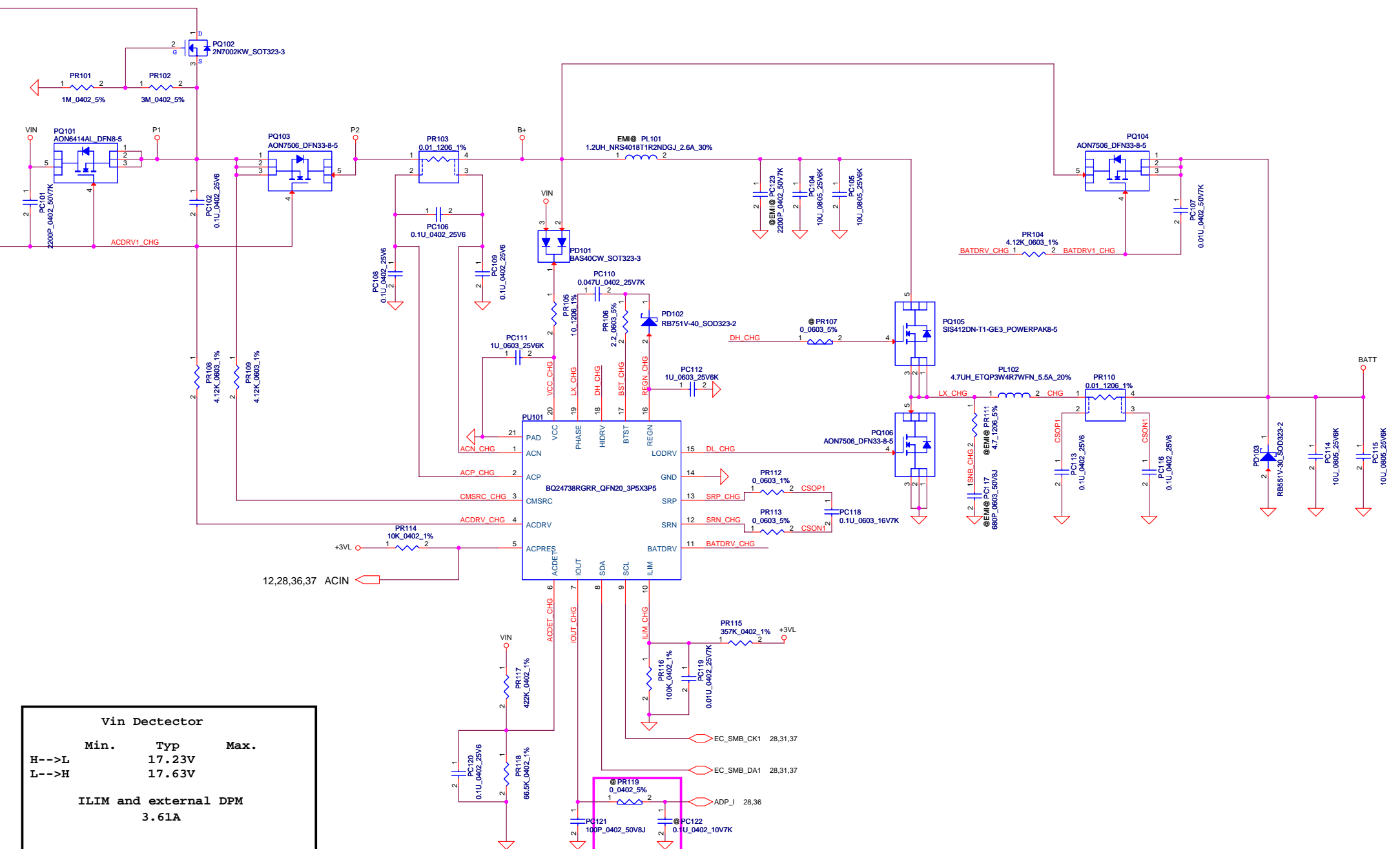
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				LA-A996P
Date: Tuesday, February 25, 2014				Sheet 36 of 47



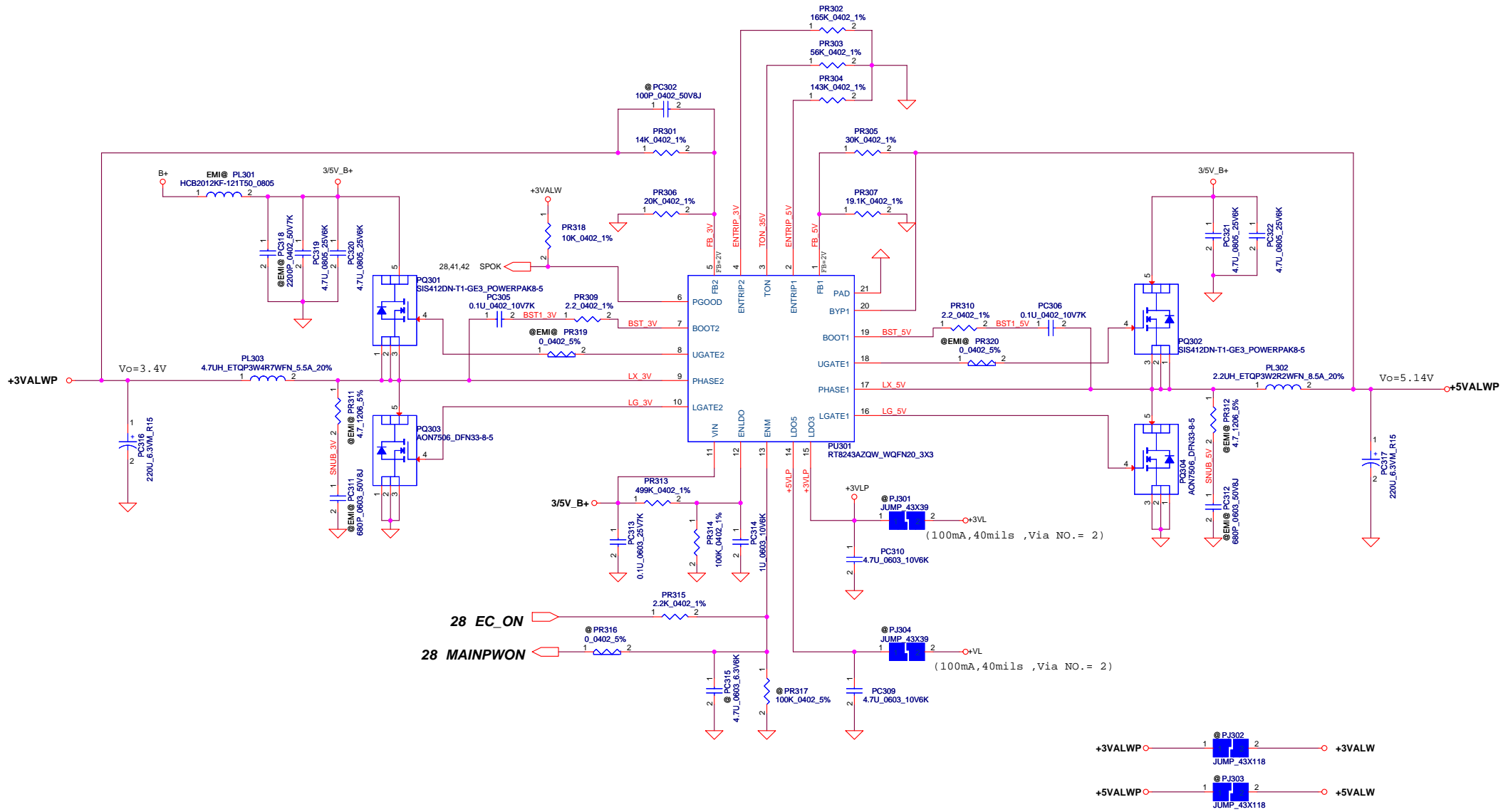
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	BATT Conn
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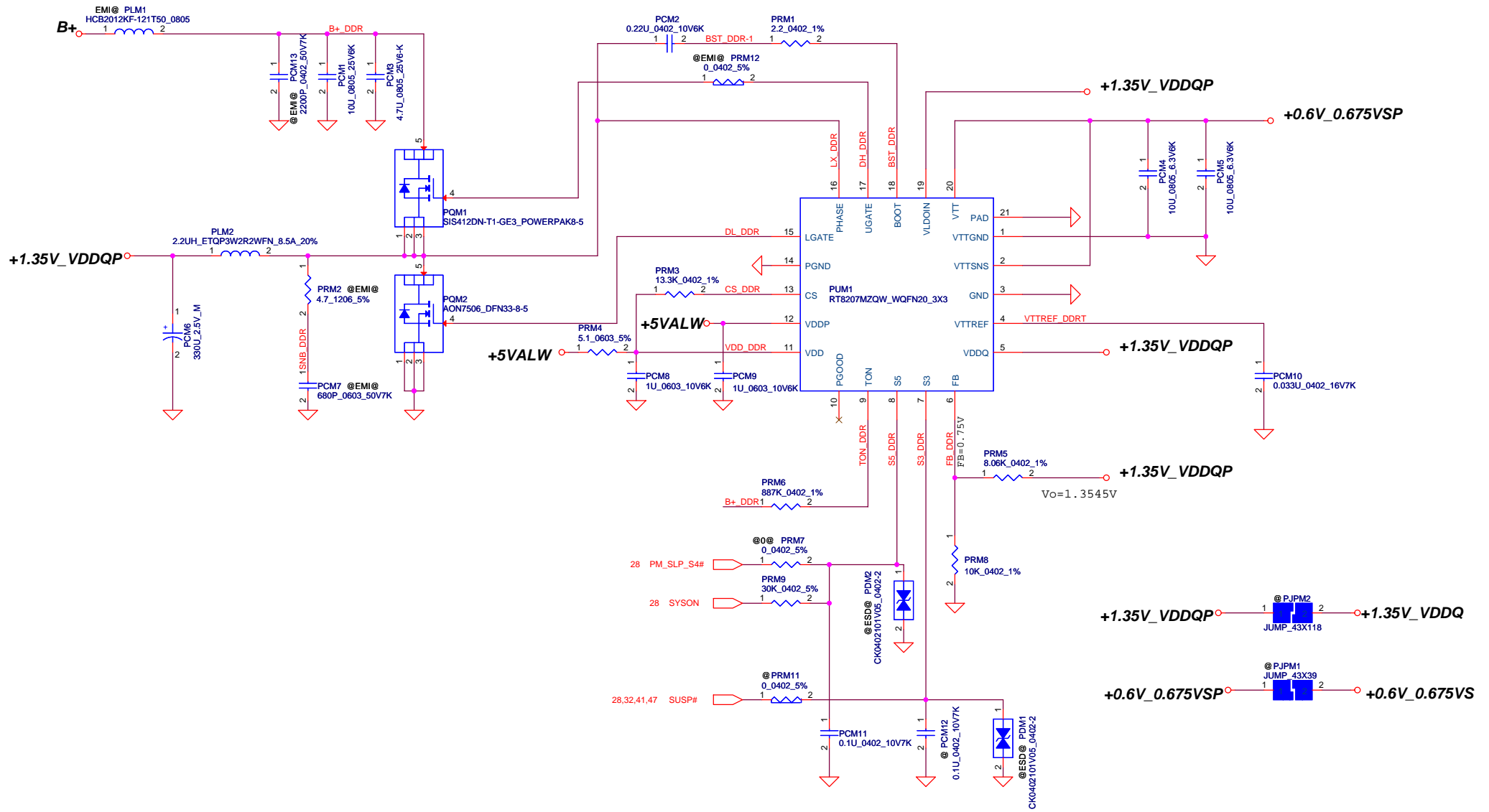
Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
		3.61A	

Please locate the RC
Near EC chip
2011-02-22

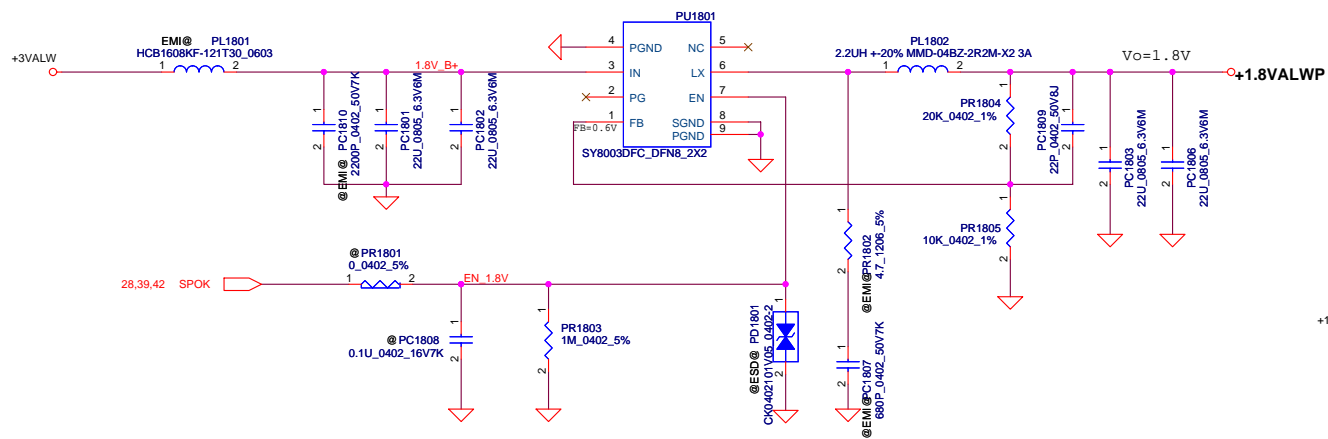
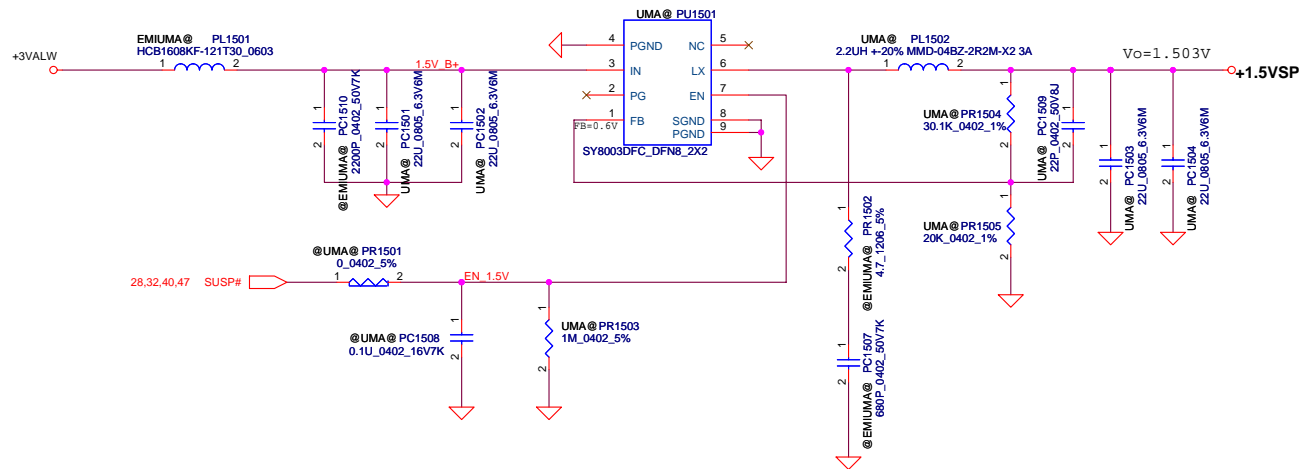
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	CHARGER
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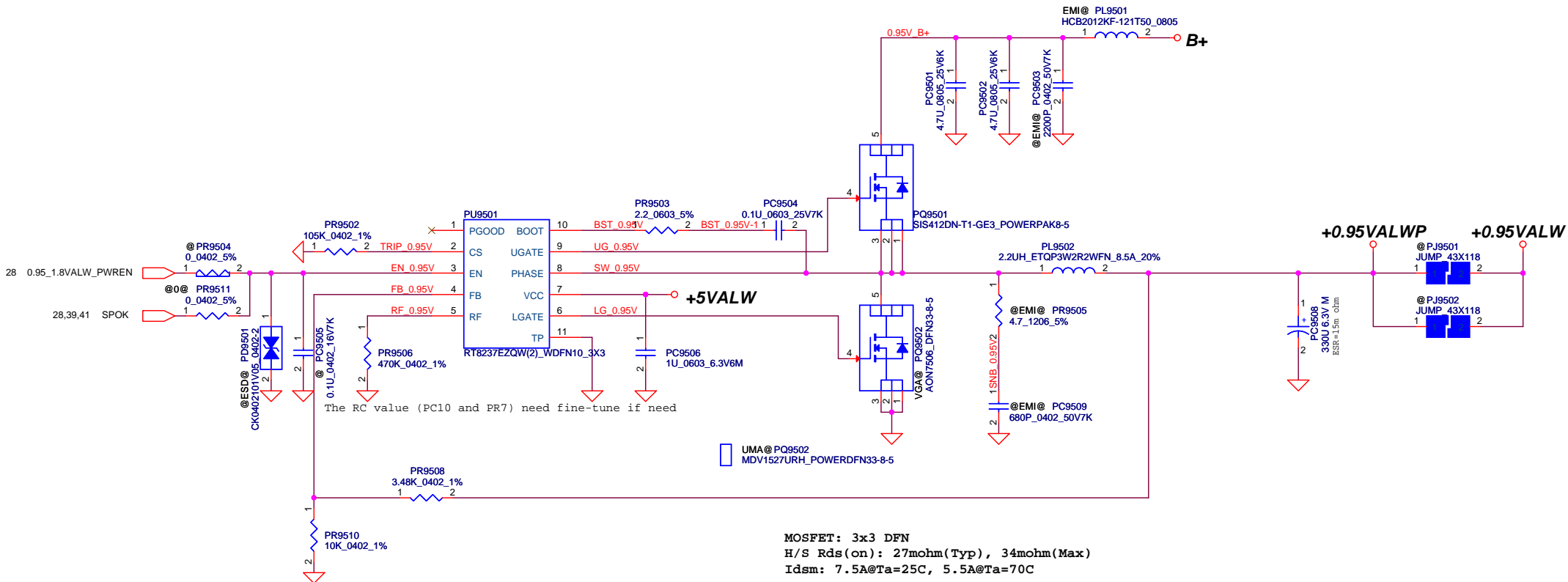
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title
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The RC value (PC10 and PR7) need fine-tune if need

UMA@ PQ9502
MDV1527URH_POWERDFN33-8-5

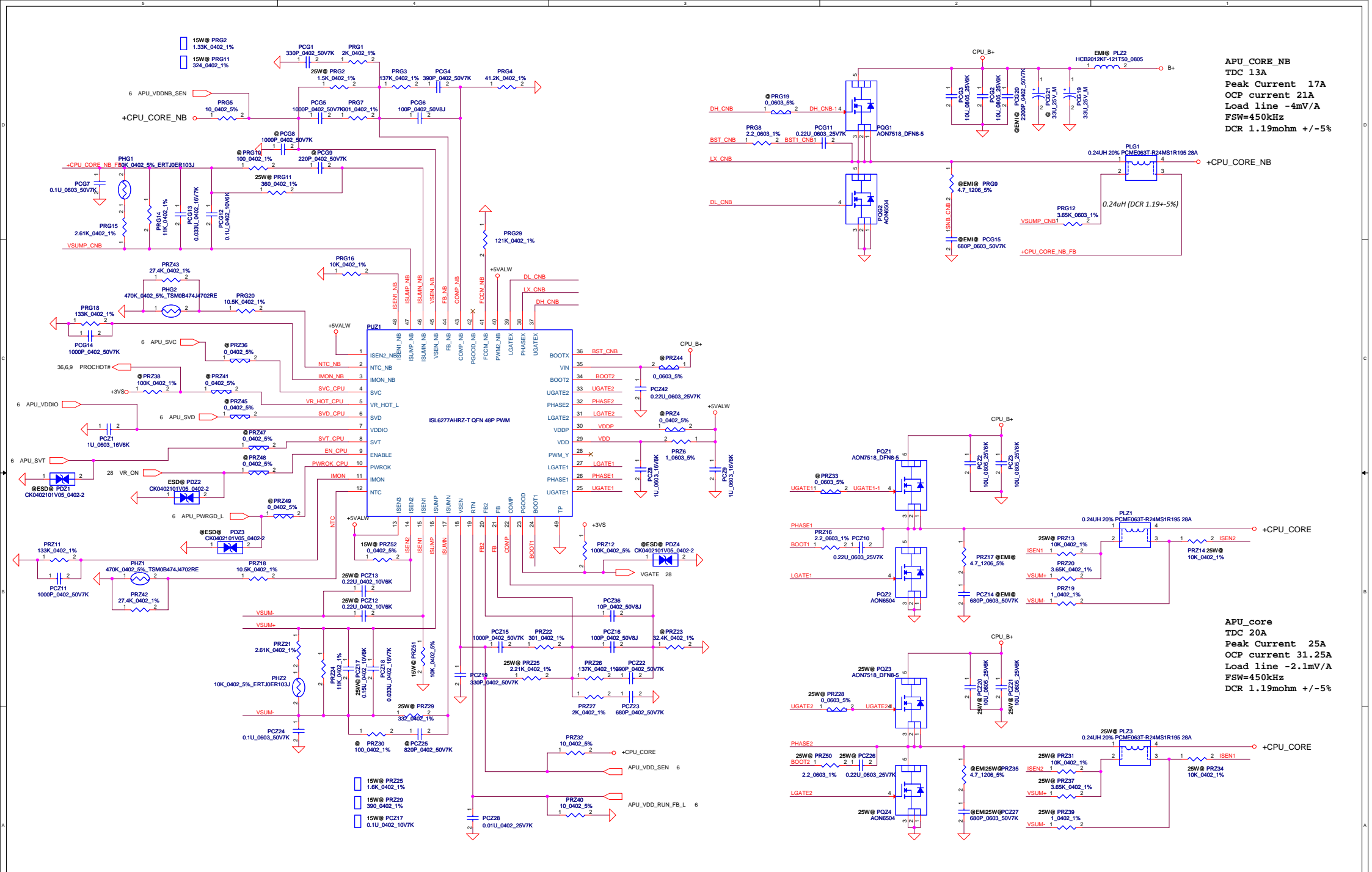
MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Imax=8A
OCP~10.977A
OVP: 120%~130%
VFB=0.704V, Vout=0.949V
MOSFET footprint: SIS412DN

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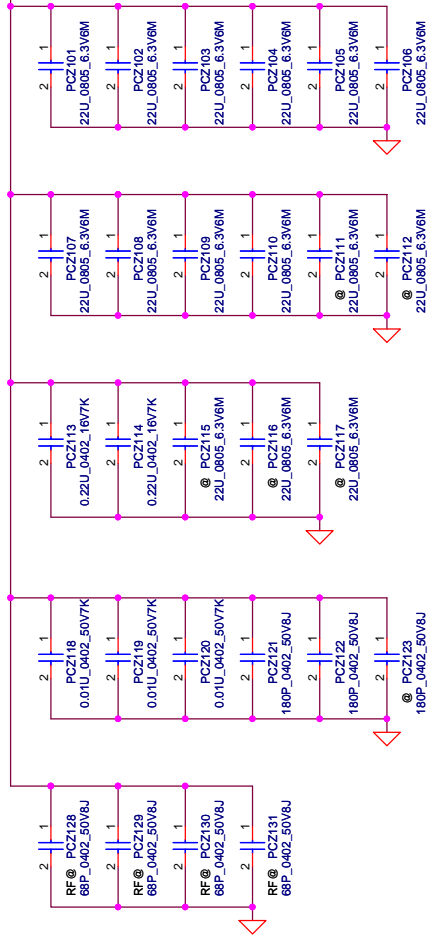
APU_CORE_NB
 TDC 13A
 Peak Current 17A
 OCP current 21A
 Load line -4mV/A
 FSW=450kHz
 DCR 1.19mohm +/-5%

APU_core
 TDC 20A
 Peak current 31.25A
 OCP current 31.25A
 Load line -2.1mV/A
 FSW=450kHz
 DCR 1.19mohm +/-5%

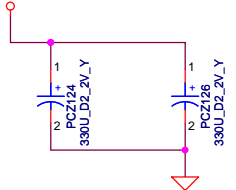
Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/07	Deciphered Date	2012/11/07	CPU CORE/CPU CORE NB	
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+CPU_CORE

+CPU_CORE

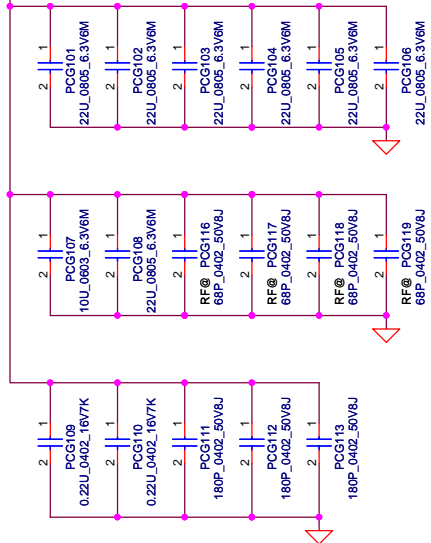


+CPU_CORE Local

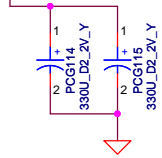


+CPU_CORE_NB

+CPU_CORE_NB



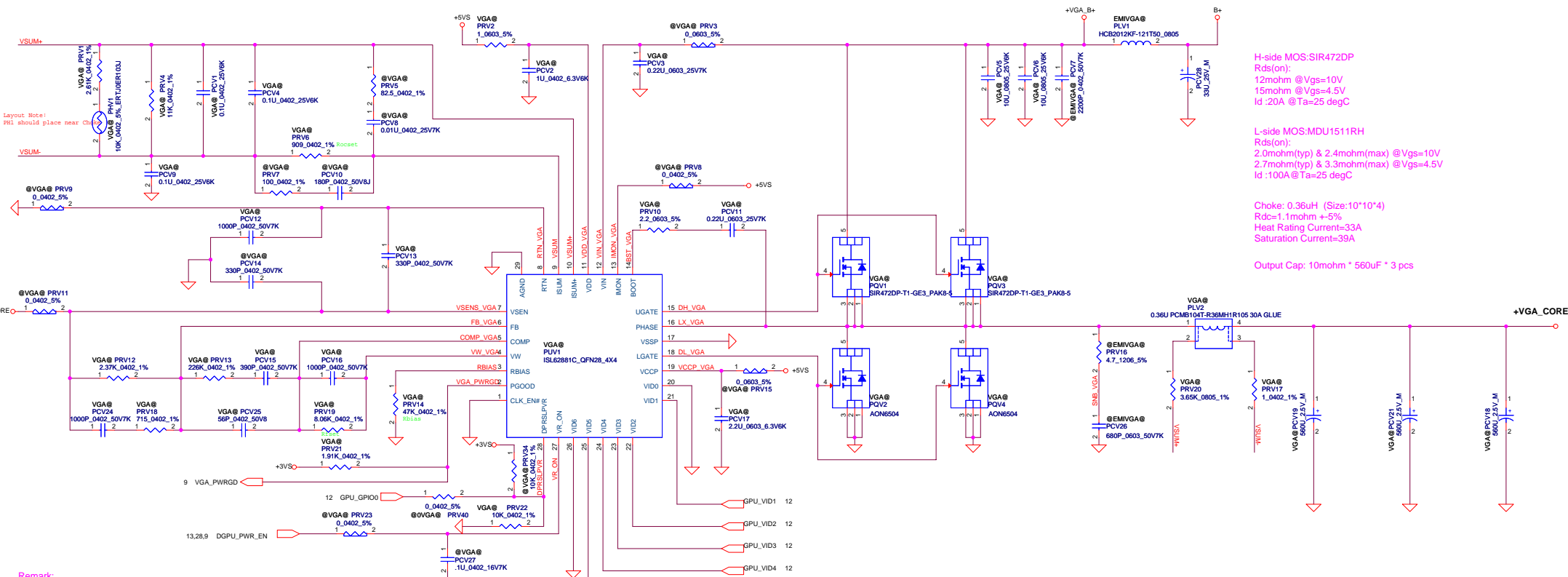
+CPU_CORE_NB Local



	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
+CPU_CORE	2	10	2		3	2
+CPU_CORE_NB	2	7	2	1		3

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)



H-side MOS: SIR472DP
Rds(on):
12mohm @Vgs=10V
15mohm @Vgs=4.5V
Id:20A @Ta=25 degC

L-side MOS: MDU1511RH
Rds(on):
2.0mohm(typ) & 2.4mohm(max) @Vgs=10V
2.7mohm(typ) & 3.3mohm(max) @Vgs=4.5V
Id :100A @Ta=25 degC

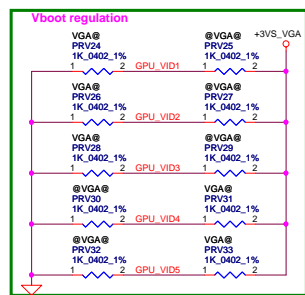
Choke: 0.36uH (Size:10*10*4)
Rdc=1.1mohm +5%
Heat Rating Current=33A
Saturation Current=39A

Output Cap: 10mohm * 560uF * 3 pcs

Remark:
1. Rbias=147K
=>set the controller for CPU_CORE application
Rbias=47k
=>set the controller for GPU_CORE application

2. Switching frequency setting:
Rset(kohm)=period(us)*0.29*2.65
=8.06kohm
Fsw=1/period(us)=300KHZ

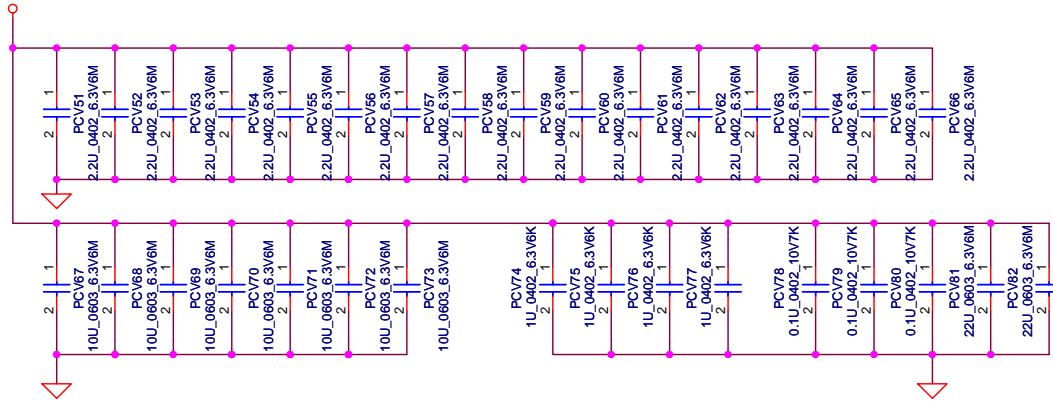
3. Operation mode:
When GPU_CORE VR application
DPRSLPVR (pin28)=0 => 1 phase CCM mode
DPRSLPVR (pin28)=1 => 1 phase DE mode



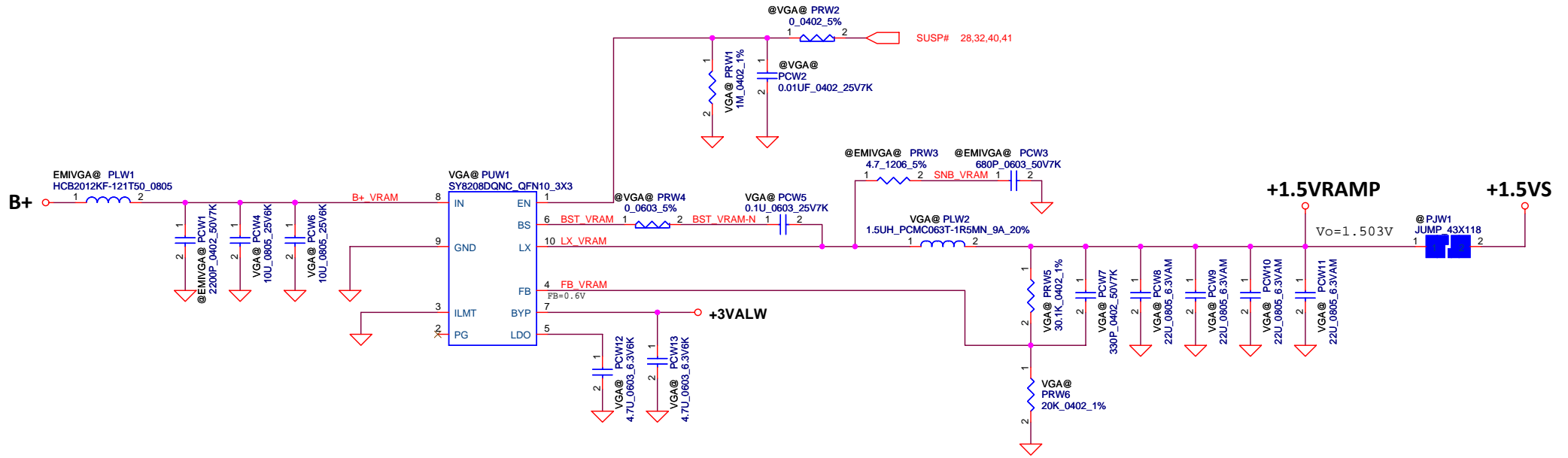
TDC 21A
Peak Current = 31.5A
OCP Current = 37.8A
Load line disable

Module model information:
ISL62881C_V1A for IC
ISL62881C_V1B for SW

+VGA_CORE



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