



PCB

DA600004Q00

Compal Confidential

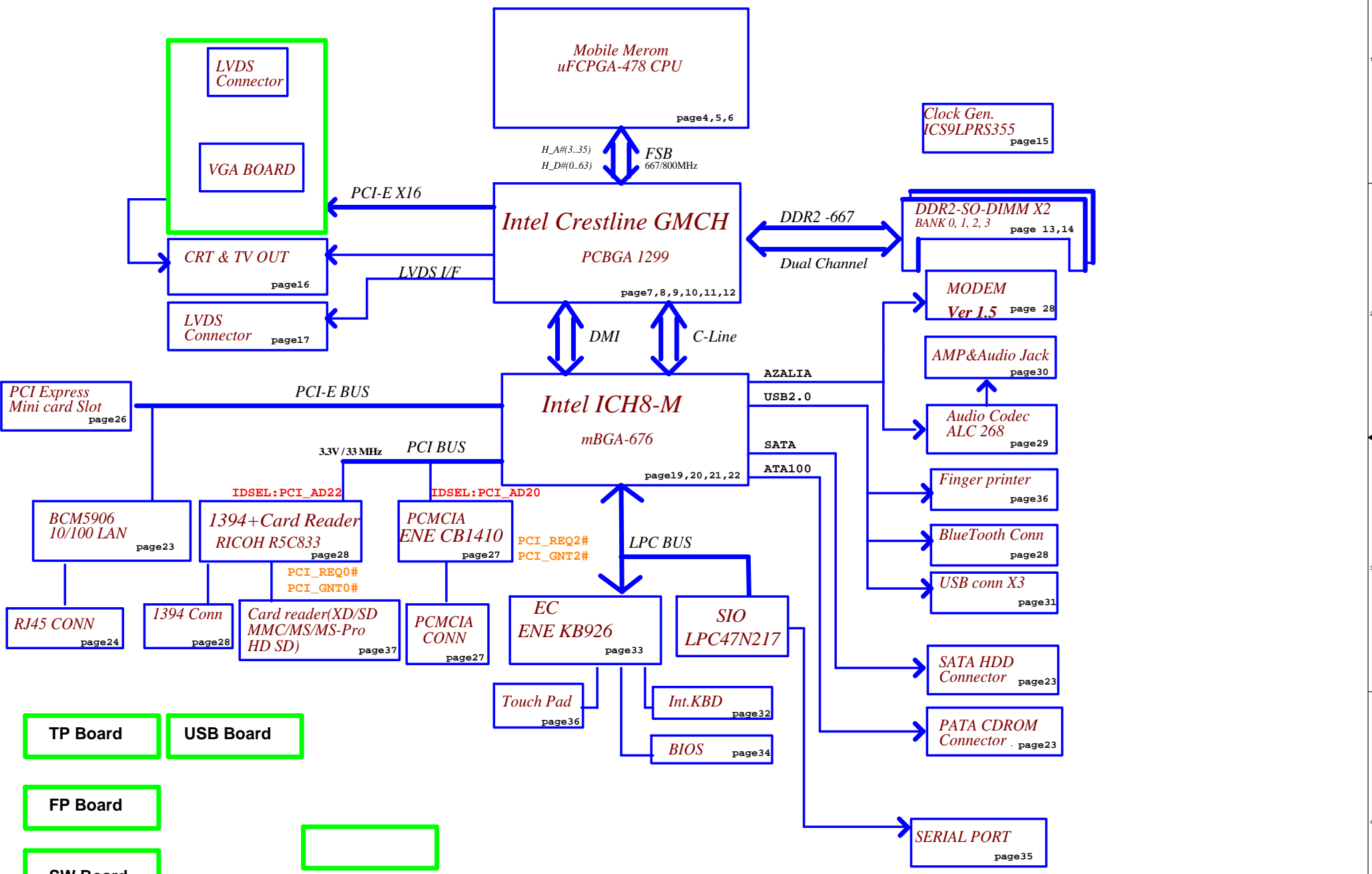
Tuesday, March 06, 2007

IGT10/11 Schematics Document

Mobile Merom uFCPGA with Intel Crestline_GM/PM+ICH8-M core logic

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				IGT10/11 LA-3591P	0.2
				Date:	Sheet 1 of 48

REV: 0.2



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				IGT10/11 LA-3591P
				Rev 0.2
Date: Tuesday, March 06, 2007				Sheet 2 of 48

Voltage Rails **O MEANS ON** **X MEANS OFF**

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +5V +VGA_CORE +CPU_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON **S3 : STR**
X MEANS OFF **S4 : STD**
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	MB ID(H)	MB ID(L)
0		
* 1	IEL10	
2	IDL11	IDL01
3	HDL10	HDL00
4		HDL20
5	IDL12	HDL30
6		
7		

	MB ID
H	15"
L	14"

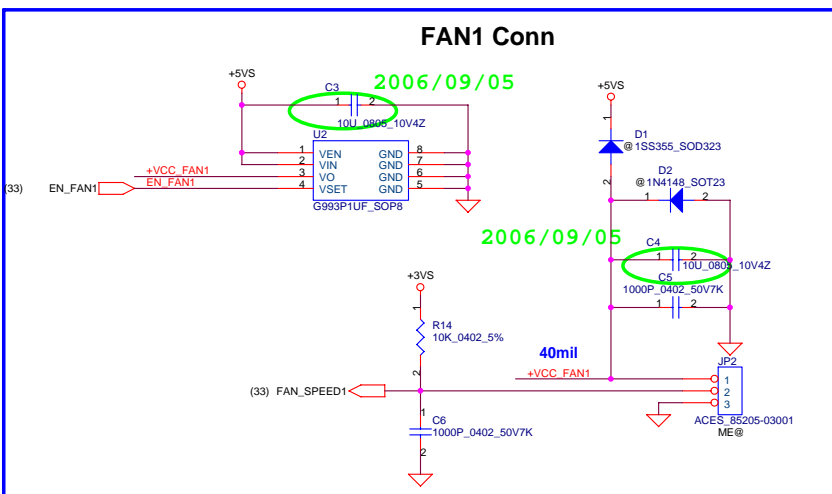
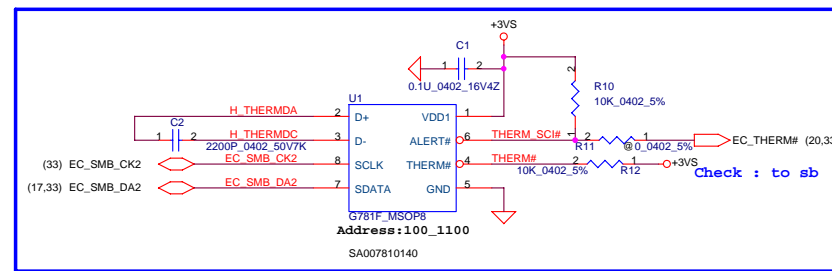
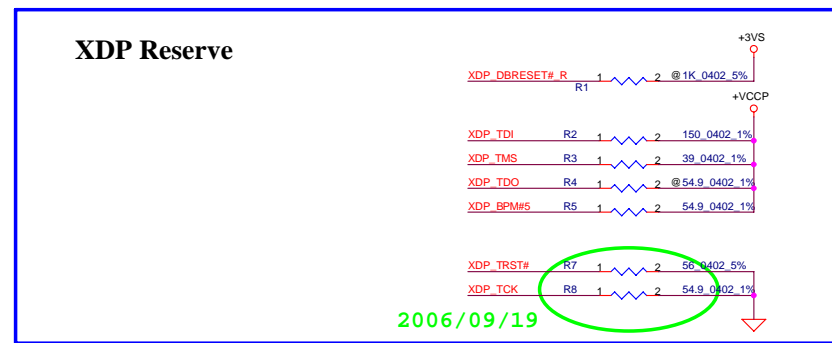
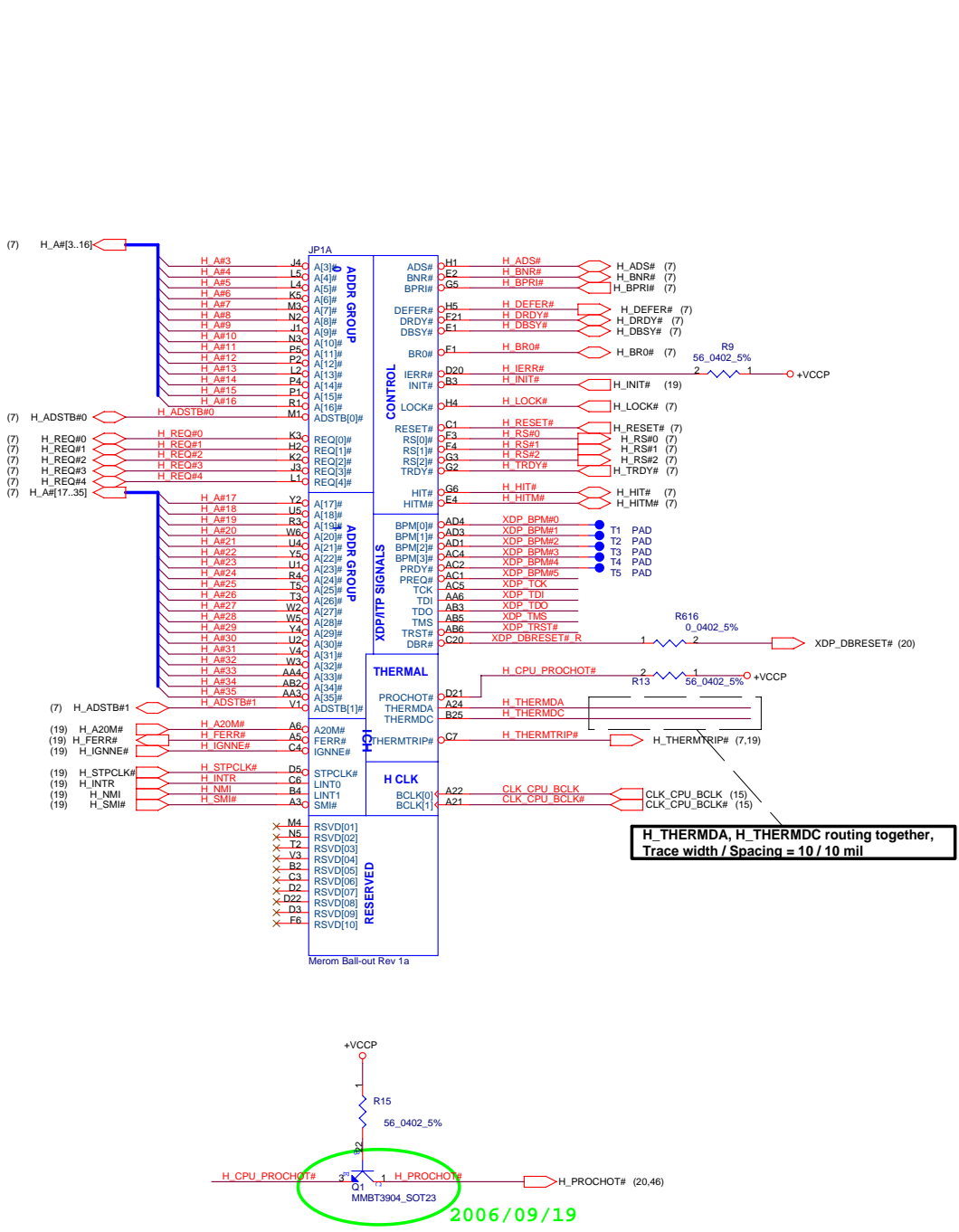
BOM Structure

MARK	FUNCTION
@	NC FOR ALL
GIGA@	BCM5787
100@	BCM5906
UMA@	Internal 965GM
VGA@	965PM + Ext VGA

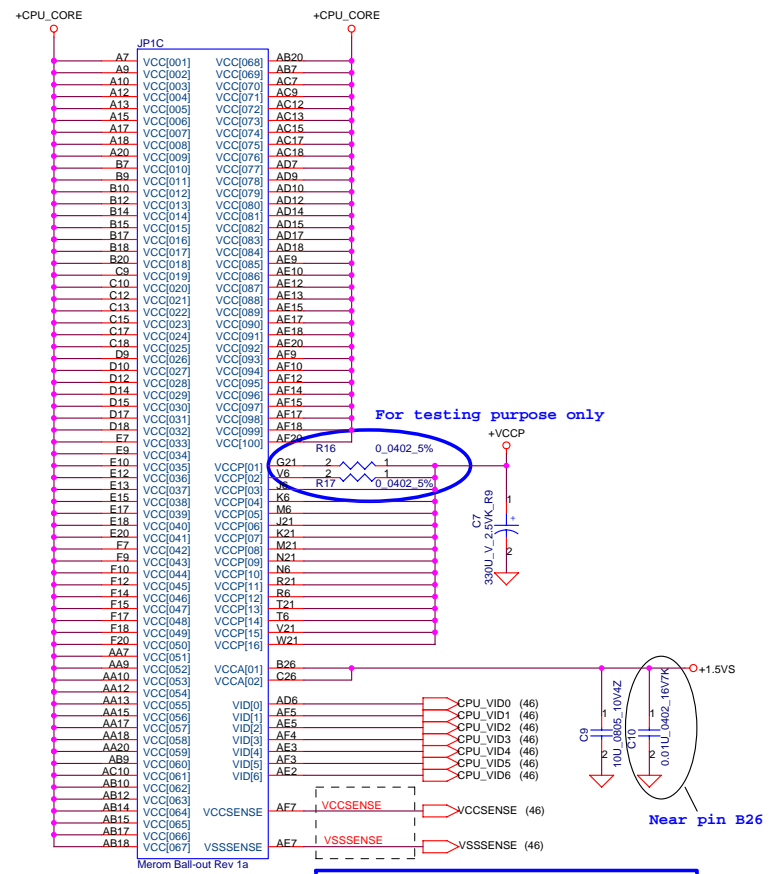
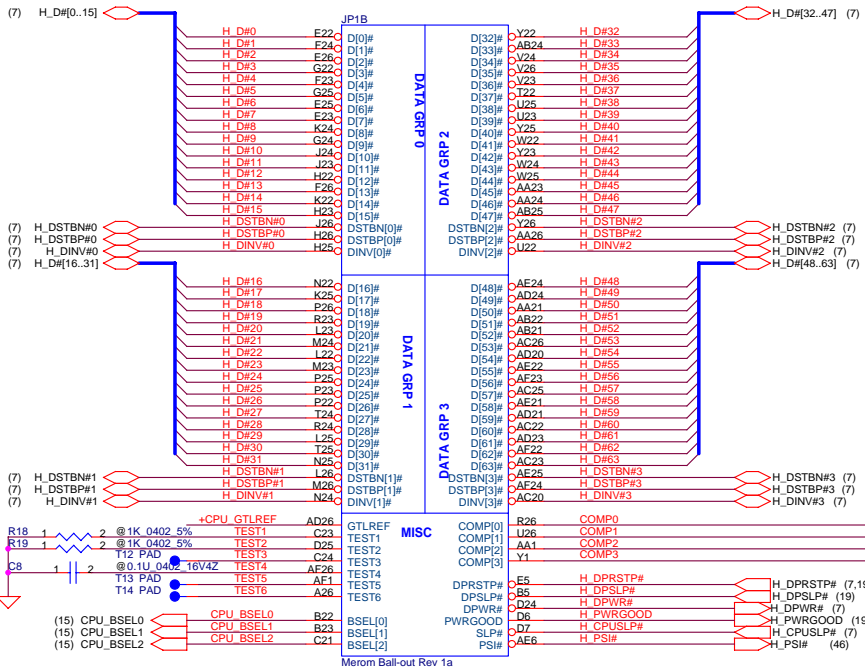
Address

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	RIGHT SIDE
7	BT (HDL20)
8	FINGER PRINTER
9	TV TUNER



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Document Number	IGT10/11 LA-3591P		Revision	Rev	0.2
Date:	Tuesday, March 06, 2007	Sheet	4	of	48

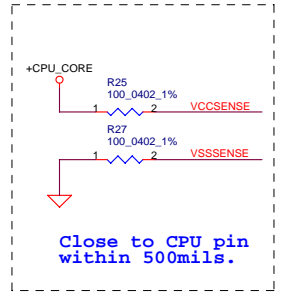
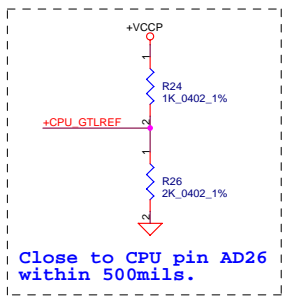


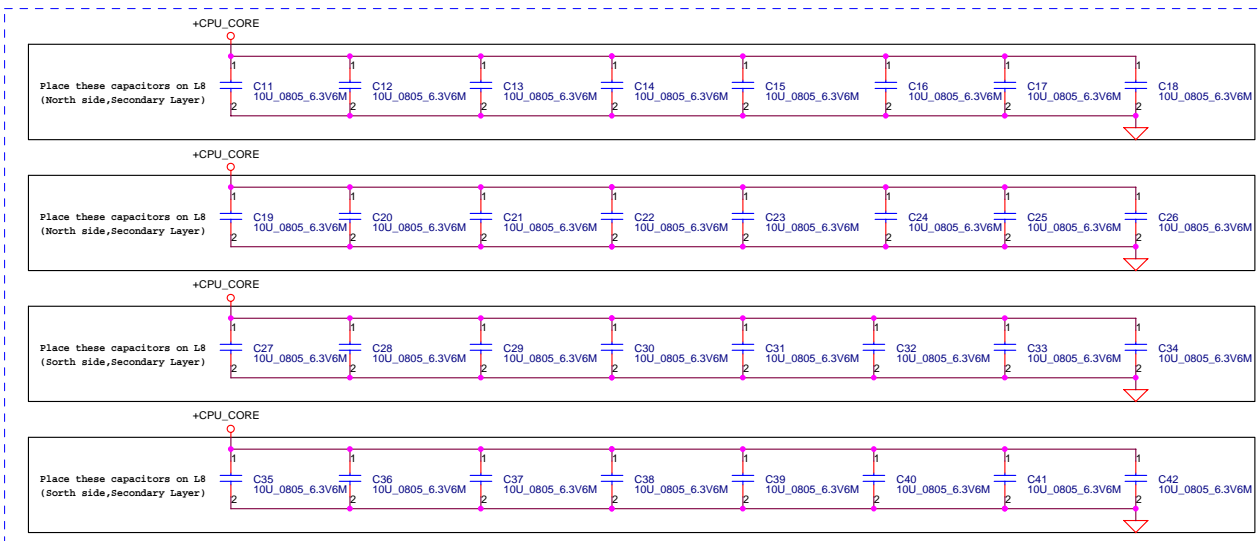
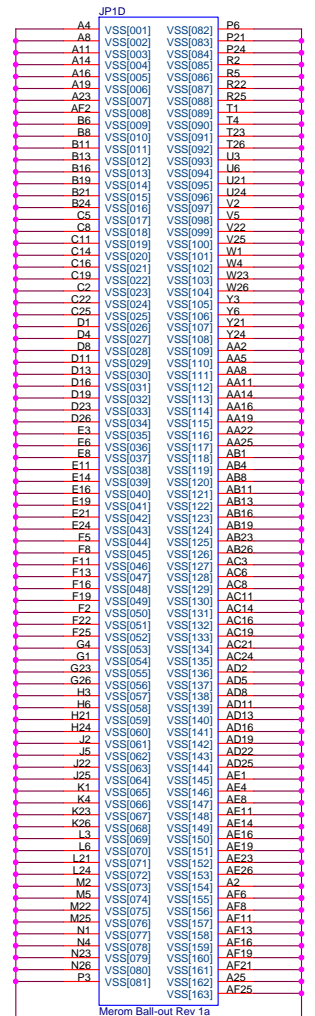
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

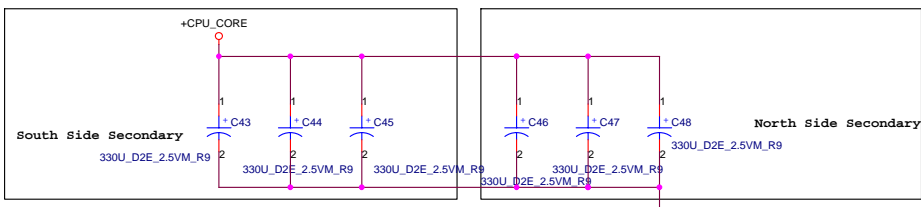
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

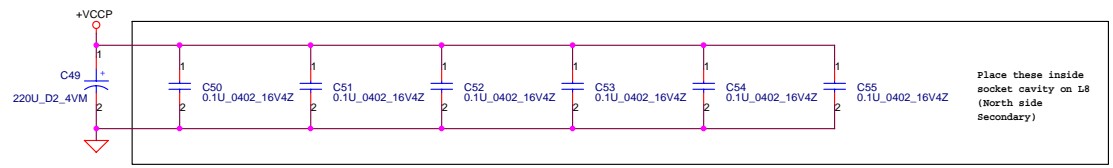




Mid Frequency Decoupling

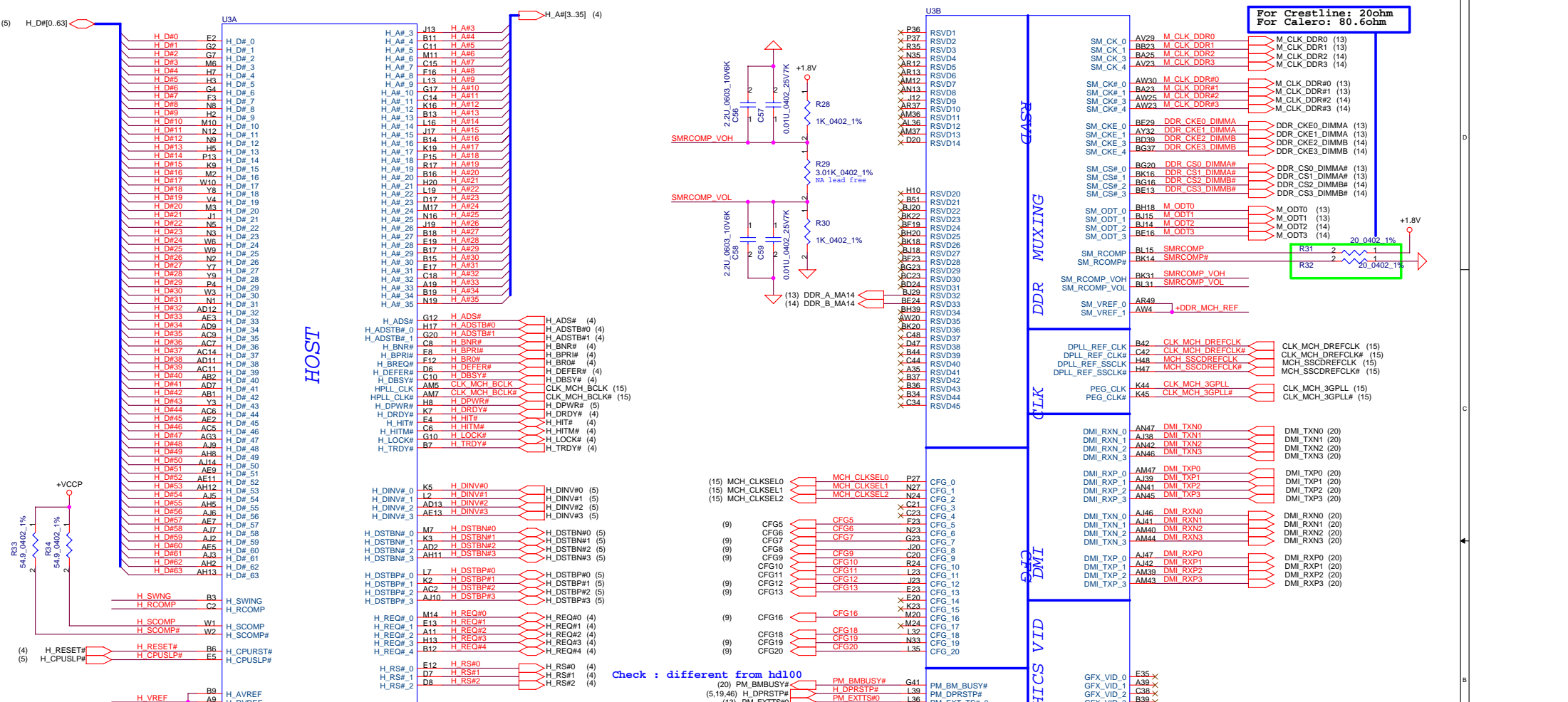


ESR <= 1.5m ohm
Capacitor > 1980uF

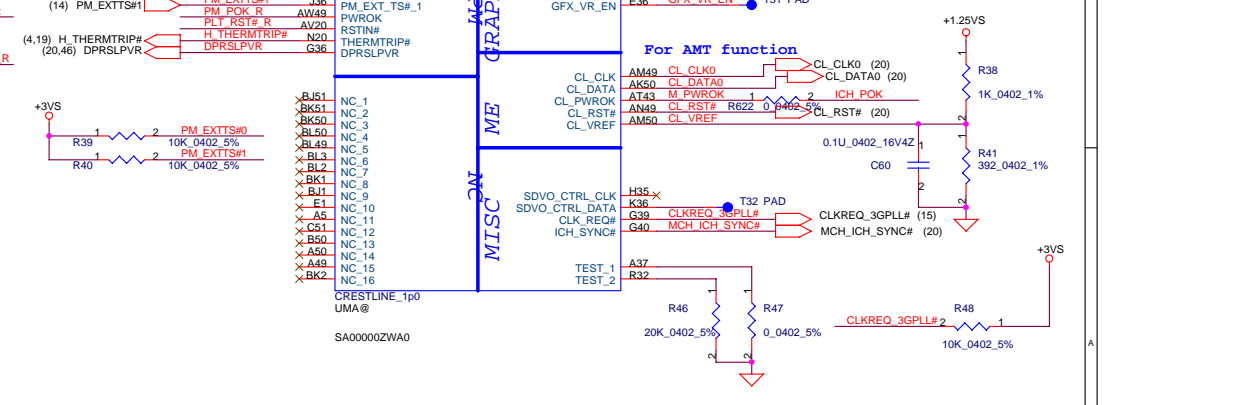
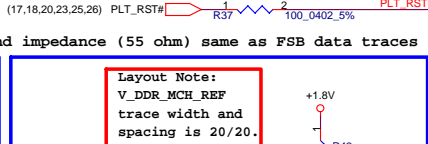
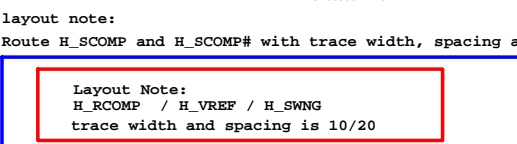


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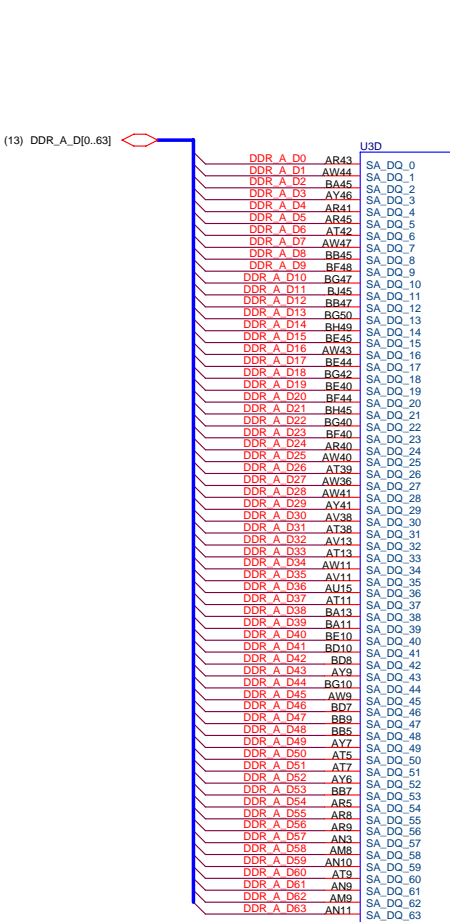
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Document Number		Merom(3/3)-GND&Bypass	
Revision	0.2	Date:	Tuesday, March 06, 2007
Sheet	6	of	48



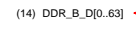
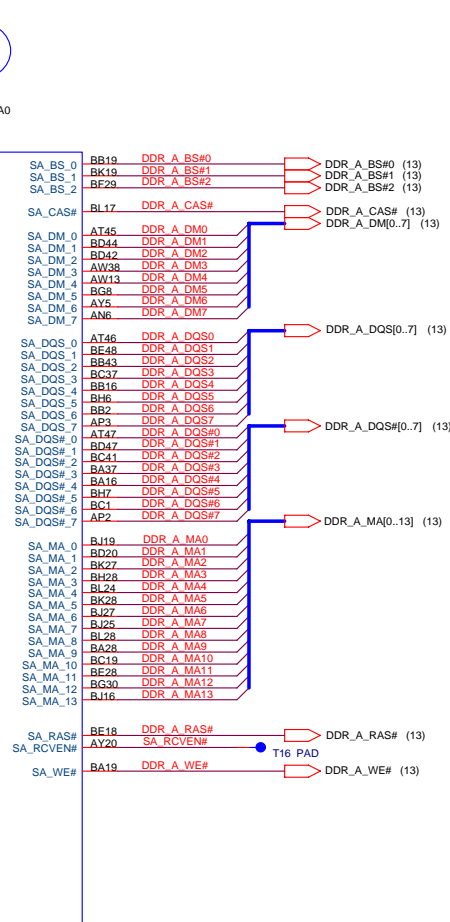
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSb data traces



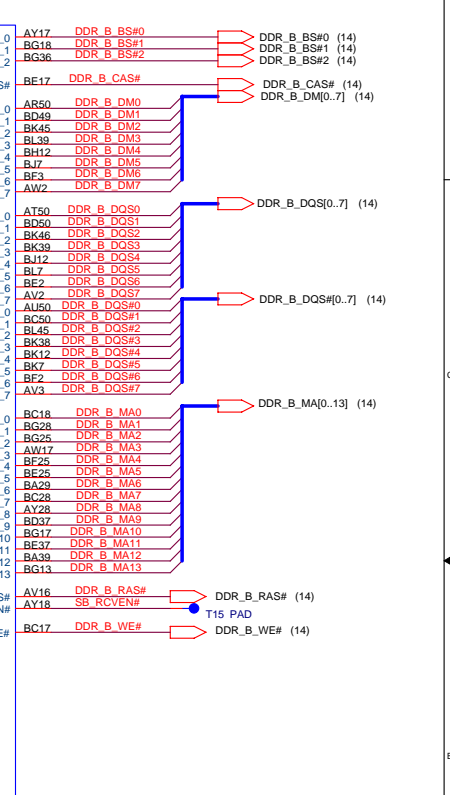
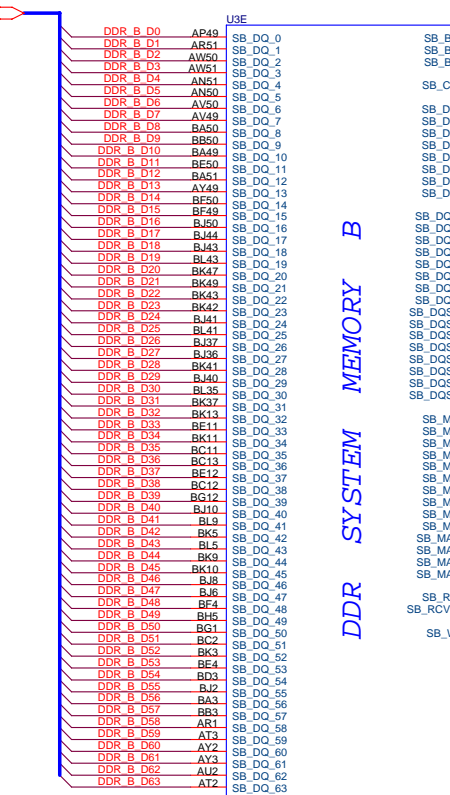
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Document Number	IGTI/011 LA-3591P		Rev	0.2	
Date	Tuesday, March 06, 2007	Sheet	7	of 48	



DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



CRESTLINE_1p0
UMA@
SA00000ZWA0

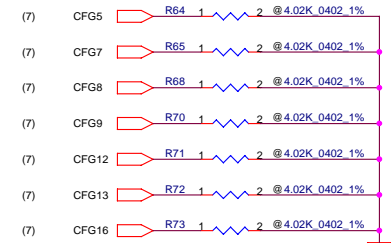
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UMA@
SA00000ZWA0

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			Date	Tuesday, March 06, 2007
			Sheet	8 of 48

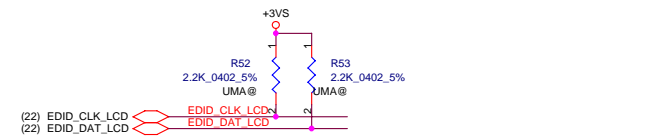
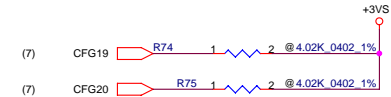
Compal Electronics, Inc.
CRESTLINE((2/6)-DDR2 A/B CH

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu. *

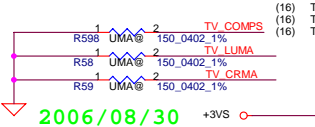


CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

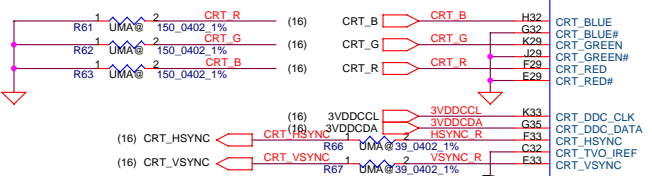


For Crestline: 2.4kohm
For Calero: 1.5kohm

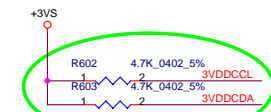
2006/09/13



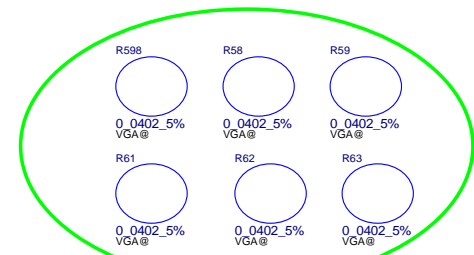
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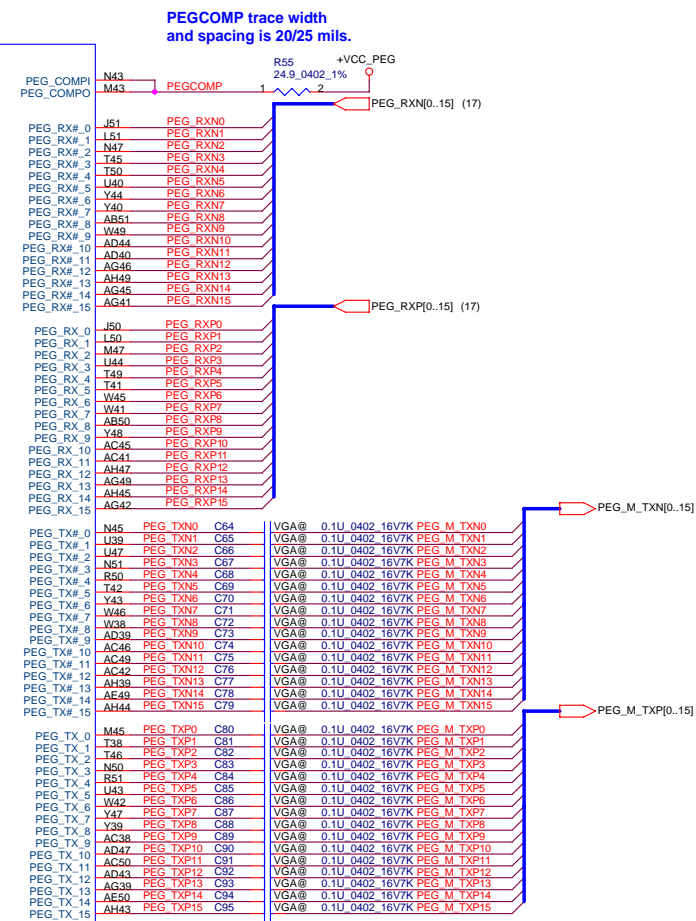
For Crestline: 1.3kohm
For Calero: 255ohm

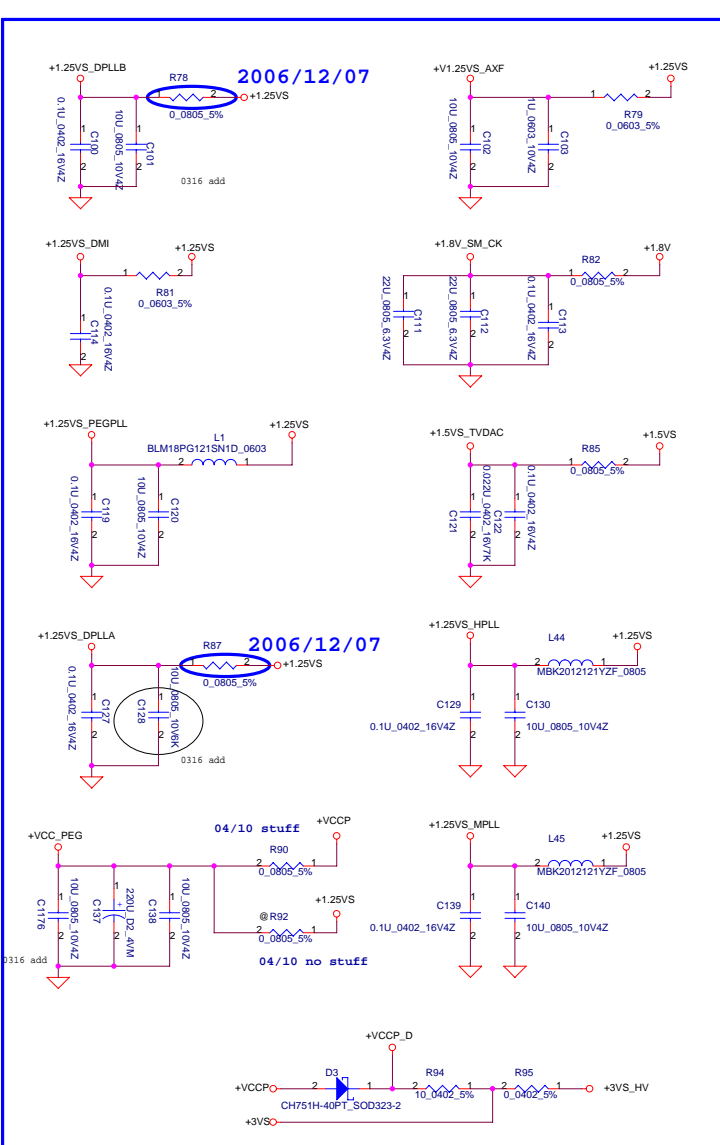
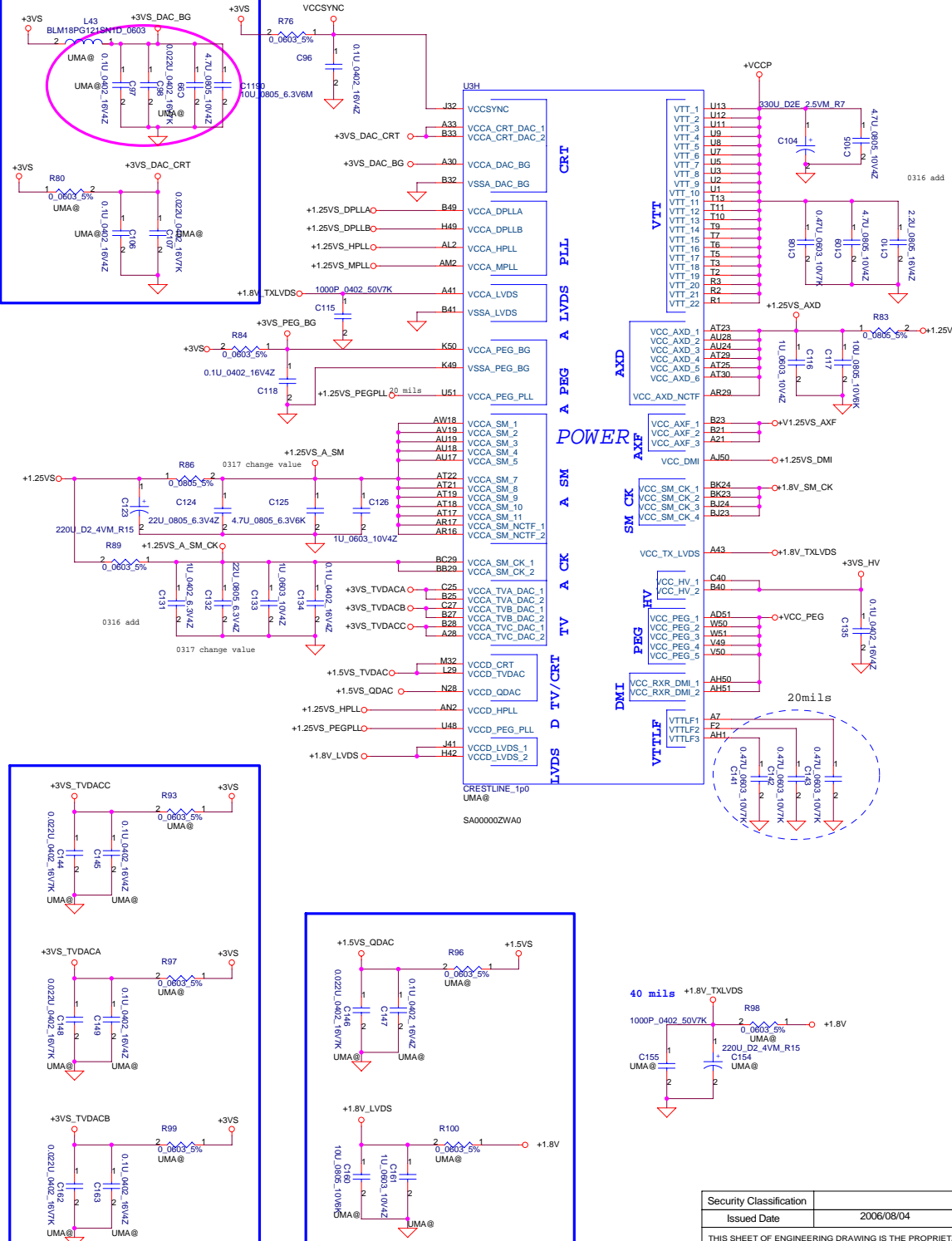


2006/09/06



2006/09/18

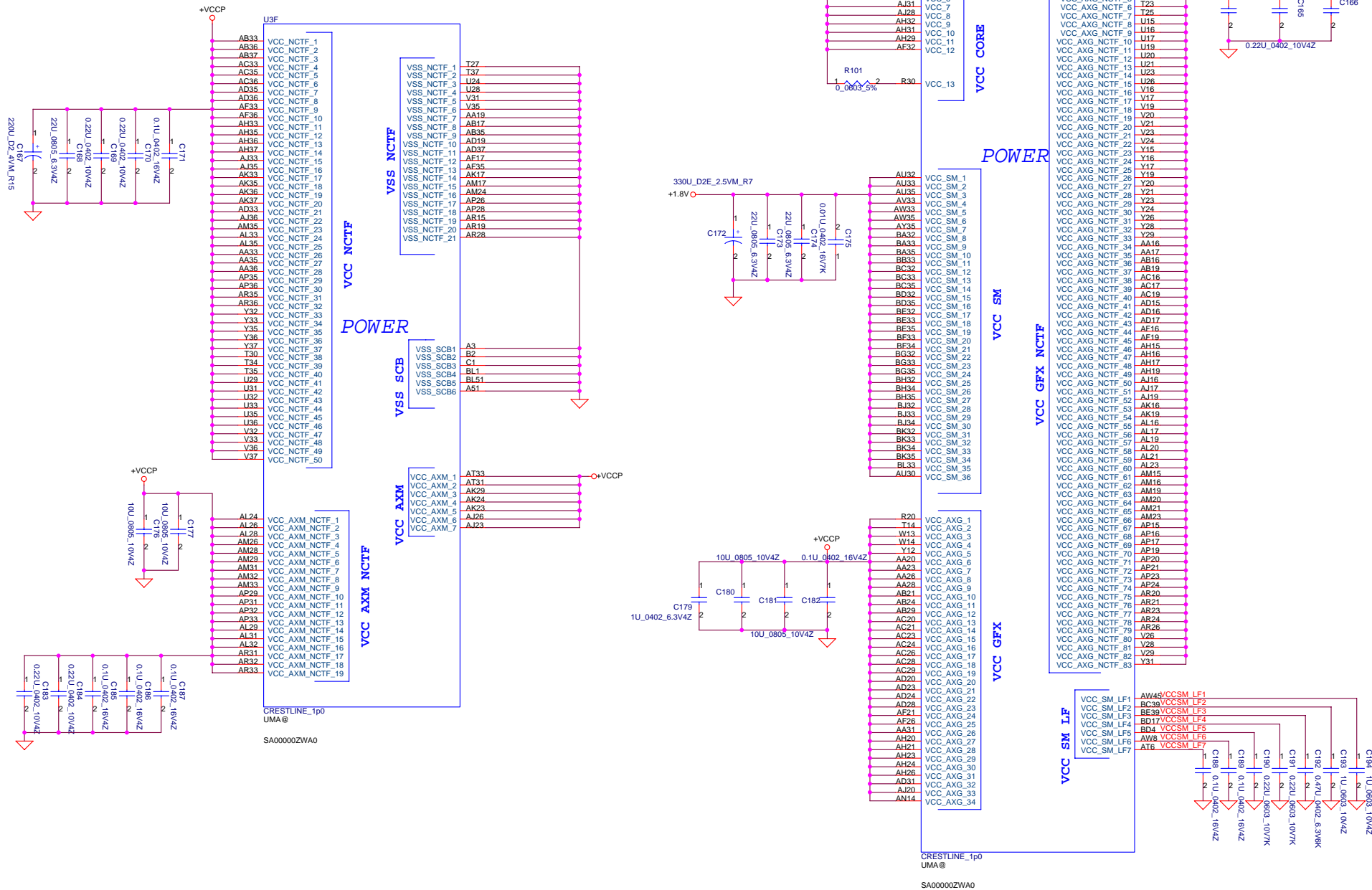




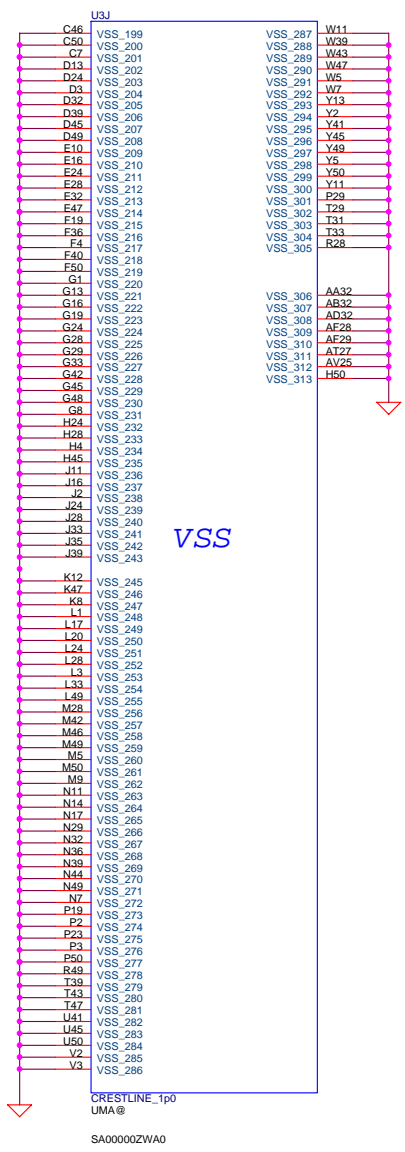
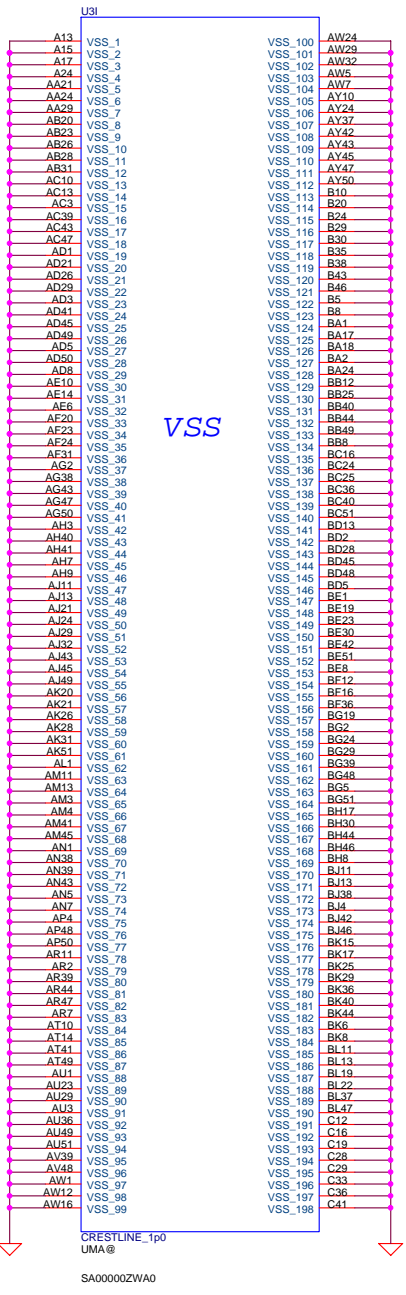
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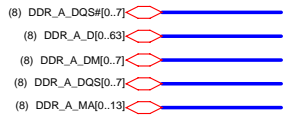
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CRESTLINE(4/6)-PWR	
Document Number	IGT1011 LA-3591P
Date:	Tuesday, March 06, 2007
Sheet	10 of 48



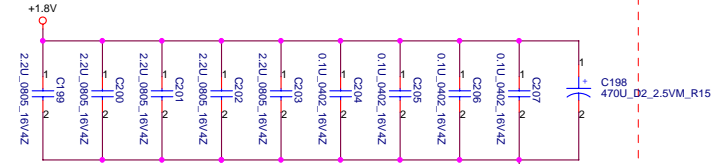
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			IGT10/11 LA-3591P	0.2	
			Date	Tuesday, March 06, 2007	Sheet 11 of 48



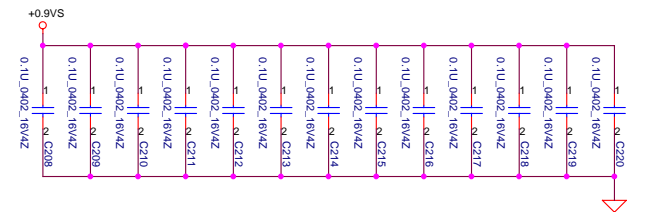
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Date: Tuesday, March 06, 2007				Rev 0.2
Sheet 12 of 48				



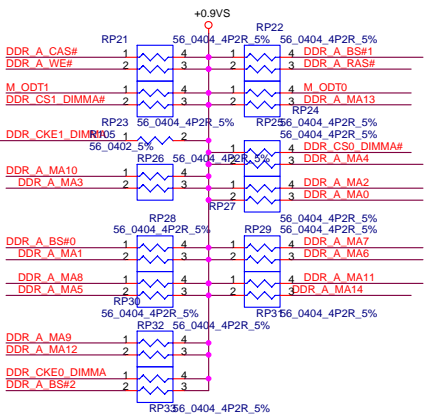
Layout Note:
Place near JP41



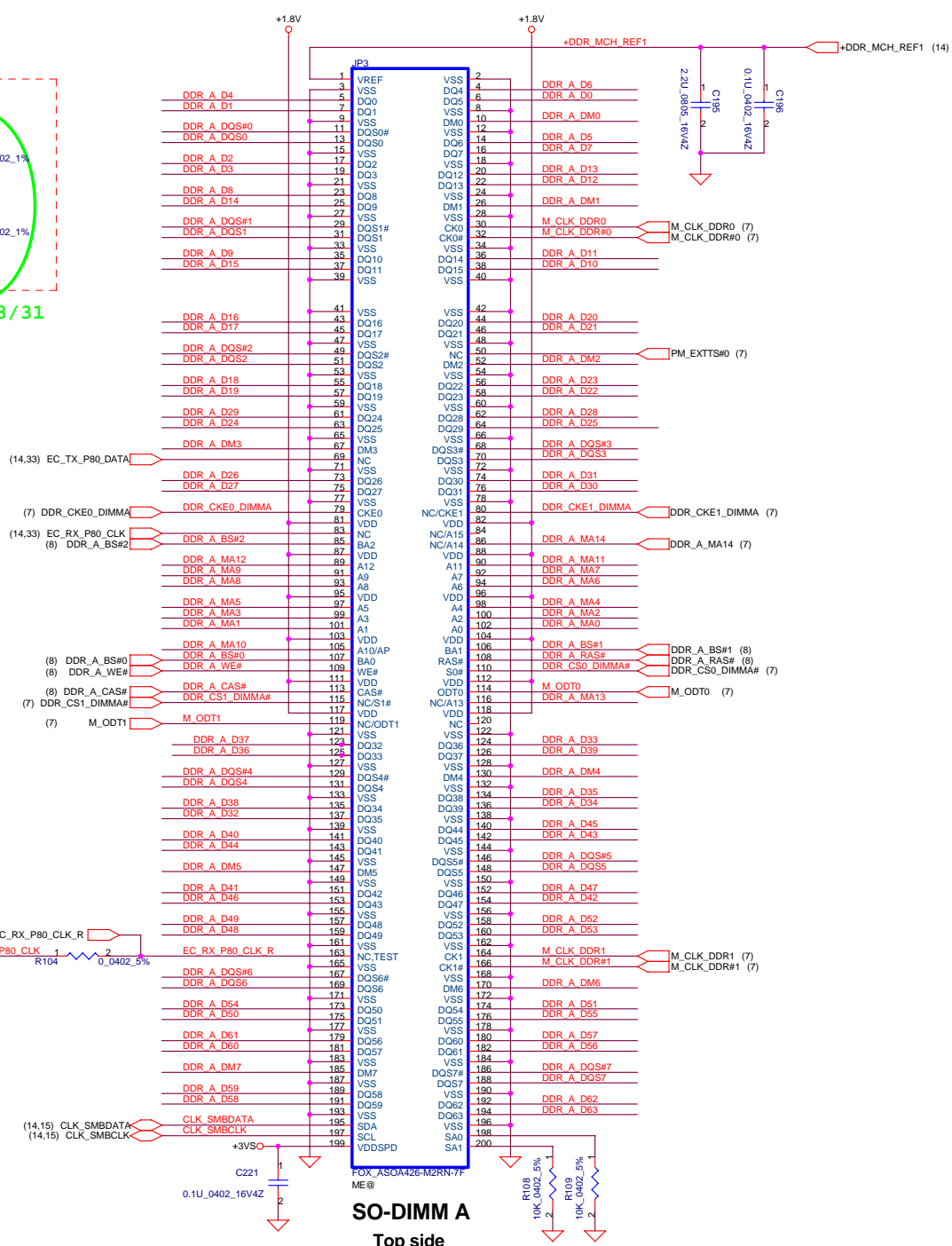
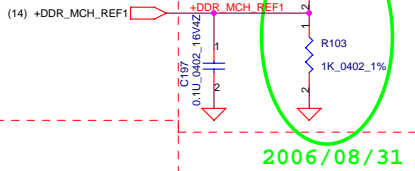
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



Layout Note:
+DDR_MCH_REF
trace width and spacing is 20/20.

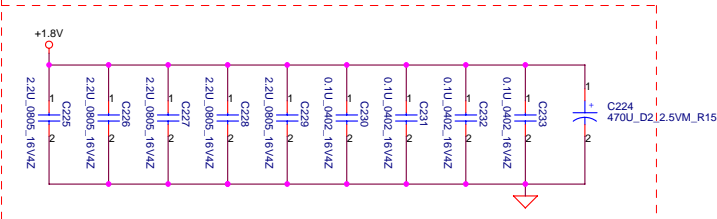


SO-DIMM A
Top side

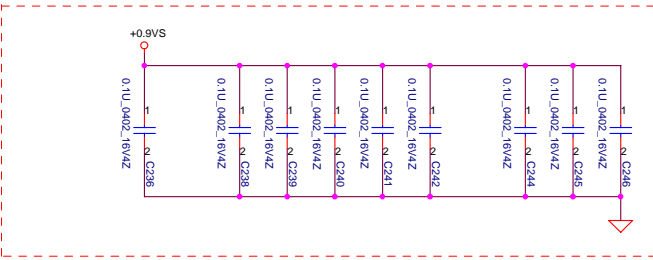
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Document Number	IGT10/11 LA-3591P		Rev	0.2	
Date	Tuesday, March 06, 2007	Sheet	13	of 48	

- (8) DDR_B_DQS#0[0..7]
- (8) DDR_B_D[0..63]
- (8) DDR_B_DM[0..7]
- (8) DDR_B_DQS#0[0..7]
- (8) DDR_B_MA[0..13]

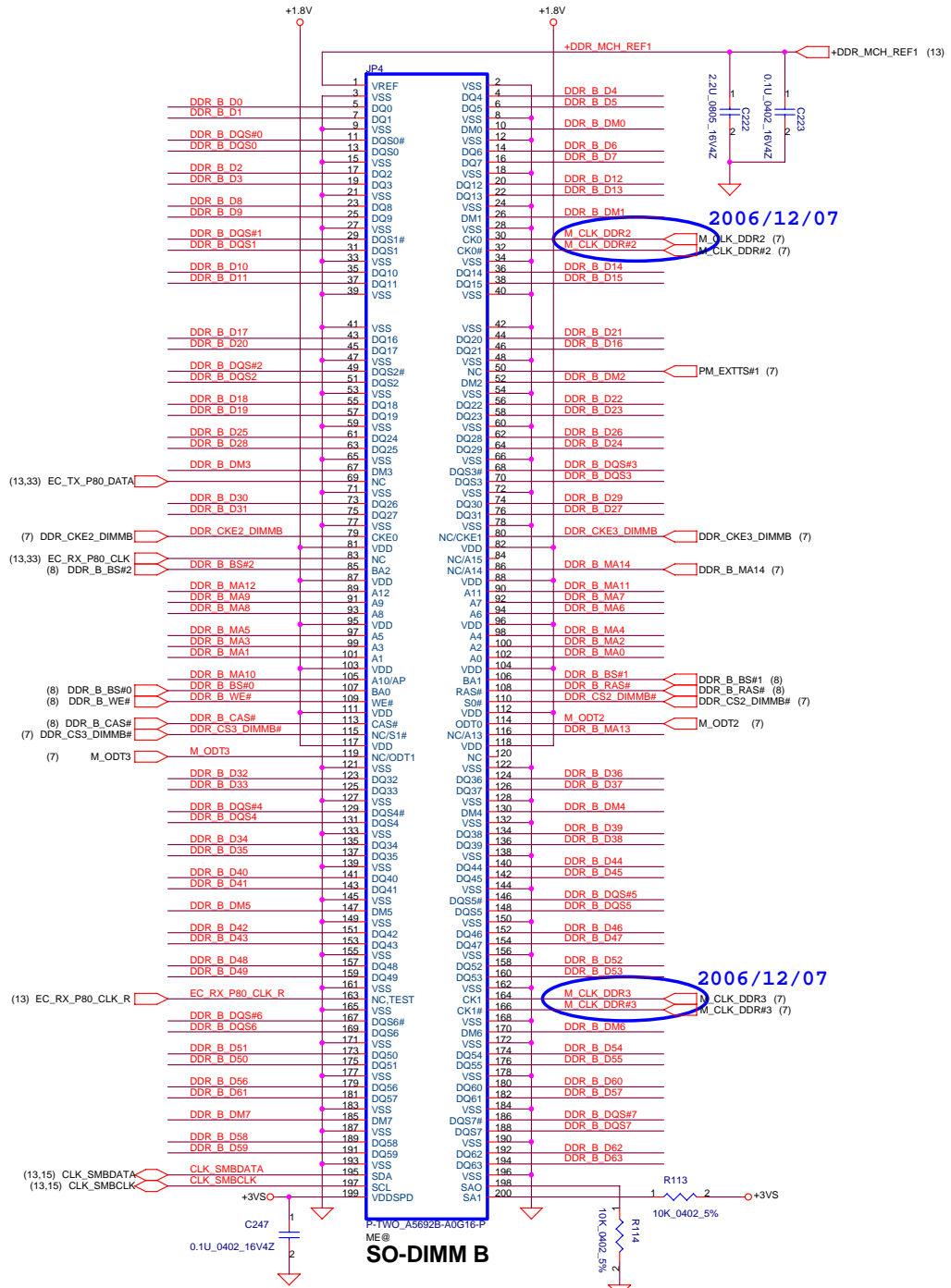
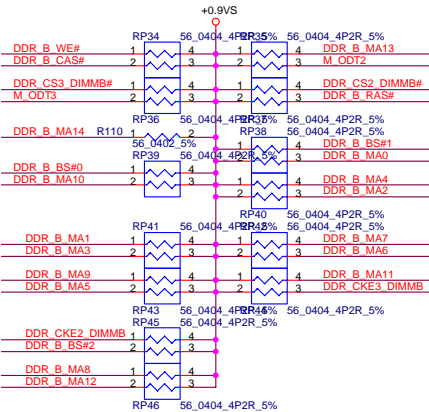
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VVS



Layout Note:
Place these resistor closely JP4, all trace length Max=1.5"



2006/12/07

2006/12/07

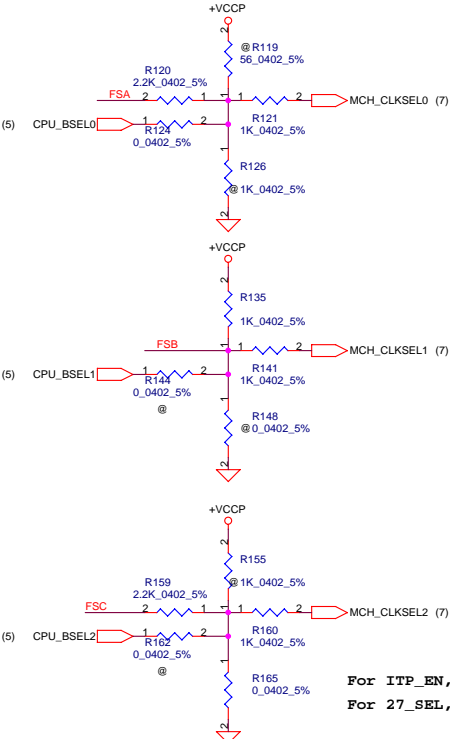
SO-DIMM B

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Date:	Tuesday, March 06, 2007	Sheet	14	of 48	

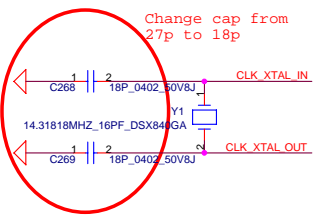
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Set:

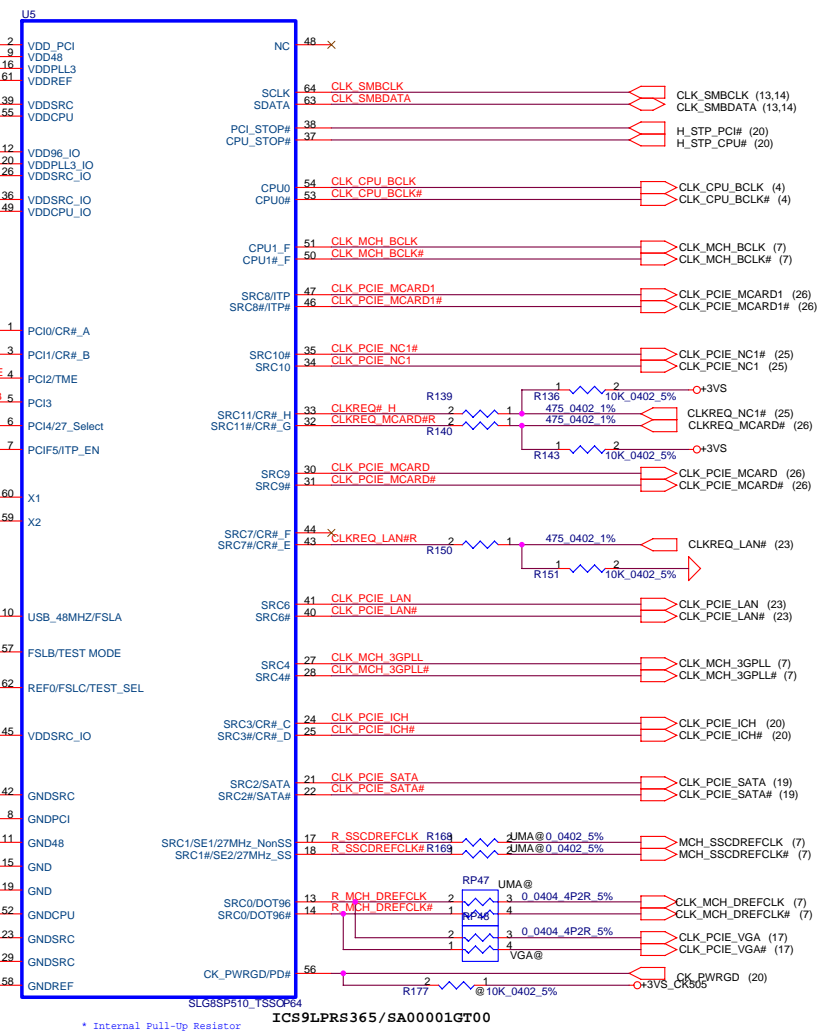
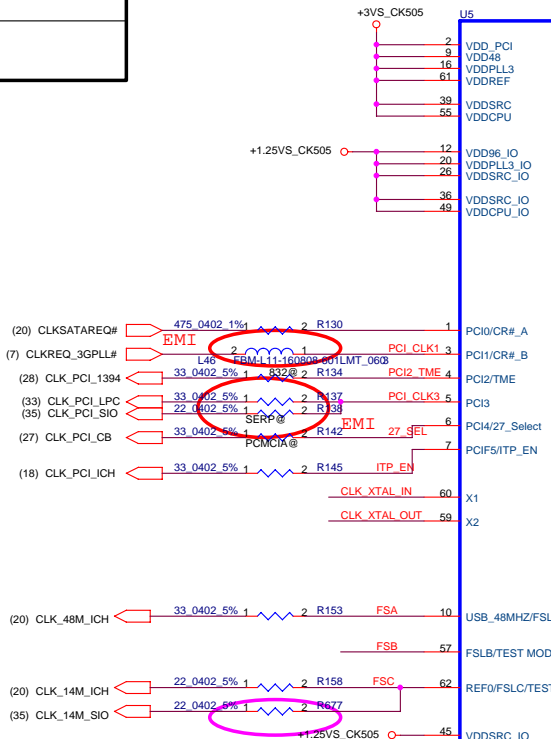
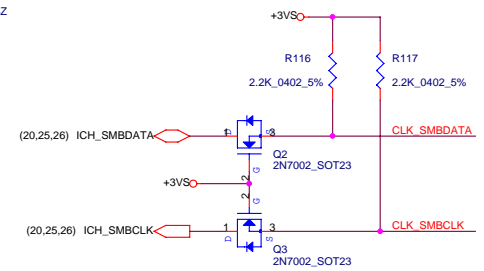
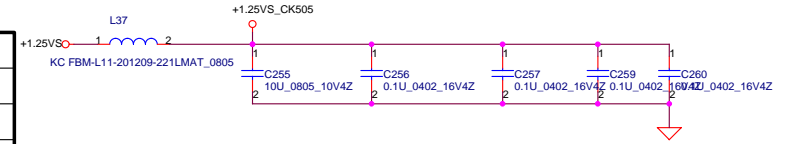
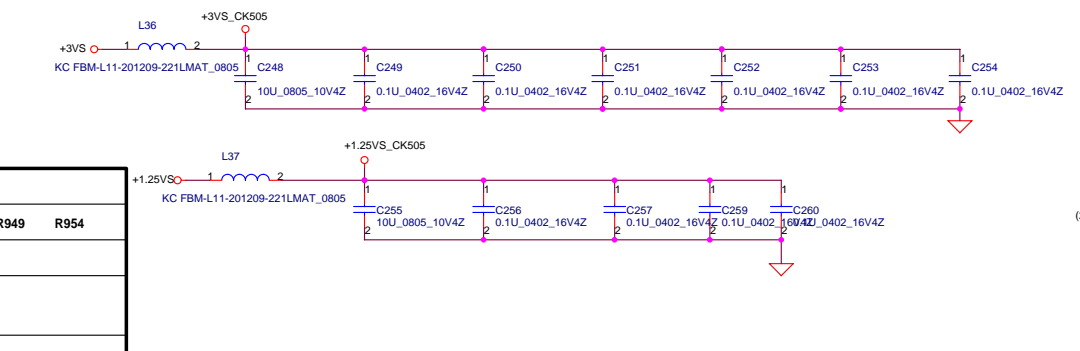
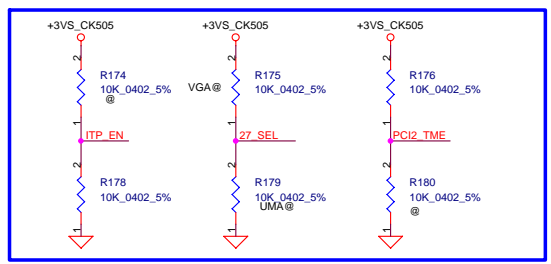
CPU Driven	Stuff	R919	R940	R956
*(Default)	No Stuff	R914	R921	R930
	Stuff	R919	R940	R956
667MHz	No Stuff	R949	R943	R921
	Stuff	R959	R930	R914
800MHz	No Stuff	R919	R940	R956
	Stuff	R949	R943	R914



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
 For 27_SEL, 0 = Enable DOT96 & SRC1,
 1 = Enable SRC0 & 27MHz
 For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
 1 = Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil



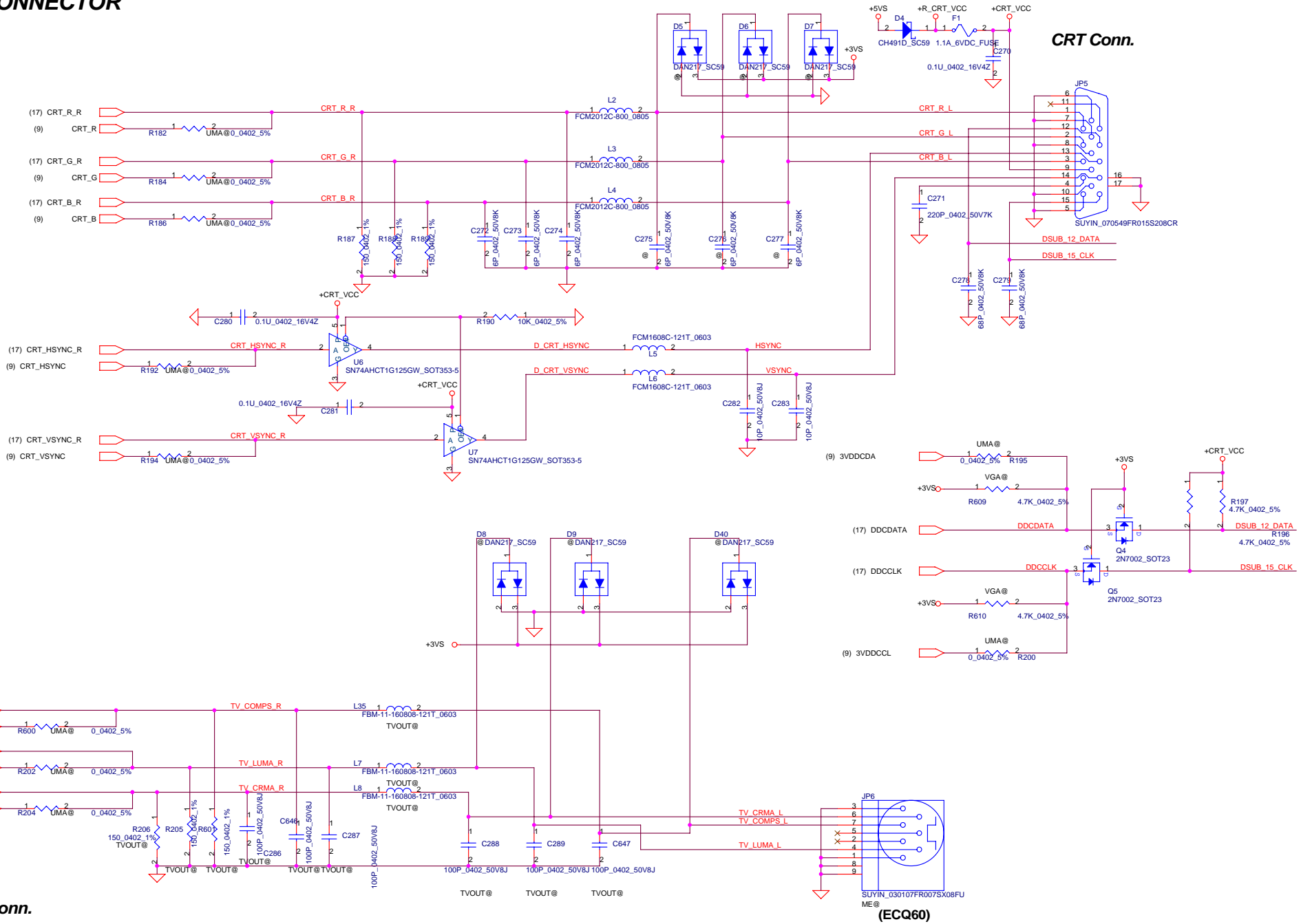
Place close to U41

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Date:	Tuesday, March 06, 2007	Sheet	15	of 48	

CRT CONNECTOR

Near to JP13

CRT Conn.



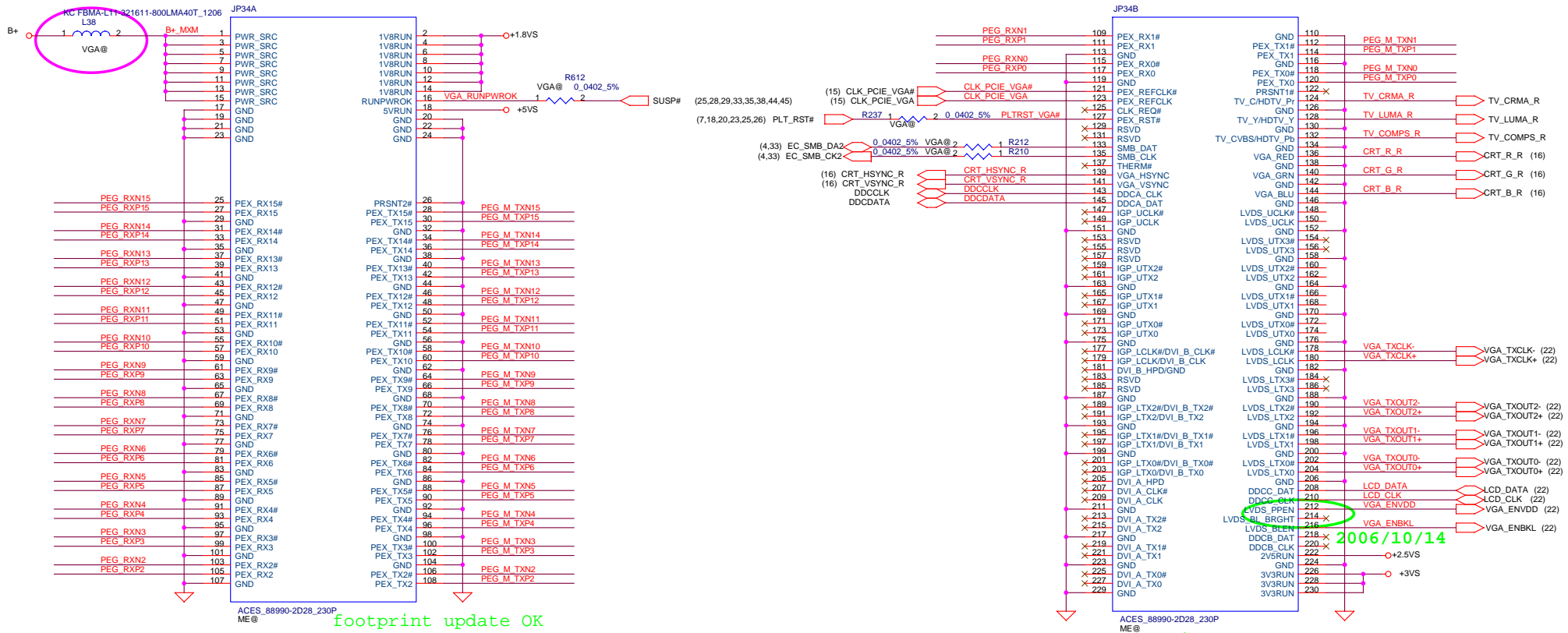
TV-OUT Conn.

- 1. Y ground
- 2. C ground
- 3. Y (luminance+sync)
- 4. C (chrominance)

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Date: Tuesday, March 06, 2007			Rev 0.2
Sheet			16 of 48

PEG_M_TXP[0..15] (9)
 PEG_M_TXN[0..15] (9)
 PEG_RXP[0..15] (9)
 PEG_RXN[0..15] (9)

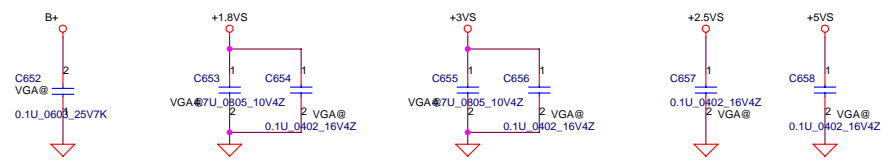
MXM VGA BOARD Conn.



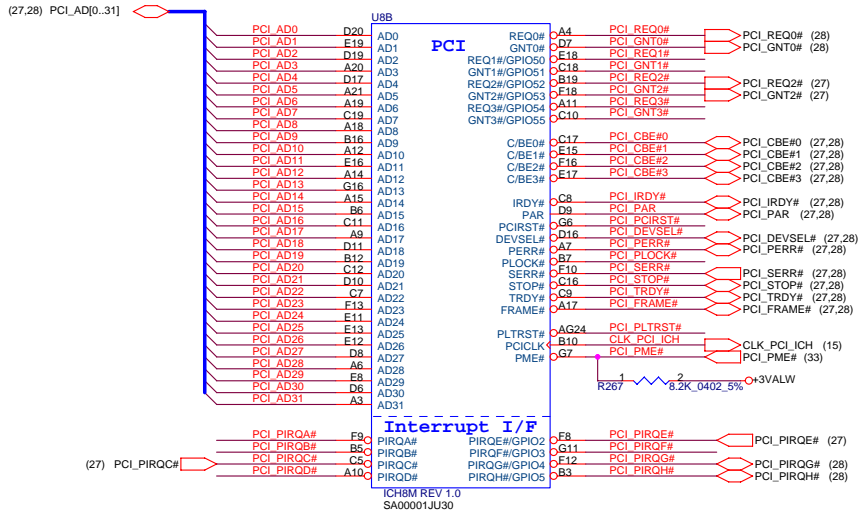
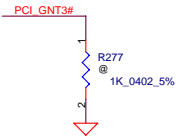
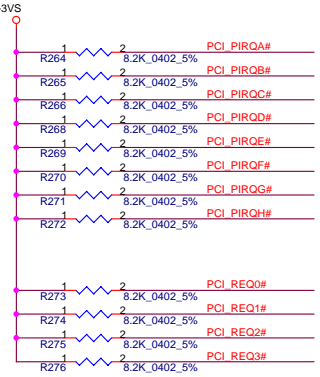
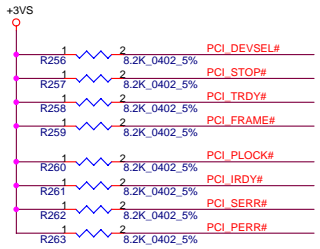
footprint update OK

footprint update OK

2006/09/13

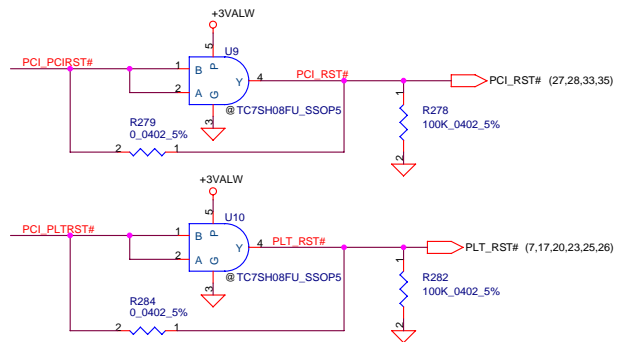
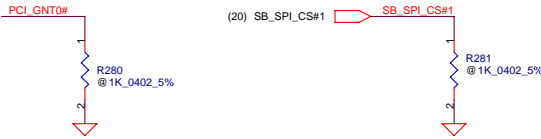
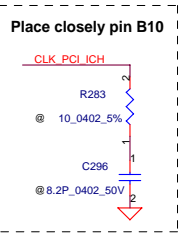


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				Rev 0.2
				Sheet 17 of 48



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



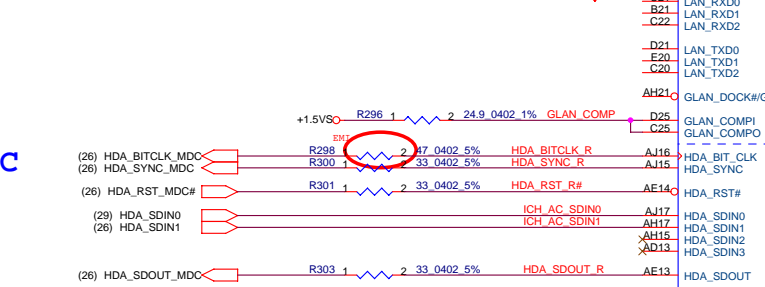
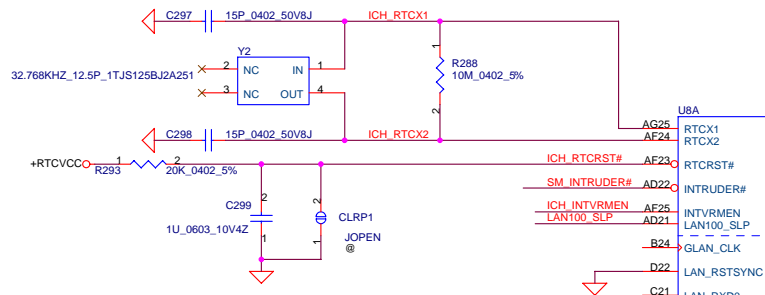
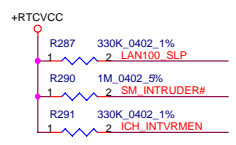
Compal Electronics, Inc.

ICH8(1/4)-PCI/INT

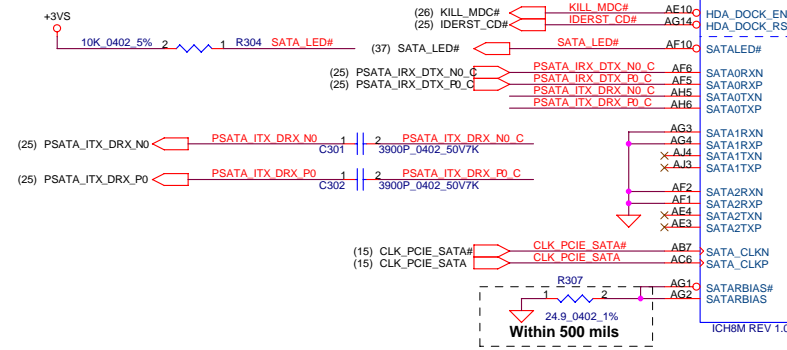
IGT10/11 LA-3591P

ICH8M Internal VR Enable Strap
 (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

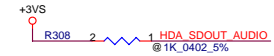
LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_INTVRMEN	



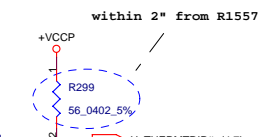
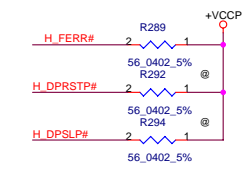
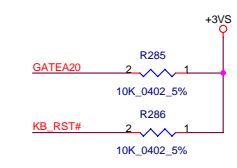
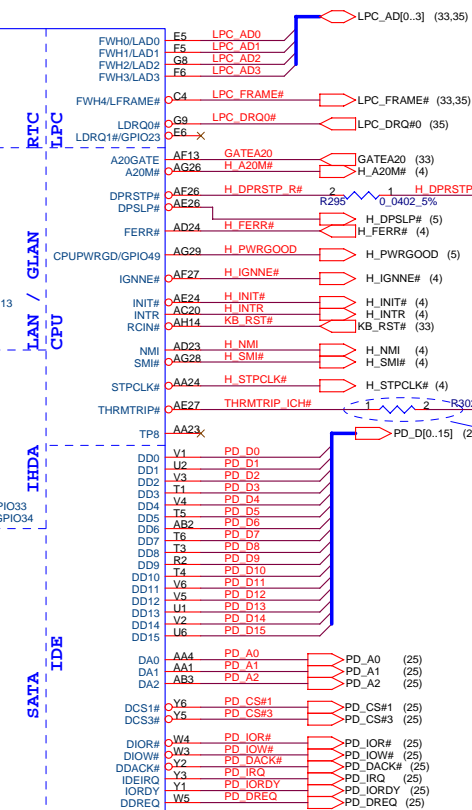
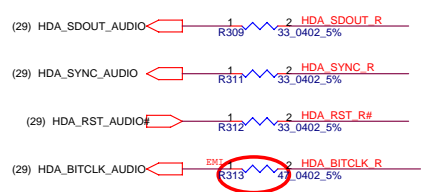
TO MDC



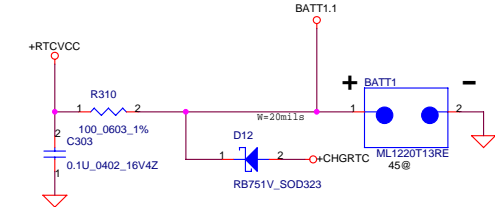
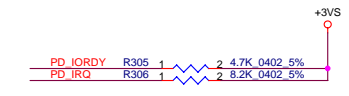
XOR CHAIN ENTRANCE STRAP:RSVD



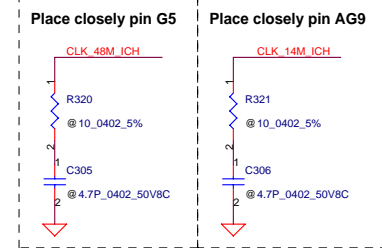
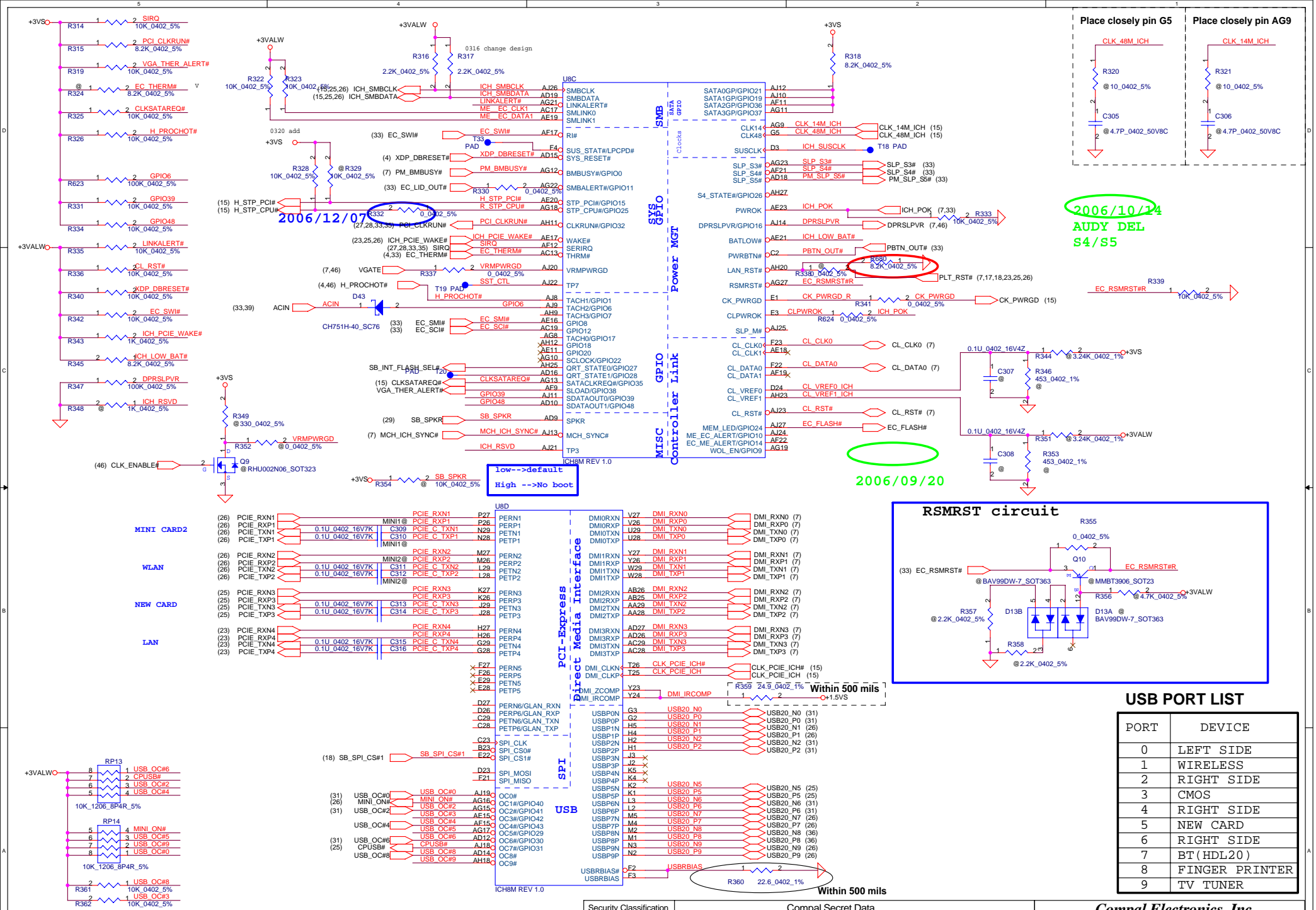
TO CODEC Close to ICH



placed within 2" from ICH8M

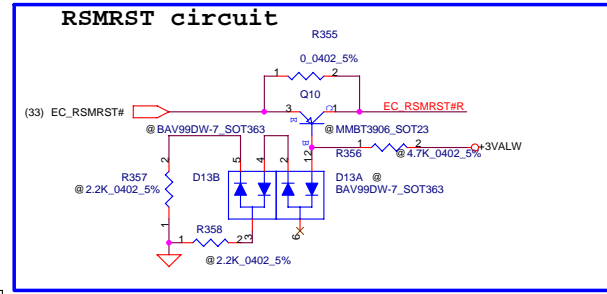


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			Date: Tuesday, March 06, 2007
			Sheet 19 of 48



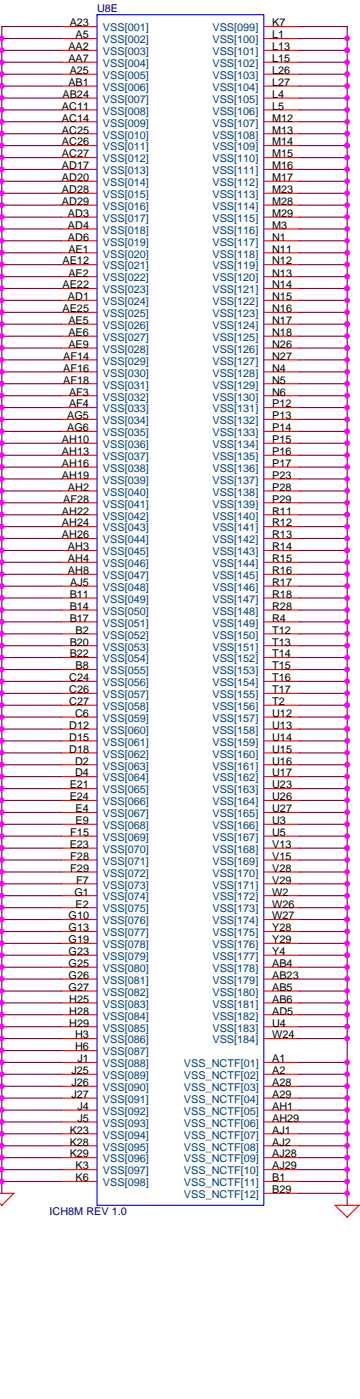
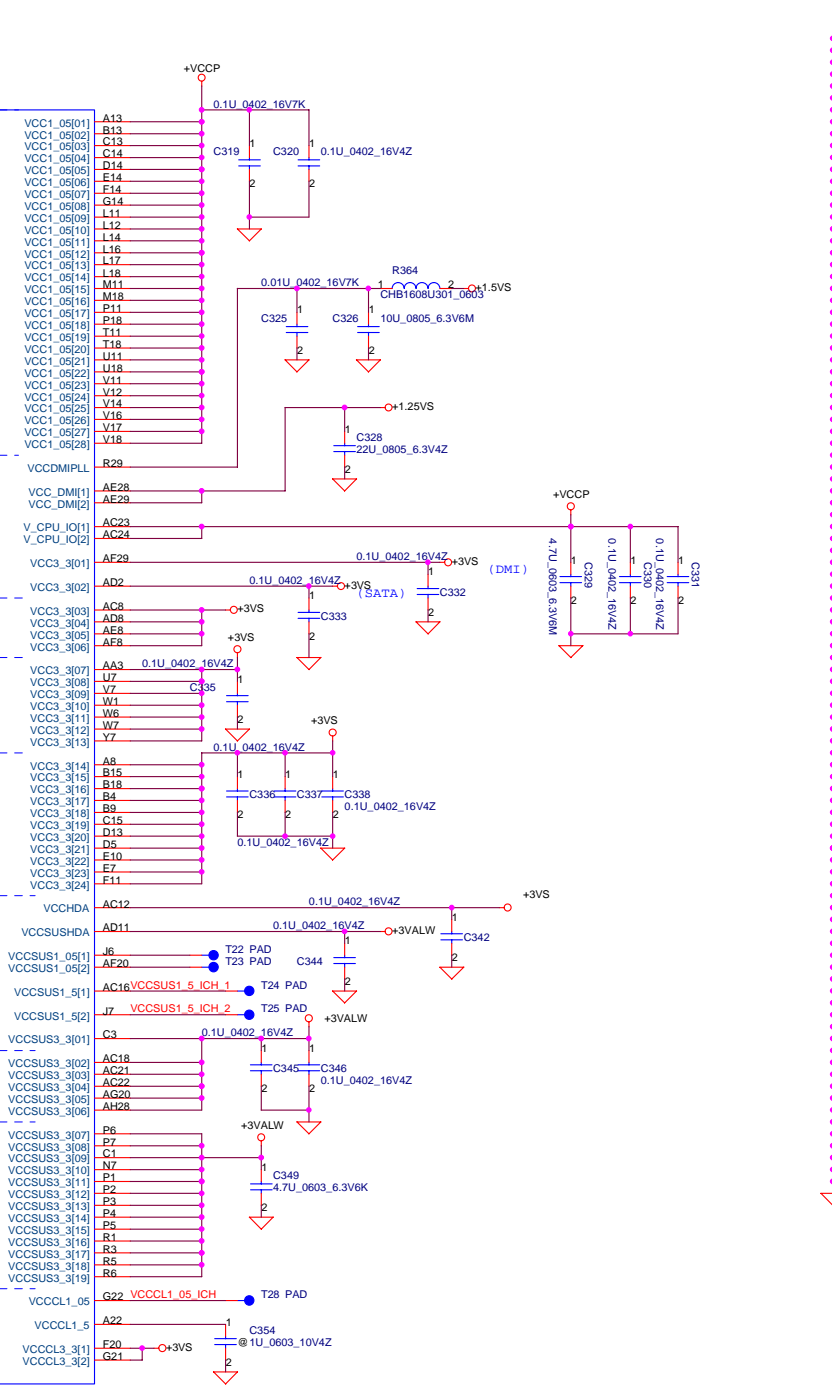
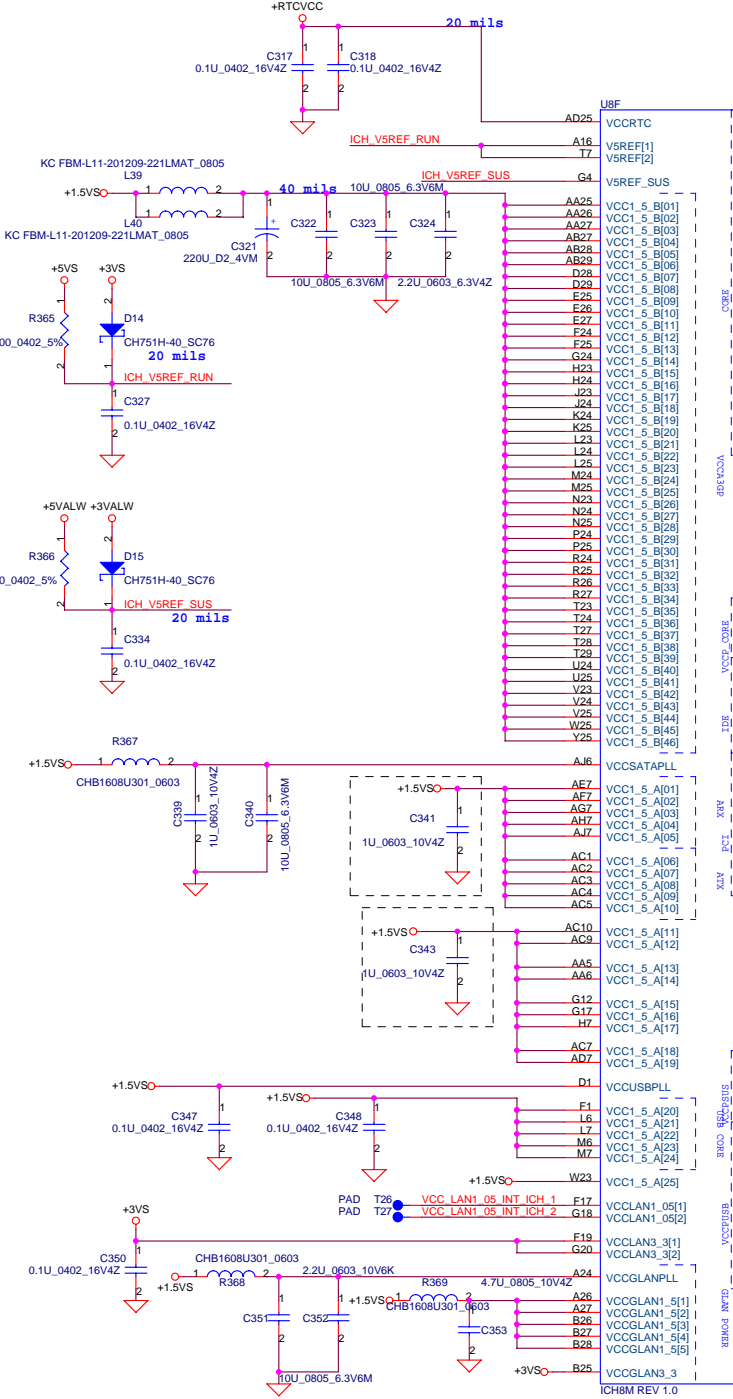
2006/10/14
AUDY DEL
S4/S5

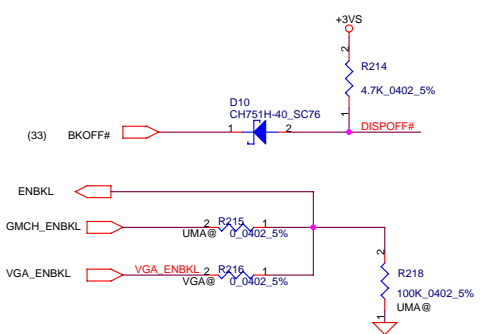
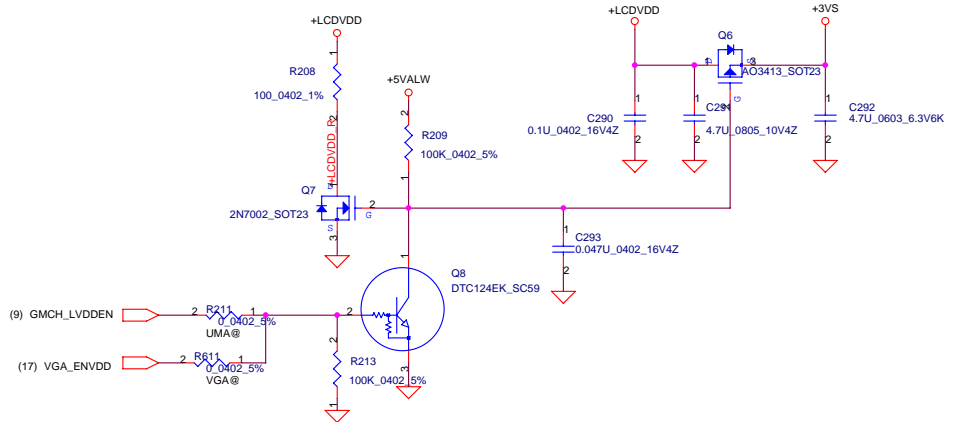
2006/09/20



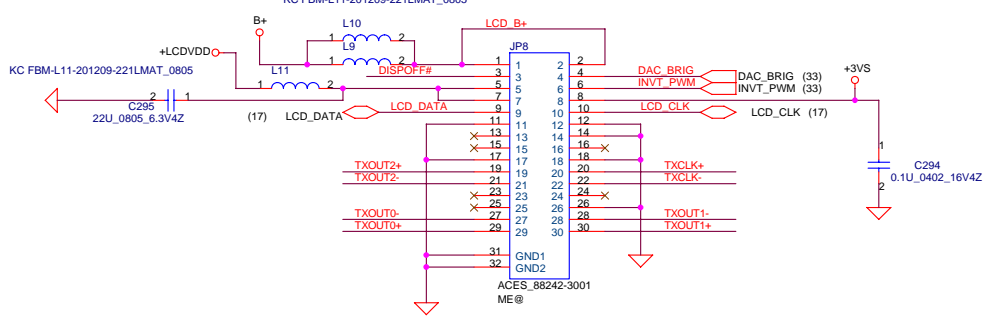
USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	RIGHT SIDE
7	BT (HDL20)
8	FINGER PRINTER
9	TV TUNER

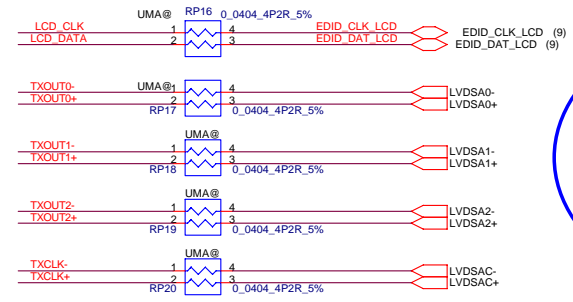




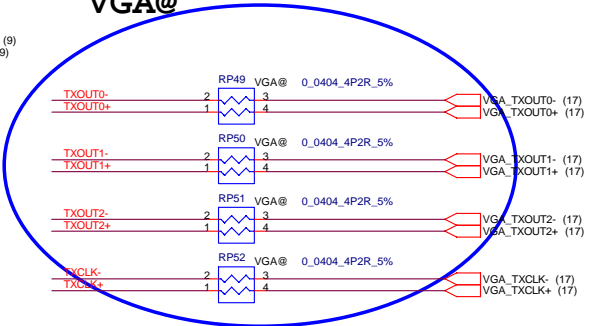
LCD/PANEL BD. Conn.



UMA@



VGA@



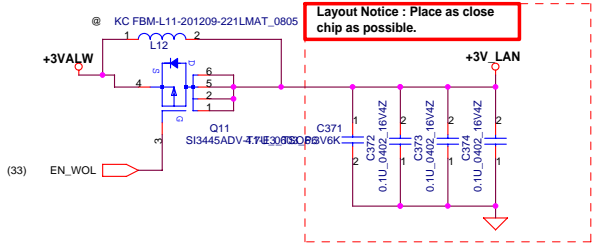
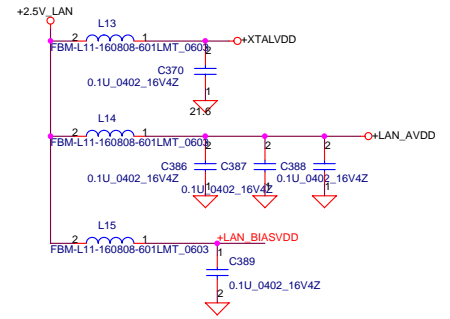
2006/12/06

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			IGT10/11 LA-3591P	0.2
			Date: Tuesday, March 06, 2007	Sheet 22 of 48

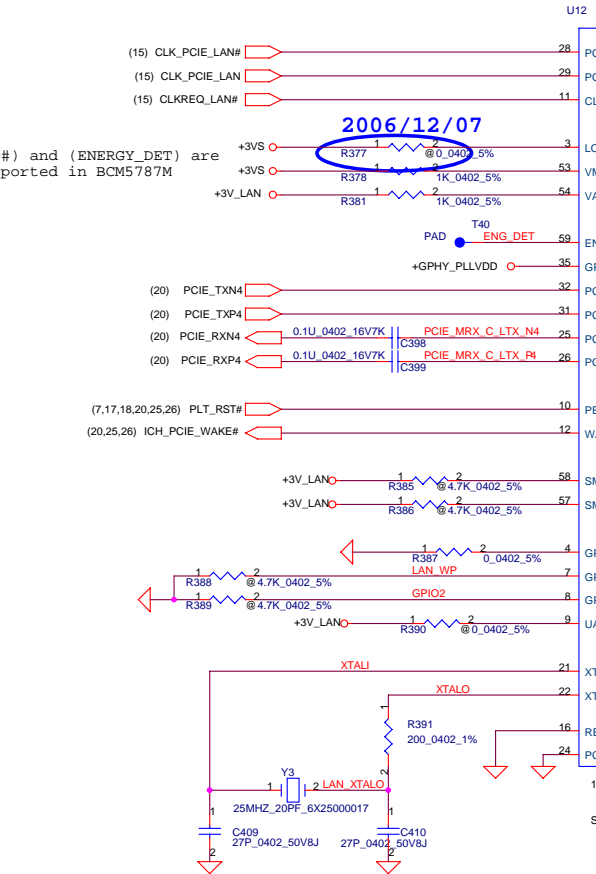
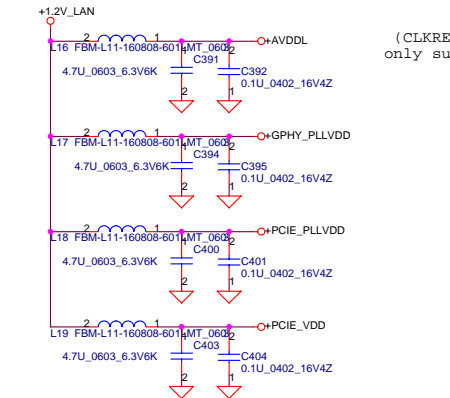
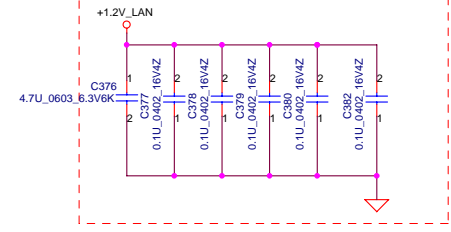
Compal Electronics, Inc.

LVDS CONN

Layout Notice : Filter place as close chip as possible.



Layout Notice : 1.2V filter. Place as close chip as possible.



2006/12/07

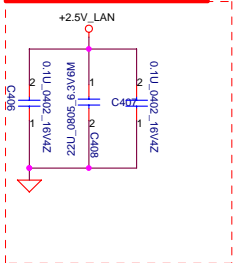
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

2006/12/26

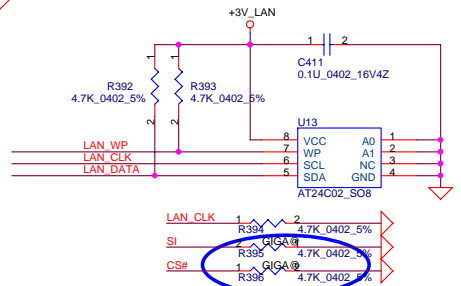
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.



2006/12/27



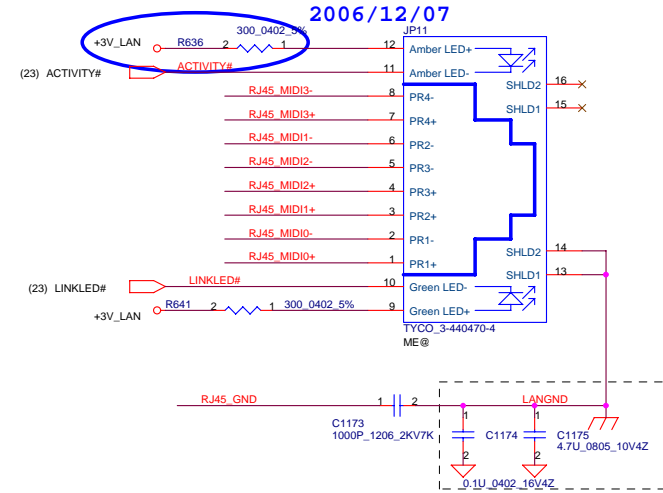
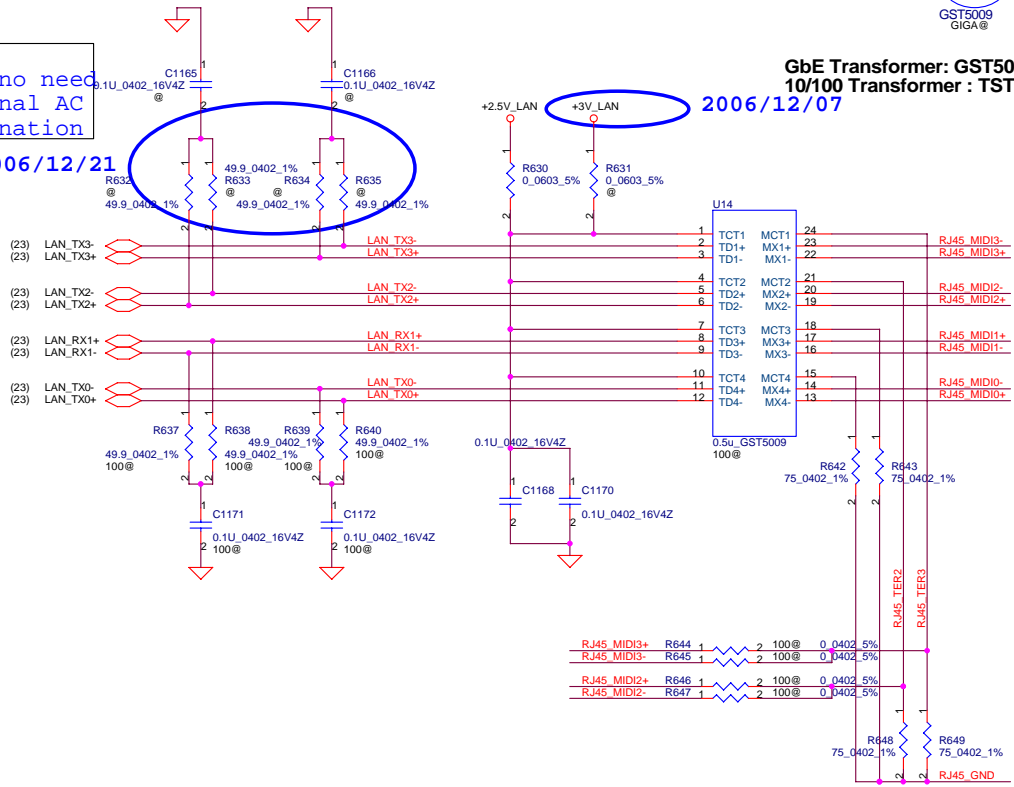
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Title			BCM5787MKML
Document Number			IGT10/11 LA-3591P
Date:	Tuesday, March 06, 2007	Sheet	23 of 48

5787 no need external AC termination

2006/12/21

2006/12/07

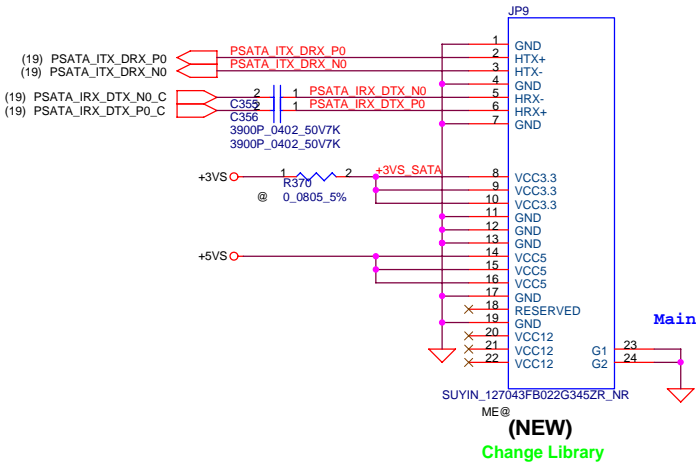
GbE Transformer: GST5009 (SP050005610)
10/100 Transformer : TST1284-LF (SP050001X10)



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				Date:	Tuesday, March 06, 2007	Sheet 24 of 48

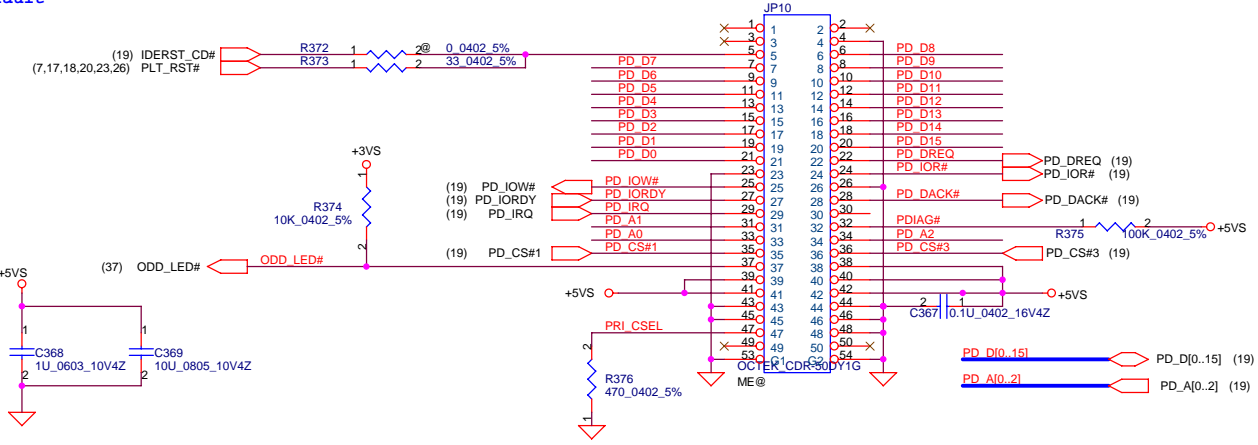
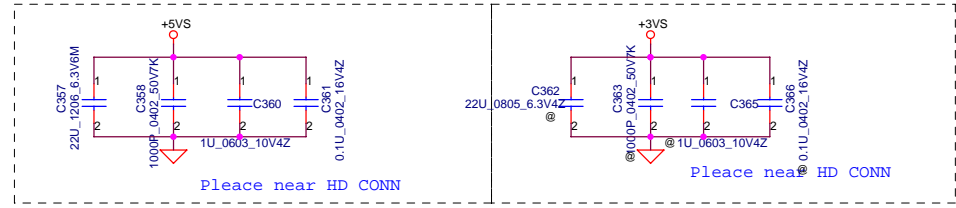
LAN CONN
IGT10/11 LA-3591P

SATA HDD Conn.

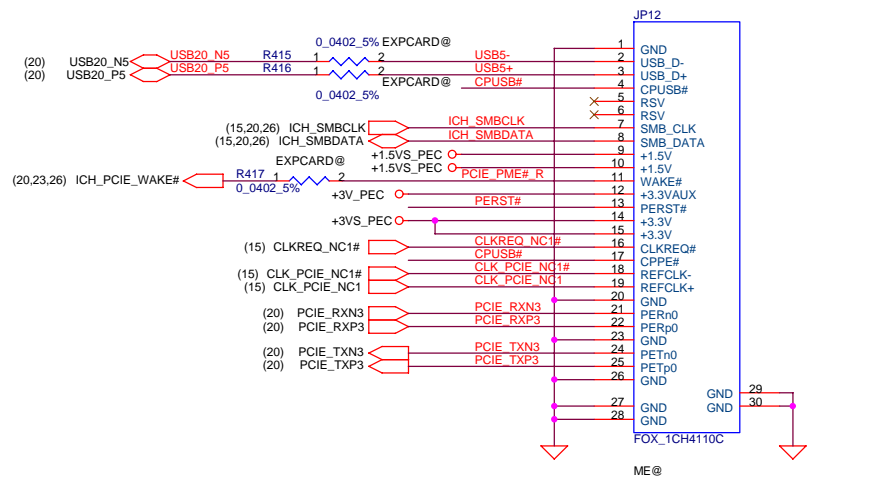
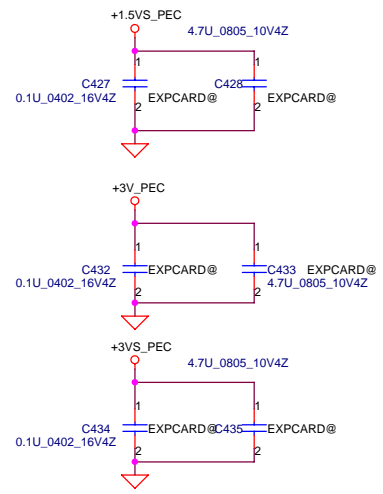
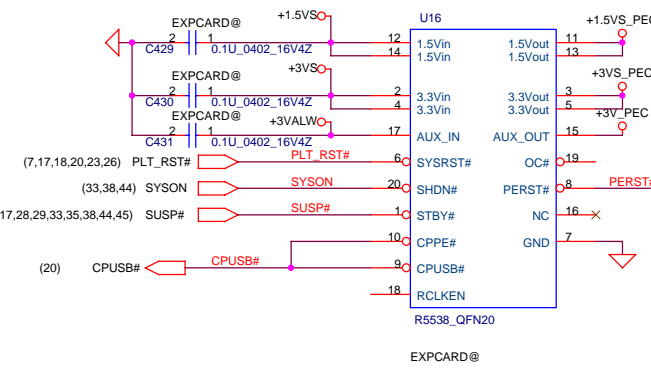


Main SATA +5V Default

(NEW)
Change Library



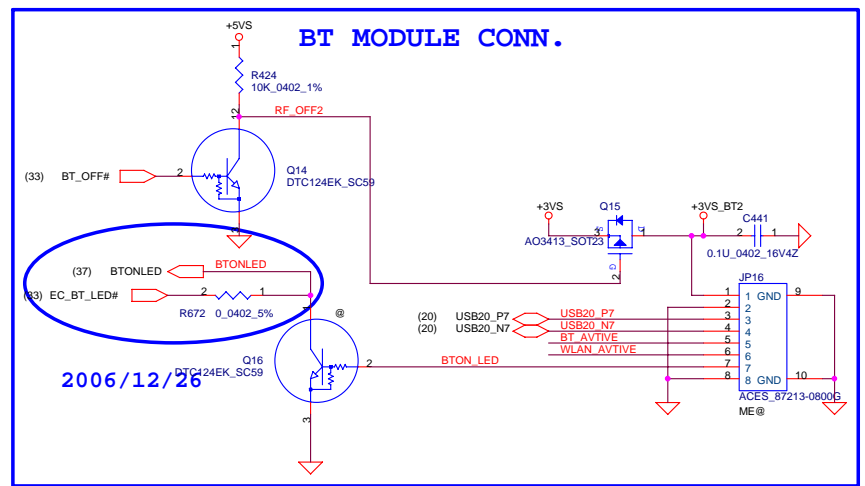
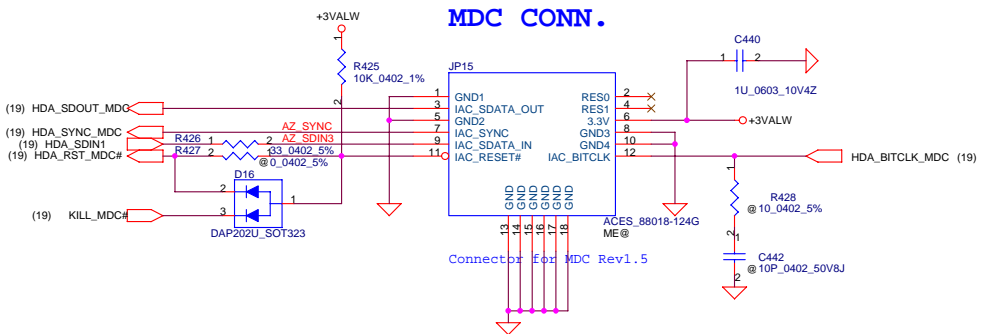
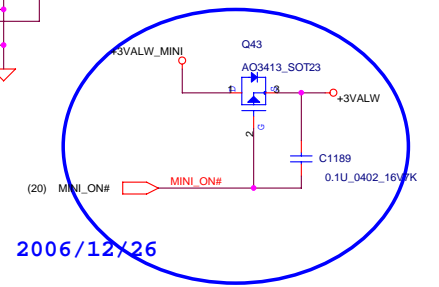
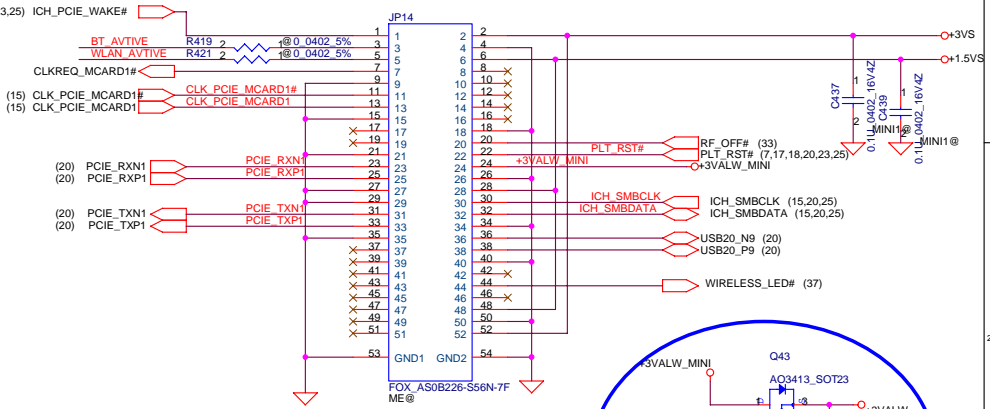
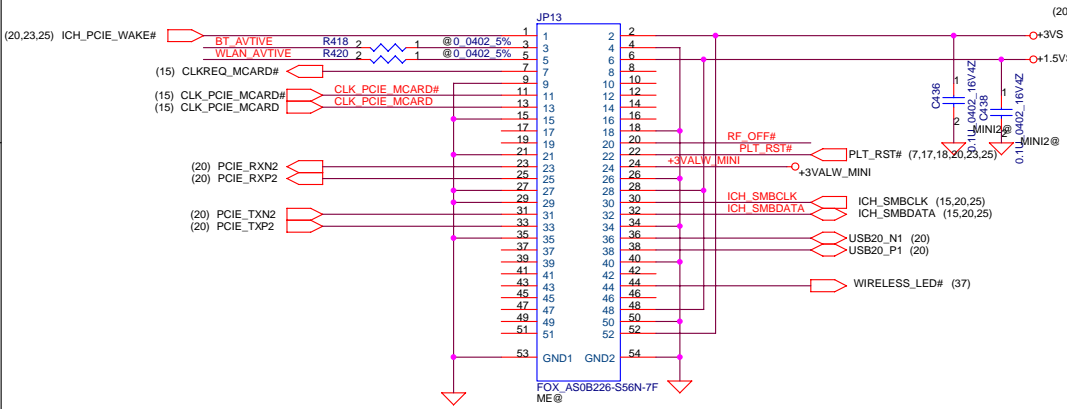
Express Card Power Switch



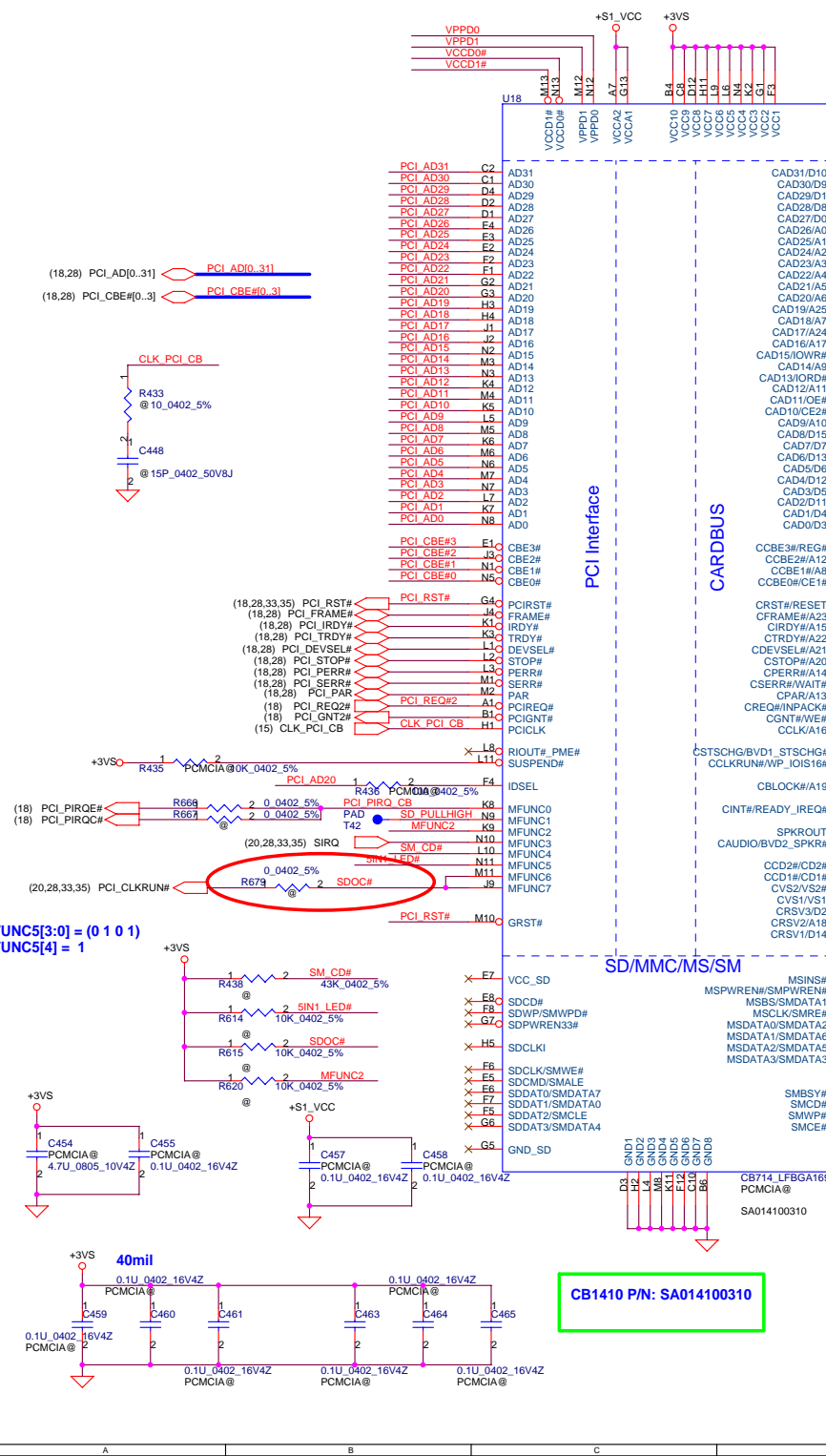
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			Sheet 25 of 48

Mini-Express Card(Slot 1-WLAN)

Mini-Express Card(Slot 2-TV-Tuner)

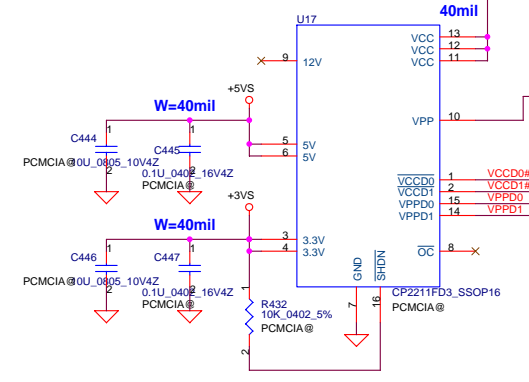


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				IGT10/11 LA-3591P
				Rev 0.2
Date: Tuesday, March 06, 2007				Sheet 26 of 48

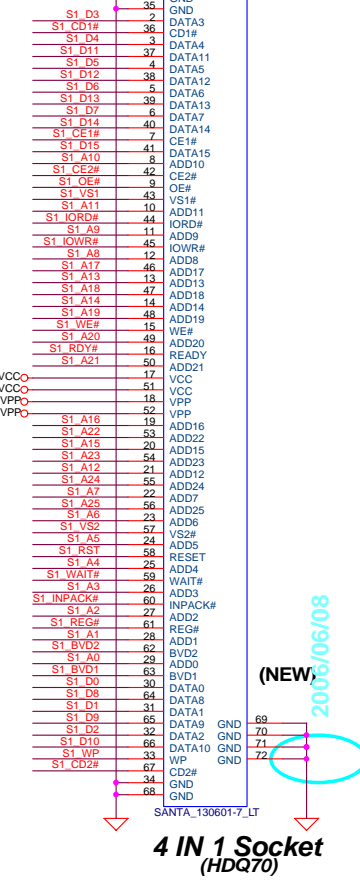


**IDSEL:AD20
(PIRQE#B#,
GNT#2,
REQ#2)**

PCMCIA Power Control



PCMCIA Socket



(NEW) 2006/06/08

4 IN 1 Socket (HDQ70)

CB1410 P/N: SA014100310

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Date:	Tuesday, March 06, 2007	Sheet	27	of 48	

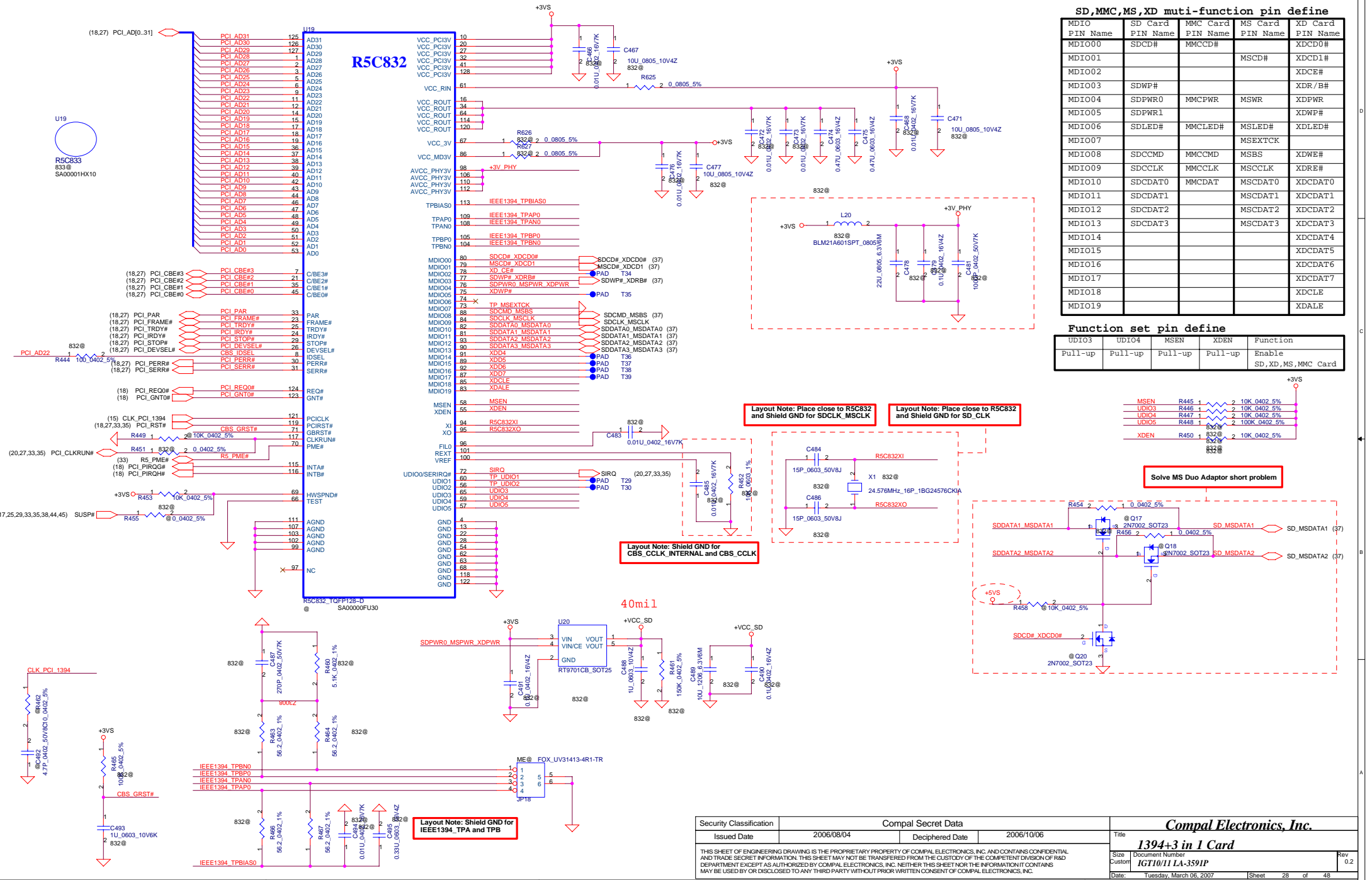
SD,MMC,MS,XD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLEL#	MSLED#	XDLED#
MDIO07				
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDR#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

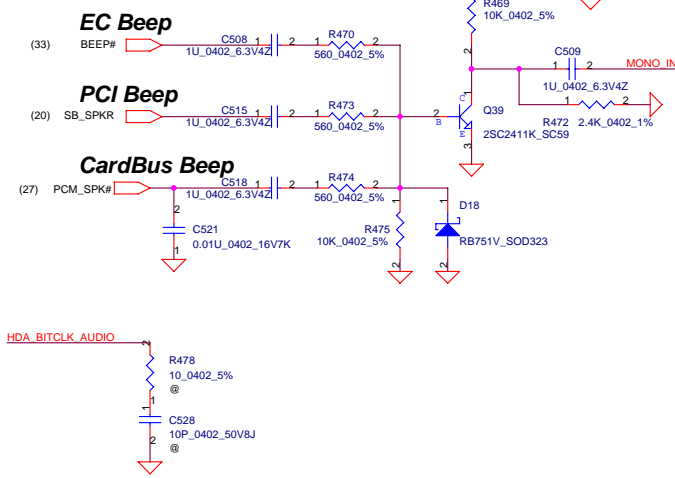
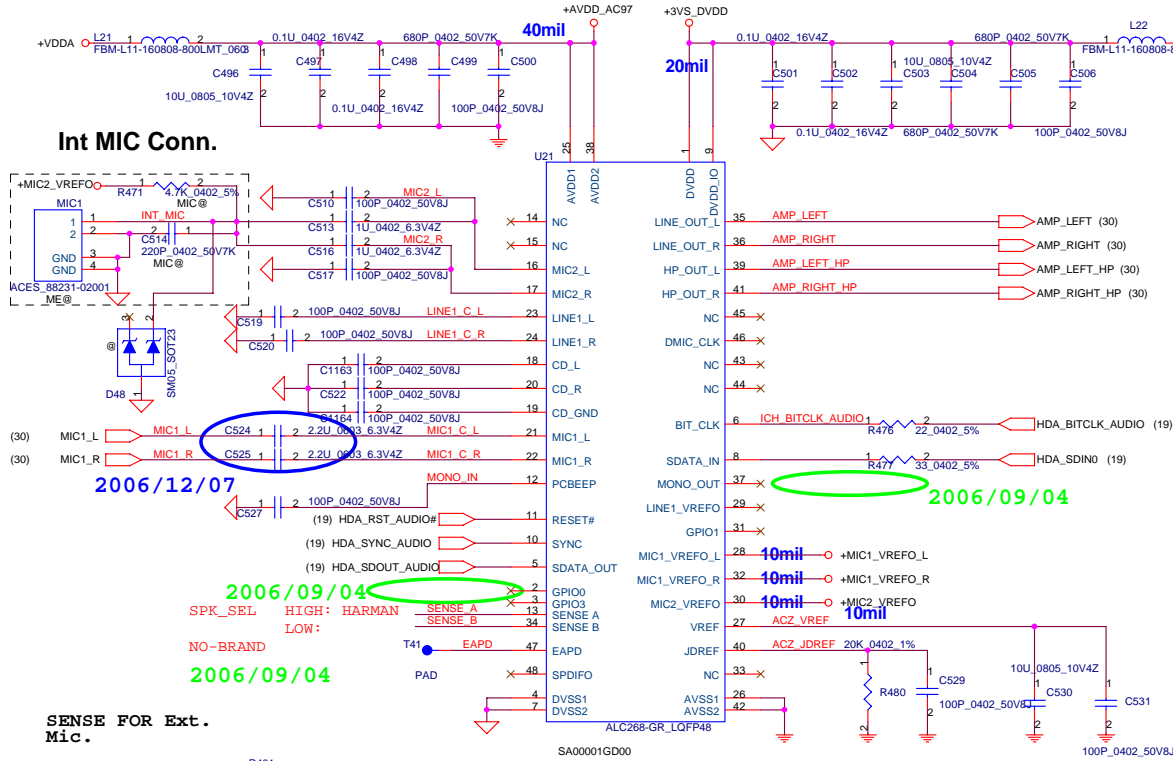
Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable

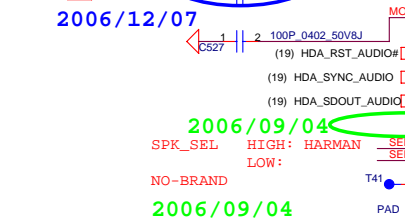
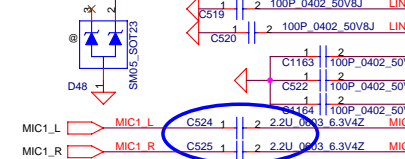
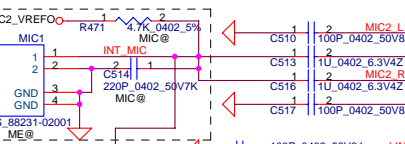
SD, XD, MS, MMC Card



HD Audio Codec



Int MIC Conn.



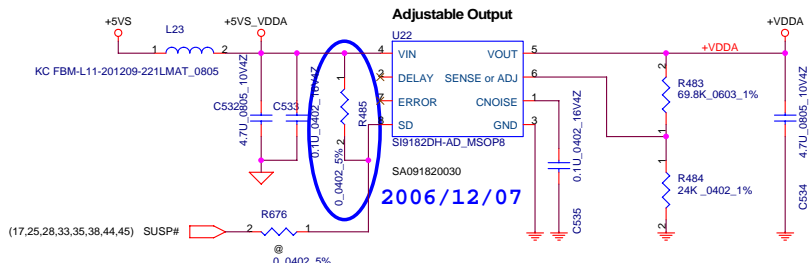
SENSE FOR Ext. Mic.

SENSE FOR Int. Mic.

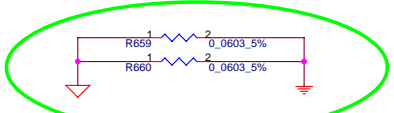
SENSE FOR HP

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Regulator for CODEC

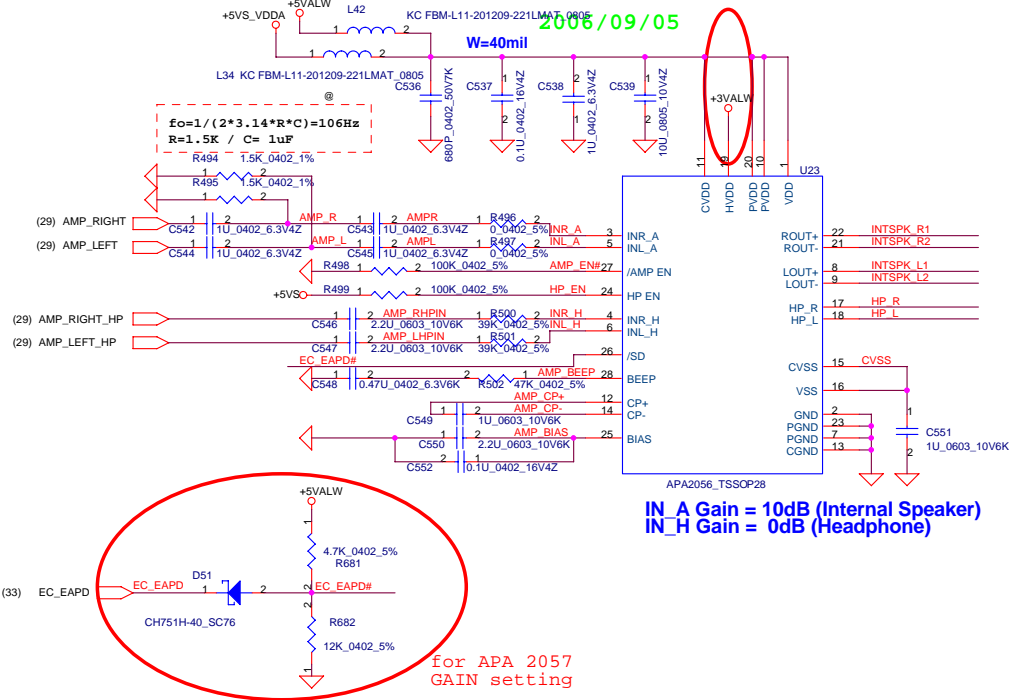


2006/09/04



2006/10/20

APA2056 SPK/HP Amplifier



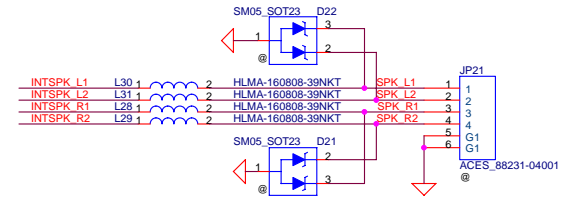
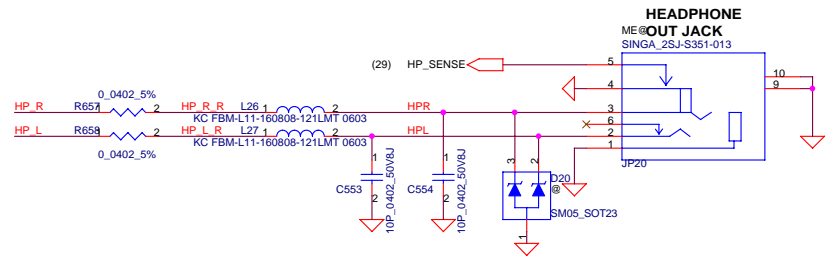
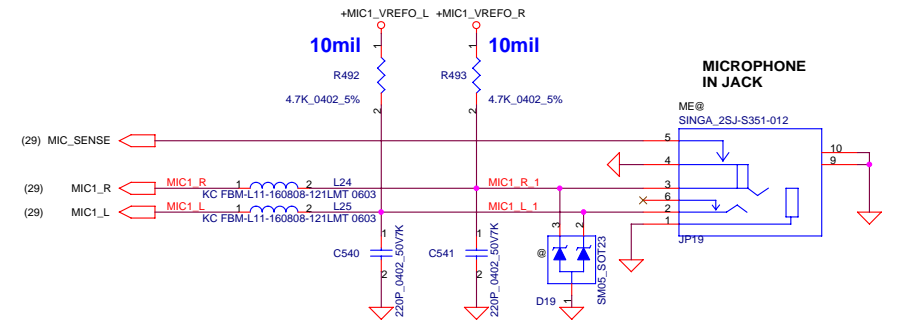
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

for APA 2057
GAIN setting

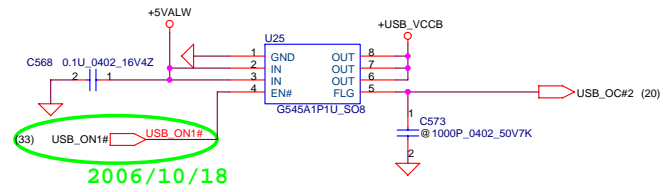
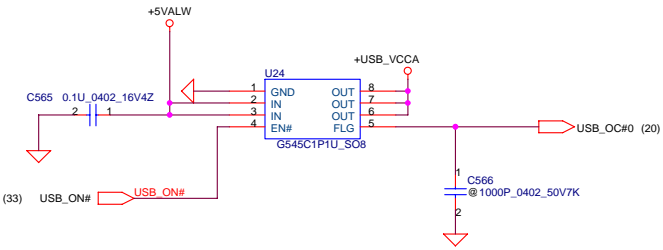
APA2057 gain setting table

gain	V	V(low)	V(high)
8		3.21	3.27
9		3.33	3.39
10		3.45	3.51

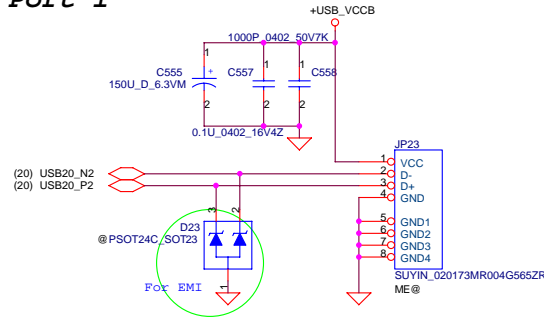
← current setting (3.48V)



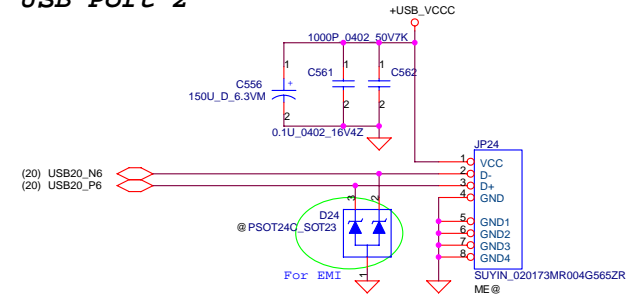
USB Port



USB Port 1

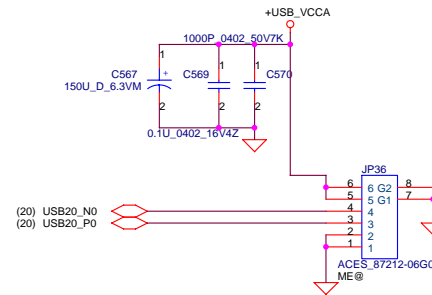


USB Port 2



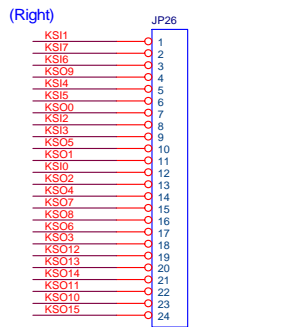
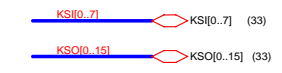
USB Port 3

USB board



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Date:	Tuesday, March 06, 2007	Sheet	31	of 48

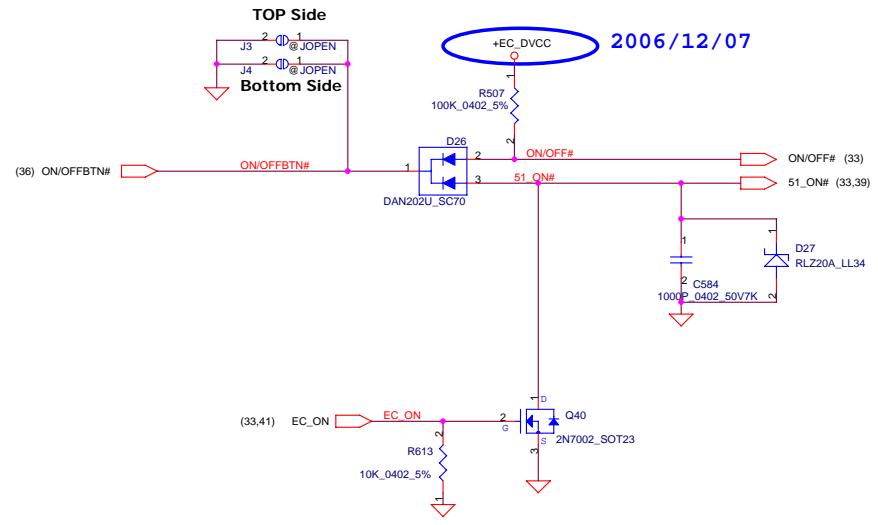
INT_KBD CONN



ACES_85201-24051
ME@

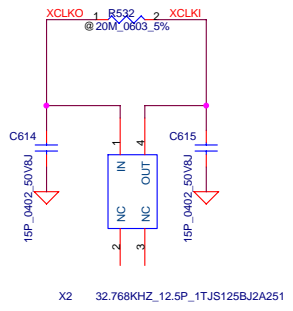
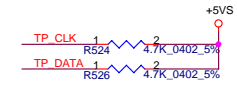
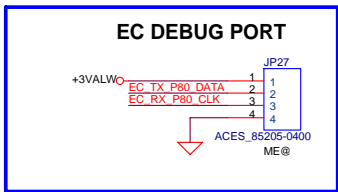
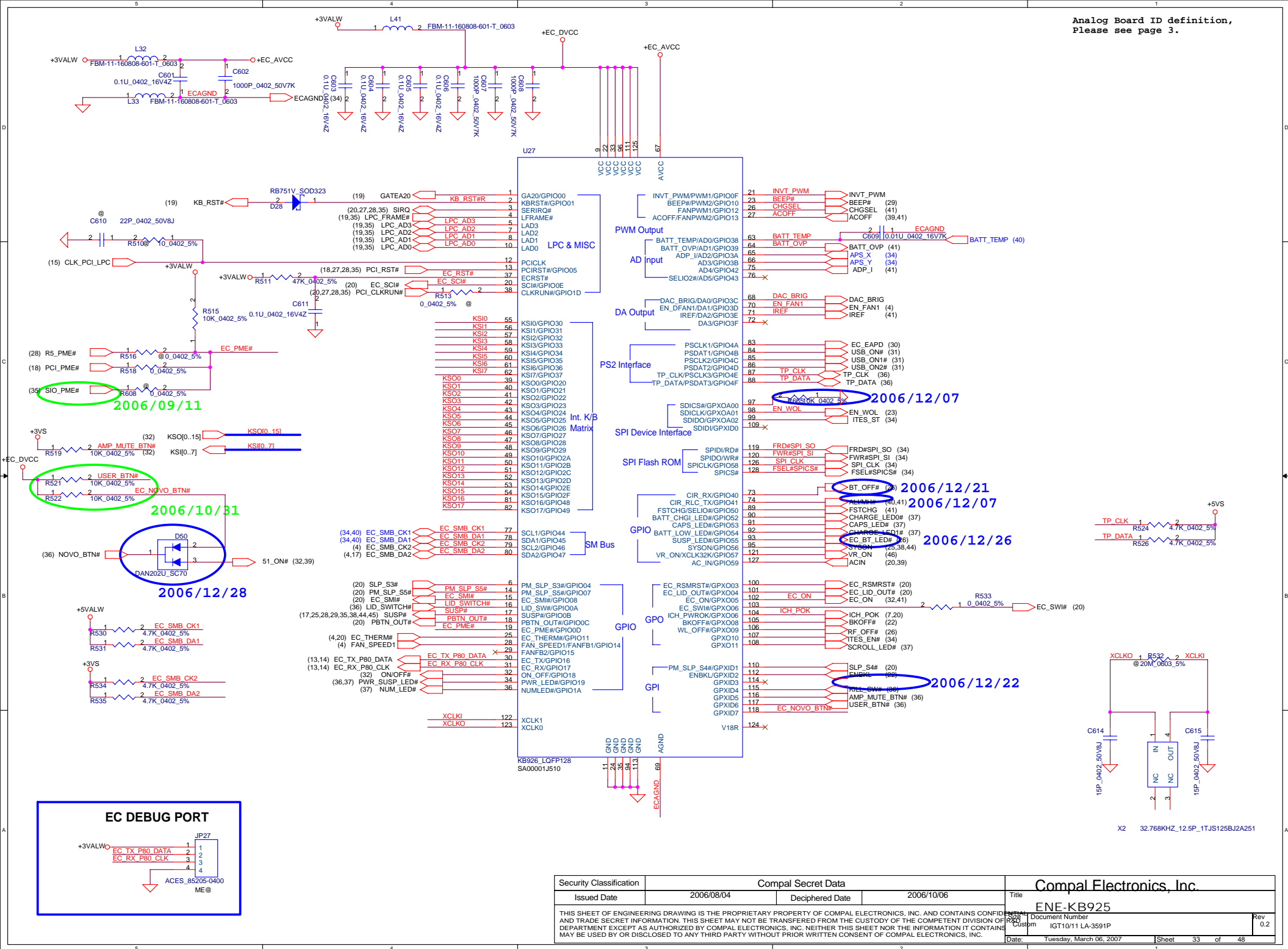
KSI1	@C576	1	2	100P_0402_50V8J
KSI7	@C577	1	2	100P_0402_50V8J
KSI6	@C578	1	2	100P_0402_50V8J
KSO9	@C579	1	2	100P_0402_50V8J
KSI4	@C580	1	2	100P_0402_50V8J
KSI5	@C581	1	2	100P_0402_50V8J
KSO0	@C582	1	2	100P_0402_50V8J
KSI2	@C583	1	2	100P_0402_50V8J
KSI3	@C585	1	2	100P_0402_50V8J
KSO5	@C586	1	2	100P_0402_50V8J
KSO1	@C587	1	2	100P_0402_50V8J
KSI0	@C588	1	2	100P_0402_50V8J
KSO2	@C589	1	2	100P_0402_50V8J
KSO4	@C590	1	2	100P_0402_50V8J
KSO7	@C591	1	2	100P_0402_50V8J
KSO8	@C592	1	2	100P_0402_50V8J
KSO6	@C593	1	2	100P_0402_50V8J
KSO3	@C594	1	2	100P_0402_50V8J
KSO12	@C595	1	2	100P_0402_50V8J
KSO13	@C596	1	2	100P_0402_50V8J
KSO14	@C597	1	2	100P_0402_50V8J
KSO11	@C598	1	2	100P_0402_50V8J
KSO10	@C599	1	2	100P_0402_50V8J
KSO15	@C600	1	2	100P_0402_50V8J

Power BTN



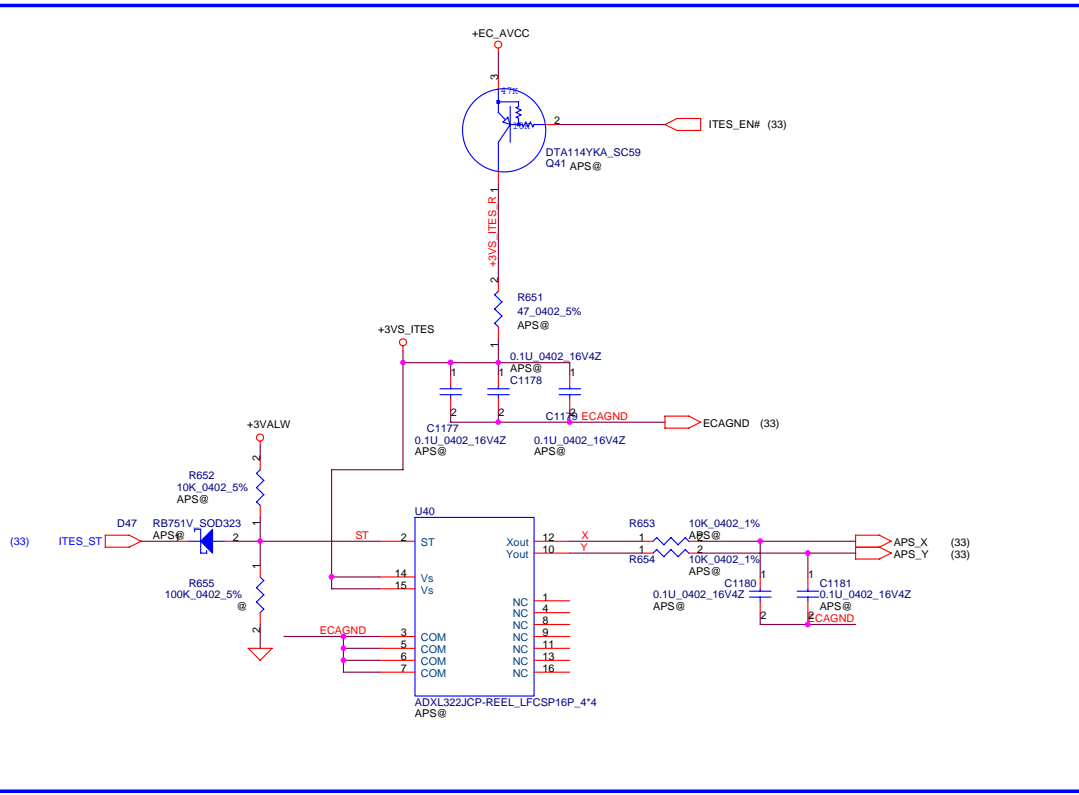
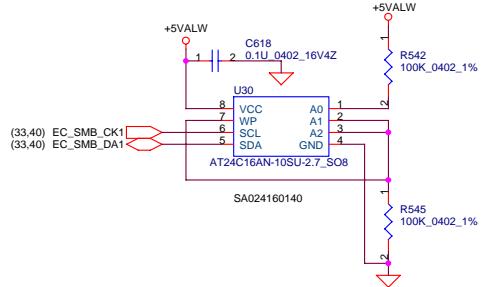
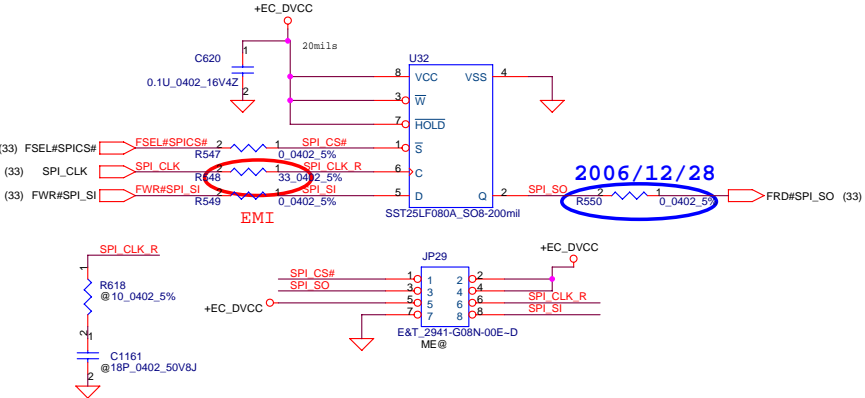
2006/12/07

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				IGT10/11 LA-3591P
				Rev 0.2
				Date: Tuesday, March 06, 2007
				Sheet 32 of 48



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				Customer	IGT10/11 LA-3591P
				Date	Tuesday, March 06, 2007
				Sheet	33 of 48

SPI Flash (8Mb*1)

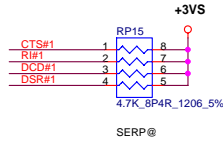
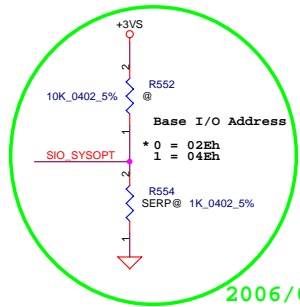


2006/10/14

DEL ISA
BIOS

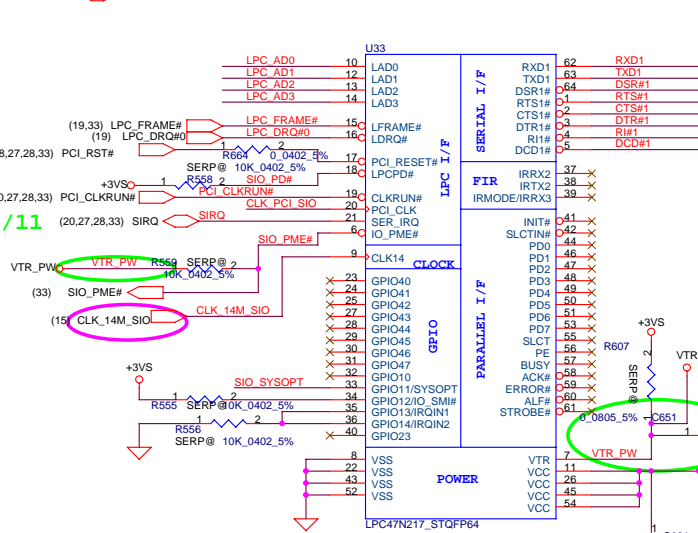
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				Tuesday, March 06, 2007		0.2
				Sheet		48

SUPER I/O SMsC LPC47N217

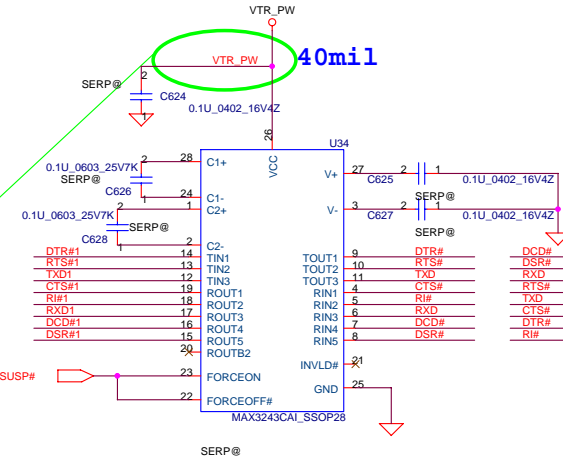
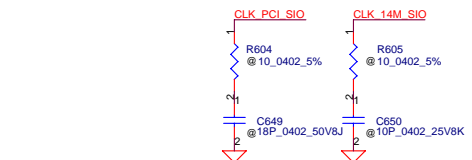


(19.33) LPC_AD[0..3] \Rightarrow LPC_AD[0..3]

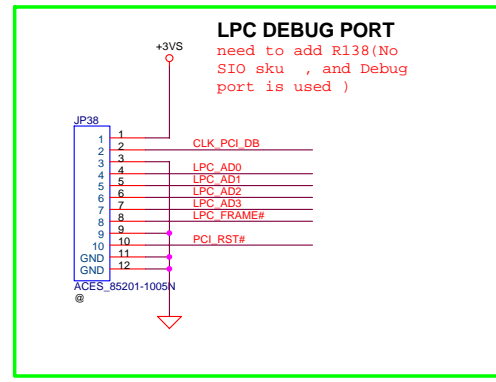
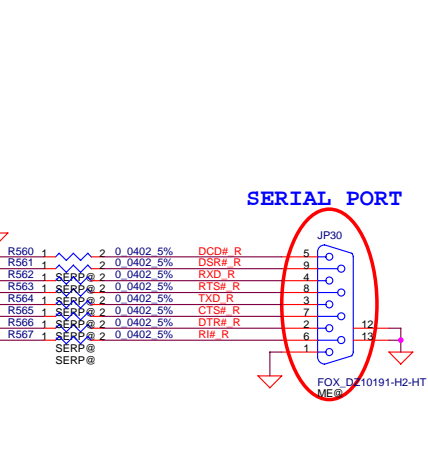
2006/09/11



Close to u33 pin



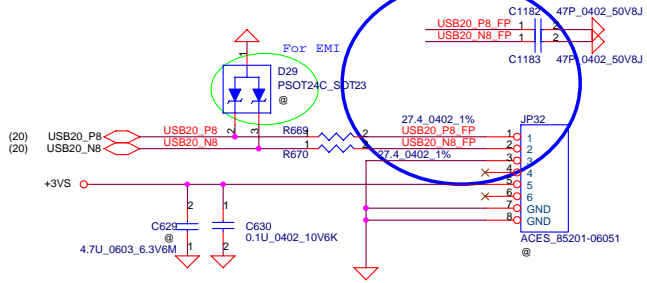
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Date:	Tuesday, March 06, 2007	Sheet	35	of 48	

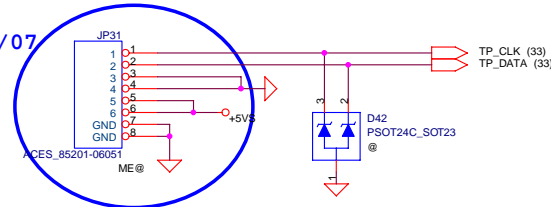
Finger Print

2006/12/22

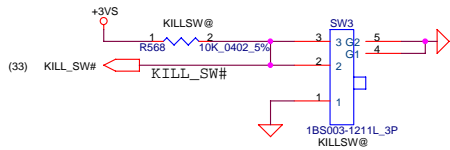


T/P Board

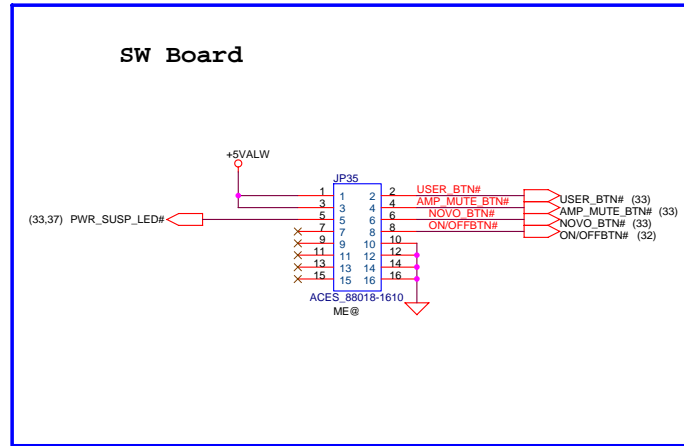
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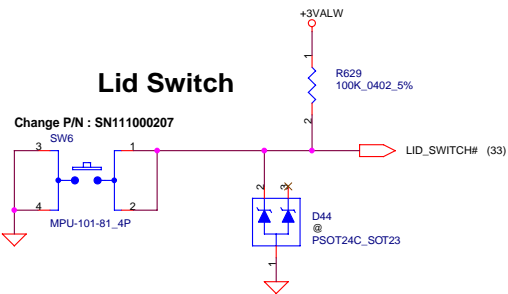
Kill Switch



SW Board



LID Switch



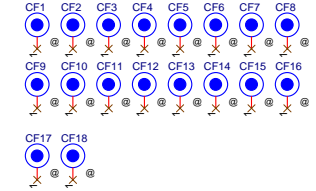
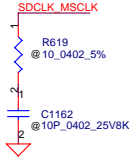
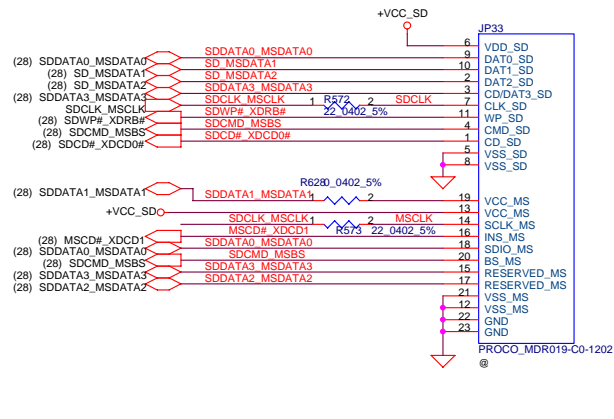
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Date: Tuesday, March 06, 2007				Sheet 36 of 48

Compal Electronics, Inc.

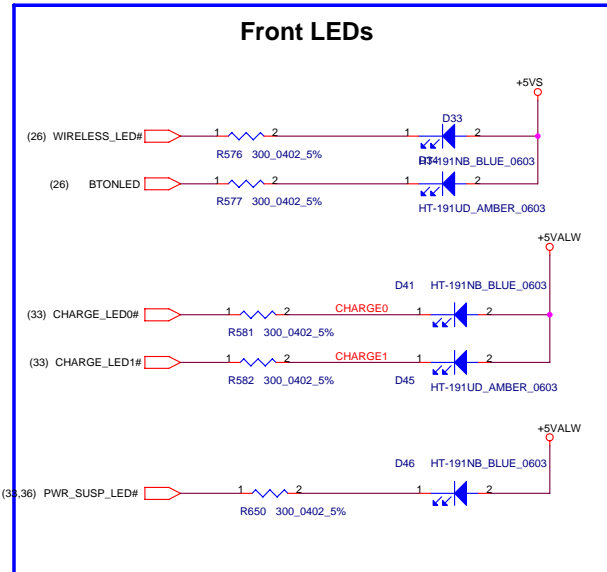
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IGT10/11 LA-3591P

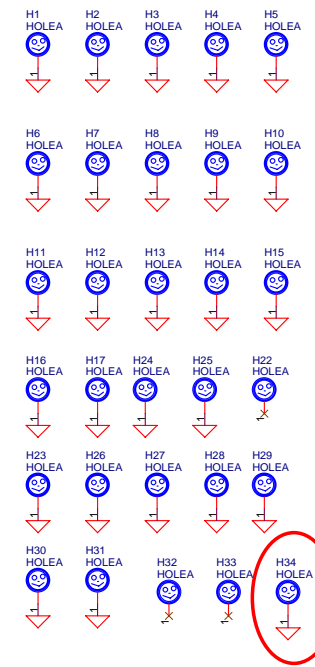
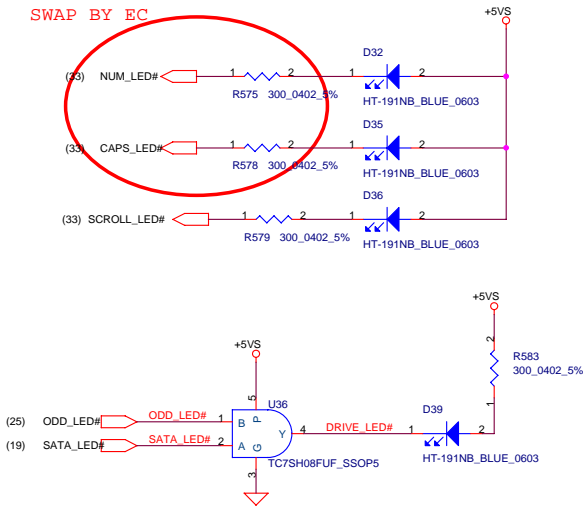
3 in 1 Card Reader



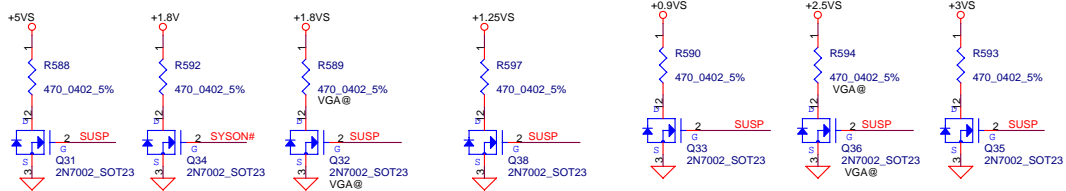
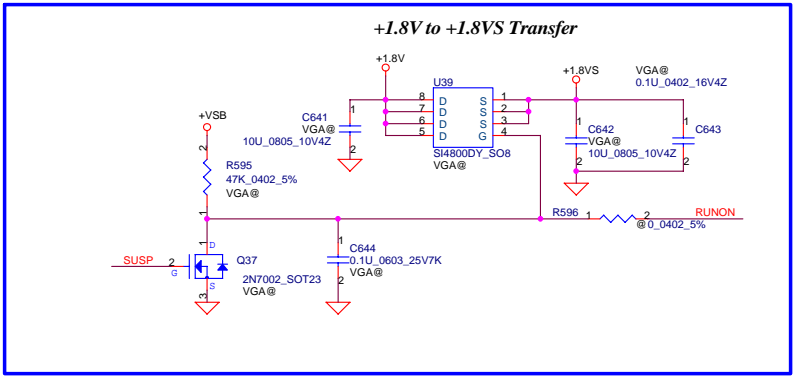
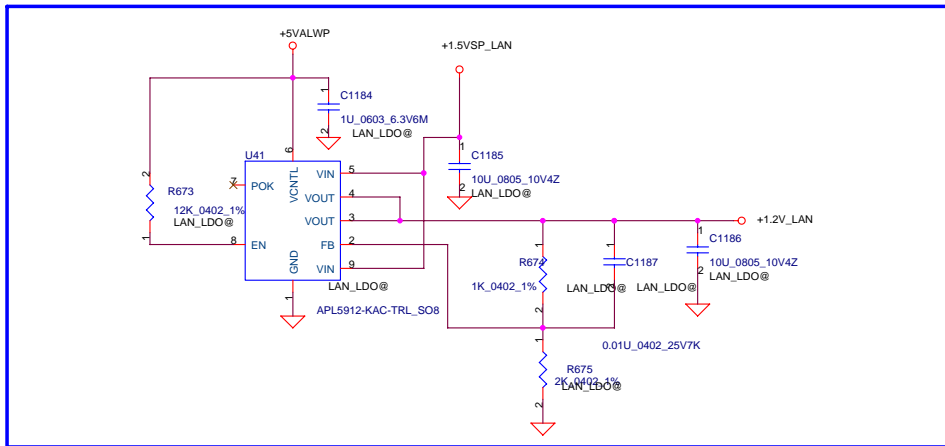
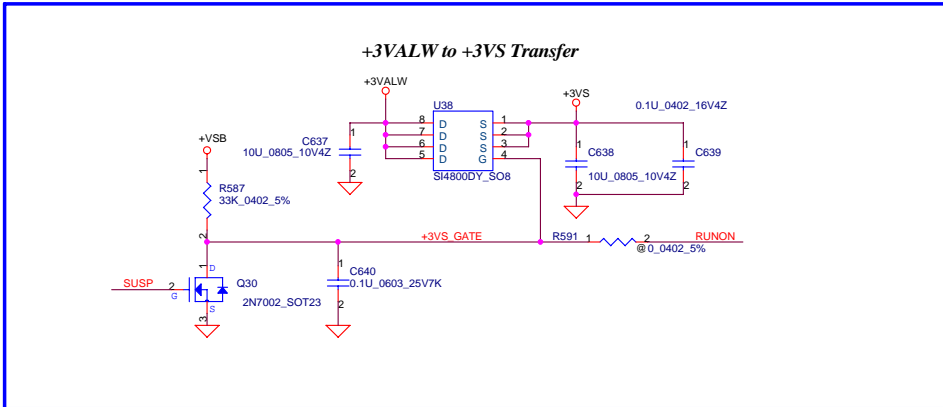
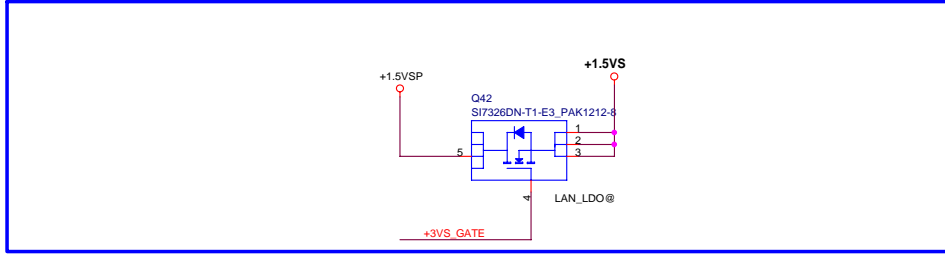
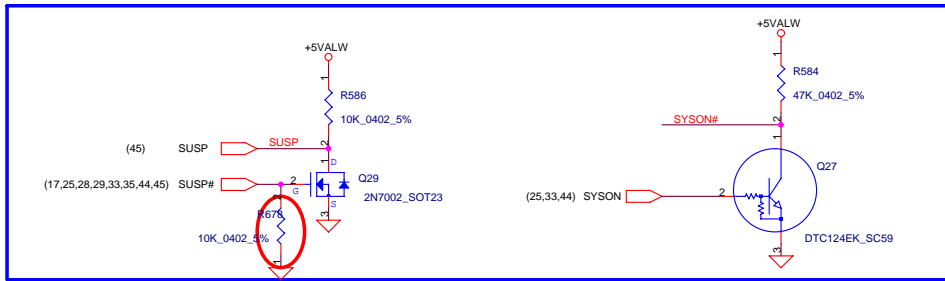
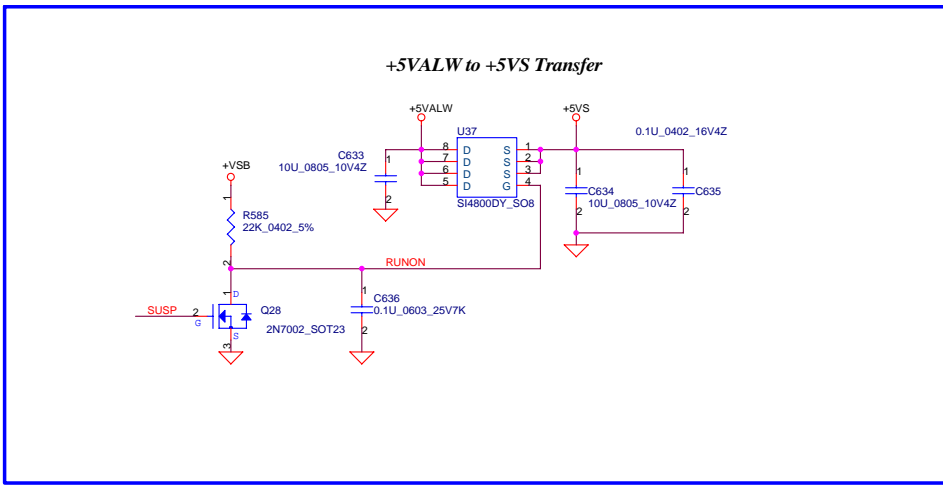
Front LEDs



SWAP BY EC



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			Sheet	Rev
			37	0.2
			of	48



Security Classification	Compal Secret Data		Title	
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Date: Tuesday, March 06, 2007				Sheet 38 of 48

OCP==>8A
Vripple=

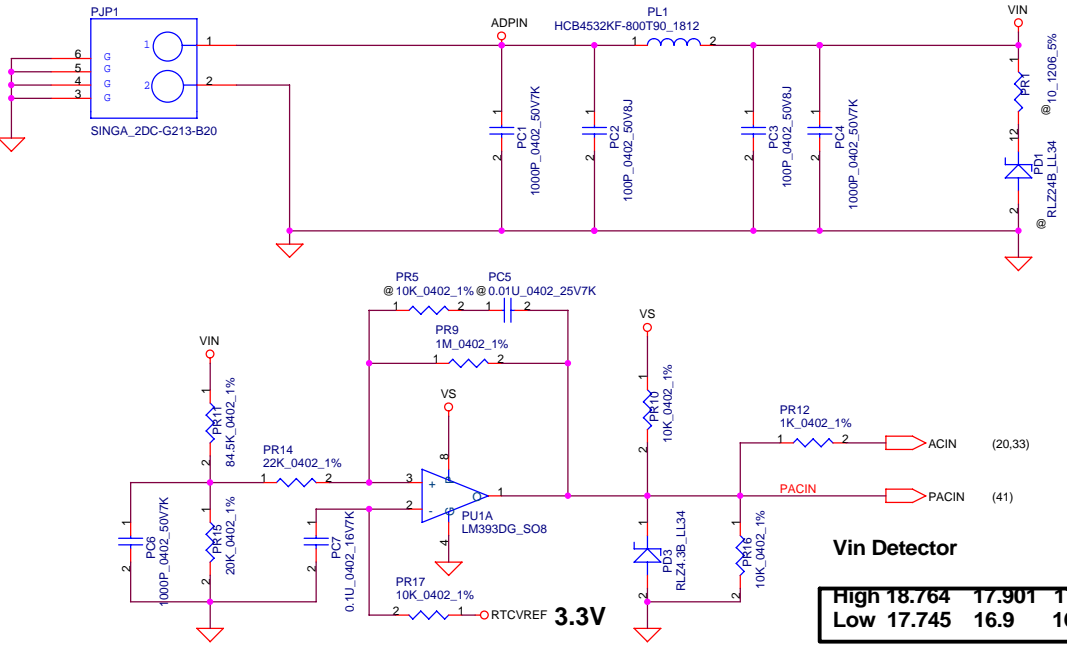
DC231000400

ACIN

BATT ONLY

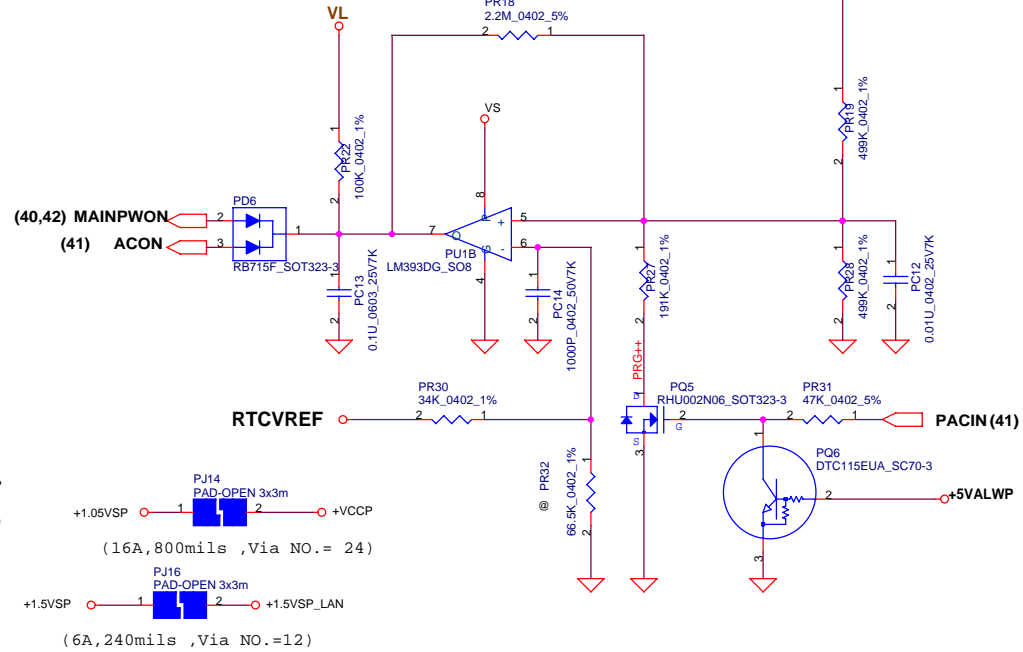
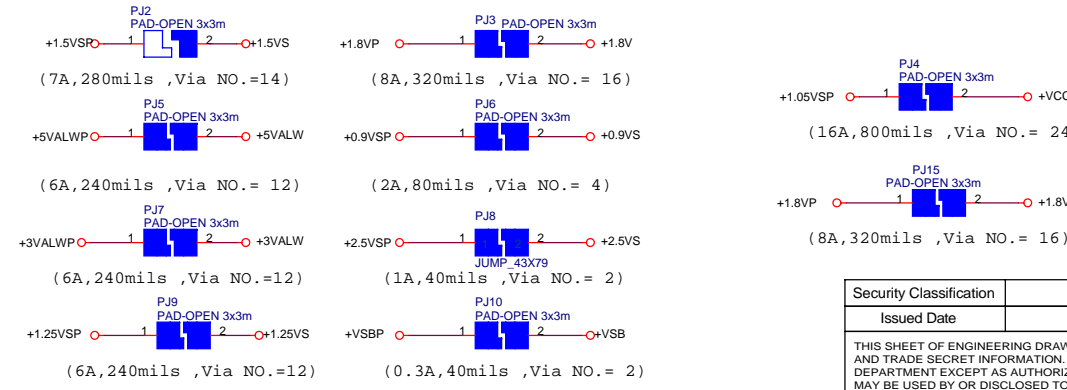
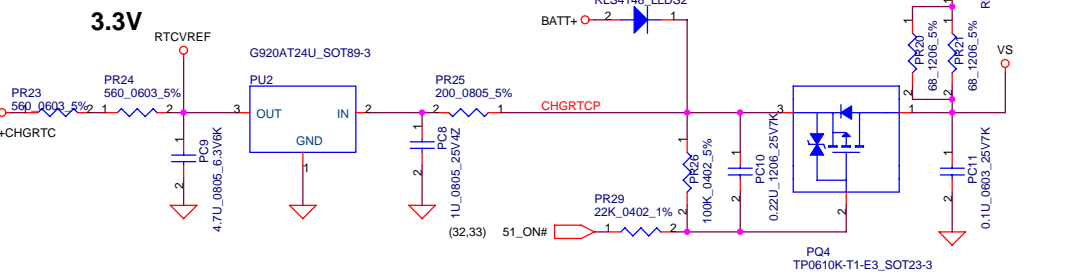
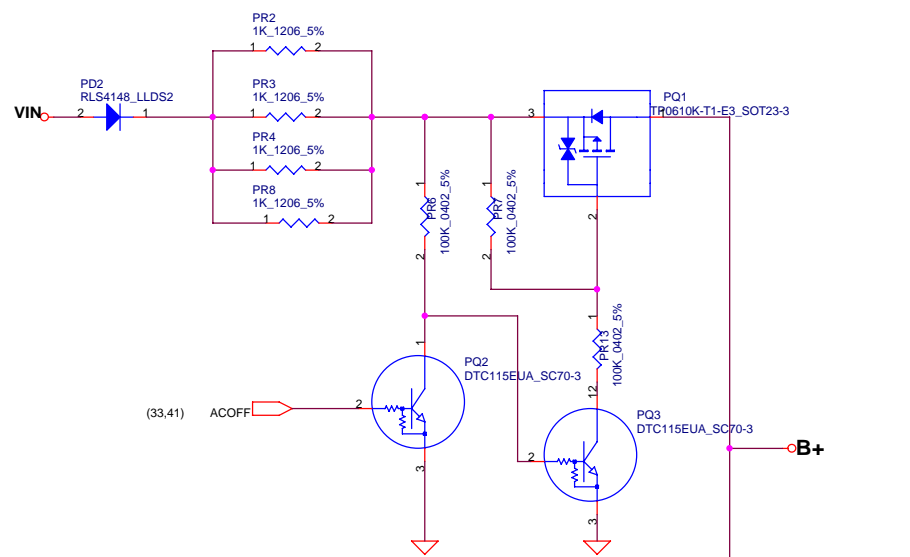
	Precharge detector	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V	
L->H	15.562V	15.97V	16.388V	

	Precharge detector	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V	
L->H	7.196V	7.349V	7.505V	



Vin Detector

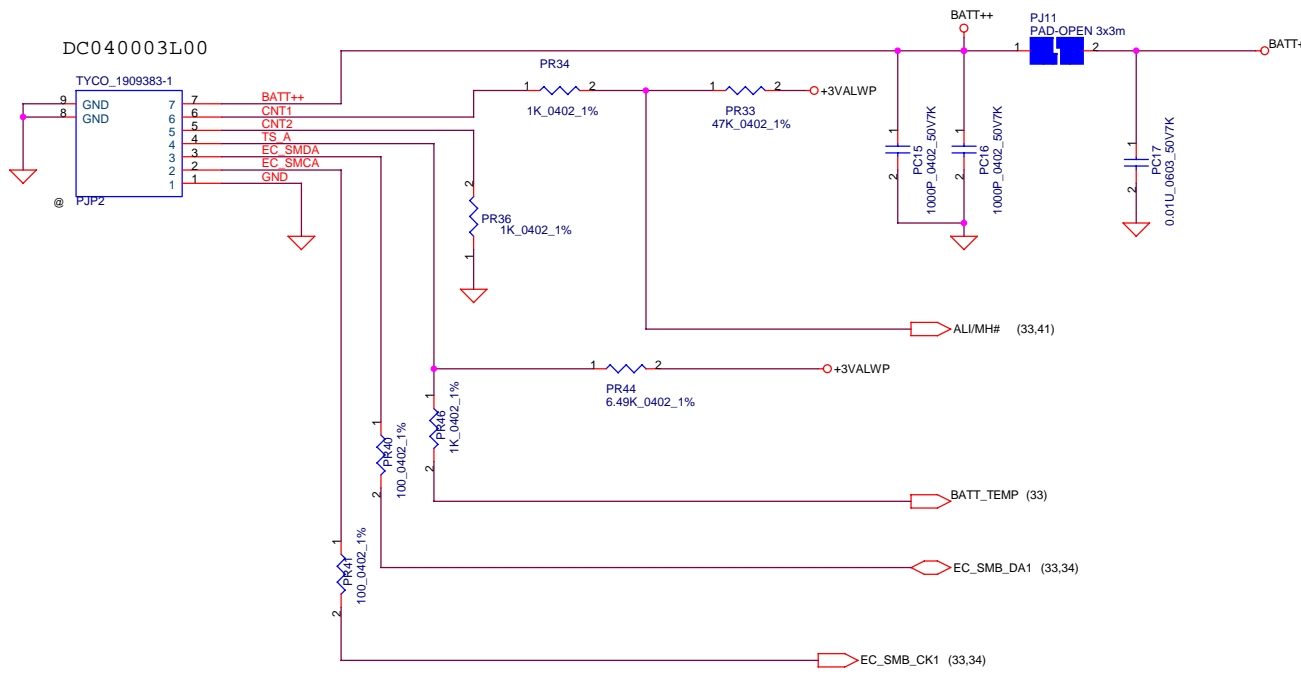
High	18.764	17.901	17.063
Low	17.745	16.9	16.03



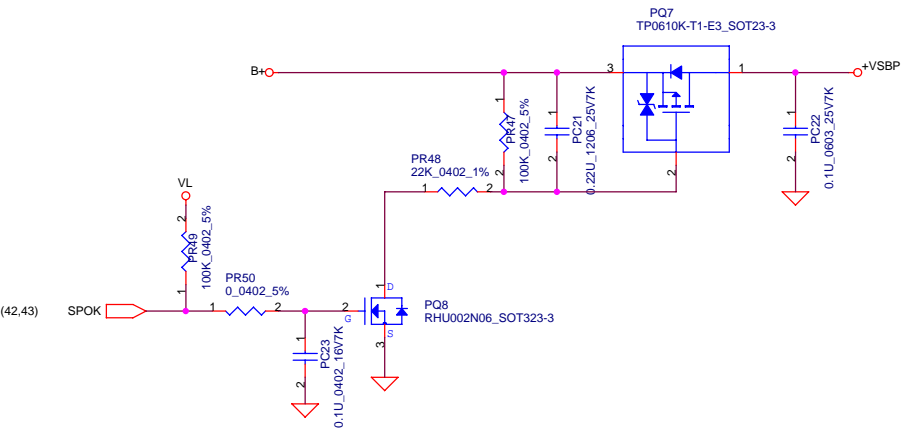
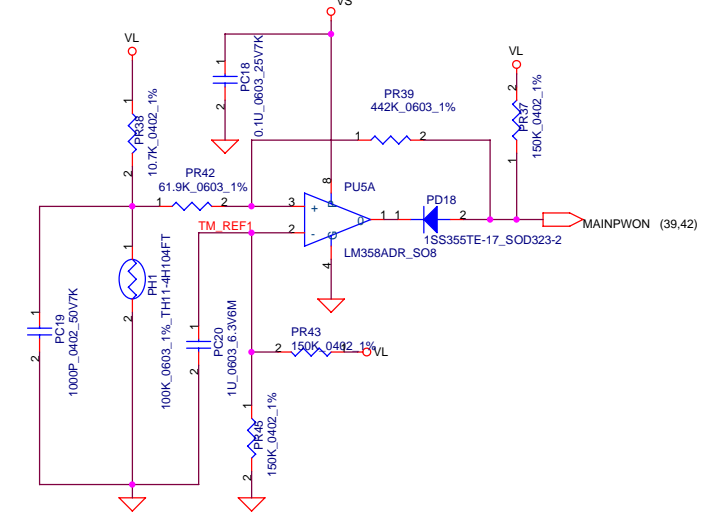
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DCIN/DECTOR		
Title	Document Number	Rev
		0.2
Date:	Tuesday, March 06, 2007	Sheet 39 of 48



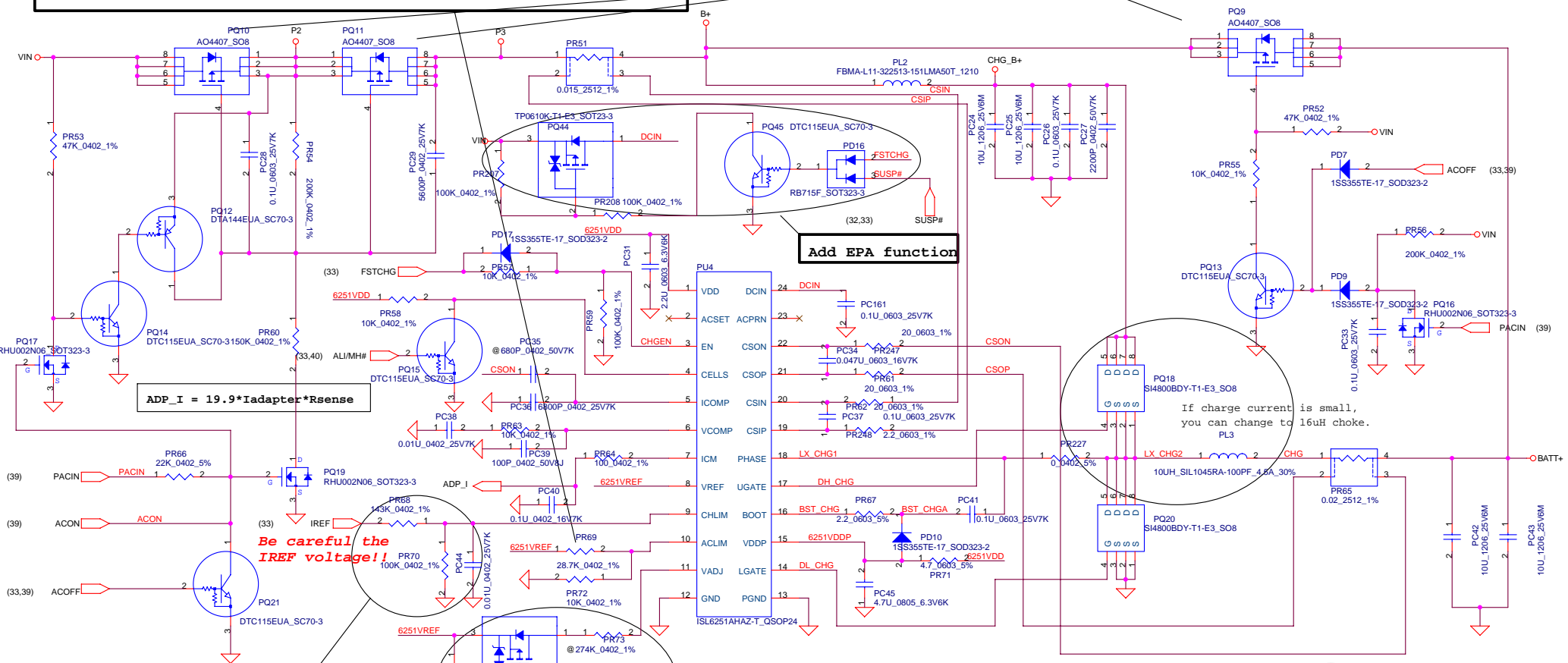
PH1 under CPU bottom side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C



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Date:	Tuesday, March 06, 2007	Sheet	40 of 48	

65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A
 90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A

65W PQ10,PQ11,PQ9->FDS4435



Add EPA function

$ADP_I = 19.9 * I_{adapter} * R_{sense}$

Be careful the IREF voltage!!

If this area float, charge voltage is 4.2V/cell

If charge current is small, you can change to 16uH choke.

Overshoot solution during CC->CV

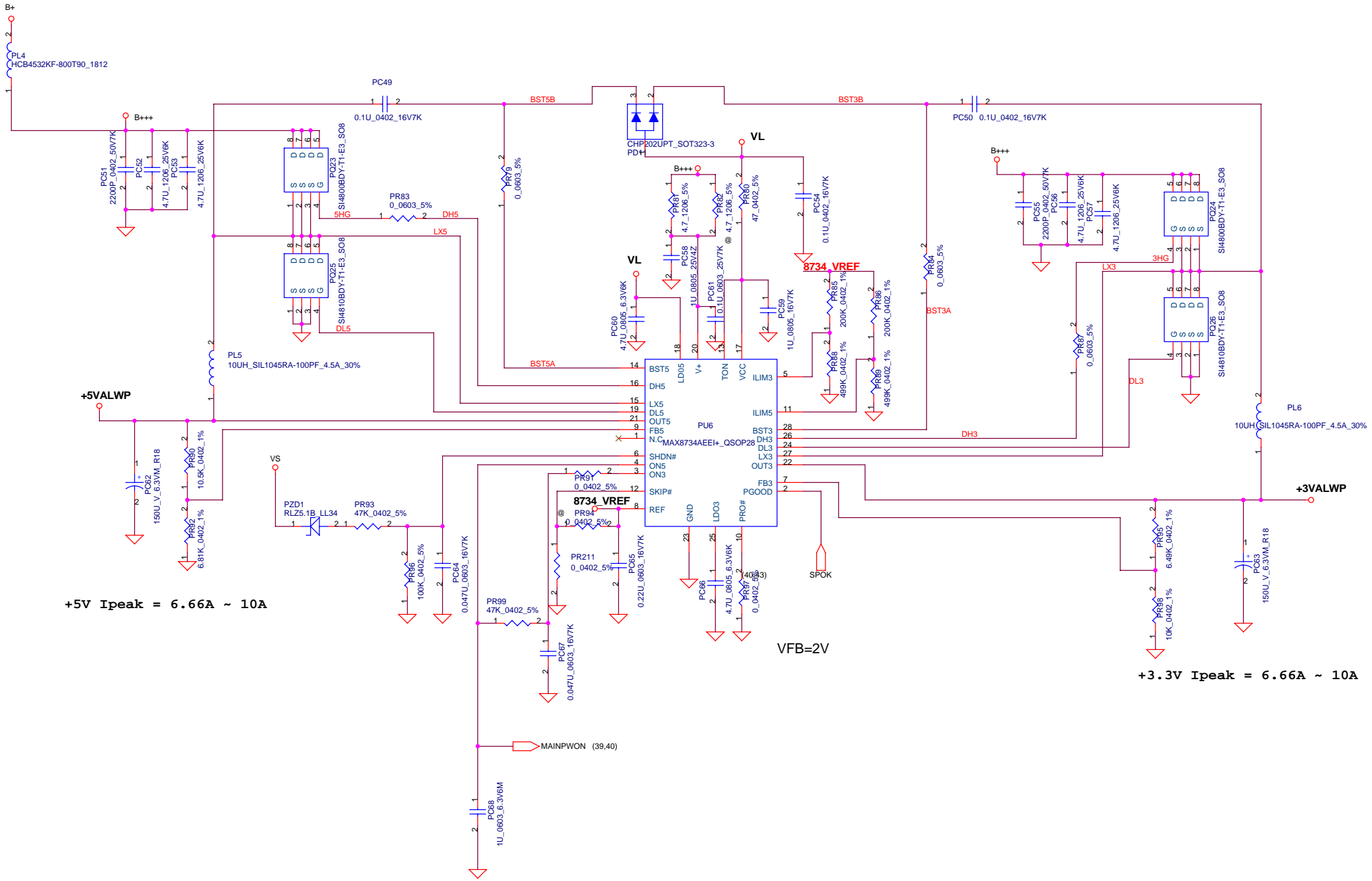
CP mode
 $I_{input} = (1/0.02) * (0.05 * V_{a1m} / 2.39 + 0.05)$
 where $V_{a1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{a1m} = 0.6667V$, $I_{input} = 4.263A$

CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 * I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

Charge Voltage
 3S CC-CV MODE : 12.6V (CELLS=GND, ALI/MH#=3.3V)
 4S CC-CV MODE : 16.8V (CELLS=VDD, ALI/MH#=0V)

OVP voltage :
 LI-3S : 13.50V -- BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+

BATT Type	Charging Voltage (0x15)	ALI/MH#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

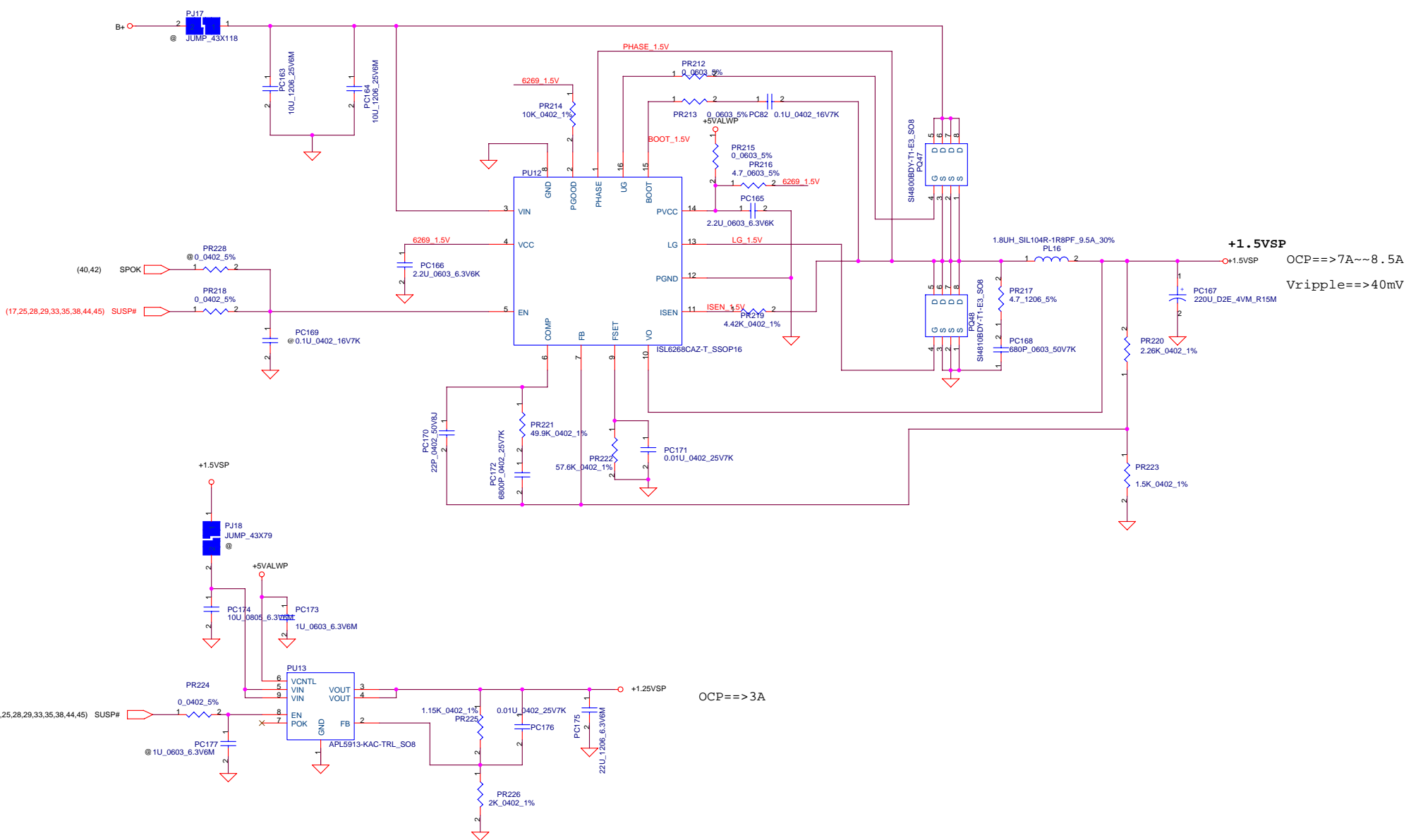


+5V I_{peak} = 6.66A ~ 10A

VFB=2V

+3.3V I_{peak} = 6.66A ~ 10A

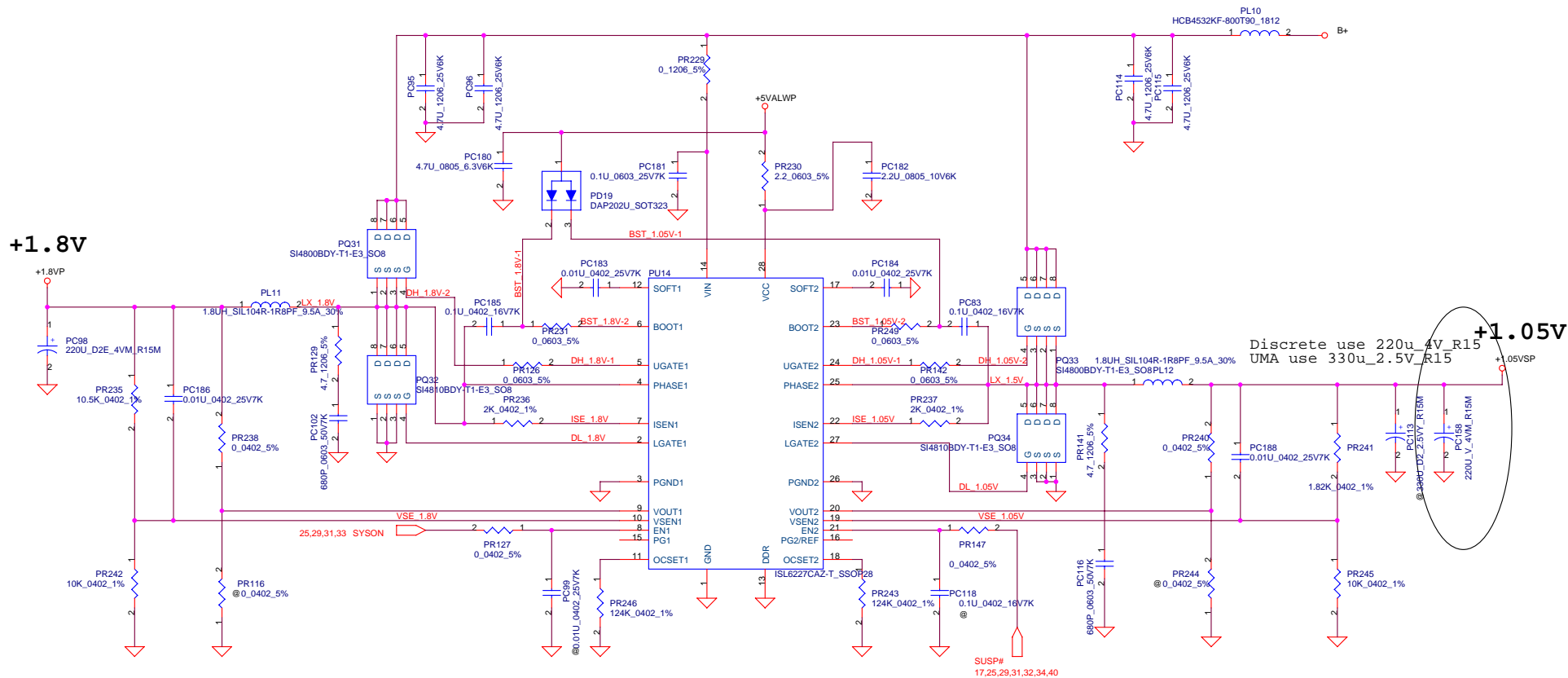
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Date:	Tuesday, March 06, 2007	Sheet	42 of 48	Rev 0.1



+1.5VSP
 OCP==>7A~8.5A
 Vripple==>40mV

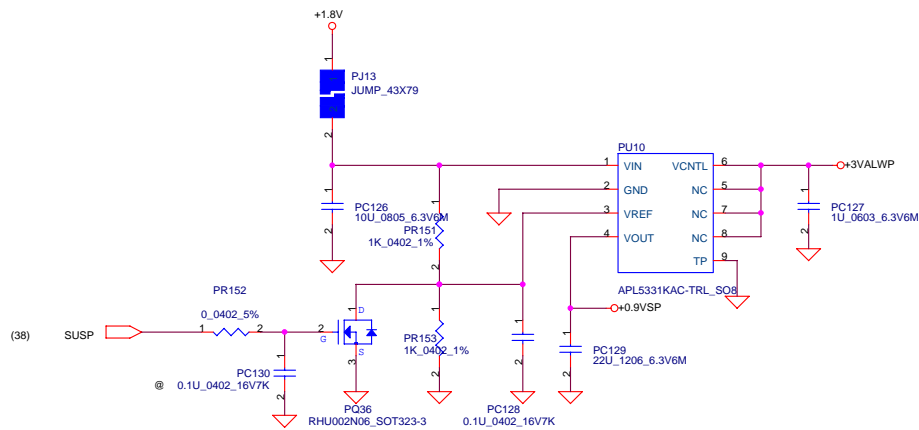
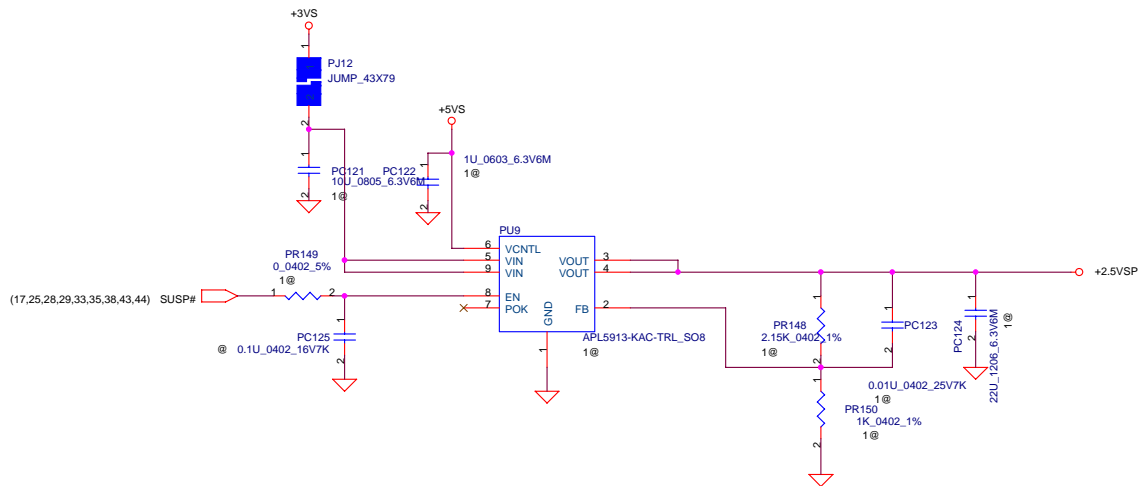
OCP==>3A

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Date: Tuesday, March 06, 2007				0.1
Sheet 43 of 48				

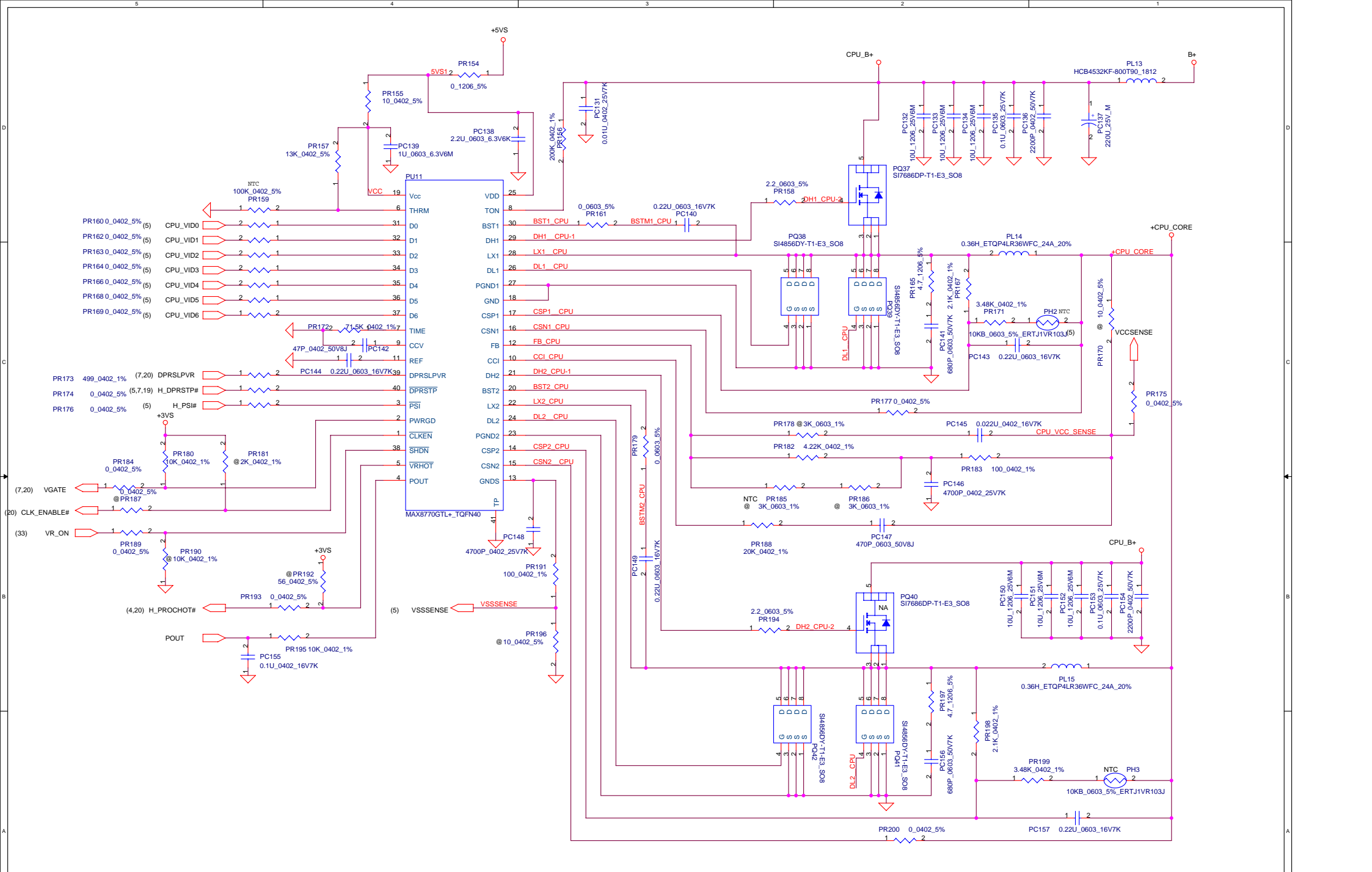


Discrete use 220u_4V_R15
UMA use 330u_2.5V_R15

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Date: Tuesday, March 06, 2007				1
Sheet 44 of 48				0.1



Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/17	Deciphered Date	2006/10/17	2.5VSP0.9VSP
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Date: Tuesday, March 06, 2007				Sheet 45 of 48



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Issued Date	2005/10/17	Deciphered Date	2006/10/17	Title
				+CPU_CORE
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Date:	Tuesday, March 06, 2007	Sheet	46 of 48	

page	Reason for change	Modify list
EVT P39,P42,P43,P44,P46	Shortage issue : needs to change another source	SM010018210 Replace
P46	Shortage issue : needs to change another source	Change SB578400080 to SB000008L80
DVT P39	1.Inrush decrease 2.Change to Standard part	1.Change PC1/PC4 from 0.01U to 1000P 2. PR1/PD1 no function,Change PD5 from RB751V to RL4148;Add PC6
P40	1.LM358A replace of LM393 2.Add Diode to anti reverse voltage 3.Modify component size	1.PU5A replace of PU3A 2.Add PD18 close to PU5A 3.Change PC15/PC16 from 0603 to 0402
P41	1.Add BATT-OVP function 2.Overshoot solution during CC<->CV 3.Change torlance 4.Change to Standard part 5. Add PR227 to anti reverse voltage 6. 65W change to Standard part 7.Add EPA Function	1.Change PR78 value from 150K to 105K 2-1.Add PR209 ,PC162 ,PR210 ,PQ44 ,PC161 ,PQ45 ;Del PQ46/PC30 2-2.Del PD8 ; Add PD17 3. Change torlance from 0 ohm 5% to 10Kohm 1% at PR57 4. PD10: Change CH751H to 1SS355TE ; original PU5B to PU5A; Del PC46;Change PQ20 from SI4810 to SI4800 5. PR227 : currently use 0ohm. (In the future use 2.2ohm) 6. Change PQ9/P10/PQ11 to FDS4435; Change PR69 to 39.2K 7.Add PD16/PR57/PR208/PR207/PC161
P42	1.Change 5V/3.3V in SKIP mode 2.Change to Standard part 3.For EPA function	1.Add PR211 (@ PR94) 2-1.Change PC62/PC63 from SGA20151360 to SF22001M300 2-2. Change PC49/PC50 from 0603_25V7K to 0402_16V7K 2-3. Change PL5/PL6 from 4.7UH to 10UH 3.Change PR95 from 6.81K to 6.49K
P43	Update 1.5VSP/1.25VSP to Standard part	1-1.Reduce capacitor value from 22u_1206_6.3V6M to 10u_0805_6.3VM at PC174 1-2.Change from dual PWM IC to single PWM IC for 1.5VSP (PU12), Del PU7,PC69,PC71,PC72, ,PC74,PC75,PC76,PC77,PC78,PC79,PC80,PC81,PC82,PC83,PC84, PC85,PC86,PC87,PC88,PC90,PC91, PC93,PC94,PD12,PD13,PL7,PL8,PL9,PQ27,PQ28,PQ29,PQ30, PR100,PR102,PR103,PR104,PR105,PR106,PR107,PR108,PR109,PR110,PR111,PR112,PR113,PR114 ,PR115,PR116,PR117,PR118,PR119,PR120,PR121,PR122,PR123 Add Part:PC82,PC163,PC164,PC165,PC166,PC167,PC168,PC169PC170,PC171,PC172,PC173,PC174, PC175,PC176,PC177,PJ17,PJ18,PL16,PQ47,PQ48,PR212,PR213,PR214,PR215,PR216,PR217,PR218, PR219,PR220,PR221PR222,PR223,PR224,PR225,PR226,PR228 1-3.APL5913(PU13) replace of APL5912
P44	Update 1.05VSP/1.8VP to Standard part	1-1.Change PC107/PC110/PC100 size from 0603 to 0402 1-2.Change PD14/PD15 from RB751 to 1SS355TE 1-3.Change PC158 size from R9M to R15M;Change PC98 from NEC to Panasonic 1-4.Add PC113
P45	Update 2.5VSP/0.9VSP to Standard part	1-1.Change PC121 capacitor from 22u_1206_6.3V6M to (@ 10U_0805_6.3VM) 1-2. APL5913 replace of APL5912 at PU9 1-3.Change PC126 capacitor from 22u_1206_6.3V6M to 10U_0805_6.3VM 1-4. Add PR149 1-5.UMA part : Del total 2.5VSP circuit->PU9/PC122/PC121/PR148/PR150/PC123/PC124/PR149
P46	Update +CPU_CORE to Standard part	1-1.Change PC132/PC133/PC134/PC150/PC151/PC152 size from 10u_1206_25VAK to 10u_1206_25V6M 1-2.Change PQ38/PQ39/PQ41/PQ42 from 8113 to SI4856 1-3.Change PR158/PR194 from 0ohm to 2.2ohm 1-4.Change PC137 to 3000hrs

Title			<Title>
Size	Document Number	Rev	
Custom:Doc>		<RevCode>	
Date:	Tuesday, March 06, 2007	Sheet	47 of 48

B-TEST

page	Reason for change	Modify list
P22	DFX ISSUE	ADD RP49- RP52
P26	LED control by EC	ADD R672
P30	Reduce "bo" sound when enter sleep mode	ADD L42
P35	DFX ISSUE	Del SIO debug port
P36	F/P DFX	ADD C1182 C1183 R669 R670

C-TEST

page	Reason for change	Modify list
P10	fixed tv out ripple	ADD L43 C1190
P35	fixed COM PORT function	re connect L4M & mirror jp30 connection
P38	fixed 1st ac plug in then led flash	SUSP# pull low lok (add r678)