COMPAL CONFIDENTIAL

MODEL NAME : AAL15

PCB NO : DA800140000

BOM P/N :

GPIO MAP:

SKL-U+MEC1404 VC board

2015-07-09

REV : 1.0 (A00)

@ : Nopop Component
i3SKL2.3GR1@/i5SKL2.3GR1@/i7SKL2.5GR1@/SKL1.6G23R1@:CPU R1
i3SKL2.3GR3@/i5SKL2.3GR3@/i7SKL2.5GR3@/SKL1.6G23R3@:CPU R3
UMA@/DIS@ : UMA & DIS Type
DSX@/N_DSX@: DSX Mode
EMI@/ESD@/HDMI@EMI@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Nopop Component
CMC@ : XDP Component
CONN@ : Connector Component
100@/1000@/LAN_SW@ : LAN type
3234@/3246@ : CODEC type
CRT@/HDMI@ : CRT/HDMI
TP_WAKE@/NOTP_WAKE@ : TouchPad wake
ODD@/NOZPODD@/ZPODD@ : ODD and Zero Power

EXOR1@/MESOR1@ : GPU R1
EXOR3@/MESOR3@ : GPU R3
EXO@/MESO@ : GPU relative component
2G_H@/2G_S@/2G_M@/4G_H@/4G_S@/4G_M@ : VRAM type
V_4G@ : 4G VRAM Support component

ZZZ **PCB**

DAZ1GG00100
PCB@

PCB AAL15 LA-D071P LS-D071P/D072P/D073P
(LS-D071P/D072P/D073P/B844P/B845P/B915P)

ZZZ **PCB**

DA800140000
MB@

PCB 1G9 LA-D071P REV0 M/B 4

UC1 **CPU R1**

i7-R1 — SA000092P2L — i7SKL2.5GR1@
FJ8066201930408 SR2EZ D1 2.5G BGA

i5-R1 — SA000092O2L — i5SKL2.3GR1@
FJ8066201930409 SR2EY D1 2.3G BGA

i3-R1 — SA000092N3L — i3SKL2.3GR1@
FJ8066201931104 SR2EU D1 2.3G BGA

i5(2+3e) ES0 — SA00008Y40L — SKL1.6G23@
FJ8066201930823 QJ57 J0 1.6G

UC1 **CPU R3**

i7-R3 — SA000092P3L — i7SKL2.5GR1@
FJ8066201930408 SR2EZ D1 2.5G A31!

i5-R3 — SA000092O3L — i5SKL2.3GR3@
FJ8066201930409 SR2EY D1 2.3G A31!

i3-R3 — SA000092N4L — i3SKL2.3GR3@
FJ8066201931104 SR2EU D1 2.3G A31!

Layout Dell logo

REV: X00
PWB: 9HTP8

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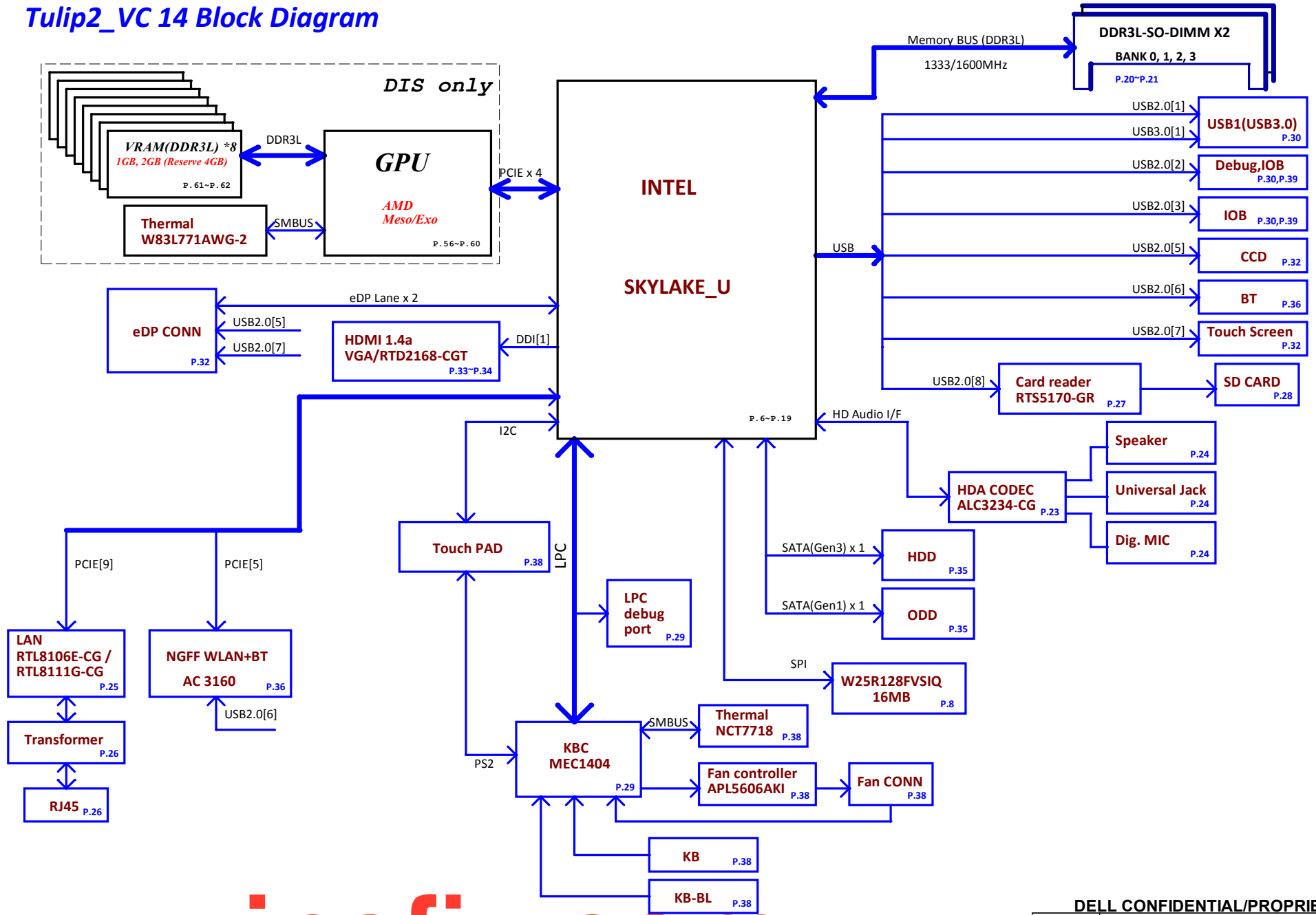
Tulip2_VC 14 Block Diagram



Compal Electronics, Inc.

Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State \ power plane	+1.0V_PRIM +RTC_CELL +1.8V_EDRAM +1.8V_PRIM +5VALWP +3VALWP +5VALW +3VALW +1.0V_MPHYGT +1.0V_PRIM_CORE +3.3V_ALW_DSW	+3VALW_PCH +1.0V_VCCST	+1.35V_MEM +1.0V_VCCSTG +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +VCC_EDRAM +VCC_EOPIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	Pre-EVT
2	100	13.7	2.902	EVT
3	100	17.8	2.801	DVT1
4	100	22.1	2.703	DVT2
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port1
USB3.0-2	SSIC-1			N/A
USB3.0-3	SSIC-2			N/A
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		LAN/GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	SATA ODD
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	N/A

USB PORT#	DESTINATION
1	USB3.0 Port1
2	IO/DB
3	IO/DB
4	N/A
5	CCD
6	Card Reader
7	Touch Screen
8	BT
9	N/A
10	N/A

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Title: Port assignment

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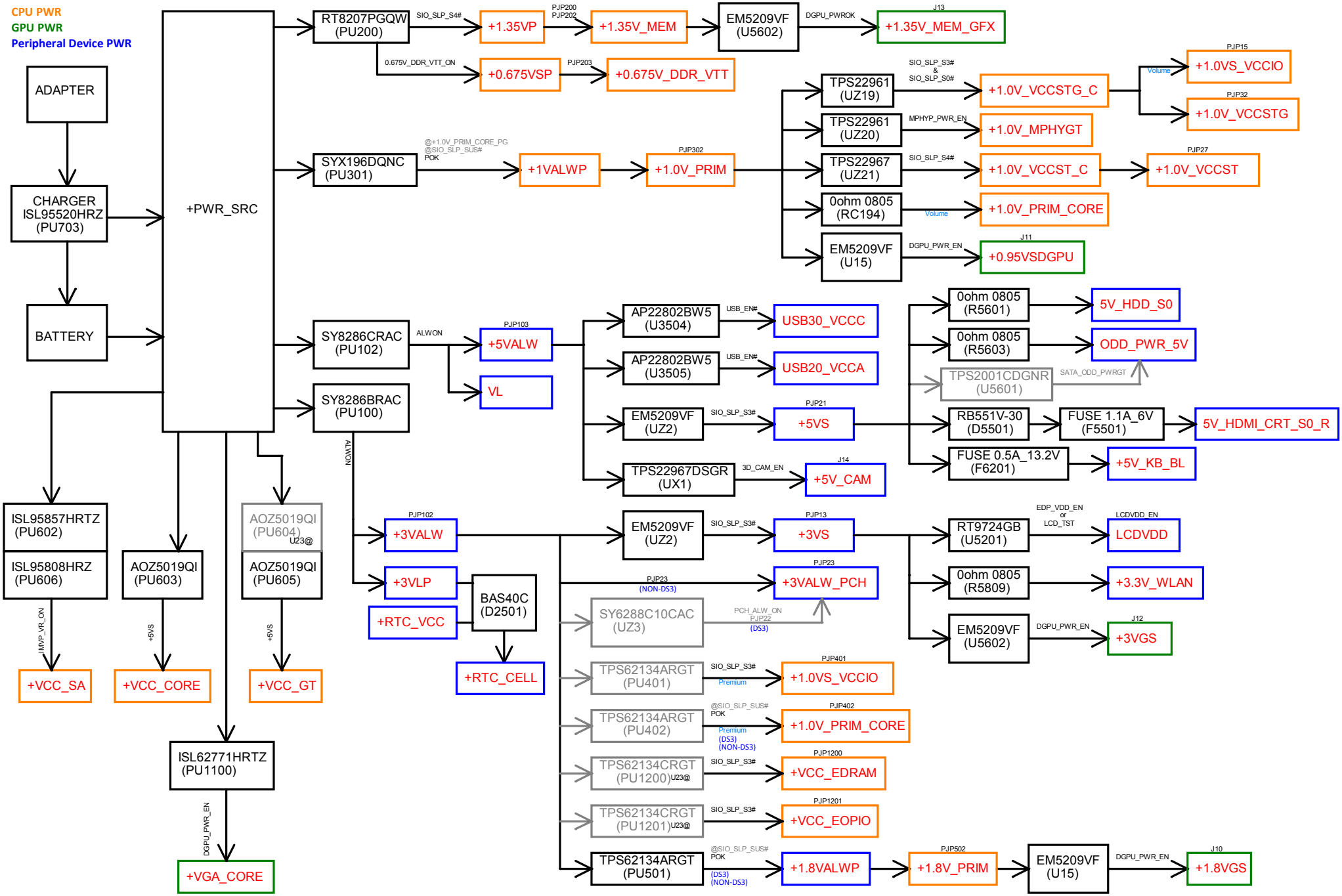

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Title: Power rails

Size | Document Number: LA-D071P | Rev: 1.0(A00)

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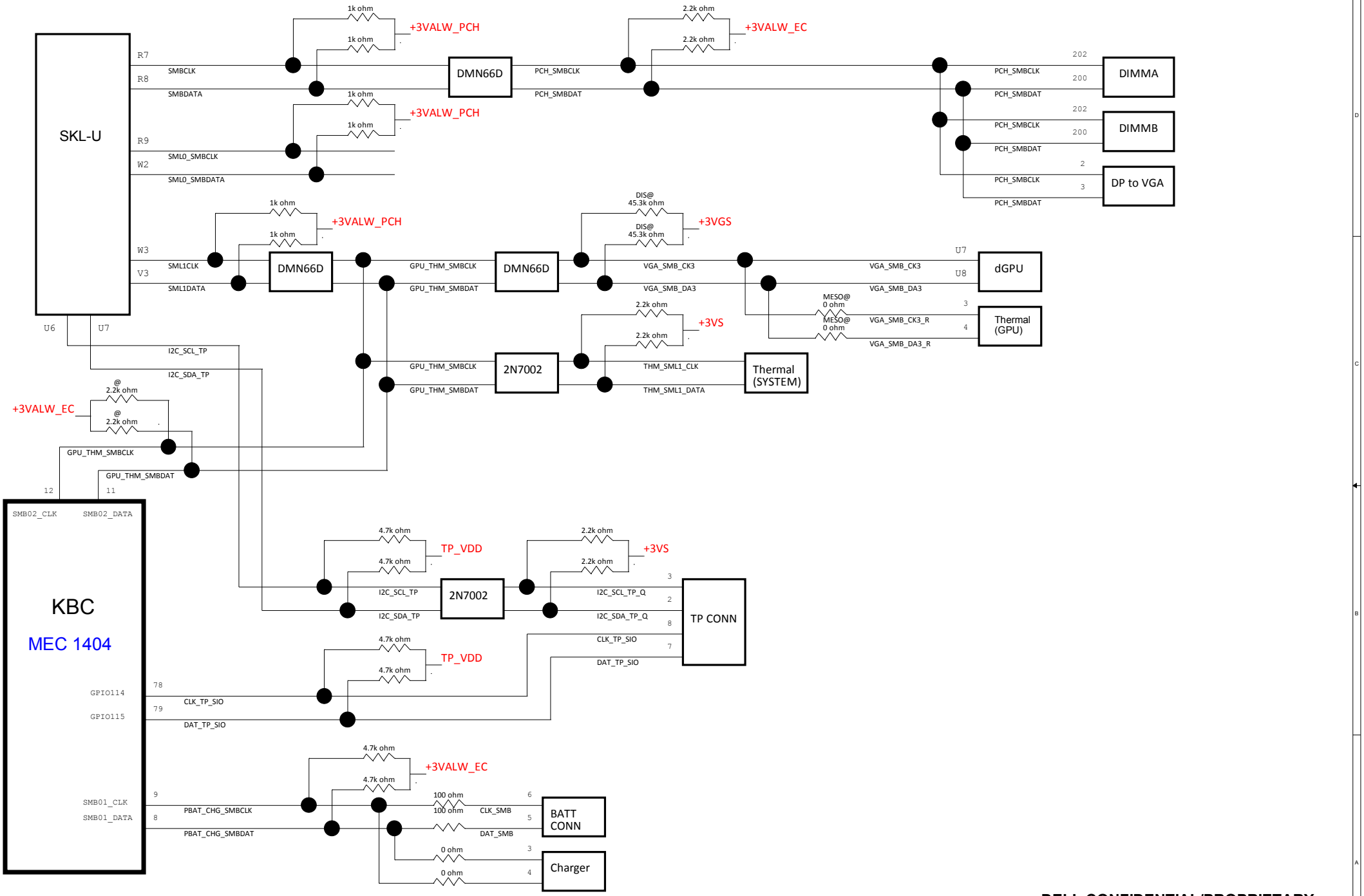

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Title: SMbus Block diagram

Size | Document Number: LA-D071P | Rev: 1.0(A00)

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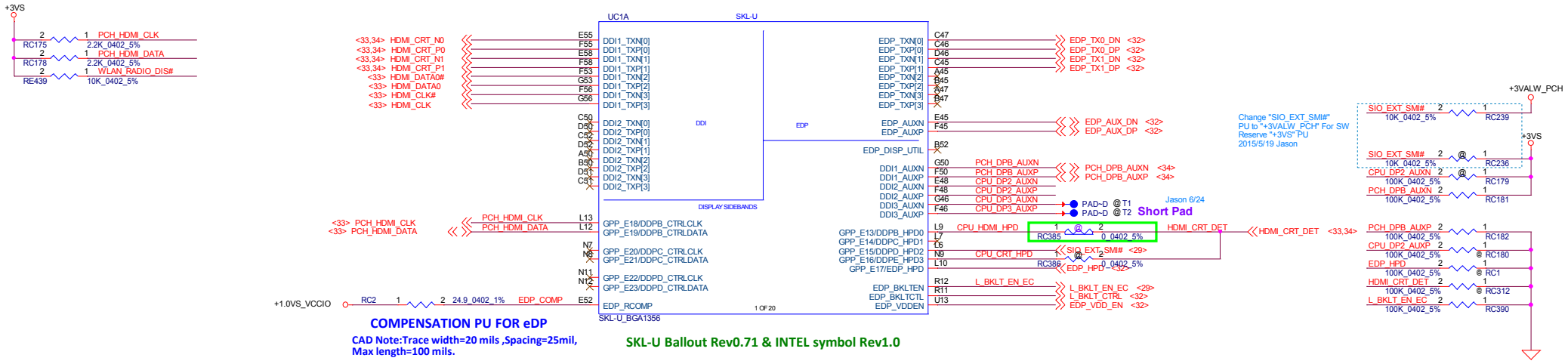

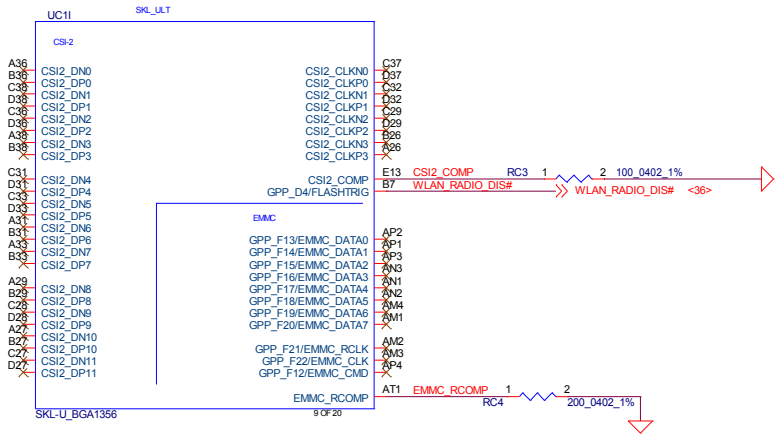

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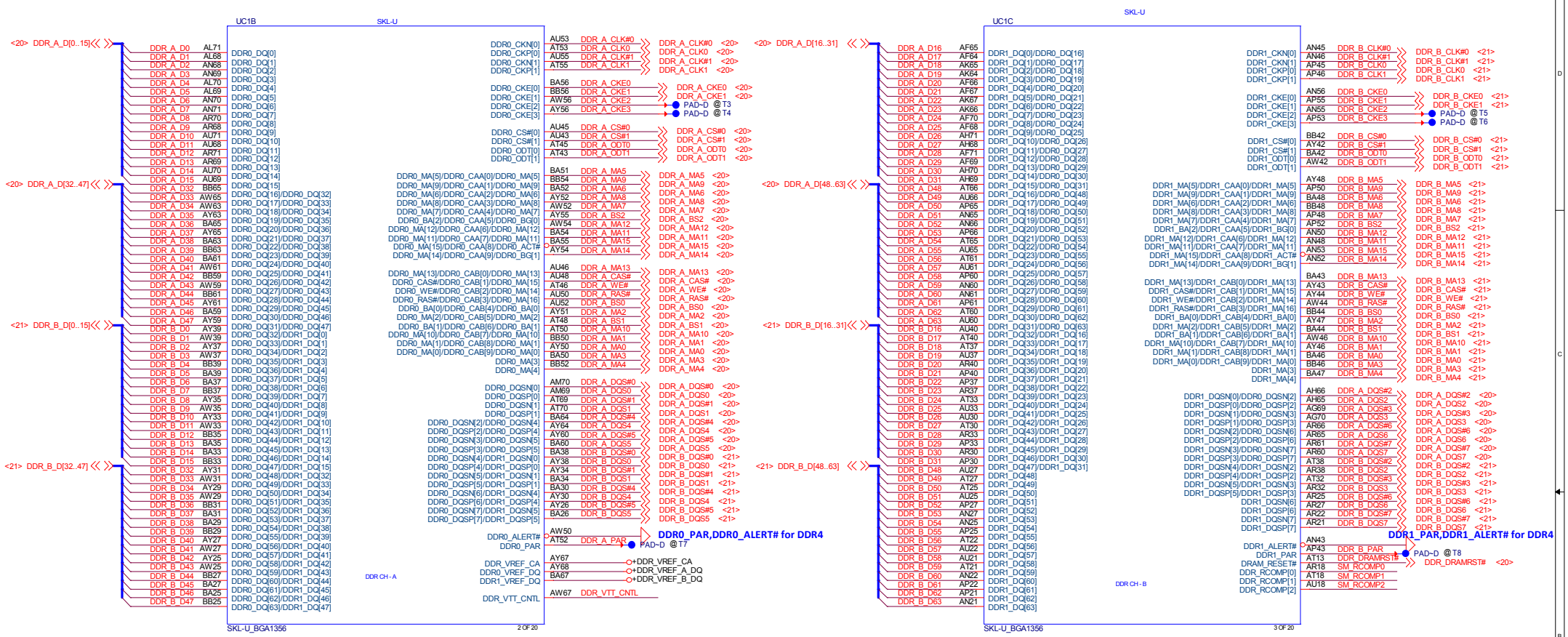
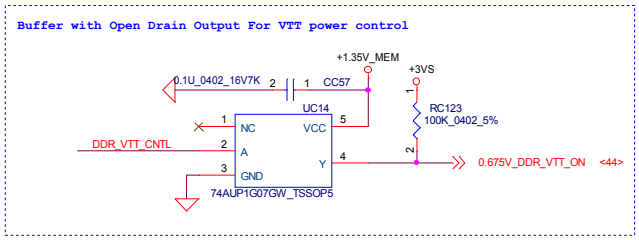
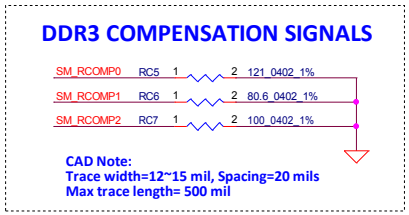
DDR3L, Ballout for side by side(Non-Interleave)







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Title: CPU (2/14)

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E SKL-U

SPI - FLASH
PCH_SPI_CLK_R1 AV2 SPI0_CLK
PCH_SPI_D1_R1 AW3 SPI0_MISO
PCH_SPI_D0_R1 AV3 SPI0_MOSI
PCH_SPI_D2_R1 AW2 SPI0_IO2
PCH_SPI_D3_R1 AU4 SPI0_IO3
PCH_SPI_CS#0_R1 AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#

SPI - TOUCH
ONE_DIMM# M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V4 GPP_D21/SPI1_IO2
M1 GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

C-LINK
G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

SMBUS, SMLINK
GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 PCH_SMB_ALERT#
GPP_C3/SML0CLK R9 SML0_SMBCLK
GPP_C4/SML0DATA W2 SML0_SMBDATA
GPP_C5/SML0ALERT# W1 GPP_C5
GPP_C6/SML1CLK W3 SML1CLK
GPP_C7/SML1DATA V3 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23

LPC
GPP_A1/LAD0/ESPI_IO0 AY13 LPC_LAD0 <29>
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_LAD1 <29>
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_LAD2 <29>
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_LAD3 <29>
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_LFRAME# <29>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT#/LPCPD#

GPP_A0/RCIN# AW13 <29> SIO_RCIN#
GPP_A6/SERIRQ AY11 <29> SERIRQ
GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 PCI_CLK_LPC0 EMI@ RC16 22_0402_5% CLK_DP2VGA <34>
GPP_A10/CLKOUT_LPC1 AY9 PCI_CLK_LPC1 EMI@ RC18 22_0402_5% CLK_PCI_LPC_MEC <29>
GPP_A8/CLKRUN# AW11 CLKRUN# EMI@ RC22 22_0402_5% CLK_PCI_LPDEBUG <29>
CLKRUN# <29>

SKL-U_BGA1356 5 OF 20

+3VS
QC2A DMN66D0LDW-7_SOT363-6
SMBCLK PCH_SMBCLK <20,21,34>
QC2B DMN66D0LDW-7_SOT363-6
SMBDATA PCH_SMBDAT <20,21,34>

+3VALW_PCH
QC5A DSX@ DMN66D0LDW-7_SOT363-6
SML1CLK GPU_THM_SMBCLK <29,38,57>
QC5B DSX@ DMN66D0LDW-7_SOT363-6
SML1DATA GPU_THM_SMBDAT <29,38,57>

N_DSX@
SML1CLK RC0801 N_DSX@ 0_0402_5% GPU_THM_SMBCLK
SML1DATA RC0802 N_DSX@ 0_0402_5% GPU_THM_SMBDAT

+3VS
RC267 10K_0402_5% ONE_DIMM#
RC268 10K_0402_5%

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

+3VS
RC13 10K_0402_5%
RC21 10K_0402_1%

<14> XDP_SPI_SI RC355 CMC@ 1K_0402_1% PCH_SPI_D0_R1
<14> XDP_SPI_IO2 RC354 CMC@ 1K_0402_1% PCH_SPI_D2_R1
RC21/44 place to within 1100 mil of SPI0_MOSI/SPI0_IO2 pin for XDP

Reserve for RF
CLK_PCI_LPC_MEC 12P_0402_50V8J @EMI@ CC4
CLK_PCI_LPDEBUG 12P_0402_50V8J @EMI@ CC5

+3VS
PCH_SMBDAT 2.2K_0402_5% RN19
PCH_SMBCLK 2.2K_0402_5% RN20

+3VALW_PCH
SMBCLK RC12 1K_0402_5%
SMBDATA RC14 1K_0402_5%
SML1CLK RC15 1K_0402_5%
SML1DATA RC17 1K_0402_5%
SML0_SMBCLK RC19 1K_0402_5%
SML0_SMBDATA RC20 1K_0402_5%
SUS_STAT#/LPCPD# @RC369 8.2K_0402_5%

+3VS
CLKRUN# RC27 8.2K_0402_5%

PCH_SPI_CLK_0_R
RC29 33_0402_5% @EMI@
CC8 33P_0402_50V8J @EMI@

+3.3V_SPI
RC339 4.7K_0402_5% PCH_SPI_CS#0_R1
RC30 1K_0402_5% PCH_SPI_D2_R1
RC31 @ 1K_0402_5% PCH_SPI_D3_R1
RC316 1K_0402_5% PCH_SPI_D3_R1

PCH_SPI_D1_R1 RC317 33_0402_5% PCH_SPI_D1_0_R <29>
PCH_SPI_D0_R1 RC318 33_0402_5% PCH_SPI_D0_0_R <29>
PCH_SPI_CLK_R1 RC319 33_0402_5% PCH_SPI_CLK_0_R <29>
PCH_SPI_D3_R1 RC320 33_0402_5% PCH_SPI_D3_0_R
PCH_SPI_D2_R1 RC327 33_0402_5% PCH_SPI_D2_0_R

+3VALW_PCH
PCH_SMB_ALERT# RC23 @ 8.2K_0402_5%

TLS CONFIDENTIALITY
HIGH ENABLE
LOW(DEFAULT) DISABLE

+3VALW_PCH
GPP_C5 RC25 @ 10K_0402_5%

EC interface
HIGH ESPI
LOW(DEFAULT) LPC

+3VALW_PCH
Modify Value to 150k for WW52 MOW
2015/03/03 Jason
GPP_B23 RC365 CMC@ 150K_0402_5%

EXI BOOT STALL BYPASS
HIGH ENABLE
LOW(DEFAULT) DISABLE

9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

Short Pad

128Mb Flash ROM
+3.3V_SPI
CC9 0.1U_0402_25V6

<29> PCH_SPI_CS#0_R1
PCH_SPI_CS#0_R1 RC37 @ 0_0402_5% PCH_SPI_CS#0_R2
PCH_SPI_D1_0_R RC329 15_0402_1% PCH_SPI_D1_0_R3
PCH_SPI_D2_0_R RC330 15_0402_1% PCH_SPI_D2_0_R3

UC5 W25Q128FVSIQ_SO8
/CS VCC
IO1 IO3
IO2 CLK
GND IO0
PCH_SPI_D3_0_R3 RC331 15_0402_1% PCH_SPI_D3_0_R
PCH_SPI_CLK_0_R3 RC332 15_0402_1% PCH_SPI_CLK_0_R
PCH_SPI_D0_0_R3 RC333 15_0402_1% PCH_SPI_D0_0_R

Main:
SA00005VV10, S IC FL 128M W25Q128FVSIQ SOIC8P SPI ROM
2nd:
SA00008KK00, S IC FL 128M GD25B128CSIGR SOP 8P 3.3V
SA00006PD00, S IC FL 128M EN25QH128A-104HIP SOP 8P
Jason 2015/03/04

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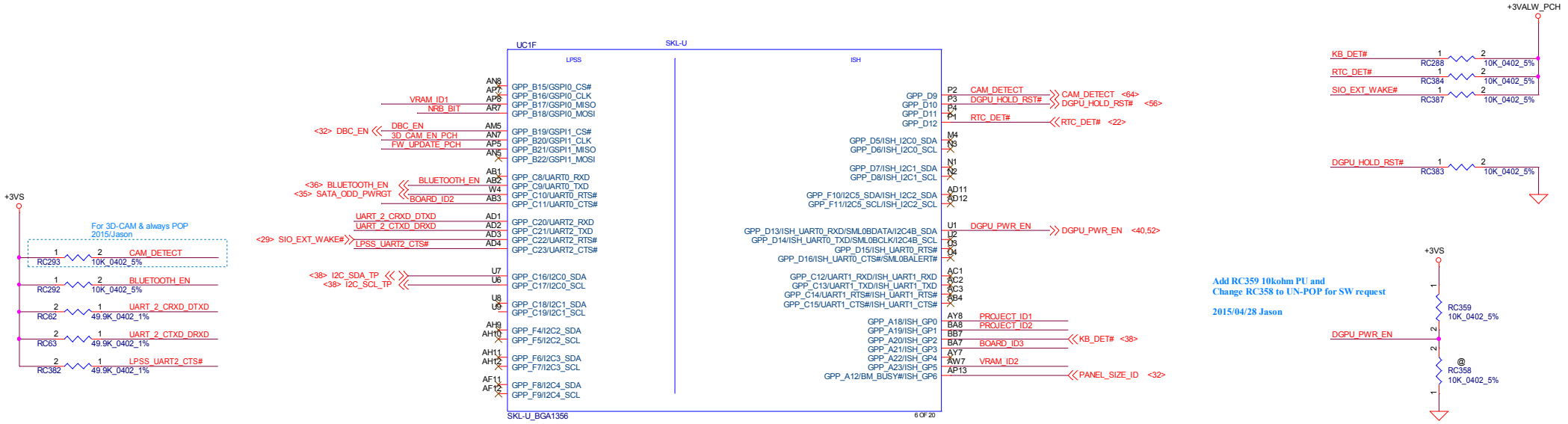
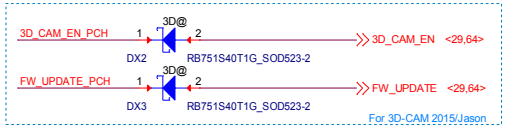
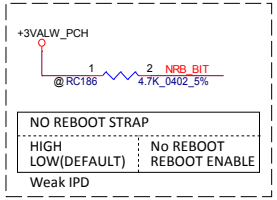
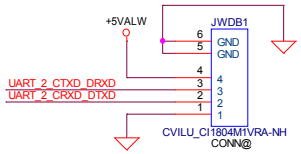


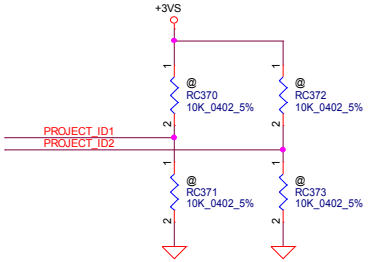




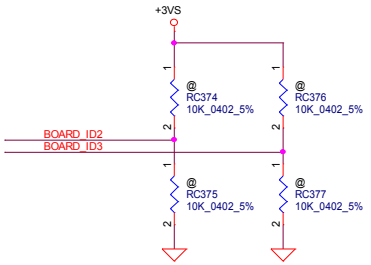
Win7 Debug solution

Option 2 : For Open Chassis Platforms

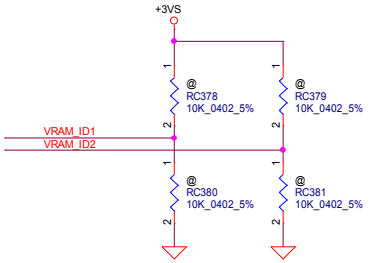




Reserve for TULIP/VanGogh MB switch



Reserve for MB Platform(SKL) switch



Reserve for VRAM Type switch

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Title: CPU (4/14)

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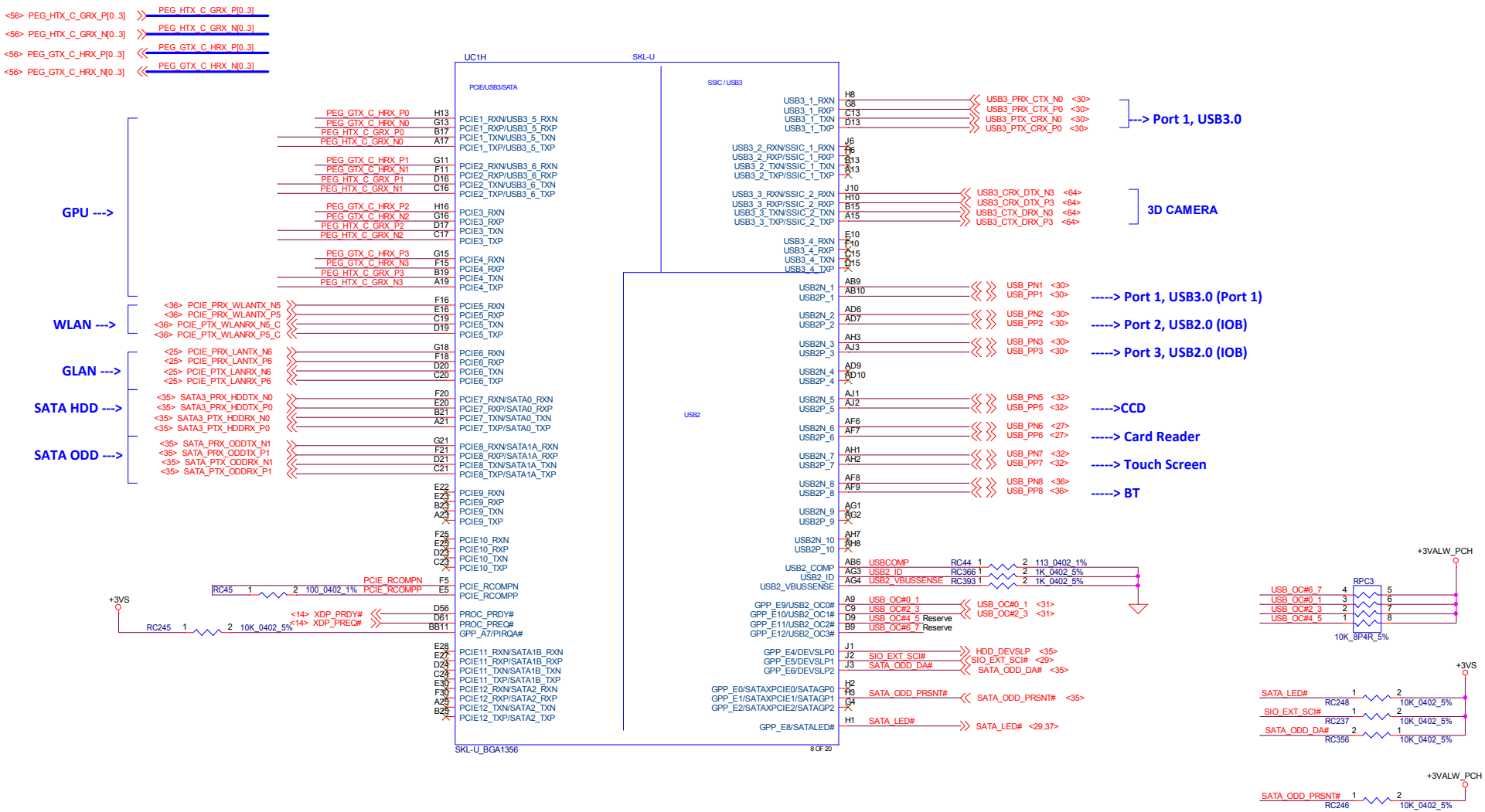

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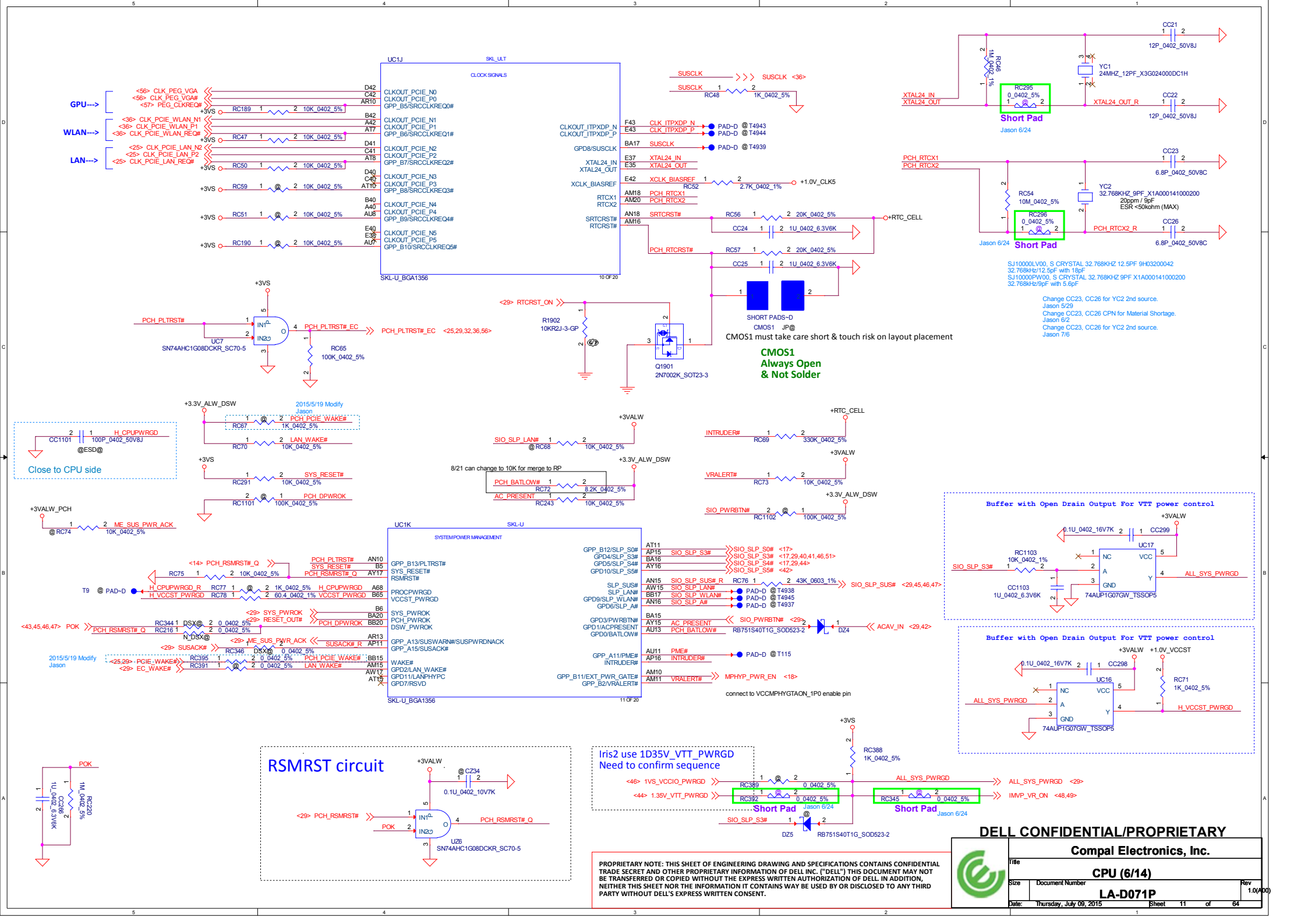
UC1J
SKL_ULT
CLOCK SIGNALS
GPU--->
WLAN--->
LAN--->
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
RTCX1
RTCX2
SRTCRST#
RTCRST#
SKL-U_BGA1356
10 OF 20
SUSCLK
XTAL24_IN
XTAL24_OUT
PCH_RTCX1
PCH_RTCX2
PCH_RTCRST
SRTCRST#
XCLK_BIASREF
+1.0V_CLK5
+RTC_CELL
SHORT PADS~D
CMOS1 JP@
CMOS1 must take care short & touch risk on layout placement
CMOS1
Always Open
& Not Solder
Q1901
2N7002K_SOT23-3
UC7
SN74AHC1G08DCKR_SC70-5
PCH_PLTRST#
PCH_PLTRST#_EC
RC65
100K_0402_5%
Close to CPU side
CC1101
100P_0402_50V8J
@ESD@
H_CPUPWRGD
+3.3V_ALW_DSW
2015/5/19 Modify
Jason
PCH_PCIE_WAKE#
LAN_WAKE#
SYS_RESET#
PCH_DPWROK
+3VALW_PCH
ME_SUS_PWR_ACK
+3VALW
SIO_SLP_LAN#
8/21 can change to 10K for merge to RP
PCH_BATLOW#
AC_PRESENT
INTRUDER#
VRALERT#
SIO_PWRBTN#
UC1K
SKL-U
SYSTEMPOWER MANAGEMENT
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD1/LANPHYPC
GPD7/RSVD
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
SKL-U_BGA1356
11 OF 20
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SIO_SLP_SUS#
SIO_SLP_LAN#
SIO_SLP_WLAN#
SIO_SLP_A#
SIO_PWRBTN#
AC_PRESENT
PCH_BATLOW#
PME#
INTRUDER#
VRALERT#
MPHYP_PWR_EN
connect to VCCMPHYGTAON_1P0 enable pin
ACAV_IN
DZ4
RB751S40T1G_SOD523-2
PAD~D @T4938
PAD~D @T4945
PAD~D @T4937
PAD~D @T115
Buffer with Open Drain Output For VTT power control
74AUP1G07GW_TSSOP5
ALL_SYS_PWRGD
H_VCCST_PWRGD
IMVP_VR_ON
Iris2 use 1D35V_VTT_PWRGD
Need to confirm sequence
1VS_VCCIO_PWRGD
1.35V_VTT_PWRGD
Short Pad
Jason 6/24
DZ5
RSMRST circuit
PCH_RSMRST#
PCH_RSMRST#_Q
POK
UZ6
SN74AHC1G08DCKR_SC70-5
0.1U_0402_10V7K
XTAL24_IN
XTAL24_OUT
XTAL24_OUT_R
YC1
24MHZ_12PF_X3G024000DC1H
PCH_RTCX2_R
YC2
32.768KHZ_9PF_X1A000141000200
20ppm / 9pF
ESR <50kohm (MAX)
SJ10000LV00, S CRYSTAL 32.768KHZ 12.5PF 9H03200042
32.768kHz/12.5pF with 18pF
SJ10000PW00, S CRYSTAL 32.768KHZ 9PF X1A000141000200
32.768kHz/9pF with 5.6pF
Change CC23, CC26 for YC2 2nd source.
Jason 5/29
Change CC23, CC26 CPN for Material Shortage.
Jason 6/2
Change CC23, CC26 for YC2 2nd source.
Jason 7/6
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Compal Electronics, Inc.
Title
CPU (6/14)
Size
Document Number
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Rev
1.0(A00)
Date: Thursday, July 09, 2015
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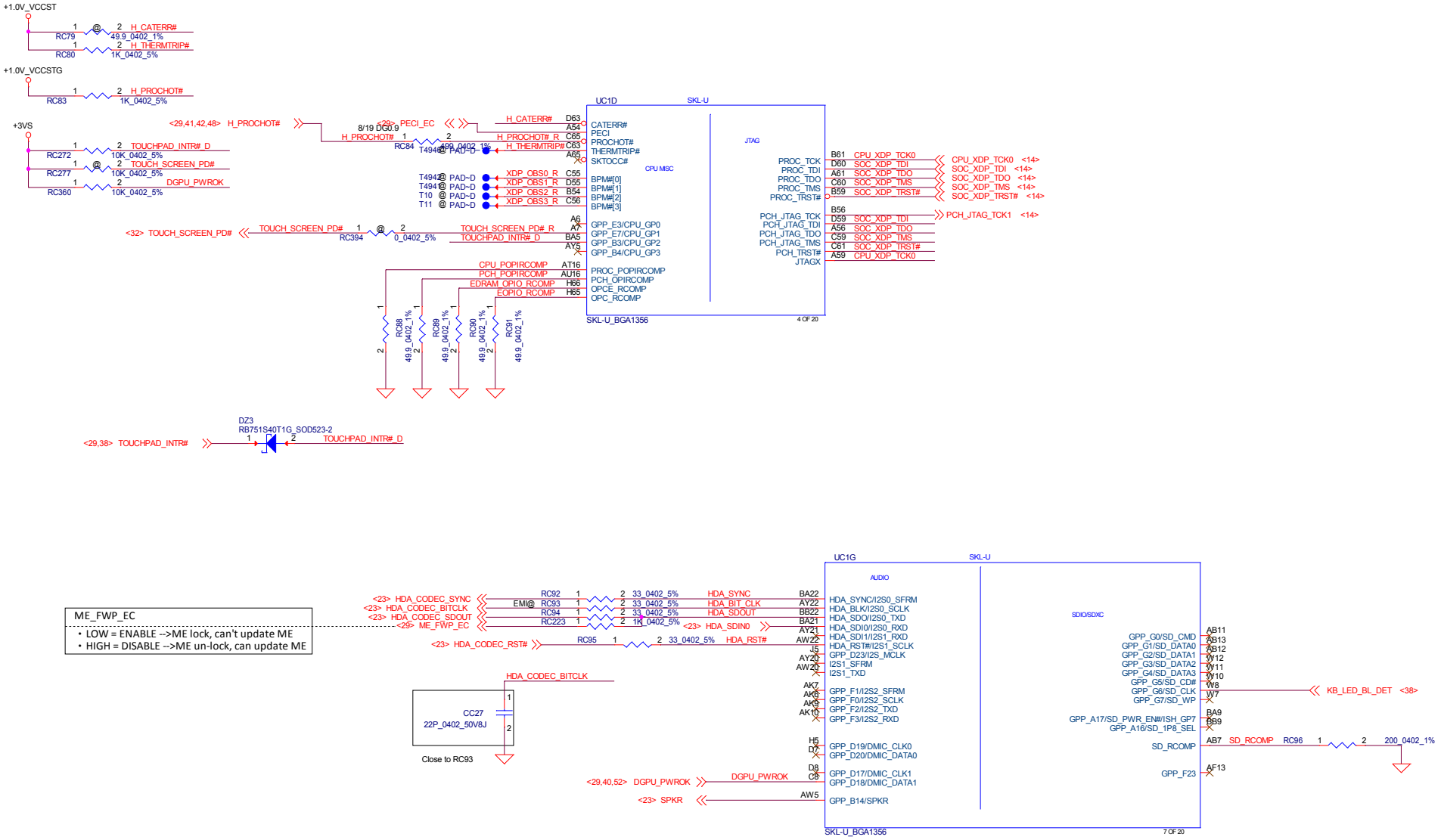

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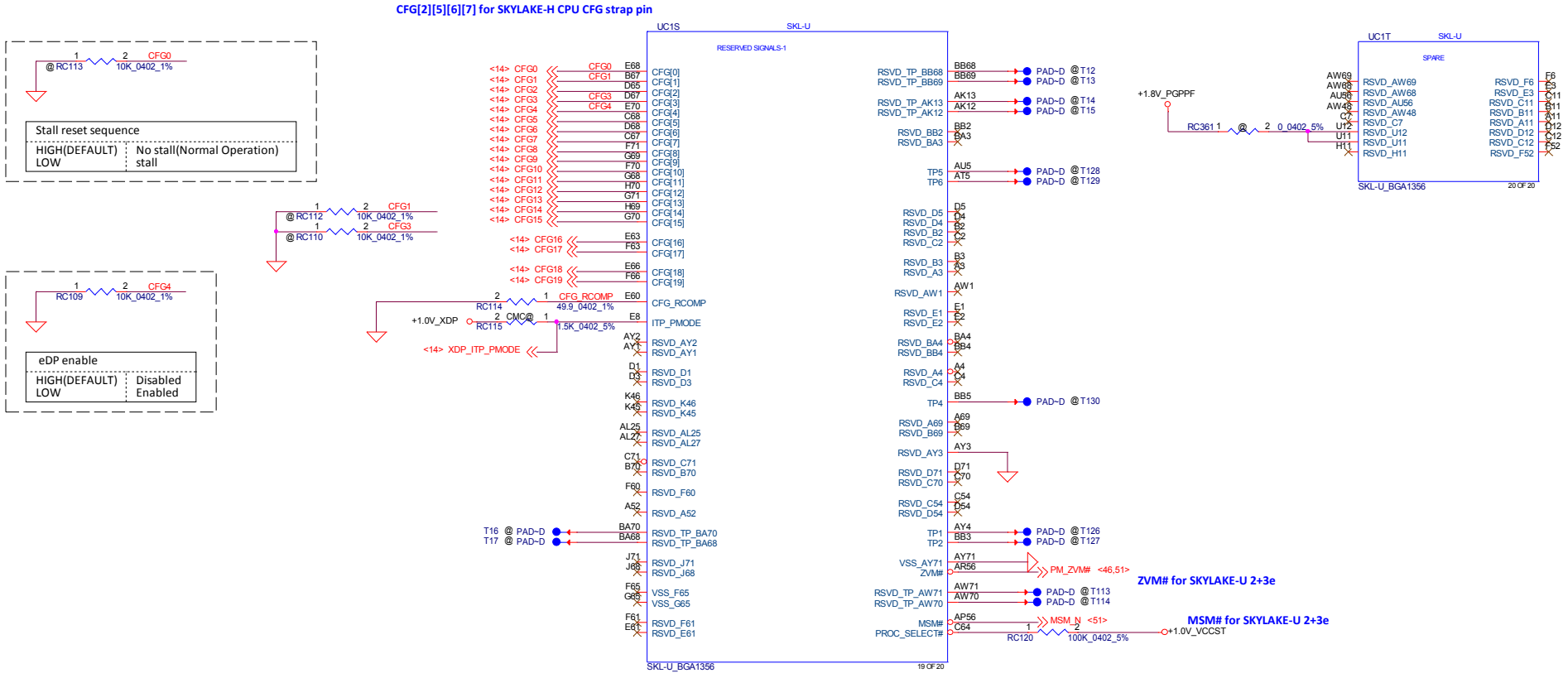
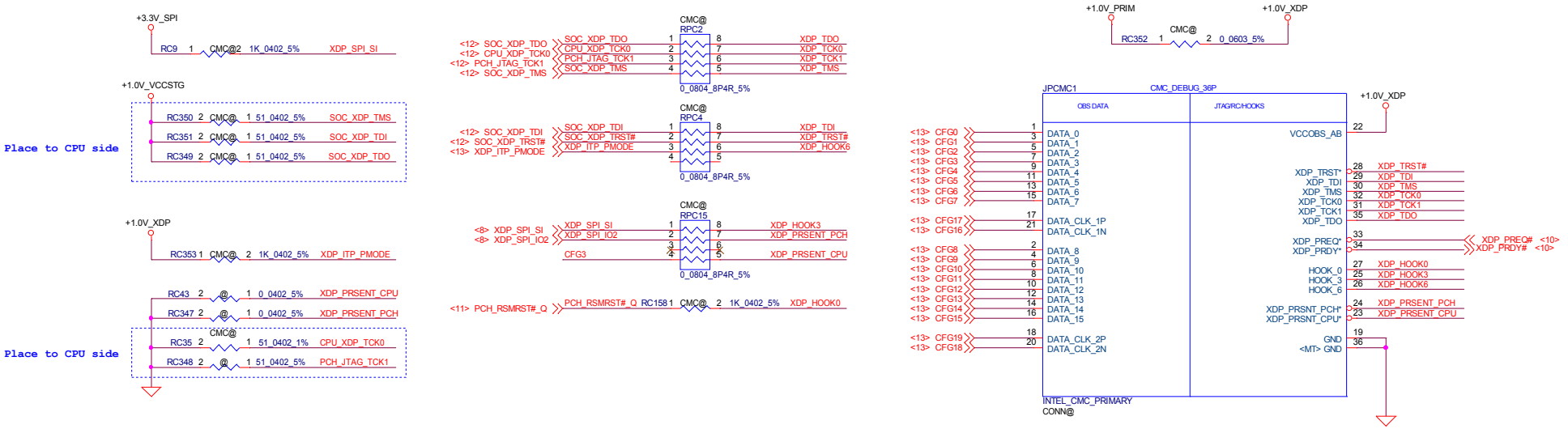
Compal Electronics, Inc.

Title	CPU (7/14)	
Size	Document Number	Rev
	LA-D071P	1.0(A00)
Date: Thursday, July 09, 2015	Sheet 12 of 64	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	CPU (8/14)
Size	Document Number: LA-D071P
Rev	1.0(A00)
Date: Thursday, July 09, 2015	Sheet 13 of 64



Compal Electronics, Inc.

Title: CPU (9/14)

Size | Document Number: LA-D071P | Rev: 1.0(A00)

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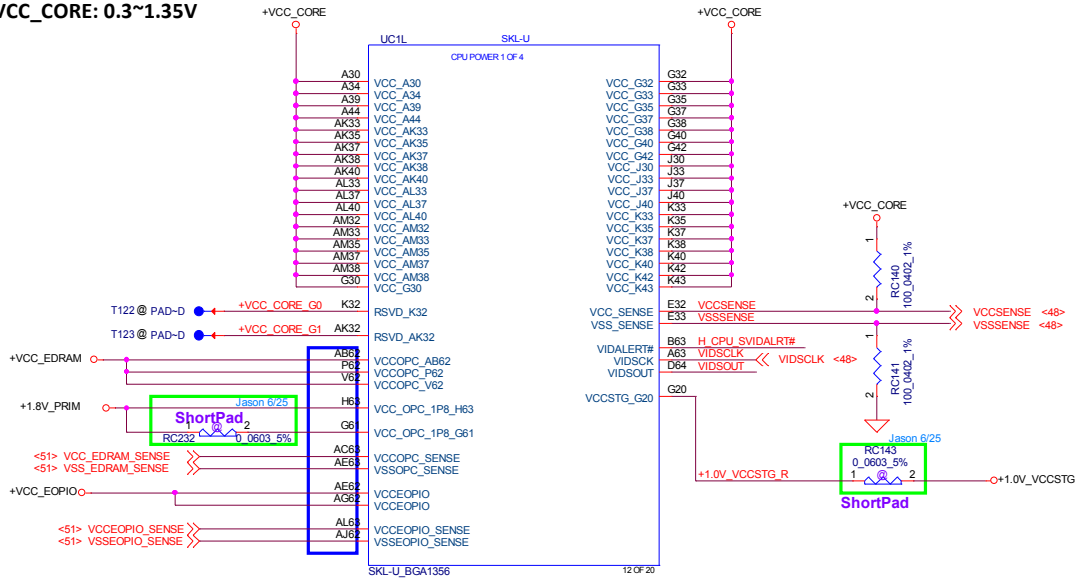
+VCC_CORE: 0.3~1.35V

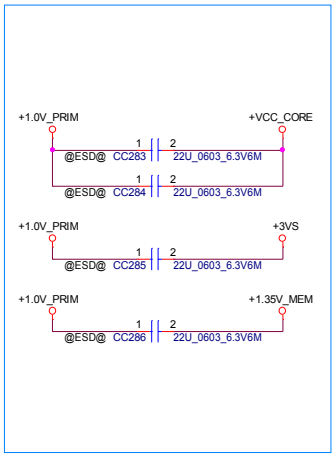


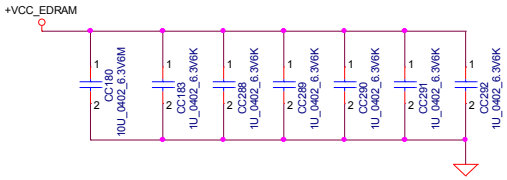
VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

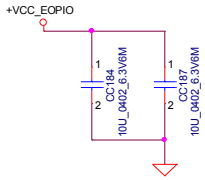
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

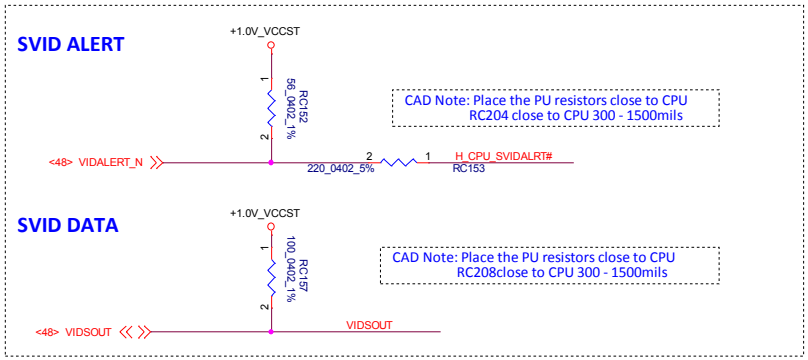
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

ESD Request









Compal Electronics, Inc.

Title: CPU (10/14)

Size | Document Number: LA-D071P | Rev: 1.0(A00)

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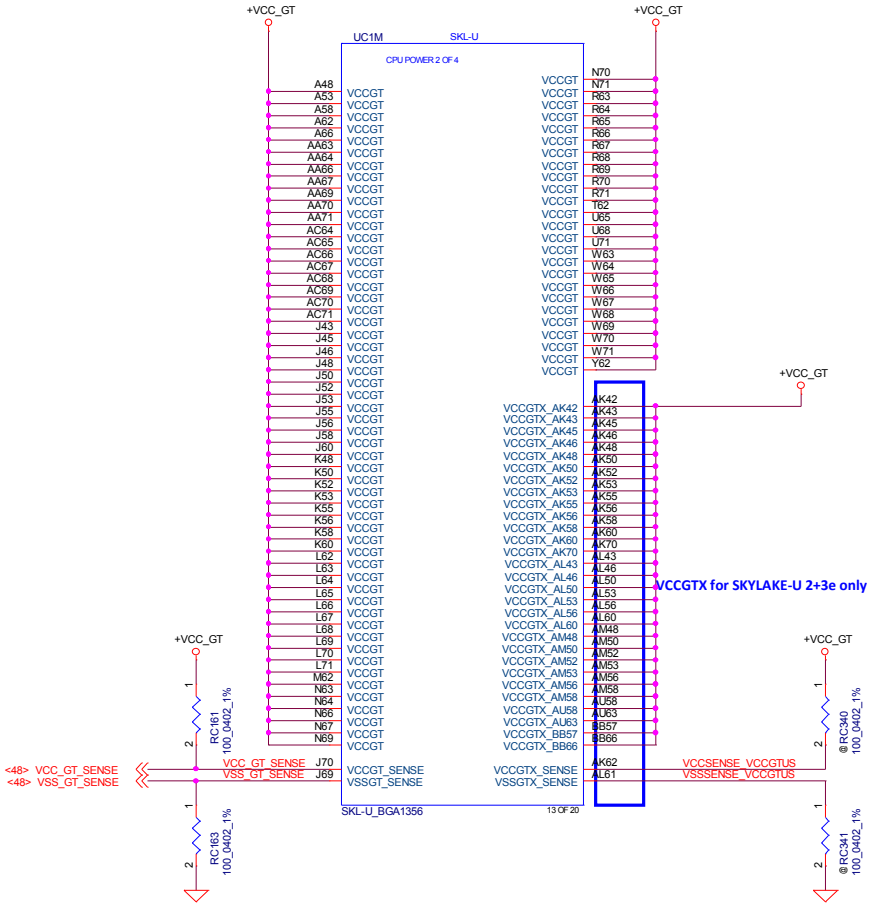
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

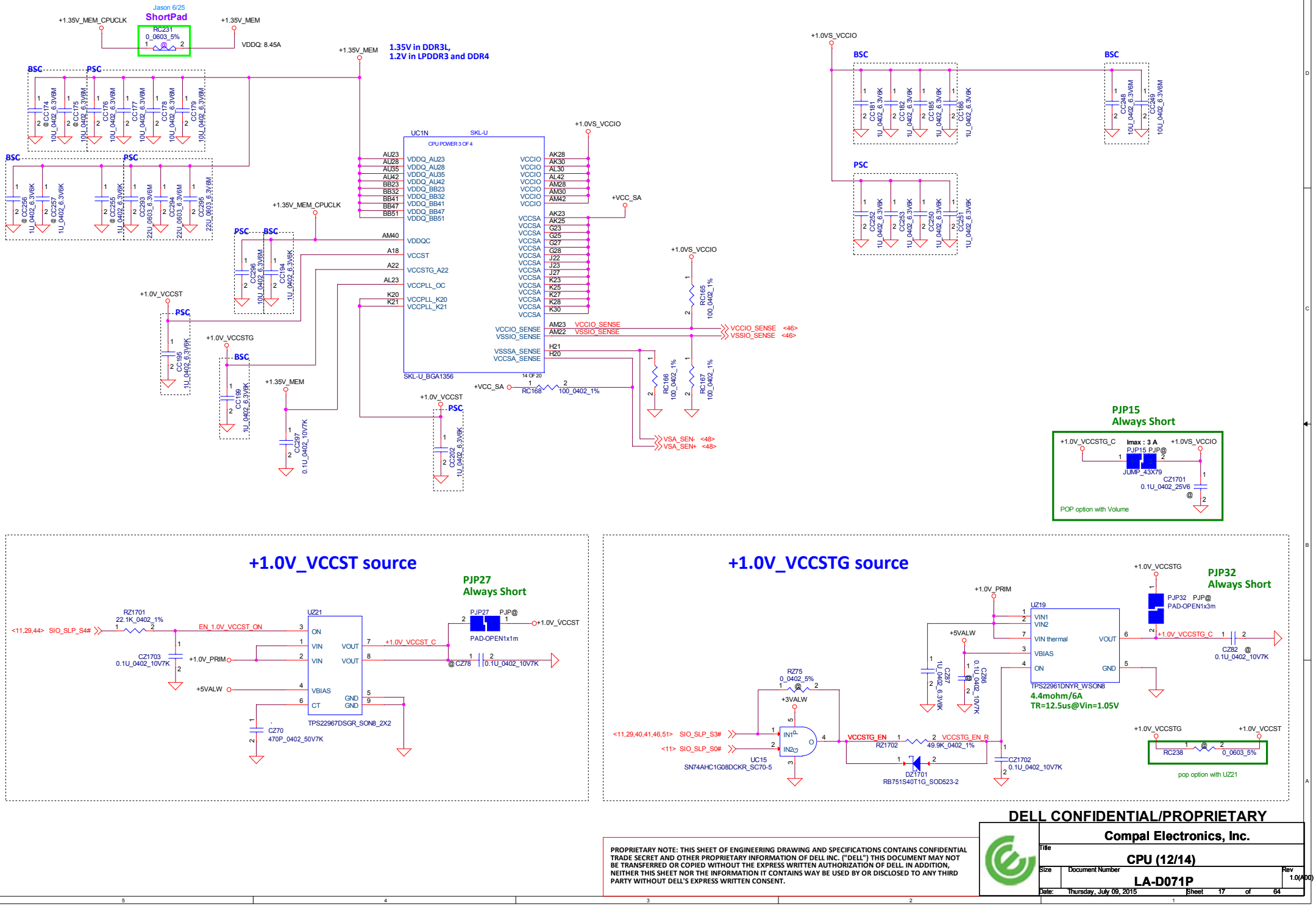


Compal Electronics, Inc.

Title: CPU (11/14)

Size | Document Number: LA-D071P | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 16 of 64



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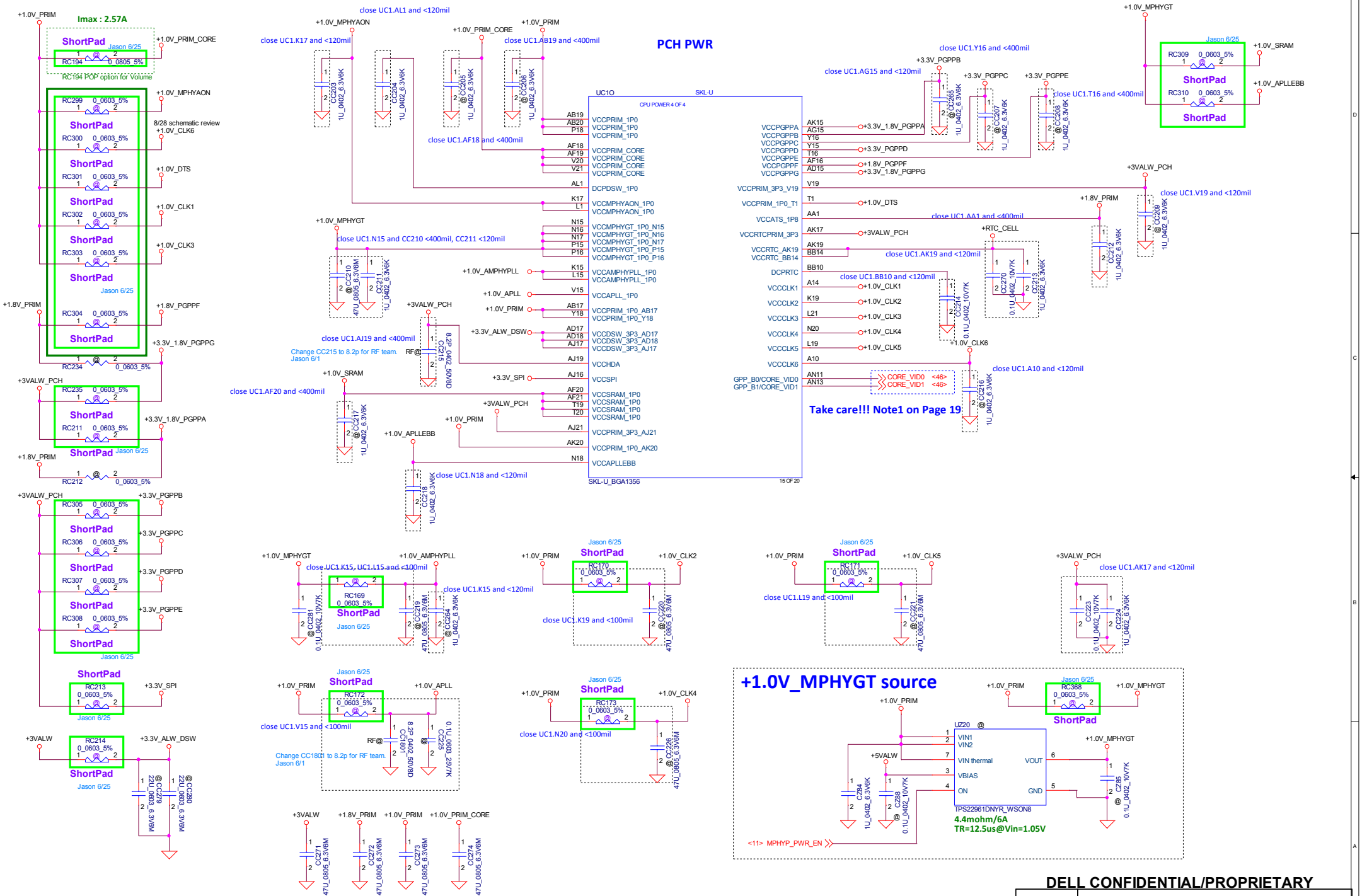
Title: CPU (12/14)

Size: | Document Number: LA-D071P | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 17 of 64



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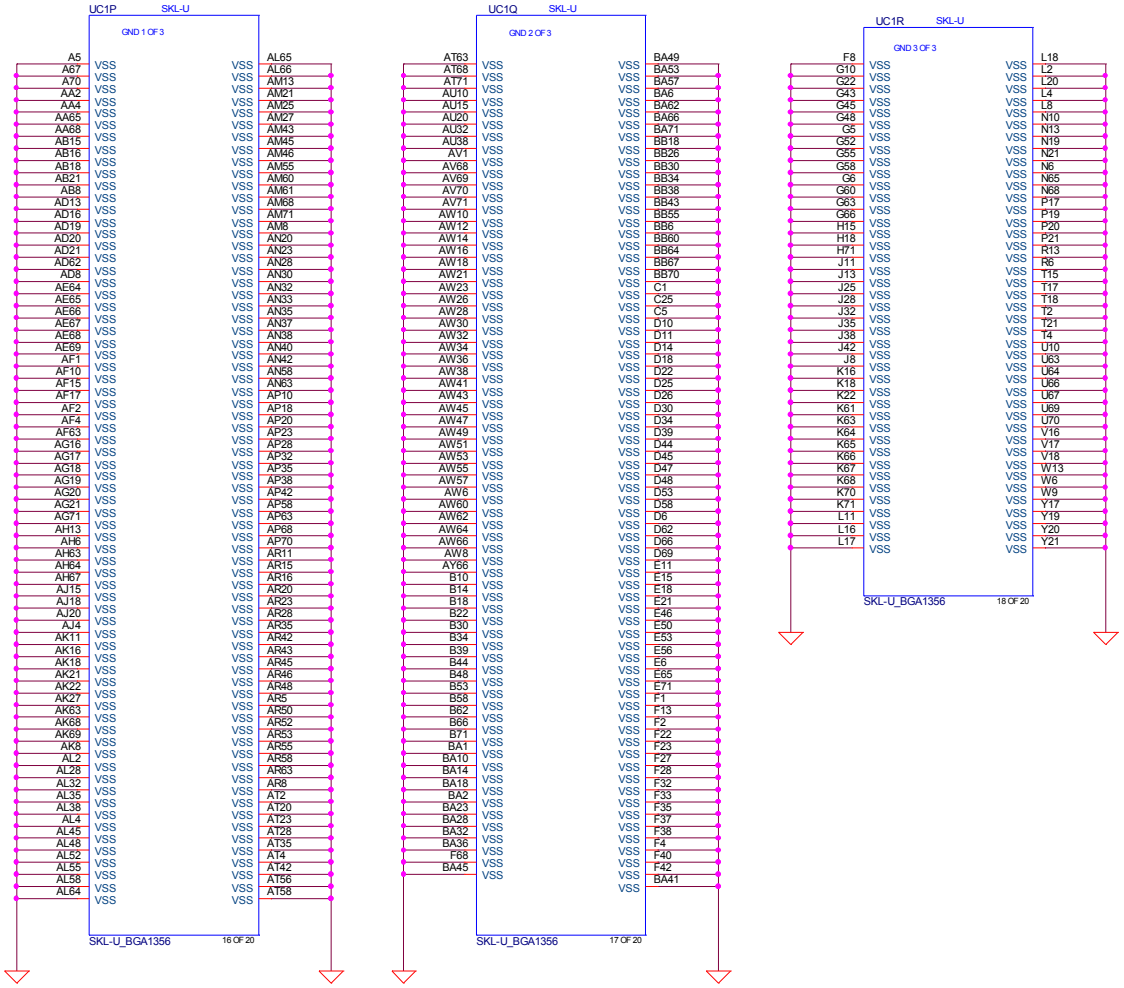
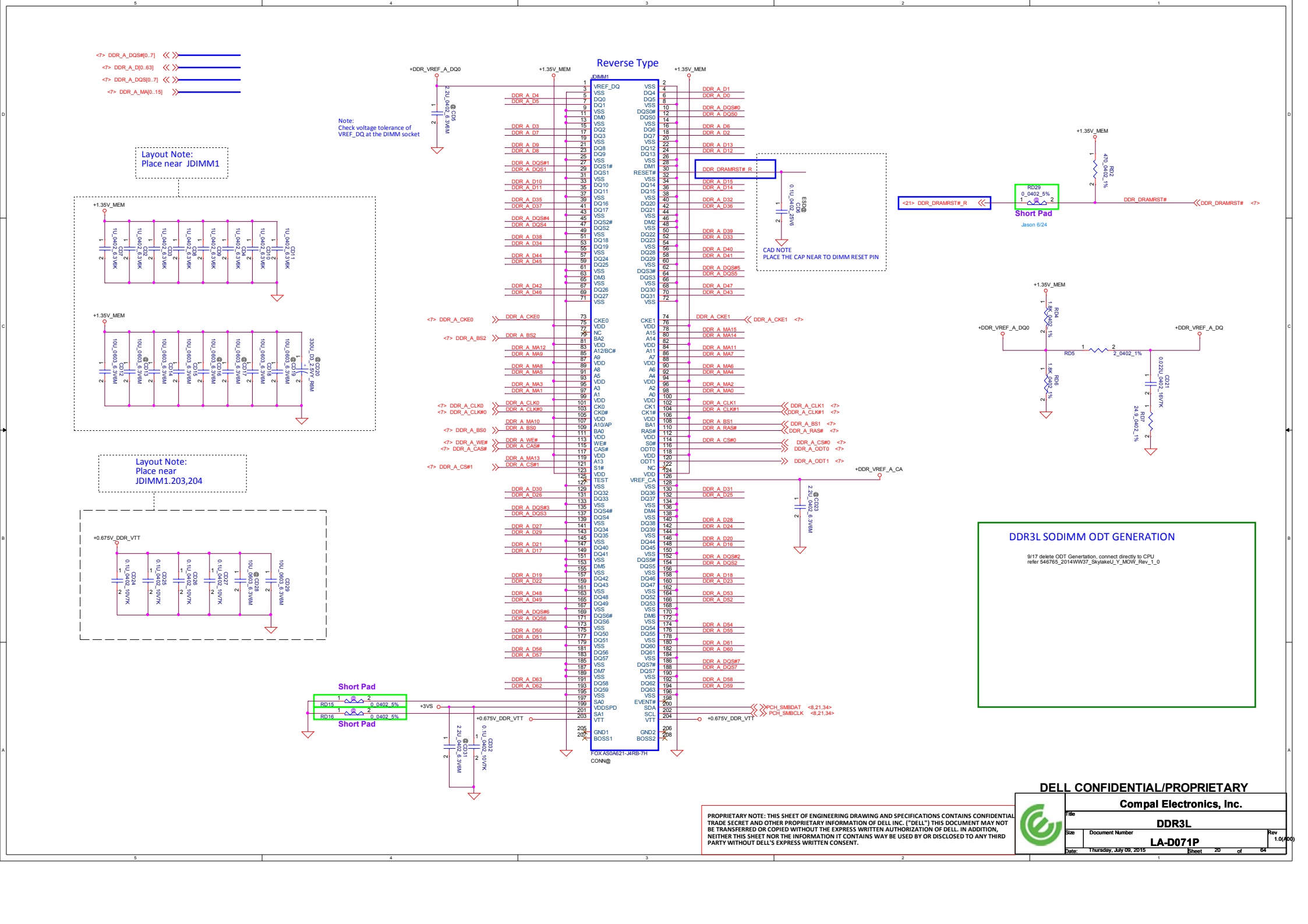
Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



Compal Electronics, Inc.		
Title: CPU (14/14)		
Size	Document Number: LA-D071P	Rev: 1.0(A00)
Date: Thursday, July 09, 2015	Sheet 19 of 64	


Reverse Type
JDIMM1
FOX AS0A621-J4RB-7H
CONN@
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket
Layout Note:
Place near JDIMM1
Layout Note:
Place near
JDIMM1.203,204
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN
Short Pad
Jason 6/24
DDR3L SODIMM ODT GENERATION
9/17 delete ODT Genertation, connect directly to CPU
refer 546765_2014WW37_SkylakeU_Y_MOW_Rev_1_0
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Compal Electronics, Inc.
DDR3L
LA-D071P
Thursday, July 09, 2015
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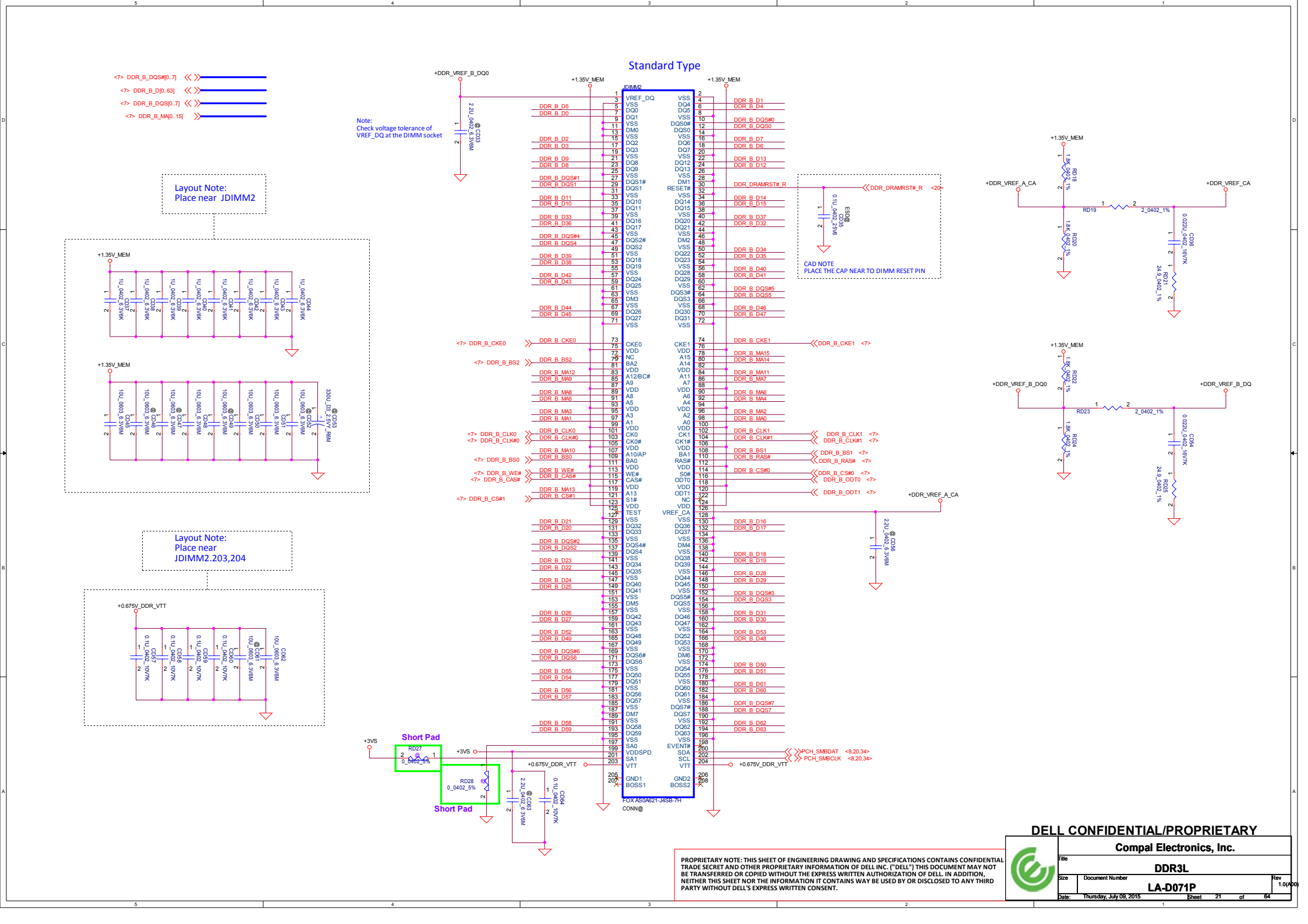

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Compal Electronics, Inc.	
Title	DDR3L
Size	Document Number: LA-D071P
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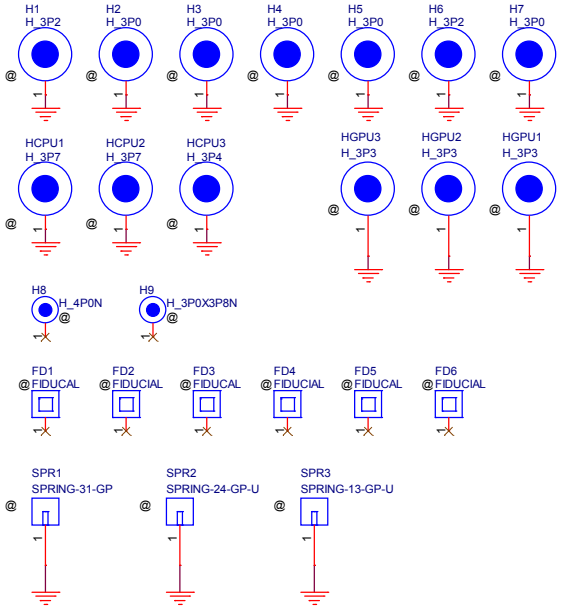
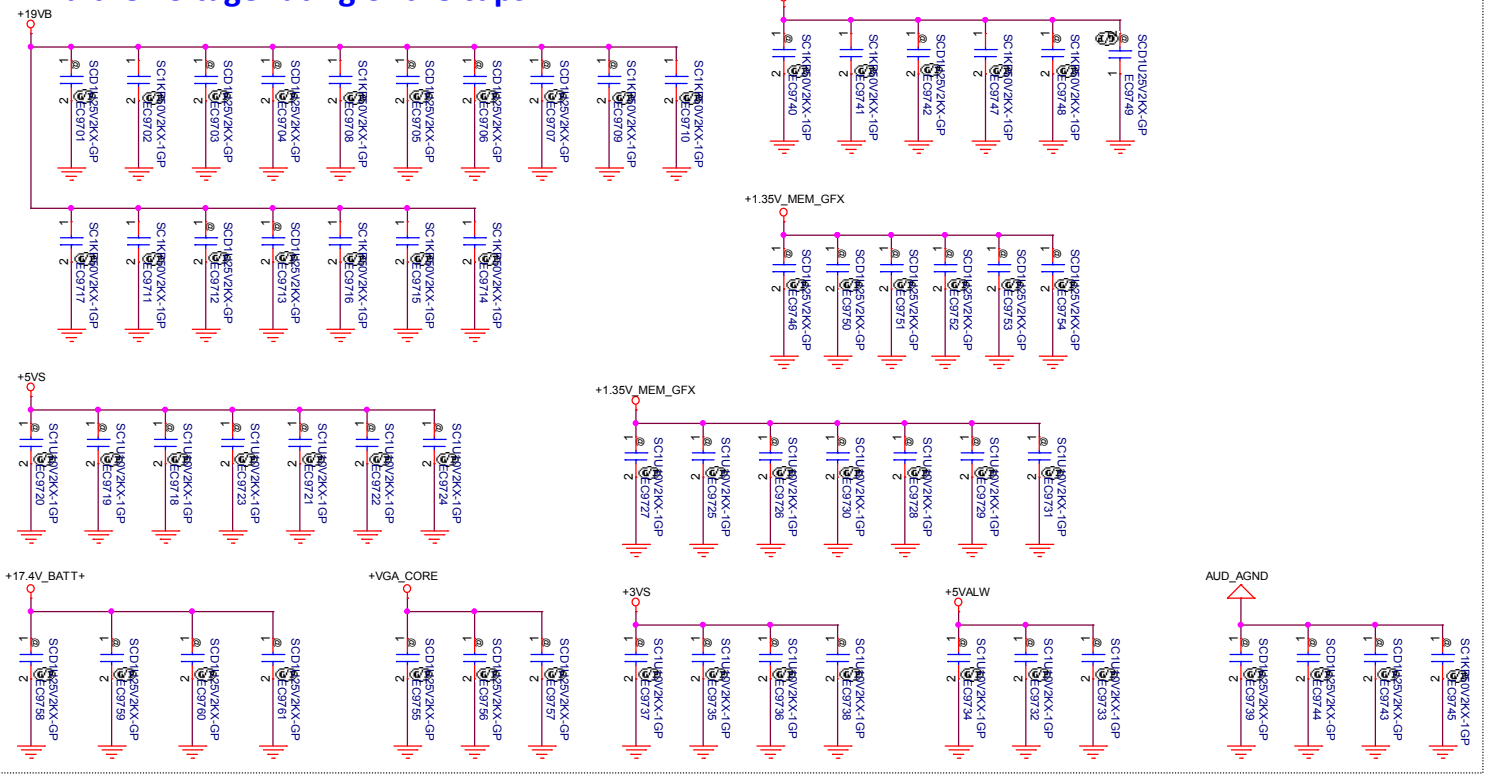
Main Func = Other

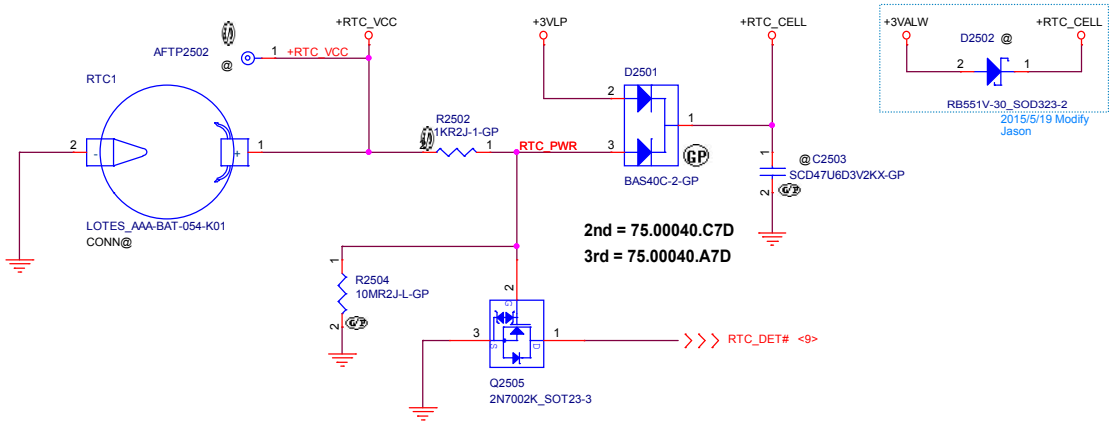
Screw hole/FD/EMI stop



Mind the voltage rating of the caps.



Main Func = RTC



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

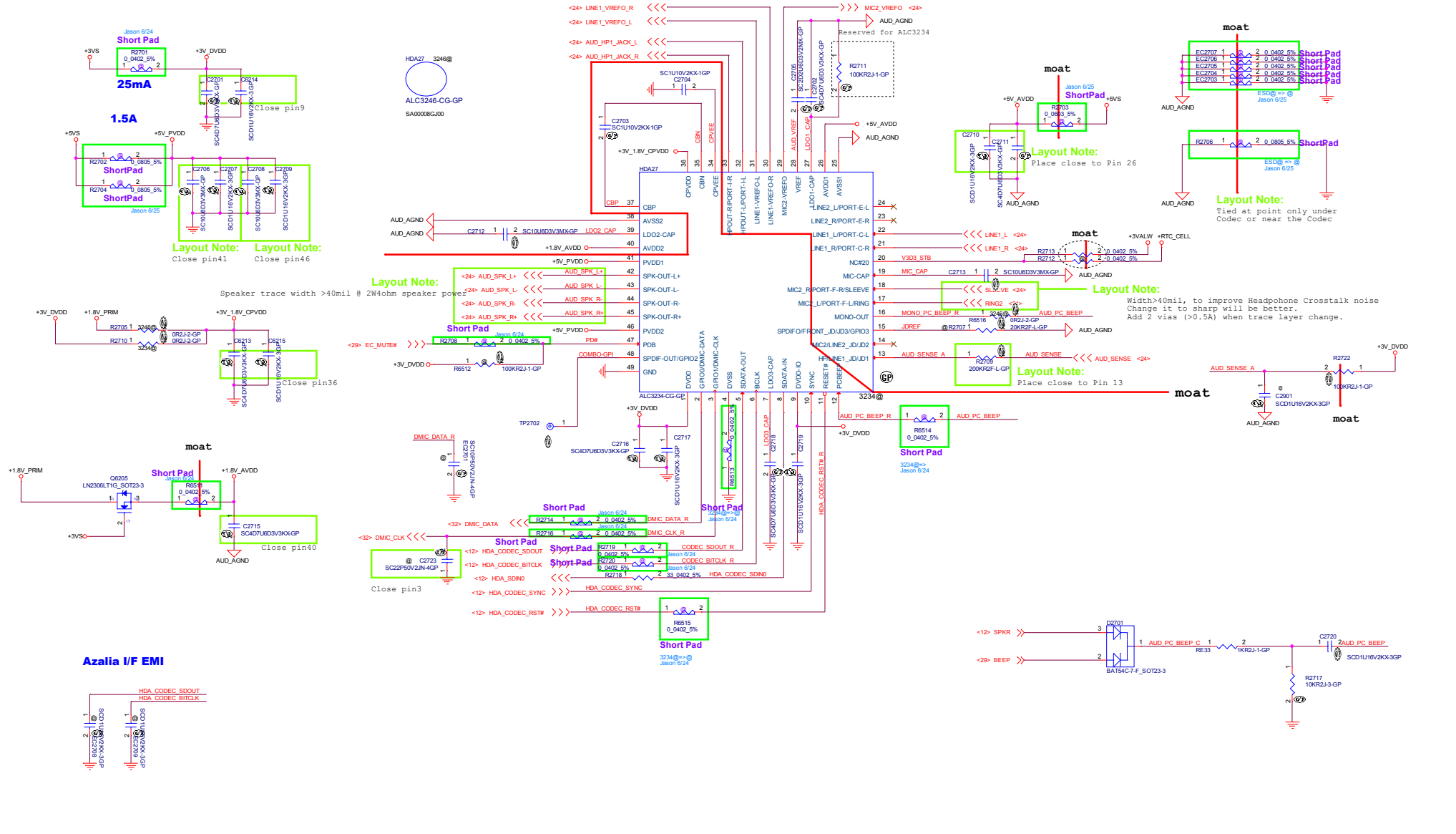
Compal Electronics, Inc.

Title: **RTC/Screw hole/EMI caps**

Size	Document Number	Rev
	LA-D071P	1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 22 of 64

Main Func = Audio



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Issued Date	2015/07/09	Deciphered Date 2016/07/31	Title: CODEC ALC3234/3246
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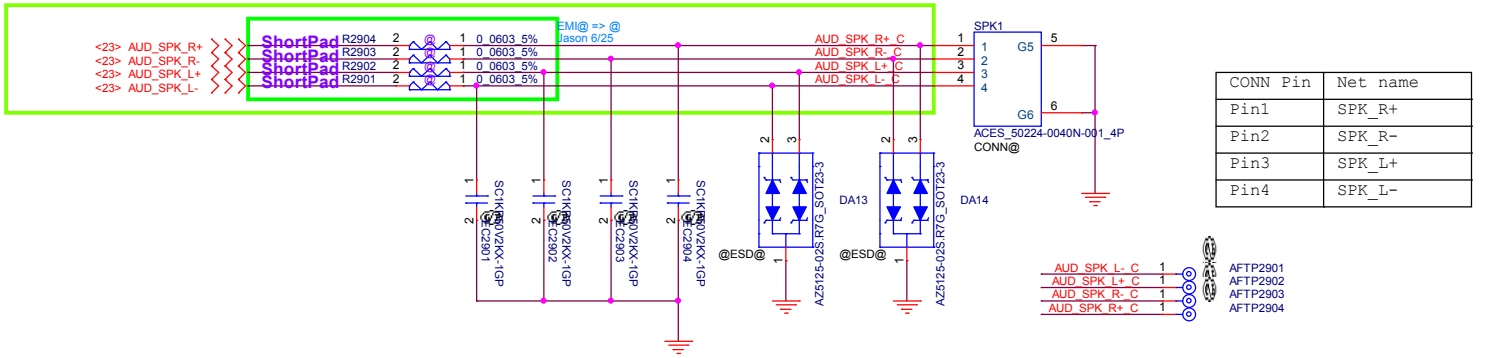
			Date: Thursday, July 09, 2015 Sheet 23 of 64

Main Func = Audio

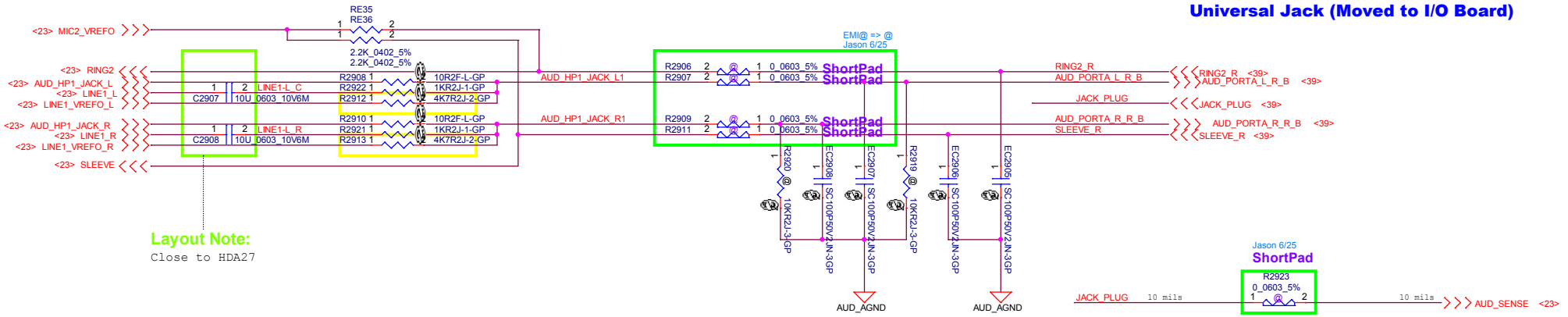
Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)



Layout Note:
Close to HDA27

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Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: SPKR/JACK

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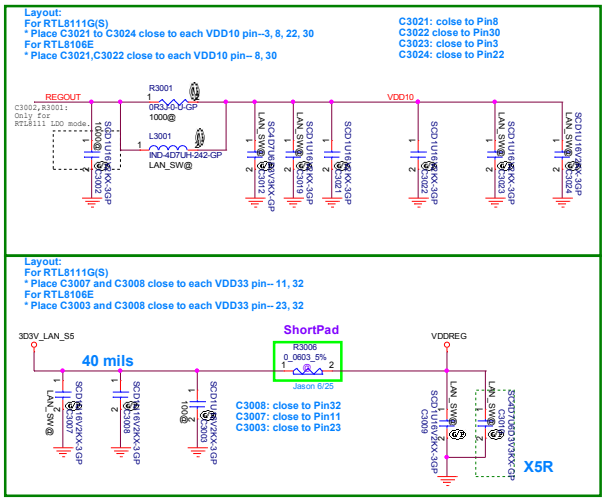
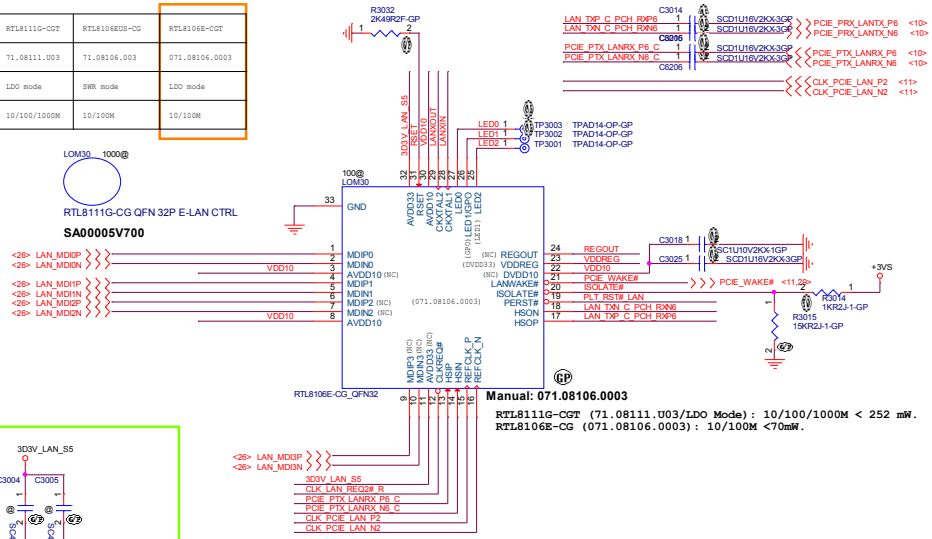
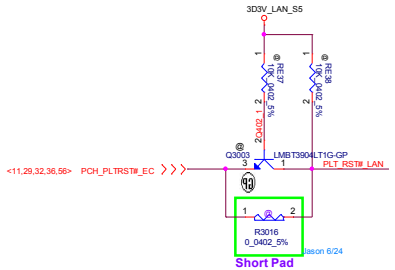
Main Func = LAN

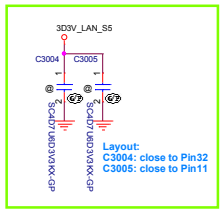
LAN CHIP (10/100/1000M & 10/100M co-lay)

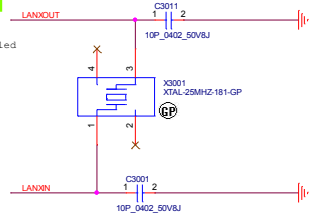


RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CGT
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

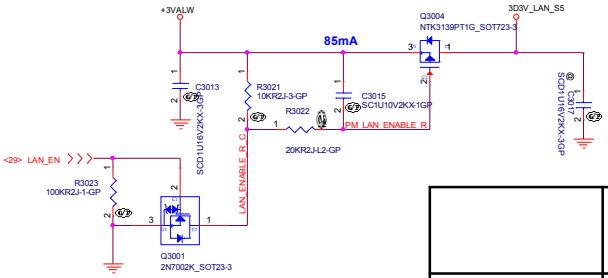


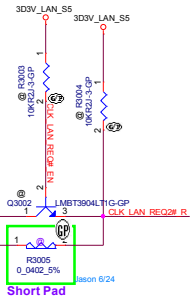






3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.





	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	O

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Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.	
Title	LAN RTL8106/8111
Document Number	LA-D071P
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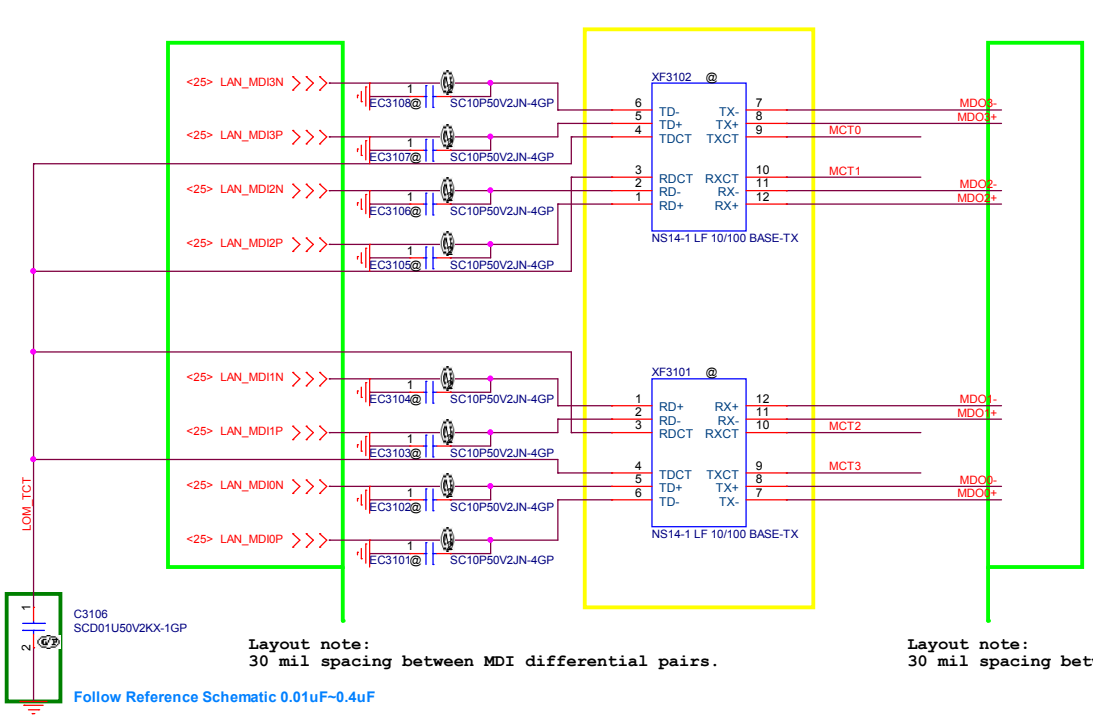
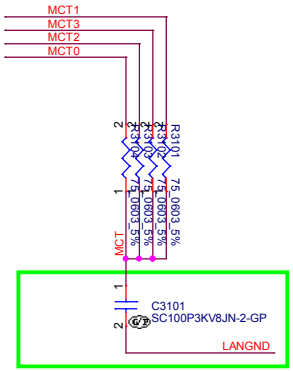
Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)

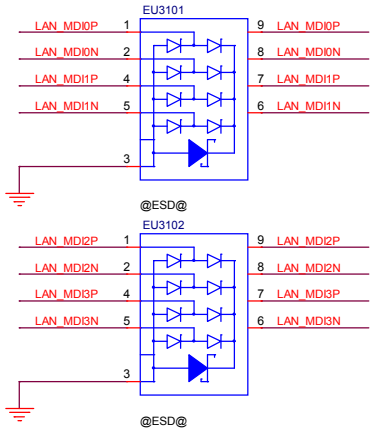


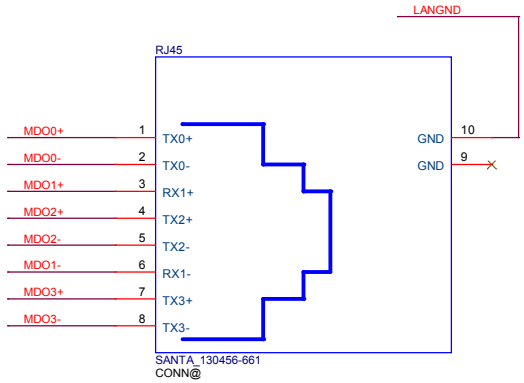
Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



Layout note:
30 mil spacing between MDI differential pairs.





XF3102
SP050007K00
1000@
S X'FORM_ NS14-1 LF 10100 BASE-TX

XF3101
SP050007K00
S X'FORM_ NS14-1 LF 10100 BASE-TX

Main:
SP050007K00, S X'FORM_ HD-081-A LAN
2nd:
SP050008L00, S X'FORM_ NS681677 LAN
Jason 2015/04/27

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

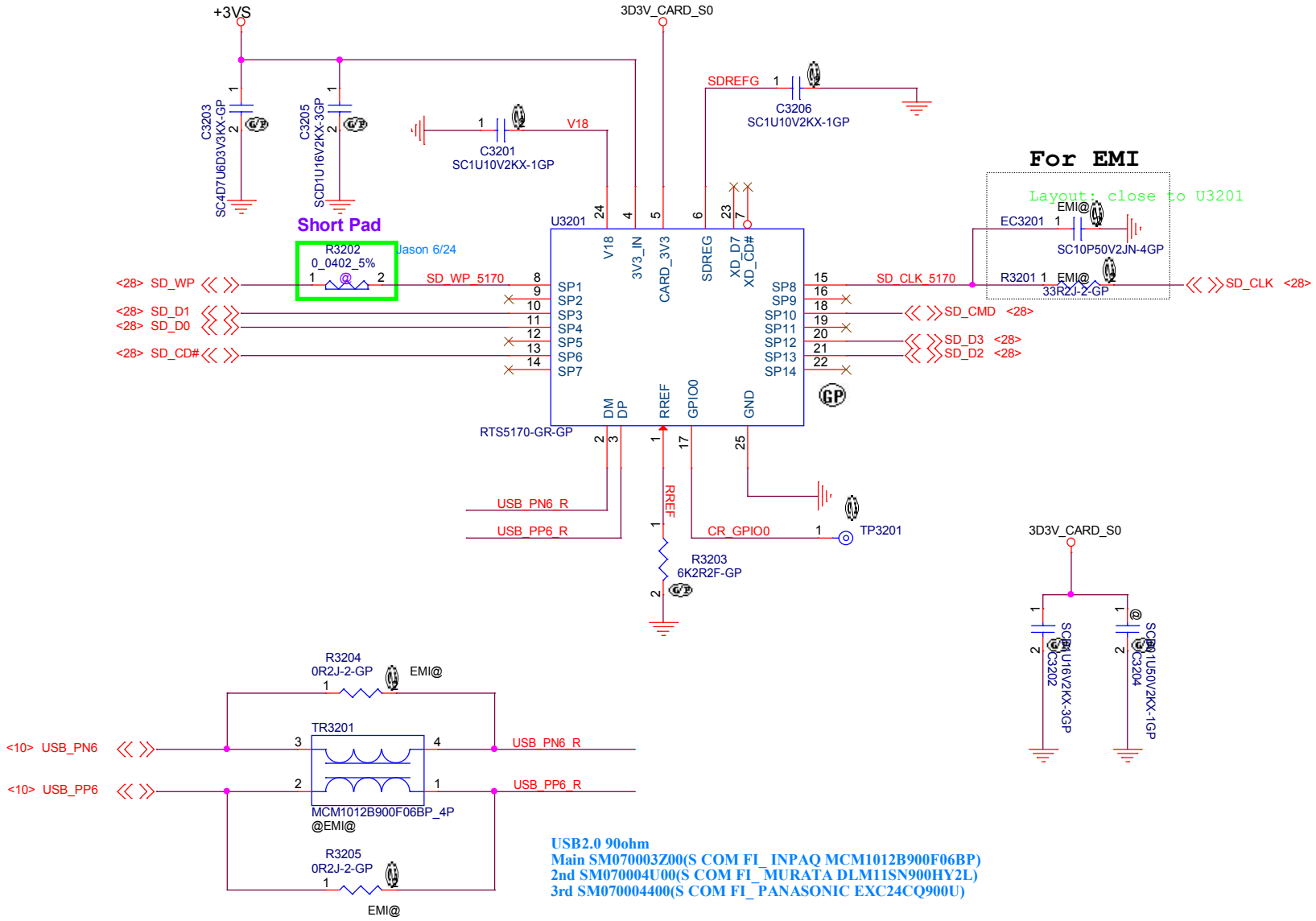
Title: XFOM&RJ45

Size | Document Number: LA-D071P | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 26 of 64

Main Func = Card Reader

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



USB2.0 90ohm
Main SM070003Z00(S COM FI_INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_PANASONIC EXC24CQ900U)

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

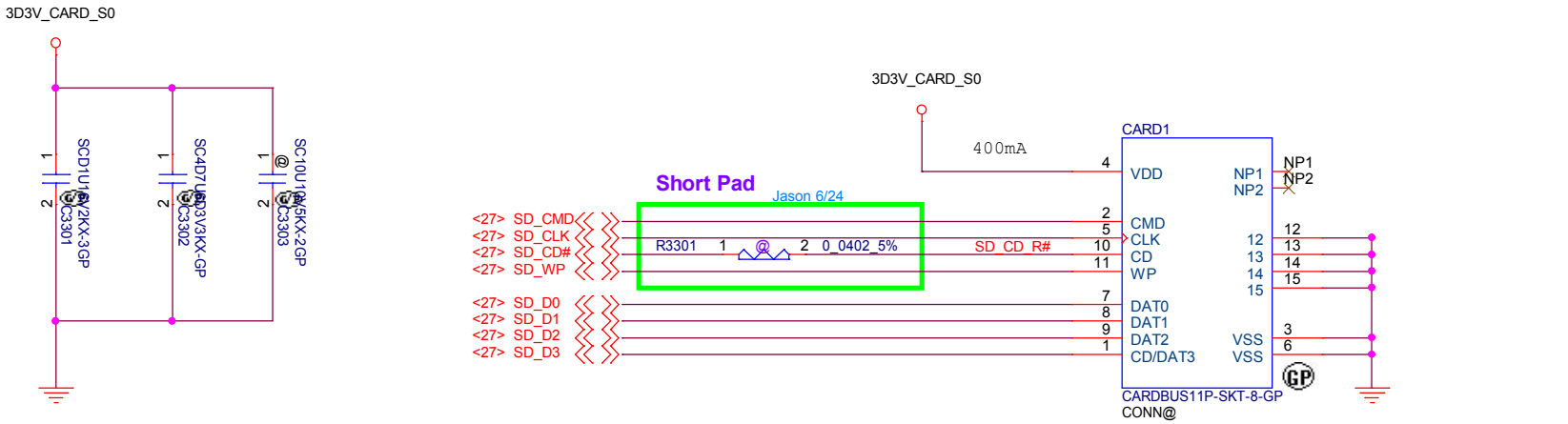
Compal Electronics, Inc.

Title: Card Reader RTS5170

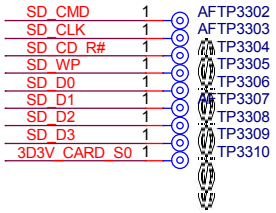
Size	Document Number	Rev
	LA-D071P	1.0(A00)

Date: Thursday, July 09, 2015 Sheet 27 of 64

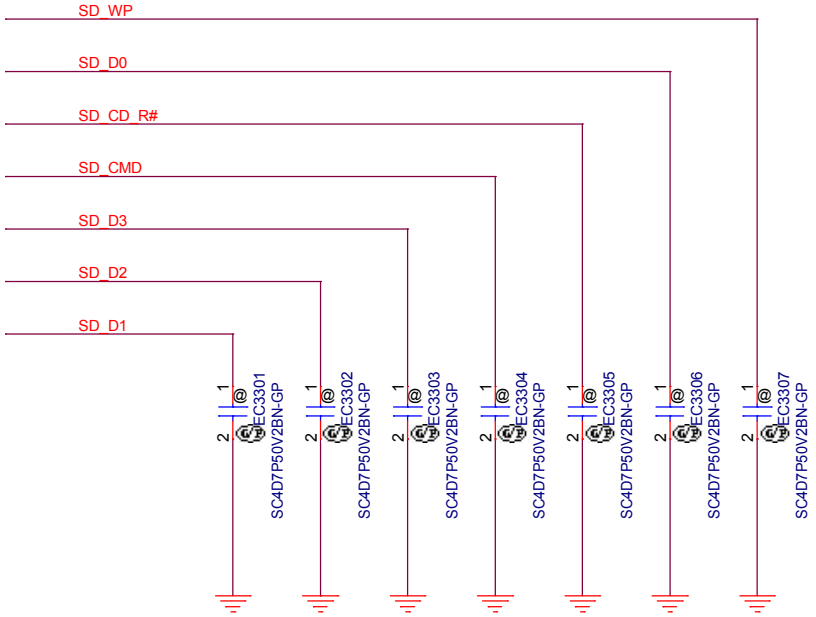
Main Func = Card Reader



2rd = 020.I0002.0001



For EMI Reserved



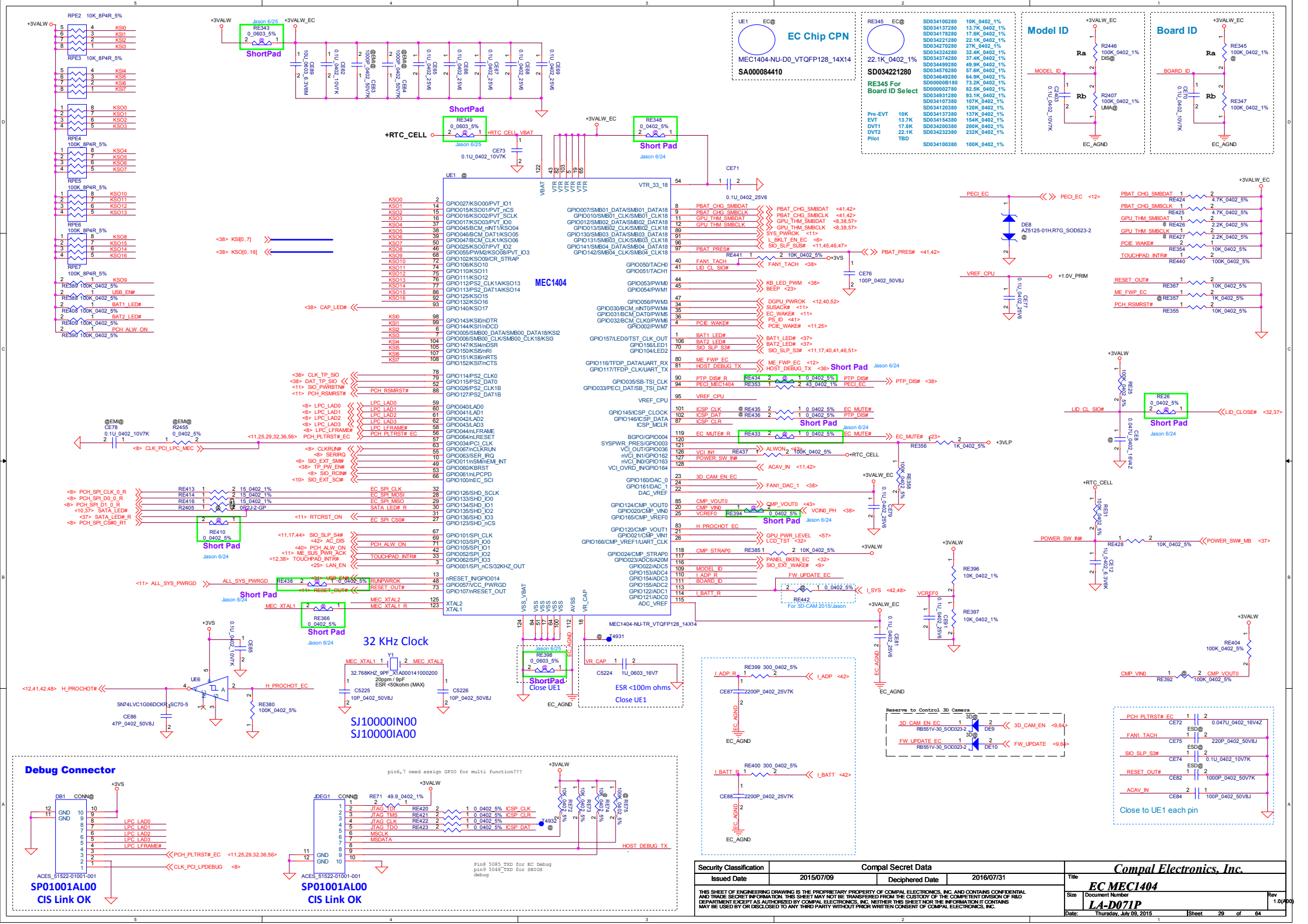
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **Card Reader RTS5170**

Size	Document Number	Rev
	LA-D071P	1.0(A00)

Date: Thursday, July 09, 2015 Sheet 28 of 64



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: EC MEC1404

Size: | Document Number: LA-D071P | Rev: 1.0(A00)

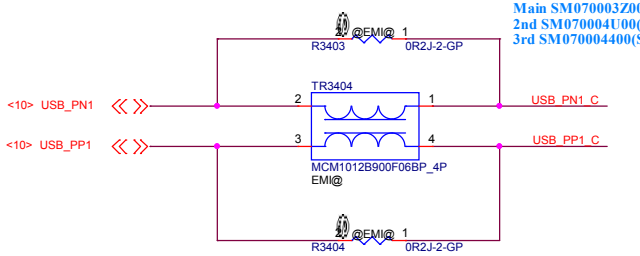
Date: Thursday, July 09, 2015 | Sheet 29 of 64

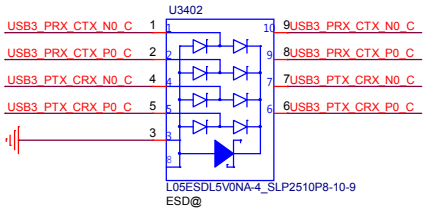
Main Func = USB3.0 Port1

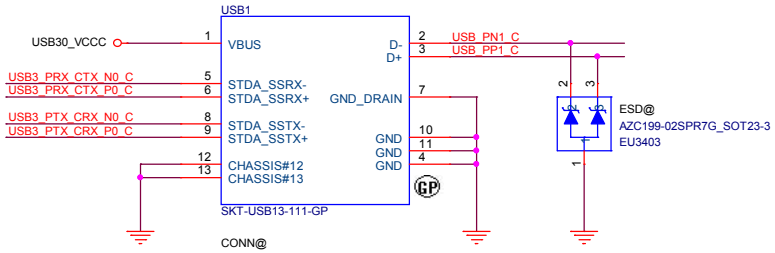
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1

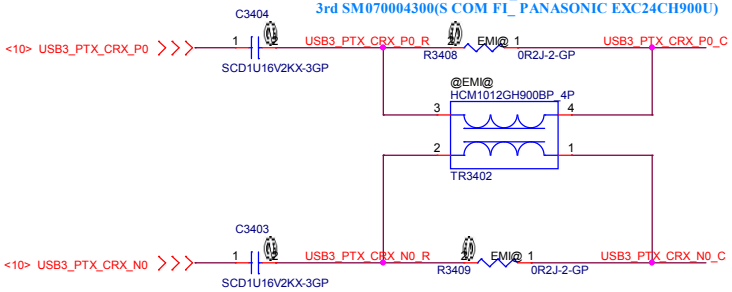
USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)



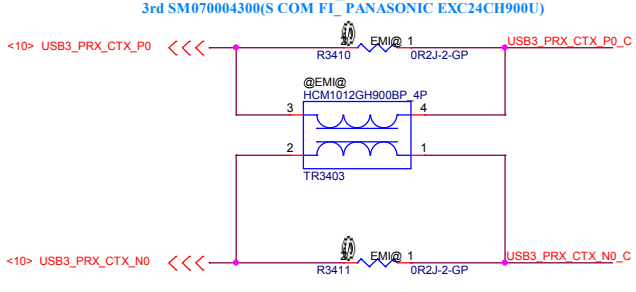




USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

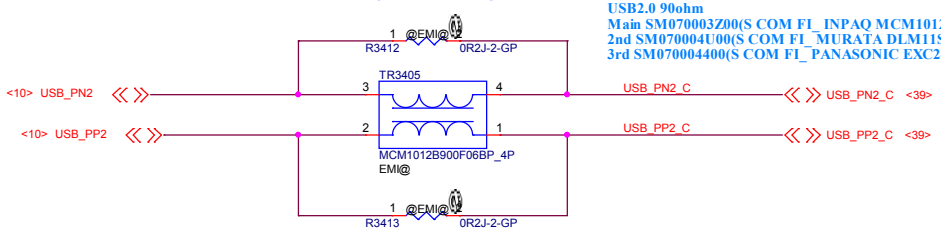


USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

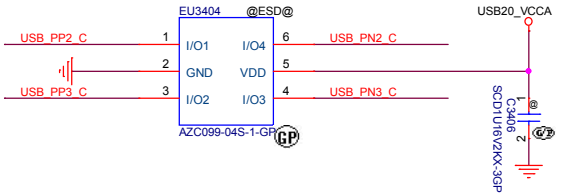


USB2 (USB2.0) CMC

USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)

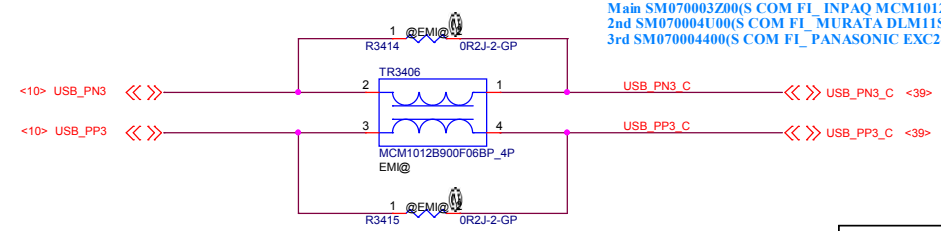


USB ESD Diode



USB3 (USB2.0) CMC

USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

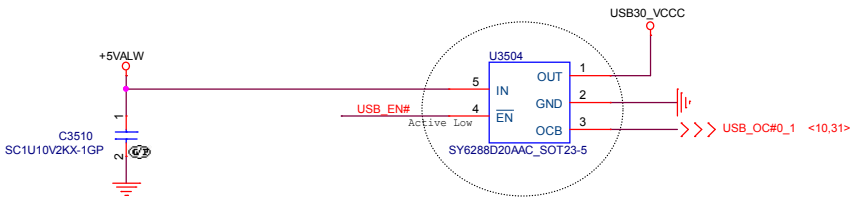
Compal Electronics, Inc.

Title: USB3.0 CONN

Size	Document Number	Rev
	LA-D071P	1.0(A00)

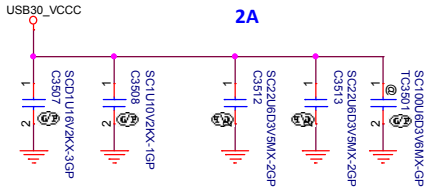
Date: Thursday, July 09, 2015 Sheet 30 of 64

Main Func = USB3.0 Port1

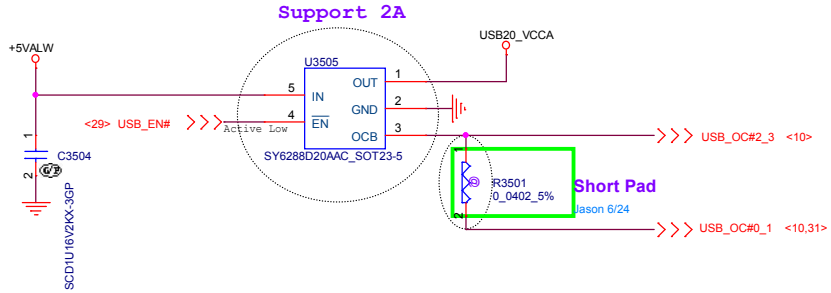


USB3.0 Port1

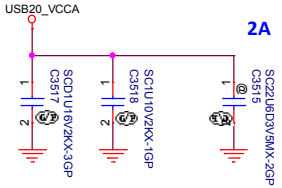
Layout Note: Close USB1



Main Func = USB2.0 Port3



USB2.0 Port3 (IO Board)



Main Func =

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

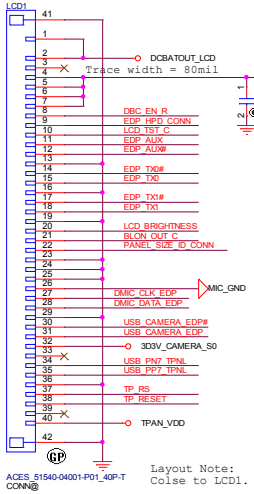
Compal Electronics, Inc.

Title: **USB Power SW**

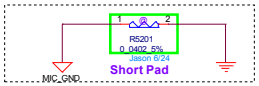
Size	Document Number	Rev
	LA-D071P	1.0(A00)

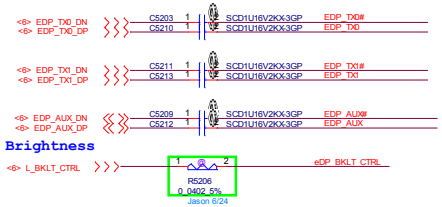
Date: Thursday, July 09, 2015 | Sheet 31 of 64

Main Func = LCD



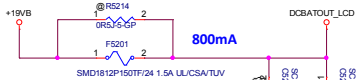
Layout Note:
Colse to LCD1.

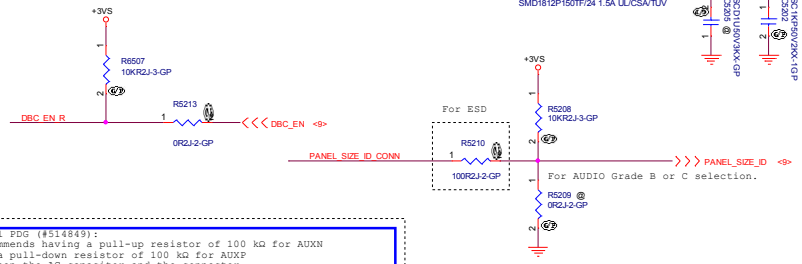




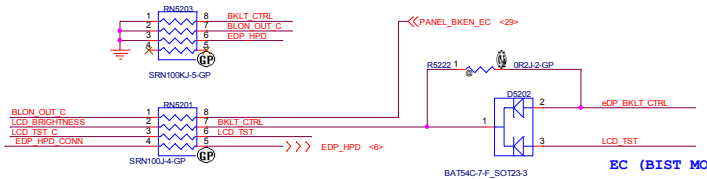
EE note: Never change R5211 to short pad after MP

INVERTER POWER

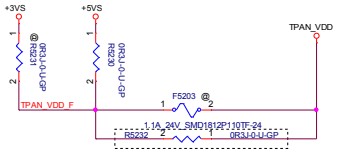




Intel PDG (#514849):
Recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.

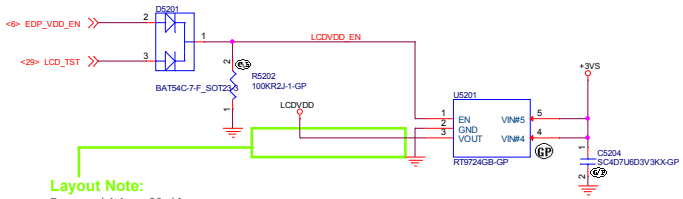


EC (BIST MODE)



EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

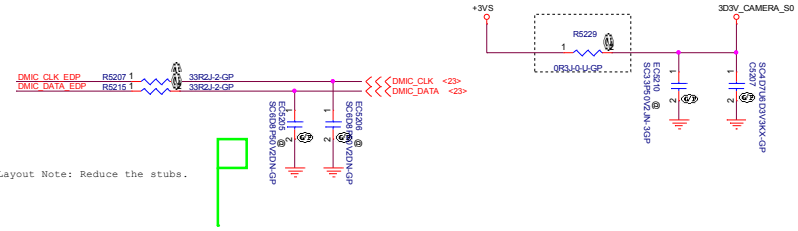
LCDVDD



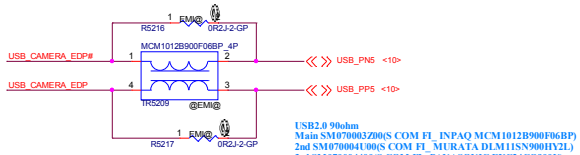
Layout Note:
Trace width = 80mil

Main Func = CAM

EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201



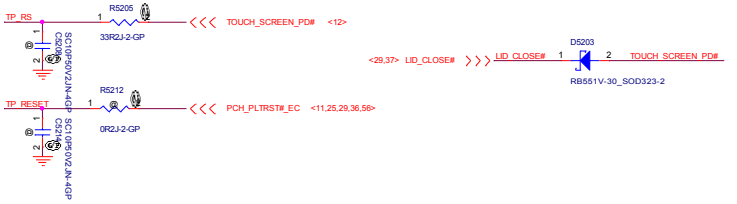
Layout Note: Reduce the stubs.

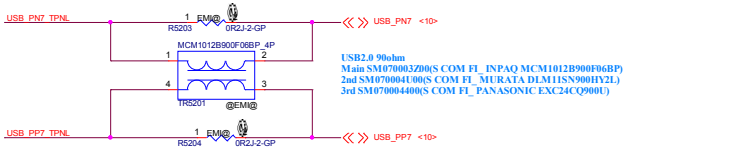


USB2.0 90ohm
Main SM070003Z00(S COM FI_INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_PANASONIC EXC24CQ900U)

Main Func = TS

Touch Panel



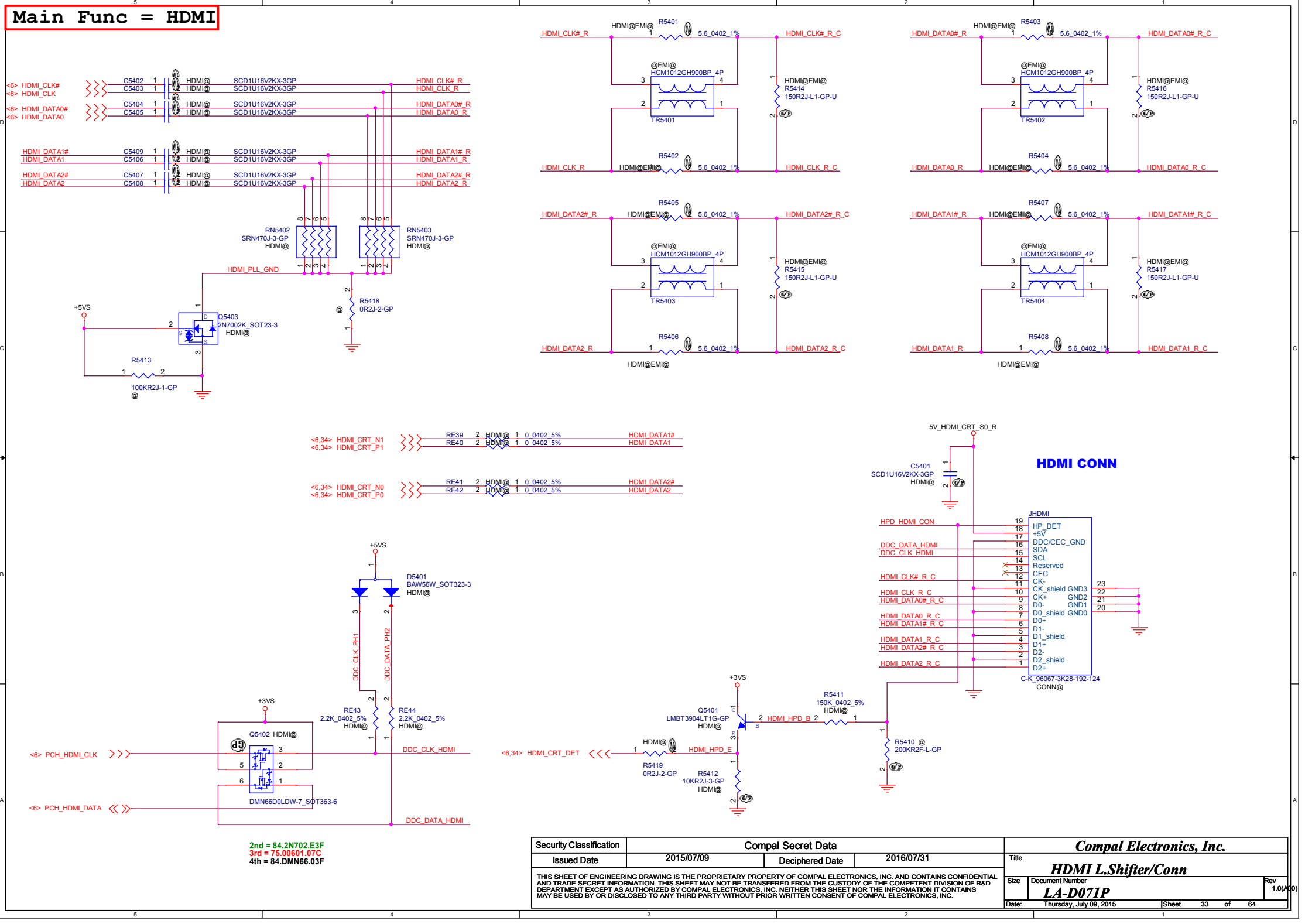


USB2.0 90ohm
Main SM070003Z00(S COM FI_INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_PANASONIC EXC24CQ900U)

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.	
Title	LCD/Inverter CONN
Size	Document Number: LA-D071P
Rev	1.0(A00)
Date: Thursday, July 09, 2015	Sheet 32 of 64

Main Func = HDMI



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

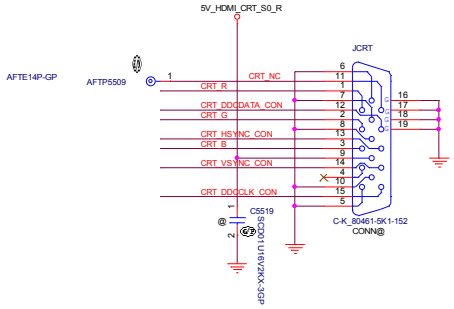
Compal Electronics, Inc.

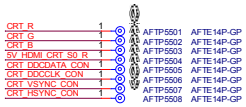
Title: **HDMI L.Shifter/Conn**

Size	Document Number	Rev
	LA-D071P	1.0(A00)

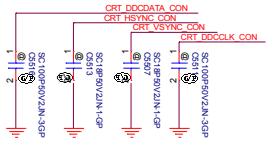
Date: Thursday, July 09, 2015 Sheet 33 of 64

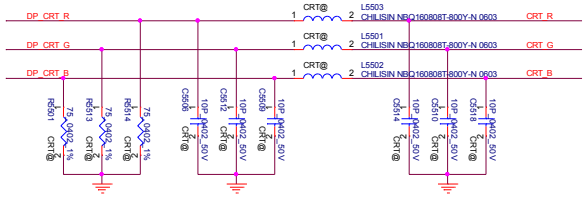
1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

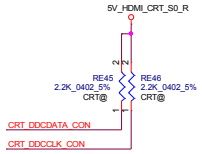


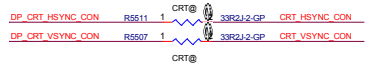


CRT RGB
CRT H/VSYNC
CRT SMBUS

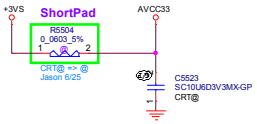


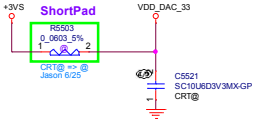


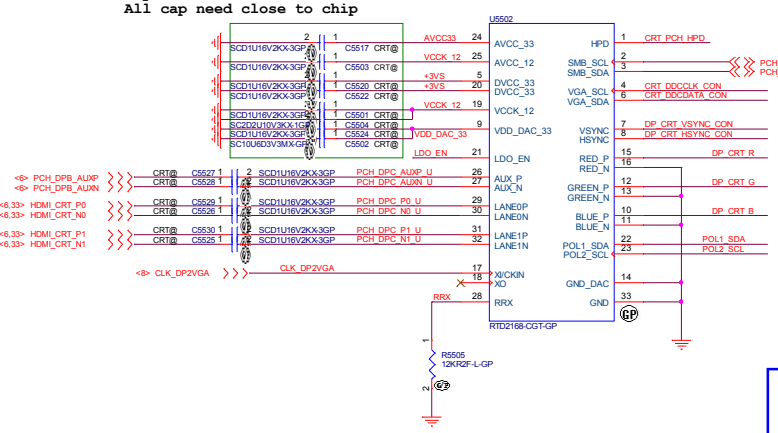


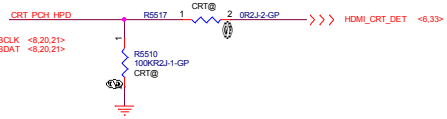


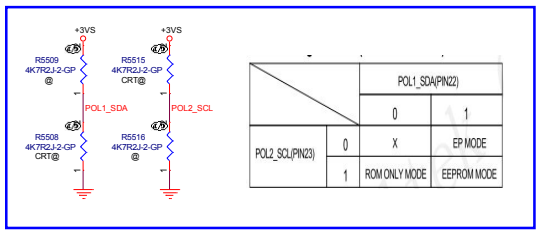
Layout note:
All cap need close to chip



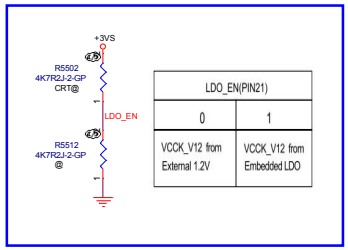








POL2_SCL(PIN23)	POL1_SDA(PIN22)	
	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE



LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

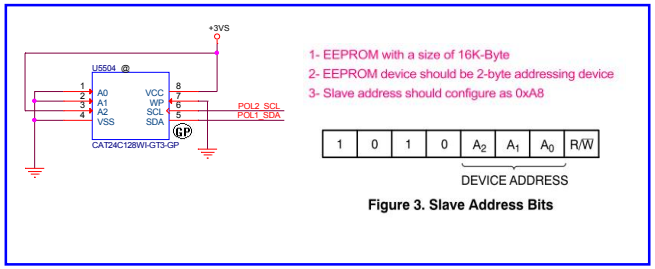


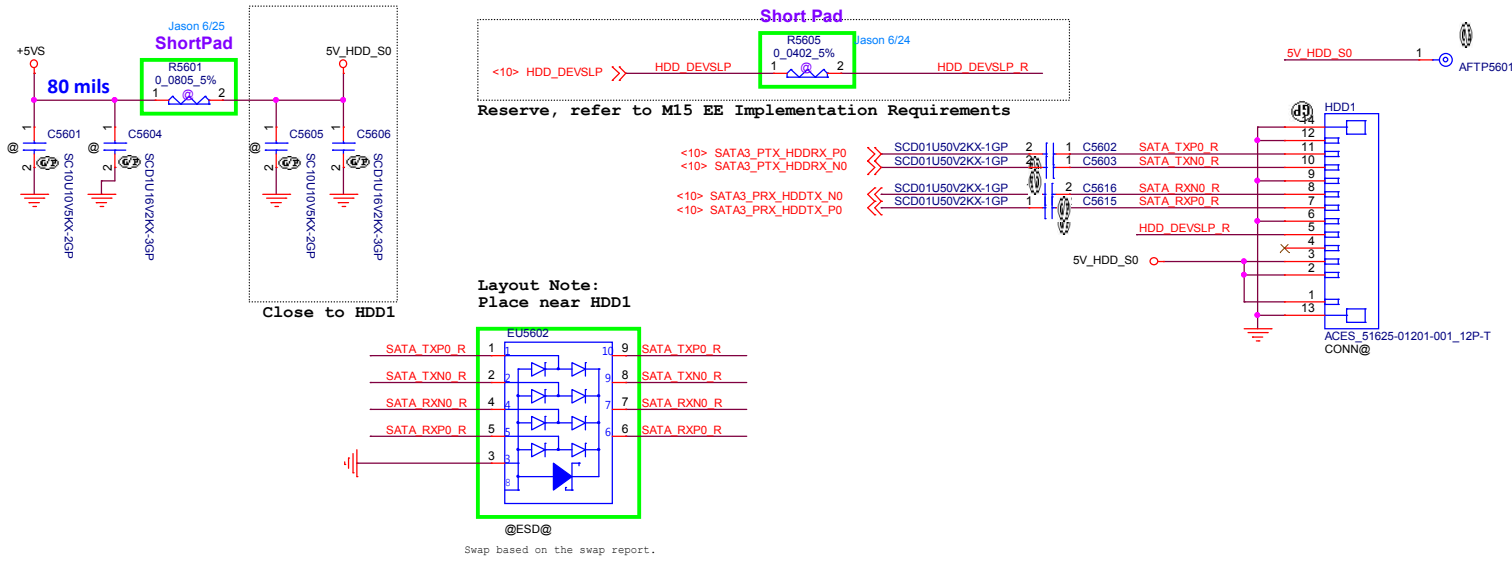
Figure 3. Slave Address Bits

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	DP to VGA Converter		
Size	Document Number		Rev
B	LA-D071P		1.0(A00
Date:	Thursday, July 09, 2015	Sheet	34 of 64

Main Func = HDD

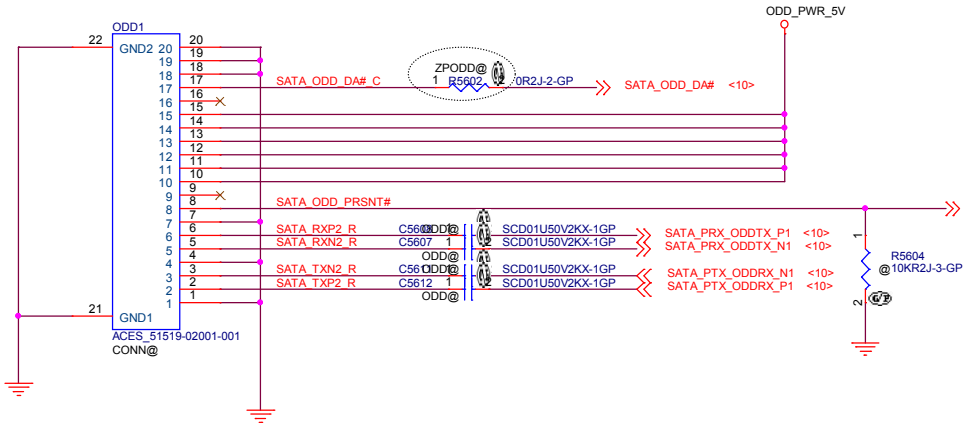
SATA HDD Connector



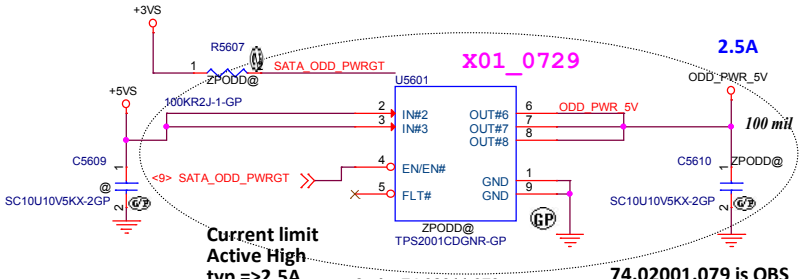
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

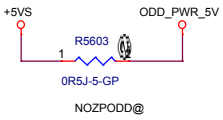
Main Func = ODD

ODD Connector

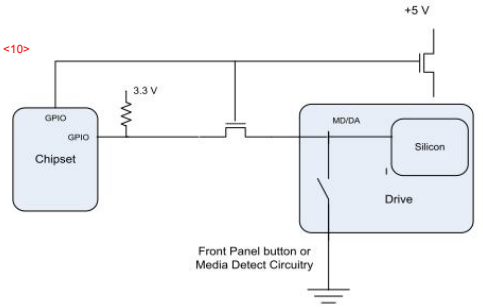


SATA Zero Power ODD





74.02001.079 is OBS
Will use 74.06288.079
but 74.06288.079 is also OBS
we will use 074.06288.0079.



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

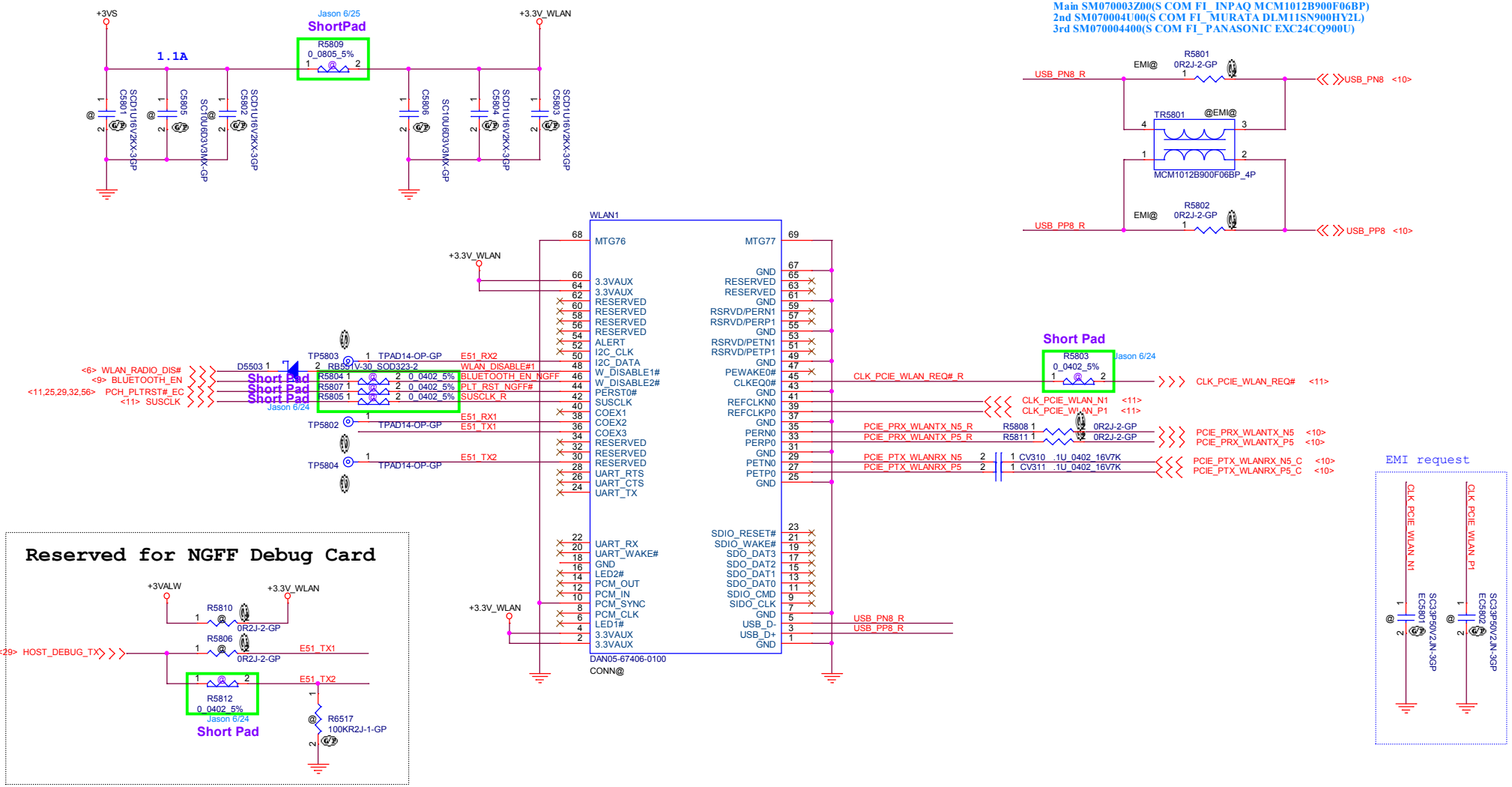
Compal Electronics, Inc.

Title: HDD/ODD

Size | Document Number: LA-D071P | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 35 of 64

Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

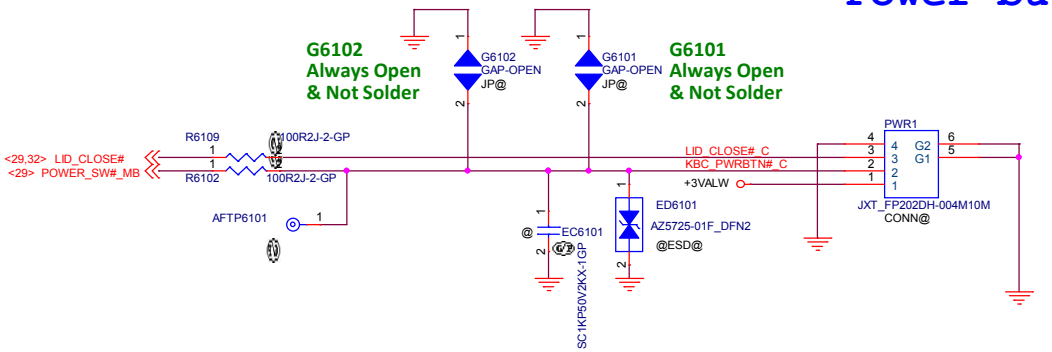
Title: NGFF_WLAN CONN

Size	Document Number	Rev
	LA-D071P	1.0(A00)

Date: Thursday, July 09, 2015 Sheet 36 of 64

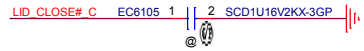
Main Func = Power BTN

Power button



EC6101 must be used 1000pF.

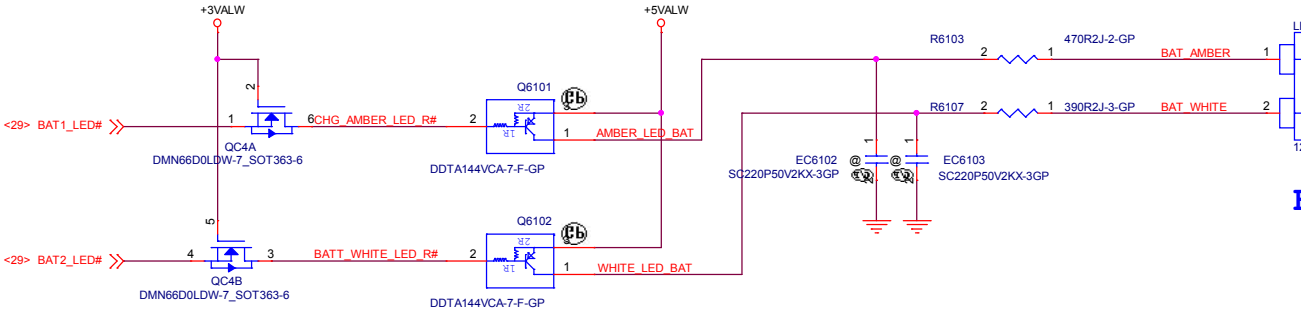
For EMI Reserved



Main Func = Battery LED

Low actived from KBC GPIO

Battery LED1(AMBER_LED)

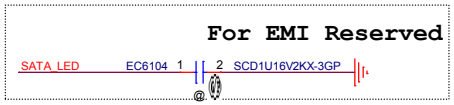


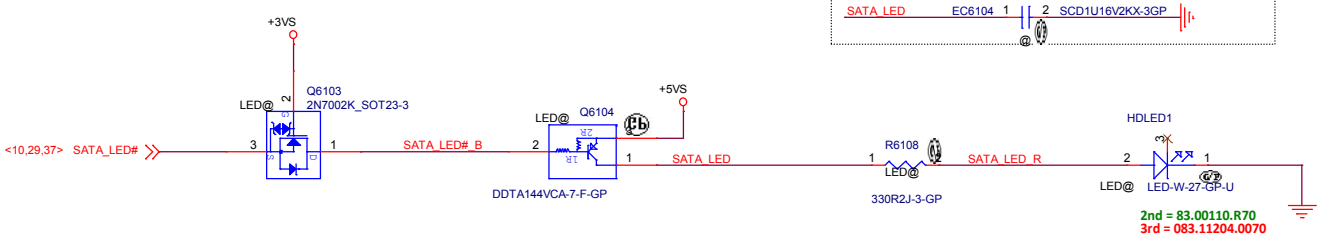
Need CIS Symbol

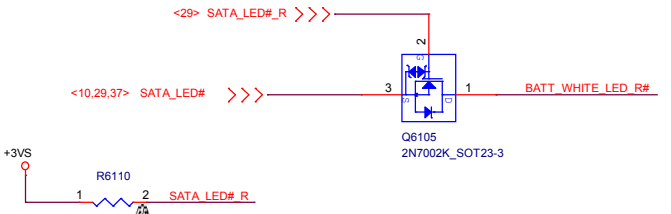
Battery LED2 (WHITE_LED)

Main Func = HDD LED

For EMI Reserved







SATA HDD LED
LOW actived from PCH GPIO

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.	
Title	LED Bard/Power Button
Size	Document Number: LA-D071P
Rev	1.0(A00)
Date: Thursday, July 09, 2015	Sheet 37 of 64

Main Func = KB

Keyboard Backlight (Reserved)

KB Backlight Power Consumption: 285mA max.

For EMI Reserved

CAP LED Control
LOW actived from KBC GPIO

Main Func = TPAD

Check leakage
Jason 2015/03/06

2015/5/19 Modify
Jason

EC/PS2

PCH/I2C

EMI depop location

2015/5/19 Modify
Jason

Check leakage
Change to PU TP_VDD (DVT1)
Jason 2015/03/06

2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

TP_VDD Discharge

Main Func = Thermal

Fan controller1

Layout Note:
Need 10 mil trace width.

Layout Note:
Signal Routing Guideline:
Trace width = 15mil

Main:
SA000067P00, S IC NCT7718W MSOP 8P THEMAL SENSOR
2nd:
SA00007WP00, S IC F75397M MSOP 8P THEMAL SENSOR
Jason 2015/03/03

2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

Address: X100_1100(4C), 1001_100X(98)

Layout Note:
C2607 close THM26

DXN and DXP routing width and spacing is 10 mil / 10 mil.

Short Pad

Close to Thermal sensor

Close to KBC
VD_IN1 for system thermal sensor

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/07/09	Deciphered Date 2016/07/31	Title: Keyboard/Touch Pad/Thermal
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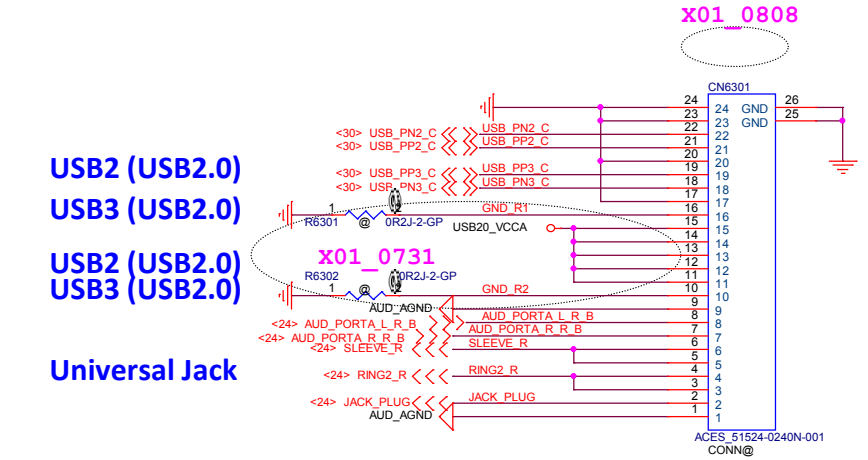
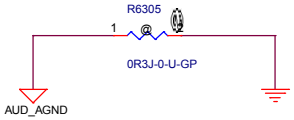
			Date: Thursday, July 09, 2015, Sheet 38 of 64

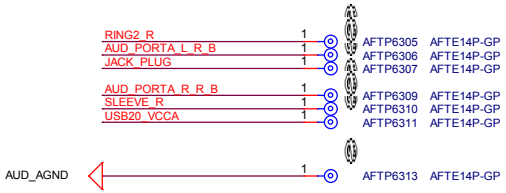
Main Func = IO Connector

I/O Board Connector





Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/07/09	Deciphered Date	2016/07/31
Title	IO Board Connector		
Size	Document Number		Rev
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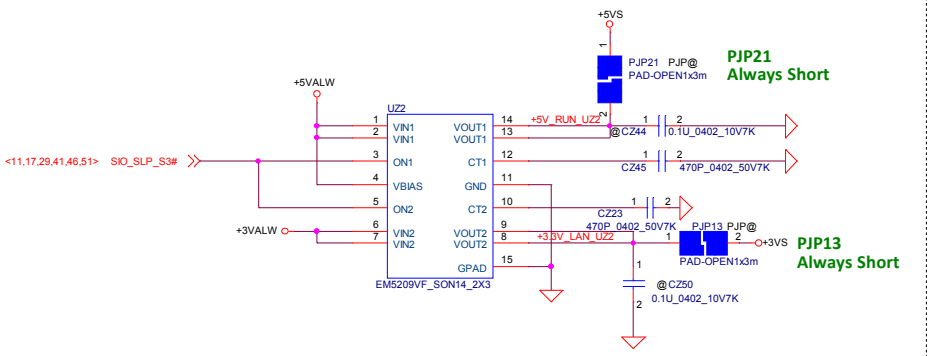
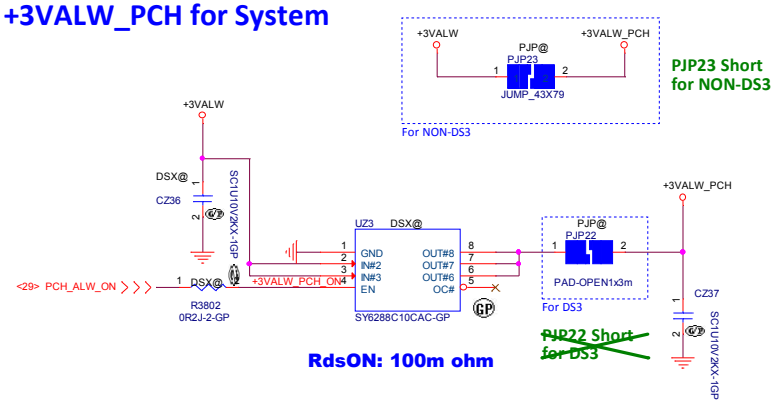
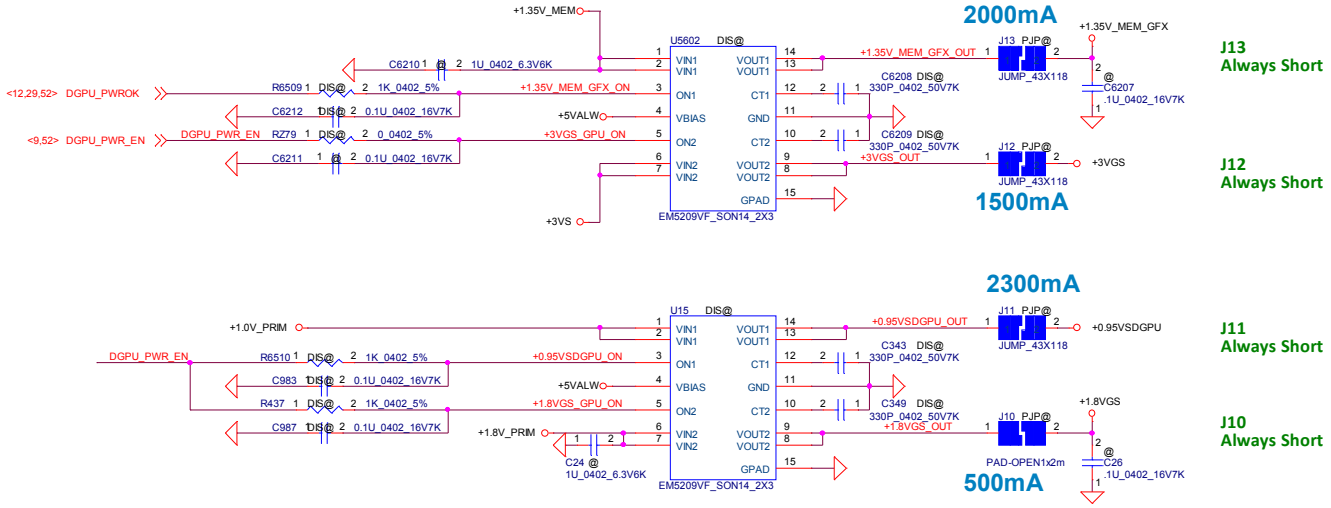
+5V_RUN/+3.3V_RUN for System



+3VALW_PCH for System



+3V/+0.95V/+1.8V/+1.35V for GPU

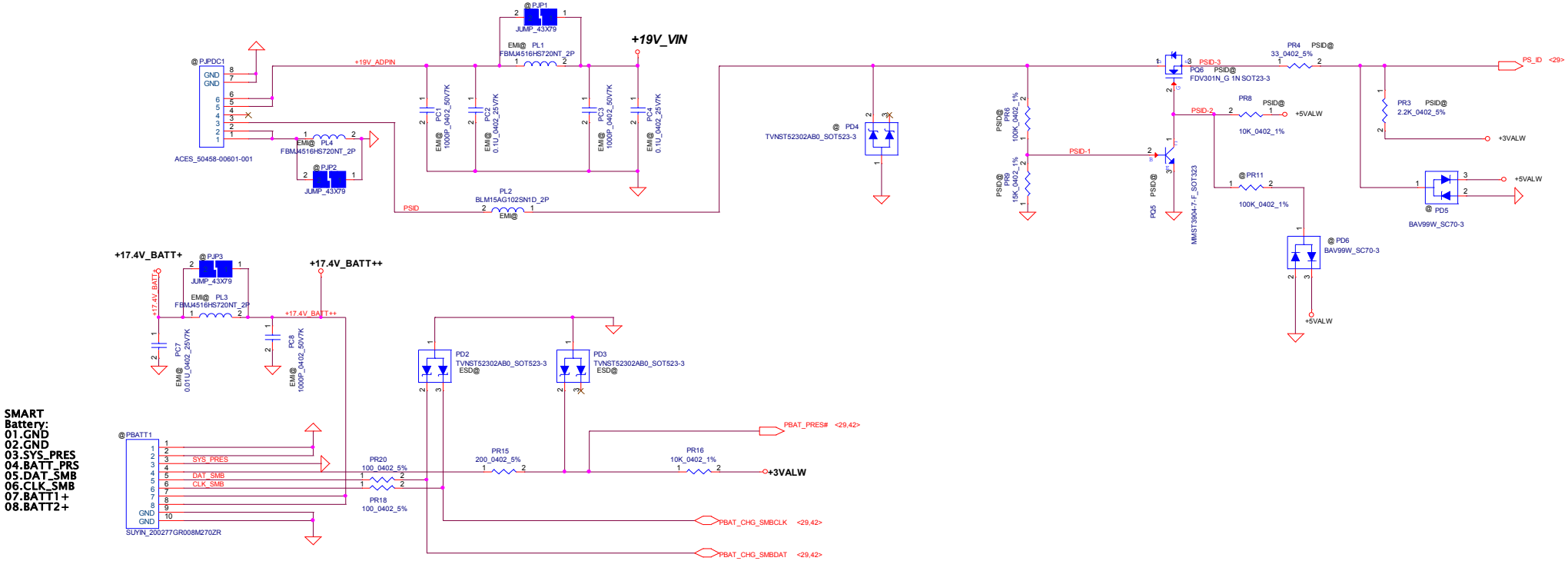


Compal Electronics, Inc.

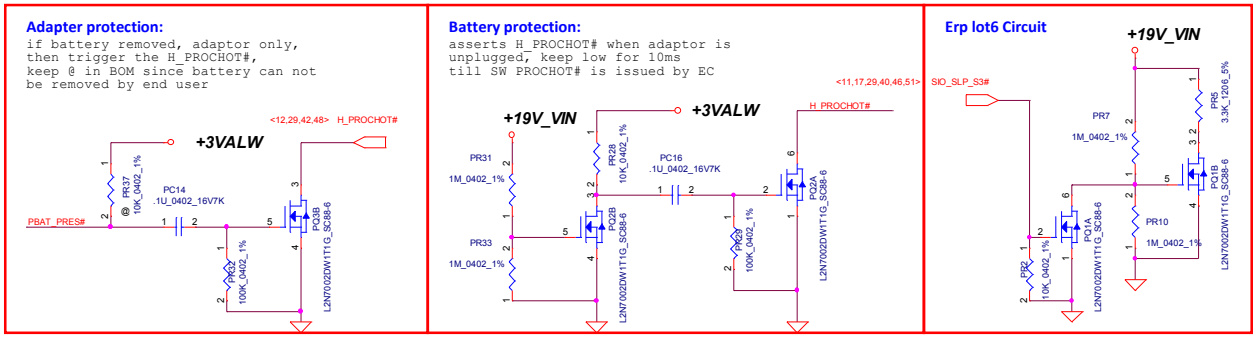
Title: Power control

Size: | Document Number: LA-D071P | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 40 of 64



Other component (37.1)



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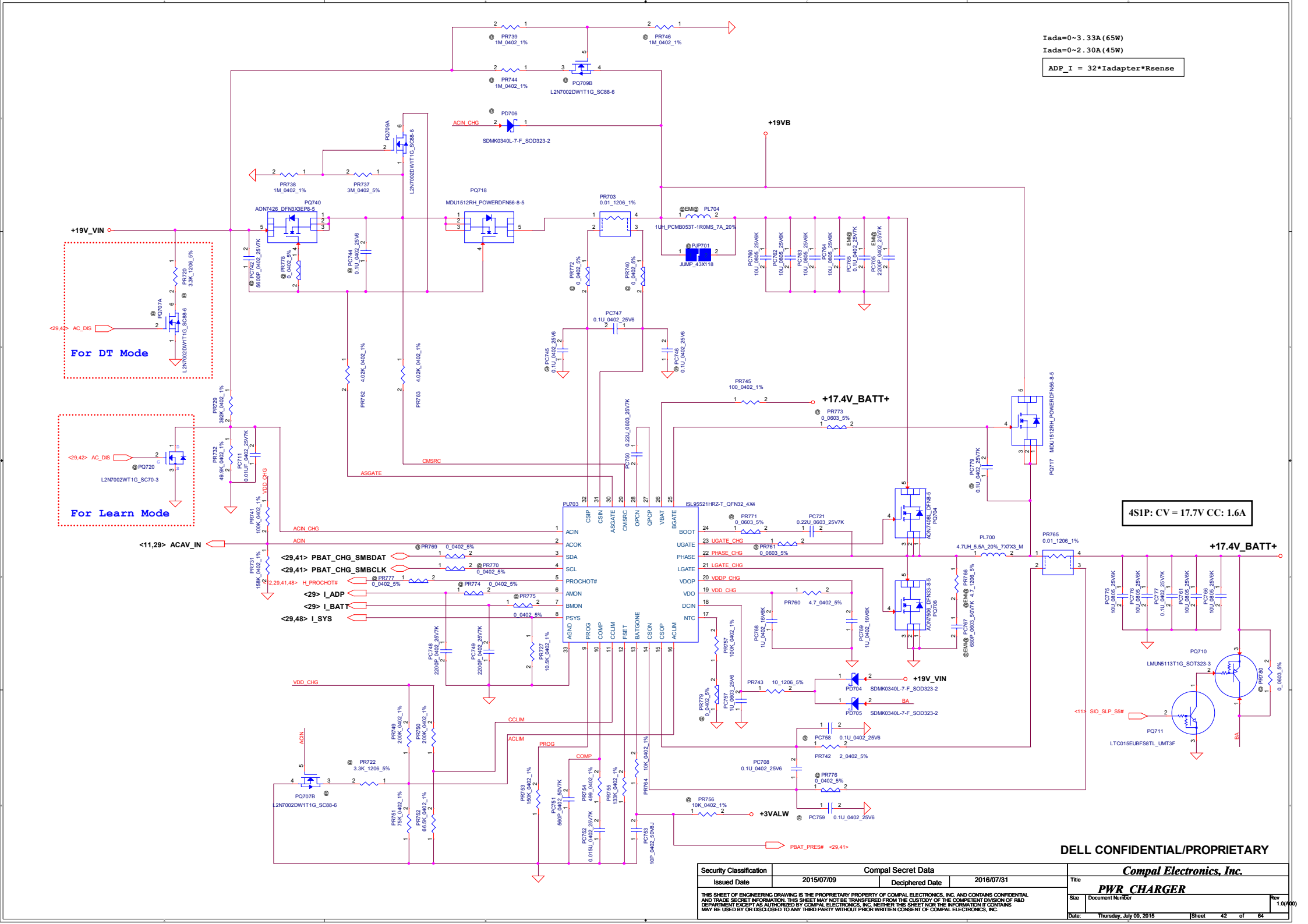
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev 1.0(A00)
Date: Thursday, July 09, 2015		Sheet 41 of 64	


Iada=0~3.33A(65W)
Iada=0~2.30A(45W)
ADP_I = 32*Iadapter*Rsense
4S1P: CV = 17.7V CC: 1.6A
For DT Mode
For Learn Mode
+19V_VIN
+19VB
+17.4V_BATT+
+3VALW
ISL95521HRZ-T_QFN32_4X4
PU703
PQ717 MDU1512RH_POWERDFN56-8-5
PQ718 MDU1512RH_POWERDFN56-8-5
PQ740 AON7426_DFN3X3EP8-5
PL704 1UH_PCMB053T-1R0MS_7A_20%
PL700 4.7UH_5.5A_20%_7X7X3_M
PQ710 LMUN5113T1G_SOT323-3
PQ711 LTC015EUBFS8TL_UMT3F
PBAT_PRES# <29,41>
<11,29> ACAV_IN
<29,41> PBAT_CHG_SMBDAT
<29,41> PBAT_CHG_SMBCLK
<29> I_ADP
<29> I_BATT
<29,48> I_SYS
<11> SIO_SLP_S5#
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Compal Electronics, Inc.
PWR_CHARGER
Security Classification
Compal Secret Data
Issued Date
2015/07/09
Deciphered Date
2016/07/31
Document Number
Rev 1.0(A00)
Date: Thursday, July 09, 2015
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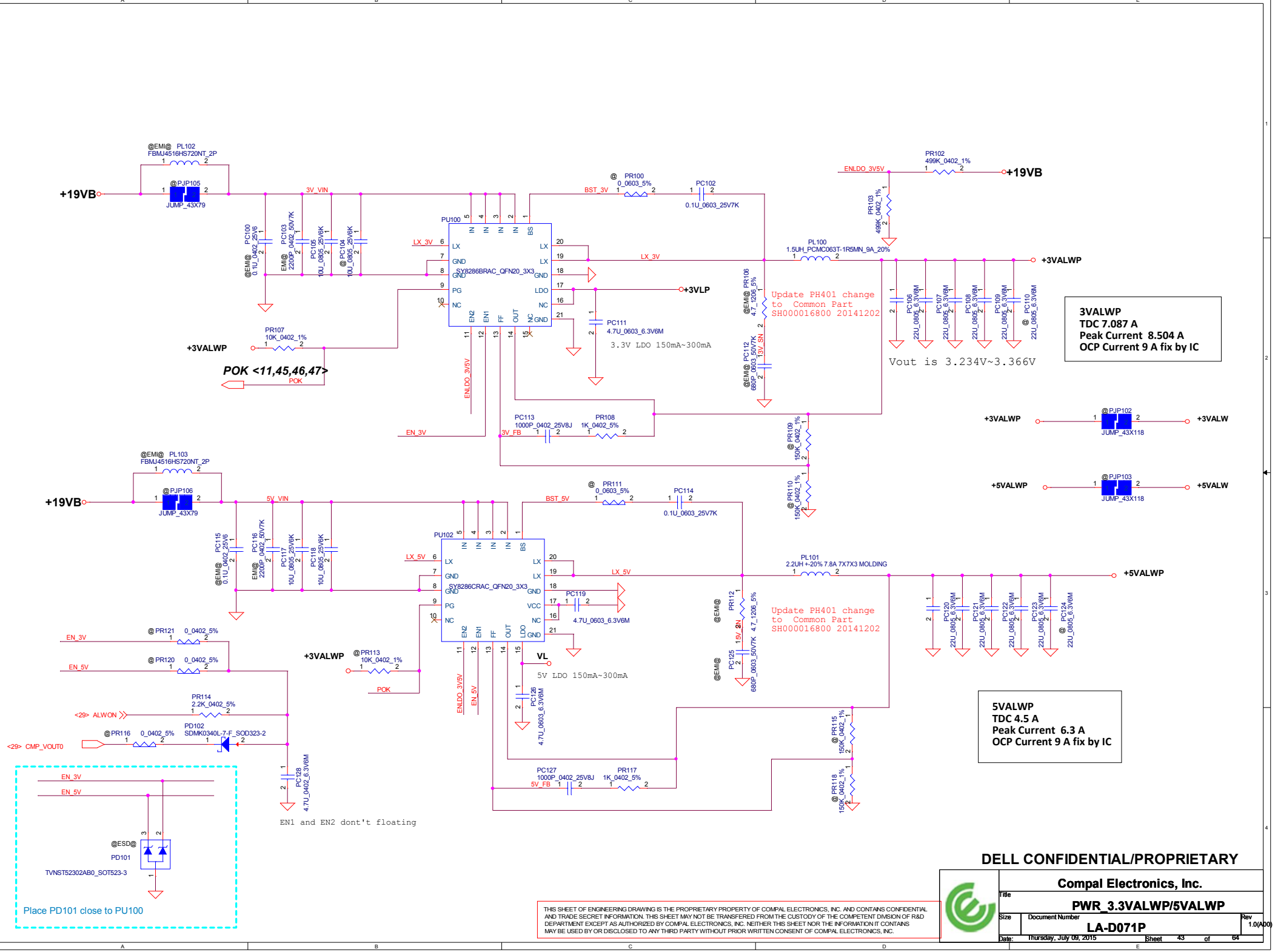
+19VB
@EMI@ PL102 FBMJ4516HS720NT_2P
@PJP105 JUMP_43X79
3V_VIN
PC100 0.1U_0402_25V6
PC103 2200P_0402_50V7K
PC105 10U_0805_25V6K
PC104 10U_0805_25V6K
PU100 SY8286BRAC_QFN20_3X3
LX_3V
BST_3V
@ PR100 0_0603_5%
PC102 0.1U_0603_25V7K
PR102 499K_0402_1%
ENLDO_3V5V
PR103 499K_0402_1%
PL100 1.5UH_PCMC063T-1R5MN_9A_20%
+3VALWP
PC106 22U_0805_6.3V6M
PC107 22U_0805_6.3V6M
PC108 22U_0805_6.3V6M
PC109 22U_0805_6.3V6M
@ PC110 22U_0805_6.3V6M
@EMI@ PR106 4.7_1206_5%
@EMI@ PC112 680P_0603_50V7K
1.5V_SN
PC111 4.7U_0603_6.3V6M
3.3V LDO 150mA~300mA
+3VLP
PR107 10K_0402_1%
POK <11,45,46,47>
POK
ENLDO_3V5V
EN_3V
PC113 1000P_0402_25V8J
PR108 1K_0402_5%
3V_FB
Update PH401 change to Common Part SH000016800 20141202
Vout is 3.234V~3.366V
3VALWP
TDC 7.087 A
Peak Current 8.504 A
OCP Current 9 A fix by IC
@PJP102 JUMP_43X118
+3VALW
@EMI@ PL103 FBMJ4516HS720NT_2P
@PJP106 JUMP_43X79
5V_VIN
PC115 0.1U_0402_25V6
PC116 2200P_0402_50V7K
PC117 10U_0805_25V6K
PC118 10U_0805_25V6K
PU102 SY8286CRAC_QFN20_3X3
LX_5V
BST_5V
@ PR111 0_0603_5%
PC114 0.1U_0603_25V7K
PR109 150K_0402_1%
PR110 150K_0402_1%
@PJP103 JUMP_43X118
+5VALW
PL101 2.2UH +-20% 7.8A 7X7X3 MOLDING
+5VALWP
PC119 4.7U_0603_6.3V6M
PC120 22U_0805_6.3V6M
PC121 22U_0805_6.3V6M
PC122 22U_0805_6.3V6M
PC123 22U_0805_6.3V6M
@ PC124 22U_0805_6.3V6M
@EMI@ PR112 4.7_1206_5%
1.5V_2N
@EMI@ PC125 680P_0603_50V7K
Update PH401 change to Common Part SH000016800 20141202
5VALWP
TDC 4.5 A
Peak Current 6.3 A
OCP Current 9 A fix by IC
@PR121 0_0402_5%
@PR120 0_0402_5%
EN_3V
EN_5V
PR114 2.2K_0402_5%
<29> ALWON
@PR116 0_0402_5%
PD102 SDMK0340L-7-F_SOD323-2
<29> CMP_VOUT0
@PR113 10K_0402_1%
+3VALWP
POK
VL
5V LDO 150mA~300mA
PC126 4.7U_0603_6.3V6M
PC128 4.7U_0402_6.3V6M
PC127 1000P_0402_25V8J
PR117 1K_0402_5%
5V_FB
@PR115 150K_0402_1%
@PR118 150K_0402_1%
EN1 and EN2 dont't floating
@ESD@ PD101 TVNST52302AB0_SOT523-3
Place PD101 close to PU100
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Compal Electronics, Inc.
PWR_3.3VALWP/5VALWP
LA-D071P
Rev 1.0(A00)
Thursday, July 09, 2015
Sheet 43 of 64
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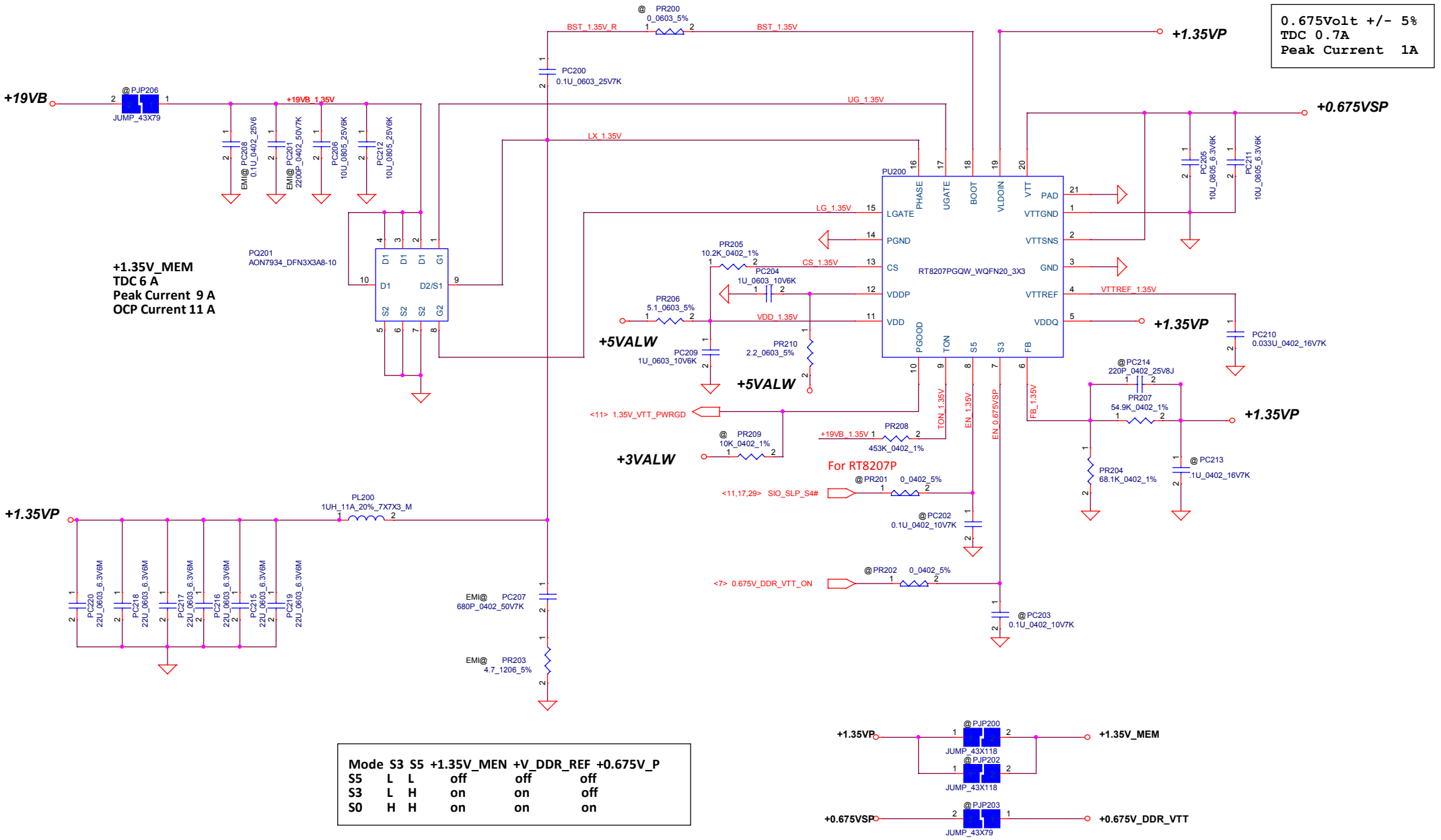
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A
+19VB
+1.35VP
+0.675VSP
+1.35V_MEM
TDC 6 A
Peak Current 9 A
OCP Current 11 A
+5VALW
+3VALW
PU200
RT8207PGQW_WQFN20_3X3
PQ201
AON7934_DFN3X3A8-10
PL200
1UH_11A_20%_7X7X3_M
For RT8207P
+1.35V_MEN
+V_DDR_REF
+0.675V_P
S5 L L off off off
S3 L H on on off
S0 H H on on on
+0.675V_DDR_VTT
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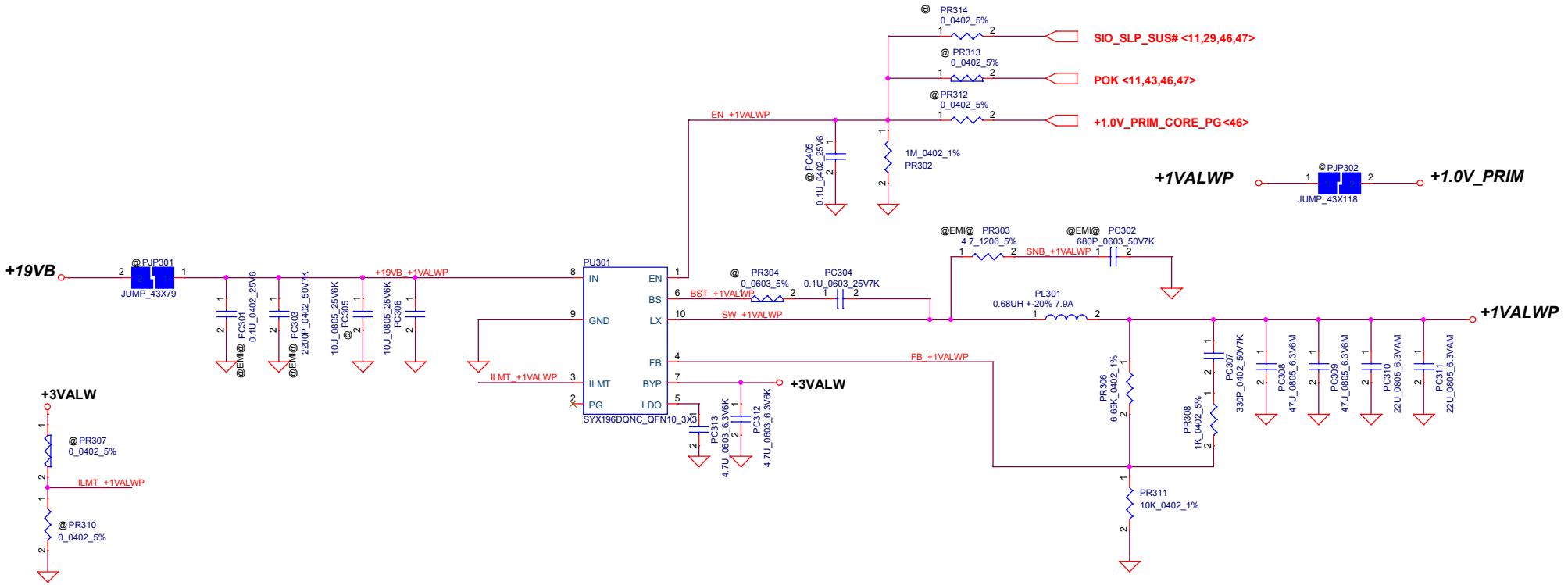
Compal Secret Data
2015/07/09
2016/07/31
PWR_+1.35V_MEN/+0.675V_DDR_VTT
Thursday, July 09, 2015



+1.0V_PRIM
TDC 2.63 A
Peak Current 3.748 A
OCP Current 6.0 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm , 12.0mohm	

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Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Title	PWR_+1VALWP		
Size: Custom	Document Number		Rev: 1.0(A00)
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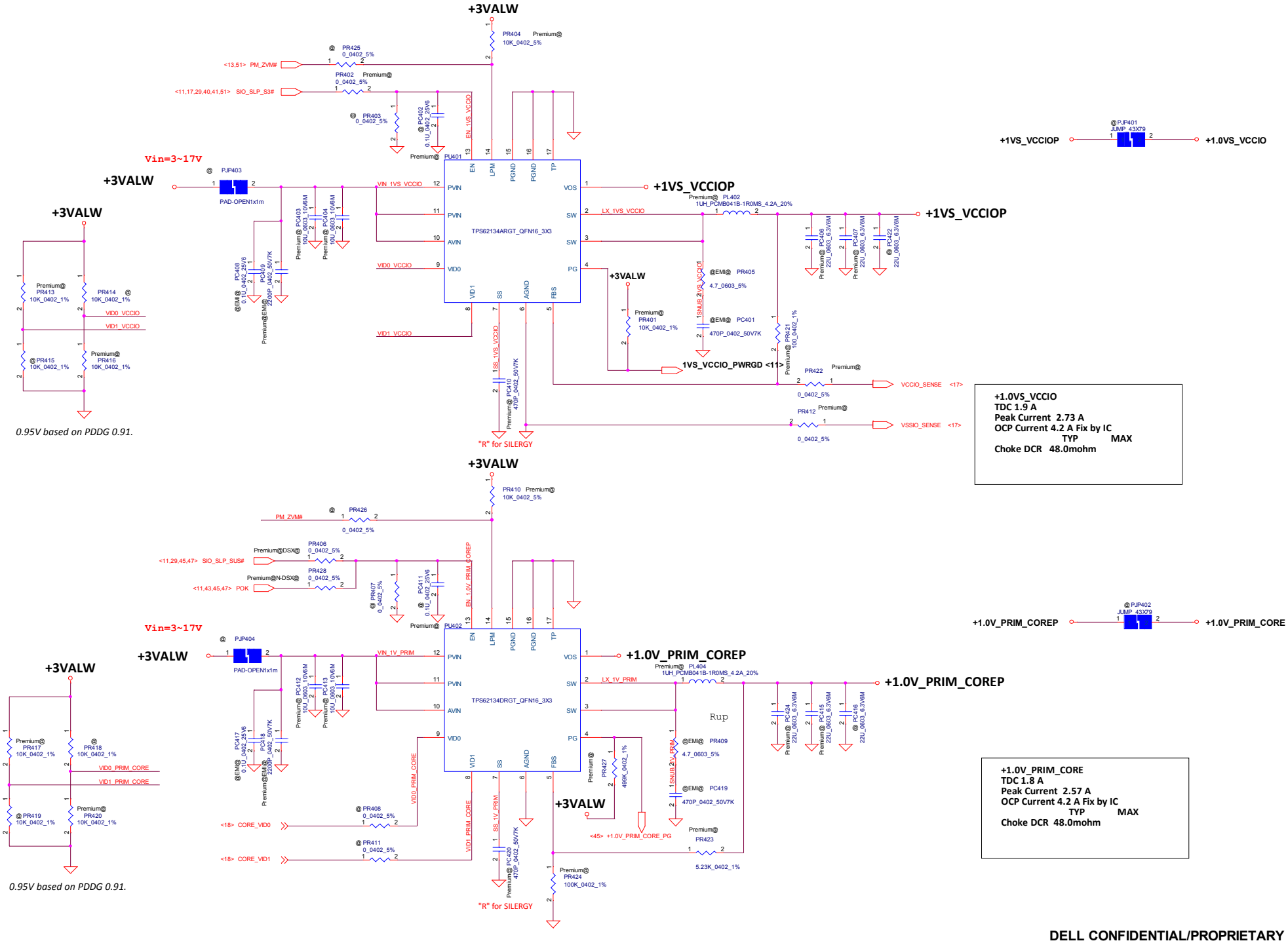

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Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

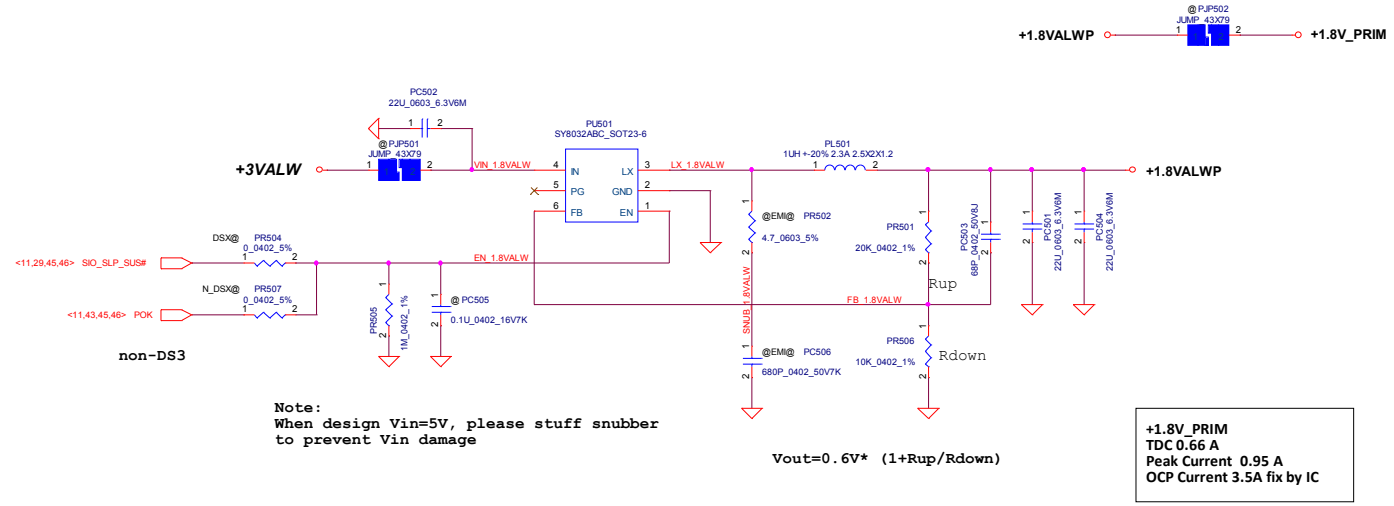
Compal Electronics, Inc.

Title: PWR_+1VS_VCCIOP/+1.0V_PRIM_COREP

Size	Document Number	Rev
		1.0(A00)

Date: Thursday, July 09, 2015 Sheet 46 of 64

TDC = 0.76A
Prak current : 1.096A
OCP : 3A
FB=0.6V



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

+1.8V_PRIM
TDC 0.66 A
Peak Current 0.95 A
OCP Current 3.5A fix by IC

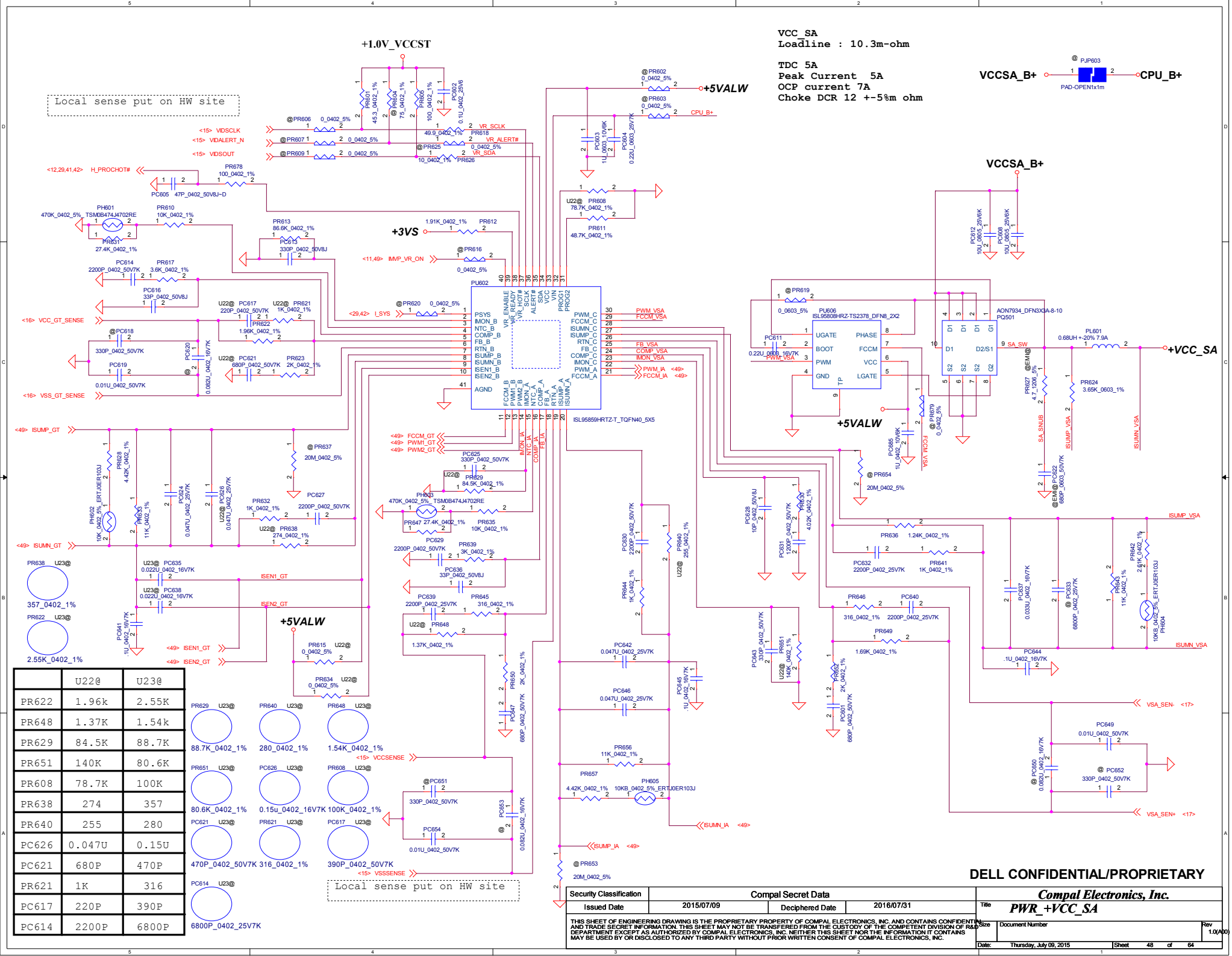
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: PWR +1.8V_PRIM and +1.5VS

Size	Document Number	Rev
C		1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 47 of 64



	U22@	U23@
PR622	1.96k	2.55K
PR648	1.37K	1.54k
PR629	84.5K	88.7K
PR651	140K	80.6K
PR608	78.7K	100K
PR638	274	357
PR640	255	280
PC626	0.047U	0.15U
PC621	680P	470P
PR621	1K	316
PC617	220P	390P
PC614	2200P	6800P

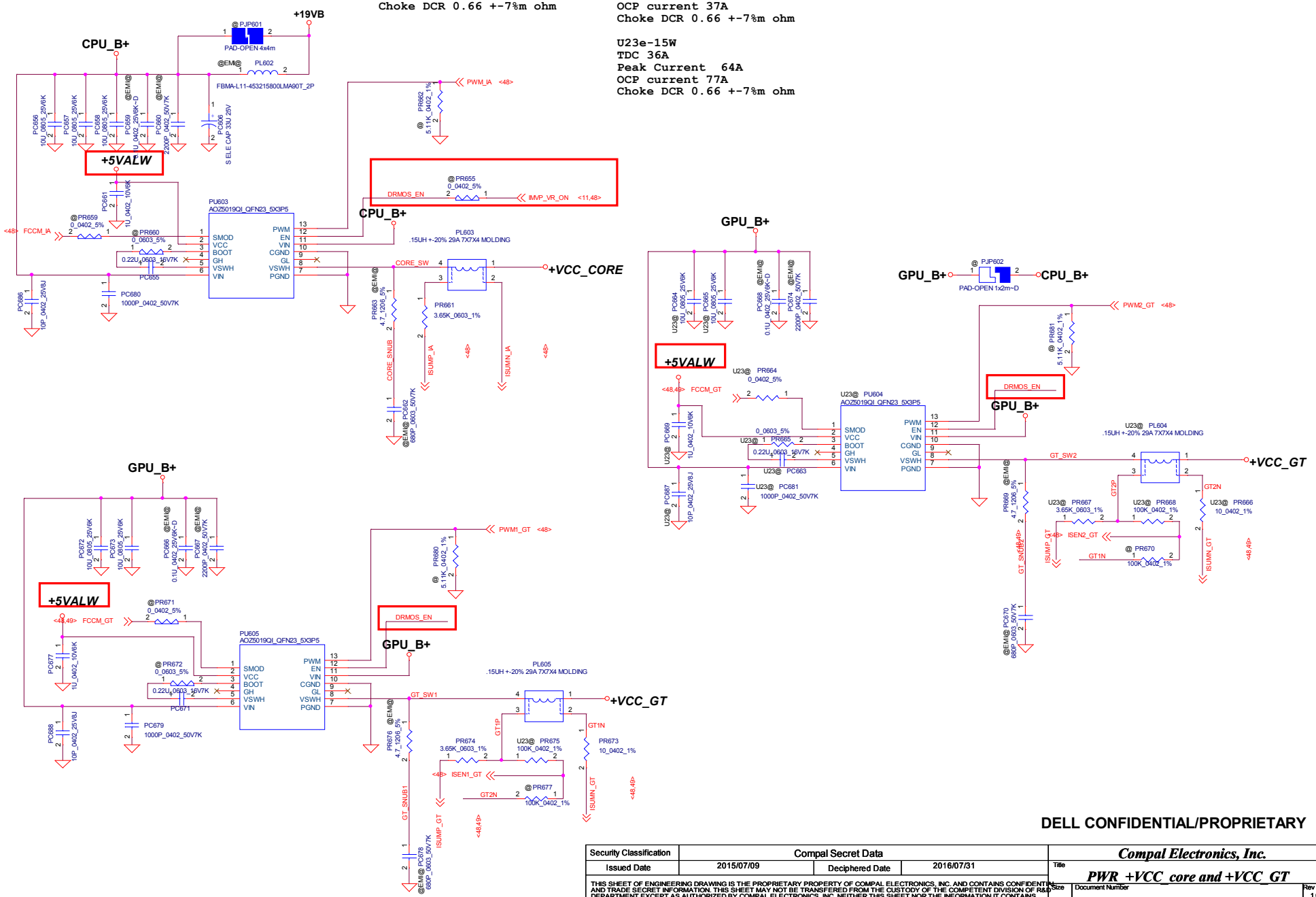
VCC_core
U22 - 15W
Loadline : 2.4m-ohm
U23e - 15W
Loadline : 2.4m-ohm

TDC 21A
Peak Current 29A
OCP current 34A
Choke DCR 0.66 +-7%m ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
U23e - 15W
Loadline : 2m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7%m ohm

U23e-15W
TDC 36A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7%m ohm



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Issued Date	2015/07/09	Deciphered Date	2016/07/31

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Compal Electronics, Inc.

Title: PWR_+VCC_core and +VCC_GT

Size | Document Number | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 49 of 64

VCC_CORE Place on CPU
U22-15W
22U_0603 * 18 pcs +1U_0201*35 pcs+220u_D2*2 pcs
U23e-15W
22U_0603 * 27 pcs +1U_0201*35 pcs+330u_D2*2 pcs

VCC_GT Place on CPU
U22-15W
22U_0603 * 25 pcs +1U_0201*12 pcs+330u_D2*1 pcs
U23e-15W
22U_0603 * 48 pcs +1U_0201*12 pcs+330u_D2*4 pcs

+VCC_CORE

+VCC_GT

VCC_SA Place on CPU
U22-15W
22U_0603 * 9 pcs + 1U_0201*7 pcs
U23e-15W
22U_0603 * 12 pcs + 1U_0201*7 pcs

+VCC_SA

+VCC_GT

For GTX

+VGA_CORE

For VGACORE

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Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: PWR_CPU&VGA bulk and MLCC

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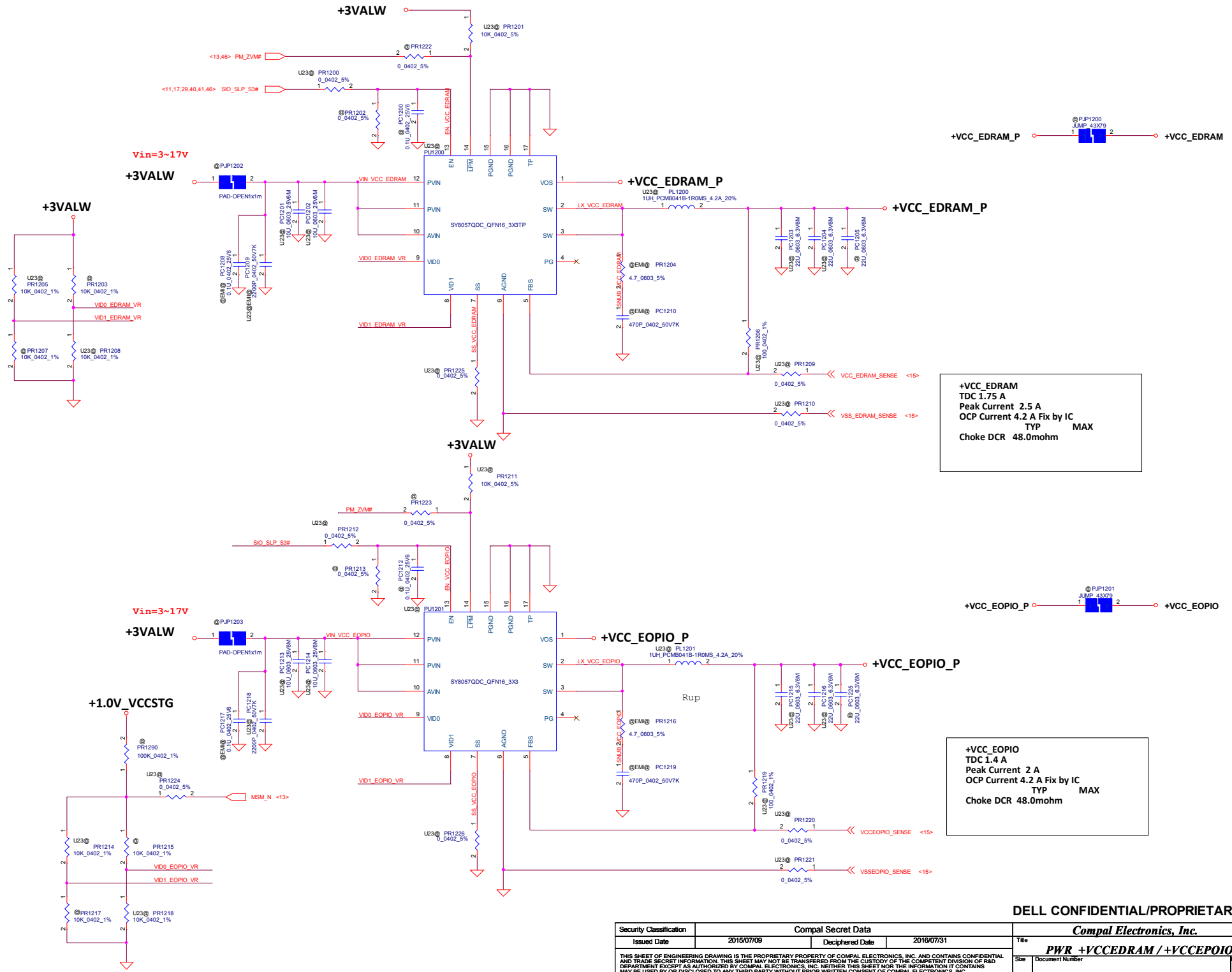
Date: Thursday, July 09, 2015 | Sheet 50 of 64



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Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: PWR +VCCEDRAM / +VCCEPOIO

Size	Document Number	Rev
		1.0(A00)

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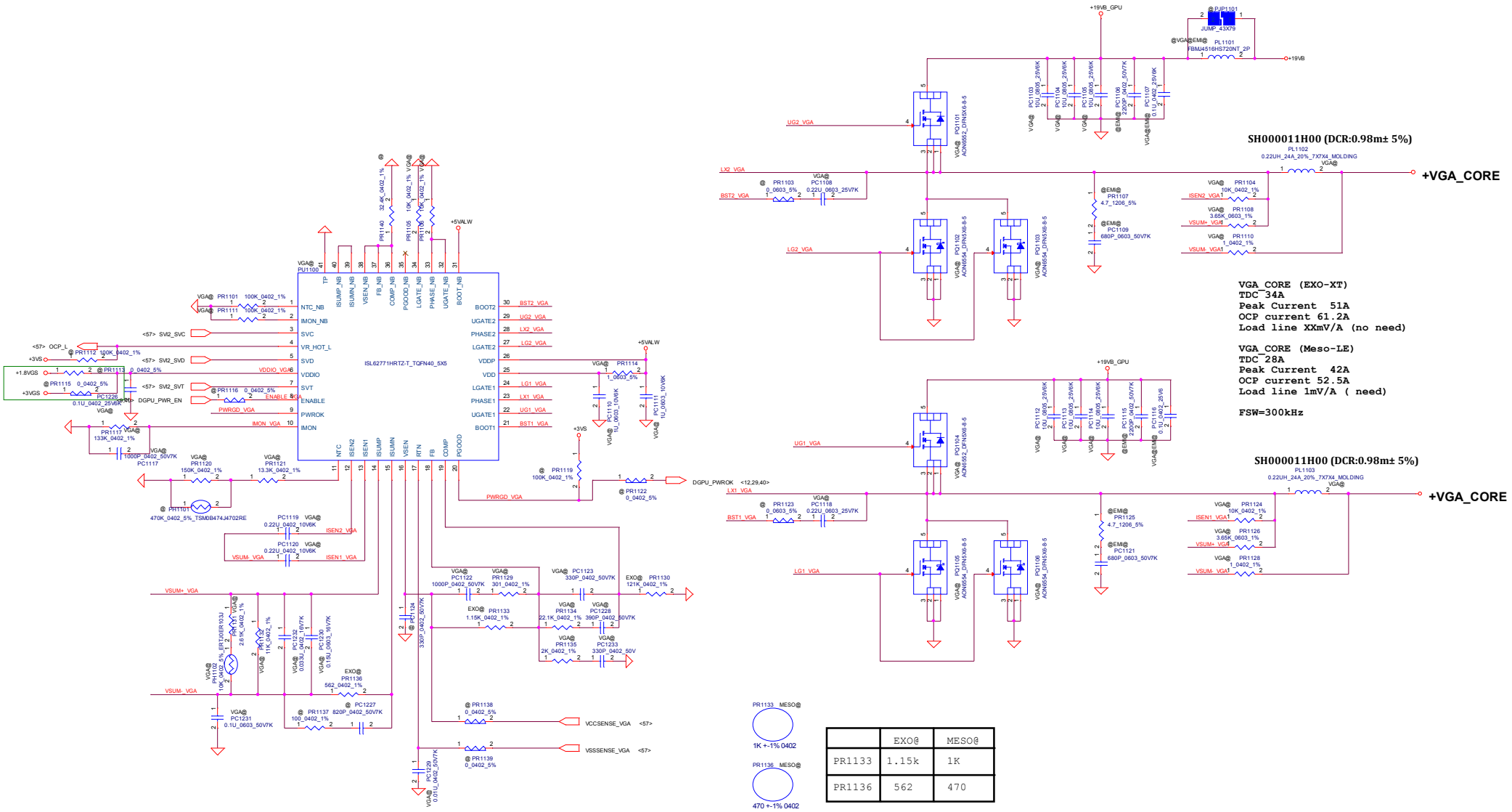

	EXO@	MESO@
PR1133	1.15k	1K
PR1136	562	470

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/07/09	Deciphered Date	2016/07/31
			Title: PWR_VGA_CORE
			Size: Custom; Document Number; Rev: 1.0(A00)
			Date: Thursday, July 09, 2015; Sheet 52 of 64

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	HW or PWR	NA	COMPAL	NA	NA	NA
2				COMPAL			
3				COMPAL			
4				COMPAL			
5				COMPAL			
6				COMPAL			
7				COMPAL			
8				COMPAL			
9				COMPAL			
10				COMPAL			
11				COMPAL			0.2(X01)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Title	PWR_Change list		
Size	Document Number		Rev 1.0(A00)
Date:	Thursday, July 09, 2015	Sheet 53 of 64	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1		HW	20141124	COMPAL	Power sequence	1. Add RC344 for PCH_DPWROK reserved. 2. Add UC13, RC343, RC345, RE429 for IMVP_VR_ON.	0.1(X00)
2		HW	20141124	COMPAL	Debug conn	1. Delete JAPS1, JSPI1	0.1(X00)
3		HW	20141125	COMPAL	Correct XDP conn and GPIO check	1. Change XDP conn 2. Add RE430 for GPIO021 reserve 3. Add RC356, RC357, RC358 for GPIO pull-up 4. Delete RC227, RC290, UC12, RC224	0.1(X00)
4		HW	20141126	COMPAL	Circuit double	1. Delete P32, P33 for double circuit.	0.1(X00)
5		HW	20141128	COMPAL	GPIO modify	1. Add RC360 for PWRGD_VGA 2. Delete RC283, RC174, RC247, R6503, R6504, RC26, RC357, Q2505, R2504 , C620, C621, U74 3. Add D86, Q6204, U5602	0.1(X00)
6		HW	20141203	COMPAL	GPIO modify	1. Add RE437 2. Delete DE6	0.1(X00)
7		HW	20141204	COMPAL	Follow M16 EE implementation guide modify	1. Delete C6203, R6205, R6208, R6217, R6213, Q2602, C2610, R2612, R2602, R2607 2. Add C6214, C6215, R6512, R6514, R6515, RC361	0.1(X00)
8		HW	20141210	COMPAL		1. Add D5503, RE439,	0.1(X00)
9		HW	20141212	COMPAL	PCH Strap modify	1. Add RC365 2. Change VCCIO, EOPIO, EDRAM power enable by S3# 3. Delete RC362, RC363 4. VCCST_PWRGD control by EC	0.1(X00)
10		HW	20141216	COMPAL	1. DDR_VTT_CNTL 2. CODEC 3. LPC connector 4. VCCSTG control	1. Add UC14, CC57, RC123 for DDR_VTT_CNTL buffer 2. Delete RE134 3. Change RE33 to 1K and move to D2701 pin1 4. Change R2717 to 10K 5. Move C2901 to ADD_SENSE_A and change to 0.1uF 6. Move EC2901-EC2904 to R2901-R2904 pin1 7. Move R2819, R2920, EC2905-EC2908 to R2806, R2907, R2909, R2911 pin1 8. Change C2907, C2908 to 10uF/10V/0603 9. Change DB2 location to DB1 10. Add UC15 for VCCSTG control, delete RE73	0.1(X00)
11		HW	20141217	COMPAL	1. SMBus power rail 2. PROCPWRGD 3. USB2_ID 4. CODEC 5. Touch pad 6. VRAM 7. GPU power	1. pop RC15, RC17, de-pop RE426, RE427 2. RC77 de-pop 3. Add RC366 to GND for USB2 OTG setting 4. Change CODEC pin20 from +3VALW to +RTC_CELL 5. Add D83, RE440 for touch pad INT# 6. GPU VRAM bit/Byte swap 7. U5602 IN1/OUT1 swap with IN2/OUT2	0.1(X00)
12		HW	20141218	COMPAL	1. GPU 2. EC 3. CPU 4. DDI to VGA	1. Add RC367, delete RV60, RV254, RV255 for MESO VGA CORE power 2. Add RV260 for GPU_PWR_LEVEL 3. Change VREF_CPU to +1.0V_VCCST 4. Delete RC359, connect VCC_OPC_1P8 to +1.8V_PRIM 5. Change CC283-CC286 pin1 to +1.0V_PRIM 6. Add CC288-CC292 for +VCC_EDRAM 7. Add CC293-CC295 for VDDQ 8. Add CC296 for VDDQC 9. Add CC297 for VDDFLL_OC 10. Change UZ20 VIN from +1.0V_MPHYAON to +1.0V_PRIM 11. Add RC638 for +1.0V_PRIM to +1.0V_MPHYGT 12. Delete R5409 for HDMI power config 13. Change U5502 pin 5, 20 from 3D3V_S0 to +3VS 14. Change HDD_DEVSLP to port 0	0.1(X00)
13		HW	20141219	COMPAL	1. GPU 2. CODEC	1. Add PCIe series caps for SOM control. 2. Swap VRAM bit for layout 3. Change +3V_1.8V_CPVDD to DGND	0.1(X00)
14		HW	20141222	COMPAL	1. Power rail 2. Debug solution	1. Change VGA_CORE to +VGA_CORE 2. Delete PJP702 3. Add R6517, RC369 for debug port 4. Swap RP pin for layout routing smoothly	0.1(X00)
15		HW	20141223	COMPAL	1. Power rail 2. Debug solution	1. Change +1.0VS_VCCSTG to +1.0V_VCCSTG 2. Delete RC369 3. Add R4621, R4622, RC207, R4702, R4703, R4704, R4706, C4701, U4701 , JWRD1 for debug port 4. Change PWR1, TPAD1 connector source 5. Delete LV25, LV26, +VDDCI	0.1(X00)
16		HW	20141224	COMPAL	1. Debug solution	1. Delete R4621, R4622, RC207, R4702, R4703, R4704, R4706, C4701 , U4701, RC207 for debug port 2. Add RC62, RC63 for debug port	0.1(X00)
17		HW	20141226	COMPAL	1. EMI CAP	1. Delete CC284, CC287, CC254 for placement	0.1(X00)
18		HW	20141228	COMPAL	1. GPIO 2. BSIO	1. Change CLK_PCI_LPC_MEC to PCI_CLK_LPC1 2. Delete 94947; Add RS208-RS210 for PANEL_SIZE_ID 3. Add RC369 for SUS_STAT#/LPCPD# 4. Add RC307-RC373 for PROJECT_ID1, PROJECT_ID2 5. Add RC374-RC377 for BOARD_ID2, BOARD_ID3 6. Add RC378-RC381 for VRAM_ID1, VRAM_ID2 7. Swap SIO_EXT_SCI# to GPP_E5 8. Swap BLUETOOTH_EN to GPP_C9 9. Swap I2C_SDA_TP to GPP_C16 10. Swap I2C_SCL_TP to GPP_C17 11. Add RC382 for LPSS UART2_CTS# 12. Swap WLAN_RADIO_DIS# to GPP_D4 13. Add RC383 for DGPU_HOLD_RST# 14. Change RC358 to GND for DGPU_PWR_EN 15. Add R2504, Q2505, RC384 for EC_DET# 16. Swap SIO_EXT_SMI# to GPP_E15 17. Swap SATA_ODD_DA# to GPP_E6 18. Add RC385, RC386 for HDMI_CRT_DET 19. Replace UE1 AC_PRESENT by DGPU_PWROK 20. Add RC387 for SIO_EXT_WAKE# 21. Add D84 for AC_PRESENT 22. Add R5809, Delete RE411 23. Delete RC342 and EC_DPWROK 24. Add RE441 for FAN1_TACH 25. Delete UC13, QE2, RE67, RE68, Add RC389 for ALL_SYS_PWRGD 26. Add UC16, CC298, RC71 for VCCST_PWRGD 27. Delete RS77, RE429, CE83 28. Add RC390 for L_BKLT_EN_EC, delete D5502, R6506 29. Change VREF_CPU connect to +1.0V_PRIM 30. Swap PCIE_WAKE# to GPIO002 31. Swap CLK_PCIE_LAN_REQ# to port2 32. Swap LAN from PCIE port9 to port6 33. Swap USB2 port4 and port8 device (BT and Card Reader)	0.1(X00)
19		HW	20141229	COMPAL	1. GPIO	1. Change UE3 to single channel load switch 2. Add CS801, CS802, CS805, RS809 for WLAN power 3. Add RC391 for EC_WAKE# 4. Add RC391 for ALL_SYS_PWRGD	0.1(X00)
20		HW	20141230	COMPAL	1. GPIO	1. Add Q1901, R1902 for RTCRST_ON	0.1(X00)
21		HW	20150108	COMPAL	1. Change CPU part number 2. Change capacitor part number 3. Change USB Load switch symbol and part number 4.Add CPU dummy symbol, modify PCB dummy symbol	1.Change part number SA01405071 to SA0000BM40L:UC1A-UC1T 2.Change part number SE102104K80 to SE102104K00 : CC214,CC223,CC270, CC281,CC297,CD24,CD25,CD26,CD27,CD32,CD57,CD58,CD59,CD60,CD64,CE34,CE44, CE50,CE78,CE82,CE86,CE85,CE88 3.Add CPU dummy symbol 2.36,2.6G on page1 4.Modify PCB dummy symbol part description to "PCB" 5.Change symbol and part number from SA00007RM00 to SA00007U200 : U3504,U3505	0.1(X00)

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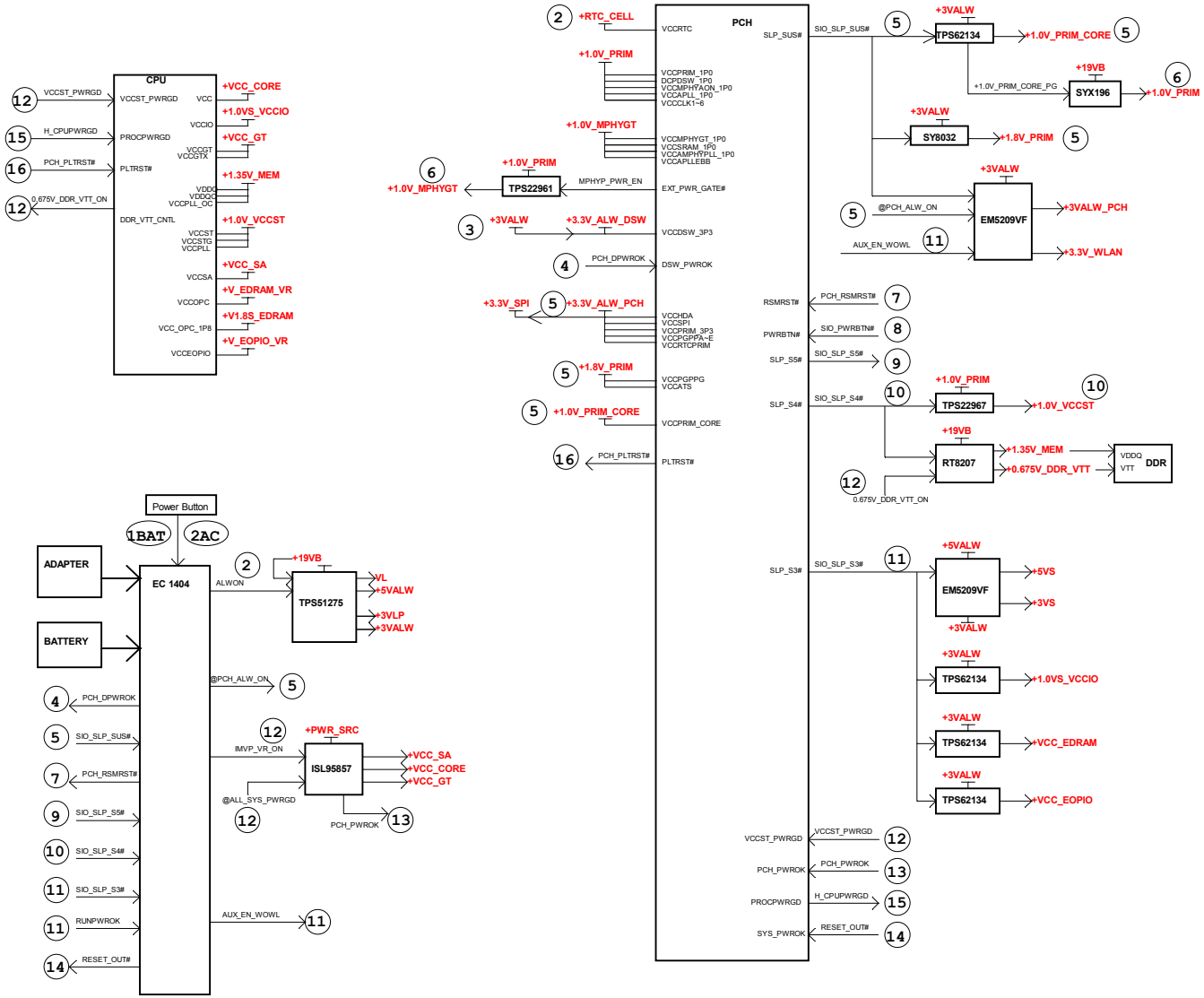
EE_Change list

LA-D971P

Timing Diagram for S5 to S0 mode



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Power Sequence

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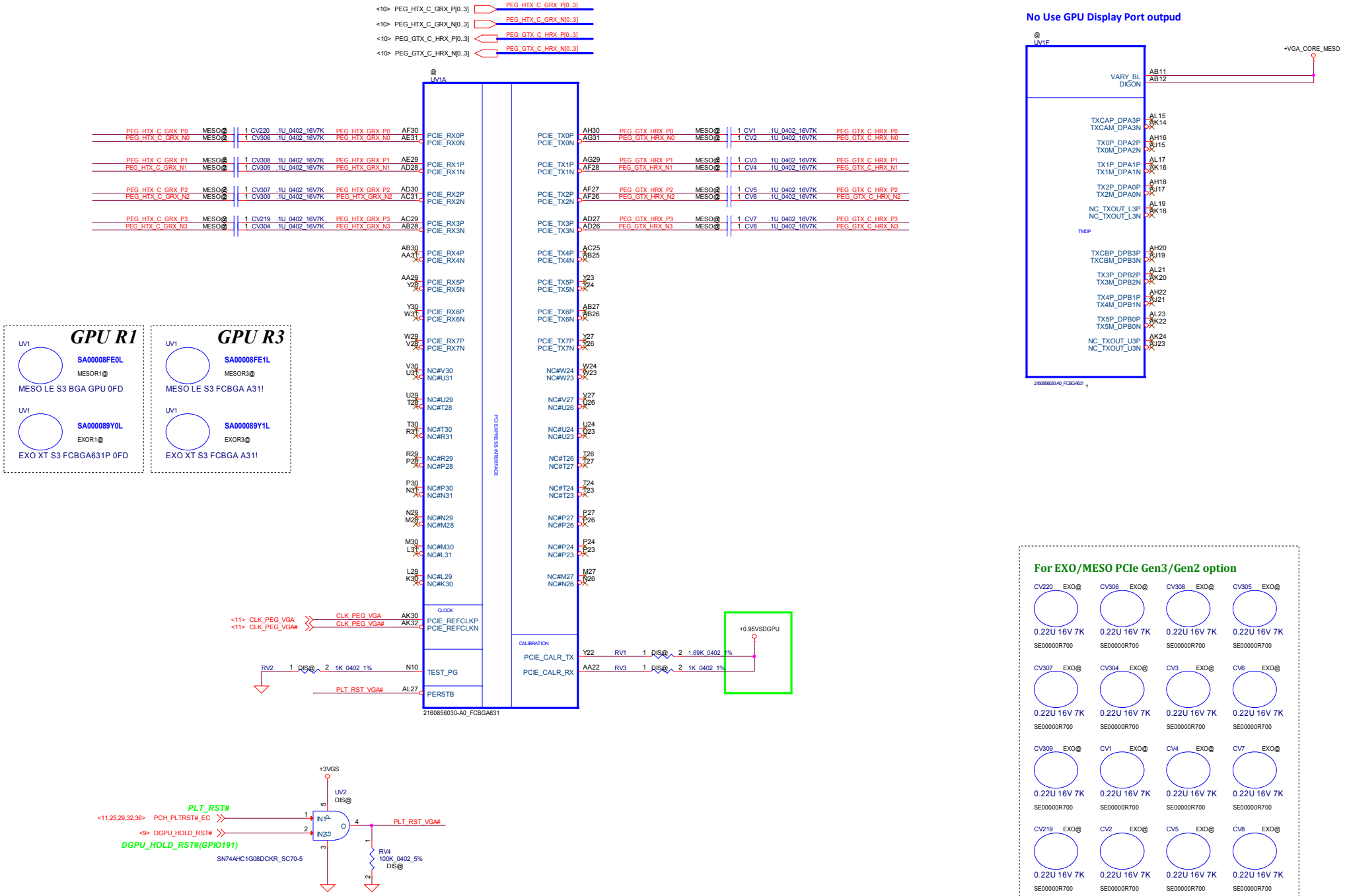
	LA-D071P	1.0A(0S)

Date: Thursday, July 09, 2015 Sheet 55 of 64



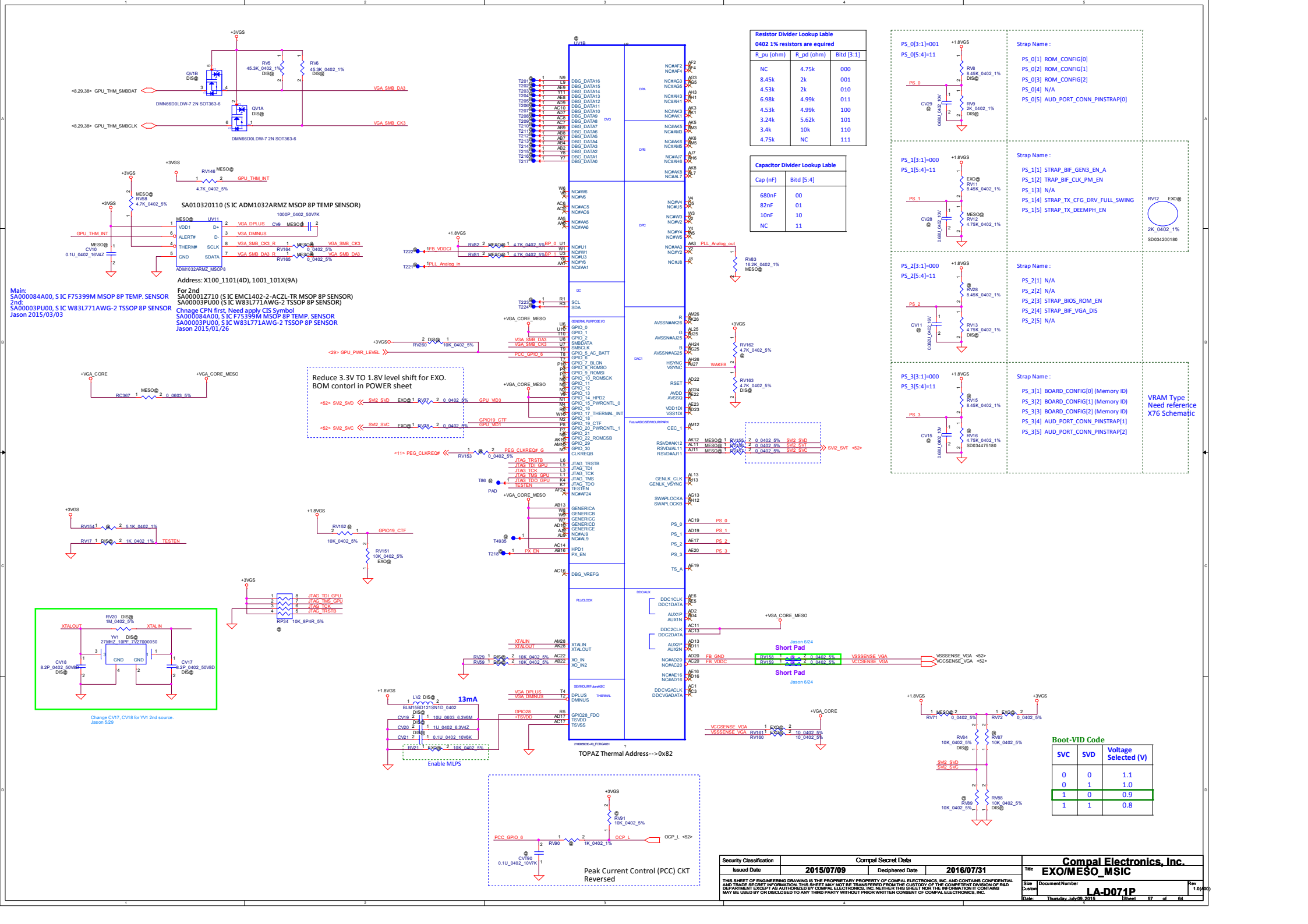
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: EXO/MESO_PCIE/DP

Size: Custom | Document Number: LA-D071P | Rev: 1.0(A00)

Date: Thursday, July 09, 2015 | Sheet 56 of 64


SA010320110 (S IC ADM1032ARMZ MSOP 8P TEMP SENSOR)
Address: X100_1101(4D), 1001_101X(9A)
Main:
SA000084A00, S IC F75399M MSOP 8P TEMP. SENSOR
2nd:
SA00003PU00, S IC W83L771AWG-2 TSSOP 8P SENSOR
Jason 2015/03/03
For 2nd
SA00001Z710 (S IC EMC1402-2-ACZL-TR MSOP 8P SENSOR)
SA00003PU00 (S IC W83L771AWG-2 TSSOP 8P SENSOR)
Chnage CPN first, Need apply CIS Symbol
SA000084A00, S IC F75399M MSOP 8P TEMP. SENSOR
SA00003PU00, S IC W83L771AWG-2 TSSOP 8P SENSOR
Jason 2015/01/26
Reduce 3.3V TO 1.8V level shift for EXO.
BOM contorl in POWER sheet
Change CV17, CV18 for YV1 2nd source.
Jason 5/29
13mA
Enable MLP5
TOPAZ Thermal Address-->0x82
Peak Current Control (PCC) CKT Reversed
Short Pad
Jason 6/24
Short Pad
Jason 6/24
Resistor Divider Lookup Lable
0402 1% resistors are equired
R_pu (ohm) R_pd (ohm) Bitd [3:1]
NC 4.75k 000
8.45k 2k 001
4.53k 2k 010
6.98k 4.99k 011
4.53k 4.99k 100
3.24k 5.62k 101
3.4k 10k 110
4.75k NC 111
Capacitor Divider Lookup Lable
Cap (nF) Bitd [5:4]
680nF 00
82nF 01
10nF 10
NC 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=11
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
VRAM Type
Need refererice
X76 Schematic
Boot-VID Code
SVC SVD Voltage Selected (V)
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
Compal Secret Data
Issued Date 2015/07/09
Deciphered Date 2016/07/31
Security Classification
Compal Electronics, Inc.
EXO/MESO_MSIC
LA-D071P
Rev 1.0(400)
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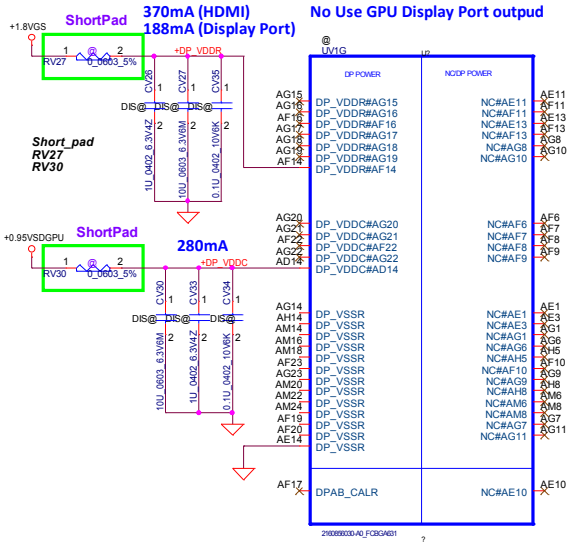
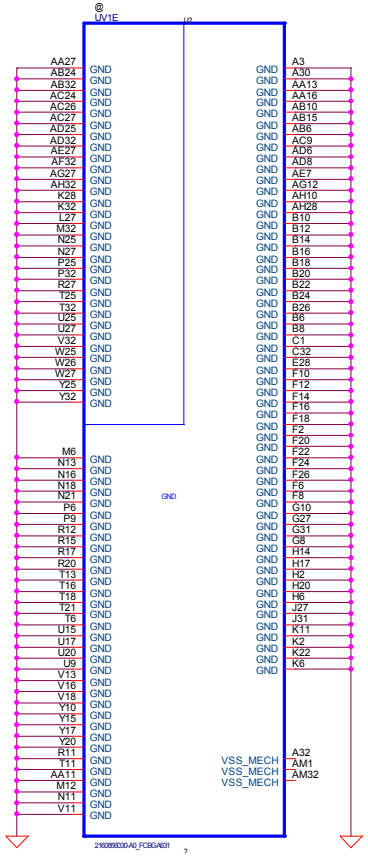
+1.35VS_VGA TO +1.35V_MEM_GFX

JP9 DEFAULT SHORT





Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	EXO/MESO_Power/GND		
Size: Custom	Document Number: LA-D071P		Rev: 1.0(A00)
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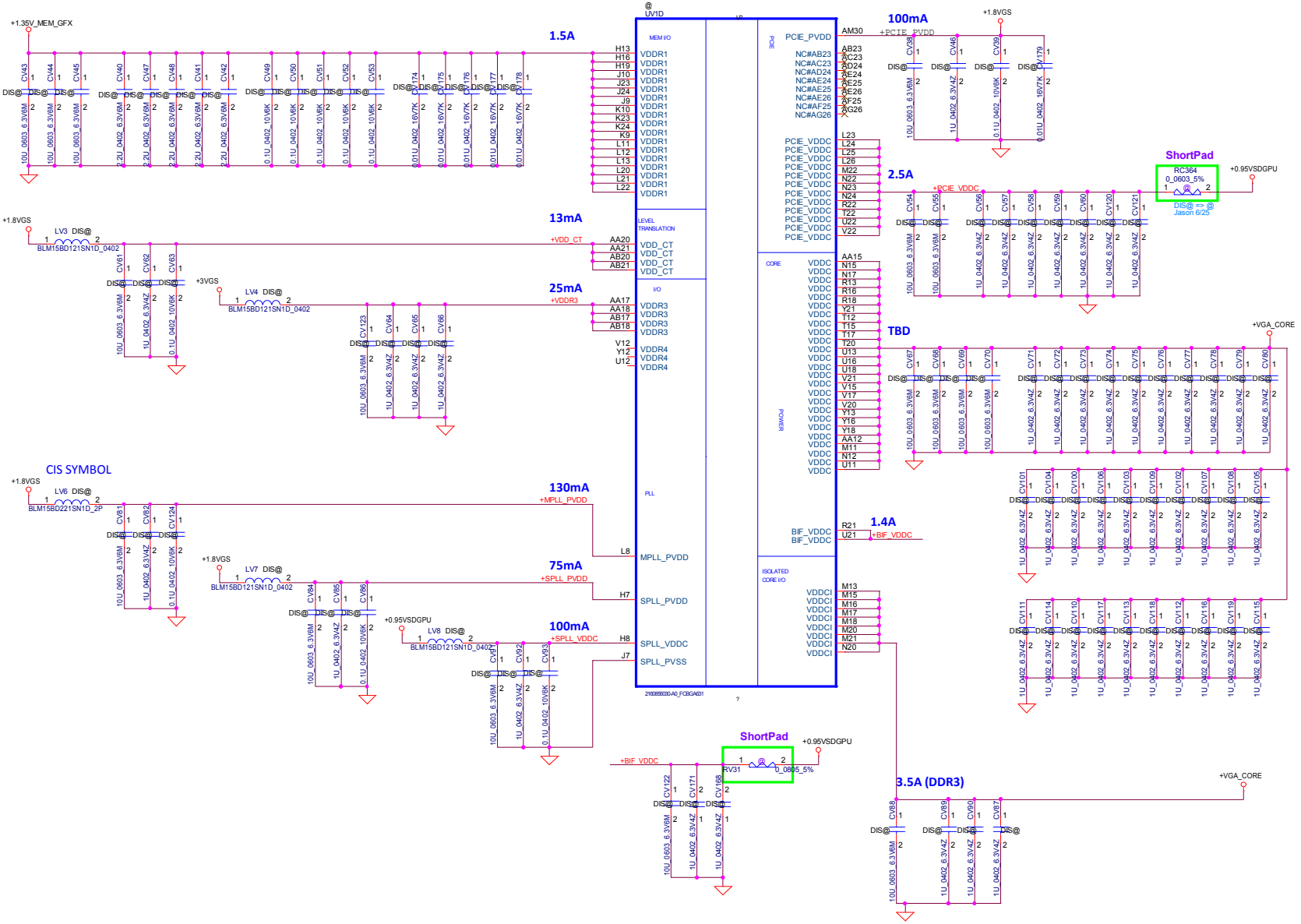
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VSDGPU		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: EXO/MESO_Power

Size: Custom | Document Number: LA-D071P | Rev: 1.0(A00)

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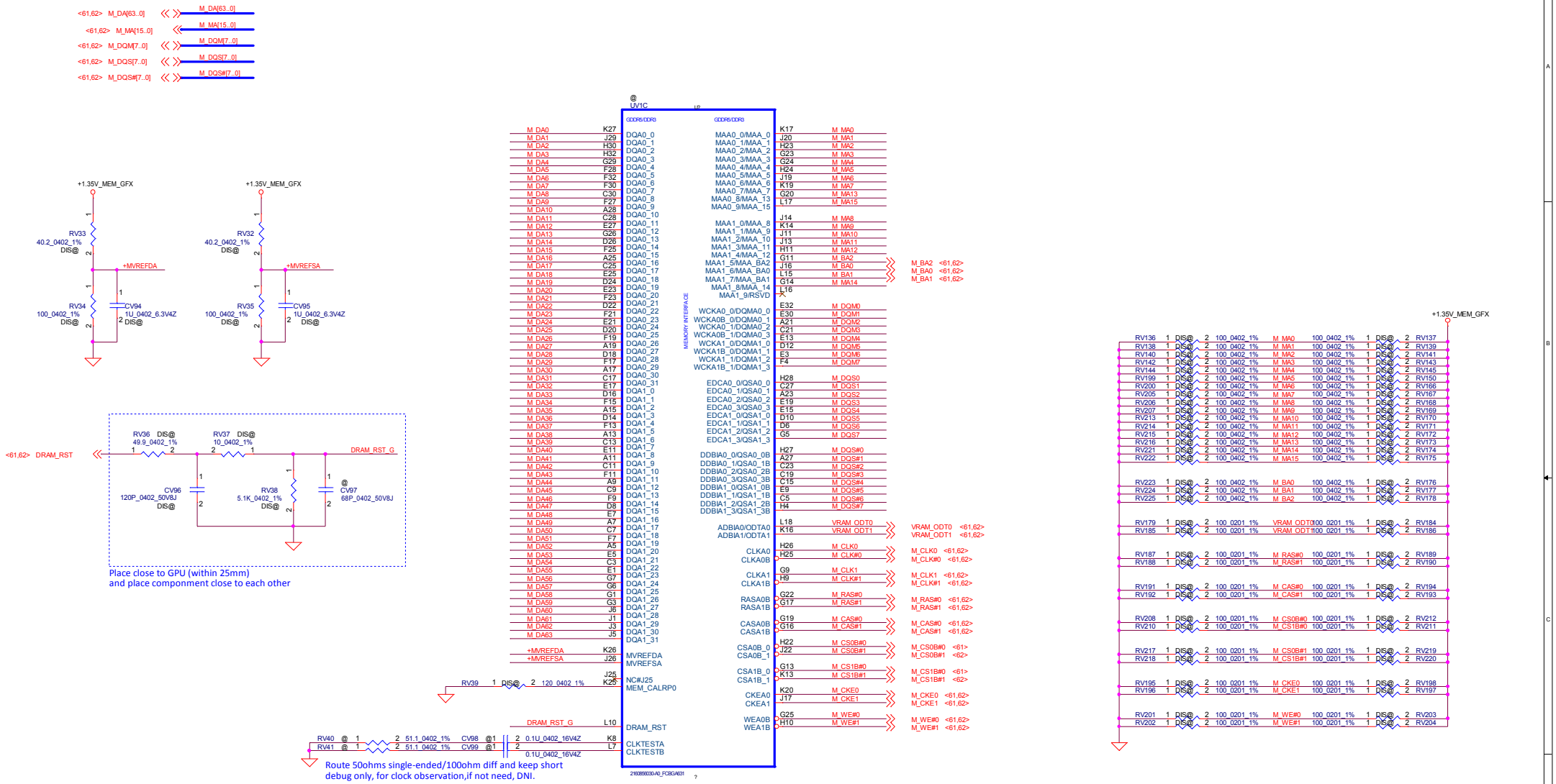

Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation,if not need, DNI.

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: EXO/MESO_MEM

Size: Custom | Document Number: LA-D071P | Rev: 1.0(A00)

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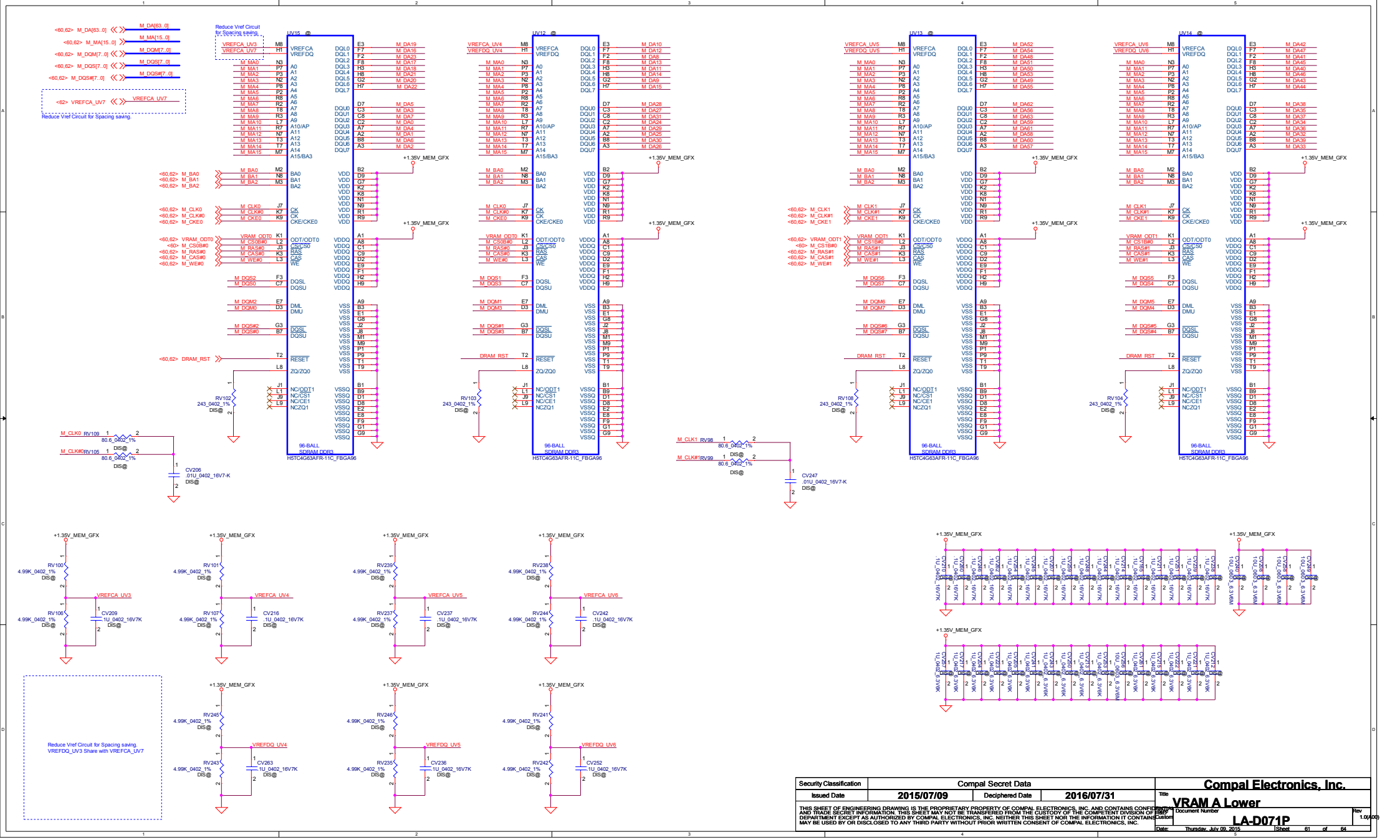

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: VRAM A Lower

Document Number: LA-D071P

Rev: 1.0(A00)

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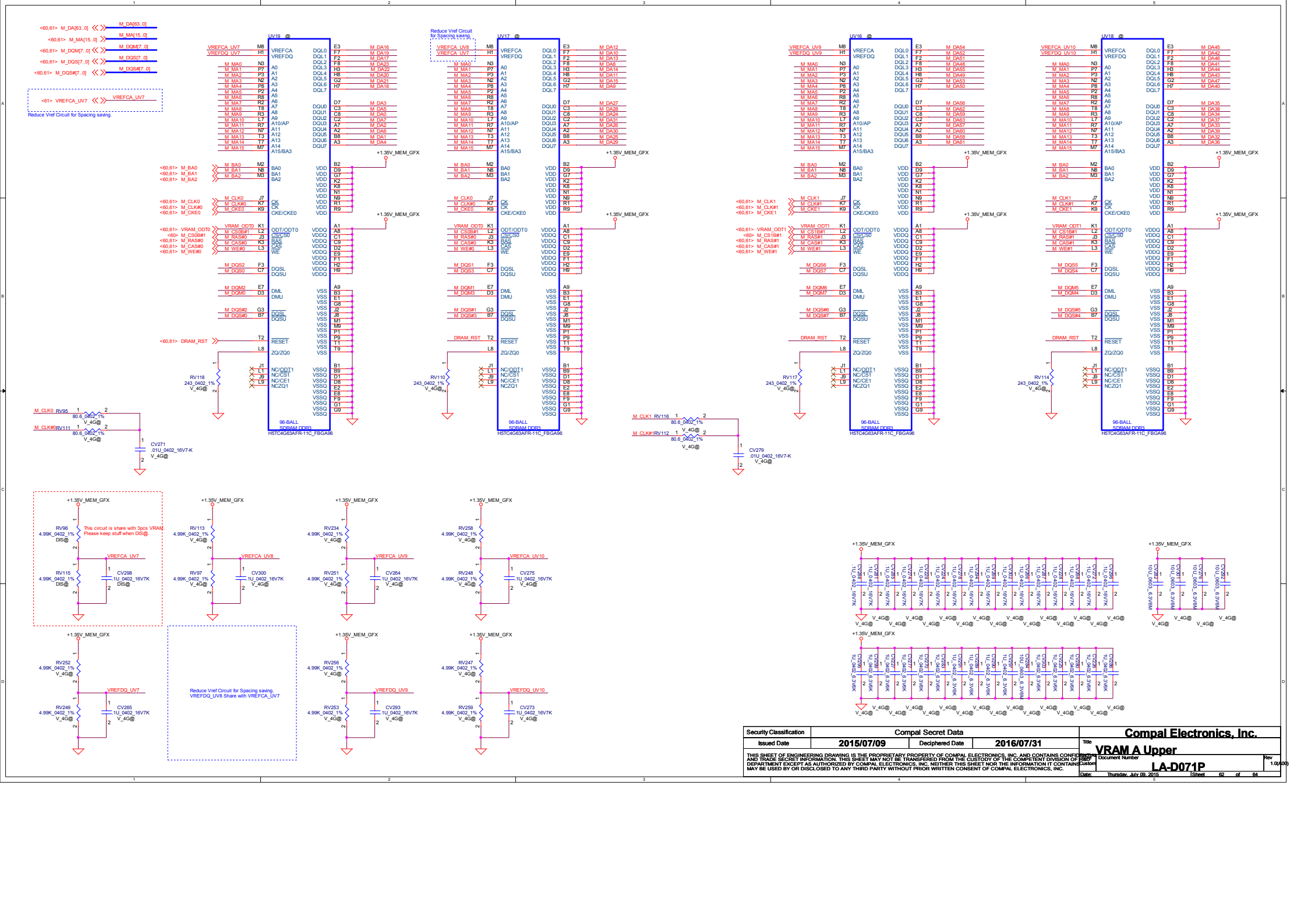

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: VRAM A Upper

Document Number: LA-D071P

Rev: 1.0(A00)

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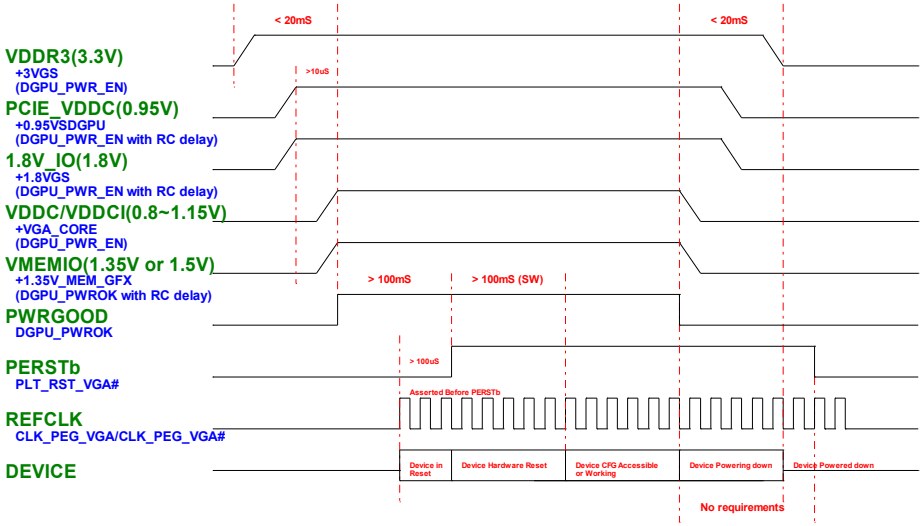
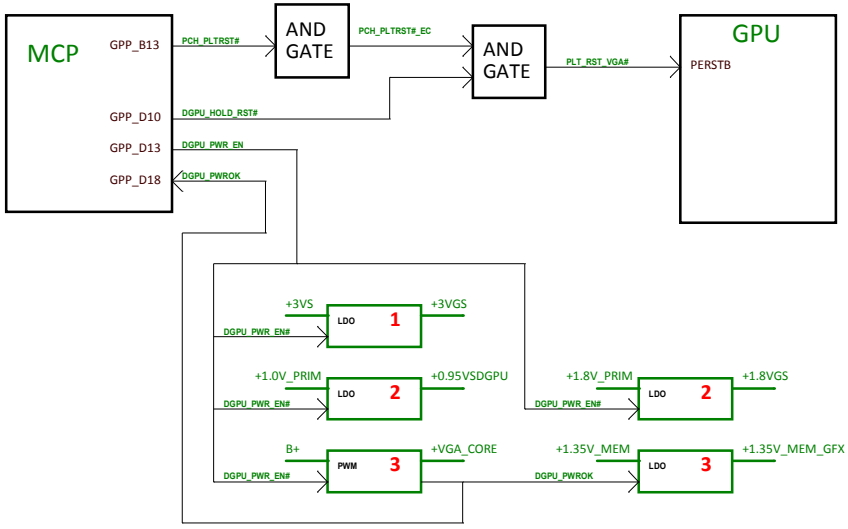
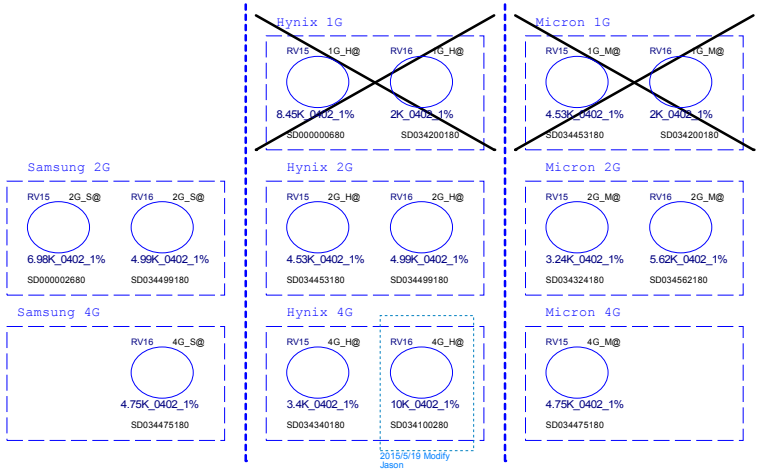
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µs).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.







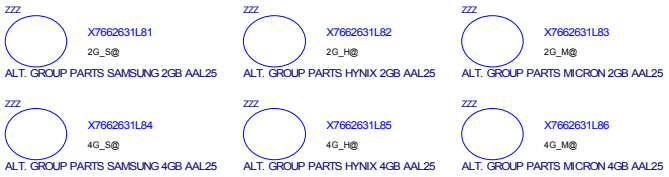


Table 3–21 Resistor Divider Lookup T

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD EXO-XT VRAM Only

Memory ID	P/N	Vendor	Configuration	Size
000	SA000076P2L	SAMSUNG	256MX16 K4W4G1646E-BC1A FBGA 96P	4GB
110	SA00008DN0L	HYNIX	256MX16 H5TC4G63CFR-N0C FBGA 96P	4GB
111	SA000077K0L	Micron	256M16 MT41J256M16HA-093G:E FBGA	4GB
011	SA000076P2L	SAMSUNG	256MX16 K4W4G1646E-BC1A FBGA 96P	2GB
100	SA00008DN0L	HYNIX	256MX16 H5TC4G63CFR-N0C FBGA 96P	2GB
101	SA000077K0L	Micron	256M16 MT41J256M16HA-093G:E FBGA	2GB

For AMD MESO-LE VRAM Only

Memory ID	P/N	Vendor	Configuration	Size
011	SA000076P2L	SAMSUNG	256MX16 K4W4G1646E-BC1A FBGA 96P	2GB
100	SA00008DN0L	HYNIX	256MX16 H5TC4G63CFR-N0C FBGA 96P	2GB
101	SA000077K0L	Micron	256M16 MT41J256M16HA-093G:E FBGA	2GB

Compal Electronics, Inc.

Title: EXO/MESO_NOTE

Size: | Document Number: LA-D071P | Rev: 1.0(A00)

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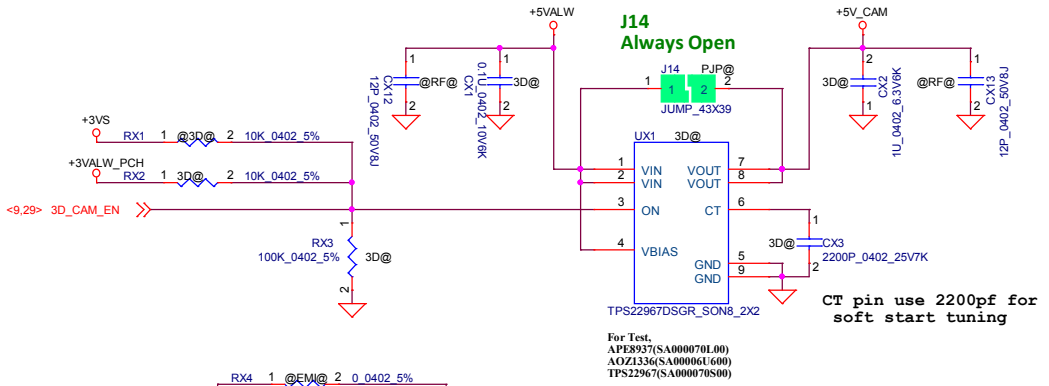
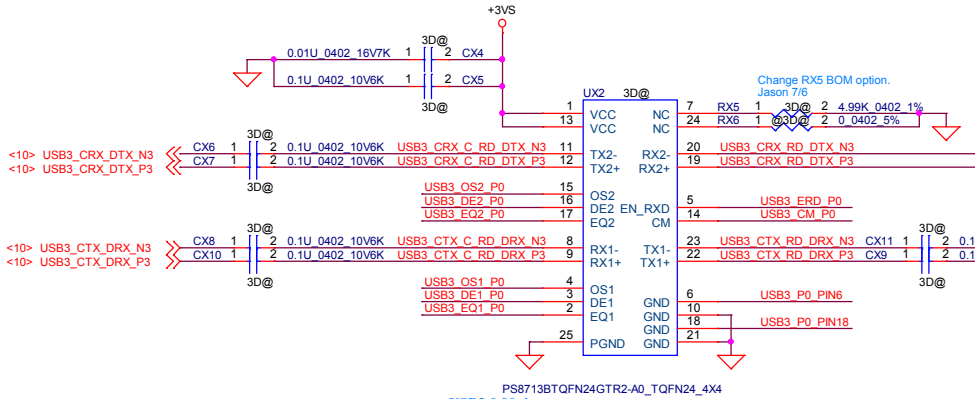
	Vendor	PS8713B	TI	Spec			schematic netname	3Vs		GND	
1	VDD	VCC	Same								
2	B_EQ0	EQ1	**LL:** 9.5dB (default)	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_EQ1_P0	RI23	@	RI32	@
3	DE0	DE1	LL: 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE1_P0	RI26	@	RI35	@
4	EQ1	OS1	**LL:** 9.5dB	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_OS1_P0	RI22	@	RI40	@
5	PD#	EN_RXD	it can be left open				USB3_ERD_P0	RI44	@	RI48	@
6	B_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN6	RI53	@	RI49	@
7	REXT	NC		4.99K						RI56	4.99K
8	B_Inn	RX1-	Same								
9	B_Inp	RX1+	Same								
10	GND	GND	Same								
11	A_OUTn	TX2-	Same								
12	A_OUTp	TX2+	Same								
13	VDD	VCC	Same								
14	TST/NC	CM	4.7K ohm resistor for perfomance adjustment				USB3_CM_P0	RI42	@	RI46	@
15	A_EQ1	OS2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_OS2_P0	RI19	@	RI87	@
16	A_DE0	DE2	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE2_P0	RI20	@	RI31	@
17	A_EQ0	EQ2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_EQ2_P0	RI21	@	RI36	@
18	A_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN18	RI52	@	RI50	@
19	A_Inp	RX2+	Same								
20	A_Inn	RX2-	Same								
21	GND	GND	Same								
22	B_OUTp	TX1+	Same								
23	B_OUTn	TX1-	Same								
24	I2C_EN	NC	this pin canbe NC or connected to GND				NC			RI57	@

+5VALW TO +5V_3DCAM

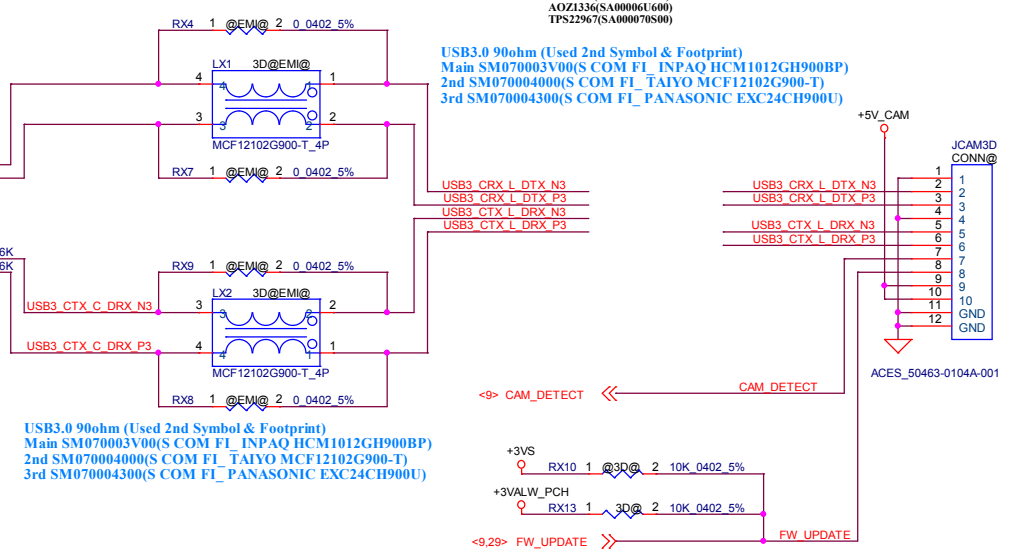


For Test,
APE5937(SA000070L00)
AOZ1336(SA00006U600)
TPS22967(SA000070S00)

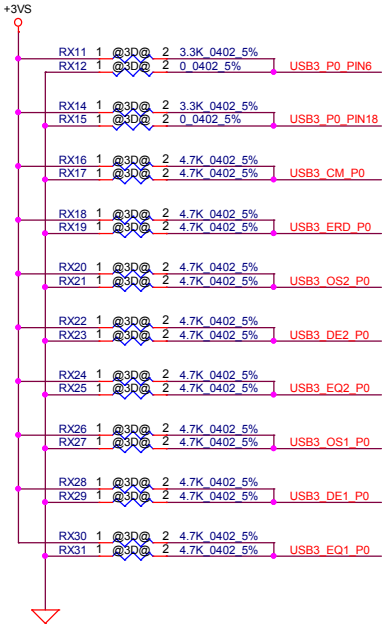


USB3.0 90ohm
Main SA00005OR20 (S IC PS8713BTQFN24GTR2-A1 TQFN USB3.0) PARADE
2nd SA00008M500 (S IC SN65LVPE512RGER VQFN 24P USB3 REDRI) TI

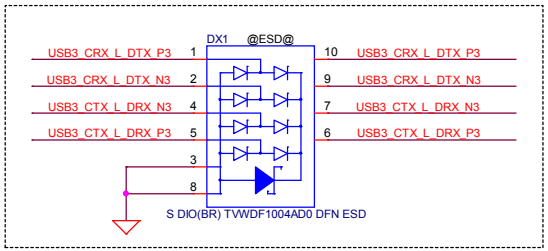
Change Main source CPN to
SA00005OR30 (S IC PS8713BTQFN24GTR2-A2 USB3.0 REPEATE) PARADE
Because Vendor Ver. change. Jason 2015/5/29



USB3.0 90ohm (Used 2nd Symbol & Footprint)
Main SM070003V00(S COM FI_INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_PANASONIC EXC24CH900U)



Layout request to swap pin !



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