


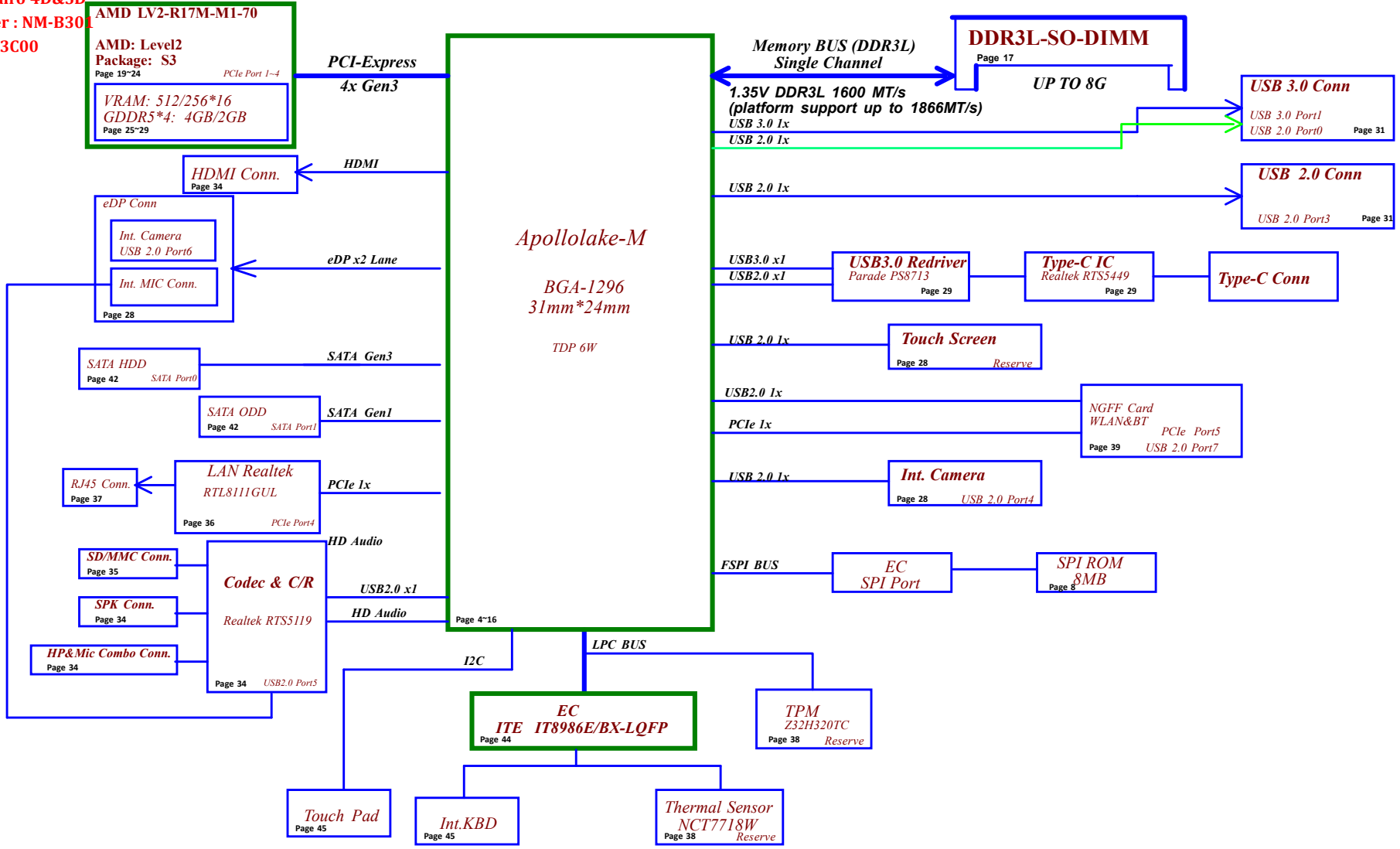
# LCFC Confidential

## APL G 320 M/B DG424/DG524 Schematics Document Intel Apollolake M-Processor with DDRIII L + NV(AMD LV2-R17M-M1-70) GPU

2017-02-28

REV: 1.0

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2013/08/08	Deciphered Date	2014/01/21	<b>Cover Page</b>			
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					C	DG424/DG524	1.0
					Date:	Thursday, March 09, 2017	Sheet 1 of 58



Power Plane / State	V20B+ +3VL +5VL	+3VALW +5VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.35V	+5VS +3VS +1.8VS +1.05VS VTT +CPU_CORE +VNN
S0	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
SOIX(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	Type C
	1	USB3.0
USB 2.0	0	Type C (USB 2.0)
	1	USB3.0 (2.0)
	2	Touch Screen
	3	USB2.0
	4	Finger Print
	5	CARD READER
	6	CAMERA
7	BT	

PCIe PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0	dGPU	PCIe1(Func0):Root Port#3	CLKREQ0
1			
2			
3	LAN	PCIe0(Func0):Root Port#1	CLKREQ1
4			
5	WLAN	PCIe0(Func1):Root Port#2	CLKREQ2

BOM Structure Table

BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
EMC_14@	EMC 14" part
EMC_USB@	EMC USB TVS part
CD@	Cost Down part
RF@	For RF part
RF_NS@	For RF un-stuff part
RF_PXNS@	For RF GPU un-stuff part
14@	For 14" part
15@	For 15" part
8111GUL@	8111GUL LAN SKU part@
8111H@	8111H LAN SKU part@
PX@	Discrete GPU SKU part
TOPAZ@	TOPAZ dGPU SKU part
EXO@	R16M-M1-30 dGPU SKU part
UMA@	UMA SKU ID part
TMSEN@	Thermal Sensor part
TMSEN_PX@	dGPU Thermal Sensor part
TMSEN_UMA@	UMA Thermal Sensor part
TPM@	TPM part
NOVOTON@	NOVOTON TPM part
NATIONZ@	NATIONZ TPM part
TS@	Touch Screen part
FP@	Finger Print part
KBL@	KB Backlight part
UART@	UART debug part
RTCST@	Clear RTCST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N3350_B0@	Apollolake N3350 B0 stepping QS CPU part
N3450_B0@	Apollolake N3450 B0 stepping QS CPU part
N4200_B0@	Apollolake N4200 B0 stepping QS CPU part
N3350_B1@	Apollolake N3350 B1 stepping MP CPU part
N3450_B1@	Apollolake N3450 B1 stepping MP CPU part
N4200_B1@	Apollolake N4200 B1 stepping MP CPU part
M2GX4@	Micron 2GB(256x16x4) VRAM X76 SKU
S2GX4@	Samsung 2GB(256x16x4) VRAM X76 SKU
H2GX4@	Hynix 2GB(256x16x4) VRAM X76 SKU
M2G@	Micron 2GB VRAM
S2G@	Samsung 2GB VRAM
H2G@	Hynix 2GB VRAM
PCB@	PCB part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

DDI PORT LIST

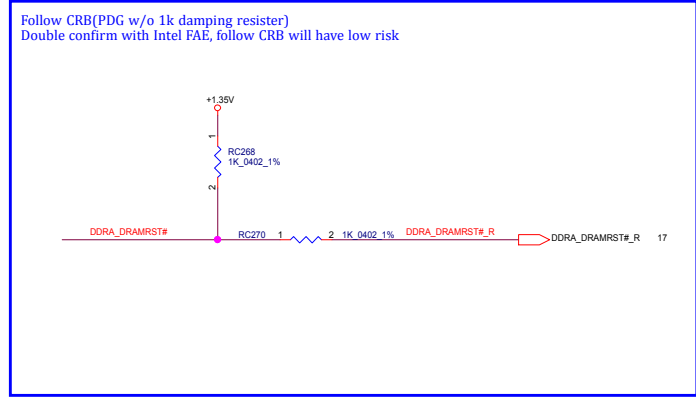
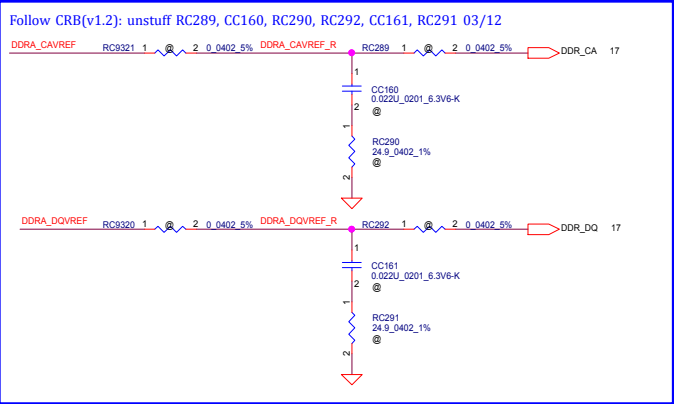
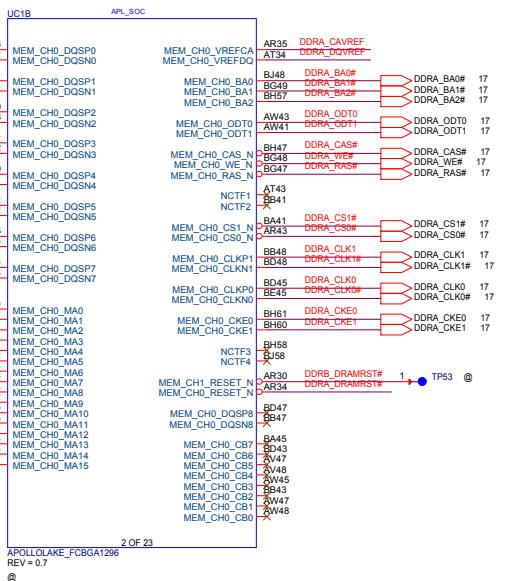
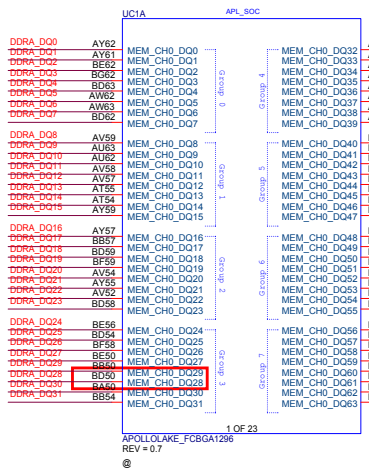
Port	Device
DDI0	NC
DDI1	HDMI
eDP	eDP

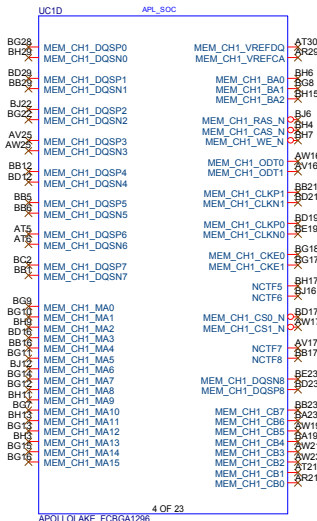
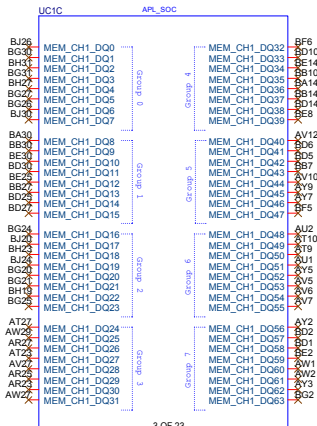
EC SM Bus0 address		EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
PMIC	0x68	Smart Battery	0x16	Thermal Sensor	0x98(reserve)	DDR SO-DIMM	0xA0
		Charger	0x12			Wlan	Rsvd

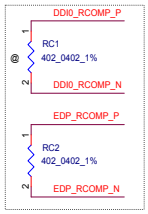
I2C4 Bus address (Touch Pad)

Device	Address
Slave	0x15
Descriptor	0x0001

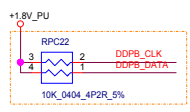
- DDRA\_DQ[63:0] 17
- DDRA\_MA[15:0] 17
- DDRA\_DQS[7:0] 17
- DDRA\_DQS#[7:0] 17



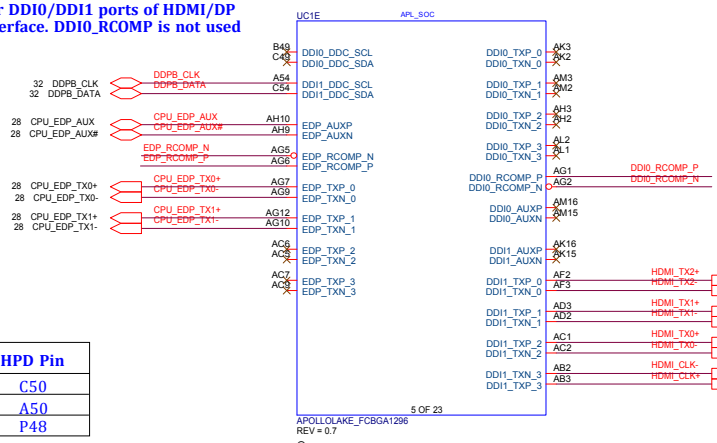




eDP RCOMP is used for DDIO/DDI1 ports of HDMI/DP as well as the eDP interface. DDIO\_RCOMP is not used



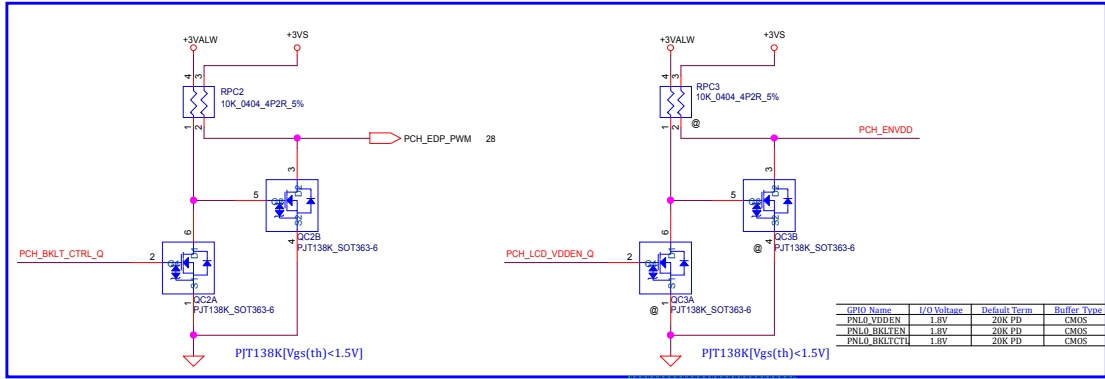
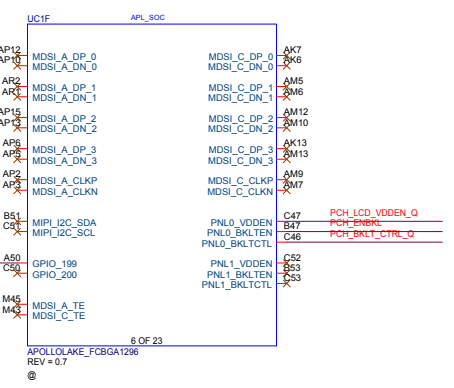
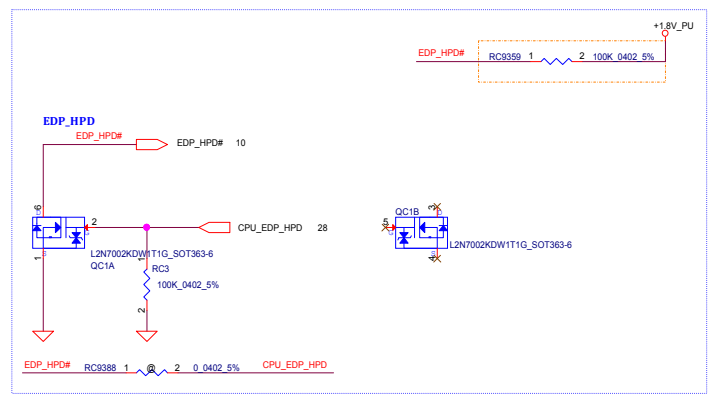
eDP



HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

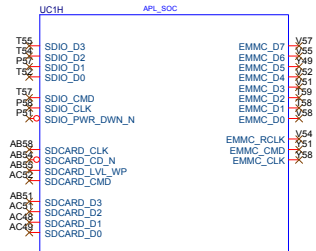
**DDI PORT LIST**

Port	Device	HPD Net	HPD Pin
DDIO	DP TO VGA	VGA_HPD#	C50
DDI1	HDMI	HDMI_HPD#	A50
EDP	eDP	EDP_HPD#	P48

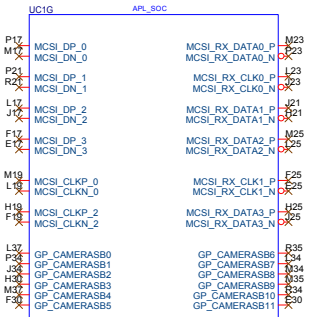


GPIO Name	I/O Voltage	Default Term	Buffer Type
PNL0_VDDEN	1.8V	20K PD	CMOS
PNL0_BKLTEN	1.8V	20K PD	CMOS
PNL0_BKLTCTL	1.8V	20K PD	CMOS

PCH\_LCD\_VDDEN\_Q VOH min is 1.35V, SY6288C20 VIH min is 1.35V, do NOT use level shift (Follow BMWC1)  
PCH\_ENBKL can direct connect to EC for costdown

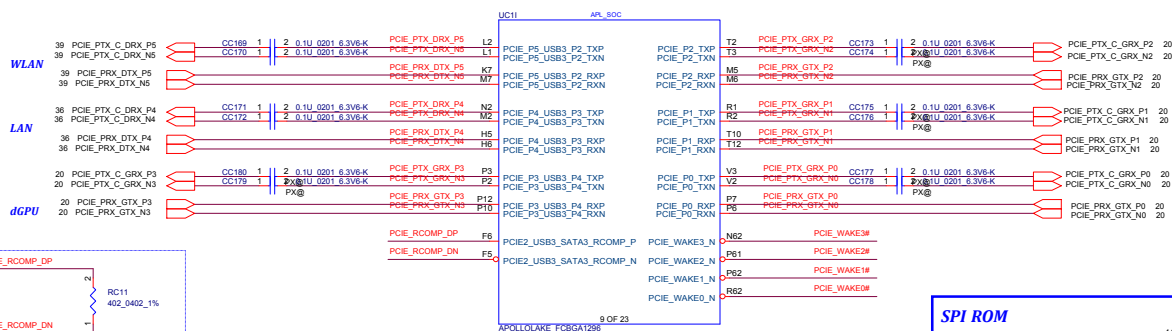


8 OF 23  
 APOLLOLAKE\_FCBGA1296  
 REV = 0.7  
 ©

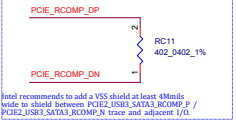
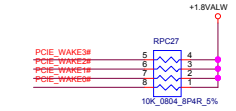


7 OF 23  
 APOLLOLAKE\_FCBGA1296  
 REV = 0.7  
 ©

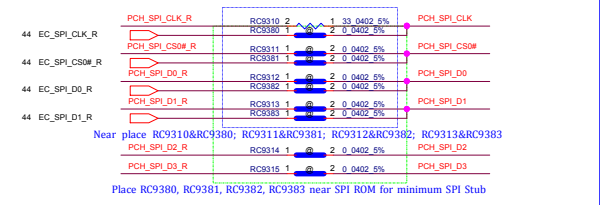
PCIe Configuration			
Port	Config	Device	BIOS Device ID Map
P0	X4	dGPU	PCIe1(Func0):Root Port#3
P1			
P2			
P3	X1	LAN	PCIe0(Func0):Root Port#1
P4			
P5			



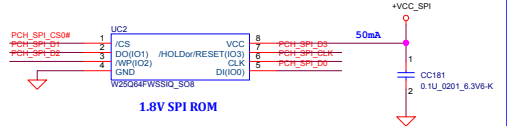
dGPU



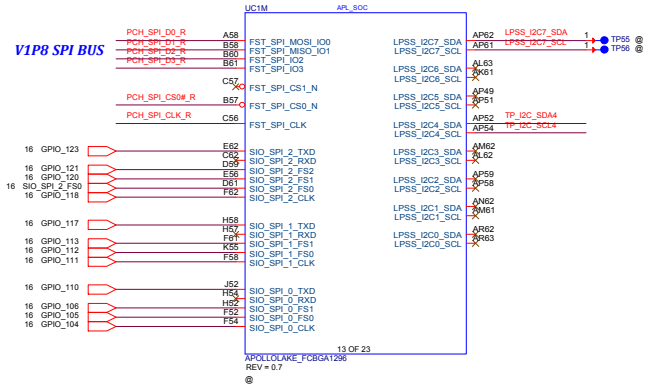
### SPI ROM



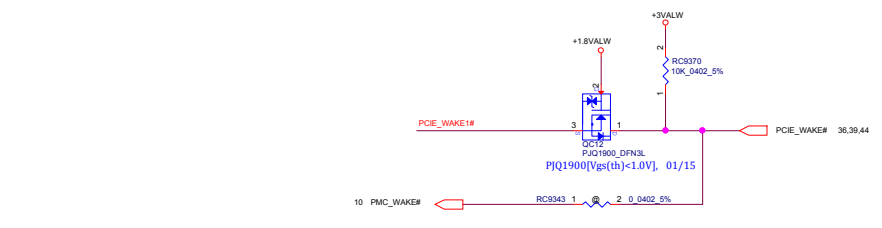
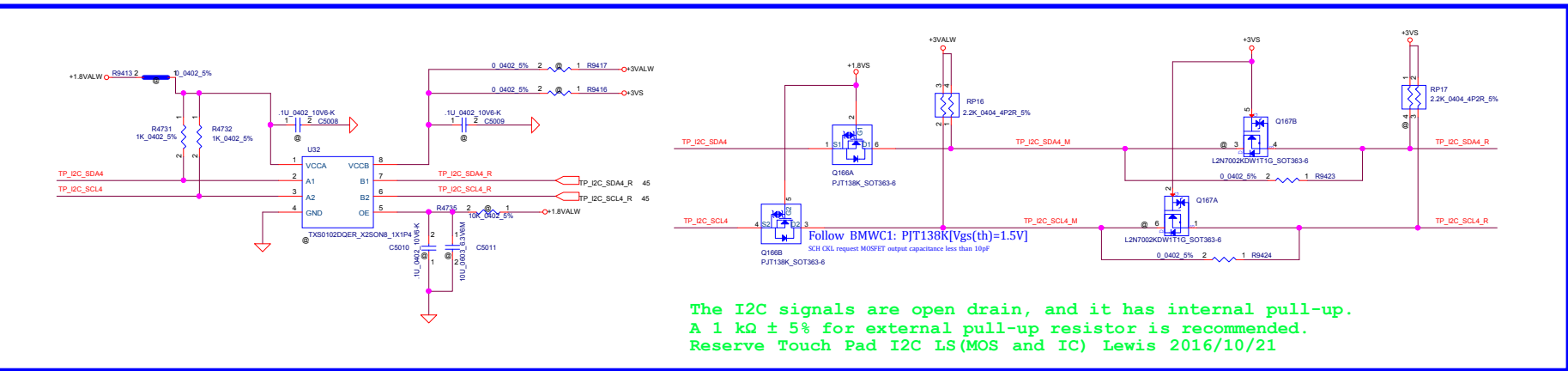
Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
FST_SPL_CS0_B	PCH_SPL_CS0#	1.8V	20K PU	CMOS
FST_SPL_MOSI_I00	PCH_SPL_D0	1.8V	20K PD	CMOS
FST_SPL_MISO_I01	PCH_SPL_D1	1.8V	20K PU	CMOS
FST_SPL_I02	PCH_SPL_D2	1.8V	20K PU	CMOS
FST_SPL_I03	PCH_SPL_D3	1.8V	20K PU	CMOS
FST_SPL_CLK	PCH_SPL_CLK	1.8V	20K PD	CMOS



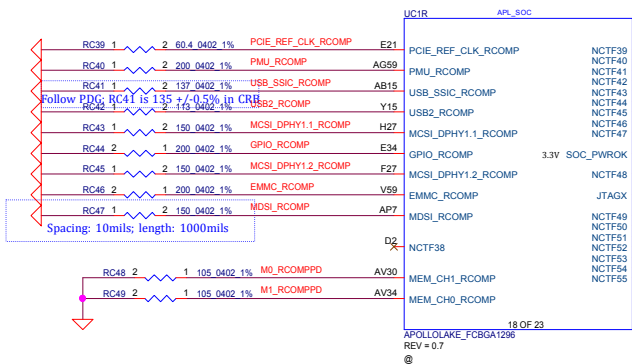
### VIPB SPI BUS



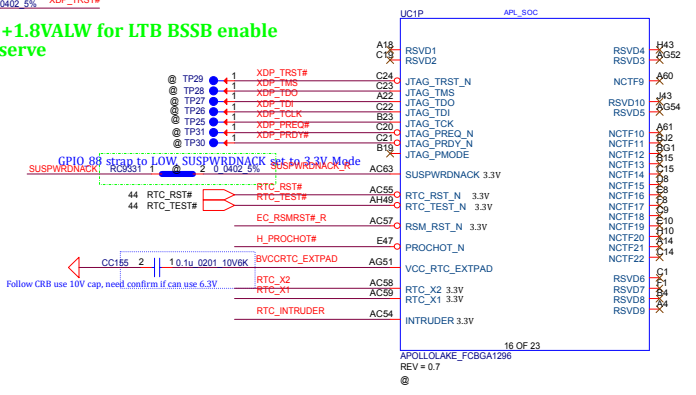
The I2C signals are open drain, and it has internal pull-up. A 1 kΩ ± 5% for external pull-up resistor is recommended. Reserve Touch Pad I2C LS(MOS and IC) Lewis 2016/10/21





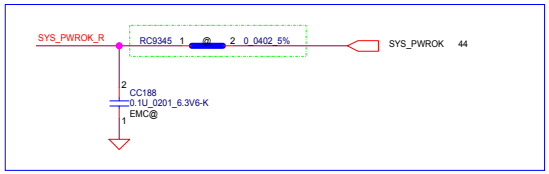
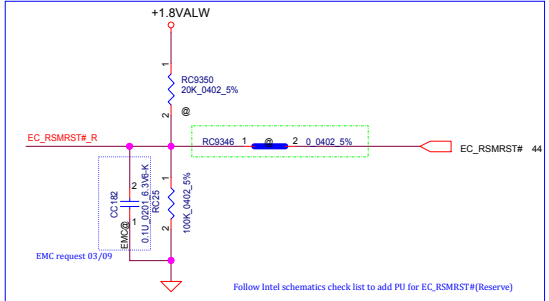
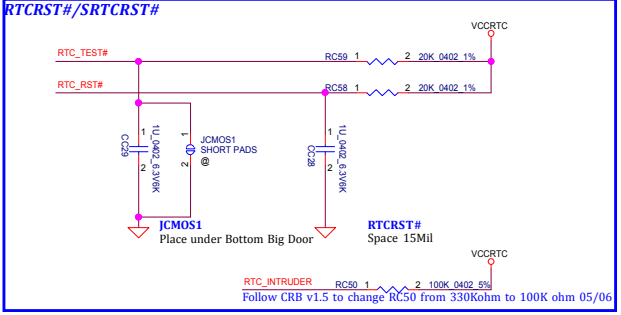
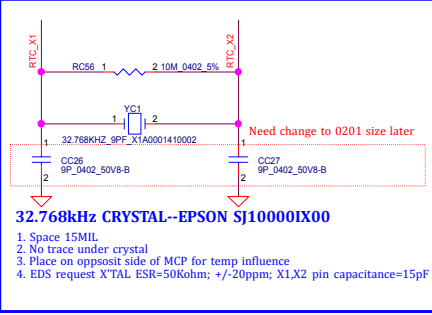


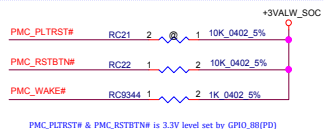
+1.8VALW  
 RM115.1 @ 2 10 0402 5% XDP\_TRST#  
**use 10ohm pull up to +1.8VALW for LTB BSSB enable lewis 2016/10/21 reserve**



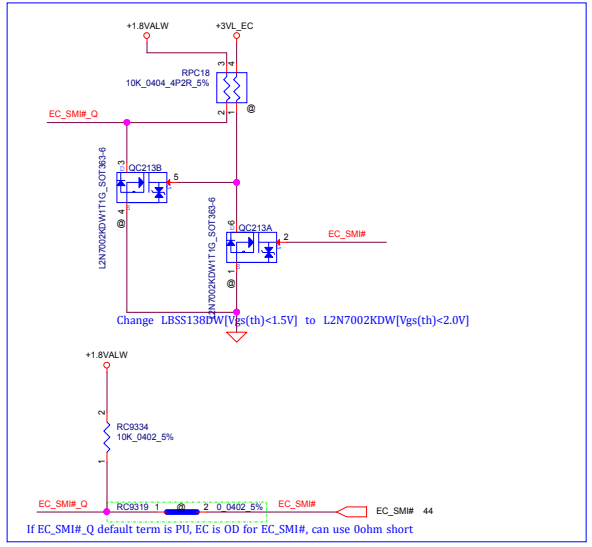
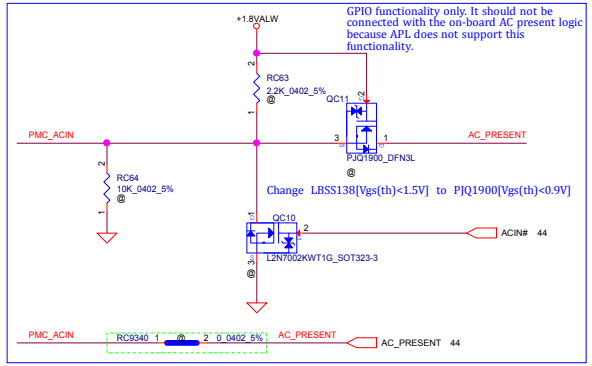
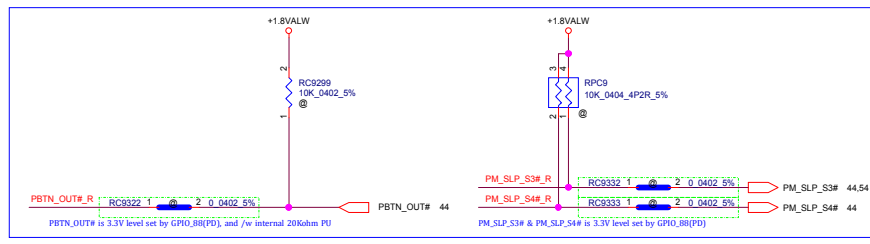
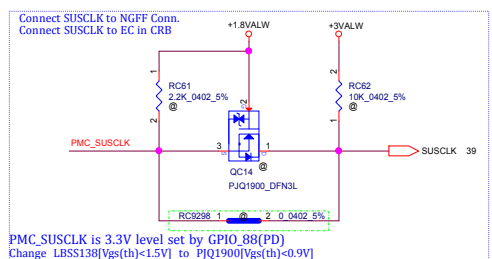
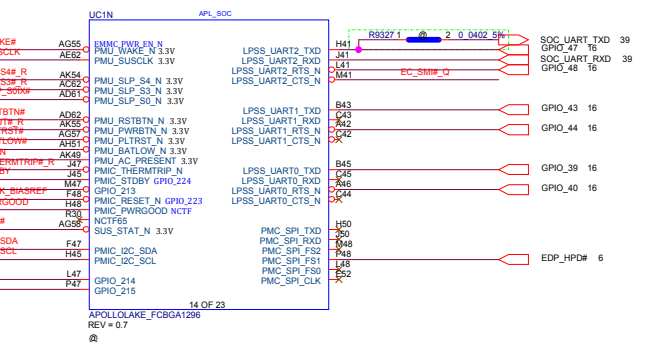
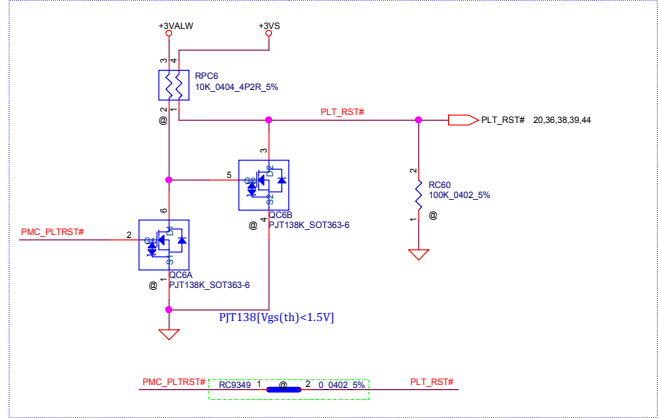
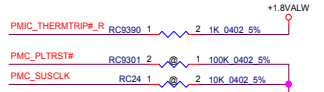
**RCOMP RESISTOR REQUIREMENT**

INTERFACE	PIN NAME	LOCATION	VALUE(ohm)
CSI1.1	MCSI_DPHY1.1_RCOMP	RC43	150 +/-1%
CSI 1.2 (DPHY/CPHY)	MCSI_DPHY1.2_RCOMP	RC45	150 +/-1%
USB2 and 3.3V mode GPIO	USB2_RCOMP	RC42	113 +/-1%
PCIe Refclk	PCIE_REF_CLK_RCOMP	RC39	60.4 +/-1%
modPHY (PCIe, USB3, SATA)	PCIE2_USB3_SATA3_RCOMP_P/N	RC11	402 +/-1%
MDSI	MDSI_RCOMP	RC47	150 +/-1%
SSIC	USB_SSIC_RCOMP	RC41	137 +/-1%
EMMC, Legacy and GPIO signals including 1.8V mode SD Card, PMU, LPC, SMBUS.	EMMC_RCOMP	RC46	200 +/-1%
	GPIO_RCOMP	RC44	200 +/-1%
	PMU_RCOMP	RC40	200 +/-1%
eDP	EDP_RCOMP_P/N	RC2	402 +/-1%
DDI	DDIO_RCOMP_P/N	RC1	402 +/-1%
Memory	MEM_CH0_RCOMP/MEM_CH1_RCOMP	RC49 RC48	105 +/-1%





follow CRB reserve PU for PMC\_RESET#  
 PMC\_RESET# is 1.8V voltage, need double check  
 SKL\_XCLK\_BIASREF

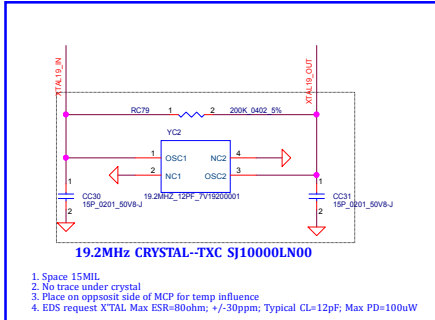
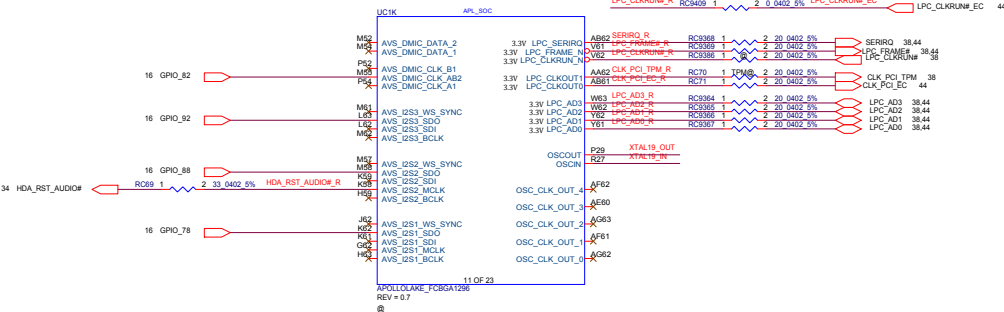
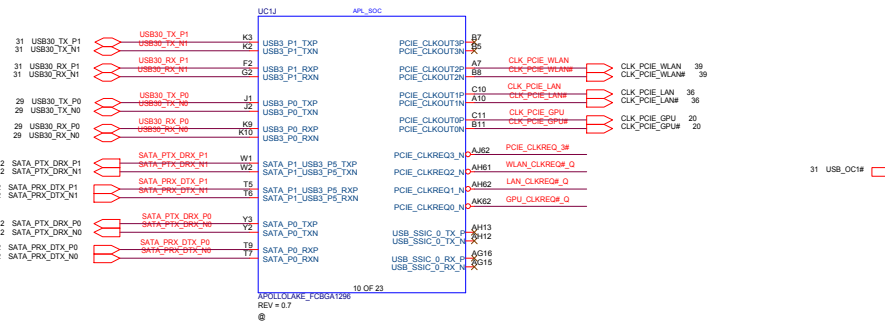


**USB (3.0)**

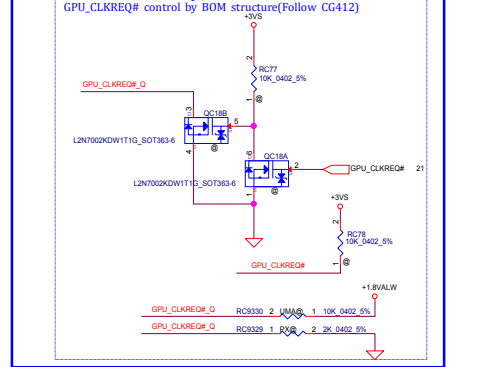
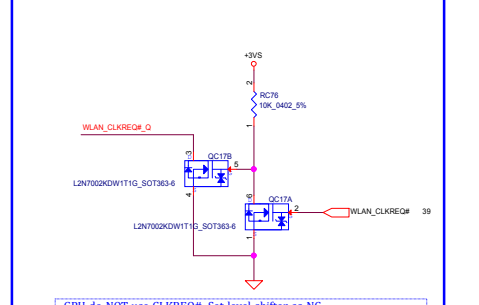
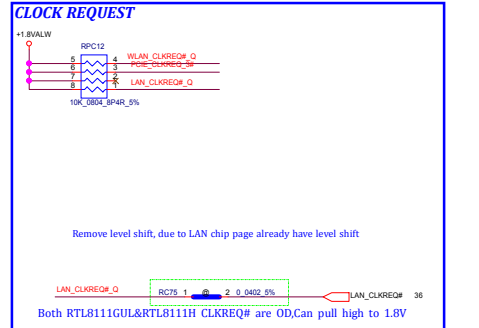
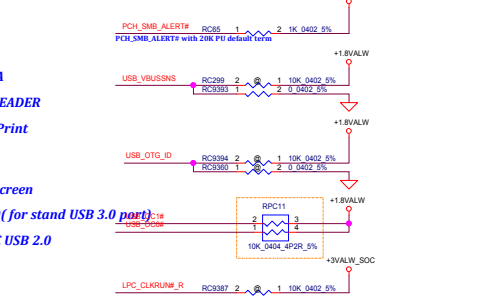
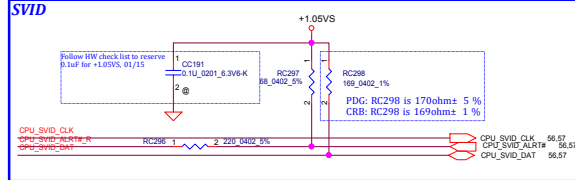
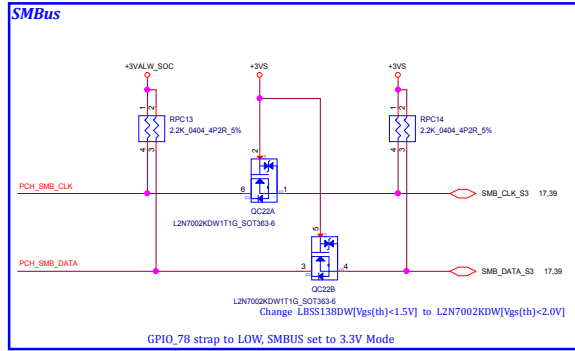
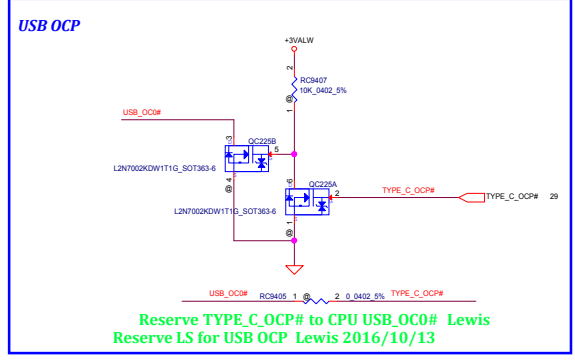
**Type C**

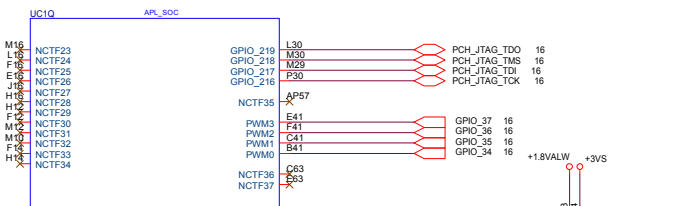
**ODD**

**HDD**

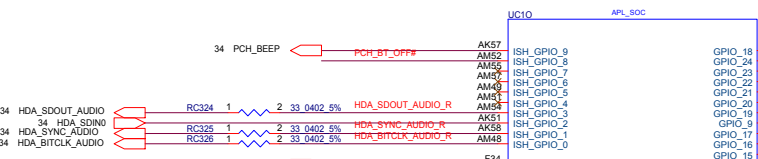


**USB2\_OC0\_N:** Used by the controller to disable I/O in case of overcurrent - USB port 0 (OTG port)  
**USB2\_OC1\_N:** Used by the controller to disable I/O in case of overcurrent - USB host ports [7:1]

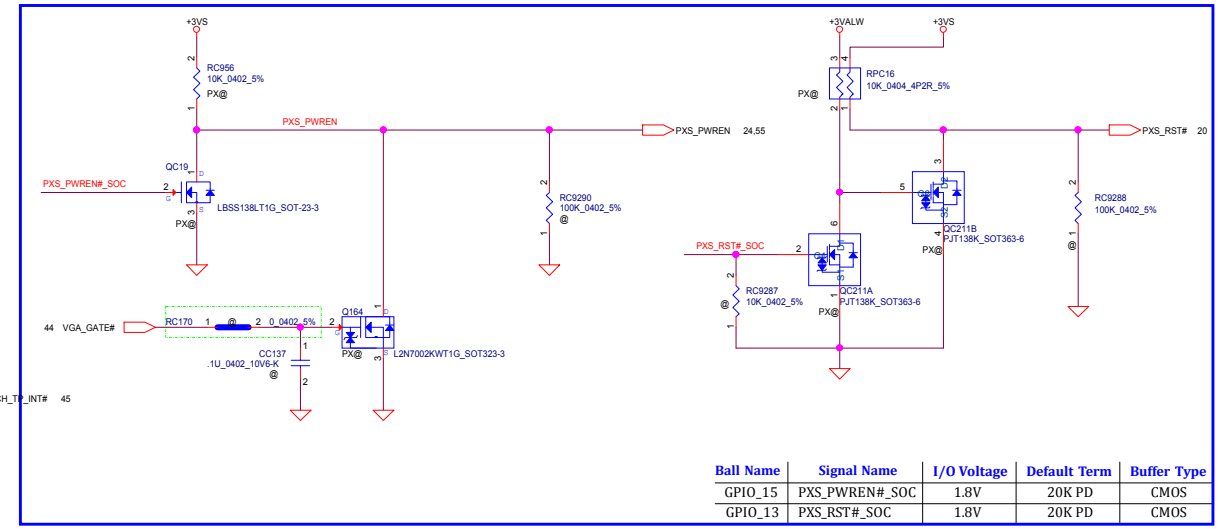
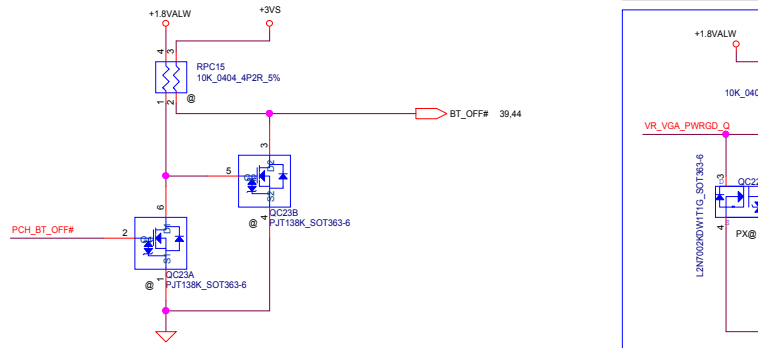
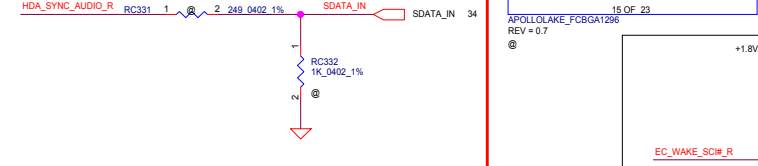




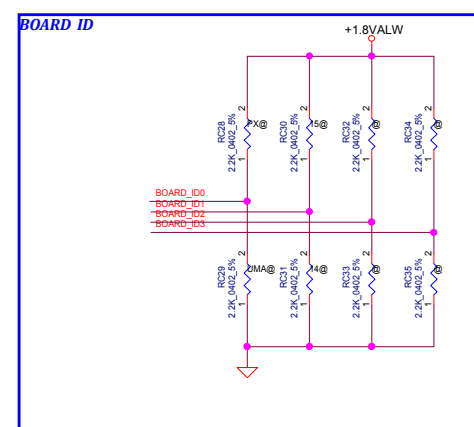
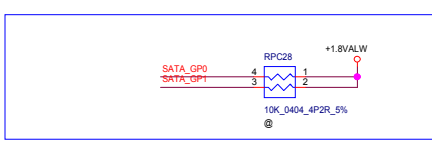
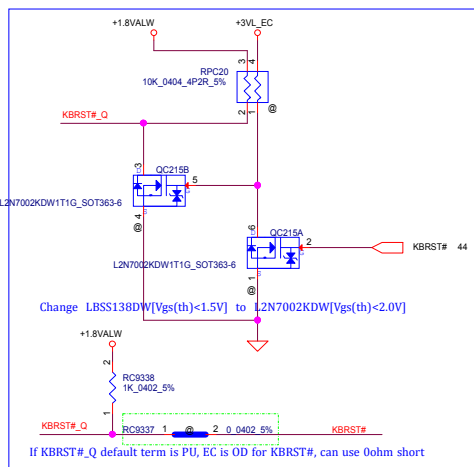
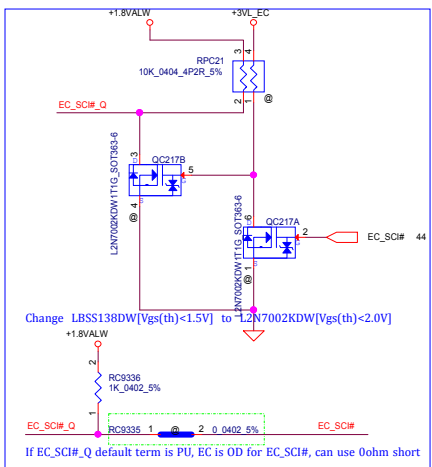
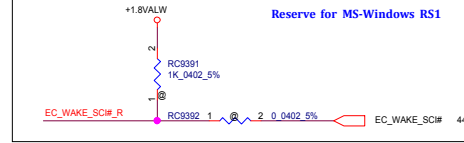
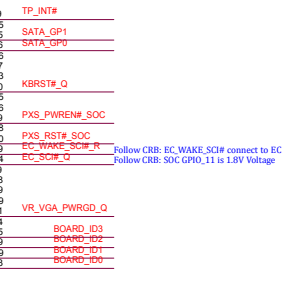
TP\_INT# IS Output,pull up @ touch pad conn side  
CRB direct connect to GPIO\_18  
Lewis 2016/10/13



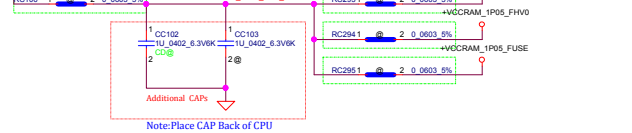
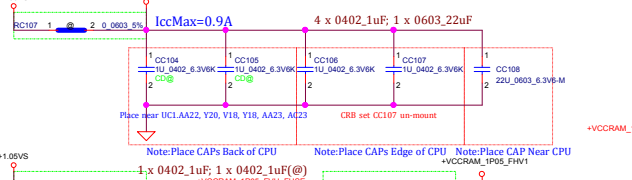
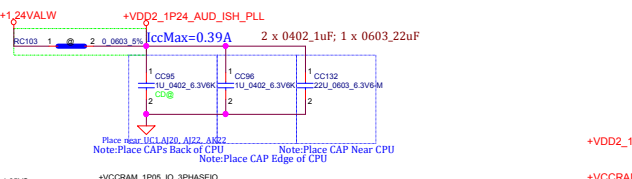
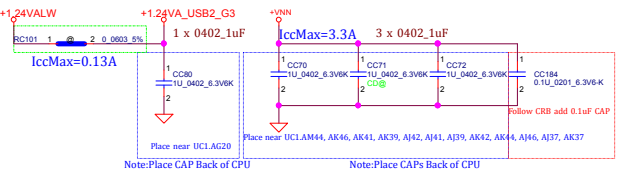
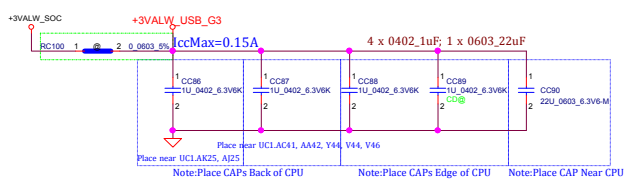
Sighting Alert(DOC#560733)  
1206618869: HD Audio SDI I/O Pin Issue  
Follow Intel request to remove for QS CPU



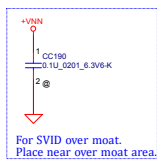
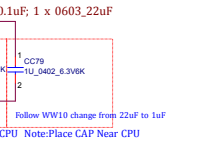
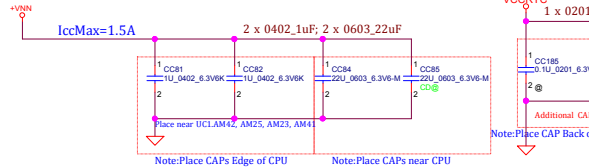
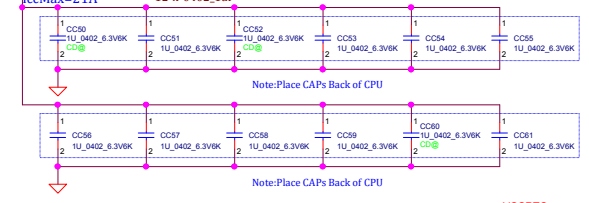
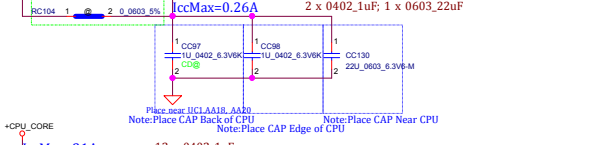
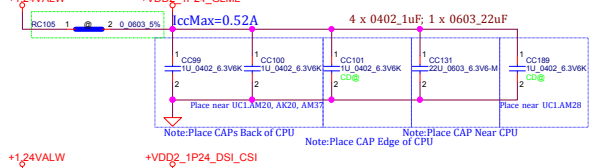
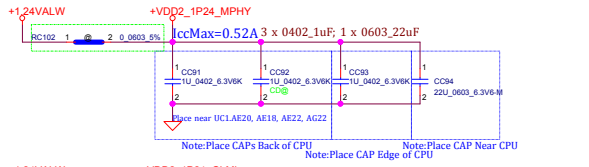
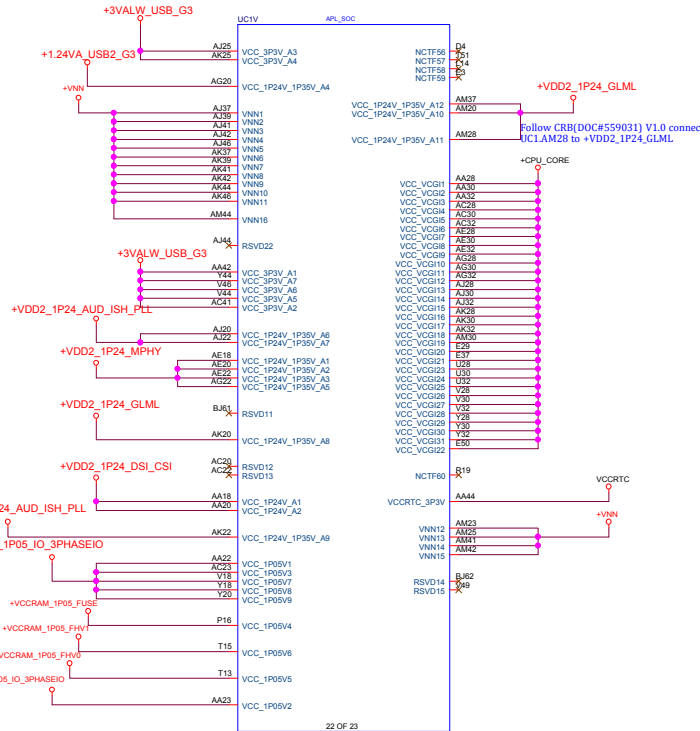
Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
GPIO_15	PXS_PWREN#_SOC	1.8V	20K PD	CMOS
GPIO_13	PXS_RST#_SOC	1.8V	20K PD	CMOS

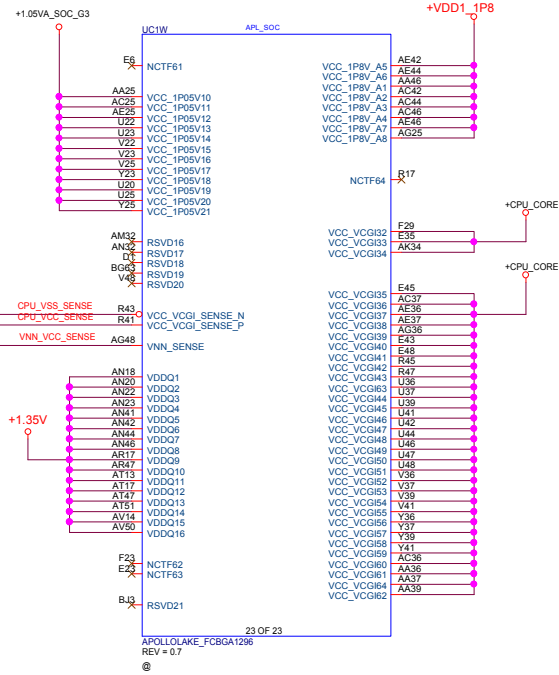
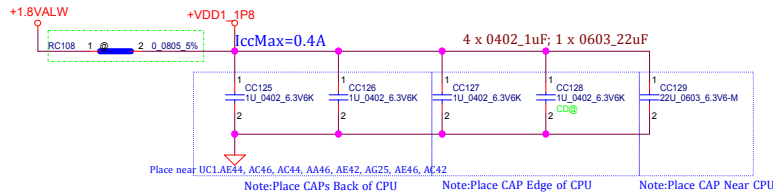
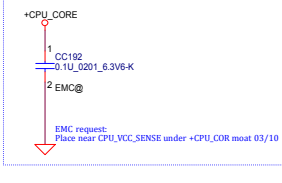
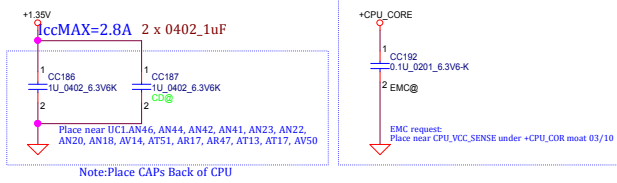
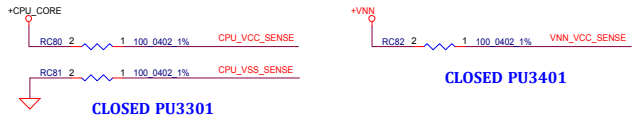
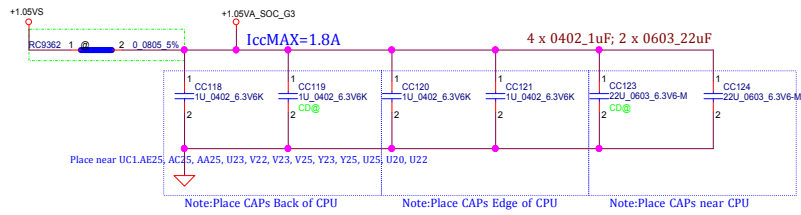


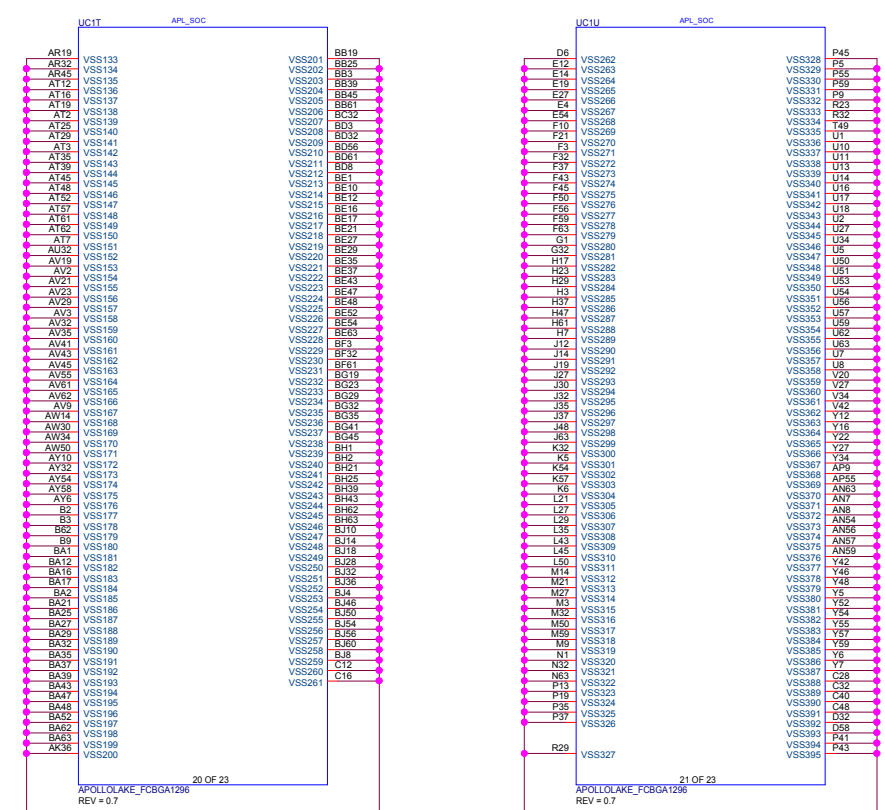
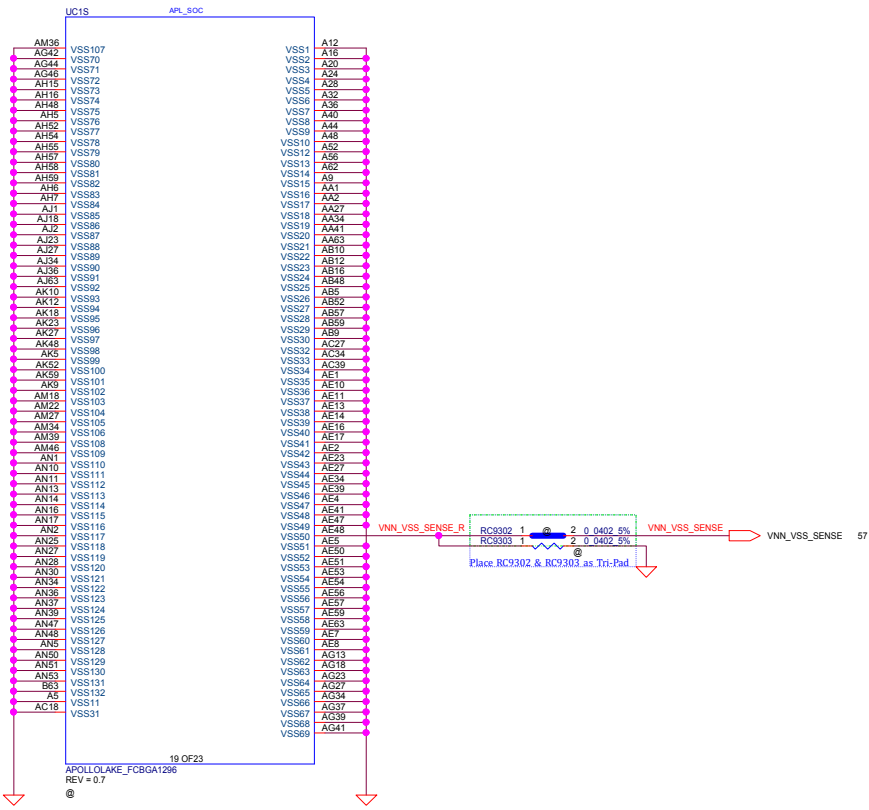
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description
0				UMA SKU
1		Reserve	Reserve	GPU SKU
	0			14" Panel
	1			15" Panel



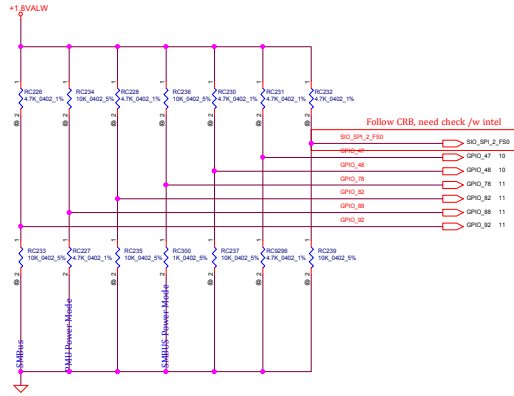
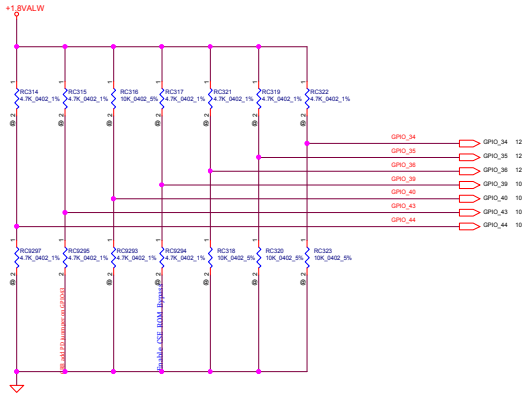
Follow CRB: P16, T15, T13 are different power trace. Maybe can merge them to one net



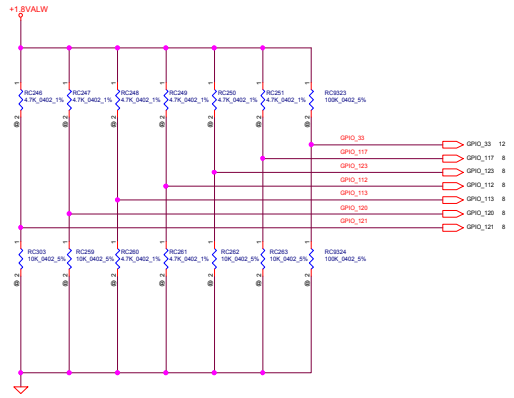
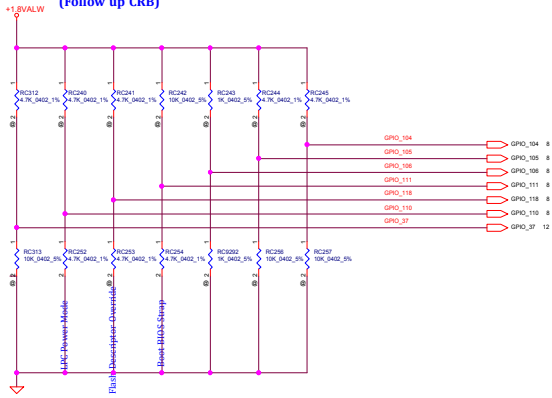




**Hardware STRAPS  
(Follow up CRB)**

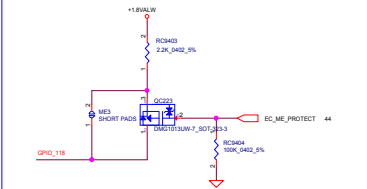


**Hardware STRAPS  
(Follow up CRB)**



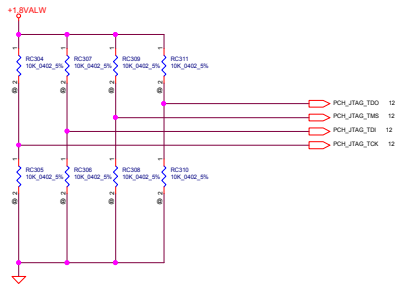
**ME\_PROTECT Circuit**

Change to P-MOS Diodes DMG101310W7 09/02



EC_ME_PROTECT	GPIO 118	TXE Flash Descriptor Override
Low	High	Override
High	Low	No Override (Normal Operation)

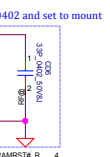
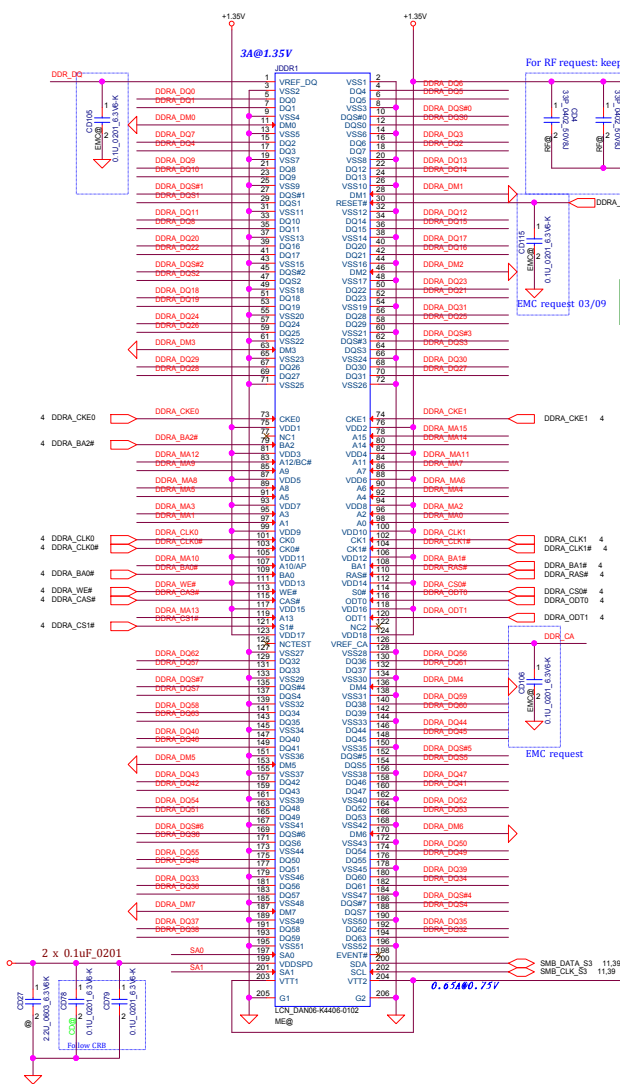
GPIO#	Purpose	Internal Termination	Schematics Setting	Pin usage	Remark
GPIO_33	RSVD	20K PD	Floating	N/A	Follow CRB(DOC#r: 561386); EDS(v2.1) P54
GPIO_34	RSVD	20K PD	Floating		EDS(v2.1) P47
GPIO_35	RSVD	20K PD	Floating		EDS(v2.1) P47
GPIO_36	RSVD	20K PD	Floating		EDS(v2.1) P47
GPIO_37	RSVD	20K PD	Floating	N/A	Follow CRB(DOC#r: 561386); EDS(v1.5) P57
GPIO_39	Enable CSE ROM Bypass	20K PD	Floating	1 = Enable bypass 0 = Disable bypass (default)*	This strap tells CSE (TXE3.0) to bypass ROM EDS(v2.1) P47
GPIO_40	RTC Clock Timer Bypass	20K PD	Floating	1 = Enable bypass 0 = Disable bypass (default)*	Only be used when an external oscillator is used to supply a 32.768kHz clock to RTC_X1. EDS(v2.1) P47
GPIO_43	RSVD	20K PU	4.7K PD	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_44	Allow SPI as a boot source	20K PU	Floating	1 = Enable(Default)* 0 = Disable	EDS(v2.1) P47
GPIO_47	Force DNX FW Load	20K PD	Floating	1 = Force 0 = Do not force(Default)*	Recovery strap for corrupted FW image EDS(v2.1) P47
GPIO_48	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P47
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. SMBus signals are 3.3V mode. EDS(v2.1) P47
GPIO_82	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_88	PMU 1.8V/3.3V mode select	20K PD	4.7K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. PMU signals are 3.3V mode. EDS(v2.1) P48
GPIO_92	SMBus No Re-Boot	20K PD	Floating	1 = Enable 0 = Disable(Default)*	Should strap this pin LOW. Functionality is handled by the PMC. EDS(v2.1) P48
GPIO_104	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_105	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_106	RSVD	20K PU	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	4.7K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. LPC signals are 3.3V mode. EDS(v3.1.1) P48
GPIO_111	RSVD	20K PU	4.7K PD	1 = Leave these regions unmapped by the System Agent 0 = Map these regions to the boot SPI	Pull LOW for designs that boot from SPI and HIGH otherwise. EDS(v3.1.1) P48
GPIO_112	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_113	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_117	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_118	Flash Descriptor Override	20K PD	4.7KPD	1 = Override 0 = No Override (Normal Operation)*	This strap enables the platform to override security features in the SPI. EDS(v2.1) P48
GPIO_120	Top swap override	20K PD	Floating	1 = Enable 0 = Disable (default)*	This strap enables platform to change different SPI ROM location. ESD(v2.1) P48
GPIO_121	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_123	RSVD	20K PU	Floating	Ensure this strap is PU when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48





# DDR Mapping table

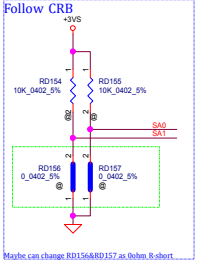
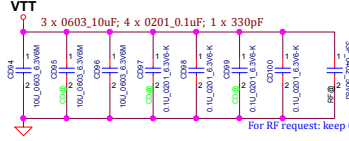
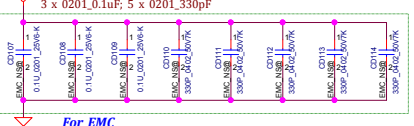
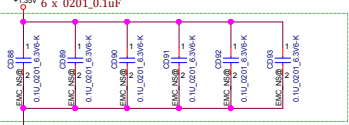
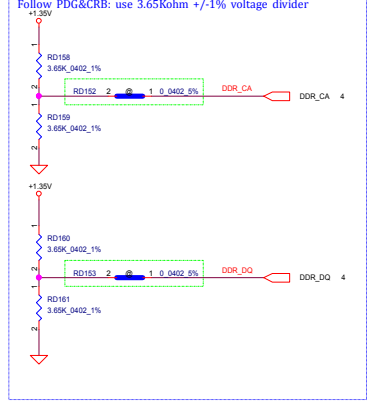
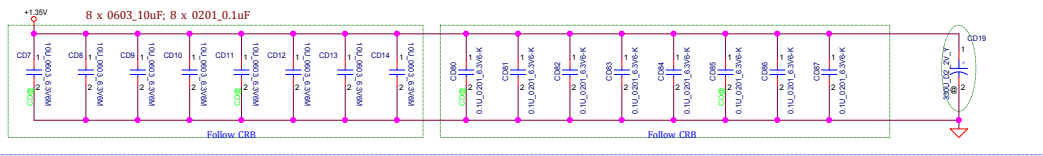
- DDR\_A\_DQ0---DQ0
- DDR\_A\_DQ1---DQ1
- DDR\_A\_DQ2---DQ2
- DDR\_A\_DQ3---DQ3
- DDR\_A\_DQ4---DQ4
- DDR\_A\_DQ5---DQ5
- DDR\_A\_DQ6---DQ6
- DDR\_A\_DQ7---DQ7
- DDR\_A\_DQ8---DQ8
- DDR\_A\_DQ9---DQ9
- DDR\_A\_DQ10---DQ10
- DDR\_A\_DQ11---DQ11
- DDR\_A\_DQ12---DQ12
- DDR\_A\_DQ13---DQ13
- DDR\_A\_DQ14---DQ14
- DDR\_A\_DQ15---DQ15
- DDR\_A\_DQ16---DQ16
- DDR\_A\_DQ17---DQ17
- DDR\_A\_DQ18---DQ18
- DDR\_A\_DQ19---DQ19
- DDR\_A\_DQ20---DQ20
- DDR\_A\_DQ21---DQ21
- DDR\_A\_DQ22---DQ22
- DDR\_A\_DQ23---DQ23
- DDR\_A\_DQ24---DQ24
- DDR\_A\_DQ25---DQ25
- DDR\_A\_DQ26---DQ26
- DDR\_A\_DQ27---DQ27
- DDR\_A\_DQ28---DQ28
- DDR\_A\_DQ29---DQ29
- DDR\_A\_DQ30---DQ30
- DDR\_A\_DQ31---DQ31
- DDR\_A\_DQ32---DQ32
- DDR\_A\_DQ33---DQ33
- DDR\_A\_DQ34---DQ34
- DDR\_A\_DQ35---DQ35
- DDR\_A\_DQ36---DQ36
- DDR\_A\_DQ37---DQ37
- DDR\_A\_DQ38---DQ38
- DDR\_A\_DQ39---DQ39
- DDR\_A\_DQ40---DQ40
- DDR\_A\_DQ41---DQ41
- DDR\_A\_DQ42---DQ42
- DDR\_A\_DQ43---DQ43
- DDR\_A\_DQ44---DQ44
- DDR\_A\_DQ45---DQ45
- DDR\_A\_DQ46---DQ46
- DDR\_A\_DQ47---DQ47
- DDR\_A\_DQ48---DQ48
- DDR\_A\_DQ49---DQ49
- DDR\_A\_DQ50---DQ50
- DDR\_A\_DQ51---DQ51
- DDR\_A\_DQ52---DQ52
- DDR\_A\_DQ53---DQ53
- DDR\_A\_DQ54---DQ54
- DDR\_A\_DQ55---DQ55
- DDR\_A\_DQ56---DQ56
- DDR\_A\_DQ57---DQ57
- DDR\_A\_DQ58---DQ58
- DDR\_A\_DQ59---DQ59
- DDR\_A\_DQ60---DQ60
- DDR\_A\_DQ61---DQ61
- DDR\_A\_DQ62---DQ62
- DDR\_A\_DQ63---DQ63




- DDR\_A\_DQ0..63] 4
- DDR\_A\_CS0..7] 4
- DDR\_A\_CS8..15] 4
- DDR\_A\_MA0..15] 4

$OSCON (220uF, 6.3V, 4.2L, ESR17m)*1=(SF00002Y00)$

Layout Note: Place near DIMM



0.65000.737

Security Classification	LC Future Center Secret Data		Title		
Issued Date	2013/08/08	Deciphered Date	2013/08/05		Blank
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## Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

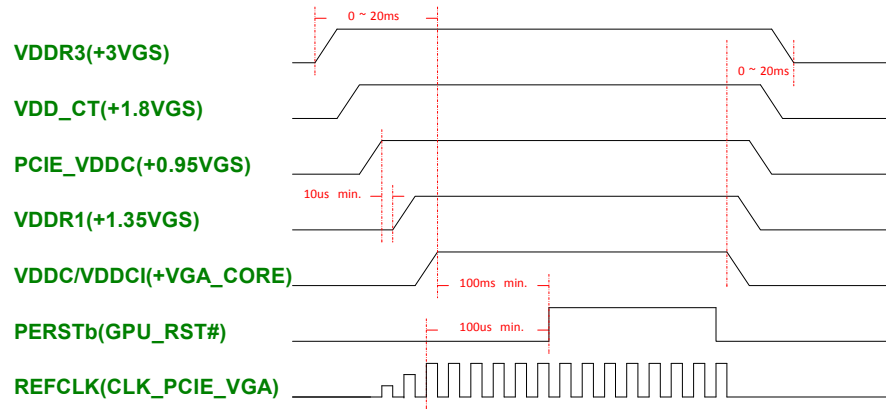
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10  $\mu$ s before VDDC, VDDCI, and VMEMIO start to ramp up.

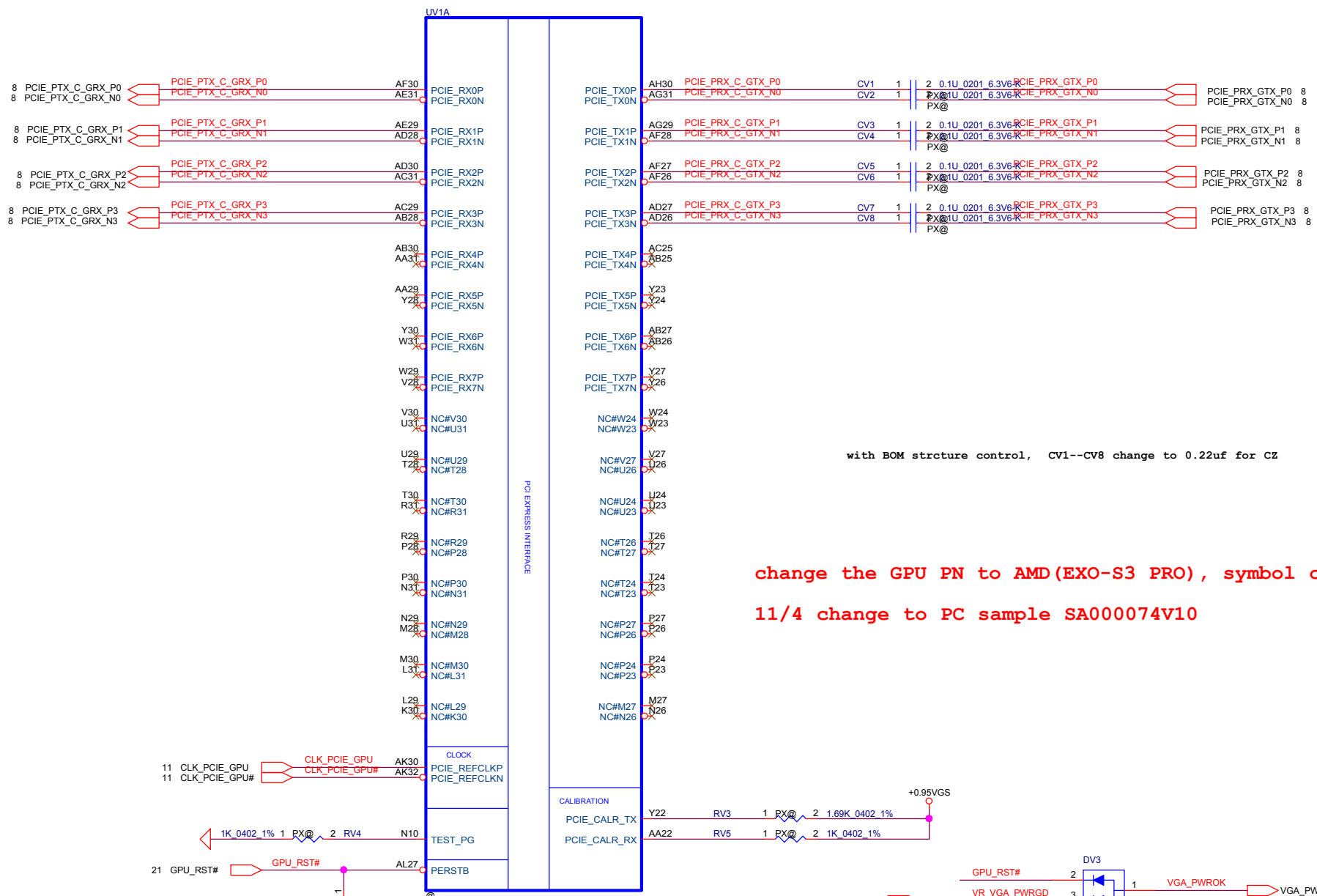
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

The gate circuits must meet the slew rate requirement (such as  $\leq 50$  mV/ $\mu$ s). For power down, reversing the ramp-up sequence is recommended.



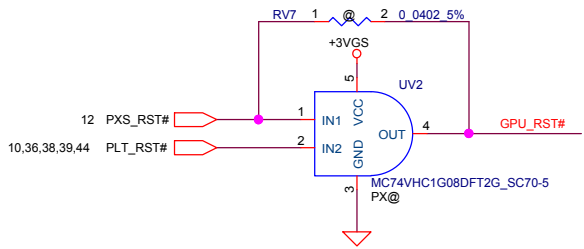
## VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC4H24AJR-R0C	100	4.53K	4.99K
	Micron EDW4032BABG-70-F	111	4.75K	NC
	Samsung K4G41325FE-HC28	110	3.4K	10K
		000	NC	4.75K
		010	4.53K	2K
		001	8.45K	2K



with BOM structure control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok  
11/4 change to PC sample SA000074V10

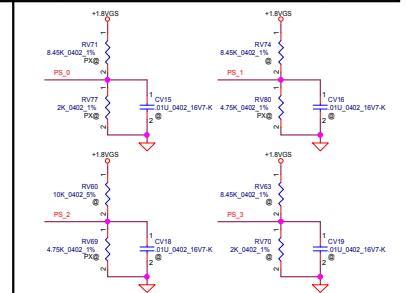
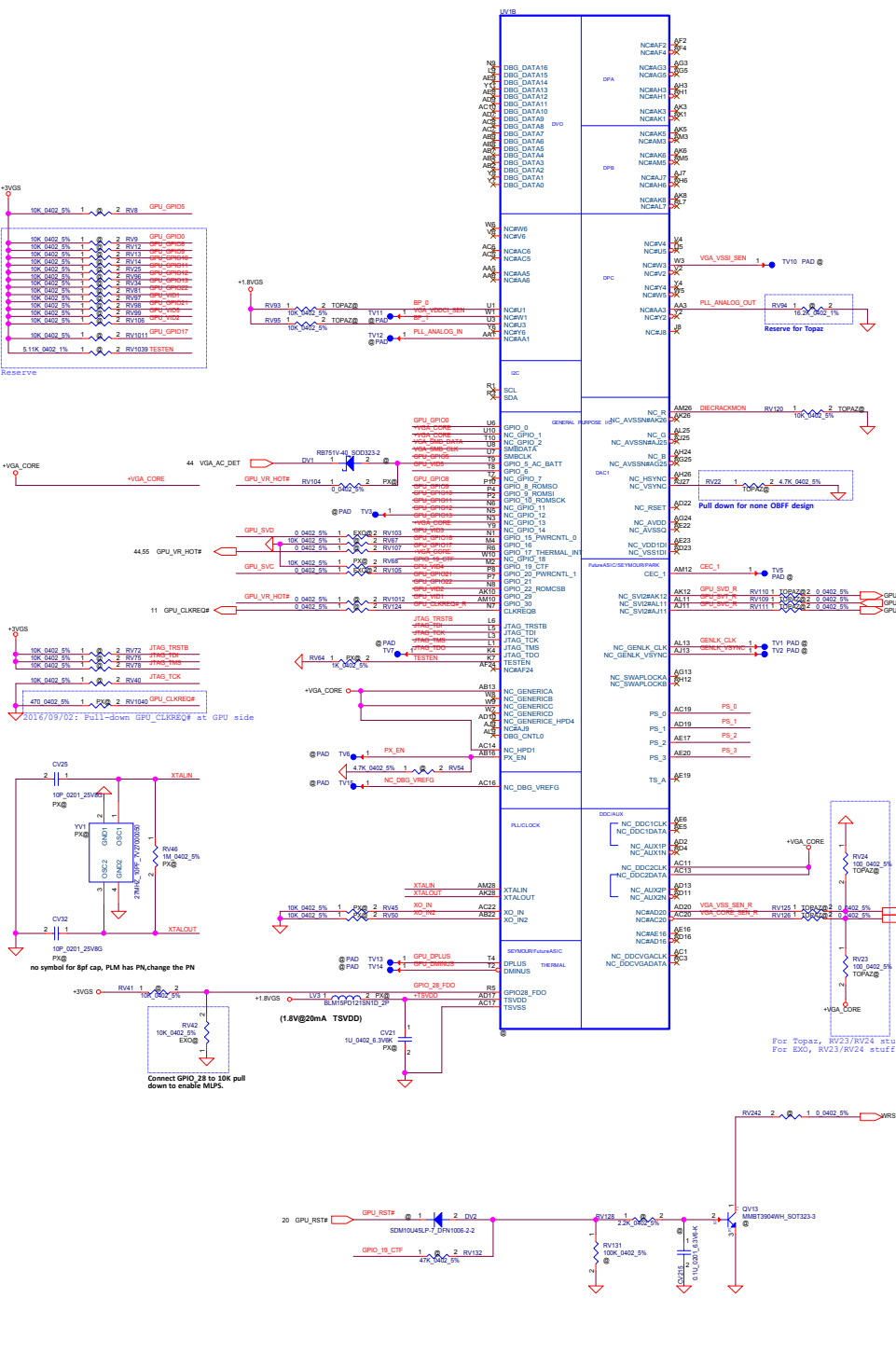


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	<b>ATI_EXO-PRO_PCIE</b>	
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Size Custom	Document Number	Date		Rev	
	<b>DG424/DG524</b>	Thursday, March 09, 2017		1.0	
		Sheet 20 of 58			

**CONFIGURATION STRAPS**  
**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS:  
 \* DO NOT INSTALL RESISTOR  
 1 = INSTALL 10K RESISTOR  
 NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	BIOS_CONF[0]1	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_0[2]	ROM_CONF[0]1	Define the primary memory capacity size when STRAP_BIOS_ROM_EN = 0	001 = 256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONFN_PFNSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of auto-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported 0 = PCIe GEN3 is not supported	1 = GEN3 is supported
PS_1[10]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_1[14]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[14]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter full-swing is enabled 1 = The transmitter full-swing is disabled	1
PS_1[15]	STRAP_TX_DEMPH_EN	0 = Tx deemphasis disabled 1 = Tx deemphasis enabled	1 = Enable
PS_2[1]	N/A	Reserved	0
PS_2[2]	N/A	Reserved	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capability enabled 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1]	BOARD_CONF[0]	Board configuration related settings, such as memory ID	
PS_3[2]	BOARD_CONF[1]	100 = Hynix 1G 111 = Micron 1G 110 = Samsung 1G	000 = Hynix 2G 010 = Micron 2G 100 = Samsung 2G
PS_3[4]	AUD_PORT_CONFN_PFNSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user (combine with PS_3[5]).	
PS_3[5]	AUD_PORT_CONFN_PFNSTRAP[2]	111 = No usable endpoints. 100 = One usable endpoint. 100 = Three usable endpoints. 010 = Four usable endpoints. 010 = Five usable endpoints. 000 = Six usable endpoints.	111 = No usable endpoints.



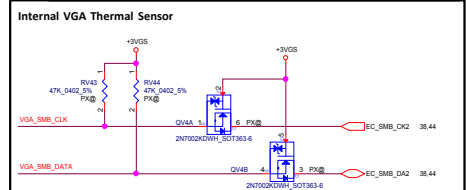
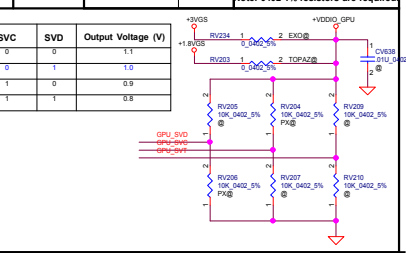
MLPS	Bit					R_pu (Ω)	R_pd (Ω)	Bits [3:1]
	5	4	3	2	1			
PS_0 [5:1]	1	1	0	0	1	RV71=8.45K	RV77=2K	CV15=NC
PS_1 [5:1]	1	1	1	0	1	RV74=8.45K	RV80=2K	CV16=NC
PS_2 [5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3 [5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=NC

with BOM structure control, RV63/RV70 change to different values to adjust VRAM config

with BOM structure control, when config PEG3, RV74 change to 8.45K, RV80 change

Capacitor Value (nF)	Bits [5:4]
4530	4590
3340	3600
3490	10000
50	4950
NC	111

Note: 0402 1% resistors are required



UV1F

NC\_VARY\_BL  
NC\_DIGON

AB11  
AB12

+VGA\_CORE


NC\_UPHYAB\_TMDPA\_TX0N ΔL15  
 NC\_UPHYAB\_TMDPA\_TX0P ΔK14  
 NC\_UPHYAB\_TMDPA\_TX1N ΔH16  
 NC\_UPHYAB\_TMDPA\_TX1P ΔJ15  
 NC\_UPHYAB\_TMDPA\_TX2N ΔL17  
 NC\_UPHYAB\_TMDPA\_TX2P ΔK16  
 NC\_UPHYAB\_TMDPA\_TX3N ΔH18  
 NC\_UPHYAB\_TMDPA\_TX3P ΔJ17  
 NC\_TXOUT\_L3P ΔL19  
 NC\_TXOUT\_L3N ΔK18

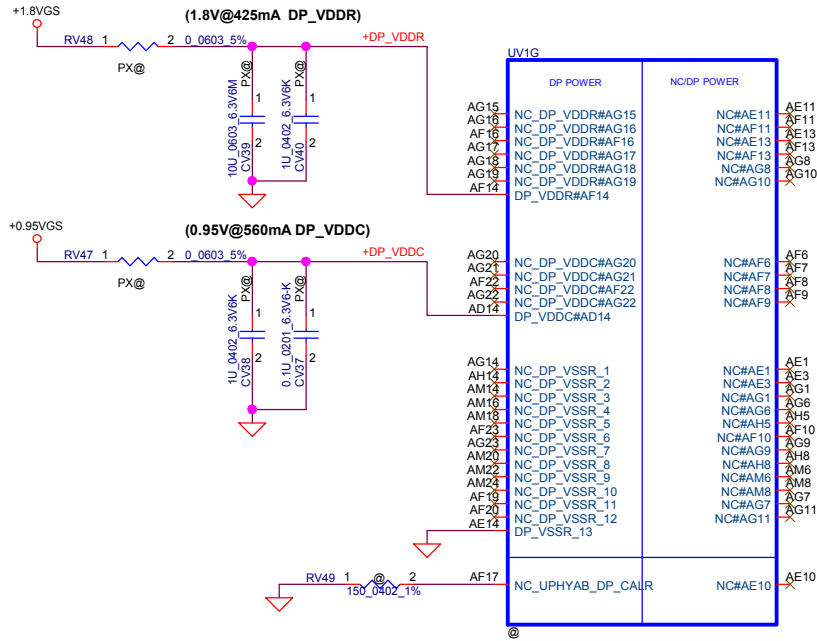
TMDP

NC\_UPHYAB\_TMDPB\_TX0N ΔH20  
 NC\_UPHYAB\_TMDPB\_TX0P ΔJ19  
 NC\_UPHYAB\_TMDPB\_TX1N ΔL21  
 NC\_UPHYAB\_TMDPB\_TX1P ΔK20  
 NC\_UPHYAB\_TMDPB\_TX2N ΔH22  
 NC\_UPHYAB\_TMDPB\_TX2P ΔJ21  
 NC\_UPHYAB\_TMDPB\_TX3N ΔL23  
 NC\_UPHYAB\_TMDPB\_TX3P ΔK22  
 NC\_TXOUT\_U3P ΔK24  
 NC\_TXOUT\_U3N ΔJ23

@

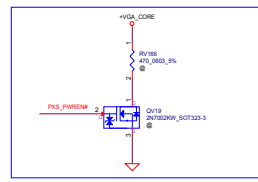
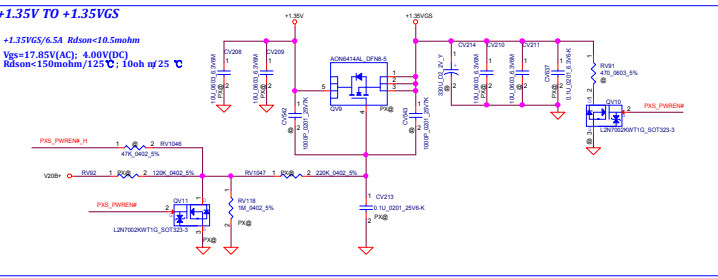
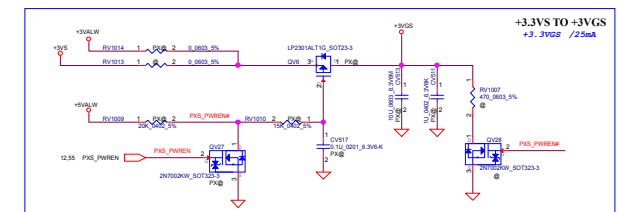
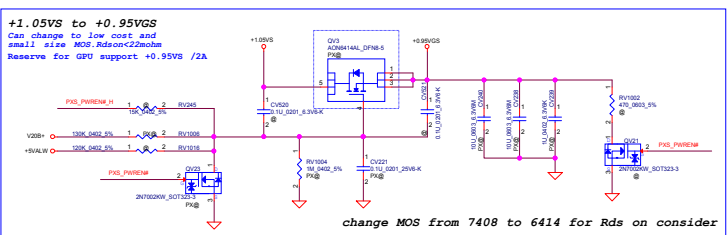
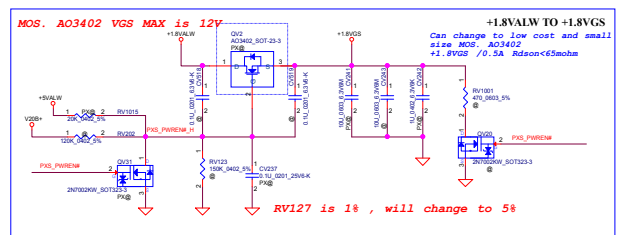
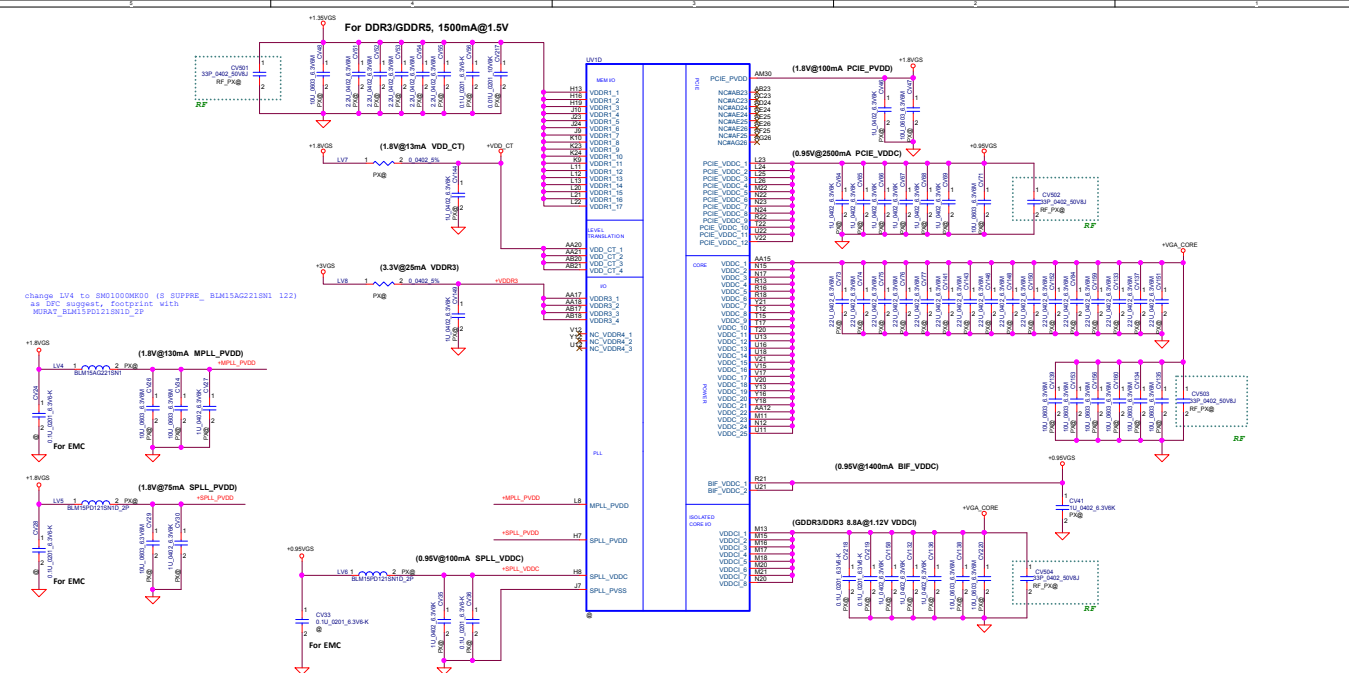
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ATI_EXO-PRO_TMDP		
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Date:	Thursday, March 09, 2017	Sheet 22 of 60

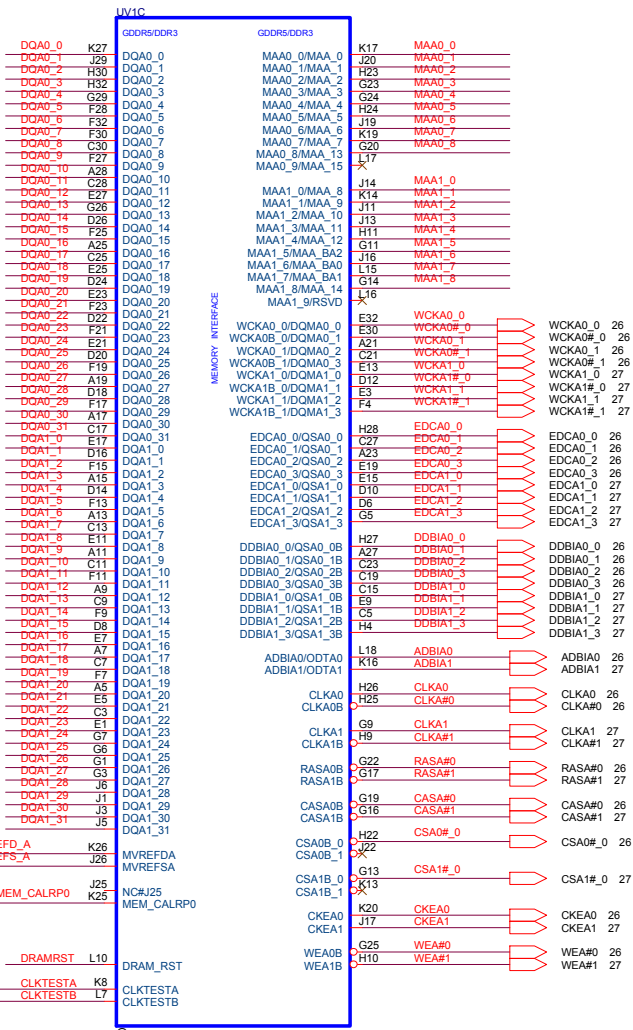
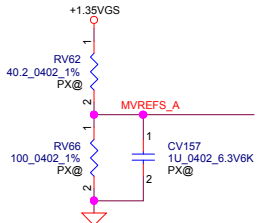
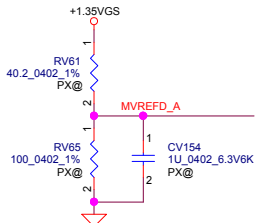
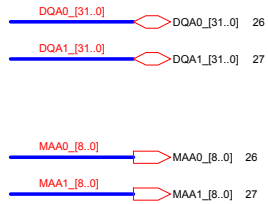


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ATI_EXO-PRO_DP Power		
Size Custom	Document Number	Rev 1.0
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**ATI\_EXO-PRO\_MEM IF**

Size Custom Document Number **DG424/DG524** Rev 1.0

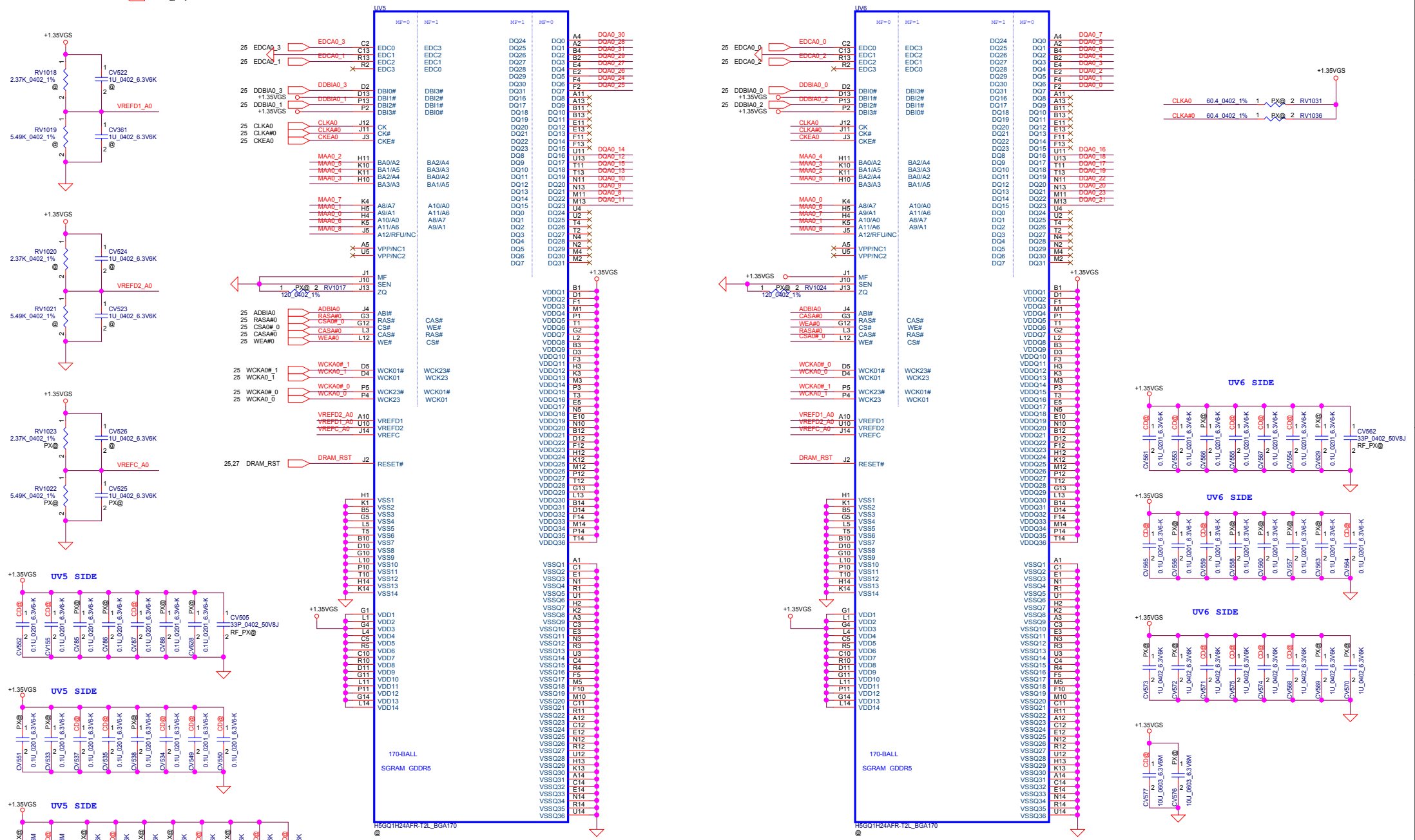
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# Lower 32 bits



## MF=0 No Mirror

## MF=1 Mirror



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				DG424/DG524	1.0
				Date	Thursday, March 09, 2017
				Sheet	26 of 60

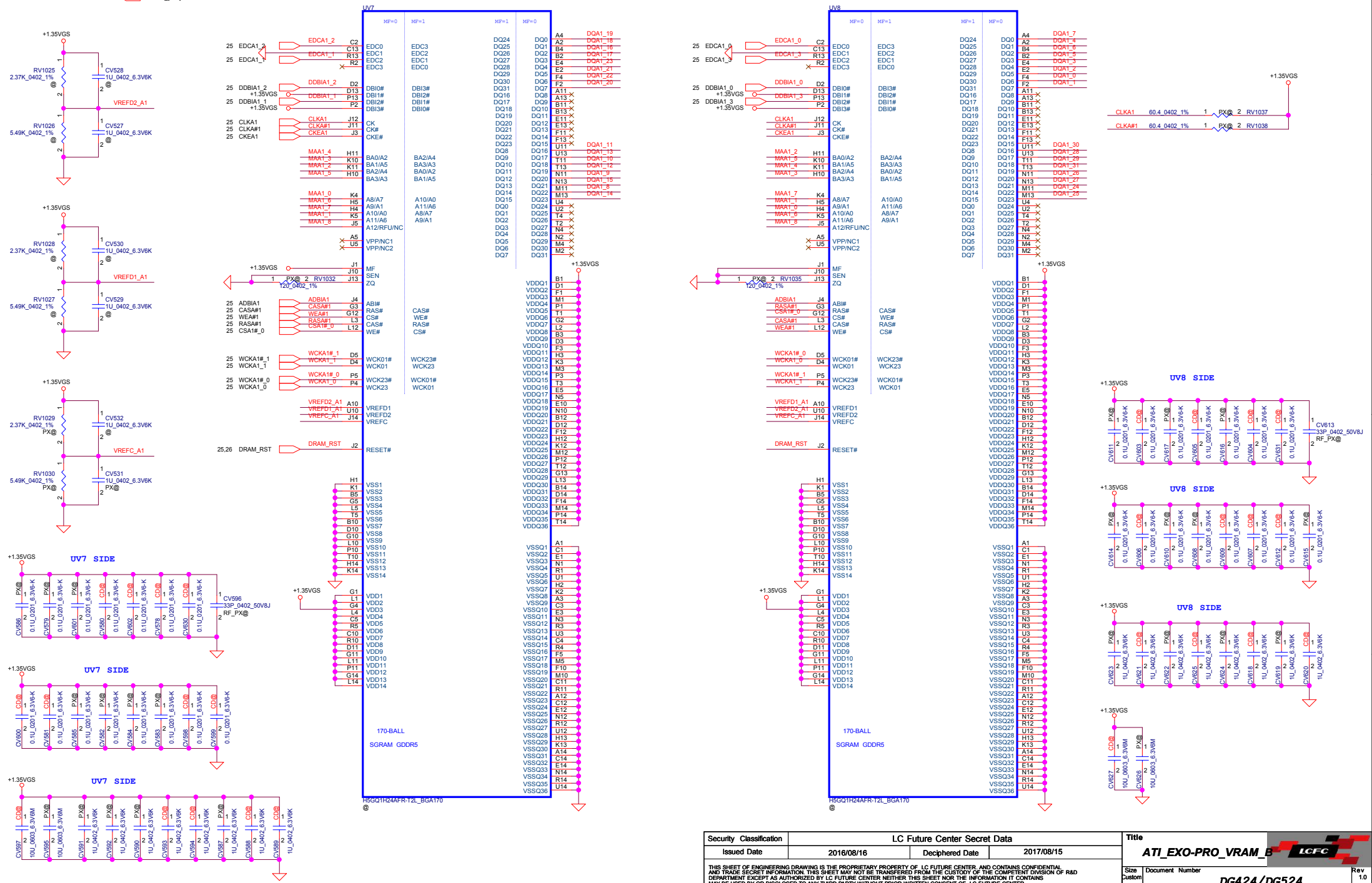
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# Upper 32 bits



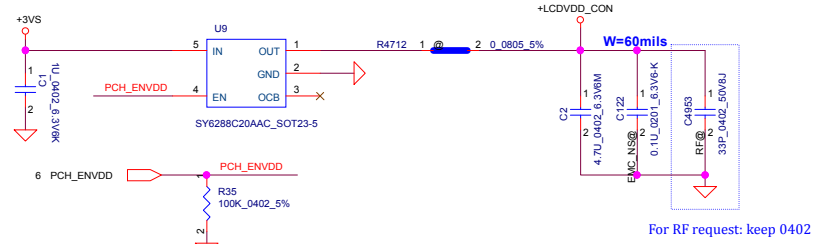
## MF=1 Mirror

## MF=0 No Mirror

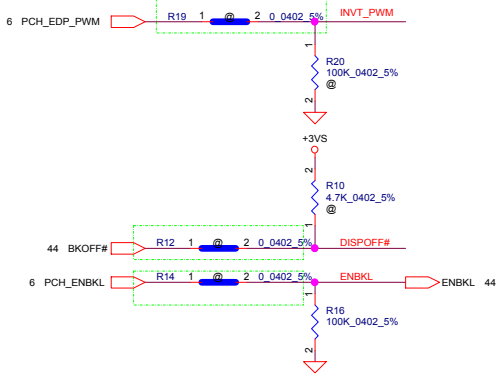


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Size	Document Number	Rev	
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Date:	Thursday, March 09, 2017	Sheet	27 of 60

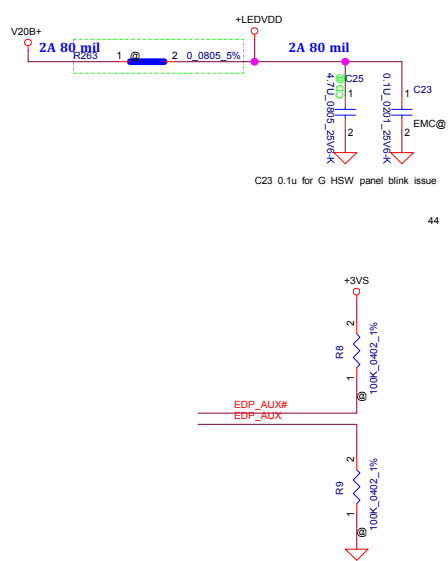
### LCD POWER CIRCUIT



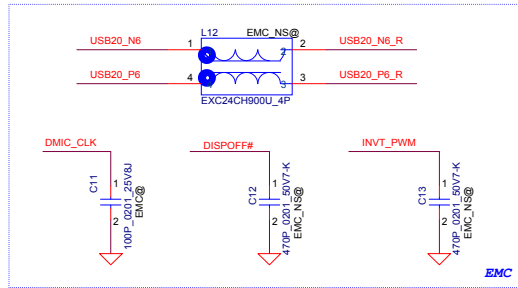
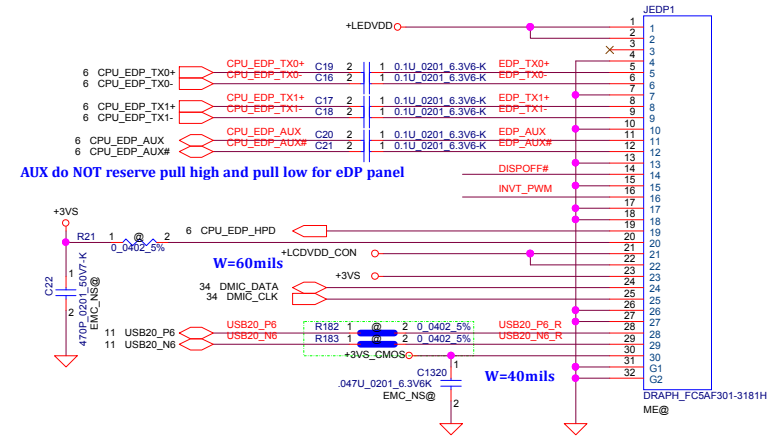
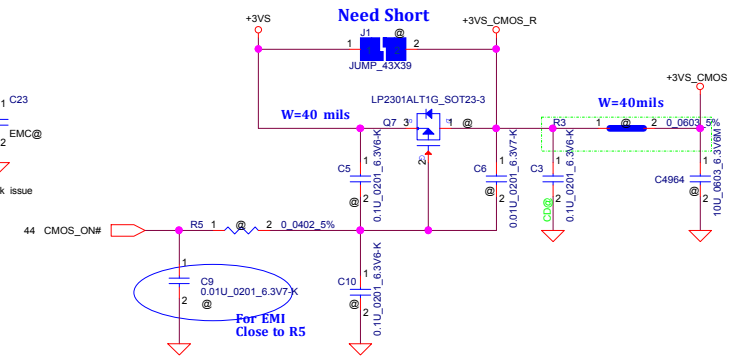
APL SoC output enable Voh min is 1.8V-0.45V=1.35V



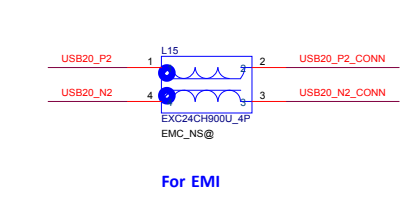
### B+ to +LEDVDD POWER



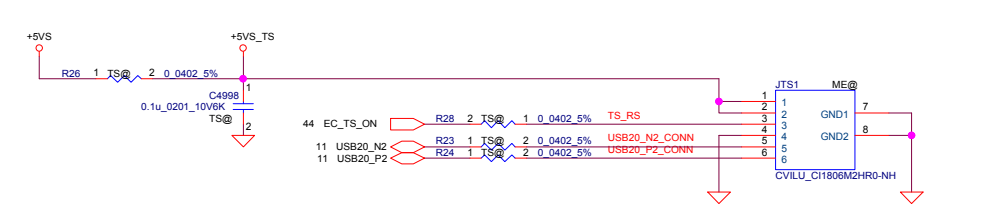
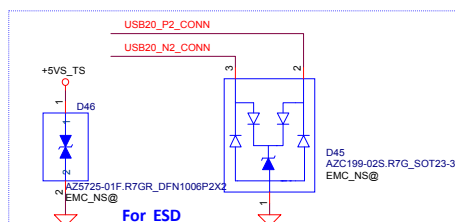
### CMOS CAMERA



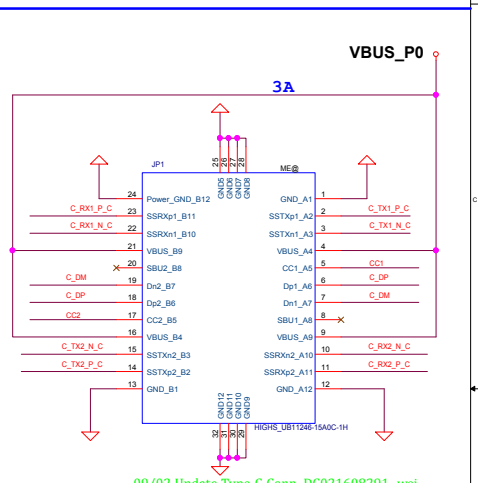
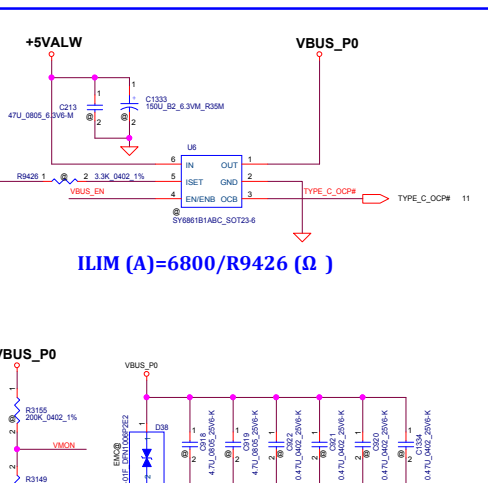
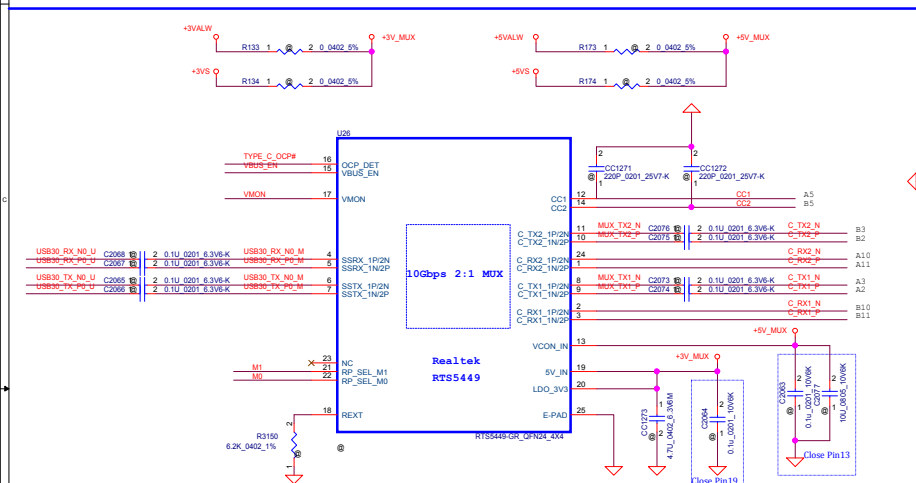
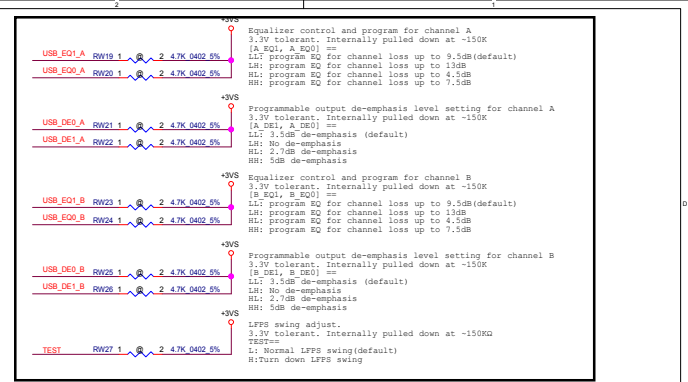
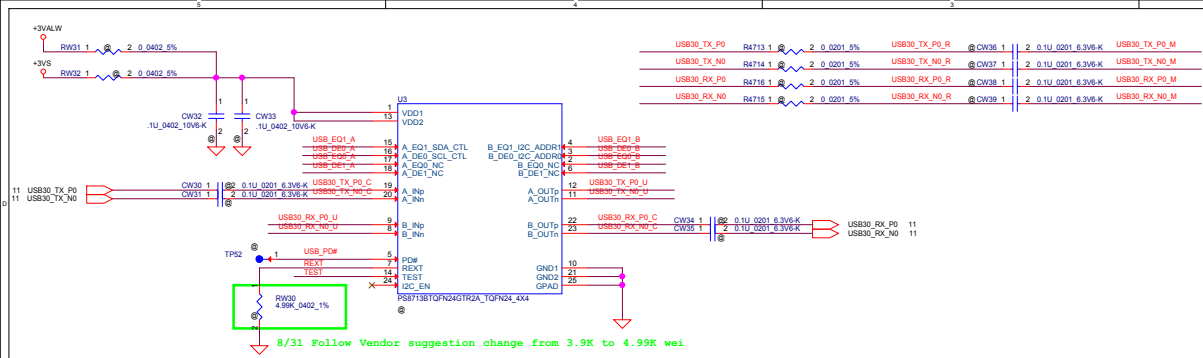
### Touch Screen



### Touch Screen



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Rp configuration

Rp: 1.5A (now)

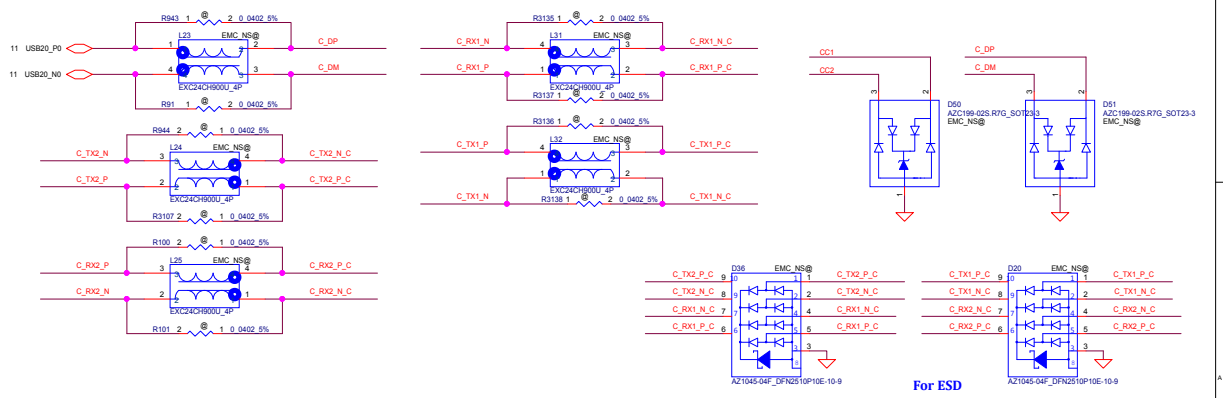
Rp	M1	M0	Note
Rp: 900mA	0	1	R3144/R3142 mount
Rp: 1.5A	1	0	R3139/R3143 mount
Rp: 3.0A	1	1	R3139/R3142 mount

For C\_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

For C\_VBUS power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount



5

4

3

2

1

D

D

C

C

B

B

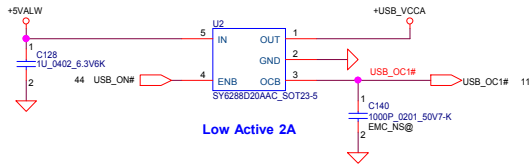
A

A

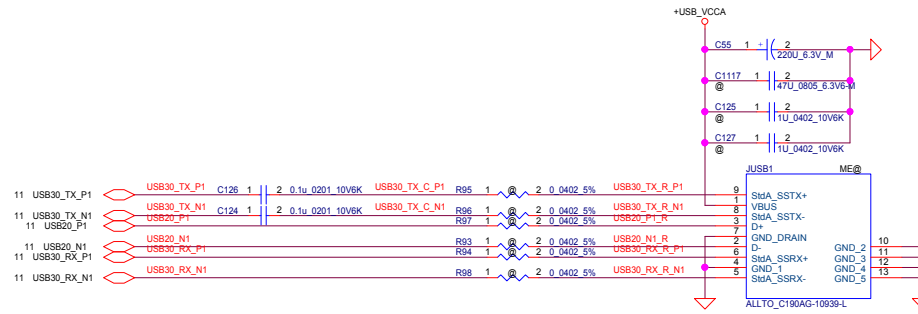
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<small>Date:</small> Thursday, March 09, 2017				<small>Sheet</small> 30	<small>of</small> 58
				<small>Rev</small> 1.0	



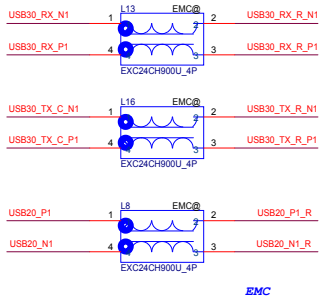
# USB3.0 Port X 1



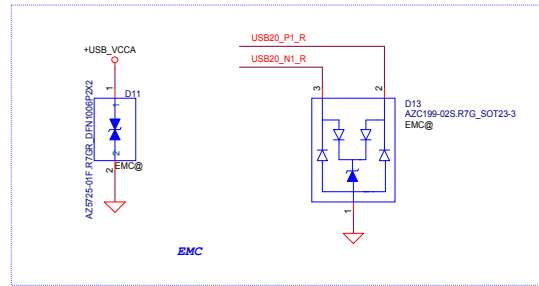
Low Active 2A



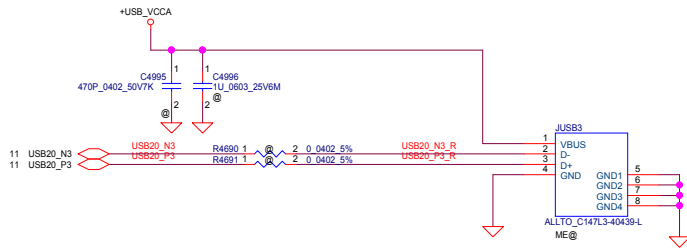
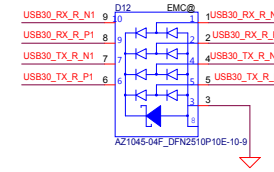
09/05 Update USBConn. P/N DC021609011 wei



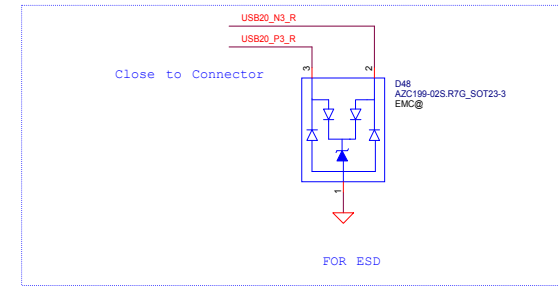
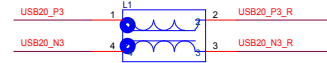
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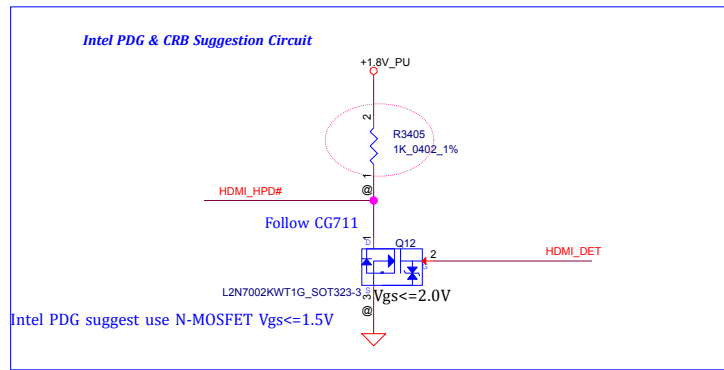
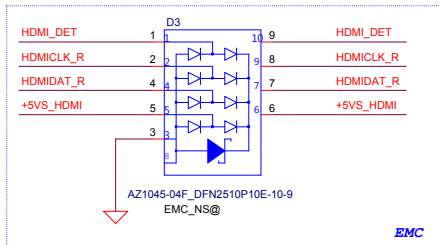
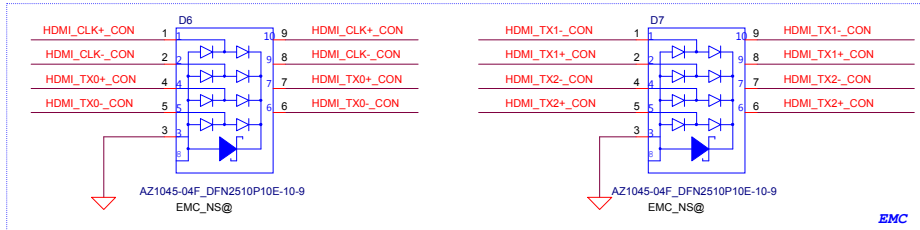
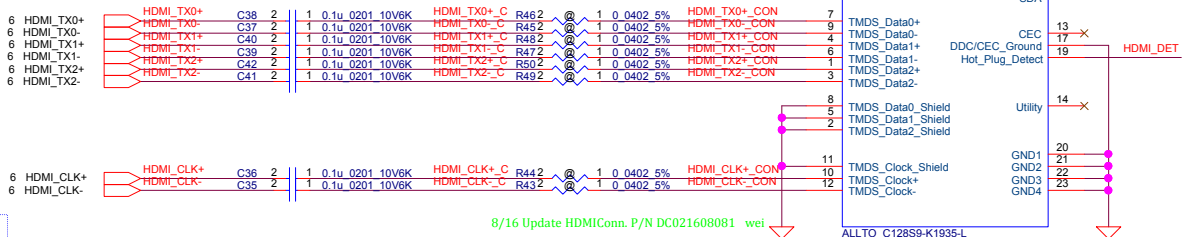
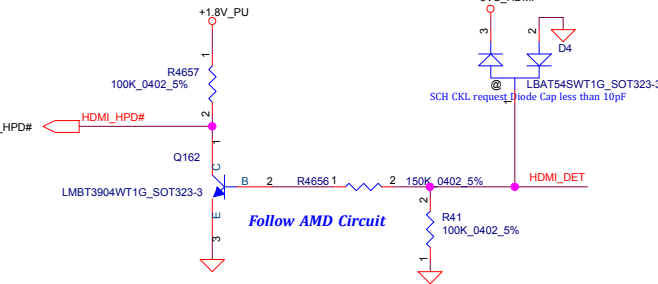
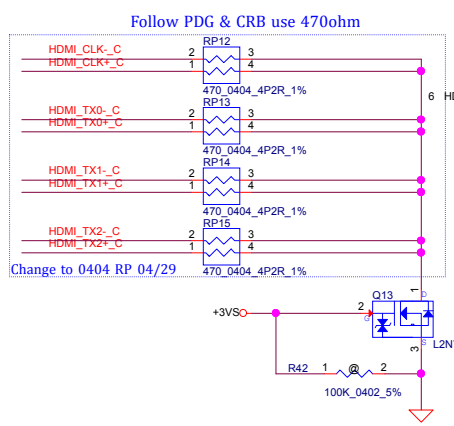
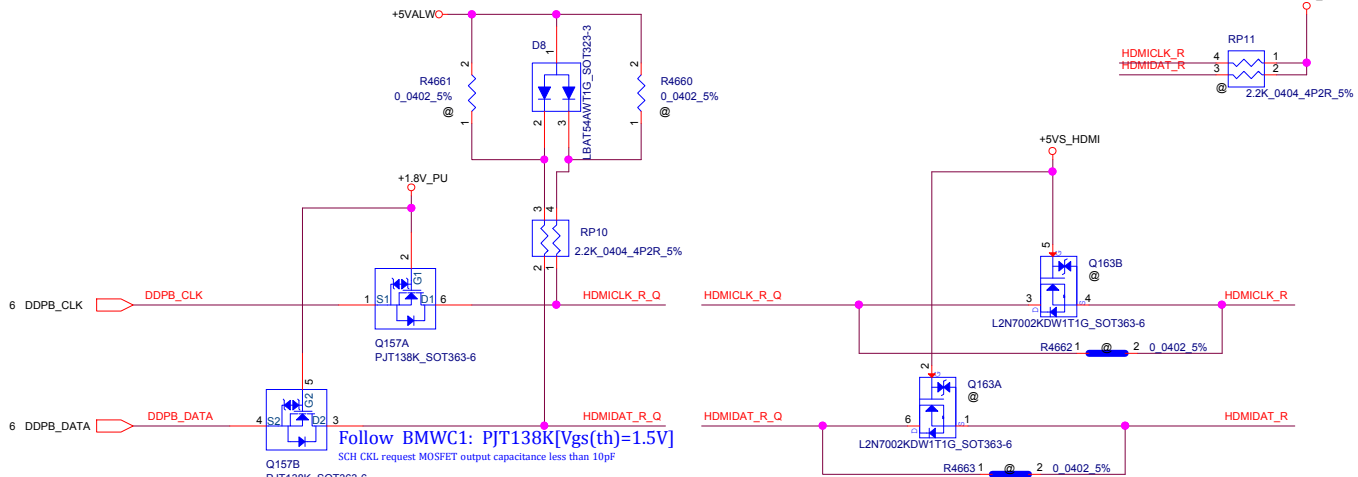
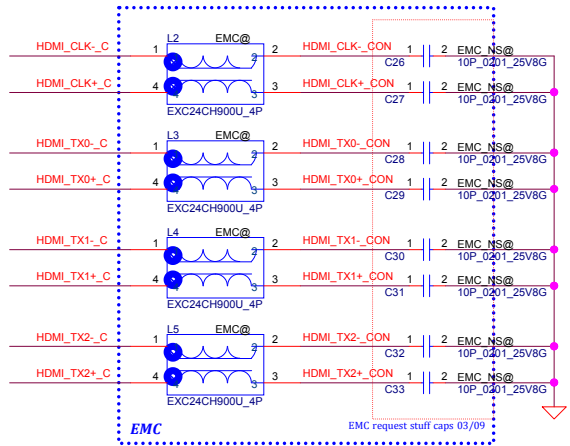
EMC



Update footprint symbol lewis



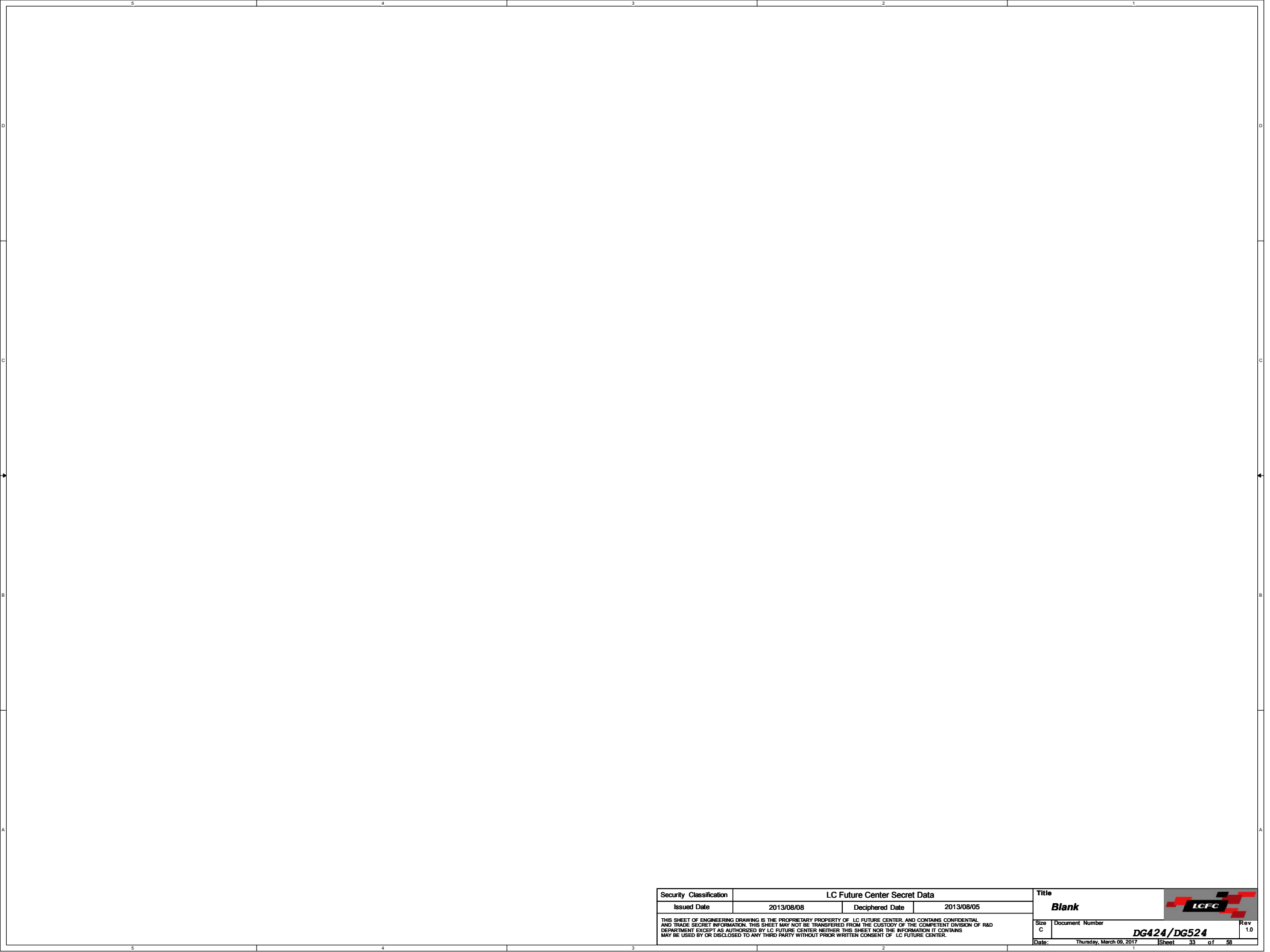
FOR ESD




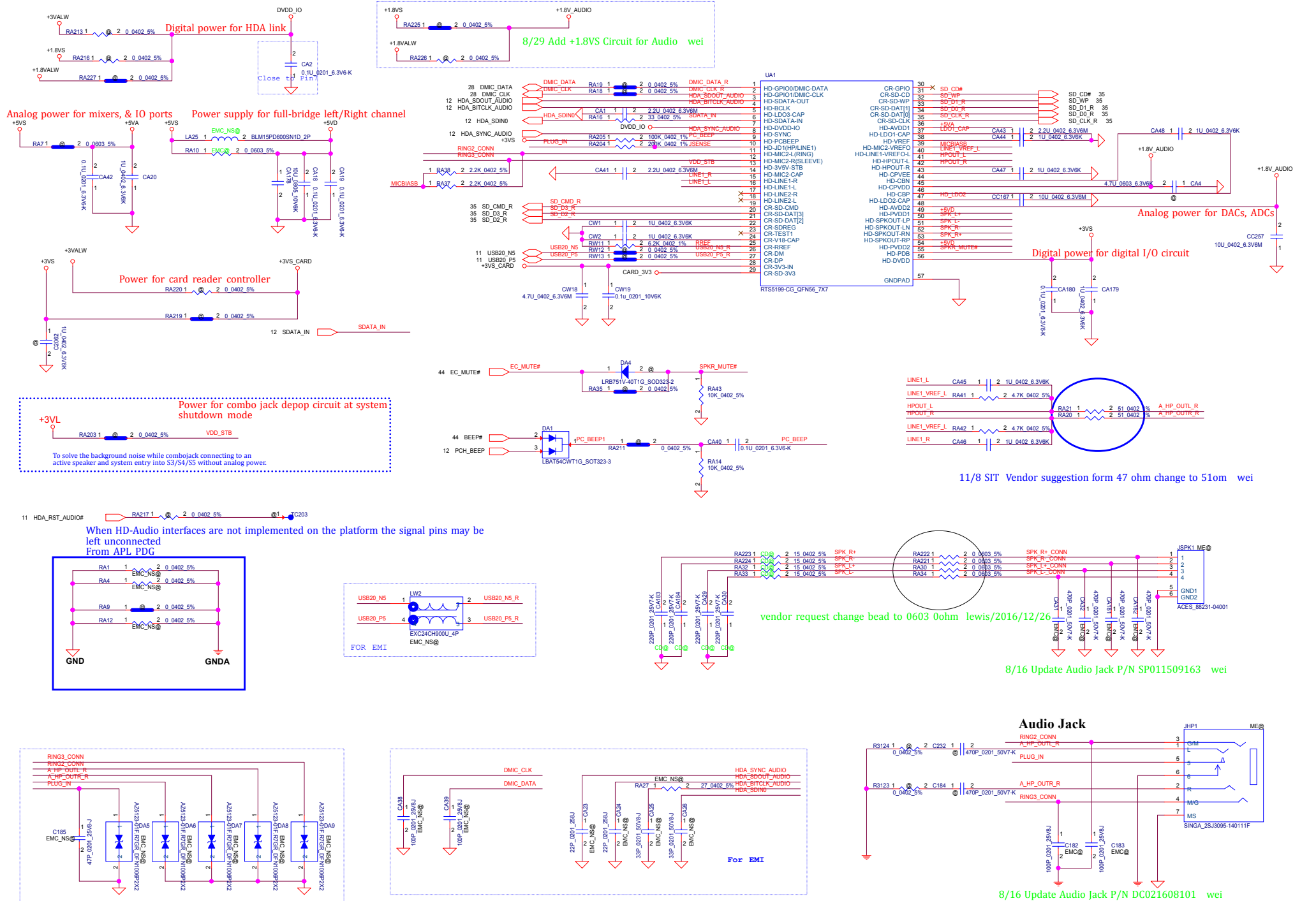
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HDMI_CONN		
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Size	Document Number			1.0	
C	DG424/DG524				
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8/29 Add +1.8VS Circuit for Audio wei

Digital power for digital I/O circuit

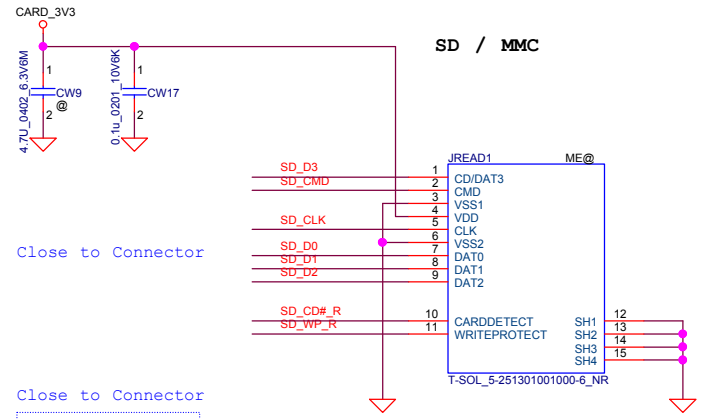
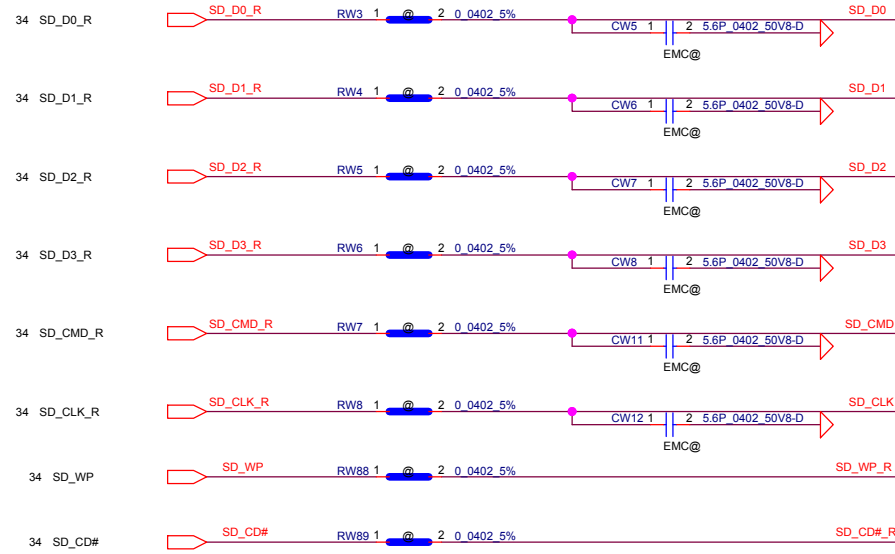
11/8 SIT Vendor suggestion form 47 ohm change to 51om wei

vendor request change bead to 0603 0ohm lewis/2016/12/26

8/16 Update Audio Jack P/N SP011509163 wei

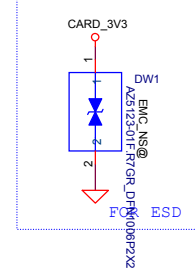
8/16 Update Audio Jack P/N DC021608101 wei

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Size	Document Number		DG424/DG524				Date		Thursday, March 09, 2017
<span style="float: right;">Sheet 34 of 58</span>									

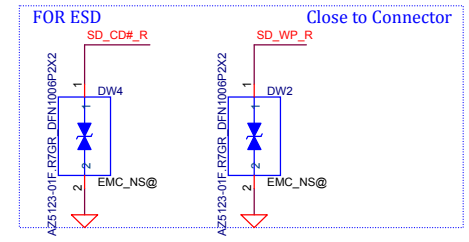


Close to Connector

Close to Connector



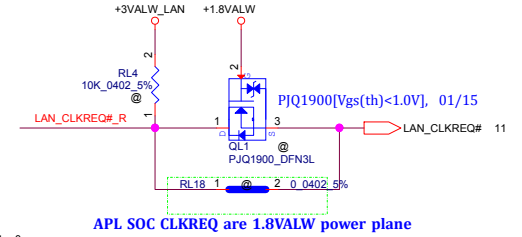
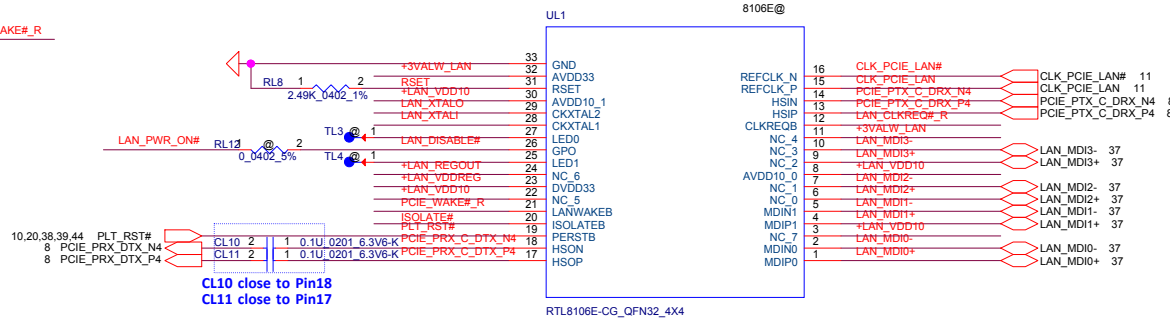
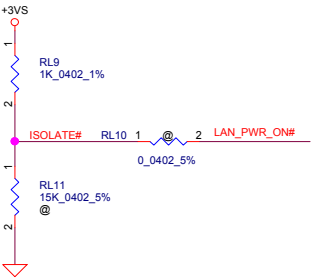
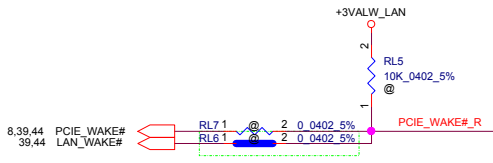
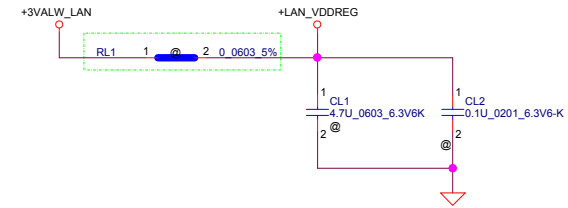
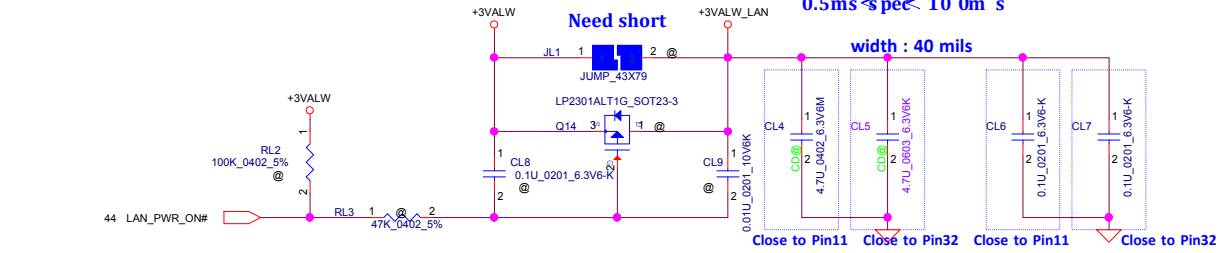
8/16 Update Conn. P/N SP07000WG00 wei



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Date:				Thursday, March 09, 2017 Sheet 35 of 58 Rev 1.0

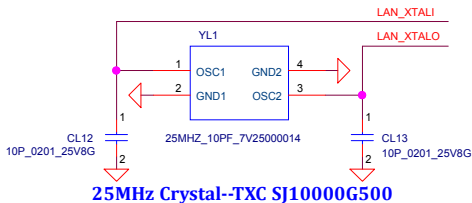
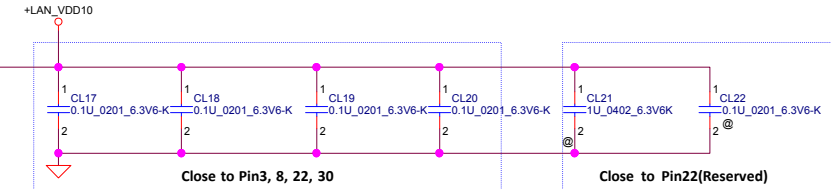
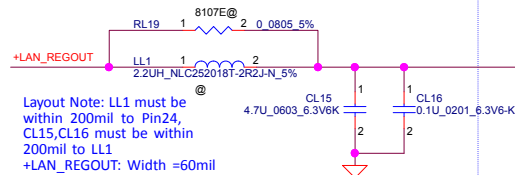
**+3VALW TO +3VALW\_LAN**

**+3VALW\_LAN rising time (10%~90%):**  
 $0.5ms \leq t_{pec} < 10\ 0m\ s$



CL10 close to Pin18  
 CL11 close to Pin17

**For RTL8111GUL SWR mode**  
**For RTL8111H /RTL 8107E (LDO mode) RL19 stuff f**

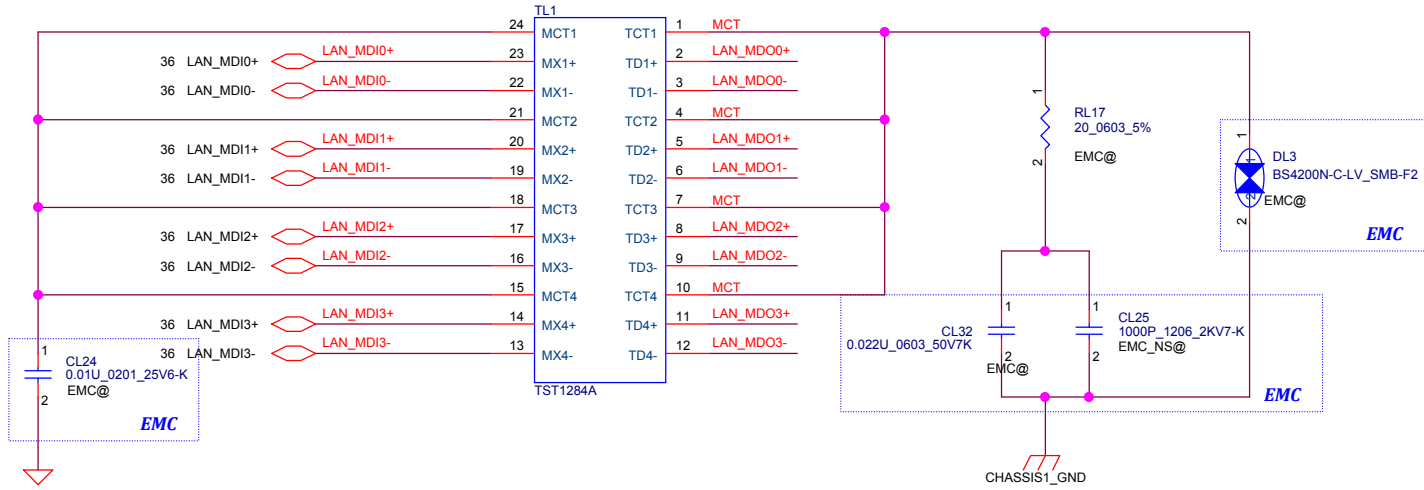
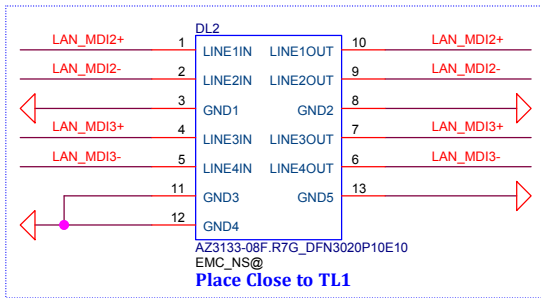
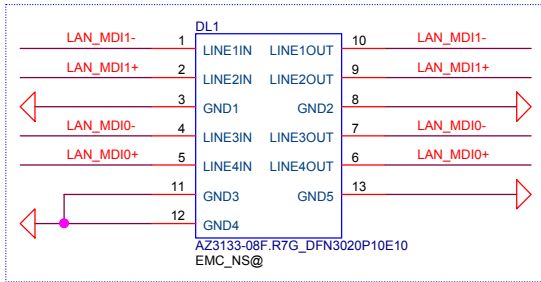


**25MHz Crystal--TXC SJ10000G500**

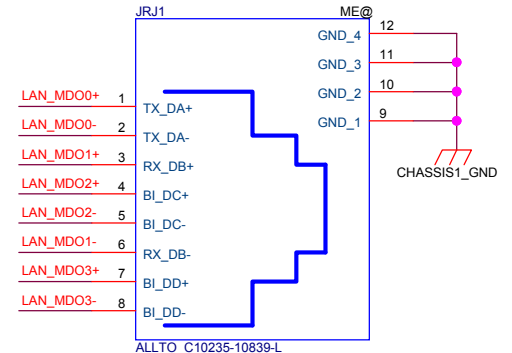
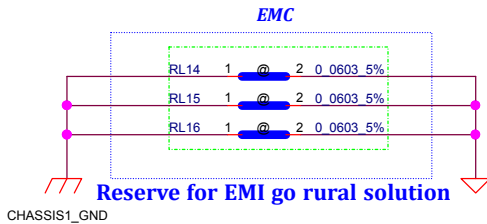
Follow common pool change 25MHz X'tal from EPSON to TXC. 03/01

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Issued Date		2013/08/08	Deciphered Date	2013/08/05	<b>LAN_RTL8106E</b>
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DL1/DL2  
1'S PN:SC300004X00



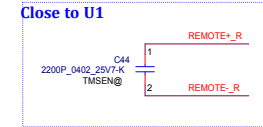
**change TL1 PN SP050008C00 to SP050009G00;  
TL1 is SP050008C00 footprint**



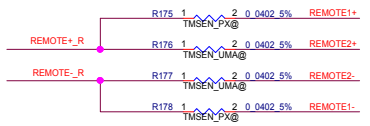
8/16 Update Rj45 P/N DC021608091 wei

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Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN_Transformer	
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**THERMAL SENSOR**

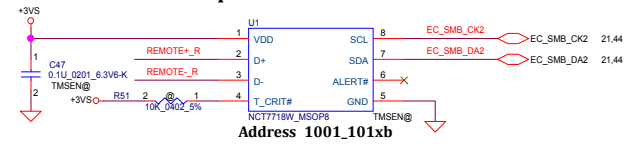


Set Thermal Sensor as a BOM Structure



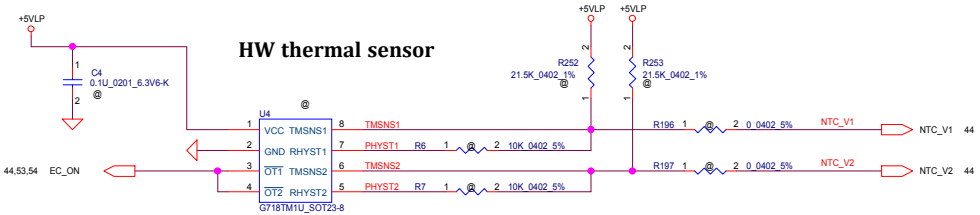
REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/Space:10/10 mil  
Trace length:<8"

**SMSC thermal sensor placed near DIMM**



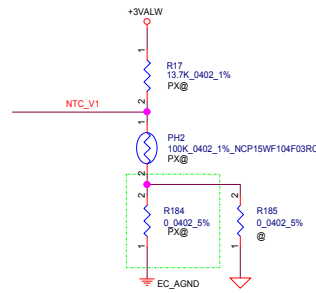
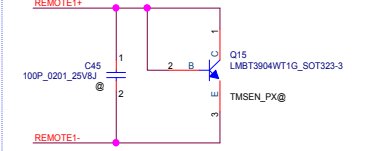
Address 1001\_101xb

**HW thermal sensor**

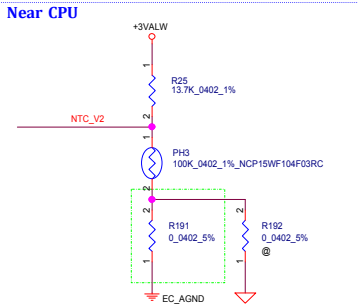
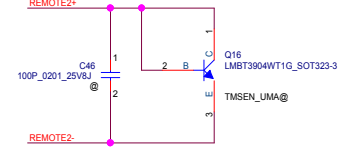


Over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C

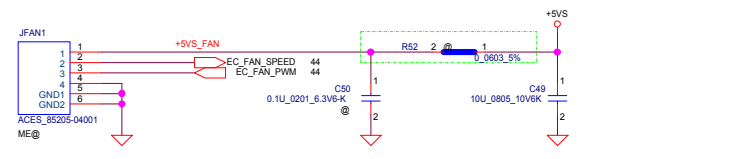
**Near GPU&VRAM**



**Near CPU Core**

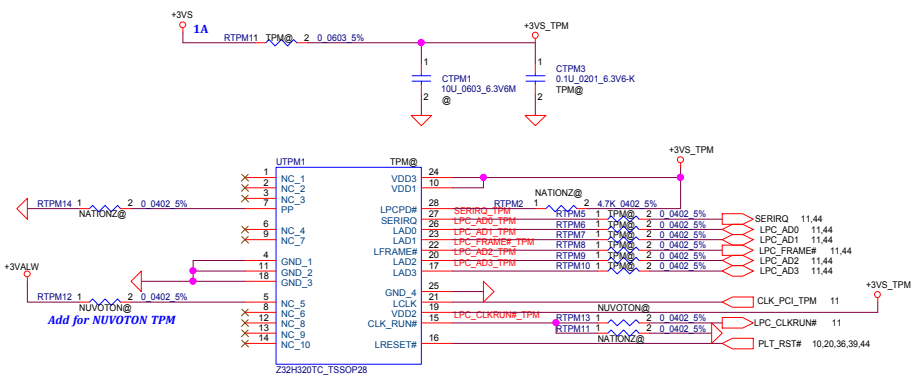


**FAN Conn**



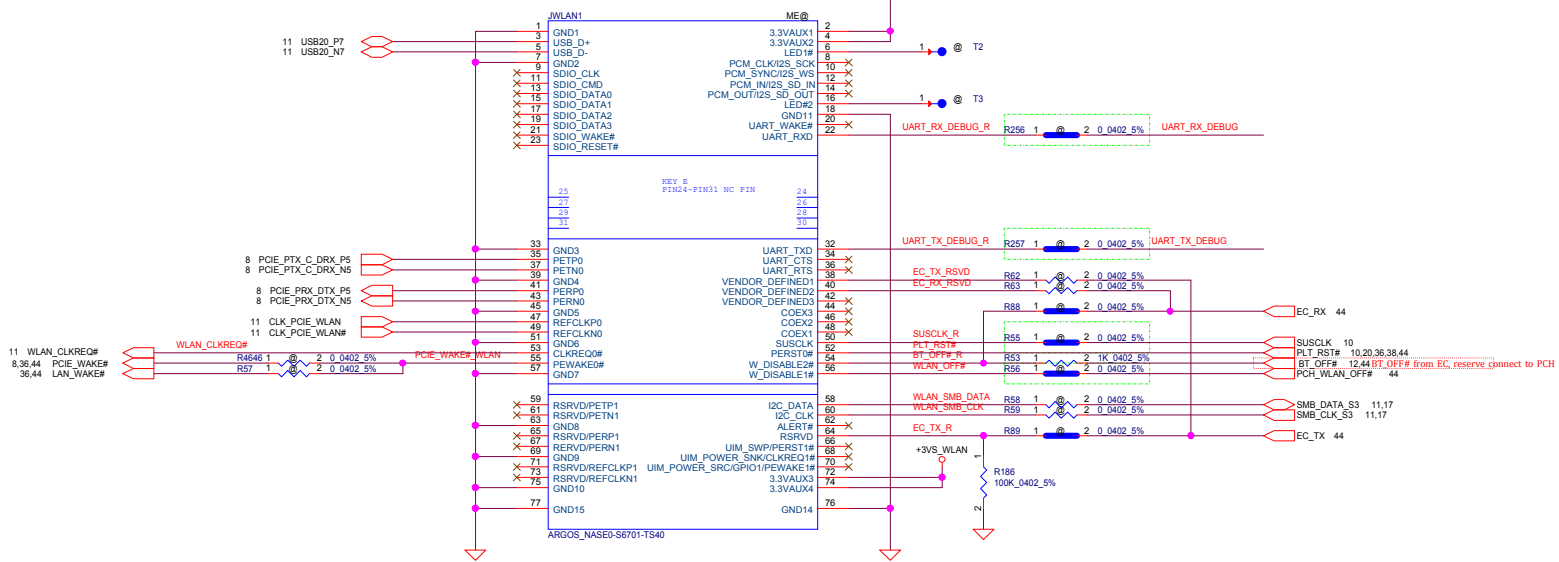
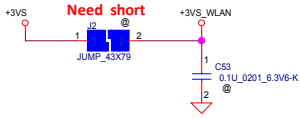
Update FAN conn. footprint to SP020008X0J  
SP020012200 main source is SP020008X0J  
Lewis 2016/10/14

**TPM**



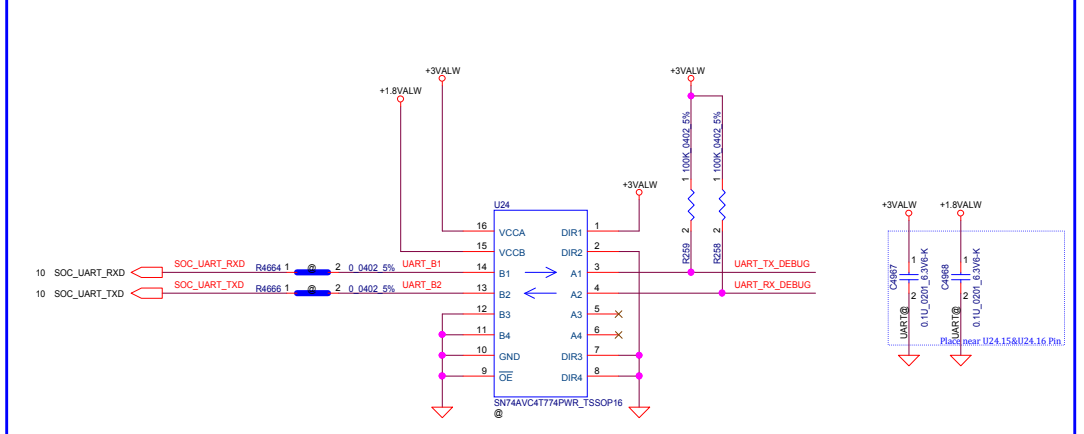
Security Classification				LC Future Center Secret Data				Title	
Issued Date		2013/08/08		Deciphered Date		2013/08/05		Thermal sensor/FAN CONN/TPM	
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# Mini-Express Card(WLAN/WiMAX)



8/16 Update Conn. P/N SP070013200 wei  
Copy DG421 symbol

## UART Transceiver



A

B

C

D

E

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Issued Date	2013/08/08	Deciphered Date	2013/08/05	<b>Blank</b>	
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				Rev	1.0

A

B

C


D

E



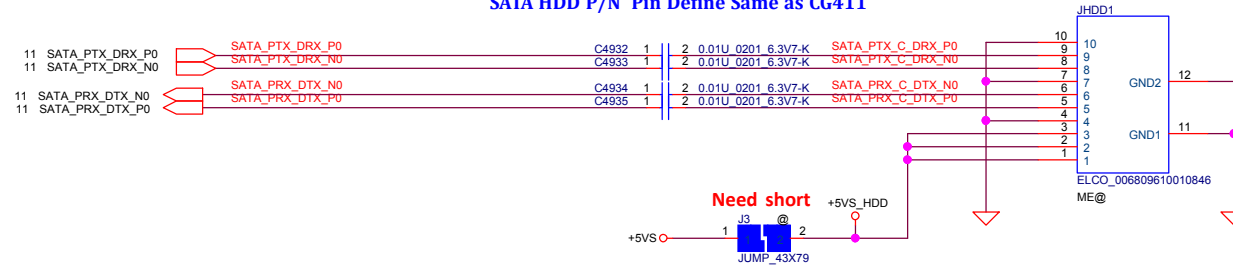


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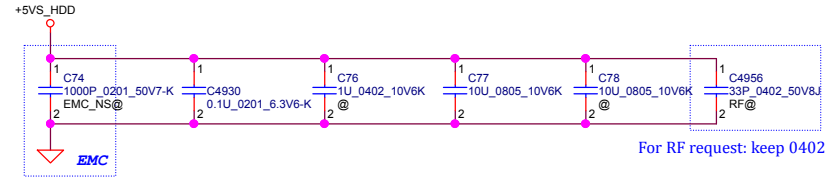
Title		
<b>Blank</b>		
Size	Document Number	Rev
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# SATA HDD Conn.

SATA HDD P/N Pin Define Same as CG411



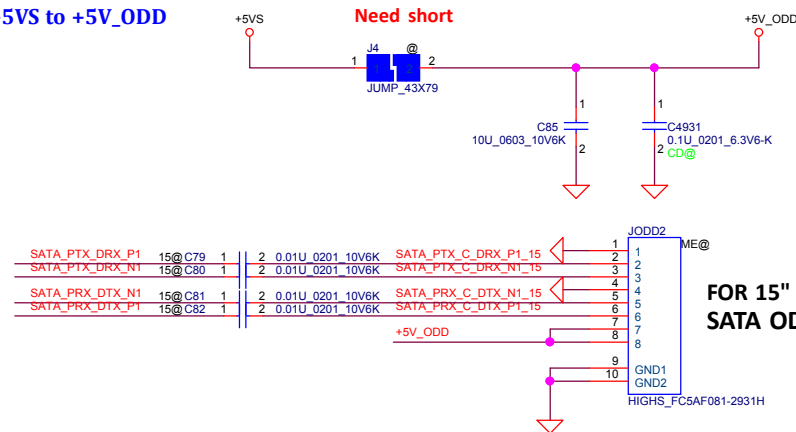
Need short



For RF request: keep 0402

+5VS to +5V\_ODD

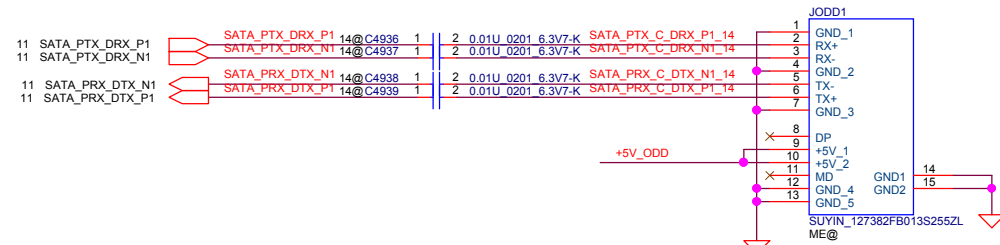
Need short



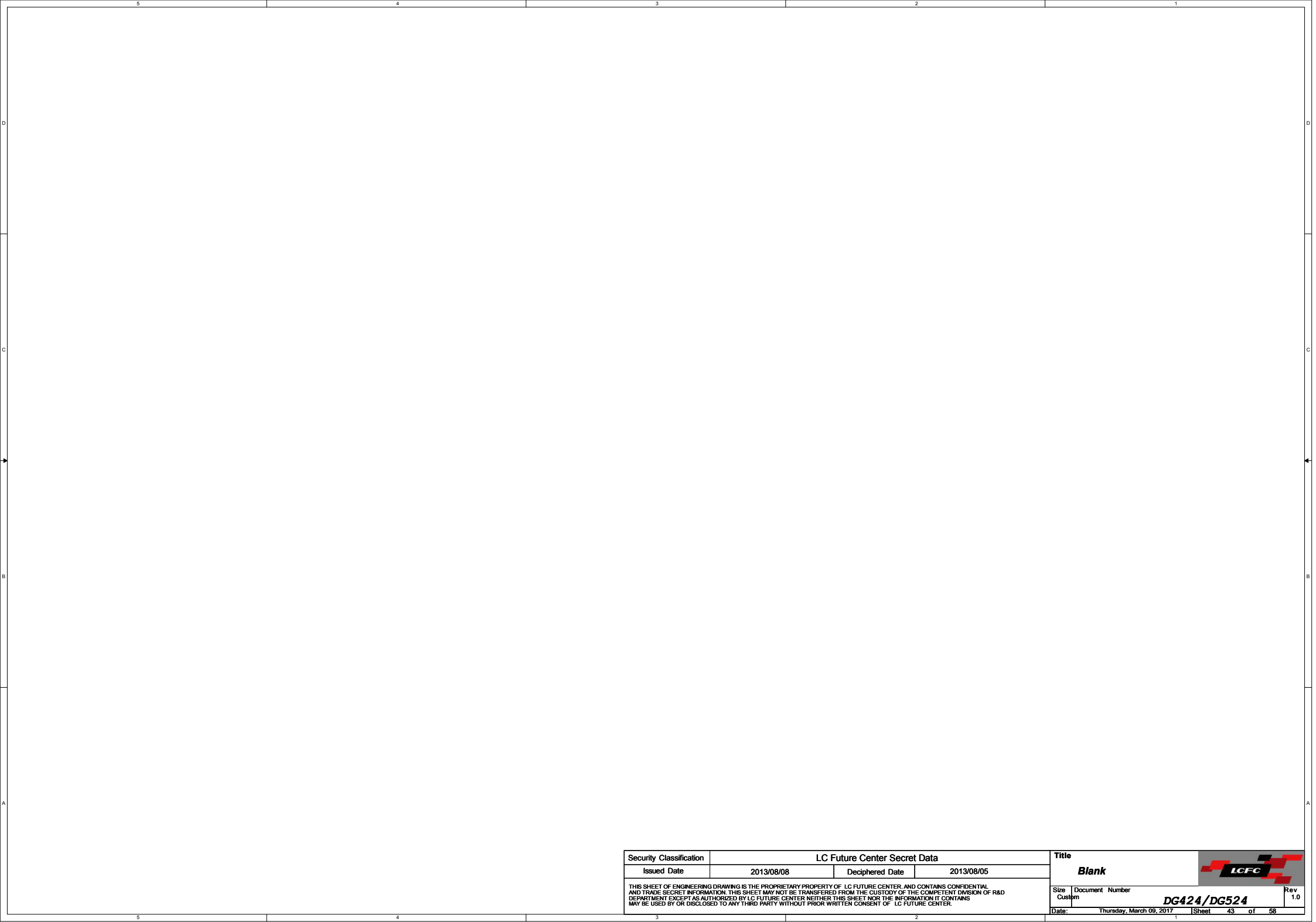
FOR 15" SATA ODD FFC Conn

8/16 Update Conn. P/N SP01001YV00 wei

FOR 14" SATA ODD Conn.



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C


C

B

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A

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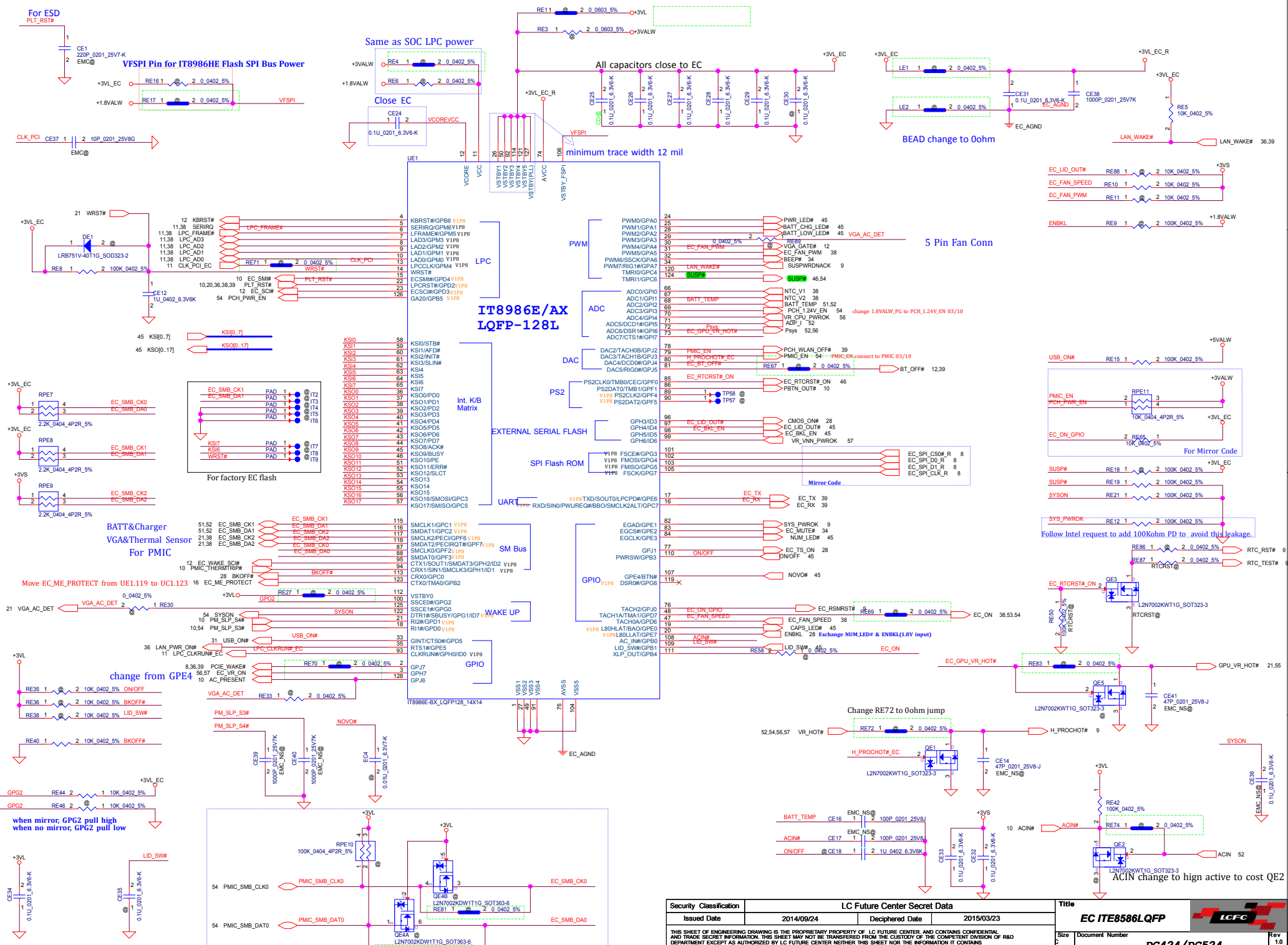
5


4

3

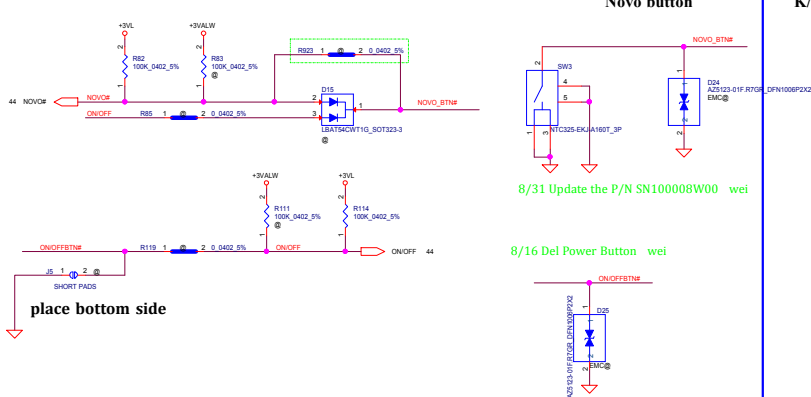
2

1

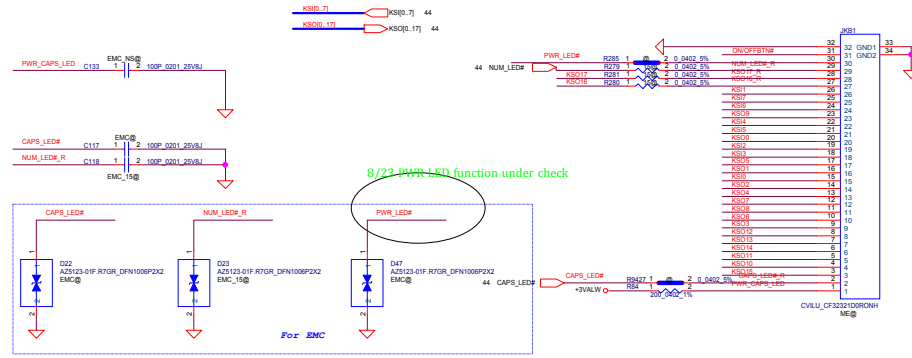


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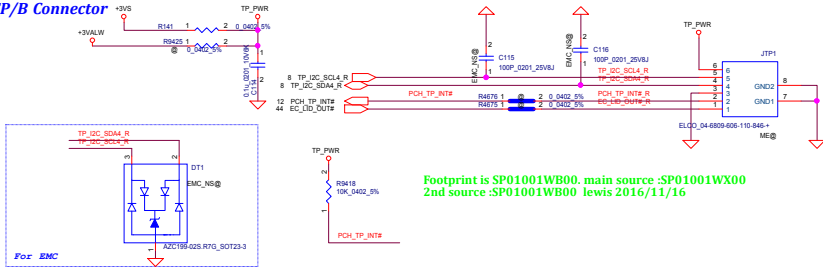
**ON/OFF switch**



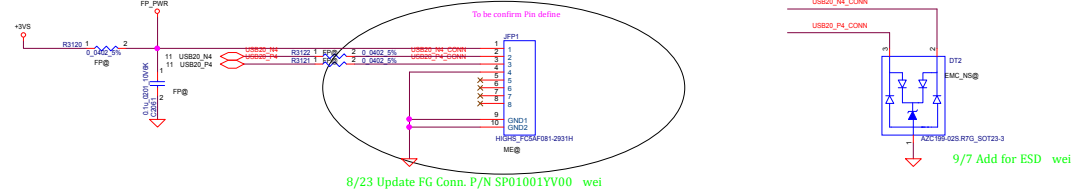
**K/B Connector**



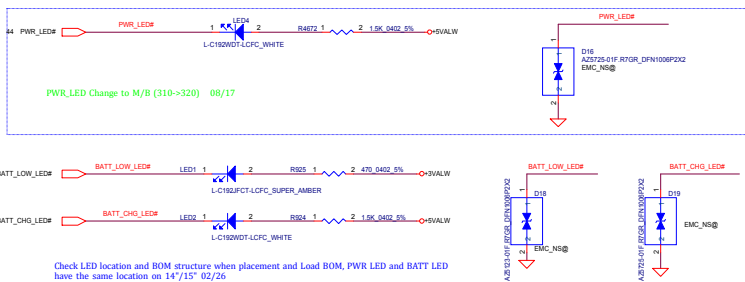
**TP/B Connector**



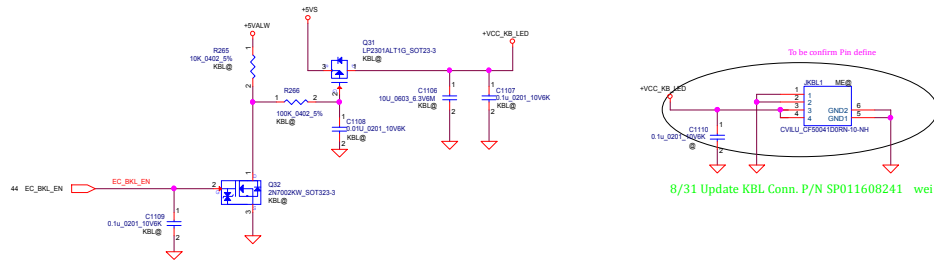
**Finger Print Connector**



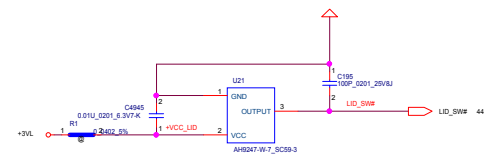
**LED**

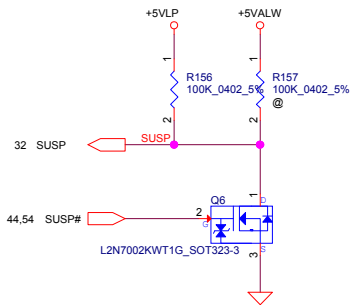


**KB Backlight Connector**

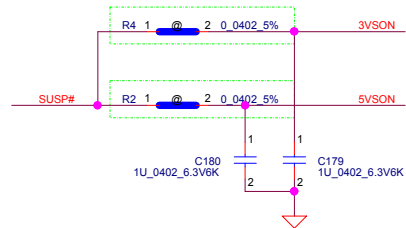


**LID Switch**



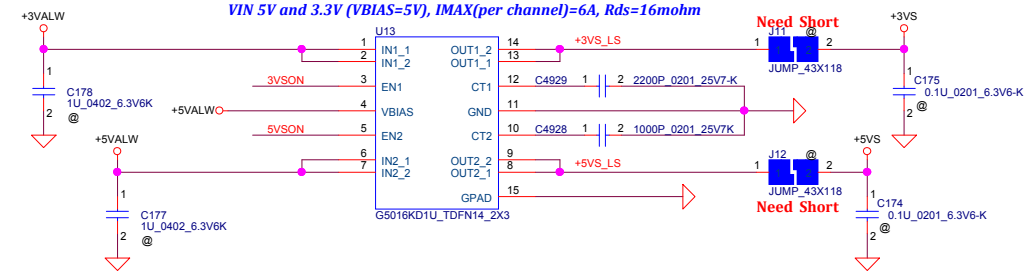


**+5VS/+3VS Load Switch**



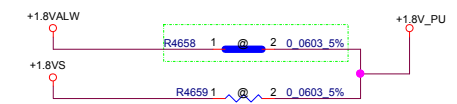
**Load Switch**  
 +5VALW To +5VS  
 +3VALW To +3VS

**modify load swtich from APL3523 to G5016KD1U TDFN 14P**  
 +3VS, C173 --> 2.78ms  
 +5VS, C176 --> 1.71ms

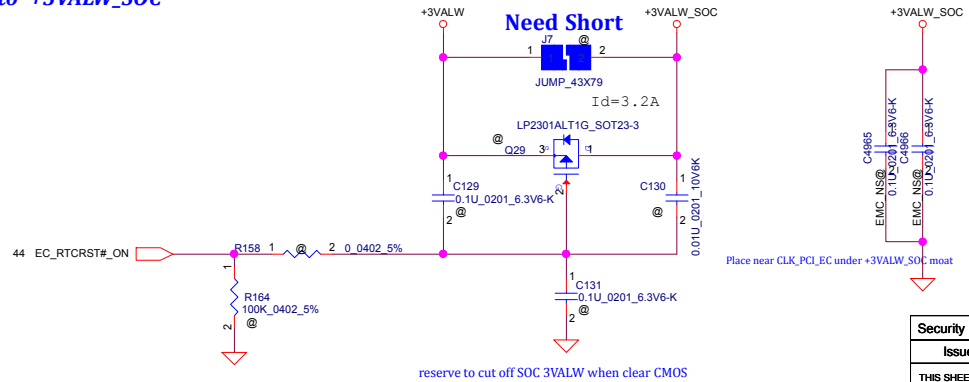


**Delete +3.3VALW to +1.5VS**

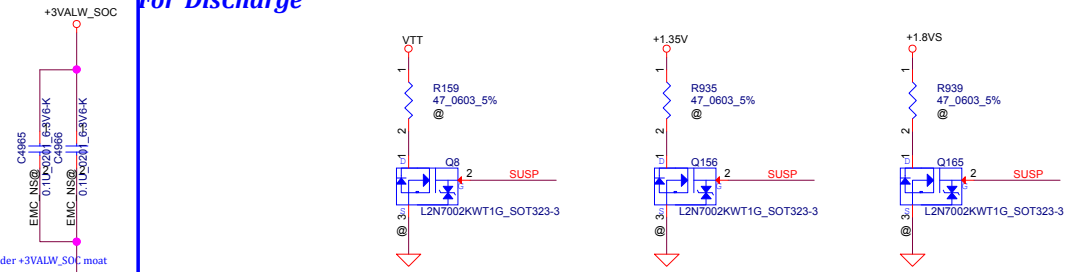
**+1.8V\_PU Power Rail**



**+3VALW to +3VALW\_SOC**



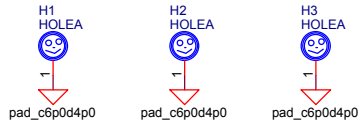
**For DisCharge**



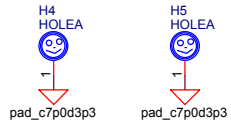
reserve to cut off SOC 3VALW when clear CMOS

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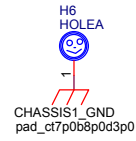
**CPU Thermal Holes3**



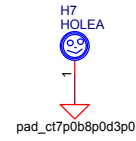
**GPU Thermal Holes2**



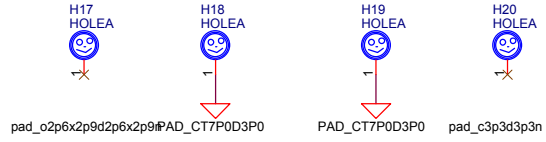
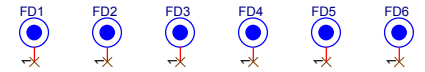
**Close to RJ45**



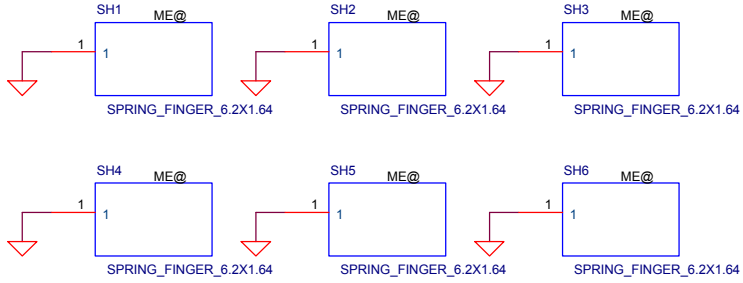
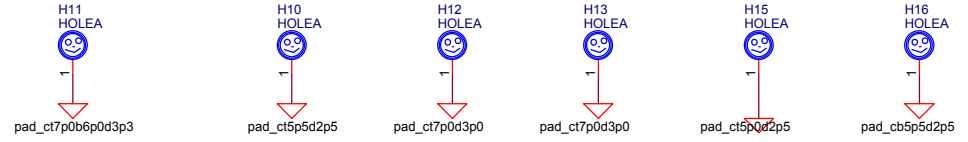
**Close to Audio jack**



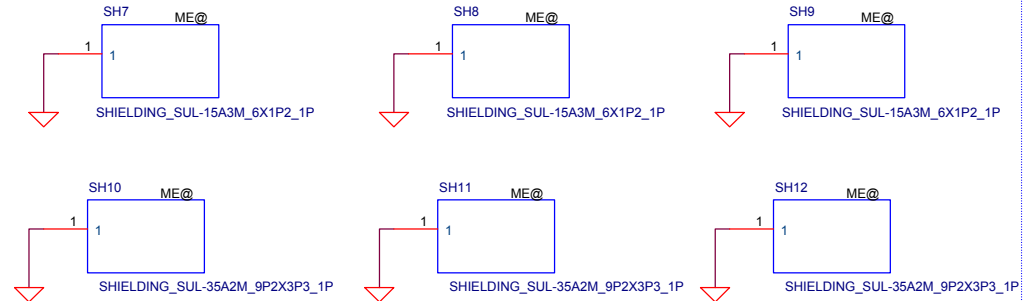
**PCB Federal Mark PAD**




**WLAN Standoff**

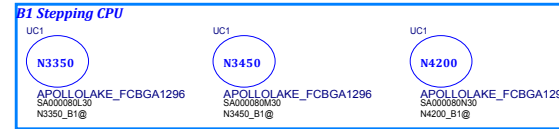
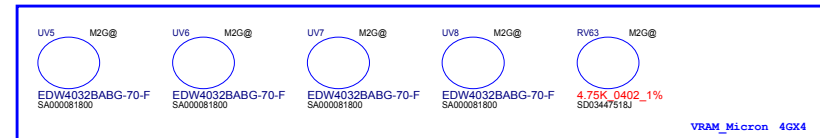
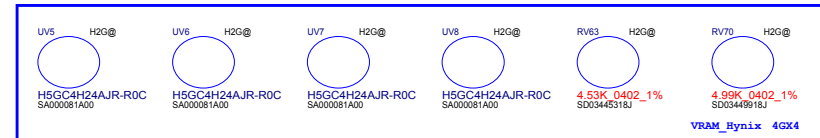
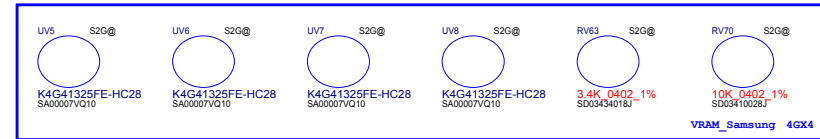
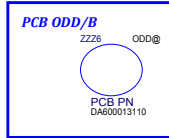
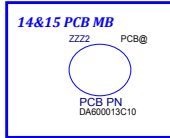
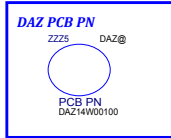
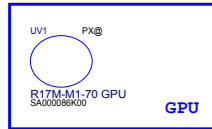
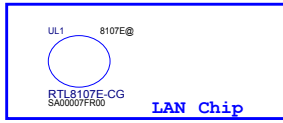
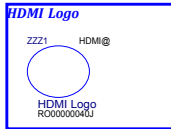


**USB3.0 Shielding**



**DDR3L Shielding**

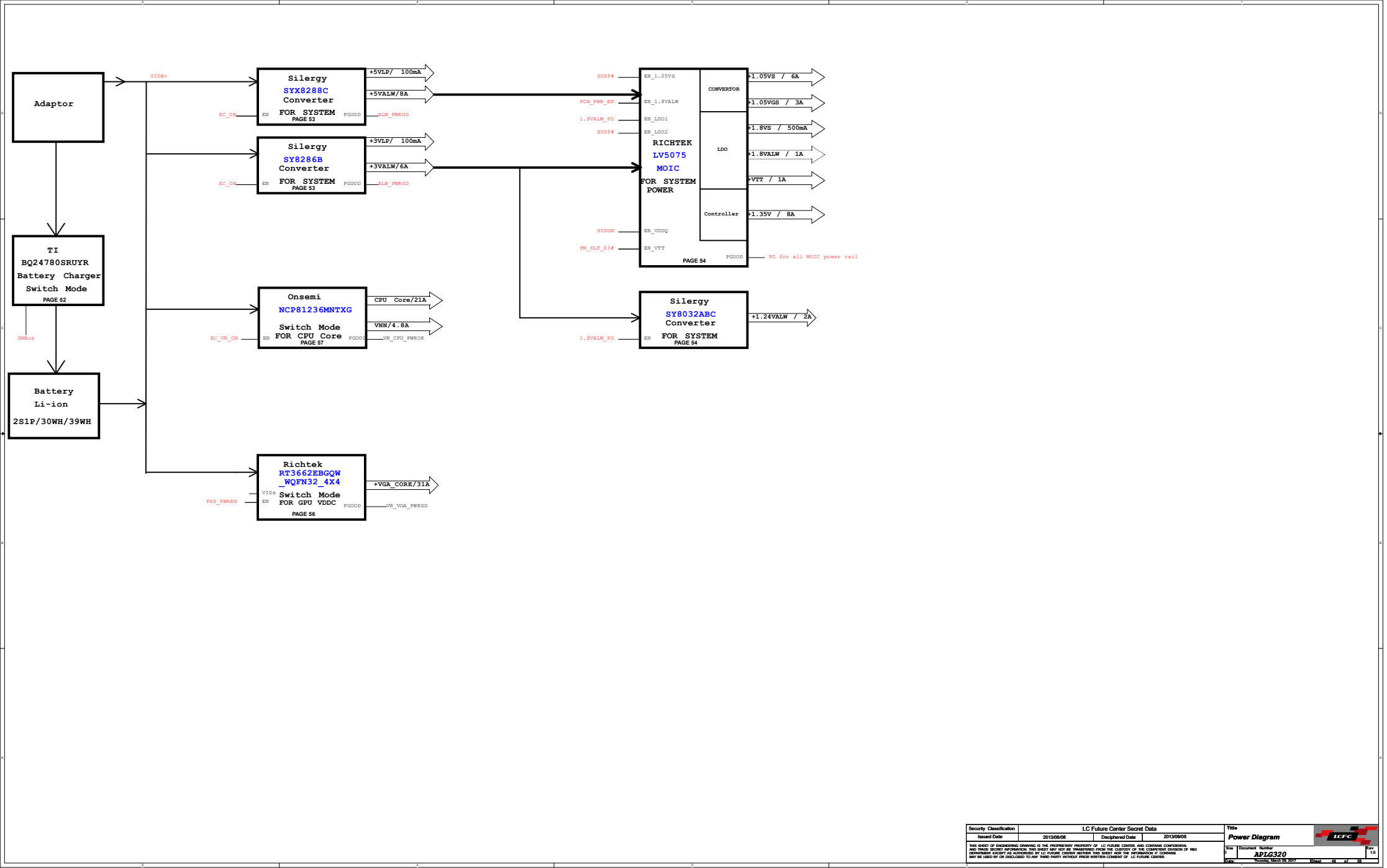
Security Classification	LC Future Center Secret Data			Title <b>Hole</b>	
Issued Date	2013/08/08	Deciphered Date	2013/08/05		
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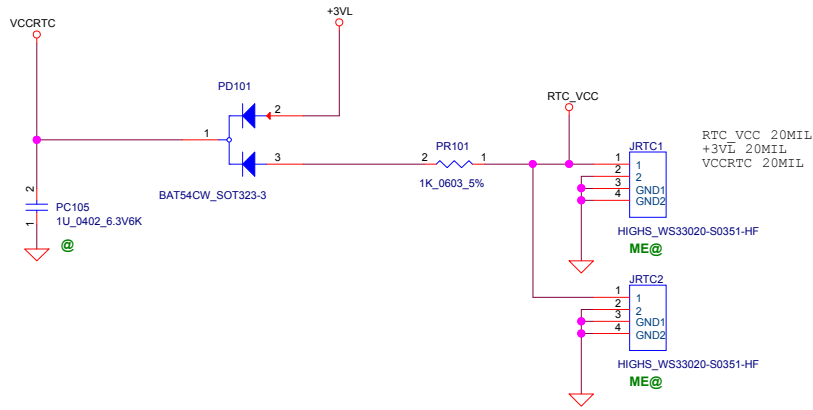
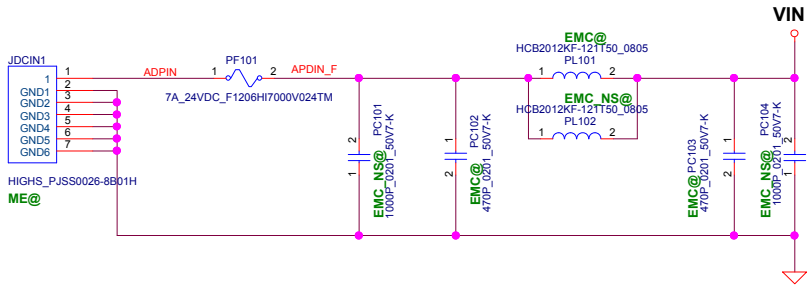


**VRAM ID config**

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC4H24AJR-R0C	100	4.53K	4.99K
	Micron EDW4032BABG-70-F	111	4.75K	NC
	Samsung K4G41325FE-HC28	110	3.4K	10K
		000	NC	4.75K
		010	4.53K	2K
		001	8.45K	2K







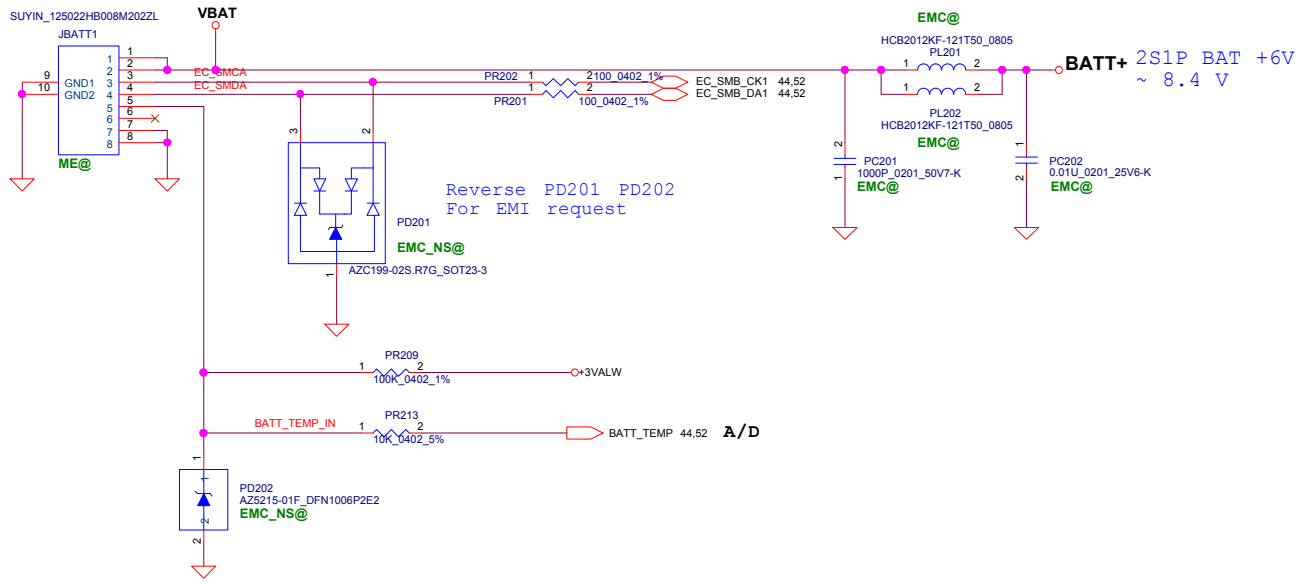
35mm cable

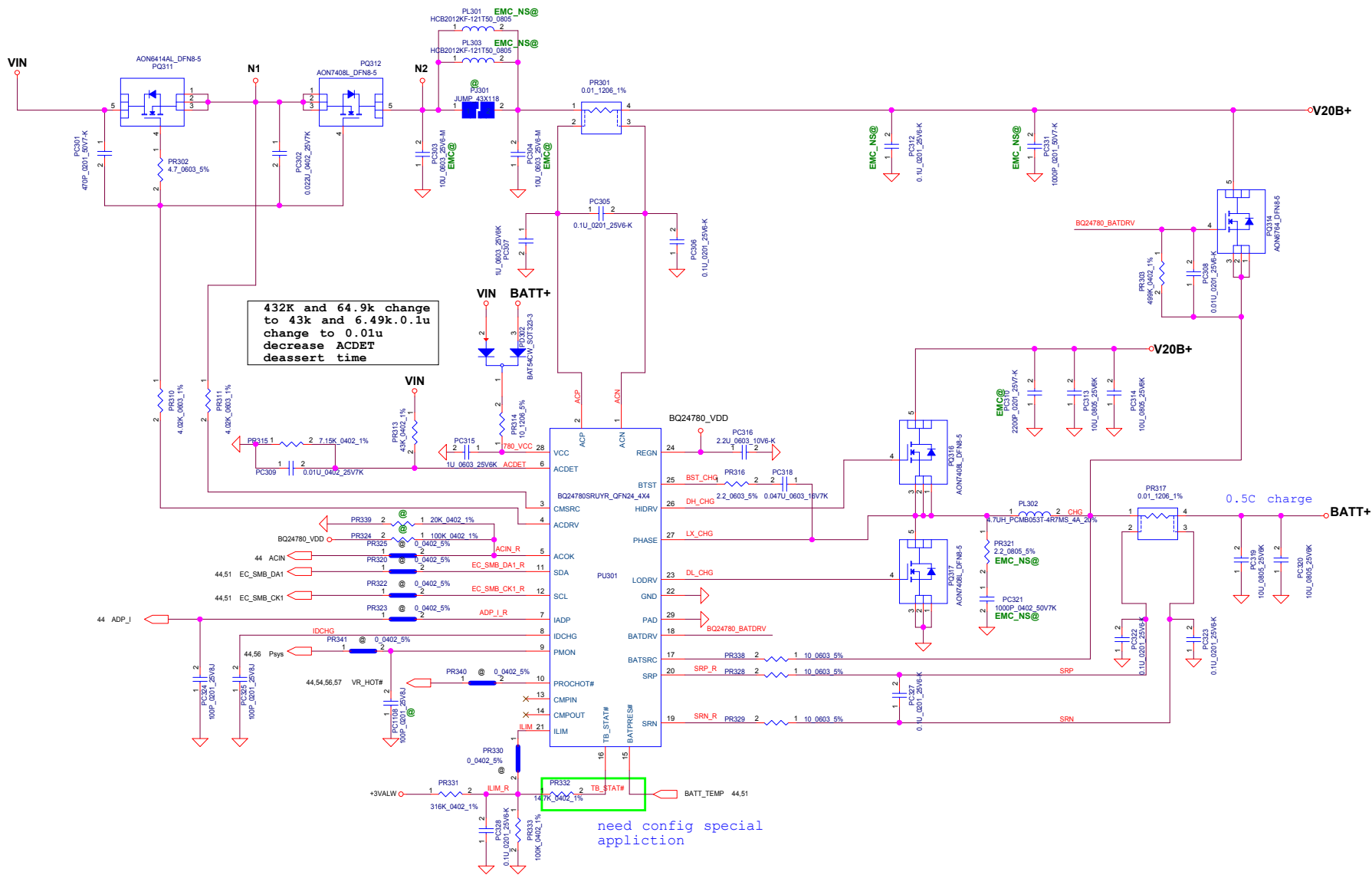
**RTC Battery for GCM BOM  
(2nd source and quoted price )**

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title		
PWR-DCIN / RTC charger		
Size	Document Number	Rev
Custom	APLG320	1.0
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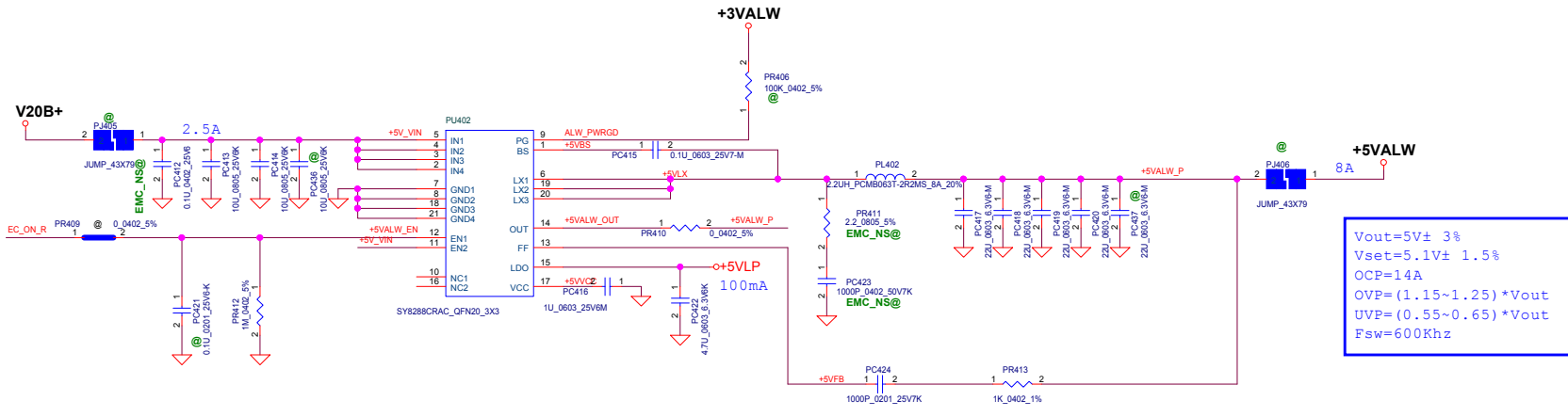
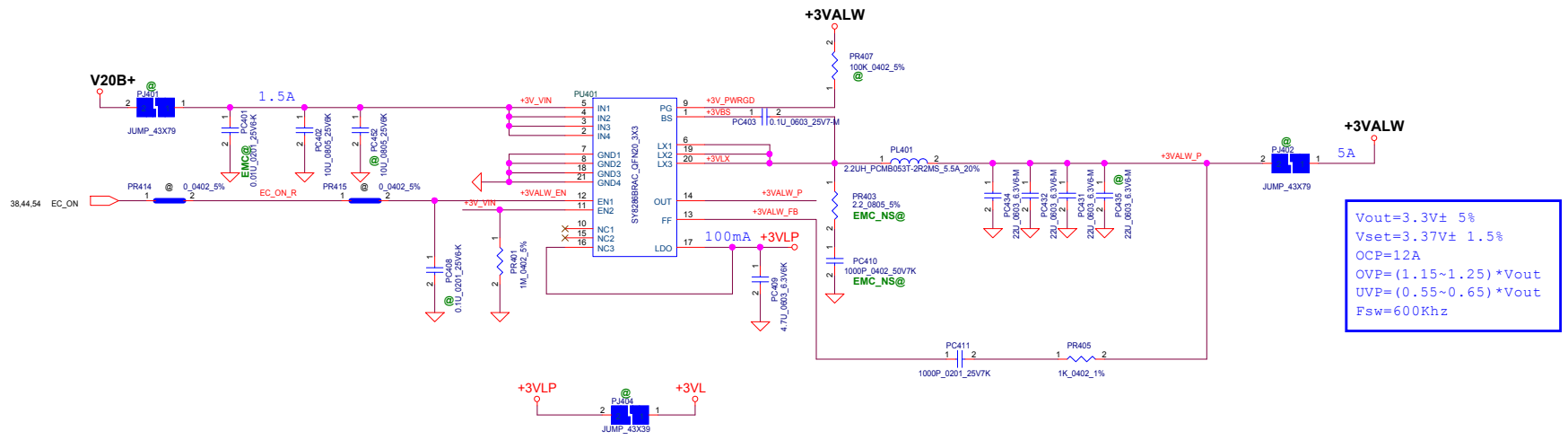
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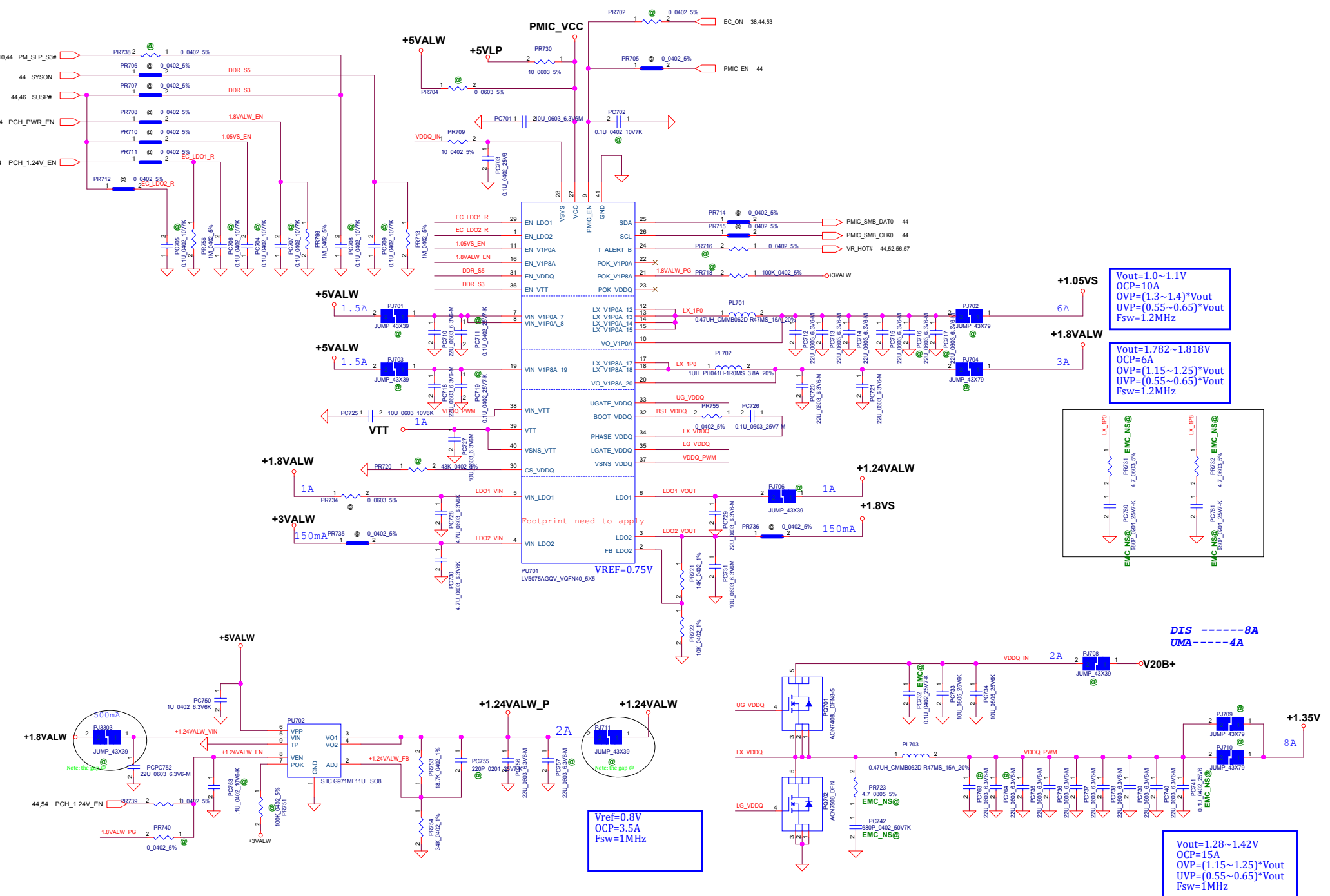


432k and 64.9k change to 43k and 6.49k. 0.1u change to 0.01u decrease ACDET deassert time

need config special application

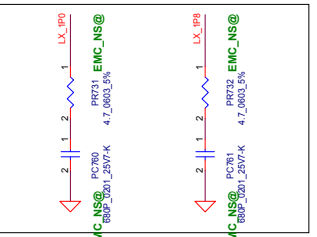


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Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR_3VALW/5VALW	
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$V_{out}=1.0\sim 1.1V$   
 $OCP=10A$   
 $OVP=(1.3\sim 1.4)*V_{out}$   
 $UVP=(0.55\sim 0.65)*V_{out}$   
 $Fsw=1.2MHz$

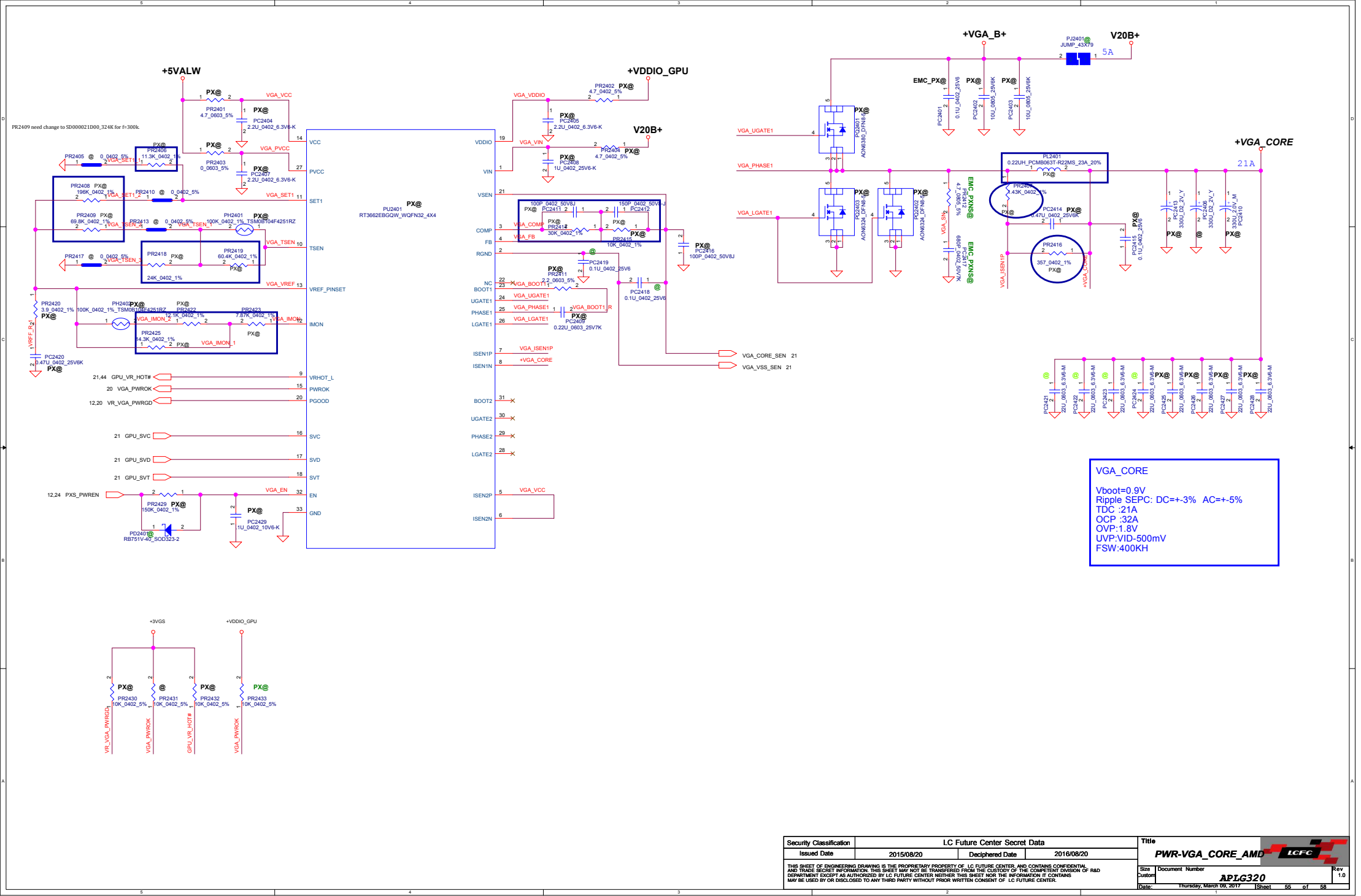
$V_{out}=1.782\sim 1.818V$   
 $OCP=6A$   
 $OVP=(1.15\sim 1.25)*V_{out}$   
 $UVP=(0.55\sim 0.65)*V_{out}$   
 $Fsw=1.2MHz$

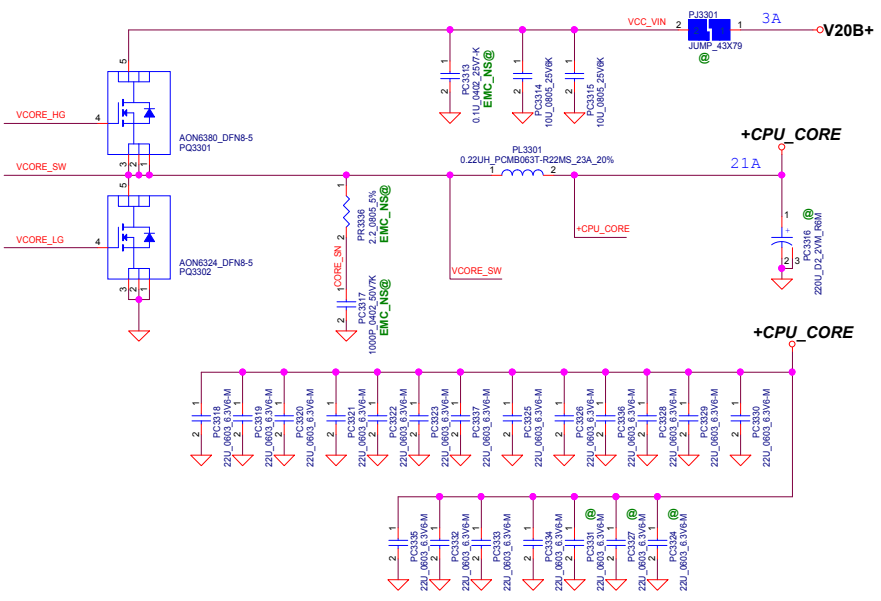
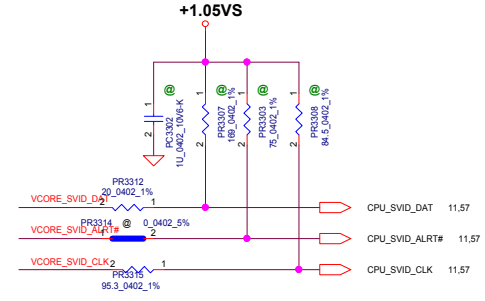
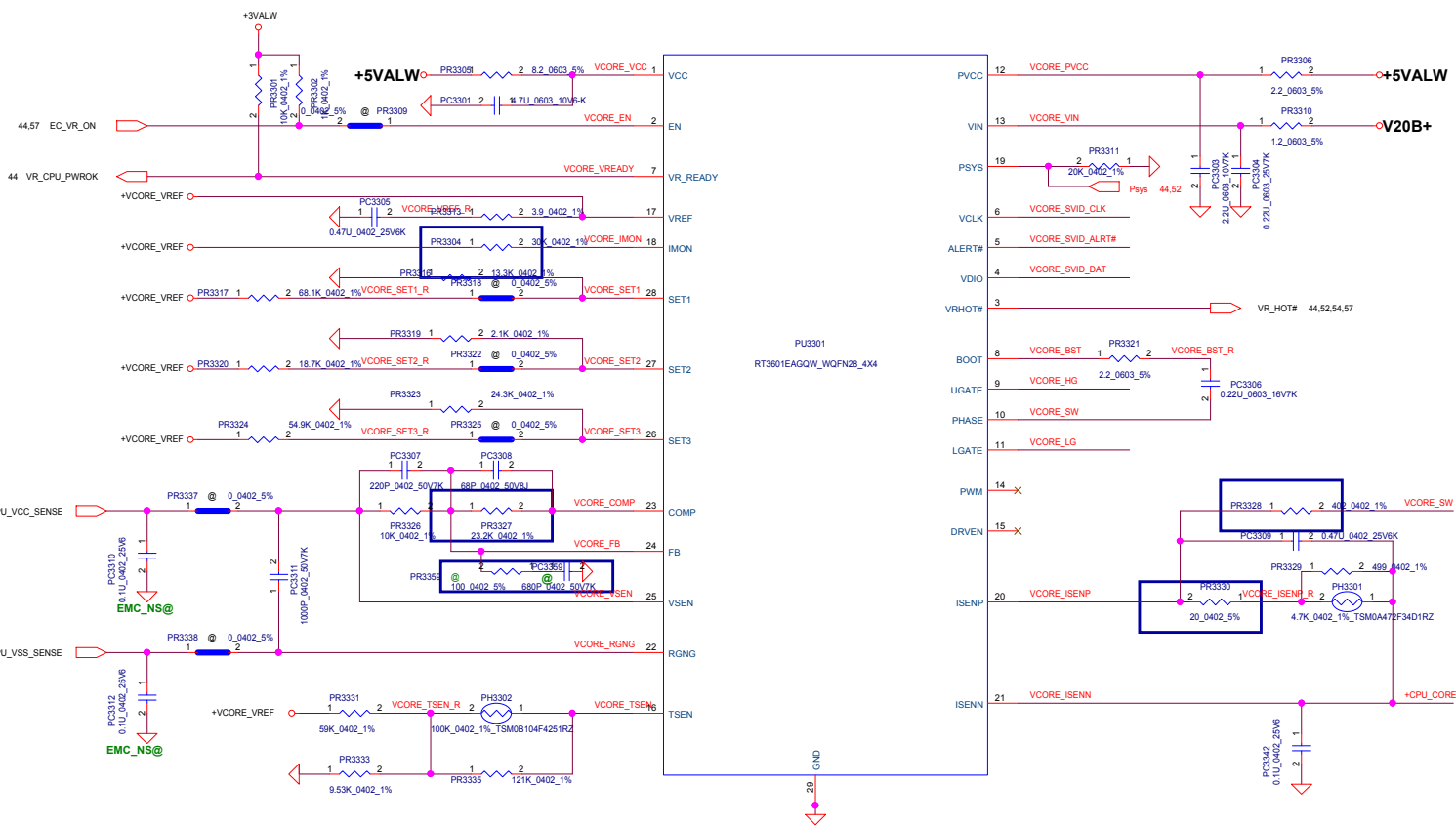


DIS -----8A  
 UMA-----4A

$V_{out}=1.28\sim 1.42V$   
 $OCP=15A$   
 $OVP=(1.15\sim 1.25)*V_{out}$   
 $UVP=(0.55\sim 0.65)*V_{out}$   
 $Fsw=1MHz$

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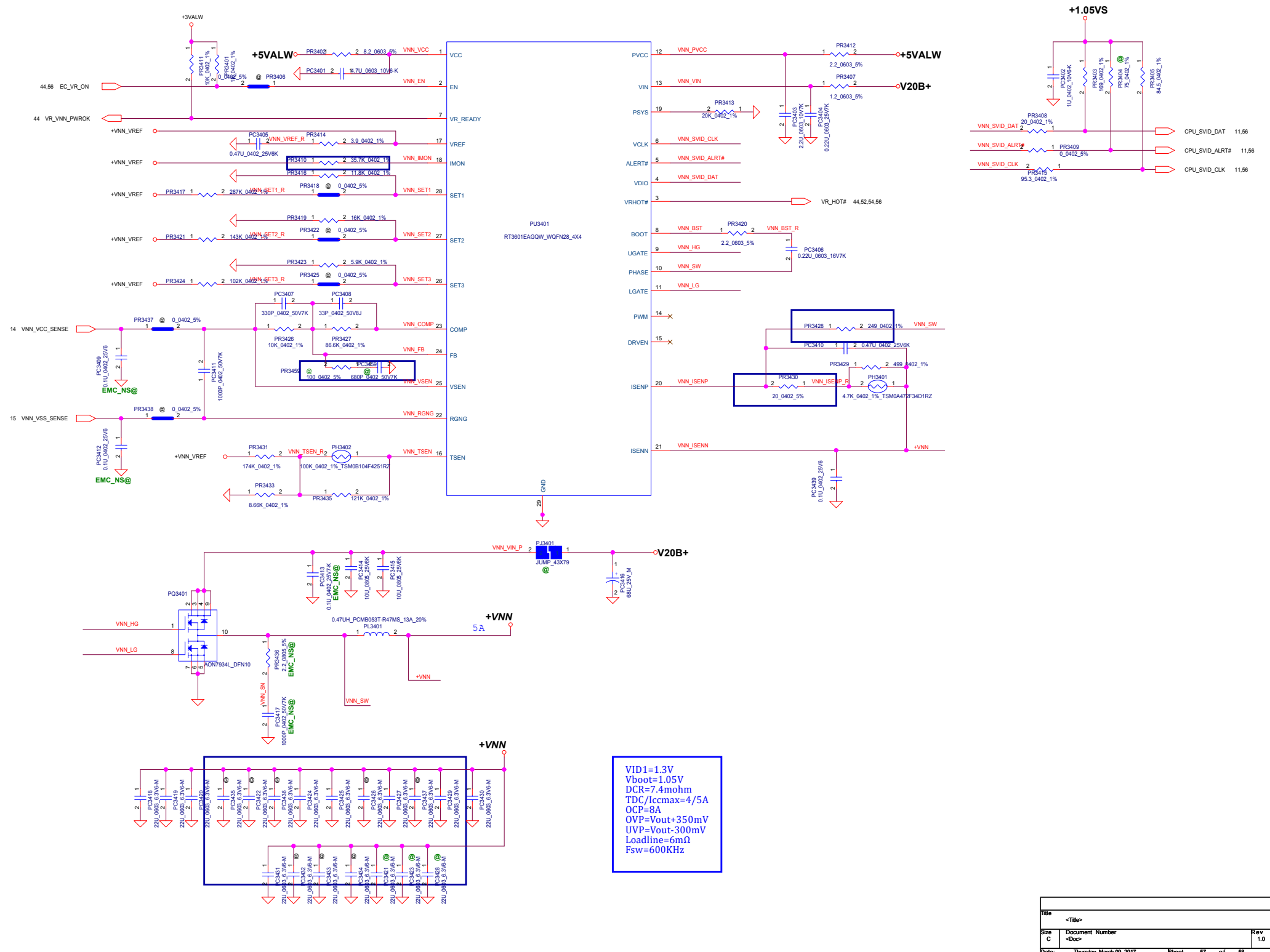




VID1=1.3V  
 Vboot=0V  
 DCR=2.5mohm  
 TDC/Iccmax=18/21A  
 OCP=33.6A  
 OVP=Vout+350mV  
 Loadline=6mΩ  
 UVP=Vout-300mV  
 Fsw=600KHz

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR	
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				Rev 1.0	





VID1=1.3V  
 Vboot=1.05V  
 DCR=7.4mohm  
 TDC/Iccmax=4/5A  
 OCP=8A  
 OVP=Vout+350mV  
 UVP=Vout-300mV  
 Loadline=6mΩ  
 Fsw=600KHz

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C	<Doc>	
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20161216:SDV to SIT

- 1.p56-p57 add R=100ohm,C=680pF in FB pin;
- 2.pr3324 change to 55,4kohm,pr3323 change to 24.3k;
- 3.VNN pr3430 from 0ohm change to 20ohm, pr3428 from 210 change to 249ohm,pr3410 from 34k to 35.7k;
- 4.Vcore pr3330 from 0ohm change to 20ohm, pr3328 change from 287ohm to 402ohm,pr3327 change from 28.7k to 23.2k, pr3304 change from 24k to 30k;
5. GPU change 14 items to support AMD request.

20161219:SDV to SIT

- 1.DEL 8pcs MLCC for VNN test result.(PC3422,PC3426,PC3434,PC3436,PC3437,PC3432,PC3435,PC3433)

20161226:SDV to SIT

1. PMIC change 1.24V Vin from 3VALW to 1.8VALW;
- 2.change PR2431 from PX@ to @, PR2433 from @ to PX@,
- 3.change PR734 to @.

20170104:SDV to SIT

1. PMIC change LV5075B TO LV5075A

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Custom	APLG320			1.0	
Date:	Thursday, March 09, 2017		Sheet	58	of 58