

# PHQAA

## Marseille 10R/10RG

### LA-6832P REV 0.2 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)  
2010-09-03 Rev 0.1

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**Intel CPU**  
Sandy Bridge

rPGA-989  
37.5mm\*37.5mm

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200pin DDRIII-SO-DIMM X2

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DMI X4  
5GT/s

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USB port 2  
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FingerPrinter  
USB port 8  
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Felica  
USB port 9  
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Int. Camera  
USB port 11  
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**Intel PCH**  
Cougar Point - M

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25mm\*25mm

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USB  
5V 480MHz

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5V 3GHz(300MB/s)

PCIe 1x  
1.5V 5GT/s

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PCIeMini Card  
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PCIeMini Card  
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SATA ODD  
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TP & Light Pipe/B  
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Cap Sensor  
& Light Sensor/B  
LS-6062P  
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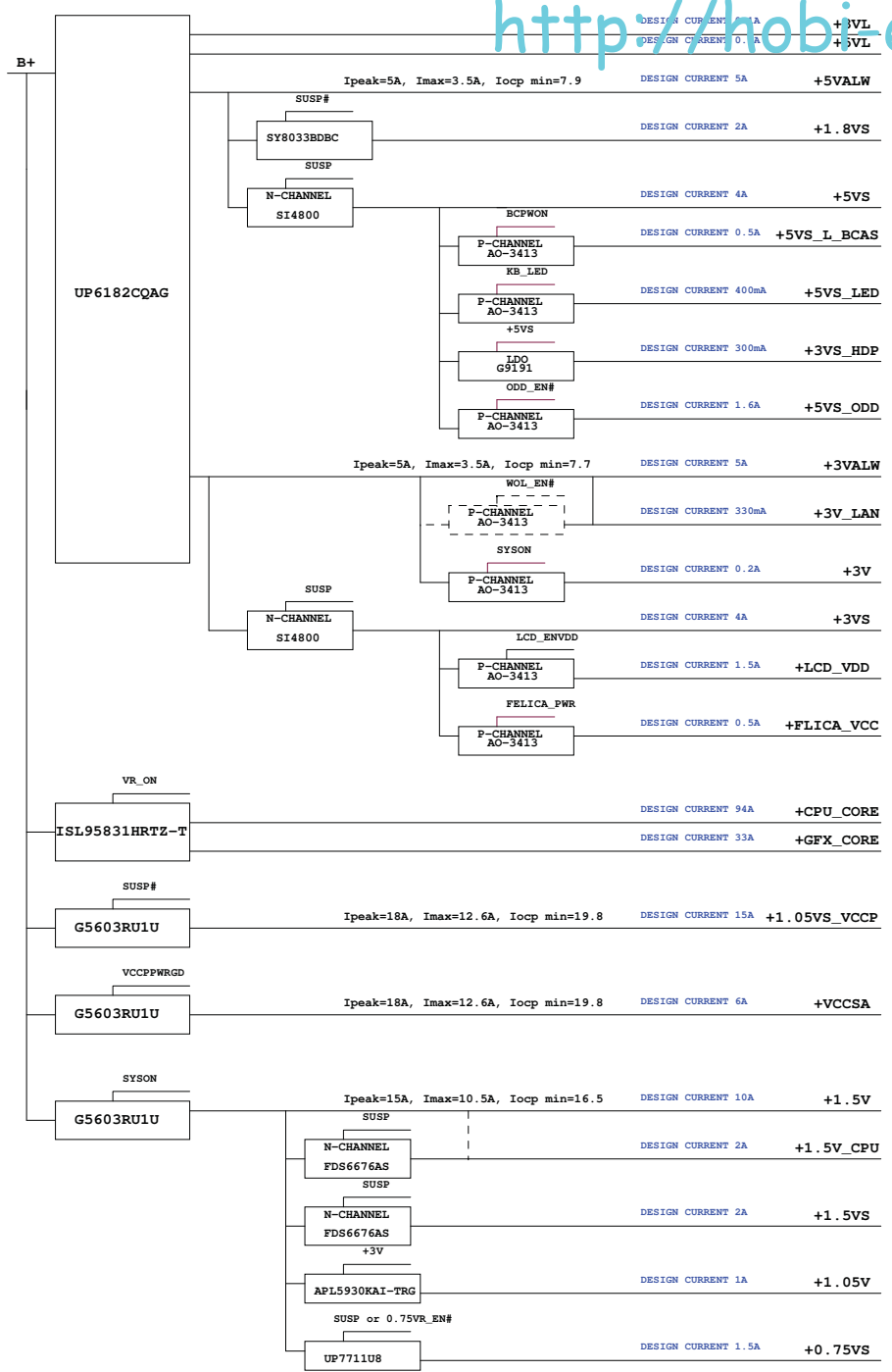
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LS-6063P  
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Audio & USB/B  
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Finger Printer/B  
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DA300006JM0  
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**Voltage Rails**

( O MEANS ON X MEANS OFF )

power plane / State	+RTCVC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

**BTO Option Table**

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@

Function	S3 Power Saving			GPU				
description	S3 Power Saving			N11P & N11E			N11M	
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

**PCH SM Bus Address**

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

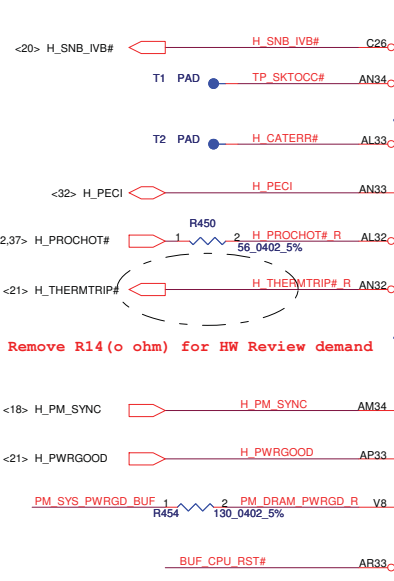
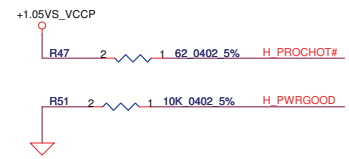
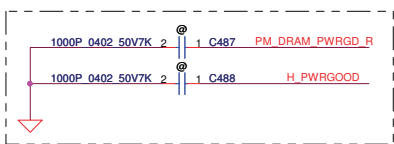
**EC SM Bus1 Address**

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
+3VL	Cap. Sensor		Virtual I2C

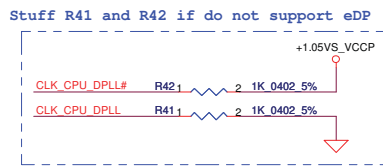
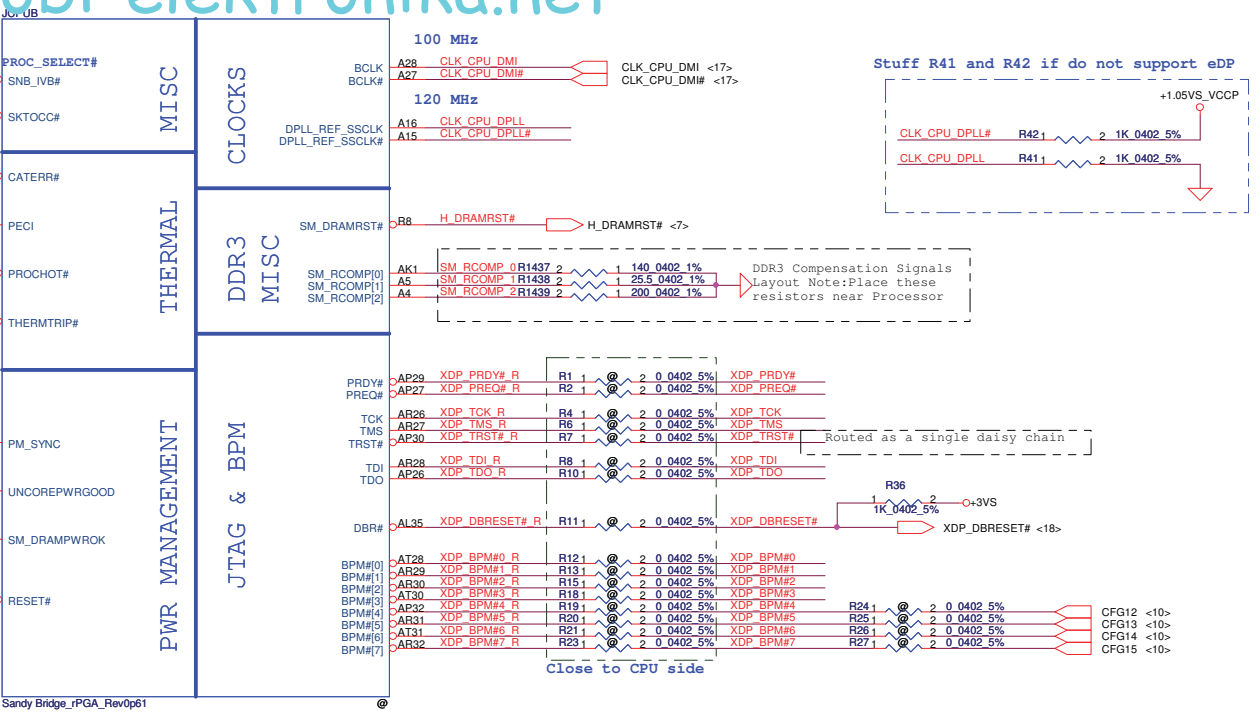
**EC SM Bus2 Address**

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW



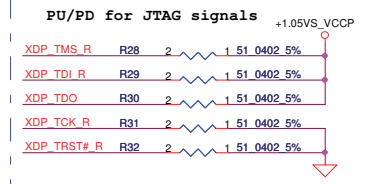
Remove R14 (0 ohm) for HW Review demand



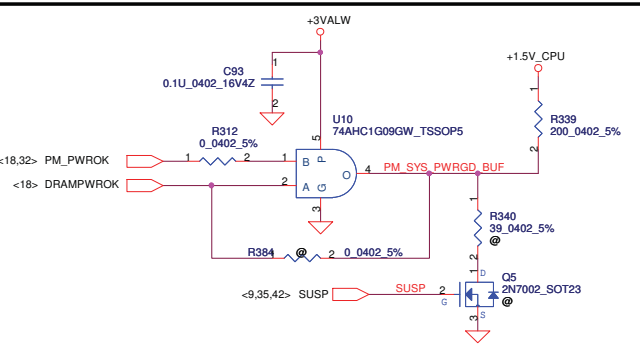
DDR3 Compensation Signals  
Layout Note: Place these resistors near Processor

Routed as a single daisy chain

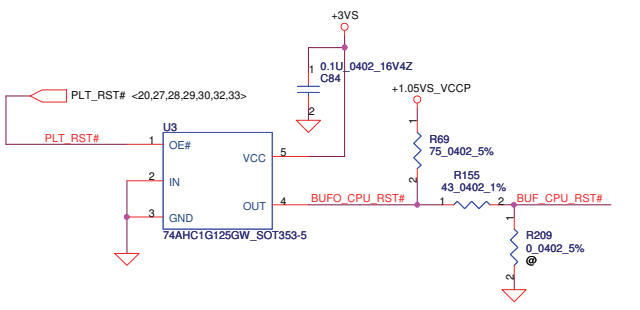
Close to CPU side



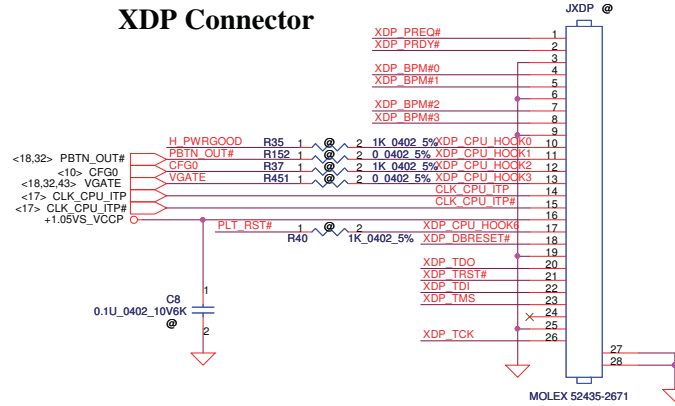
PU/PD for JTAG signals



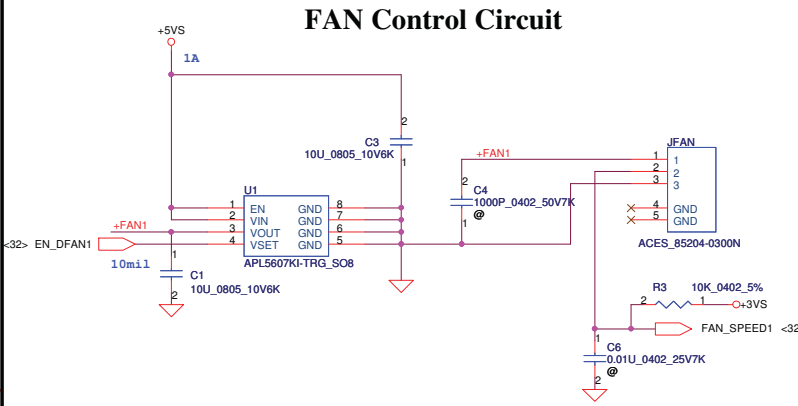
Buffered Reset to CPU



XDP Connector

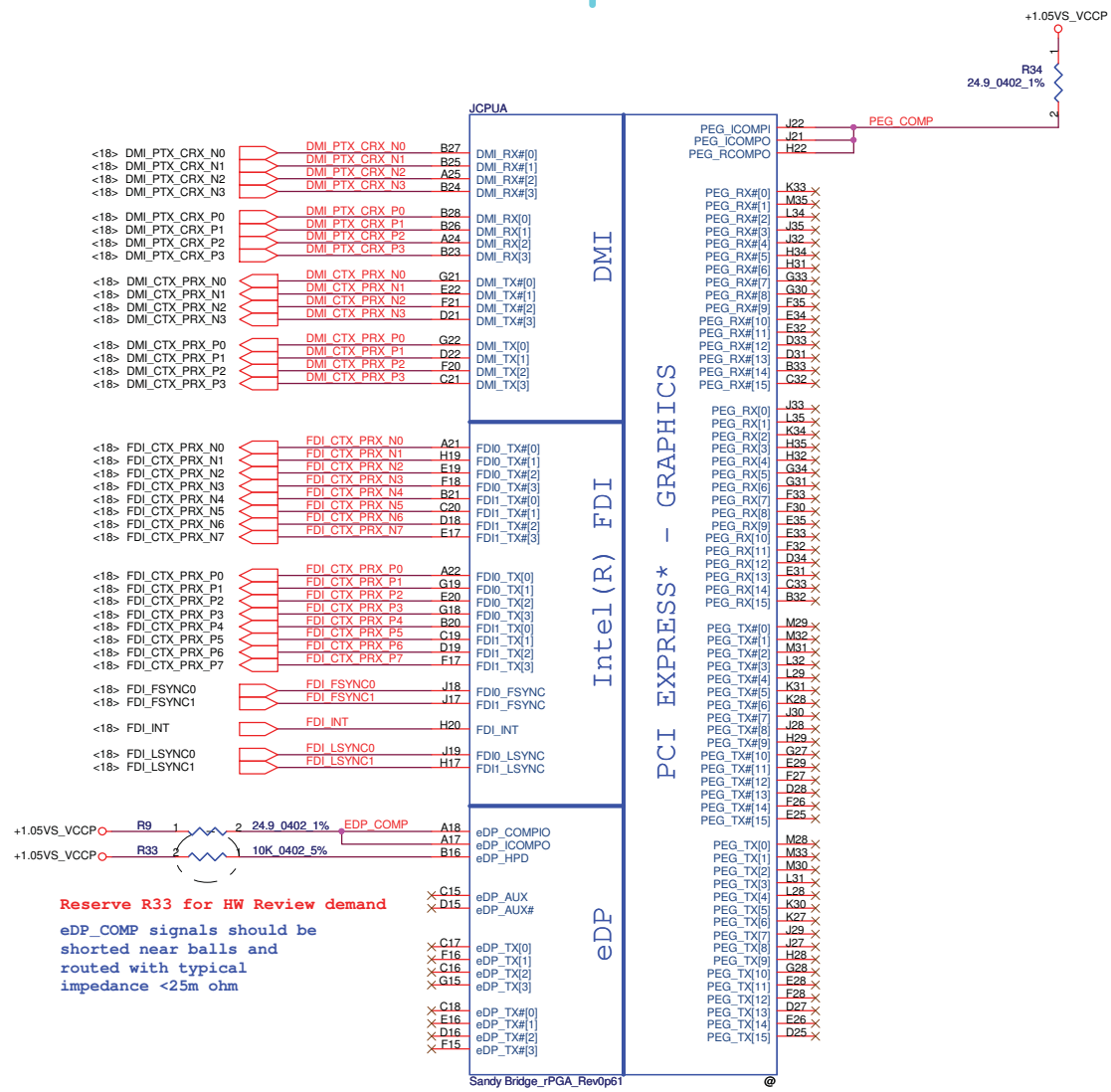


FAN Control Circuit

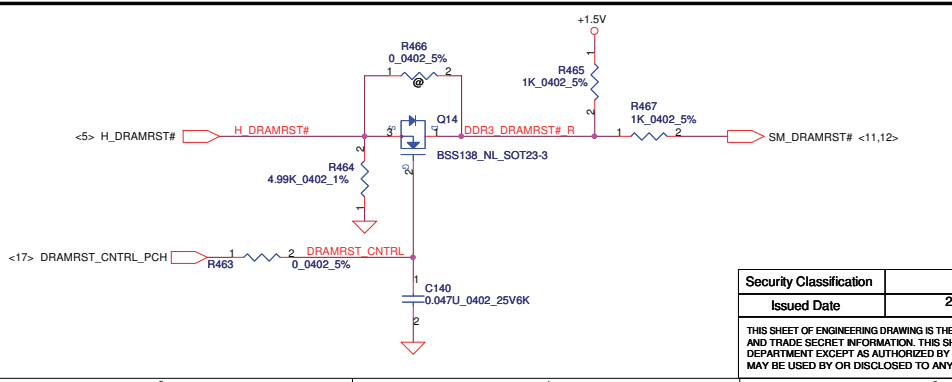
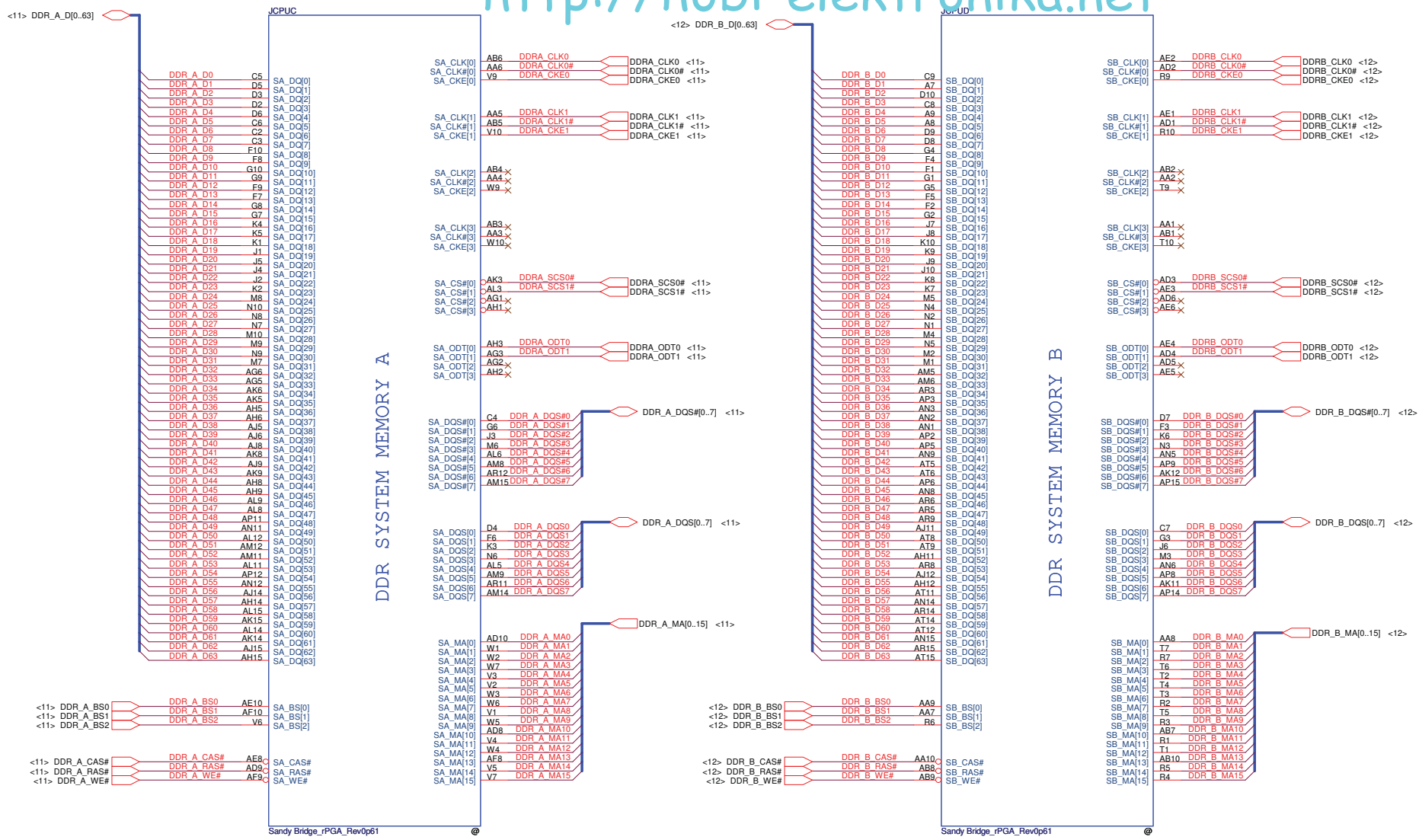


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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)



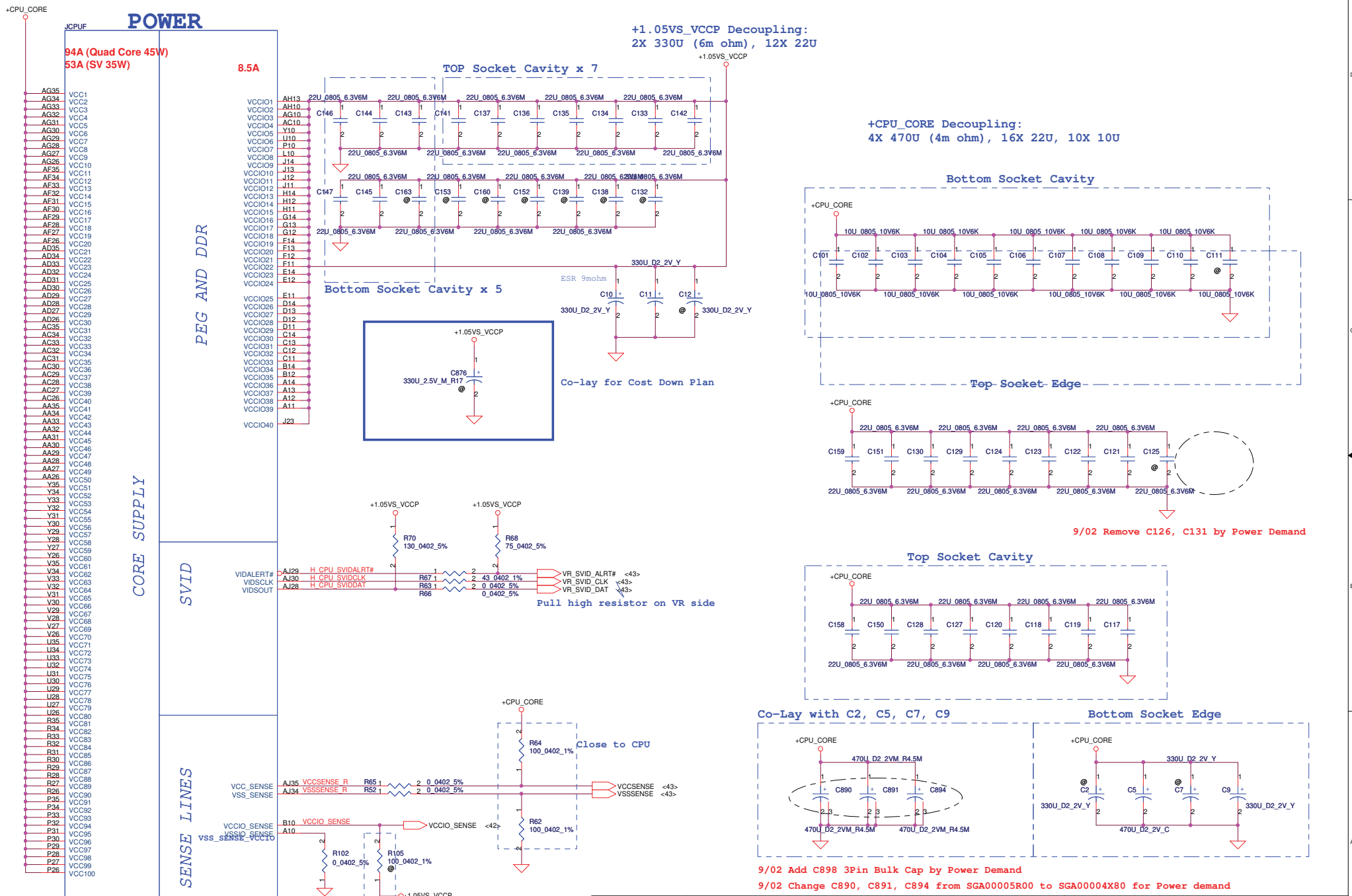
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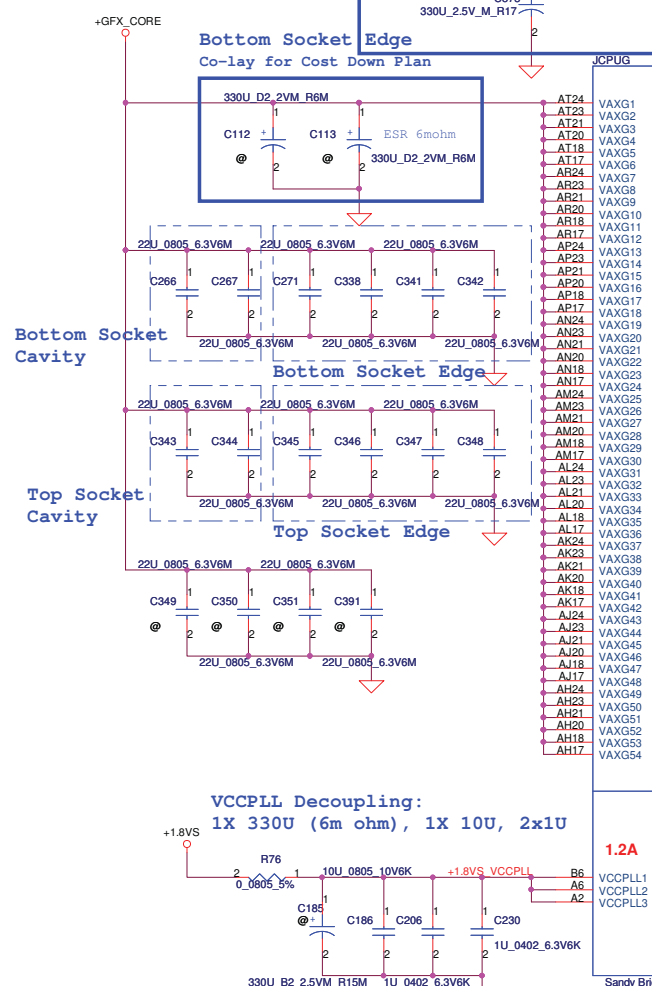
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Sandy Bridge_DDR3			
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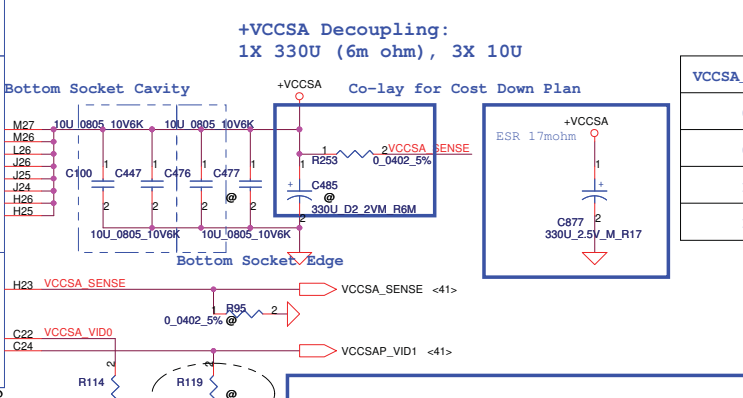
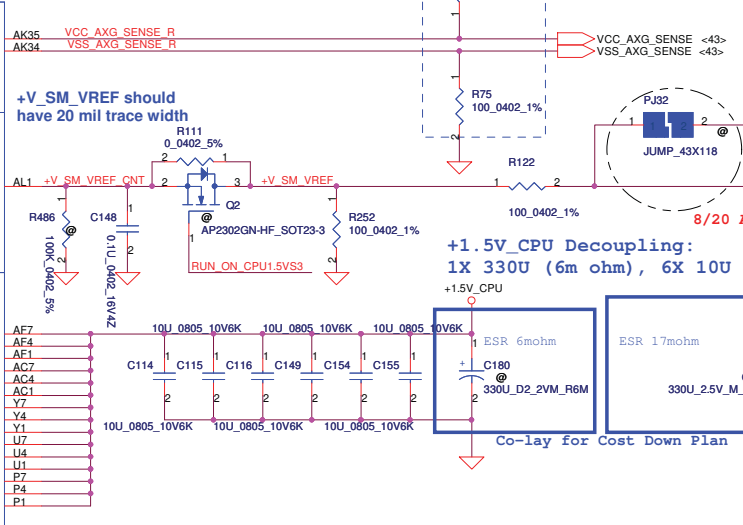
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**+GFX\_CORE Decoupling:**  
2X 470U (4m ohm), 12X 22U

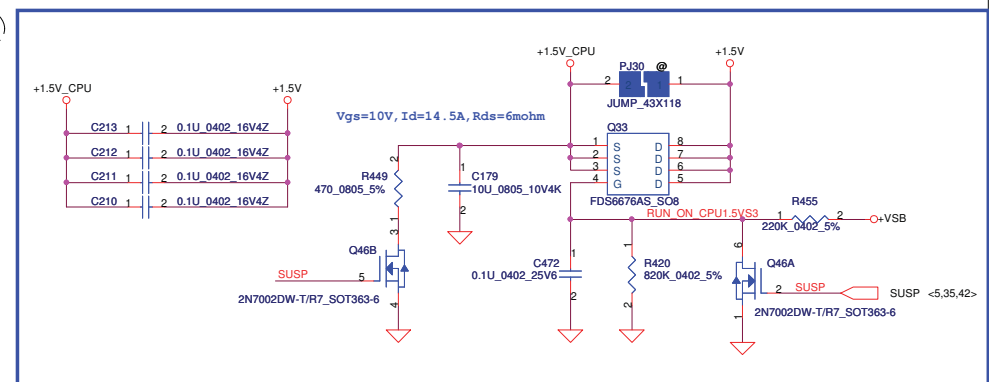


**POWER**

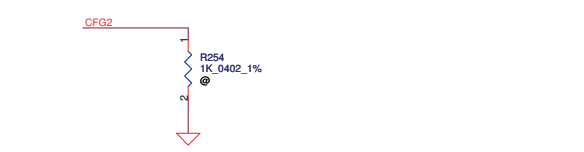
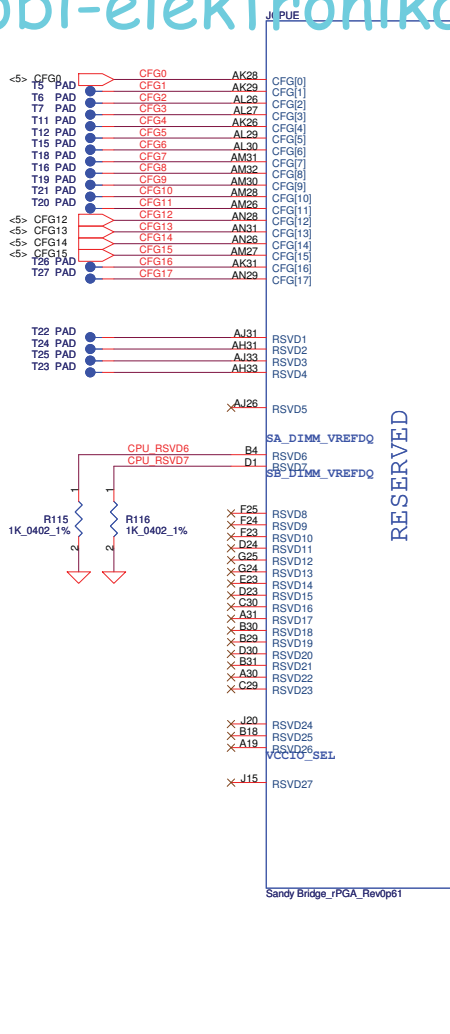
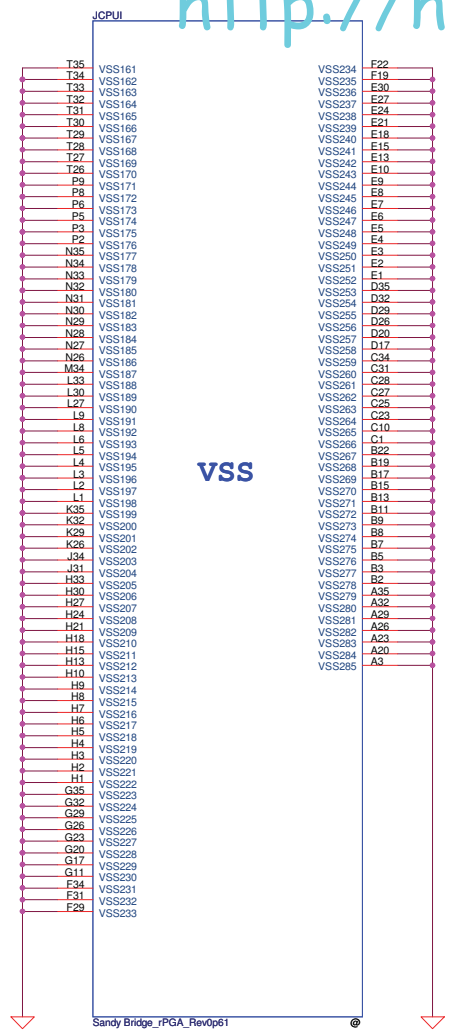
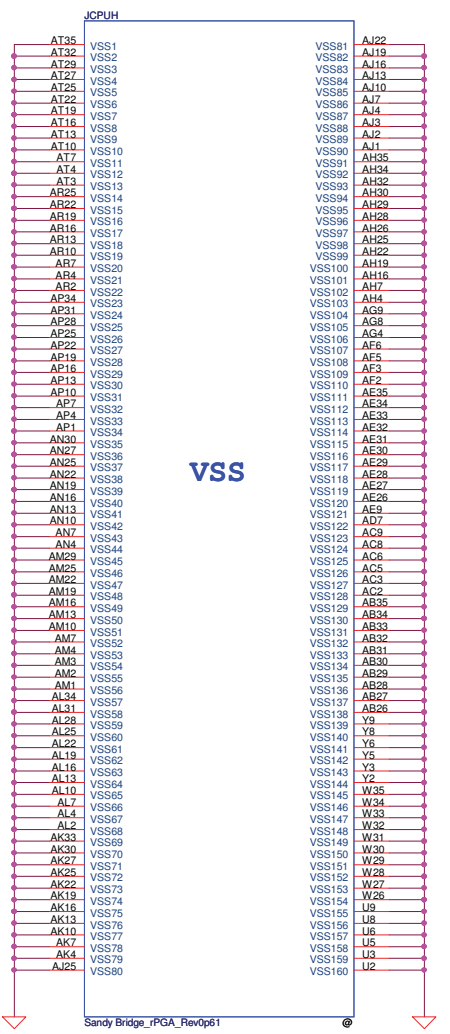


VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

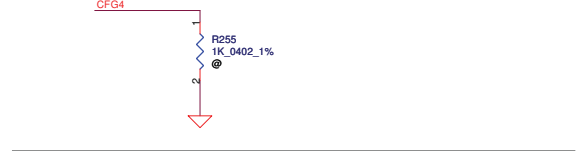
For Sandy Bridge



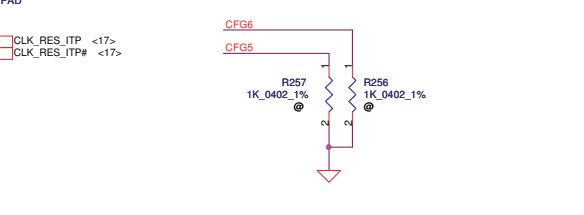
**CFG Straps for Processor**  
(CFG[17:0] internal pull high to VCCIO)



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Embedded Display Port Presence Strap	
CFG4	* 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

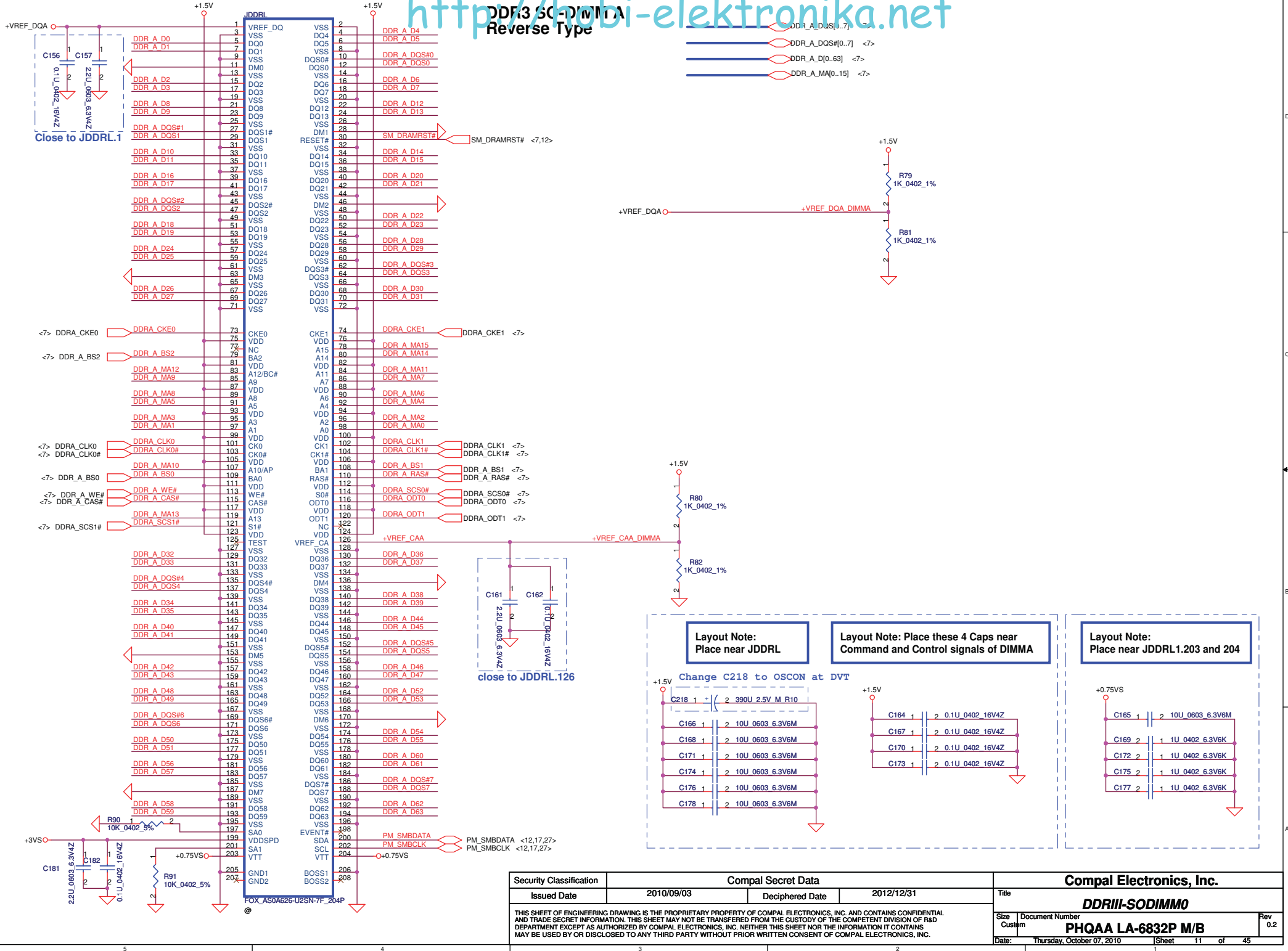


PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

DDR3 SDRAM Reverse Type



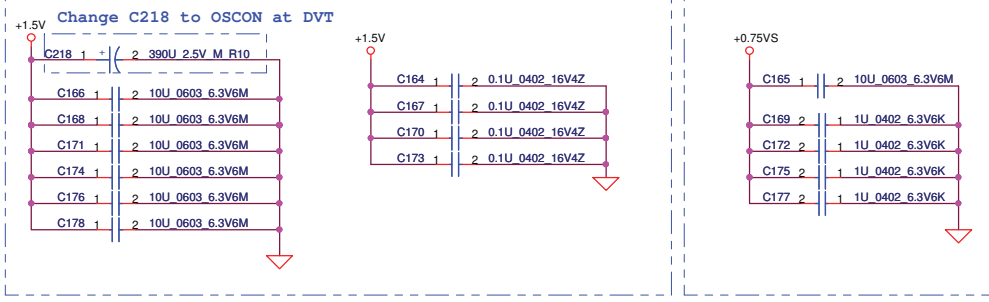
Close to JDDR.L1

close to JDDR.L126

Layout Note: Place near JDDR.L

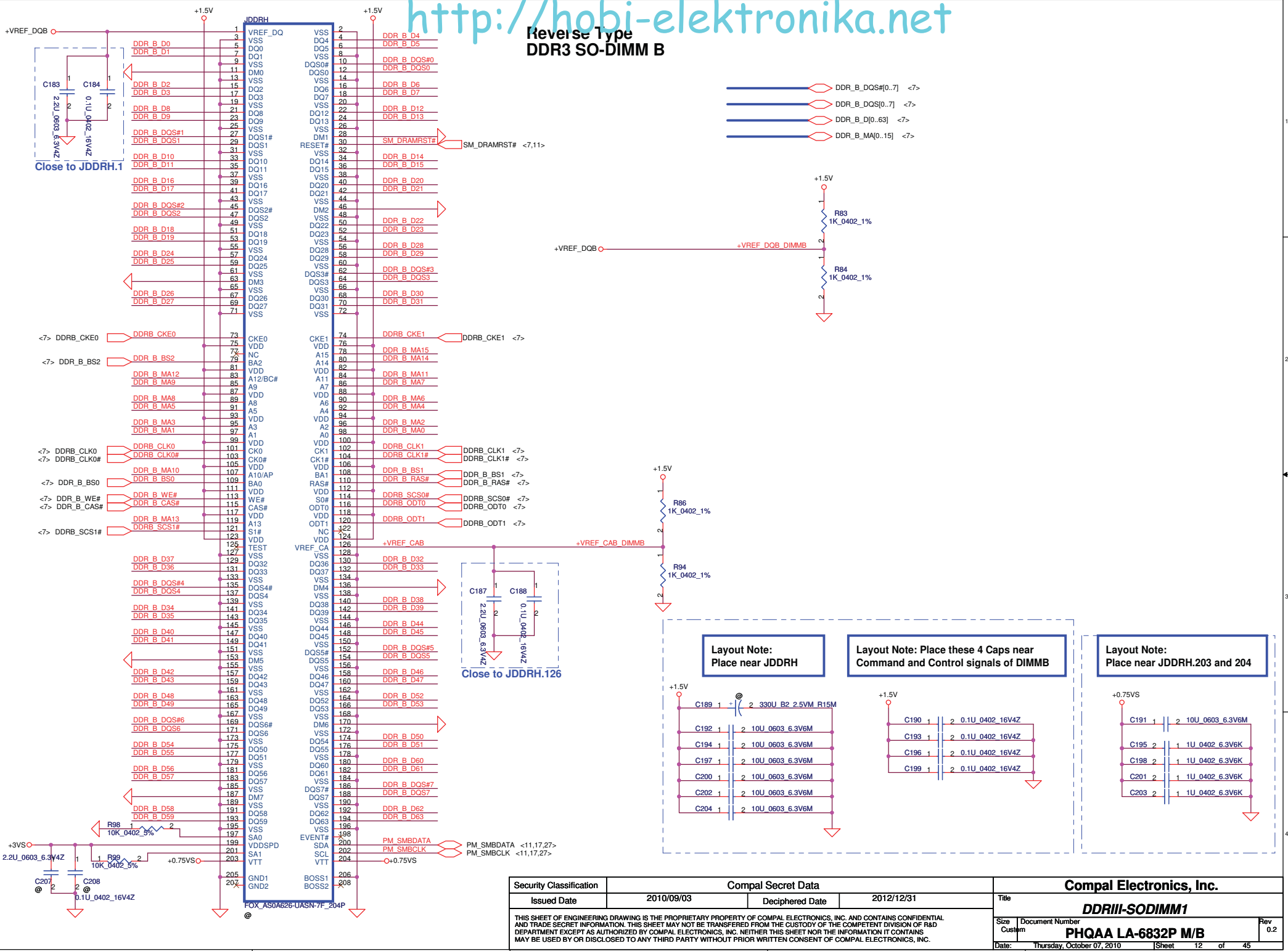
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

Layout Note: Place near JDDR.L1.203 and 204



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Compal Electronics, Inc.			DDRIII-SODIMMO	
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Reverse Type  
DDR3 SO-DIMM B



- DDR\_B\_DQS# [0..7] <7>
- DDR\_B\_DQS [0..7] <7>
- DDR\_B\_D [0..63] <7>
- DDR\_B\_MA [0..15] <7>

SM\_DRAMRST# <7,11>

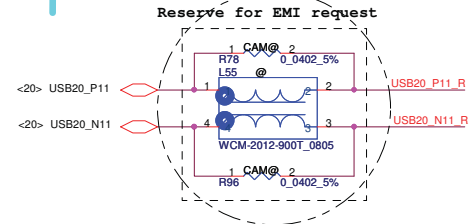
Close to JDDR.H.126

Layout Note:  
Place near JDDR.H

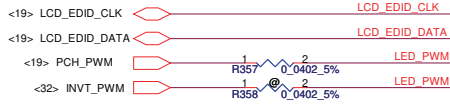
Layout Note: Place these 4 Caps near  
Command and Control signals of DIMMB

Layout Note:  
Place near JDDR.H.203 and 204

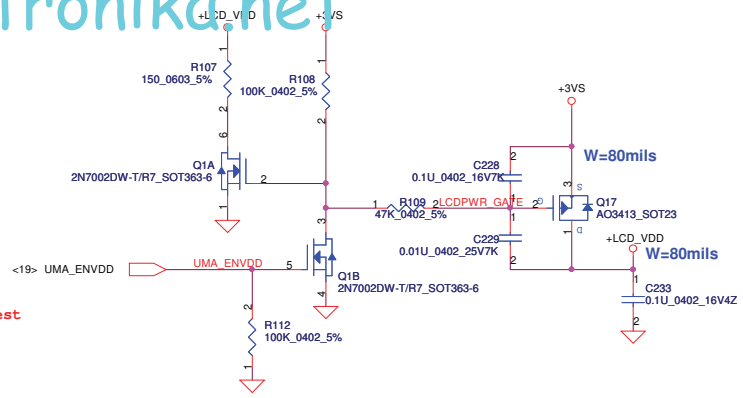
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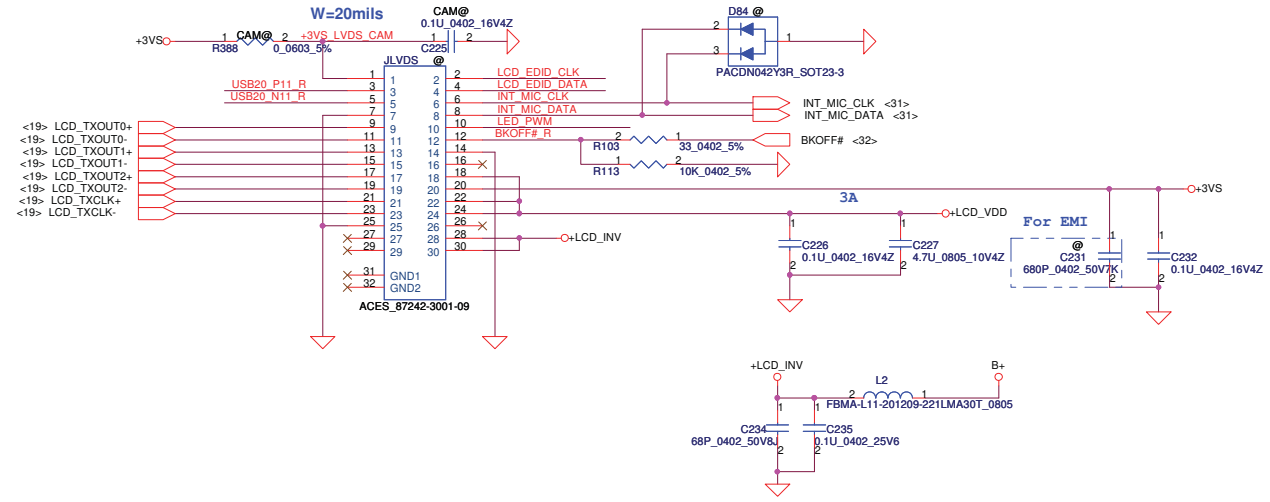
8/20 Swap USB20\_P11 and USB20\_N11 for layout request



Close to LVDS Connector

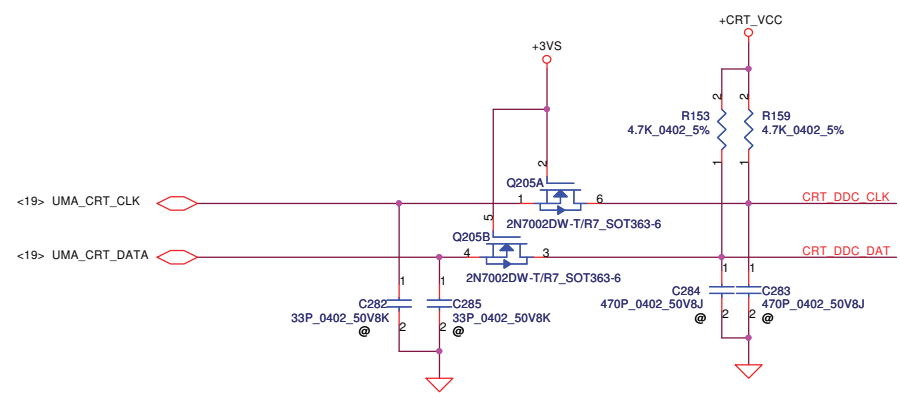
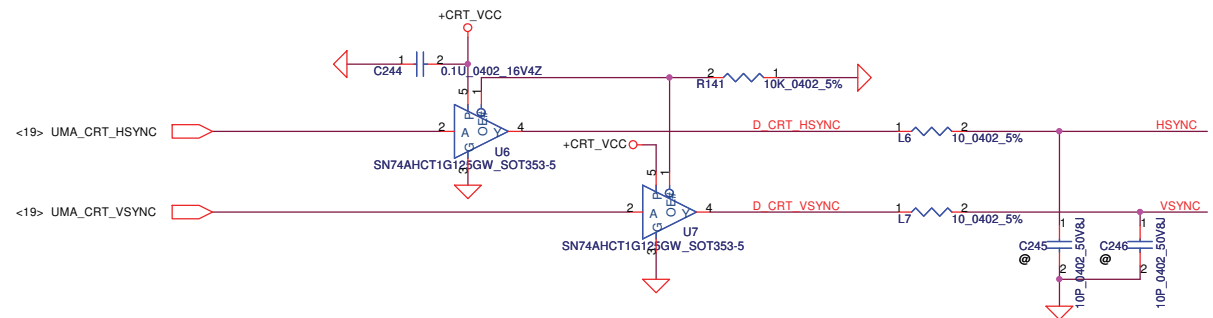
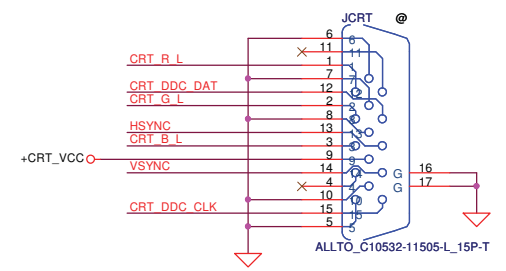
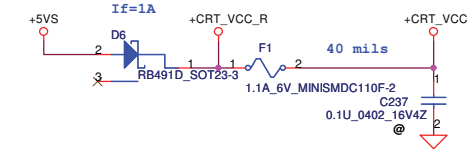
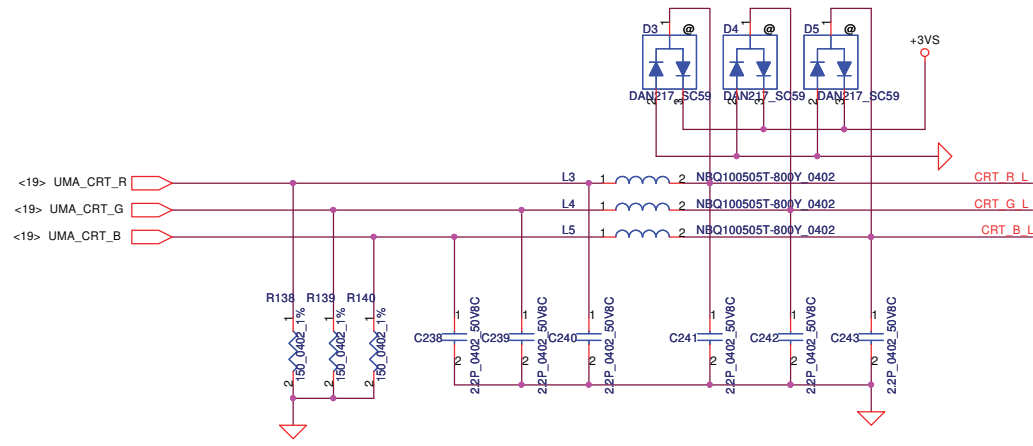


LCD/PANEL BD. Conn.



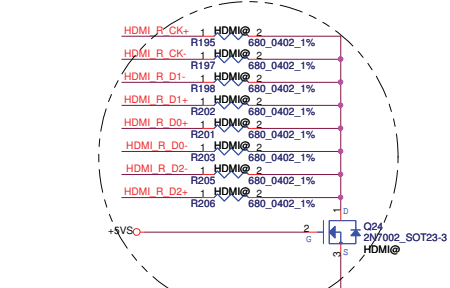
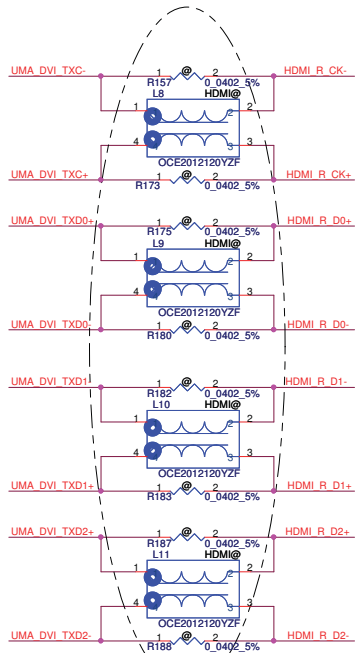
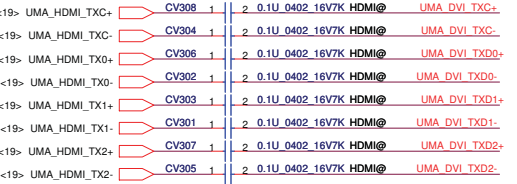
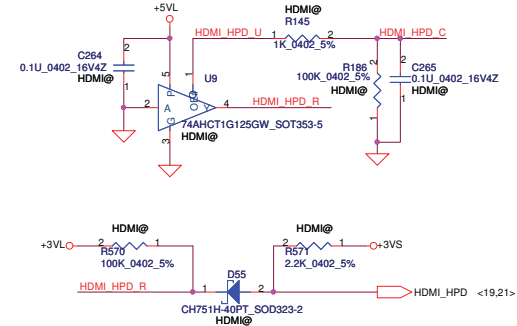
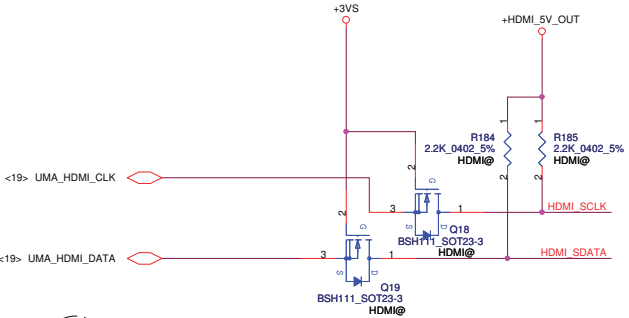
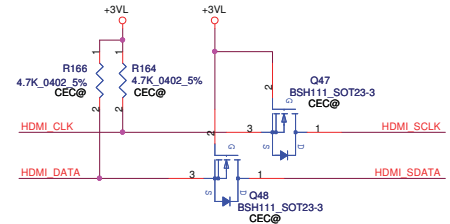
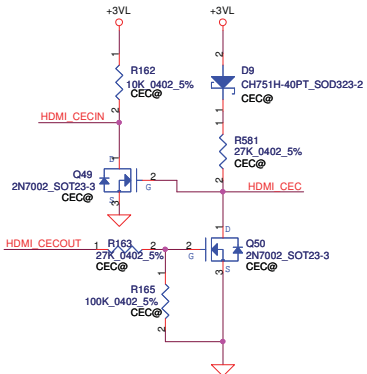
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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				Customer	0.2
				Date: Thursday, October 07, 2010	
				Sheet	13 of 45
				Title: LVDS/eDP	
				PHQAA LA-6832P M/B	

### CRT CONNECTOR



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Size	Document Number	Rev		0.2	
PHQAA LA-6832P M/B		Date		Thursday, October 07, 2010 Sheet 14 of 45	

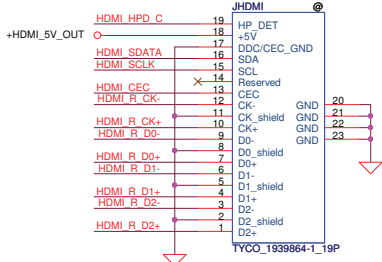
# HDMI CEC Controller



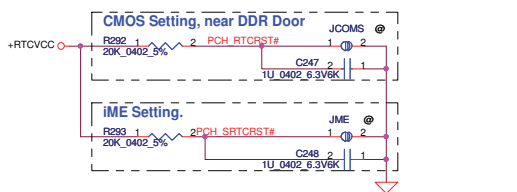
08/18 Change R195, R197, R198, R202, R201, R203, R205, R206 to SD028680080 for UMA request

08/13 Change L8, L9 L10, L11 from SM070001600 to SM070001310 by EMI demand

## HDMI Connector

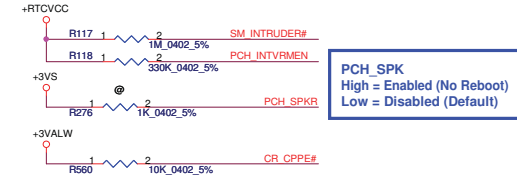


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				Sheet	of
				15	45



**Integrated SUS 1.05V VRM Enable**

PCH\_INTVRMEN High - Enable Internal VRs (must be always pulled high)



**HDA\_SDO**

ME debug mode, this signal has a weak internal pull down

\*Low = Disable (default)

High = Enable (flash descriptor security override)

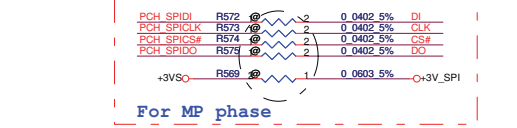
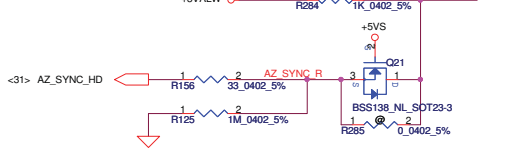
**HDA\_SYNC**

\*This signal has a weak internal pull down

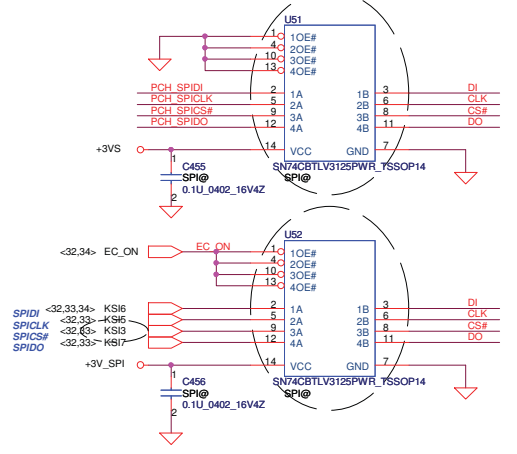
H=>On Die PLL is supplied by 1.5V

L=>On Die PLL is supplied by 1.8V

Need to pull high for Huron River platform

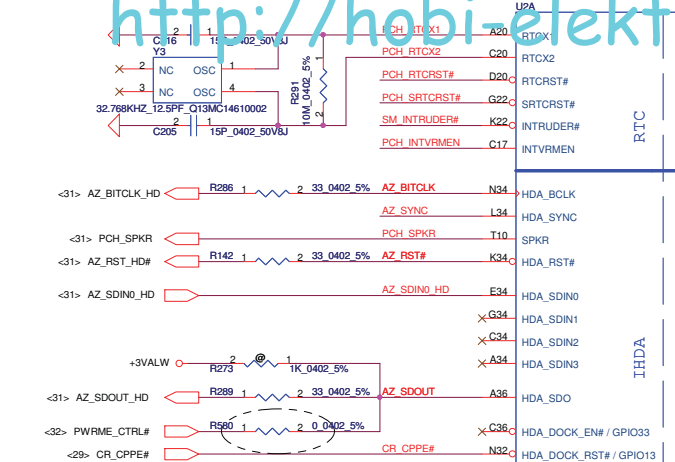


8/ 12 Change R572, R573, R574, R575, R569 from @ to mount

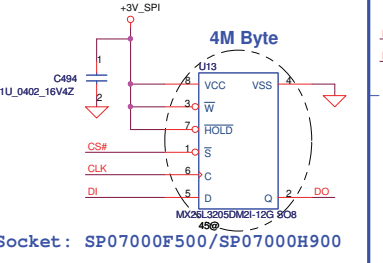
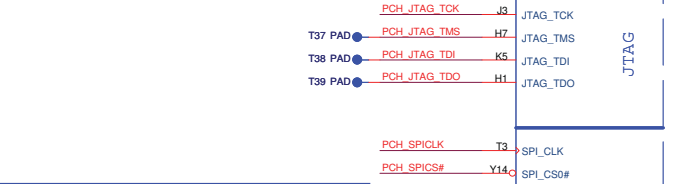


8/12 Change U51, U53 P/N form SA00000BJ20 to SA00000CA00

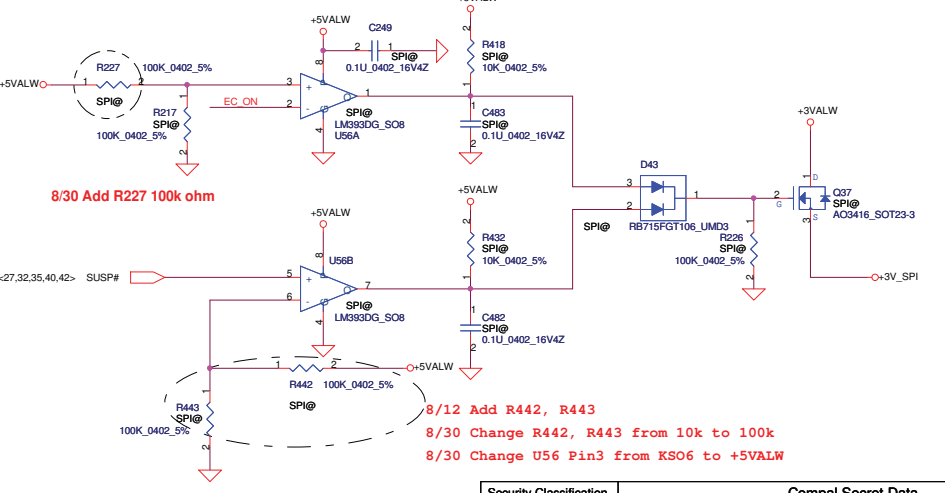
8/30 Change U53 PIN 9 from KS14 to KS13



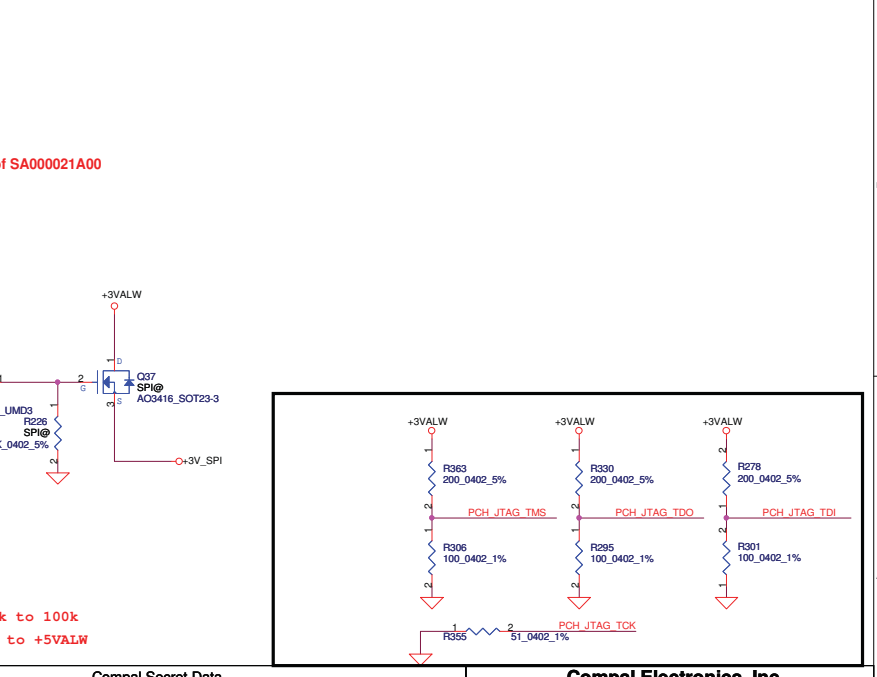
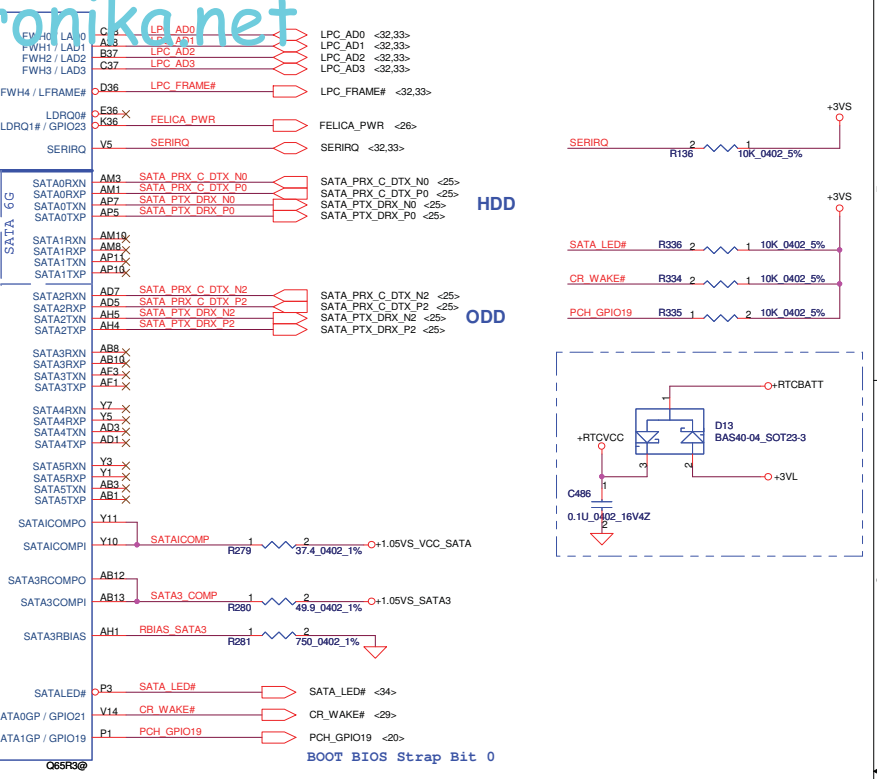
8/30 Change PWRME\_CTRL# to HDA\_SDO by PCH EDS



Please close to U2 PCH 8/30 Change U13 from SA000001A00 to SA000003IN00 due to EOL of SA000001A00



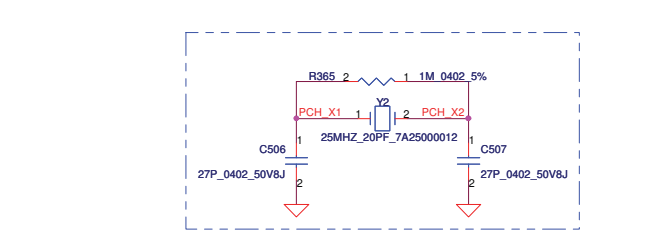
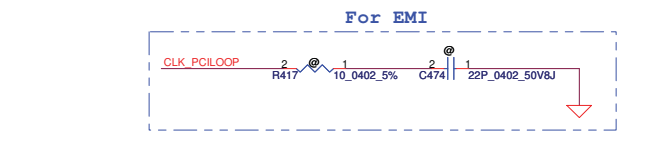
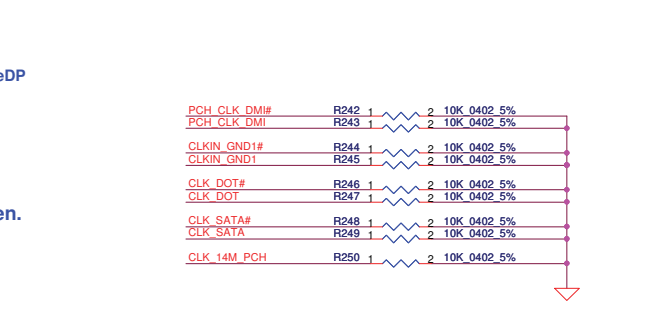
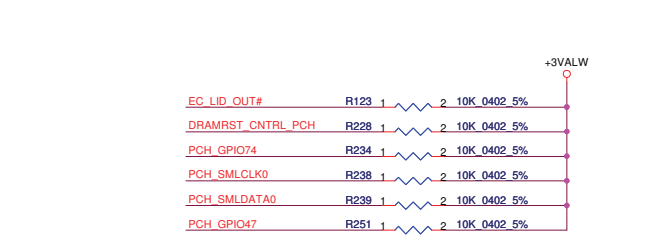
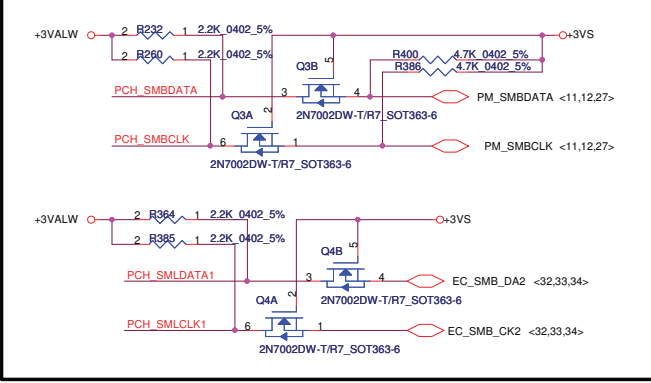
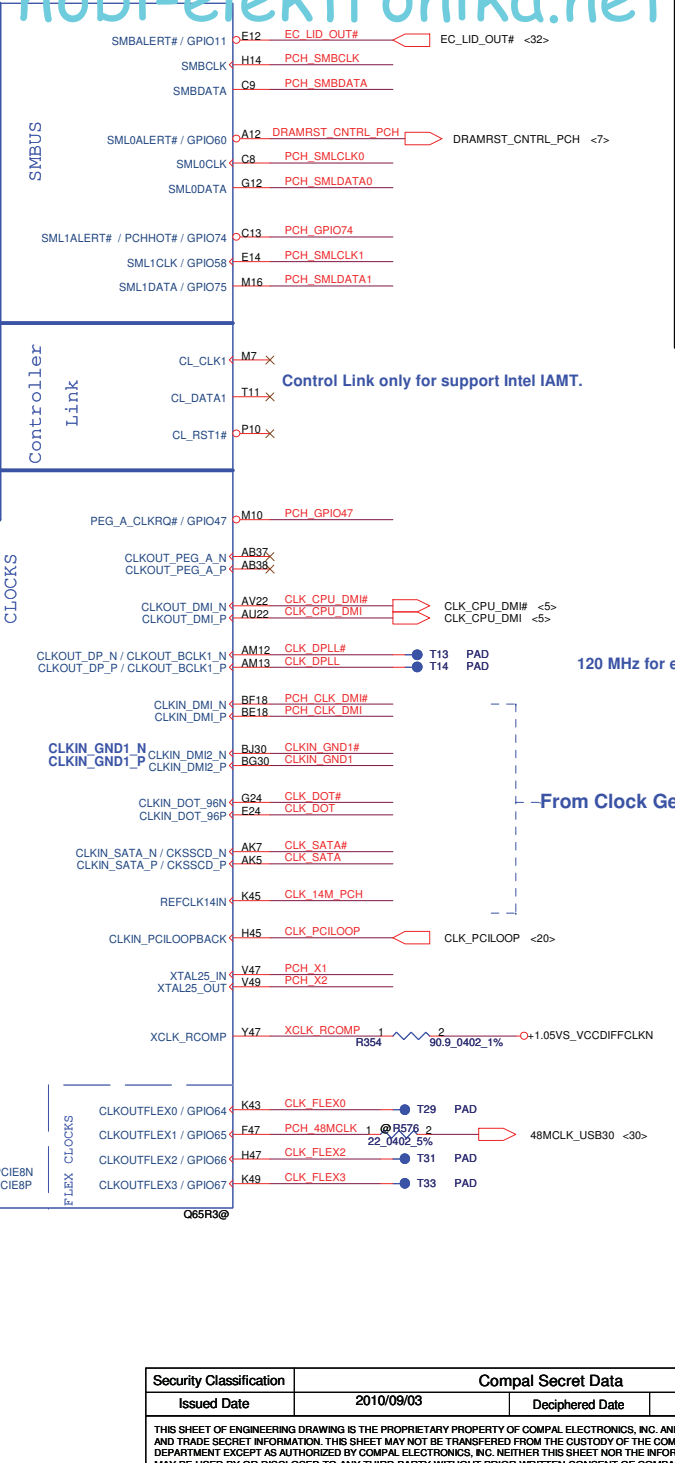
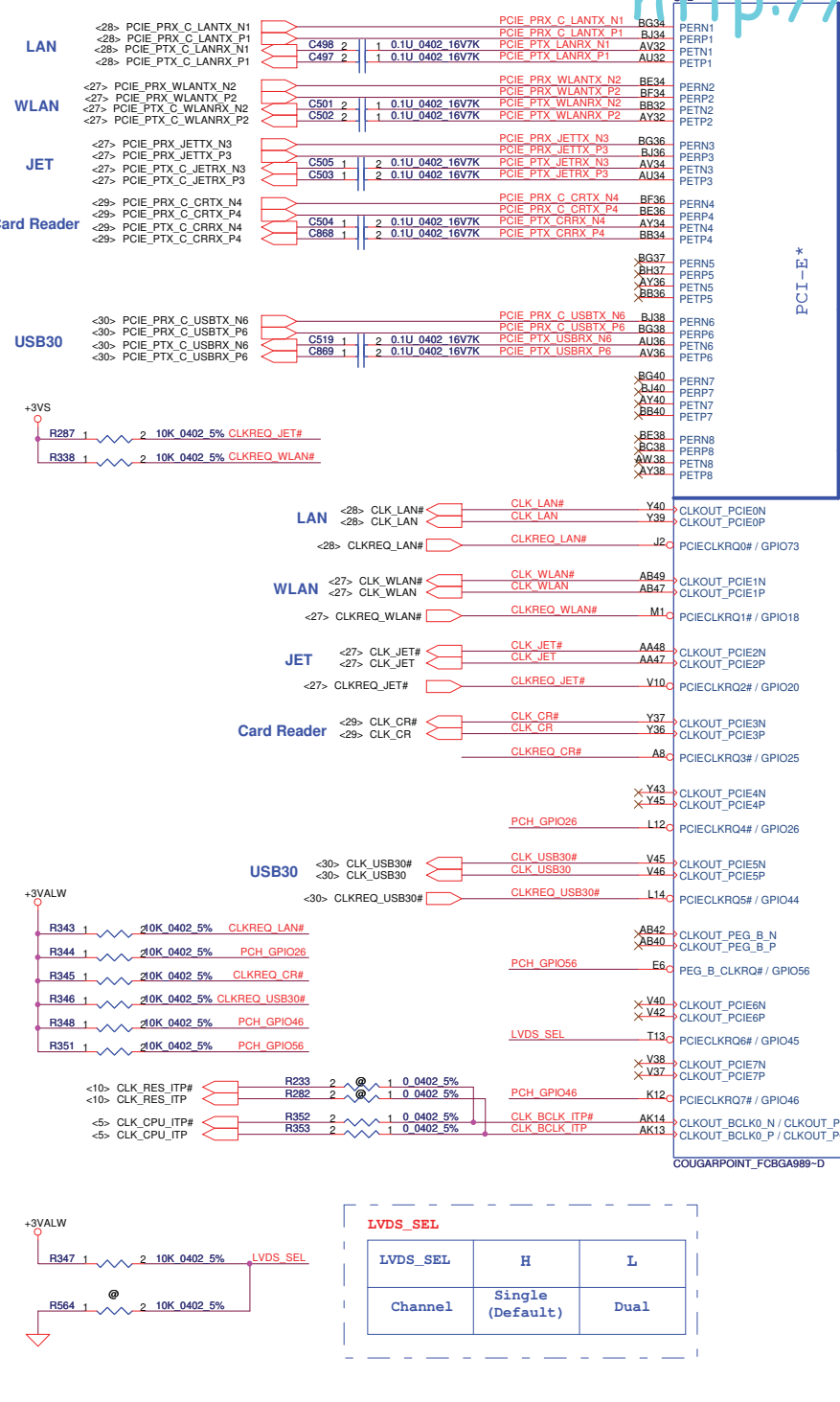
Please close to U2 PCH, and between U2 & U13



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Title <b>PCH_HDA/JTAG/SATA/SPI/LPC</b>			
Size	Document Number	Rev	
Custom	PHQAA LA-6832P M/B	0.2	
Date:	Thursday, October 07, 2010	Sheet	16 of 45

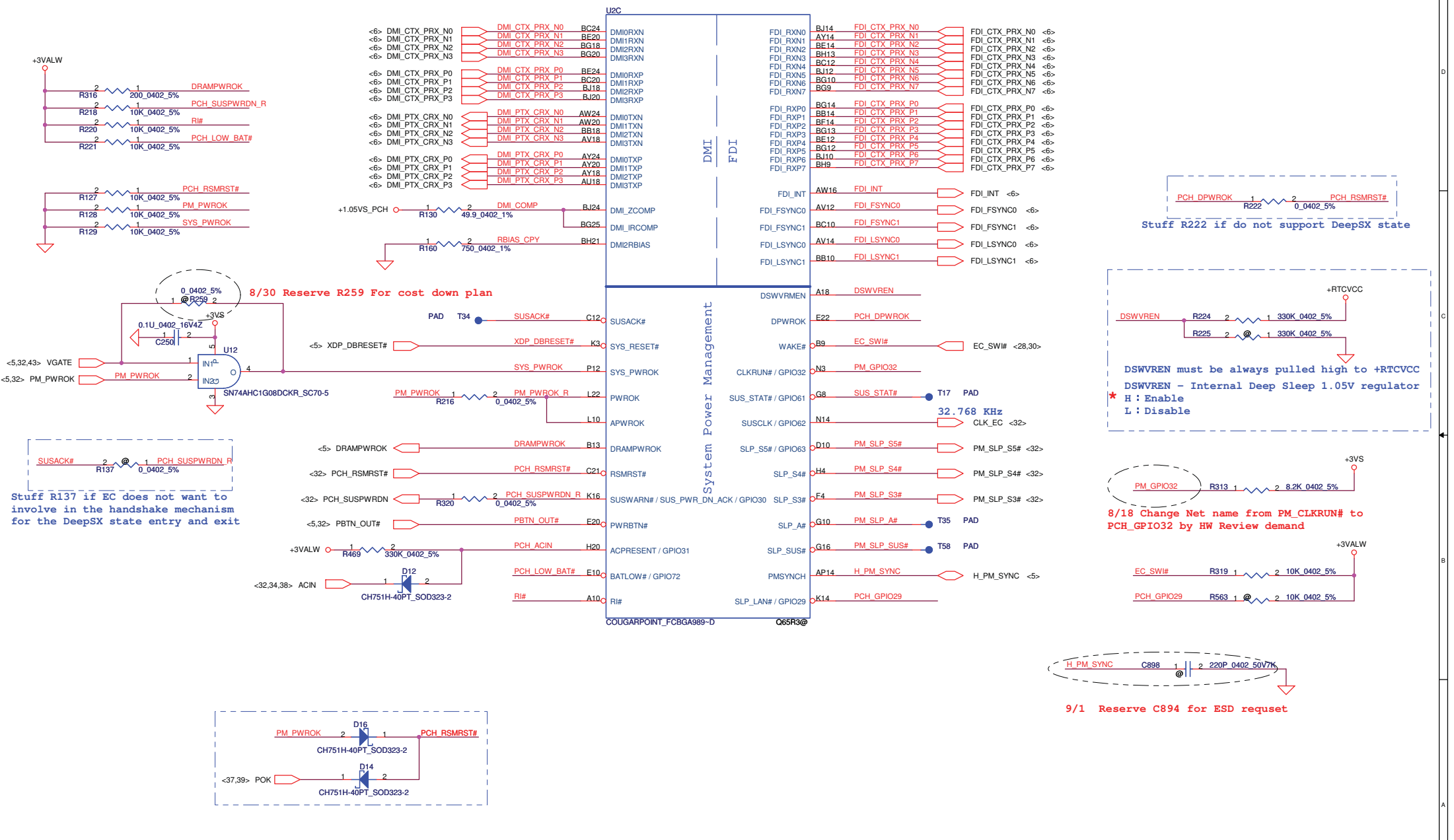




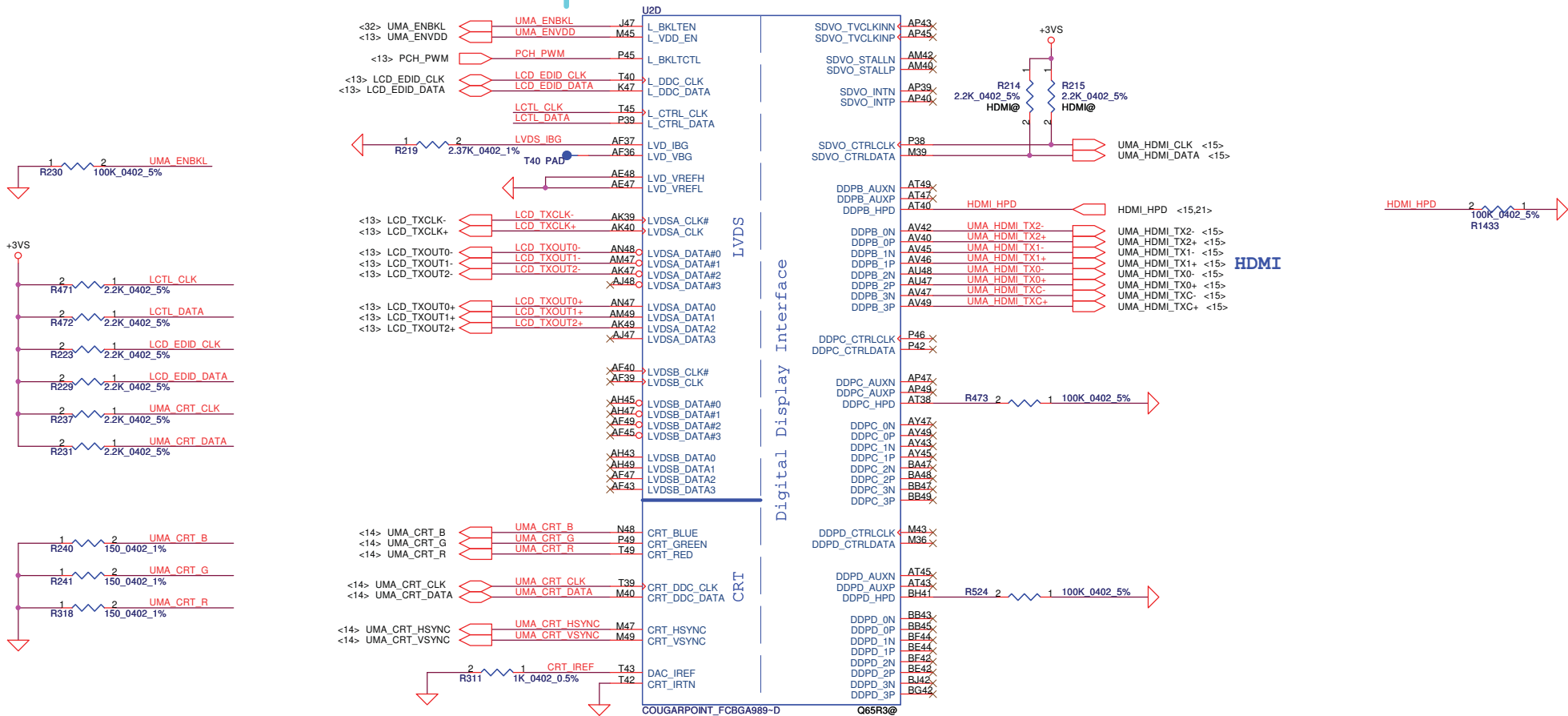
**LVDS\_SEL**

LVDS_SEL	H	L
Channel	Single (Default)	Dual

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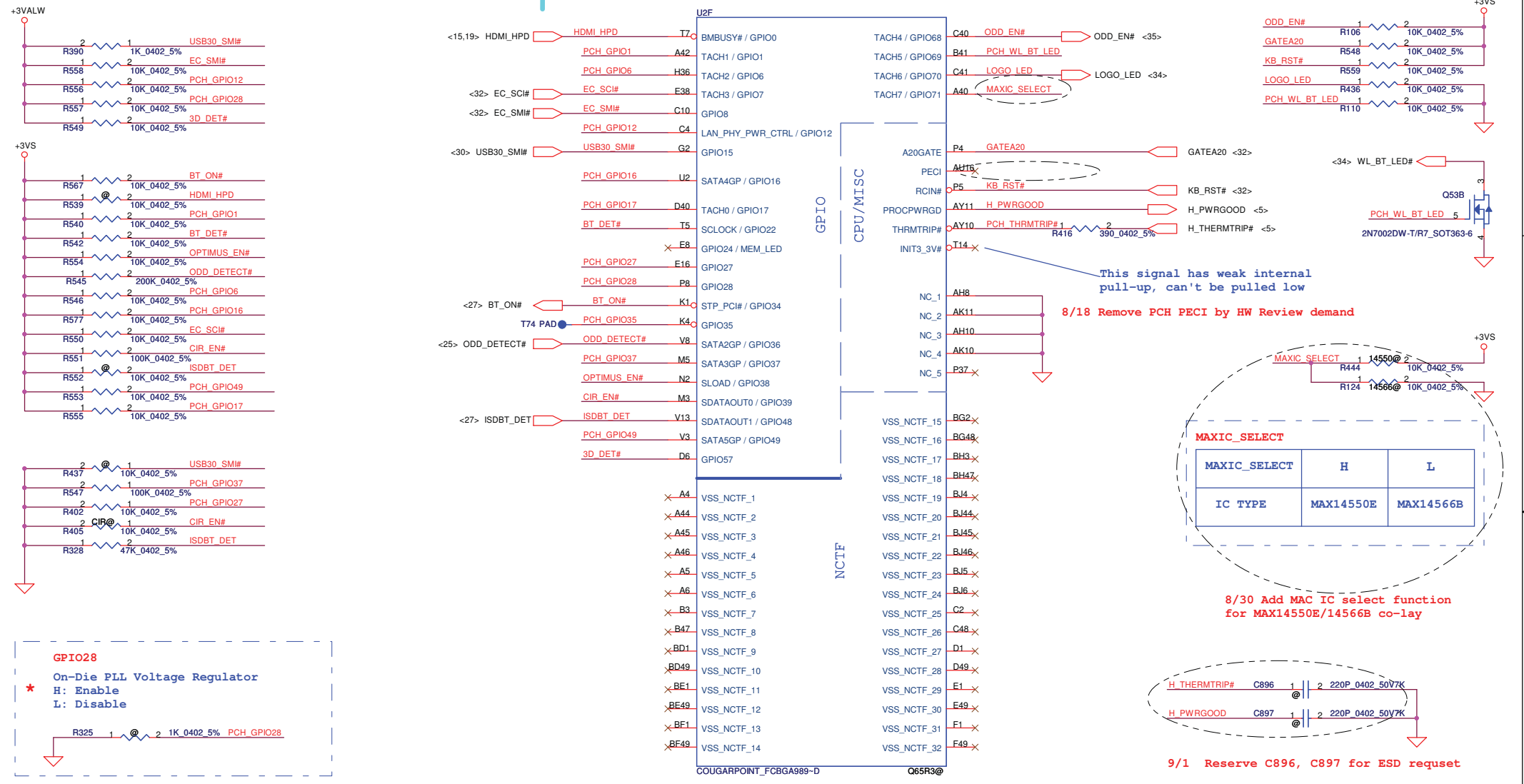


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				PCH_DMI/FDI/PM		
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**GPIO28**  
 On-Die PLL Voltage Regulator  
 H: Enable  
 L: Disable

R325 1K 0402 5% PCH\_GPIO28

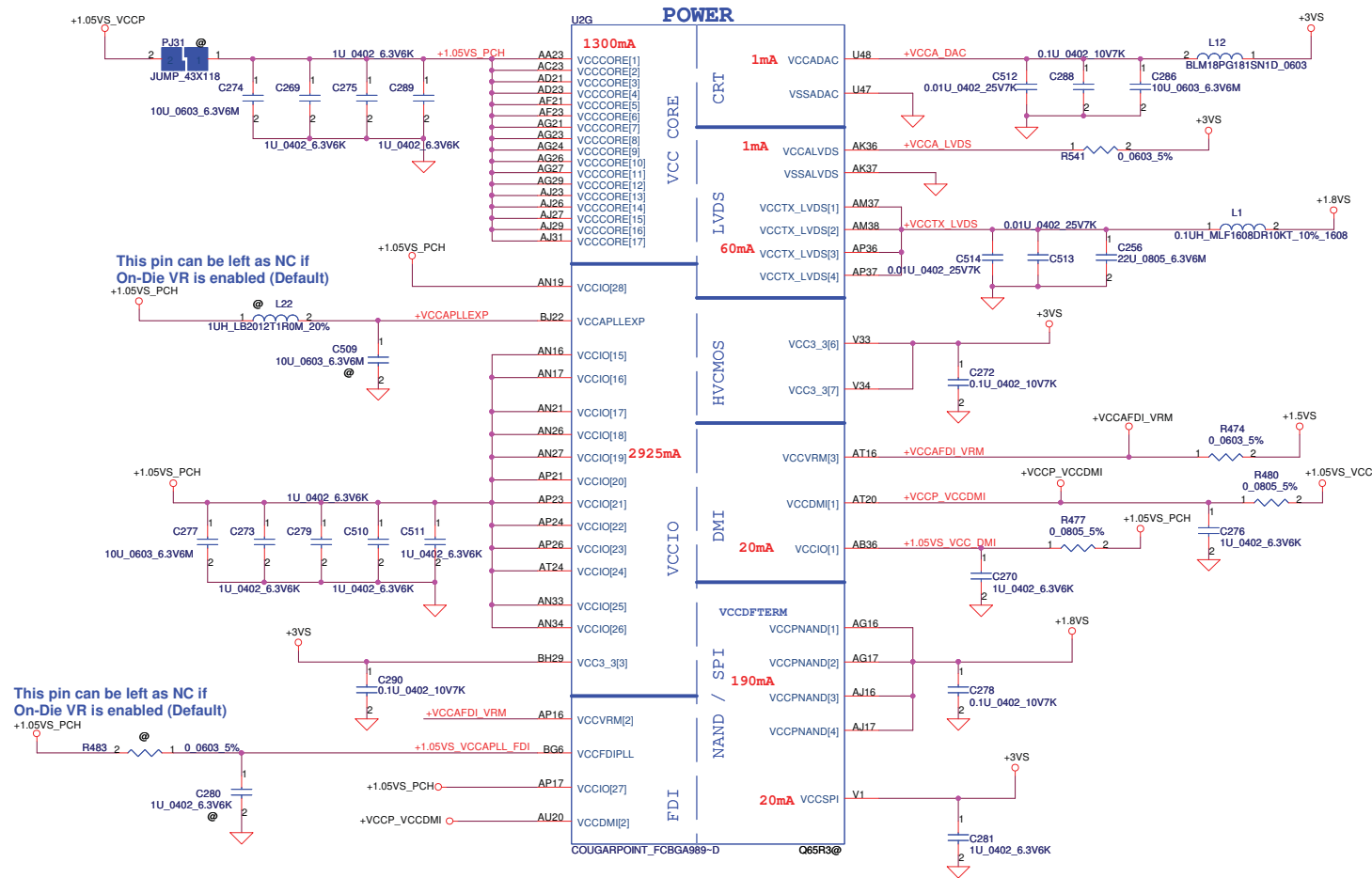
**GPIO8**  
 Integrated Clock Chip Enable (Removed)  
 H: Disable  
 \* L: Enable

R326 1K 0402 5% EC\_SMI#

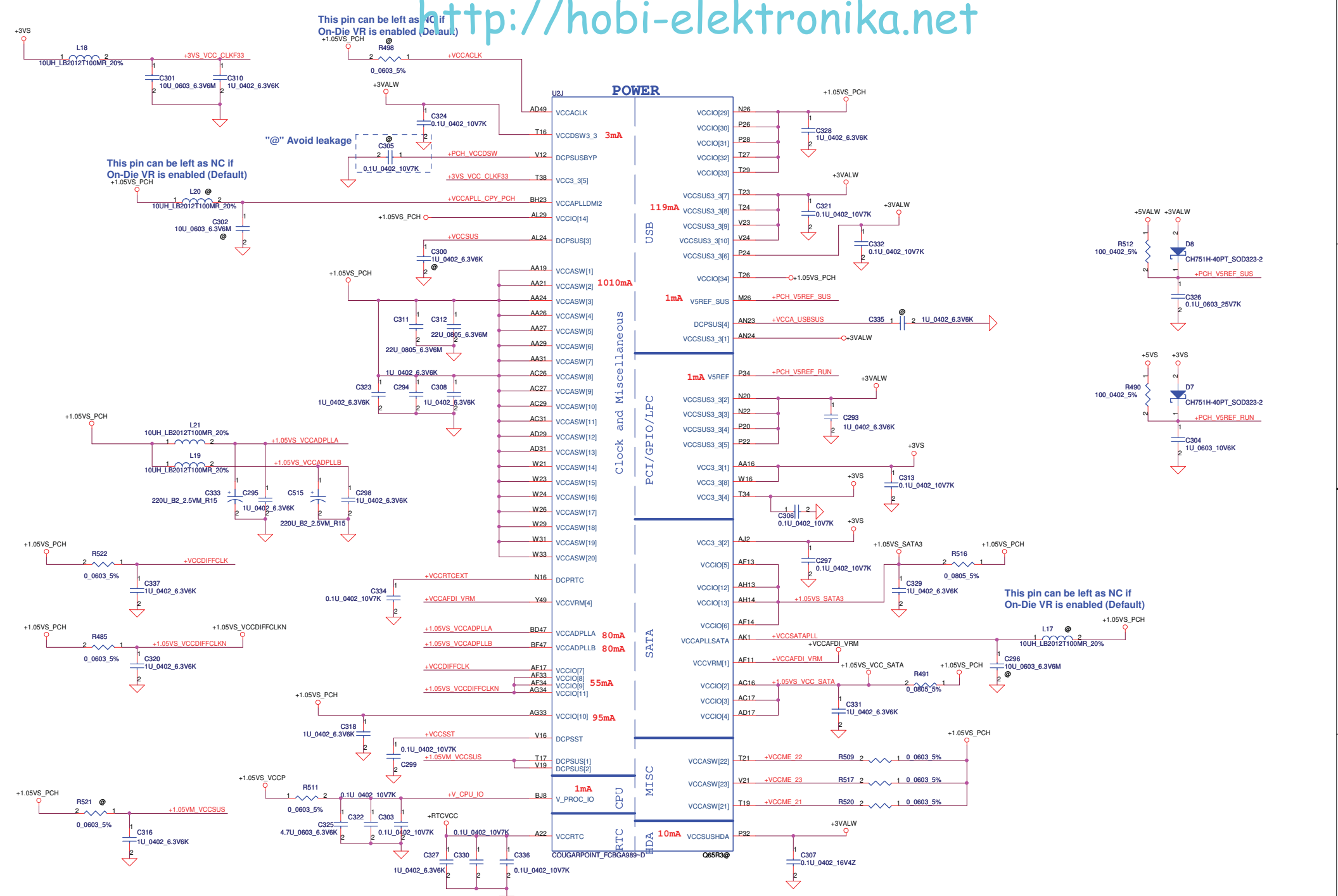
Integrated clock enable functionality is achieved by soft-strap  
 The current default is clock enable

**OPTIMUS\_EN#**

OPTIMUS_EN#	H	L
SKU	Discrete	Optimus



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADP1LLA	1.05	0.08
VCCADP1LLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

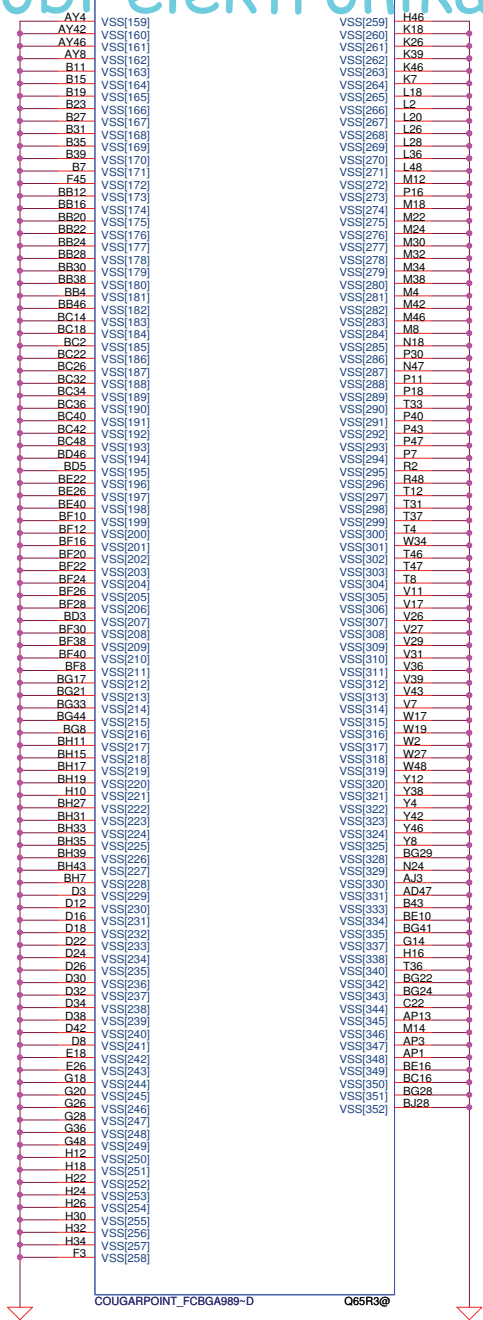
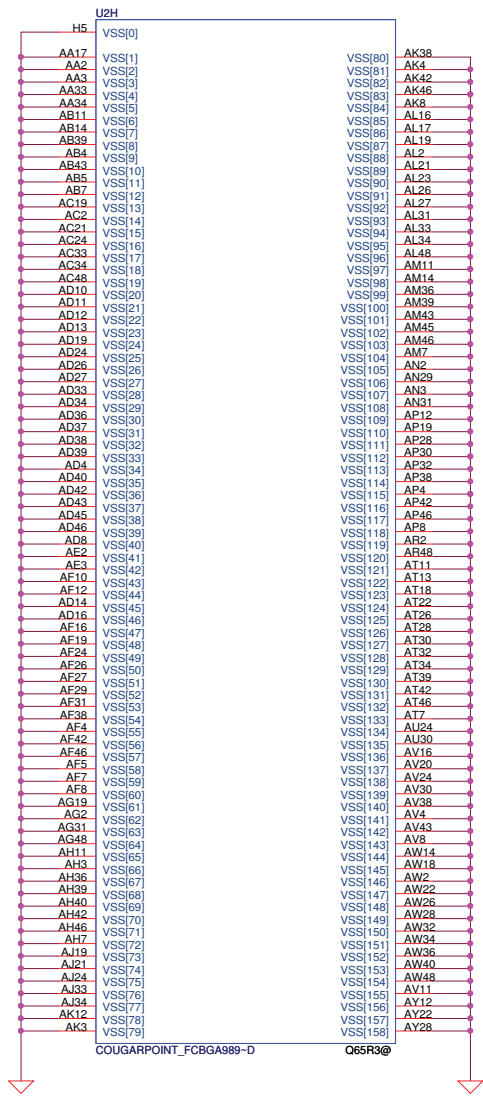


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**PCH\_POWER-2**

PHQAA LA-6832P M/B

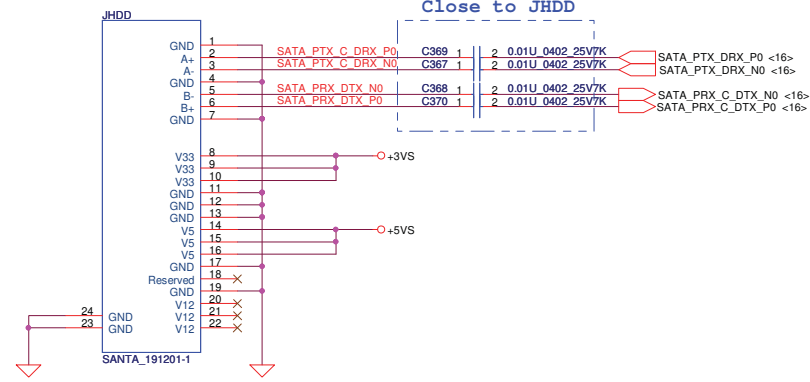
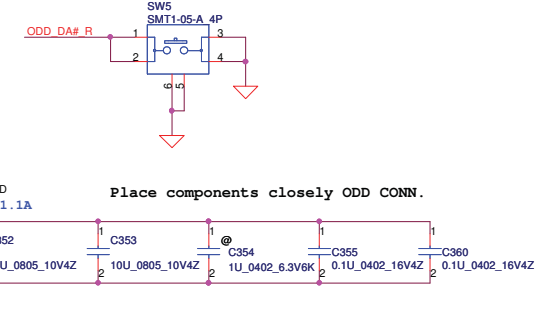
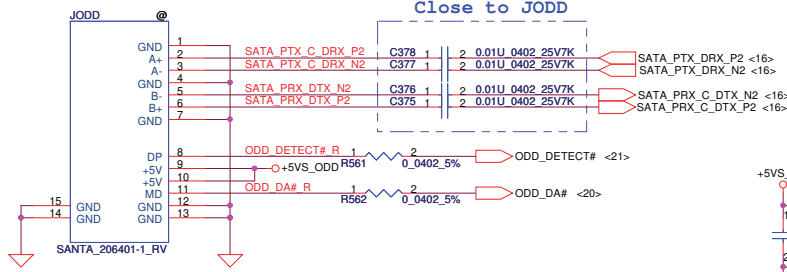
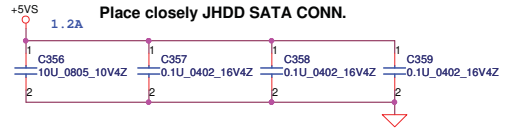


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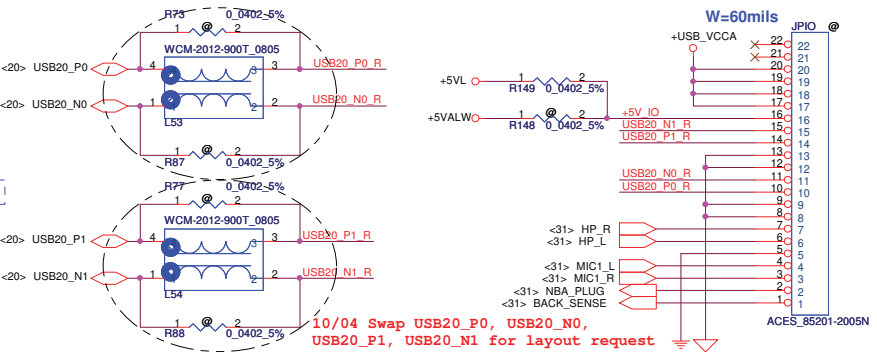
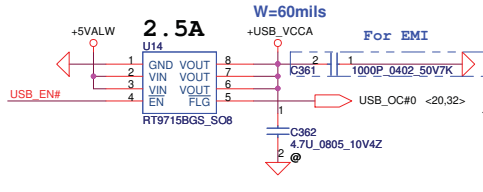


SATA (O)DD Conn

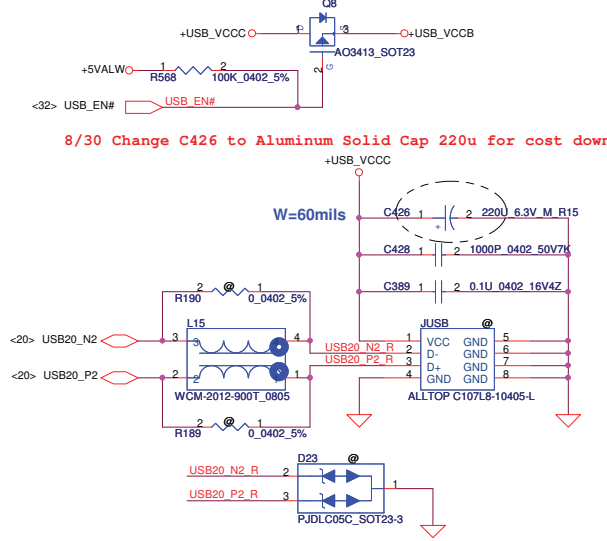
SATA HDD Conn.



USB Board@ Right Side

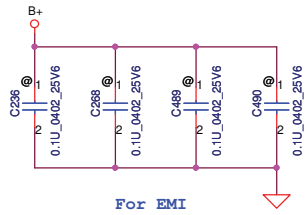


USB Board@ Left Side

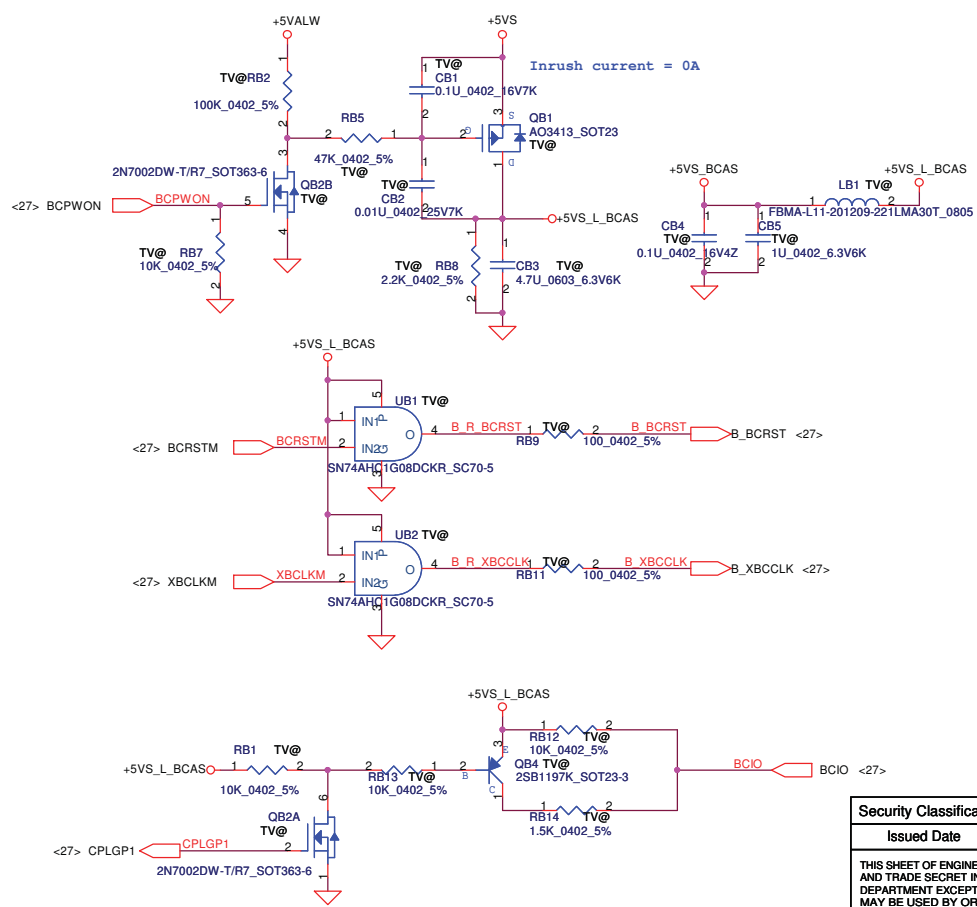


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Screw cap for ESD request

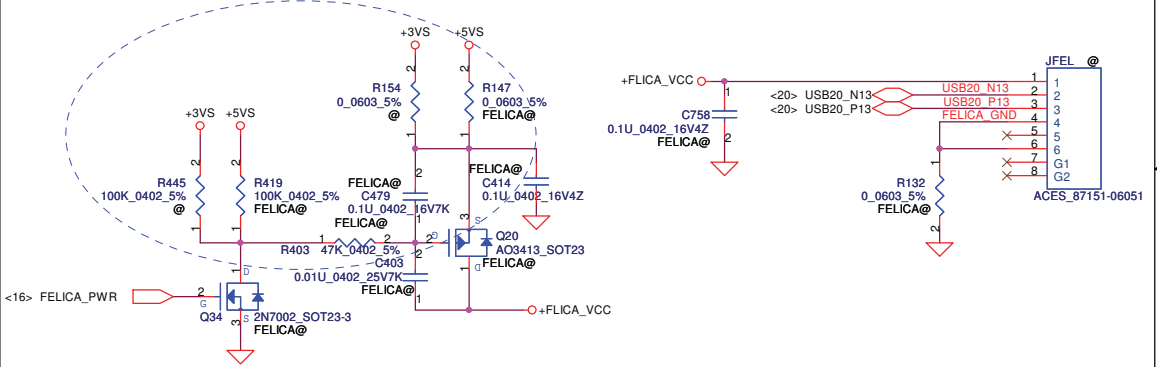


B-CAS Circuit

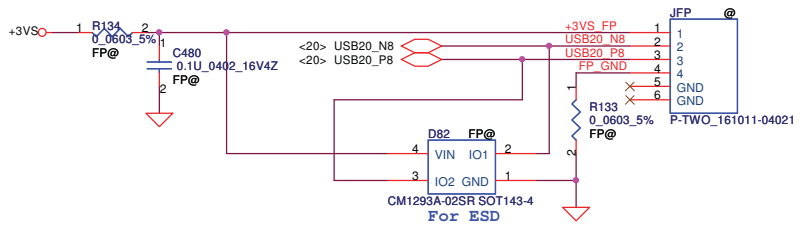


Felica

Reserve +3VS Felica by Customer demand.  
2010/09/27

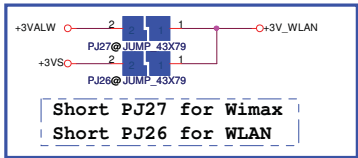


Finger printer



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Size	Document Number	PHQAA LA-6832P M/B		Rev 0.2	
Date:	Thursday, October 07, 2010	Sheet	26	of 45	

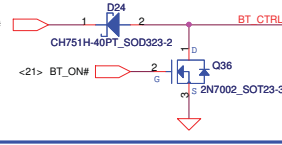
### Slot 1 Half PCIe Mini Card-WLAN/ WiMax



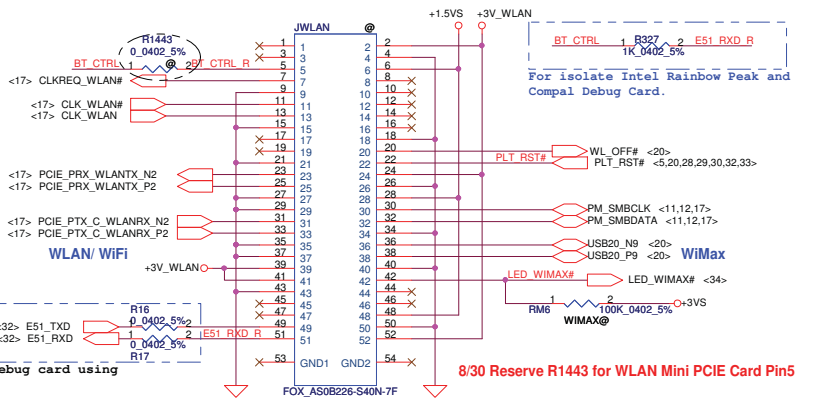
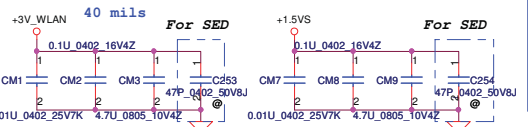
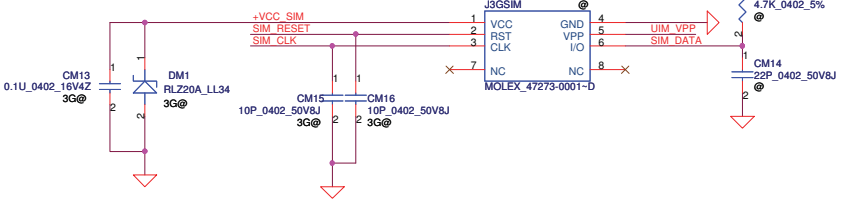
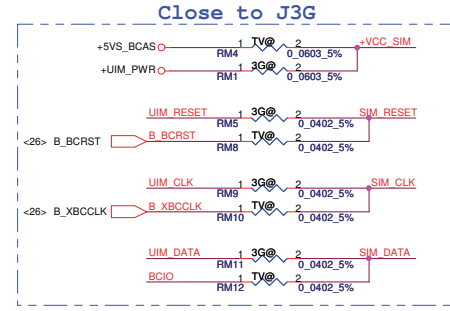
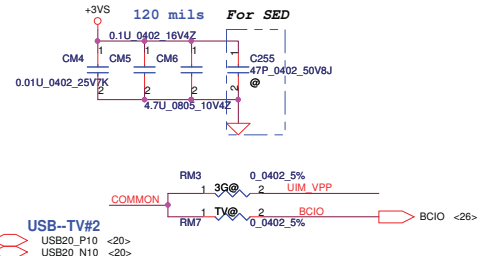
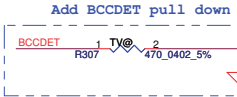
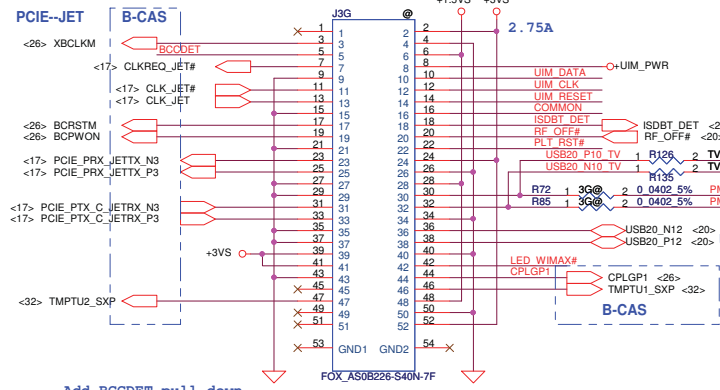
WLAN&BT Combo module inputs

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

\*\*If +3V\_WLAN is +3VS, please remove D24



### Sot 2 Full PCIe Mini Card-3G/TV Tuner



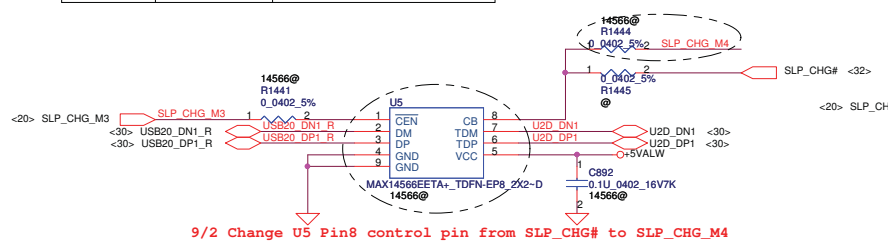
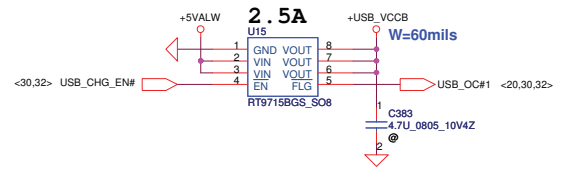
8/30 Reserve R1443 for WLAN Mini PCIe Card Pin5

### USB Sleep & Charge Auto-Mode Mode3/Mode4

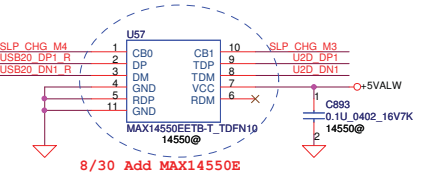
CB0 SLP_CHG#	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

CB: SLP_CHG#	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

CB0 SLP_CHG_M4	CB1 SLP_CHG_M4	STATUS
0	0	AUTO MODE
0	1	MODE3
1	0	MODE4
1	1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM



9/2 Change U5 Pin8 control pin from SLP\_CHG# to SLP\_CHG\_M4  
9/2 Add 14566@ & 14550@



8/30 Add MAX14550E

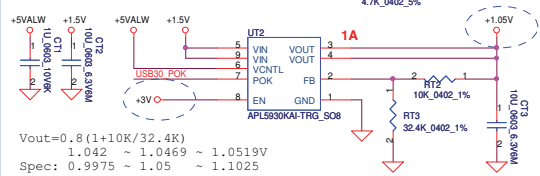
Security Classification	Compal Secret Data		Title	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Compal Electronics, Inc.
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PCIE-WLAN/JET/3G/TV/NewCard  
PHQAA LA-6832P M/B

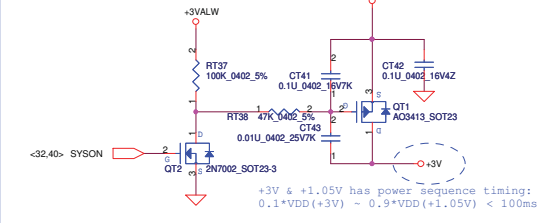




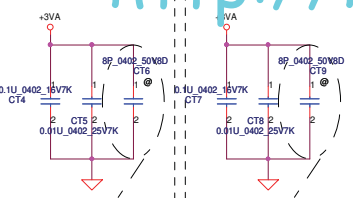
+1.5V to +1.05V Transfer



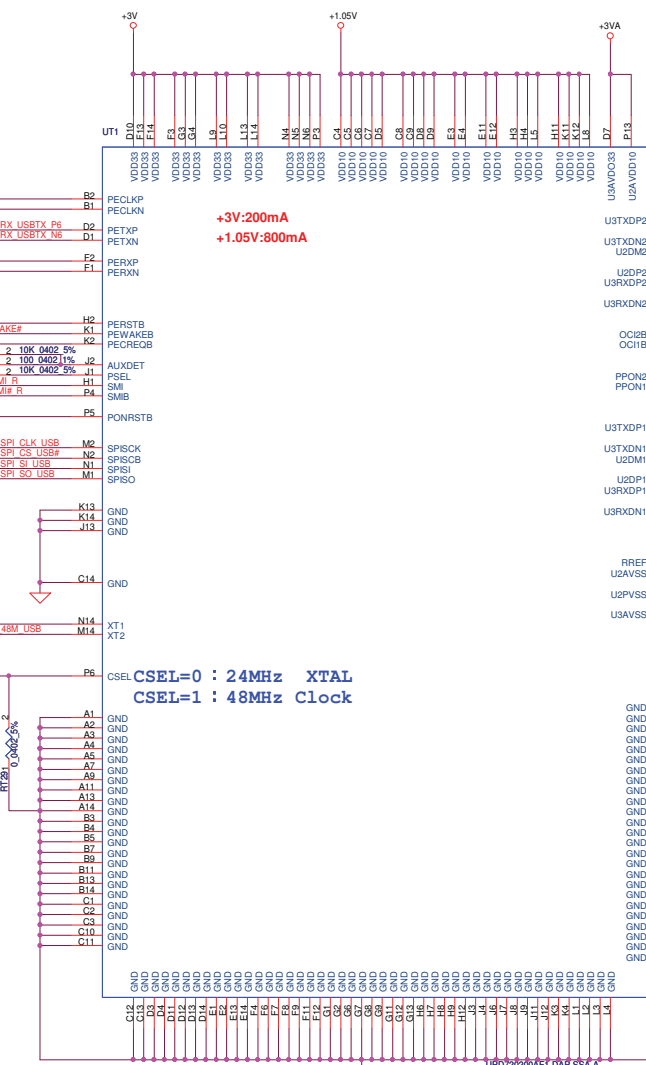
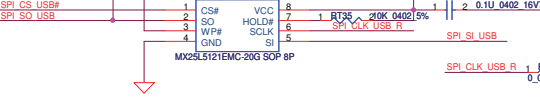
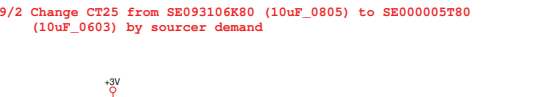
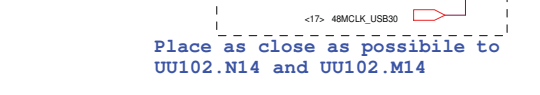
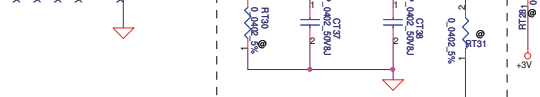
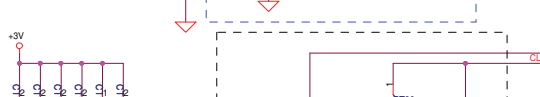
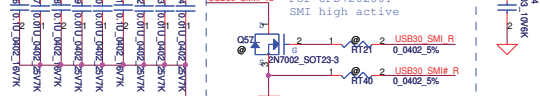
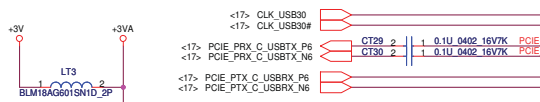
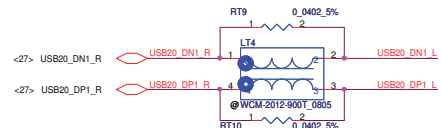
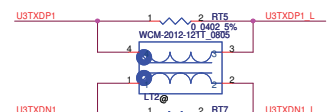
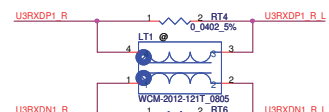
+3VALW to +3V Transfer



Close to U102.D Close to U102.P1



Follow Vendor recommend.

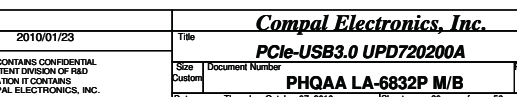
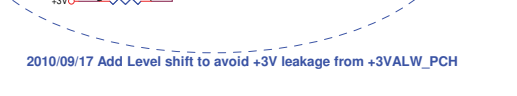
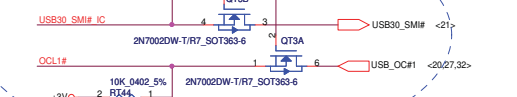
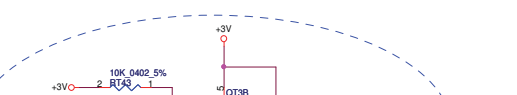
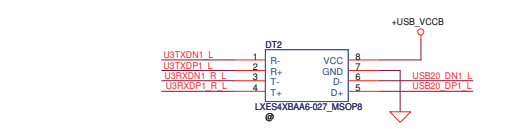
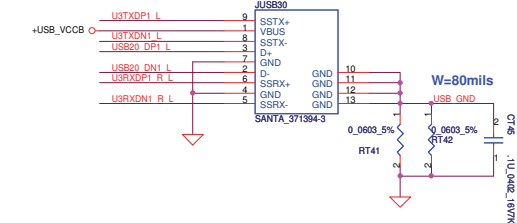
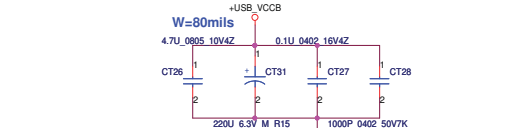


+3V:200mA  
+1.05V:800mA

CSEL=CSEL=0 : 24MHz XTAL  
CSEL=1 : 48MHz Clock

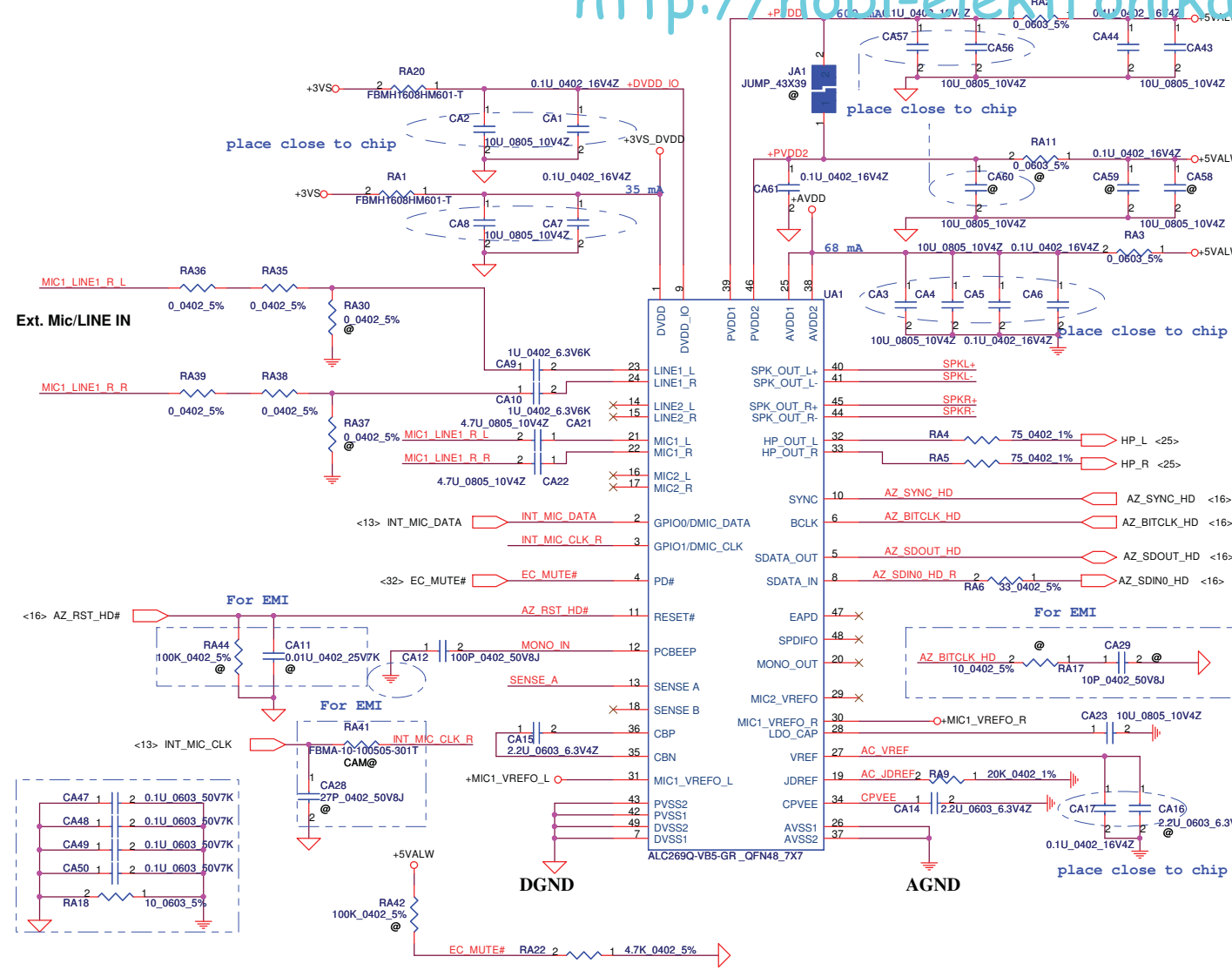
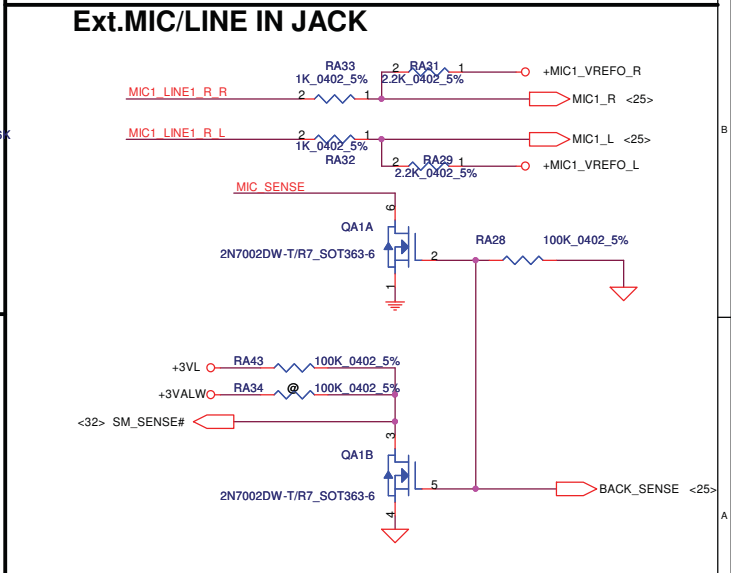
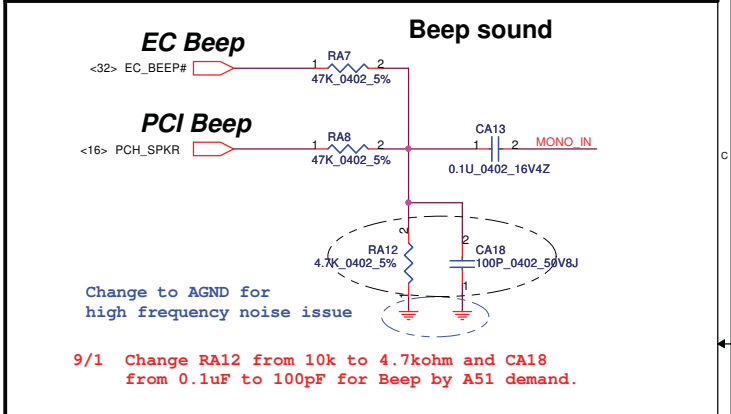
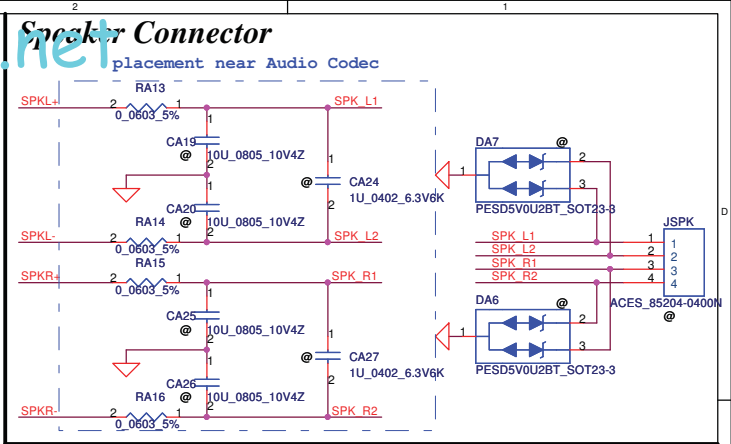
Place as close as possible to U102.N14 and U102.M14

9/2 Change CT25 from SE093106K80 (10uF\_0805) to SE000005T80 (10uF\_0603) by sourcer demand

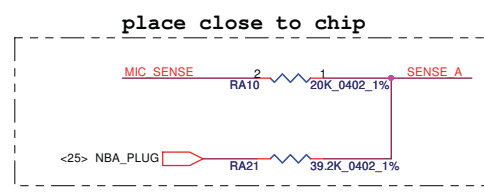


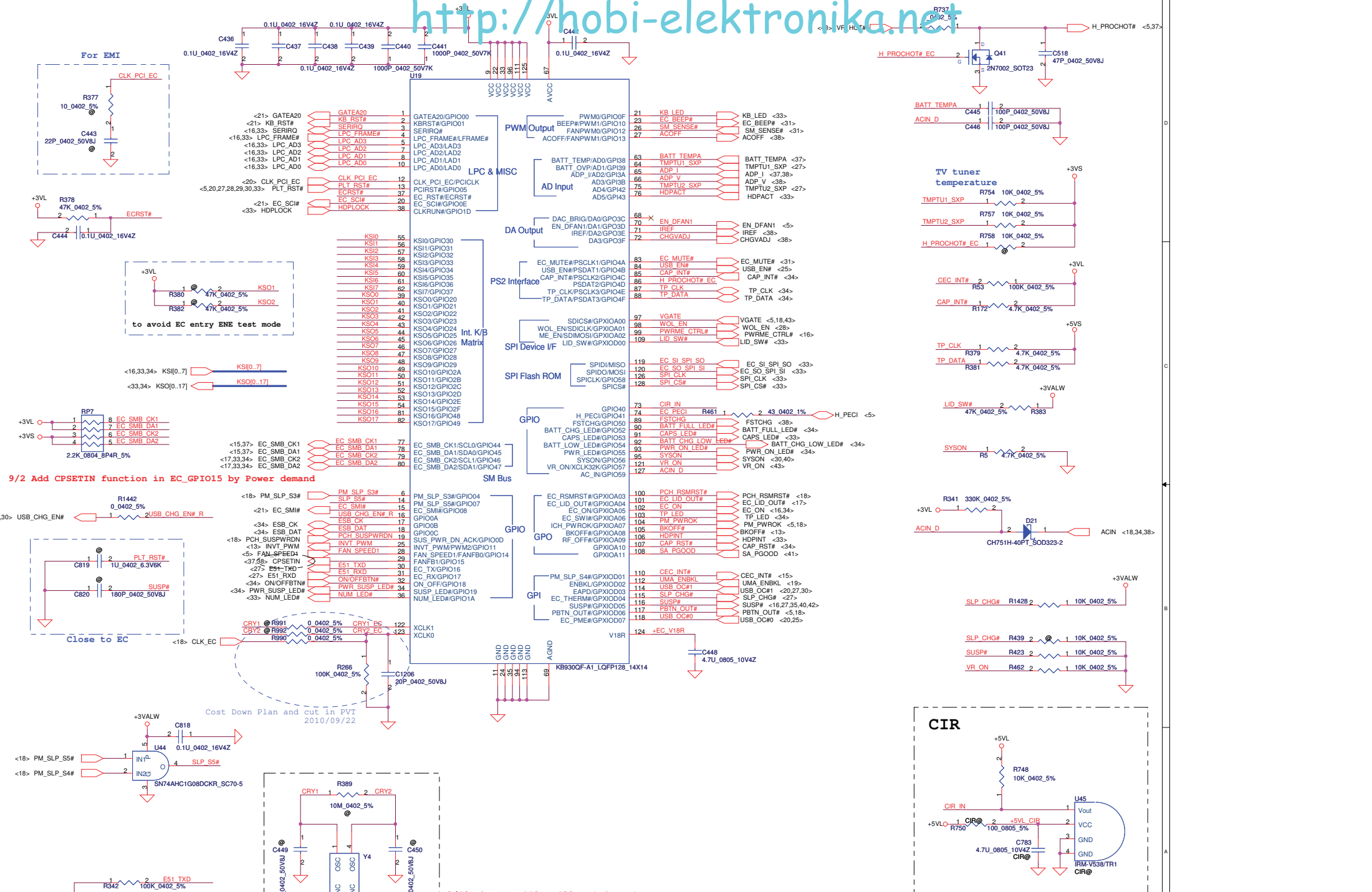
2010/09/17 Add Level shift to avoid +3V leakage from +3VALW\_PCH

Table with 4 columns: Security Classification, Issued Date, Deciphered Date, Title. Includes Compal Secret Data, 200910/9, 2010/01/23, and PCIE-USB3.0 UPD720200A.



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	





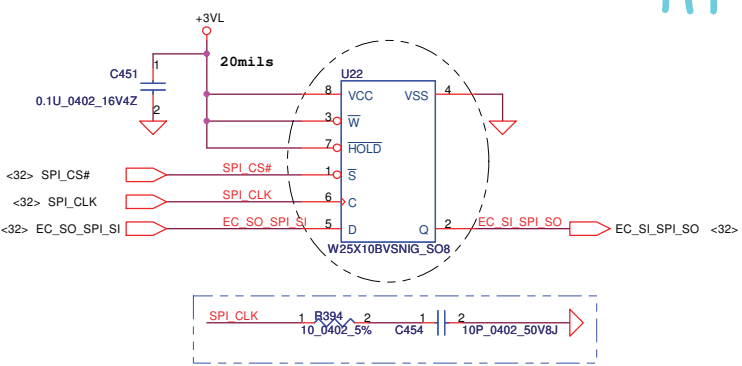
Security Classification	Compal Secret Data	
Issued Date	2010/09/03	Deciphered Date
		2012/12/31

Compal Electronics, Inc.		
LPC-EC-KB930		
Title	PHQAA LA-6832P M/B	
Size	Document Number	Rev
		0.2
Date:	Thursday, October 07, 2010	Sheet 32 of 45

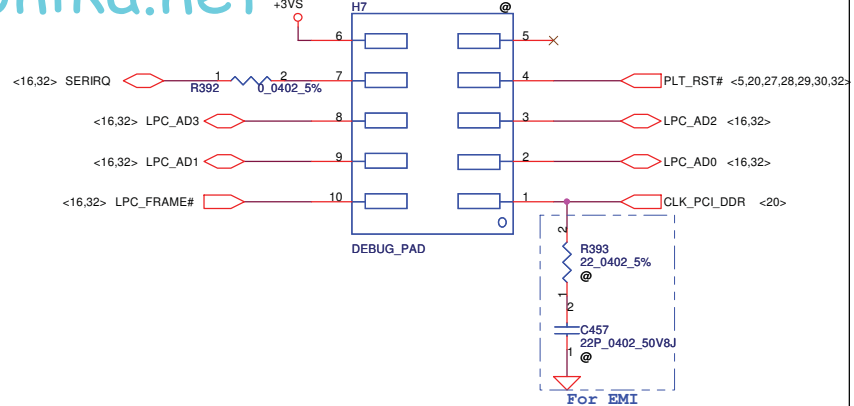
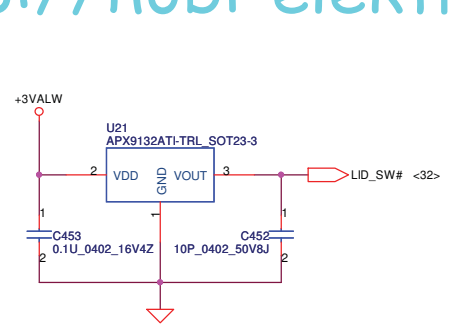
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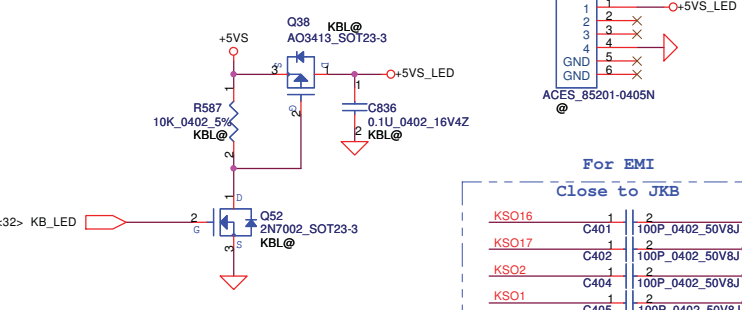
# SPI Flash (256KB)



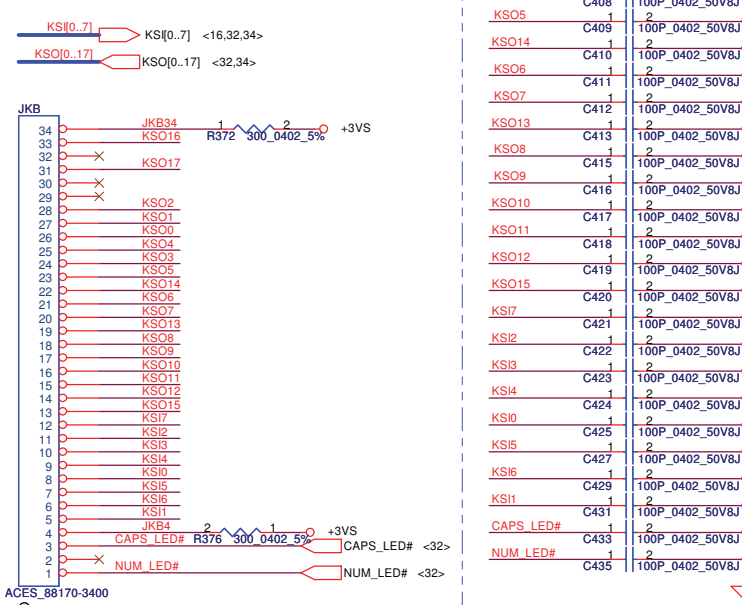
8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00  
 9/03 Change U22 change to SA00003FL10



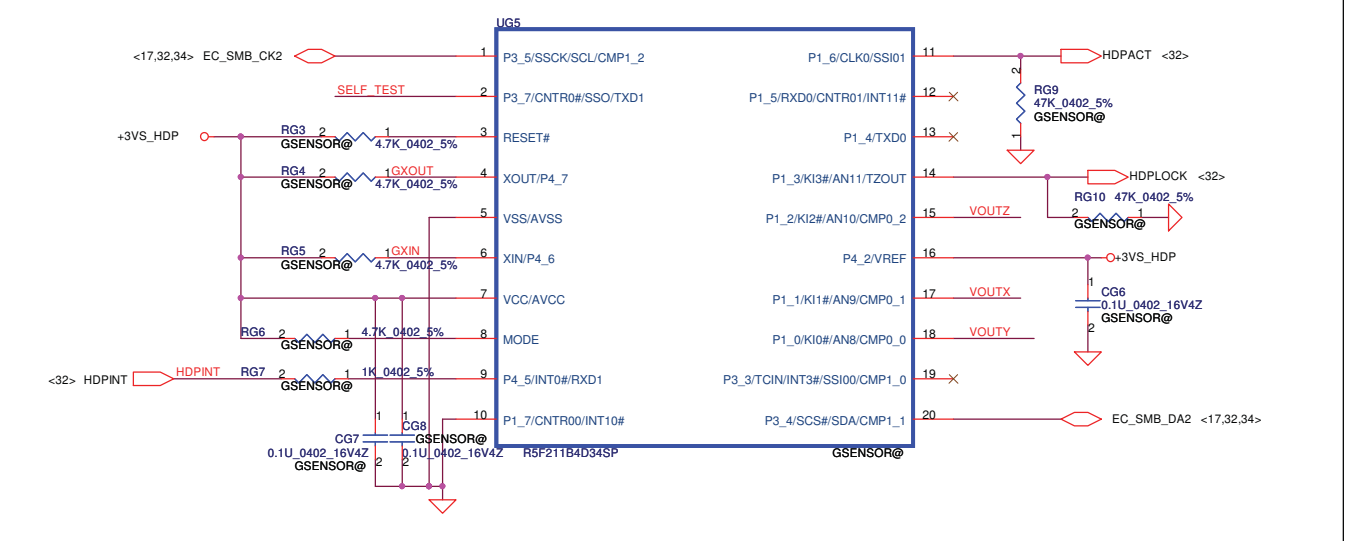
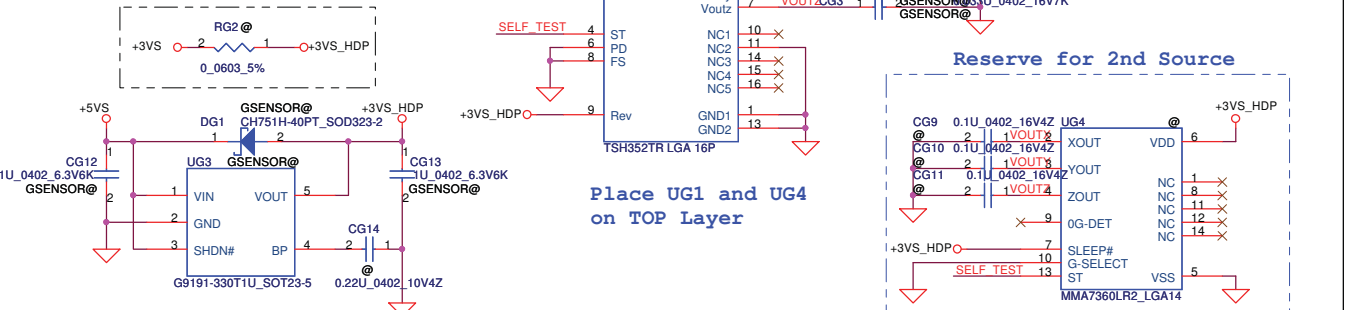
# Keyboard LED



# KEYBOARD CONN.

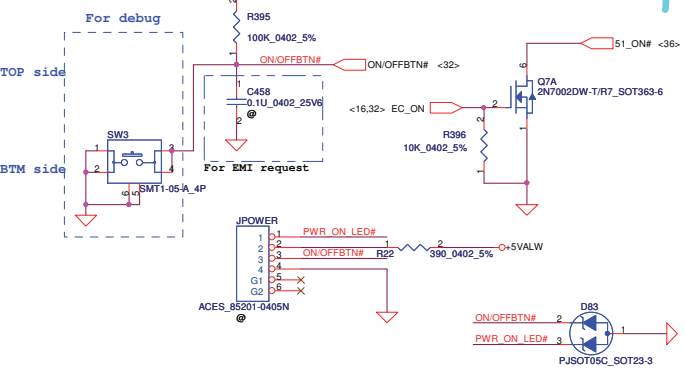


# G-Sensor

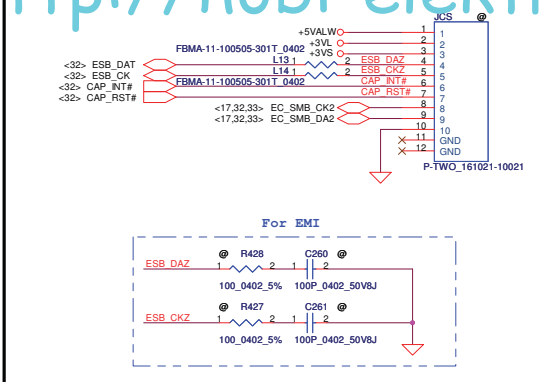


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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				Document Number
				PHQAA LA-6832P M/B
				Rev 0.2
Date:	Thursday, October 07, 2010	Sheet	33	of 45

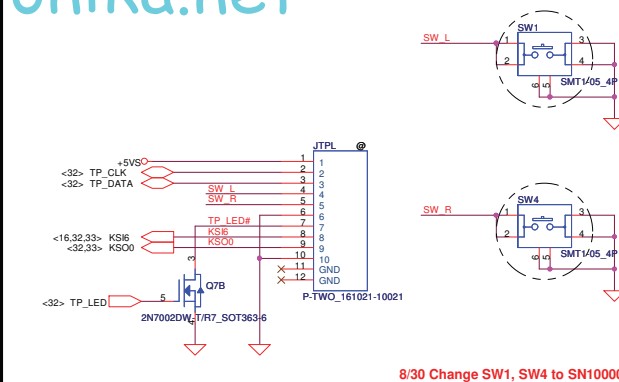
### Power Button



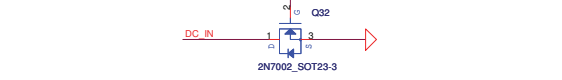
### Cap. Sensor / Light Sensor / Touchpad & Light Pipe Connector



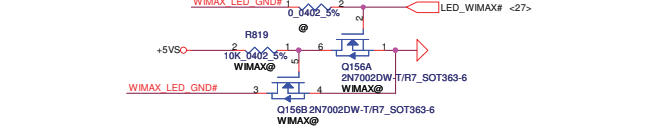
### Cap. Sensor / Light Sensor / Touchpad & Light Pipe Connector



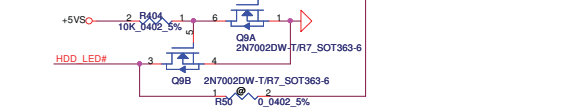
### DC-IN LED



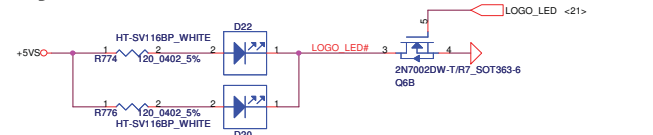
### WiMAX LED



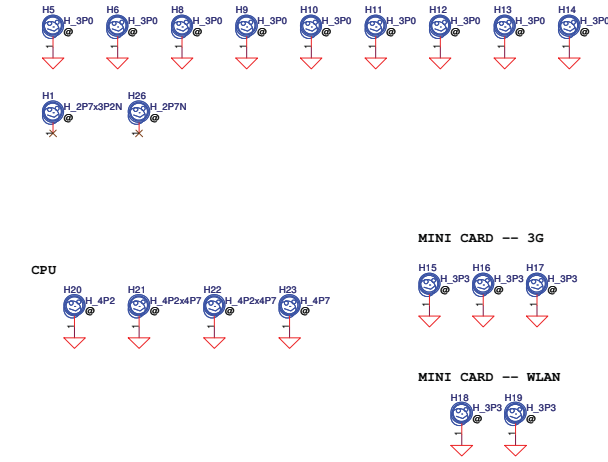
### HDD LED



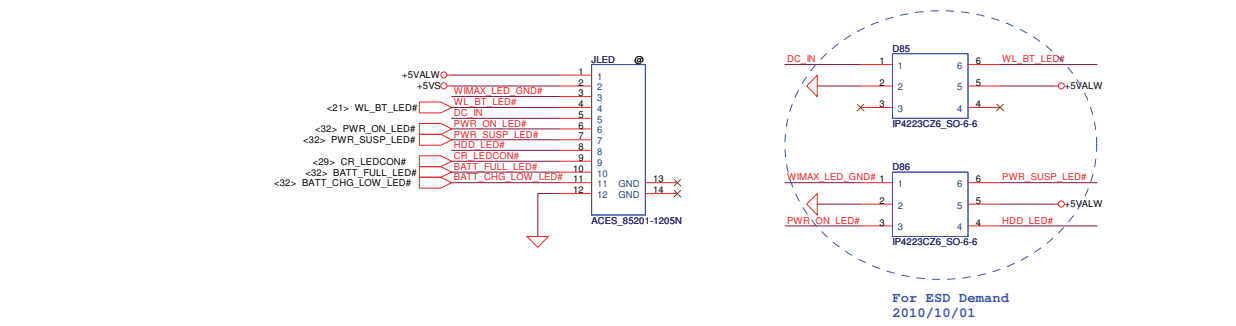
### Logo LED



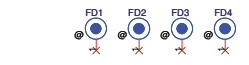
### Screw Hole



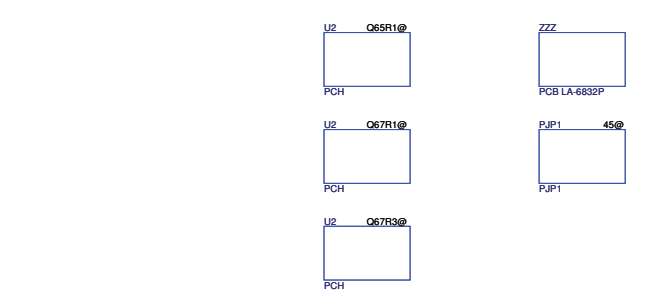
### LED/B Connector



### PCB Federal Mark PAD

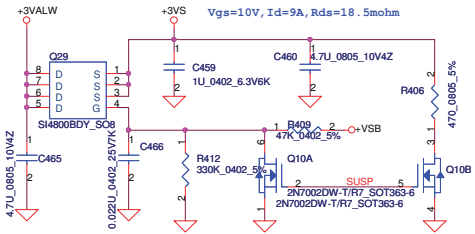


### ISPD



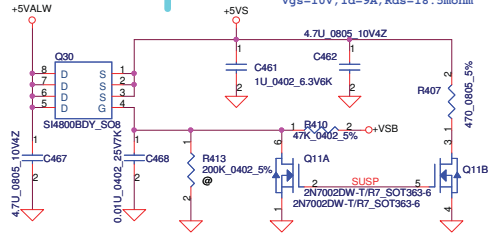
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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Date:	Thursday, October 07, 2010	Sheet	34	of 45

**+3VALW TO +3VS**

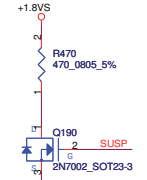
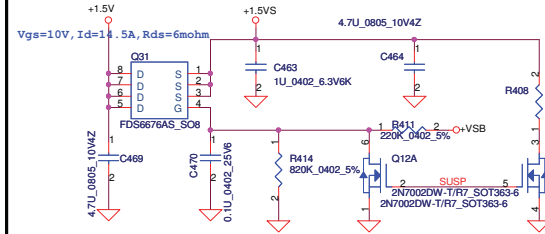


<http://www.hobby-elektronika.net>

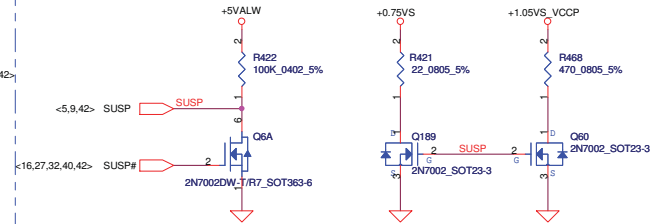
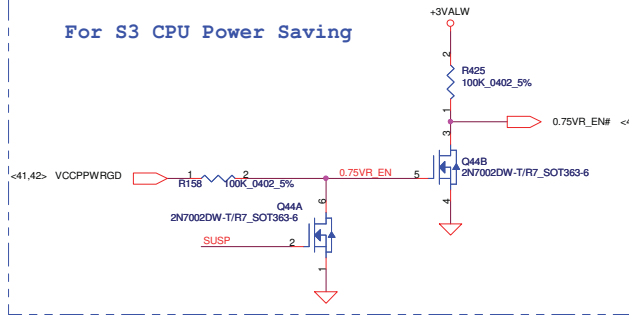
**+5VALW TO +5VS**



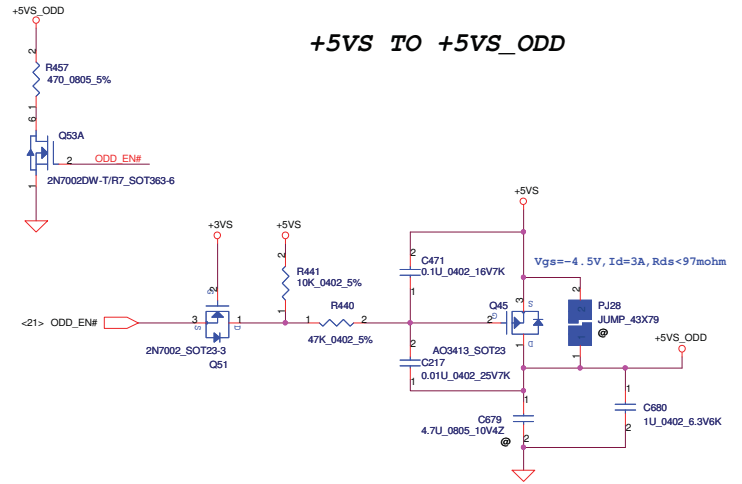
**+1.5V to +1.5VS**



**For S3 CPU Power Saving**

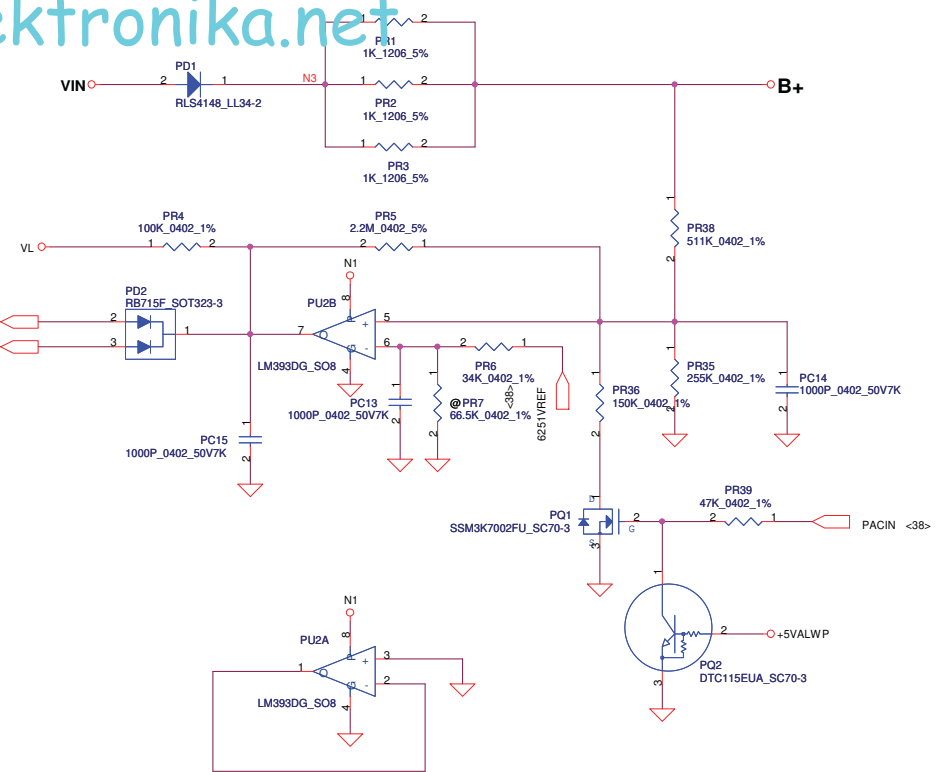
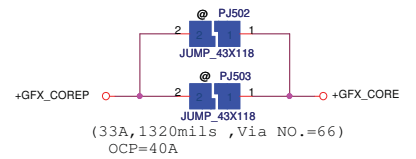
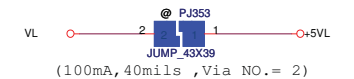
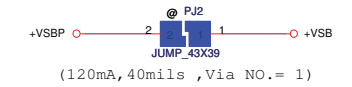
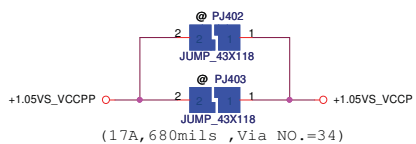
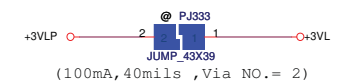
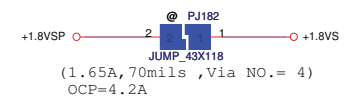
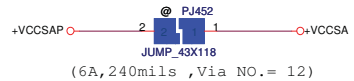
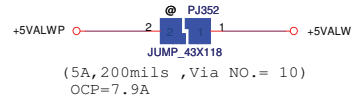
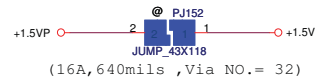
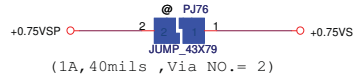
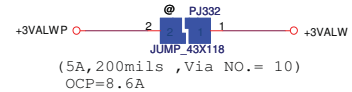
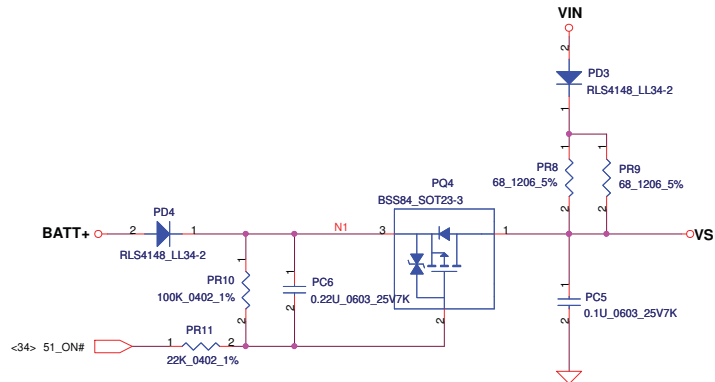
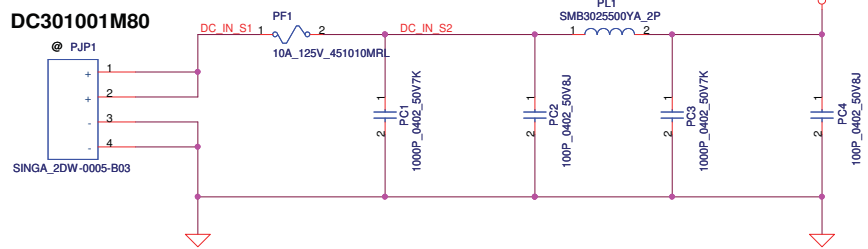


**+5VS TO +5VS\_ODD**

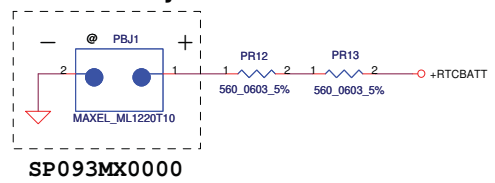


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Size	Document Number	Rev		
	PHQA LA-6832P M/B	0.2		
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DC301001M80



RTC Battery

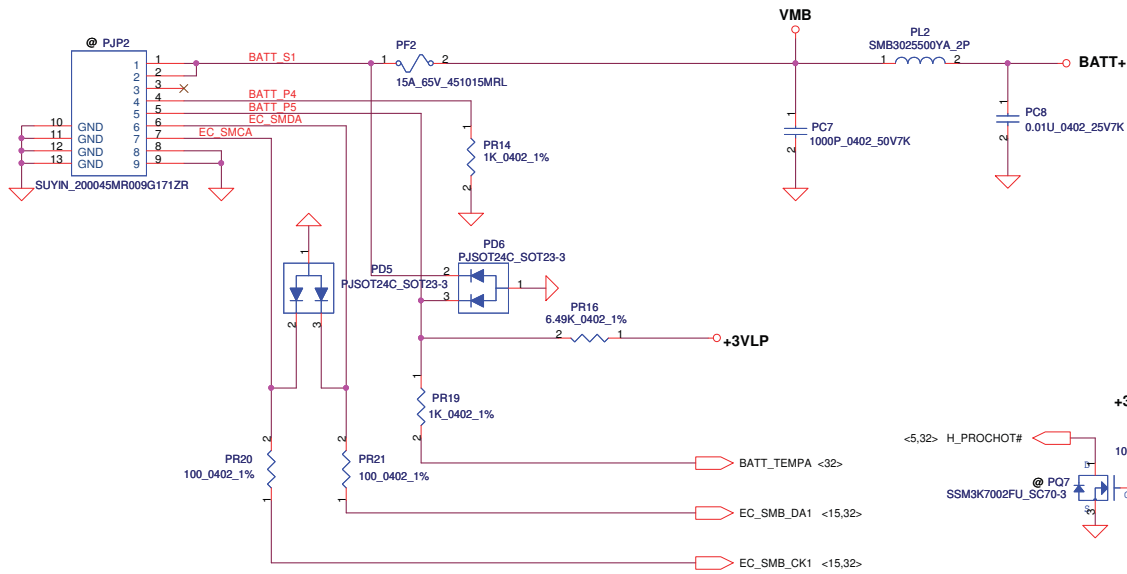


SP093MX0000

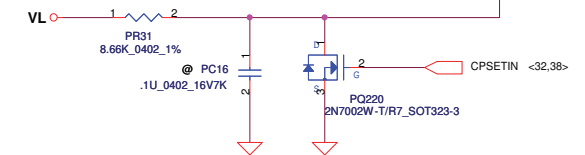
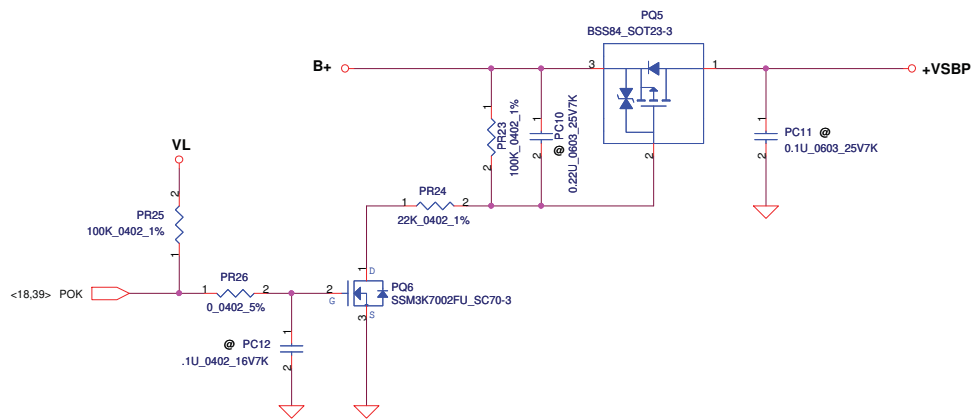
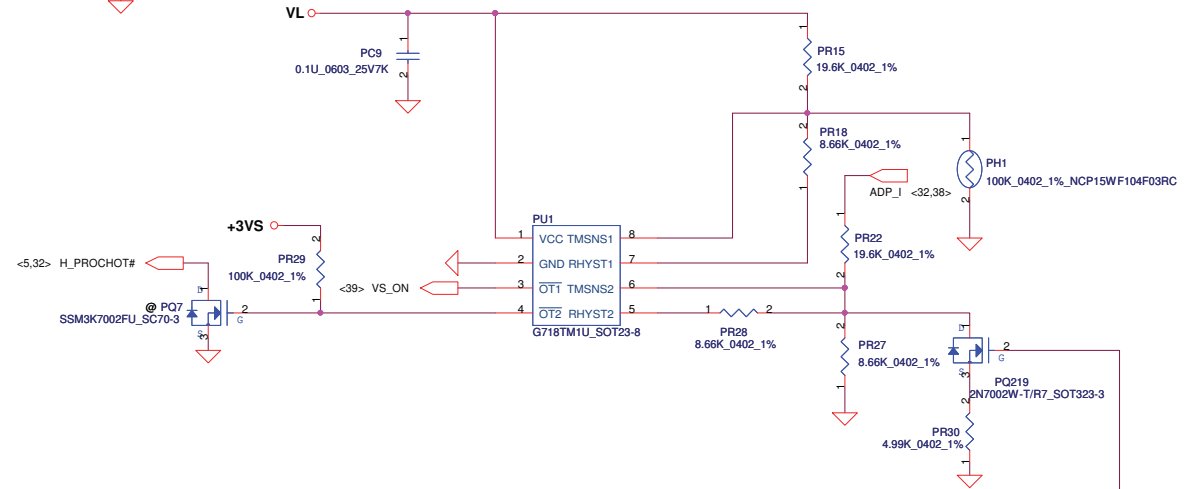
ACIN

Precharge detector			
	Min.	typ.	Max.
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

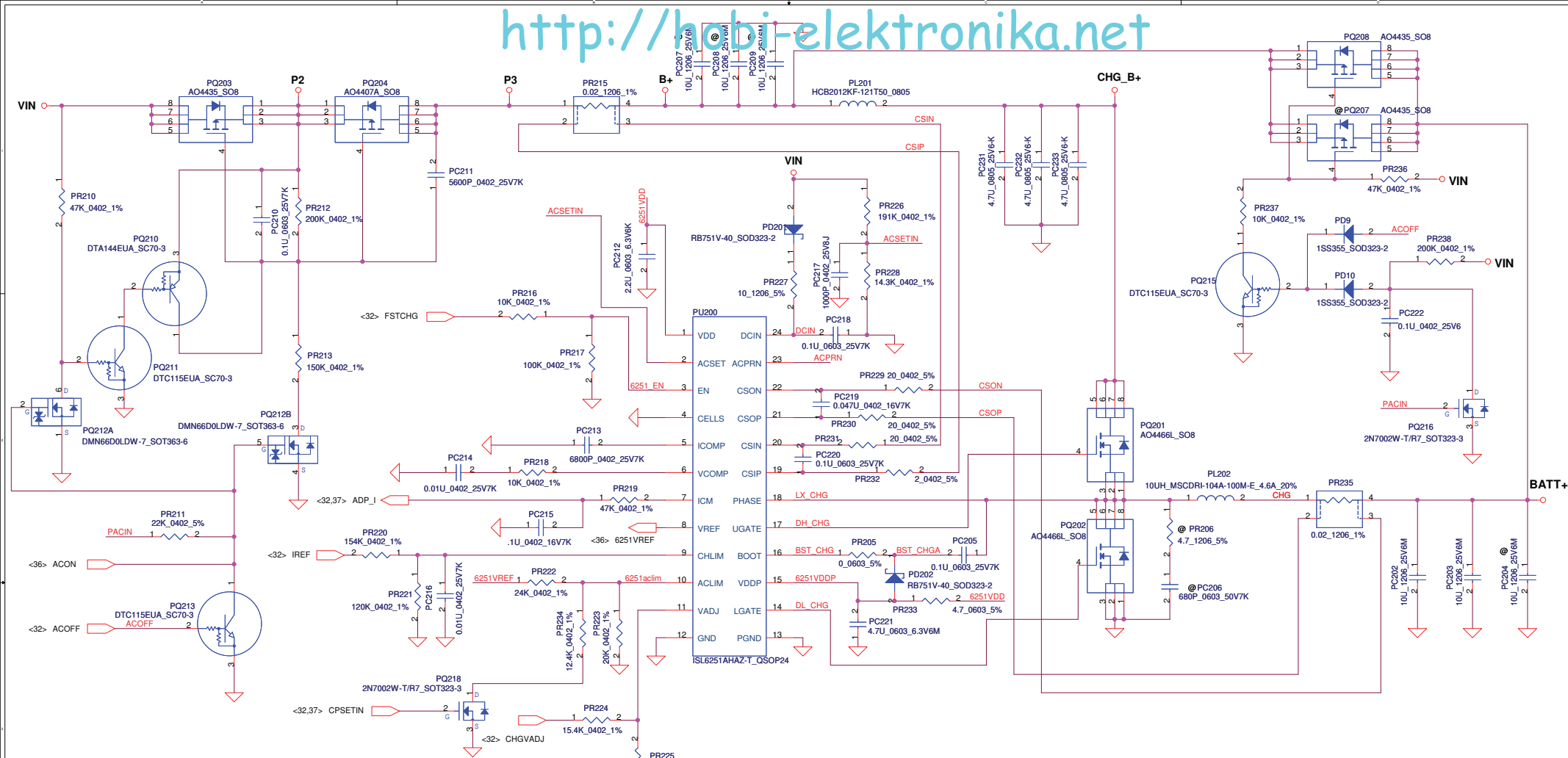
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**PH1 under CPU botten side :**  
 CPU thermal protection at 95 degree C  
 Recovery at 56 degree C



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**CP mode**

I <sub>ada</sub> =0~3.42A (65W)	CP= 92%*I <sub>ada</sub> ; CP=3.147A
V <sub>acLim</sub> =1.08V (65W)	PR222=75k PR223=20k PR45=0.02
I <sub>ada</sub> =0~3.947A (75W)	CP= 92%*I <sub>ada</sub> ; CP=3.63A
V <sub>acLim</sub> =0.736V (75W)	PR222=24k PR223=20k PR45=0.02
I <sub>ada</sub> =0~4.737A (90W)	CP= 92%*I <sub>ada</sub> ; CP=4.36A
V <sub>acLim</sub> =0.736V (90W)	PR222=53.6k PR223=20k PR45=0.015
I <sub>ada</sub> =0~6.316A (120W)	CP= 92%*I <sub>ada</sub> ; CP=5.81A
V <sub>acLim</sub> =0.736V (120W)	PR222=8.25k PR223=26.7k PR45=0.015

CC=0.25A~3A  
 IREF=1.016\*I<sub>charge</sub>  
 IREF=0.254V~3.048V  
 VCHLIM need over 95mV

**CHGVADJ=(V<sub>cell</sub>-4)\*9.445**

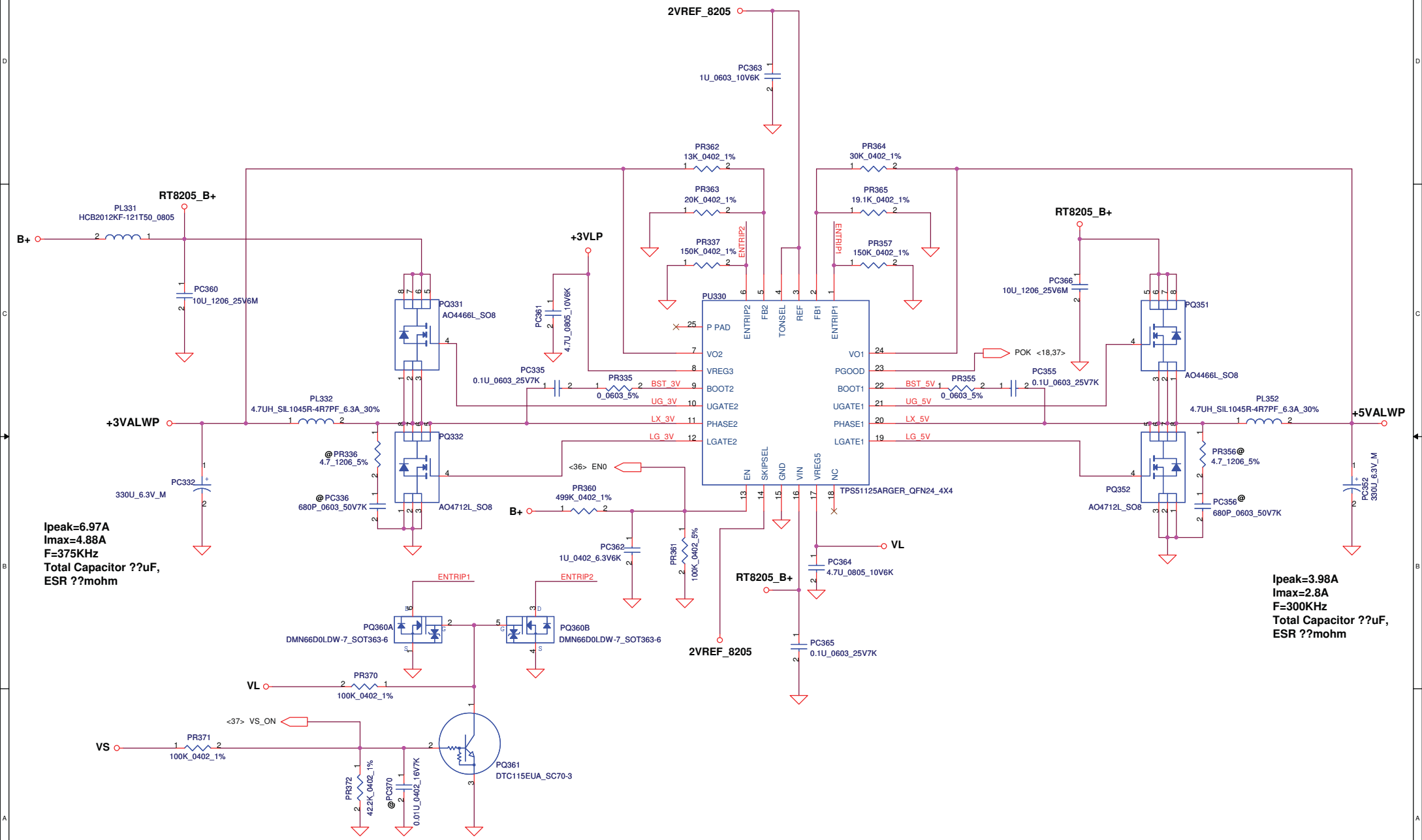
V <sub>cell</sub>	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

**Vin Detector**

High 18.089V  
 Low 17.44V

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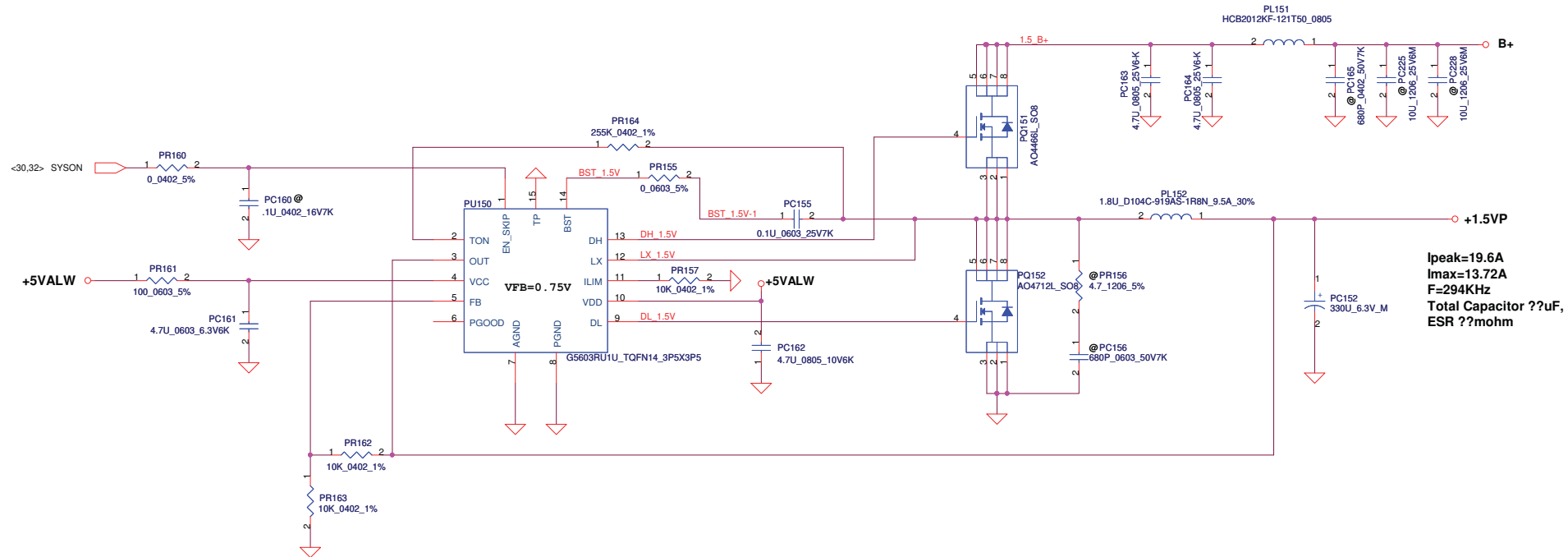
Compal Electronics, Inc.		
<b>CHARGER</b>		
Title	Document Number	Rev
	<b>NHQAA LA-6831P M/B</b>	0.1
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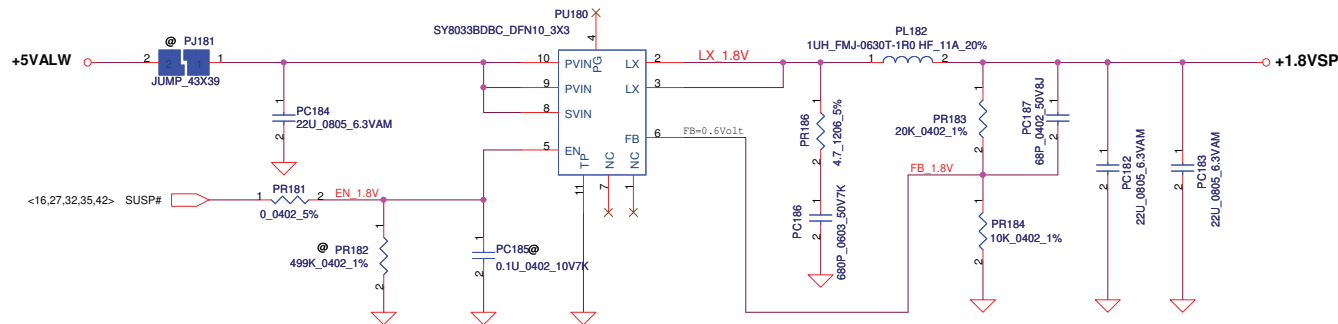
**I<sub>peak</sub>=6.97A**  
**I<sub>max</sub>=4.88A**  
**F=375KHz**  
**Total Capacitor ??uF,**  
**ESR ??mohm**

**I<sub>peak</sub>=3.98A**  
**I<sub>max</sub>=2.8A**  
**F=300KHz**  
**Total Capacitor ??uF,**  
**ESR ??mohm**

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				<b>3VALWP/5VALWP</b>	
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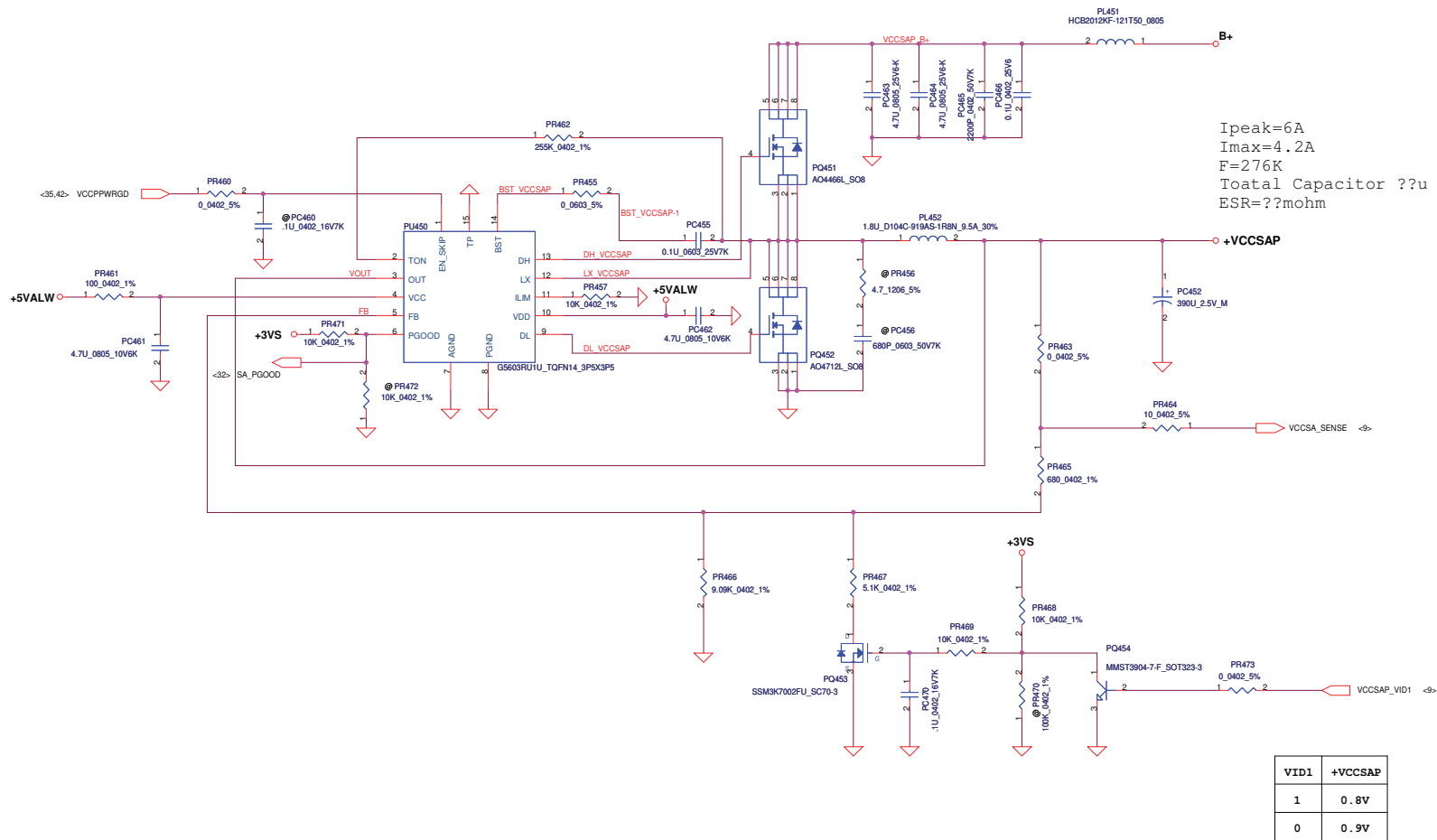
**I<sub>peak</sub>=19.6A**  
**I<sub>max</sub>=13.72A**  
**F=294KHz**  
**Total Capacitor ??uF,**  
**ESR ??mohm**



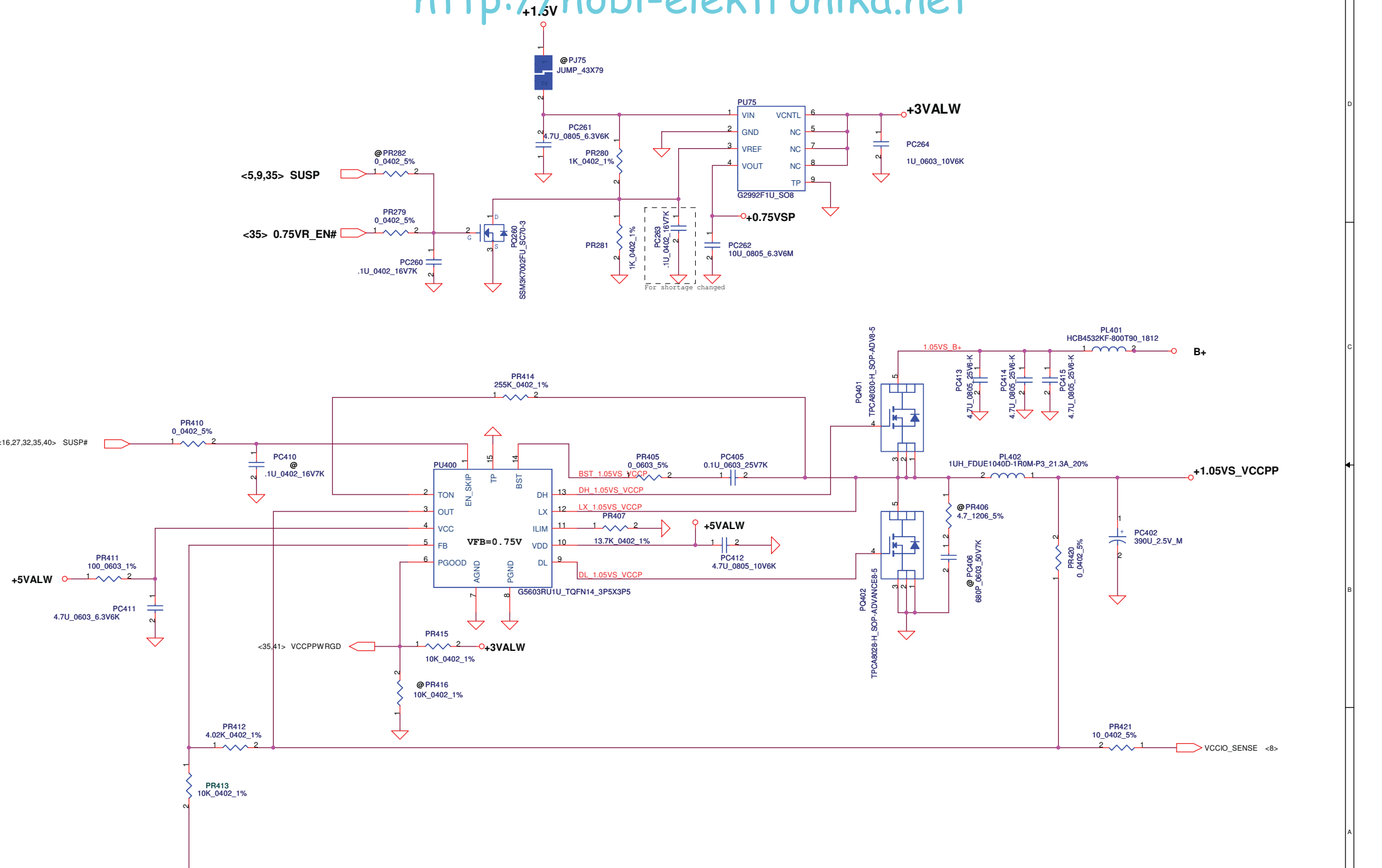
**I<sub>peak</sub>=1.308A**  
**I<sub>LIM</sub> = 4A**  
**F=1MHz**  
**Total Capacitor ??uF,**  
**ESR ??mohm**

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VID1	+VCCSAP
1	0.8V
0	0.9V



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				<b>+1.05V_VCCP/+0.75VSP</b>	
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NO	DATE	PAGE
1.	2010/09/07	P37-PWR_BATTERY CONN / OTP
2.	2010/09/07	P40-PWR+1.5VP/+1.8VSP
3.	2010/09/07	P41-PWR_VCCSAP
4.	2010/09/07	P40-PWR+1.5VP/+1.8VSP
5.	2010/09/07	P53-PWR_VCCSAP
6.	2010/09/07	P50-PWR-CHARGER
7.	2010/09/07	P50-PWR-CHARGER
8.	2010/09/07	P50-PWR-CHARGER
9.	2010/09/07	P55-PWR-CPU_CORE/GFX
10.	2010/09/07	P50-PWR-CHARGER
11.	2010/09/07	P55-PWR-CPU_CORE/GFX
12.	2010/09/07	P55-PWR-CPU_CORE/GFX
12.	2010/09/07	P55-PWR-CPU_CORE/GFX

MODIFICATION LIST
Remove PQ7 SSM317002FU
Change PQ152 to AO4712L
Change PQ452 to AO4712L
Change PQ151 to AO446L
Change PQ451 to AO446L
Change PQ201,PQ202 to AO4466L
Change PQ203 to AO4435L and remove PQ207
Add PR234 12.4k
Add PR560 0 Ohm
Add PR222 24k and PR223 20k
Add PR544 3.83k,PR545 27.4k,PH502 470k
Change PR551 from 3.83k to 3.65k
Change PC550 0.33u to 0.22u and add PC551 0.1u

PURPOSE
Adapter protect circuit not ready
Use same part number
Use same part number
Use same part number
Use same part number
Use same part number
For UMA SKU
For DC and QC CP setting
Set CPU VBOOT to 0V
For CP setting
Add CPU NTC NET
For CPU_CORE load line
For shortage issue

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# HW PIR (Product Improve Record)

<http://hobi-elektronika.net>

NHQAA LA-6832P SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2010/09/03

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	07/21		Delete	306, DHDMI@, DIS@, EDP@, NO3D@, OPT@, UMA@
2)	08/11		Update room	
3)	08/11	09	Change	R119 change to @
4)	08/12	16	Add	R442, R443
5)	08/12	16	Change	R572, R573, R574, R575, R569 from @ to mount
6)	08/12	20	Remove	USB20_P3/N3 from PCH
7)	08/12	30	Remove	RT1, USB20, RT14, RT20, RT23, RT24
8)	08/12	32	Change	C449, C450, Y4 from @ to mount
9)	08/13	15	Change	L8, L9 L10, L11 from SM070001600 to SM070001310
10)	08/13	30	Change	RT11 to @
11)	08/13	30	Change	RT19 to USB30@
12)	08/13	30	Change	CT3 from SE000005TNO to SE000005T80
13)	08/13	30	Remove	RT25, RT27
14)	08/17	5	Remove	R14
15)	08/18	6	Reserve	R33
16)	08/18	9	Reserve	R119
17)	08/18	11	Remove	R32, R89
18)	08/18	12	Remove	R35, R97
19)	08/18	26	Reserve	C236, C268, C490
20)	08/18	15	Remove	R435, R438, R453(0 ohm)
21)	08/18	15	Change	R195, R197, R198, R202, R201, R203, R205, R206 to SD028680080
22)	08/18	15	Remove	R207
23)	08/18	18	Change	Net name from PM_CLKRUN# to PCH_GPIO32
24)	08/18	20	Change	R324 From 1K to 2.2K
25)	08/18	21	Remove	PCH PECC signal
26)	08/18	25	Remove	C363, C364, C365, C366
27)	08/18	30	Change	U14 to SA00004600
28)	08/18	30	Change	USB30@ to always mount
29)	08/18	27	Remove	all new card function
30)	08/20	9	Add	PJ32
31)	08/20	13	Swap	USB20_P11 and USB20_N11
32)	08/20	25	Swap	USB20_F0, USB20_N0, USB20_P1, USB20_N1
33)	08/23		Update Power schematic	
34)	08/23	20	Swap	PCI_PIRQC#, PCH_GPIO4, PCH_GPIO2, PCI_PIRQA#
35)	08/23	20	Swap	SLP_CHG_M3, SLP_CHG_M4, USB_OC#0
36)	08/30	18	Reserve	R259
37)	08/30		Change	USB3.0 Connector
38)	08/30	21	Add	USB Sleep & Charge MAXIC_Select pin in GPIO71(Remove T73)
39)	08/30	25	Change	C426 to Aluminum Solid Cap 220u
40)	08/30	27	Add	USB Sleep & Charge IC: MAX14550E
41)	08/30	28	Add	16pin X'form for cost down, and P/N is SP050006E00
42)	08/30	28	Change	PWRME_CTRL# from PCH_GPIO32 to HDA_SDO
43)	08/30	16	Change	U53 Pin 9 from KS14 to KS13
44)	08/30	16	Change	R442, R443 from 10k to 100K
45)	08/30	16	Change	U56 Pin3 from KSO6 to +5VALW
46)	08/30	16	Add	R227 100k ohm
47)	08/30	28	Reserve	D85 and D86
48)	08/30	30	Swap	USRXDNI_R, USRXDNI_R_L, USRXDP1_R, USRXDP1_R_L
49)	08/30	16	Change	U13 from SA000021A00 to SA000031N00
50)	08/30	27	Reserve	R1443 for WLAN Mini PCIE Card Pin5
51)	08/30	33	Change	U22 From SA00003GK00 to SA00003GM10
52)	08/30	34	Change	SW1, SW4 to SM100002Y00
53)	09/01	28	Add	L15 for ISM Test
54)	09/01	31	Change	R112 from 10k to 4.7kohm and CA18 from 0.1uF to 100pF
55)	09/01	32	Add	CPSETIN to power
56)	09/01	18,20,21	Reserve	C894, C895, C896, C897
57)	09/02	08	Remove, add	C126, C131 and add C898 3Pin Bulk Cap
58)	09/02	27	Add	14566@ & 14550@
59)	09/02	27	Change	U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4
60)	09/02	33	Change	EC ROM size from 256KB(SA00003GM10) to 128KB(SA00003PL10)
61)	09/02	11	Change	C165,C166,C168,C171,C174,C176,C178 from SE093106M80 to SE000005T80
62)	09/02	12	Change	C191,C192,C194,C197,C200,C202,C204 from SE093106M80 to SE000005T80
63)	09/02		Change	CT25 from SE093106K80 (10uF_0805) to SE000005T80 (10uF_0603)
64)	09/03	08	Change	C890, C891, C894 from SGA00005K00 to SGA00004X80
65)	09/06	33	Change	U22 change to SA00003PL10
66)	09/06	28	Delete	UL4 8105ELDQ@ and 8105ESWR@

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HW-PIR

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