

# Compal Confidential

## Everest Schematics Document

Intel Merom Processor with Calistoga + DDRII + ICH7M

2007-05-15

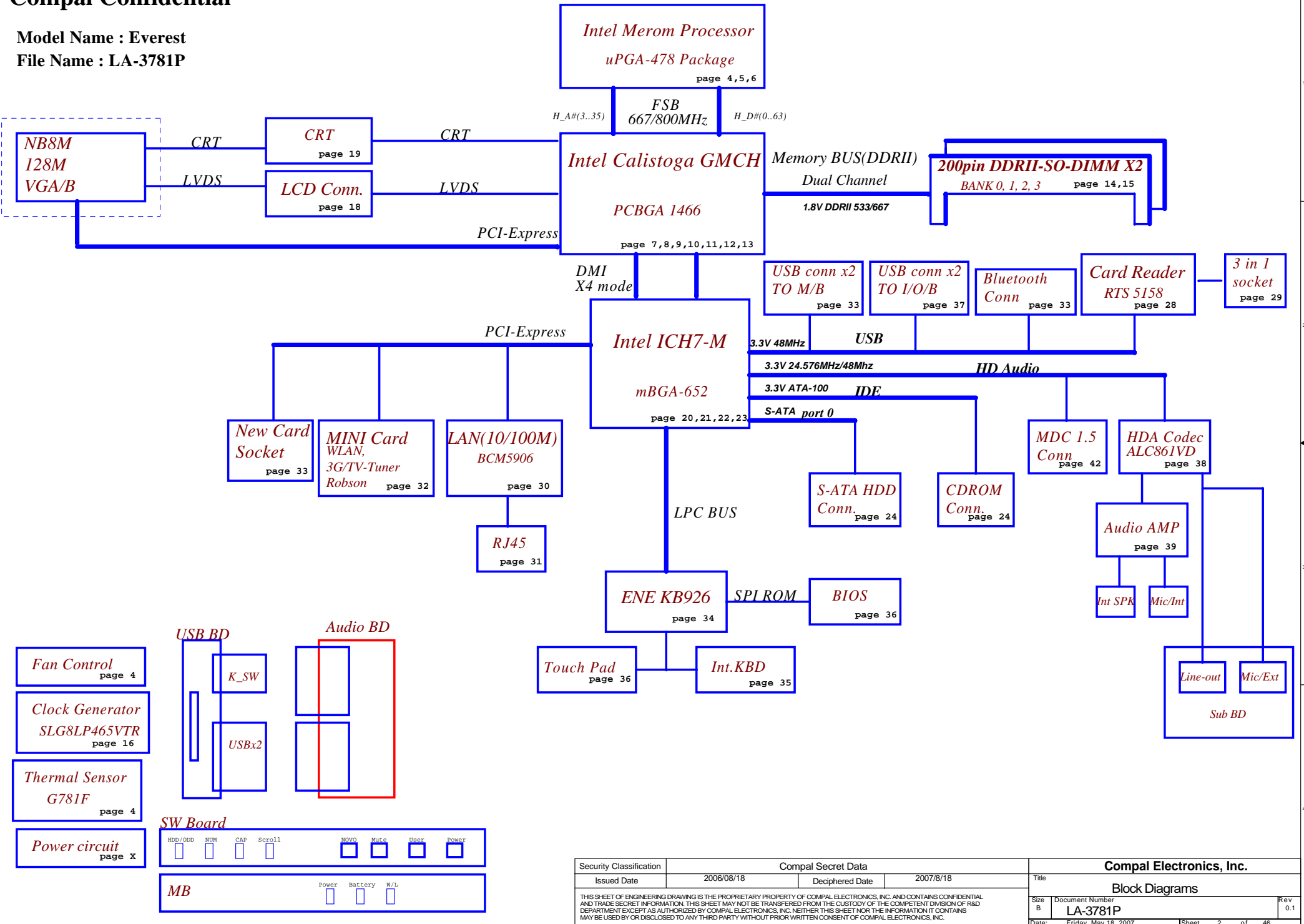
REV: 1.0

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*kyexain@hotmail.com*

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Model Name : Everest  
File Name : LA-3781P



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Title Block Diagrams			
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
No PCI Device			

## No PCI Device

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	GMT-781	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## ICH7M SM Bus address

Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb
Wireless	
NewCard	
LAN	

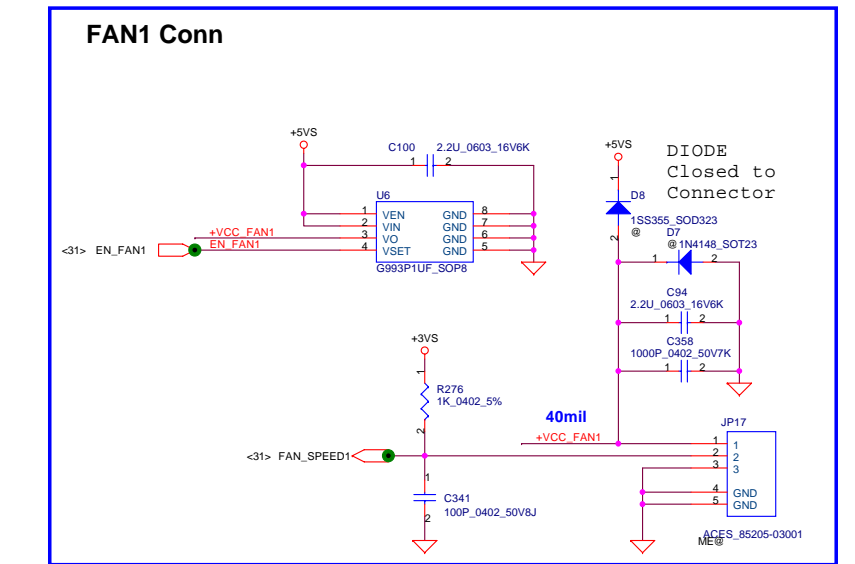
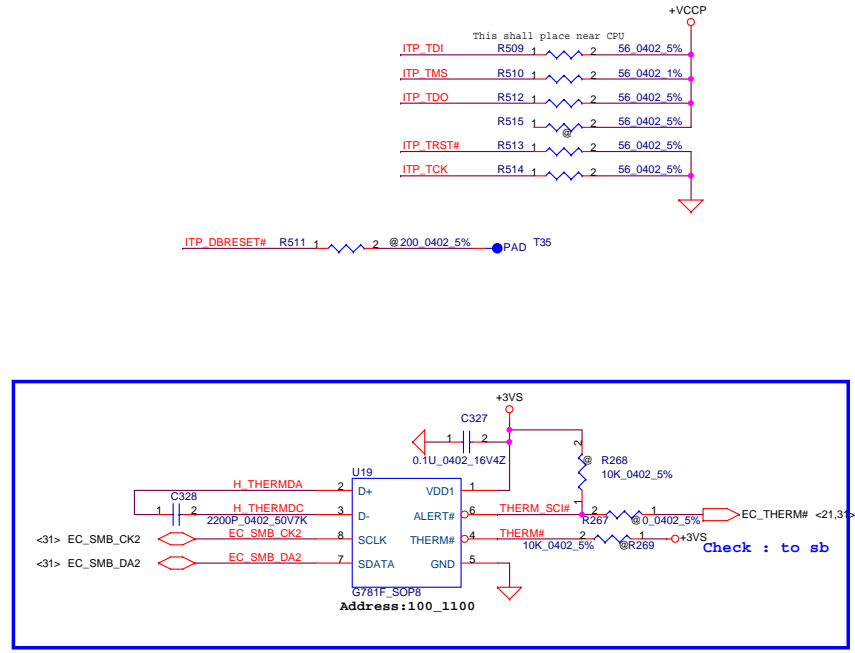
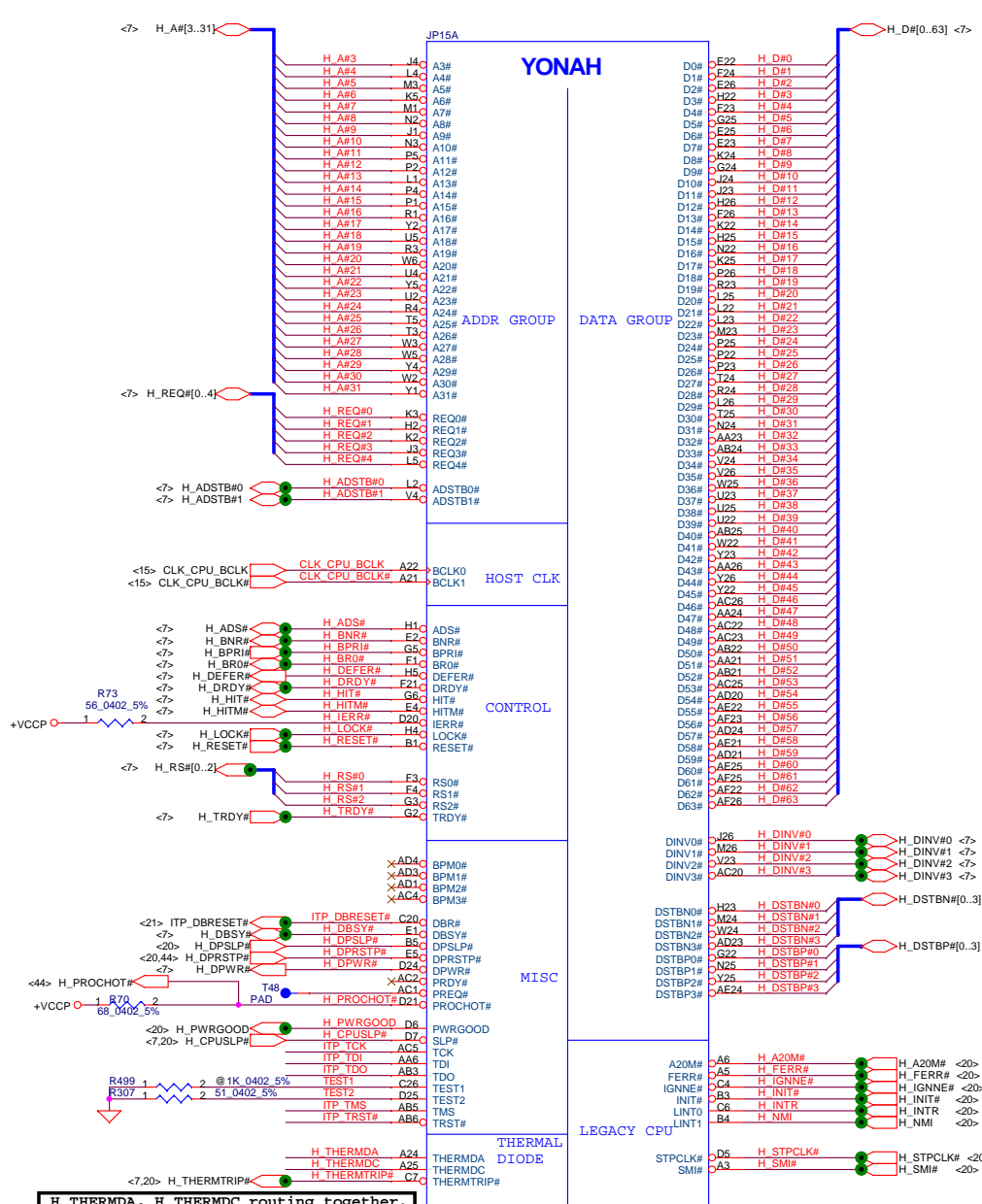
## BOARD ID Table

ID	BRD ID	R54/42 (Rb)	Vab
IHL00	0	R01 (EVT)	0
	1	R02 (DVT)	8.2K
	2	R03 (PVT)	18K
IHLV3	3	R10A (MP)	33K
	4	R01 (EVT)	56K
	5	R02 (DVT)	100K
	6	R03 (PVT)	200K
IGT30	7	R10A (MP)	NC

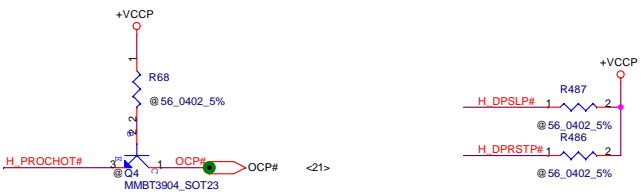
## PANEL ID Table

ID	UMA_DES	Vab
0	IHL00/IGT30 UMA	3.30V
1	IHLV3 UMA	2.20V
2		
3		
4		
5		
6	IHLV2 VGA	0.25V
7	IHL00/IGT30 VGA	0V

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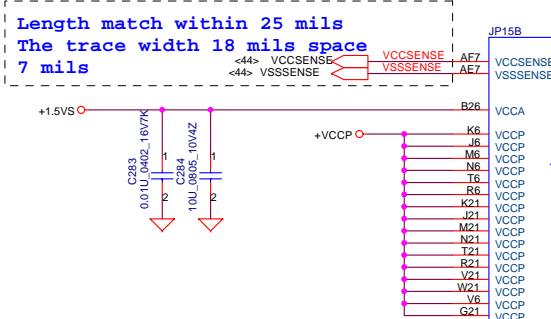
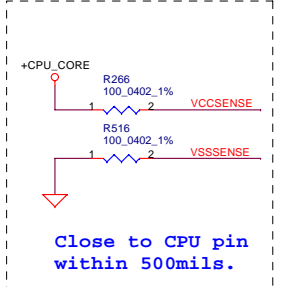
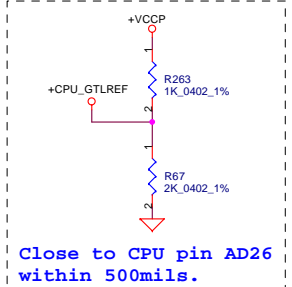
H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil



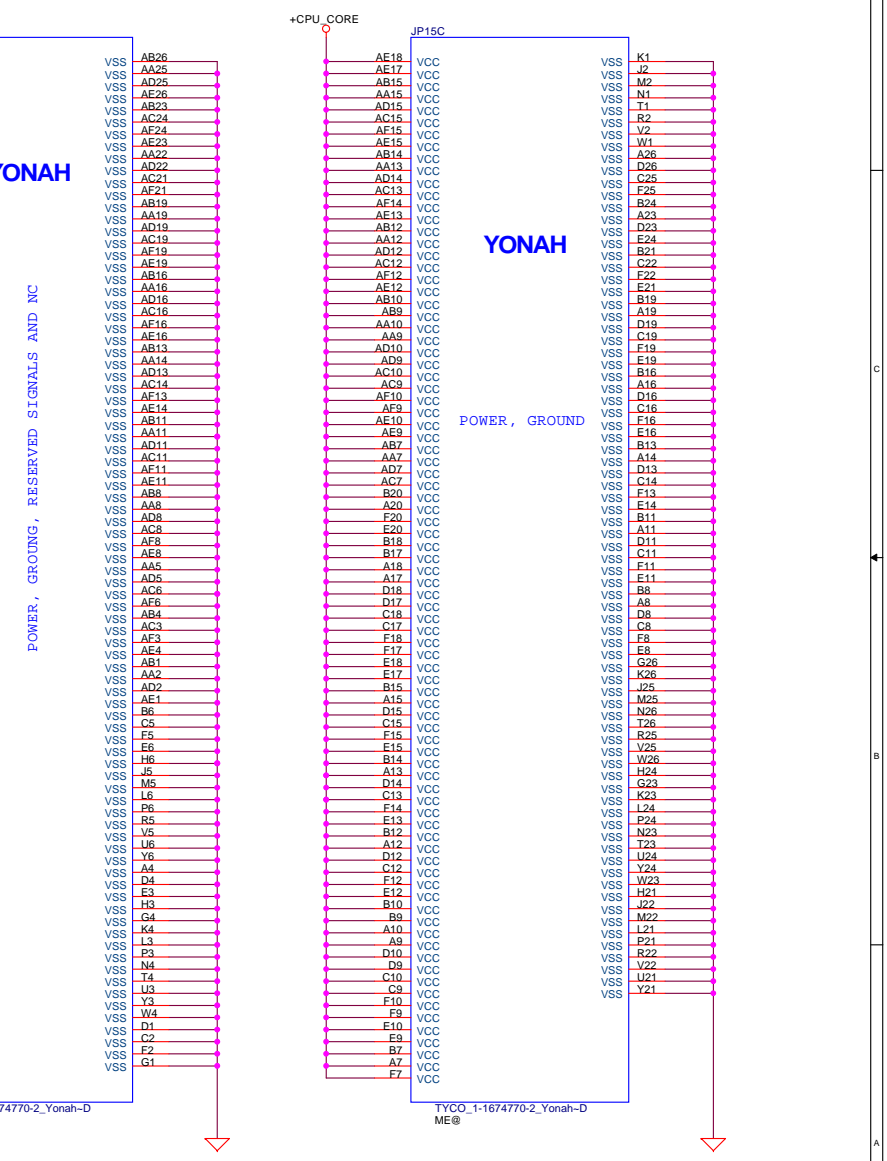
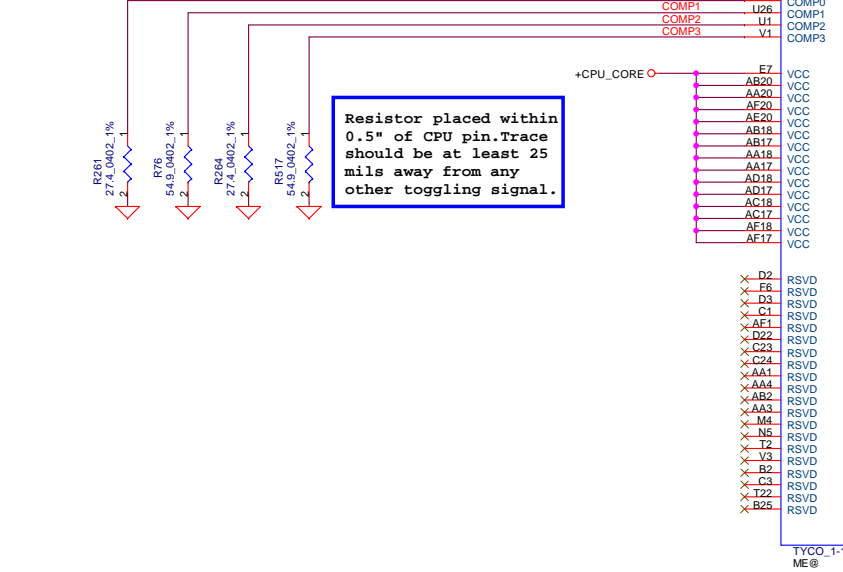
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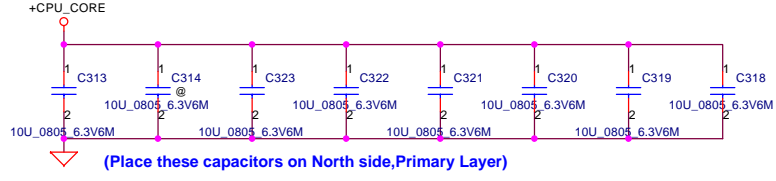
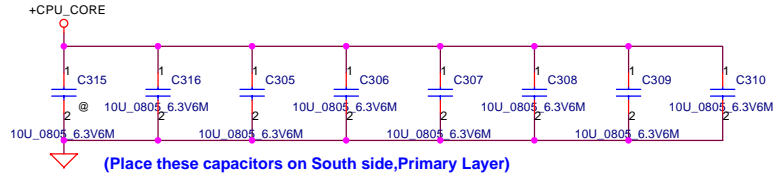
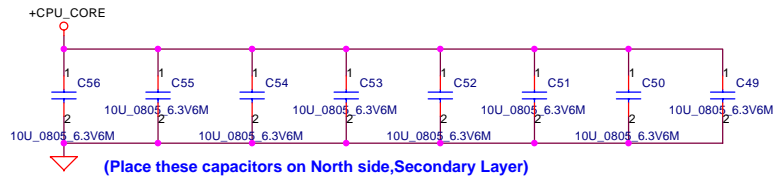
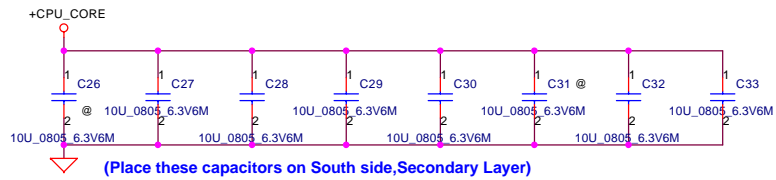
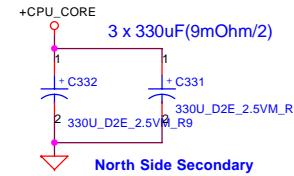
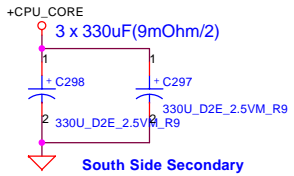
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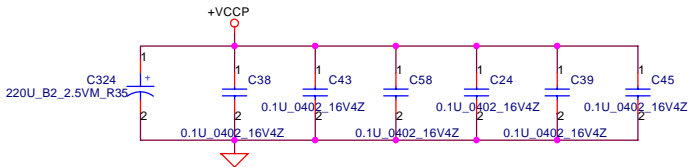
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



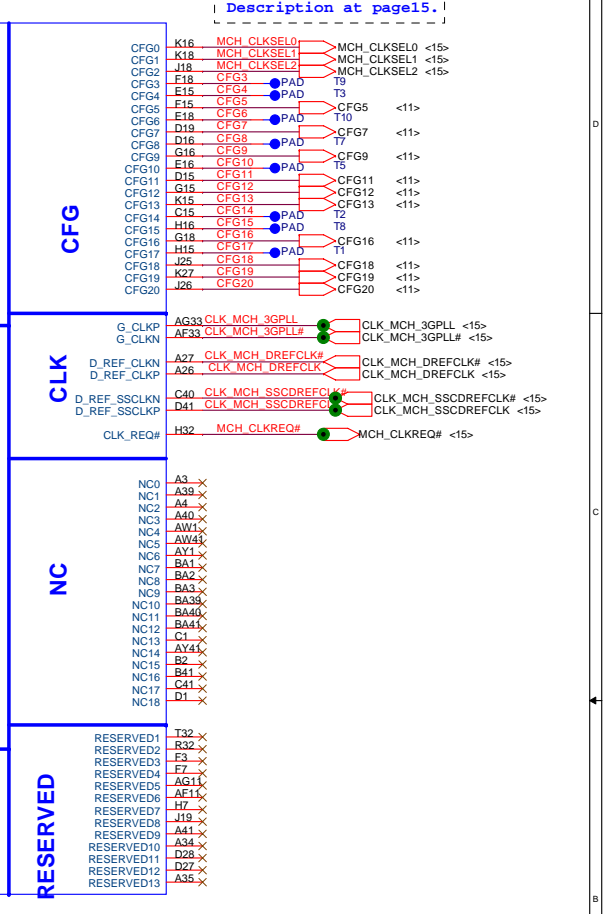
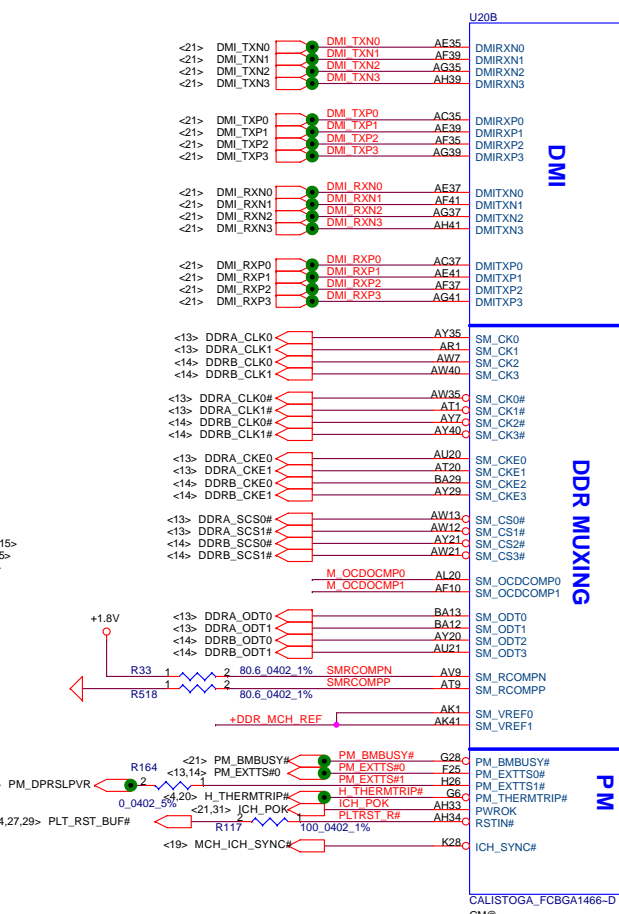
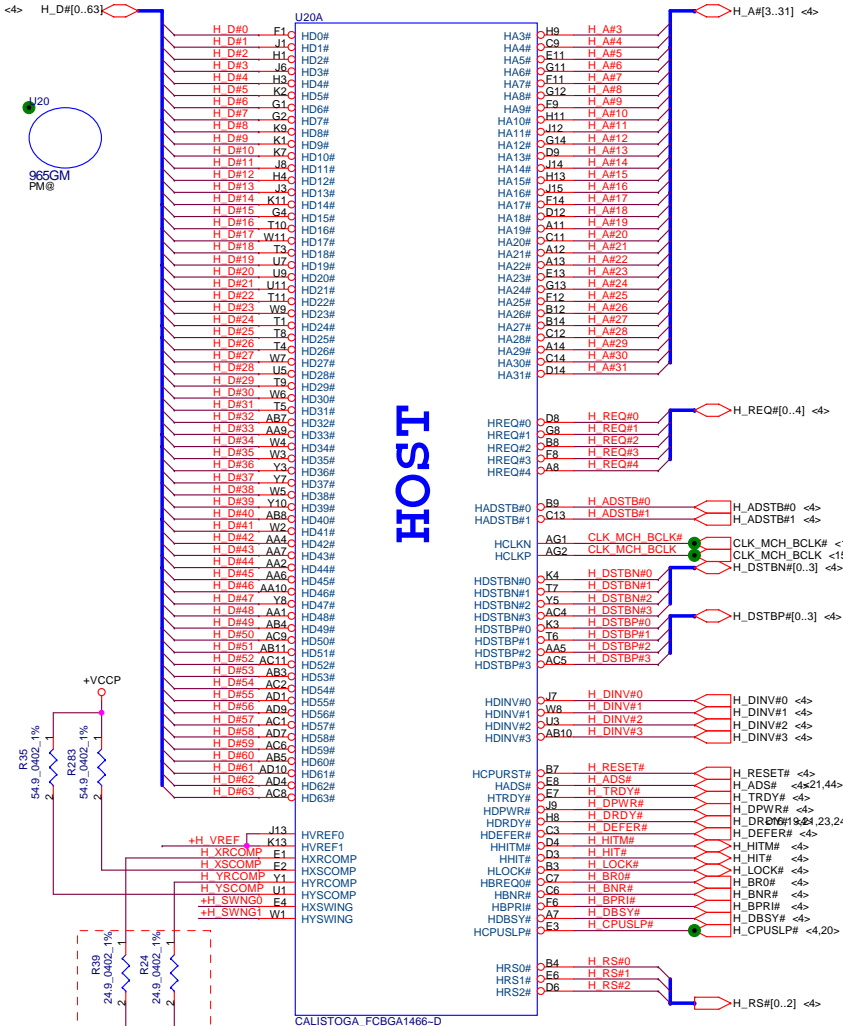


9/25 10U checked. OK for use!

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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Description at page 5.

**HOST**

**DDR MUXING**

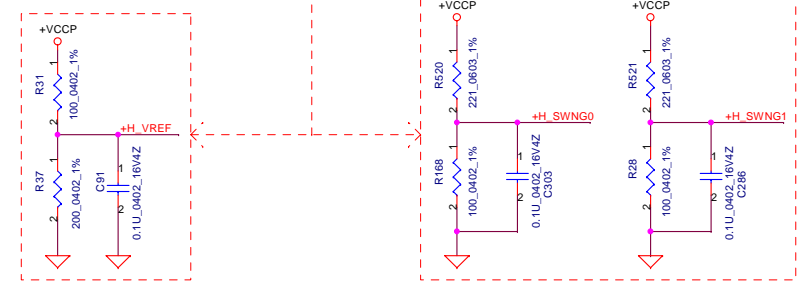
**NC**

**PM**

**RESERVED**

**Layout Note:**  
+DDR\_MCH\_REF trace width and spacing is 20/20.

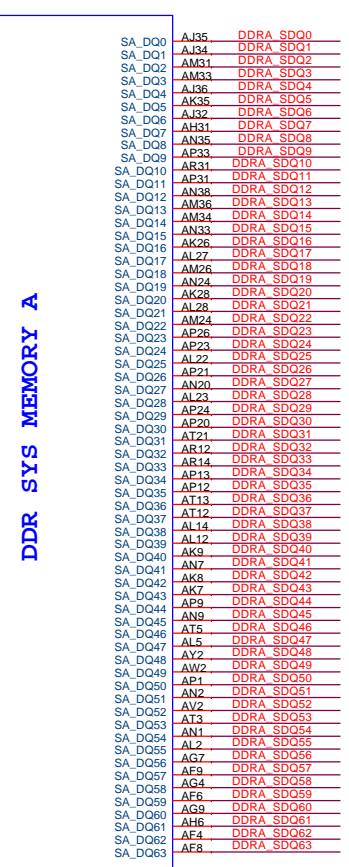
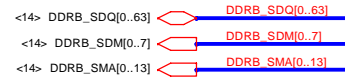
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H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 10/20.



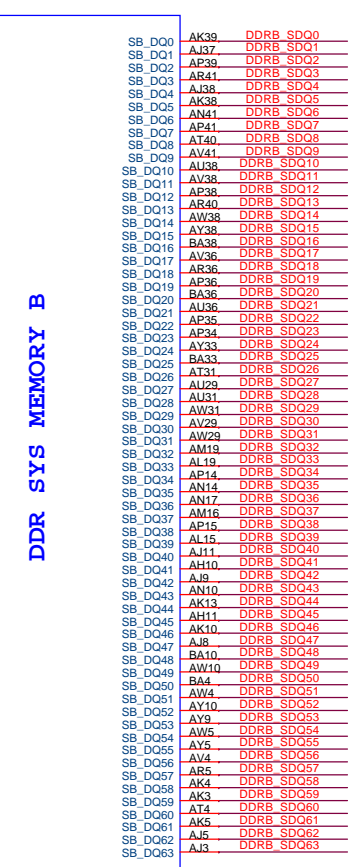
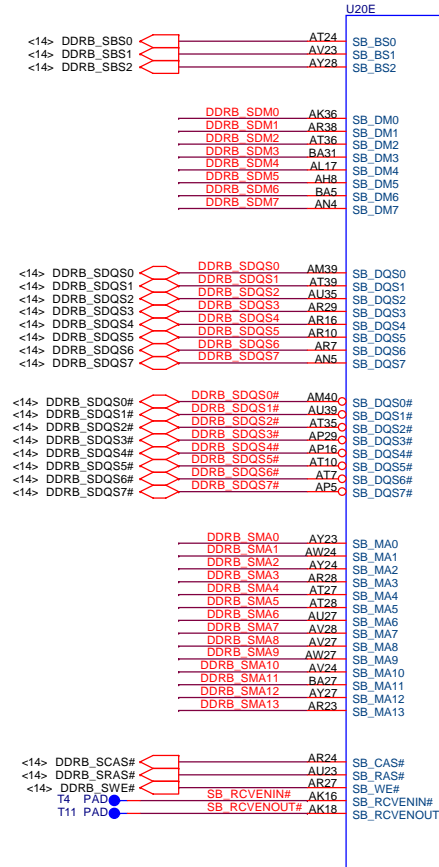
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DDR SYS MEMORY A



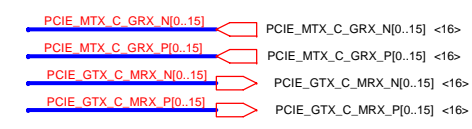
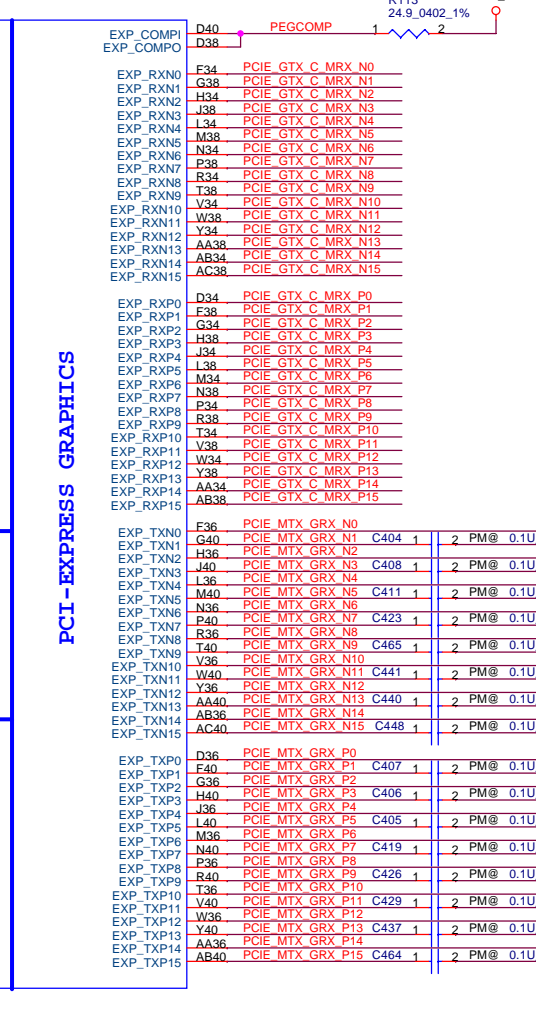
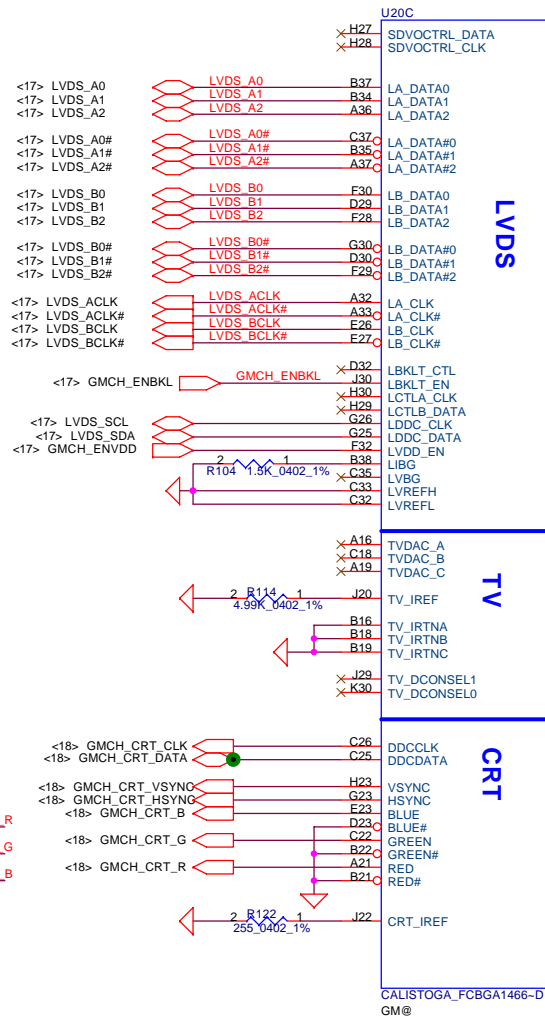
DDR SYS MEMORY B

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GM@

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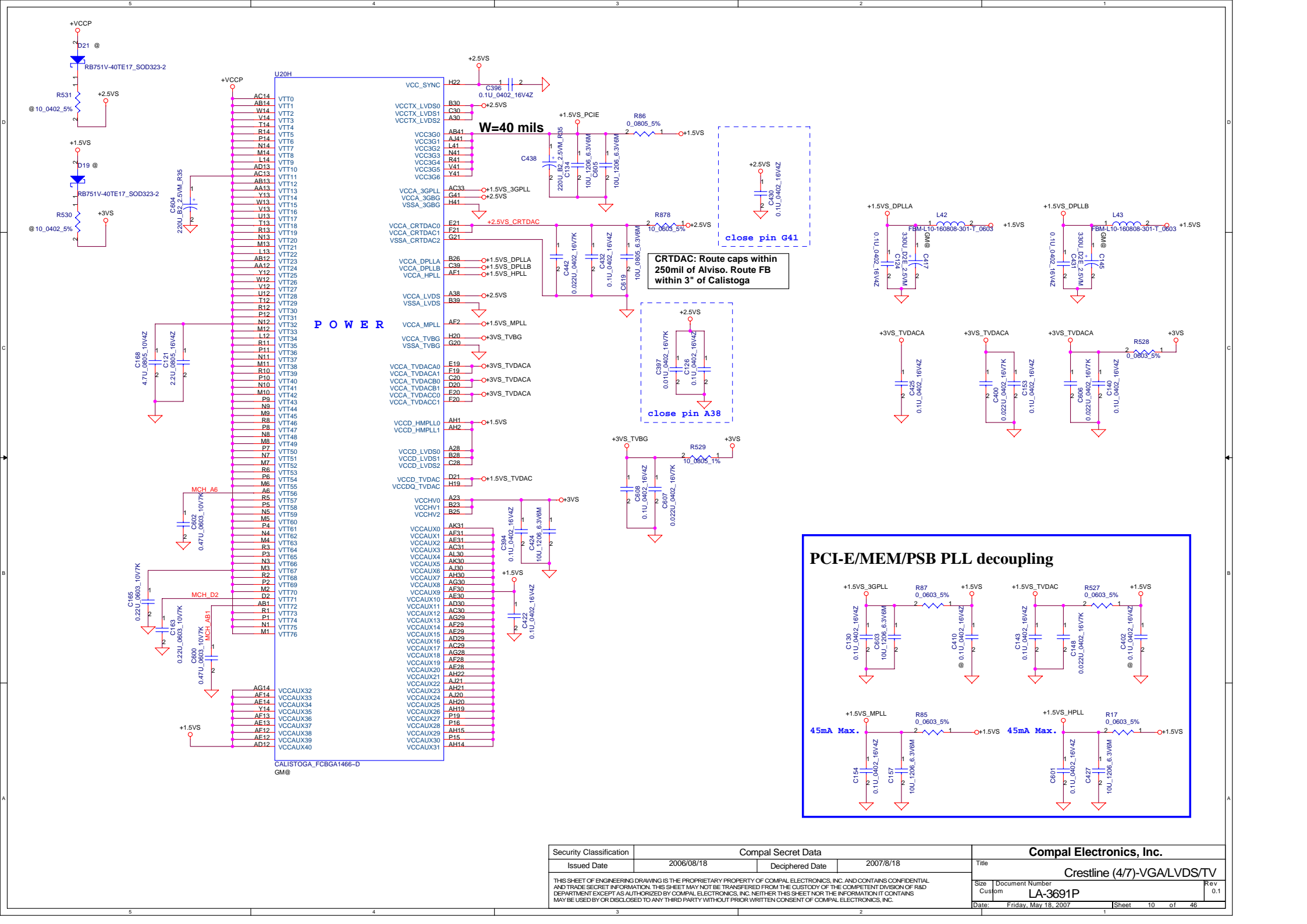




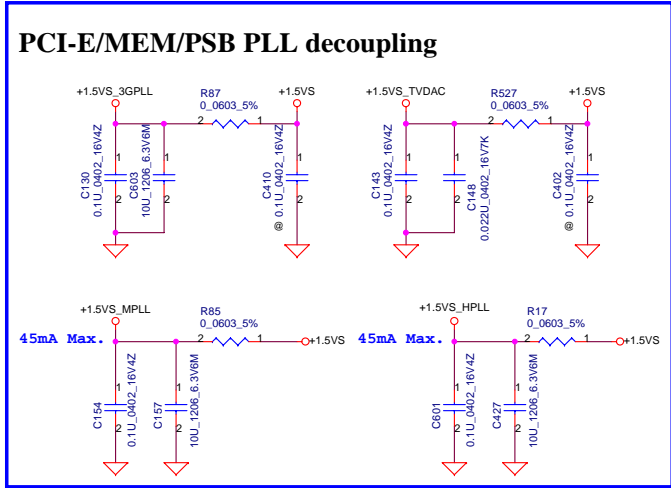
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EXP_TXN0	F36 PCIE MTX GRX N0	C175 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N0
EXP_TXN1	G40 PCIE MTX GRX N1	C404 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N1
EXP_TXN2	H36 PCIE MTX GRX N2	C144 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N2
EXP_TXN3	J40 PCIE MTX GRX N3	C408 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N3
EXP_TXN4	L36 PCIE MTX GRX N4	C142 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N4
EXP_TXN5	M40 PCIE MTX GRX N5	C411 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N5
EXP_TXN6	P40 PCIE MTX GRX N6	C423 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N6
EXP_TXN7	R36 PCIE MTX GRX N7	C172 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N7
EXP_TXN8	T40 PCIE MTX GRX N8	C465 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N8
EXP_TXN9	V36 PCIE MTX GRX N9	C162 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N9
EXP_TXN10	W40 PCIE MTX GRX N10	C441 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N10
EXP_TXN11	Y36 PCIE MTX GRX N11	C166 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N11
EXP_TXN12	AA40 PCIE MTX GRX N12	C440 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N12
EXP_TXN13	AB36 PCIE MTX GRX N13	C177 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N13
EXP_TXN14	AC40 PCIE MTX GRX N14	C448 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N14
EXP_TXN15	AD40 PCIE MTX GRX N15	C448 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_N15
EXP_TXP0	D36 PCIE MTX GRX P0	C133 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P0
EXP_TXP1	F40 PCIE MTX GRX P1	C407 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P1
EXP_TXP2	G36 PCIE MTX GRX P2	C129 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P2
EXP_TXP3	H40 PCIE MTX GRX P3	C406 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P3
EXP_TXP4	J36 PCIE MTX GRX P4	C178 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P4
EXP_TXP5	L40 PCIE MTX GRX P5	C405 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P5
EXP_TXP6	M36 PCIE MTX GRX P6	C167 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P6
EXP_TXP7	N40 PCIE MTX GRX P7	C419 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P7
EXP_TXP8	P36 PCIE MTX GRX P8	C161 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P8
EXP_TXP9	R40 PCIE MTX GRX P9	C426 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P9
EXP_TXP10	T36 PCIE MTX GRX P10	C155 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P10
EXP_TXP11	V40 PCIE MTX GRX P11	C429 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P11
EXP_TXP12	W36 PCIE MTX GRX P12	C173 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P12
EXP_TXP13	Y40 PCIE MTX GRX P13	C437 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P13
EXP_TXP14	AA36 PCIE MTX GRX P14	C170 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P14
EXP_TXP15	AB40 PCIE MTX GRX P15	C464 1	2 PM@ 0.1U 0402 10V7K	PCIE_MTX_C.GRX_P15

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GM@

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**POWER**



**CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga**

**close pin A38**

**close pin G41**

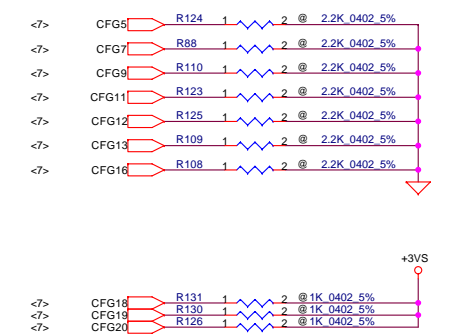
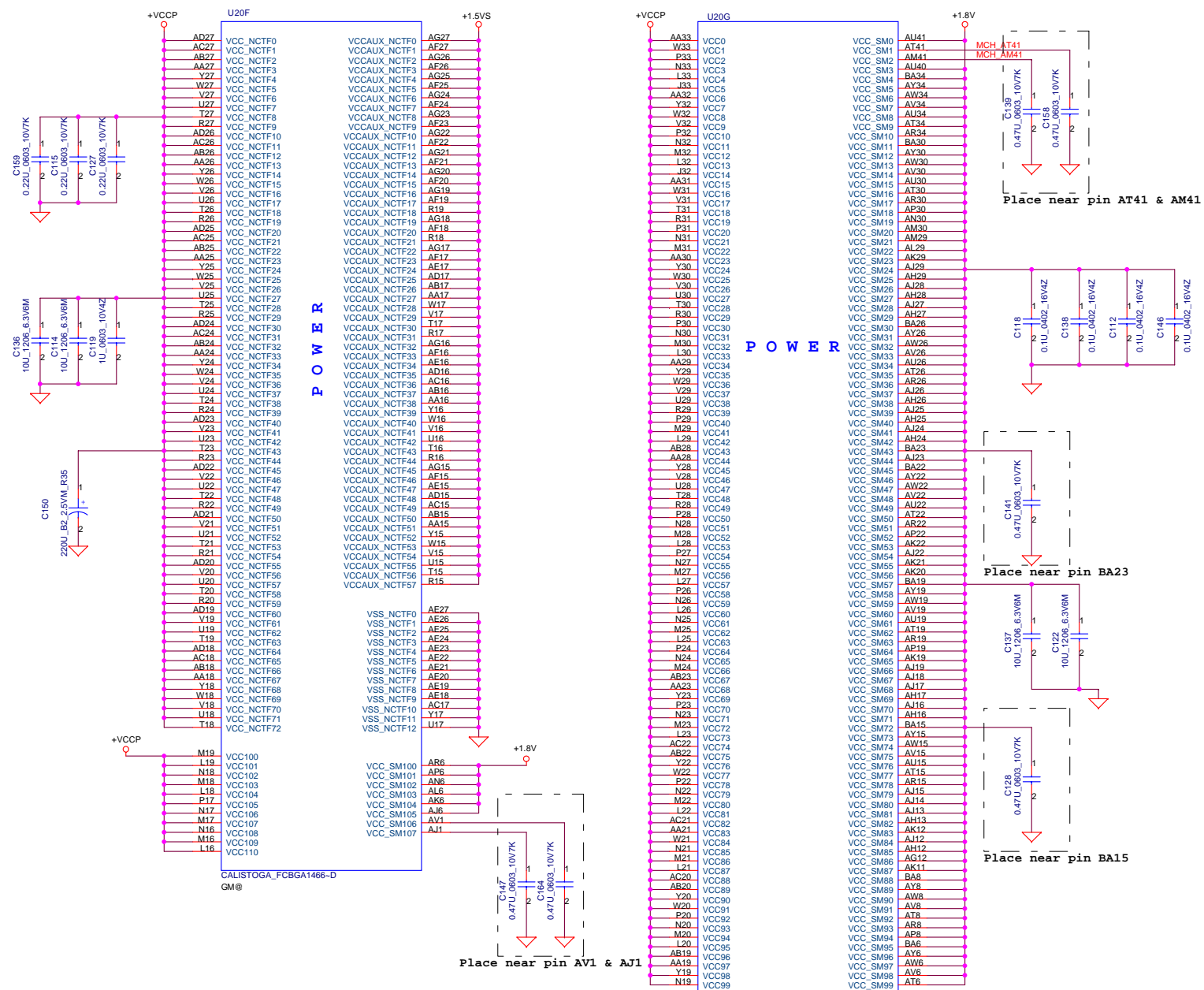
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# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

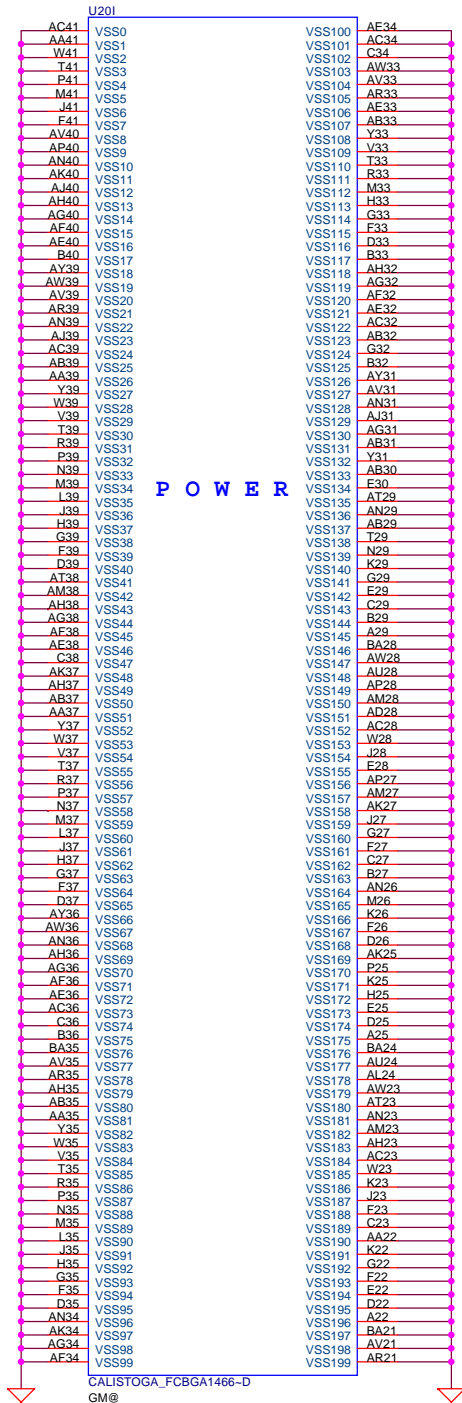
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved 1 = Calistoga *
PSB 4X CLK Enable	0 = Reserved 1 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.



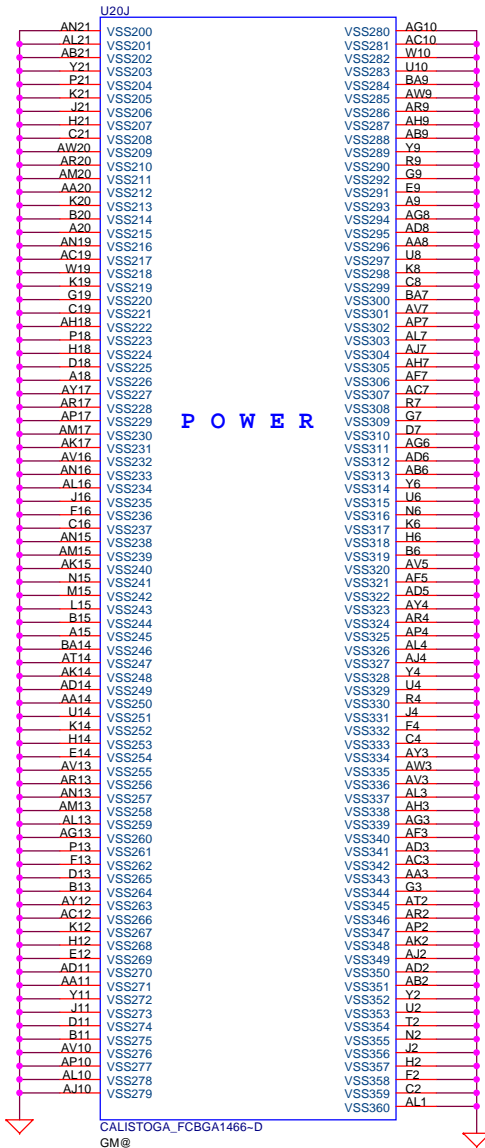
Security Classification	Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date
		2007/8/18

Title		Compal Electronics, Inc.	
		Crestline (5/7)-VCC	
Size	Document Number	Rev	
Custom	LA-3691P	0.1	

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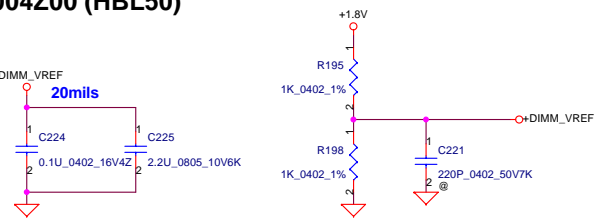
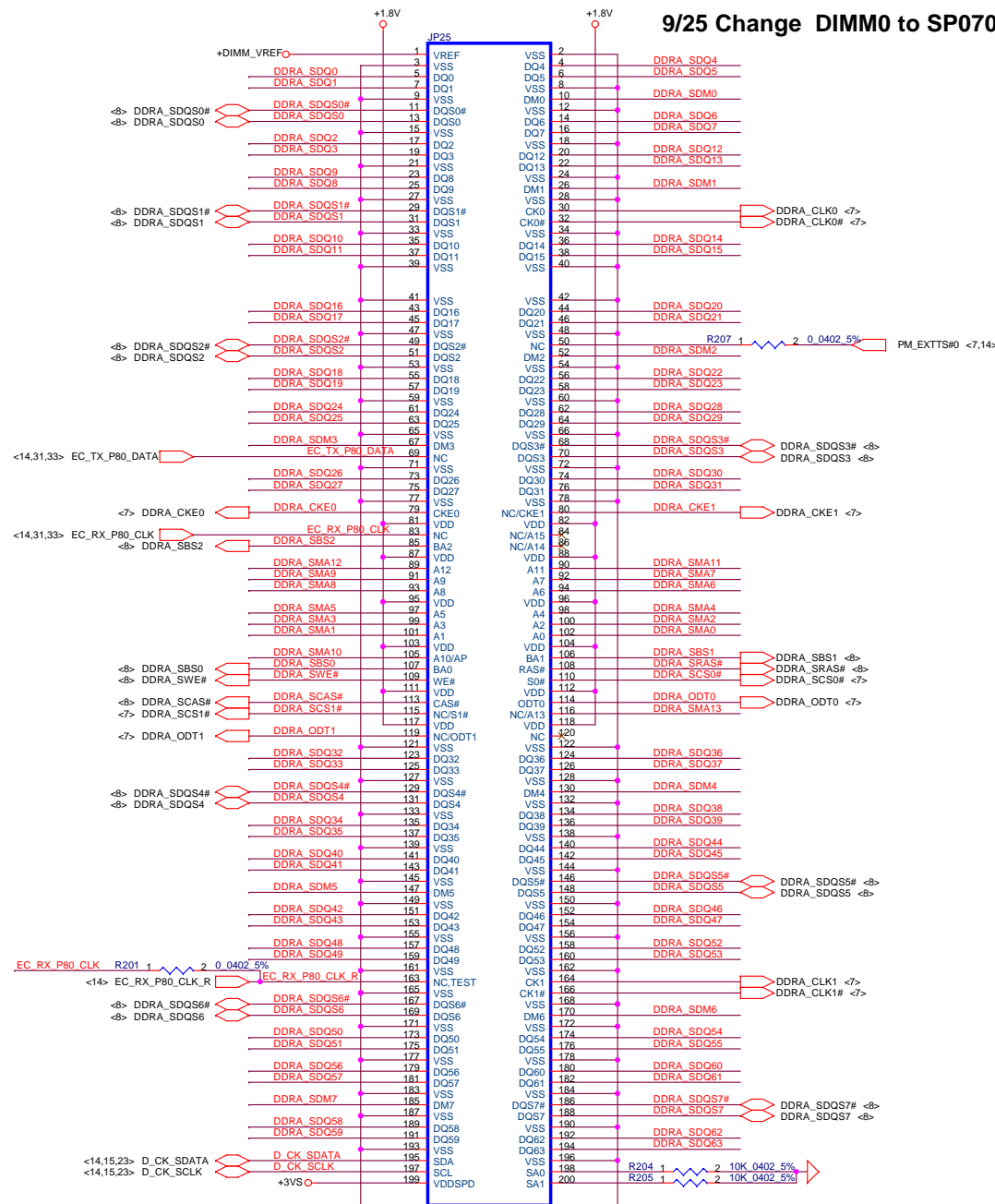
POWER



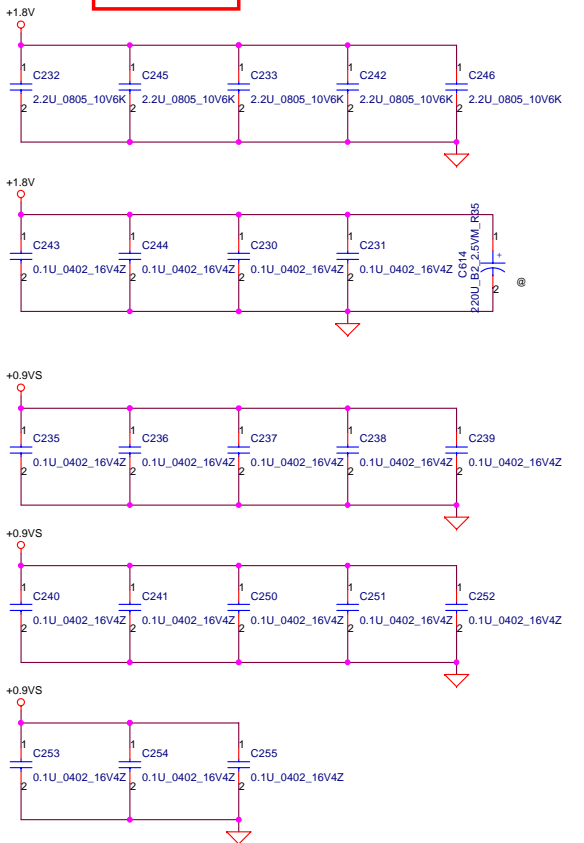
POWER

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number			Rev	
B	LA-3691P			0.1	
Date:	Friday, May 18, 2007	Sheet	12	of	46

### 9/25 Change DIMM0 to SP070004Z00 (HBL50)



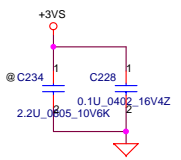
**Layout Note:**  
Place near JP35



**Layout Note:**  
Place these resistor closely JP35, all trace length Max=1.5"

**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

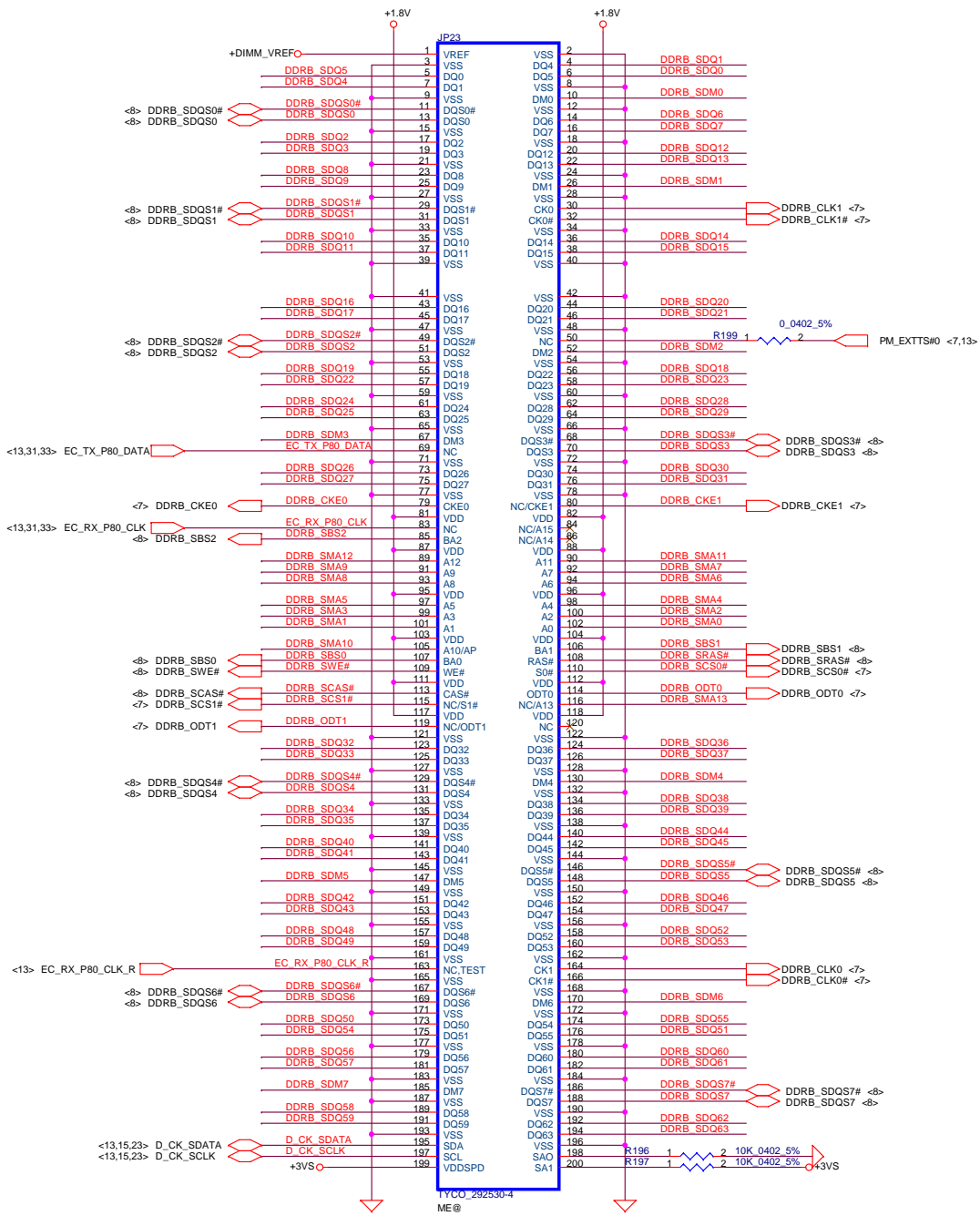
**DIMM0 STD H:5.2mm (BOT)**



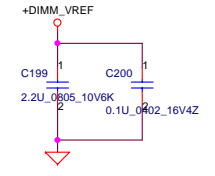
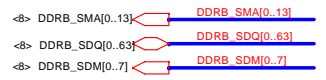
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	DDRII-SODIMM0	
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				Date: Friday, May 18, 2007	Rev 0.1
				Sheet 13	of 46

[netain@normal.com](mailto:netain@normal.com)

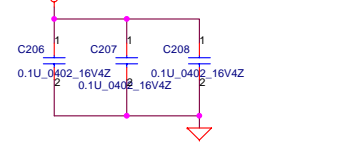
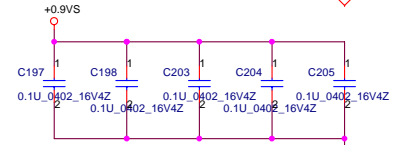
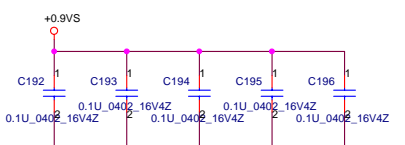
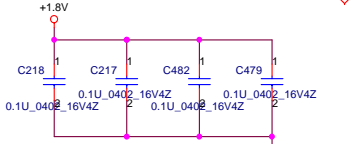
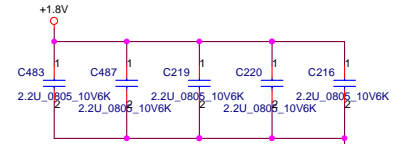
# 9/25 Change DIMM1 to SP070006F00



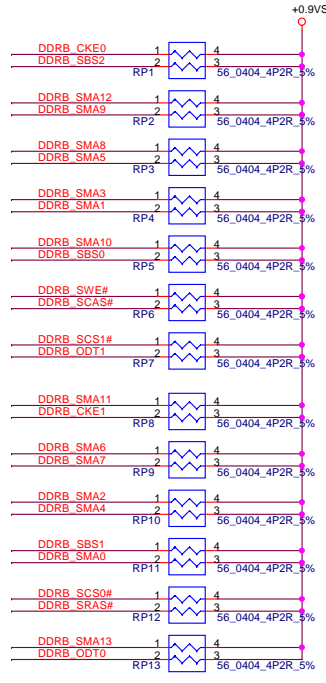
**DIMM1 STD H:9.2mm (BOT)**



**Layout Note:**  
Place near JP34



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP35, all trace length Max=1.5"

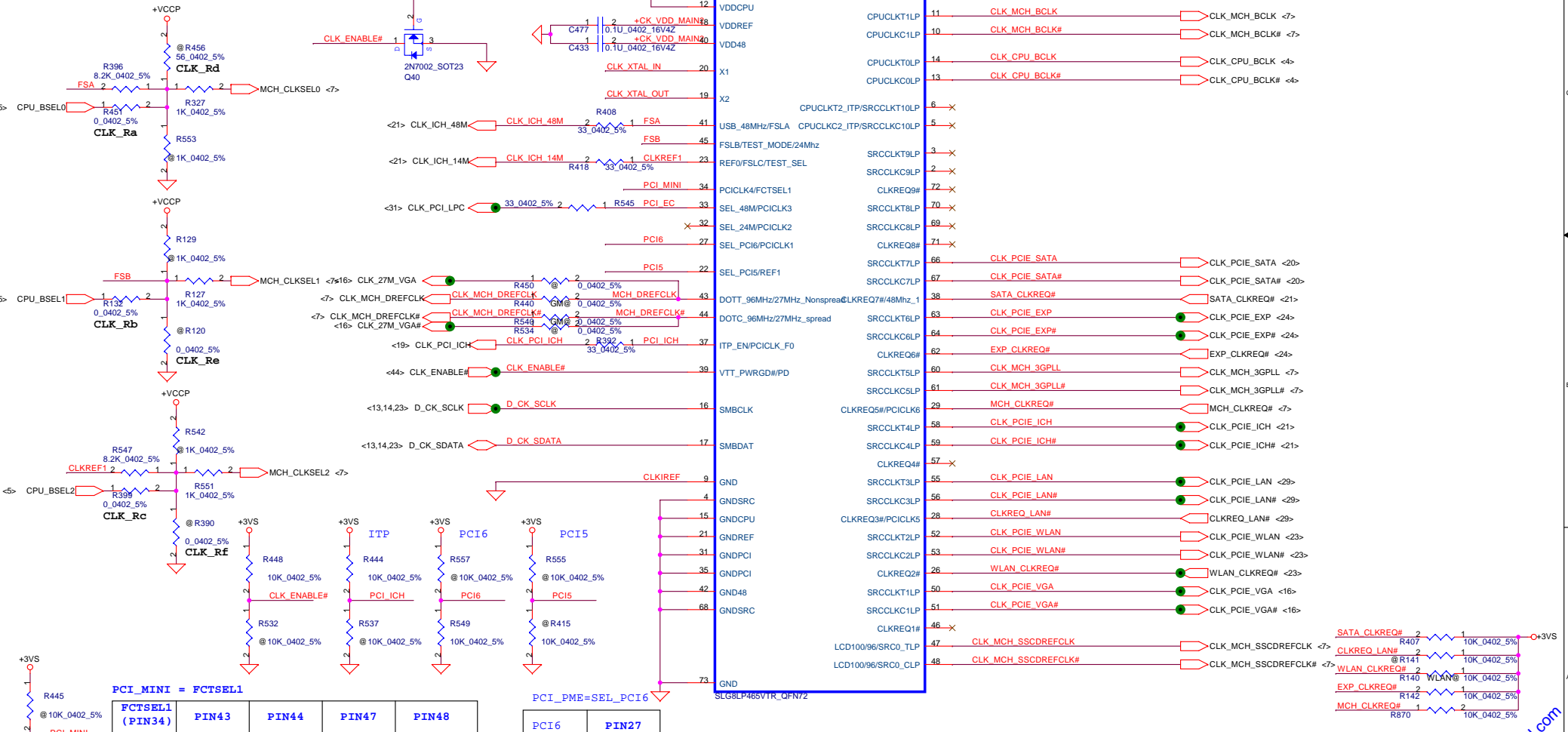
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
				DDR11-SODIMM1		
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				B	LA-3691P	0.1
				Date:	Friday, May 18, 2007	Sheet 14 of 46

FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

**FSB Frequency Selet:**

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
*(Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
533MHz	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	Stuff	CLK_Rd	CLK_Re	CLK_Rf



Place crystal within 500 mils of CK410

Place near U4

PCI\_MINI = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

PCI\_PME=SEL\_PCI6

PCI6	PIN27
0	CLKREQ5
1	PCICLK6

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		2006/10/06

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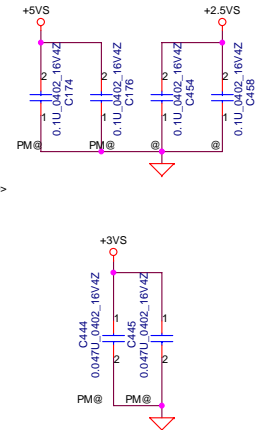
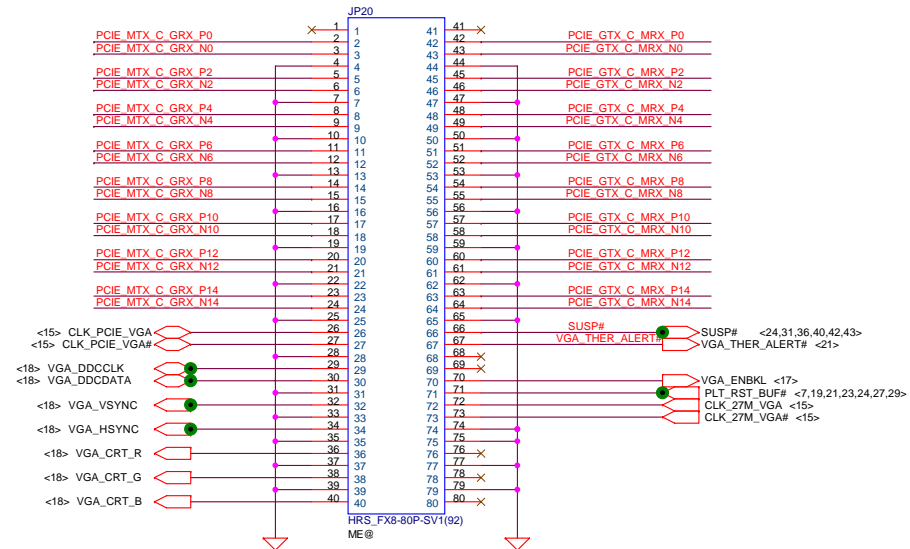
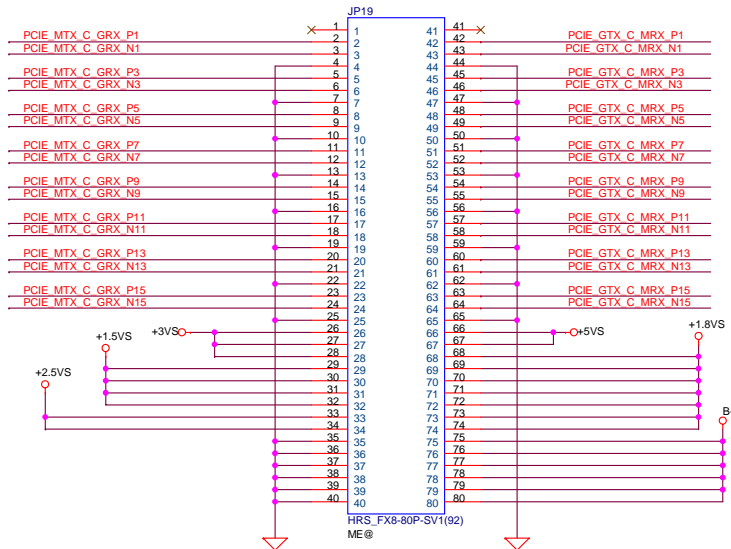
Title		
Compal Electronics, Inc.		
Clock generator		
Size	Document Number	Rev
	LA-3691P	0.1
Date:	Friday, May 18, 2007	Sheet 15 of 46

MAX. 4.06A @ 1.8V

MAX. 130mA @ 2.5V

MAX. 655mA @ 3.3V

- <-> PCIE\_MTX\_C\_GRX\_N[0..15] <-> PCIE\_MTX\_C\_GRX\_P0..15
- <-> PCIE\_MTX\_C\_GRX\_P[0..15] <-> PCIE\_MTX\_C\_GRX\_N0..15
- <-> PCIE\_GTX\_C\_MRX\_N[0..15] <-> PCIE\_GTX\_C\_MRX\_P0..15
- <-> PCIE\_GTX\_C\_MRX\_P[0..15] <-> PCIE\_GTX\_C\_MRX\_N0..15

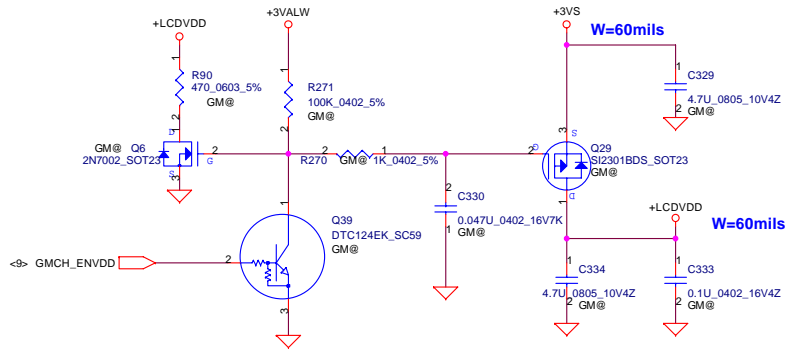


<b>Compal Electronics, Inc.</b>		
<b>VGA/B connector</b>		
Title	Document Number	Rev
	IEL10 LA-3451P	0.2
Date:	Friday, May 18, 2007	Sheet 16 of 46

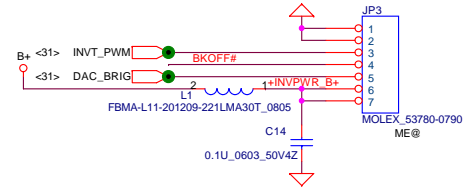
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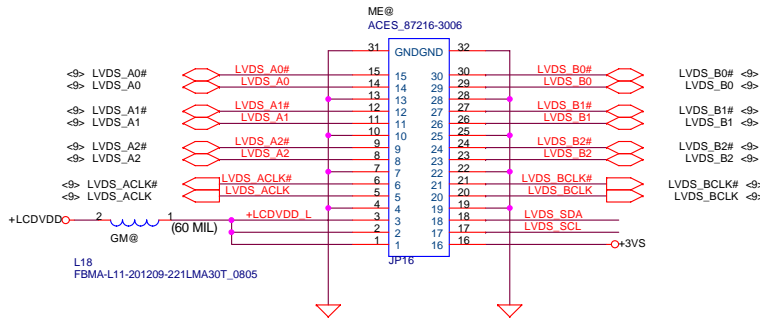
### LCD POWER CIRCUIT



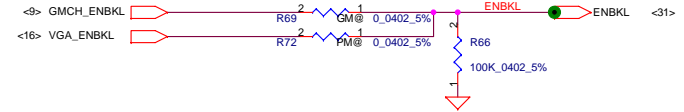
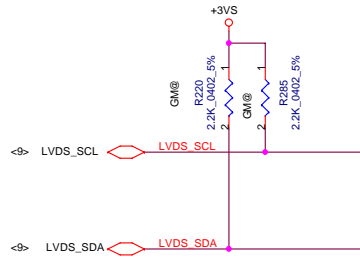
### INVERTER Conn.



### LCD/PANEL BD. Conn.



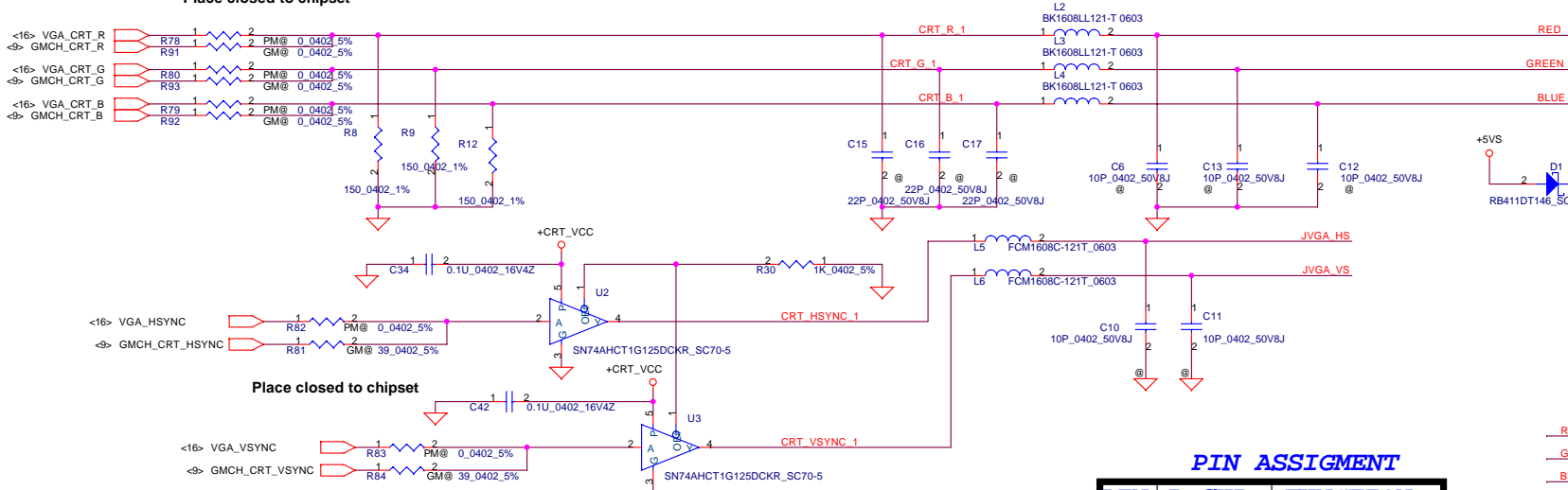
Follow HEL80's pin definition  
Except pin 29



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				LVDS & DVI Connector	
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			Sheet 17	of 46	

# CRT Connector

Place closed to chipset

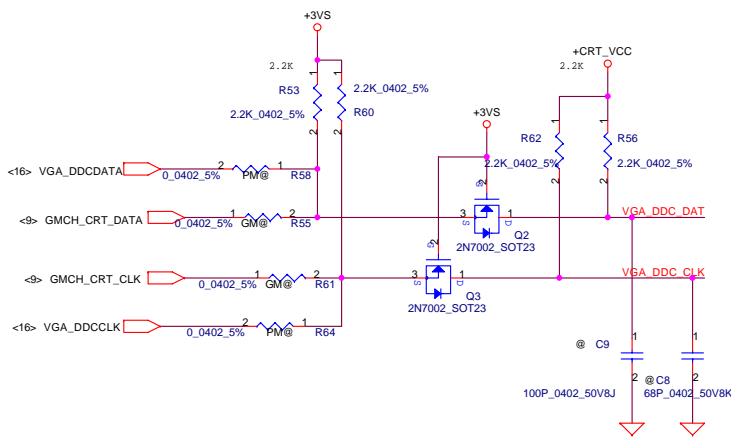
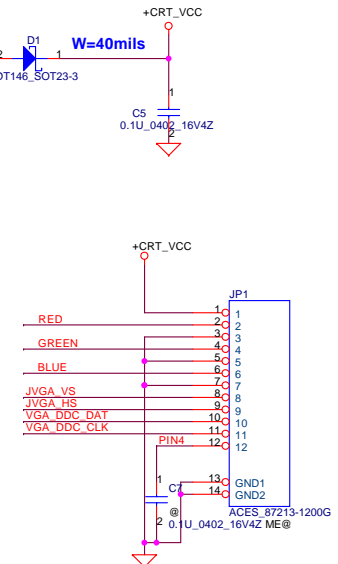


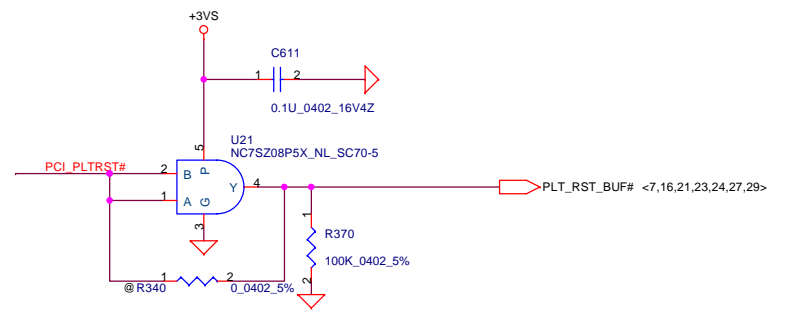
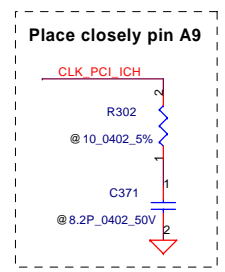
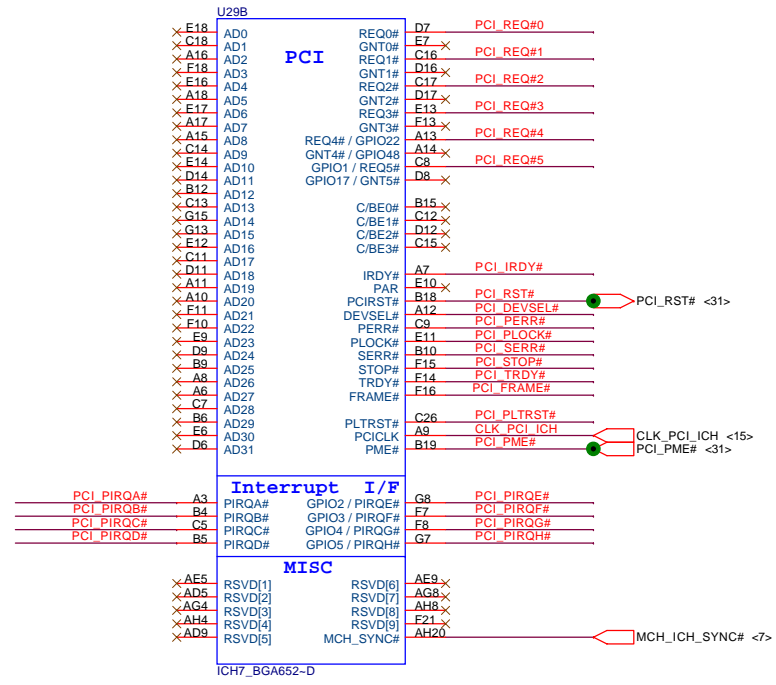
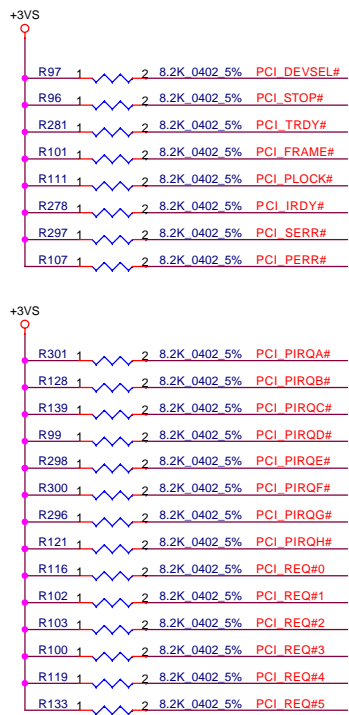
Place closed to chipset

Update Footprint

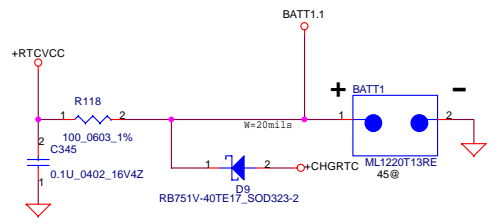
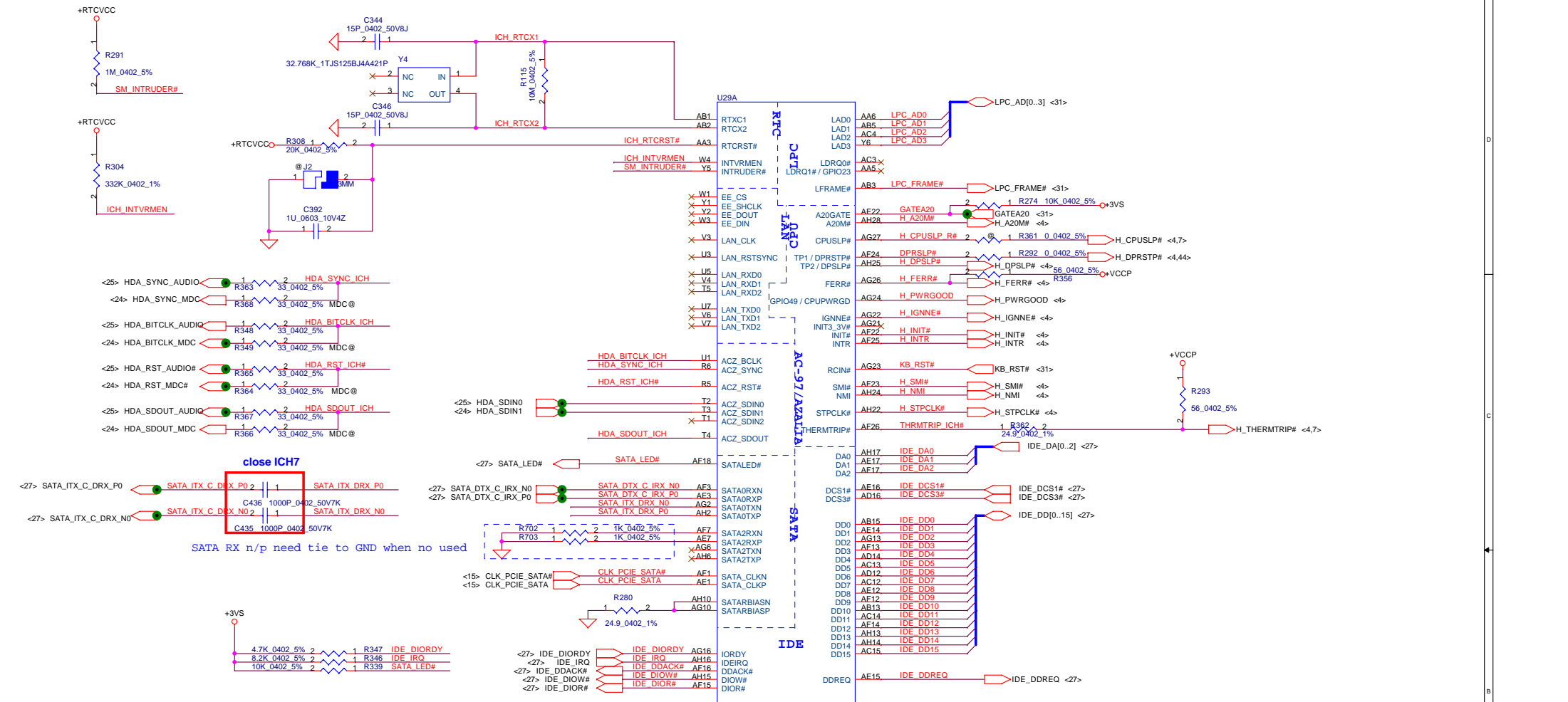
## PIN ASSIGNMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
9	10	GND
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
	5	GND
	4	

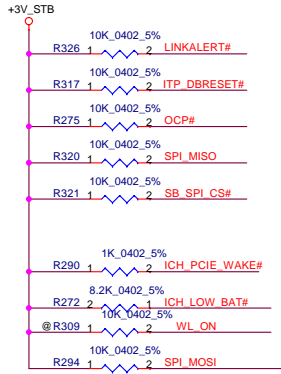
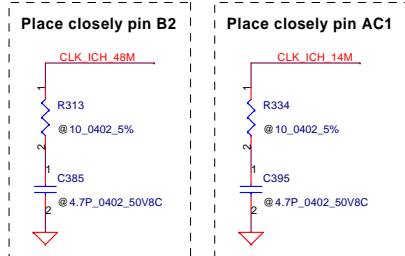
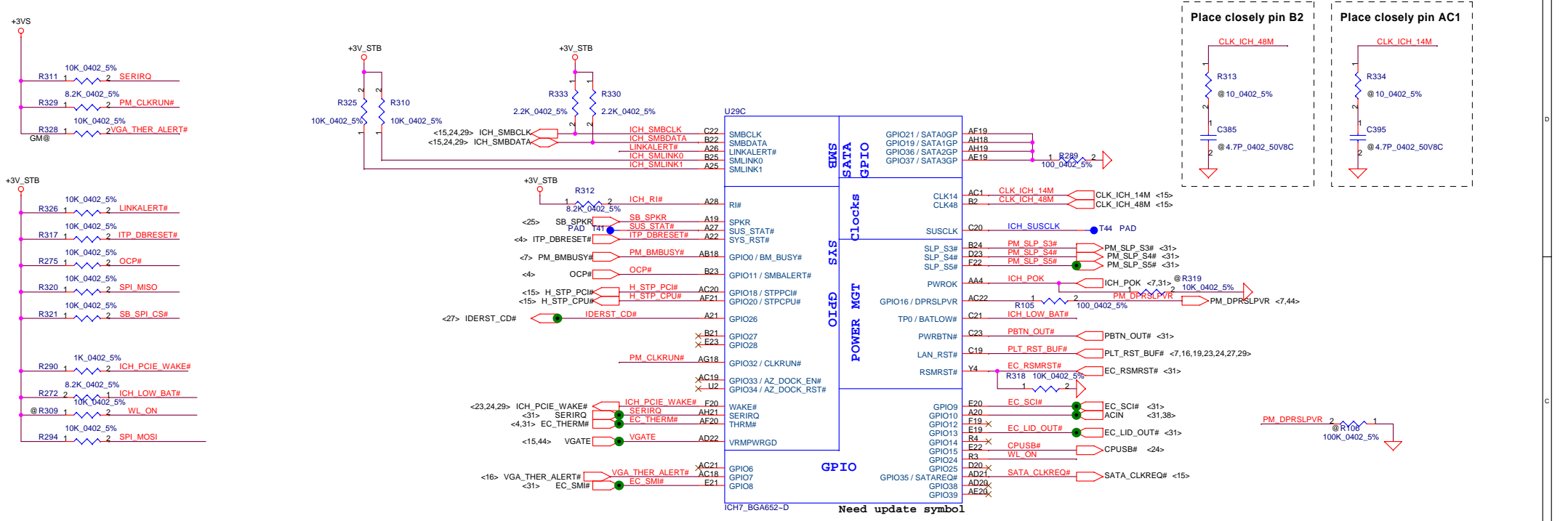




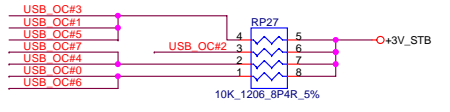
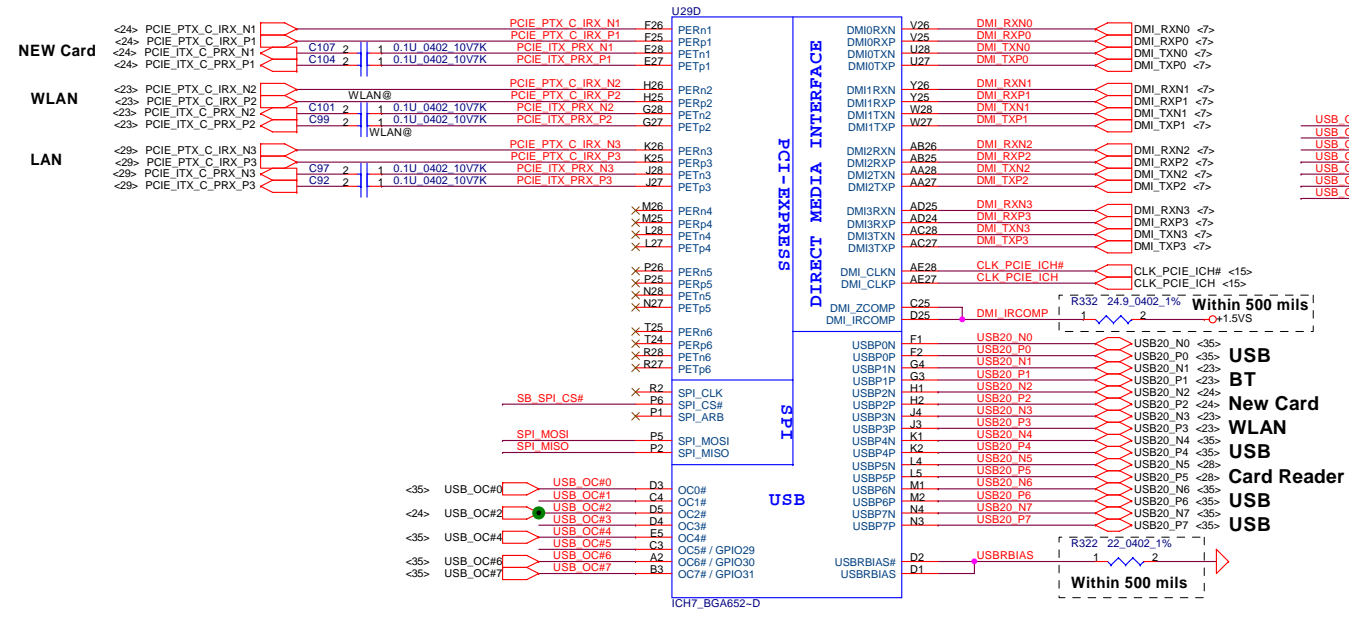
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		0.1	
Date:	Friday, May 18, 2007	Sheet	19	of	46



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	ICH8M(2/4)-LAN, IDELPC, RTC	
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				Custom	LA-3691P
				Date:	Friday, May 18, 2007
				Sheet	20 of 46
				Rev	0.1



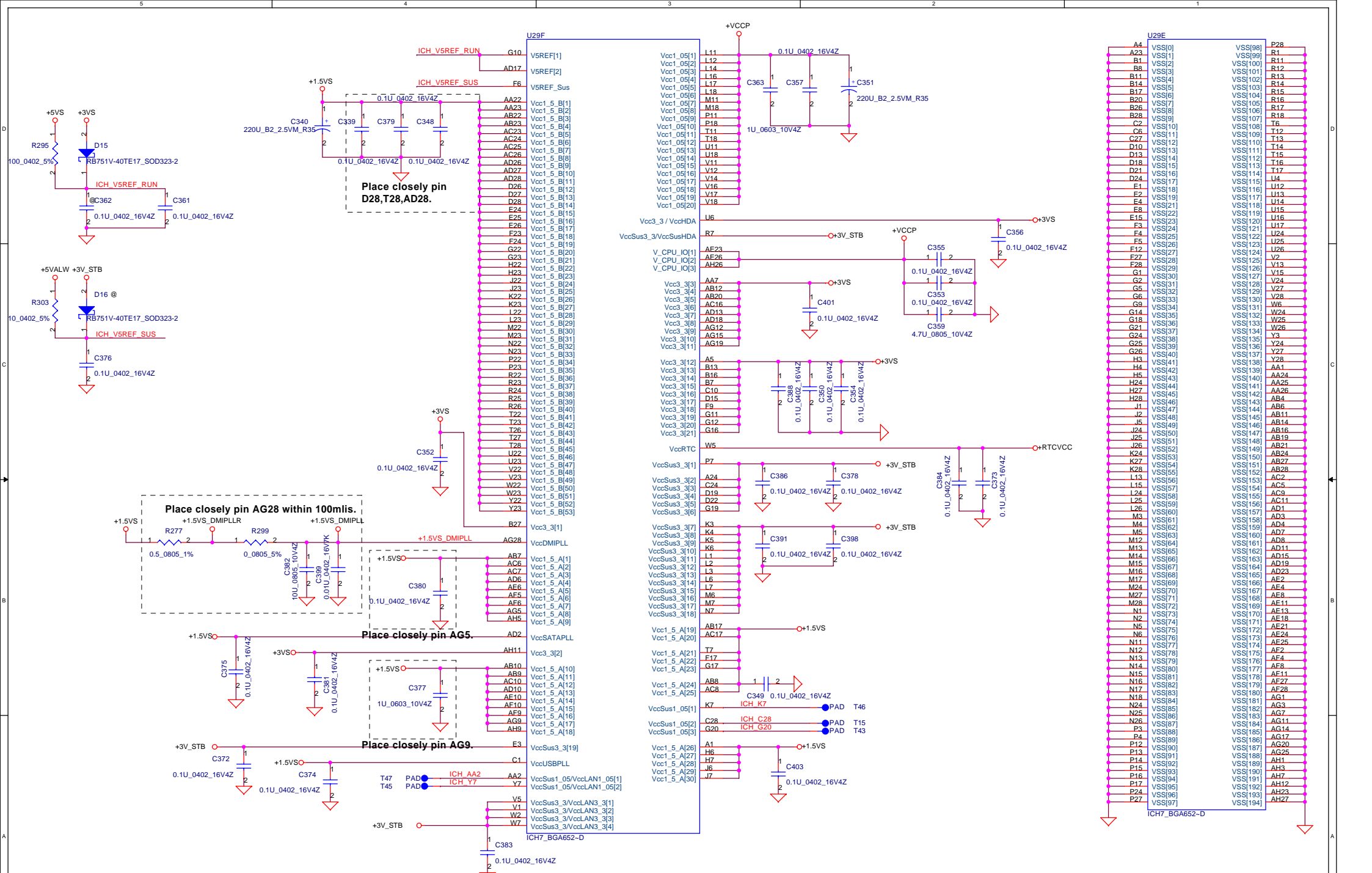
Need update symbol



Within 500 mils

Within 500 mils

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<p>IC7_BGA652-D</p>			<p><b>Compal Electronics Inc.</b></p> <p>ICH8M(3/4)-USB,GPIO,PCI-E</p>	
Size	Document Number	Rev		
Customer	LA-3691P	0.1		
Date	Friday, May 18, 2007	Sheet	21	of 46

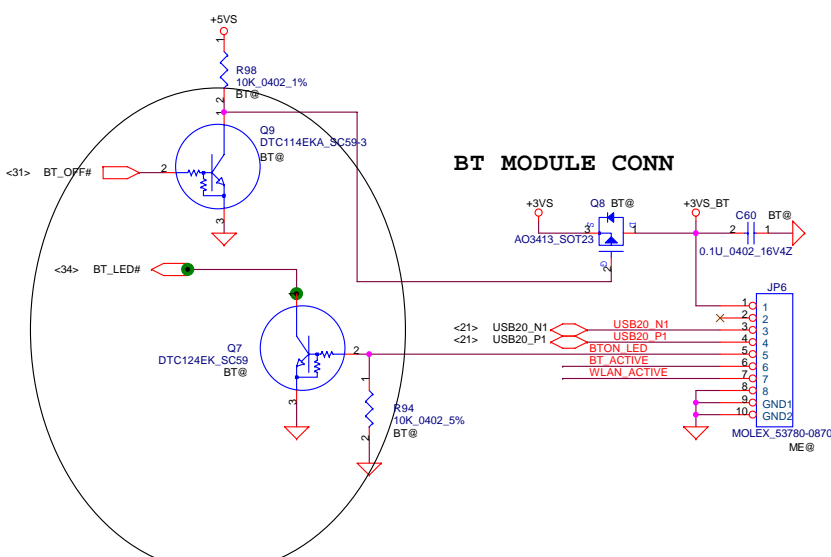
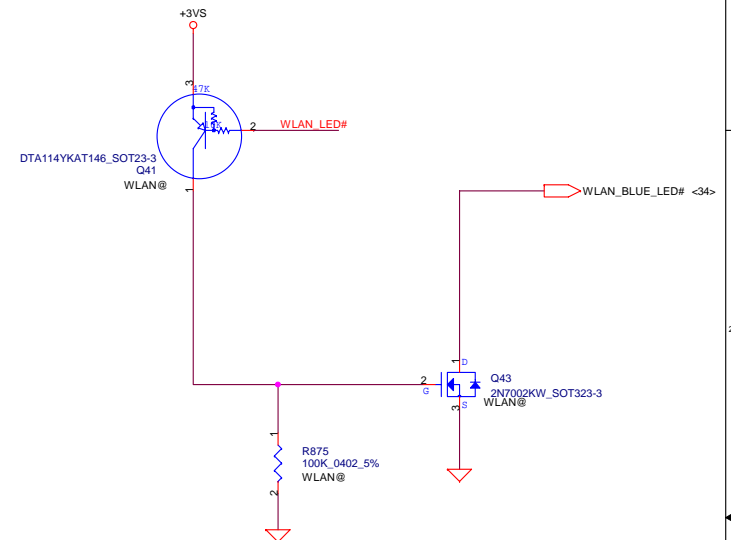
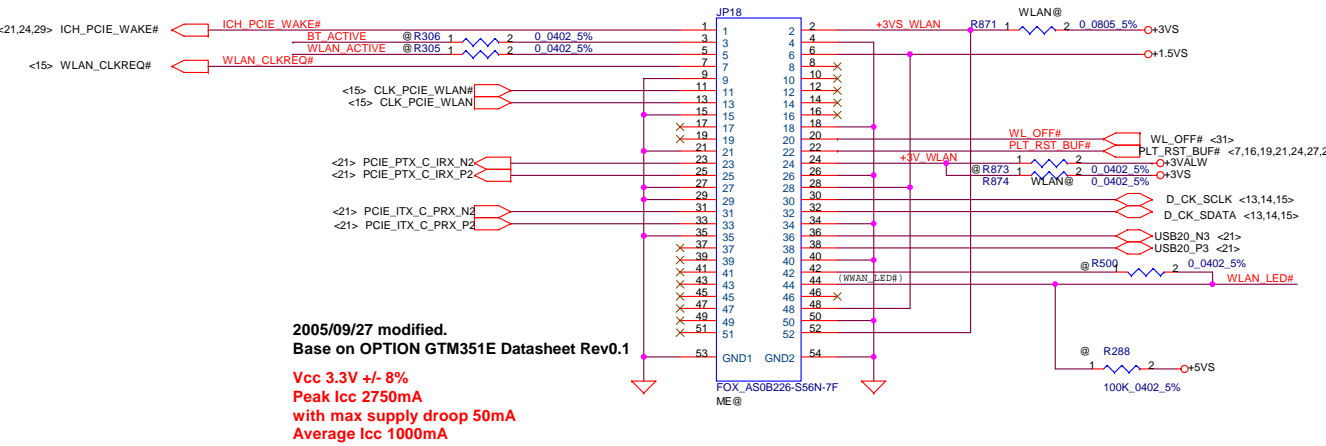
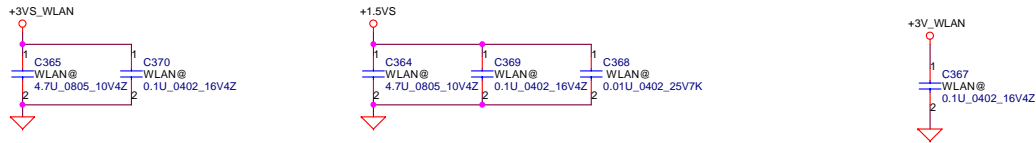


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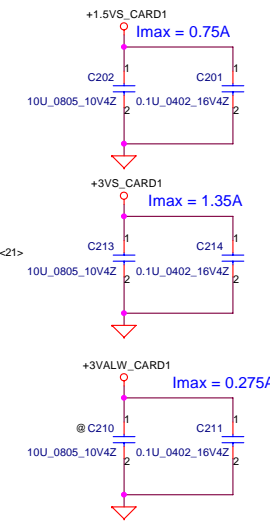
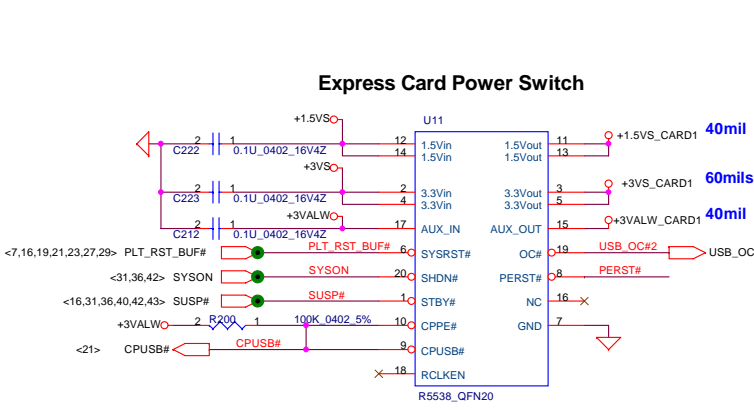
Compal Electronics, Inc.			
Title IFTXX MB LA-3541P Schematic			
Size	Document Number	Rev	
Customer	LA-3691P	0.1	
Date:	Friday, May 18, 2007	Sheet	22 of 46

# Mini-Express Card for 3G Or TV Tuner

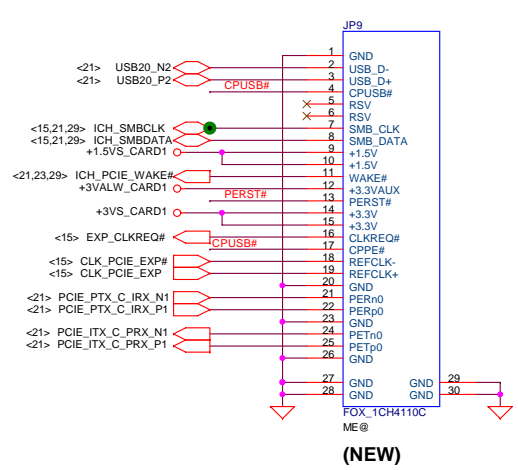
## Mini-Express Card for WLAN



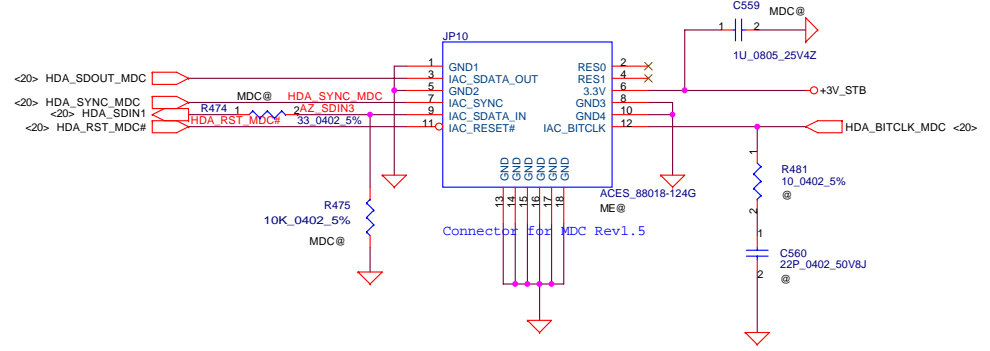
Security Classification	Compal Secret Data			Title		
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/3G/FeliCa/FP		
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				LA-3691P		0.1
Date:	Friday, May 18, 2007	Sheet	23	of	46	



### New Card Socket (Left/TOP)



### MDC CONN.



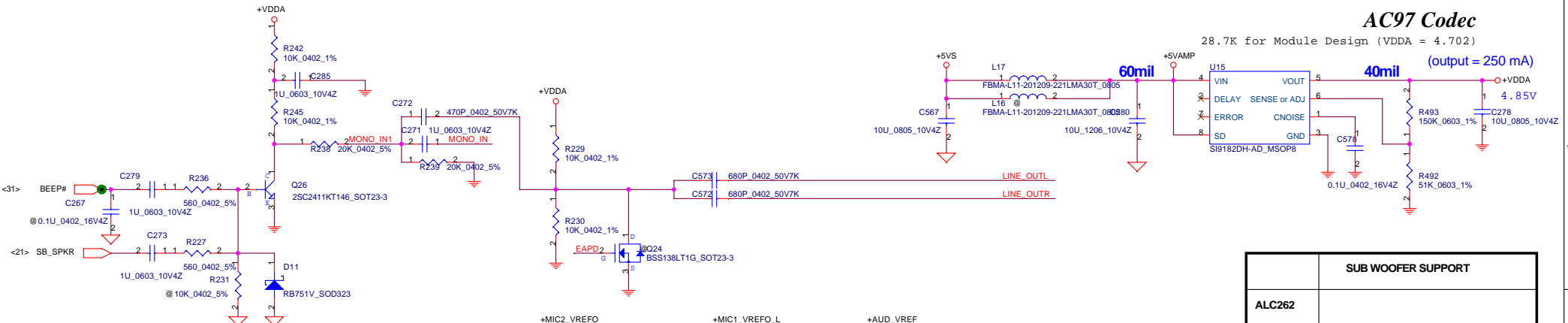
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	NEW CARD & USB Connector
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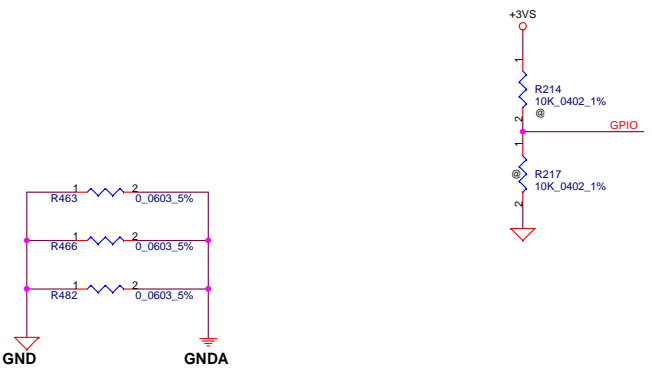
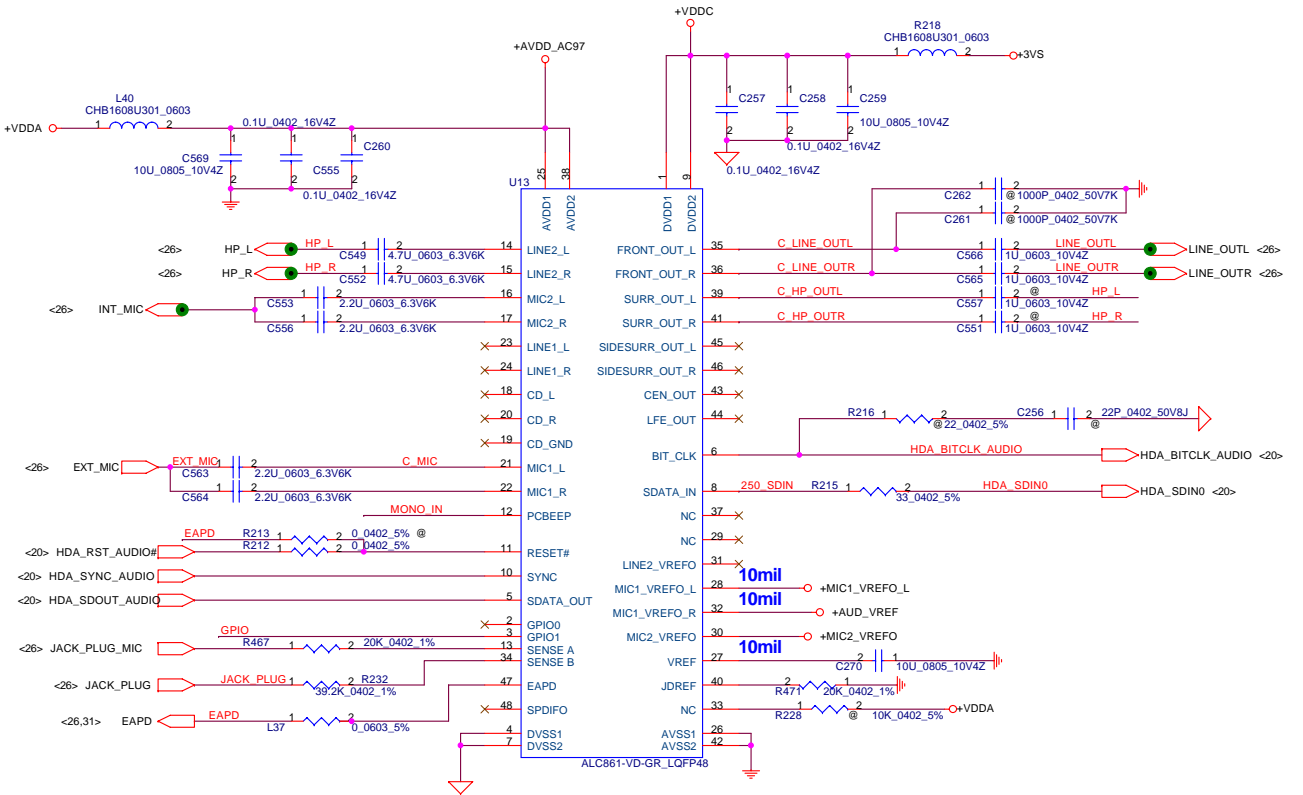
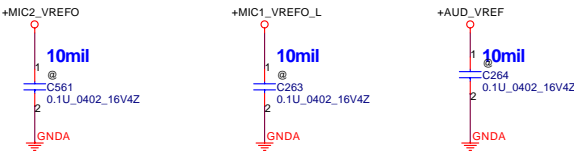
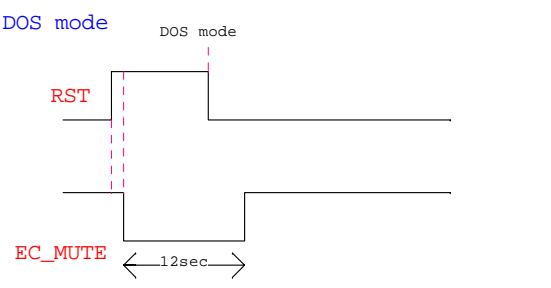
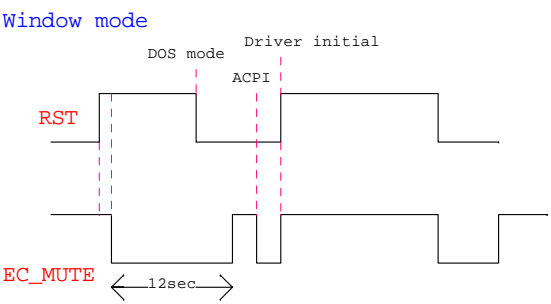
# AC97 Codec

28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)



SUB WOOFER SUPPORT	
ALC262	
ALC861D	



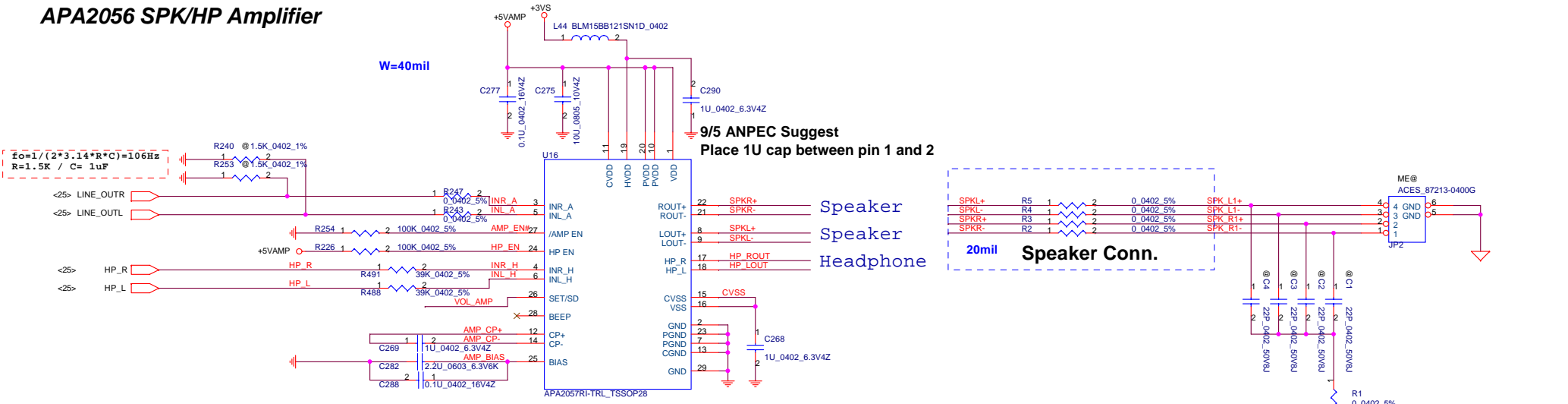
Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date
		2006/10/06

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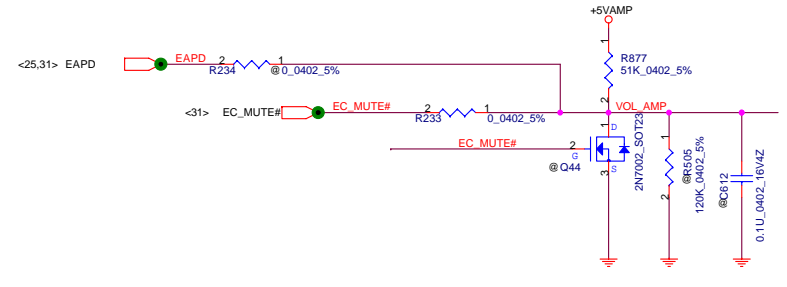
Compal Electronics, Inc.		
Title	ALC861 VD Codec	
Size	Document Number	Rev
Custom	IEL10 LA-3451P	0.2
Date:	Friday, May 18, 2007	Sheet 25 of 46

Review@hotmail.com

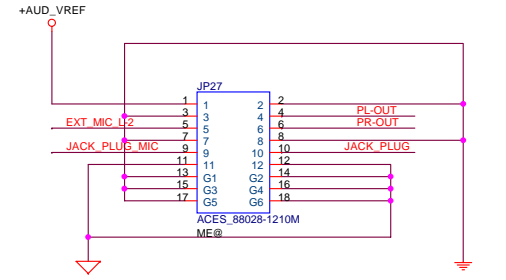
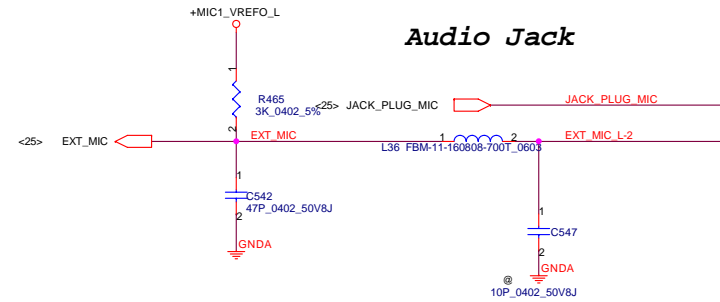
# APA2056 SPK/HP Amplifier



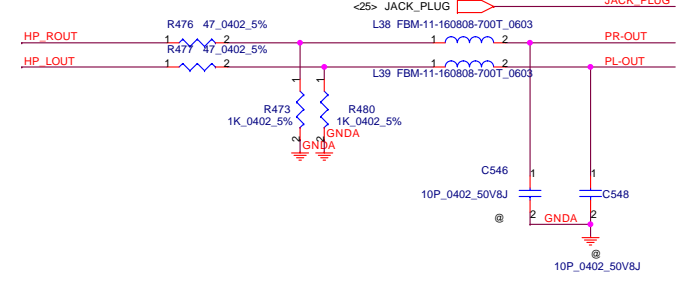
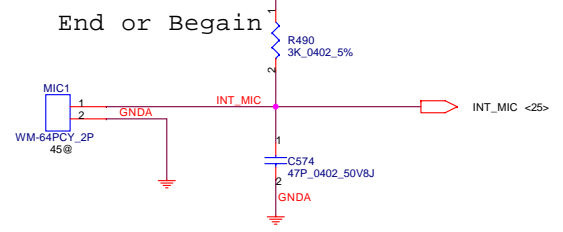
**IN\_A Gain = 10dB (Internal Speaker)**  
**IN\_H Gain = 0dB (Headphone)**



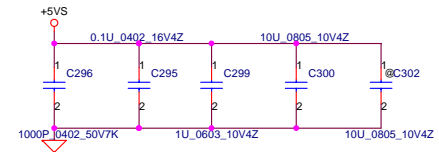
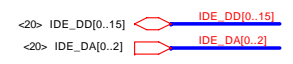
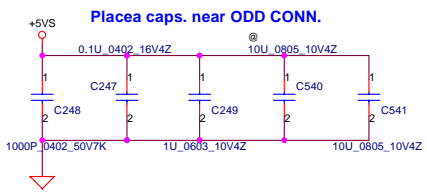
**EXT MIC**



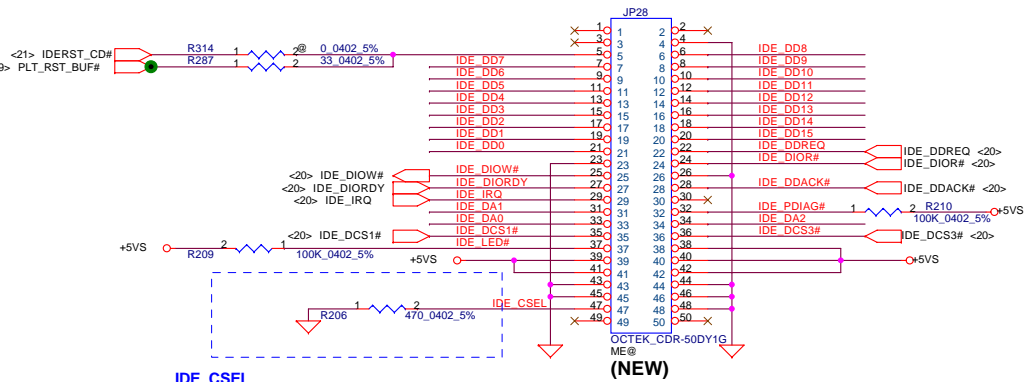
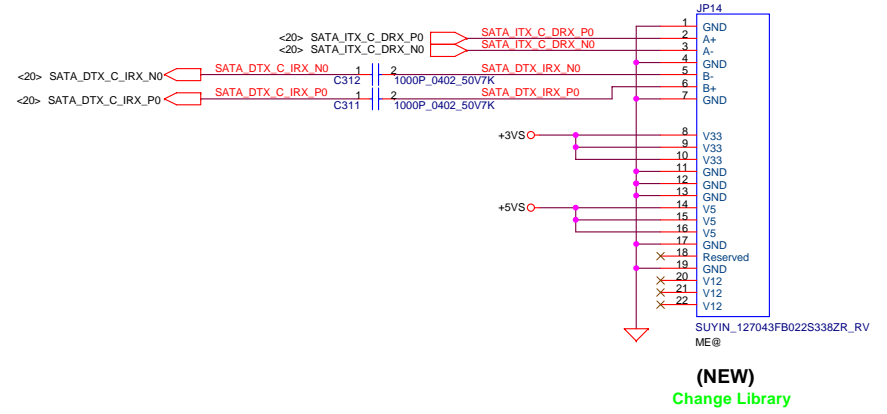
**INT MIC**



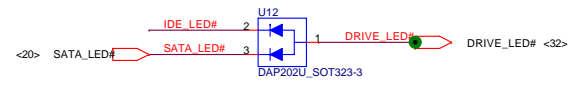
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	AMP/V/R/Audio Jack/MIC	
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Size	Document Number	Rev		Date	
Custom	LA-3691P	0.1		Monday, May 21, 2007	
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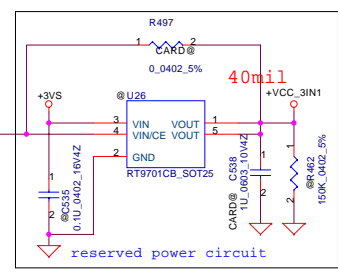
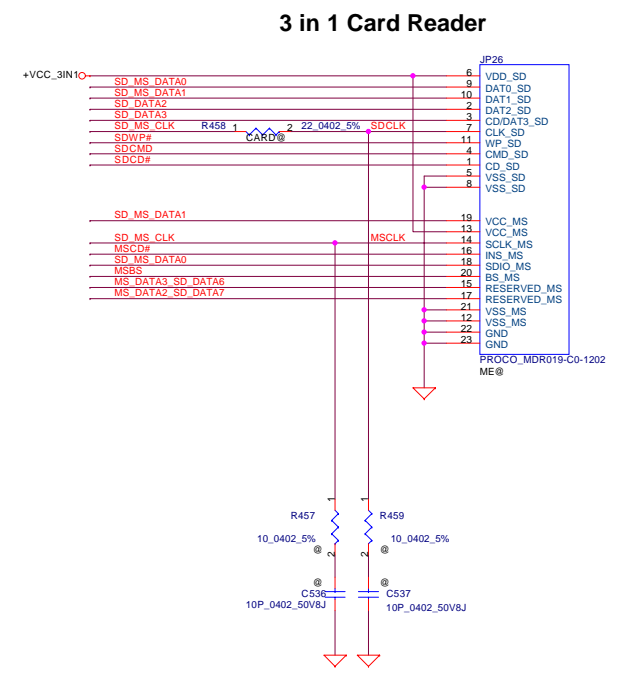
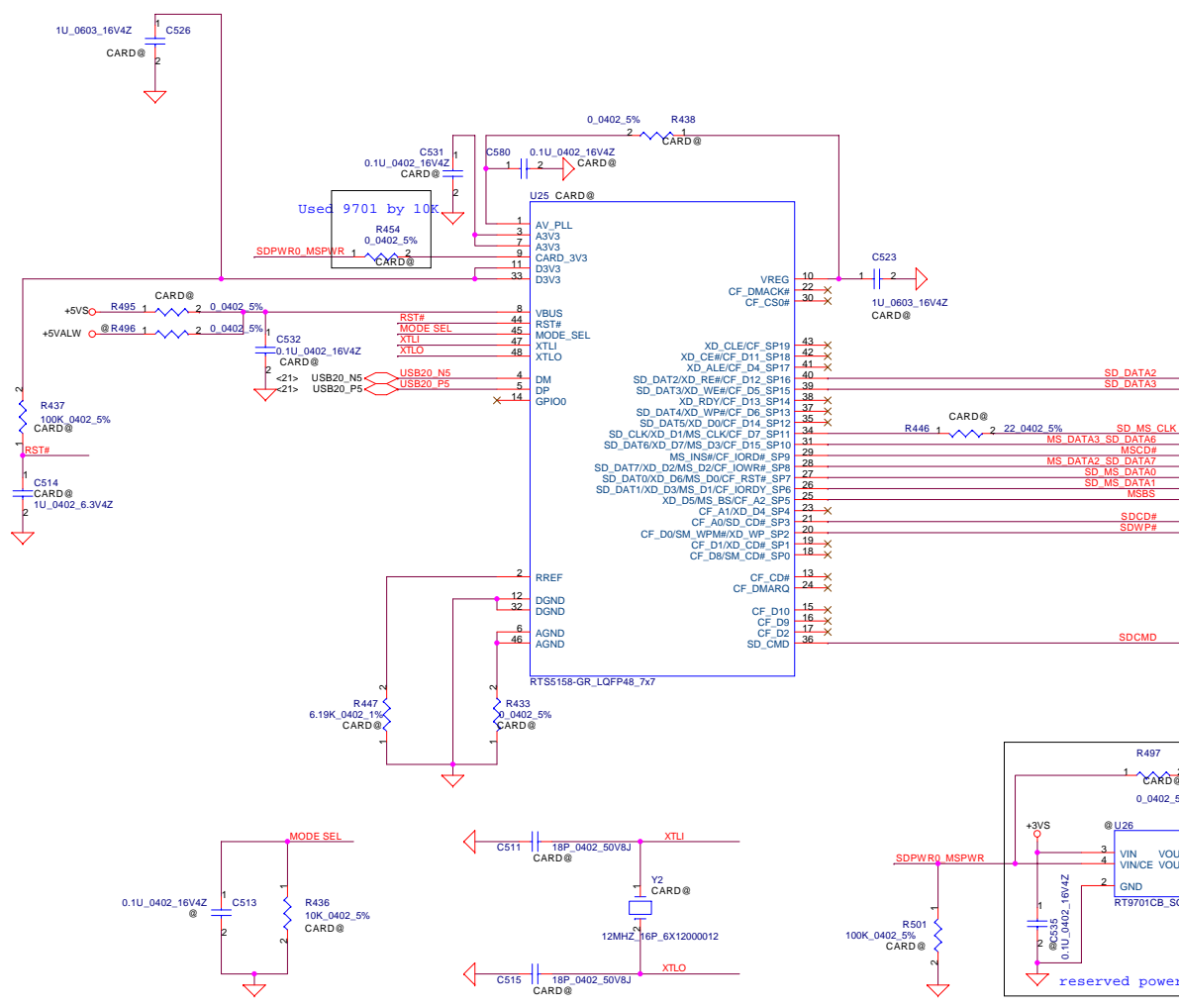
**SATA HDD Conn.**



**IDE\_CSEL**  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)



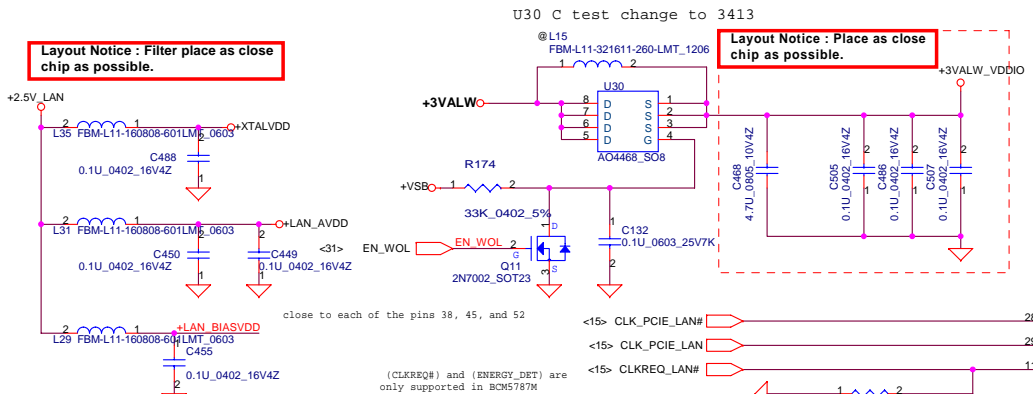
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	HDD & ODD Connector
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**3 in 1 Card Reader**

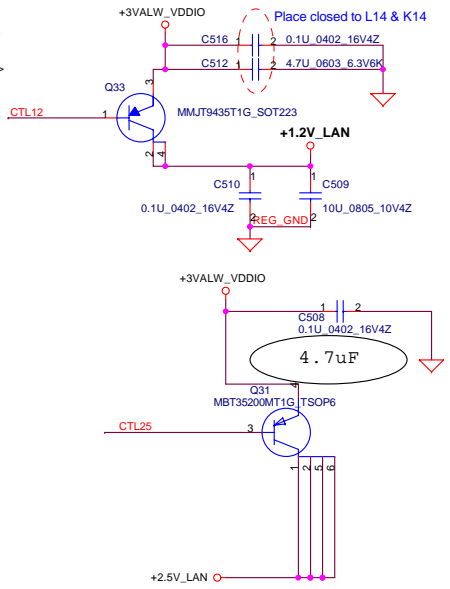
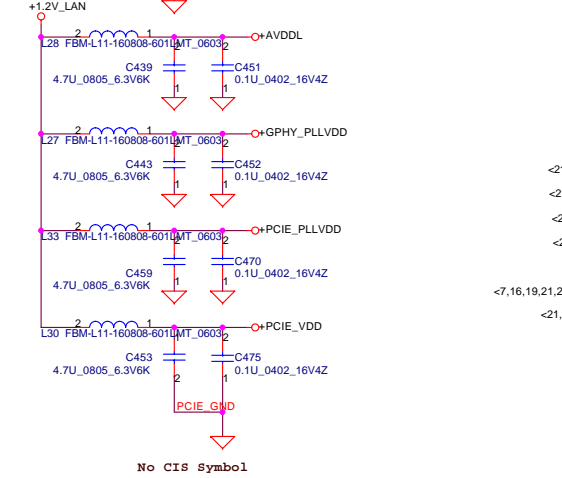
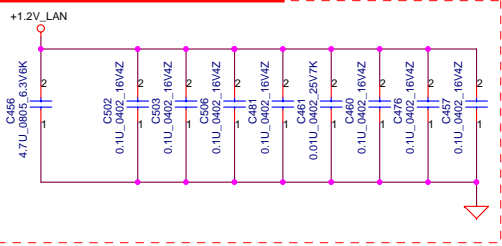
Security Classification	Compal Secret Data		Title		<b>Compal Electronics, Inc.</b> <b>1394+3 in 1 Card</b>
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Size	
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Date: Friday, May 18, 2007					Rev 0.1
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Layout Notice : Filter place as close chip as possible.



Layout Notice : Place as close chip as possible.

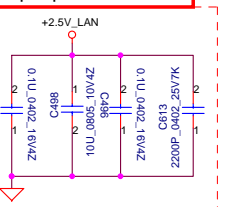
Layout Notice : 1.2V filter. Place as close chip as possible.



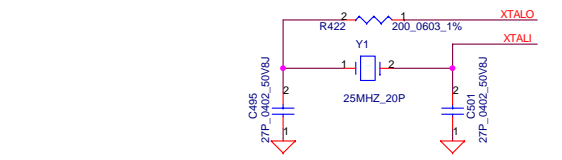
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

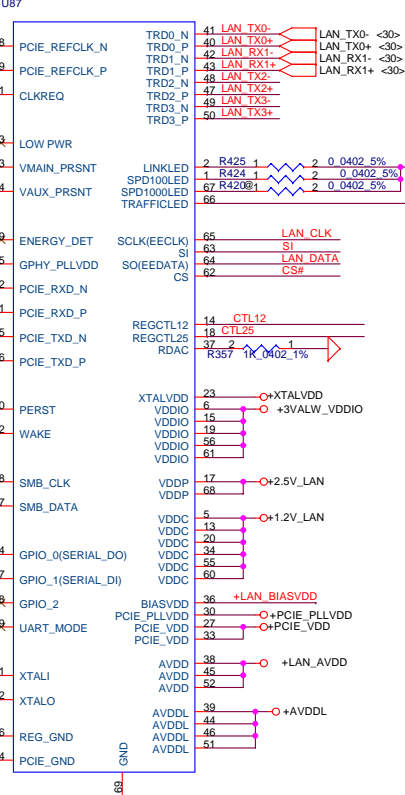
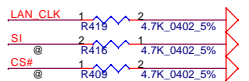
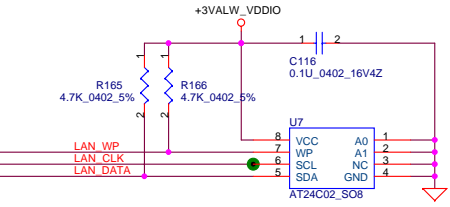


Close to U87



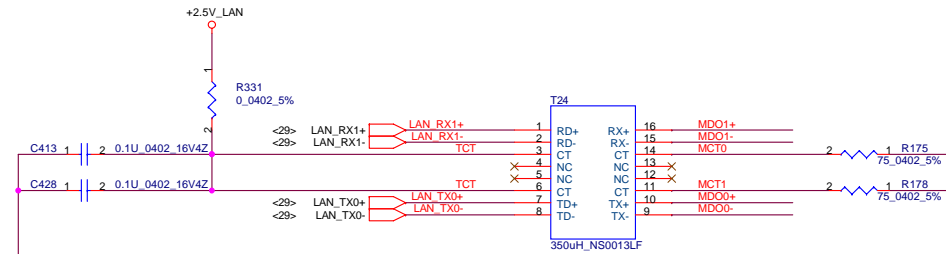
Pin16 connect to C1206 Pin1

Pin 24 connect to C1339 Pin1



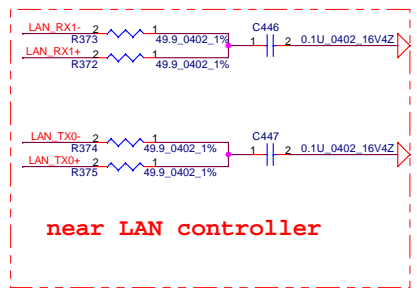
Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date
		2006/10/06
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Compal Electronics, Inc.			
Title: BCM5787M-GLAN			
Size	Document Number	Rev	
Customer	IEL20 LA-3471P	0.1	
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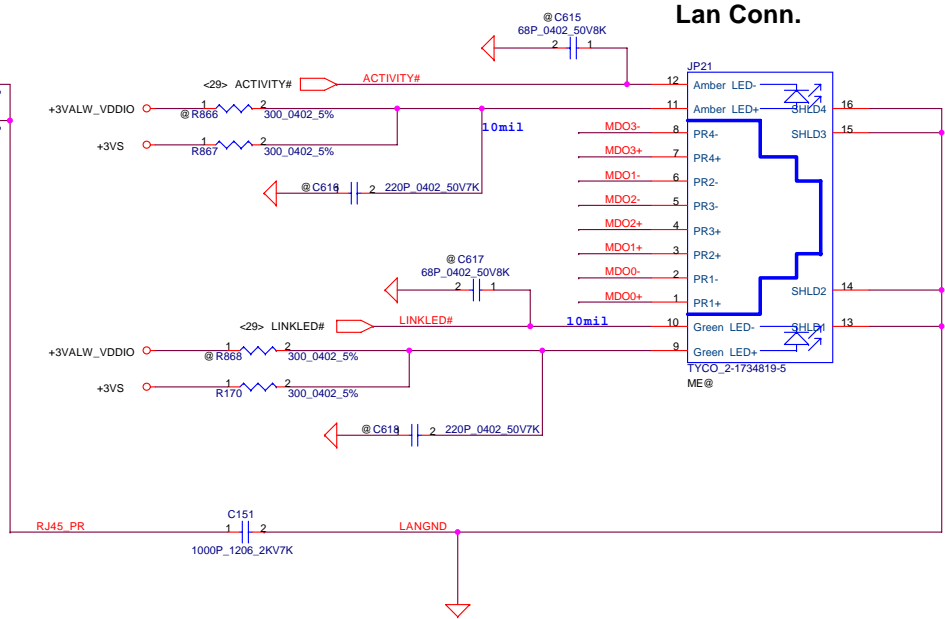


Change T1 from SP050001210 to SP050001210

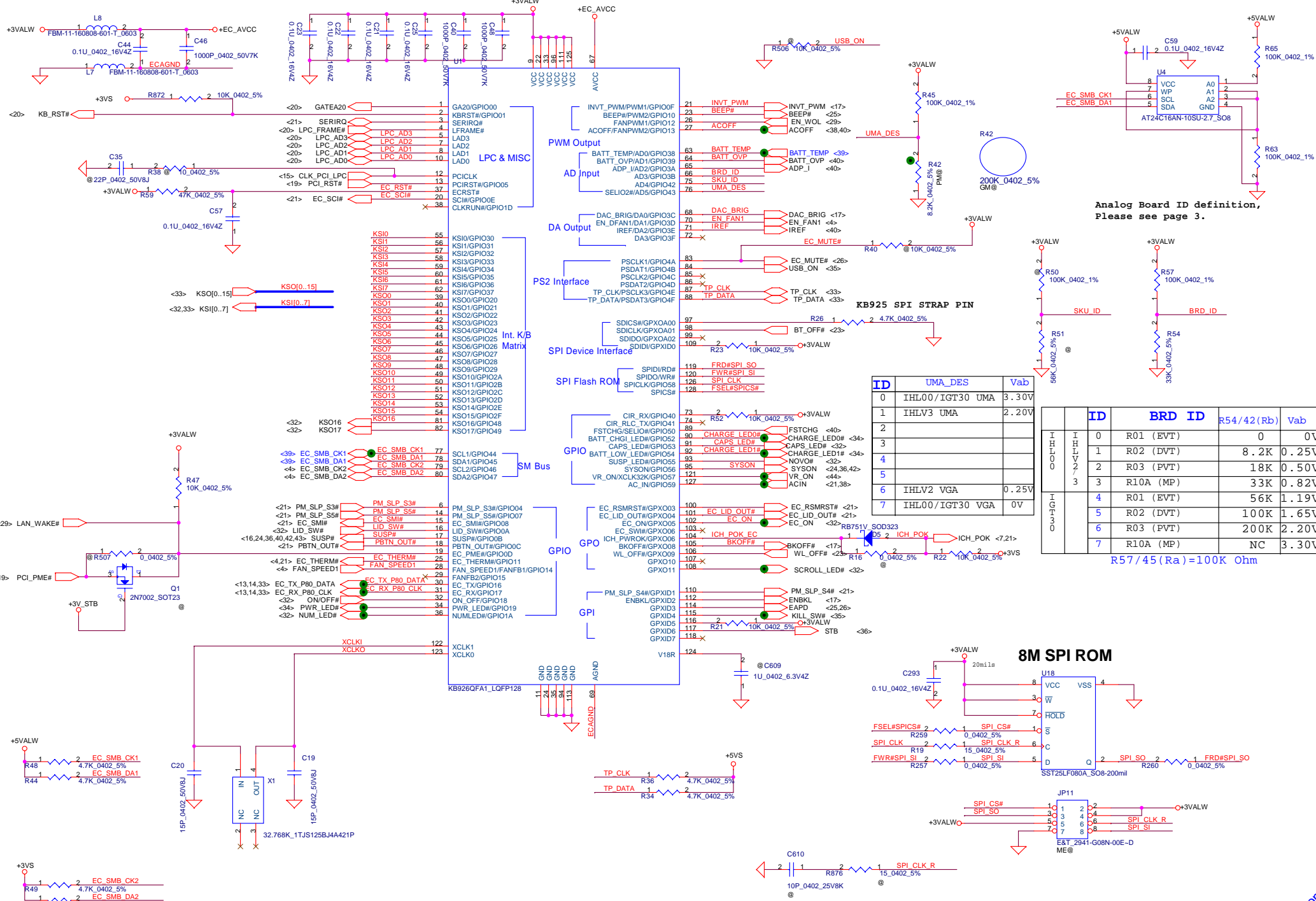
Change C468, C470, C473, C474, C475, C476 from 0.01uF to 0.1uF



near LAN controller



Security Classification	Compal Secret Data			Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	LAN CONTROLLER	
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**Analog Board ID definition, Please see page 3.**

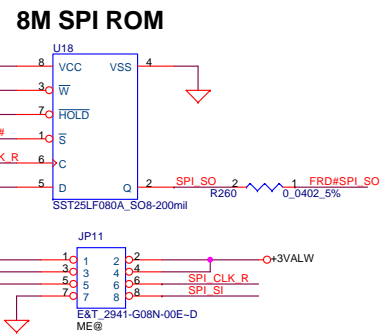
ID	UMA_DES	Vab
0	IHL00/IGT30 UMA	3.30V
1	IHLV3 UMA	2.20V
2		
3		
4		
5		
6	IHLV2 VGA	0.25V
7	IHL00/IGT30 VGA	0V

ID	BRD ID	R54/42 (Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03 (PVT)	18K	0.50V
3	R10A (MP)	33K	0.82V
4	R01 (EVT)	56K	1.19V
5	R02 (DVT)	100K	1.65V
6	R03 (PVT)	200K	2.20V
7	R10A (MP)	NC	3.30V

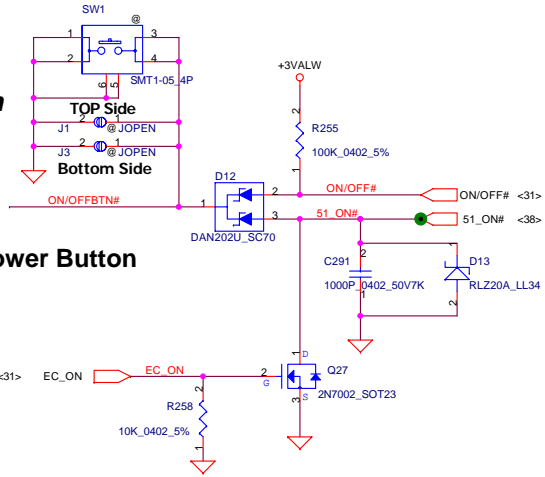
R57/45 (Ra) = 100K Ohm

ID	UMA_DES	Vab
0	IHL00/IGT30 UMA	3.30V
1	IHLV3 UMA	2.20V
2		
3		
4		
5		
6	IHLV2 VGA	0.25V
7	IHL00/IGT30 VGA	0V

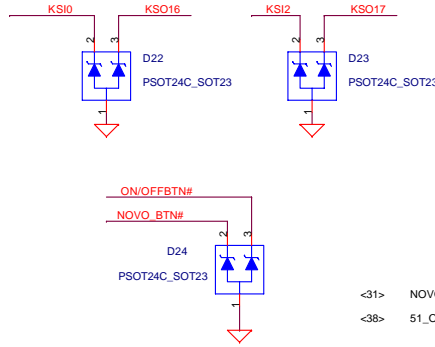


Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	<b>Compal Electronics, Inc.</b>
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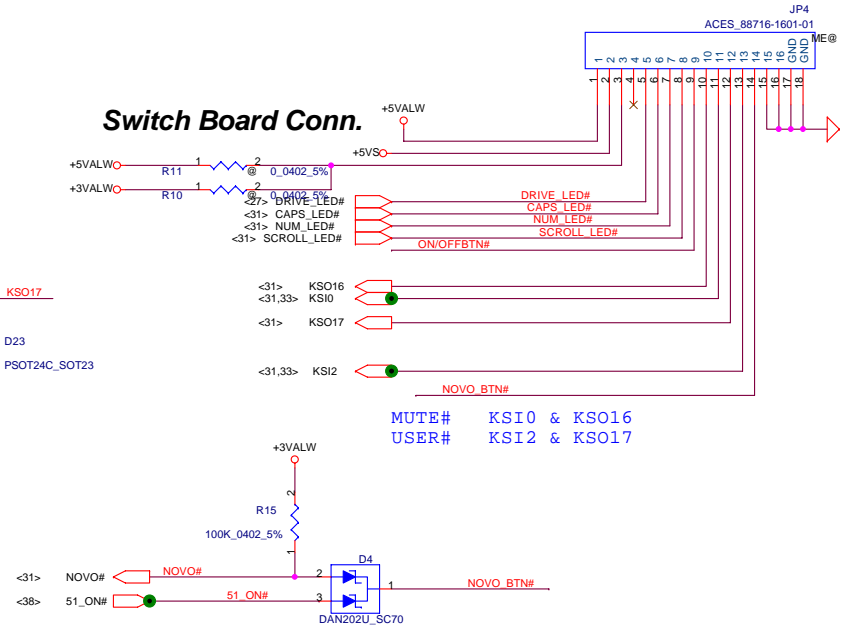
### ON/OFF switch



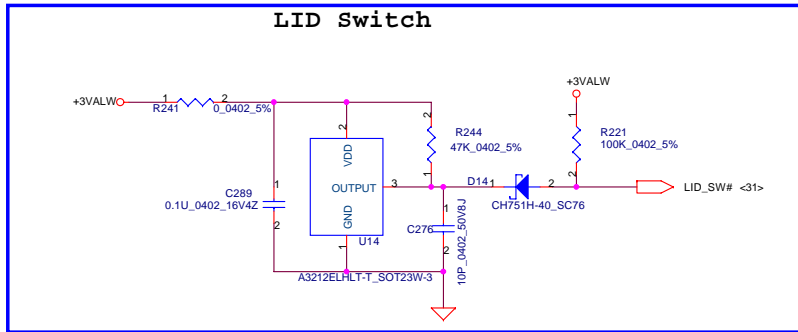
### Power Button



### Switch Board Conn.



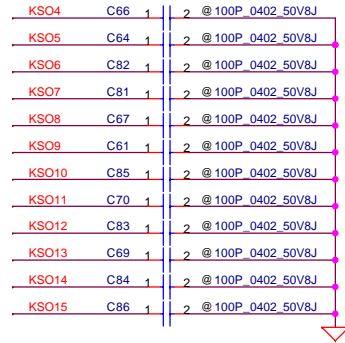
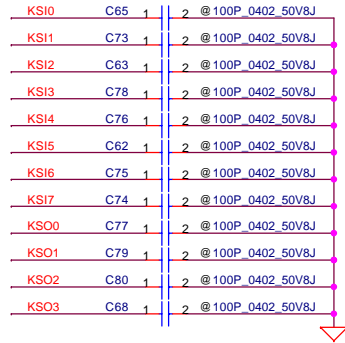
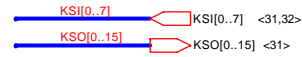
### LID Switch



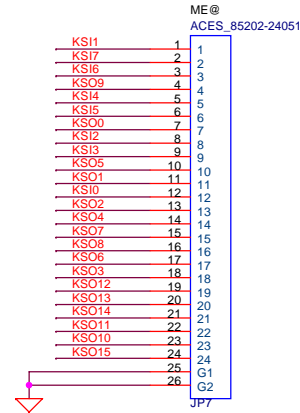
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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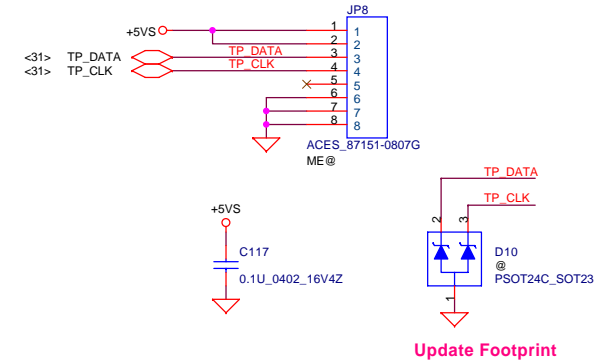
# INT\_KBD Conn.



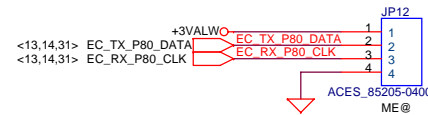
## For IHL00



## To TP/B Conn.

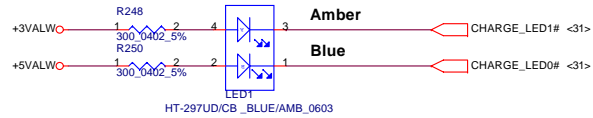
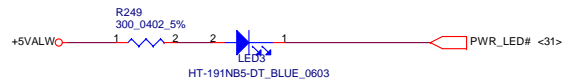


## EC DEBUG PORT

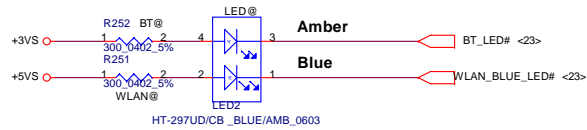


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Size	Document Number			Rev	0.1
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## LED



**Blue&Amber**

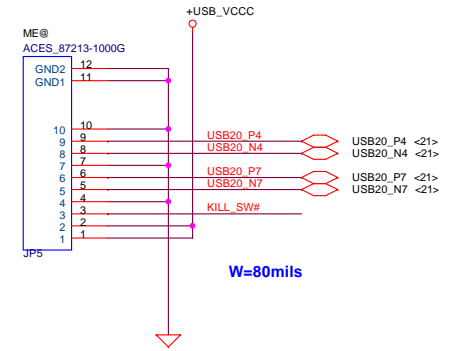
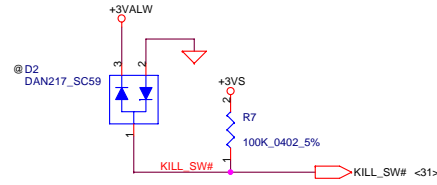


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Size B	Document Number LA-3691P
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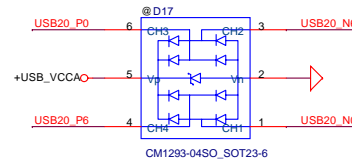
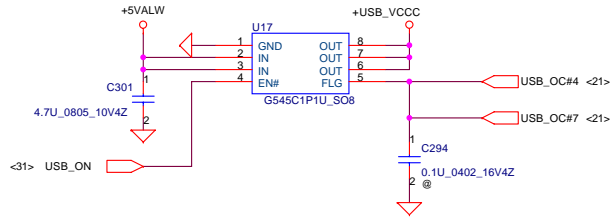
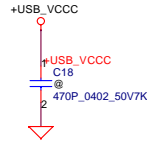
# USB Conn.

W=80mils

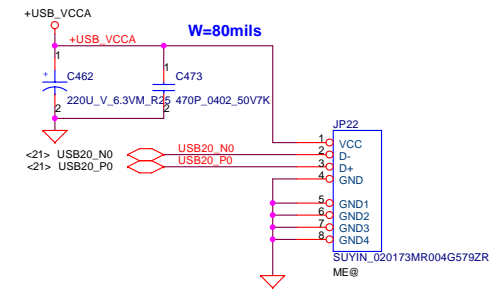
## Kill SWITCH



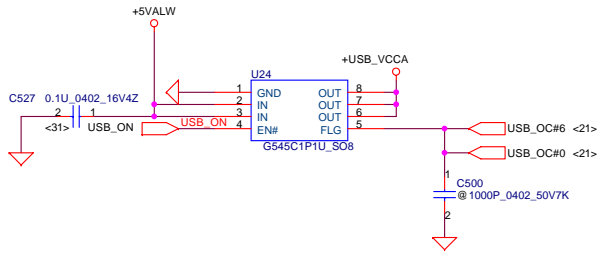
W=80mils



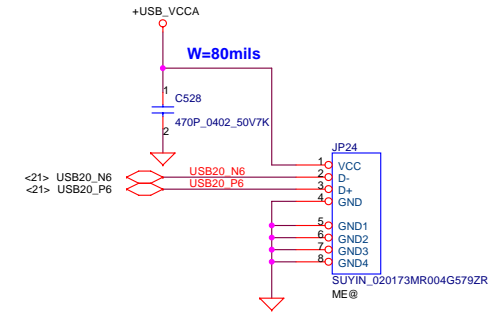
## USB CONN. 1



W=80mils



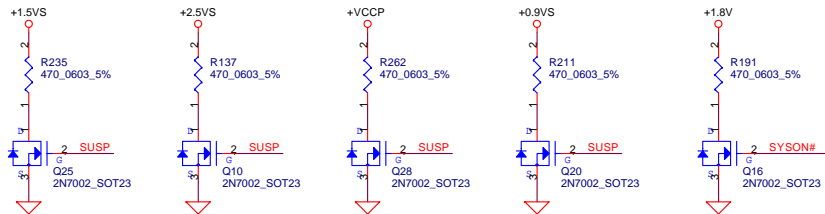
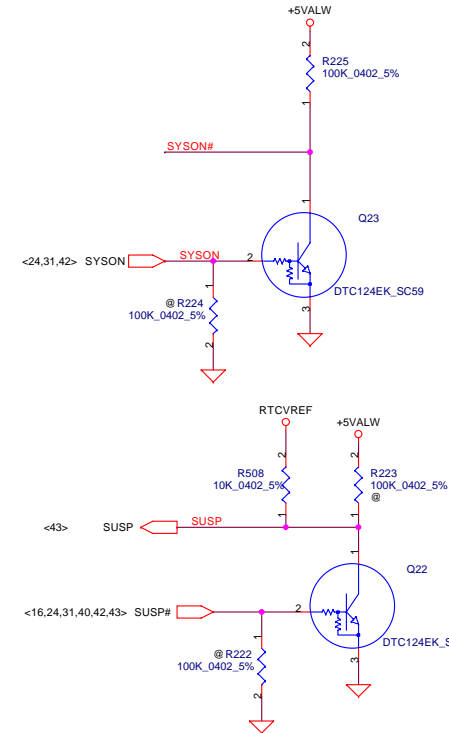
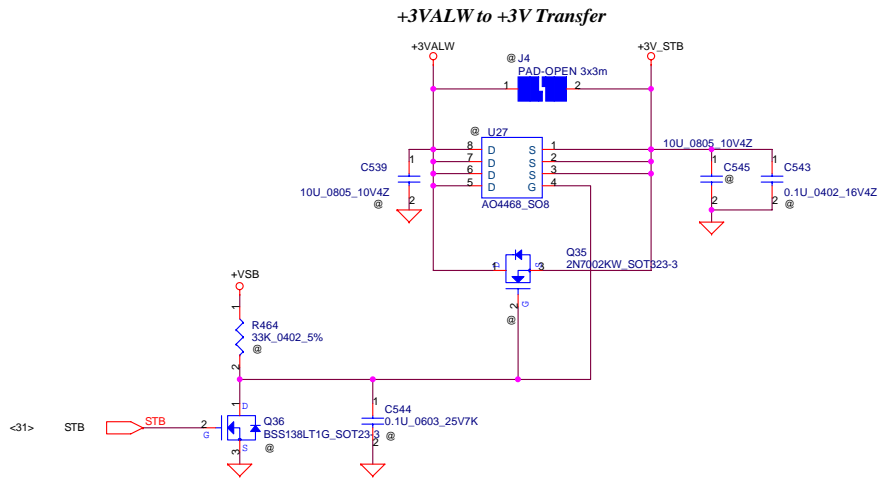
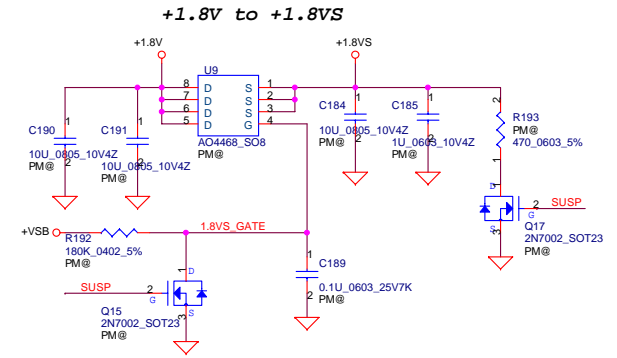
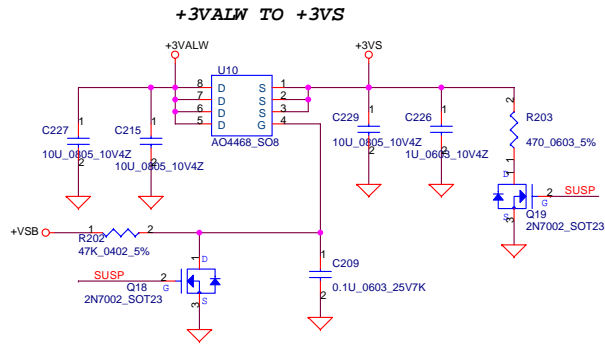
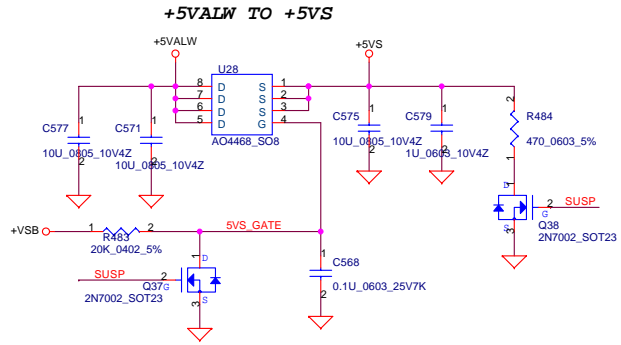
## USB CONN. 2



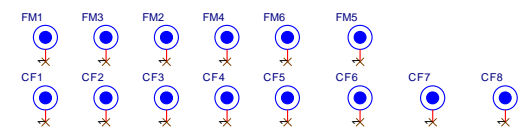
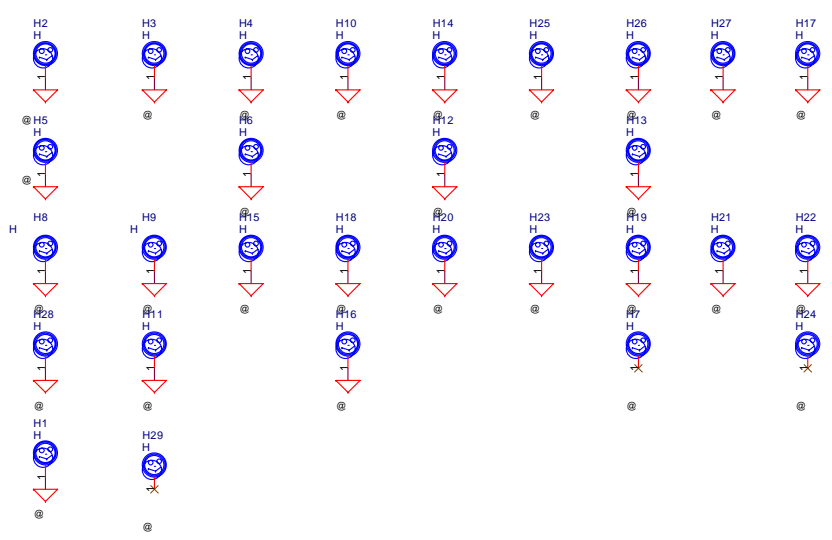
W=80mils

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Size	Document Number	Rev		Date:		Sheet
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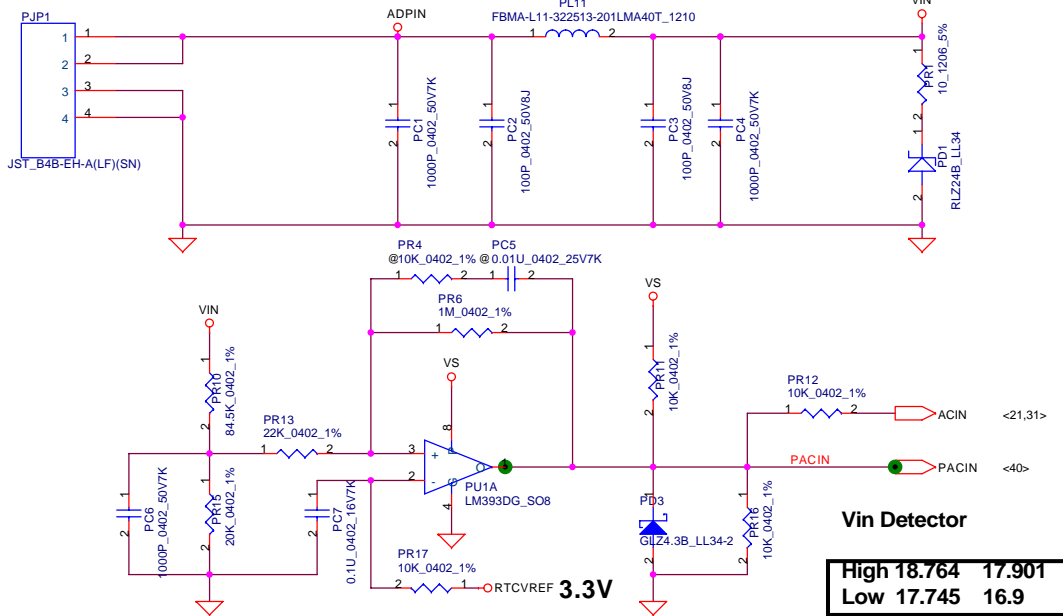
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC Interface	
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title FAN & Screw Hole	
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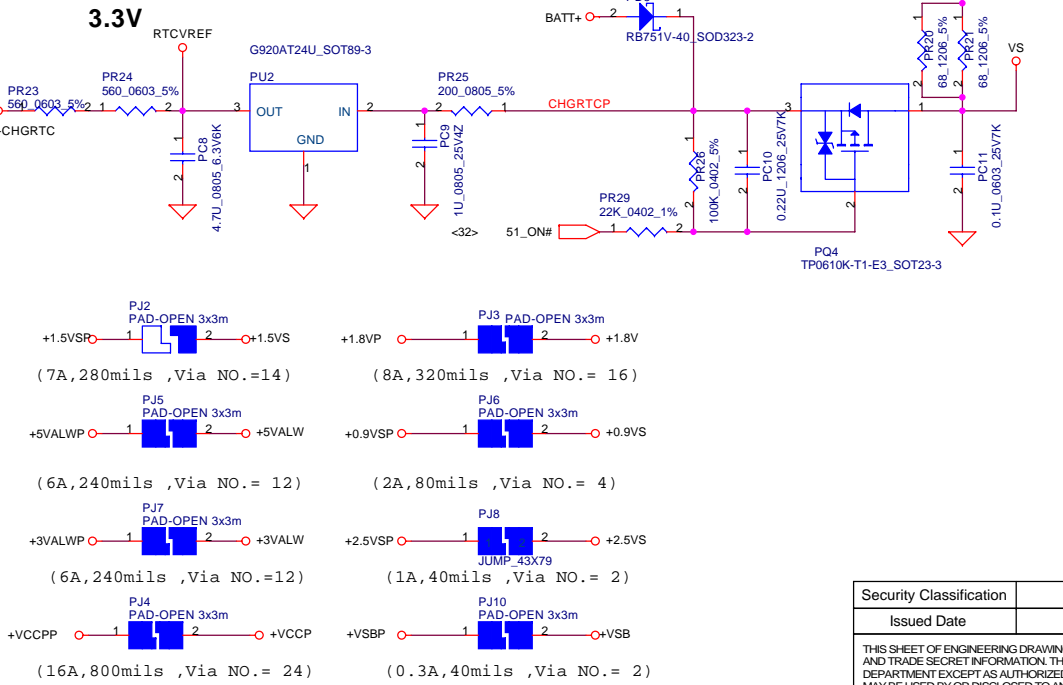
mailto:rain@hotmail.com

DC030005Q00



**Vin Detector**

High	18.764	17.901	17.063
Low	17.745	16.9	16.03

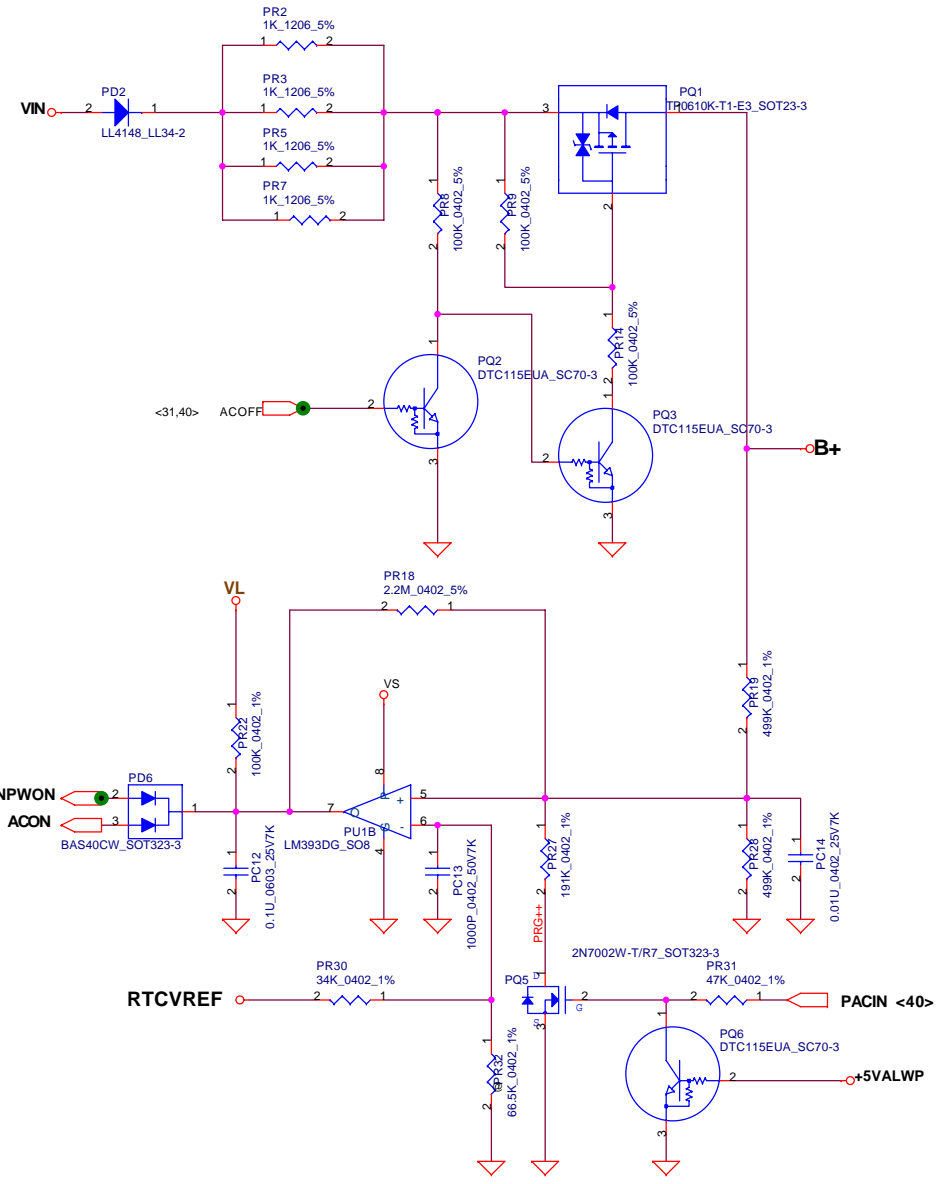


**ACIN**

	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

**BATT ONLY**

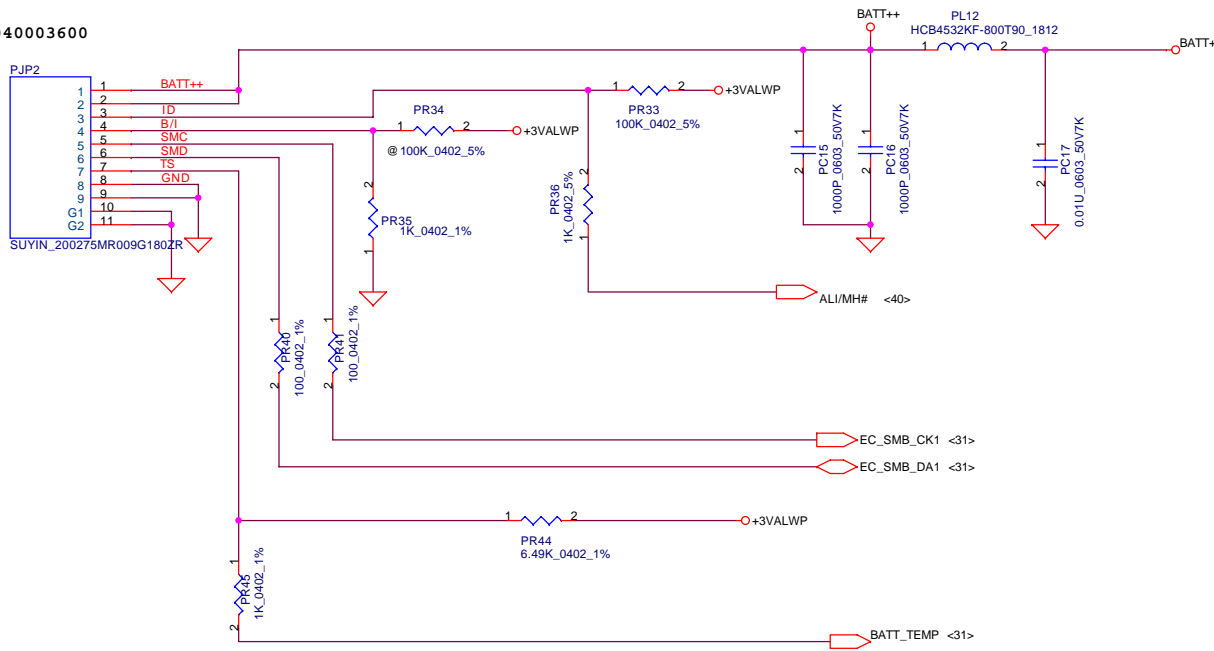
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



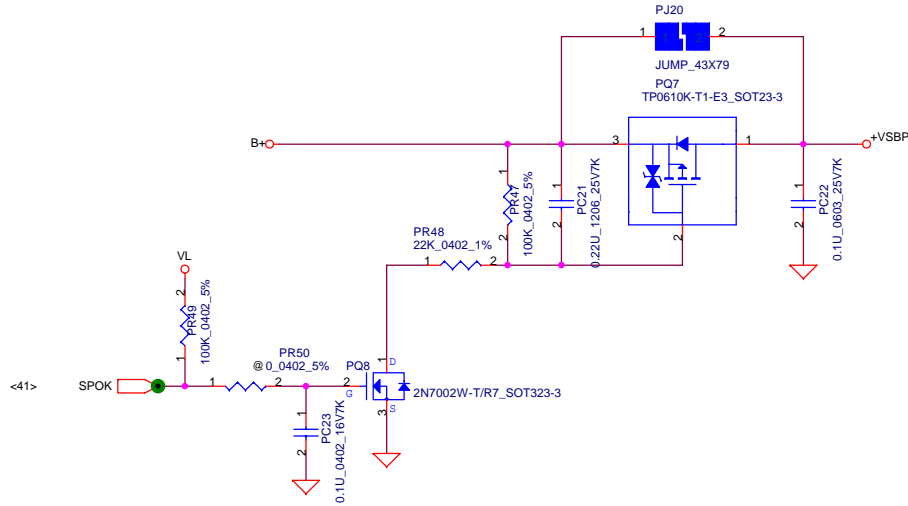
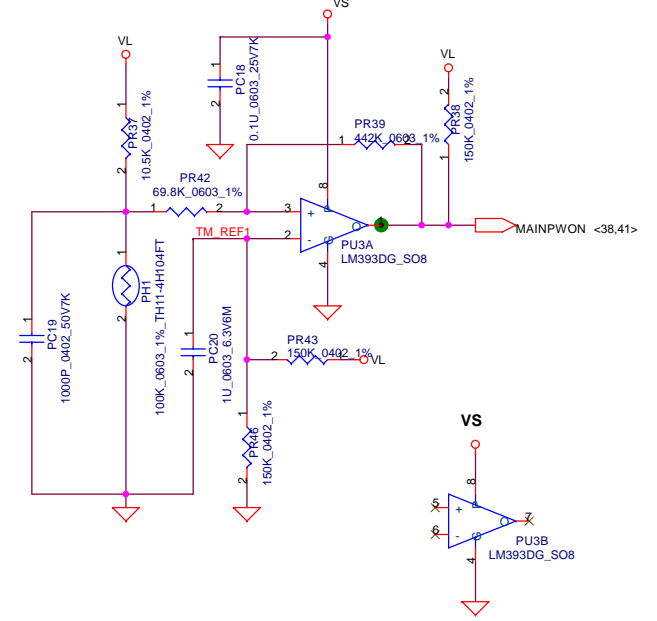
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Issued Date	2005/10/17	Deciphered Date	2006/10/17

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Title <b>DCIN/DECTOR</b>		
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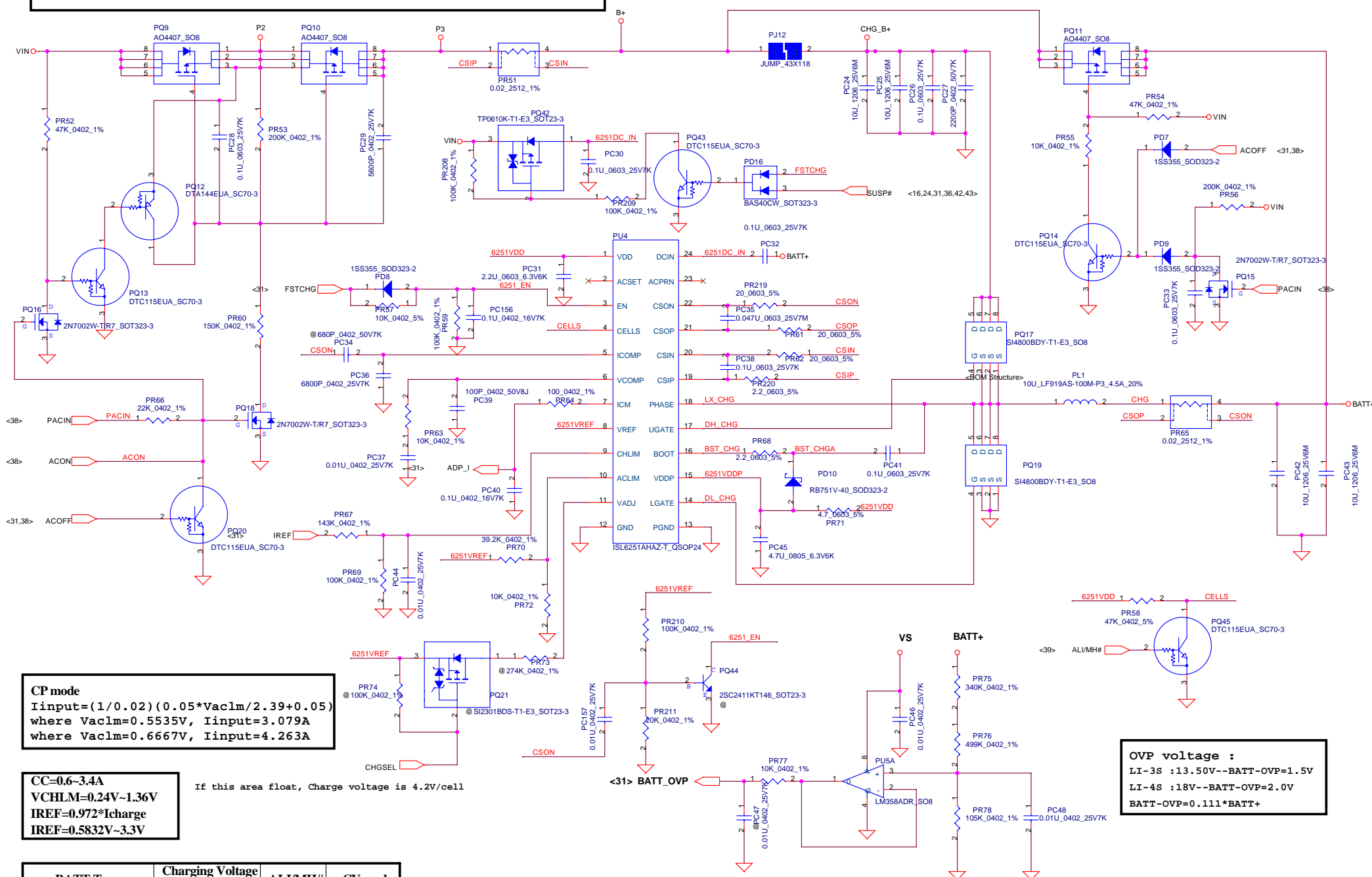
PH1 under CPU bottom side :  
 CPU thermal protection at 85 degree C  
 Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A  
 90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A

$$ADP\_I = 19.9 * I_{adapter} * R_{sense}$$



**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$   
 where  $V_{aclm} = 0.5535V$ ,  $I_{input} = 3.079A$   
 where  $V_{aclm} = 0.6667V$ ,  $I_{input} = 4.263A$

**CC=0.6~3.4A**  
 $V_{CHLM} = 0.24V \sim 1.36V$   
 $I_{REF} = 0.972 * I_{charge}$   
 $I_{REF} = 0.5832V \sim 3.3V$

If this area float, Charge voltage is 4.2V/cell

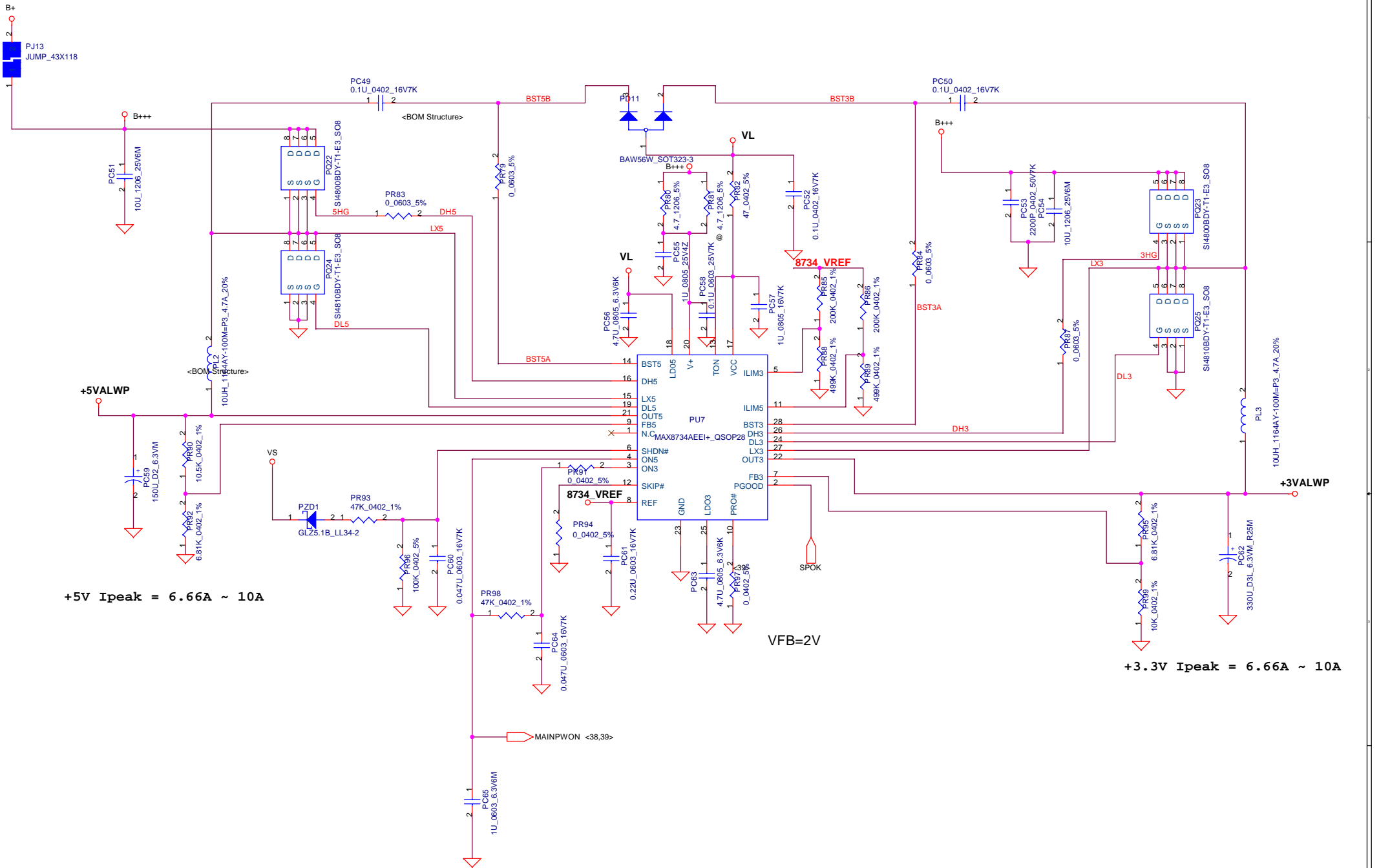
**OVP voltage :**  
 LI-3S : 13.50V -- BATT-OVP=1.5V  
 LI-4S : 18V -- BATT-OVP=2.0V  
 $BATT-OVP = 0.111 * BATT+$

BATT Type	Charging Voltage (0x15)	ALI/MH#	CV mode
4800mAH 3S pack	16800mV	LOW	16.8V
2400mAH 4S pack	12600mV	HIGH	12.60V

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Title <b>CHARGER</b>			
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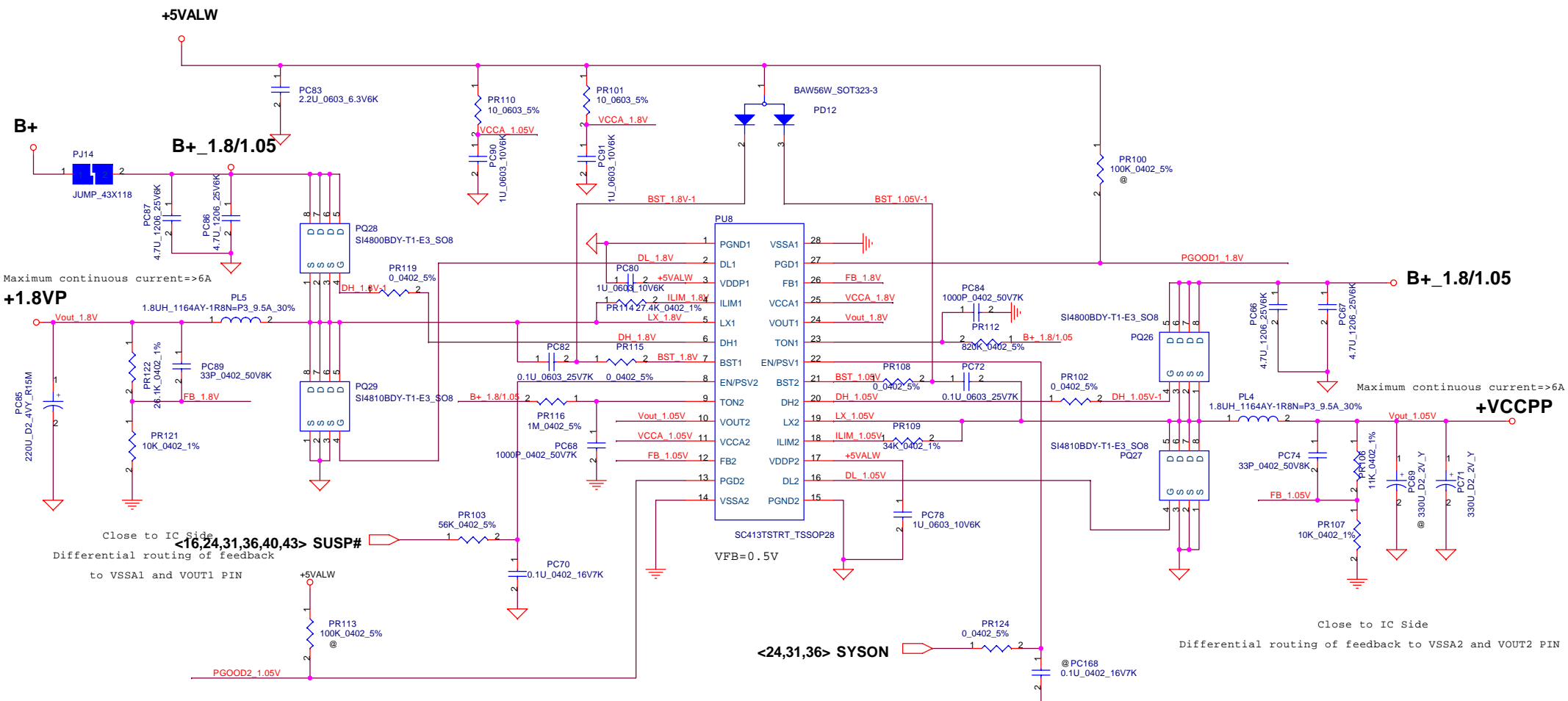


**+5V Ipeak = 6.66A ~ 10A**

**+3.3V Ipeak = 6.66A ~ 10A**

**VFB=2V**

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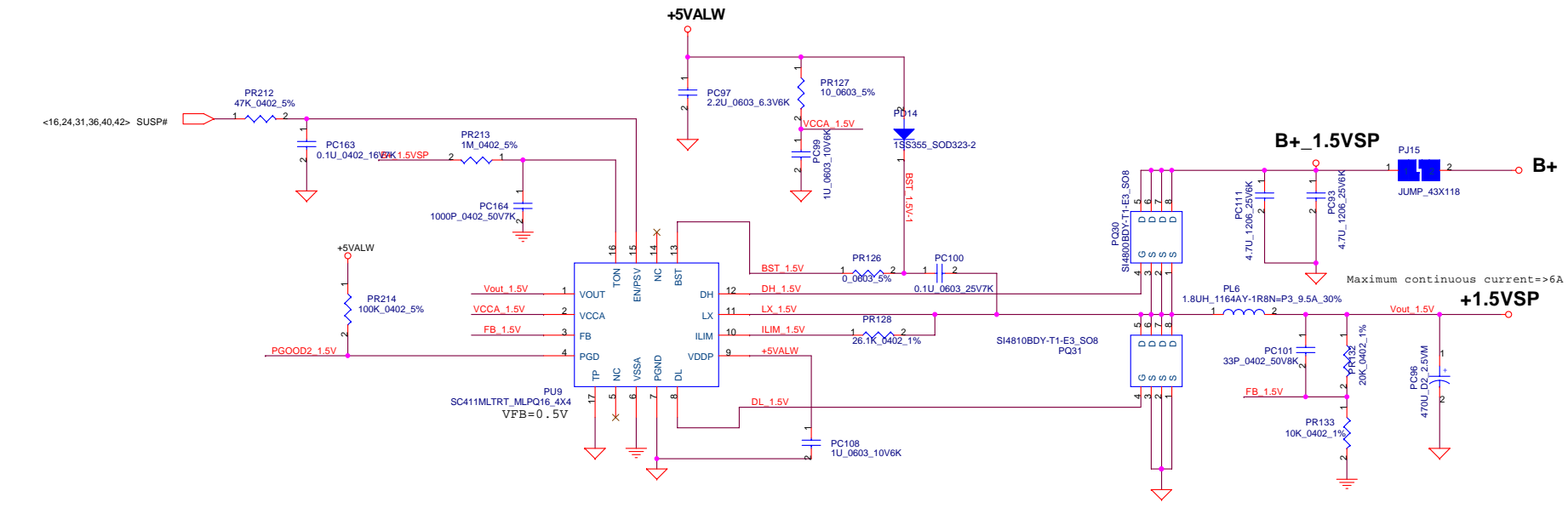
Maximum continuous current=>6A

Maximum continuous current=>6A

VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
**Ipeak=12.17A, Imax=8.519A**  
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$   
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$   
 FDS6670AS:Rds(on)=>Typ:9 mOhm  
 Max:11.5 mOhm  
 $Iocp = Ivalley + Iripple / 2$   
 $Iripple = (vin - vout) * (Ton / L) = 5.467A, 1/2 Iripple = 2.734A$   
 $Ivalleymin = 10E-6 * (PR120 / Rds(ON)max * 1.5)$   
 $= 9 * 10e-6 * (27.4K / 0.0115 * 1.5) = 14.295A > 11.73 * 1.2 = 14.076A$   
 $Ivalleymax = 10E-6 * (PR120 / Rds(ON)typ * 1.2)$   
 $= 11 * 10e-6 * (27.4K / 0.009 * 1.2) = 27.907A$   
 OCP=>17.029A~30.641A

VFB=0.5V  
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$   
**Ipeak=5.16A, Imax=3.612A**  
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$   
 $= 0.3201us$   
 AO4916 Rds(on)=>Typ:21 mOhm  
 Max:27 mOhm  
 $Ivalleymin = 9 * 10u * (29.4K / 0.027 * 1.4) = 7A$   
 $Ivalleymax = 11 * E-6 * (29.4K / 0.021 * 1.1) = 12.833A$   
 $Iripple = (vin - vout) * (Ton / L) = 2.546A, 1/2 Iripple = 1.273A$   
 $Iocp = Ivalley + Iripple / 2$   
 OCP=>8.273A~14.106A

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				+VCCPP/+1.8VP	
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**B+ 1.5VSP**

Maximum continuous current=>6A

**+1.5VSP**

Close to IC Side  
Differential routing of feedback to VSSA2 and VOUT2 PIN

**VFB=0.5V, Ipeak=14.02A, Imax=9.814A**

The current rating of +1.05VSP include +VCC\_GFX current.

$V_o = V_{FB} * (1 + PR146 / PR147) = 1.05V$

$T_{on} = (3.3E-12 * (PR142 + 37K) * (V_{out} / V_{bat})) + 50ns = 0.2391us$

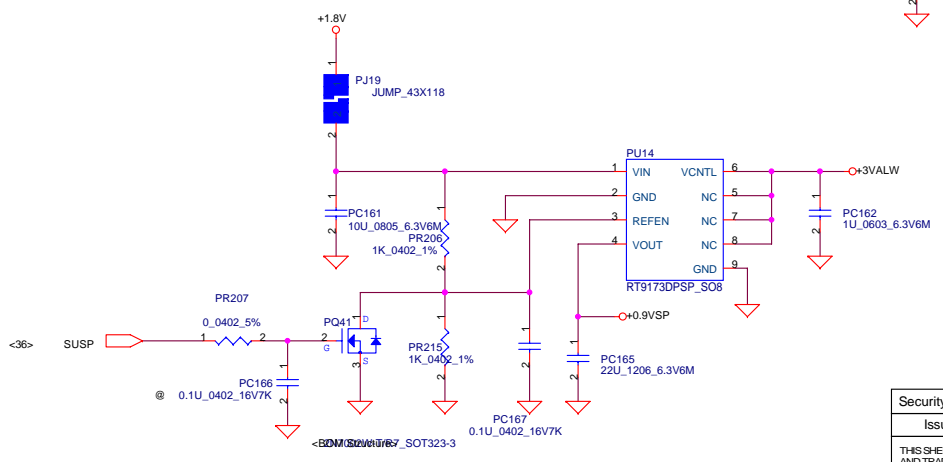
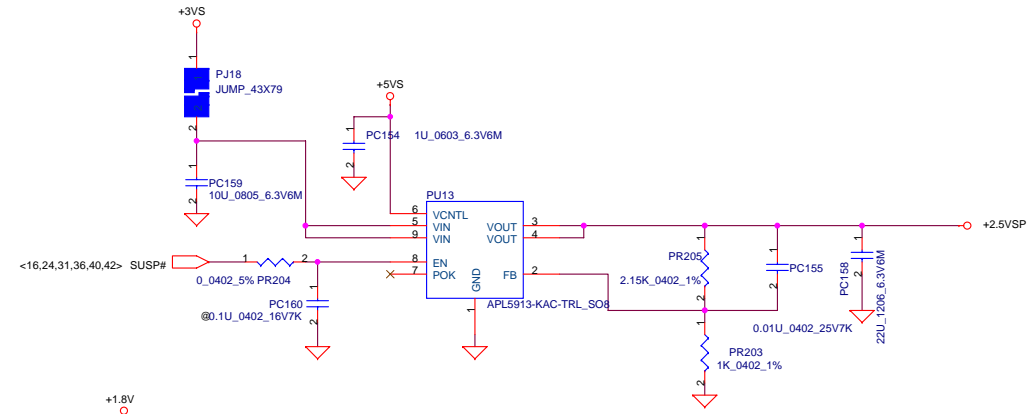
SI4810BDY:Rds(on) => Typ: 9mOhm  
Max: 11.5 mOhm

$I_{valleymin} = 9 * 10E-6 * (PR145 / R_{ds(ON)max} * 1.5)$   
**= 9 \* 10E-6 \* (26.1K / (0.0115 \* 1.5)) = 13.617A**

$I_{valleymax} = 11 * 10E-6 * (PR145 / R_{ds(ON)min} * 1.2)$   
 $= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$

$I_{ripple} = (v_{in} - v_{out}) * (T_{on} / L) = 4.292A, 1/2 I_{ripple} = 2.146A$

$I_{ocp} = I_{valley} + I_{ripple} / 2$   
**OCP => 15.763A ~ 22.222A**

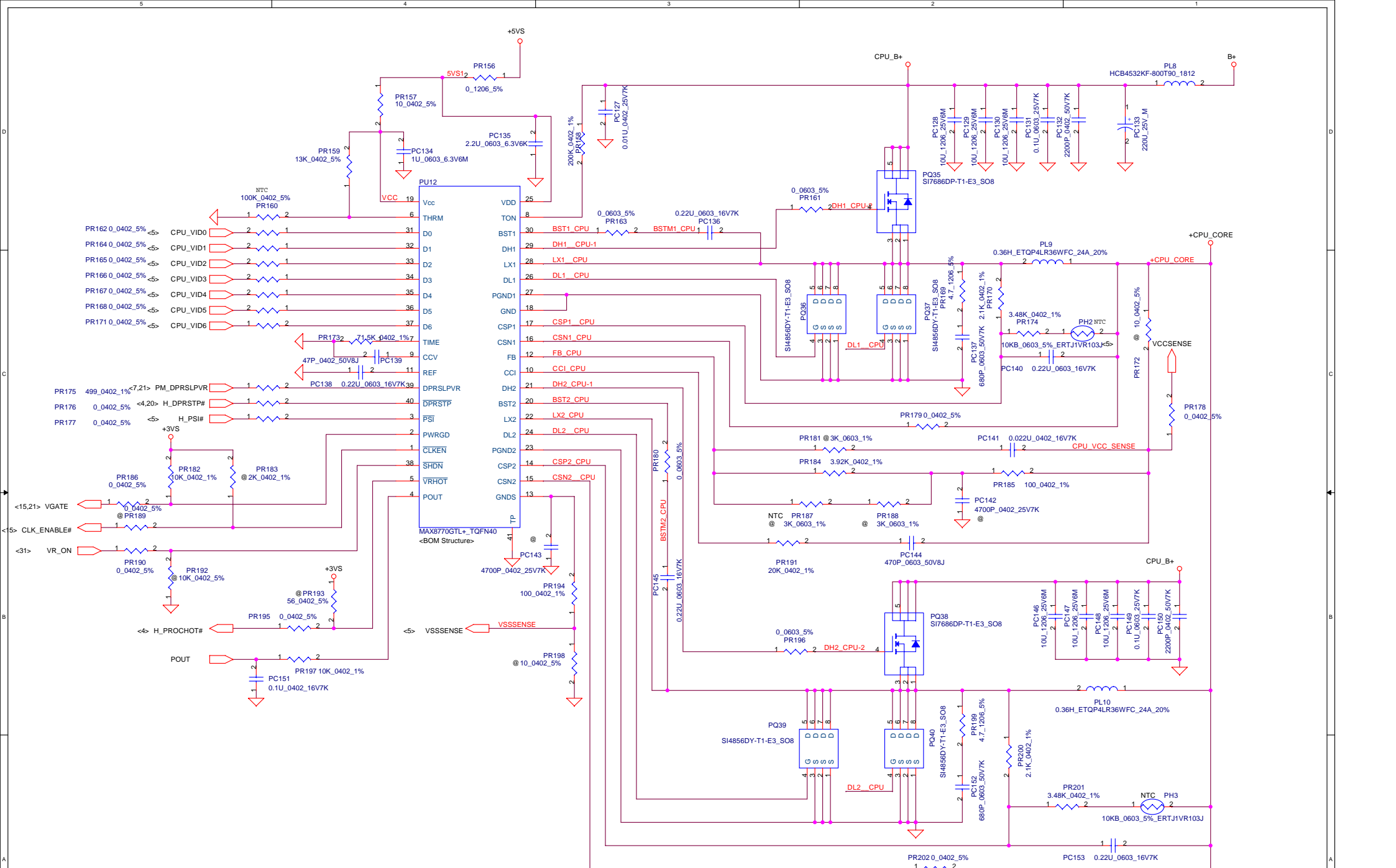


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Compal Electronics, Inc.		
1.5VSP/2.5VSP/0.9VSP		
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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List
1	USB port 2 and 4 can't work	0.2	P.35	Change U17 P/N SA005280110 to SA00001H600
2	Change symbol	0.2	P.20.31	Change Y4 and X1 to SJ132P7K220
3	CRT wave	0.2	P.10	Change L41 to R878 and reserve C619
4	To meet INTEL SPEC	0.2		Change C148.C442.C171.C400.C606.C607 from 2200P to 22N
5	Delete reserve	0.2	P.17	Delete R71,74 Delete C171
6	FACTORY REQUEST	0.2	P.35	Delete JP5 PIN3
7	To meet CRT SPEC	0.2	P.18	Remove C7
8	Tune frequency	0.2	P.28	Change C511;515 from 27p to 18p
9	EMI Request	0.2		change C632 to 2.2nF Remove R441,R145,C6,12,13,change L2,3,4 to SM01000AL00
10	EMI Request	0.2	P.30	LAN RX TX change
11	EMI Request	0.2	P.32	ADD D22;23;24
12	EMI Request	0.2	P.4	Delete ITP_BPM0-5 and R515
13	FAN issue	0.2	P.4	Change R276 from 10k to 1k ohm C341 from 1000p to 100p
14	USB issue	1.0	P.21	Change USB port 2 to NEW card port 7 to USB Change R322 to 22 ohm
15	Remove LPC debug connect	1.0	P.33	Remove JP13,R265,R441,R145
16	ESD Request and reserve	1.0		ADD T48 AND R515 AND JP9 29,30 pin to GND
17	Power improve	1.0	P.6	RemoveC26,31,314,315
18		0.2		
19		0.2		
20		0.2		

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<b>Compal Electronics, Inc.</b>		
Title	HW PIR	
Size	Document Number	Rev
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	+1.5VSP output voltage is 2V.	BOM error for +1.5VSP output.	0.2	6	1.Change the PR132 for 30K to 20K.	03/20/07	DVT
2	Power sequence update for 1.5VS.	HW request.	0.2	6	1.Add the PC163 0.1u_0402_16V. 2.Change the PR212 from 0 to 47K.	04/09/07	FVT
3	Power sequence update for +VCCPP.	HW request.	0.2	5	1.Add the PC97 0.1u_0402_16V. 2.Change the PR103 from 0 to 56K.	04/09/07	FVT
4	Reduce the overshoot on P2 point.	IFL01 issue.	0.2	1	1.Add the PR1 10_1206 and PD1 RZ24B.	04/09/07	PVT
5	Symbol issue.	DFB team request.	0.2	1/3	1.Change the symbol for the PZD1,PD2,PD3,PD4 and PQ21.	04/09/07	FVT
6	Noise issue for idle.	Noise issue for idle.	0.2	7	1.Change the PC133 from 100U to 220U 25V.	04/09/07	FVT

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Title: PIR (PWR)			
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