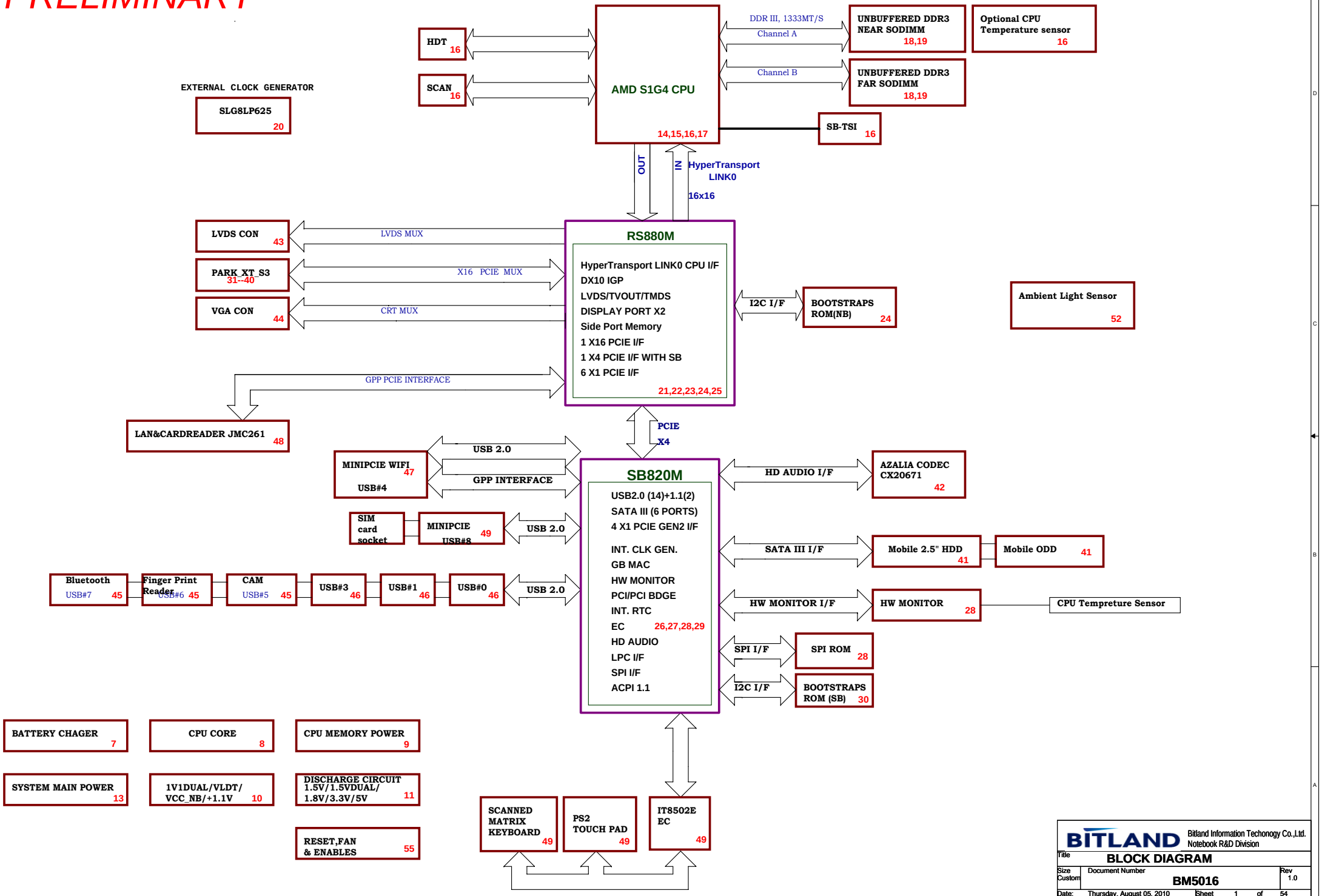
PRELIMINARY

GUAM S1G4 SCHEMATIC DESIGN



BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title	BLOCK DIAGRAM	
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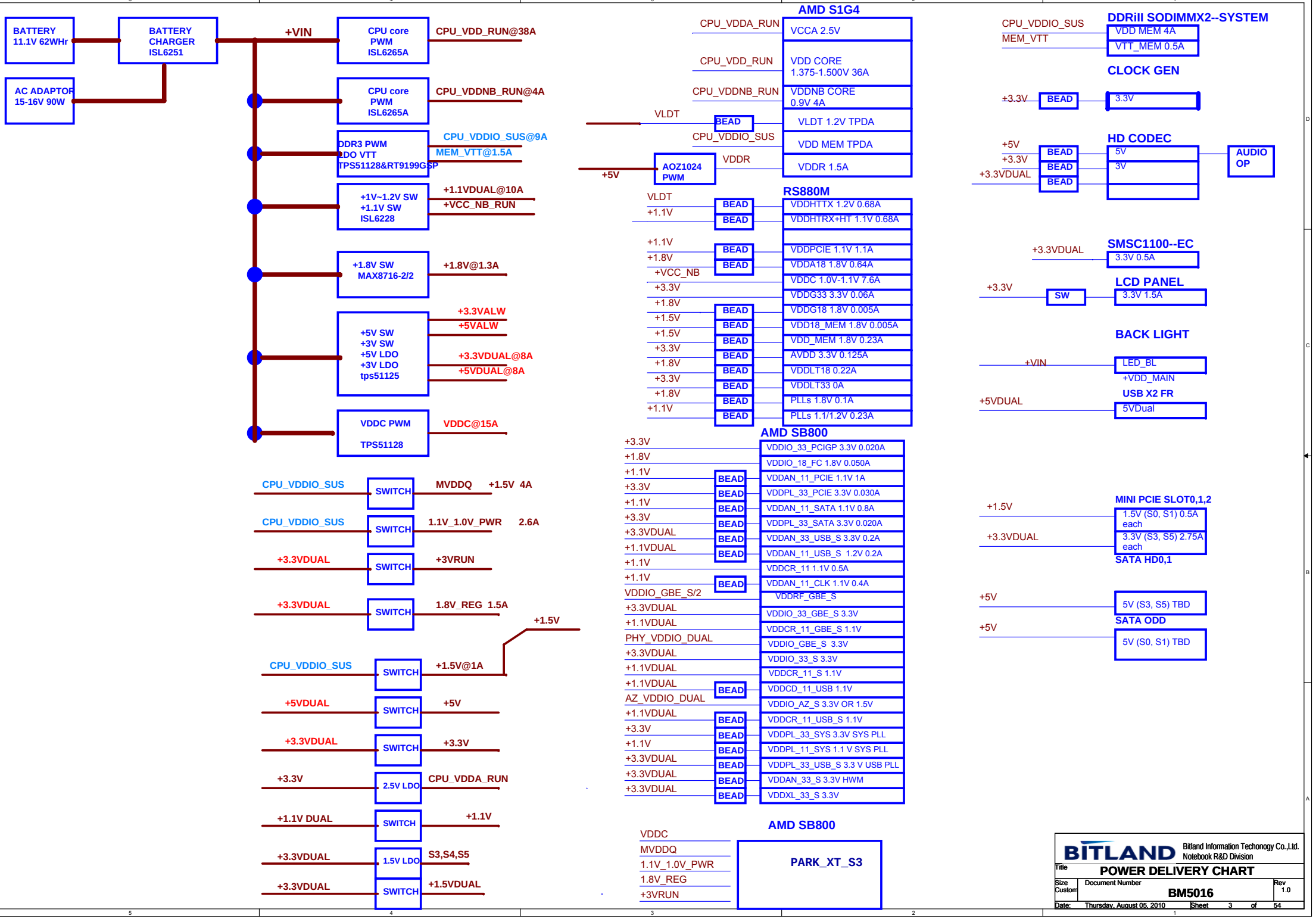
BATTERY 11.1V 62WHr
AC ADAPTOR 15-16V 90W
BATTERY CHARGER ISL6251
+VIN
CPU core PWM ISL6265A
CPU_VDD_RUN@38A
CPU core PWM ISL6265A
CPU_VDDNB_RUN@4A
DDR3 PWM LDO VTT TPS51128&RT9199GSP
CPU_VDDIO_SUS@9A
MEM_VTT@1.5A
+1V~1.2V SW +1.1V SW ISL6228
+1.1VDUAL@10A
+VCC_NB_RUN
+1.8V SW MAX8716-2/2
+1.8V@1.3A
+5V SW +3V SW +5V LDO +3V LDO tps51125
+3.3VALW
+5VALW
+3.3VDUAL@8A
+5VDUAL@8A
VDDC PWM TPS51128
VDDC@15A
CPU_VDDIO_SUS
SWITCH
MVDDQ +1.5V 4A
CPU_VDDIO_SUS
SWITCH
1.1V_1.0V_PWR 2.6A
+3.3VDUAL
SWITCH
+3VRUN
+3.3VDUAL
SWITCH
1.8V_REG 1.5A
+1.5V
CPU_VDDIO_SUS
SWITCH
+1.5V@1A
+5VDUAL
SWITCH
+5V
+3.3VDUAL
SWITCH
+3.3V
+3.3V
2.5V LDO
CPU_VDDA_RUN
+1.1V DUAL
SWITCH
+1.1V
+3.3VDUAL
1.5V LDO
S3,S4,S5
+3.3VDUAL
SWITCH
+1.5VDUAL
AMD S1G4
CPU_VDDA_RUN
VCCA 2.5V
CPU_VDD_RUN
VDD CORE 1.375-1.500V 36A
CPU_VDDNB_RUN
VDDNB CORE 0.9V 4A
VLDT
BEAD
VLDT 1.2V TPDA
CPU_VDDIO_SUS
VDD MEM TPDA
+5V
AOZ1024 PWM
VDDR
VDDR 1.5A
RS880M
VLDT
+1.1V
BEAD
VDDHTTX 1.2V 0.68A
VDDHTRX+HT 1.1V 0.68A
+1.1V
+1.8V
+VCC_NB
BEAD
VDDPCIE 1.1V 1.1A
VDDA18 1.8V 0.64A
VDDC 1.0V-1.1V 7.6A
+3.3V
VDDG33 3.3V 0.06A
+1.8V
+1.5V
+1.5V
+3.3V
+1.8V
+3.3V
+1.8V
+1.1V
BEAD
VDDG18 1.8V 0.005A
VDD18_MEM 1.8V 0.005A
VDD_MEM 1.8V 0.23A
AVDD 3.3V 0.125A
VDDLT18 0.22A
VDDLT33 0A
PLLs 1.8V 0.1A
PLLs 1.1/1.2V 0.23A
AMD SB800
+3.3V
+1.8V
+1.1V
+3.3V
+1.1V
+3.3V
+3.3VDUAL
+1.1VDUAL
+1.1V
+1.1V
VDDIO_GBE_S/2
+3.3VDUAL
+1.1VDUAL
PHY_VDDIO_DUAL
+3.3VDUAL
+1.1VDUAL
+1.1VDUAL
AZ_VDDIO_DUAL
+1.1VDUAL
+3.3V
+1.1V
+3.3VDUAL
+3.3VDUAL
+3.3VDUAL
BEAD
VDDIO_33_PCIGP 3.3V 0.020A
VDDIO_18_FC 1.8V 0.050A
VDDAN_11_PCIE 1.1V 1A
VDDPL_33_PCIE 3.3V 0.030A
VDDAN_11_SATA 1.1V 0.8A
VDDPL_33_SATA 3.3V 0.020A
VDDAN_33_USB_S 3.3V 0.2A
VDDAN_11_USB_S 1.2V 0.2A
VDDCR_11 1.1V 0.5A
VDDAN_11_CLK 1.1V 0.4A
VDDRF_GBE_S
VDDIO_33_GBE_S 3.3V
VDDCR_11_GBE_S 1.1V
VDDIO_GBE_S 3.3V
VDDIO_33_S 3.3V
VDDCR_11_S 1.1V
VDDCD_11_USB 1.1V
VDDIO_AZ_S 3.3V OR 1.5V
VDDCR_11_USB_S 1.1V
VDDPL_33_SYS 3.3V SYS PLL
VDDPL_11_SYS 1.1 V SYS PLL
VDDPL_33_USB_S 3.3 V USB PLL
VDDAN_33_S 3.3V HWM
VDDXL_33_S 3.3V
AMD SB800
VDDC
MVDDQ
1.1V_1.0V_PWR
1.8V_REG
+3VRUN
PARK_XT_S3
DDRill SODIMMX2--SYSTEM
CPU_VDDIO_SUS
MEM_VTT
VDD MEM 4A
VTT_MEM 0.5A
CLOCK GEN
+3.3V
BEAD
3.3V
HD CODEC
+5V
+3.3V
+3.3VDUAL
BEAD
BEAD
BEAD
5V
3V
AUDIO OP
SMSC1100--EC
+3.3VDUAL
3.3V 0.5A
LCD PANEL
+3.3V
SW
3.3V 1.5A
BACK LIGHT
+VIN
LED_BL
+VDD_MAIN
USB X2 FR
+5VDUAL
5VDual
MINI PCIE SLOT0,1,2
+1.5V
+3.3VDUAL
1.5V (S0, S1) 0.5A each
3.3V (S3, S5) 2.75A each
SATA HD0,1
+5V
5V (S3, S5) TBD
SATA ODD
+5V
5V (S0, S1) TBD
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POWER DELIVERY CHART
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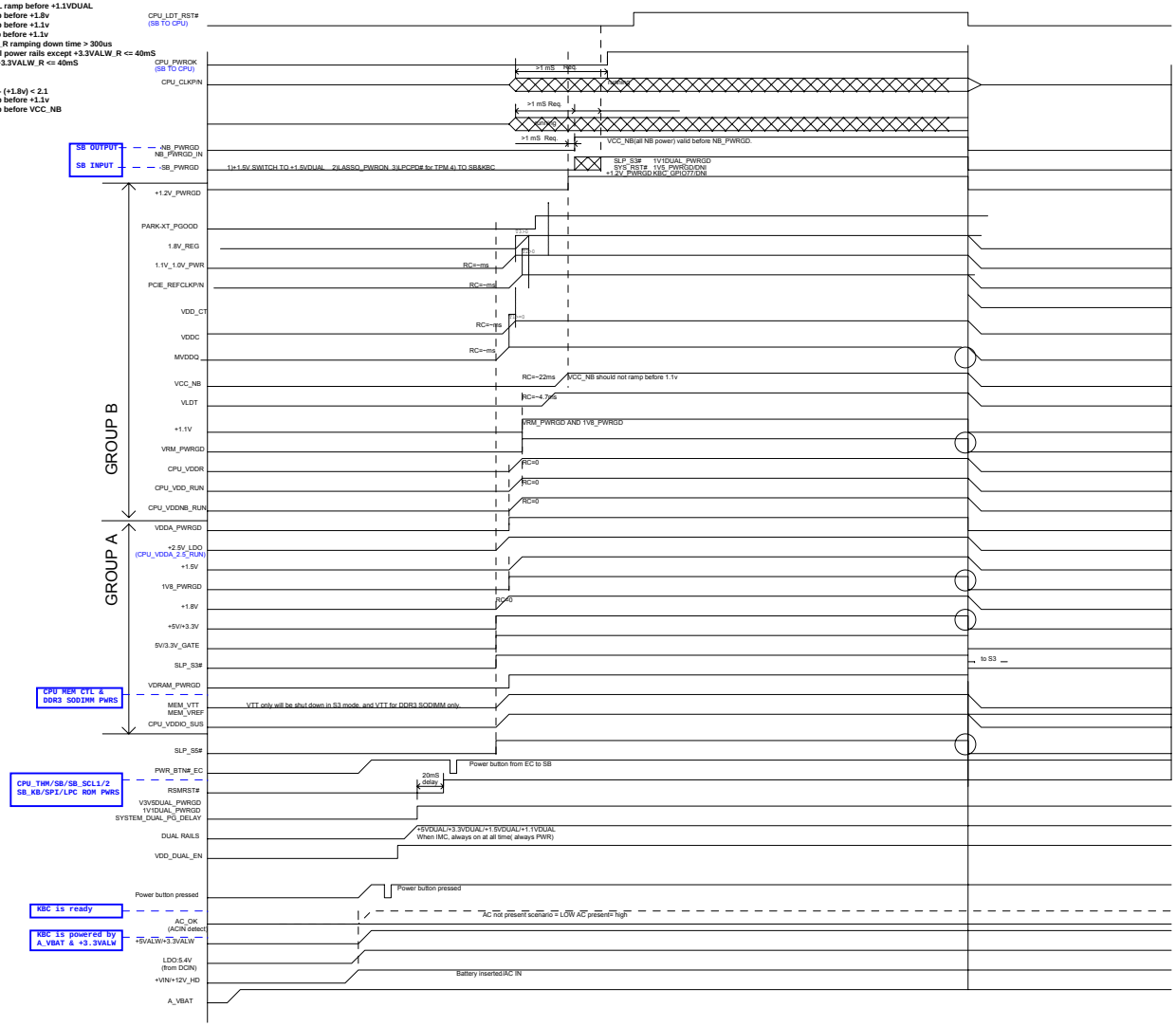
Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



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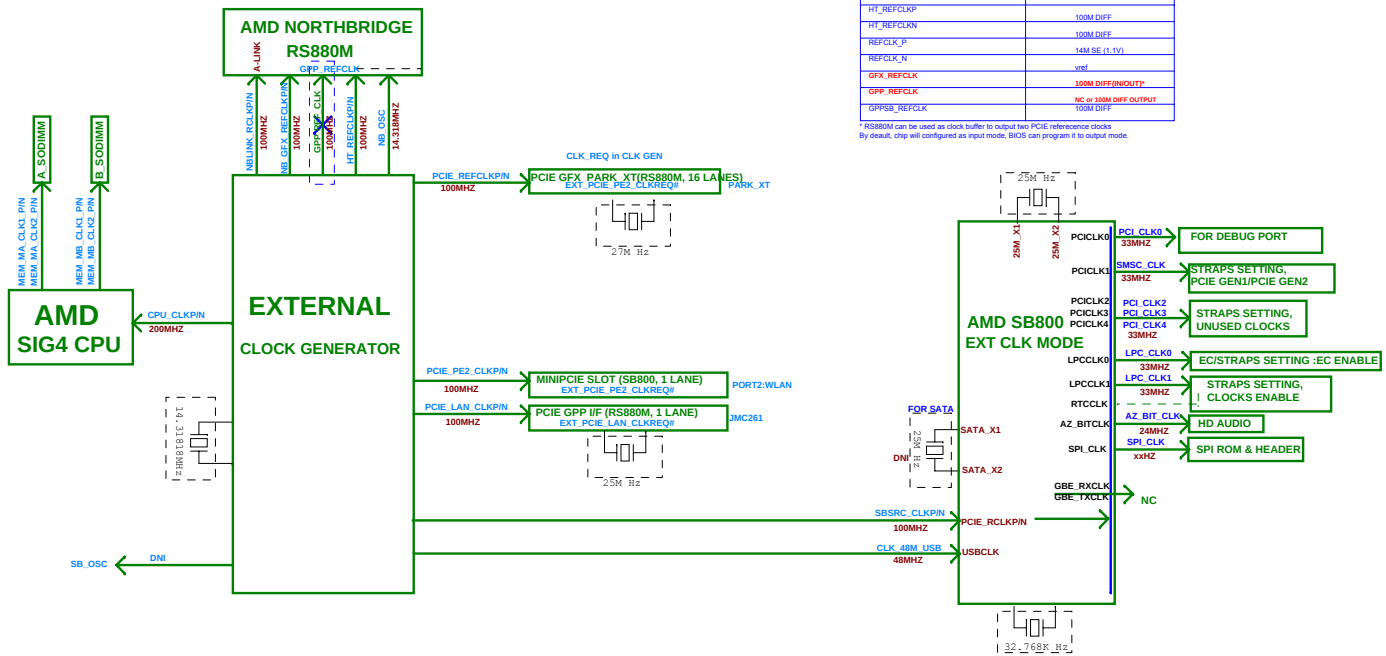
EXTERNAL CLOCK MODE

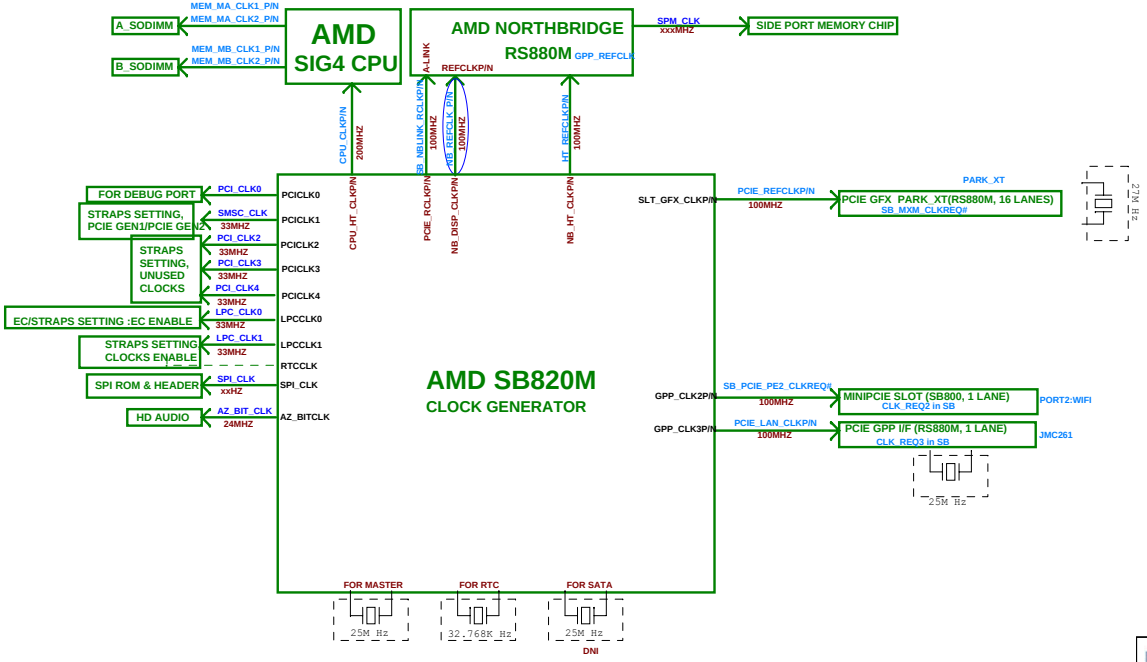
NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



INTERNAL CLOCK MODE



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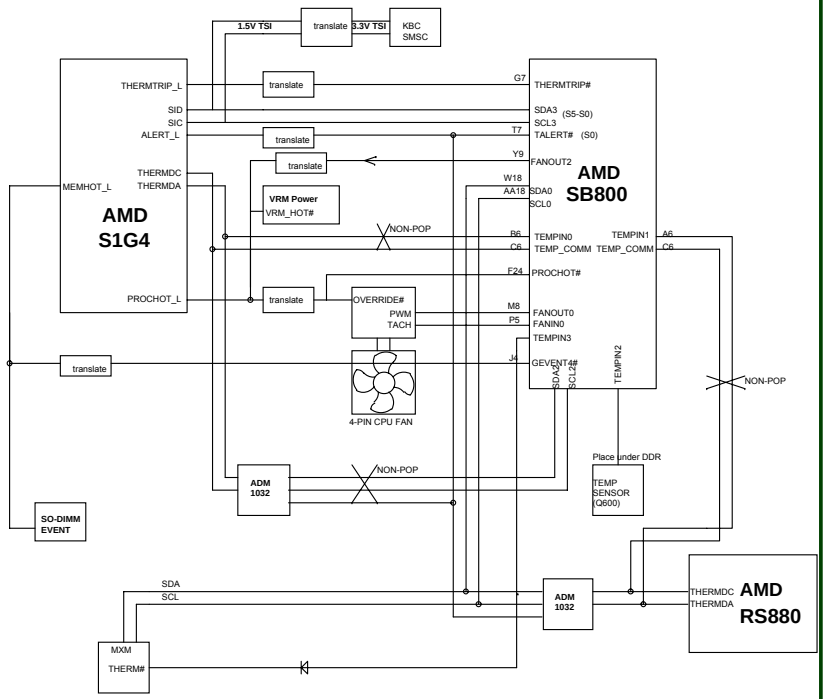
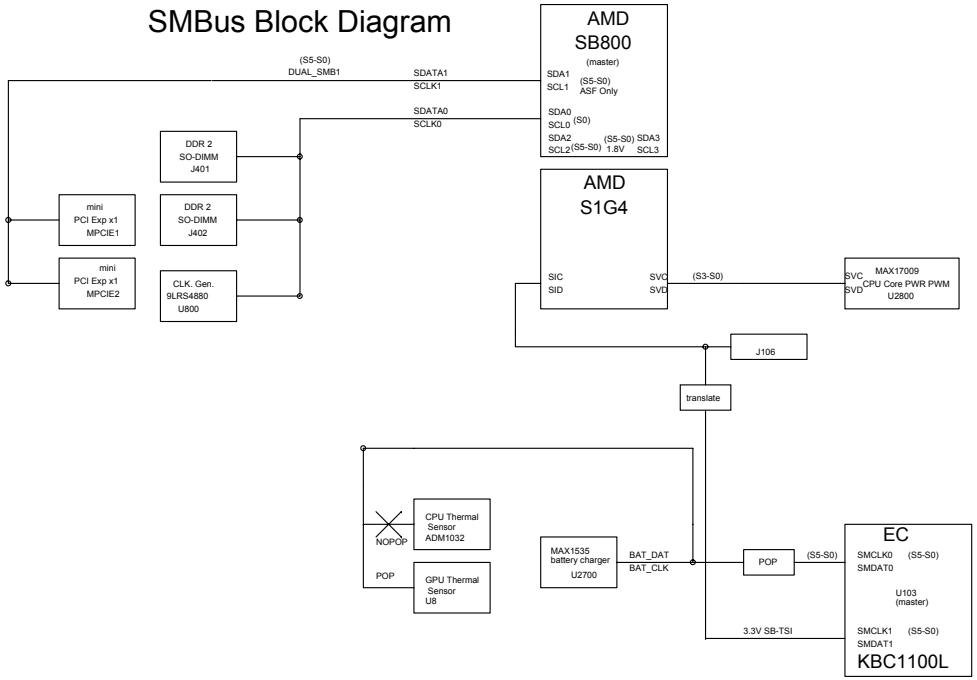
Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)



Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

SMBus Block Diagram



Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description		RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running		ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1		Halt	ON	ON	ON	ON	ON
G0	S0	C2		Stop grant, caches snoopable	ON	ON	ON	ON	ON
G0	S0	C3		TBD	ON	ON	ON	ON	ON
G0	S0	c4		TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Sleeping	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF		Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF		Suspend to diskON	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off		ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN		ON	ON	OFF	OFF	OFF
G3		OFF	Mechanical off		ON	OFF	OFF	OFF	OFF

Group Name Description

INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI/NC: DO NOT INSTALL
KBC: Stuff when use external KBC
IMC: Stuff when use internal EC
A11:Resistors marked with "A11" is only for SB800A11 ONLY.

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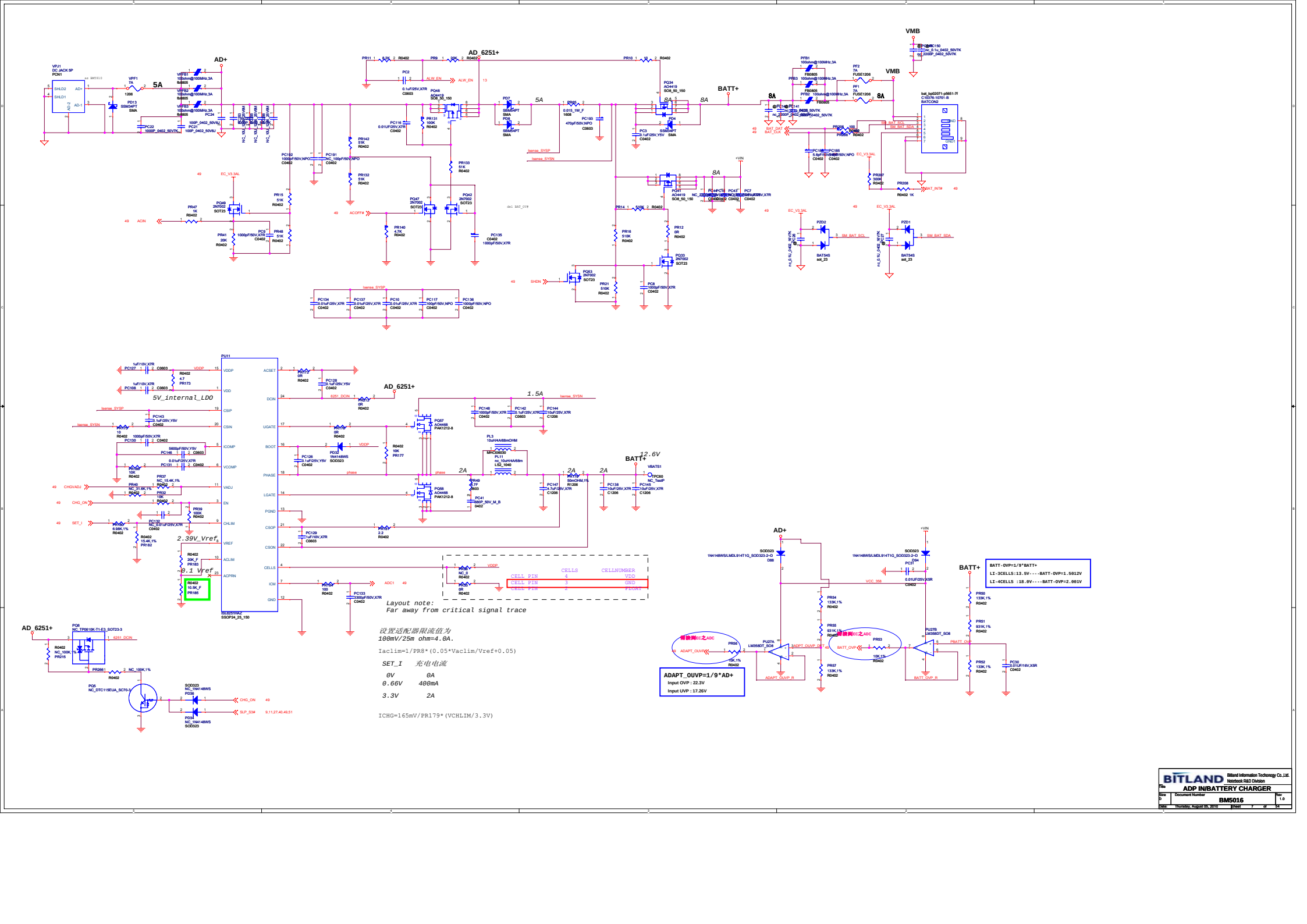
AD+
AD_6251+
VMB
BATT+
5A
8A
1.5A
2A
12.6V
5V_internal_LDO
2.39V_Vref
0.1 Vref
Layout note:
Far away from critical signal trace
設置適配器限流值為
100mV/25m ohm=4.0A.
Iaclim=1/PR8*(0.05*Vaclim/Vref+0.05)
SET_I 充电电流
0V 0A
0.66V 400mA
3.3V 2A
ICHG=165mV/PR179*(VCHLIM/3.3V)
CELL PIN 4 CELLS VDD
CELL PIN 3 CELLS GND
CELL PIN 2 CELLNUMBER FLOAT
BATT-OVP=1/9*BATT+
LI-3CELLS:13.5V----BATT-OVP=1.5012V
LI-4CELLS :18.0V----BATT-OVP=2.001V
ADAPT_OUVP=1/9*AD+
Input OVP : 22.3V
Input UVP : 17.26V
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ADP IN/BATTERY CHARGER
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

ISL6265_QFN_48 6x6

Pin 49 is GND Pin

Panasonic ETQP4LR36WFC

0.7 - 1.3 V 36A

Parallel

Close to CPU socket

Fou Uni-plane:
G16,G17,R39:Assembly
R38:Not Assembly

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Title	CPU CORE PWR	
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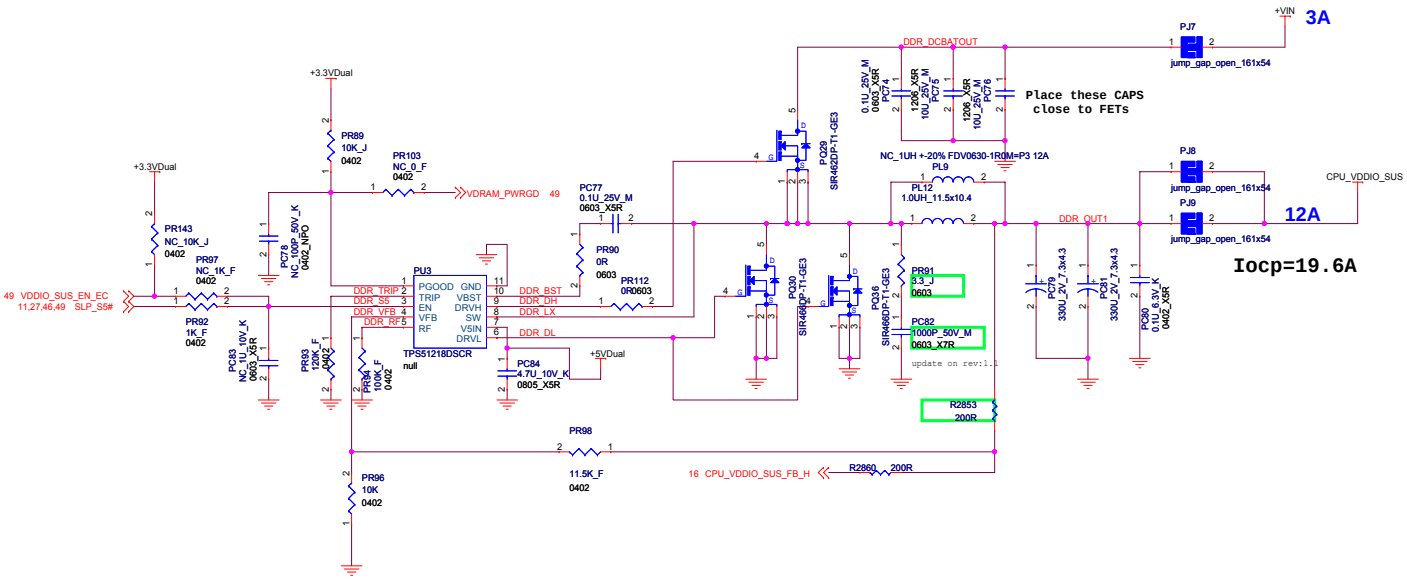

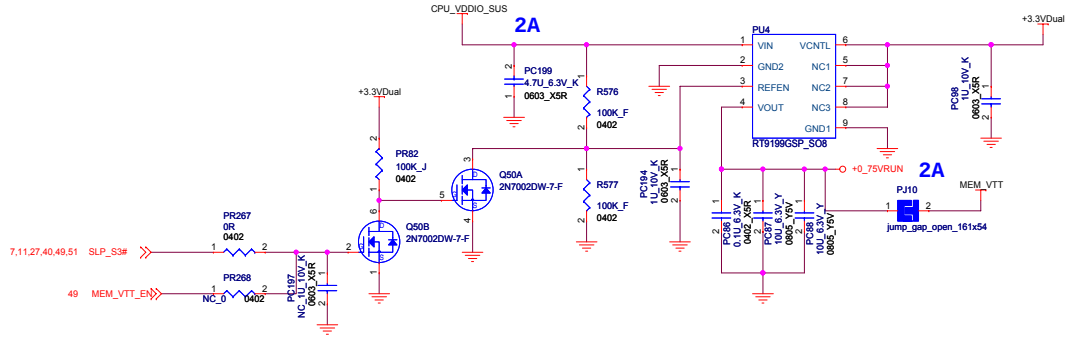

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Title	CPU MEM PWR	
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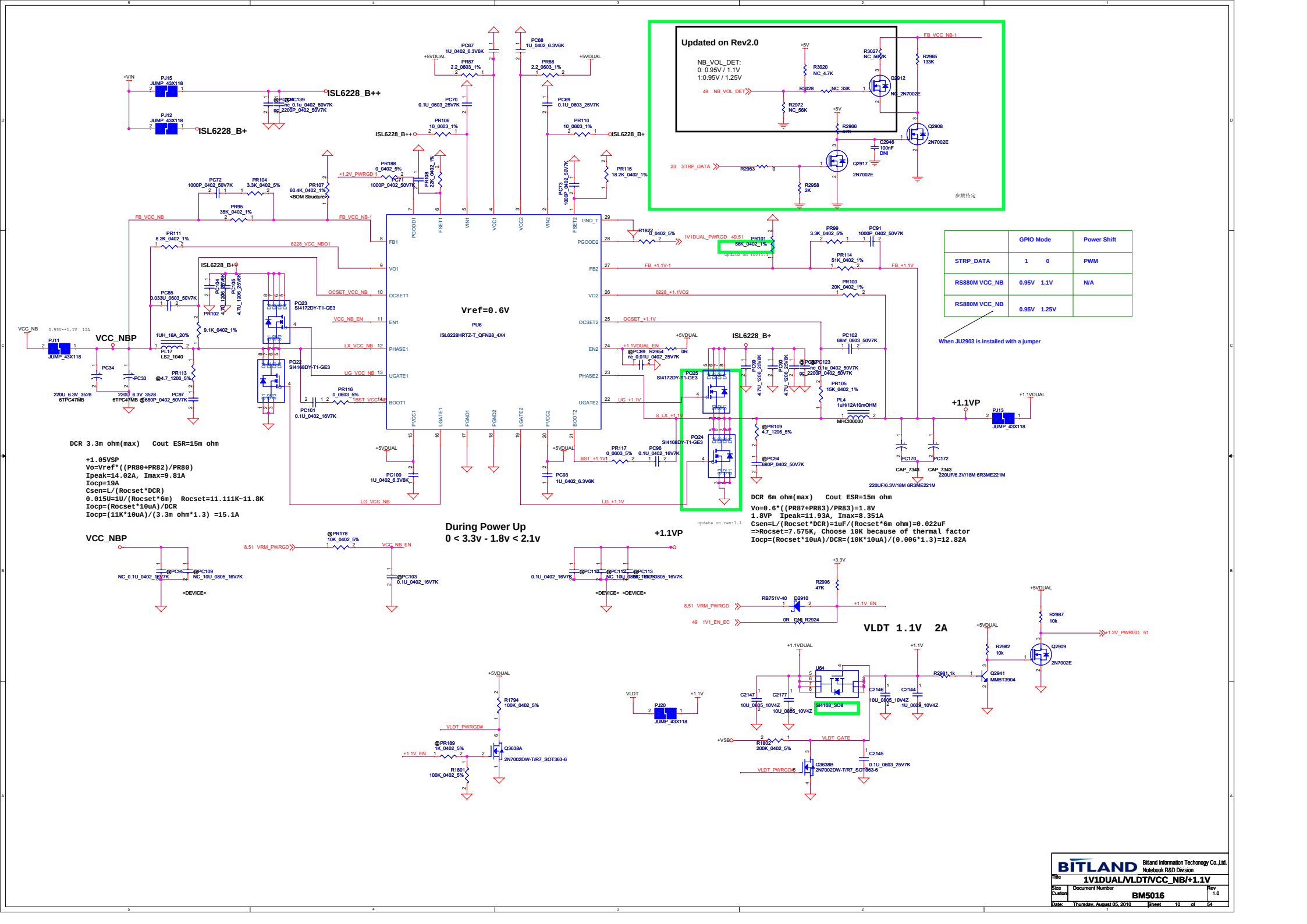

	GPIO Mode		Power Shift
STRP_DATA	1	0	PWM
RS880M VCC_NB	0.95V	1.1V	N/A
RS880M VCC_NB	0.95V	1.25V	

BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division	
Title	1V1DUAL/VLDT/VCC_NB/+1.1V	
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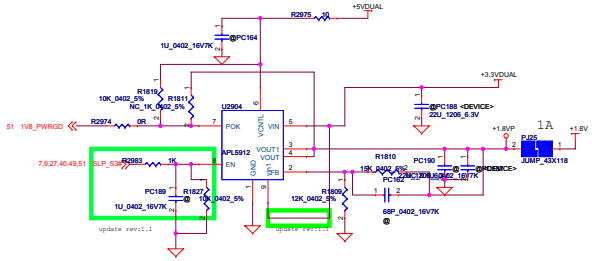
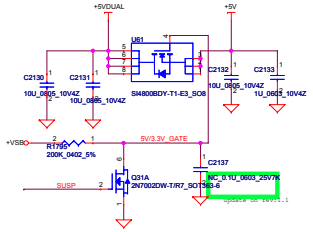
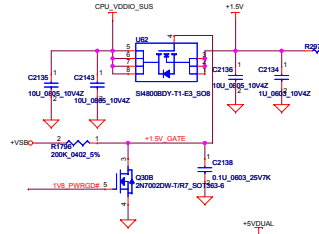
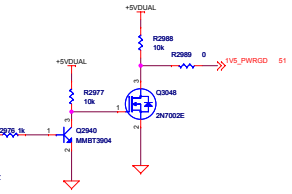


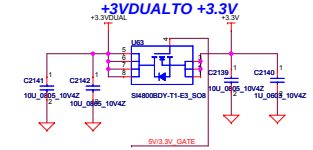
+5DUAL TO +5V

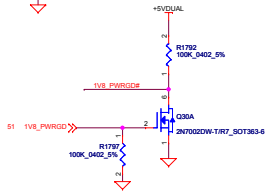


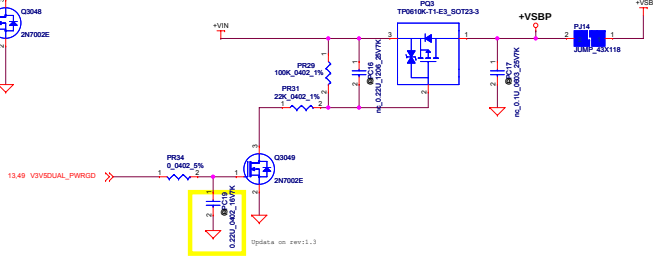


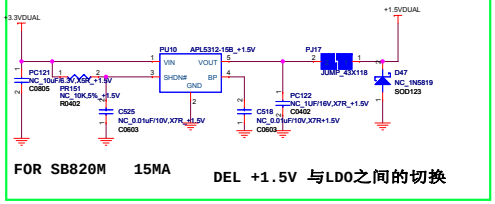


+3VDUALTO +3.3V

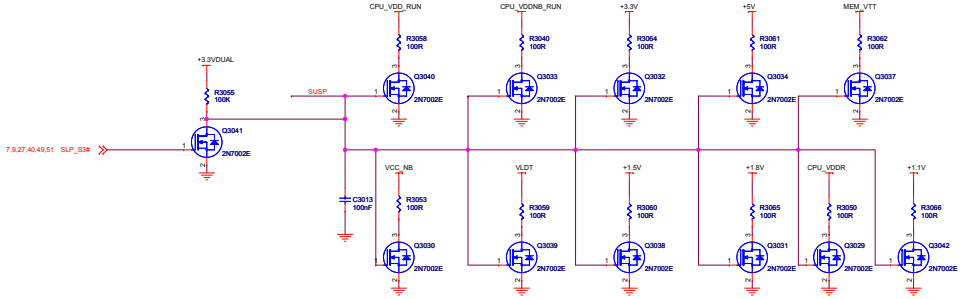


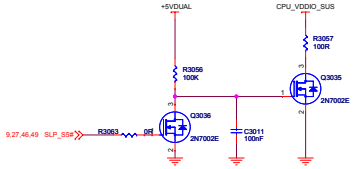






FOR SB820M 15MA **DEL +1.5V 与LDO之间的切换**





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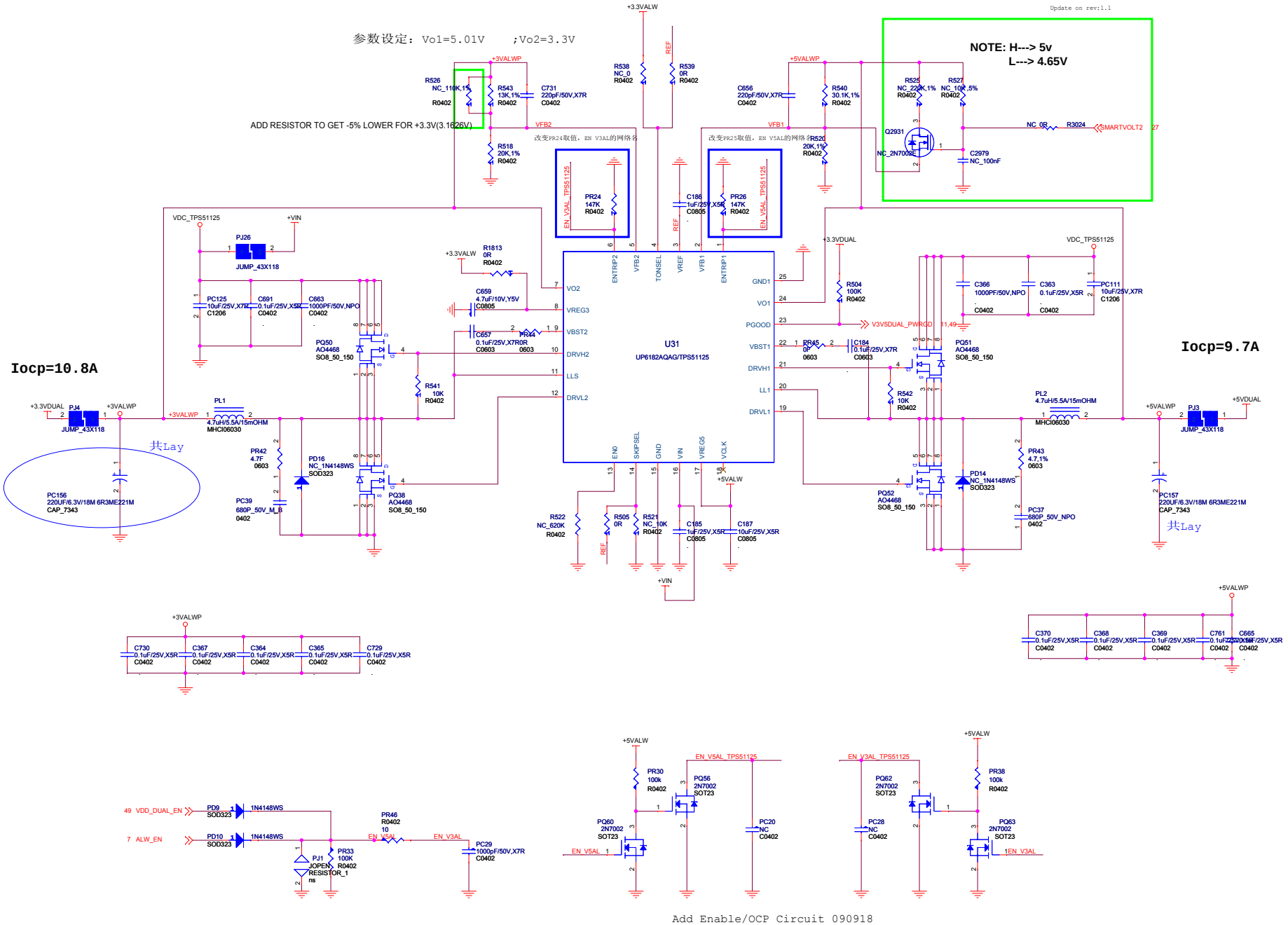

Title	SYSTEM PWR
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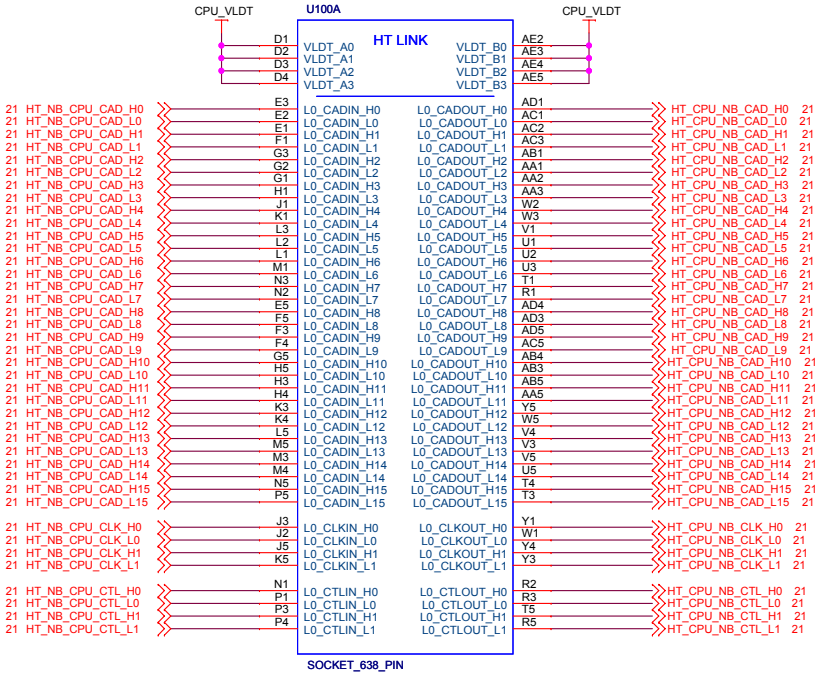
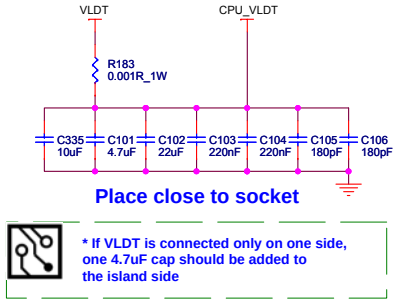
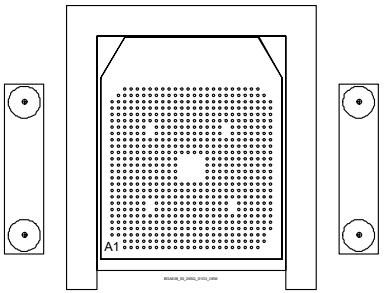
CPU_VLDT 1.1V 1.5A



DEL HTPA Soft-Touch Duo Connectors





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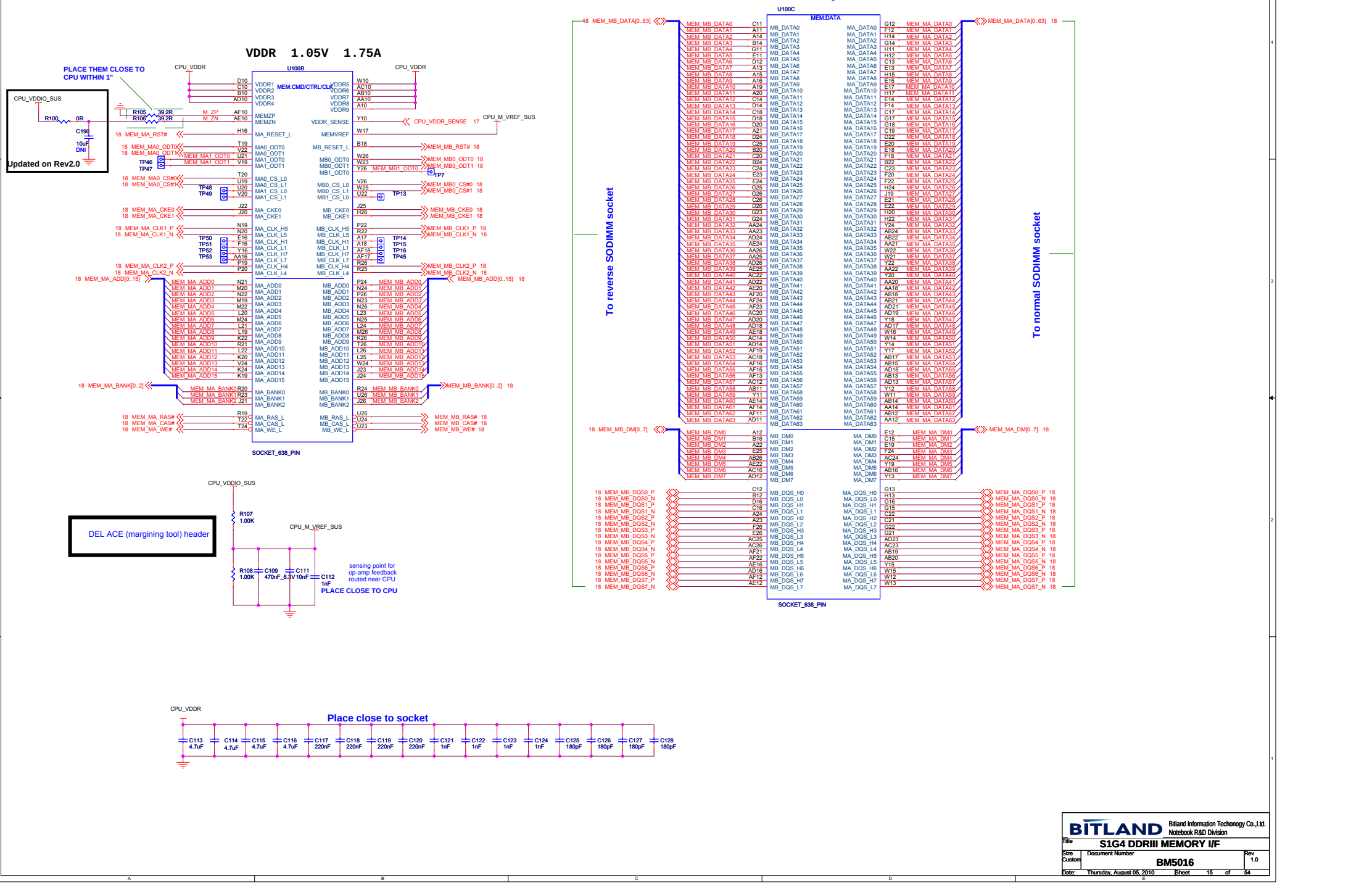
Processor Memory Interface



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Title	S1G4 DDRIII MEMORY I/F	
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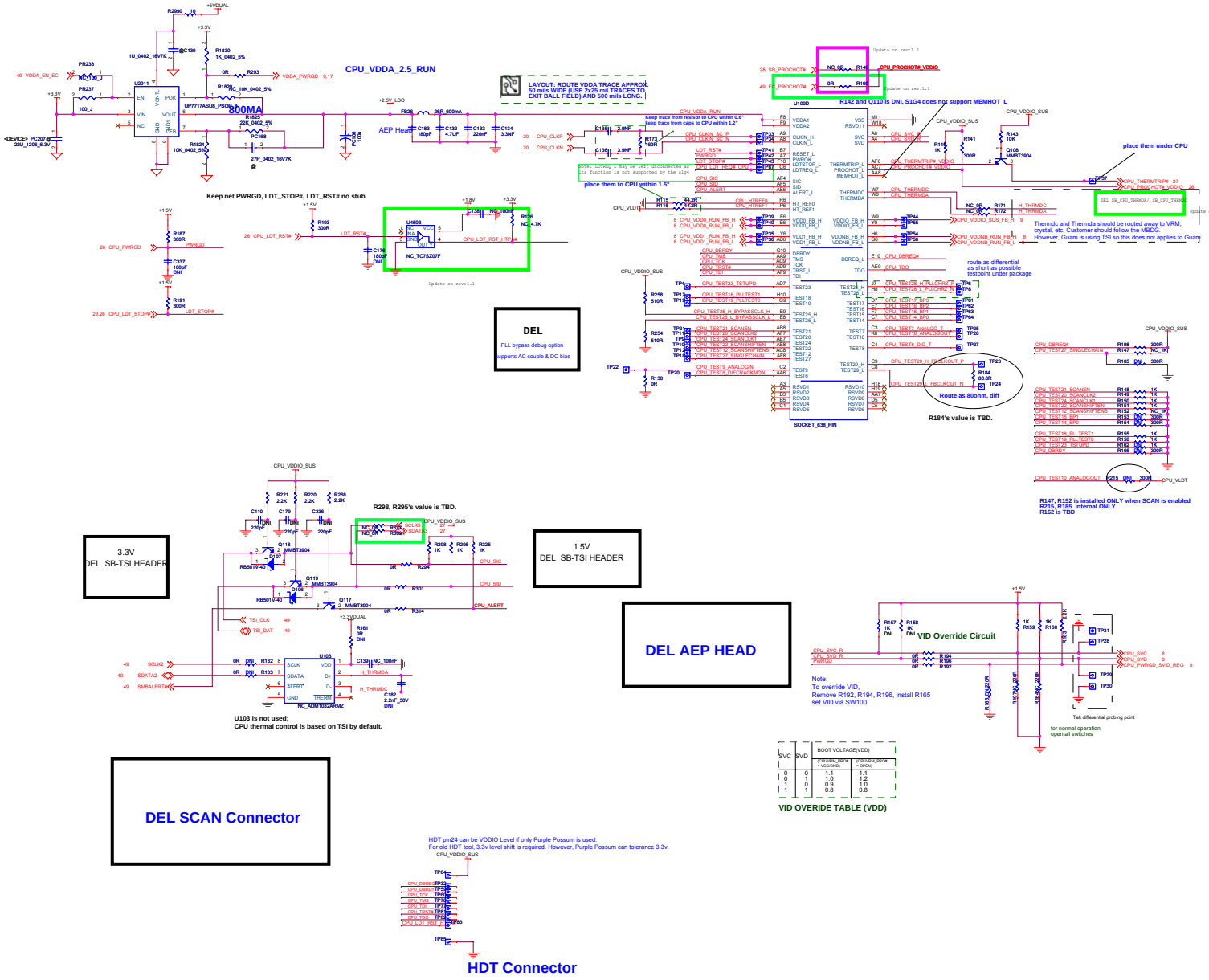

SVC	SVD	BOOT VOLTAGE(VDD)	
		[CPU0/NB_PROP + VCC(NO)]	[CPU0/NB_PROP + OPEN]
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

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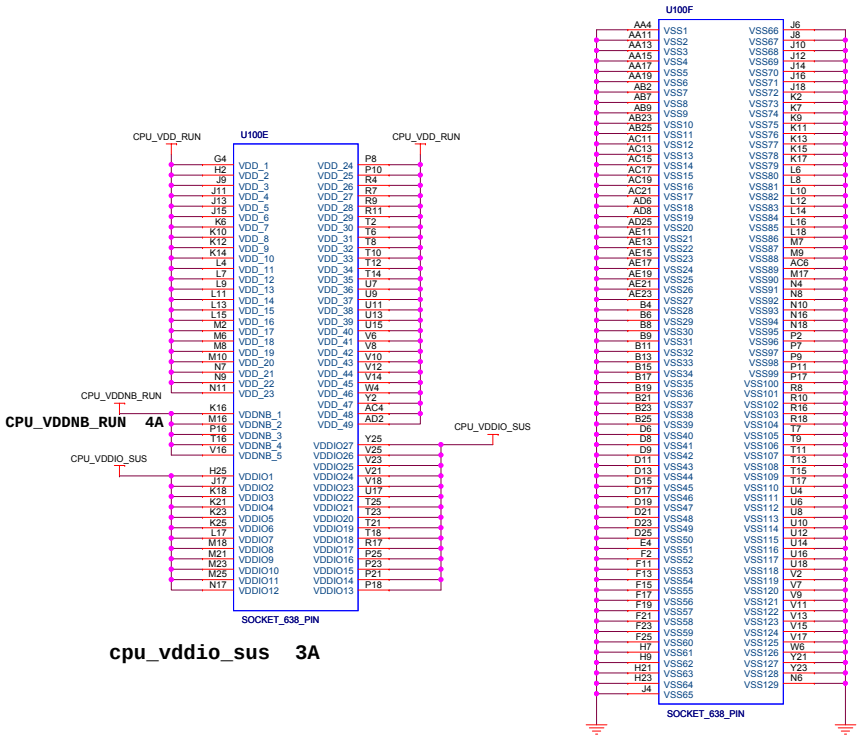
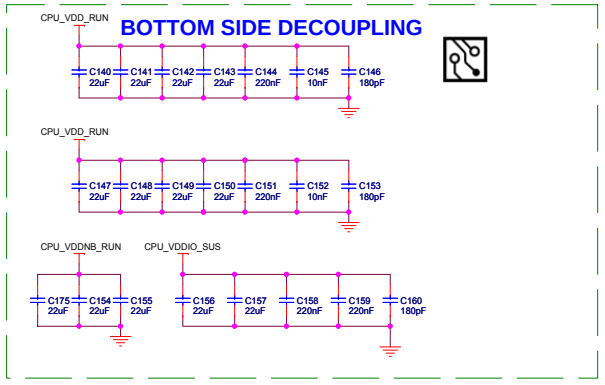
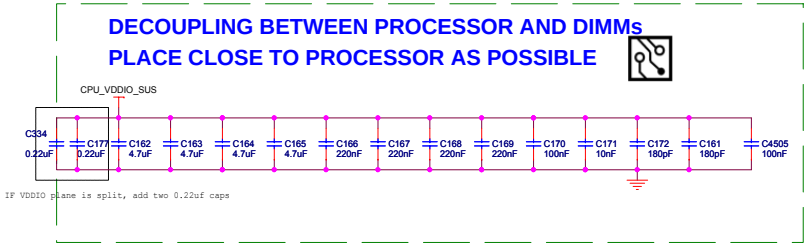
Title: S1G4 CTRL & DEBUG

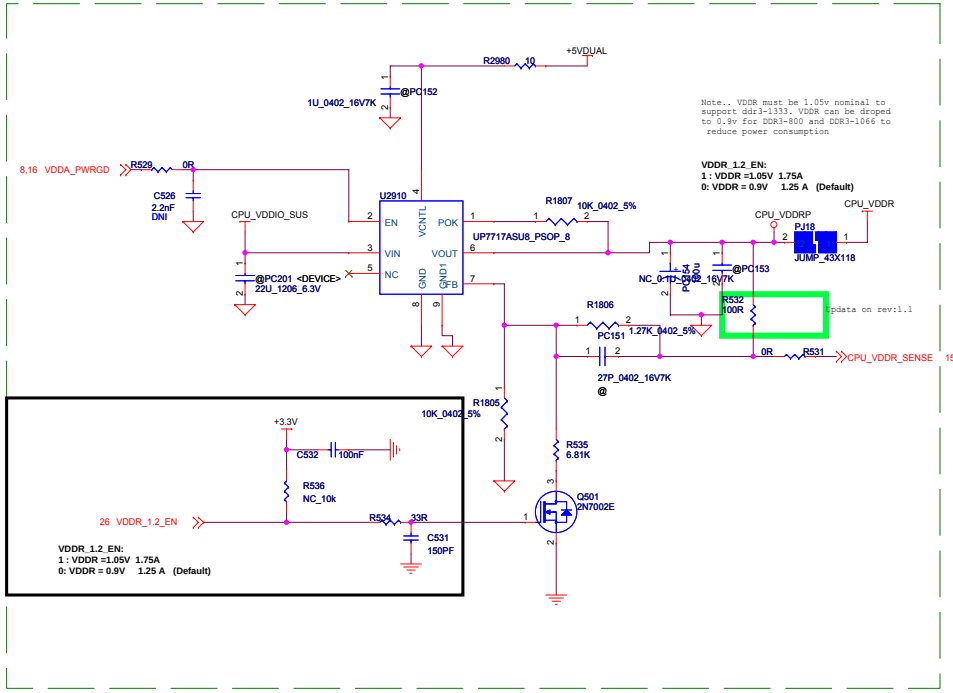
Size: D | Document Number: BM5016 | Rev: 1.0

Date: Thursday, August 05, 2010 | Sheet 16 of 54









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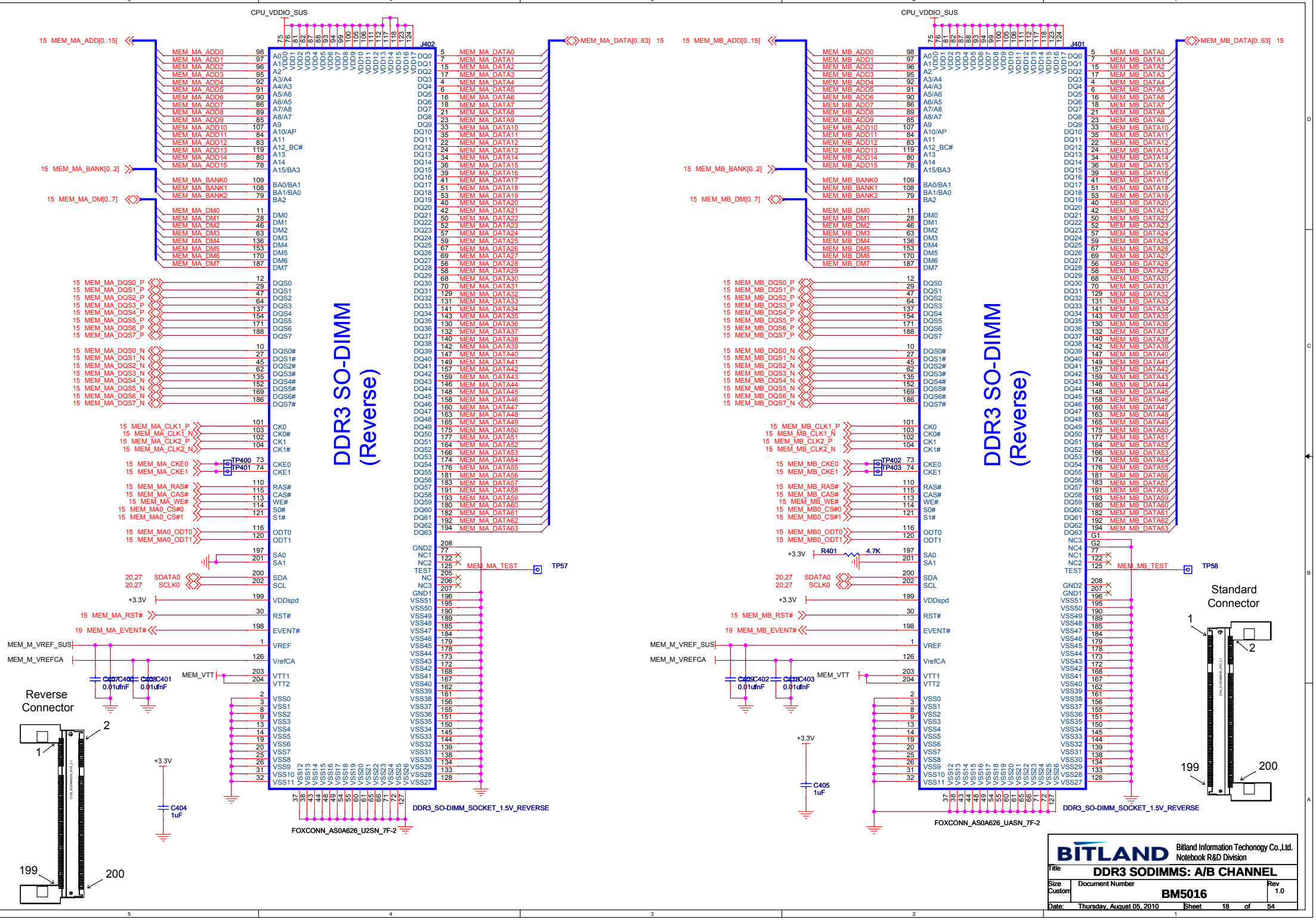
Notebook R&D Division

Title	S1G4 PWR & GND	
Size C	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 17 of 54	


CPU_VDDIO_SUS
J402
DDR3 SO-DIMM (Reverse)
15 MEM_MA_ADD[0..15]
15 MEM_MA_BANK[0..2]
15 MEM_MA_DM[0..7]
15 MEM_MA_DQS0_P
15 MEM_MA_DQS1_P
15 MEM_MA_DQS2_P
15 MEM_MA_DQS3_P
15 MEM_MA_DQS4_P
15 MEM_MA_DQS5_P
15 MEM_MA_DQS6_P
15 MEM_MA_DQS7_P
15 MEM_MA_DQS0_N
15 MEM_MA_DQS1_N
15 MEM_MA_DQS2_N
15 MEM_MA_DQS3_N
15 MEM_MA_DQS4_N
15 MEM_MA_DQS5_N
15 MEM_MA_DQS6_N
15 MEM_MA_DQS7_N
15 MEM_MA_CLK1_P
15 MEM_MA_CLK1_N
15 MEM_MA_CLK2_P
15 MEM_MA_CLK2_N
15 MEM_MA_CKE0
15 MEM_MA_CKE1
15 MEM_MA_RAS#
15 MEM_MA_CAS#
15 MEM_MA_WE#
15 MEM_MA0_CS#0
15 MEM_MA0_CS#1
15 MEM_MA0_ODT0
15 MEM_MA0_ODT1
20,27 SDATA0
20,27 SCLK0
+3.3V
15 MEM_MA_RST#
19 MEM_MA_EVENT#
MEM_M_VREF_SUS
MEM_M_VREFCA
MEM_VTT
C407C400 0.01ufnF
C408C401 0.01ufnF
C404 1uF
TP400
TP401
MEM_MA_TEST
TP57
MEM_MA_DATA[0..63] 15
DDR3_SO-DIMM_SOCKET_1.5V_REVERSE
FOXCONN_AS0A626_U2SN_7F-2
Reverse Connector
1
2
199
200
CPU_VDDIO_SUS
J401
DDR3 SO-DIMM (Reverse)
15 MEM_MB_ADD[0..15]
15 MEM_MB_BANK[0..2]
15 MEM_MB_DM[0..7]
15 MEM_MB_DQS0_P
15 MEM_MB_DQS1_P
15 MEM_MB_DQS2_P
15 MEM_MB_DQS3_P
15 MEM_MB_DQS4_P
15 MEM_MB_DQS5_P
15 MEM_MB_DQS6_P
15 MEM_MB_DQS7_P
15 MEM_MB_DQS0_N
15 MEM_MB_DQS1_N
15 MEM_MB_DQS2_N
15 MEM_MB_DQS3_N
15 MEM_MB_DQS4_N
15 MEM_MB_DQS5_N
15 MEM_MB_DQS6_N
15 MEM_MB_DQS7_N
15 MEM_MB_CLK1_P
15 MEM_MB_CLK1_N
15 MEM_MB_CLK2_P
15 MEM_MB_CLK2_N
15 MEM_MB_CKE0
15 MEM_MB_CKE1
15 MEM_MB_RAS#
15 MEM_MB_CAS#
15 MEM_MB_WE#
15 MEM_MB0_CS#0
15 MEM_MB0_CS#1
15 MEM_MB0_ODT0
15 MEM_MB0_ODT1
R401 4.7K
20,27 SDATA0
20,27 SCLK0
+3.3V
15 MEM_MB_RST#
19 MEM_MB_EVENT#
MEM_M_VREF_SUS
MEM_M_VREFCA
MEM_VTT
C409C402 0.01ufnF
C410C403 0.01ufnF
C405 1uF
TP402
TP403
MEM_MB_TEST
TP58
MEM_MB_DATA[0..63] 15
DDR3_SO-DIMM_SOCKET_1.5V_REVERSE
FOXCONN_AS0A626_UASN_7F-2
Standard Connector
1
2
199
200
BITLAND
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Notebook R&D Division
Title
DDR3 SODIMMS: A/B CHANNEL
Size
Custom
Document Number
BM5016
Rev
1.0
Date: Thursday, August 05, 2010
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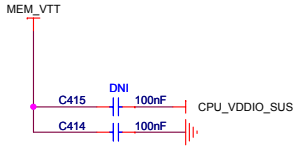
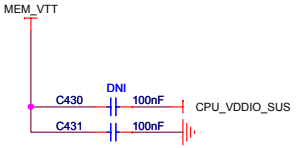
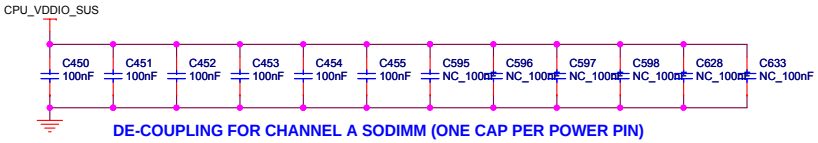


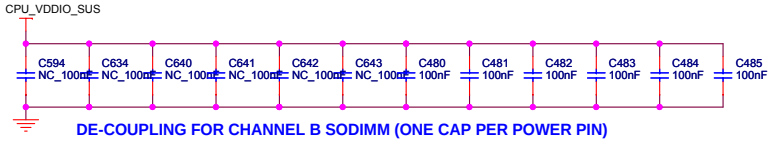
DE-COUPLING FOR CHANNEL A SODIMM



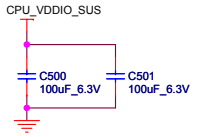
DE-COUPLING FOR CHANNEL B SODIMM

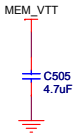


DE-COUPLING FOR CHANNEL A SODIMM (ONE CAP PER POWER PIN)

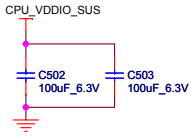


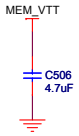
DE-COUPLING FOR CHANNEL B SODIMM (ONE CAP PER POWER PIN)

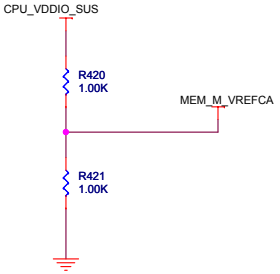




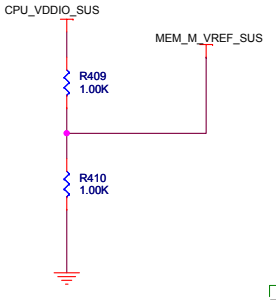
LAYOUT: PLACE CLOSE TO DIMMs



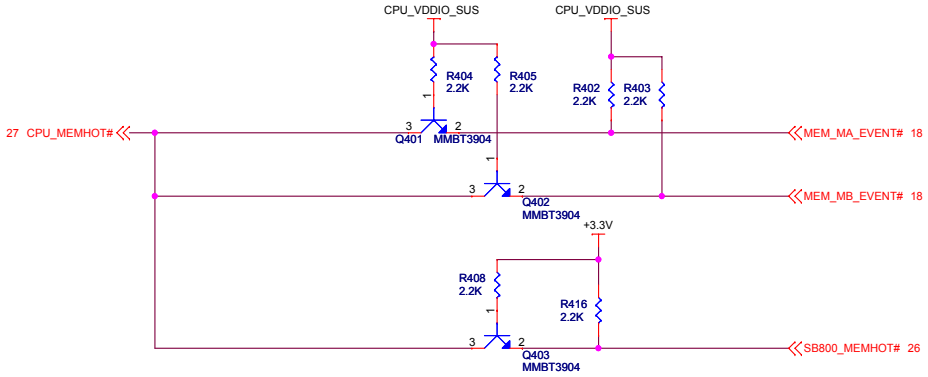




MEM_VREF_SUS

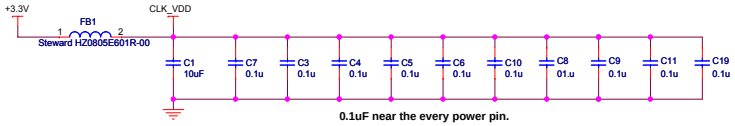


LAYOUT: PLACE CLOSE TO DIMMs



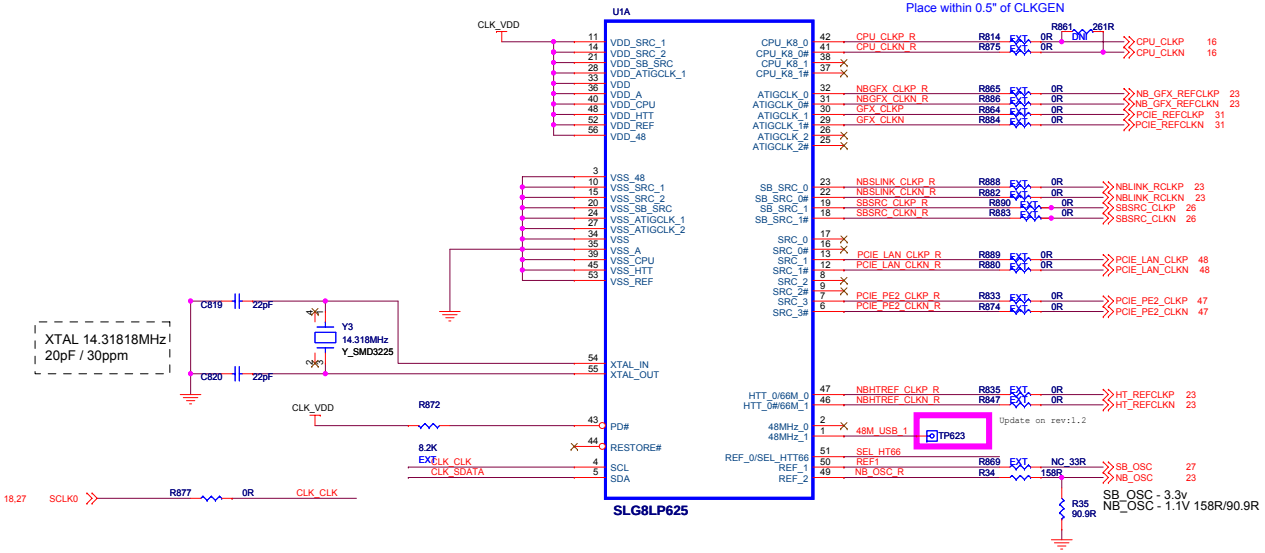
BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title	DDR3 SODIMM DECOUPLING	
Size: Custom	Document Number: BM5016	Rev: 1.0
Date: Thursday, August 05, 2010	Sheet 19 of 54	



0.1uF near the every power pin.

Place within 0.5" of CLKGEN



SB_OSC - 3.3v
NB_OSC - 1.1V 158R/90.9R

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

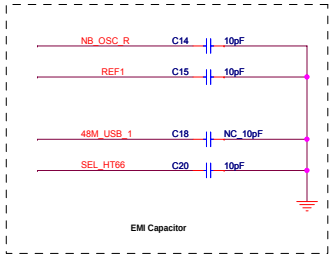
NB CLOCK INPUT TABLE

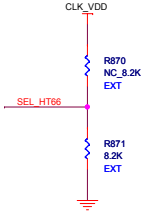
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

R34/R35 (value may change)

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 33R/43R
RS780	1.1V 200R/100R





SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

* default

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Notebook R&D Division

Title: EXTERNAL CLOCK GENERATOR

Size	Document Number	Rev
C	BM5016	1.0

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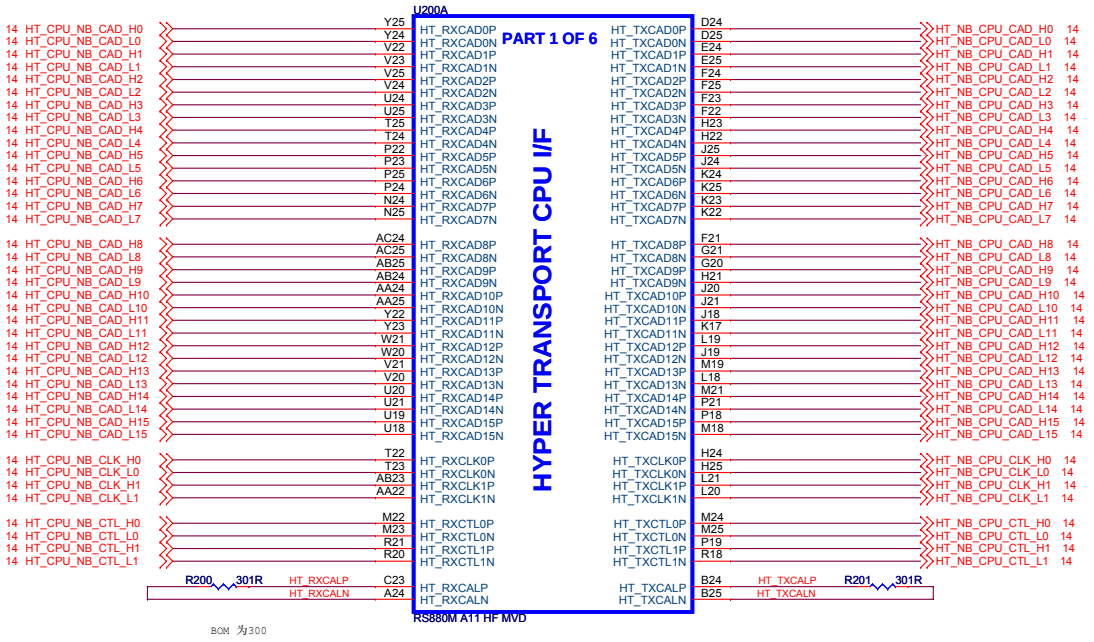
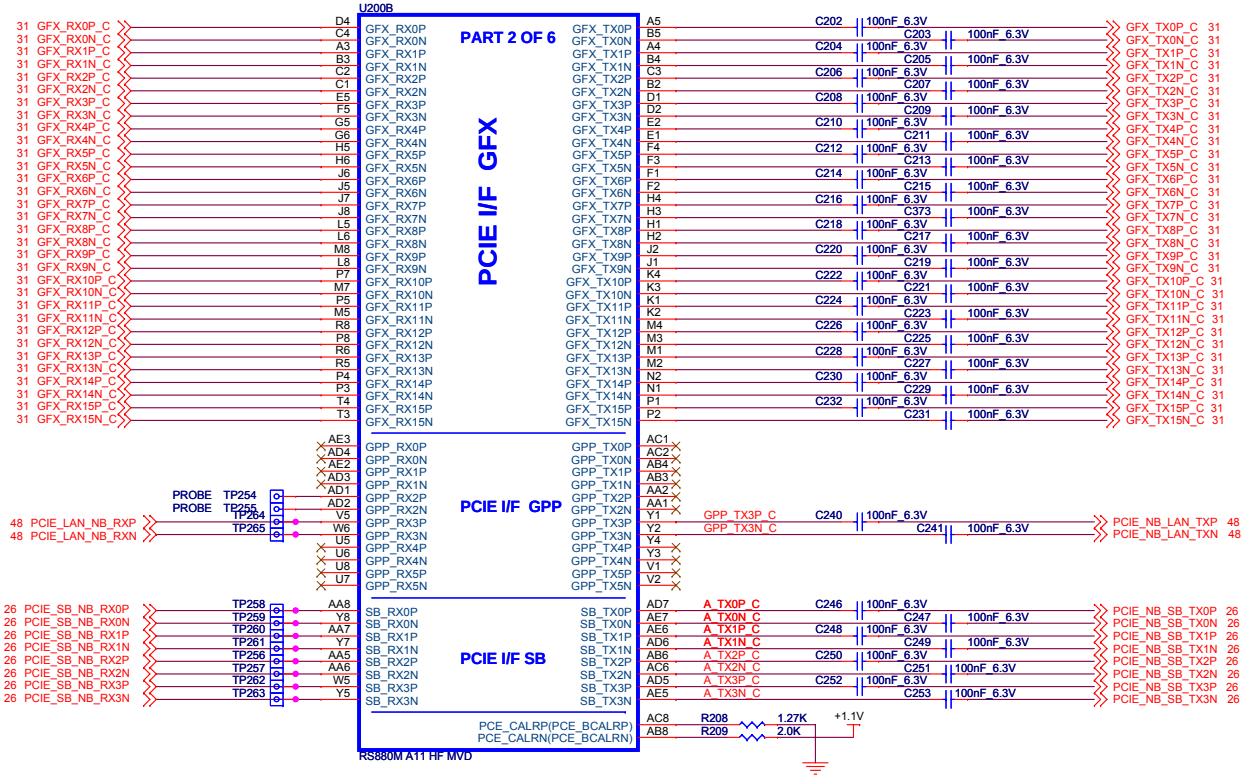


DEL HTPA PROBE CONNECTOR FOR DEBUG(NB SIDE)

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	RS880M-HT LINK I/F	
Size: Custom	Document Number: BM5016	Rev: 1.0
Date: Thursday, August 05, 2010	Sheet 21 of 54	

MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot

MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



DEL header_1x3

Keep the impendance of PCIE lane to 85ohm +/-15%
Including the A-link

All PCIe lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.

DEL PCIE MIDDLE BUS PROBE FOR DEBUG

RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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Title	RS880M-PCIE I/F	
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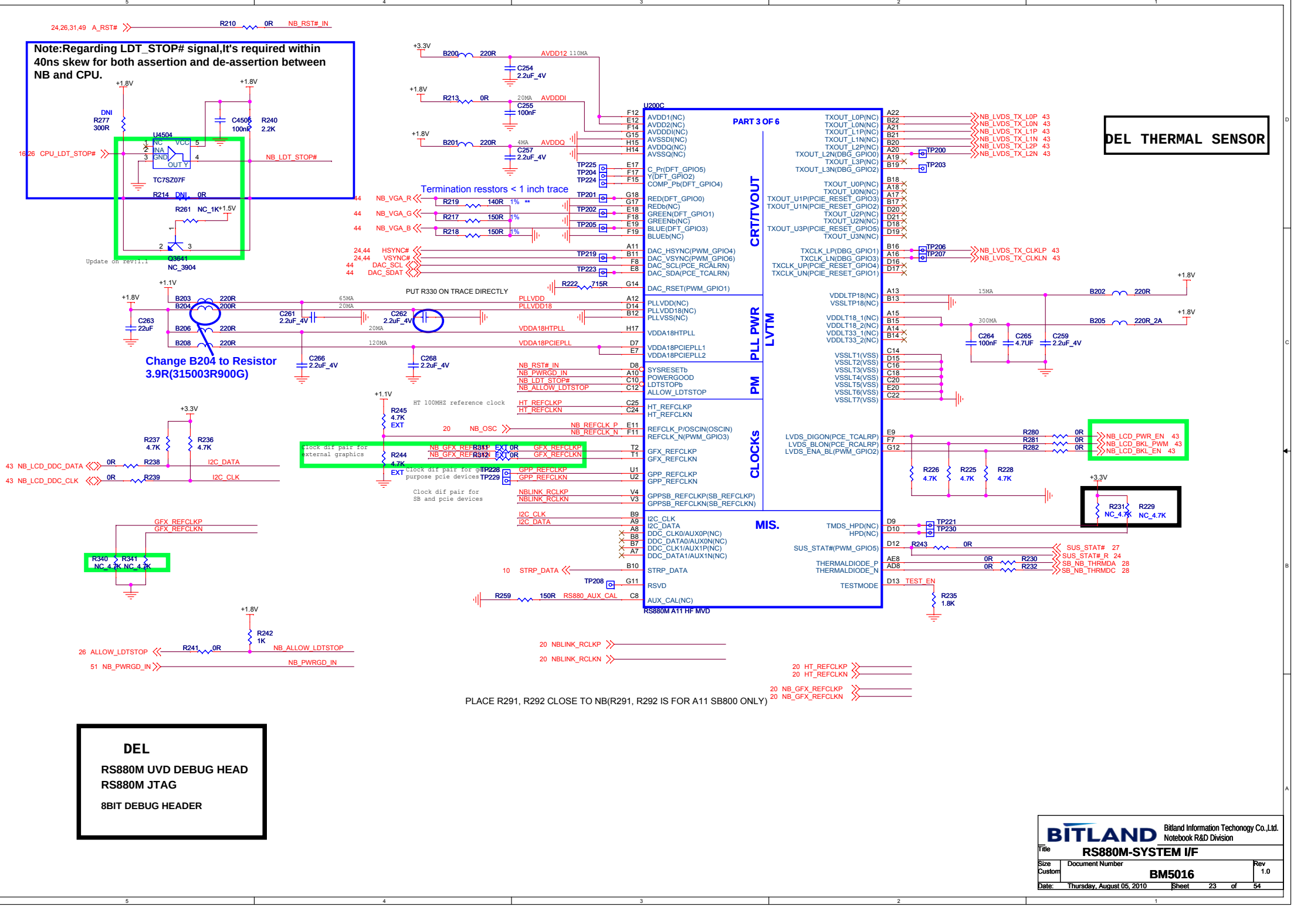
Note:Regarding LDT_STOP# signal,It's required within 40ns skew for both assertion and de-assertion between NB and CPU.
DEL THERMAL SENSOR
Termination resstors < 1 inch trace
Change B204 to Resistor 3.9R(315003R900G)
PUT R330 ON TRACE DIRECTLY
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.
RS880M A11 HF MVD
PLACE R291, R292 CLOSE TO NB(R291, R292 IS FOR A11 SB800 ONLY)
DEL
RS880M UVD DEBUG HEAD
RS880M JTAG
8BIT DEBUG HEADER
BITLAND
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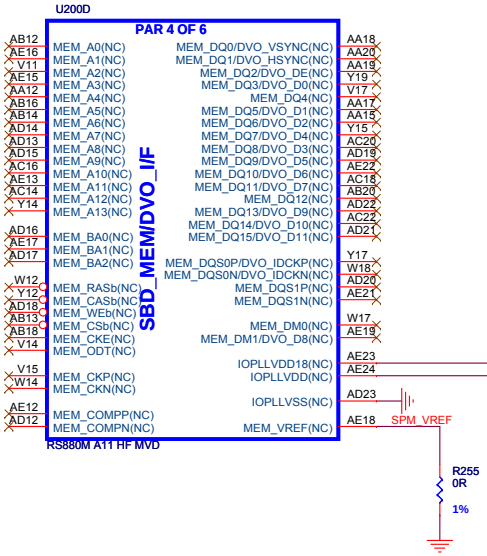
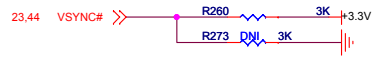
Notebook R&D Division
RS880M-SYSTEM I/F
BM5016
Thursday, August 05, 2010



DEL U202

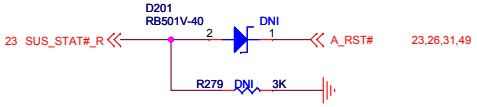
DEL SDRAM DDR3



STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

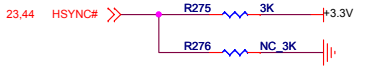
RS880M	
1 Disable	
0 Enable	



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

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Notebook R&D Division

Title	RS880M-SPMEM/STRAPS	
Size: Custom	Document Number: BM5016	Rev: 1.0
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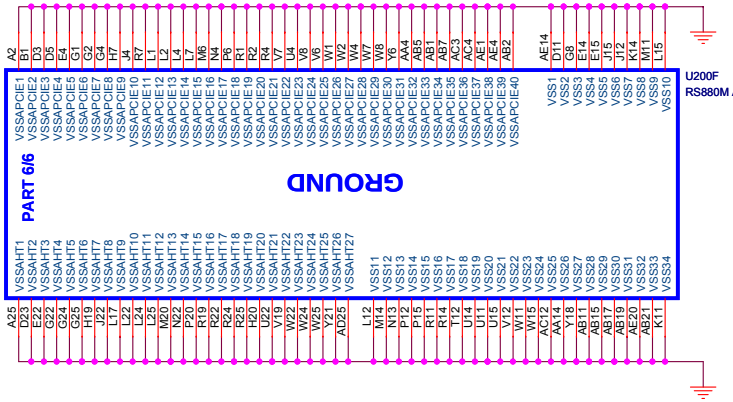
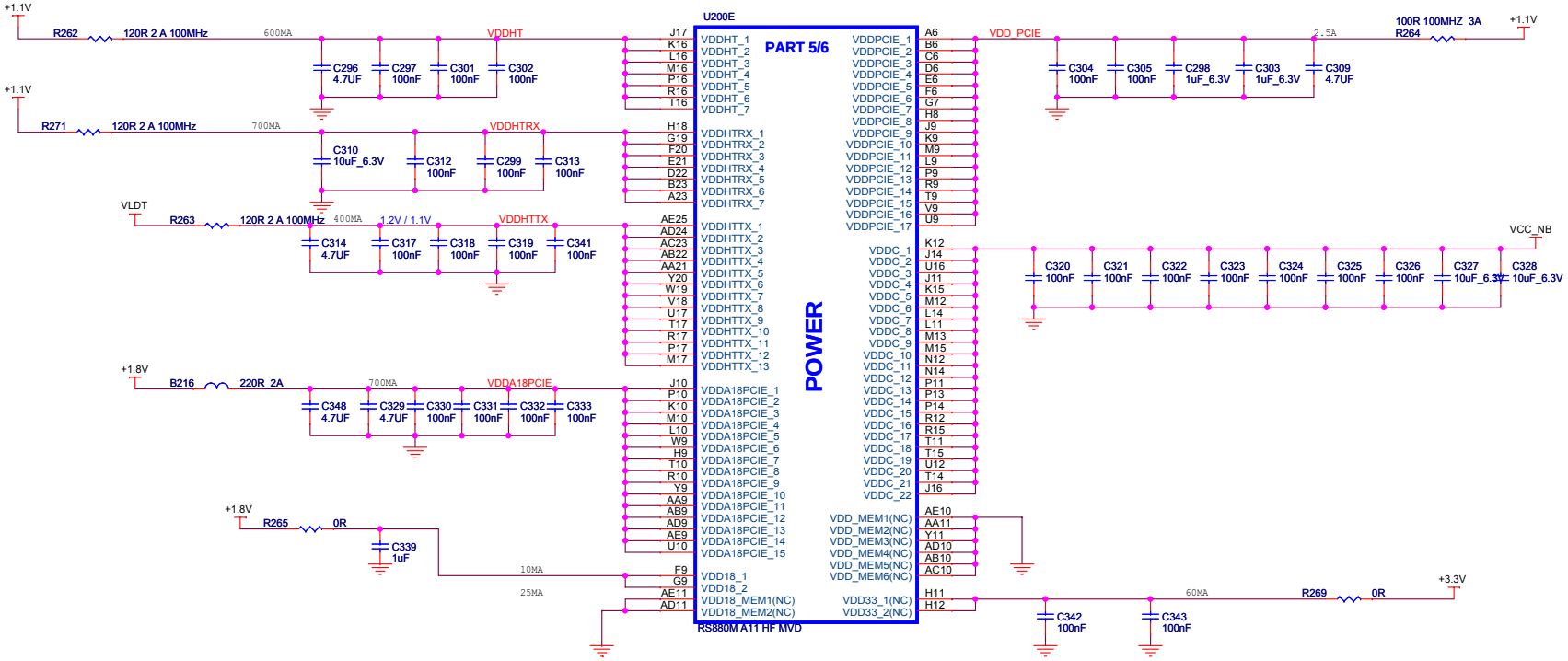


RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC



DEL FAN CIRCUIT

BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title	RS880M-POWER	
Size: Custom	Document Number: BM5016	Rev: 1.0
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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

J613 CLOSE TO U600

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED.

NOTE: The 0R serial resistor on SB CLK pair must share Pad with the serial resistor close to U800

FOR EXT GRAPHICS

FOR WIFI

FOR LAN

Updated on Rev2.0

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Update on rev:1.1

SB_GPP GFX_CLK	DEVICE MXM3.0	CLKREQ# CLK_REQG#
0	//	0
1	PE0	1
2	PE2	2
3	LAN	3
4	PE1	4
5	//	5
6	PE3	6
7	//	7
8	//	8

SB800 Part 1 of 5

SB800 A11

Update on rev:1.2

Update on rev:1.1

Updated on Rev2.0

FOR BIOS AUTO DETECTION(GUAM V.S. BIMINI)

FOR CMOS CLEAR

TEST PURPOSE ONLY

POWER EXPRESS SUPPORT

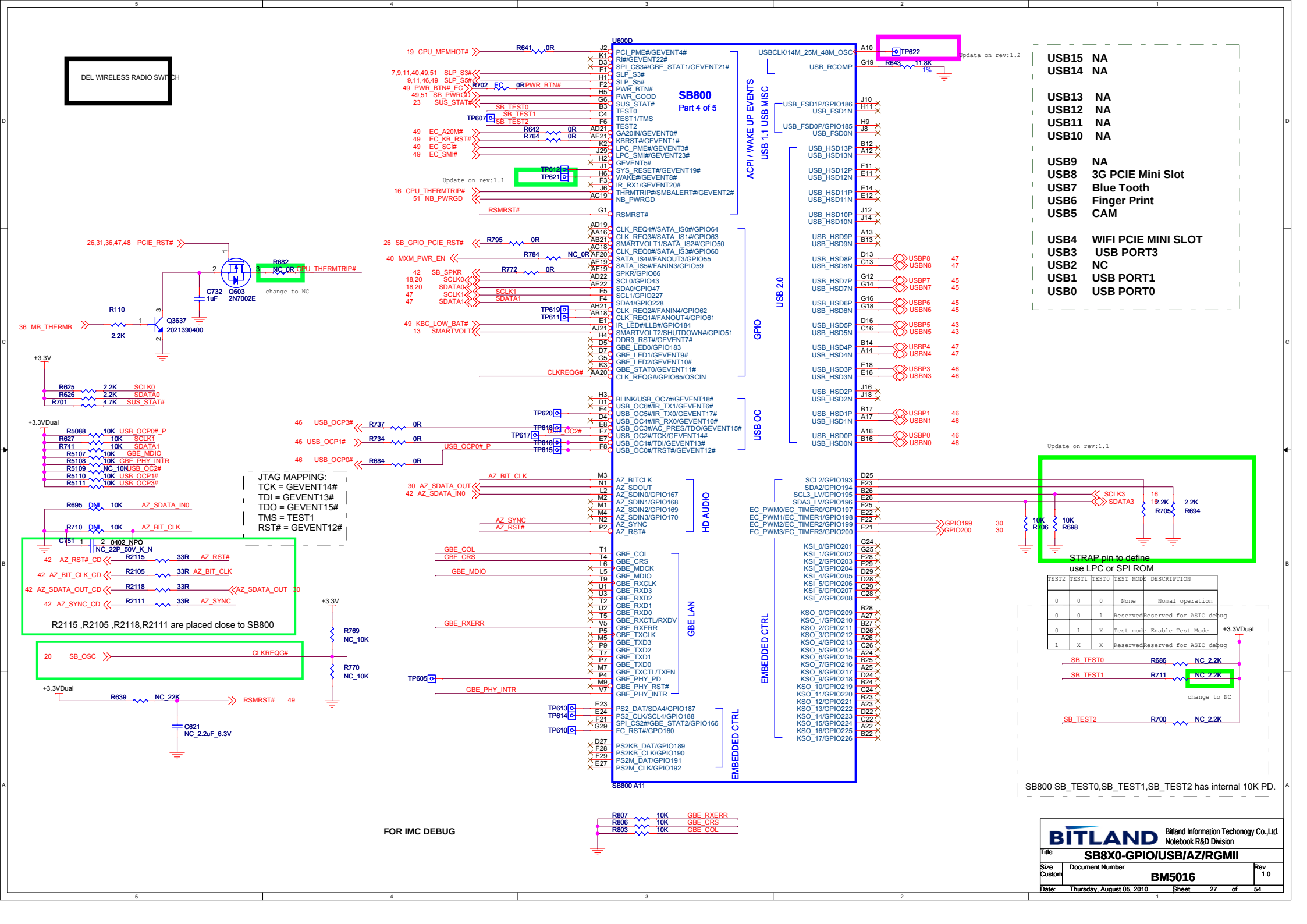
PE_GPIO0 MXM RESET	H: Enable
PE_GPIO1 MXM POWER ENABLE	H: Enable
PE_GPIO2 MODE SWITCH(BY NB)	H:MXM L:NB
TMDS_HPD0 MXM HOT PLUG	

BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division

Title: SB8X0-PCIE/PCI/CPU/LPC/CLK

Size: Custom | Document Number: BM5016 | Rev: 1.0

Date: Thursday, August 05, 2010 | Sheet 26 of 54


DEL WIRELESS RADIO SWITCH
SB800
Part 4 of 5
U600D
SB800 A11
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL
PCI_PME#/GEVENT4#
R#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
Update on rev:1.1
Update on rev:1.2
change to NC
JTAG MAPPING:
TCK = GEVENT14#
TDI = GEVENT13#
TDO = GEVENT15#
TMS = TEST1
RST# = GEVENT12#
R2115 ,R2105 ,R2118,R2111 are placed close to SB800
STRAP pin to define
use LPC or SPI ROM
TEST2 TEST1 TEST0 TEST MODE DESCRIPTION
0 0 0 None Nomal operation
0 0 1 Reserved Reserved for ASIC debug
0 1 X Test mode Enable Test Mode
1 X X Reserved Reserved for ASIC debug
SB800 SB_TEST0,SB_TEST1,SB_TEST2 has internal 10K PD.
FOR IMC DEBUG
USB15 NA
USB14 NA
USB13 NA
USB12 NA
USB11 NA
USB10 NA
USB9 NA
USB8 3G PCIE Mini Slot
USB7 Blue Tooth
USB6 Finger Print
USB5 CAM
USB4 WIFI PCIE MINI SLOT
USB3 USB PORT3
USB2 NC
USB1 USB PORT1
USB0 USB PORT0
BITLAND
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Notebook R&D Division
Title
SB8X0-GPIO/USB/AZ/RGMII
Size Custom
Document Number
BM5016
Rev 1.0
Date: Thursday, August 05, 2010
Sheet 27 of 54

SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

FOR SATA HD

FOR SATA ODD

SATA PORTS DISTRIBUTION:
0, - 2.5 INCH DISK DRIVER
1, SATA ODD
2,NOT USED
3, NOT USED
4 & 5, NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

To meet SB800 SCL1.02: DNI SATA XTAL circuit's parts

U600B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB800 A11

Connect C7 and D8, then go to GND directly.

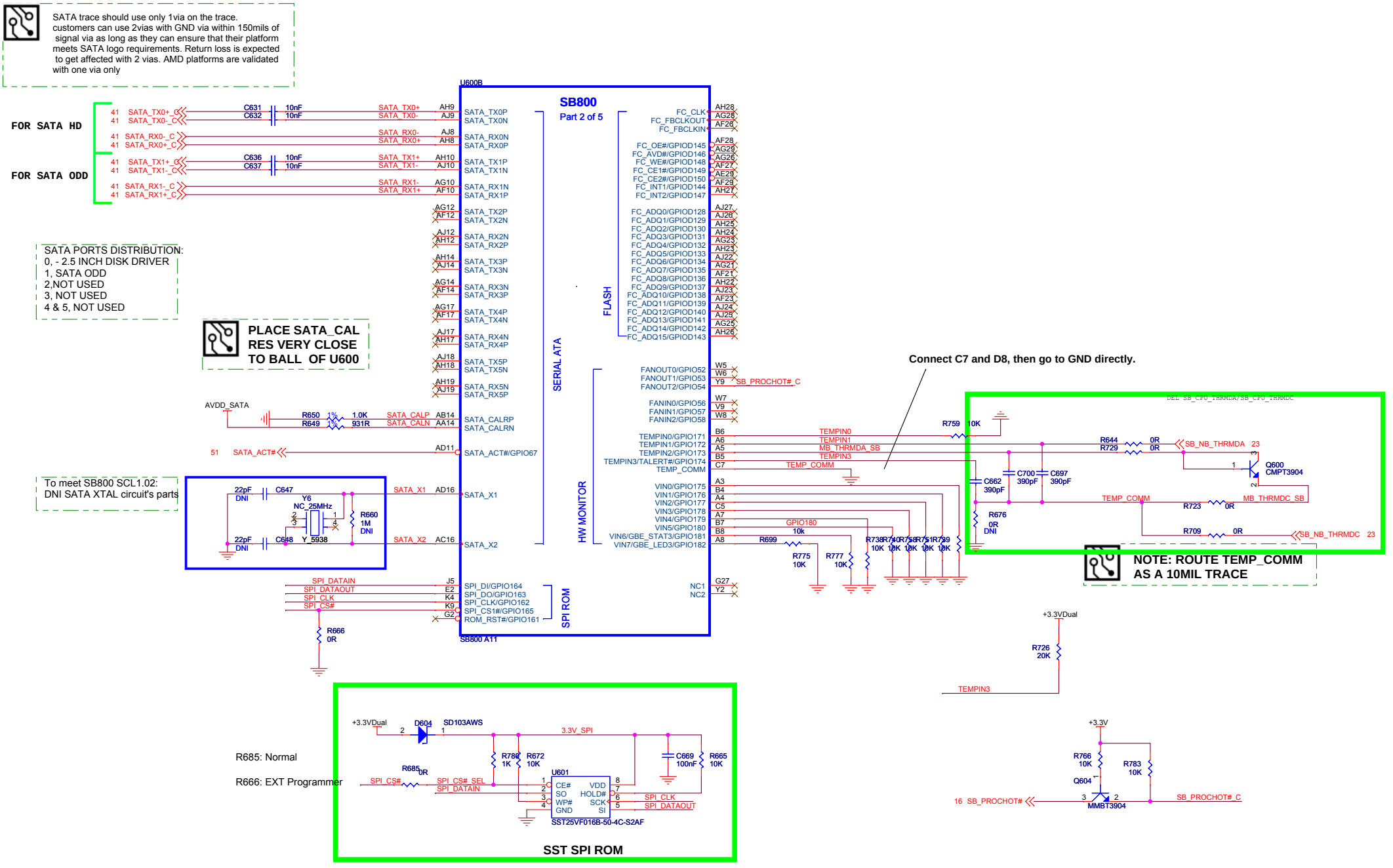
NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE

R685: Normal

R666: EXT Programmer

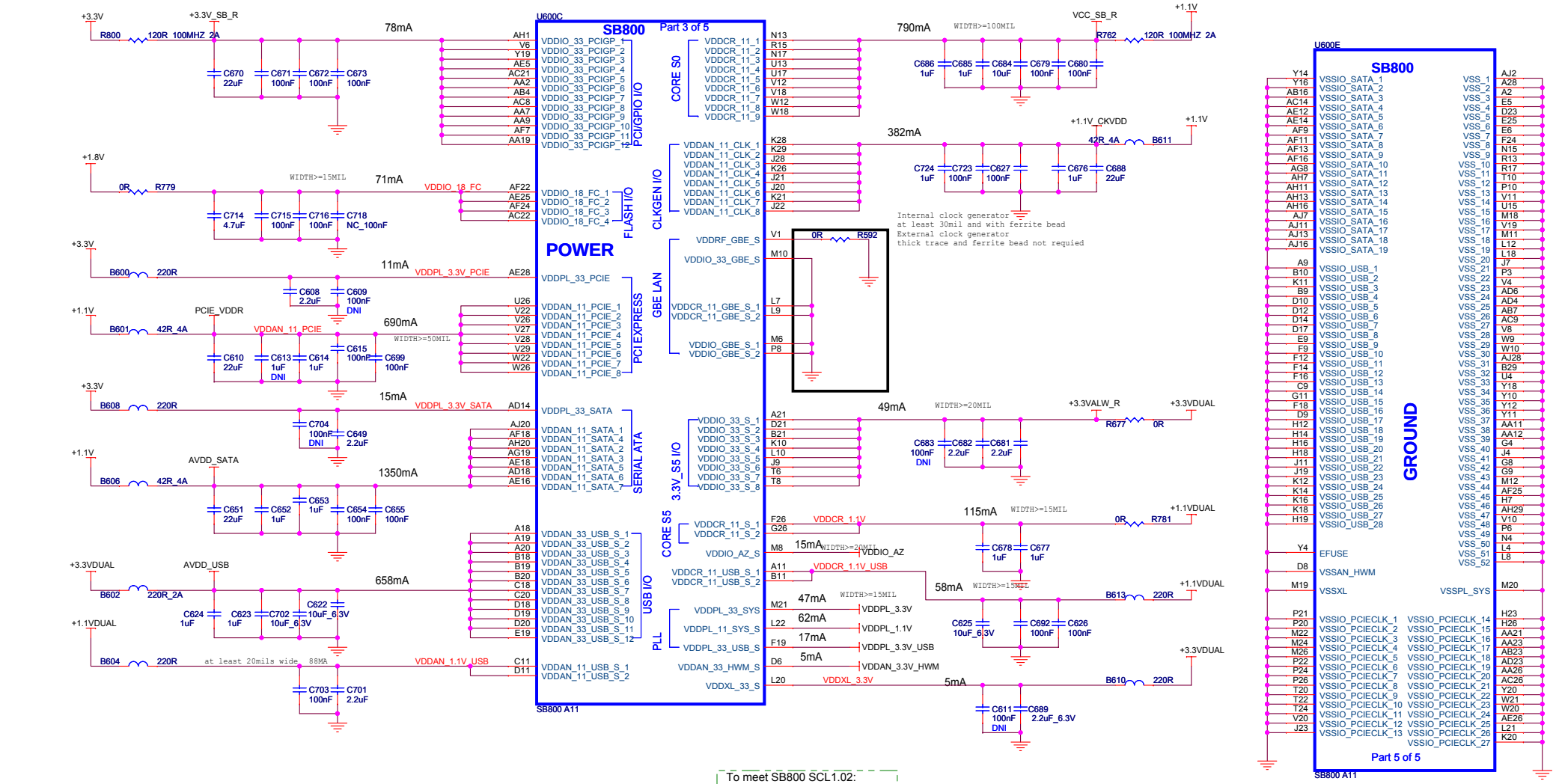
SST SPI ROM

change to SPI mode



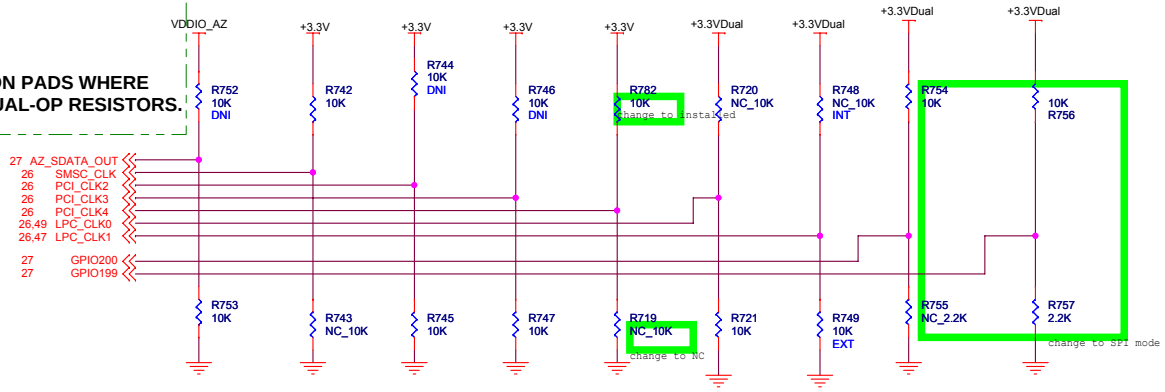
Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	SB8X0-SATA/IDE/HWM/SPI
Size: Custom	Document Number: BM5016
Rev	1.0
Date: Thursday, August 05, 2010	Sheet 28 of 54

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



Bitland Information Techonogy Co.,Ltd.	Notebook R&D Division
Title	SB8X0-POWER & DECOUPLING
Size: Custom	Document Number: BM5016
Rev	1.0
Date: Thursday, August 05, 2010	Sheet 29 of 54

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



DEL JTAG HEADER

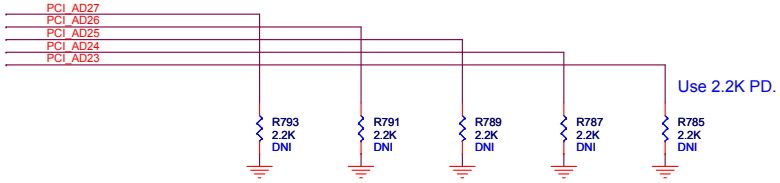
REQUIRED STRAPS

	AZ_SDOUT	SMSC_CLK	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

26 PCI_AD[27..23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

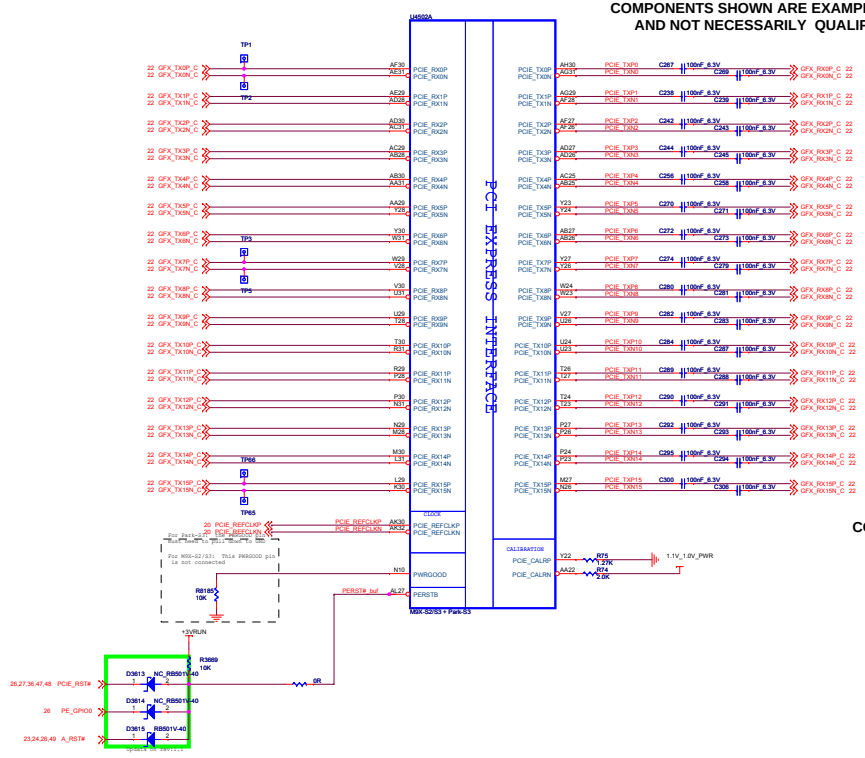
BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division

Title: SB8X0-STRAPS

Size: Custom | Document Number: BM5016 | Rev: 1.0

Date: Thursday, August 05, 2010 | Sheet 30 of 54

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



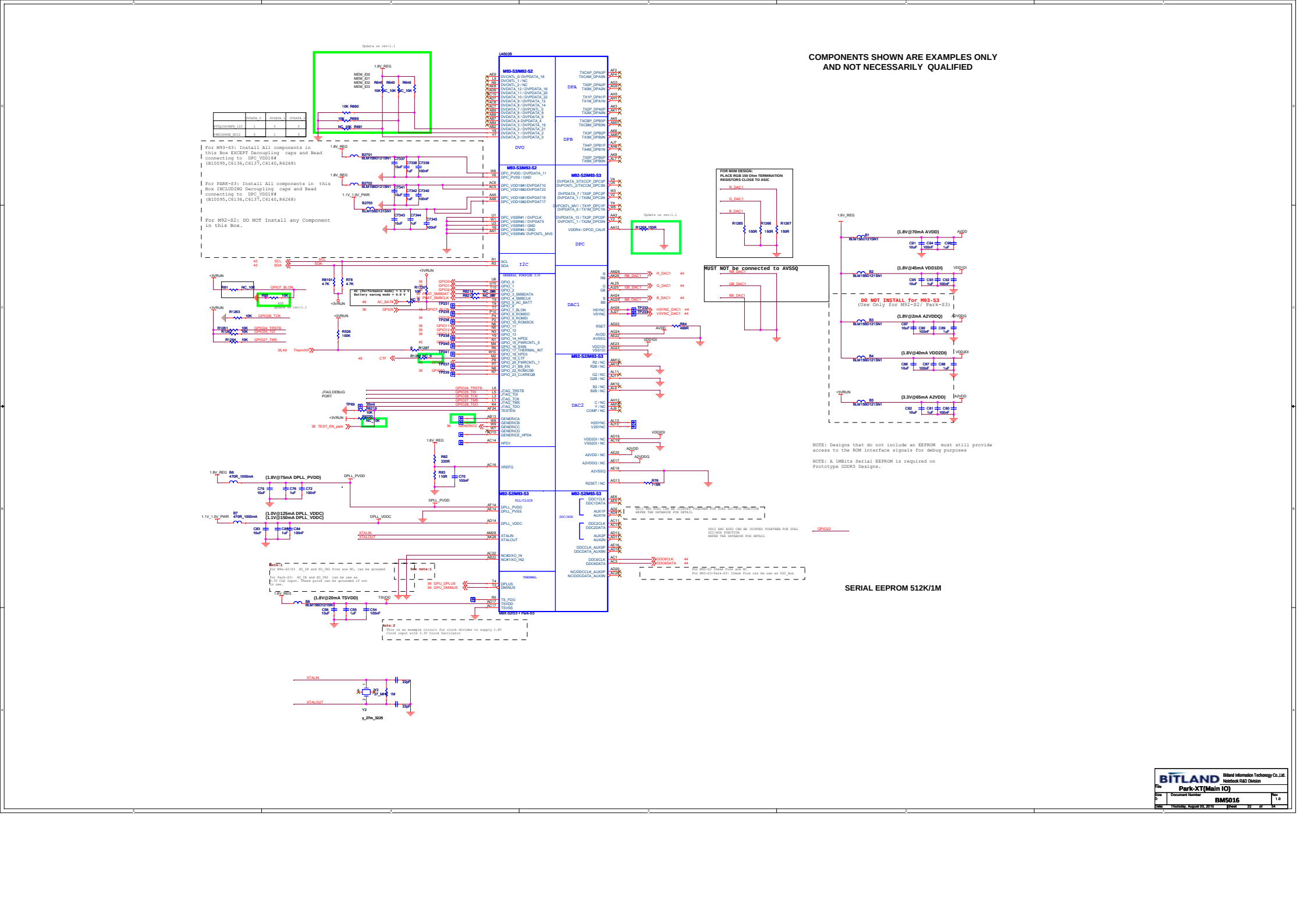
COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

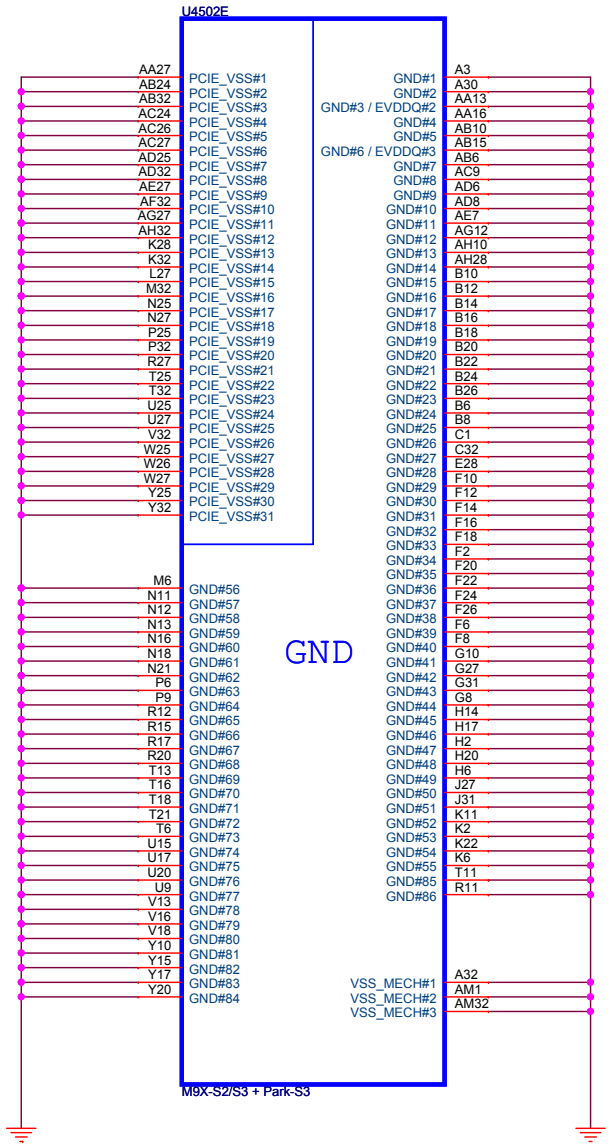
BITLAND Bitland Information Technology Co.,Ltd.
Notebook R&D Division

Title: Park-XT(PCI-E)

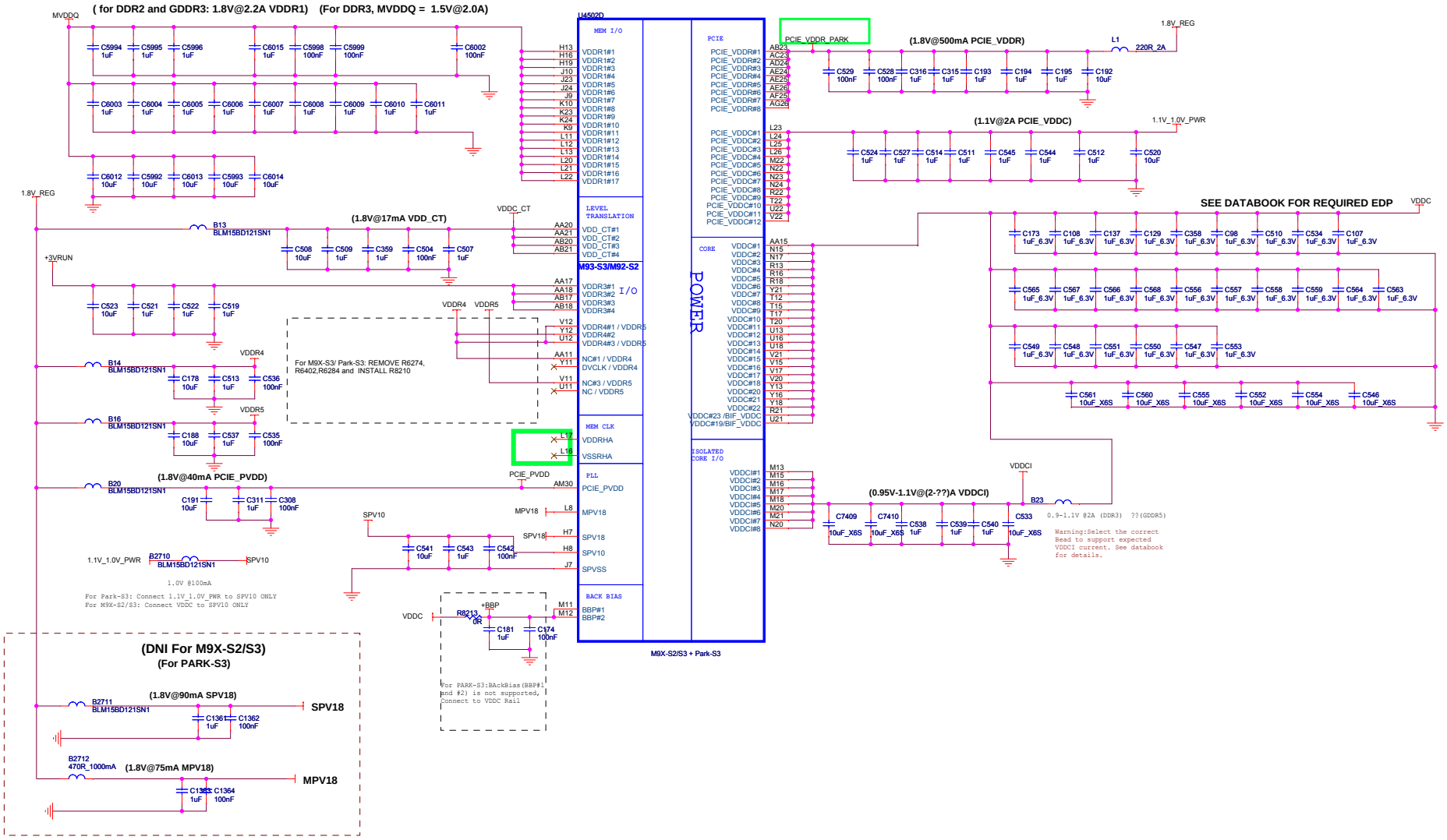
Size: D | Document Number: BM5016 | Rev: 1.0

Date: Thursday, August 05, 2010 | Sheet 31 of 54


COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED
SERIAL EEPROM 512K/1M
NOTE: Designs that do not include an EEPROM must still provide access to the ROM interface signals for debug purposes
NOTE: A 1MBits Serial EEPROM is required on Prototype GDDR5 Designs.
DO NOT INSTALL for M93-S3
(Use Only for M92-S2/ Park-S3)
MUST NOT be connected to AVSSQ
FOR M9X DESIGN:
PLACE RGB 150 Ohm TERMINATION
RESISTORS CLOSE TO ASIC
For M93-S3: Install All components in this Box EXCEPT Decoupling caps and Bead connecting to DPC_VDDl8# (B10095,C6136,C6137,C6140,R6268)
For PARK-S3: Install All components in this Box INCLUDING Decoupling caps and Bead connecting to DPC_VDDl8# (B10095,C6136,C6137,C6140,R6268)
For M92-S2: DO NOT Install any Component in this Box.
(1.8V@70mA AVDD)
(1.8V@45mA VDD1DI)
(1.8V@2mA A2VDDQ)
(1.8V@40mA VDD2DI)
(3.3V@65mA A2VDD)
(1.8V@75mA DPLL_PVDD)
(1.8V@125mA DPLL_VDDC)
(1.1V@150mA DPLL_VDDC)
(1.8V@20mA TSVDD)
BITLAND
Bitland Information Technogy Co.,Ltd.
Notebook R&D Division
Park-XT(Main IO)
BM5016

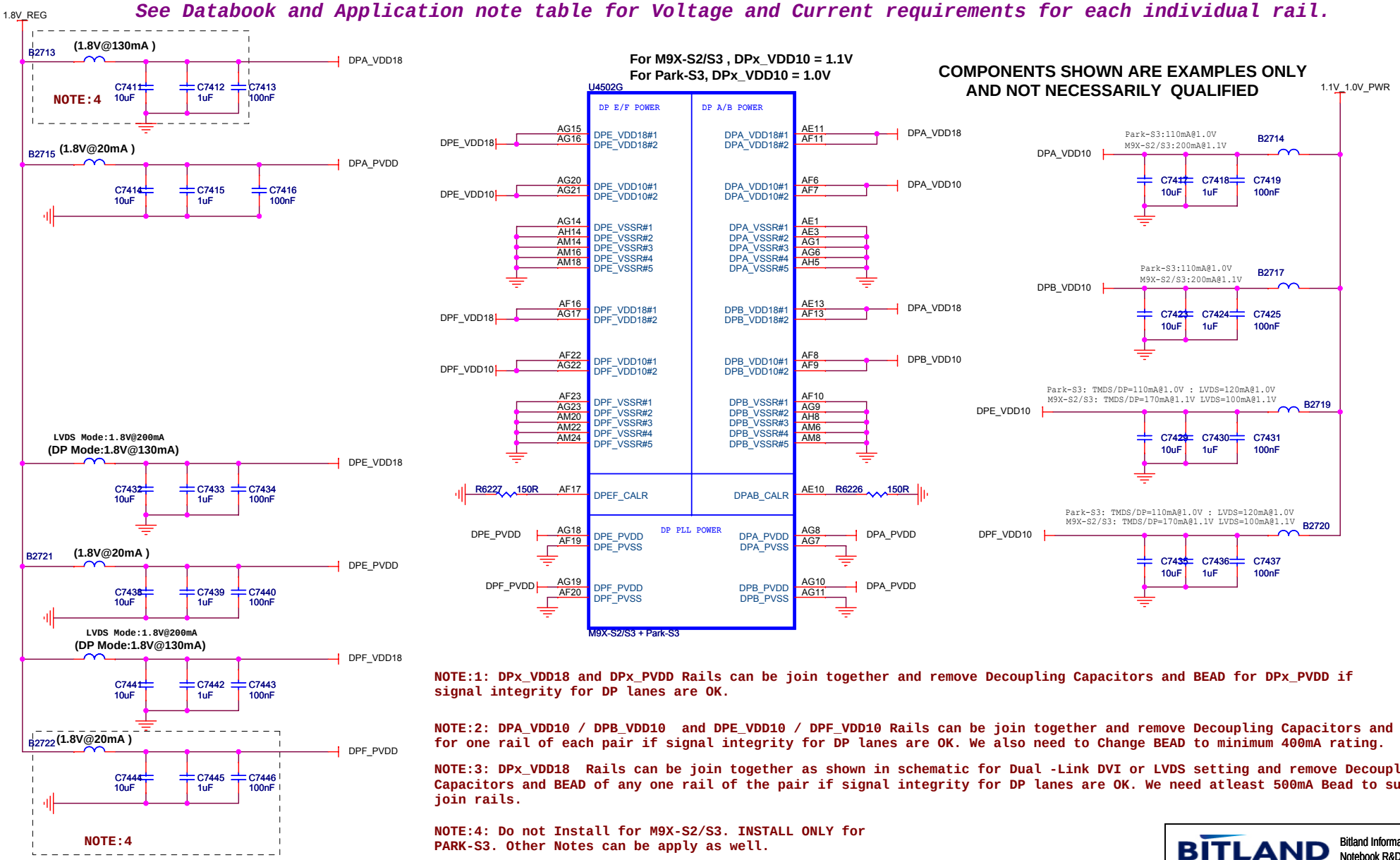


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	PARK-XT(Core_GND)	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 33 of 54	



BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division		
Title	Park_XT(Power_and_NC)		
Size C	Document Number BM5016		Rev 1.0
Date: Thursday, August 05, 2010	Sheet 34 of 54		

See Databook and Application note table for Voltage and Current requirements for each individual rail.



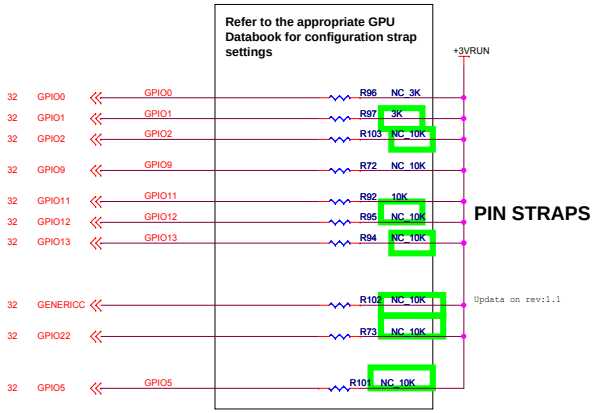
NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEAD for one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove Decoupling Capacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need atleast 500mA Bead to support join rails.

NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Park-XT(DP Power)	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 35 of 54	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC		0
AUD[0]	VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

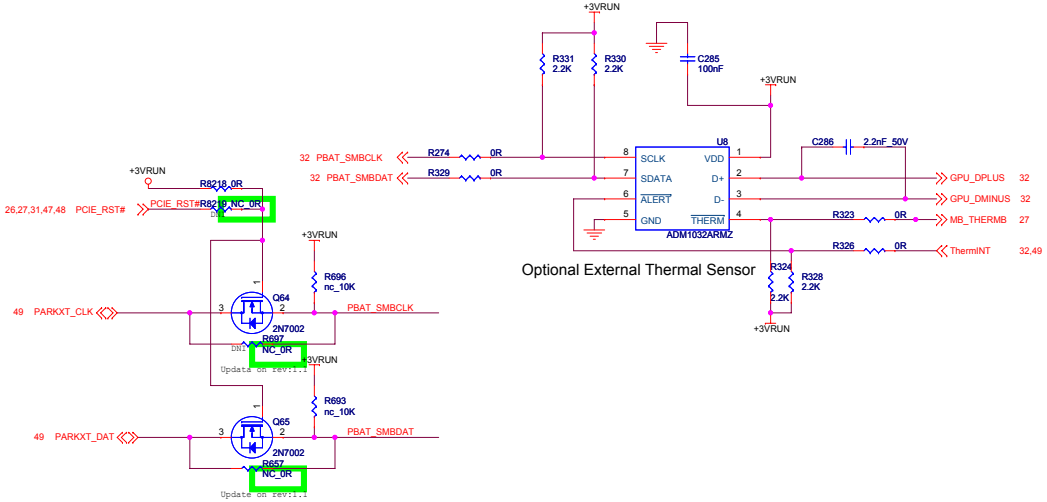
AMD RESERVED CONFIGURATION STRAPS

Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset

H2SYNC GENERICC

Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset

GPIO21_BB_EN



BITLAND Bitland Information Technology Co.,Ltd.
Notebook R&D Division

Title: MINI PCIE SLOT 1,2 (SB)

Size	Document Number	Rev
C	BM5016	1.0

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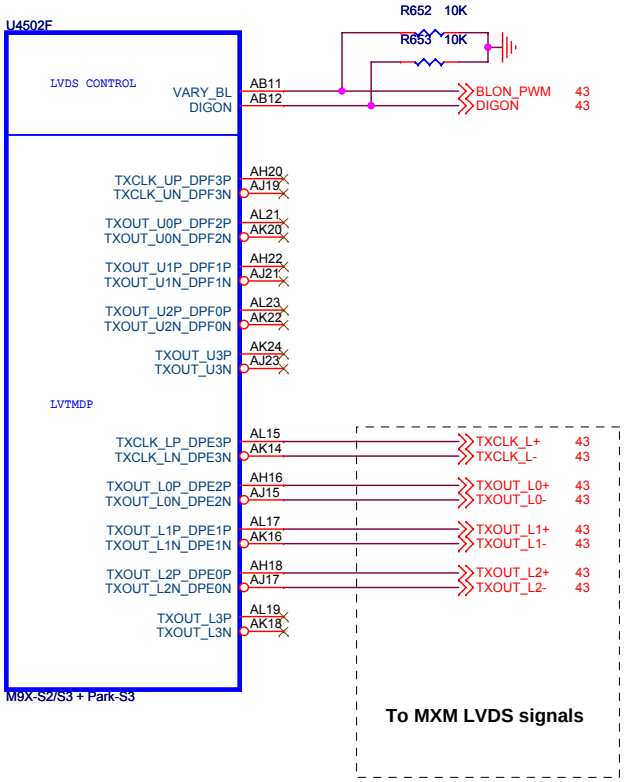
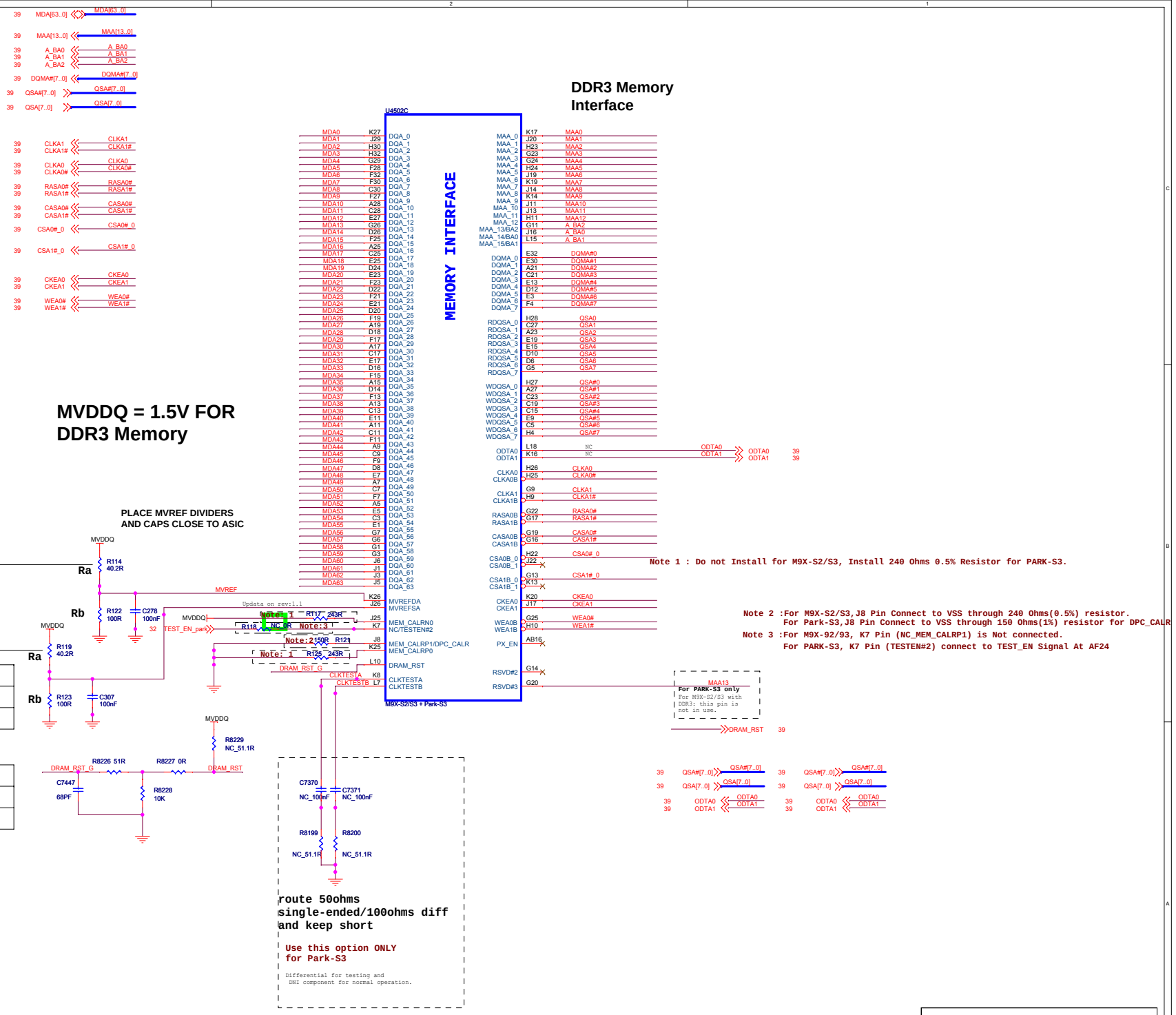
LVDS Interface



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Park-XT(DPEF_ LVDS)	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 37 of 54	

DDR3 Memory Interface



For M9X-S2/S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

For Park-S3

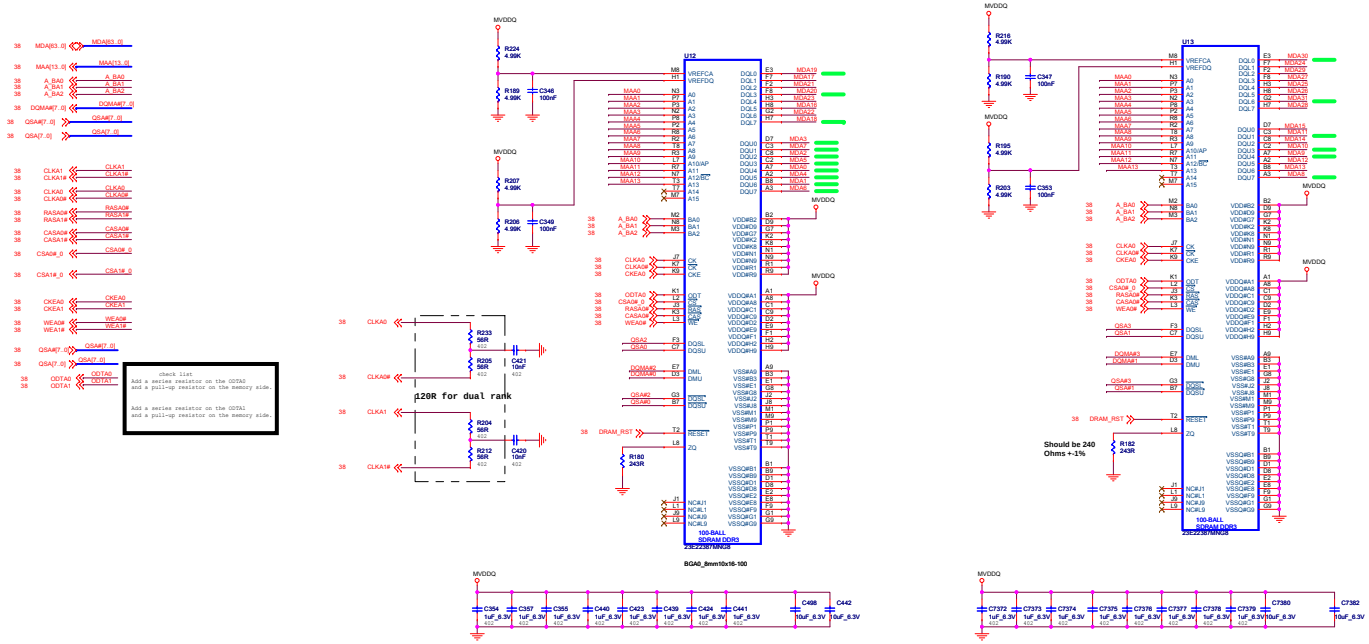
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division

Title: Park-XT(MEM Interface)

Size: C | Document Number: BM5016 | Rev: 1.0

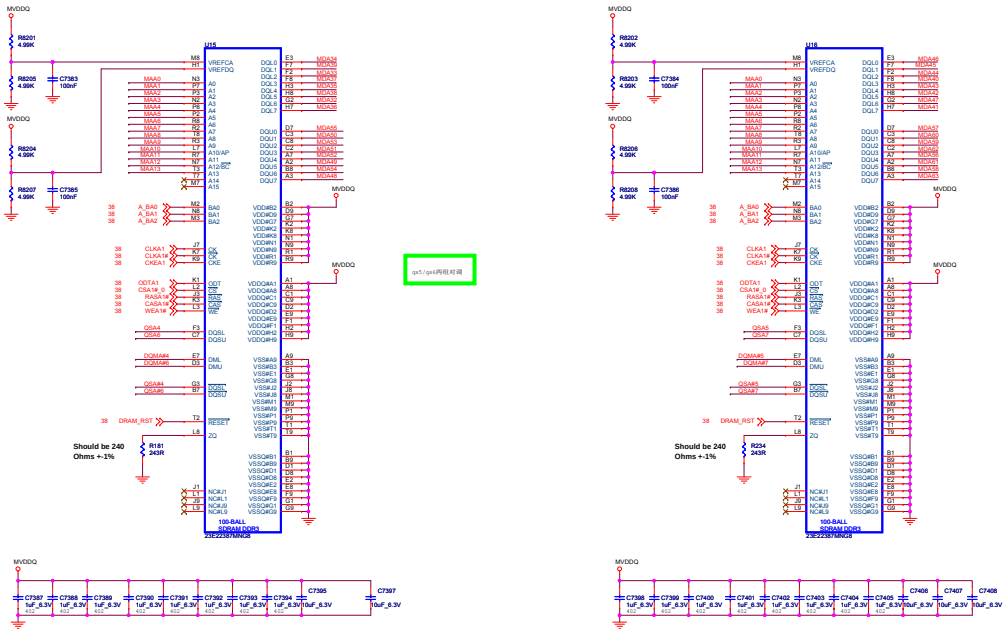
Date: Thursday, August 05, 2010 | Sheet 38 of 54



For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128KX16 DDR3.

RANK1: 256MB/ 512MB DDR3

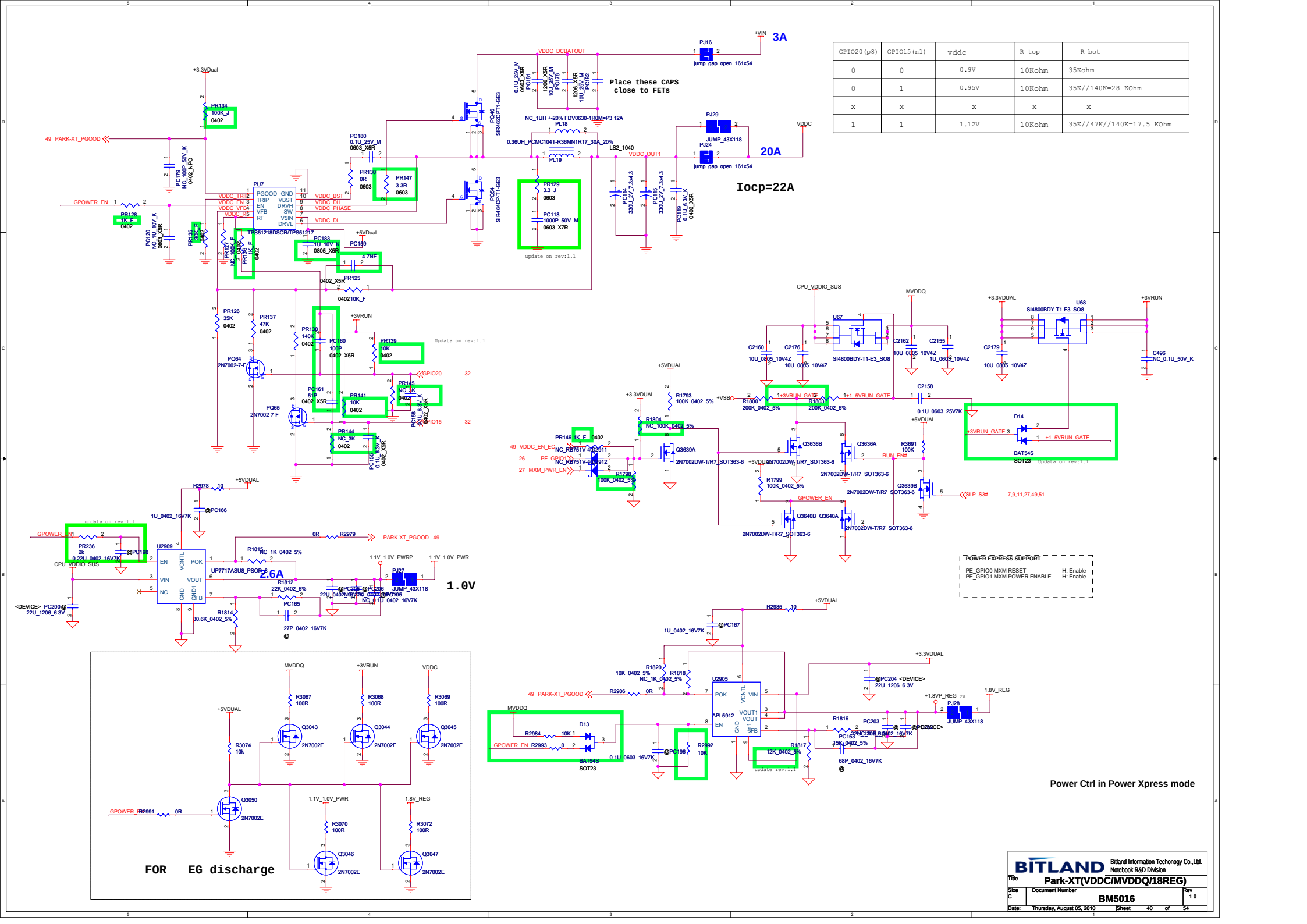
PARK_XT ENG=750MHZ ,Mem=900MHZ DDR3



For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64KX16 DDR3. MAA13 is NC

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

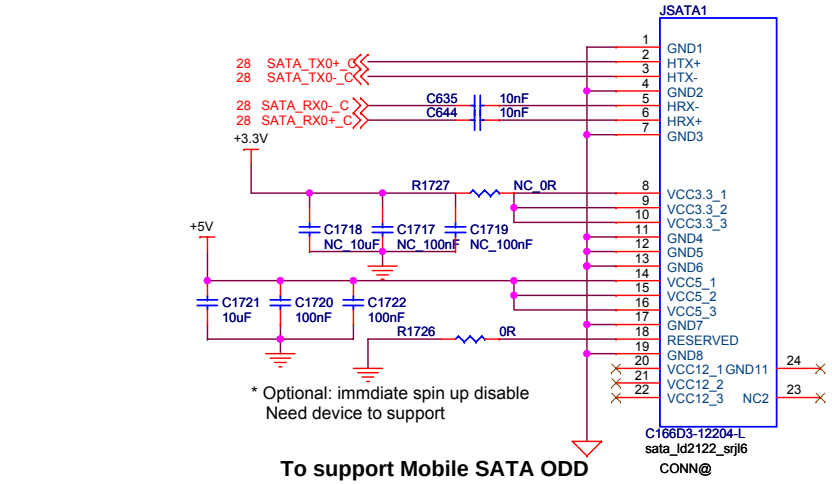
BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division		
Title	Park-XT(DDR3 Memory)		
Size	Document Number		Rev
D	BM5016		1.0
Date:	Thursday, August 05, 2010	Sheet 39 of 54	



GPIO20(p8)	GPIO15(n1)	vddc	R top	R bot
0	0	0.9V	10Kohm	35Kohm
0	1	0.95V	10Kohm	35K//140K=28 KOhm
x	x	x	x	x
1	1	1.12V	10Kohm	35K//47K//140K=17.5 KOhm

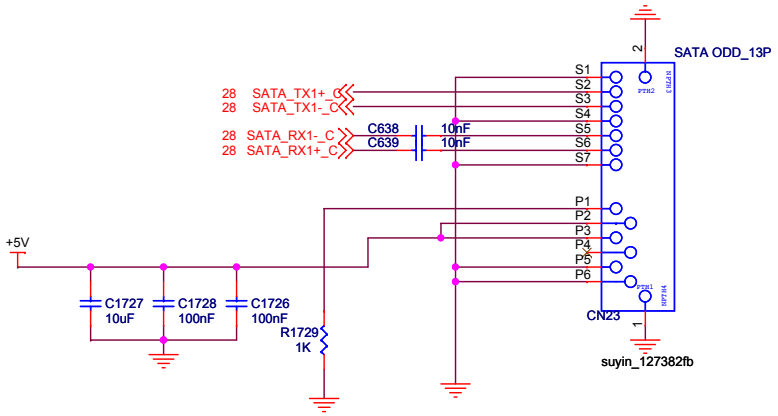
BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division			
Title	Park-XT(VDDC/MVDDQ/18REG)			
Size C	Document Number BM5016			Rev 1.0
Date: Thursday, August 05, 2010		Sheet 40 of 54		

SATA HDD Conn.

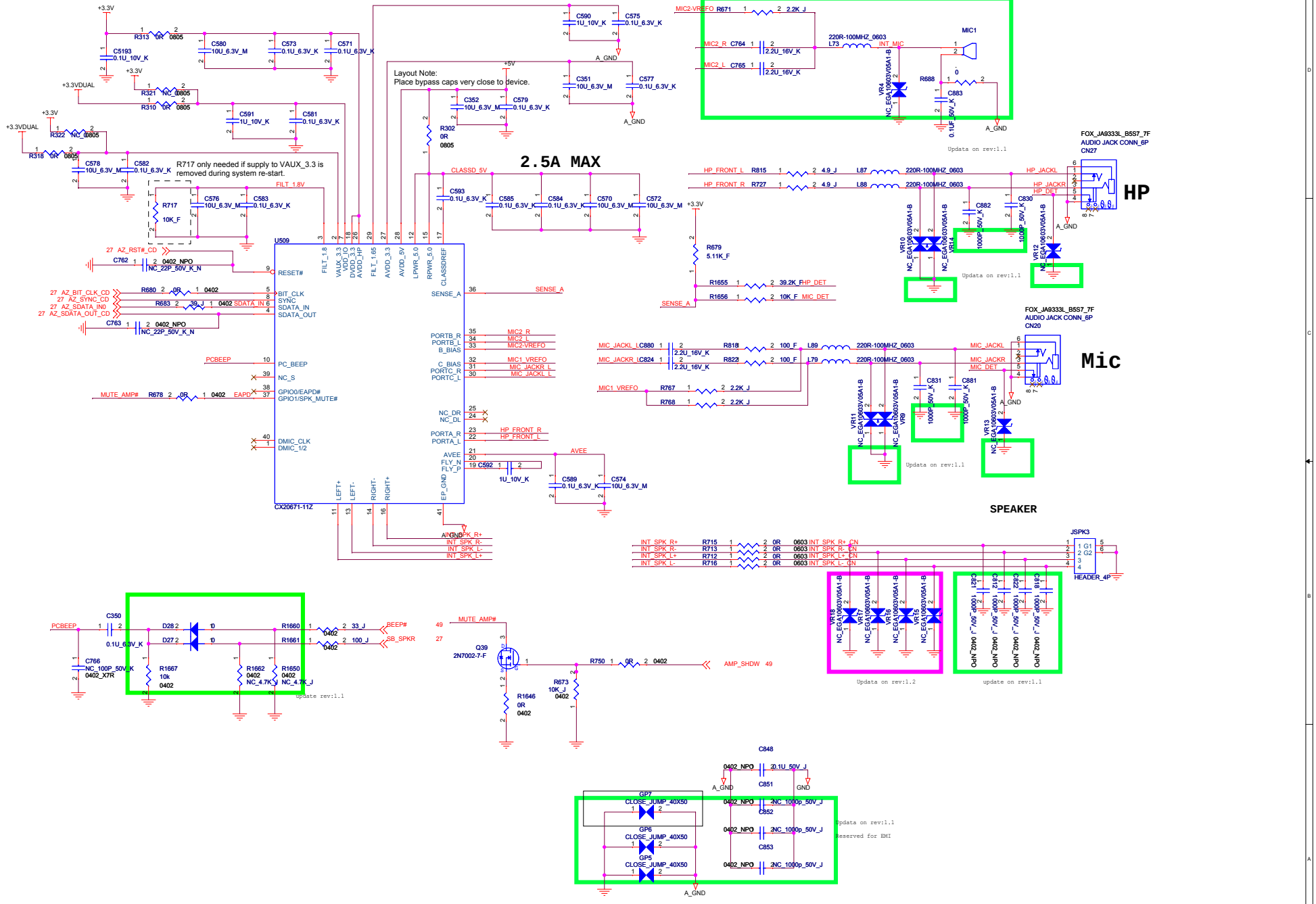


* Optional: immdiate spin up disable
Need device to support

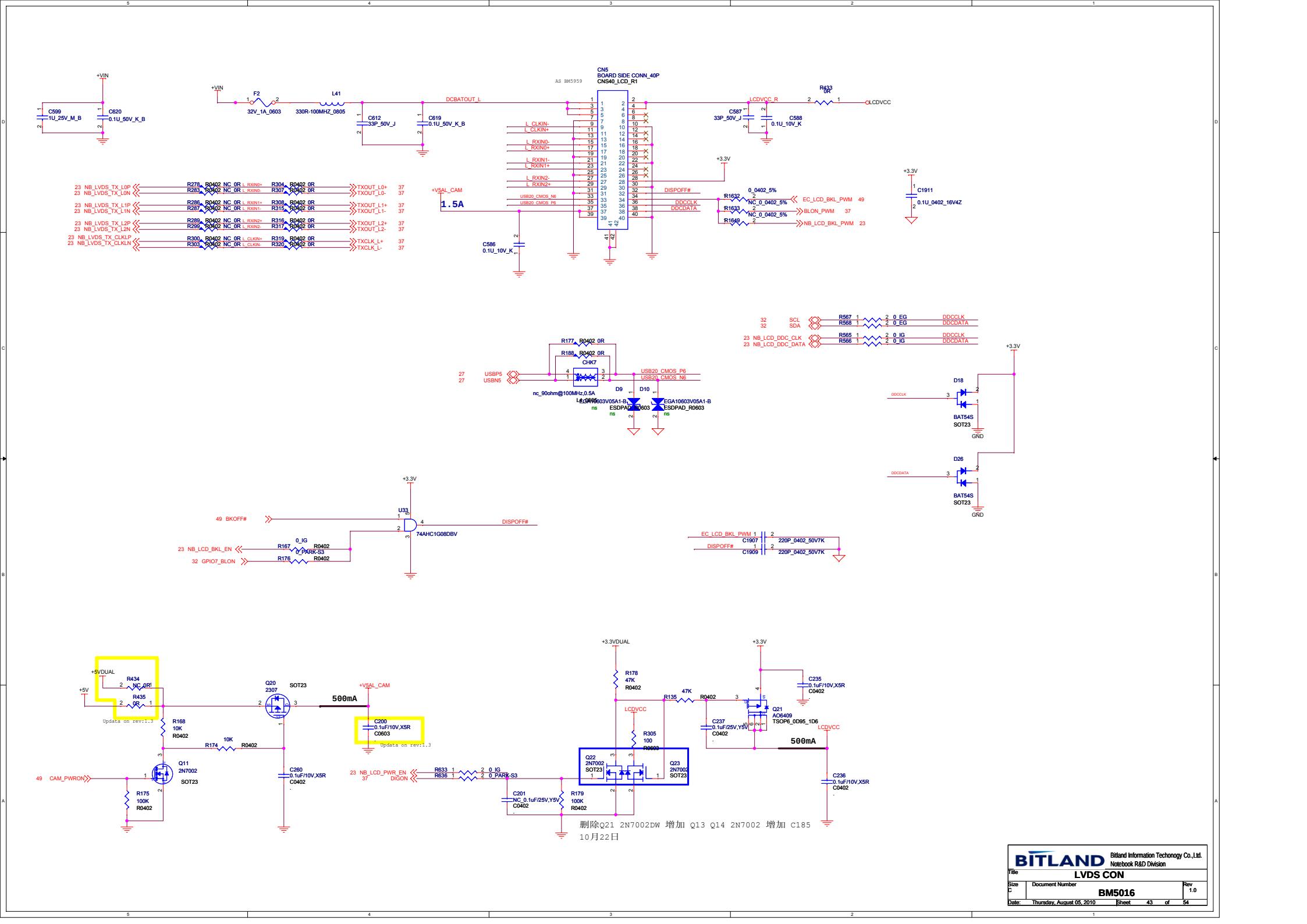
To support Mobile SATA ODD through cable



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	SATA HDD /ODD	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 41 of 54	



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	Audio (CODEC HP MIC)		
Size C	Document Number BM5016	Rev 1.0	
Date: Thursday, August 05, 2010	Sheet 42 of 54		

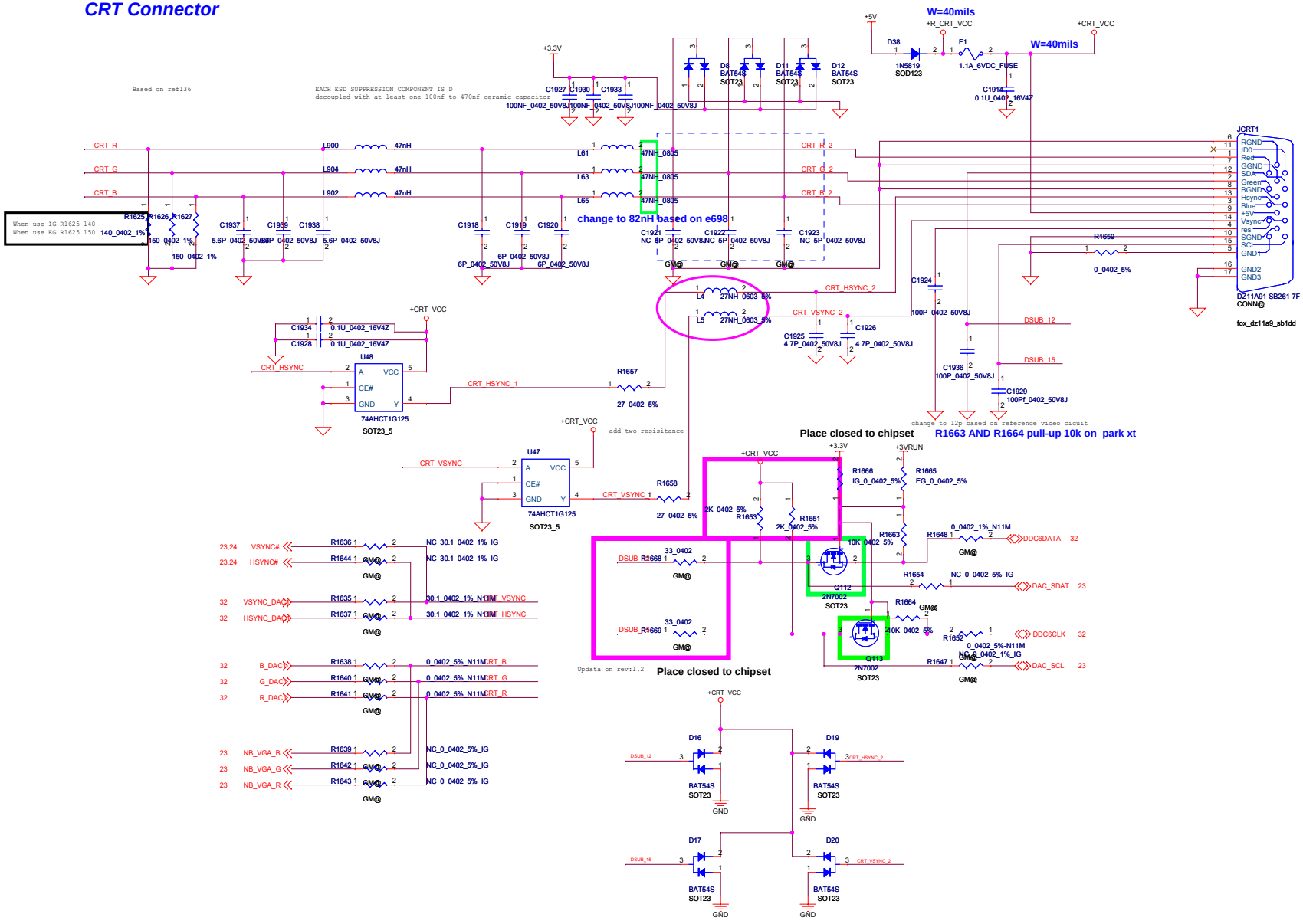


删除Q21 2N7002DW 增加 Q13 Q14 2N7002 增加 C185

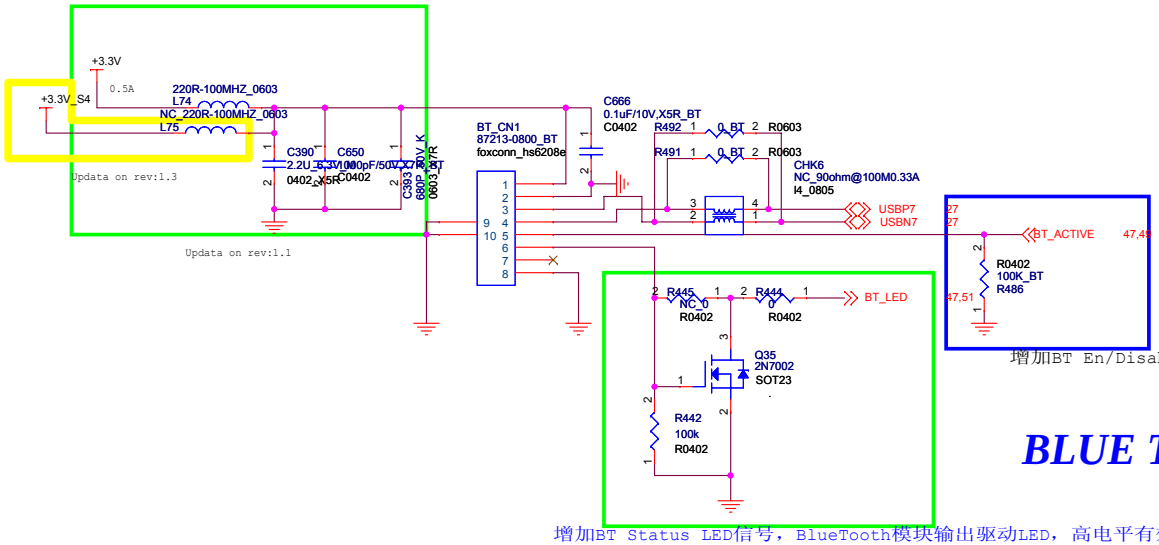
10月22日

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	LVDS CON		
Size C	Document Number BM5016		Rev 1.0
Date: Thursday, August 05, 2010	Sheet 43 of 54		

CRT Connector



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	CRT		
Size C	Document Number BM5016		Rev 1.0
Date: Thursday, August 05, 2010	Sheet 44 of 54		

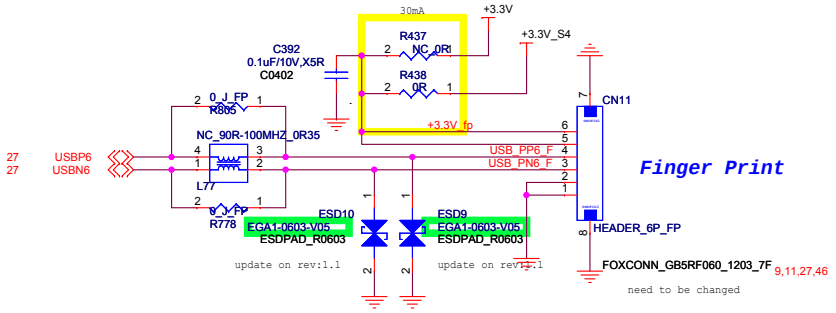


增加BT En/Disable信号，高电平有效。增加对地电阻。

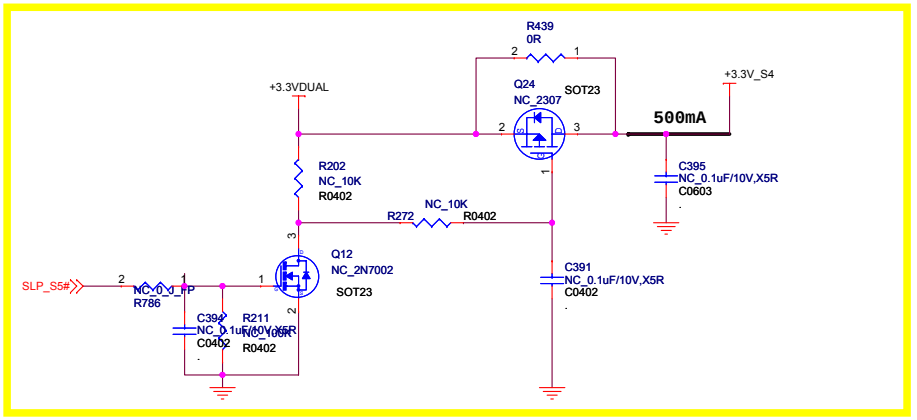
BLUE TOOTH

增加BT Status LED信号，BlueTooth模块输出驱动LED，高电平有效
2010-5-20

update on rev:1.1



Finger Print



Updata on rev:1.3

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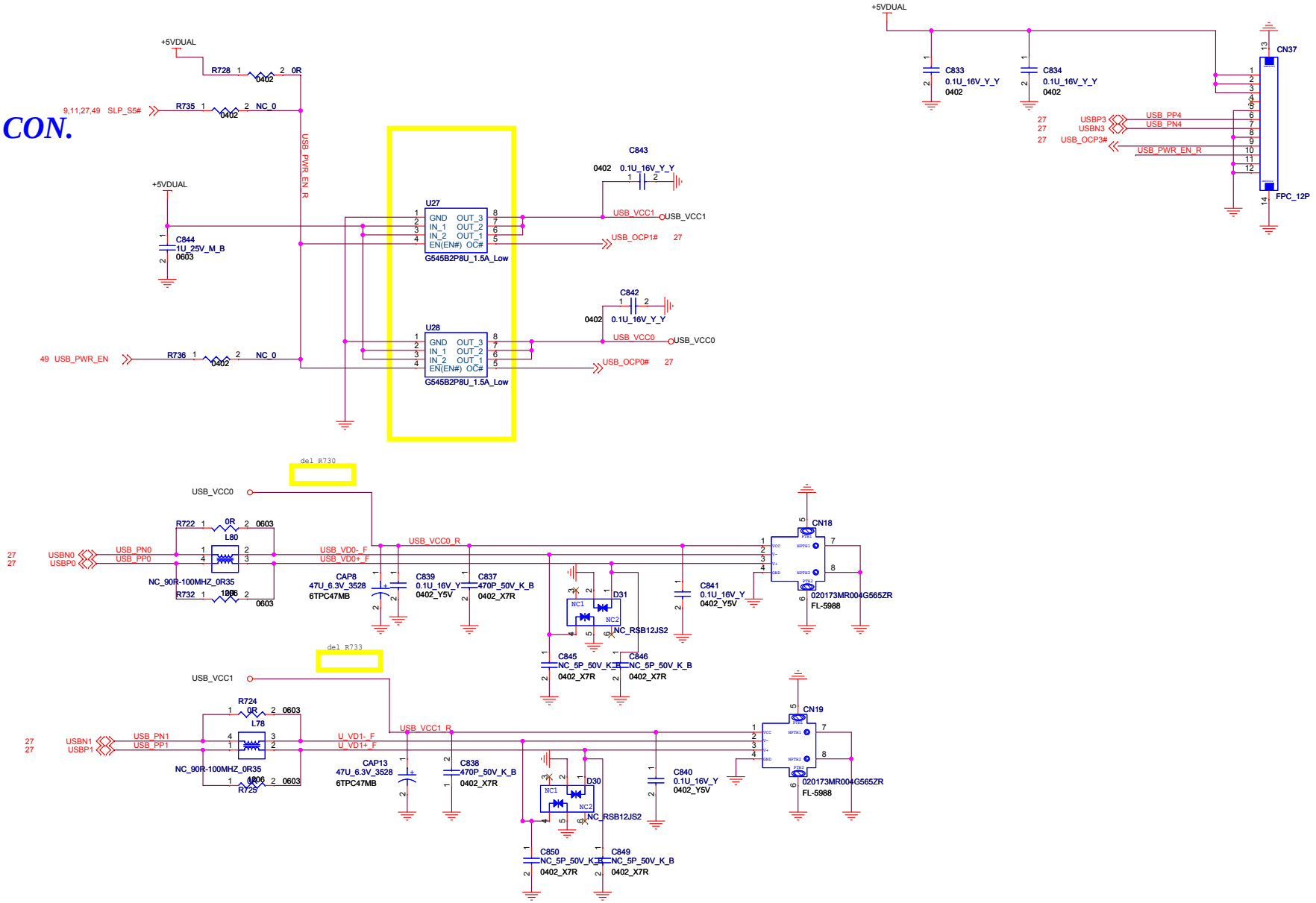
USB CON.



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Title	USB/PW_SW CONN	
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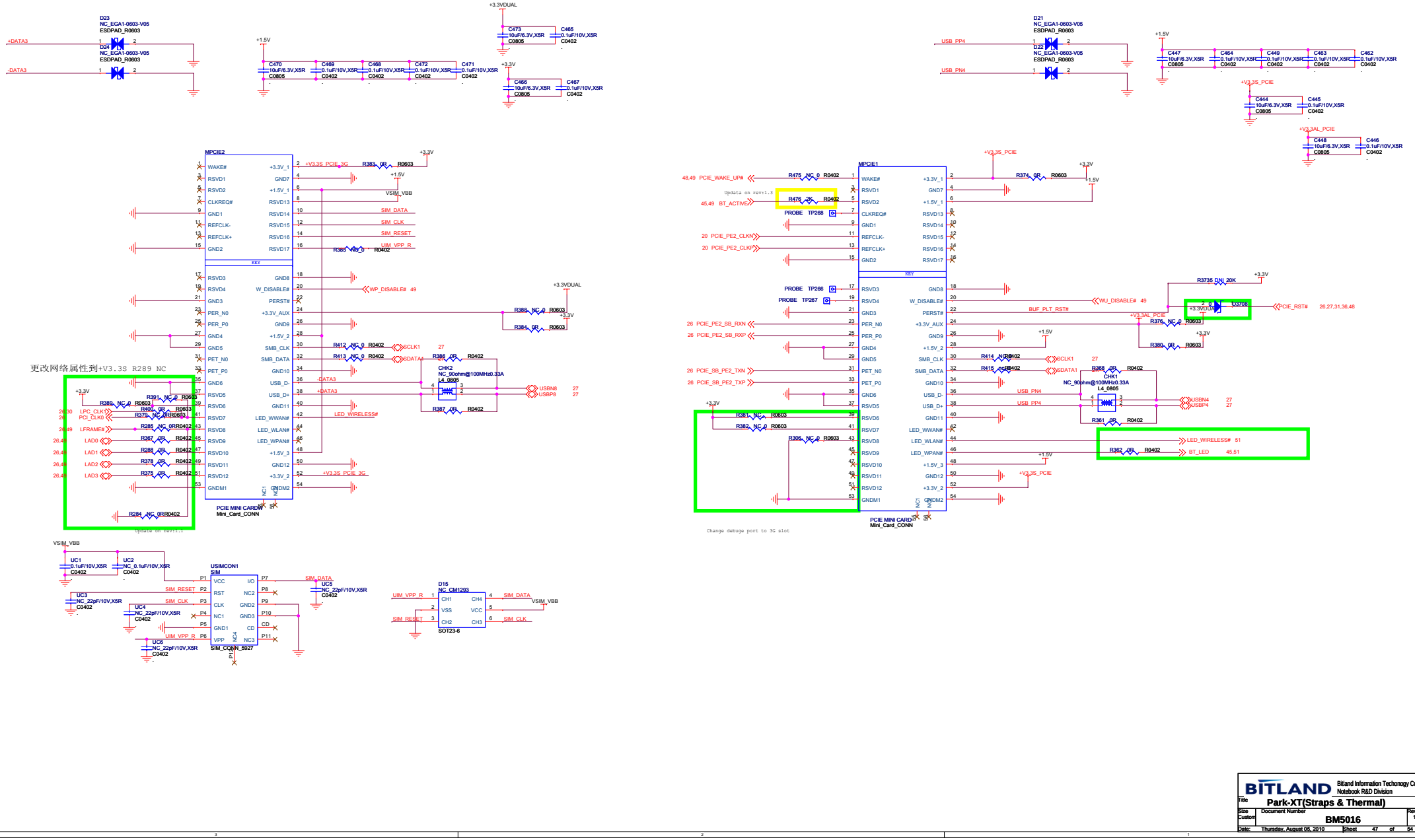

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	Park-XT(Straps & Thermal)		
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MDIO Single End = 50 Ohm

MPD connect to Main Power or RSTN for D3E application, to AUX power otherwise.

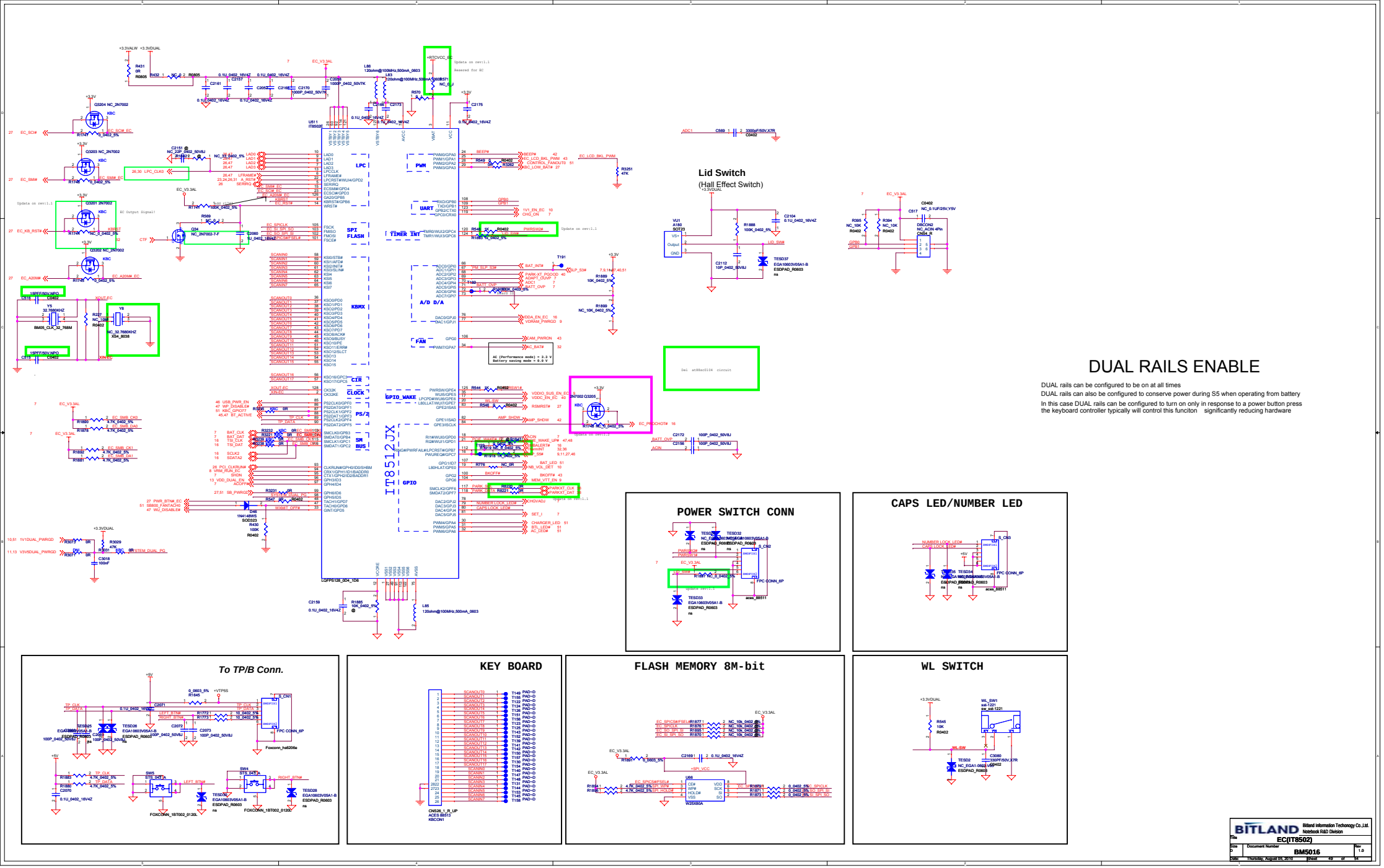
	Function			
R3	R4	R5	C2	
0	NC	NC	NC	Disable D3E
NC	NC	0	NC	Enable D3E(1)
NC	100K	NC	0.1u	Enable D3E(2)

JMC251
JMC261

Updated on Rev1.1

closed to chip.

Card Reader



BITLAND	Biland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	EC(IT8502)
Size	D
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Title	//	
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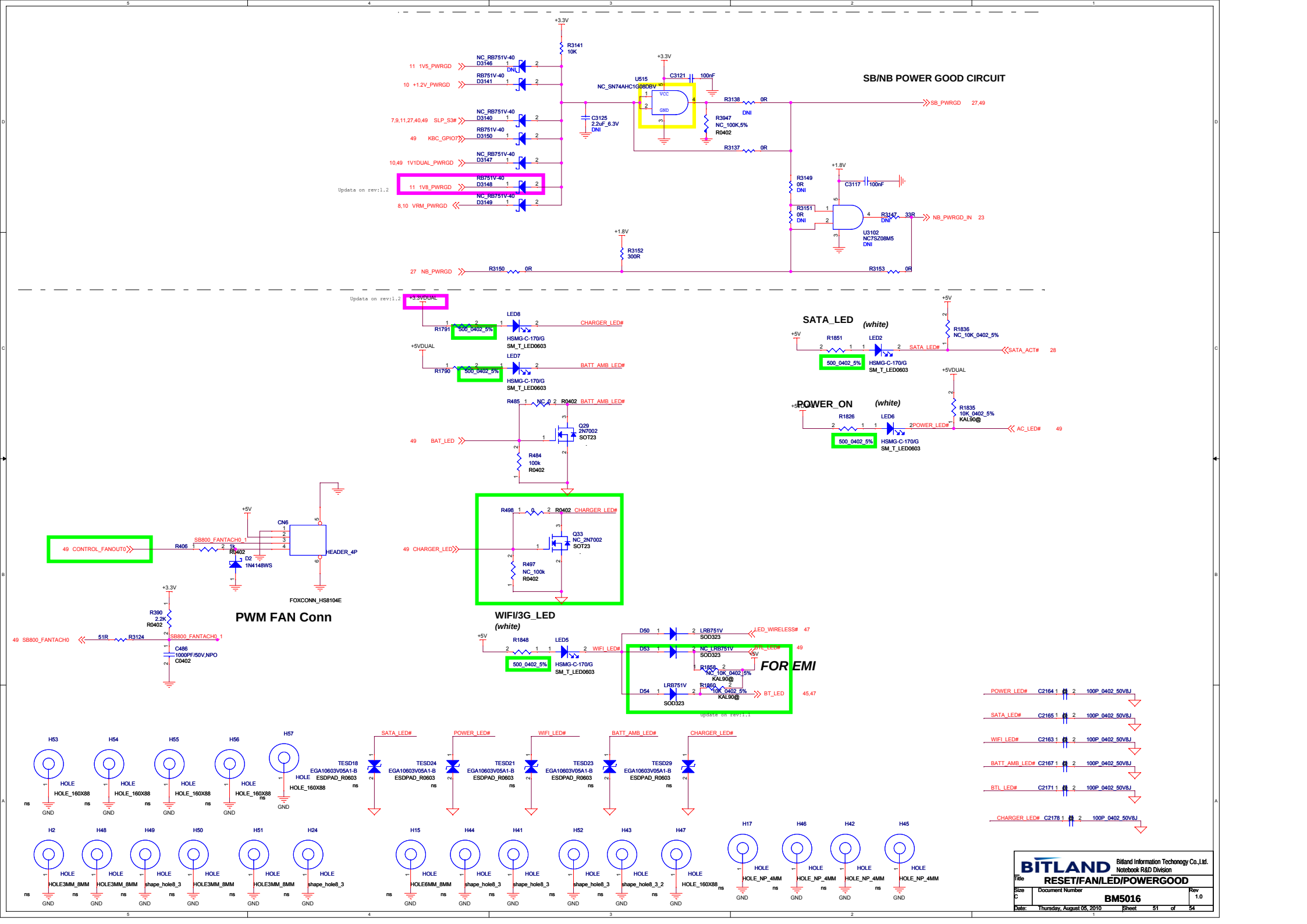
SB/NB POWER GOOD CIRCUIT
SATA_LED (white)
POWER_ON (white)
PWM FAN Conn
WIFI/3G_LED (white)
FOR EMI
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Notebook R&D Division
RESET/FAN/LED/POWERGOOD
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Title	pull up resistor
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Title	change history
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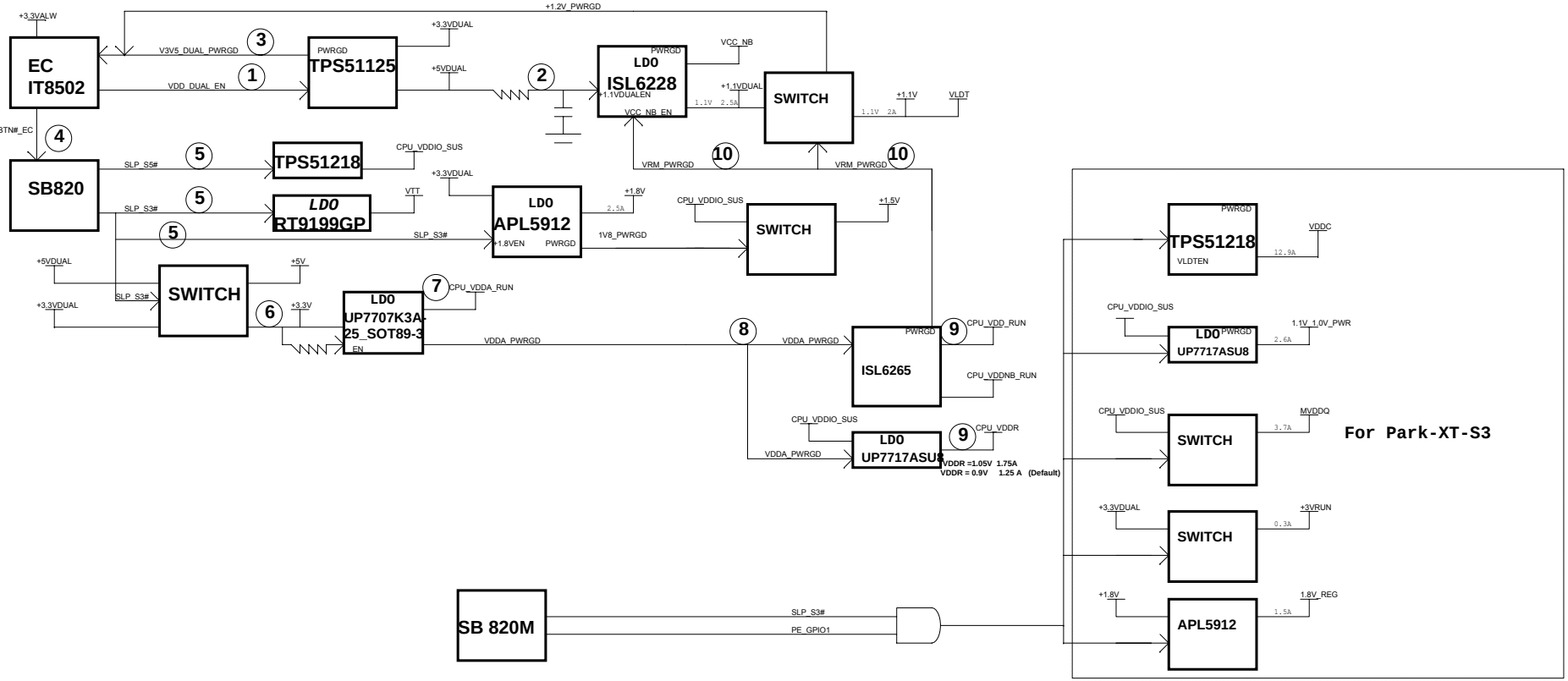

Power on Sequence required:

SB800:

1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:

1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

各电源PWM/L/MOS选型

POWER	PWM	L	H_GATE	L_GATE
+3.3VDUAL (+3.3V 8A)	TI/TPS51125RGER VQFN24	HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)
+5VDUAL (+5V 8A)		HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)
VCC_NB (+1.1V 12A)	ISL6228HRTZ-T TQFN-28	HB90109M00LFE 1.0H ±20% 12A 10mΩ SMD-6.6×7.3×3.0mm	VISHAY/SI4172DY-T1-GE3 15A +/-20V 15mΩ@4.5V SO-8pin	VISHAY/SI4168DY-T1-GE3 24A +/-20V 7.6mΩ@4.5V SO-8pin
VLDT (+1.2V 4A)		HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	L/H intergrated (待定)	
VDDIO_SUS (+1.5V 11A)	TPS51218 DSC	HB90109M00LFE 1.0H ±20% 12A 10mΩ SMD-6.6×7.3×3.0mm	VISHAY/SI4172DY-T1-GE3 15A +/-20V 15mΩ@4.5V SO-8pin	VISHAY/SI4168DY-T1-GE3 24A +/-20V 7.6mΩ@4.5V SO-8pin
CPU_VDD_RUN (+1.375--1.5V 36A)	ISL6265 QFN-48	HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	PHASE1 VISHAY/SiR462DP-T1-GE3 30A +/-20V 0.01Ω@4.5V PowerPAK SO-8pin PHASE2 VISHAY/SiR462DP-T1-GE3 30A +/-20V 0.01Ω@4.5V PowerPAK SO-8pin	VISHAY/SiR466DY-T1-E3/GE3(two) 24.5A +/-20V 6.7mΩ@4.5V SO-8pin VISHAY/Si466DY-T1-E3/GE3(two) 24.5A +/-20V 6.7mΩ@4.5V SO-8pin
CPU_VDDNB_RUN (0.9V 4A)		HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	L/H intergrated (待定)	
charger	ISL6251HAZ SSOP24_25_150	HB90100MA0LFE 10uH±20% IDC=4A DCR-Max= 71.2mΩ SMD 6.86x6.47x3.0mm	AOS/AON7408 20A RDS(ON)<34mΩ(VGS=4.5V DFN-8)	AOS/AON7702 20A RDS(ON)<14mΩ(VGS=4.5V) DFN-8

LDO

VTT	RT9199GP	(+1.5V---0.75 1.5A)
CPU_VDDA_RUN	APL5508_25DC_TRL SO789_3	(+3.3V---2.5V 500MA)
+1.8V	APL5930	(+3.3V---1.8 1.5A)
CPU_VDDR	APL5912	(+1.5V---1.05V 4A)
+1.1VDUAL	APL5930	(+3.3V---1.1V 500MA)

SWITCH

INPUT(V)	OUTPUT(V)	MOS
+5VDUAL	+5V	AO4468 (8A)
+3.3VDUAL	+3.3V	AO4468 (8A)
VLDT	+1.1V	JUMPER (4A)
CPU_VDDIO_SUS	+1.5V	AO4468 (5A)

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Title: Power sequence

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