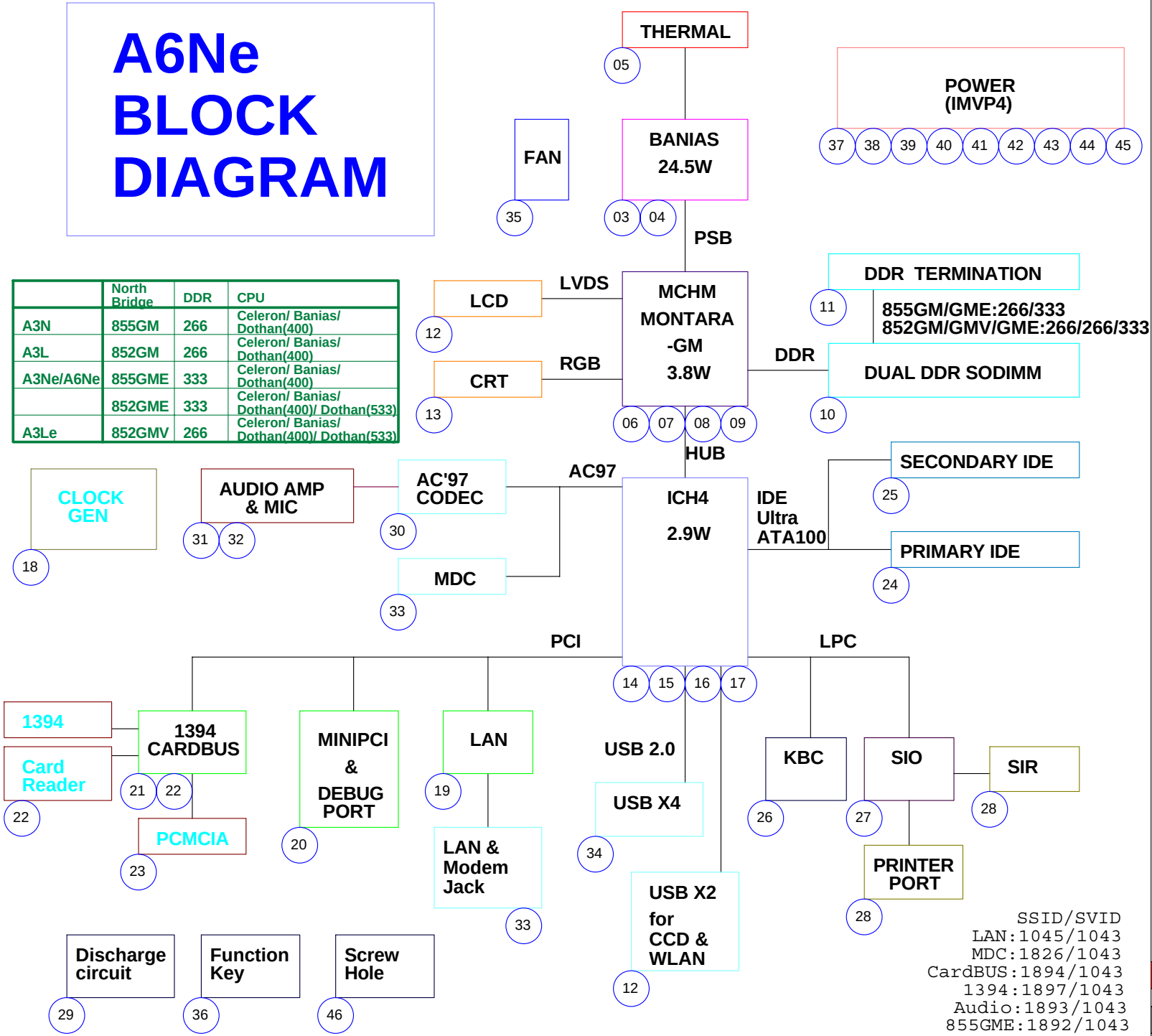
A6Ne BLOCK DIAGRAM



	North Bridge	DDR	CPU
A3N	855GM	266	Celeron/ Banias/ Dothan(400)
A3L	852GM	266	Celeron/ Banias/ Dothan(400)
A3Ne/A6Ne	855GME	333	Celeron/ Banias/ Dothan(400)
	852GME	333	Celeron/ Banias/ Dothan(400)/ Dothan(533)
A3Le	852GMV	266	Celeron/ Banias/ Dothan(400)/ Dothan(533)

SSID/SVID
LAN:1045/1043
MDC:1826/1043
CardBUS:1894/1043
1394:1897/1043
Audio:1893/1043
855GME:1892/1043

FILE LIST

01

ASUSTek COMPUTER INC. NB1

Title : BLOCK DIAGRAM

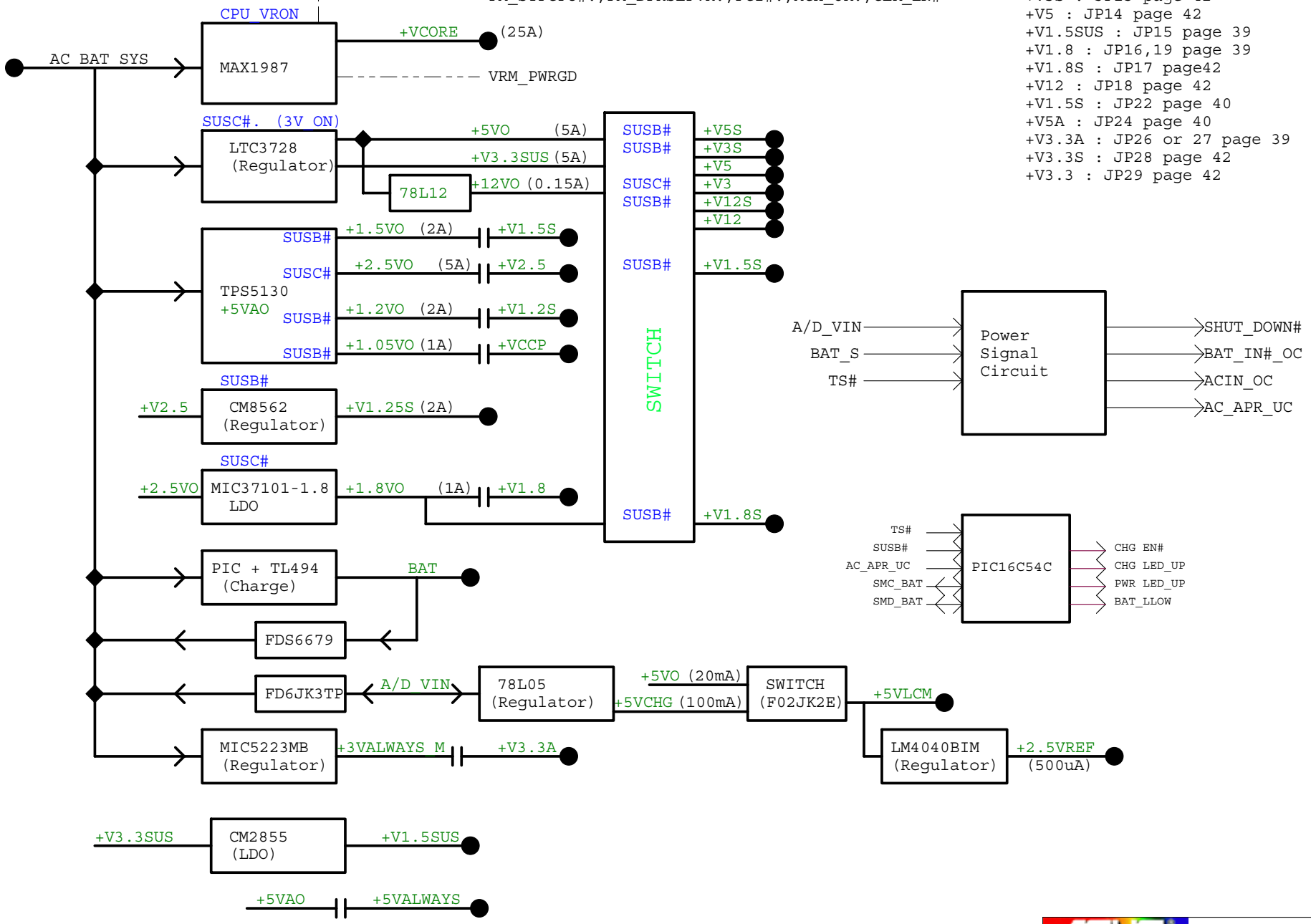
Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 1 of 51

System work voltage
Adapter in : 19.5 ~18.5 V
Battery in : 16.8 ~ 11.6V

+V1.25S : JP4,5 page 39
+V2.5 : JP6 page 40
+V1.2S : JP7 page 40
+VCCP : JP9 page 40
+V5S : JP13 page 42
+V5 : JP14 page 42
+V1.5SUS : JP15 page 39
+V1.8 : JP16,19 page 39
+V1.8S : JP17 page42
+V12 : JP18 page 42
+V1.5S : JP22 page 40
+V5A : JP24 page 40
+V3.3A : JP26 or 27 page 39
+V3.3S : JP28 page 42
+V3.3 : JP29 page 42



ASUSTek COMPUTER INC. NB1

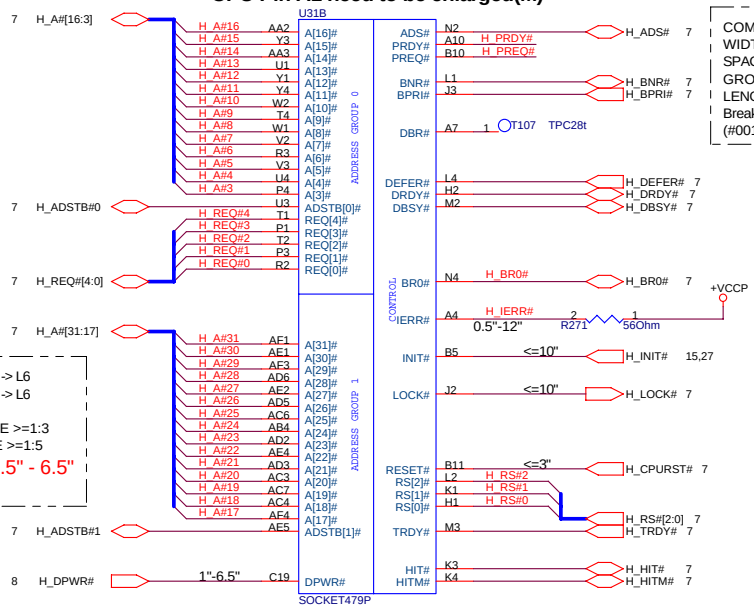
Title : POWER DIAGRAM

Engineer: Adams Lin

Size	Project Name	Rev
Custom	A6N	2.0

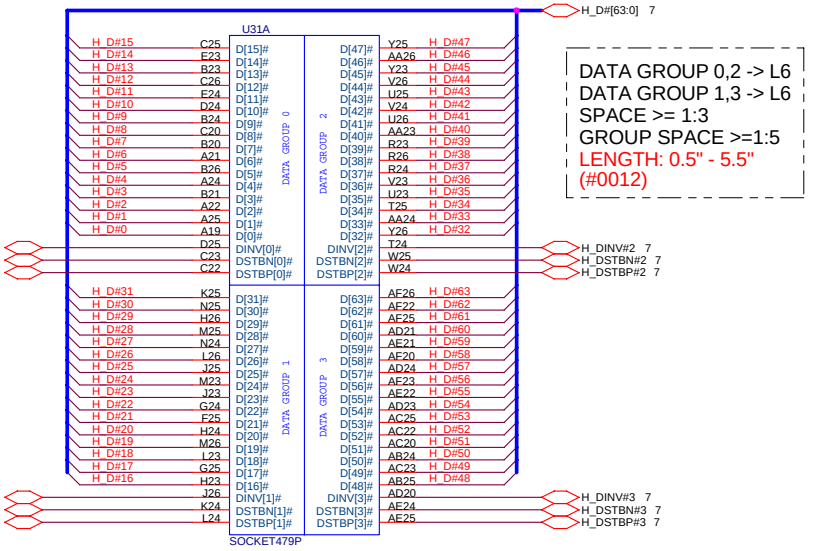
Date: Thursday, October 14, 2004 Sheet 2 of 51

CPU Pin A1 need to be enlarged(M)



COMMON CLOCK -> L6
WIDTH: 5 mils
SPACE >= 1:2
GROUP SPACE >=1:5
LENGTH: 1" - 6.5"(OPT: 4"+/-0.5")
Breakout Length:<=200 mil
(#0011)

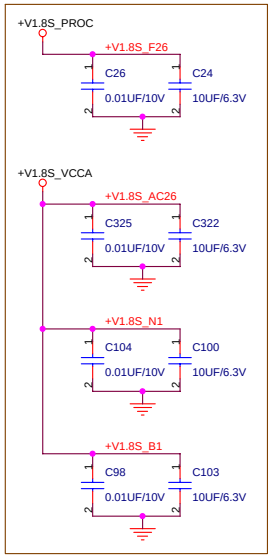
ADDR GROUP 0 -> L6
ADDR GROUP 1 -> L6
SPACE >= 1:2
STROBE SPACE >=1:3
GROUP SPACE >=1:5
LENGTH: 0.5" - 6.5"
(#0012)



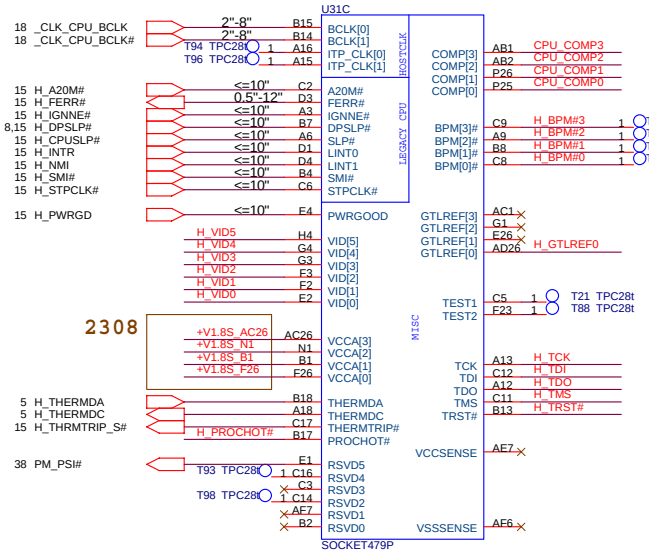
DATA GROUP 0,2 -> L6
DATA GROUP 1,3 -> L6
SPACE >= 1:3
GROUP SPACE >=1:5
LENGTH: 0.5" - 5.5"
(#0012)

CPU PLL CIRCUITS

1.71V - 1.89V(+/- 5%)
S0-S1M: 0.3A



2025 2308



	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4			Pin 1,2

TOPOLOGY 2A:
R-CPU-ICH Y-FORK
CPU-ICH: 0.5" - 12"
R - CPU <= 3"
(#0013)
R73 332Ohm
H_PWRGD

TOPOLOGY 1B:
CPU-ICH-R
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)
R71 56Ohm
H_FERR#

TOPOLOGY 2B:
MCH-CPU-ICH4
MCH-CPU:0.5"-6.5"
CPU-ICH4:0.5"-12"
(#0013)
H_DPSLP#

TOPOLOGY 1C:
CPU-R-LSC-ICH
CPU-R: 0.5" - 12"
R - LSC<= 3"
LSC-ICH:0.5"-12"
R244 56Ohm
H_PROCHOT#

TOPOLOGY 3:
CPU-ICH-R-LSC-FWH
CPU-ICH:0.5" - 12"
R - LSC <= 3"
LSC-FWH:0.5"-6"(#0013)
H_INIT#

TOPOLOGY 1B:
CPU-ICH-R
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)
R239 56Ohm
H_THRMTRIP_S#

H_GTLREF0
LENGTH <=0.5"
WIDTH = 5 mils
SPACE >= 25 mils
X BPSB(#0004)

Close to Pin AD26 of CPU
R224 1KOhm
H_GTLREF0
Same Side w/ CPU
R223 2KOhm

CPU_COMP2 :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0001)
R75 27.4Ohm
CPU_COMP2
Pin AD1,AC2 of BANIAS

CPU_COMP0 :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0001)
R221 27.4Ohm
CPU_COMP0

CPU DEBUG PORT
H_PREQ# R261 200Ohm
H_PRDY# R260 56Ohm
Close to Pin A8 of CPU

Close to Pin A12 of CPU
Width= 5 mils
Length <= 2"

CPU JTAG
H_TMS R250 39Ohm
H_TDO R247 56Ohm
H_TDI R248 150Ohm
H_TCK R246 27.4Ohm
H_TRST# R245 680Ohm

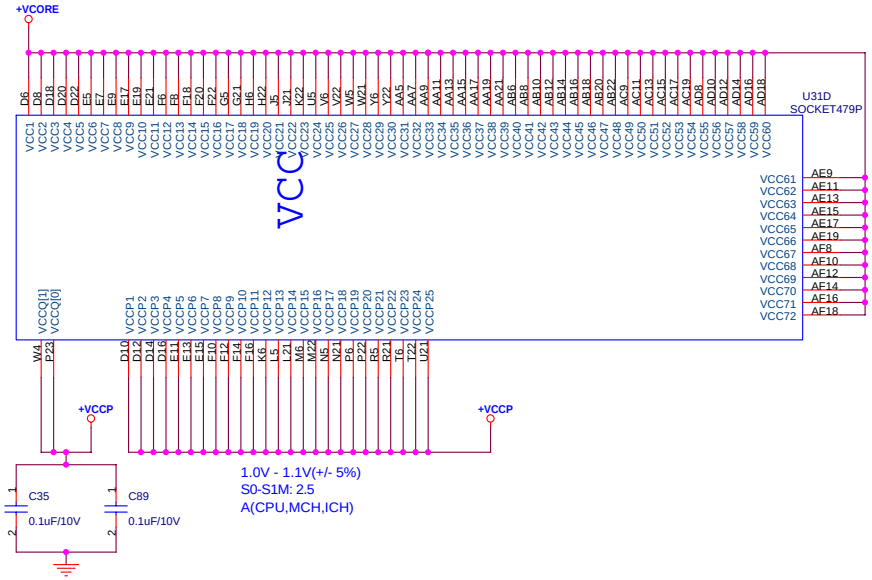
CPU_COMP3 :
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)
R76 56Ohm
CPU_COMP3
Pin AD1,AC2 of BANIAS

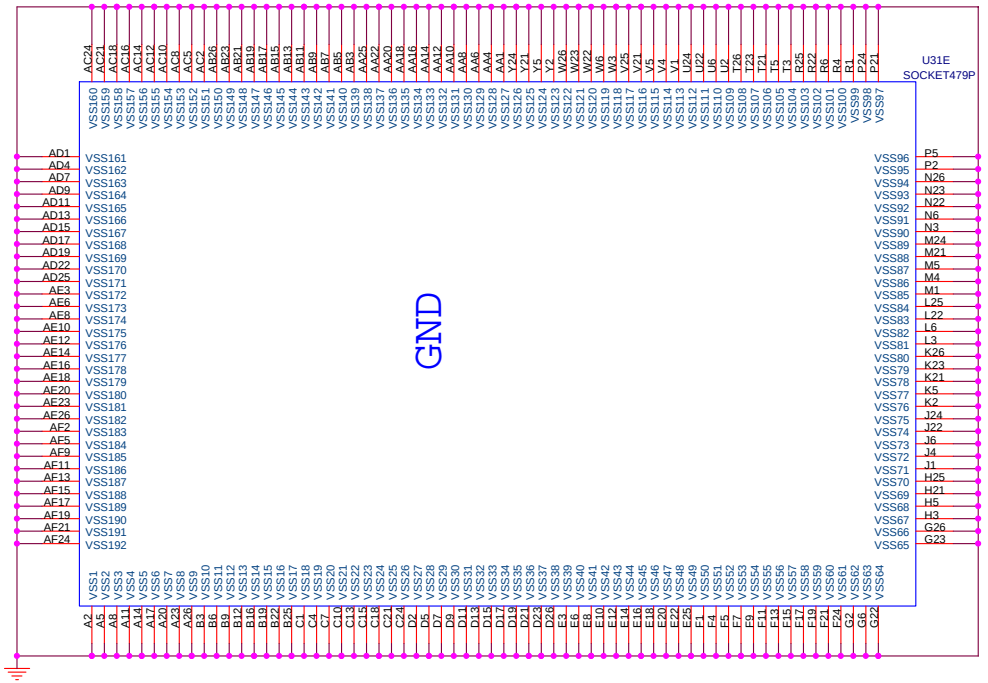
CPU_COMP1 :
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)
R222 56Ohm
CPU_COMP1

ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Title : CPU-BANIAS(HOST)
Size: Custom
Project Name: A6N
Rev: 2.0
Date: Thursday, October 14, 2004
Sheet 3 of 51

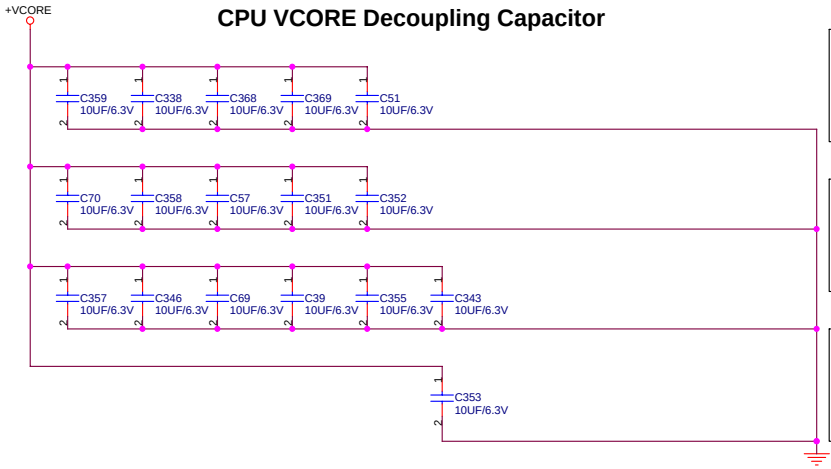
HFM(1.3GHz-1.7GHz): 1.468V
LFM(600MHz): 0.956V

0.745V - 1.356V(+/- 1.5%)
C0: 25 A
C3: 7.59A
C4: 0.9A





CPU VCORE Decoupling Capacitor



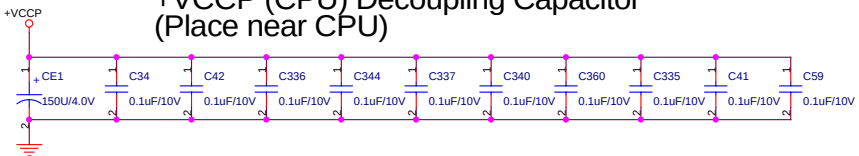
Mid Frequency Decoupling (Place around Processor)

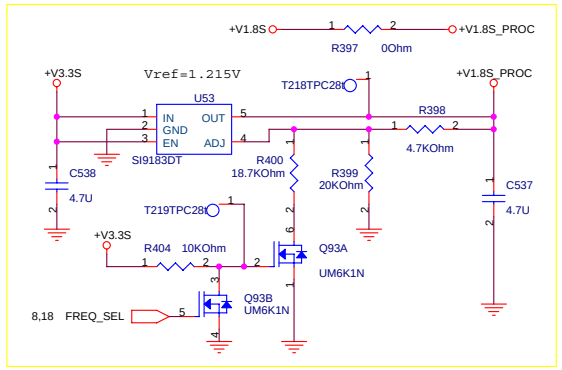
High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

M3N : Four 200 uF are located in IMVP4
A3N : Delete 10uF/6.3V from 35pcs to 17pcs

+VCCP (CPU) Decoupling Capacitor (Place near CPU)





2308

For A3N/A3NE/A3L:
Load R397

For A3LE:
Load C537, C538, Q93, R398, R399, R400, R404, U53

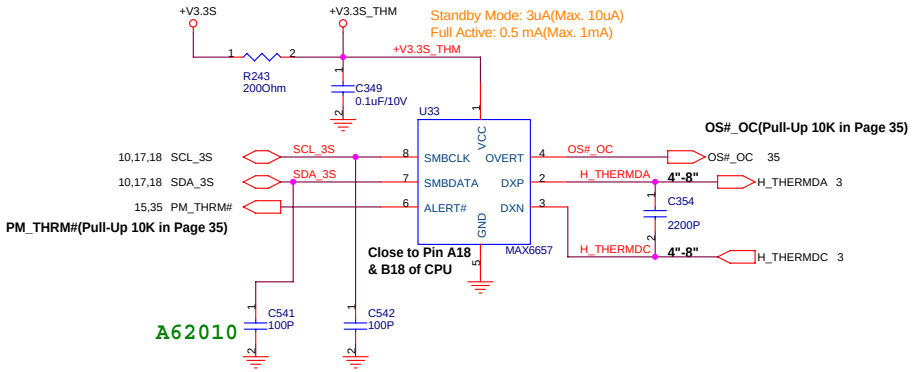
A61004

ASUSTek COMPUTER INC. NB1	Title : CPU-BANIAS(PWR)	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 4 of 51	

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



ASUSTek COMPUTER INC. NB1	Title : THERMAL	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 5 of 51	

3.8W

Thermal Power: ~ 3.8W

U32B

LxWxH=37.5x37.5x2.58

1107

DDR SYSTEM MEMORY

RG82855GM

20A3L

_DDR_DATA[63:0] 10,11
_DDR_DM[7:0] 10,11
_DDR_DQS[7:0] 10,11

(MCH-Sighting041)
M-GM system memory interface generates single pulse CKE events which may cause Intermittent hangs and display corruptions when using Micron and Infineon S0-DIMMs.

DDR_AA[12:0] 10,11
DDR_AB[2:1] 10,11
DDR_AB[5:4] 10,11

Route for COMMAND
1. DDR_AA[12:6],DDR_AA3,DDR_AA0
2. DDR_WE#
3. DDR_RAS#
4. DDR_CAS#
5. DDR_BS0#,DDR_BS1#

Route for CPC
1. DDR_AA[5:4],DDR_AA[2:1]

Route for CPC
1. DDR_AB[5:4],DDR_AB[2:1]

Route for CONTROL
1. DDR_CKE[1:0],DDR_CS[1:0]#

Route for CONTROL
DDR_CKE[3:2],DDR_CS[3:2]#

Route for CLOCK
1. CLK_DDR[2:0],CLK_DDR[2:0]#

Route for CLOCK
CLK_DDR[5:3],CLK_DDR[5:3]#

Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.

1.23125V-1.26875V
S0-S1M:Max. 80 mA
S3: 0 mA

1.225V-1.275V
S0-S1M:10 mA(Max. 50 mA)

0.2 VCCSM +/- 2%

0.8 VCCSM +/- 2%

Close to Pin AJ22

Close to Pin AJ19

ASUSTek COMPUTER INC. NB1	Title : NB-MCHM(DDR)		
	Engineer: John Hung		
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 6 of 51		

MCH_HLZCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)

MCH_HLZCOMP

MCH_HYRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)

MCH_HYRCOMP — R235 27.4Ohm

MCH_HXRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)

MCH_HXRCOMP — R226 27.4Ohm

MCH_HYSWING :
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%

MCH_HYSWING — R240 301Ohm — R241 150Ohm — C345 0.1uF/10V
Close to Pin H28

MCH_HXSWING :
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%

MCH_HXSWING — R225 301Ohm — R228 150Ohm — C328 0.1uF/10V
Close to Pin B20

LxWxH=37.5x37.5x2.58

U32A — HOST — RG82855GM

3 H_A#[31:3] — H_A#3 … H_A#31 — HA#3 … HA#31

3 H_REQ#[4:0] — H_REQ#0 … H_REQ#4 — H_REQ#0 … H_REQ#4

3 H_ADSTB#0 — H_ADSTB#0 — H_ADSTB0#
3 H_ADSTB#1 — H_ADSTB#1 — H_ADSTB1#

18 _CLK_MCH_BCLK# — HCLK#
18 _CLK_MCH_BCLK — HCLK

MCH_HYRCOMP — HYRCOMP
MCH_HYSWING — HYSWING
MCH_HXRCOMP — HXRCOMP
MCH_HXSWING — HXSWING

3 H_DSTBN#0 … 3 H_DSTBN#3 — HDSTBN#0 … HDSTBN#3
3 H_DSTBP#0 … 3 H_DSTBP#3 — HDSTBP#0 … HDSTBP#3
3 H_DINV#0 … 3 H_DINV#3 — DINV#0 … DINV#3

3 H_CPURST# — H_CPURST#

MCH_HDVREF — HDVREF0
HDVREF1
HDVREF2
MCH_HCCVREF — HCCVREF
MCH_HAVREF — HAVREF

14 HUB_PD[10:0] — HUB_PD0 … HUB_PD10 — HUB_PD0 … HUB_PD10
14 HUB_PSTRB — HUB_PSTRB
14 HUB_PSTRB# — HUB_PSTRB#
MCH_HLZCOMP — HLZCOMP
PSWING
HUB_LVREF

HUB I/F

H_D#[63:0] 3 — HD#0 … HD#63 — H_D#0 … H_D#63

H_ADS# 3
H_TRDY# 3
H_DRDY# 3
H_DEFER# 3
H_HITM# 3
H_HIT# 3
H_LOCK# 3
H_BREQ0# — H_BR0# 3
H_BNR# 3
H_BPRI# 3
H_DBSY# 3
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] 3

+V1.2S_GMCH_HI — R249 27.4Ohm — 2210
+VCCP — R49 56Ohm / H_CPURST#
+V1.2S_GMCH_HI — R251 49.9Ohm — 2210 — 0.8V +/- 2%
HUB_VSWING_MCH — R253 100Ohm — C356 0.1uF/10V
0.343V- 0.357V(Typ. 0.35V)
HUB_VREF_MCH — C362 0.01UF/10V — C363 0.1uF/10V — R262 100Ohm
+V1.2S_GMCH_HI — R252 240Ohm — 2210
2025

20A3L

MCH_HAVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)

+VCCP — 2/3(+VCCP) +/- 2% — R67 49.9Ohm — MCH_HAVREF — C81 0.1uF/10V — C79 1uF/6.3V — R66 100Ohm

MCH_HCCVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)

+VCCP — 2/3(+VCCP) +/- 2% — R270 49.9Ohm — MCH_HCCVREF — C376 0.1uF/10V — C377 1uF/6.3V — R269 100Ohm

MCH_HDVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)

+VCCP — 2/3(+VCCP) +/- 2% — R44 49.9Ohm — MCH_HDVREF — C48 0.1uF/10V — C44 0.1uF/10V — C46 0.1uF/10V — C52 1uF/6.3V — R46 100Ohm

2210

R249:
27.4ohm (10-003412704) for 855GM/852GM
37.4ohm (10-003413704) for 855GME
48.7ohm (10-003414807) for 852GME/852GMV

2210

R251:
49.9ohm (10-003414909) for 855GM/852GM
68.1ohm (10-003416801) for 855GME
86.6ohm (10-003418606) for 852GME/852GMV

2210

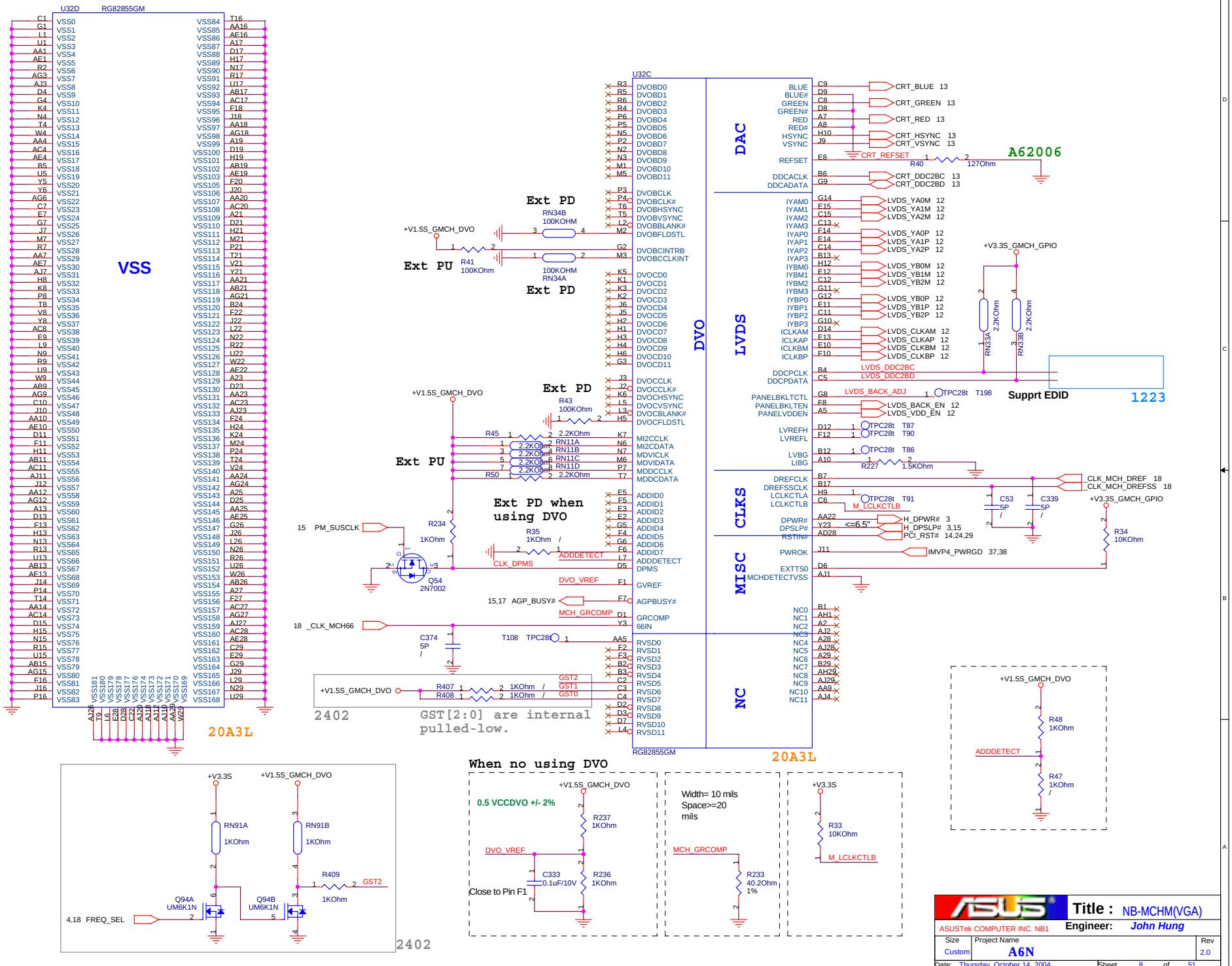
R252:
240ohm (10-003412410) for 855GM/852GM
287ohm (10-003412817) for 855GME
324ohm (10-003413214) for 852GME/852GMV

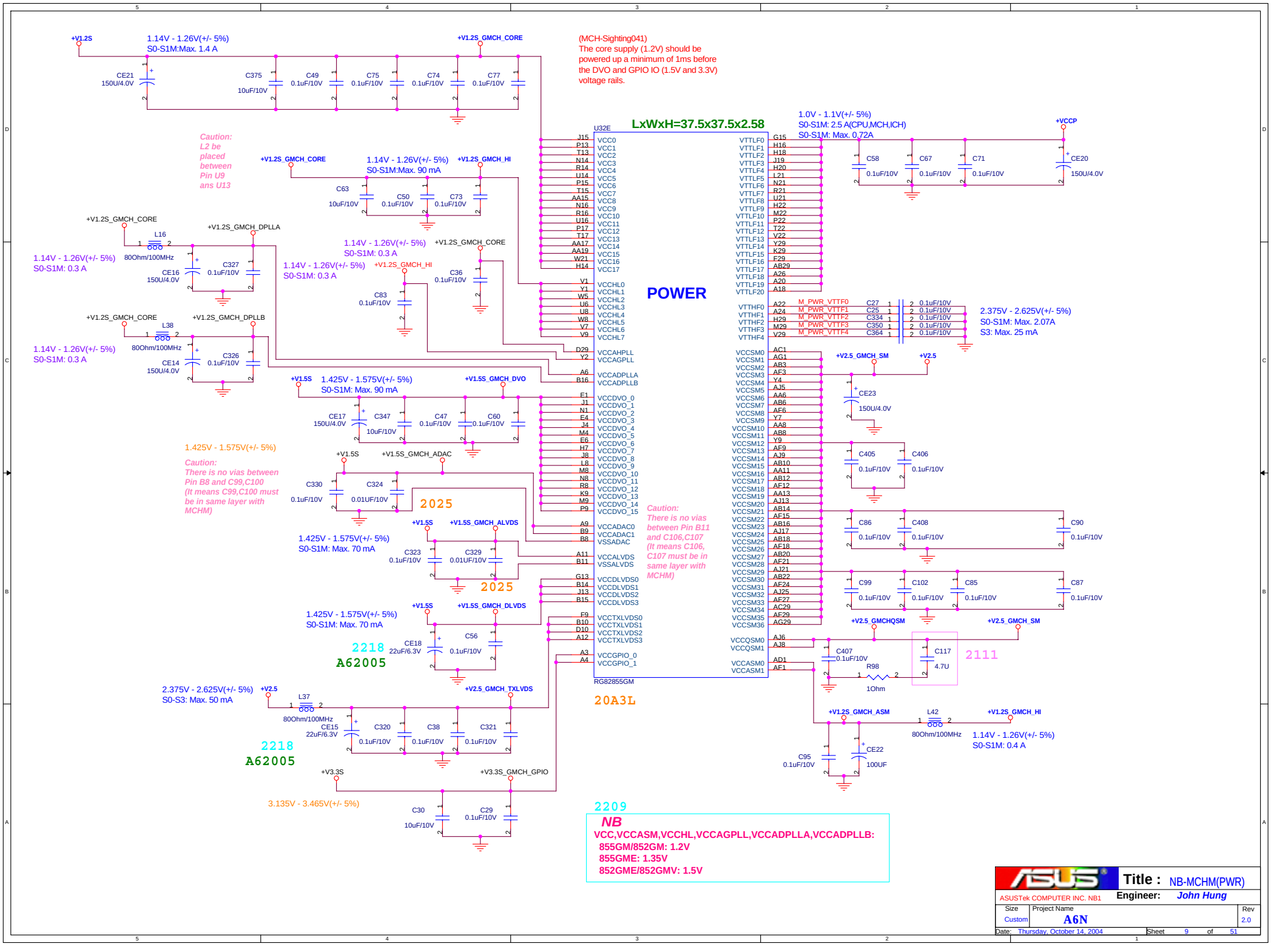
ASUSTek COMPUTER INC. NB1

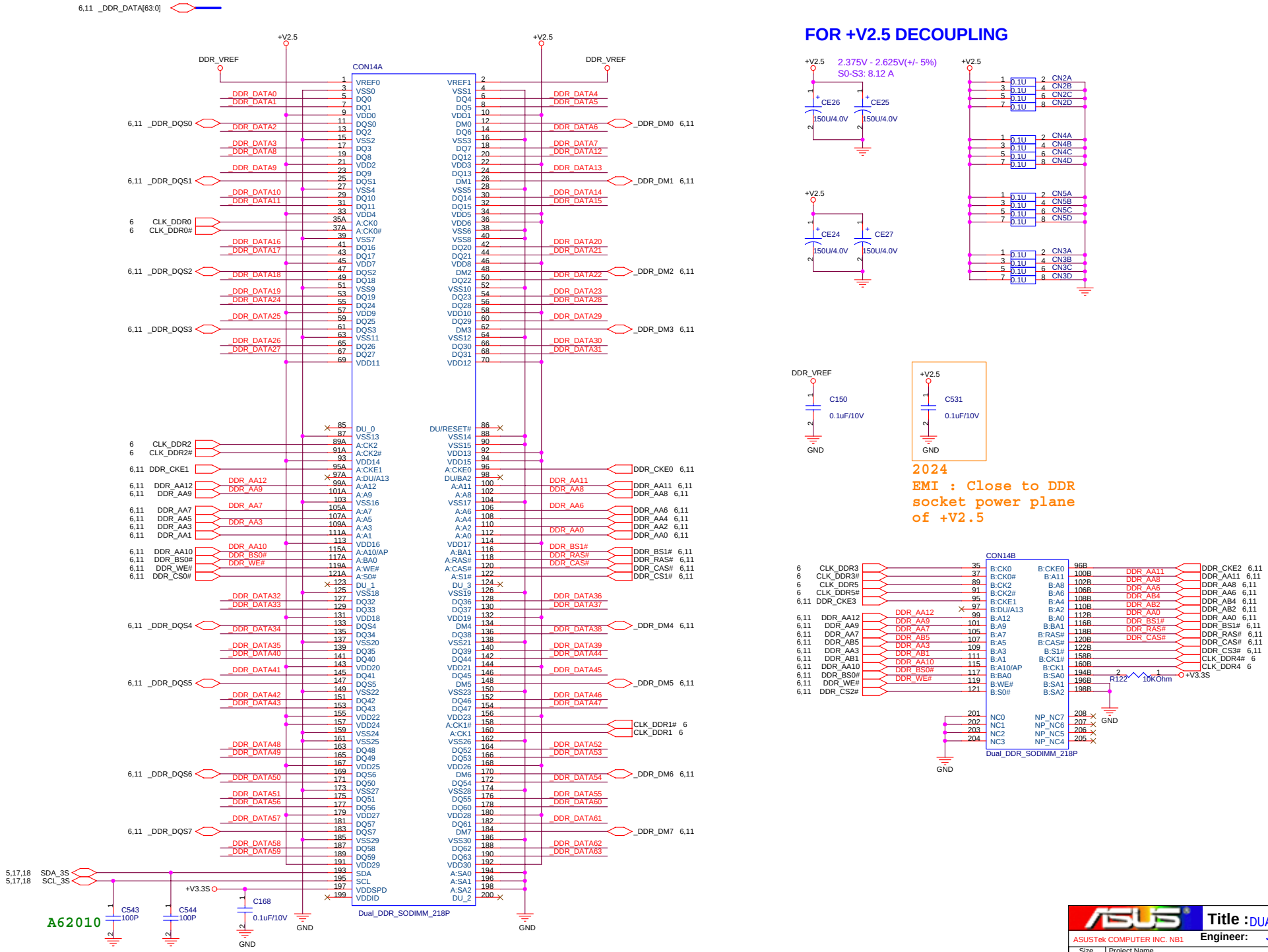
Title : NB-MCHM(HOST)
Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 7 of 51

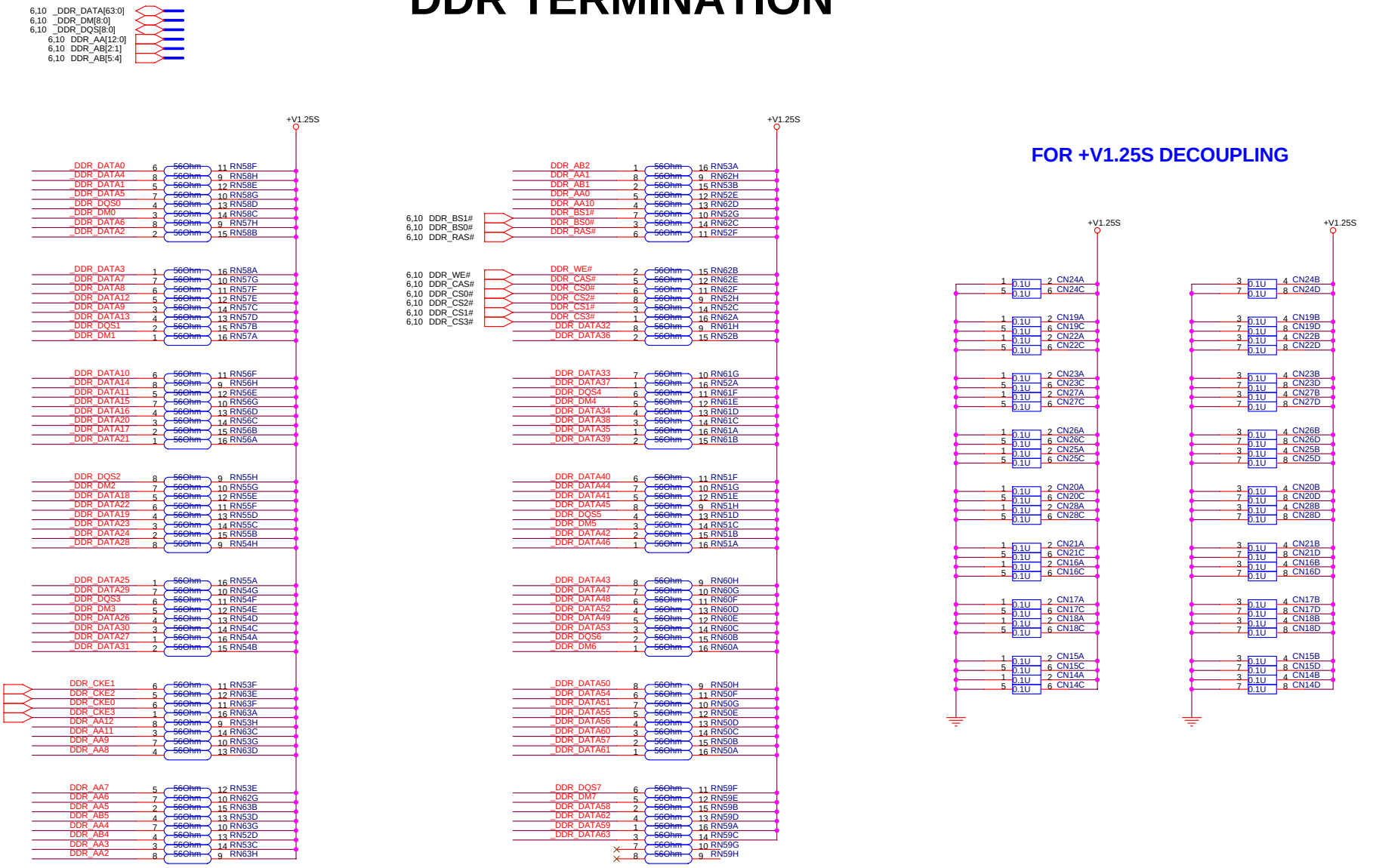

U32D RG82855GM
VSS
20A3L
U32C
DVO
DAC
LVDS
CLKS
MISC
NC
RG82855GM
20A3L
Ext PD
Ext PU
Ext PD when using DVO
GST[2:0] are internal pulled-low.
2402
When no using DVO
0.5 VCCDVO +/- 2%
Close to Pin F1
Width= 10 mils
Space>=20 mils
A62006
Supprt EDID
1223
ASUSTek COMPUTER INC. NB1
Title : NB-MCHM(VGA)
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 8 of 51


(MCH-Sighting041)
The core supply (1.2V) should be powered up a minimum of 1ms before the DVO and GPIO IO (1.5V and 3.3V) voltage rails.
LxWxH=37.5x37.5x2.58
U32E
RG82855GM
20A3L
POWER
+V1.2S
1.14V - 1.26V(+/- 5%)
S0-S1M:Max. 1.4 A
+V1.2S_GMCH_CORE
+V1.2S_GMCH_HI
S0-S1M:Max. 90 mA
+V1.2S_GMCH_DPLLA
+V1.2S_GMCH_DPLLB
S0-S1M: 0.3 A
80Ohm/100MHz
+V1.5S
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 90 mA
+V1.5S_GMCH_DVO
+V1.5S_GMCH_ADAC
+V1.5S_GMCH_ALVDS
S0-S1M: Max. 70 mA
+V1.5S_GMCH_DLVDS
+V2.5
2.375V - 2.625V(+/- 5%)
S0-S3: Max. 50 mA
+V2.5_GMCH_TXLVDS
+V3.3S
+V3.3S_GMCH_GPIO
3.135V - 3.465V(+/- 5%)
1.0V - 1.1V(+/- 5%)
S0-S1M: 2.5 A(CPU,MCH,ICH)
S0-S1M: Max. 0.72A
+VCCP
2.375V - 2.625V(+/- 5%)
S0-S1M: Max. 2.07A
S3: Max. 25 mA
+V2.5_GMCH_SM
+V2.5_GMCHQSM
+V1.2S_GMCH_ASM
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.4 A
Caution:
L2 be placed between Pin U9 ans U13
Caution:
There is no vias between Pin B8 and C99,C100 (It means C99,C100 must be in same layer with MCHM)
Caution:
There is no vias between Pin B11 and C106,C107 (It means C106, C107 must be in same layer with MCHM)
2025
2218
A62005
2111
2209
NB
VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB:
855GM/852GM: 1.2V
855GME: 1.35V
852GME/852GMV: 1.5V
Title : NB-MCHM(PWR)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size: Custom
Project Name: A6N
Rev: 2.0
Date: Thursday, October 14, 2004
Sheet 9 of 51



ASUSTek COMPUTER INC. NB1	Title : DUAL DDR SODIMM		
	Engineer: John Hung		
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 10 of 51		

DDR TERMINATION



FOR +V1.25S DECOUPLING

ASUSTek COMPUTER INC. NB1

Title : DDR TERMINATION

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 11 of 51

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output D/A signal (adjust voltage level) to adjust Back light.

A3N use D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

USB PORT 5 for CAMERA

LCD	CABLE ID:	PID3	PID2	PID1	PID0
14.1	XGA	1	1	1	1
15.1	XGA	1	1	0	1
15.1	SXGA+	1	0	1	1
15.1	WXGA	1	1	1	0
15.1	WSXGA+	0	1	1	1

RN86A,B: page 20

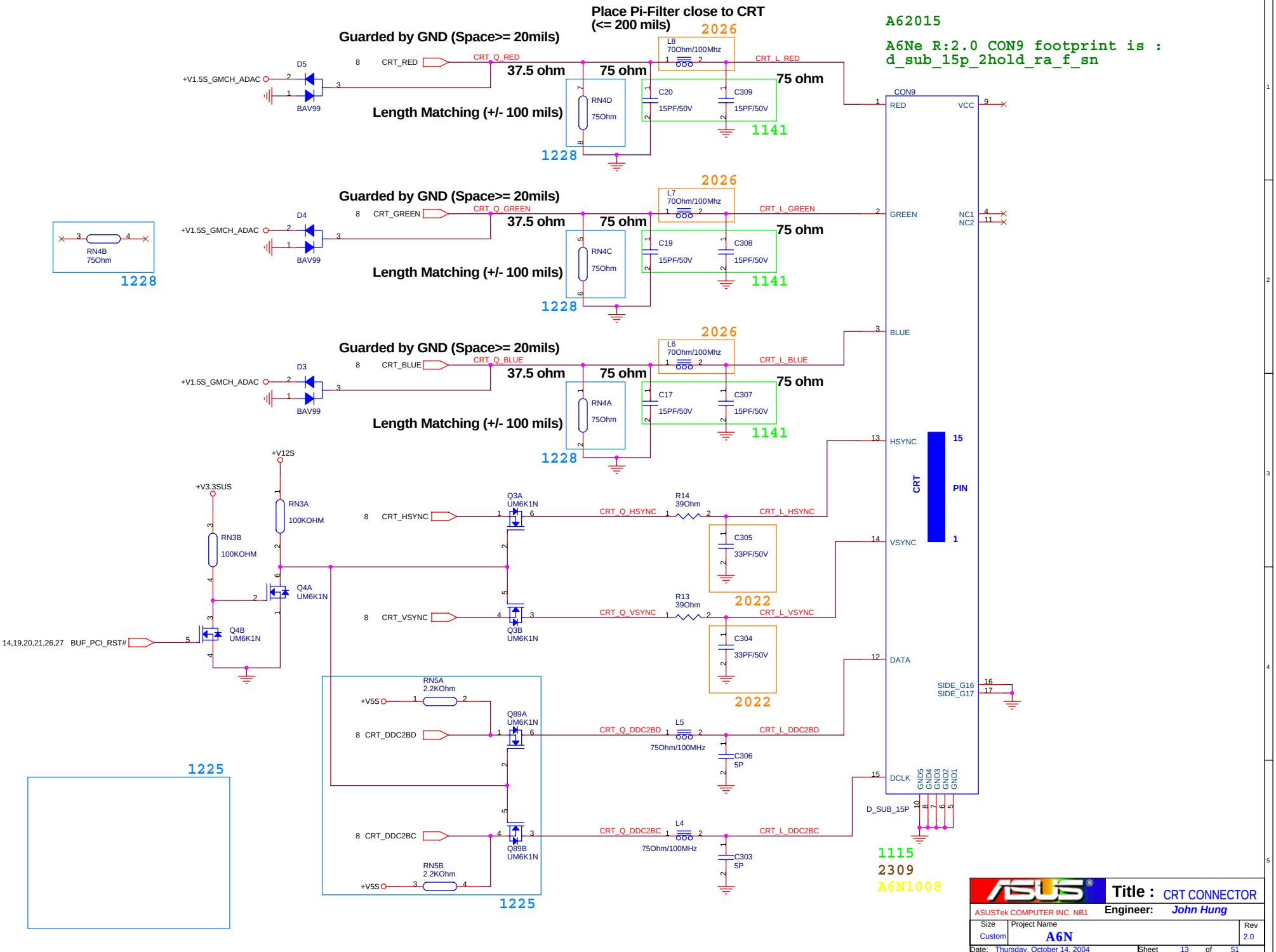
LCD Power

SI3865: US$0.22

3-3.6V
S0-S1M:410 mA(500 mA Max.)

Caution:
Must tune R369 & C270 to meet Panel Spec

Title :	LVDS & BACKLIGHT		
ASUSTek COMPUTER INC. NB1	Engineer:	John Hung	
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 12 of 51		


Place Pi-Filter close to CRT
(<= 200 mils)
A62015
A6Ne R:2.0 CON9 footprint is :
d_sub_15p_2hold_ra_f_sn
Guarded by GND (Space>= 20mils)
Length Matching (+/- 100 mils)
37.5 ohm
75 ohm
CRT_RED
CRT_Q_RED
CRT_L_RED
CRT_GREEN
CRT_Q_GREEN
CRT_L_GREEN
CRT_BLUE
CRT_Q_BLUE
CRT_L_BLUE
+V1.5S_GMCH_ADAC
D5
D4
D3
BAV99
L8
L7
L6
70Ohm/100Mhz
RN4D
RN4C
RN4A
75Ohm
C20
C19
C17
C309
C308
C307
15PF/50V
2026
1141
1228
RN4B
75Ohm
CON9
RED
GREEN
BLUE
VCC
NC1
NC2
HSYNC
VSYNC
DATA
DCLK
CRT
15
PIN
1
SIDE_G16
SIDE_G17
GND5
GND4
GND3
GND2
GND1
D_SUB_15P
+V12S
+V3.3SUS
RN3A
100KOHM
RN3B
100KOHM
Q4A
UM6K1N
Q4B
UM6K1N
14,19,20,21,26,27 BUF_PCI_RST#
Q3A
UM6K1N
Q3B
UM6K1N
CRT_HSYNC
CRT_VSYNC
CRT_Q_HSYNC
CRT_Q_VSYNC
CRT_L_HSYNC
CRT_L_VSYNC
R14
39Ohm
R13
39Ohm
C305
C304
33PF/50V
2022
RN5A
2.2KOhm
RN5B
2.2KOhm
+V5S
Q89A
UM6K1N
Q89B
UM6K1N
CRT_DDC2BD
CRT_DDC2BC
CRT_Q_DDC2BD
CRT_Q_DDC2BC
CRT_L_DDC2BD
CRT_L_DDC2BC
L5
L4
75Ohm/100MHz
C306
C303
5P
1225
1115
2309
A6N1008
Title : CRT CONNECTOR
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size
Custom
Project Name
A6N
Rev
2.0
Date: Thursday, October 14, 2004
Sheet 13 of 51

Use Daisy-Chain Topology

PCI_REQ#	PCI_REQ#?
CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL	PCI_AD?
CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

LxWxH=31x31x2.38

U20A — FW82801DBM

19,20,21,22 PCI_AD[31:0]

PCI_AD0 H5, PCI_AD1 J3, PCI_AD2 H3, PCI_AD3 K1, PCI_AD4 G5, PCI_AD5 J4, PCI_AD6 H4, PCI_AD7 J5, PCI_AD8 K2, PCI_AD9 G2, PCI_AD10 L1, PCI_AD11 G4, PCI_AD12 L2, PCI_AD13 H2, PCI_AD14 L3, PCI_AD15 F5, PCI_AD16 F4, PCI_AD17 N1, PCI_AD18 E5, PCI_AD19 N2, PCI_AD20 E3, PCI_AD21 N3, PCI_AD22 E4, PCI_AD23 M5, PCI_AD24 E2, PCI_AD25 P1, PCI_AD26 E1, PCI_AD27 P2, PCI_AD28 D3, PCI_AD29 R1, PCI_AD30 D2, PCI_AD31 P4

HUB_PD[10:0] 7

HUB_PD0 L19, HUB_PD1 L20, HUB_PD2 M19, HUB_PD3 M21, HUB_PD4 P19, HUB_PD5 R19, HUB_PD6 T20, HUB_PD7 R20, HUB_PD8 P23, HUB_PD9 L22, HUB_PD10 N22, HUB_PD11 K21 — <=6" / <=8"

R314 56Ohm

HUB_PSTRB# 7, HUB_PSTRB 7

HUB_RCOMP_ICH4, HUB_VSWING_ICH4

LPC_AD0 20,26,27; LPC_AD1 20,26,27; LPC_AD2 20,26,27; LPC_AD3 20,26,27; LPC_FRAME# 20,26,27; T48 TPC28t; LPC_DRQ#0 27

19,20,21 PCI_C/BE#0, PCI_C/BE#1, PCI_C/BE#2, PCI_C/BE#3

17,21 PCI_REQ#0; 17,20 PCI_REQ#1; 17,19 PCI_REQ#2; 17 PCI_REQ#3; 17 PCI_REQ#4

+V3.3S — RN28A 10KOhm, RN28B 10KOhm

PCI_DEVSEL# 17,19,20,21; PCI_FRAME# 17,19,20,21; PCI_IRDY# 17,19,20,21; PCI_TRDY# 17,19,20,21; PCI_STOP# 17,19,20,21; PCI_PAR 19,20,21; PCI_PERR# 17,19,20,21

PME_SB#; PCI_SERR# 17,19,20,21; PCI_LOCK# 17; PCI_RST# 8,24,29

4"-8.5"; PM_CLKRUN# 20,21,26; CLK_ICHPCI 18

21 PCI_GNT#0; 20 PCI_GNT#1; 19 PCI_GNT#2

T43 TPC28t, T49 TPC28t, T46 TPC28t, T150 TPC28t

C455 5P

ICH4 pin E8

Strap Option

Default: Pull-High 20K
Pull-Down for BIOS
TOP-BLOCK SWAP

5 10KOhm 6 RN30C

+V3.3S — RN30D 10KOhm

+V3.3 — C178 0.1uF/10V

PCI_RST# — U17 NC7SZ08P5X — BUF_PCI_RST# 13,19,20,21,26,27

Meet LPC reset >= 60 us
(Add Buffer)

+V3.3 — RN30A 10KOhm; RN30B 10KOhm

Q36 PMBS3904

20,21,27 PCI_PME# — PME_SB# — 19 PME_SB#

pull up to VccSus3_3 by internal pull-up resistor

Strap Option

Default: Pull-Down
Pull-High for Hub Interface 1.5 Buffer Mode

ICH4 USE

+V1.5S_ICH — R310 48.7Ohm — HUB_RCOMP_ICH4

1109

R-ICH4 <= 0.5"

0.8V +/- 2% ICH4(R22)<=3"

+V1.5S_ICH — R132 130Ohm — HUB_VSWING_ICH4 — C436 0.01UF/10V, C439 0.1uF/10V, R133 150Ohm

2025

Caution:
The VREF of HUB interface is 0.35V
The VSWING of HUB interace is 0.8V
But in Intel CRB, their naming convention will make people confused.

ASUSTek COMPUTER INC. NB1

Title : ICH4-M(HUBPCI)

Engineer: *John Hung*

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 14 of 51

USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Pair Width/Space: 7/10 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils

LxWxH=31x31x2.38

U20C

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBRBIAS USBRBIAS# OC0# OC1# OC2# OC3# OC4# OC5# AGPBUSY#/GPIO6 C3_STAT#/GPIO21 CPUPERF#/GPIO22 DPRSLPVR LAN_RST# PWRBTN# PWROK RI# RSMRST# SLP_S1#/GPIO19 SLP_S3# SLP_S4# SLP_S5# STP_PCI#/GPIO18 STP_CPU#/GPIO20 SSMUXSEL/GPIO23 SUSCLK SUS_STAT#/LPCPD# SYS_RESET# THRM# THRMTRIP# VGATE/VRMPWRGD

GPIO7 GPIO8 GPIO12 GPIO13 GPIO25 GPIO27 GPIO28 GPIO32 GPIO33 GPIO34 GPIO35 GPIO36 GPIO37 GPIO38 GPIO39 GPIO40 GPIO41 GPIO42 GPIO43 A20GATE A20M# CPUPWRGD CPUSLP# DPSLP# FERR# IGNNE# INIT# INTR NMI SMI# STPCLK# RCIN#

USB_PN0 USB_PP0 USB_PN1 USB_PP1 USB_PN2 USB_PP2 USB_PN3 USB_PP3 USB_PN5 USB_PP5 USB_OC#01 USB_OC#23 USB_OC#4 USB_OC#5 AGP_BUSY# PM_DPRSLPVR PM_PWRBTN# ICH4_PWROK PM_RI# PM_RSMRST# SLP_S1# PM_SLP_S3# PM_SLP_S4# PM_STPPCI# PM_STPCPU# PM_SUSCLK PM_SYSRST# PM_THRM# H_THRMTRIP_S# PM_VGATE

EXTSMI#_3A KBDSCI_3A SIO_SMI# CB_SD# 802_LED_EN# BACK_OFF# PID_0_ICH4 PID_1_ICH4 PID_2_ICH4 PID_3_ICH4 CG_FS0 CG_FS1 CG_FS2 CG_FS5 CG_FS6 FWH_WP# CPUFAN_SPD_A HA20GATE H_A20M# H_PWRGD H_CPUSLP# H_DPSLP# H_FERR# H_IGNNE# H_INIT# H_INTR H_NMI H_SMI# H_STPCLK# KBDCPURST

FW82801DBM

A6N1002 2108 R138 22.6Ohm USBRBIAS <=0.5"

USBRBIAS:
W/S: 5/5 mils
Length: <= 0.5"

A6N1002

RN31C 10KOhm 1201

+V3.3S_ICH +V3.3SUS_ICH RN31D RN31A RN31B 10KOhm

1104 CB_SD# 21 WLAN_ON# 12,20

1219 2021 1212

R139 56Ohm R156 56Ohm R313 56Ohm <=3" R383 1KOhm

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils

LxWxH=31x31x2.38

U20B

IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15

PDD0 PDD1 PDD2 PDD3 PDD4 PDD5 PDD6 PDD7 PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15

SDD0 SDD1 SDD2 SDD3 SDD4 SDD5 SDD6 SDD7 SDD8 SDD9 SDD10 SDD11 SDD12 SDD13 SDD14 SDD15

IDE_SDD0 IDE_SDD1 IDE_SDD2 IDE_SDD3 IDE_SDD4 IDE_SDD5 IDE_SDD6 IDE_SDD7 IDE_SDD8 IDE_SDD9 IDE_SDD10 IDE_SDD11 IDE_SDD12 IDE_SDD13 IDE_SDD14 IDE_SDD15

IDE_SDD[15:0] 25

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils

IDE_PDA0 IDE_PDA1 IDE_PDA2 PDCS1# PDCS3# PIORDY PDIOW# PDIOR# PDDACK# PDDREQ

SDA0 SDA1 SDA2 SDCS1# SDCS3# SIORDY SDIOW# SDIOR# SDDACK# SDDREQ

IDE_SDA0 IDE_SDA1 IDE_SDA2 IDE_SDCS1# IDE_SDCS3# IDE_SIORDY IDE_SDIOW# IDE_SDIOR# IDE_SDDACK# IDE_SDDREQ

LAN_CLK LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2 LAN_RSTSYNC

AC_RST# AC_SYNC AC_BIT_CLK AC_SDOUT AC_SDIN0 AC_SDIN1 AC_SDIN2

AC97_SYNC AC97_SDOUT AC97_RST# 30,33 AC97_BCLK_ICH4 30 AC97_SDIN0 30 AC97_SDIN1 33

AC97 | AC97_SDIN0
MDC | AC97_SDIN1

INTRUDER# SMLINK0 SMLINK1 SM_INTRUDER# 17 SM_LINK0 17 SM_LINK1 17

SERIRQ PIRQA# PIRQB# PIRQC# PIRQD# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5 IRQ14 IRQ15 APICCLK APICD0 APICD1

17,20,21,26,27 INT_SERIRQ 17,22 PCI_INTA# 17,22 PCI_INTB# 17,19,20 PCI_INTC# 17,20,22 PCI_INTD# 17 ICH4_GPI2 17 ICH4_GPI3 17 ICH4_GPI4 17 ICH4_GPI5 17,24 INT_IRQ14 17,25 INT_IRQ15

RN68A 10KOhm RN68B 10KOhm

CLK66 CLK48 CLK14 RTCRST# SPKR BATLOW#/TP[0] SMBALERT#/GPIO11 SMBCLK SMBDATA

_CLK_ICH66 18 _CLK_ICH48 18 _CLK_ICH14 18 RTC_RST# ICH4_SPKR 30 PM_BATLOW# 17 LID_ICH4#_3A 37 SCL_3A 17 SDA_3A 17

C191 5P C186 5P C184 5P C539 150PF/50V C540 150PF/50V

A62010

RTC_X2 RTC_X1 RTCX2 RTCX1 AC6 AC7

FW82801DBM

GPIO[32:43] default:
Output High
ICH4 EDS R:1.0 page 10-94
10.10.8, 10.10.9

RTC CIRCUITRY

G3: 5 uA

T201 TPC28t RTC_BAT BAT1 BATT

T200 TPC28t +V3.3A D18 RB715F

+V_RTC

RC time delay should be 10-20 ms

R383 1KOhm R156 180KOhm C212 1UF/10V C213 0.1uF/10V RTC_RST#

C225 0.047UF/10V RTC_VBIAS RTC_VBIAS 16

1215 2206 2121

C216 18P X2 SIDE 32.768KHZ +/-20ppm/12.5PF C220 18P

R170 10MOhm R166 10MOhm RTC_X1 RTC_X2

Vpeak-peak of RTC_X1 < 1V

RTC Circuits:
RTC_RST#, RTC_VBIAS, RTC_X1, RTC_X2
Width= 5 mils
Length<=1"
Need GND Guard

Measure duty-cycle of SUSCLK
(Pin AA4) must be in 30-70%

A2.1 PCB uses "xtal_3p_319x108" footprint, but the SMT recommended 1st source part uses "xtal_3p_335x110" footprint.

AC97 SDIN

ICH4 R2 AMC AC97

Outer Layer: 5 mils
W/S= 1:1
ICH4-R2: 0.9"- 13.6"
AC97-R2: 0.1"-0.4"

(#0013)

AC97_SDIN0 AC97_SDIN1

INTEL REQUEST

+V3.3 U38 NC7SZ08P5X C472 0.1uF/10V

PM_SLP_S3# SLP_S1# PM_SLP_S1# 18,35

AC97 SDOUT & SYNC

ICH4 T R2 AMC
R1
AC97

Outer Layer: 5 mils
W/S= 1:1
ICH4-(T): 1"- 8"
R1-(T): 0.1"- 0.4"
AC97-R1: <=5.6"
R2-(T): 0.1"- 0.4"
AMC-R2: 0.9"-5.6"

2119

AC97_SYNC /CUSTOMER R143 33Ohm AC97_SYNC_MDC 33 R141 33Ohm AC97_SYNC_CODEC 30

AC97_SDOUT /CUSTOMER R144 33Ohm AC97_SDOUT_MDC 33 R142 33Ohm AC97_SDOUT_CODEC 30

1 to 8 inches 0.1 to 0.4 inches 0.9 to 5.6 inches

T type routing, place R at branch point.

+V3.3S_ICH AC97_SDOUT

Strap Option Default: Pull-Down 20K

PID_0_ICH4 PID_1_ICH4 PID_2_ICH4 PID_3_ICH4 2.2KOhm RN89B RN89A RN89C RN89D PID_0 12 PID_1 12 PID_2 12 PID_3 12

2021

+V3.3S_ICH Strap Option PM_DPRSLPVR 38

Default: Pull-Down 20K
Pull-High for Not Supported

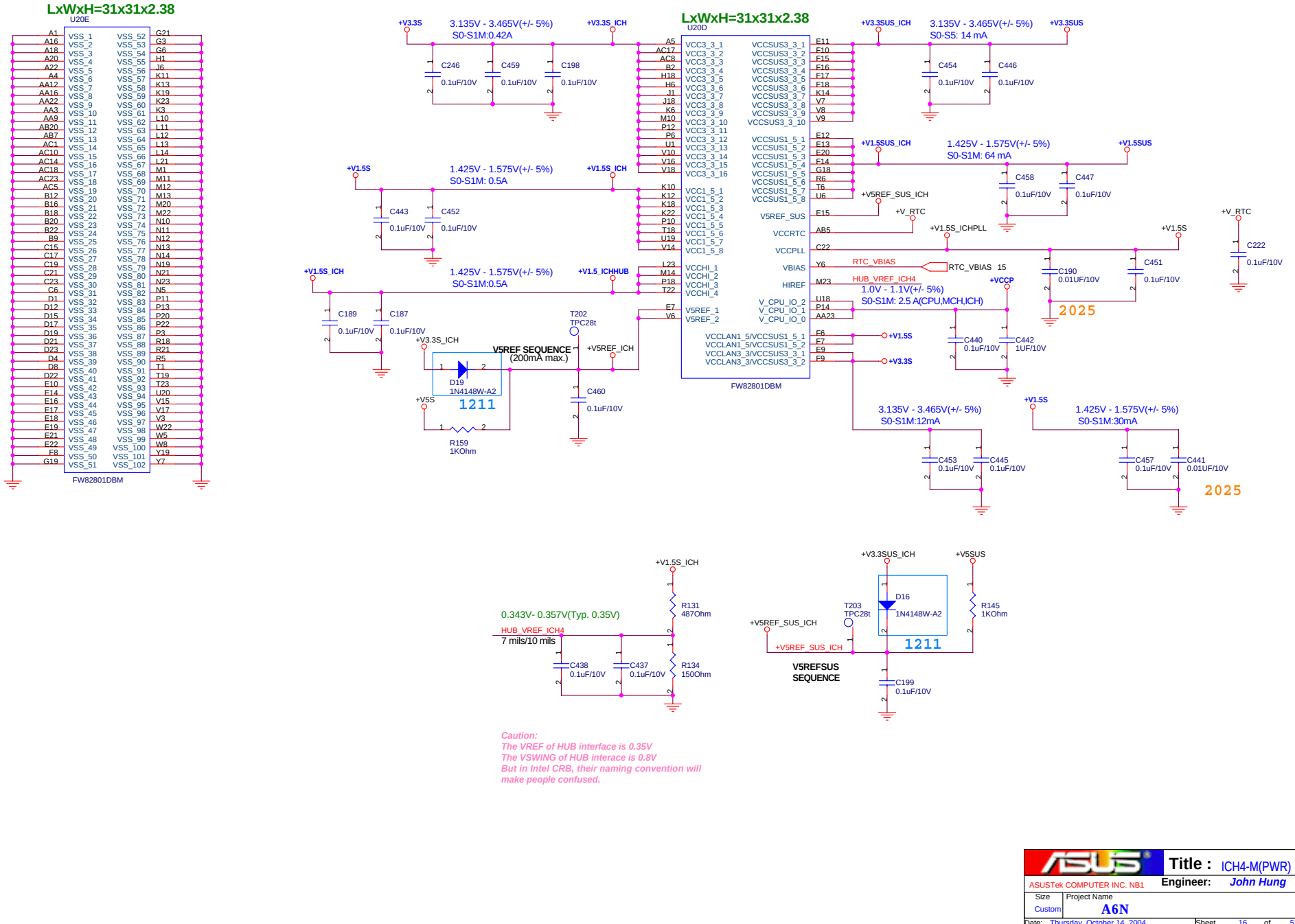
ASUSTek COMPUTER INC. NB1

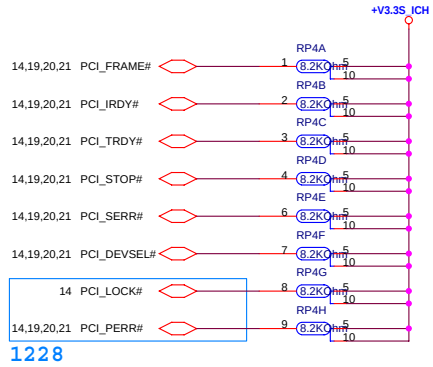
Title : ICH4-M(H_U_IDE_PM)

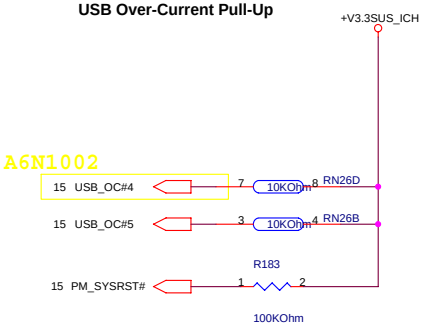
Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

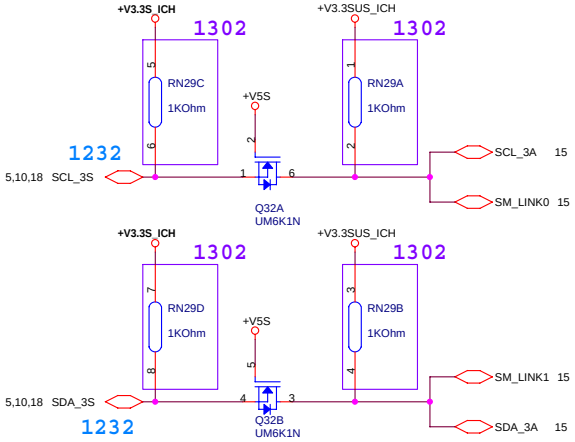
Date: Thursday, October 14, 2004 Sheet 15 of 51


LxWxH=31x31x2.38
U20E
FW82801DBM
LxWxH=31x31x2.38
U20D
FW82801DBM
+V3.3S
3.135V - 3.465V(+/- 5%)
S0-S1M:0.42A
+V3.3S_ICH
C246 0.1uF/10V
C459 0.1uF/10V
C198 0.1uF/10V
+V3.3SUS_ICH
3.135V - 3.465V(+/- 5%)
S0-S5: 14 mA
+V3.3SUS
C454 0.1uF/10V
C446 0.1uF/10V
+V1.5S
1.425V - 1.575V(+/- 5%)
S0-S1M: 0.5A
+V1.5S_ICH
C443 0.1uF/10V
C452 0.1uF/10V
+V1.5SUS_ICH
1.425V - 1.575V(+/- 5%)
S0-S1M: 64 mA
+V1.5SUS
C458 0.1uF/10V
C447 0.1uF/10V
+V5REF_SUS_ICH
+V_RTC
+V1.5S_ICHPLL
+V1.5S
+V_RTC
C222 0.1uF/10V
C451 0.1uF/10V
C190 0.01UF/10V
2025
RTC_VBIAS
RTC_VBIAS 15
HUB_VREF_ICH4
1.0V - 1.1V(+/- 5%)
S0-S1M: 2.5 A(CPU,MCH,ICH)
+VCCP
C440 0.1uF/10V
C442 1UF/10V
+V1.5S_ICH
1.425V - 1.575V(+/- 5%)
S0-S1M:0.5A
+V1.5_ICHHUB
C189 0.1uF/10V
C187 0.1uF/10V
T202
TPC28t
+V3.3S_ICH
V5REF SEQUENCE
(200mA max.)
+V5REF_ICH
D19
1N4148W-A2
1211
+V5S
R159
1KOhm
C460 0.1uF/10V
+V1.5S
+V3.3S
3.135V - 3.465V(+/- 5%)
S0-S1M:12mA
C453 0.1uF/10V
C445 0.1uF/10V
+V1.5S
1.425V - 1.575V(+/- 5%)
S0-S1M:30mA
C457 0.1uF/10V
C441 0.01UF/10V
2025
+V1.5S_ICH
0.343V- 0.357V(Typ. 0.35V)
HUB_VREF_ICH4
7 mils/10 mils
R131
487Ohm
C438 0.1uF/10V
C437 0.1uF/10V
R134
150Ohm
+V3.3SUS_ICH
+V5SUS
D16
1N4148W-A2
T203
TPC28t
+V5REF_SUS_ICH
+V5REF_SUS_ICH
1211
R145
1KOhm
V5REFSUS
SEQUENCE
C199 0.1uF/10V
Caution:
The VREF of HUB interface is 0.35V
The VSWING of HUB interface is 0.8V
But in Intel CRB, their naming convention will
make people confused.
Title : ICH4-M(PWR)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size: Custom
Project Name: A6N
Rev: 2.0
Date: Thursday, October 14, 2004
Sheet 16 of 51

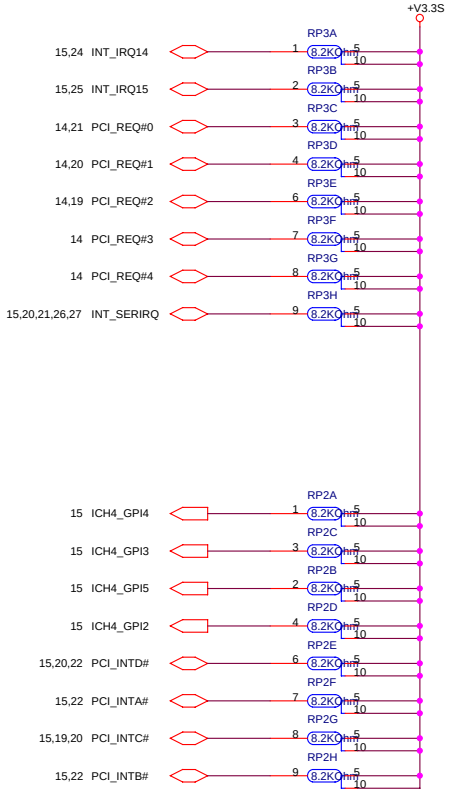


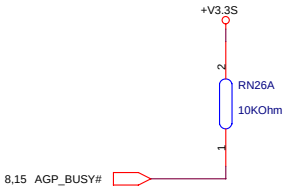


ICH4 SMLink & SMbus must be tied together



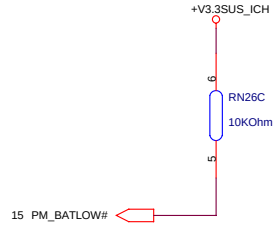
Can Swap





BATTERY LOW

ICH4



ASUSTek COMPUTER INC. NB1

Title : ICH4-M(PULLUP)

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 17 of 51

2308

+V1.8S +V1.8S_VCCA

R403 0Ohm

T220TPC28t

+V3.3S

R402 10KOhm

+V1.8S_VCCA

TPC28t T221

FREQ_SEL 4,8

R401 1KOhm

U54 SWITCH_4P

+V1.8S

1(H): FSB Freq=133MHz & VCCA[0]=1.5V
4(L): FSB Freq=100MHz & VCCA[0]=1.8V

2: Dothan(533) CPU
3: Celeron/Banias /Dothan(400) CPU

U54 switch to 1,pin1 & 4 open
U54 switch to 4,pin1 & 4 short

2208

CLK33 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: same as CLK66

CLK66 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: +/- 100 mils

CLK_EN# is OD for MAX1987

38 CLK_EN#

+V3.3S_CLK

R274 10KOhm

FS4	FS3	FUNCTION
0	0	100MHz
0	1	133MHz (D)
1	0	200MHz
1	1	166MHz

1105

1106

R368 1KOhm

For A3LE:
Load R401, R402, U54

For A3N/A3NE/A3L:
Load R403, R368

2220

2208

2208

U5

Vtt_PWRGD# 18

VID5 40
VID4 39
VID3 38
VID2 37
VID1 36
VID0 35

FS3/PCICLK_F0 5

FS4/PCICLK_F1 6

ASEL/PCICLK_F2 7

MULTSEL0/PCICLK0 10

MODE/PCICLK1 11

PCICLK2 12

PCICLK3 13

PCICLK4 16

PCICLK5 17

3V66_0 25

3V66_1 26

3V66_2 27

3V66_3/48MHz_2 29

ICS950815

14 _CLK_ICHPCI 4"-8.5" R79 33.2Ohm CLK_ICHPCI <=0.5" C389 10P

21 _CLK_CBPCI 4"-8.5" R80 33.2Ohm CLK_CBPCI <=0.5" C390 10P

20 _CLK_MINIPCI 4"-8.5" R81 33.2Ohm CLK_MINIPCI <=0.5" C391 10P

27 _CLK_SIOPCI 4"-8.5" R82 33.2Ohm CLK_SIOPCI <=0.5" C392 10P

26 _CLK_KBCPCI 4"-8.5" R83 33.2Ohm CLK_KBCPCI <=0.5" C393 10P

27 _CLK_FWHPCI 4"-8.5" R84 33.2Ohm CLK_FWHPCI <=0.5" C394 10P

19 _CLK_LANPCI 4"-8.5" R85 33.2Ohm CLK_LANPCI <=0.5" C395 10P

15 _CLK_ICH66 4"-8.5" R86 33.2Ohm CLK_ICH66 <=0.5" C396 10P

8 _CLK_MCH66 4"-8.5" R87 33.2Ohm CLK_MCH66 <=0.5" C397 10P

8 _CLK_MCH_DREFSS C524 10P R267 33.2Ohm CLK_MCH_DREFSS <=0.5"

1142

ECERA 30PF/30PPM X6

CLK_X1 <=0.5" C96 33PF/50V

CLK_X2 <=0.5" 14.318Mhz C93 33PF/50V

X1 X2

I2C address: D2H
3.3V+/-5%
S1M: 40 mA
S0: 360 mA

FS1	FS0	FUNCTION
0	0	66 MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz

+V3.3S_CLK

VDDREF 1
VDDPCI1 8
VDDPCI2 14
VDD3V66 23
VDDCPU1 50
VDDCPU2 46

+V3.3S_CLKA

VDDA 20

+V3.3S_CLK48

VDD48 34

CPUCLKT2 45 CLK_MCH_BCLK <=0.5" R59 33.2Ohm <=0.2" 2"- 8" _CLK_MCH_BCLK 7 <=0.5" R265 49.9Ohm

CPUCLKC2 44 CLK_MCH_BCLK# <=0.5" R60 33.2Ohm <=0.2" 2"- 8" _CLK_MCH_BCLK# 7 <=0.5" R266 49.9Ohm

CPUCLKT1 49 CLK_CPU_BCLK <=0.5" R57 33.2Ohm <=0.2" 2"- 8" _CLK_CPU_BCLK 3 <=0.5" R51 49.9Ohm

CPUCLKC1 48 CLK_CPU_BCLK# <=0.5" R58 33.2Ohm <=0.2" 2"- 8" _CLK_CPU_BCLK# 3 <=0.5" R52 49.9Ohm

CPUCLKT0/(FS6) 52 CG_FS6 15

CPUCLKC0/(FS5) 51 CG_FS5 15

CLK_CPU_BCLK/# must be low in C3

HOST_CLK GROUP
In L3 or L6
Pair Width/Space:4/4 mils
Group Space:>= 25 mils
Length Match: +/- 10 mils

REF0 56 CLK_ICH14 <=0.5" R68 33.2Ohm 4"-8.5" C88 10P _CLK_ICH14 15

CLK_MCH_DREF R64 33.2Ohm 3"-12" C372 10P _CLK_MCH_DREF 8

48MHz_1 31 <=0.5" R63 33.2Ohm 3"-12" C371 10P _CLK_SIO_48M 27 2208

48MHz_0 32 CLK_48M <=0.5" R62 33.2Ohm 3"-12" _CLK_ICH48 15

SDATA 30 SDA_3S 5,10,17 C370 10P
SCLK 28 SCL_3S 5,10,17

CPU_STOP# 53 PM_STPCPU# 15,38
PCI_STOP# 22 PM_STPPCI# 15
PD# 19 PM_SLP_S1# 15,35

IREF 43 R61 475Ohm

+V3.3S_CLK

R263 10KOhm

R264 / 1KOhm

FS2 41 CG_FS2 15
FS1 55 CG_FS1 15

R55 10KOhm

FS0 54 CG_FS0 15

R56 10KOhm

A62010

C545 100P C546 100P

GND8 47 GND7 42 GND6 33 GND5 24 GND4 21 GND3 15 GND2 9 GND1 4

+V3.3S_CLK

C514 0.01UF/10V C515 0.01UF/10V C385 0.1uF/10V C384 0.1uF/10V C383 0.1uF/10V C381 0.1uF/10V C92 10uF/10V

L20 120Ohm/100MHz +V3.3S

1230

+V3.3S_CLK48 L19 120Ohm/100MHz +V3.3S_CLK

C76 0.1uF/10V C72 1UF/10V

+V3.3S_CLKA L21 120Ohm/100MHz +V3.3S

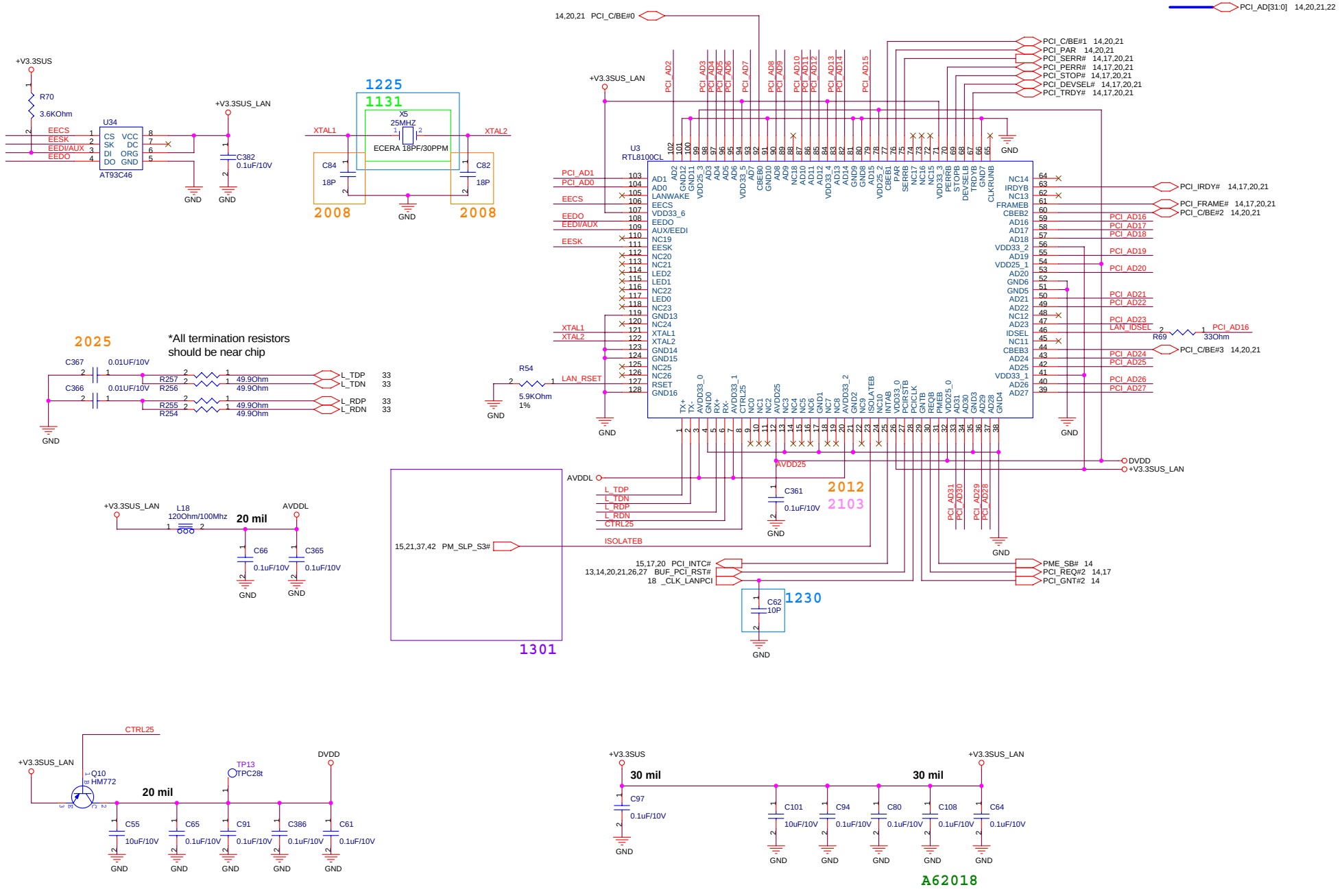
C107 0.1uF/10V C111 1UF/10V

EMI

1142

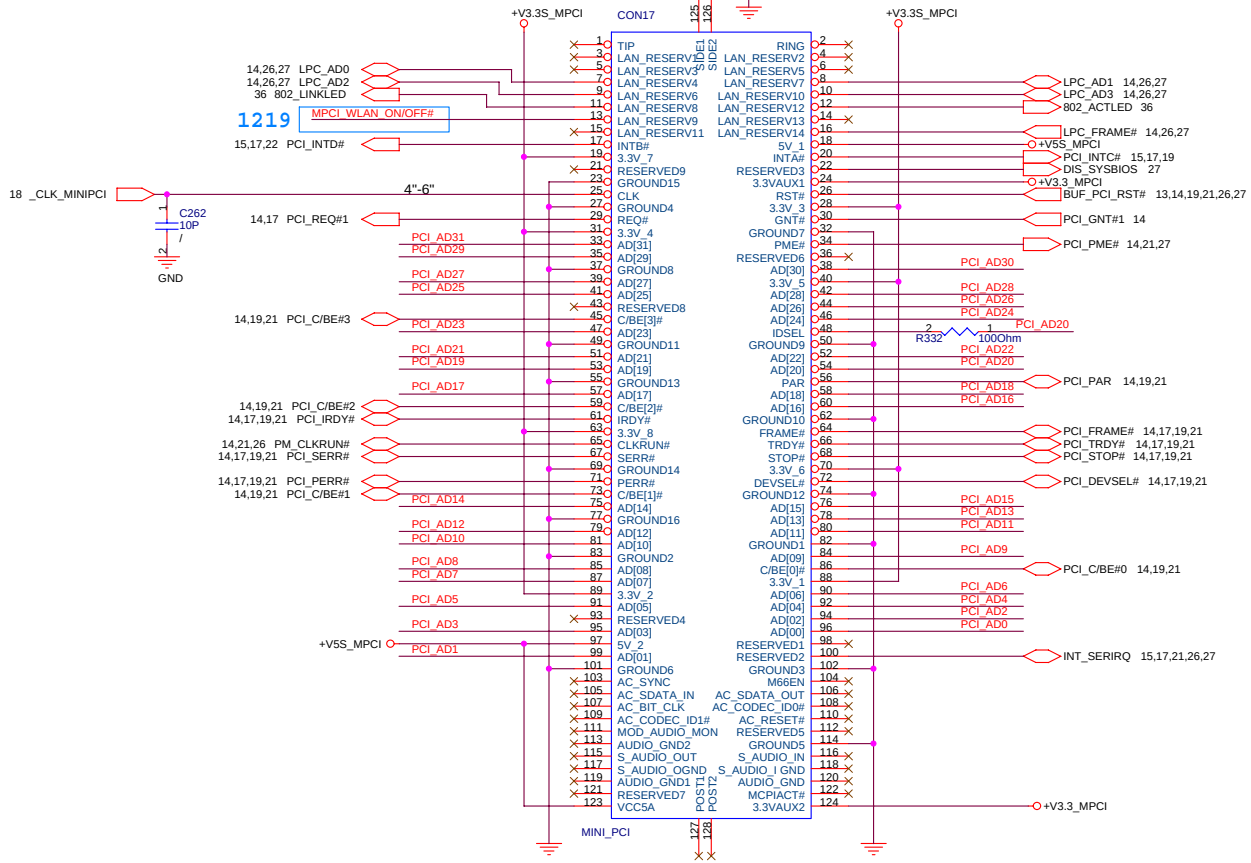
ASUSTek COMPUTER INC. NB1	Engineer: John Hung		
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 18 of 51		

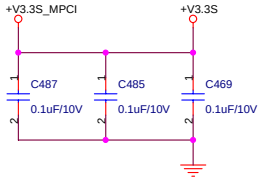
Title : CLOCK-ICS950815

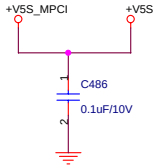

PCI_AD[31:0] 14,20,21,22
+V3.3SUS
R70
3.6KOhm
U34
EECS
EESK
EEDI/AUX
EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46
GND
+V3.3SUS_LAN
C382
0.1uF/10V
1225
1131
X5
25MHZ
XTAL1
XTAL2
ECERA 18PF/30PPM
C84
18P
C82
18P
2008
2008
GND
14,20,21 PCI_C/BE#0
+V3.3SUS_LAN
U3
RTL8100CL
PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2
LAN_RSET
R54
5.9KOhm
1%
PCI_C/BE#1 14,20,21
PCI_PAR 14,20,21
PCI_SERR# 14,17,20,21
PCI_PERR# 14,17,20,21
PCI_STOP# 14,17,20,21
PCI_DEVSEL# 14,17,20,21
PCI_TRDY# 14,17,20,21
PCI_IRDY# 14,17,20,21
PCI_FRAME# 14,17,20,21
PCI_C/BE#2 14,20,21
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
LAN_IDSEL
R69
33Ohm
PCI_AD16
PCI_C/BE#3 14,20,21
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
2025
*All termination resistors
should be near chip
C367
0.01UF/10V
C366
0.01UF/10V
R257
R256
R255
R254
49.9Ohm
L_TDP
L_TDN
L_RDP
L_RDN
33
+V3.3SUS_LAN
L18
120Ohm/100Mhz
20 mil
AVDDL
C66
C365
0.1uF/10V
AVDDL
L_TDP
L_TDN
L_RDP
L_RDN
CTRL25
C361
0.1uF/10V
2012
2103
AVDD25
DVDD
+V3.3SUS_LAN
15,21,37,42 PM_SLP_S3#
ISOLATEB
15,17,20 PCI_INTC#
13,14,20,21,26,27 BUF_PCI_RST#
18 _CLK_LANPCI
PME_SB# 14
PCI_REQ#2 14,17
PCI_GNT#2 14
C62
10P
1230
1301
CTRL25
+V3.3SUS_LAN
Q10
HM772
20 mil
TP13
TPC28t
DVDD
C55
10uF/10V
C65
C91
C386
C61
0.1uF/10V
+V3.3SUS
30 mil
C97
0.1uF/10V
+V3.3SUS_LAN
30 mil
C101
10uF/10V
C94
C80
C108
C64
0.1uF/10V
A62018
Title : LAN-RTL8100CL
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 19 of 51

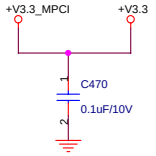
14,19,21,22 PCI_AD[31:0]

2208



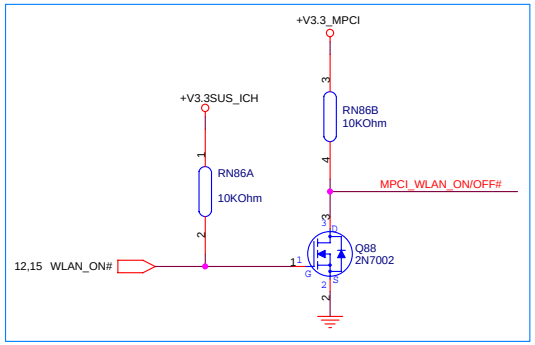






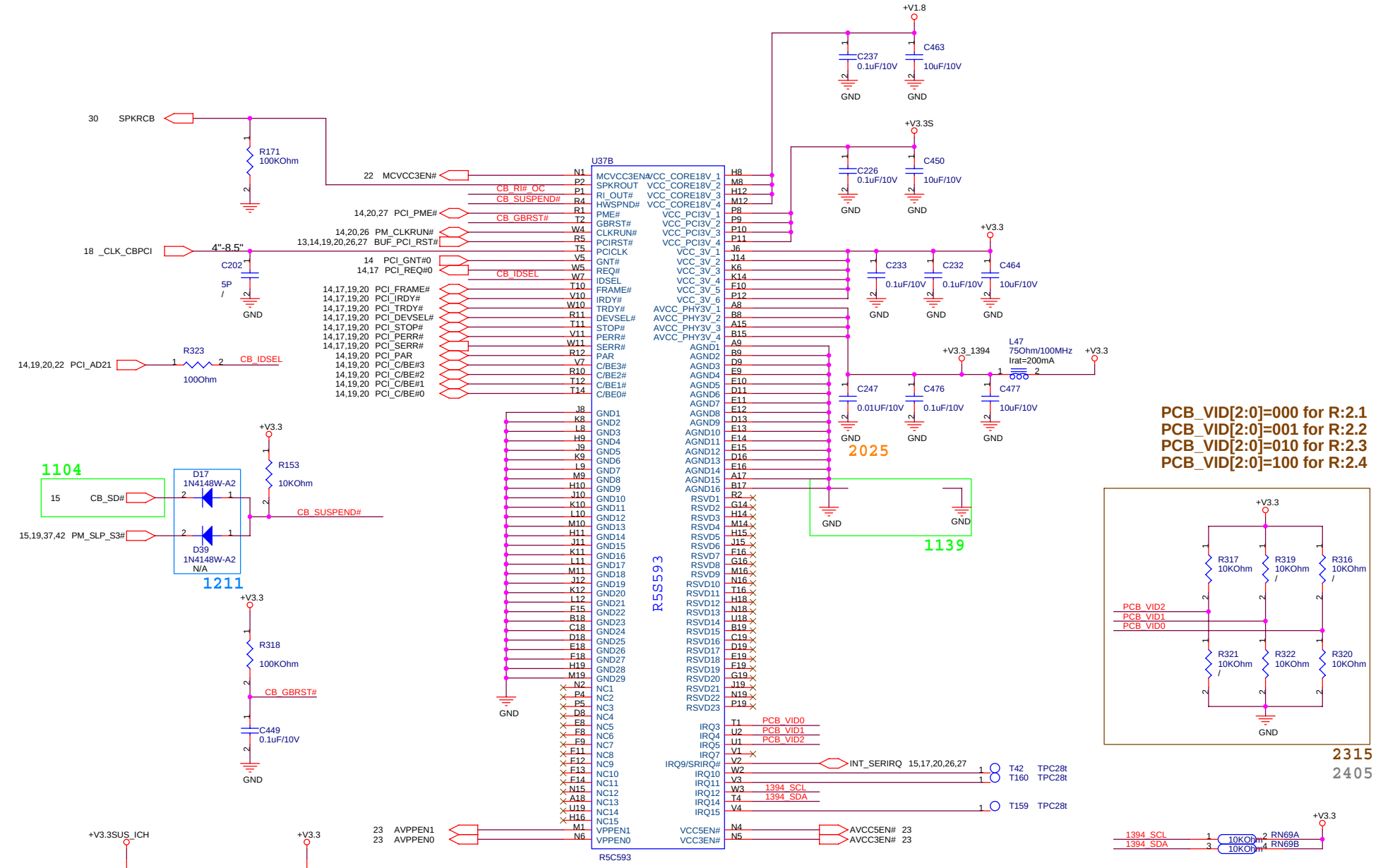
Intel Calexico(802.11a+802.11b)

802.11b	802.11a
Tx: 500-526 mA	Tx: 435-475 mA
Rx: 280-299 mA	Rx:310-327 mA
Sleep: 30 mA	Sleep: 30 mA



1219

ASUSTek COMPUTER INC. NB1	Title : MINIPCI	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 20 of 51	



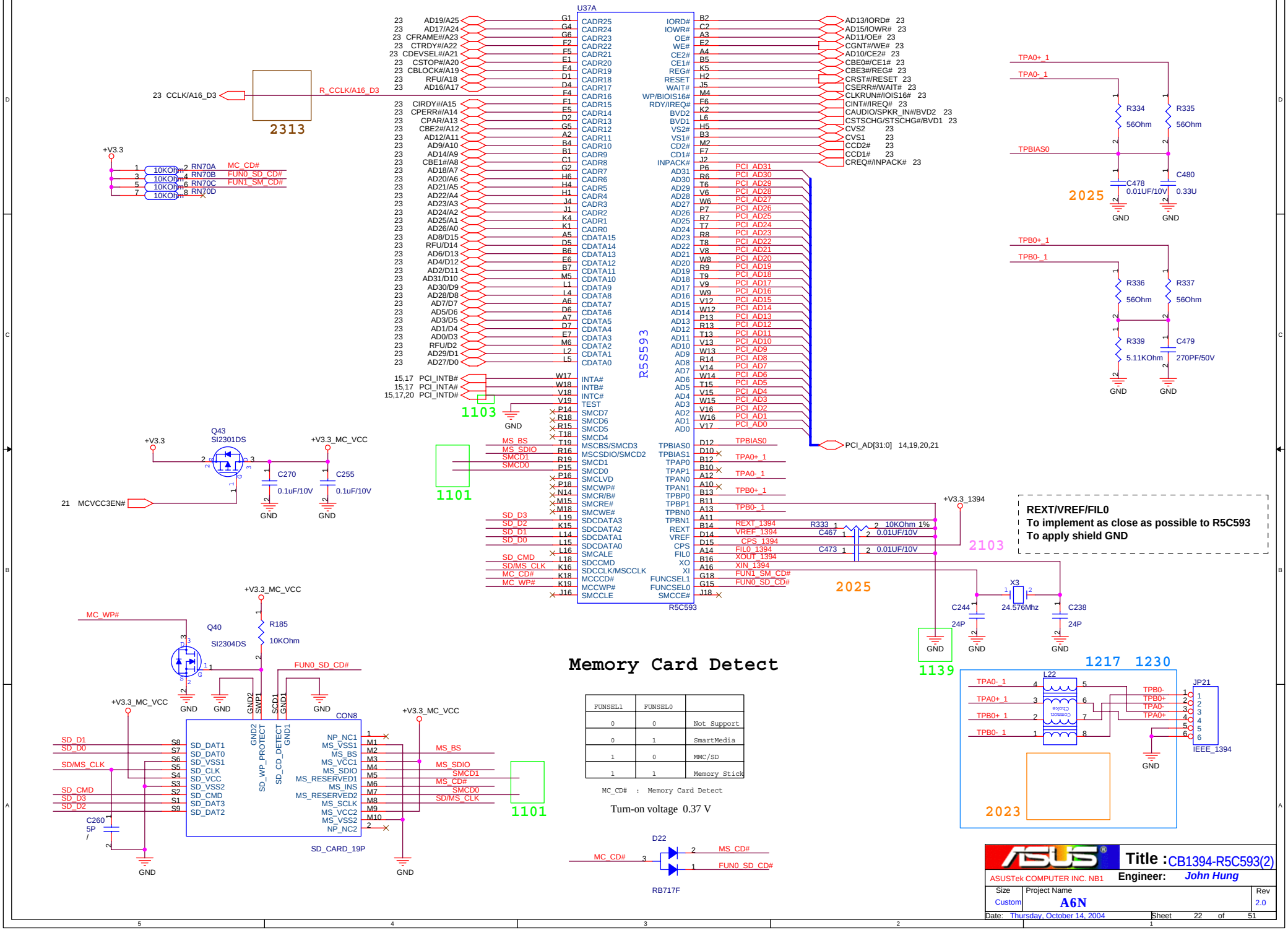
<Variant Name>

Title : CB1394-R5C593(1)

ASUSTek COMPUTER INC. NB1 **Engineer:** *John Hung*

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 21 of 51


U37A
R5C593
23 CCLK/A16_D3
R_CCLK/A16_D3
2313
+V3.3
10KOhm RN70A MC_CD#
10KOhm RN70B FUN0_SD_CD#
10KOhm RN70C FUN1_SM_CD#
10KOhm RN70D
15,17 PCI_INTB#
15,17 PCI_INTA#
15,17,20 PCI_INTD#
1103
GND
PCI_AD[31:0] 14,19,20,21
TPA0+_1
TPA0-_1
TPBIAS0
R334 56Ohm
R335 56Ohm
C478 0.01UF/10V
C480 0.33U
2025
TPB0+_1
TPB0-_1
R336 56Ohm
R337 56Ohm
R339 5.11KOhm
C479 270PF/50V
Q43 SI2301DS
+V3.3_MC_VCC
21 MCVCC3EN#
C270 0.1uF/10V
C255 0.1uF/10V
1101
MS_BS
MS_SDIO
SMCD1
SMCD0
SD_D3
SD_D2
SD_D1
SD_D0
SD_CMD
SD/MS_CLK
MC_CD#
MC_WP#
+V3.3_1394
REXT_1394
VREF_1394
CPS_1394
FIL0_1394
XOUT_1394
XIN_1394
FUN1_SM_CD#
FUN0_SD_CD#
R333_1 10KOhm 1%
C467_1 0.01UF/10V
C473_1 0.01UF/10V
2103
2025
X3 24.576Mhz
C244 24P
C238 24P
1139
1217 1230
L22
JP21
IEEE_1394
2023
REXT/VREF/FIL0
To implement as close as possible to R5C593
To apply shield GND
Q40 SI2304DS
R185 10KOhm
FUN0_SD_CD#
CON8
SD_CARD_19P
C260 5P
Memory Card Detect
FUNSEL1 FUNSEL0
0 0 Not Support
0 1 SmartMedia
1 0 MMC/SD
1 1 Memory Stick
MC_CD# : Memory Card Detect
Turn-on voltage 0.37 V
D22
RB717F
Title : CB1394-R5C593(2)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 22 of 51

CB POWER SWITCH

1105
Use PCMCIA debug card :
change R347 to 10K,
delete R

21 AVCC5EN#

21 AVCC3EN#

U49
G571

2014
AVPPEN1 21
AVPPEN0 21

2220

S0-S3: (Max. 1.25 A)
S0-S3: (Max. 1 A)
S0-S3: (Max. 1 A)
S0-S3: (Max. 0.25 A)

+V3.3 C505 10uF/10V C504 0.1uF/10V GND
+V5 C507 10uF/10V C508 0.1uF/10V GND
+V12 C509 0.1UF/25V C510 0.01uF/25V GND
+AVCC C499 0.1uF/10V C503 0.1uF/10V GND
+AVPP C511 0.1UF/25V GND

CB SOCKET

+AVCC C245 10uF/10V C248 0.1UF/25V GND
+AVPP C240 10uF/10V C243 0.1UF/25V GND

1127
CON16
PCMCIA_CON_84P

22 CCLK/A16_D3
C466 5P

+AVCC R178 47KOhm
22 CRST#/RESET
C236 0.01UF/10V
2025

22 AD19/A25
22 AD17/A24
22 CFRAME#/A23
22 CTRDY#/A22
22 CDEVSEL#/A21
22 CSTOP#/A20
22 CBLOCK#/A19
22 RFU/A18
22 AD16/A17
22 CIRDY#/A15
22 CPERR#/A14
22 CPAR/A13
22 CBE2#/A12
22 AD12/A11
22 AD9/A10
22 AD14/A9
22 CBE1#/A8
22 AD18/A7
22 AD20/A6
22 AD21/A5
22 AD22/A4
22 AD23/A3
22 AD24/A2
22 AD25/A1
22 AD26/A0
22 AD8/D15
22 RFU/D14
22 AD6/D13
22 AD4/D12
22 AD2/D11
22 AD31/D10
22 AD30/D9
22 AD28/D8
22 AD7/D7
22 AD5/D6
22 AD3/D5
22 AD1/D4
22 AD0/D3
22 RFU/D2
22 AD29/D1
22 AD27/D0
22 AD13/IORD#
22 AD15/IOWR#
22 AD11/OE#
22 CGNT#/WE#
22 AD10/CE2#
22 CBE0#/CE1#
22 CBE3#/REG#
22 CSERR#/WAIT#
22 CLKRUN#/IOIS16#
22 CINT#/IREQ#
22 CAUDIO/SPKR_IN#/BVD2
22 CSTSCHG/STSCHG#/BVD1
22 CVS2
22 CVS1
22 CCD2#
22 CCD1#
22 CREQ#/INPACK#

CB DE-BOUNCE

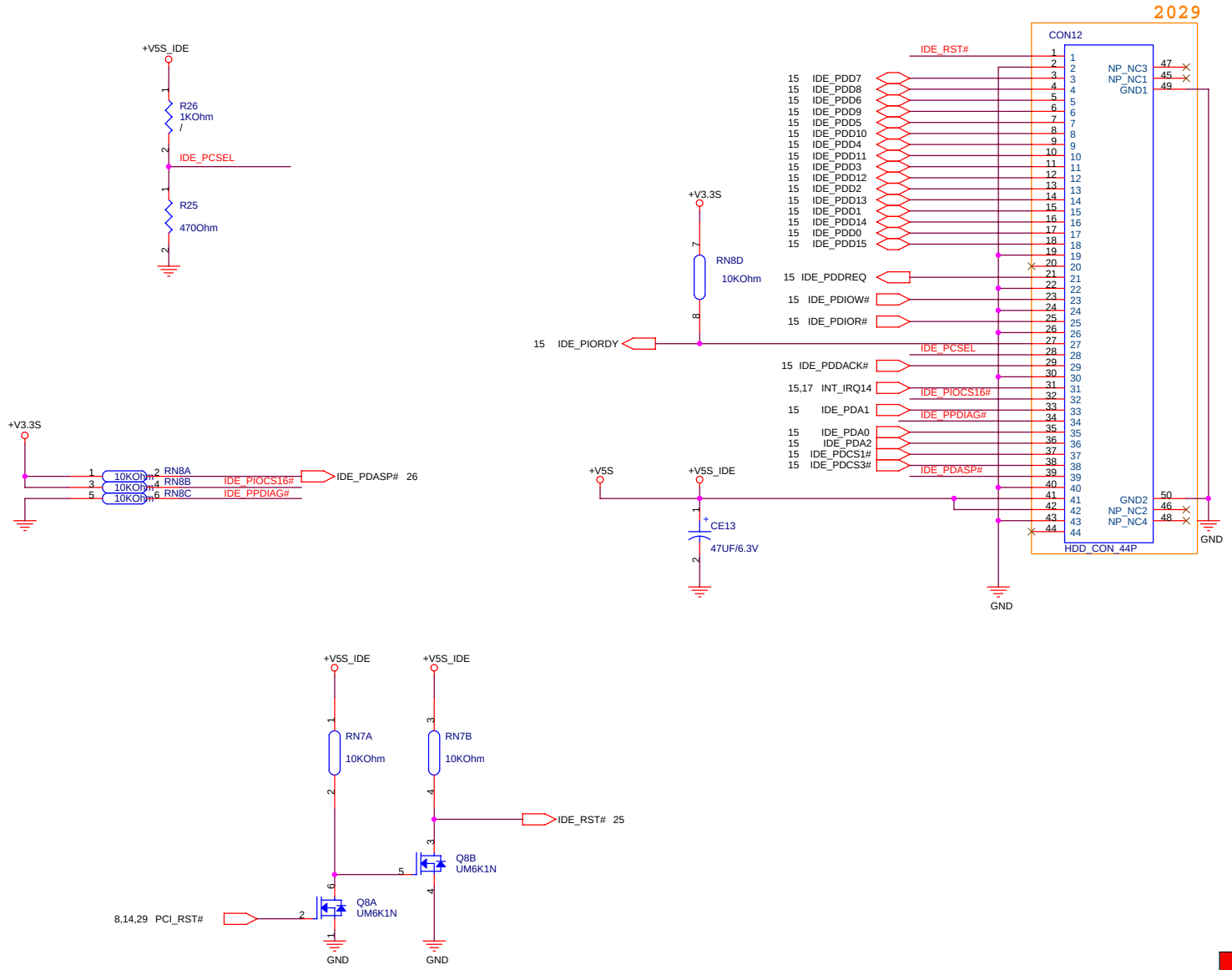
22 CCD1# C490 270PF/50V
22 CCD2# C448 270PF/50V

<Variant Name>

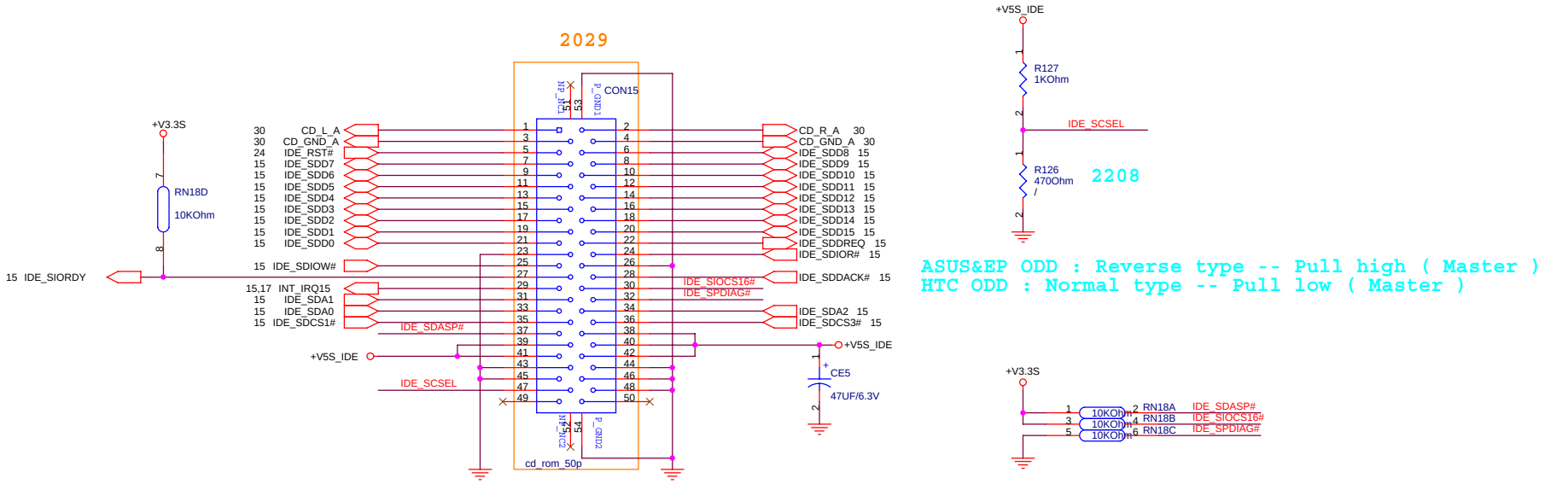
Title : PCMCIA SOCKET
ASUSTek COMPUTER INC. NB1
Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 23 of 51

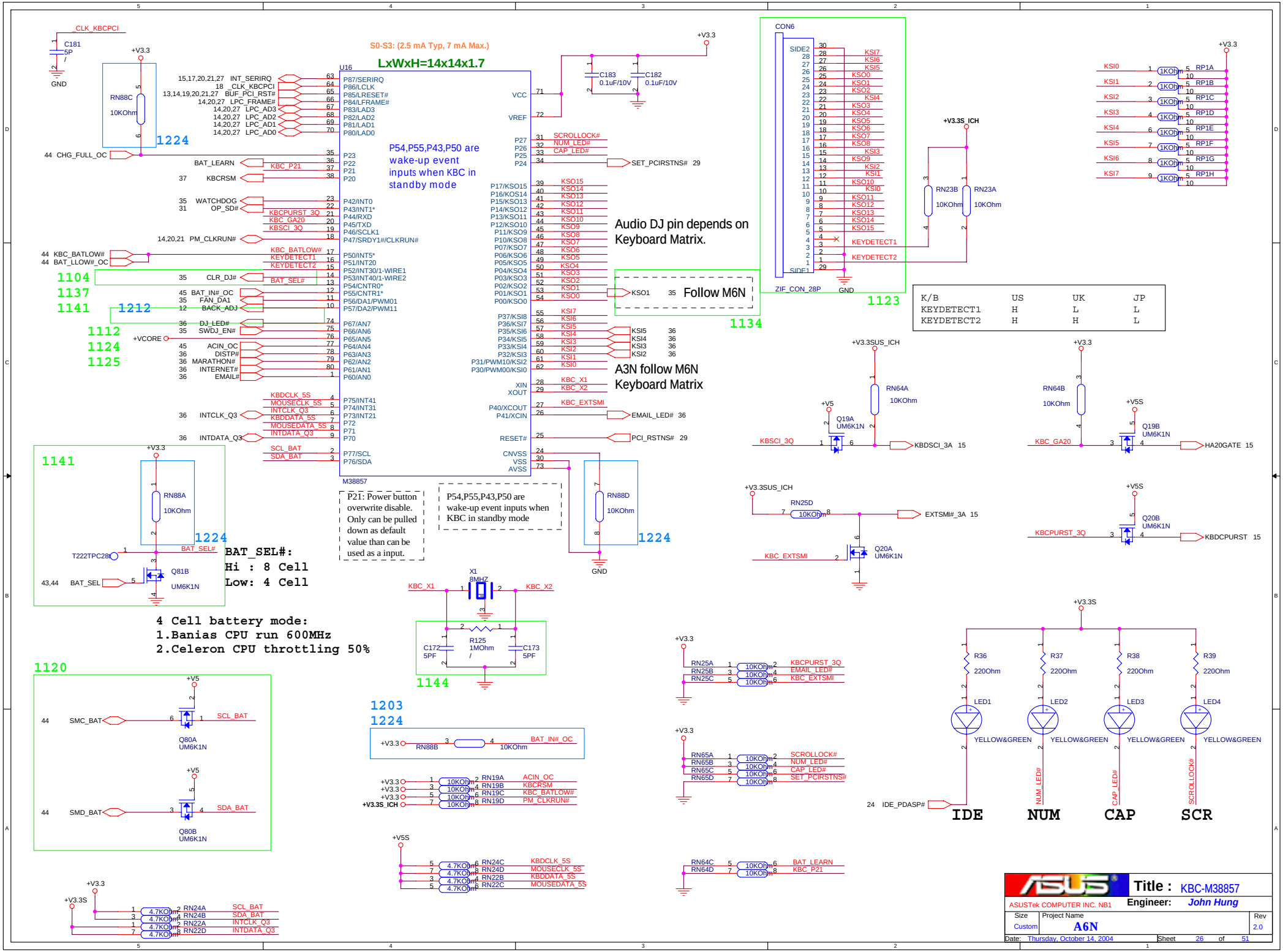


ASUSTek COMPUTER INC. NB1	Title : HDD Connector	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 24 of 51	



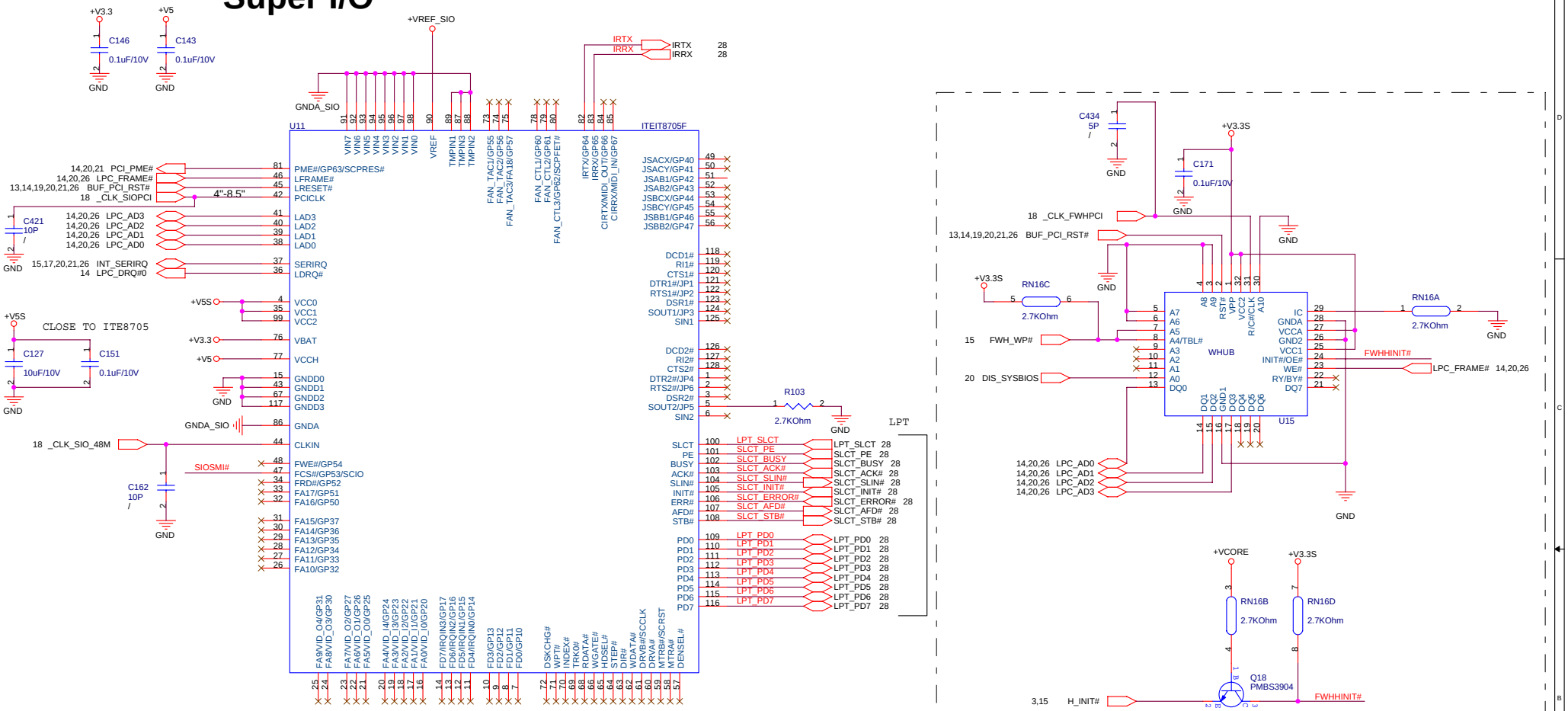
ASUS&EP ODD : Reverse type -- Pull high (Master)
HTC ODD : Normal type -- Pull low (Master)

ASUSTek COMPUTER INC. NB1	Title : ODD Connector	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 25 of 51	

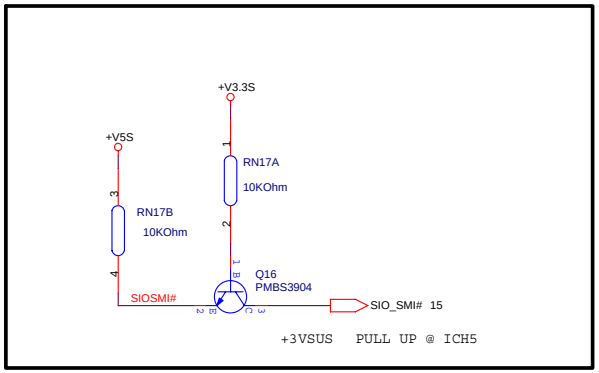

S0-S3: (2.5 mA Typ, 7 mA Max.)
LxWxH=14x14x1.7
U16
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Audio DJ pin depends on Keyboard Matrix.
Follow M6N
A3N follow M6N Keyboard Matrix
P21: Power button overwrite disable. Only can be pulled down as default value than can be used as a input.
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
CON6
ZIF_CON_28P
K/B US UK JP
KEYDETECT1 H L L
KEYDETECT2 H H L
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU throttling 50%
IDE
NUM
CAP
SCR
Title : KBC-M38857
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Project Name A6N
Date: Thursday, October 14, 2004
Sheet 26 of 51

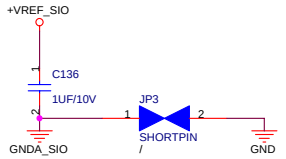
Super I/O

2208



P24: Add FHW ROM P/N: 05-001017122

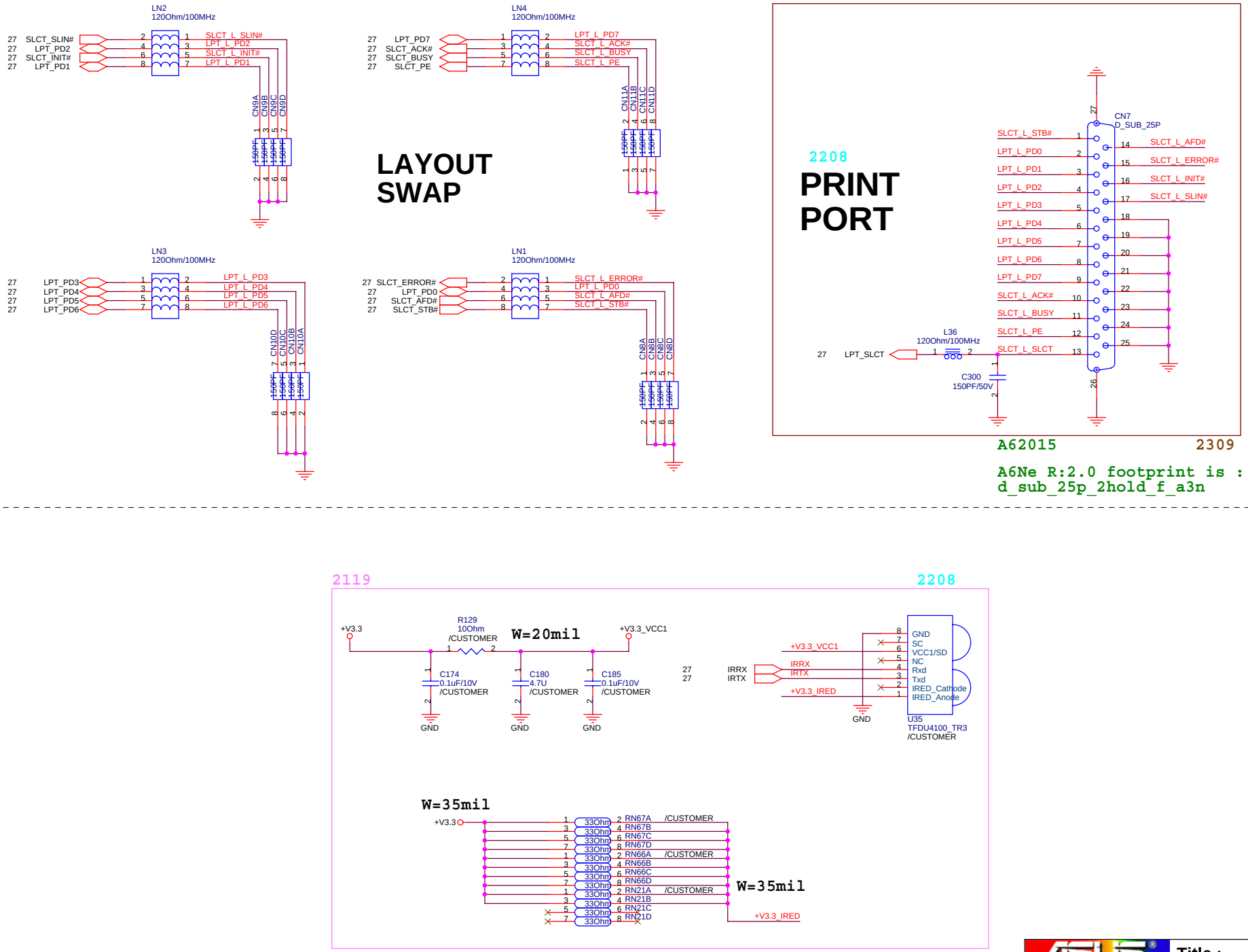




CLOSE TO ITE8705

<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : SIO-ITE8705	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 27 of 51	



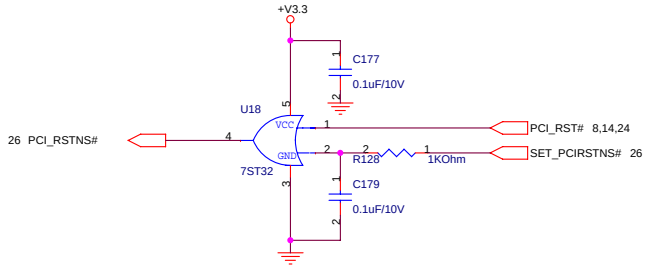
ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 28 of 51	

Title :

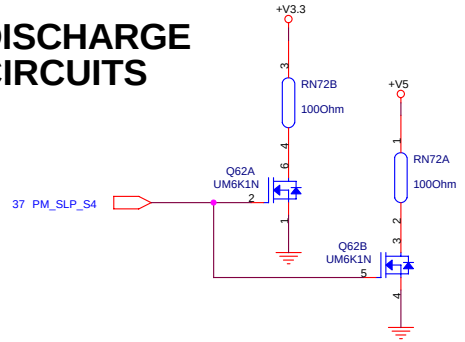
PCMCIA DEBUG Card

1105

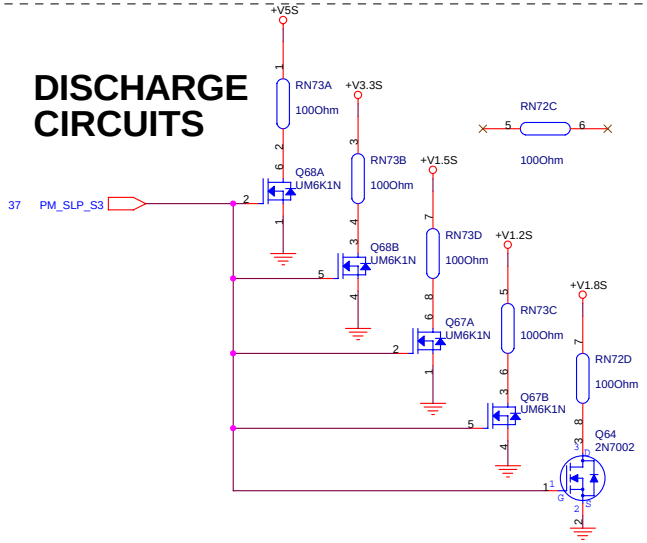
PCI_RSTNS# Gen Circuit



DISCHARGE CIRCUITS



DISCHARGE CIRCUITS



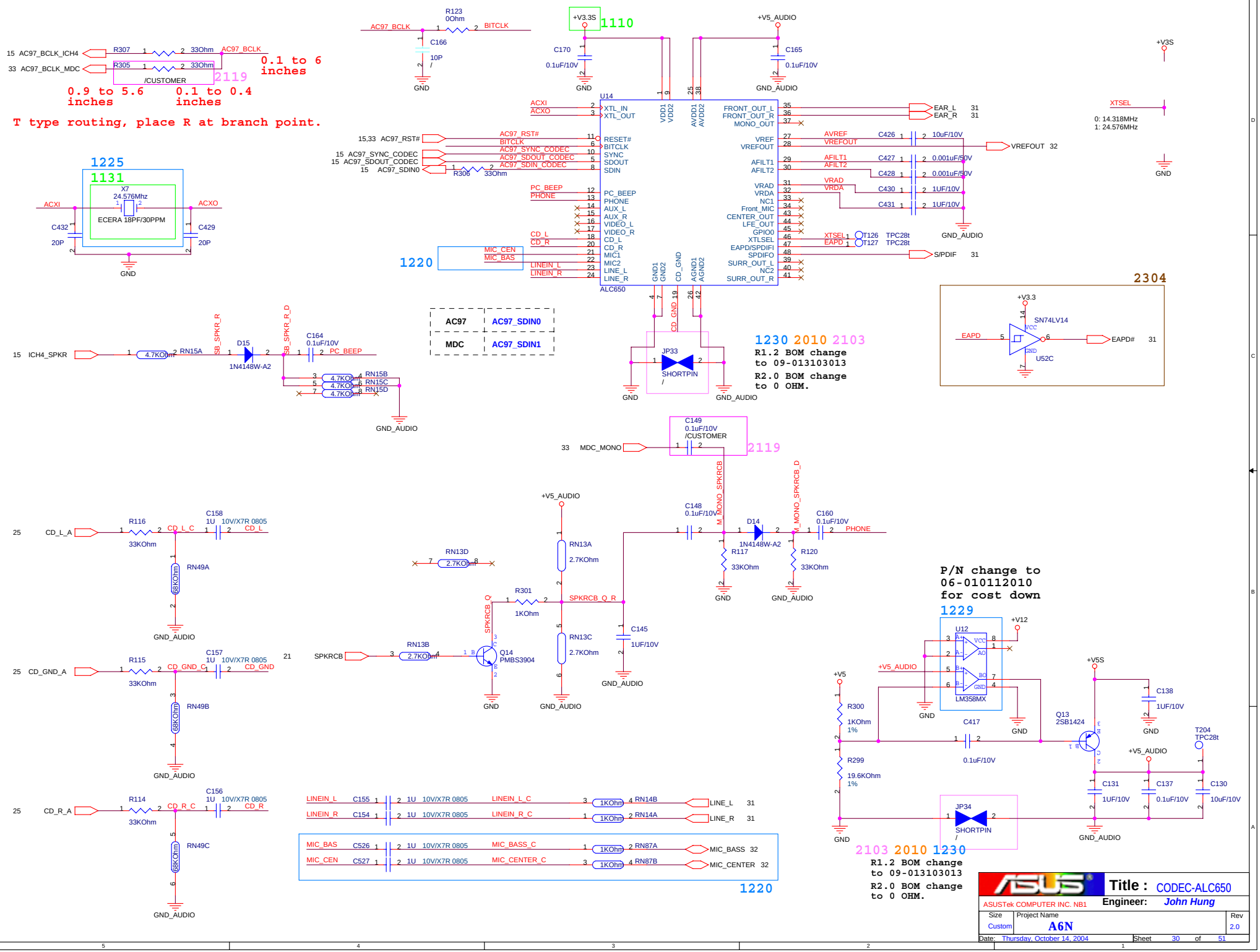
ASUSTek COMPUTER INC. NB1

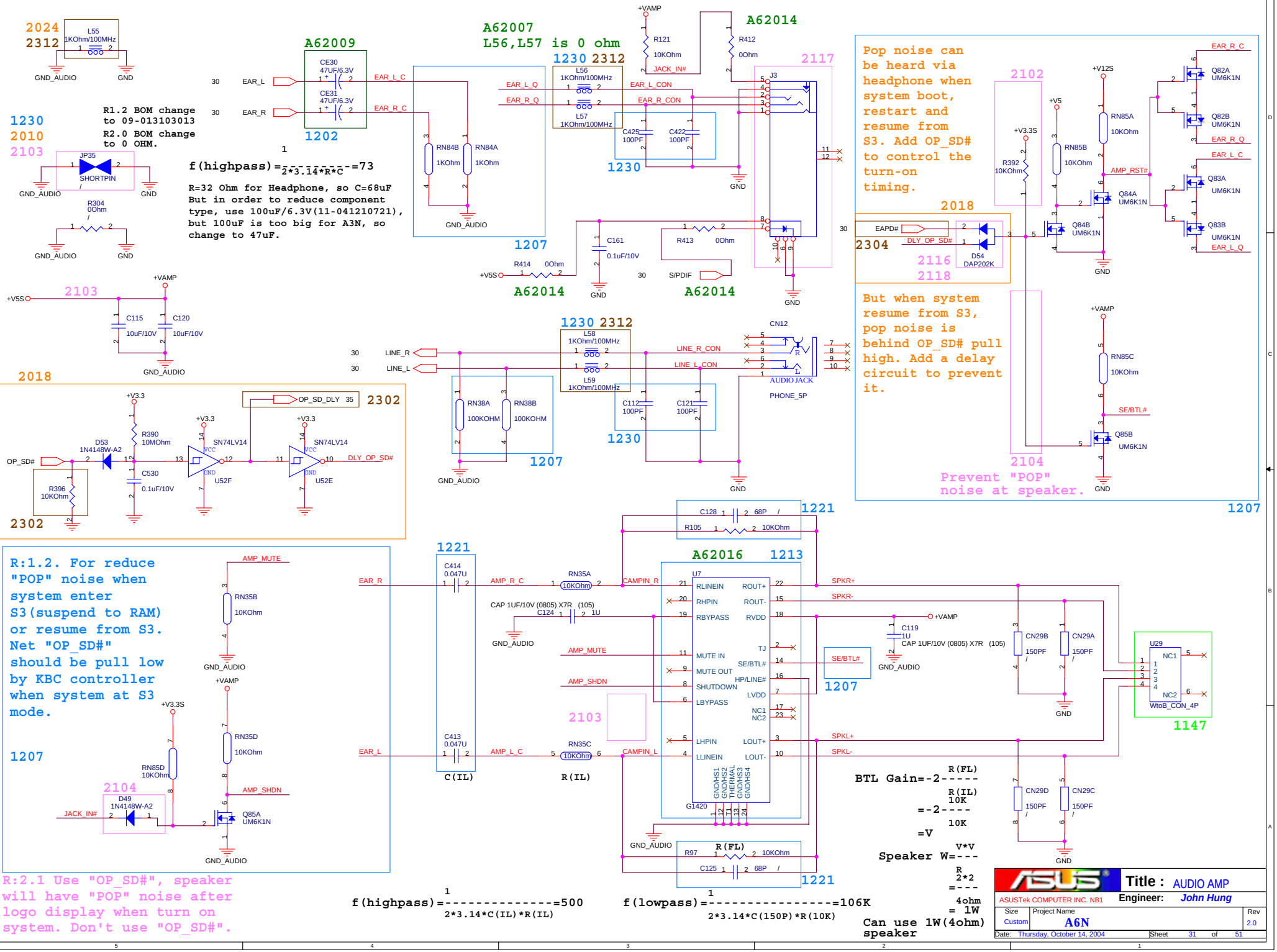
Title : Discharge circuit

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 29 of 51

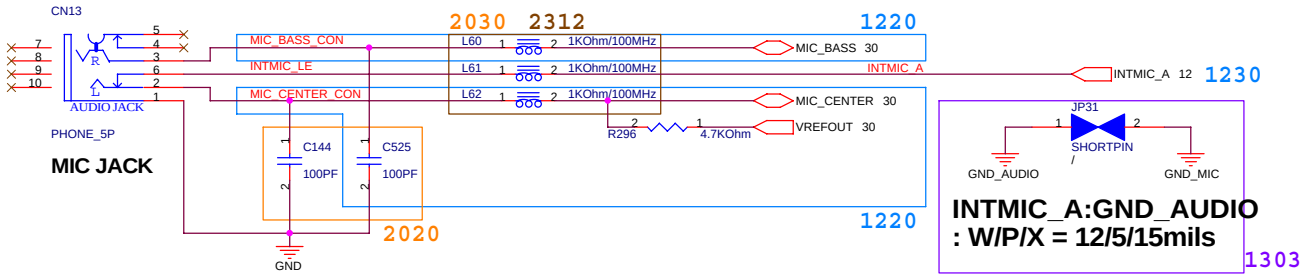

15 AC97_BCLK_ICH4
33 AC97_BCLK_MDC
R307 33Ohm
R305 33Ohm
/CUSTOMER
AC97_BCLK
2119
0.1 to 6 inches
0.9 to 5.6 inches
0.1 to 0.4 inches
T type routing, place R at branch point.
R123 0Ohm
AC97_BCLK
BITCLK
C166 10P /
GND
+V3.3S
1110
C170 0.1uF/10V
+V5_AUDIO
C165 0.1uF/10V
GND_AUDIO
U14
ACXI
ACXO
XTL_IN
XTL_OUT
VDD1
VDD2
AVDD1
AVDD2
FRONT_OUT_L
FRONT_OUT_R
MONO_OUT
EAR_L 31
EAR_R 31
15,33 AC97_RST#
15 AC97_SYNC_CODEC
15 AC97_SDOUT_CODEC
15 AC97_SDIN0
AC97_RST#
BITCLK
AC97_SYNC_CODEC
AC97_SDOUT_CODEC
AC97_SDIN_CODEC
R306 33Ohm
RESET#
SYNC
SDOUT
SDIN
VREF
VREFOUT
AVREF
AFILT1
AFILT2
VRAD
VRDA
NC1
Front_MIC
CENTER_OUT
LFE_OUT
GPIO0
XTLSEL
EAPD/SPDIFI
SPDIFO
SURR_OUT_L
NC2
SURR_OUT_R
C426 10uF/10V
C427 0.001uF/50V
C428 0.001uF/50V
C430 1UF/10V
C431 1UF/10V
VREFOUT 32
XTSEL
T126 TPC28t
T127 TPC28t
EAPD
S/PDIF 31
GND_AUDIO
+V3S
XTSEL
0: 14.318MHz
1: 24.576MHz
GND
1225
1131
X7
24.576Mhz
ECERA 18PF/30PPM
C432 20P
C429 20P
PC_BEEP
PHONE
CD_L
CD_R
MIC1
MIC2
LINE_L
LINE_R
MIC_CEN
MIC_BAS
LINEIN_L
LINEIN_R
1220
GND1
GND2
CD_GND
AGND1
AGND2
ALC650
AC97
AC97_SDIN0
MDC
AC97_SDIN1
JP33
SHORTPIN
1230 2010 2103
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.
2304
+V3.3
SN74LV14
VCC
GND
U52C
EAPD
EAPD# 31
15 ICH4_SPKR
4.7KOhm RN15A
SB_SPKR_R
D15
1N4148W-A2
SB_SPKR_R_D
C164 0.1uF/10V
PC_BEEP
RN15B 4.7KOhm
RN15C 4.7KOhm
RN15D 4.7KOhm
GND_AUDIO
33 MDC_MONO
C149 0.1uF/10V /CUSTOMER
2119
M_MONO_SPKRCB
M_MONO_SPKRCB_D
C148 0.1uF/10V
D14
1N4148W-A2
C160 0.1uF/10V
PHONE
R117 33KOhm
R120 33KOhm
+V5_AUDIO
RN13D 2.7KOhm
RN13A 2.7KOhm
R301 1KOhm
SPKRCB_Q_R
SPKRCB_Q
RN13C 2.7KOhm
C145 1UF/10V
21 SPKRCB
RN13B 2.7KOhm
Q14 PMBS3904
25 CD_L_A
R116 33KOhm
C158 1U 10V/X7R 0805
CD_L_C
CD_L
RN49A 68KOhm
25 CD_GND_A
R115 33KOhm
C157 1U 10V/X7R 0805
CD_GND_C
CD_GND
RN49B 68KOhm
25 CD_R_A
R114 33KOhm
C156 1U 10V/X7R 0805
CD_R_C
CD_R
RN49C 68KOhm
LINEIN_L
LINEIN_R
C155 1U 10V/X7R 0805
C154 1U 10V/X7R 0805
LINEIN_L_C
LINEIN_R_C
RN14B 1KOhm
RN14A 1KOhm
LINE_L 31
LINE_R 31
MIC_BAS
MIC_CEN
C526 1U 10V/X7R 0805
C527 1U 10V/X7R 0805
MIC_BASS_C
MIC_CENTER_C
RN87A 1KOhm
RN87B 1KOhm
MIC_BASS 32
MIC_CENTER 32
1220
P/N change to 06-010112010 for cost down
1229
U12
LM358MX
+V12
+V5
+V5S
R300 1KOhm 1%
R299 19.6KOhm 1%
C417 0.1uF/10V
Q13 2SB1424
C138 1UF/10V
C131 1UF/10V
C137 0.1uF/10V
C130 10uF/10V
T204 TPC28t
JP34
SHORTPIN
2103 2010 1230
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.
Title : CODEC-ALC650
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 30 of 51


A62007
L56,L57 is 0 ohm
A62009
A62014
2024
2312
L55
1KOhm/100MHz
GND_AUDIO
GND
EAR_L
EAR_R
CE30
47UF/6.3V
CE31
47UF/6.3V
EAR_L_C
EAR_R_C
1202
R1.2 BOM change
to 09-013103013
R2.0 BOM change
to 0 OHM.
1230
2010
2103
JP35
SHORTPIN
R304
0Ohm
f(highpass)=1/(2*3.14*R*C)=73
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component
type, use 100uF/6.3V(11-041210721),
but 100uF is too big for A3N, so
change to 47uF.
RN84B
1KOhm
RN84A
1KOhm
1207
+VAMP
R121
10KOhm
R412
0Ohm
JACK_IN#
L56
1KOhm/100MHz
L57
1KOhm/100MHz
EAR_L_Q
EAR_R_Q
EAR_L_CON
EAR_R_CON
C425
100PF
C422
100PF
1230
2117
J3
R414
0Ohm
+V5S
C161
0.1uF/10V
R413
0Ohm
S/PDIF
2103
+V5S
+VAMP
C115
10uF/10V
C120
10uF/10V
GND_AUDIO
2018
OP_SD_DLY
35
2302
+V3.3
R390
10MOhm
D53
1N4148W-A2
OP_SD#
C530
0.1uF/10V
SN74LV14
U52F
U52E
DLY_OP_SD#
R396
10KOhm
LINE_R
LINE_L
L58
1KOhm/100MHz
L59
1KOhm/100MHz
LINE_R_CON
LINE_L_CON
CN12
AUDIO JACK
PHONE_5P
RN38A
100KOHM
RN38B
100KOHM
C112
100PF
C121
100PF
Pop noise can
be heard via
headphone when
system boot,
restart and
resume from
S3. Add OP_SD#
to control the
turn-on
timing.
2102
+V3.3S
R392
10KOhm
+V12S
+V5
RN85A
10KOhm
RN85B
10KOhm
AMP_RST#
Q84A
UM6K1N
Q84B
UM6K1N
EAR_R_C
Q82A
UM6K1N
Q82B
UM6K1N
EAR_R_Q
EAR_L_C
Q83A
UM6K1N
Q83B
UM6K1N
EAR_L_Q
EAPD#
DLY_OP_SD#
2304
2116
2118
D54
DAP202K
But when system
resume from S3,
pop noise is
behind OP_SD# pull
high. Add a delay
circuit to prevent
it.
RN85C
10KOhm
SE/BTL#
Q85B
UM6K1N
2104
Prevent "POP"
noise at speaker.
R:1.2. For reduce
"POP" noise when
system enter
S3(suspend to RAM)
or resume from S3.
Net "OP_SD#"
should be pull low
by KBC controller
when system at S3
mode.
AMP_MUTE
RN35B
10KOhm
+VAMP
+V3.3S
RN85D
10KOhm
RN35D
10KOhm
AMP_SHDN
D49
1N4148W-A2
JACK_IN#
Q85A
UM6K1N
R:2.1 Use "OP_SD#", speaker
will have "POP" noise after
logo display when turn on
system. Don't use "OP_SD#".
1221
C414
0.047U
C413
0.047U
C(IL)
EAR_R
EAR_L
AMP_R_C
AMP_L_C
RN35A
10KOhm
RN35C
10KOhm
R(IL)
CAP 1UF/10V (0805) X7R (105)
C124
1U
C128
68P
R105
10KOhm
A62016
1213
U7
CAMPIN_R
CAMPIN_L
RLINEIN
RHPIN
RBYPASS
MUTE IN
MUTE OUT
SHUTDOWN
LBYPASS
LHPIN
LLINEIN
ROUT+
ROUT-
RVDD
TJ
SE/BTL#
HP/LINE#
LVDD
NC1
NC2
LOUT+
LOUT-
GNDHS1
GNDHS2
THERMAL
GNDHS3
GNDHS4
G1420
SPKR+
SPKR-
SPKL+
SPKL-
C119
1U
CAP 1UF/10V (0805) X7R (105)
CN29B
150PF
CN29A
150PF
CN29D
150PF
CN29C
150PF
U29
NC1
NC2
WtoB_CON_4P
1147
R97
R(FL)
10KOhm
C125
68P
f(highpass)=1/(2*3.14*C(IL)*R(IL))=500
f(lowpass)=1/(2*3.14*C(150P)*R(10K))=106K
BTL Gain=-2*R(FL)/R(IL)=-2*10K/10K=V
Speaker W=V*V/R=2*2/4ohm=1W
Can use 1W(4ohm)
speaker
ASUS
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size: Custom
Project Name: A6N
Rev: 2.0
Date: Thursday, October 14, 2004
Sheet 31 of 51

1220

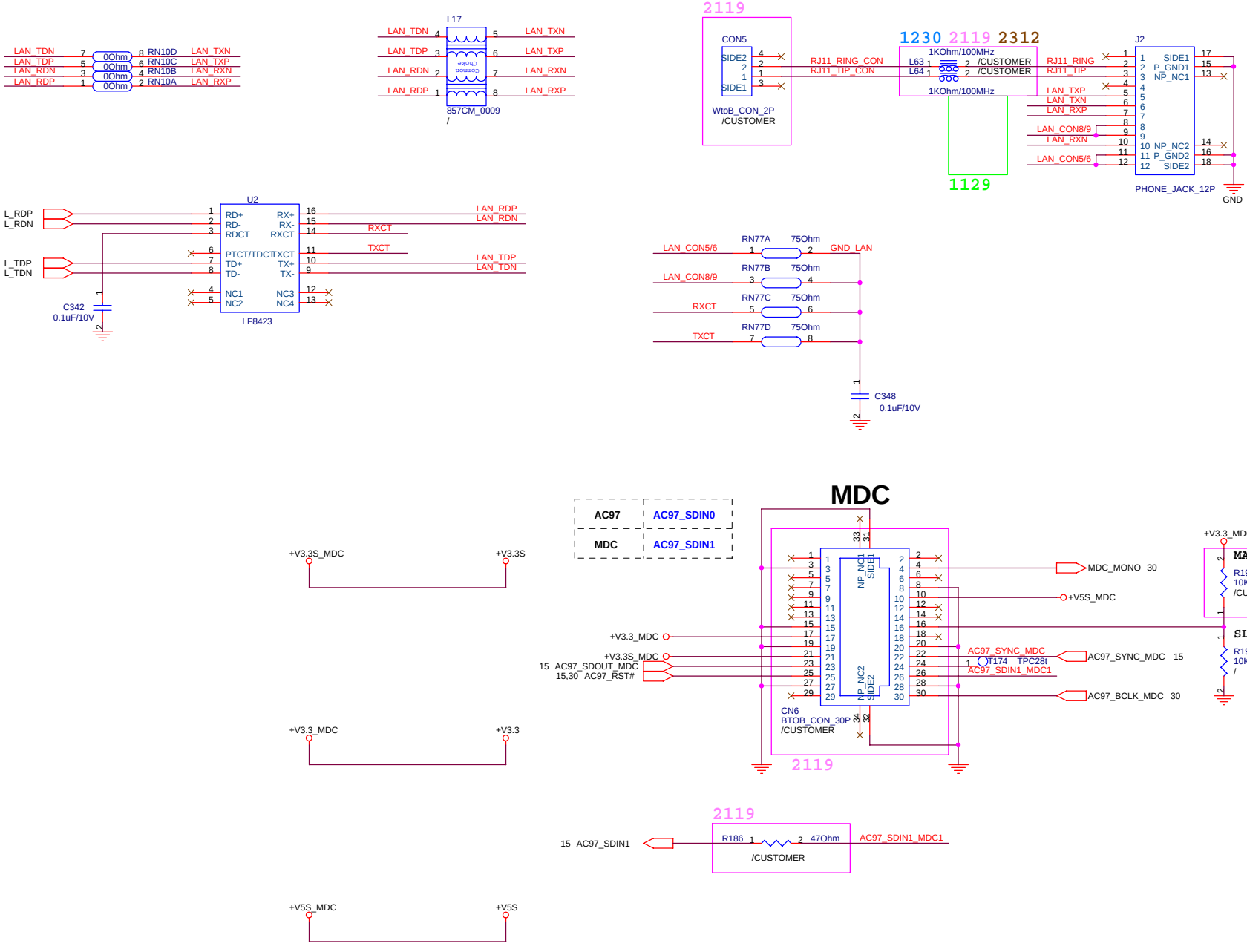
MIC OP CIRCUIT

MIC JACK



ASUSTek COMPUTER INC. NB1	Title :	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 32 of 51	

OP: FOR EMI

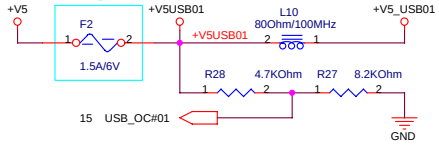


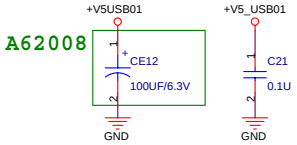
MDC

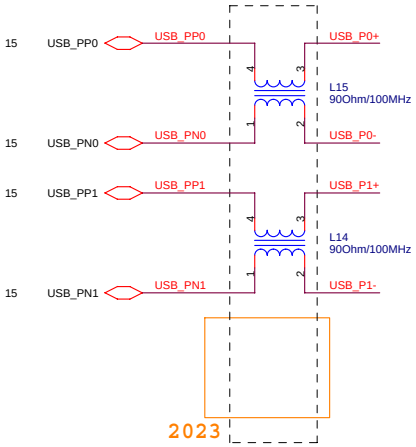
ASUSTek COMPUTER INC. NB1	Title :	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 33 of 51	

VPLP R:2.2 use 07-014110900 (
2nd source is 07-014110201)

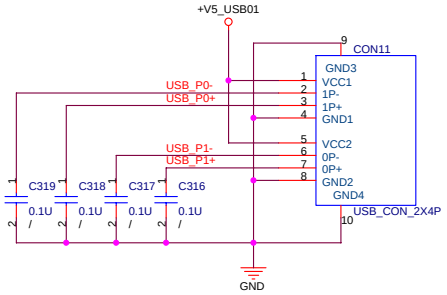
2219







R & L Co-Lay



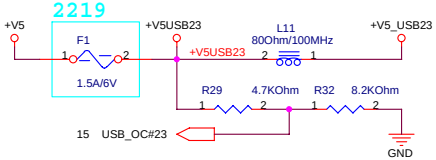
USB PORT 0 & PORT 1

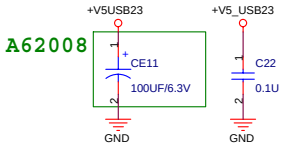
1128

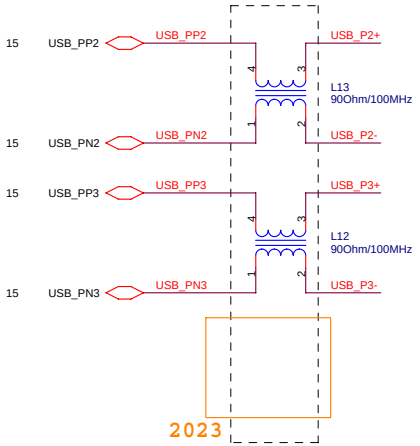
USB PORT 3 for CAMERA
Change to page 12

VPLP R:2.2 use 07-014110900 (
2nd source is 07-014110201)

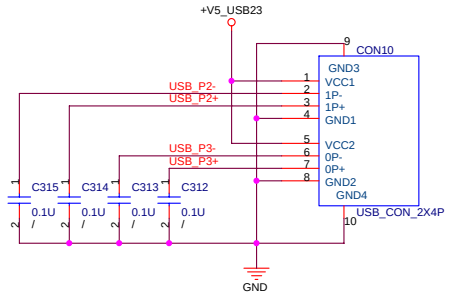
2219







R & L Co-Lay



A6N1002

USB PORT 2 & PORT 3

1128

USB PORT 4

A6N1002

ASUSTek COMPUTER INC. NB1

Title : USB

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

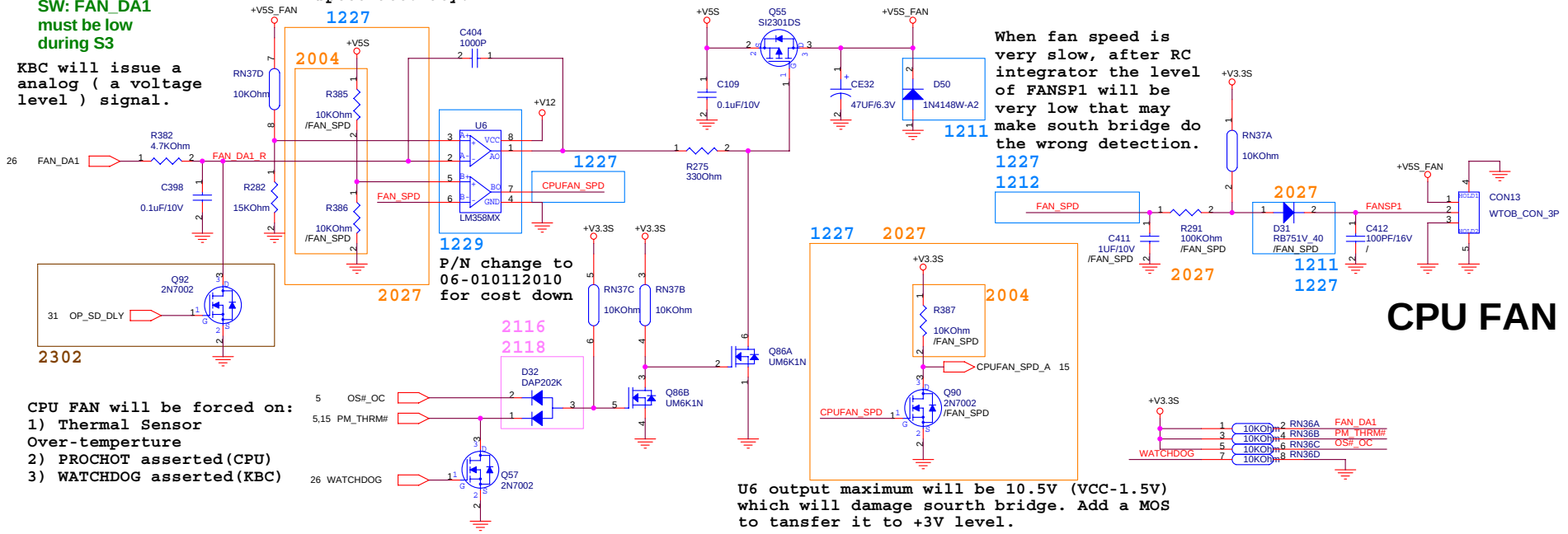
Date: Thursday, October 14, 2004 Sheet 34 of 51

Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.



When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

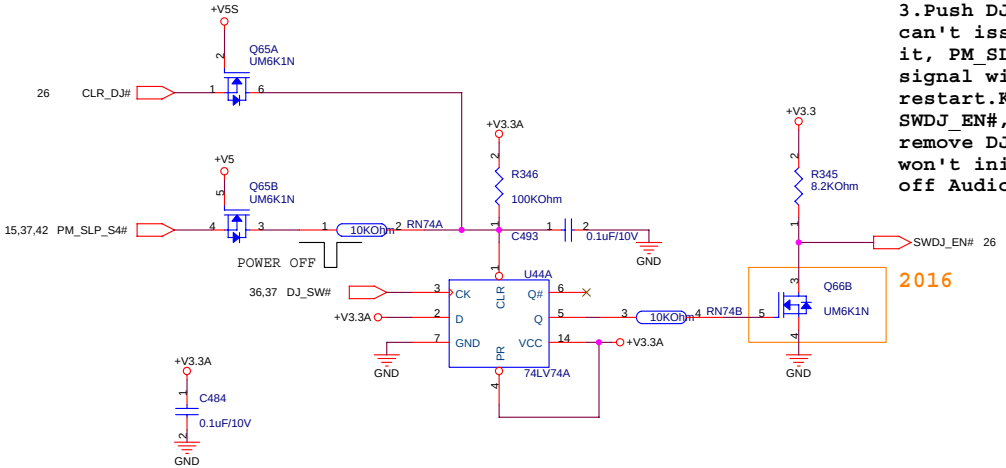
CPU FAN

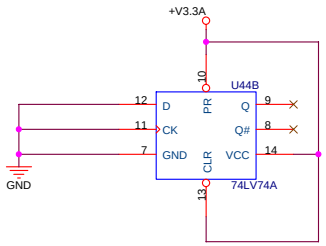
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

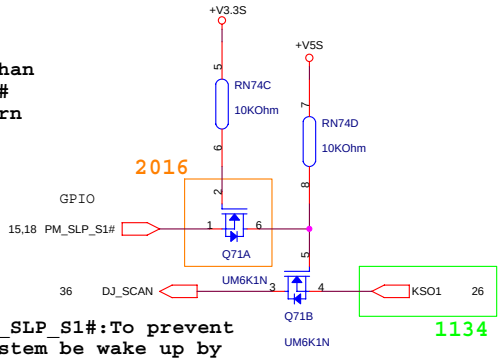
U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

Audio DJ

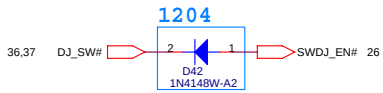
SWDJ_EN# function :
1.Push DJ_SW#, turn on Audio DJ.
2.PM_SLP_S4# will keep high.
3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.







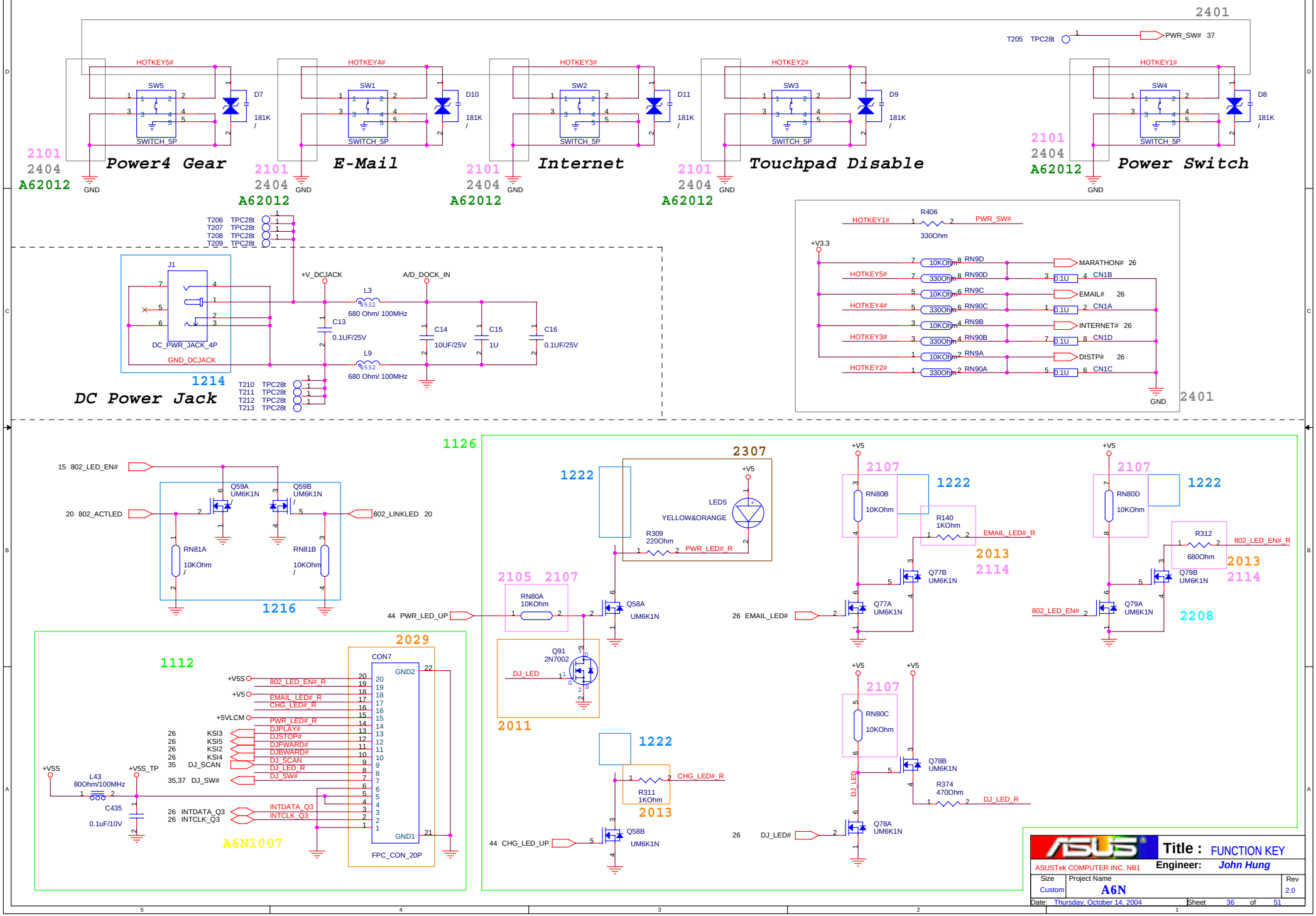
PM_SLP_S1#:To prevent system be wake up by Audio DJ Key when system enter S1 or S3.

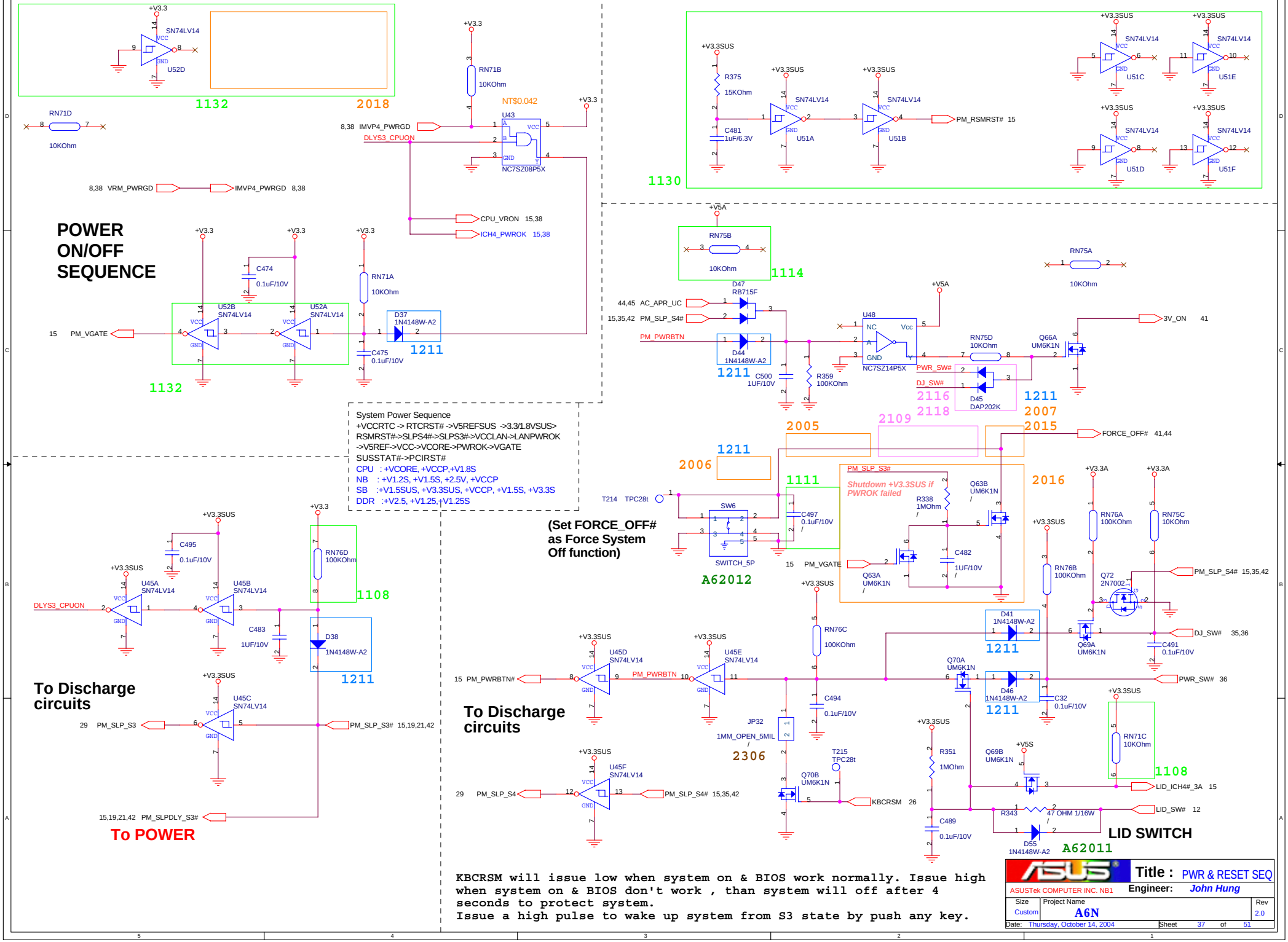


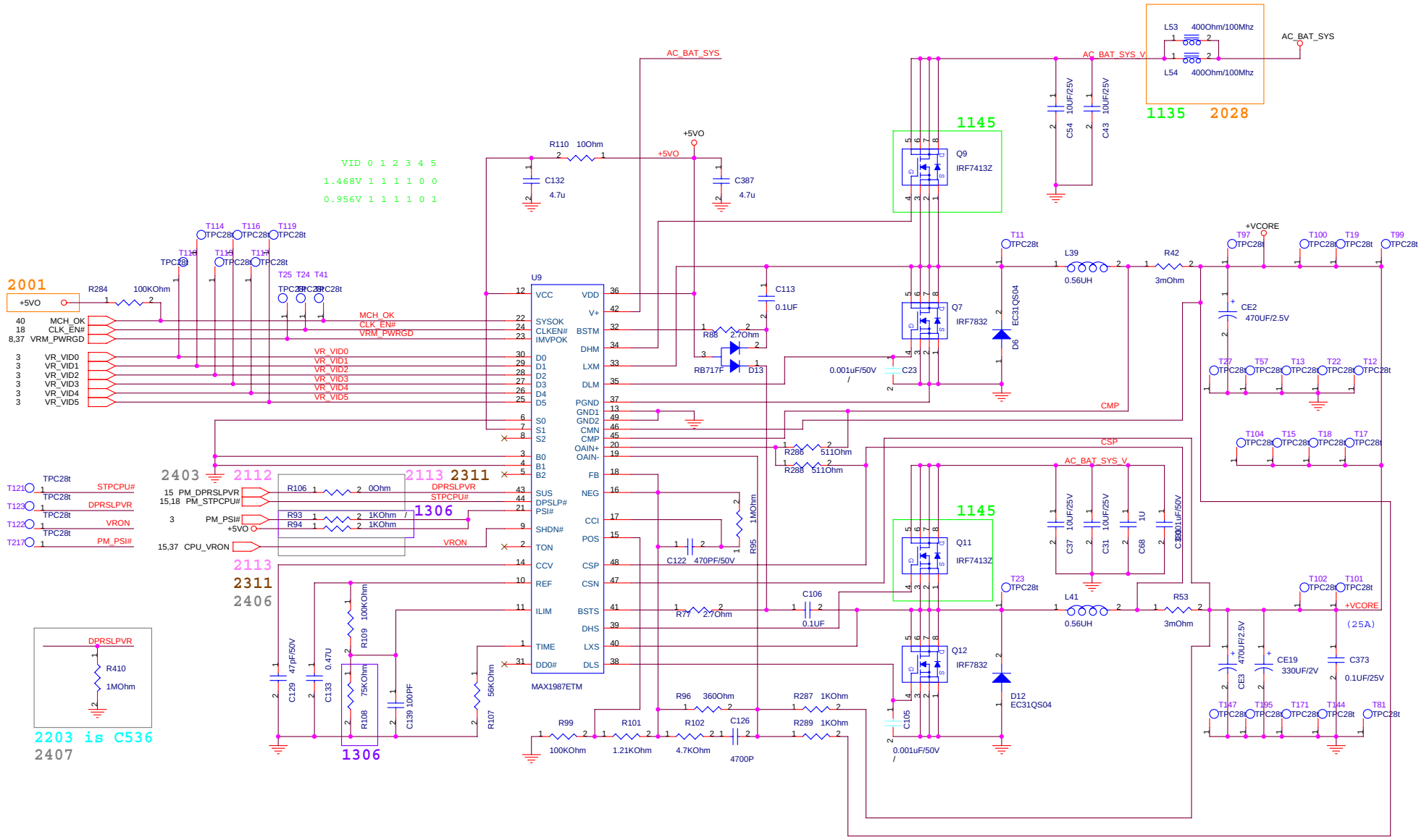
When power on, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D42 to Enable AudioDJ in OS.
Use D42 to Turn off AudioDJ when system be turned on in DJ mode.

<Variant Name>

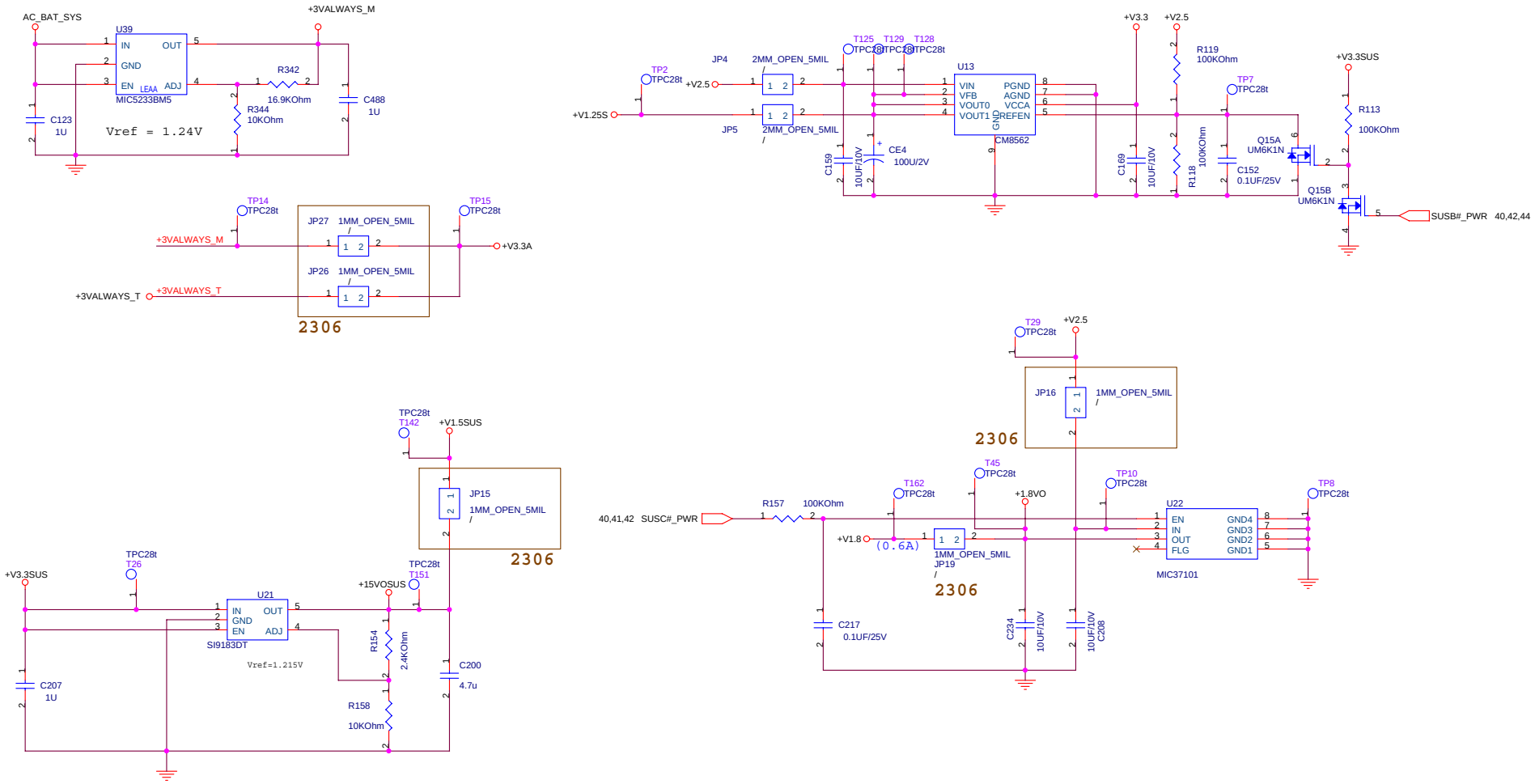
ASUSTek COMPUTER INC. NB1	Title : FAN&Audio DJ	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 35 of 51	


2401
T205 TPC28t
PWR_SW# 37
HOTKEY5#
SW5
SWITCH_5P
D7
181K
Power4 Gear
2101
2404
A62012
GND
HOTKEY4#
SW1
D10
E-Mail
HOTKEY3#
SW2
D11
Internet
HOTKEY2#
SW3
D9
Touchpad Disable
HOTKEY1#
SW4
D8
Power Switch
T206 TPC28t
T207 TPC28t
T208 TPC28t
T209 TPC28t
J1
DC_PWR_JACK_4P
GND_DCJACK
+V_DCJACK
A/D_DOCK_IN
L3
680 Ohm/ 100MHz
C13
0.1UF/25V
C14
10UF/25V
C15
1U
C16
0.1UF/25V
L9
680 Ohm/ 100MHz
1214
T210 TPC28t
T211 TPC28t
T212 TPC28t
T213 TPC28t
DC Power Jack
R406
330Ohm
+V3.3
RN9D
RN90D
RN9C
RN90C
RN9B
RN90B
RN9A
RN90A
10KOhm
330Ohm
0.1U
MARATHON# 26
EMAIL# 26
INTERNET# 26
DISTP# 26
CN1B
CN1A
CN1D
CN1C
1126
15 802_LED_EN#
20 802_ACTLED
Q59A UM6K1N
Q59B UM6K1N
802_LINKLED 20
RN81A
RN81B
10KOhm
1216
2307
1222
LED5
YELLOW&ORANGE
R309
220Ohm
PWR_LED#_R
2105
2107
RN80A
10KOhm
Q58A
UM6K1N
44 PWR_LED_UP
Q91
2N7002
DJ_LED
2011
2107
RN80B
R140
1KOhm
EMAIL_LED#_R
2013
2114
Q77B
Q77A
26 EMAIL_LED#
RN80D
R312
680Ohm
802_LED_EN#_R
Q79B
Q79A
802_LED_EN#
2208
RN80C
Q78B
R374
470Ohm
DJ_LED_R
Q78A
26 DJ_LED#
1112
2029
CON7
GND2
GND1
FPC_CON_20P
+V5S
+V5
+5VLCM
802_LED_EN#_R
EMAIL_LED#_R
CHG_LED#_R
PWR_LED#_R
DJPLAY#
DJSTOP#
DJFWARD#
DJBWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
26 KSI3
26 KSI5
26 KSI2
26 KSI4
35 DJ_SCAN
35,37 DJ_SW#
L43
80Ohm/100MHz
C435
0.1uF/10V
+V5S_TP
26 INTDATA_Q3
26 INTCLK_Q3
INTDATA_Q3
INTCLK_Q3
A6N1007
CHG_LED#_R
R311
1KOhm
2013
44 CHG_LED_UP
Q58B
UM6K1N
Title : FUNCTION KEY
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 36 of 51


POWER ON/OFF SEQUENCE
System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.8VSUS>
RSMRST#->SLPS4#->SLPS3#->VCCLAN->LANPWROK
->V5REF->VCC->VCORE->PWROK->VGATE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+V1.8S
NB : +V1.2S, +V1.5S, +2.5V, +VCCP
SB :+V1.5SUS, +V3.3SUS, +VCCP, +V1.5S, +V3.3S
DDR :+V2.5, +V1.25,+V1.25S
(Set FORCE_OFF# as Force System Off function)
To Discharge circuits
To Discharge circuits
To POWER
LID SWITCH
KBCRSM will issue low when system on & BIOS work normally. Issue high when system on & BIOS don't work , than system will off after 4 seconds to protect system.
Issue a high pulse to wake up system from S3 state by push any key.
Title : PWR & RESET SEQ
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size: Custom
Project Name: A6N
Rev: 2.0
Date: Thursday, October 14, 2004
Sheet 37 of 51

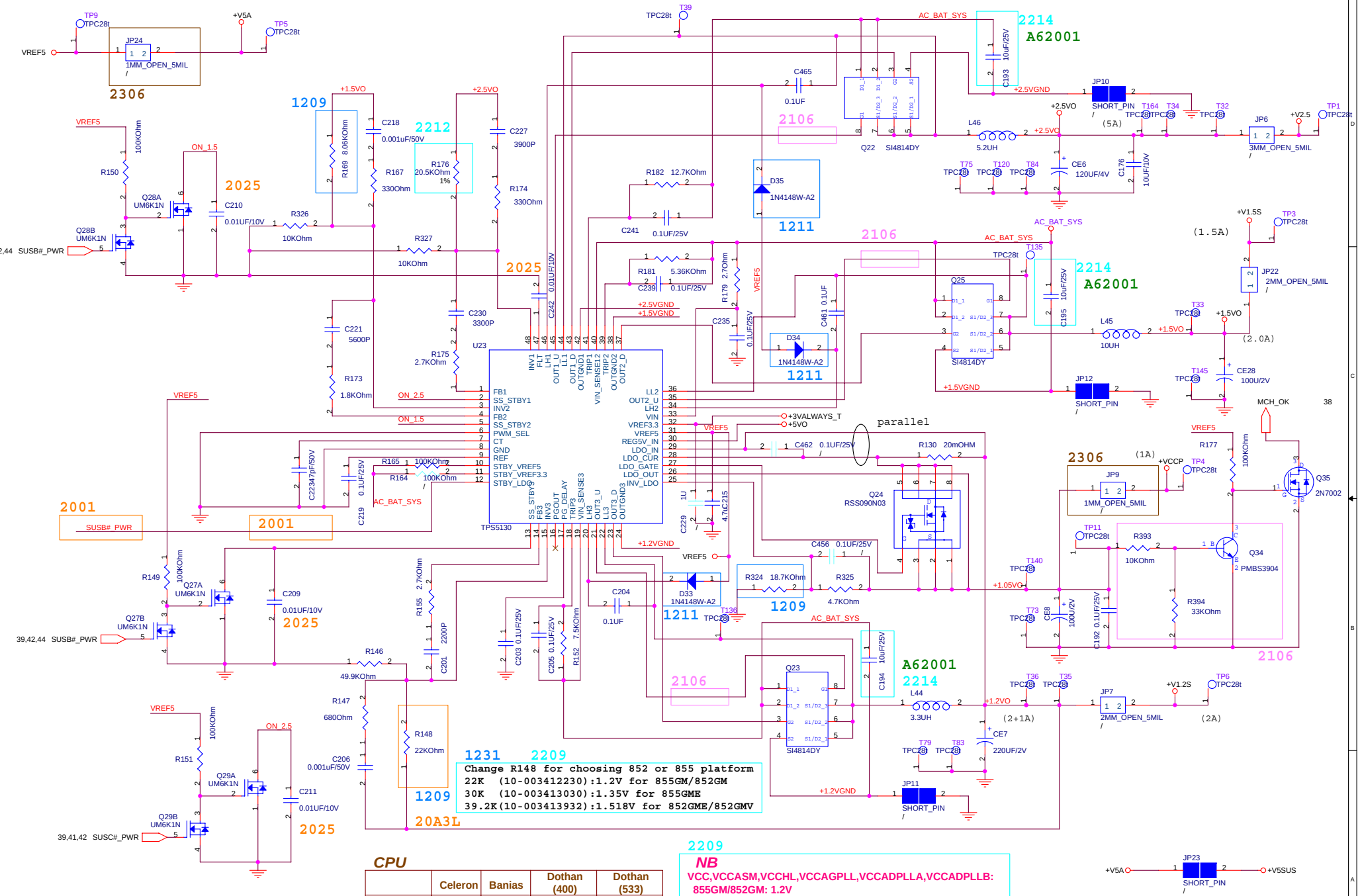


ASUSTek COMPUTER INC. NB1	Title : Vcore	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 38 of 51	



<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : 1.25V&1.8V	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 39 of 51	



CPU

	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4			Pin 1,2

NB

VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB:
855GM/852GM: 1.2V
855GME: 1.35V
852GME/852GMV: 1.5V

Title	2.5V&1.5V&1.2V&1.05V
Company	ASUSTek COMPUTER INC. NB1
Engineer	Adams Lin
Size	Custom
Project Name	A6N
Rev	2.0
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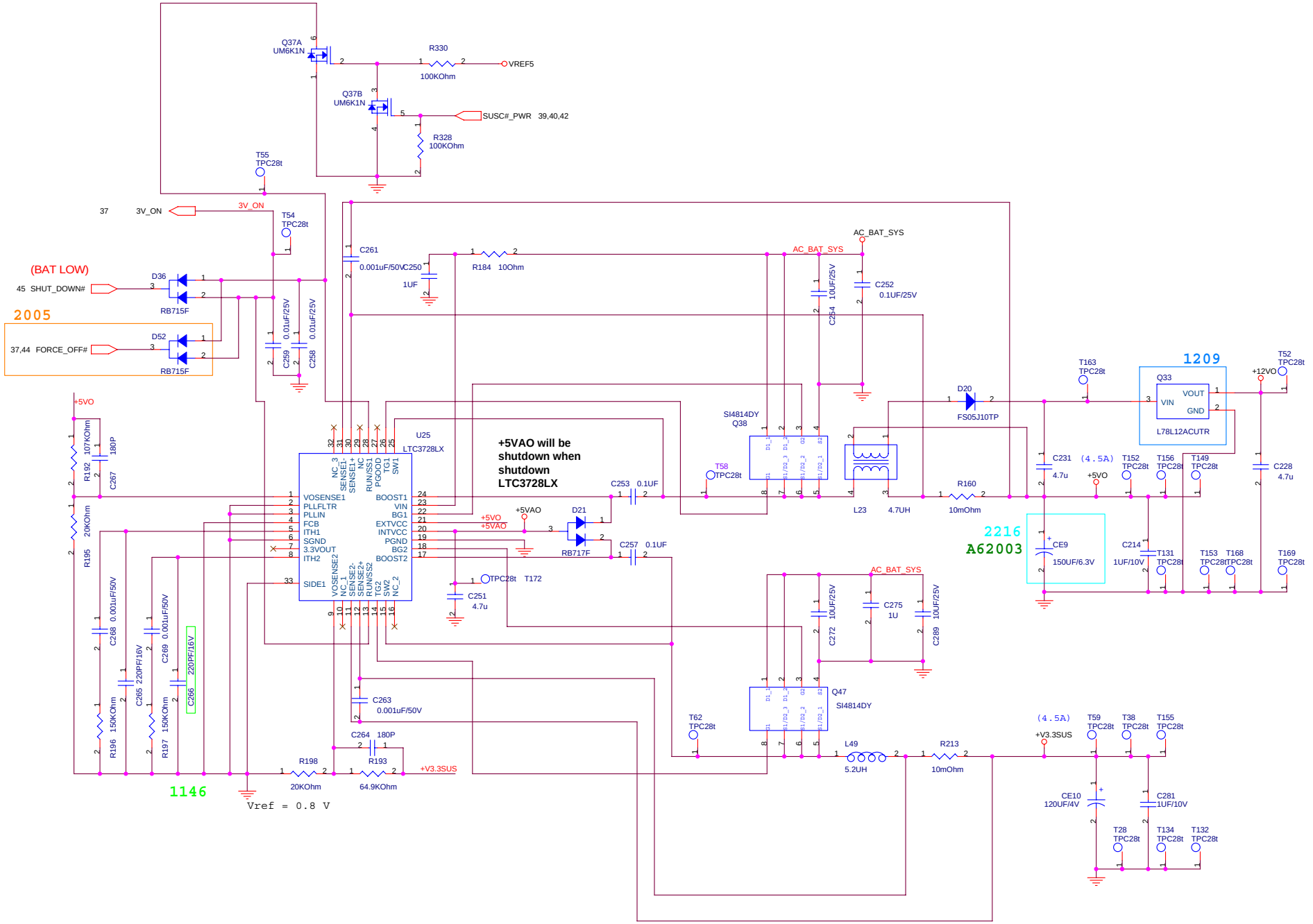
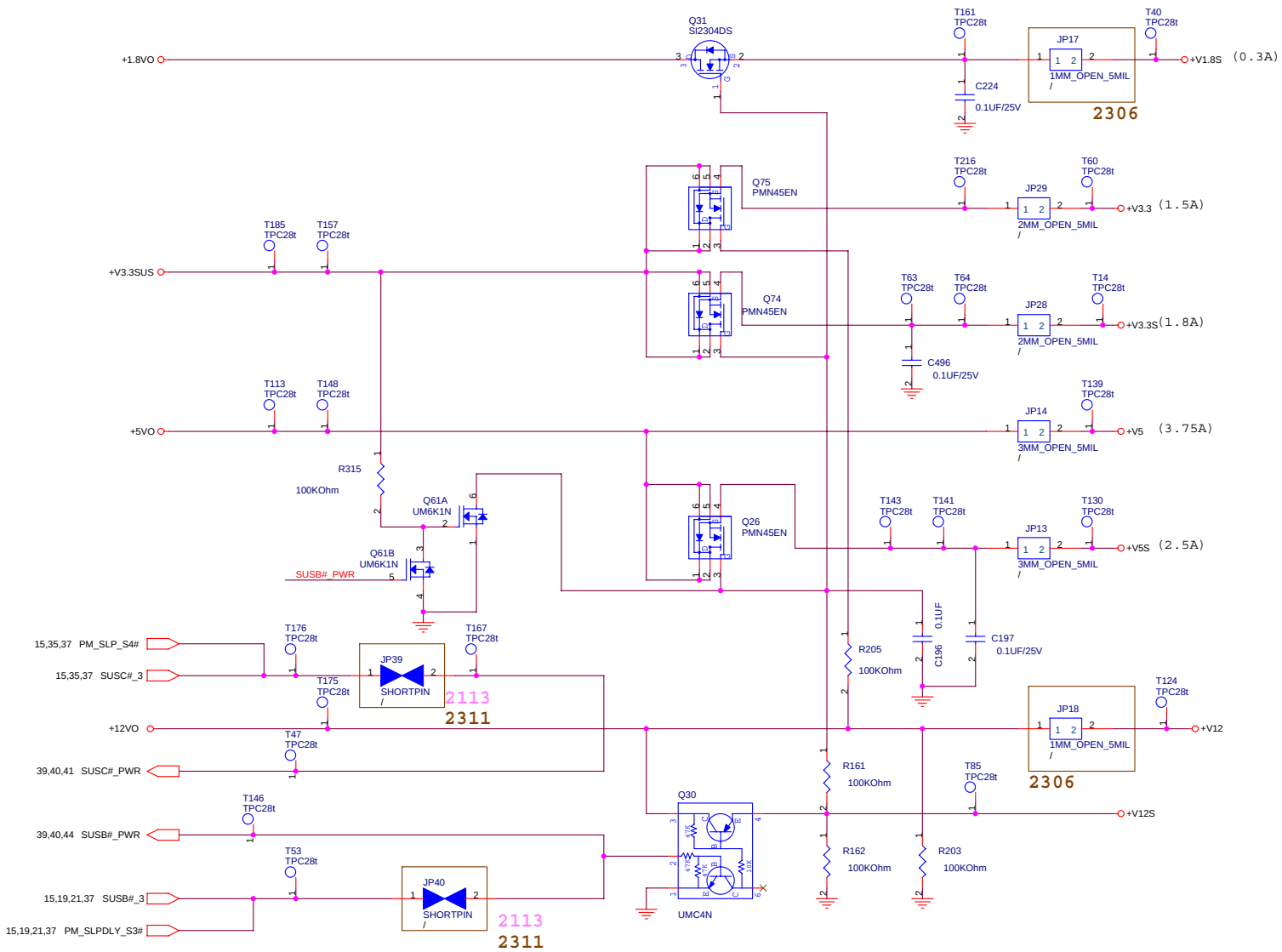


<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : SYSTEM	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 41 of 51	



<Variant Name>

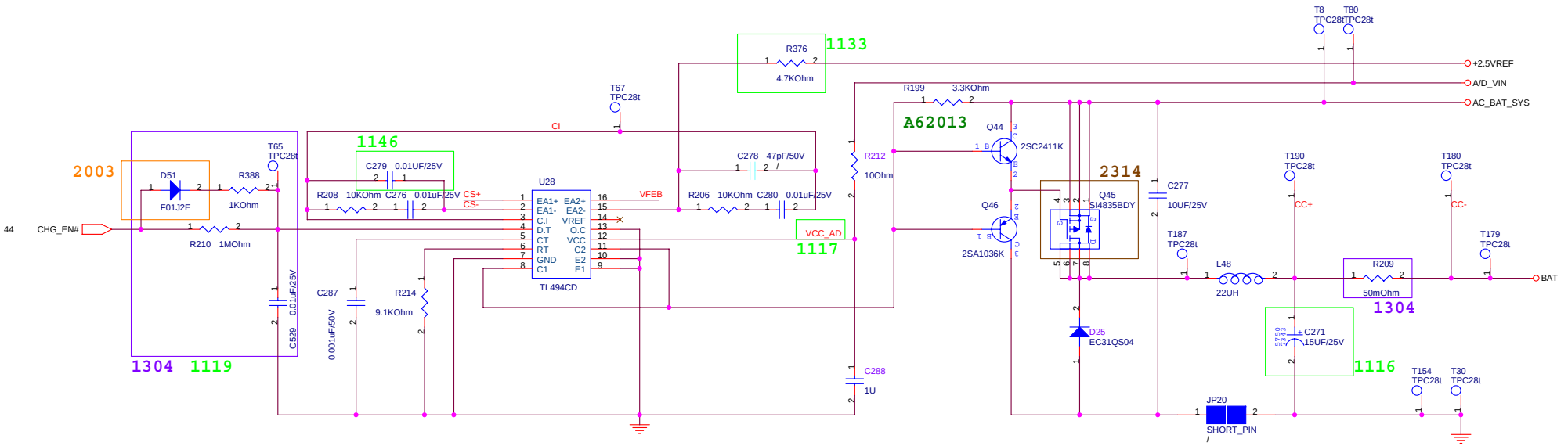
ASUSTek COMPUTER INC. NB1

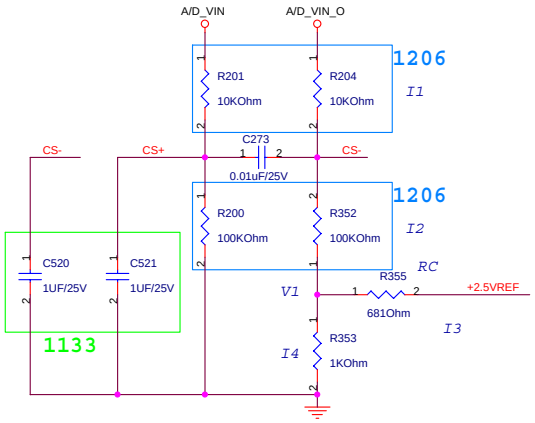
Title : LOAD SYWITCH

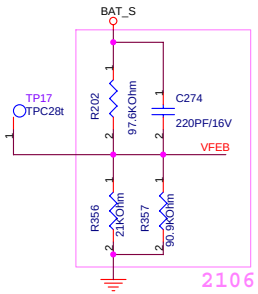
Engineer: Adams Lin

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 42 of 51

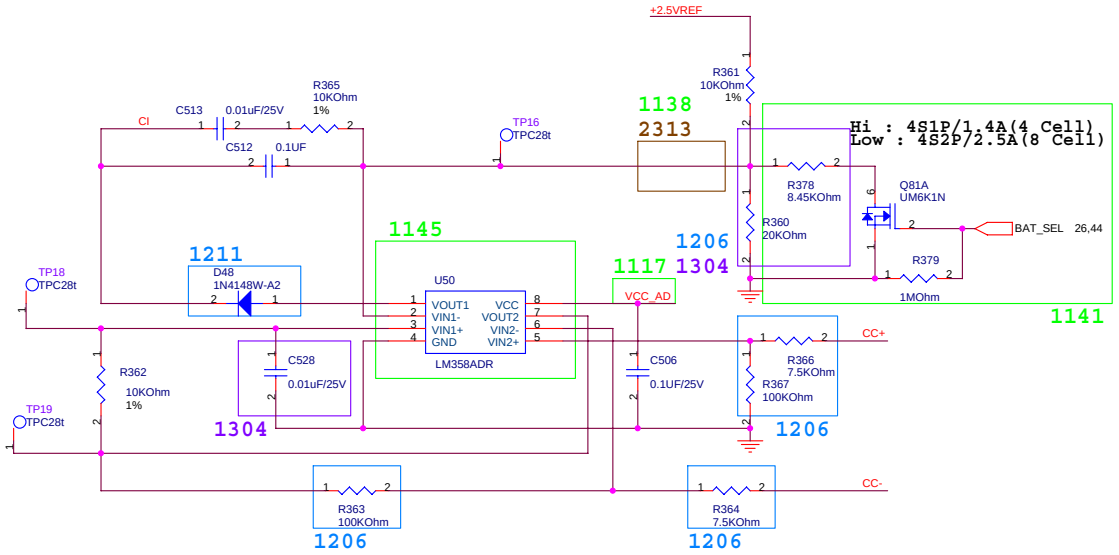






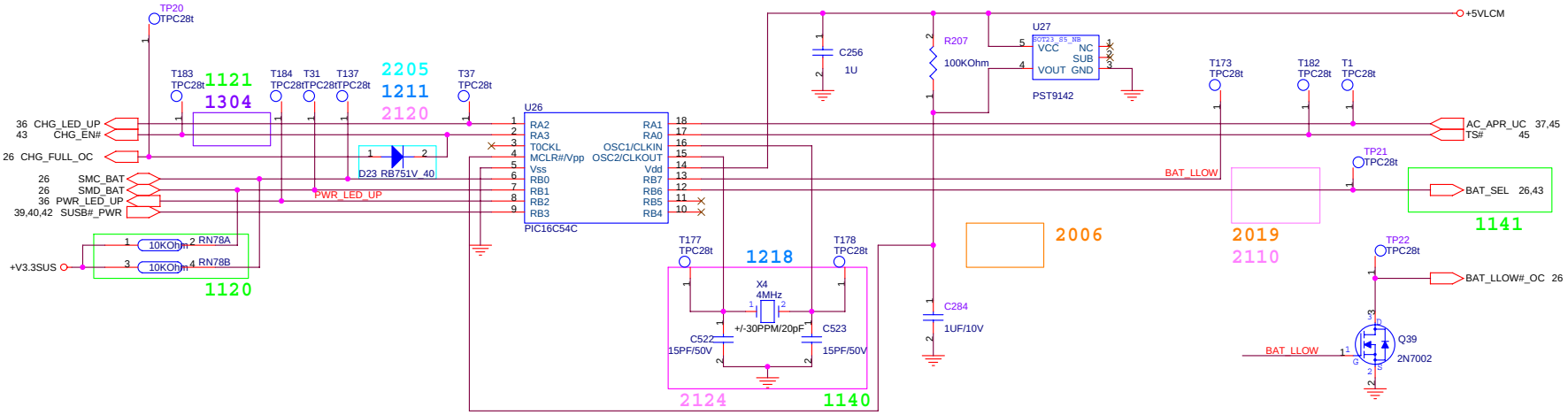
Current sharing = 3.1A

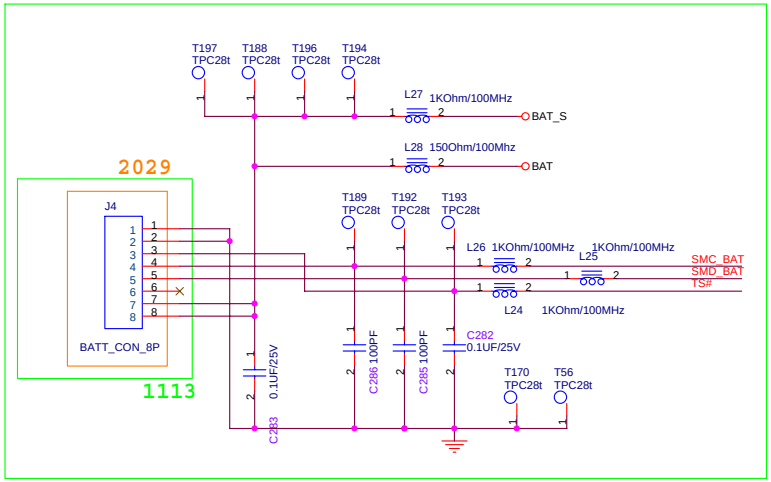
```
A/D_VIN=19V   A/D_VIN_O=19V-3.1A*50mohm=18.845V
CS+=CS-=19*(100/110)=17.272727V
I1=(18.845V-17.272727V)/10K=0.15723mA
V1=17.272727V-(0.15723mA*100K)=1.5497V
I4=1.5497V/1K=1.5497mA
I3=1.5497mA-0.15723mA=1.39247mA
RC=(2.5V-1.5497V)/1.39247mA=681 ohm
```

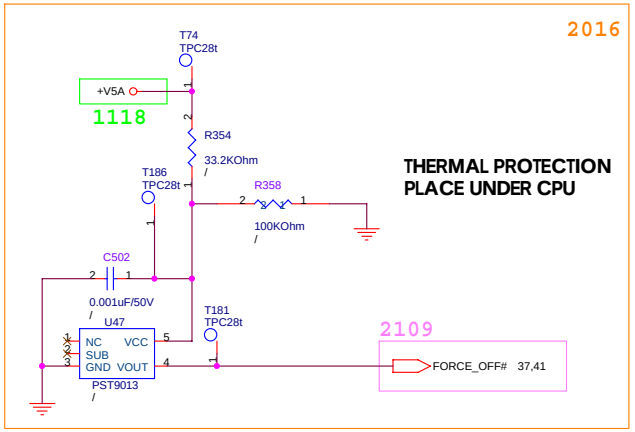


<variant_name>

ASUSTek COMPUTER INC. NB1	Title : CHARGER	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 43 of 51	

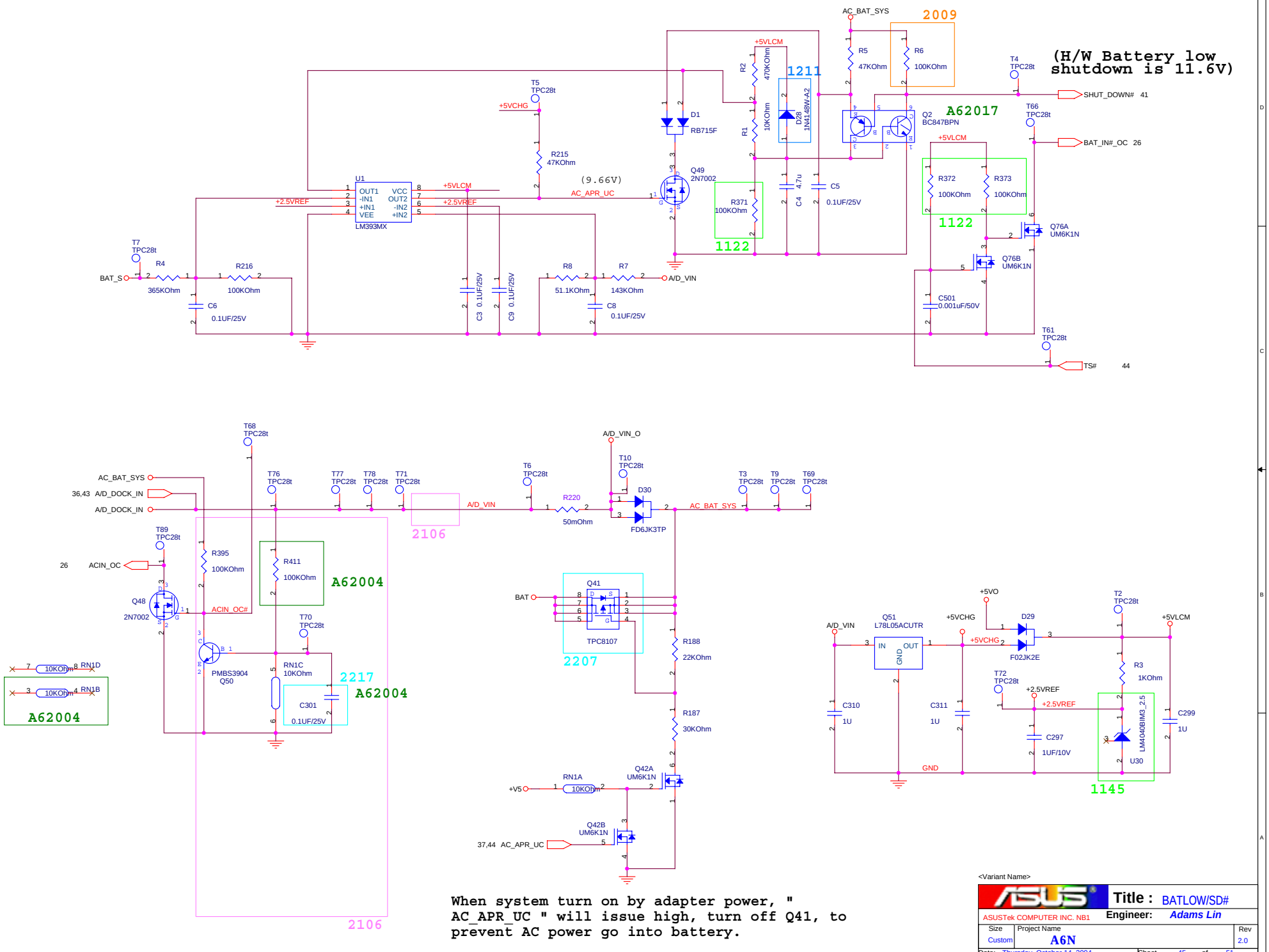






<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : PIC16C54	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 44 of 51	


(H/W Battery low shutdown is 11.6V)
When system turn on by adapter power, " AC_APR_UC " will issue high, turn off Q41, to prevent AC power go into battery.
Title : BATLOW/SD#
ASUSTek COMPUTER INC. NB1
Engineer: Adams Lin
Project Name A6N
Size Custom
Rev 2.0
Date: Thursday, October 14, 2004
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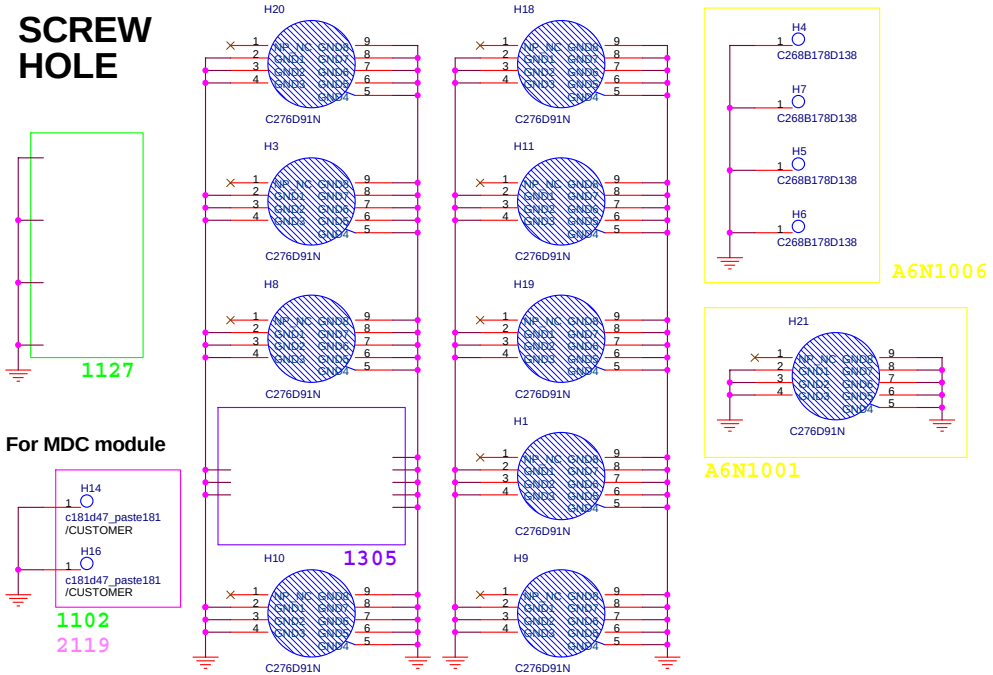
<Variant Name>

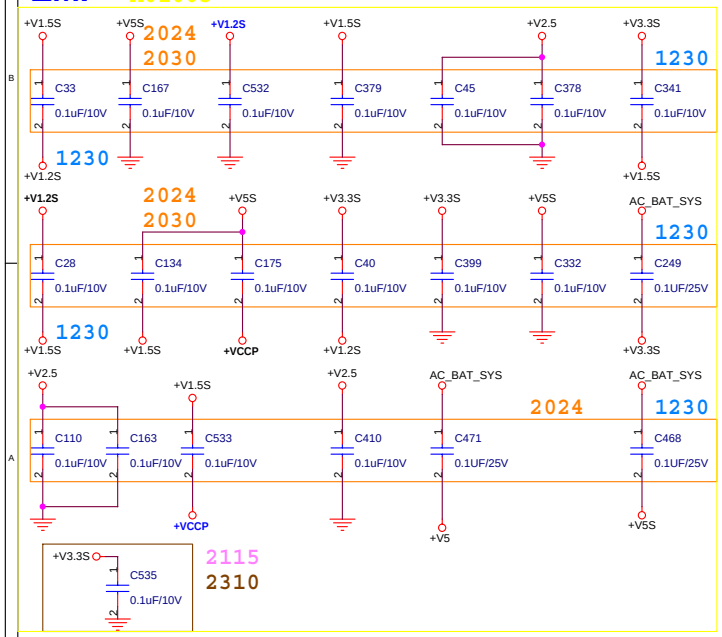
SCREW HOLE



CPU Throttling(BIOS setting): 100 degree C.
System shutdown(BIOS setting) : 110 degree C.
~~H/W shutdown(page 44, U47 , no load) : 105 degree C(Need fine turn R354).~~

EMI

A61005



Short Pad location:
Page37: JP32
Page39: JP4,5,15,16,19,26,27
Page40: JP6,7,9,22,24
Page42: JP13,14,17,18,28,29

Don't Short Pad: JP26
JP4:+V2.5 --Power In
JP5:+V1.25S
JP6:+V2.5(A6N bottom)
JP7:+V1.2S(A6N bottom)
JP9:+VCCP
JP13:+V5S
JP14:+V5
JP15:+V1.5SUS
JP16:+V2.5 --Power IN
JP17:+V1.8S
JP18:+V12
JP19:+V1.8
JP22:+V1.5S
JP24: VREF5-->+V5A(A6N top)
JP26:+3VALWAYS_T-->+V3.3A(open)
JP27:+3VALWAYS_M-->+V3.3A(short)
JP28:+V3.3S
JP29:+V3.3
JP32:KBCRSM

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	20 mils

37.5 OHM	WIDTH
TOP/BOT	12 mils

42 OHM	WIDTH
TOP/BOT	10 mils

55 OHM	WIDTH
TOP/BOT	5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	7 mils/ 10 mils

100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#

CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

<Variant Name>

ASUSTek COMPUTER INC. NB1

Title : SCREW HOLE

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

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FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

Rev	Date	Description
R1.0	03/12/19	1. Initial release.
R1.1 Green Block	04/02/03	1. Connect SDD0,SDD1 for RICOH request. Page 22. 2. Add MDC screw hole P/N & footprint. Page 46. 3. Connect CardBus chip INTC to PCI_INTD#. page 22. 4. Change CB_SD# location from KBC to ICH4 GPIO25. page 15,21,26. 5. Delete PCMCIA debug card function. page 18,23,29. 6. Host clock frequency select failed.Add a pull-down R to FS3 so that FS[4:3]=00 and Host clock frequency=100MHz. page18. 7. Load wrong value. Change RN39~RN48 from 56Ohm to 10Ohm. page 6. 8. Load wrong value. Change pull-up RN . page 37. 9. The value in M3N schematic is wrong. Change HUB_RCOMP_ICH4 pull-up R from 48.7KOhm to 48.7Ohm. page 14. 10. Modify +V3S to +V3.3S. page 30. 11. Can not boot in battery mode.Remove C497. page 37. 12. Modify 20-pin connector pin define and add DJ_LED function for new touchpad. page 26,36. 13. Due to height limitation, change BATT CONN. page 44. 14. Remove the pull-up RN75B because AC_APR_UC has been pulled-up in page 45. page 37. 15. Change CRT CONN because the original one was reversed. page 12. 16. C271 change form 10UF/25V/X5R to 15UF/25V/POSCAP. page 43. 17. U50 VCC change from +5VLCM to VCC_AD(19V). page 43. 18. For wrong connection, change R354 pull-up power plane from +5VO to +5VA. page 44. 19. Change R210 from 47K to 470K/0402. page 43. 20. Add RN78 to pull high SMC_BAT and SMD_BAT, and add UM6K1N to prevent leakage current into KBC. page 26,44. 21. For Power RD request, add R370 to CHG_EN#. page 44. 22. Replace RN32 with 3 single 100K resistor. page 45. 23. Change KB CONN pin definition because R1.0 was reversed. page 26. 24. Remove INVTER_A from KBC and load L33 because BIOS RD decide to use NB to control the pannel backlight. page 12,26. 25. Because P67/AN8 of KBC38857 cannot receive PWM signal, move CPUFAN_SPD_A to P57/DA2/PWM11 of KBC38857. page 26. 26. Change LEDs' power to 5V level. page 36. 27. Modify PCMCIA socket footprint. page 23,46. 28. Combine connector : Change CON1,delete CON3,CON4. page 12, 34. 29. Swap LAN connection(J2 pin5~12) for wrong connecting. page 33. 30. Modify PM_RSMRST# circuit. page 37. 31. For cost down, change X5,X7. page 19,30. 32. Combine two NC7SZ14P5 into one SN74LV14APWR for cost down.page 37. 33. To reduce jitter when charging, add R376,C520&C521. page 43. 34. For M6N R1.1 wrong connection, change Audio DJ DJ_SCAN pin from KSO4 to KSO1. page 26,35. 35. For Power RD request, add two beads L53&L54 at Vin Side. page 38. 36. Modify EDID and panel ID optional circuit. page 12. 37. Change CLR_DJ# to P53 because P54 of M38857 cannot be configured as output. page 26. 38. Add R377 for Power RD request. page 43. 39. Based on Ricoh's suggestion, remove CB_AGND and connect all AGND to generic GND. page 21,22. 40. For cost down, change X4. page 44. 41. Modify for battery 4S2P and 4S1P application. page 26,43,44. 42. For EMI RD request, change Cap of CRT Pi-filter from 3.3pF to 15pF. page 13. 43. Delete spread spectrum IC ICS91718 circuit because few model use it and not easy to buy. page 18.

ASUSTek COMPUTER INC. NB1

Title : 2nd source

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

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Rev	Date	Description
R1.1 Green Block	04/02/03	44. Change C172 & C173 from 22pF to 5pF and unload R125 to obtain more accurate 8MHz frequency. page 26. 45. For cost down, Power RD request to change Q9&Q11 to 07-005198012, U30 to 06-006002411, and U50 to 06-010112010. page 38,43,45. 46. For Power RD request, change , C266 from 33pF to 220pF, C279 from 0.1uF to 0.01uF. page 41,43. 47. Change U29 P/N for ME. page 31.
R1.2 Blue Block	04/02/19	1. LAN_RST# changes to 10K Ohm pull-down to GND. Page 15. 2. To be able to hear low frequency in headphone mode, change C423 & C424 from 10uF/10V to CE30,CE31 47uF/6.3V. Page 31. 3. Pull high BAT_IN#_OC, whose OC means Open Collector, to +V3.3 at KBC. Page 26. 4. There is only one SS0540 in A3N, change to 1SS355. page 35. 5. The power of LCD EEPROM connect to +V3.3S_LCD. When BIOS want to read EEPROM data, the EEPROM is still OFF,because +V3.3S_LCD is not enabled at this moment. Change EEPROM power to +V3.3S. page 12. 6. Change R360,R363,R364,R366,R367,R378 value for charger at C.C. mode and change R200,R201,R204,R352 at C.S. mode to get more accurate current limit value. page 43. 7. Add de-POP(reduce pop noise) circuit. page 31. 8. Change Fan control function from PWM mode to DC mode. page 35. 9. Based on Power RD's request, change Q33,R169,R148,R324. page 40,41. 10. S5N can not turn on some panels since its diodes in inverter circuit have higher forward voltage. Follow S5N, change DAP202K and 1SS35 in inverter circuit to Schottky diode RB717F and RB751V-40 respectively. page 12. 11. Electrical characteristics of diode 1SS35 and 1N4148-A2 can be compatible, but 1N4148-A2 has lower price. For cost down, change 1SS355 to 1N4148-A2. page 12,16,21,35,37,40,43,44,45. 12. Change "Back light adjust" function from North Bridge to KBC. Change "CUPFAN_SPD_A" from KBC to ICH4 for BIOS request. page 8,12,26,35. 13. For cost down, change audio AMP from APA2020A to G1420. page 31. 14. A3N R1.1 uses the same AC_IN jack as L3F, which was found easy to be damaged. Change it to solider one used on A2. page 36. 15. Follow M6N and W1N to modify RTC circuit. page 15. 16. Un-mount Q59 and RN81 to control WLAN led directly from SB's GPIO pin: 802_LED_EN#. page 36. 17. Swap 1394 TPB0+/-,TPA0+/- for smoother layout. page 22. 18. X4 is dip type and at top side which may be lost in SMT IR re-flow for bottom side. Change X4 to SMD type. page 44. 19. Add mini-PCI and USB WLAN hardware disable circuit page 12,15,20. 20. QT report a bug: The "Center/Subwoofer Speaker Out" is invalid after setting "Number of Speakers" to 6-channel mode for 5.1 speaker output and then executed "Speaker Test". Modify relative circuit. page 30,32. 21. Fine tune audio amp low-pass frequency. page 31. 22. Delete RN79 because after experiment we find it can be un-mounted. page 36. 23. Remove LCD EDID relative circuit. page 8,12. 24. Combin R191,R308,R380 and R381 into 4R8P RN88. page 26. 25. Follow S5N to modify CRT_DDC circuit to prevent current leakage. page 13. 26. Although crystal DIP type is cheaper than SMD type, but costs more manpower. Change X5 and X7 back to SMD type. page 19,30. 27. Improve accuracy of reading fan speed. page 35. 28. Swap RN4 and pin8,9 of RP4 for smoother layout. page 13,17. 29. For cost down, change U6 and U12 NS LM358MX (06-010008000) to TI LM358ADR (06-010112010). page 30,35. 30. For EMI RD's request to modify BOM. page 18,19,22,30,31,32,33,46. 31. Add description of choosing 855GM or 852GM/GME/GMV platform by changing R148. page 40. **32. Debug code will stop at "A0" or "06". Modify SMBus layout: 1. Daisy chain routing. 2.Don't cross power plane when the trace refer to power plane. Page 17.**

Rev	Date	Description
R1.3 Purple Block	04/03/11	1. Pin23, ISOLATEB, of LAN 8100CL need to be low in S3. Follow MB P4PE-X to connect it with PM_SLP_S3#. page 19. **2. Debug Code will stop at "13". Change SMBus Pull-High RN29 from 4.7KOhm(0402) to 1KOhm(0603). page 17.** 3. Improve MIC layout. page 12,32. 4. For Power RD's request to modify charger circuit. page 43,44. 5. Delete screw hole H2, to prevent CN7 short with H2. Layout engineer create a new screw hole. page 46. 6. For Power RD's request to modify BOM. Change R108 from 100K to 75K for OCP, un-mount R93 and mount R94 to meet Intel CPU spec. page 38.
R2.0 Orange Block	04/04/15	1. Sometimes Debug Code will stop at "00" in ON/OFF test. Modify power sequence circuit , delete R163. page 38,40. 2. Based on request came from factory to update all testpoints' symbol because all testpins are changed from 75mil to 68mil. All pages that include test points. 3. Power team request, cost down D51 part. page43. 4. Fine-tune R385,R386 and R387 to get more accurate level of fan ON/OFF detection. page35. 5. When system with battery only. System can't be power on after push Force OFF button SW6. Because SW6 connect to SHUT_DOWN#, but this signal will be latch low(power design: when battery low, page 46 : battery low detect circuit will issue low than latch it.) when it is at low state. Don't connect SHUT_DOWN# to SW6 at page 37.(SHUT_DOWN# already connected to 3V_ON at page 41. Connect SW6 to U25, and change D40 to 1N4148(delete at item 2015). Page 37. 6. Because A3N use SW6 as "Force OFF" button ,not "Reset" button. We don't need connect SW6 to PIC16C54C. Delete D24.page37,44. 7. Can't turn on Audio DJ when system only with battery and no adapter. Because +V3.3SUS will be turn off when system only with battery. Need turn on +V3.3SUS by connect DJ_SW# to 3V_ON. Change D45 to DAP202K. Page 37. 8. LAN crystal accurate is 39.2ppm, it can't meet spec. +/-30ppm). Change from 15pF to 18pF to meet spec. page 19. 9. Some system can't boot by battery only. Because signal "SHUTDOWN#" be latch at low state. Change R6 value from 470K to 100K. Page 45. 10.QT bug : Noise occur from headphone via speaker out jack. Change R124,R298,R285 from Bead to 0 ohm. Page 30,31. 11.The Power LED should not be bright when enabled Audio DJ in power off mode. Page 36. 12.The inductor will cause the 2.5V power control loop unstable. Change L40 to R389 Page 19. 13. Balance the LED Brightness. Fine tune R value,R140 470-->220,R311,R312 470-->1K. Page 36. 14. G571(U49) 593 Control Signal(U37) VPPD0 : VPPEN1 VPPD1 : VPPEN0 Otherwise, CardBus Card may be destroyed. Page 23. 15. When issue OTP_RESET#, system can't be turn off & display white screen. Because LTC3728 can't be shutdown by only put low 3V_ON. Need shutdown +V3.3SUS & +5VO at the same time. Delete D40. Page 37. 16. Change Q63,Q66,Q71 and no load Q63,R338,C482,R354,R358,C502,U47 for cost down. page 35,37,44. 17. Add test point for Taipei Factory request. page 6,12,15,16,19,30,36,37,38,39,42,43,44 18. QT bug: Pop noise can be heard via headphone when system boot, restart and resume from S3. Modify De-Pop circuit. page 31,37. 19. Taipei factory request : Add R391 for different battery charge current test at 8 cells and 4 cells. Page44.

ASUSTek COMPUTER INC. NB1

Title : REVISION(2)

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

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Rev	Date	Description
R2.0 Orange Block	04/04/27	20. EMI request, load C144, C525. page 32. 21. ICH4 GPIO [24:43] , default state is output high, if PID_[0:3] be connected to GND by LCD cable, these GPIO will issue +V3.3(default output high) short to GND during system power on. Add R=2.2K to prevent this kind of situration. Page 15. 22. Measurement team Problem: VGA EA fail below items 1,V-SYNC:under shoot over 30% of high level voltage range. 2,H-SYNC:over shoot over 30% of high level voltage range, under shoot over 30% of high level voltage range. Change Change C304, C305 from 5pF to 33pF. Page 13. 23. EMI request use Choke on USB & 1394 ports. Delete option R, don't co-layout. Page 22,34. 24. EMI request : Add C531,C532,C533,C535. Delete C147,C433. Change C110,C163 connection. Change C410 location. Change C378,C379,C410,C163,C110 to 0.1uF/10V. Change C471,C468 to 0.1uF/25V. Change C45,C33,C28,C134,C332,C399,C341 to 0.1uF/10V and don't load. Change C40 to 0.1uF/10V. Change C249 to 0.1uF/25V and don't load.Page 10,46. Change R104 from 0 ohm to bead. Page 31. 25. Change C26,C98,C104,C325(page3), C362(page7), C324,C329(page9), C436(page14), C190,C441(page16), C366,C367(page19), C247(page21), C467,C473,C478(page22), C236(page23), C209,C210,C211,C242(page40), from 0.01uF/25V to 0.01uF/10V. Use 10V is OK. 26. Measurement team Problem: VGA EA fail in rise time and fall time of RGB signal at resolution 1024X768 at 60Hz. Change L6,L7,L8 from 75Ohm/100MHz to 70Ohm/100MHz. Page 13. 27. Load FAN on/off component : /FAN_SPD. page 35. 28. Change L53,L54 from 09-012400000 to 09-012400001 for cost down. page38. 29. CON1,CON7,CON12,CON15 and J4 change to formal P/N. page 12,24,25,36,44. 30. For EMI RD's request, change R384 from 0 ohm to Ferrite bead, and add EMI capacitors: C28,C33,C45,C134,C167,C175,C332,C341,C399,C249. Page 32,46. A3L. For A3L platform : change U32 to 852GM, R148. page 6,7,8,9,40.
R2.1 Pink Block	04/05/14	1. For ESD test fail at switch, If we want to use ESD protect diode, we can't connect switch pin 1&2, pin3&4 to make sure the energy will go through ESD diode : SW1~5. page36. 2. Forget pull high at D54.3. Add R392 pull high to +V3.3S. page 31. 3. For cost down. Delete R=0 OHM. R389,R331,R124,R298,R285,R281,R276(no load),R290(no load). page 19,22,30,31 4. QT report that a "pop" noise occurs when booting. This is because the timing of OP_SD# to control audio AMP ON. Change D49 from DAP2020K to 1N4148W-A2 to control the AMP shutdown only the JACK_IN#, and control SE/BTL# by D54.3. page 31. 5. In audio DJ mode, DJ_LED turns on Q91 and PWR_LED_UP will connect to GND which may demage PIC. Use RN80A to prevent it. page 36. 6. Power RD modification: Delete 0 Ohm: R135,R136,R137 Delete U24, change Q34 to 3904 and add R393,R394. Change R202,R356,R357 BOM to modify BAT CV tolerance to more accurate. Delet Q5,Q1,C18,R9,R10,RN2 and add R395. page 40,43,45. 7. Swap RN80 for smoother layout. page 36. 8. QT bug: when booting or being idle, two A3 with USB CCD module will sometimes appear "Hi-speed device plug into low-speed hub" in Windows XP/2000. Adjust USBRBIAS and USBRBIAS# external resistor R138 from 18.2ohm to 22.6ohm. page 15.

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R2.1 Pink Block	04/07/16	9. For TPE_ENG Power RD's request to unify OTP_RESET#, FORCE_OFF#_SW and FORCE_OFF# into single name: FORCE_OFF#. page 37,44. 10. About 2019 item, factory don't need it now. Delete R391. page 44. 11. C117 don't need use 25V, change to 4.7uF/10V. page 9. 12. Factory found that there are two A3 systems will fail at On Off test. Net " PM_DPRSLPVR" will be issued wrong status by Vcore Power IC MAX1987 when system on . Add a 20pF at R106.2 or change R106 from 1K to 0 OHM can solve this issue. Change R106 to 0 OHM. Page 38. 13. Power request. Don't need use 1K ohm, change R100,R292,R329,R168 from 1K to 0 ohm. Page 38,42. 14. Fine tune E-mail LED (R140 : from 220 to 1K)& Wireless LED (R312 : from 1K to 680) for customer's request. Page 36. 15. Because C535 will touch with the boss of C mechanical part. Don't load C535. Page 46. 16. Even we pull down pin 1 or pin 2 of DAP202K, the UM6K1N is still possible to be turn on. It is because that the maximum forward voltage of DAP202K is 1.2V but the gate threshold voltage of UM6K1N is 0.8V~1.5V. Change D32,D45 and D54 from DAP202K to RB717F since the maximum forward voltage of RB717F is only 0.37V. Page 31,35,37. 17. Phone jack (P/N: 12-140001087) used in A3N/L has been phased out. The vendor suggests us to use 12-140001088 as substitution. Page 31. 18. As R2.1 item 16, we changed D32,D45 and D54 from DAP202K to RB717F. But SMT reports that RB717F has smaller package than DAP202K such that may cause connection between RB717F and pad failed. In A3 design, the forward current will be no more than 0.5mA. According to DAP202K forward characteristics, it's impossible to reach the minimum threshold voltage of UM6K1N (0.8V). So it's safe to change D32, D45 and D54 from RB717F back to DAP202K. Page 31,35,37. 19. 5E customer doesn't need the MDC and SIR function, so A3L removes the relative components: R30, R31, R129, R143, R144, R186, R190, R305, RN21, RN66, RN67, C149, C174, C180, C185, CN6, CON5, H14, H16, U35. Page 15,28,30,33,46. 20. D23 uses DIODE 1N4148W-A2 but its larger forward voltage may makes KBC M38857 detect error. Change it to Schottky diode SS0540 that has smaller forward voltage. Page 44. 21. Taipei SMT reports that X2 (07-010303271) has open risk, and recommends us to use 07-010303273 as first source, 07-010303271 and 07-010703273 as second source for manufacturability improve. Page 15 22: Factory found that there are some X4 part don't work. Change C522,C533 from 33pF to 15pF. Page 44.

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R2.2 Light Blue Block	04/09/22	3. Refer to R2.1 item 12, reserve C536 but load 1M ohm for PM_DPRSLPVR. Page 38. 6. Modify layout footprint for R:2.1 item 21. Page 15. 7. Based on Power RD's request, change Q41 from 07-005151010 to 07-005159010 for cost down. Page 45. 8. 7H Project Vulpix : Remove Super I/O : U11,C143,C146,C127,C151,C136,R103,RN17,Q16,R82,R63. Page 27,18. Remove Printer Port : LN1,LN2,LN3,LN4,CN8,CN9,CN10,CN11,L36,CN7,C300. Page 28. Remove IR: R129,U35,C174,C180,C185,RN21,RN66,RN67. Page 28. Remove MiniPCI Port : CON17,C487,C485,C469,C486,C470,R332,R81. Page 20,18. Remove WLAN function : RN86,Q87,Q88,Q79,R312. Page 12,20,36. Remove USB CMOS camera & USB WLAN funciton : CE29,L51,L52,L50,C11,C12. Page 12. Set normal type ODD as master : No load R127, Load R126. Page 25. 9. Power "VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB" have different defined value in datasheet and RDDP. Confirmed with Intel FAE to get the final correct value, and will be phased in on R2.2 and R:2.4 BOM. Page 9,40. 10. R249,R251,R252 will have different value based on different North Bridge. All the corresponding values are listed in Page 7 and will be phase in on R2.2 and R:2.4 BOM. Page 7. 11. Because Vendor (CC&C) can't support hardware On/Off WLAN module function, don't load Q87 at R:2.2 & R2.4. Page 12. 12. Factory found that there are some DDR SO-DIMM(UNIFOSA,MOSEL)will fail during Memory test of Run-In test. Change R176 from 19.6K to 20.5K 1% , fine tune +V2.5 from 2.5V to 2.592V. Add SO-DIMM noise margin at R:2.2 & R:2.4. Page 40. 13.For 5E customer,don't need USB CMOS camera,no load L51,C12. Page12. 14. Change C193,194,195 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.5mm height(11-03B210621) to 2.0mm(11-031110621). Page 40. 15. For M/E request, add a second source 12-172010300 on CON2. Page 12. 16. Change CE9 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.8mm height(11-08D210711) to 1.8mm(11-08D215706). Page 41. 17.When the system temperature rise high due to the system running at heavy loading. The leak current(IR) of D30 schottky diode will be increased, the H/W AC detect circuit will make a wrong state. Net " ACIN_OC " will issue " high". Change C301 from 0.1uF to 1Kohm, it can solve this problem. Make sure it will issue "low" at this moment.Page 45. 18. For the request from 7H customer, change CE15,CE18 from Tantalum capacitor (11-015000220) to Oxi capacitor. Page 9. 2004/9/29 : Change at VPLP R:2.2, A3L R:2.4,A3Le R:2.4,A3Ne R:2.4. 19. For the request from 7H customer, follow the USB spec. , one port max current is 0.5A, so two ports max current is 1A. Change F1,F2 from 1.5A/6V polyswitch to 1.1A/6V polyswitch, P/N is 07-014110900 (2nd source is 07-014110201). Change at VPLP R:2.2 only. Page 34
	04/10/01	20. 7H customer found that there are some VPLP system use Bufferlo WLI-CB-AG54 Wireless LAN PC-card will fail at some channel when connect to Access Point. Add C390 with 10pF and change C499 from 0.1uF to 1000pF (11-034110241) to reduce clock and power noise. Modify VPLP BOM onley. Page 18,23.
	04/10/14	21. +V5A will issue leakage current to +V3.3SUS by U48.4 --> D45 --> RN76B when plug in Battery module only. Change C379 from 0.1uF to 1K ohm (10-004401020). Page 46.

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R2.3 Brown Block	04/07/23	1. For Vendor request : Pin footprint diameter is 1.0mm+/-0.05, but ASUS rule is diameter*diameter =(L*L+W*W). Modify Battery Connector J1 as vendor spec. **NO FIX**. Page 44. 2. For Thermal RD request : Let the fan be off before BIOS control because it can let user doesn't feel the fan on-off noise obvious while system boot. Use OP_SD_DLY to control it. Page 31,35. 3. None (the same as R:2.2 item 1) 4. QT Bug: Noise occurred during system resume from S1. The timing of DLY_OP_SD# and AC97_RST# still can not prevent the pop noise. Realtek recommands to use pin47 EAPD to substitute AC97_RST#. This pin can be controlled by codec driver to meet our timing request. Page 30,31. 5. Change D23 to SCHOTTKY RB751V-40 to decrease part type. Page 44. 6. Modify short pad for factory's request. page 37(JP32), page 39(JP15,16,19,26,27), page 40(JP9,24), page 42(JP17,18). 7. For A3 series ID2 power switch, add a Blue LED,change R309 from 470 ohm to 220 ohm. Page 36. 8. Add CPU +VCCA power switch circuit to meet Celeron/ Banias/ Dothan(400)/ Dothan(533) CPU spec. Page 3,4,18. 9. Base on Factory SMT request : modify CN7 & CON9 footprint (only for 1.6mm thickness PCB). page 13,28. 10. Re-load C535 because the position is changed and will not touch with boss of C mechanical part. page 46. 11. Modify R106, R100, R292, R329, R168 to Short Pin JP36, JP37, JP38, JP39, JP40 for power function parts cost down. page 38,42. 12. To synchronize the parts in the schematic with BOM, change R104, R302, R303, R91, R92, R384, R111, R112, R31, R30 to L55, L56, L57, L58, L59, L60, L61, L62, L63, L64. page 31,32,33. 13. Remove 0 ohm: R377 and R180 for cost down. page 22,43. 14. Based on Power RD's request, change Q45 from 07-005151010 to 07-005159010 for cost down. Page 43. 15. BIOS RD request to distinguish PCB version by reading PCB_VID[2:0]. Change PCB_VID[2:0] configuration and add descriptions. Page 21. *. Because R:2.4 item 2. We can't phase in R:2.3.
R2.4 Gray Block	04/08/27	1. To improve ESD margin. Add De-Bounce circuit. Page 36. 2. Add GST[2:0] strap circuit for supporting Dothan 533 CPU. Page 8. 3. Taipei Factory repored that some A3N systems still failed(13/5000) in resuming from suspend to RAM. Power RD request to change JP36 back to R106 and change the value to 100K ohm. Page 38. 4. For EMI request. Connect switch pin 1&2, pin3&4 of SW1~5. page36. 5. Change PCB VID for R.2.4 page 21. 6. Remove JP37 and JP39. page36. 7. As R2.4 item 3, Power RD find the root cause: When system booting or resuming from S3, the siganl " PM_DPRSLPVR" from South Bridge, it will be floating in a short time(40ms) and cause +VCORE output wrong voltage(0.76V). Add a resistor 1M ohm between net " PM_DPRSLPVR" and GND in order to keep PM_DPRSLPVR at low state when floating. Add R106 = 0ohm and change C536 to R410 (1M ohm). page 38.

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A6N R1.0 Yellow Block	04/08/27	1. Add a screw hole. page 46. 2. Delete WLAN USB port and swap some USB port for layout request. Delete L52,C518,C519,C11.Page 12,15,17,34. 3. Change all test point from S00050(part number) to S00049. All Pages. 4. Power team request : CM2855 will be phased out after 2004/09, change part to SI9183, change R398,R400 value, and delete R405.Page 4. 5. For EMI request, change capacitor connection. Page 46. 1. C33 +V1.2S-----+V1.5S 2. C378,C45 +V2.5-----GND 3. C379 +V1.5S------GND 4. C332 +V5S--------GND 5. C535 +V3.3S-------GND 6. C471 +V5 -----------+AC_BAT_SYS 7. C468 +V5S-----------+AC_BAT_SYS 8. C533 +V1.5S----------+VCCP 9. C134 +V5S-------+V1.5S 10. C28 +V5S---------+V1.2S 11. C175 +V5S-----+VCCP 12. C341 +V3.3S--------+V1.5S 6. For layout request. Modify screw hole. page 46. 7. Swap pin1~6 of CON7 connection for new Touch Pad membrane. Page 36. 8. For ID team request. Change the color of CRT connector. Page 13.

Rev	Date	Description
A6N R2.0 Green Block	04/09/23	1. Change C193,194,195 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.5mm height(11-03B210621) to 2.0mm(11-031110621). Page 40. 2. For M/E request, add a second source 12-172010300 on CON2. Page 12. 3. Change CE9 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.8mm height(11-08D210711) to 1.8mm(11-08D215706). Page 41. 4. Power: When the system temperature rise high due to the system running at heavy loading. The leak current(IR) of D30 schottky diode will be increased, the H/W AC detect circuit will make a wrong state. Net " ACIN_OC " will issue " high". To solve this problem, change RN1B (10K ohm) to R411 (100K ohm) to make sure it will issue "low" at this moment. Change C301 from 1K to 0.1uF at A6Ne R:1.1 Page 45. 5. For the request from 7H customer, change CE15,CE18 from Tantalum capacitor (11-015000220) to Oxi capacitor. Page 9.
	04/09/30	6. Measurement team test fail at CRT function : Pattern: White cross hatch with one pixel lines on black background at 31 kHz. Change R40 from 137 ohm to 127 ohm. Page 8.
	04/09/30	7. Measurement team test fail at Audio quality : PC-D-A (Back Panel). Change L56,L57 from Bead to 0 ohm, P/N is 10-003400000. Page 31.
	04/09/30	8. Factory found that some Aluminum Electrolytic capacitor CE29, CE11, CE12 will fail at soldering process. Change them to OxiCap. Page 12,34.
	04/10/01	9. Factory found that some Aluminum Electrolytic capacitor CE30, CE31 will fail at soldering process. Change them to OxiCap. Page 31.
	04/10/06	10. Measurement team tested SMB waveform fail, fail item : Data & Clock will issue Glitch at falling edge. Add C541, C542, C543, C544, C539, C540, C545, C546 with 100pF to fine-tune SMBUS signal quality. Page 5,10,15,18.
	04/10/01	11. +V3.3A will issue leakage current to +V3.3SUS by CON1 pin 8,14 and L31, R343. Change R343 to diode D55. Page 37.
	04/10/01	12. A3 series tested fail at ESD function. To improve ESD function. Change 4pin Switch to 5pin switch. Add a GND pin. Page 36,37
	04/10/05	13. For the request from power team Adams, change R199 from 0603 to 0805 package. Page 43.
	04/10/05	14. For EMI engineer request, add R412, R413, R414 for test. Page 31.
	04/10/12	15. The position pin of CON9 & CN7 are base on 1.2mm PCB design, but A3& A6 PCB is 1.6mm. Modify the length of position pin of these connector. Page 13,28.
	04/10/12	16. For cost down , add 06-045021010 AUDIO AMP. TPA0102 (power is 1.5W)as first source and change original part (power is 2W) as second source. Page 31.
	04/10/12	17. For power team request. Change Q2 from UMZ1N(Not easy buy it) to BC847BPN. Page 45.
	04/10/14	18. +V5A will issue leakage current to +V3.3SUS by U48.4 --> D45 --> RN76B when plug in Battery module only. Change C108 from 0.1uF to 1K ohm (10-004401020). Page 19.

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