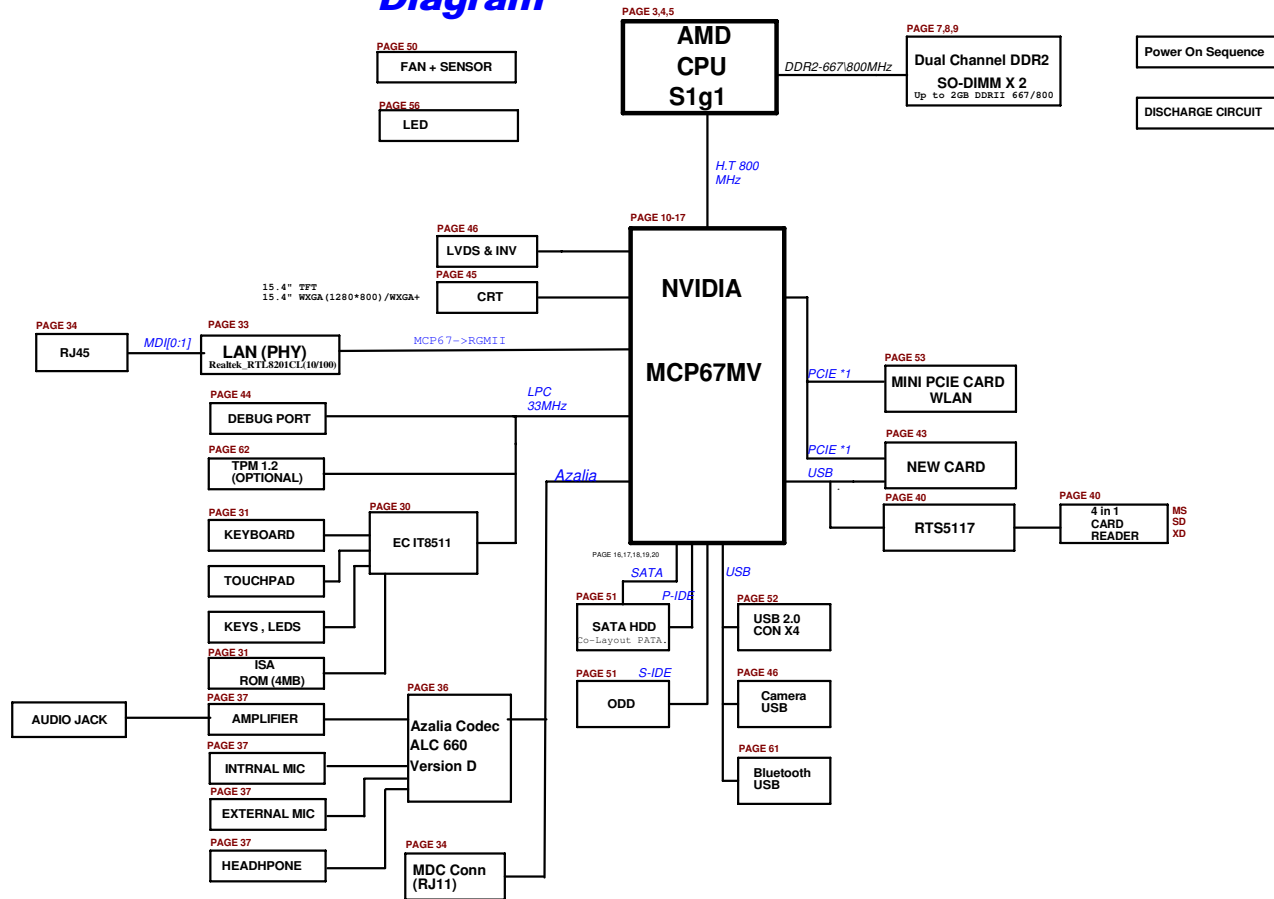

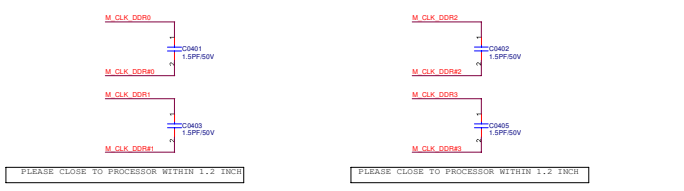
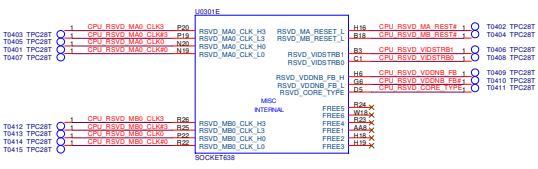
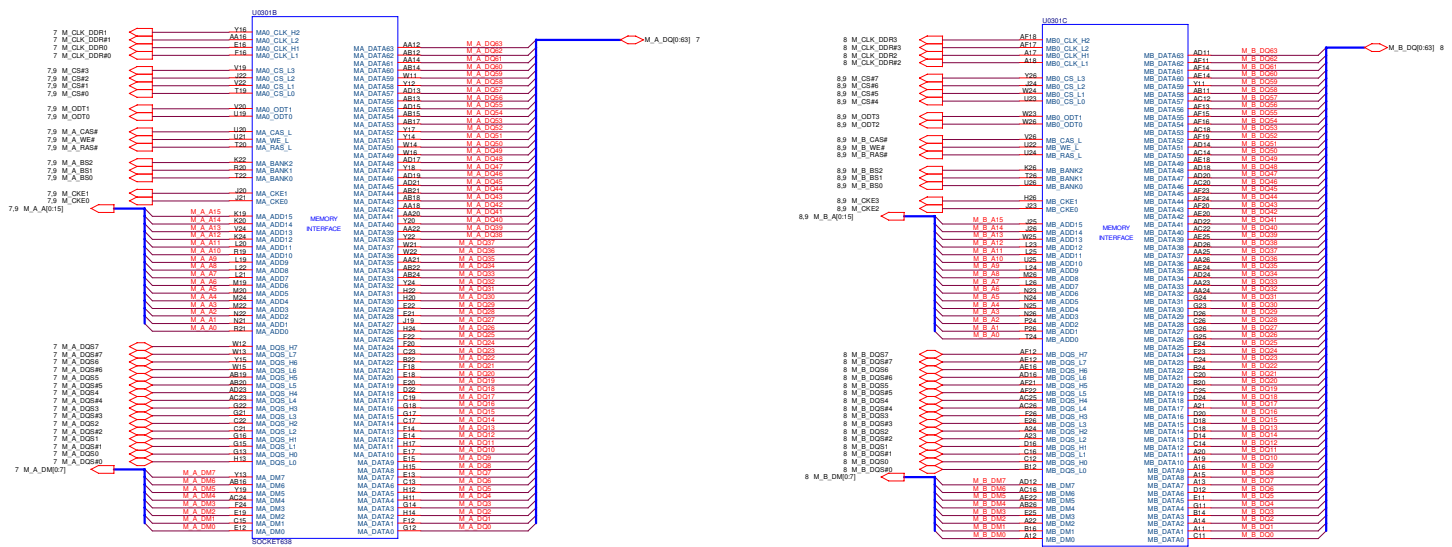


F5N Block Diagram



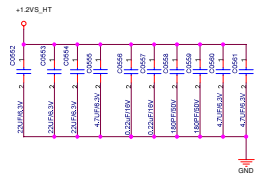
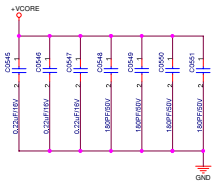
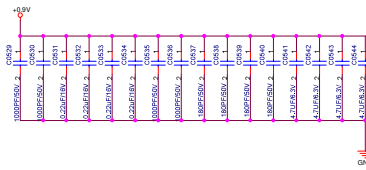
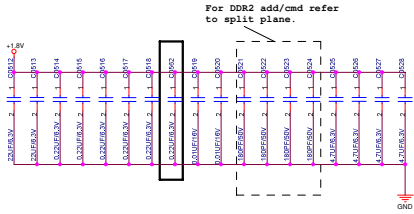
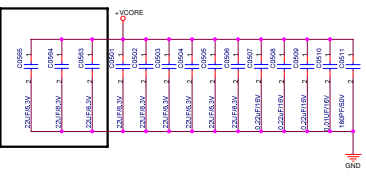
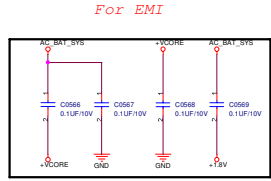
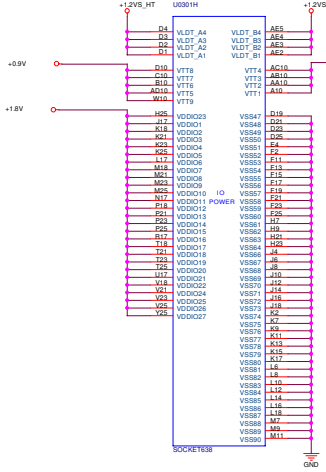
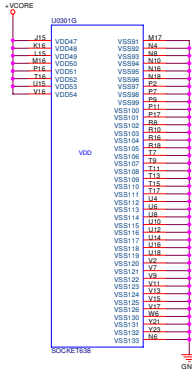
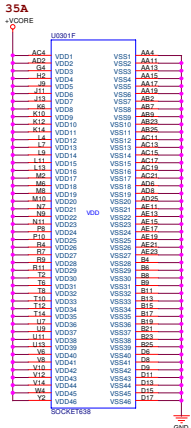
ASUS		Title : FSU	
ASUSTek Computer Inc. Engineer: He Wang			
Rev	Project Name	Rev	
1.0	FSU	1.0	
Date: 2008-05-29 10:00	Sheet: 1 of 26		

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-11-28 2011			




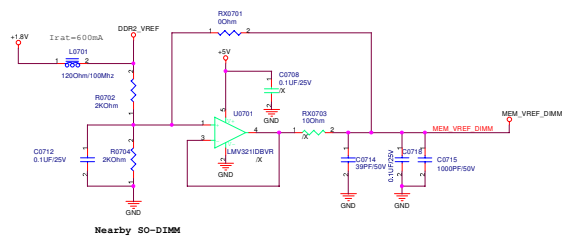
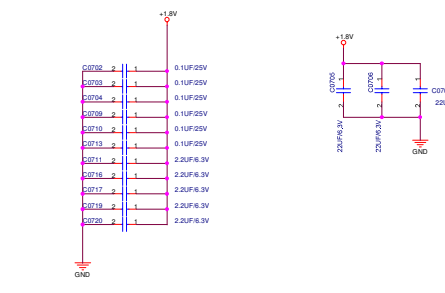
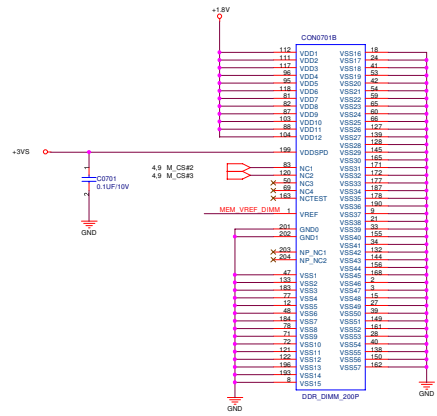
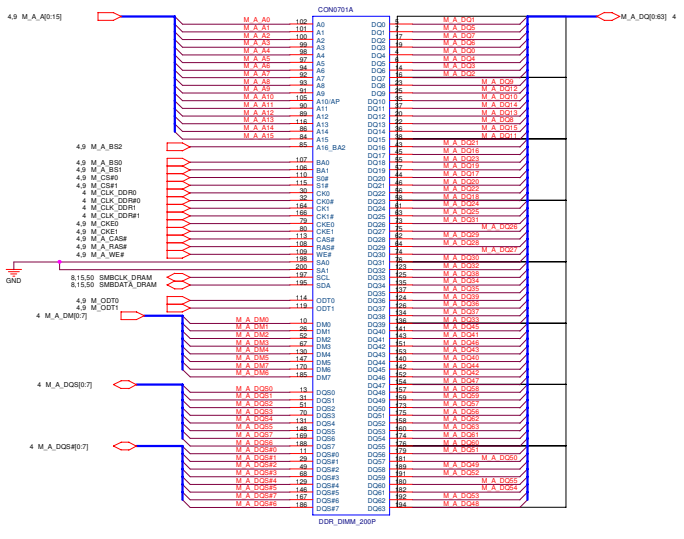
PLEASE CLOSE TO PROCESSOR WITHIN 1.2 INCH

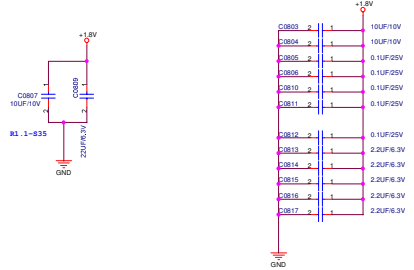
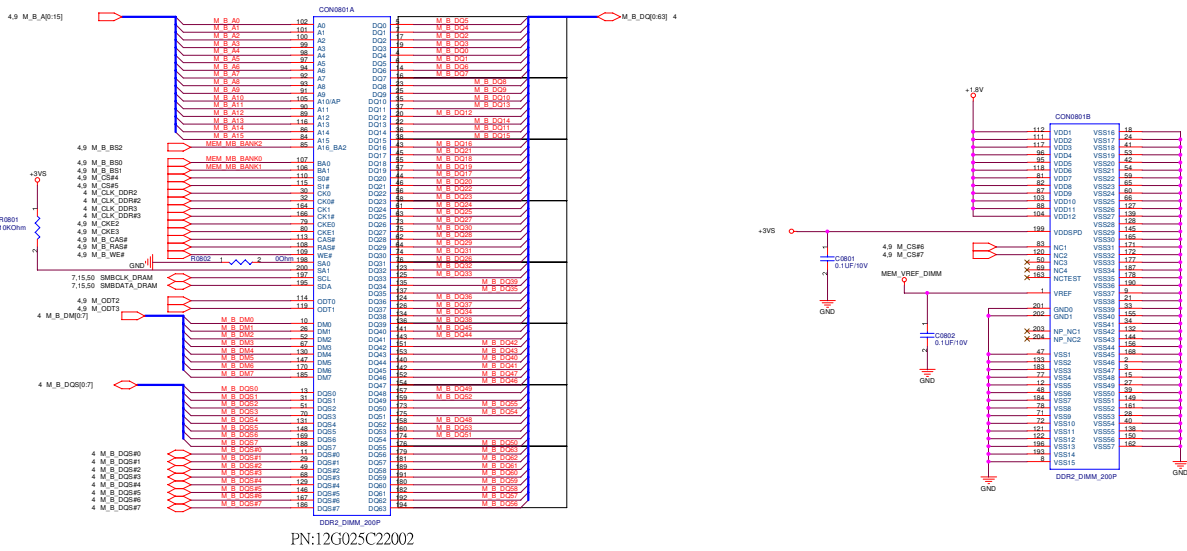
ASUS		Title: FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
B528	Project Name	Rev	1.0
C	FSU		
Date: 08-10-2007	Sheet: 4	of	8



For DDR2 add/cmd refer to split plane.

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-09-29 10:07	Sheet: 6		of 26

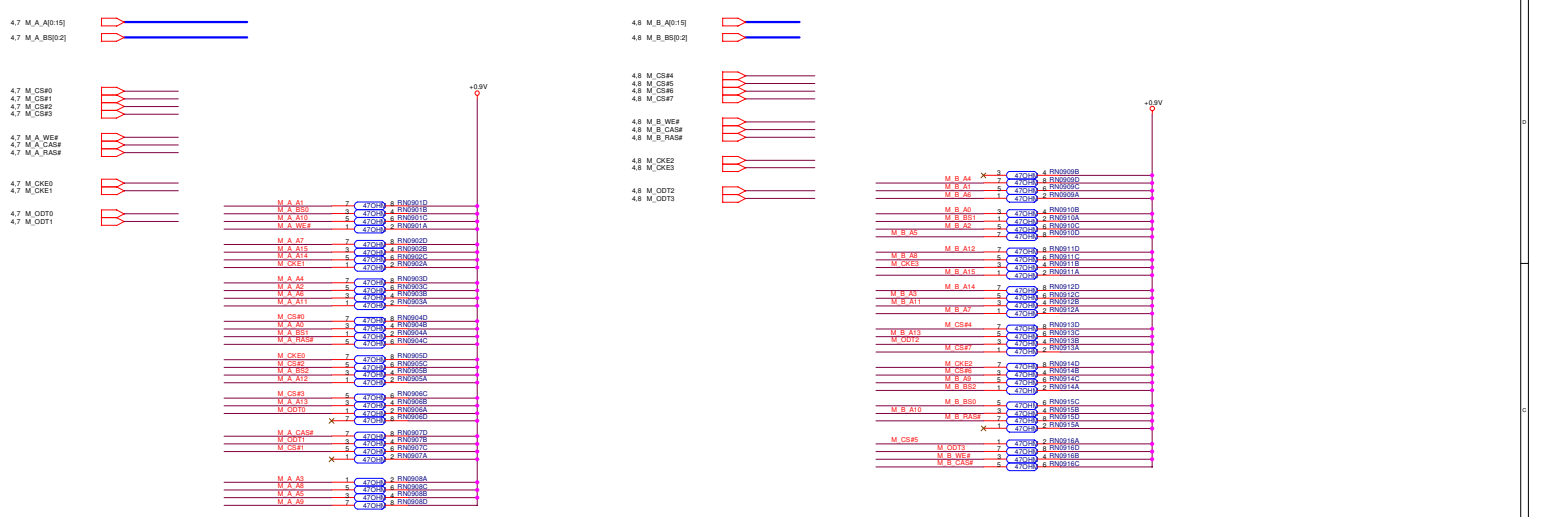




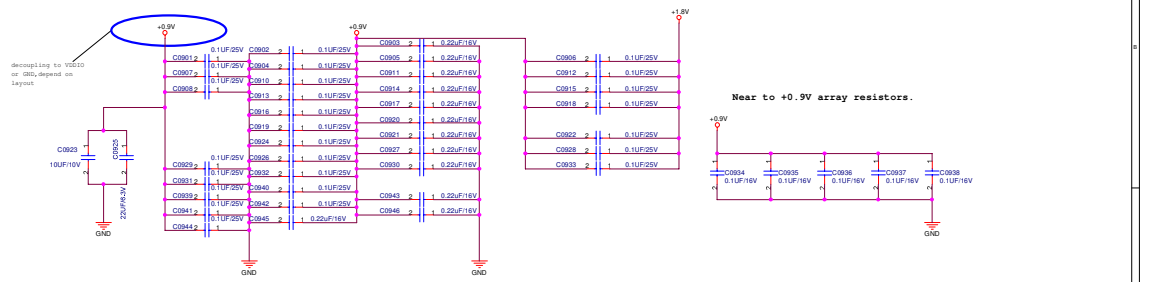
ASUS Title : FSU
ASUSTek Computer Inc. Engineer: He Wang

Rev	Project Name	Rev
C	FSU	1.0

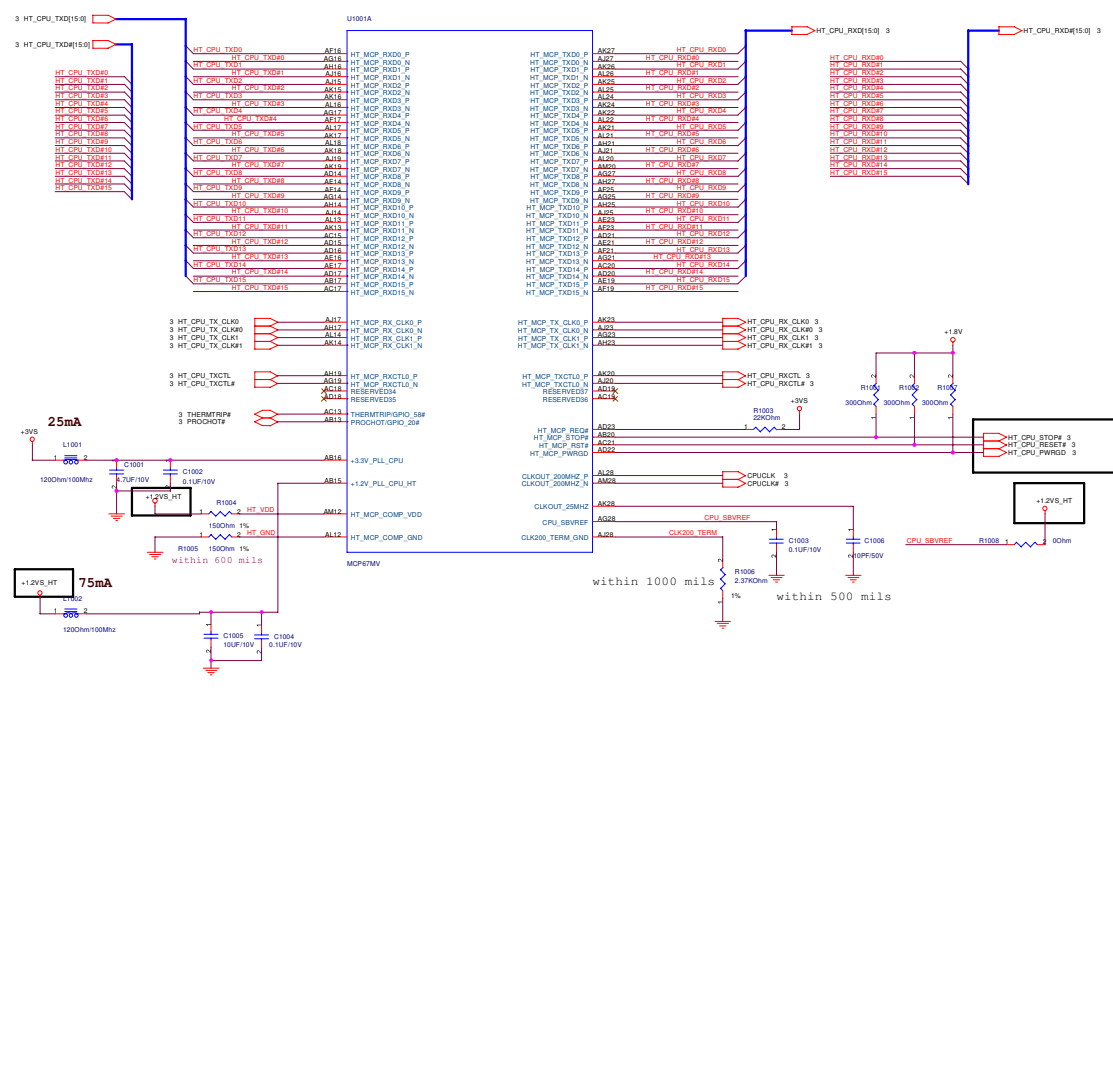
Date: 08-10-2007 Sheet: 6 of 10

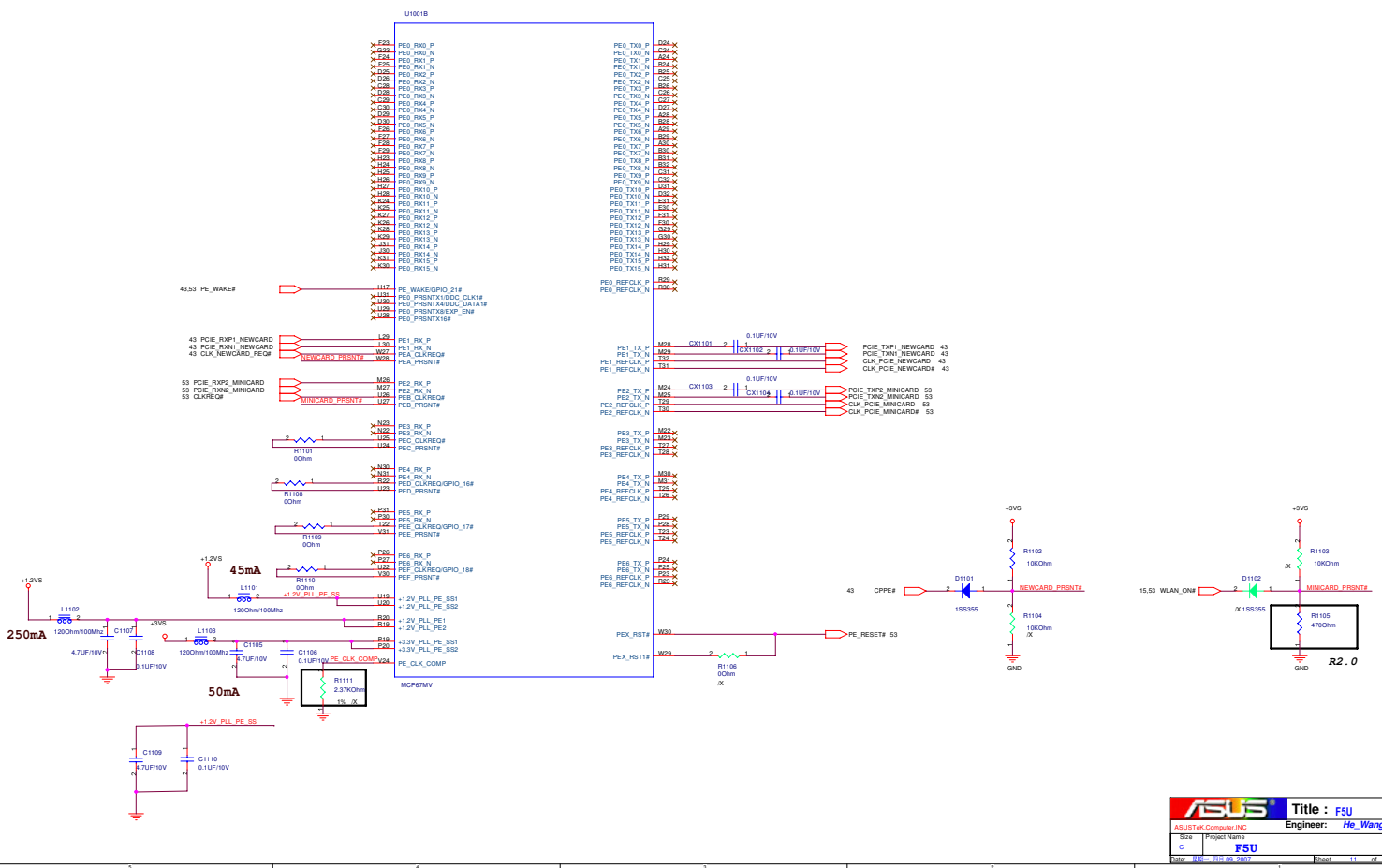


Layout Note: Place one cap close to every 2 pullup resistors terminated to +0.9V

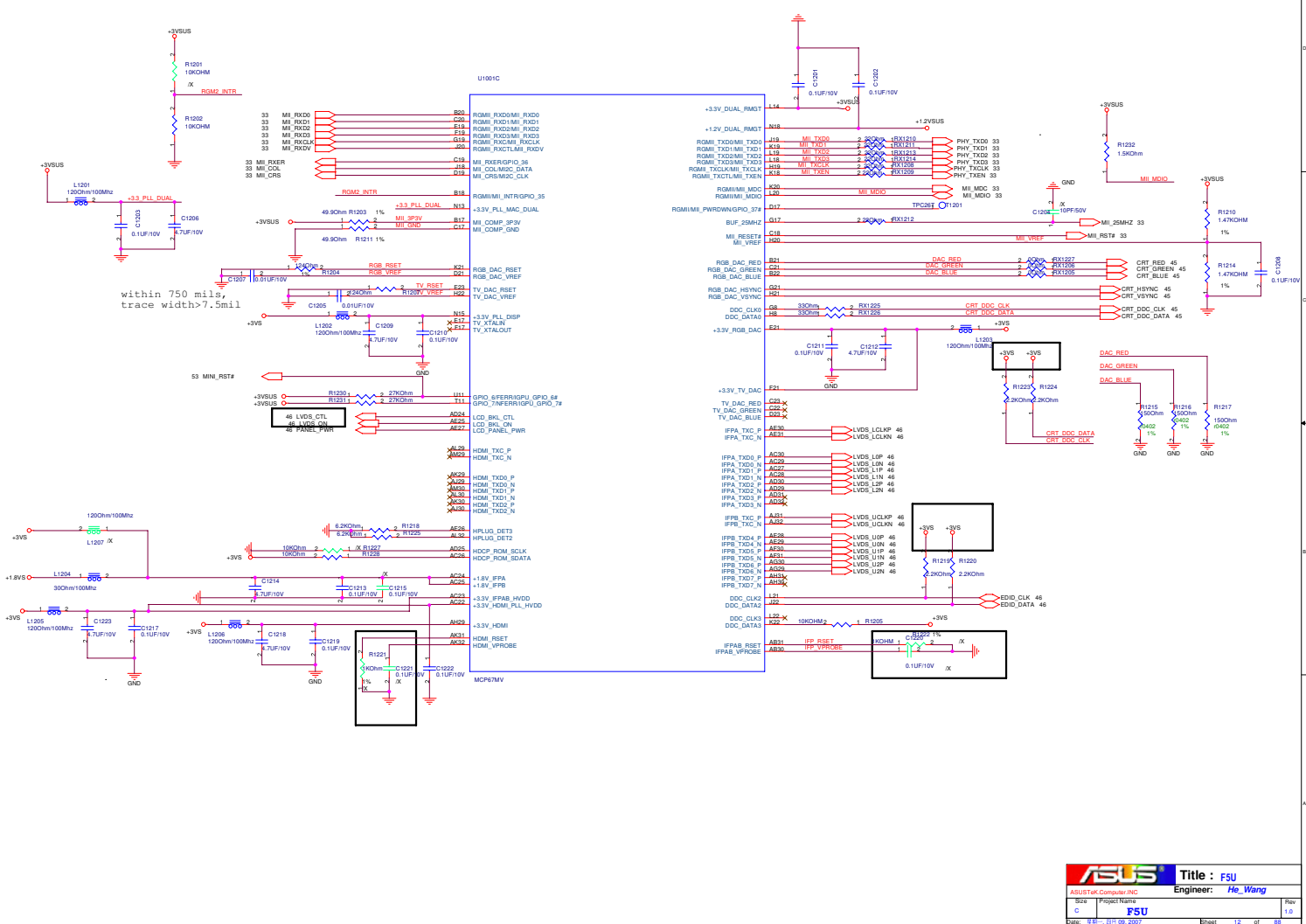


ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
BSZ	Project Name	Rev	1.0
C	FSU		
Date: 2011-08-25 10:07	Sheet: 8	of	88

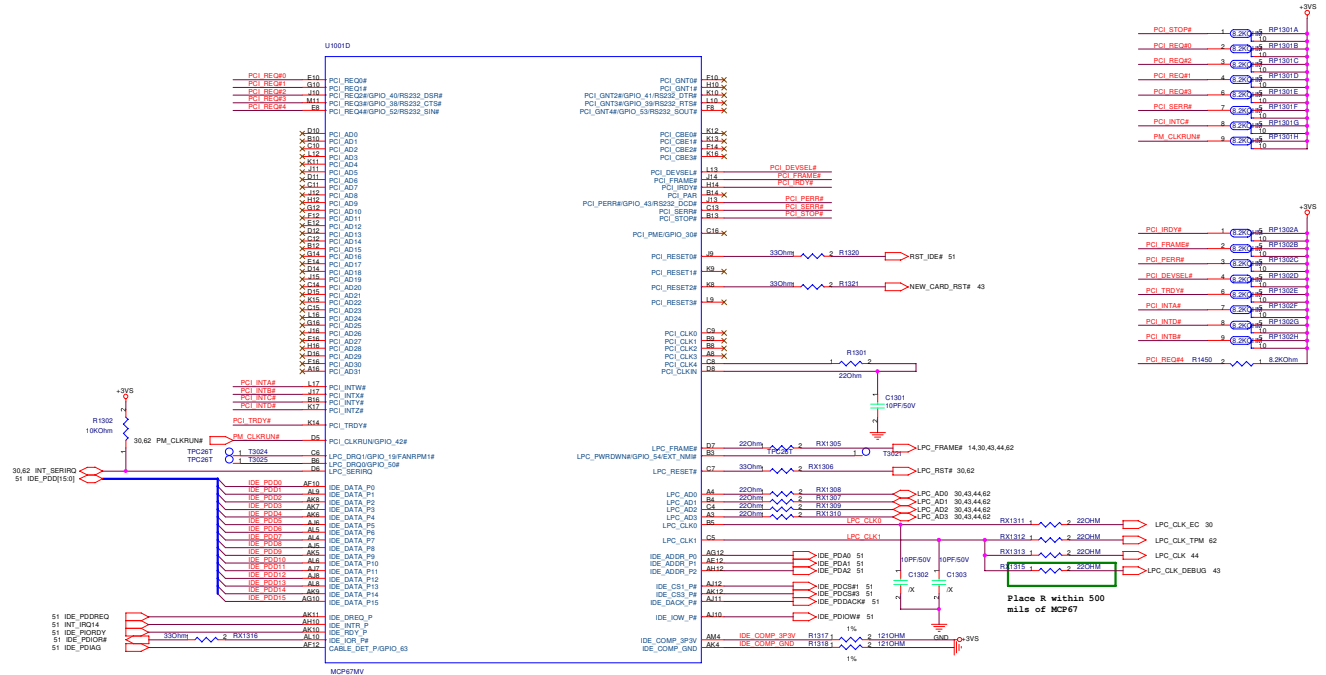




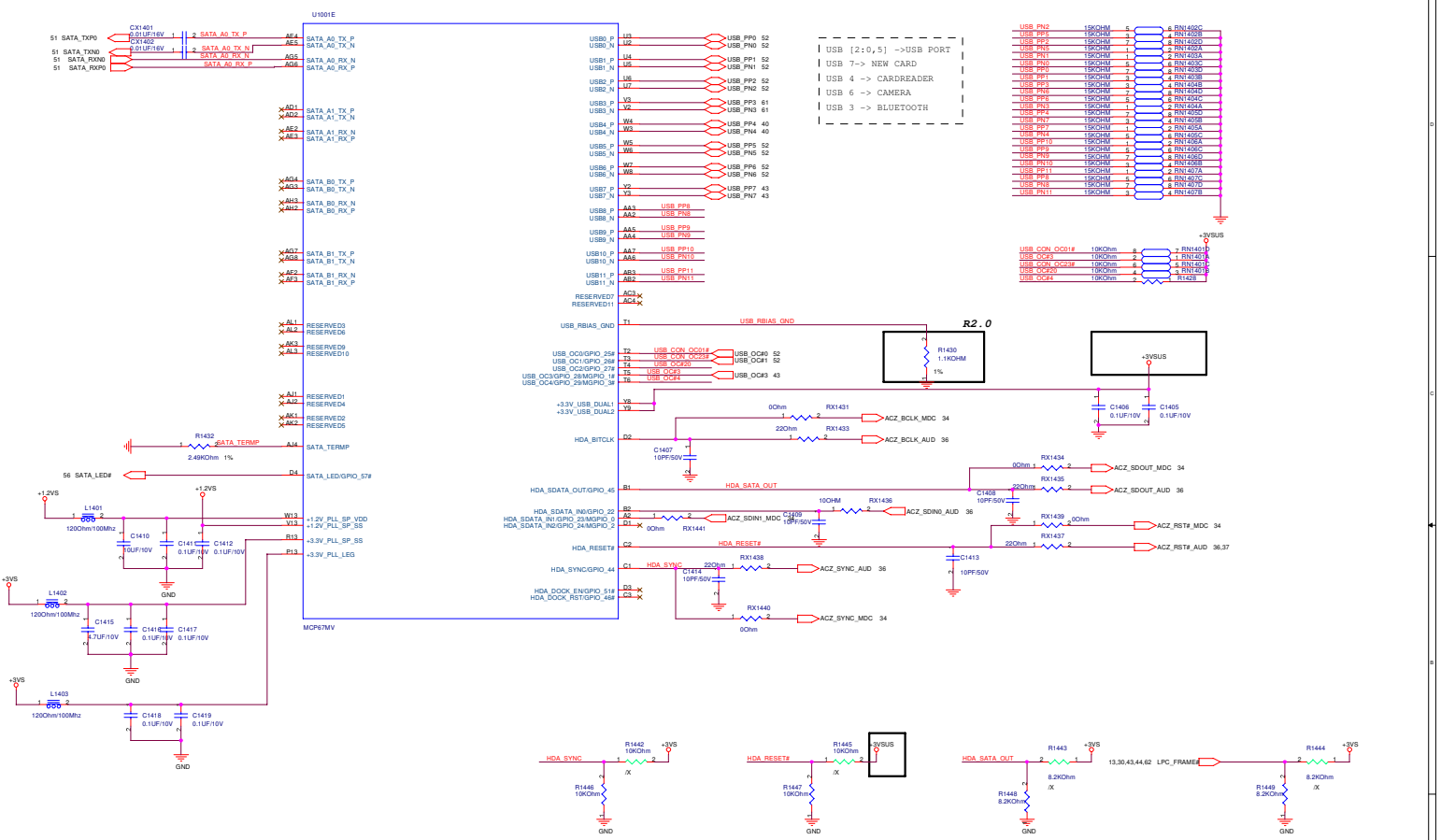
ASUS		Title : FSU	
ASUSTek Computer INC		Engineer: He Wang	
B24	Project Name		Rev
C	FSU		1.0
Date: 2007-09-25 2:07	Sheet: 11	of	26



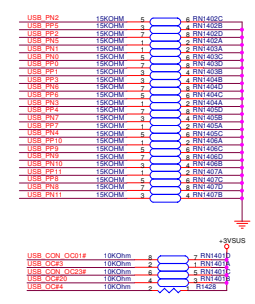
		Title : FSU	
		ASUSTek Computer Inc. Engineer: He Wang	
Rev	Project Name		Rev
1	FSU		1.0
Date: 08-01-2007		Sheet: 15	of 26



ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
B24	Project Name		Rev
C	FSU		1.0
Date: 2011-01-20 10:00	Sheet: 13	of	20



| USB [2:0,5] -> USB PORT
 | USB 7 -> NEW CARD
 | USB 4 -> CARDREADER
 | USB 6 -> CAMERA
 | USB 3 -> BLUETOOTH

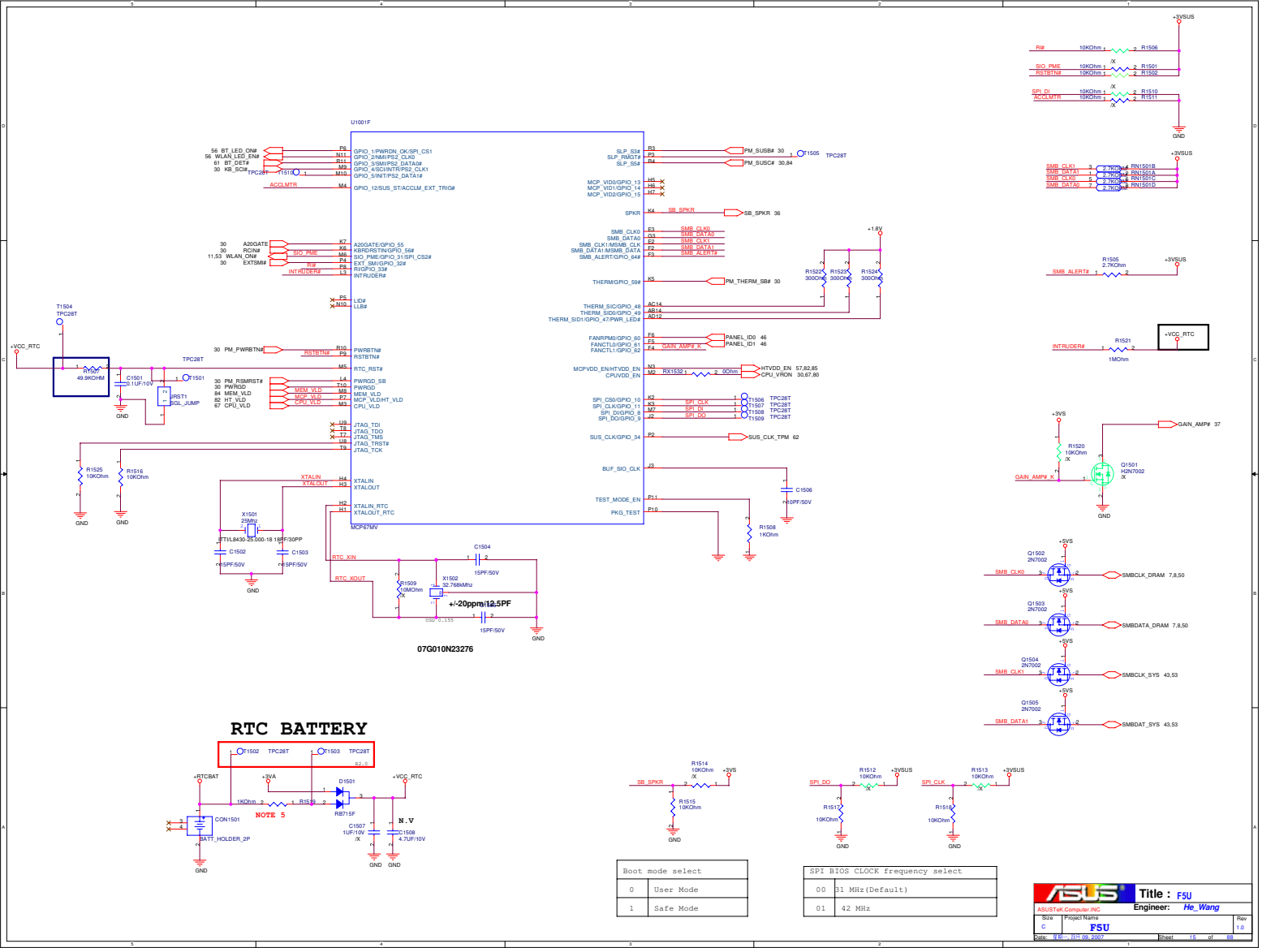


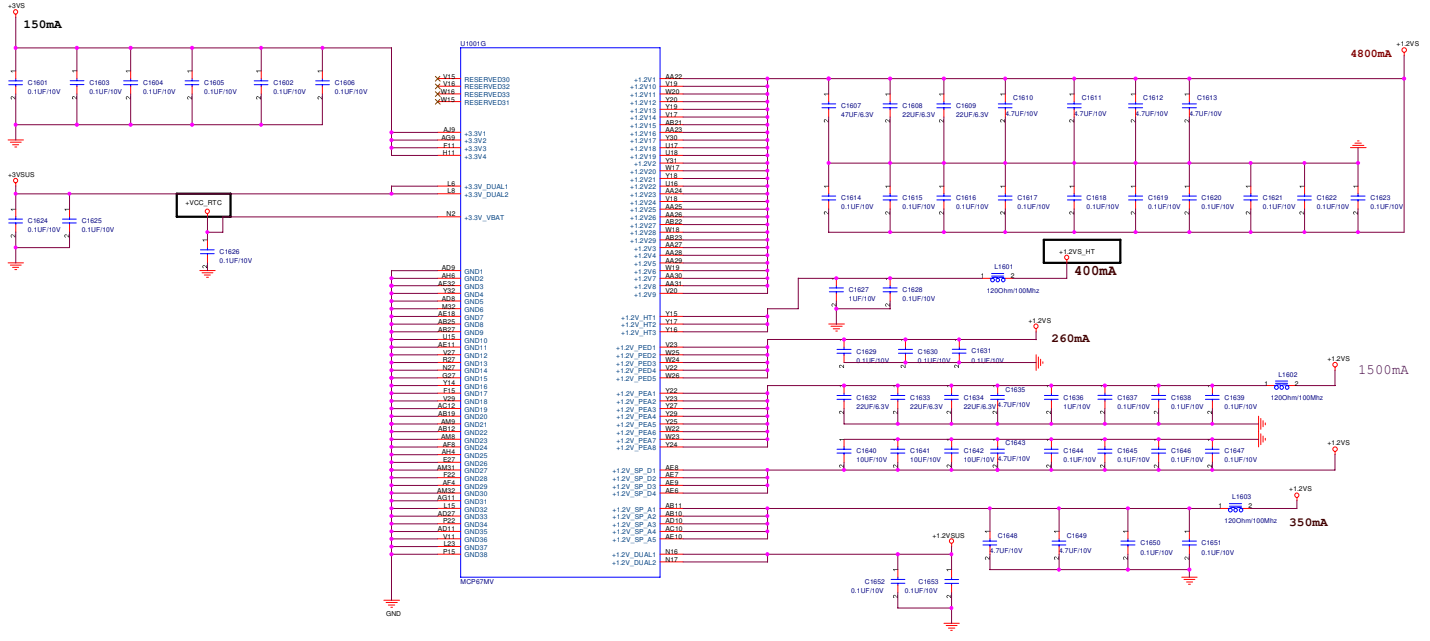
SIO CLOCK select	
0	14.31818 MHz (Default)
1	24 MHz


Networking select	
0	MII
1	RGMI

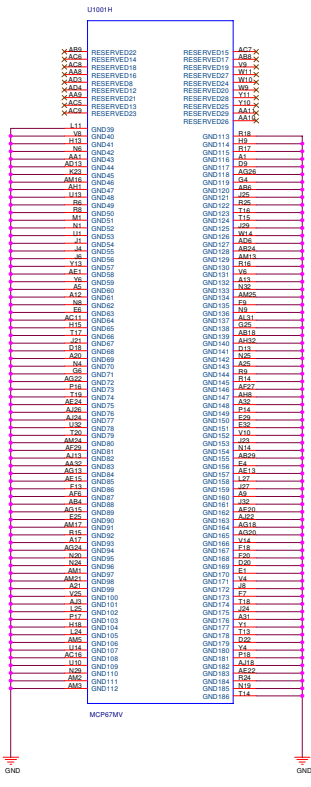
BIOS Select	
00	LPC BIOS
01	PCI BIOS

ASUS Title : FSU
 ASUSTek Computer INC Engineer: He Wang
 Rev: C Project Name: FSU Rev: 1.0
 Date: 2011-09-20 09:00:00 Sheet: 14 of 26







		Title : FSU
<small>ASUS is a registered trademark of ASUSTek Computer Inc.</small>		
BSN	Project Name	Engineer: He Wang
C	FSU	Rev 1.0
<small>Date: 2007-09-25 15:57</small>	<small>Sheet: 16</small>	<small>of 20</small>





RESERVED200	RESERVED15	ACT-V
RESERVED14	RESERVED17	ABR-K
RESERVED16	RESERVED18	WBR-K
RESERVED7	RESERVED27	WLR-K
RESERVED28	RESERVED24	WBR-K
RESERVED12	RESERVED20	WLR-K
RESERVED21	RESERVED28	LTR-K
RESERVED13	RESERVED25	AAK-K
RESERVED23	RESERVED29	AAK-K
RESERVED28	RESERVED28	AAK-K
L11	GND39	R18
GND39	GND40	R9
GND40	GND41	R17
GND41	GND42	A1
GND42	GND43	Y5
GND43	GND44	AG28
GND44	GND45	Y8
GND45	GND46	AB6
GND46	GND47	Y9
GND47	GND48	GND120
GND48	GND49	B26
GND49	GND50	GND122
GND50	GND51	T16
GND51	GND52	Y29
GND52	GND53	GND124
GND53	GND54	W14
GND54	GND55	AB6
GND55	GND56	AB24
GND56	GND57	R13
GND57	GND58	V8
GND58	GND59	A1
GND59	GND60	N32
GND60	GND61	AN2C
GND61	GND62	E9
GND62	GND63	V8
GND63	GND64	AI31
GND64	GND65	Y5
GND65	GND66	GND138
GND66	GND67	Y5
GND67	GND68	AG18
GND68	GND69	AN2C
GND69	GND70	GND141
GND70	GND71	N5
GND71	GND72	GND143
GND72	GND73	AN2C
GND73	GND74	R14
GND74	GND75	AG27
GND75	GND76	AS8
GND76	GND77	GND146
GND77	GND78	P14
GND78	GND79	E8
GND79	GND80	V10
GND80	GND81	Y8
GND81	GND82	N14
GND82	GND83	AN2C
GND83	GND84	E4
GND84	GND85	AG1A
GND85	GND86	L27
GND86	GND87	Y5
GND87	GND88	AG
GND88	GND89	Y5
GND89	GND90	AG20
GND90	GND91	AG18
GND91	GND92	AG20
GND92	GND93	GND163
GND93	GND94	GND164
GND94	GND95	GND165
GND95	GND96	GND166
GND96	GND97	GND167
GND97	GND98	GND168
GND98	GND99	GND169
GND99	GND100	GND170
GND100	GND101	Y8
GND101	GND102	Y7
GND102	GND103	T16
GND103	GND104	Y8
GND104	GND105	GND178
GND105	GND106	T16
GND106	GND107	D28
GND107	GND108	Y8
GND108	GND109	AI18
GND109	GND110	AE22
GND110	GND111	R8
GND111	GND112	N19
GND112	GND113	T14
GND113	GND114	GND188


		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2007-05-25 10:07	Sheet: 17	of	28


		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 18	of	28


		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-05-25 10:07	Sheet: 18	of	28


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 25	of 25


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 21 of 28	


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 25 of 25	


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-11-28 2007		Sheet: 23 of 28	


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 24 of 28	

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 25 of 25	

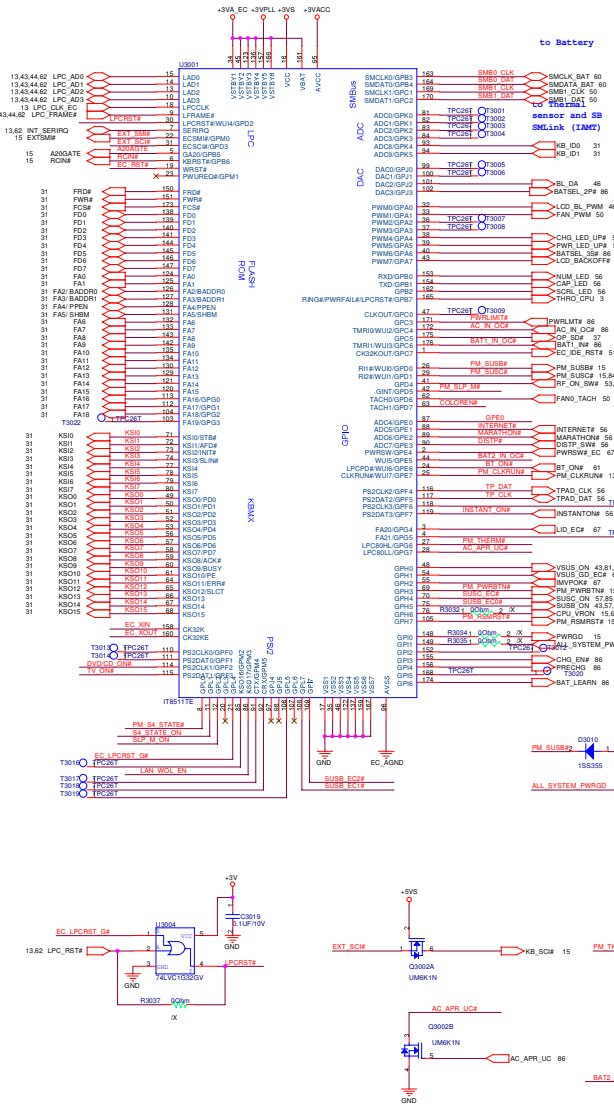
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ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 25	of 25

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-11-28 2007		Sheet: 21 of 28	

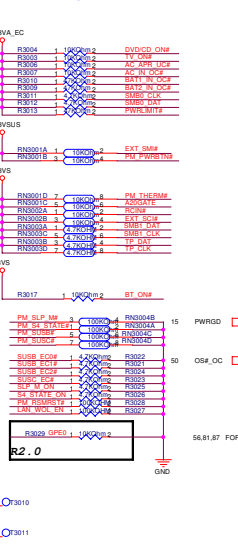
		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 25 of 25	

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 25	of 25

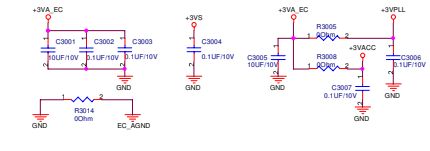
For IT8511 Core IC



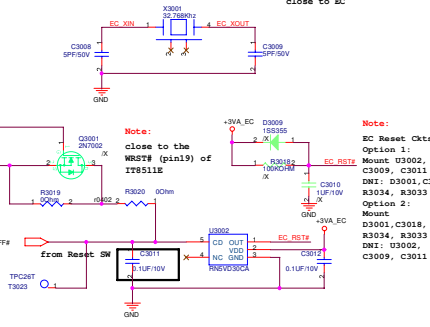
For Pull-up/Pull-down



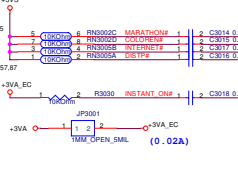
For IT8511 Power



For Xtal



For Instant Key

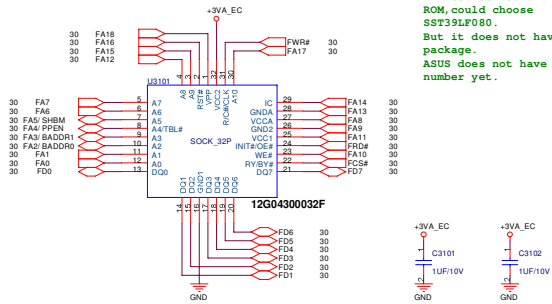


Note:
EC Reset Ckts:
Option 1:
Mount U3002,
C3009, C3011
DNE1: U3001, C3018,
R3014, R3033
Option 2:
Mount
D3001, C3018,
R3014, R3033
DNE1: U3002,
C3009, C3011

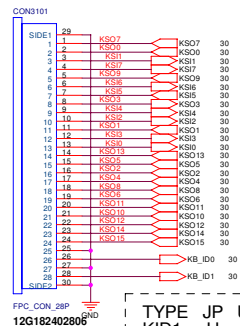
ASUS		Title: FSU	
ASUSTek Computer, Inc.		Engineer: He Wang	
Doc No:	Project Name:	Rev:	
Doc No:	FSU	Rev:	1.0
Date: 8/8	10/26/2007	Sheet:	30 of 38

ISA ROM (4Mbits)

SST-PLCC32 4Mbits Flash ROM
 PN:05G001014110
 (FLASH SST SST39VF040-70-4C-NHE
 4M-70 PLCC-32)
 If need to use 8Mbits ISA ROM, could choose SST39LF080.
 But it does not have PLCC32 package.
 ASUS does not have part number yet.



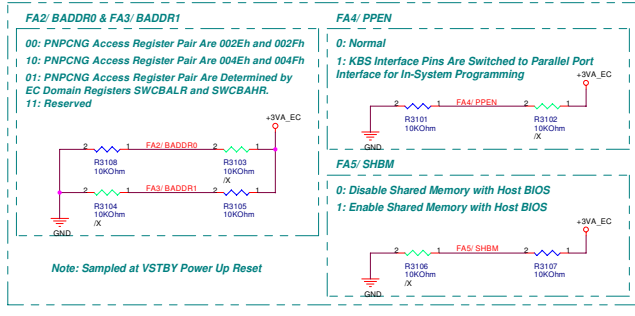
KBC connector




TYPE	JP	UK	US
KID1	H	H	L
KID2	L	H	L

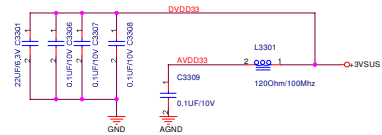
ISA ROM

EC Hardware Strapping

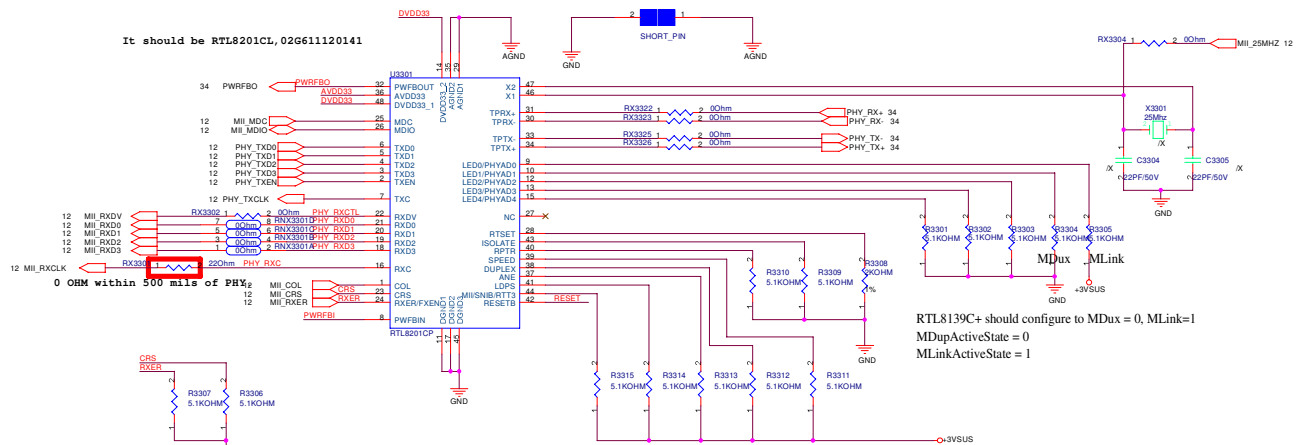


ASUS		Title : FSU	
ASUS Tek Computer INC		Engineer: He_Wang	
Size	Project Name	Rev	
Custom	FSU	1.0	
Date: 11/11/2007	Sheet	31	of 38

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-03-29 10:07		Sheet: 01	of 01

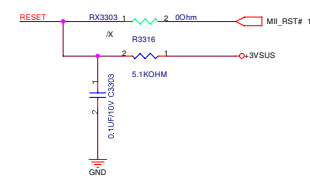
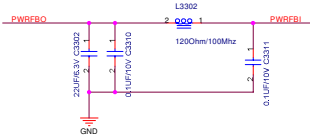


It should be RTL8201CL, 02G61120141

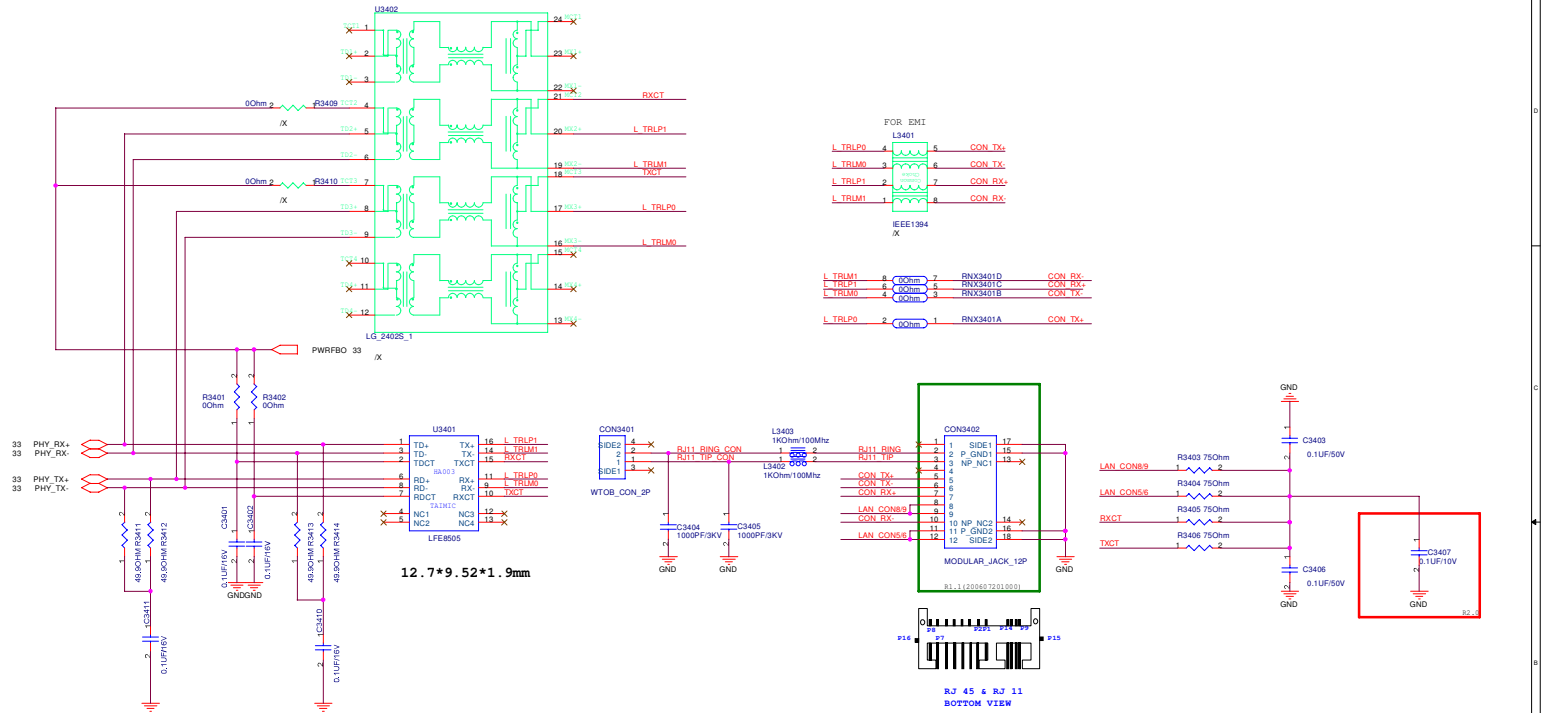


RTL8139C+ should configure to MDux = 0, MLink=1
 MDupActiveState = 0
 MLinkActiveState = 1

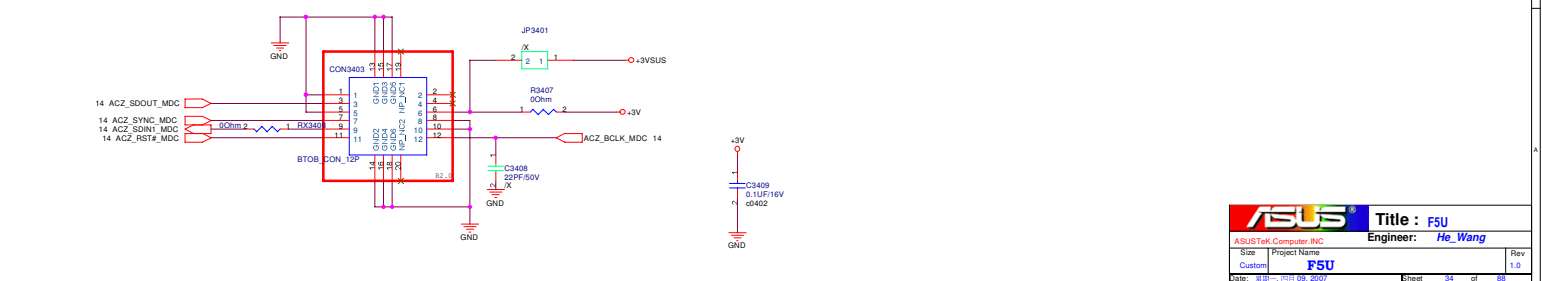
- ISOLATE: set high to isolate the RTL8201CP from the MAC, this will also isolate the MC/MDIO management interface
- RPTR: set high to put the RTL8201CP into repeater mode
- SPEED: this pin is latched to input during a power on or reset condition. set high to put the RTL8201CP into 100Mbps operation
- DUPLEX: Set high to enable full duplex
- ANE: Set high to enable auto-negotiation mode, set low to force mode
- LDPS: set high to put the RTL8201CP into LDPS mode
- MII/SNIB: pull high to set the RTL8201CP into MII mode operation. set low for SNI mode



LAN PORT



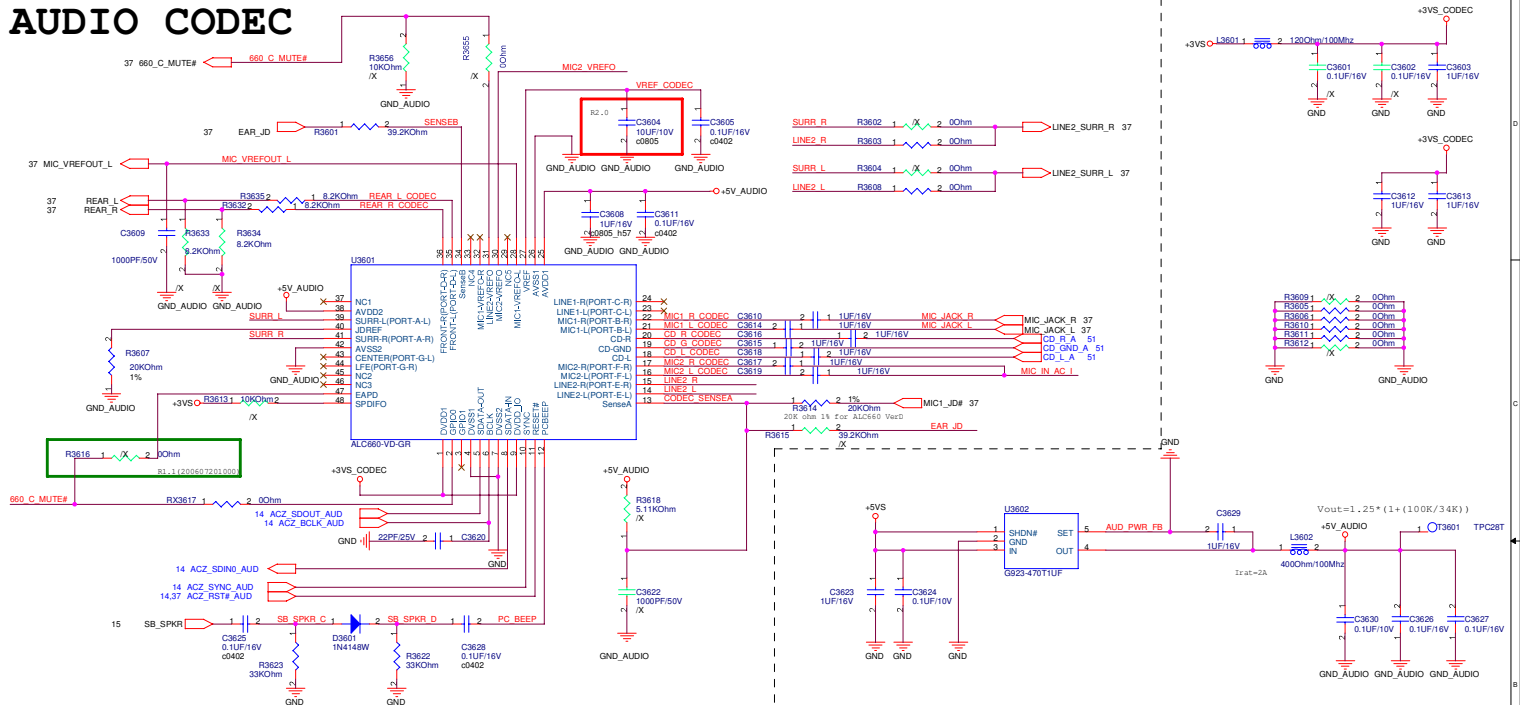
MDC CONN.



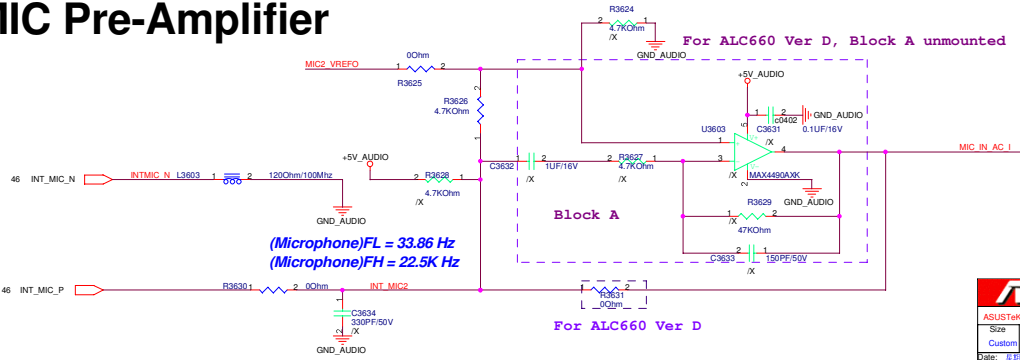
ASUS Title: FSU
 ASUSTek Computer, INC Engineer: He_Wang
 Size Project Name Rev
 Custom FSU 1.0
 Date: 2011.09.20 File: 34 of 38

		Title : FSU
ASUS Tek Computer INC		Engineer: He_Wang
Size	Project Name	Rev
Custom	FSU	1.0
Site: 010-11-28-2007		Sheet 05 of 08

AUDIO CODEC

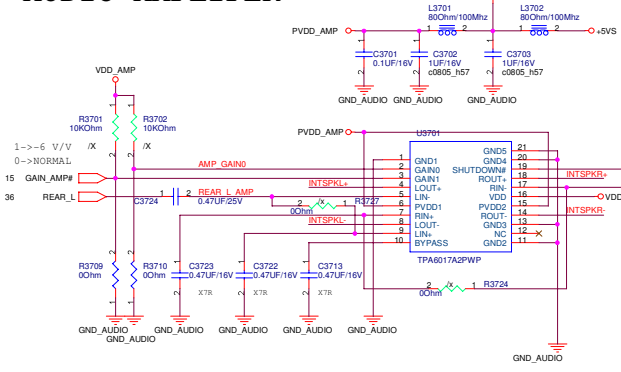


Internal MIC Pre-Amplifier

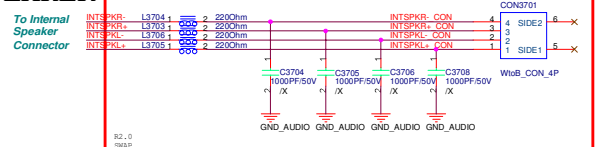


ASUS		Title : FSU	
ASUSTek Computer, Inc		Engineer: He_Wang	
Size	Project Name	Date	Rev
Custom	FSU	Date: 11/11/09 2007	1.0
Date: 11/11/09 2007		Sheet	36 of 38

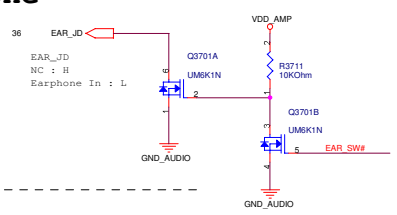
AUDIO AMPLIFIER



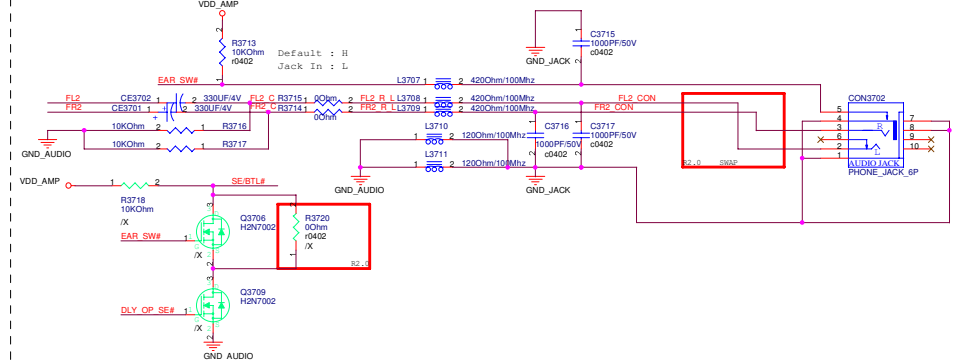
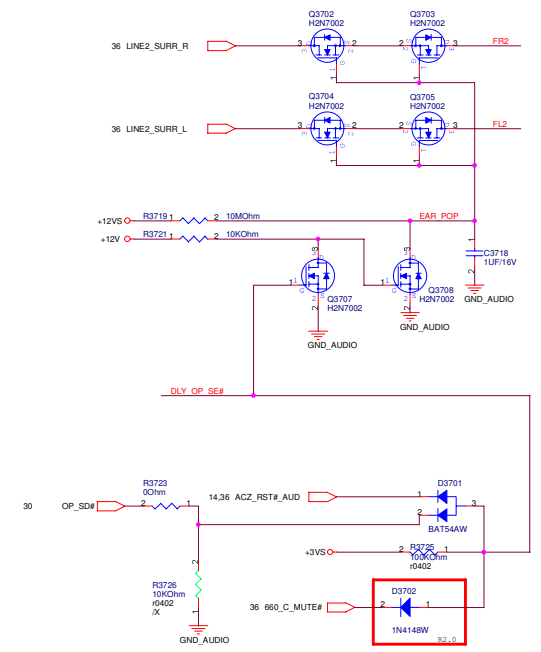
SPEAKER



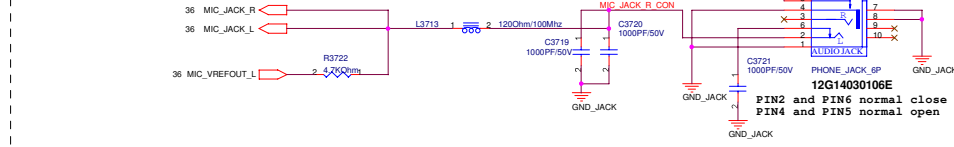
HeadPhone




DEPOP CIRCUIT




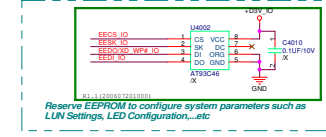
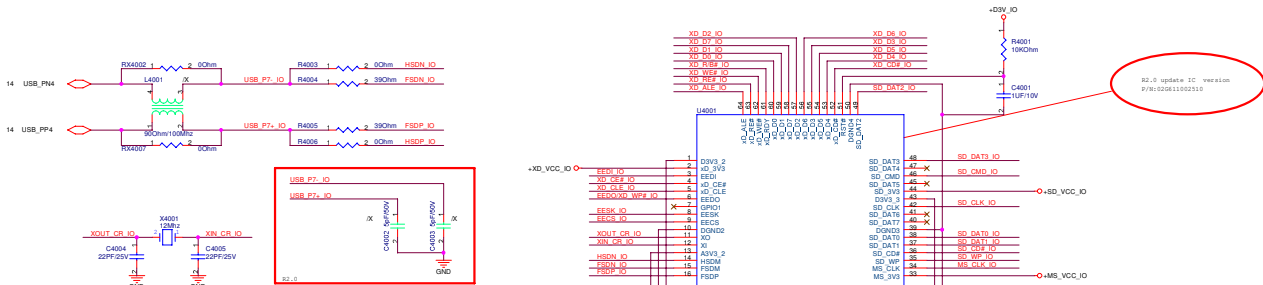
External Microphone



ASUS Title : FSU
 ASUSTek Computer, INC Engineer : He_Wang
 Size Project Name
 Custom FSU
 Date: 08/09/2007 Sheet 37 of 38

		Title : FSU	
ASUSTeK Computer INC		Engineer: He_Wang	
Size	Project Name		Rev
Custom	FSU		1.0
Date: 2007-11-28		Sheet	38 of 38

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 01	of	01



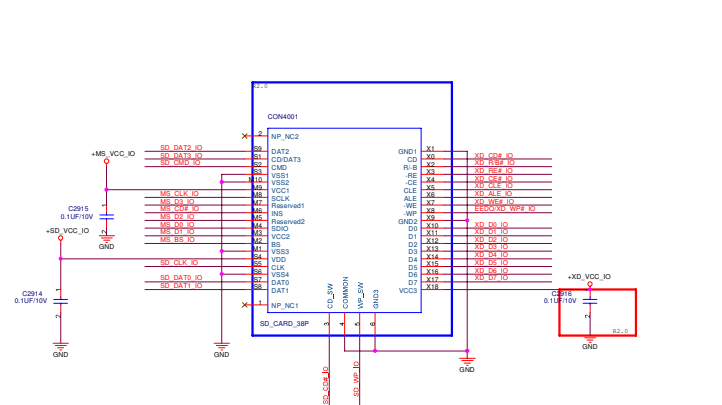
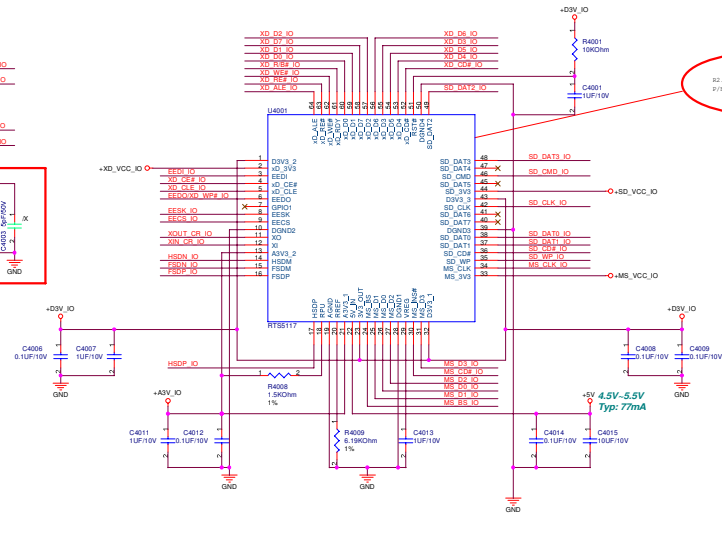
Reserve EEPROM to configure system parameters such as LUN Settings, LED Configuration...etc




	R2910	R2911
SD/MMC only	No Stuff	No Stuff
xD/SD/MMC/MS/MS-Pro Combo Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	No Stuff
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	4.7K

IO_R41 should be present if system doesn't use EEPROM to configure LED.


Through these pull-high resistors, EEPROM can be saved if no other requirement about other parameters.



SD update IC version P/N:0261102310

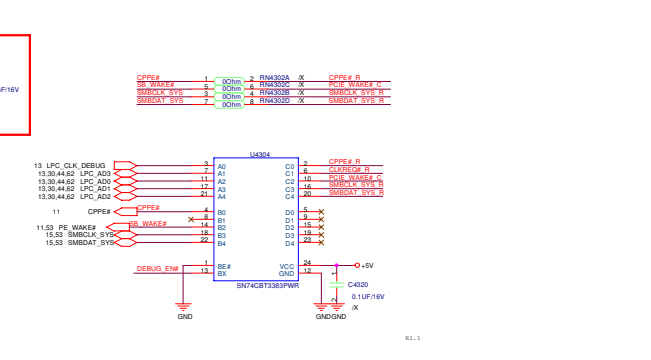
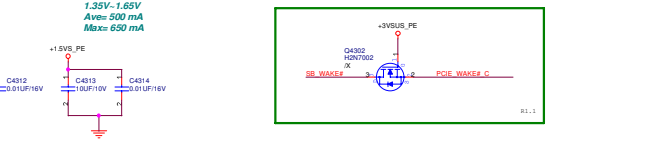
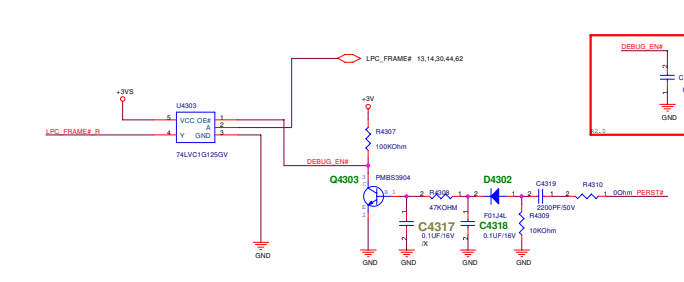
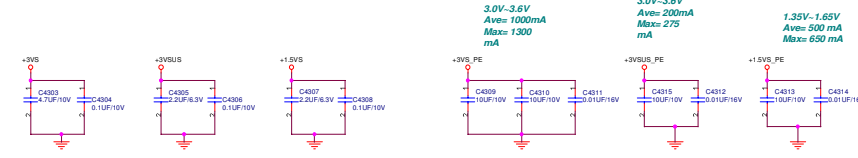
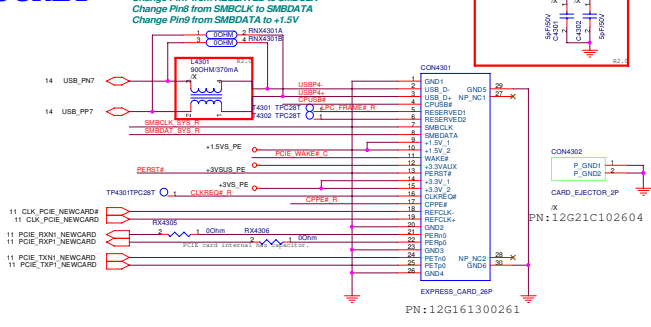
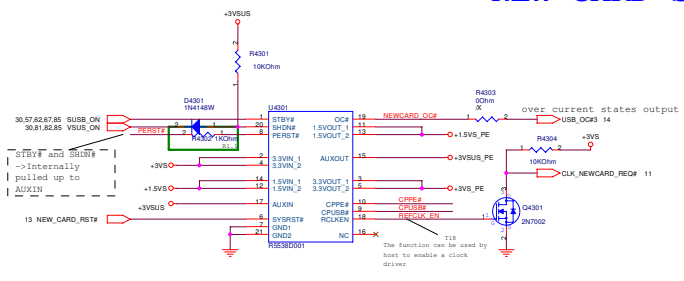
		Title : FSU
ASUSTeK Computer INC		Engineer: He_Wang
Size	Project Name	Rev
Custom	FSU	1.0
Date: 11/23/2007	Sheet	41 of 88



		Title : FSU	
<small>ASUSTeK Computer INC</small>		Engineer: He_Wang	
Size	Project Name		Rev
Custom	FSU		1.0
Date: 11/28/2007		Sheet	42 of 68

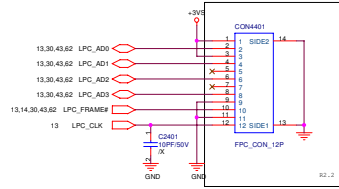
NEW CARD SOCKET

!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V



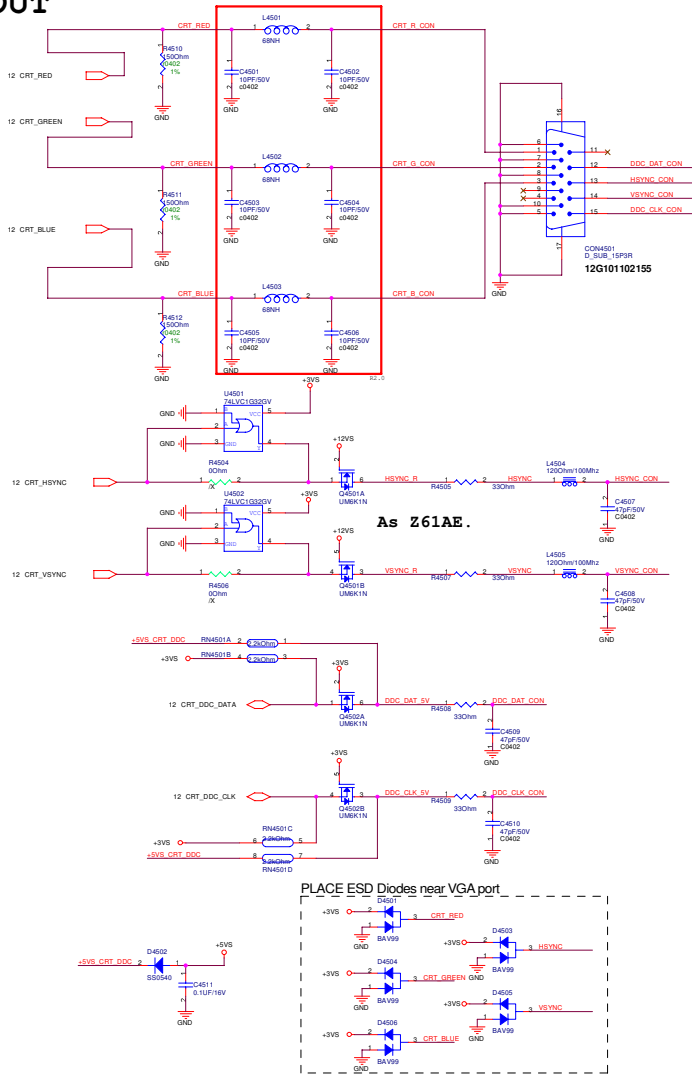
ASUS Title : FSU
 ASUSTek Consumer I/C Engineer: He Wang
 Rev: 1.0
 Date: 2010-09-23 09:20:00 Sheet: 41 of 48

LPC DEBUG CONNECTOR



		Title : FSU	
ASUSTeK Computer INC.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU		1.0
Date: 2011-01-26 10:07	Sheet: 44	of	88

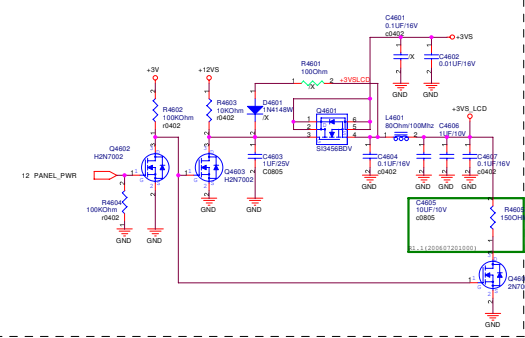
VGA OUT



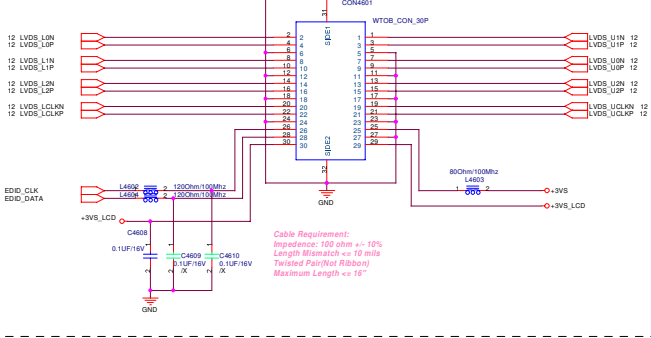
COM4501
D_SUB_15PFR
12G101102155

ASUS		Title : FSU	
ASUSTek Computer INC			
Project Name		Engineer: He Wang	
Rev	FSU	Rev	1.0
Date: 2007-08-29 10:07	Sheet: 45	of	48

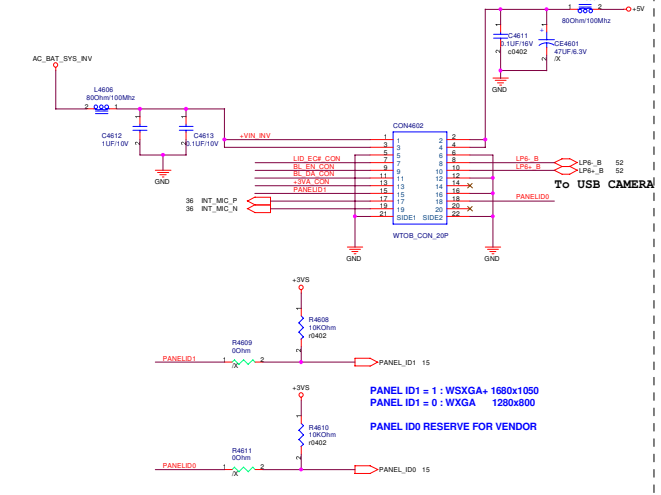
LCD Power



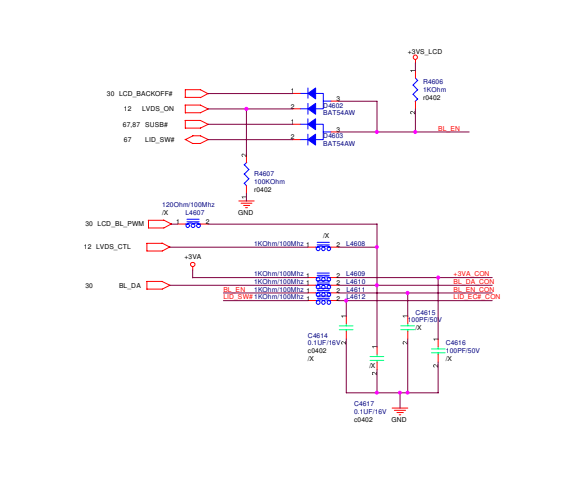
LCD LVDS Interface




INVERTER Interface





Backlight Enable



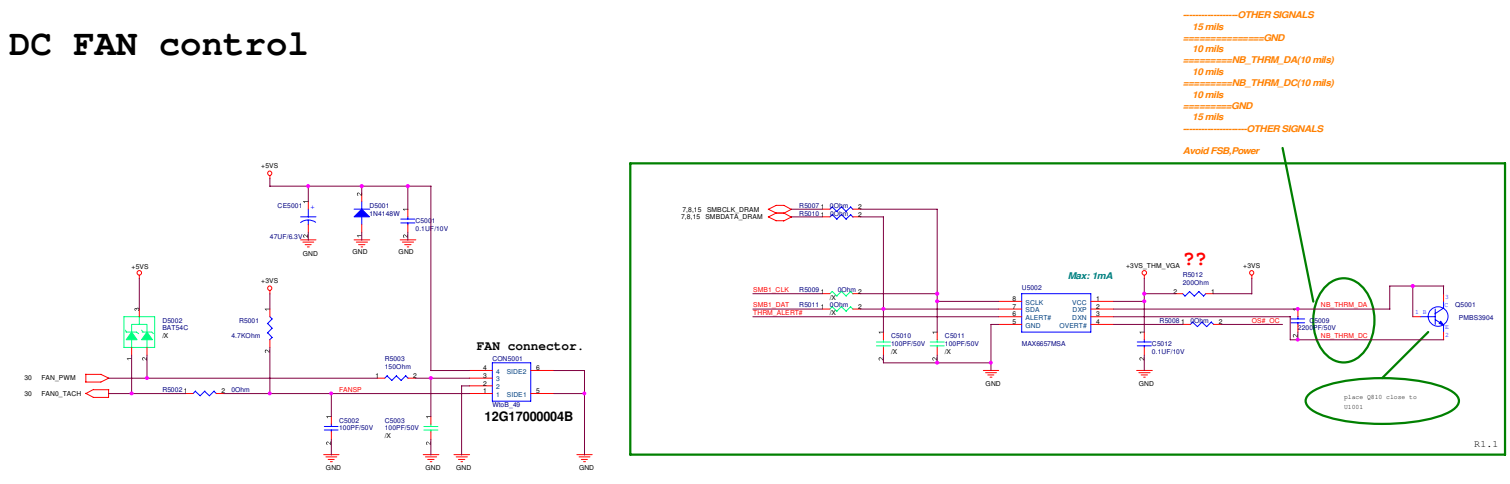
ASUS		Title : FSU	
ASUSTek Computer INC		Engineer: He Wang	
B24	Project Name		Rev
C	FSU		1.0
Date: 02-10-2007	Sheet: 45	of	49

		Title : FSU	
ASUSTeK Computer INC		Engineer: He_Wang	
Size	Project Name		Rev
Custom	FSU		1.0
Date: 11/28/2007		Sheet	47 of 88

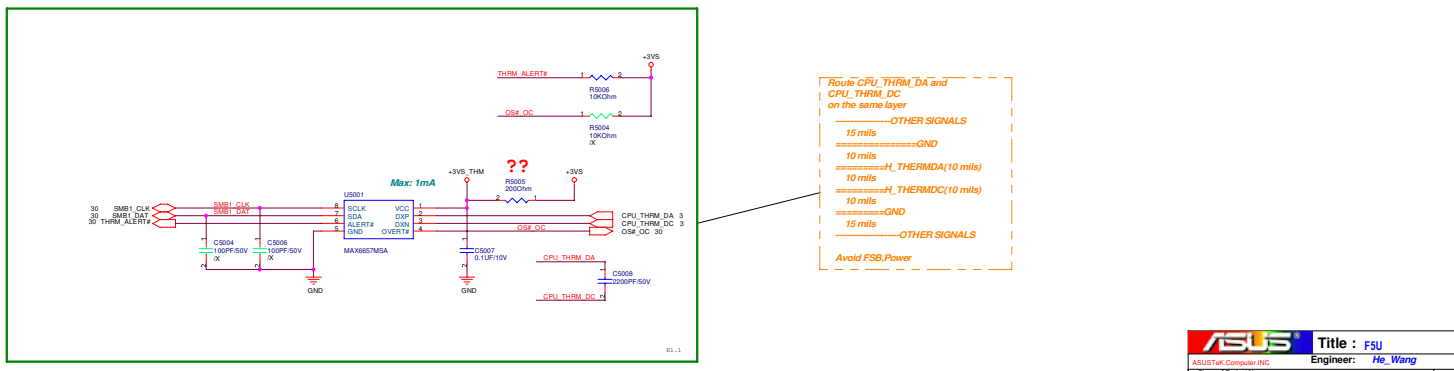
		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 48	of	50

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-03-25 10:07		Sheet: 41	of 48

DC FAN control

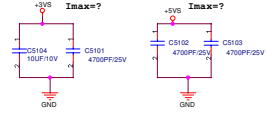
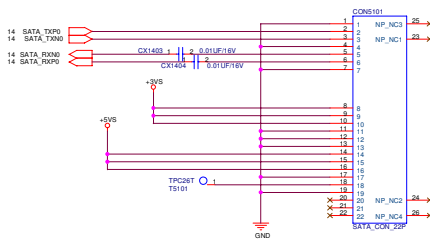


Thermal Sensor

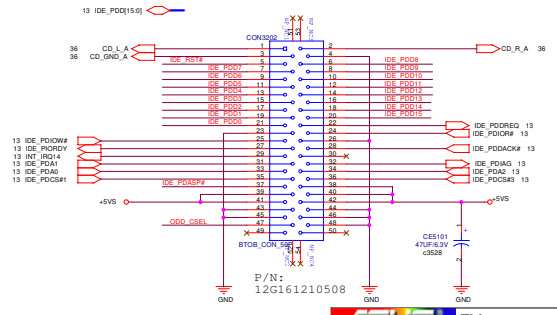
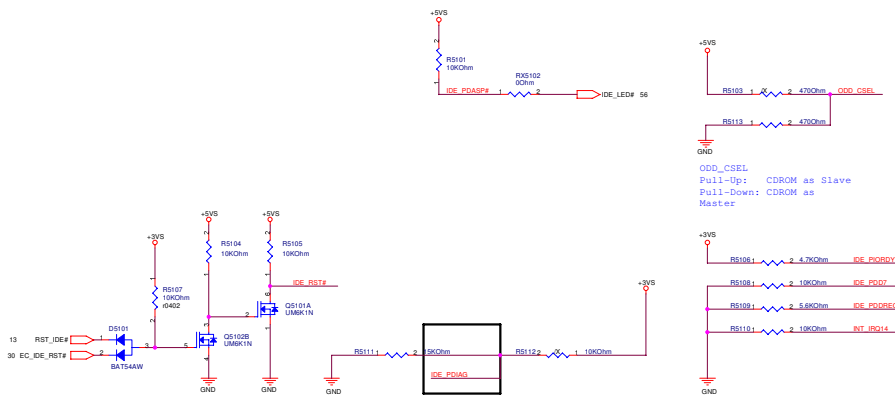


ASUS		Title : FSU	
ASUSTek Computer Inc.	Project Name	Engineer: He Wang	Rev
CS	FSU		1.0
CS	11/19/2017	Sheet	30 of 38

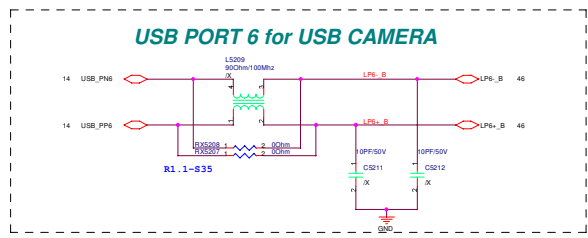
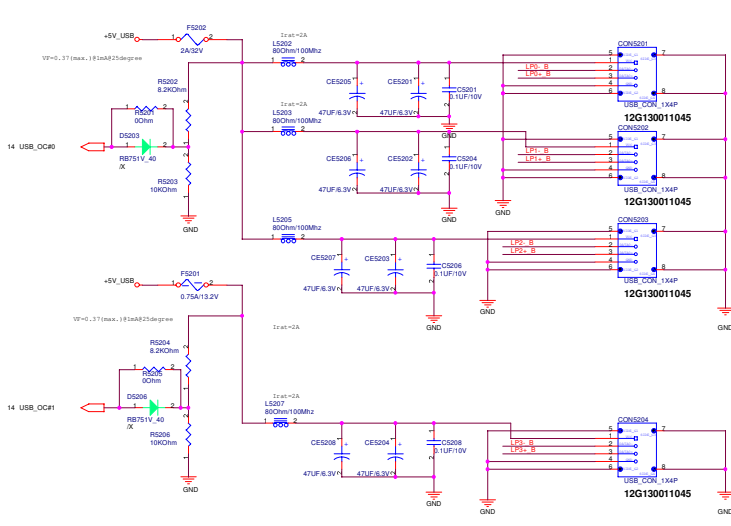
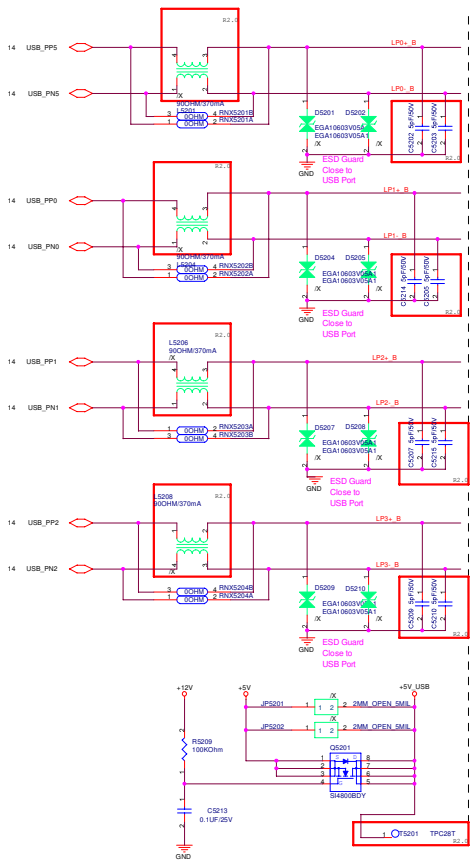
SATA_HDD(Default)



CD-ROM

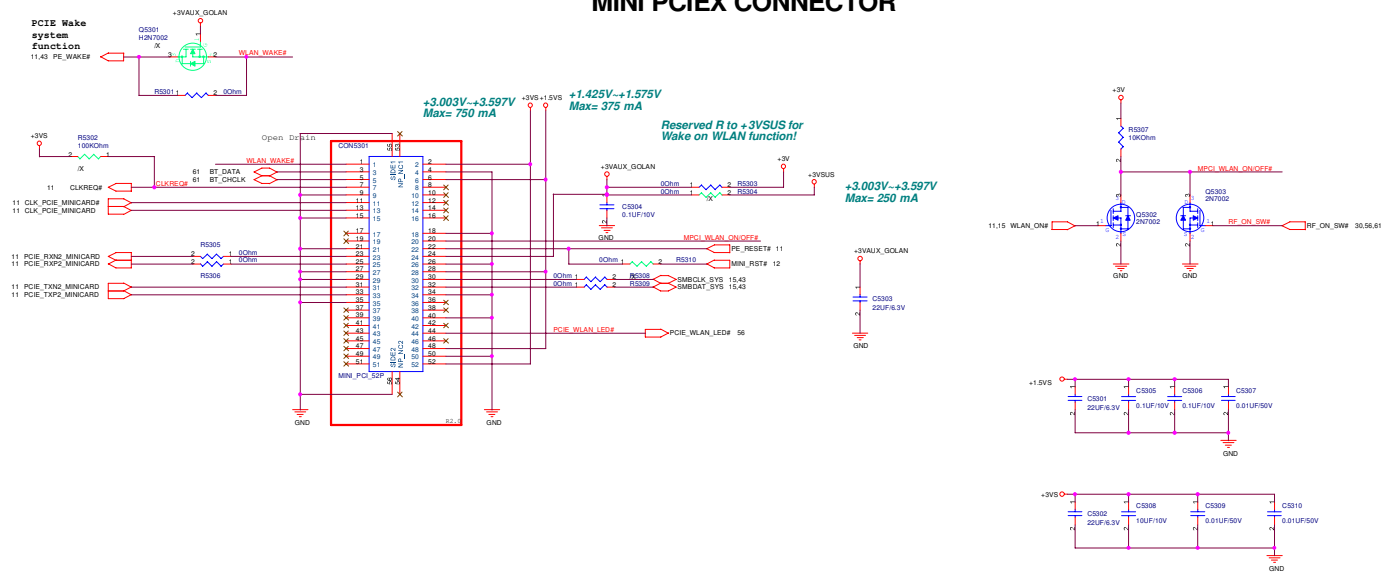


ASUS
ASUSTek Computer Inc.
Title: FSU
Engineer: He Wang
Rev: 1.0
Date: 08-10-2007 Sheet: 51 of 88





ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Rev	Project Name	Rev	
1	FSU	1.0	
Date: 2011-01-20 10:07	Sheet: 51	of	58

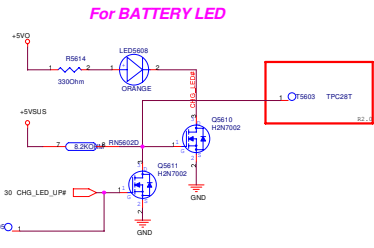
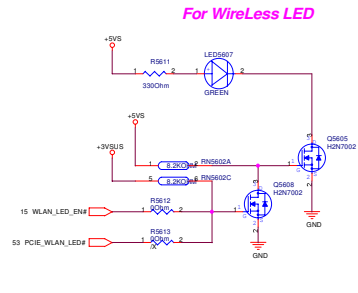
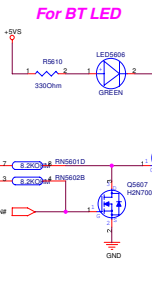
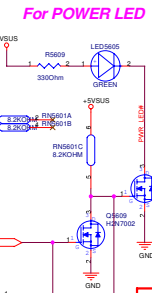
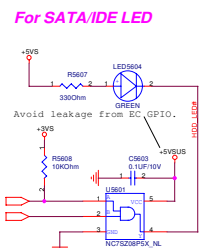
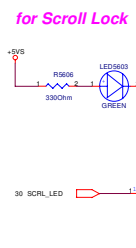
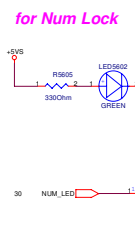
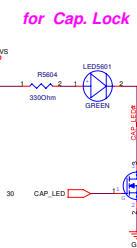
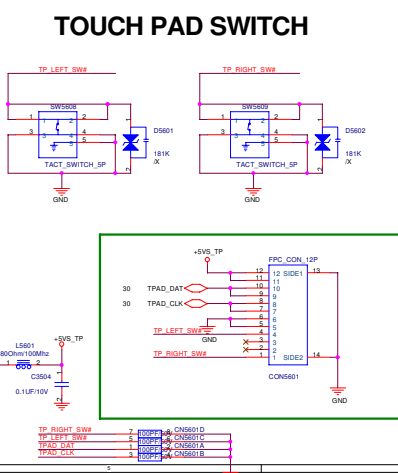
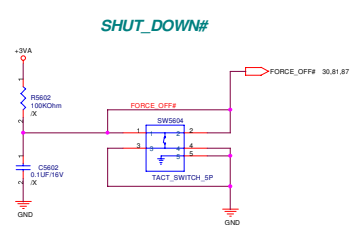
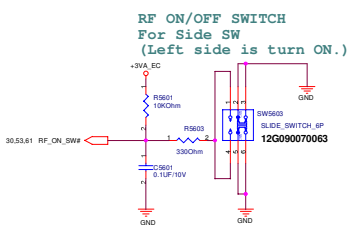
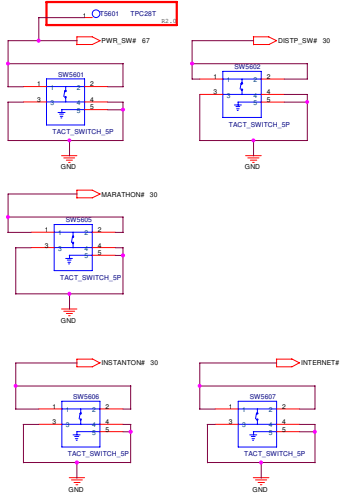
MINI PCIEX CONNECTOR



ASUS		Title : FSU	
ASUSTek Computer Inc.			
Rev	Project Name	Engineer: He Wang	
C	FSU	Rev 1.0	
Date: 2011-07-29 10:07	Sheet: 51		Total: 58

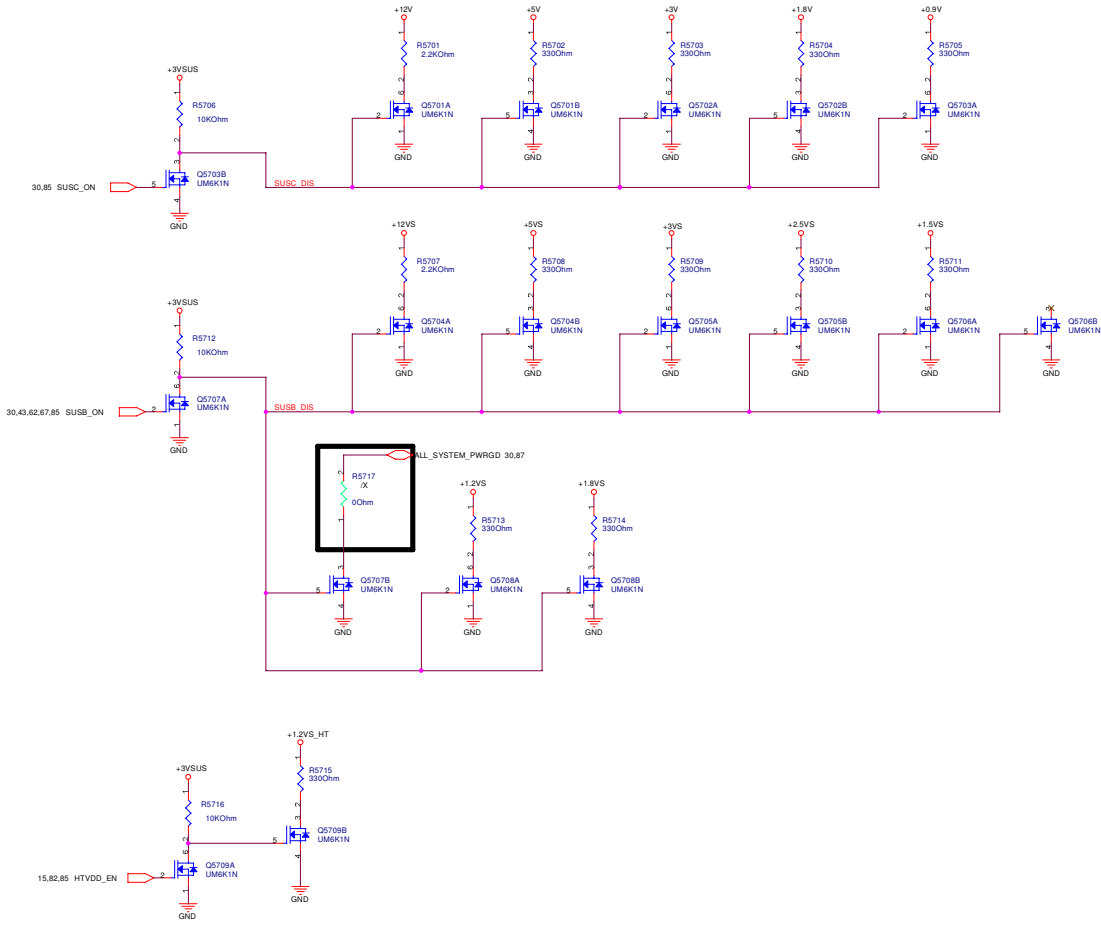
		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-09-29 10:07	Sheet: 54	of	58

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 05	of	06





ASUS		Title : FSU	
ASUSTek Computer INC.		Engineer: He Wang	
B24	Project Name		Rev
C	FSU		1.0
Date: 08-10-2007	Drawn: 56	By: 56	56

DISCHARGE CIRCUIT

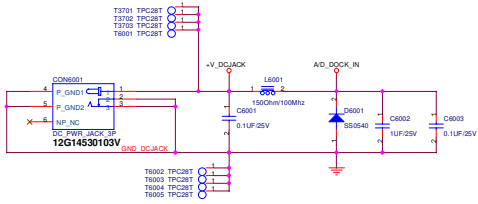


ASUS		Title : FSU	
ASUSTek Computer, INC		Engineer: He_Wang	
Size	Project Name	Rev	
Custom	FSU	1.0	
Date: 2011.09.20	Drawn: 37	of	38

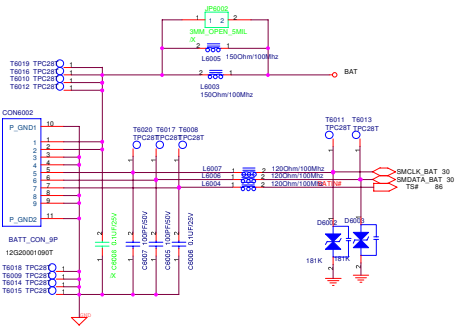
		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 01	of	01

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 01	of	01

Adaptor IN Circuit

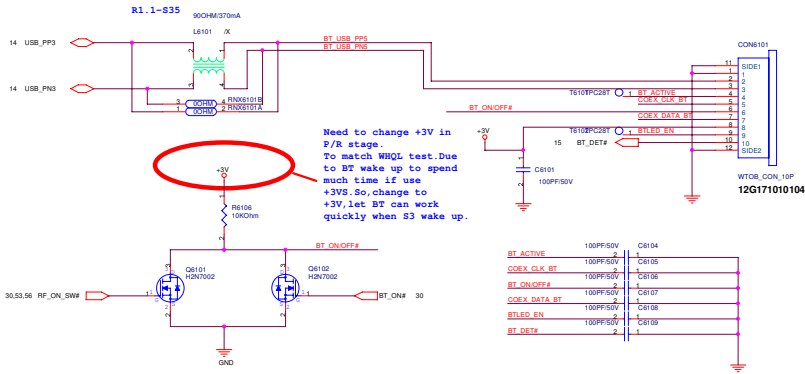


BATTERY IN CIRCUIT

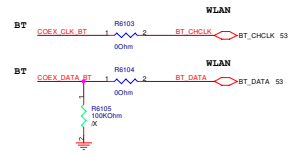
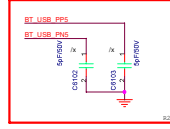


ASUS		Title : FSU	
ASUSTek Computer INC.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-29 10:07	Sheet: 65	of	68

BLUETOOTH CONNECTOR

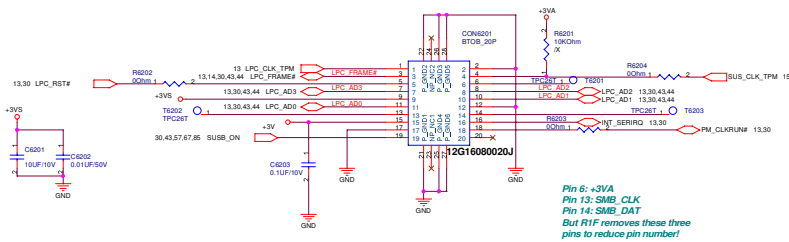


Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT





ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 61	of	68


TPM CONN.




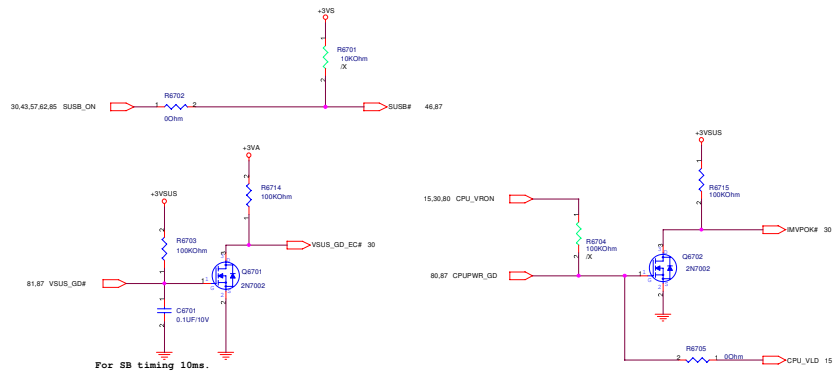
ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU		1.0
Date: 2011-01-20 10:07	Sheet: 61	of	68

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-03-29 10:07		Sheet: 01	of 01

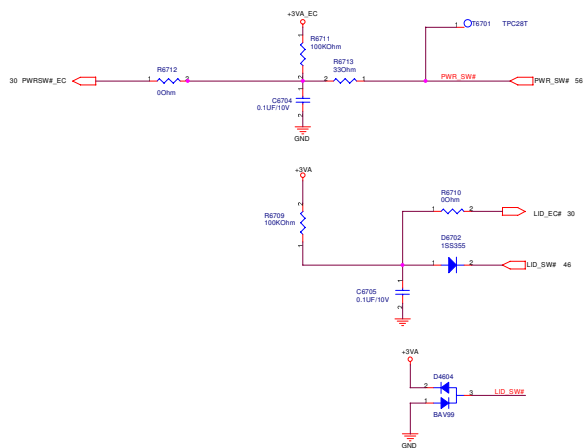
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ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-05-25 10:07	Sheet: 64	of	68

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-05-25 10:07	Sheet: 65	of	68

		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-03-29 10:07		Sheet: 01	of 01

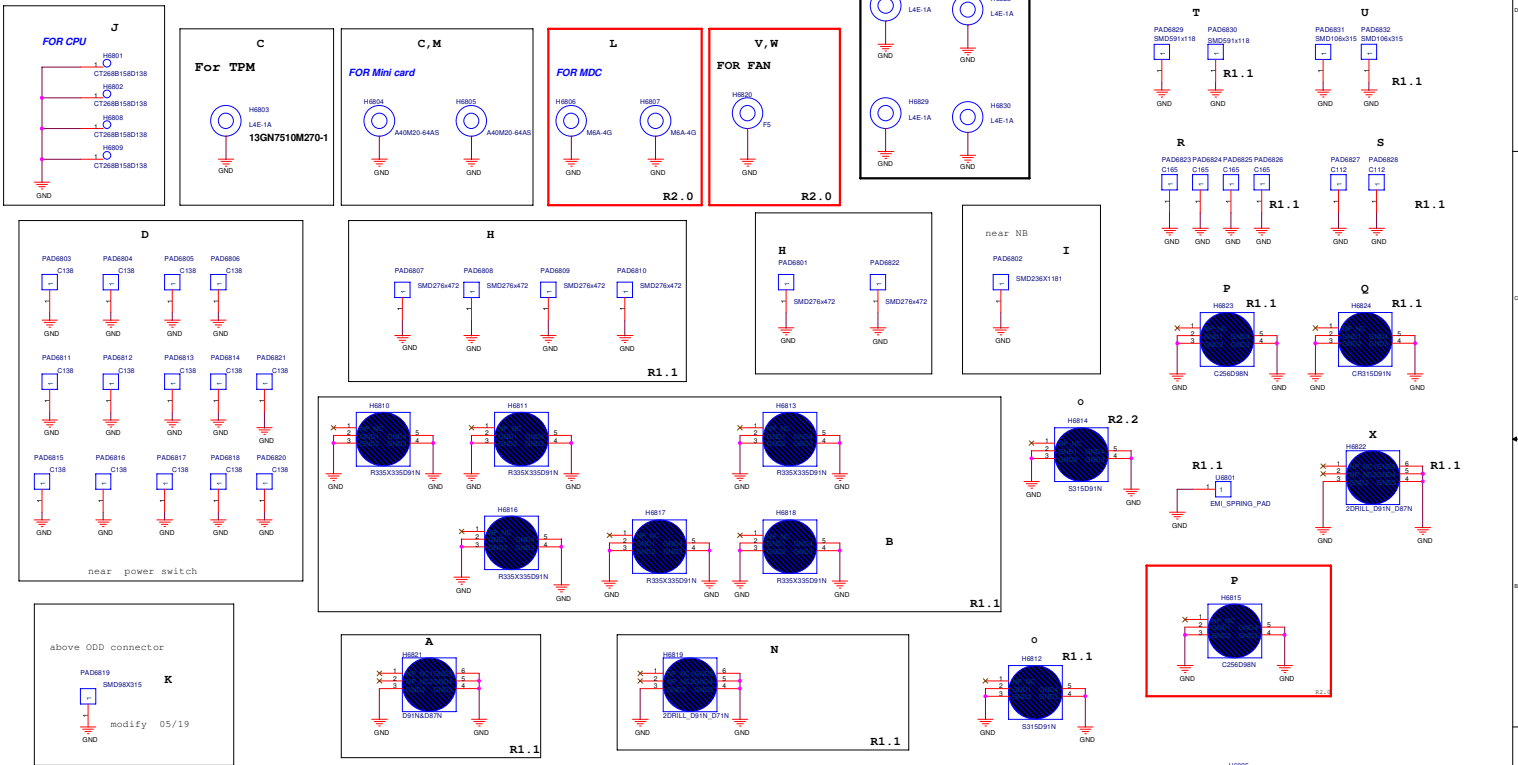


POWER SWITCH





ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-20 10:07	Sheet: 67	of	88


FOR Thermal
R2.0





ASUS		Title : FSU	
ASUSTek Computer Inc.			
8528	Project Name	Engineer: He Wang	
C	FSU	Rev	1.0
Date: 2019-05-20 10:07	Sheet: 68	of	68


		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 01	of	01


		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-03-29 10:07		Sheet: 01	of 01


		Title : FSU	
ASUS Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-10-26 2007		Sheet: 11 of 28	


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 15 of 28	


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 13 of 28	


		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-26 2007		Sheet: 14 of 28	

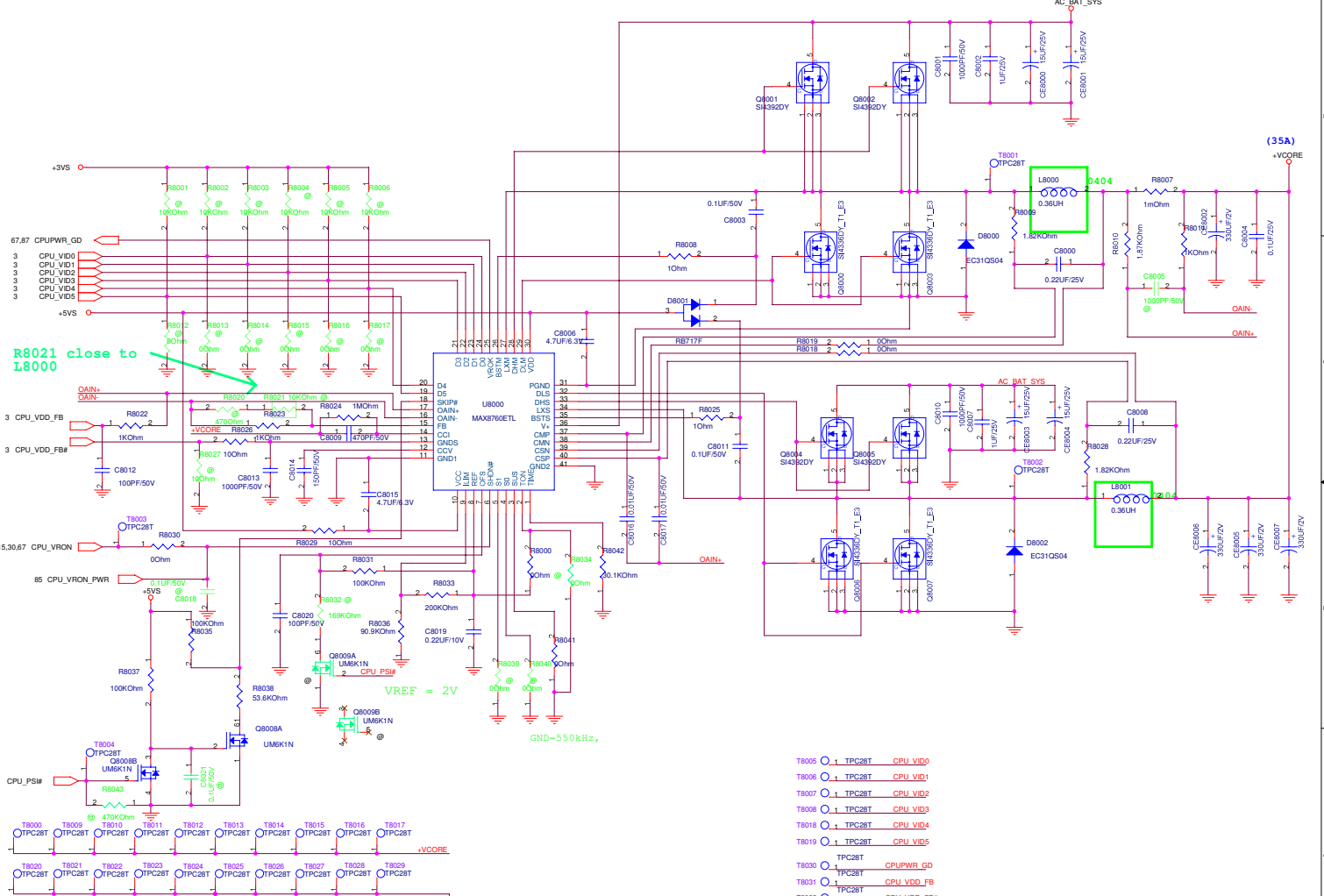
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ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date:	2011-11-28 2007	Sheet:	15 of 28

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-11-28 2007		Sheet: 16 of 28	

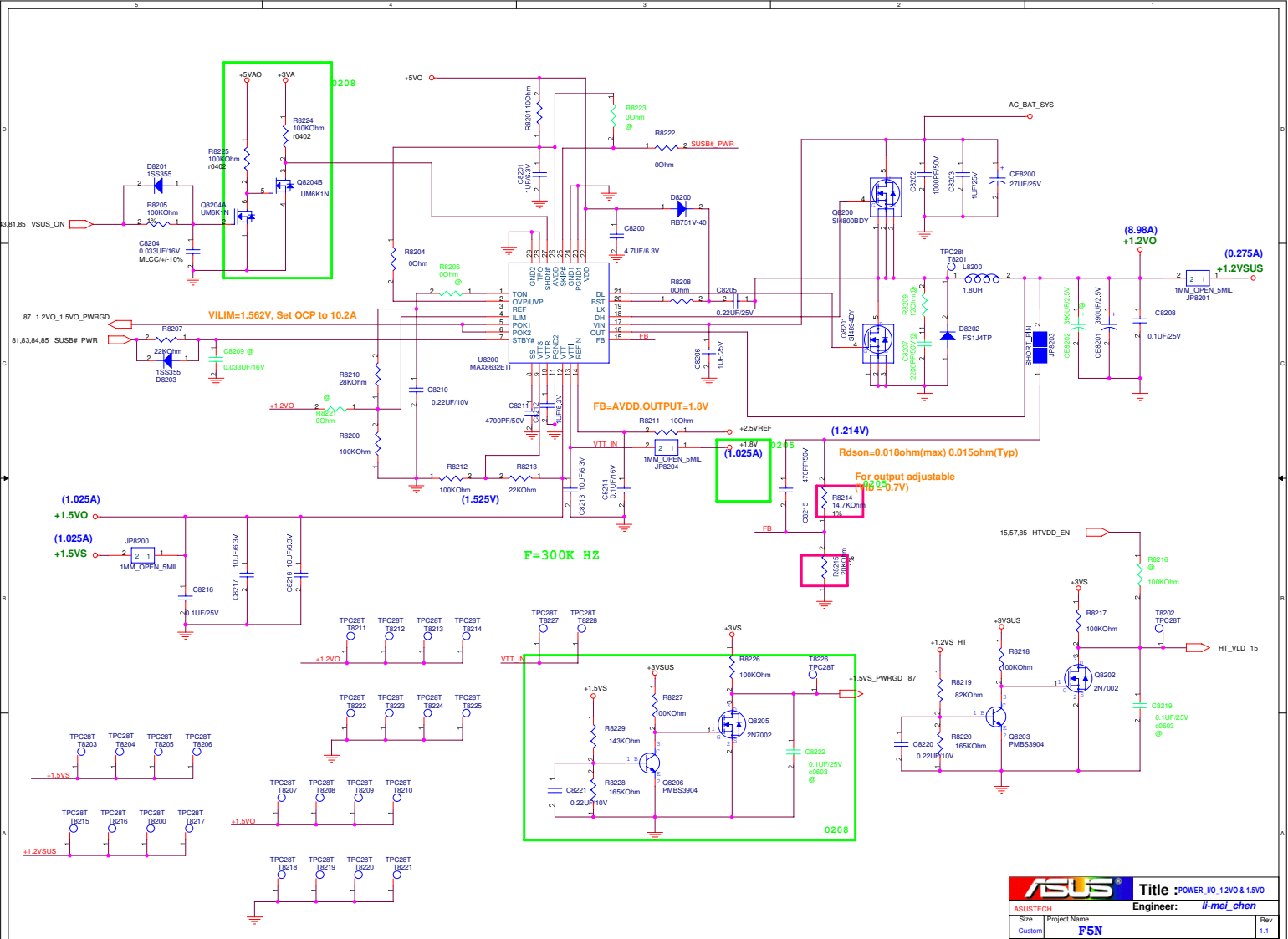
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ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2007-10-26 2007		Sheet: 11	of 28

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-11-28 2007		Sheet: 15 of 25	

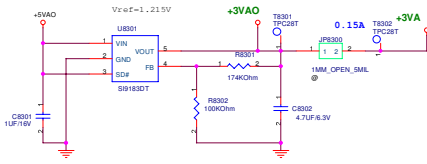
		Title : FSU	
ASUSTeK Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-03-29 10:07		Sheet: 01	of 01



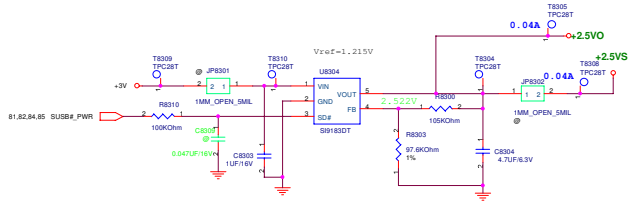
ASUS		Title : POWER_VCORE	
ASUSTek	Project Name	Engineer: li-mei_chen	
Size	Custom	F5N	Rev 1.1
Date: 11/11/09	09/2007	Sheet 80	of 88



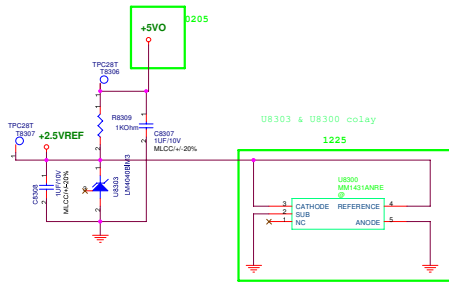
ASUS		Title : POWER_I0_1.2V0 & 1.5V0	
ASUSTECH	Project Name	Engineer: li-mei_chen	
Custom	F5N	Sheet	82 of 88
Date: 11/19/09	Rev	1.1	



+3VA

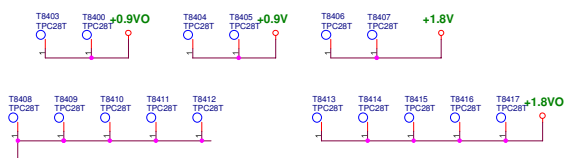
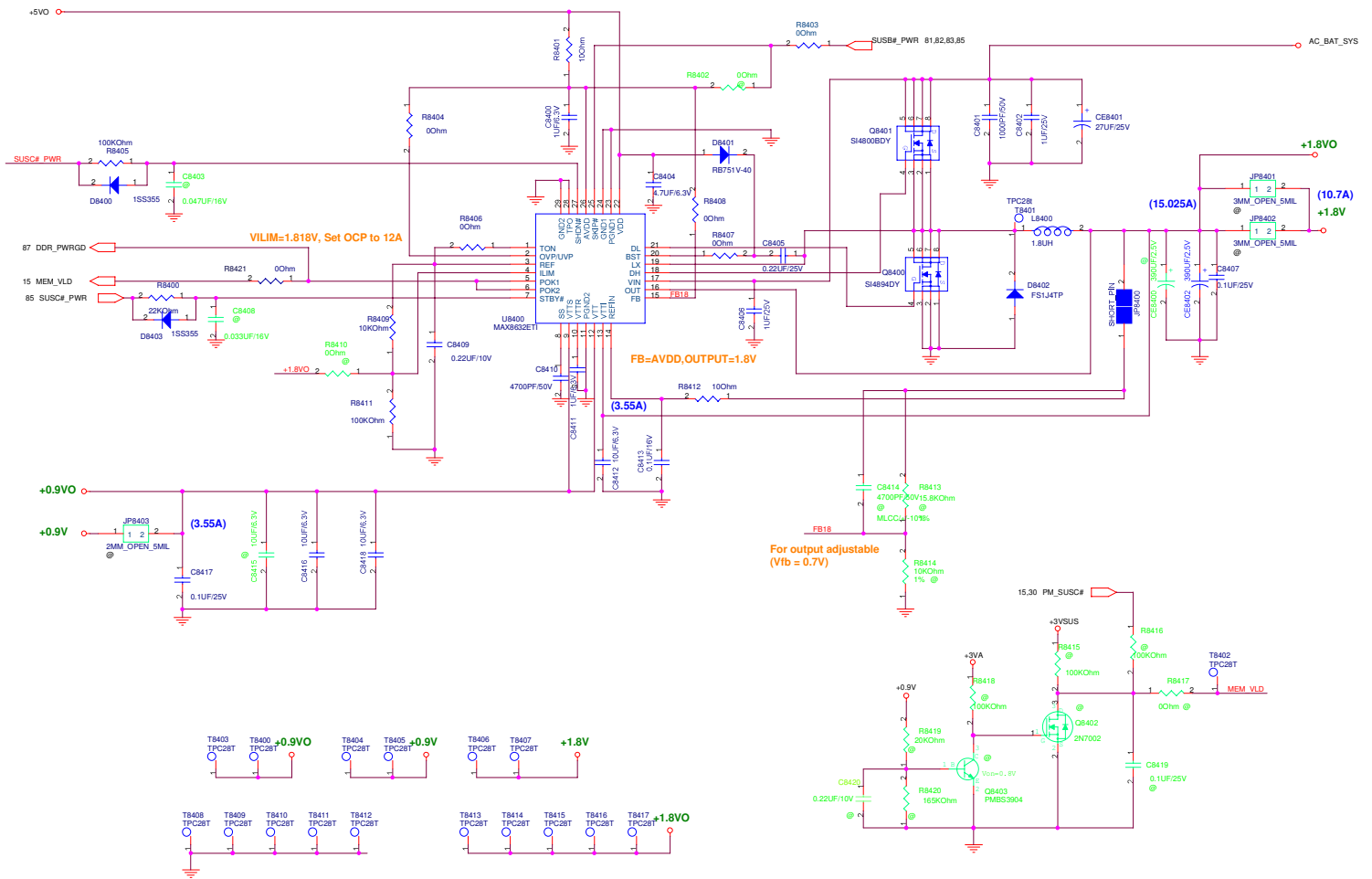


+2.5VS

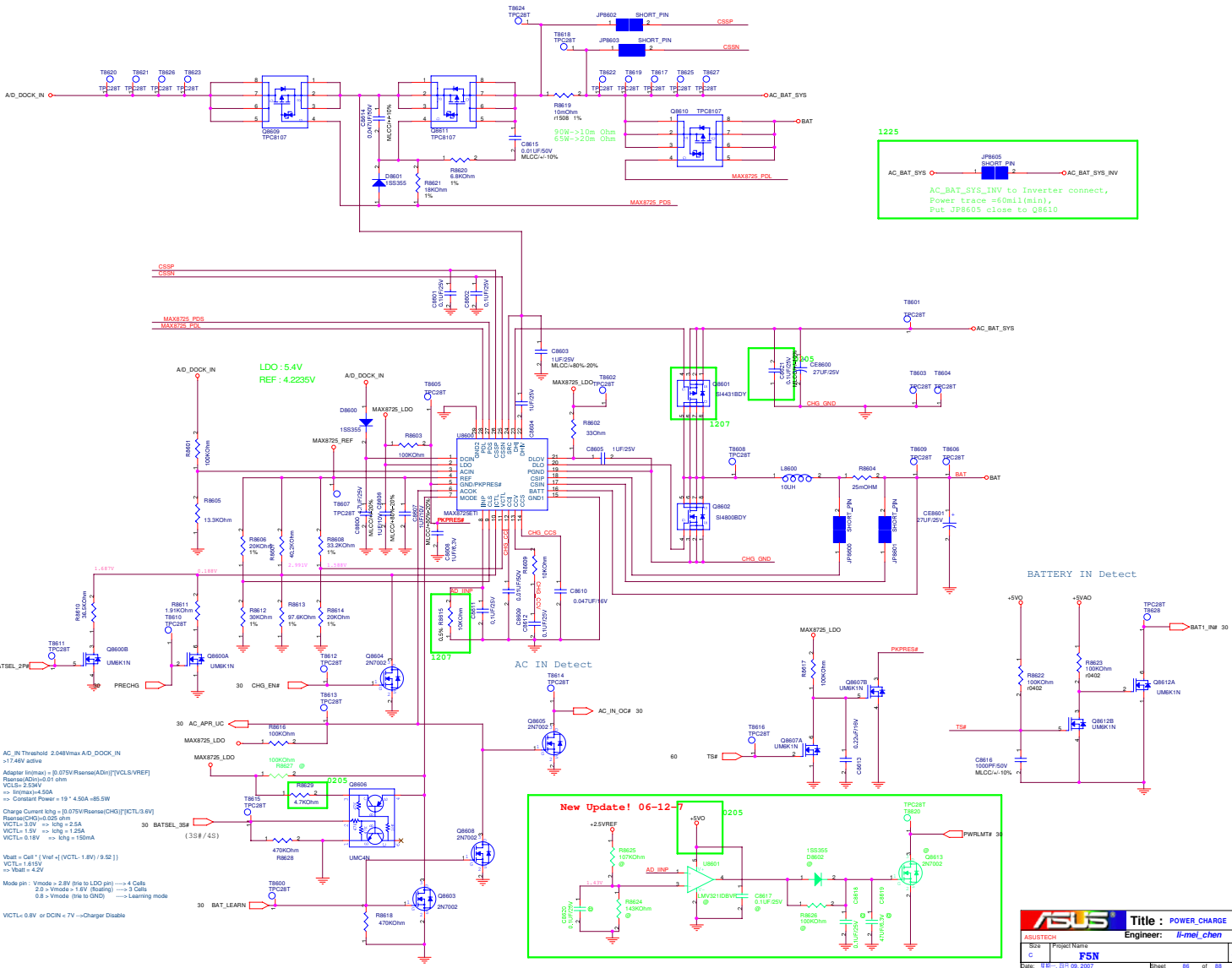


+2.5VREF

ASUS		Title : POWER_IO_L00	
ASUSTECH	Project Name	Engineer: li-mei_chen	
Size	Rev	1.1	
C	FSN		
Date: 2011-07-26 20:00	Sheet: 61	of 68	

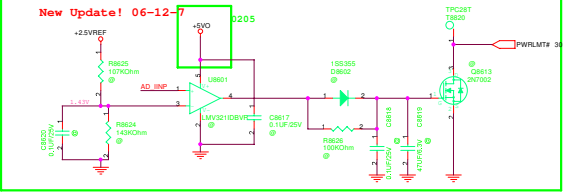


ASUS		Title : POWER_IQ_D0R1	
ASUSTECH	Project Name	Engineer: li-mei_chen	
Custom	F5N	Size	Rev 1.1
Date: 11/11/09 2007	Sheet 84	of 88	



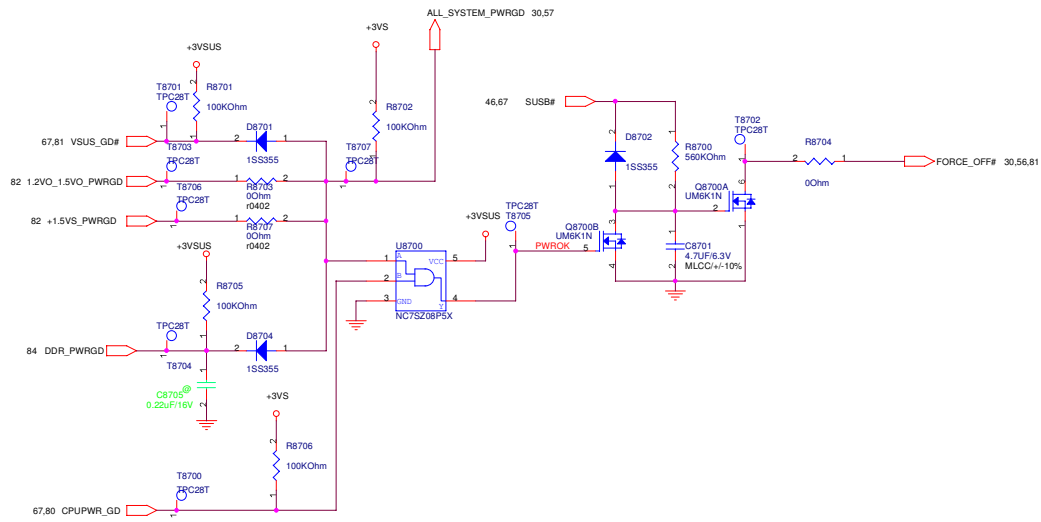
1225
 AC_BAT_SYS_INV to Inverter connect,
 Power trace =60mil(min),
 Put JP8605 close to Q8610

LDO : 5.4V
 REF : 4.2235V

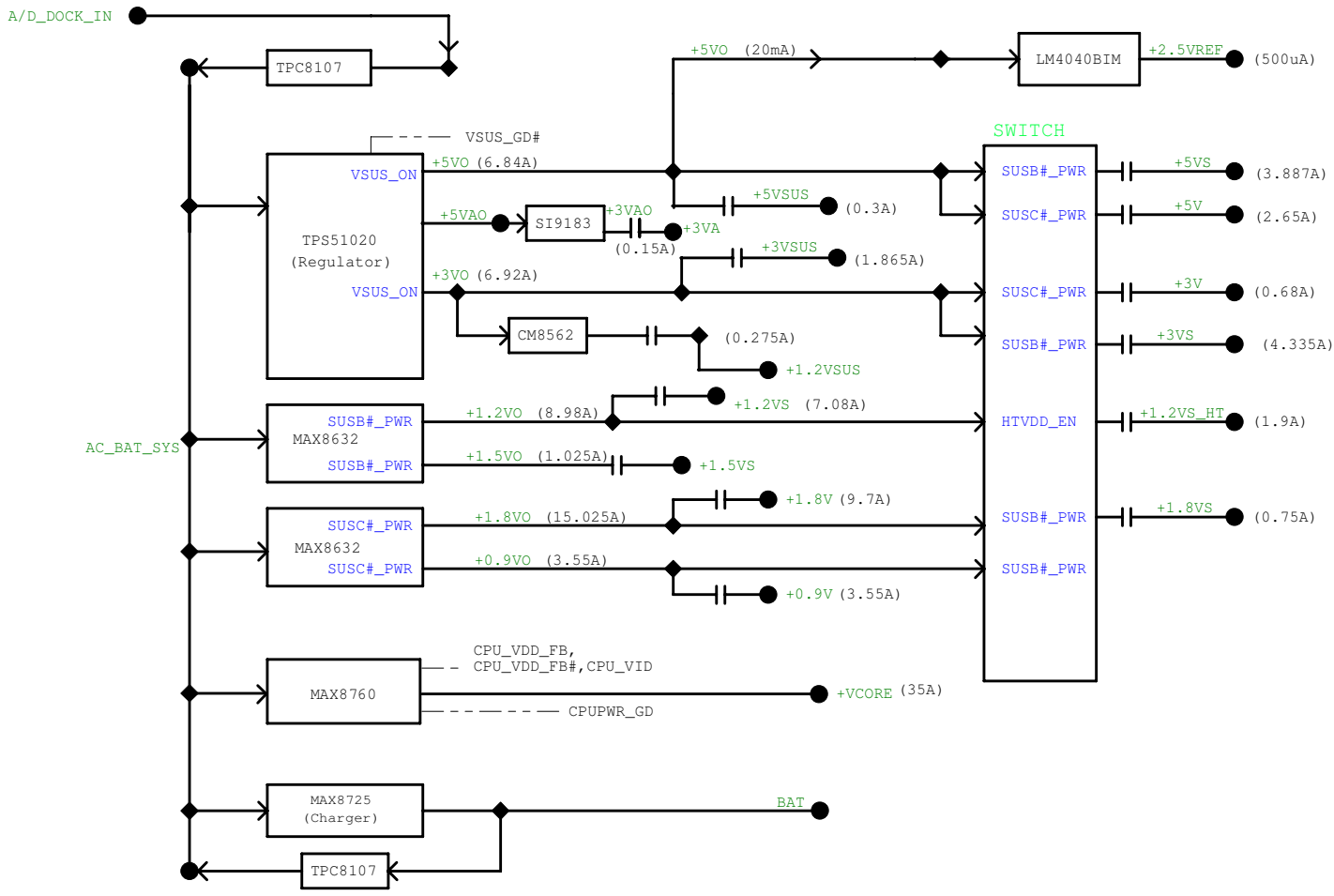


- AC_IN Threshold 2.048Vmax A.D_DOCK_IN
 => 1749V active
- Adapter In(max) = (0.075V/Rsense/AD)/[VCL5/VREF]
 Rsense=40mΩ/0.01 ohm
 VCL5= 2.54V
 => In(max)=4.50A
- Charge Current kIq = (0.075V/Rsense/CHG)/[VCL2/3.6V]
 Rsense=CHG=0.025 ohm
 VCL2= 3.6V => Iqg = 2.5A
 VCL1= 1.5V => Iqg = 1.25A
 VCL1= 0.18V => Iqg = 150mA
- Vbat = Cell * [Vref - (VCL1 - 1.8V) / 9.52]
 VCL1 = 1.51V
 => Vbat = 4.5V
- Mode pin : Vmode > 2.8V (High to LDO pin) => 4 Cells
 2.8 > Vmode > 1.6V (Floating) => 3 Cells
 0.8 > Vmode (pin to GND) => Learning mode
- VCL1= 0.6V or DCIN < TV -->Charger Disable

ASUS		Title : POWER_CHARGE	
Rev	Project Name	Engineer: li-mei_chen	
C	F5N		
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ASUS		Title : POWER_PROTECT	
ASUSTECH	Project Name	Engineer:	li-mei_chen
Size	Custom	F5N	Rev 1.1
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ASUS		Title : POWER DIAGRAM	
ASUSTECH	Project Name	Engineer: <i>li-mei_chen</i>	Rev
Size	Custom	F5N	1.1
Date: 11/11/09	09/2007	Sheet	88 of 88