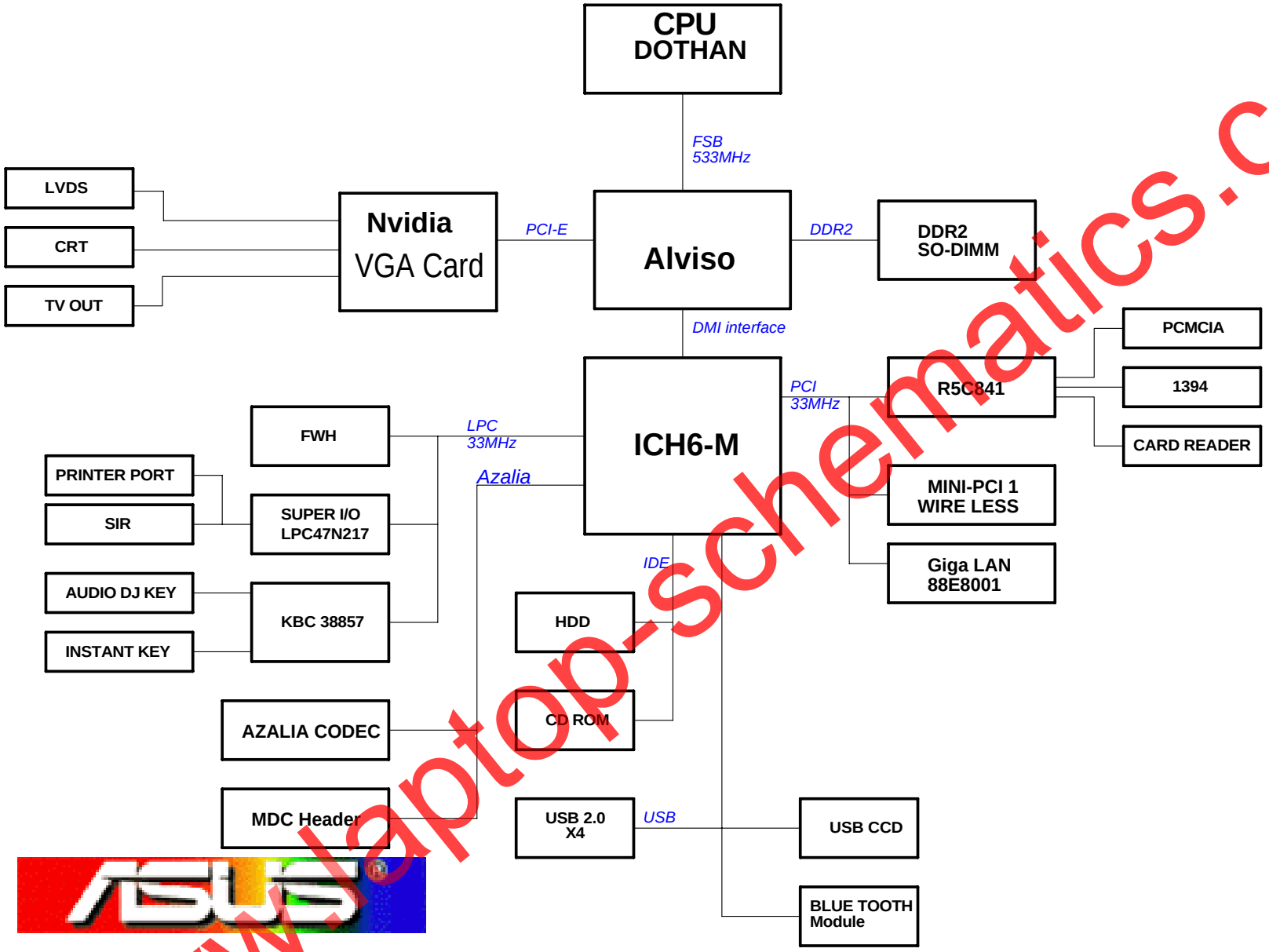
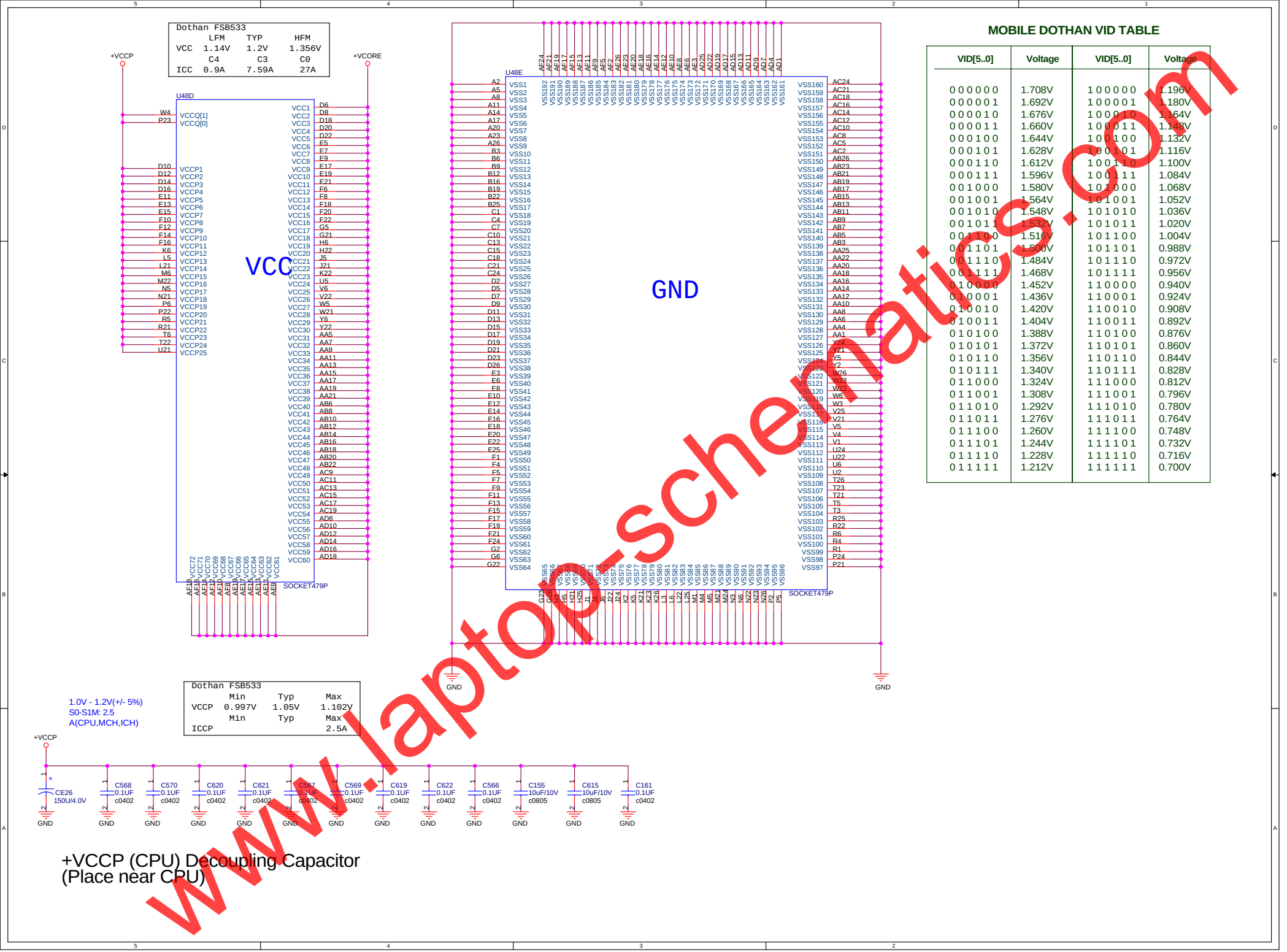




MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

Fan Speed Control

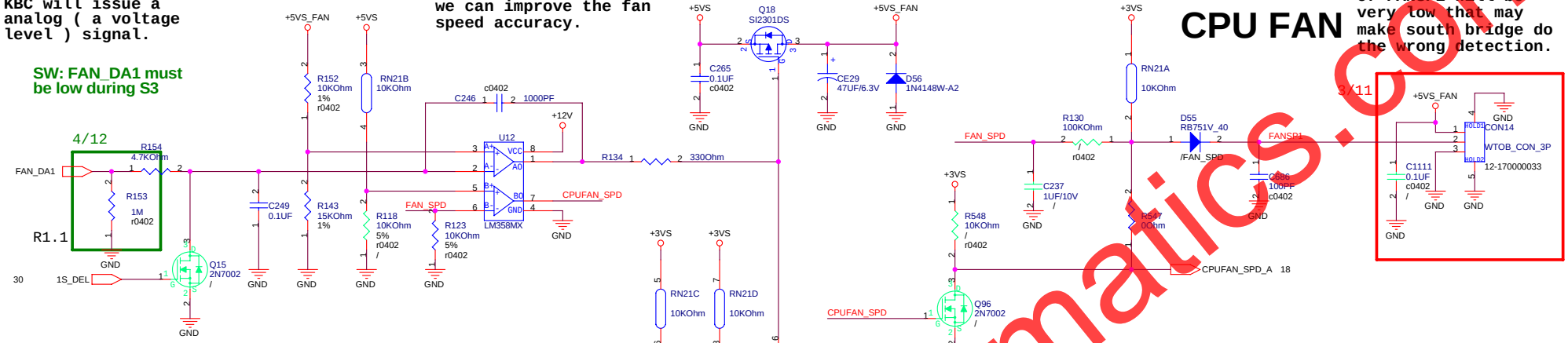
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

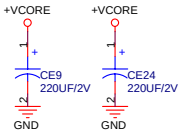
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

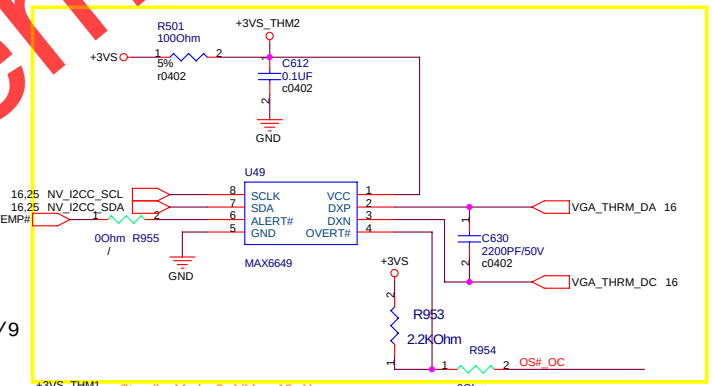
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN

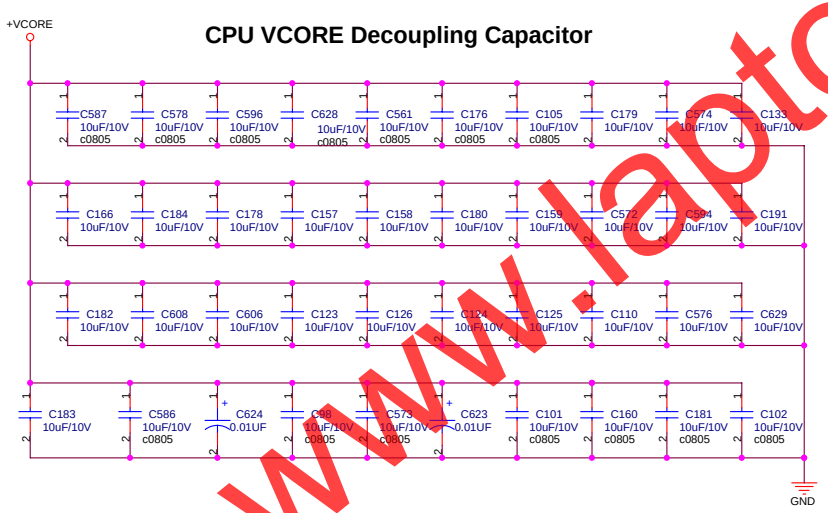


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)





CPU VCORE Decoupling Capacitor



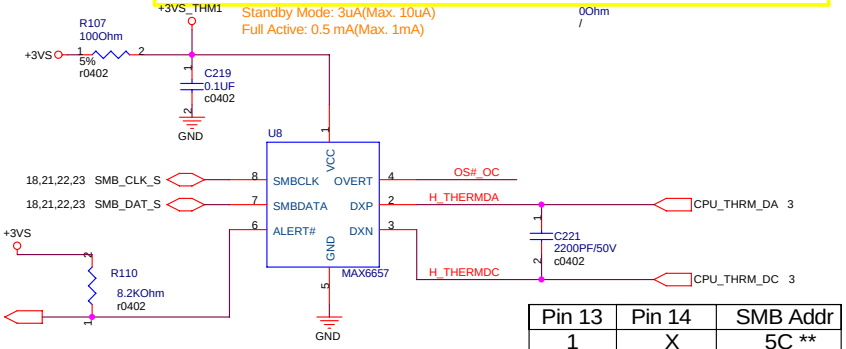
Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

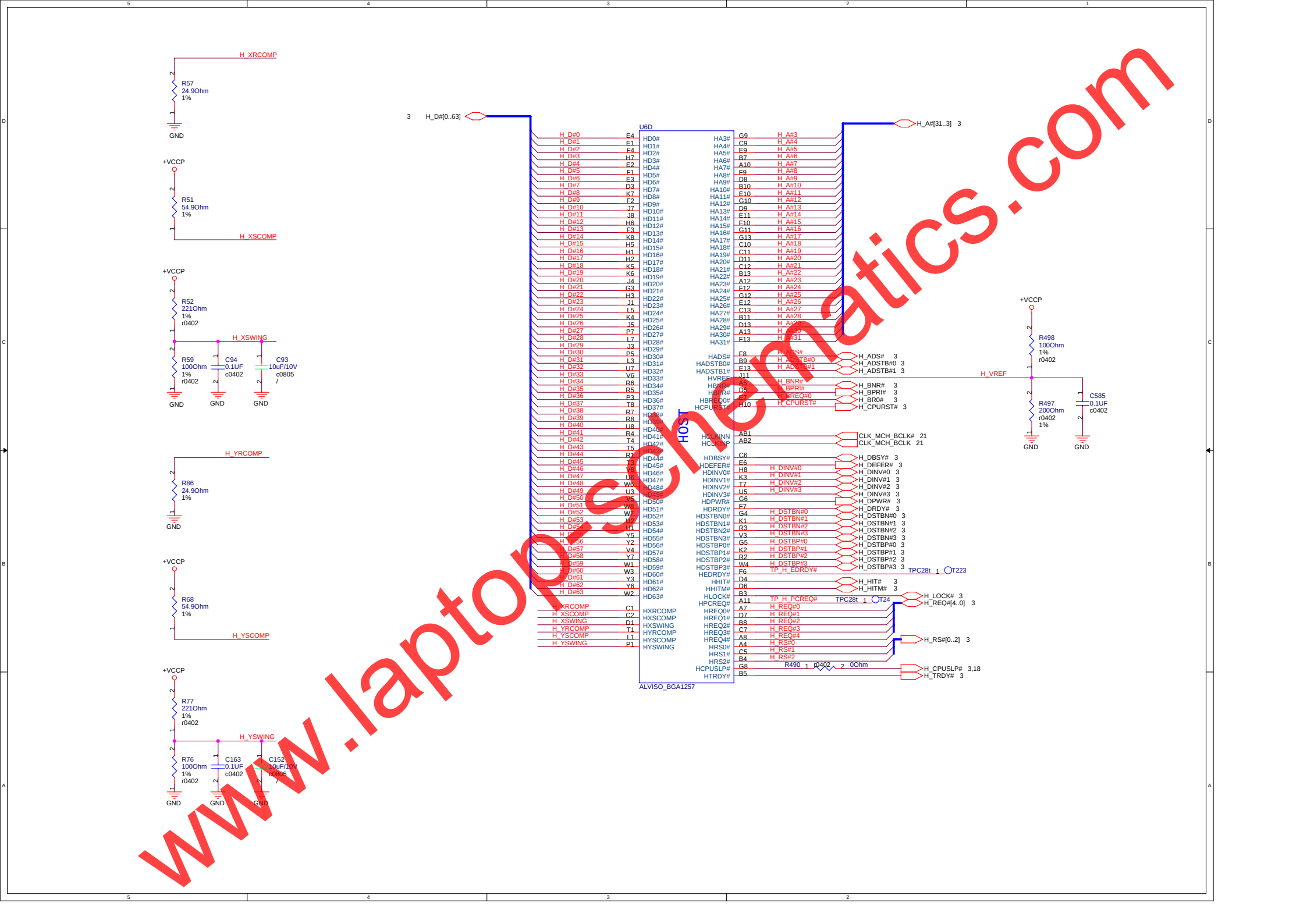
+VCORE Bulk Decoupling

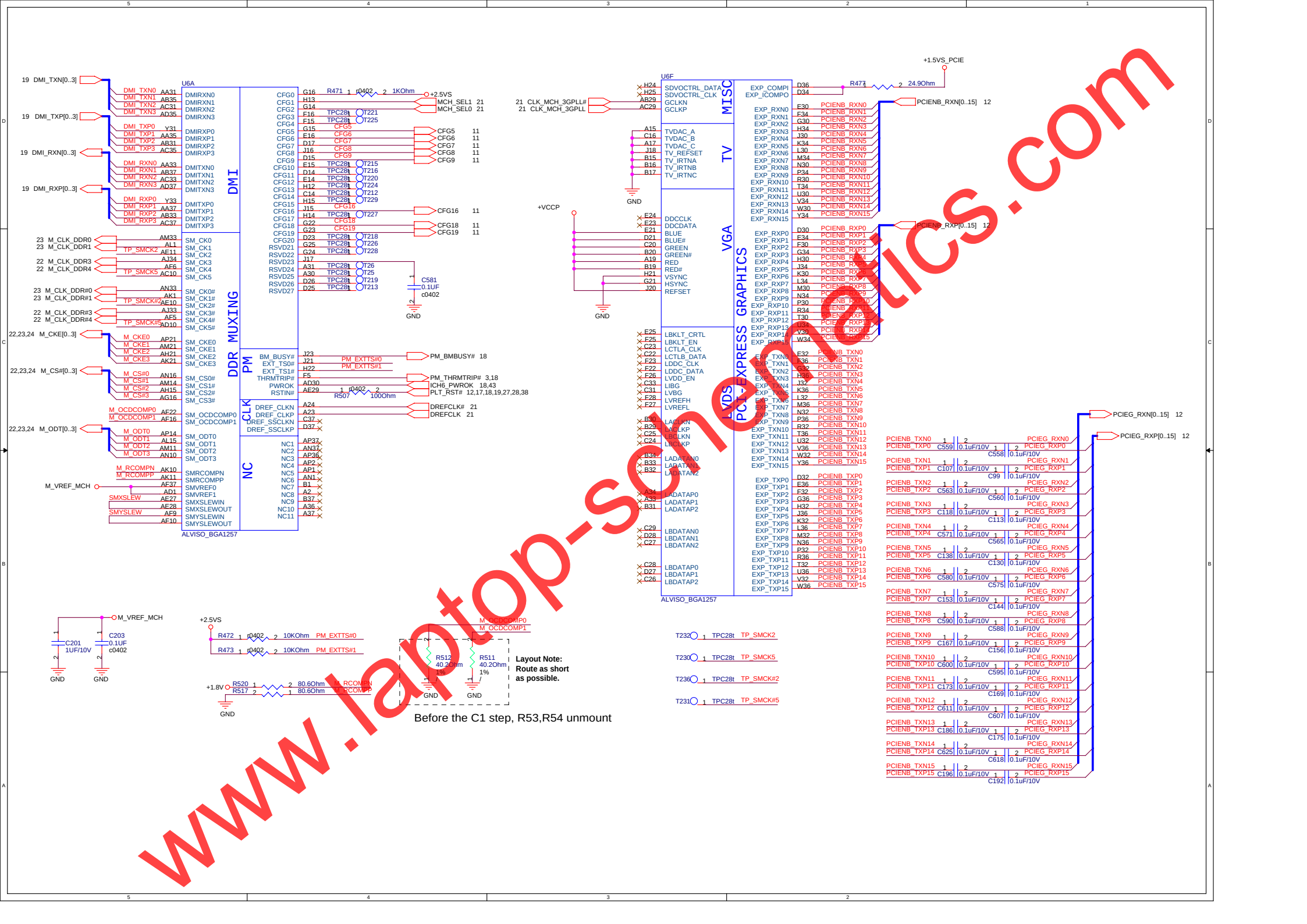
Close to Pin A18 & B18 of CPU

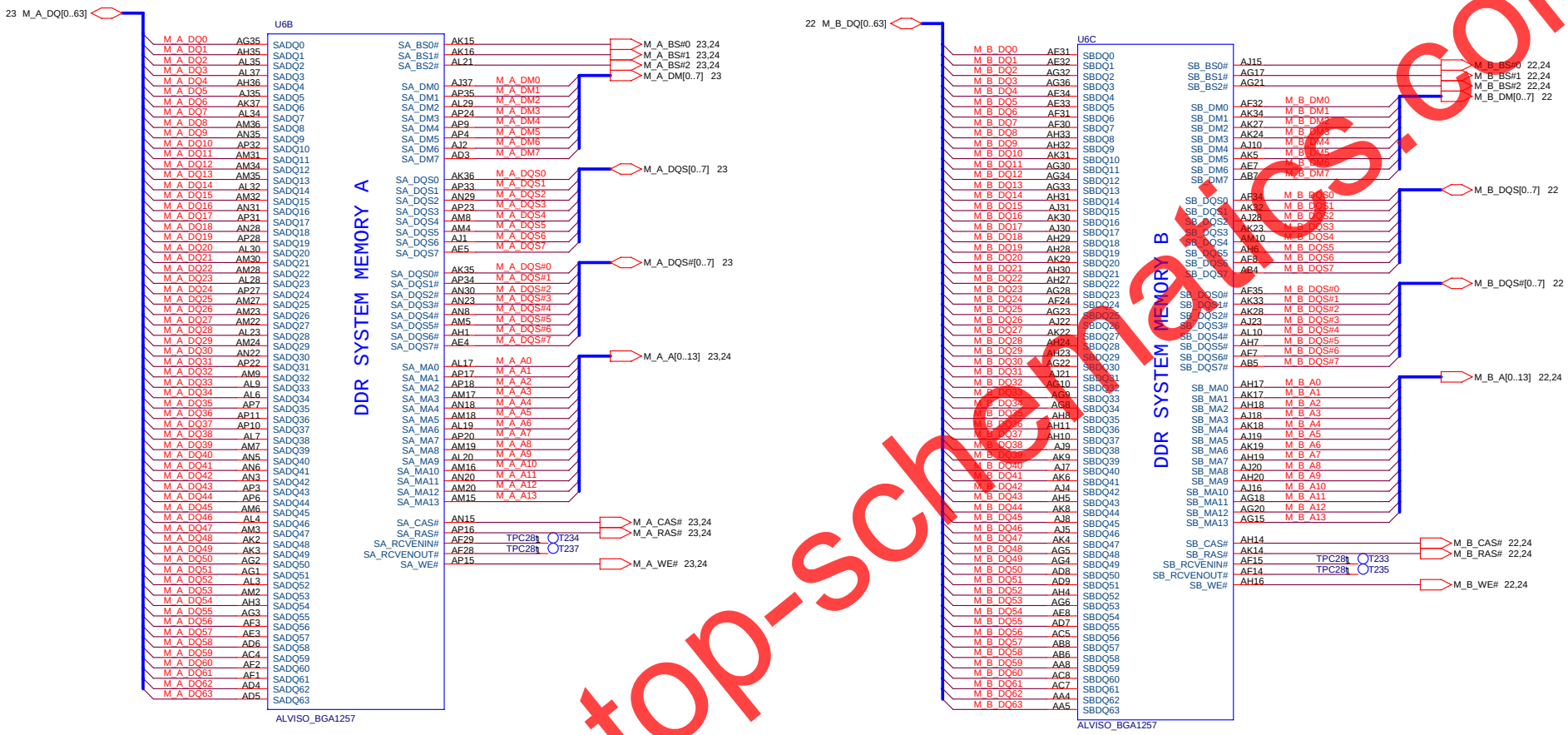
Four 200 uF are located in IMVP4

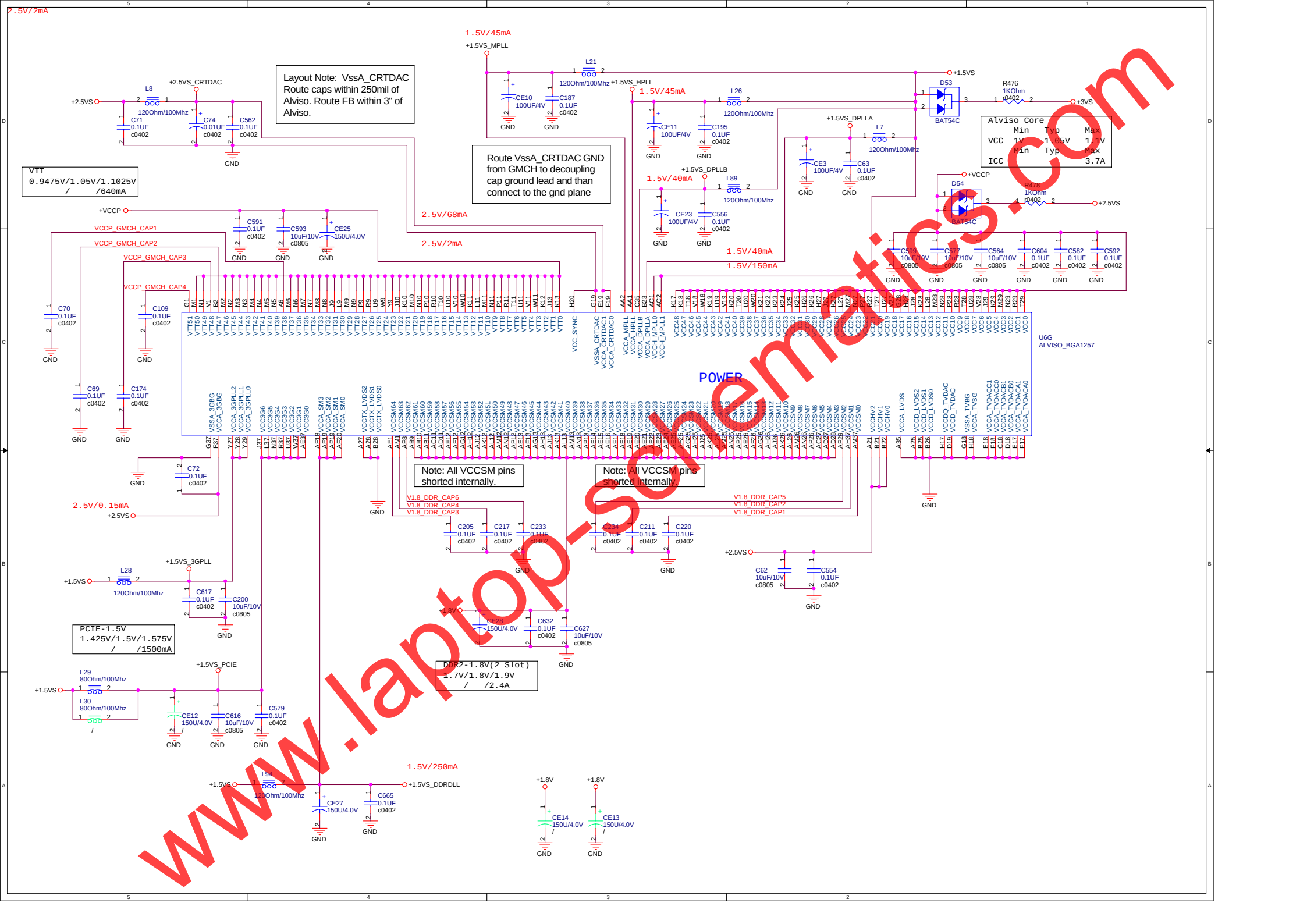


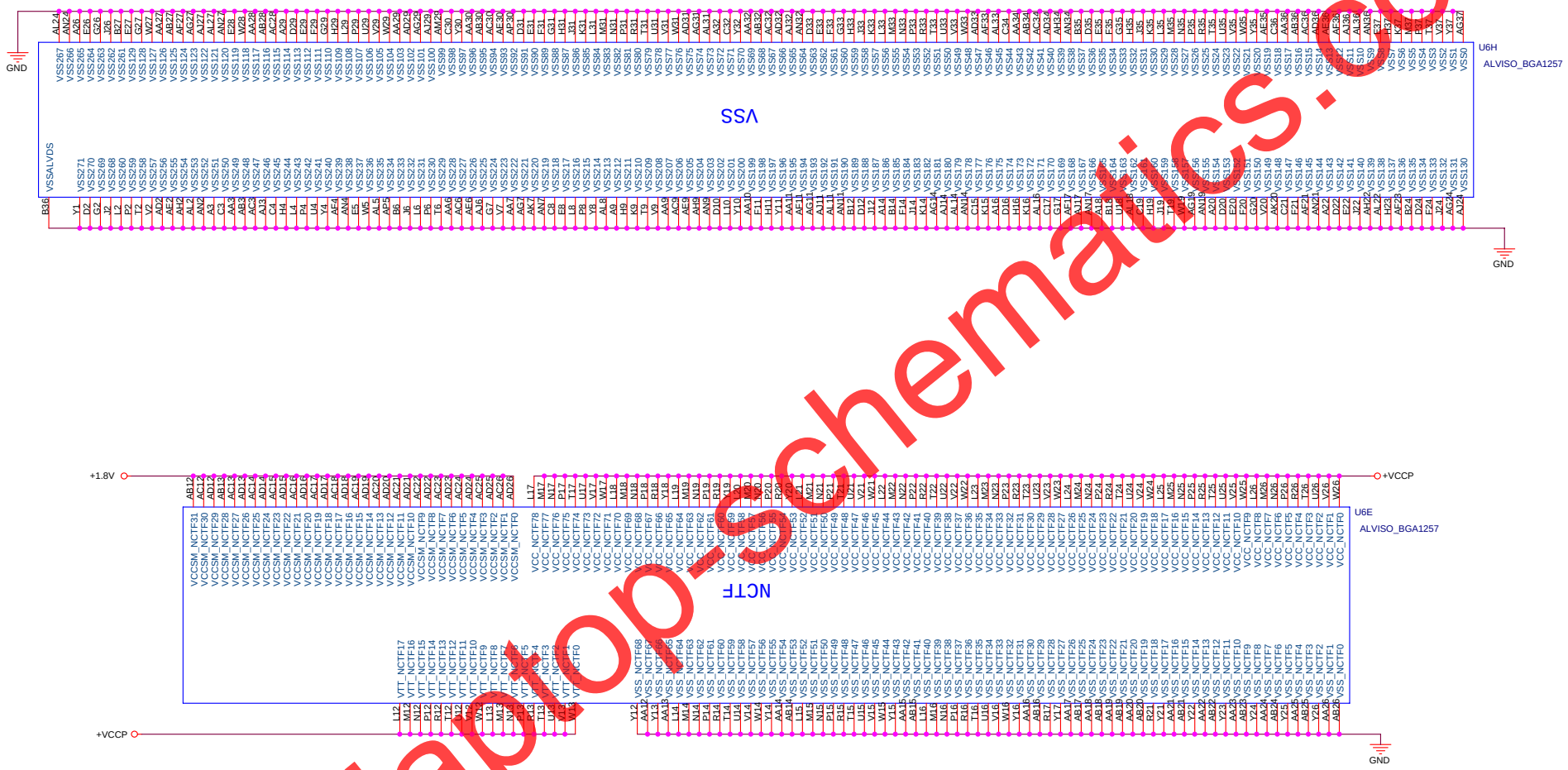
Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58




U6A
DMI
DDR MUXING
PM
CLK
NC
ALVISO_BGA1257
U6F
MISC
TV
VGA
LVDS
PCI-E EXPRESS GRAPHICS
ALVISO_BGA1257
+1.5VS_PCIE
+2.5VS
+1.8V
+VCCP
GND
Layout Note:
Route as short
as possible.
Before the C1 step, R53,R54 unmount
www.laptop-schematics.com



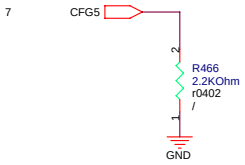




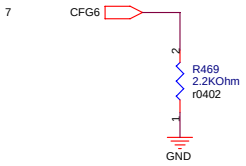
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present
(Default)

CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)

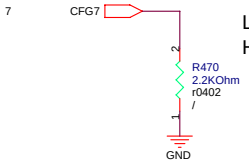


CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)



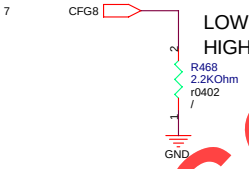
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



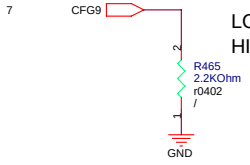
CFG8 : PCI-X POWER Saving

LOW = PCI-X POWER Saving
HIGH (Default)



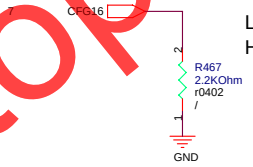
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



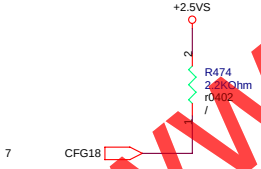
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



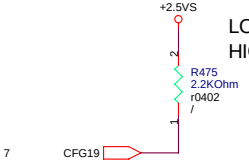
CFG18 : VCC SELECT

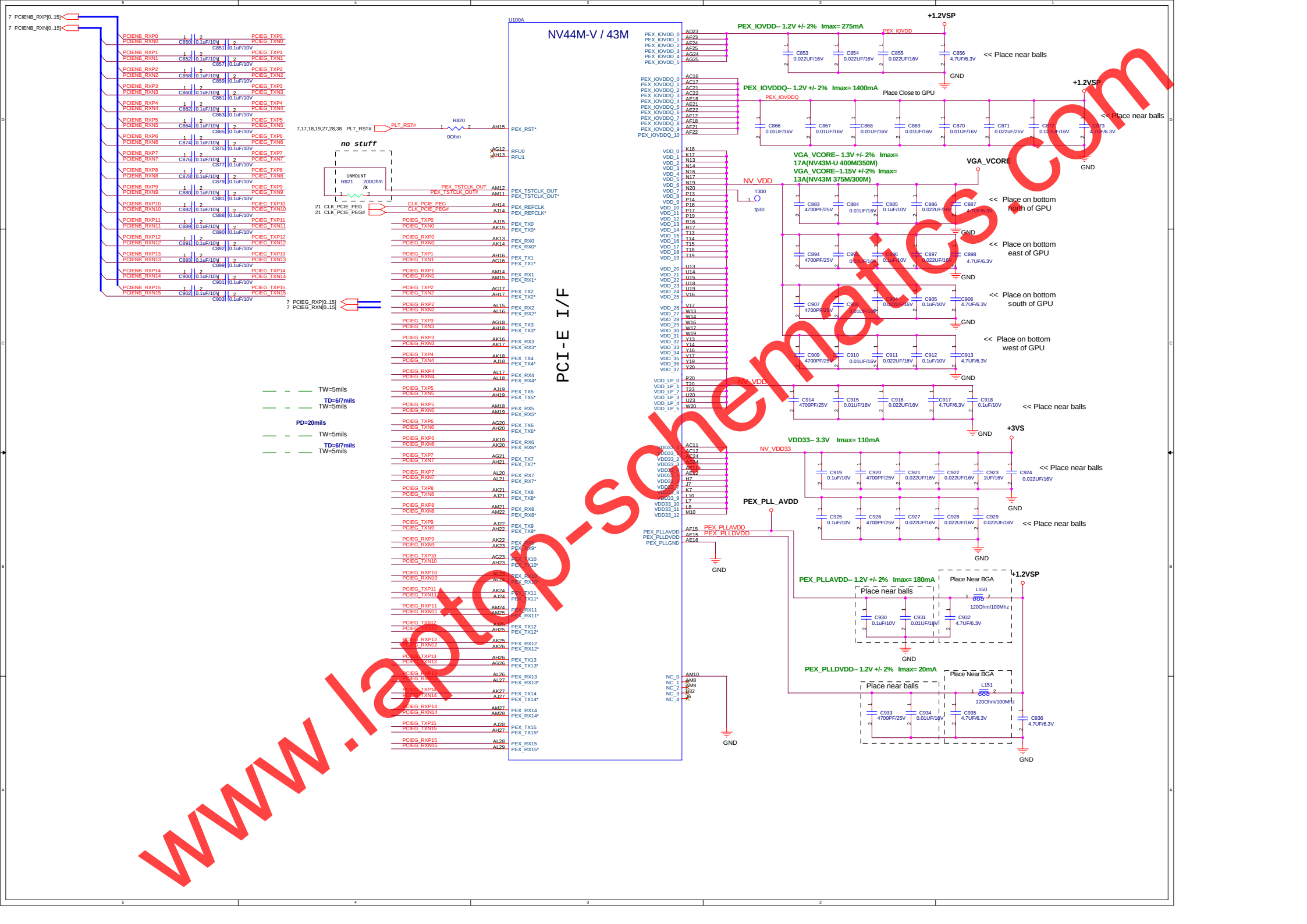
LOW = 1.05V (Default)
HIGH = 1.5V

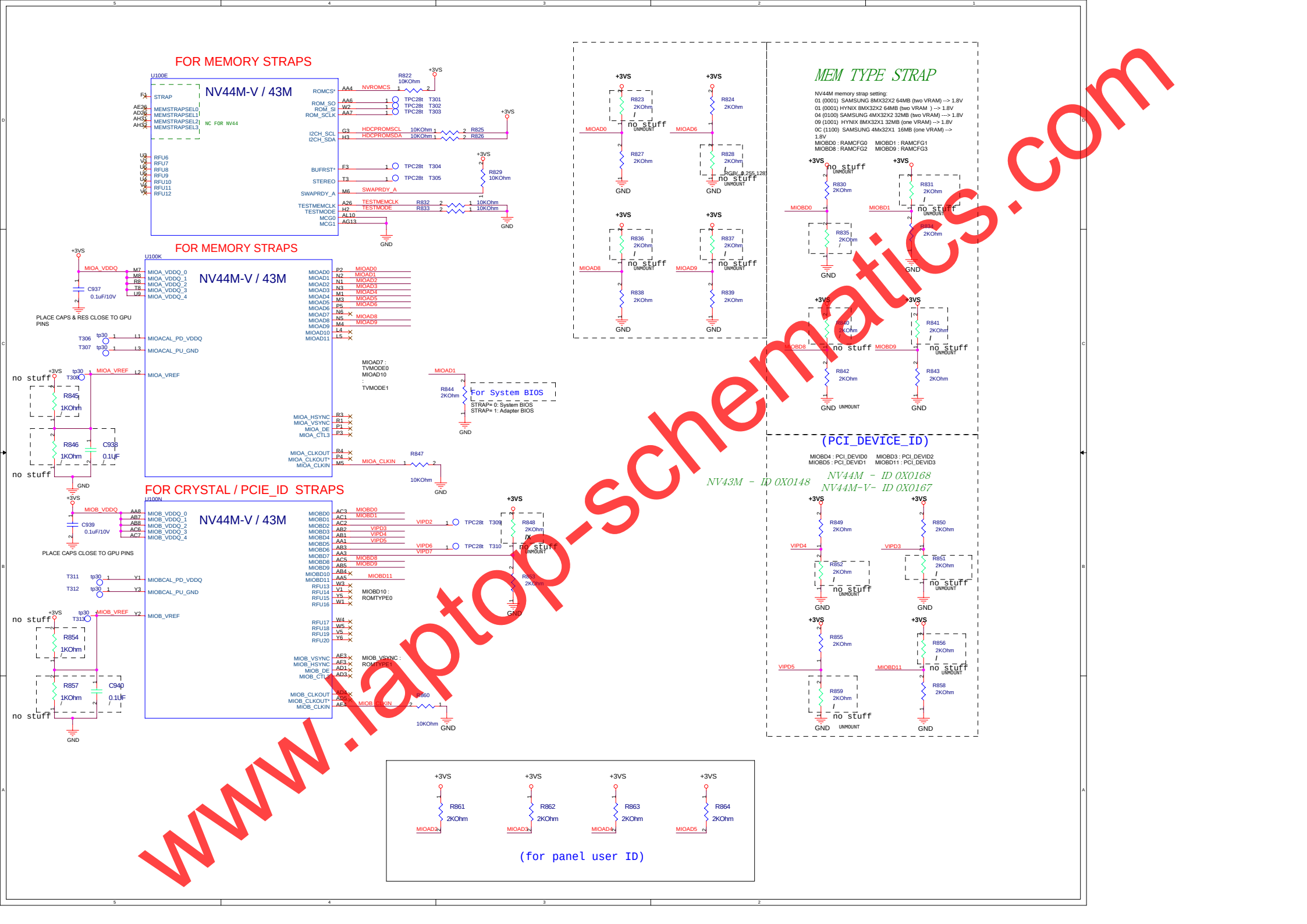


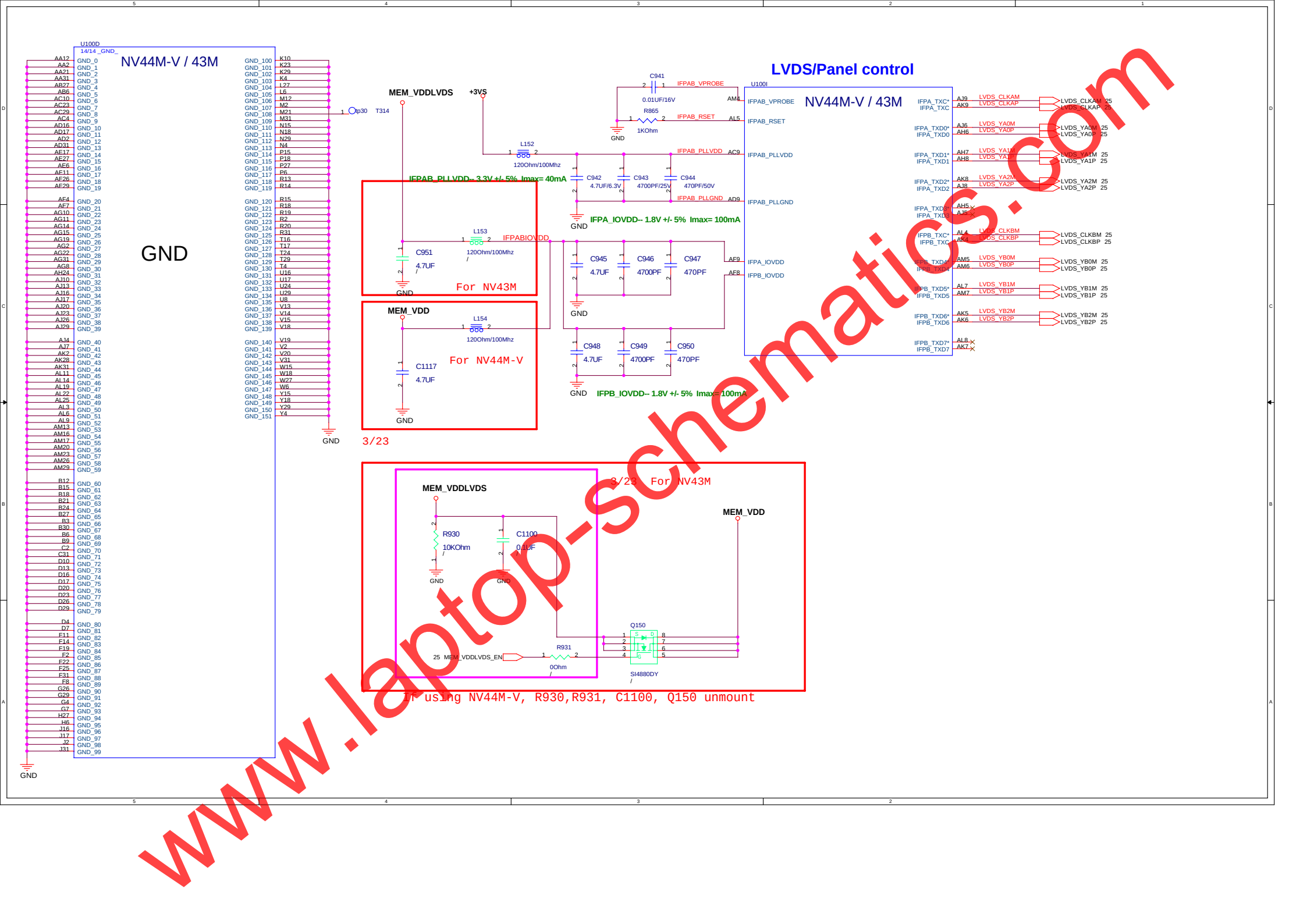
CFG19 : VTT SELECT

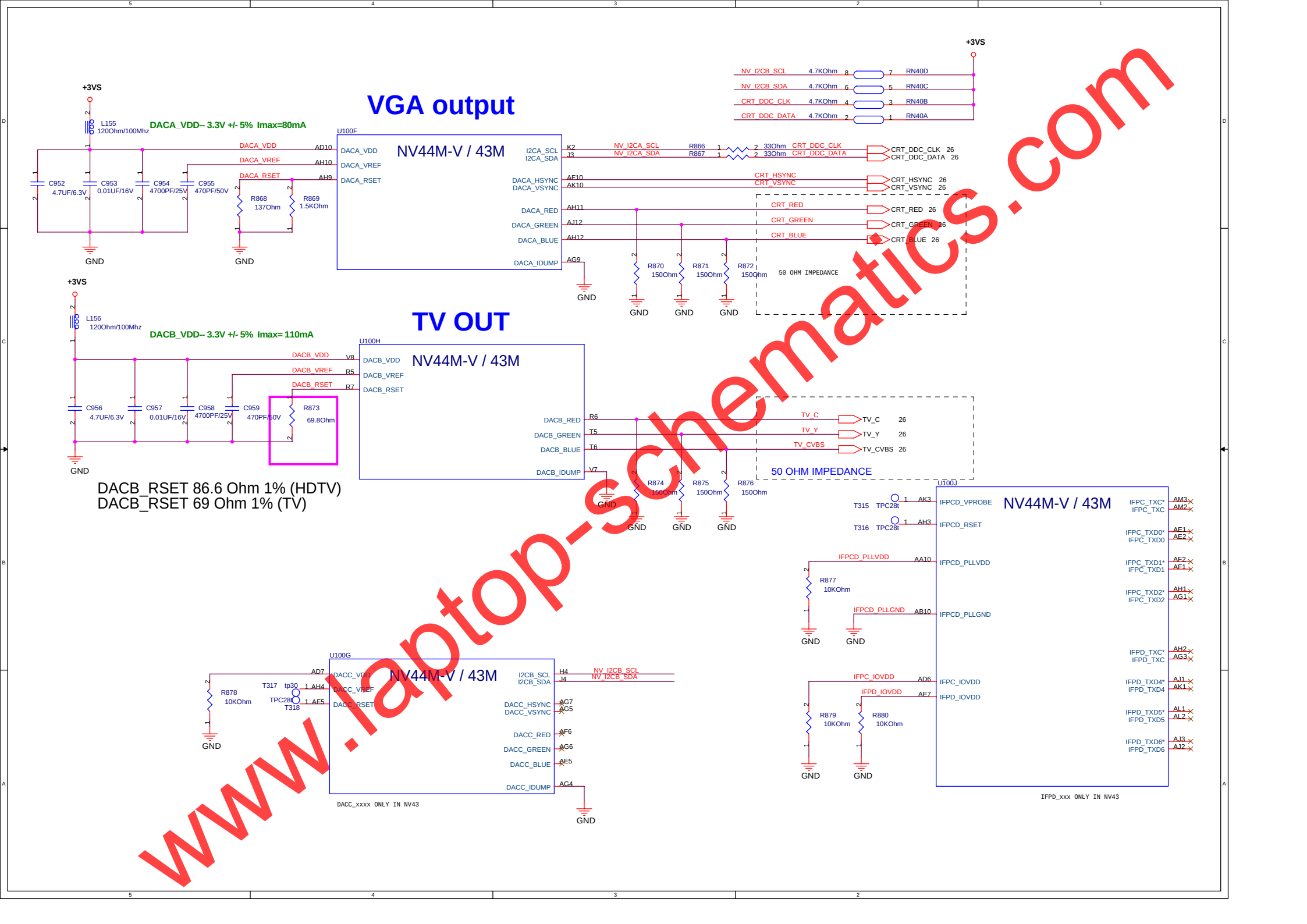
LOW = 1.05V (Default)
HIGH = 1.2V

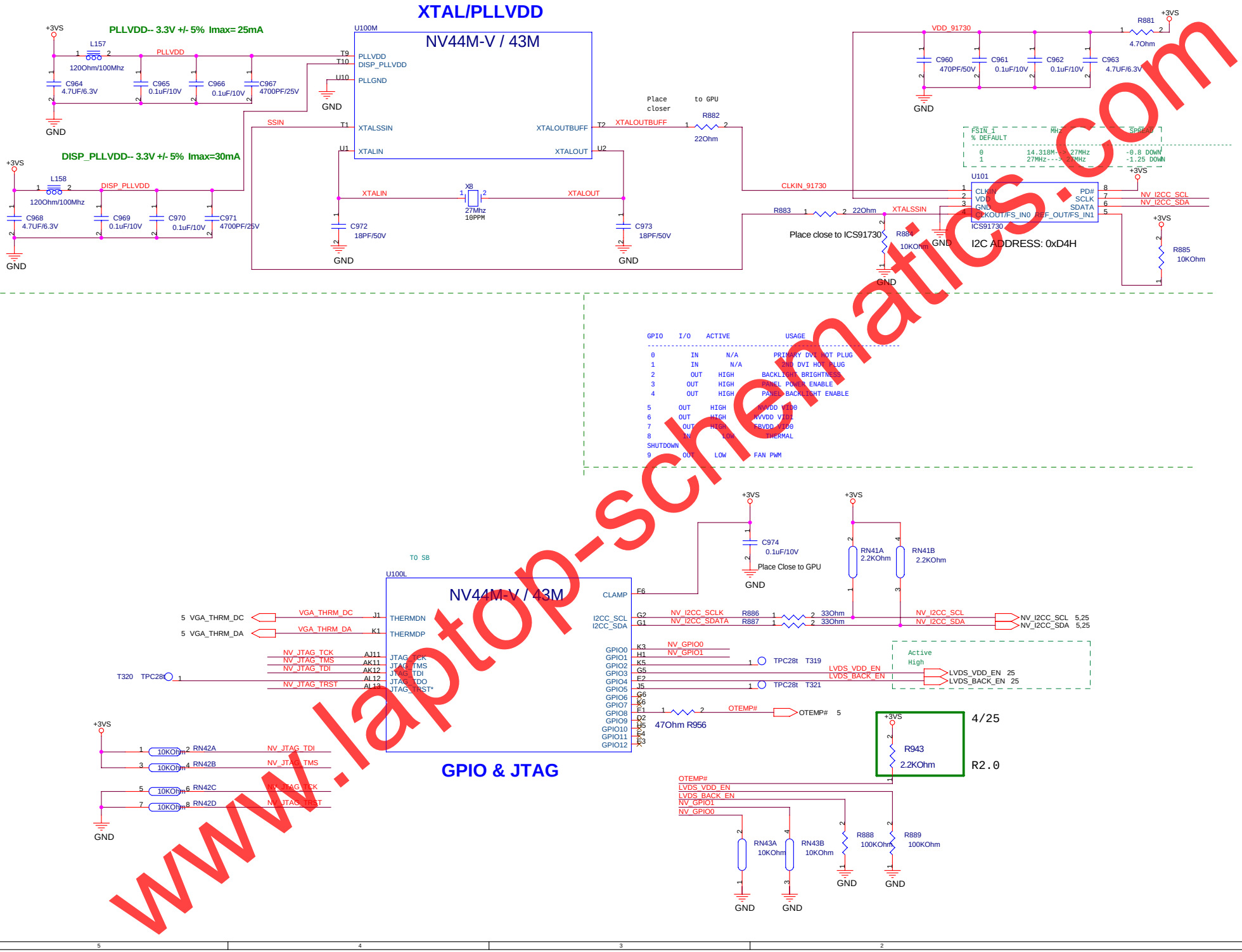


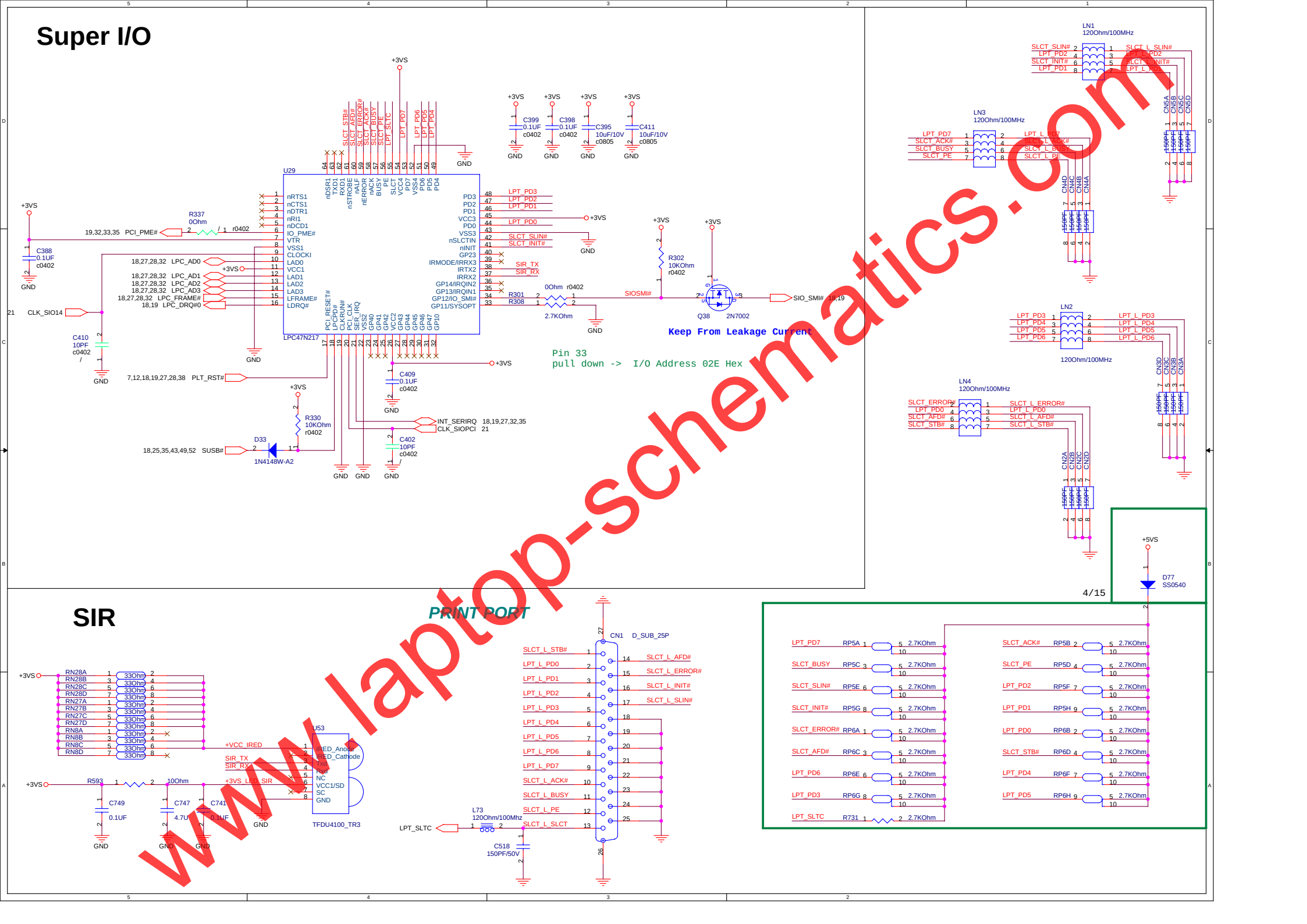


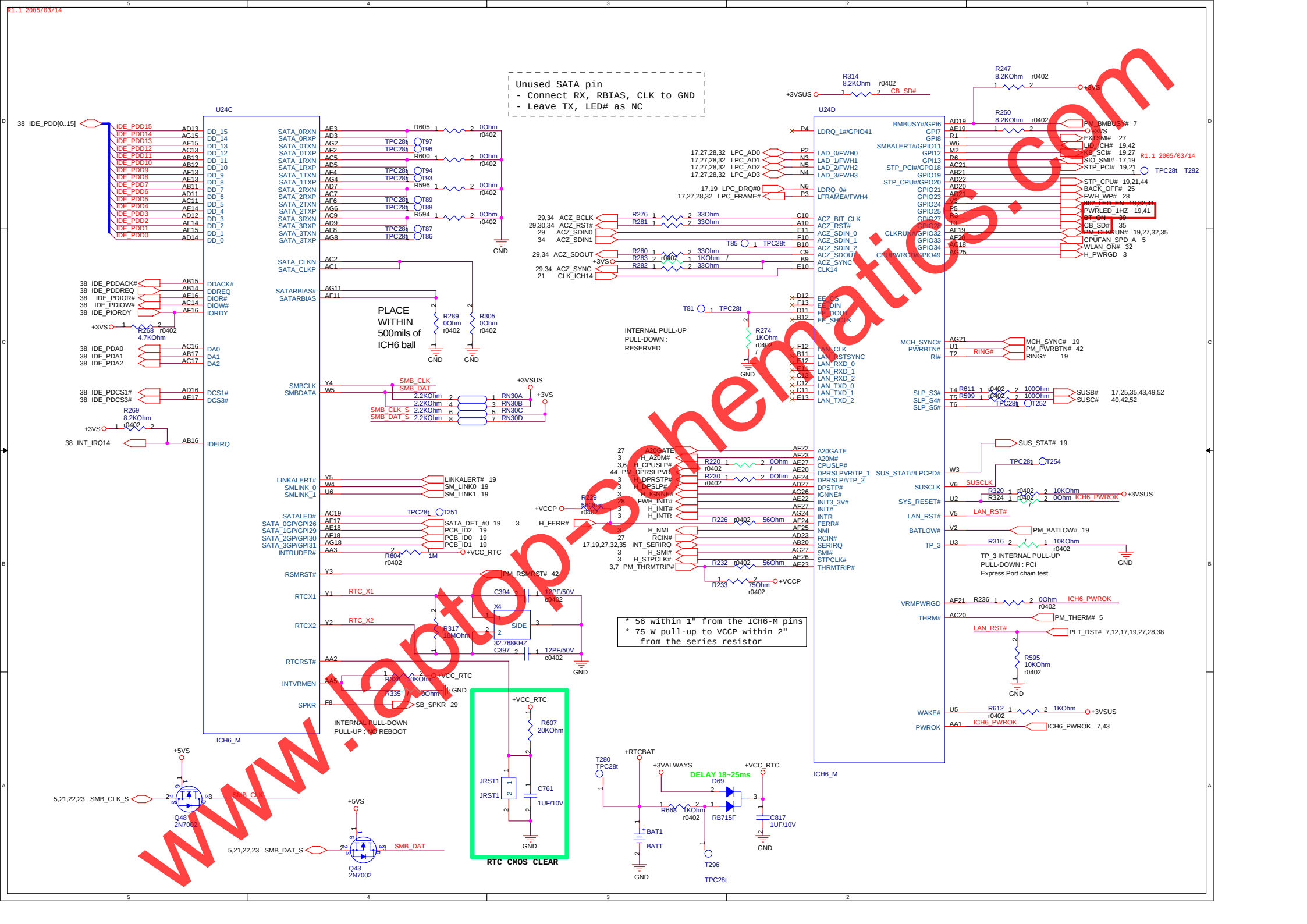




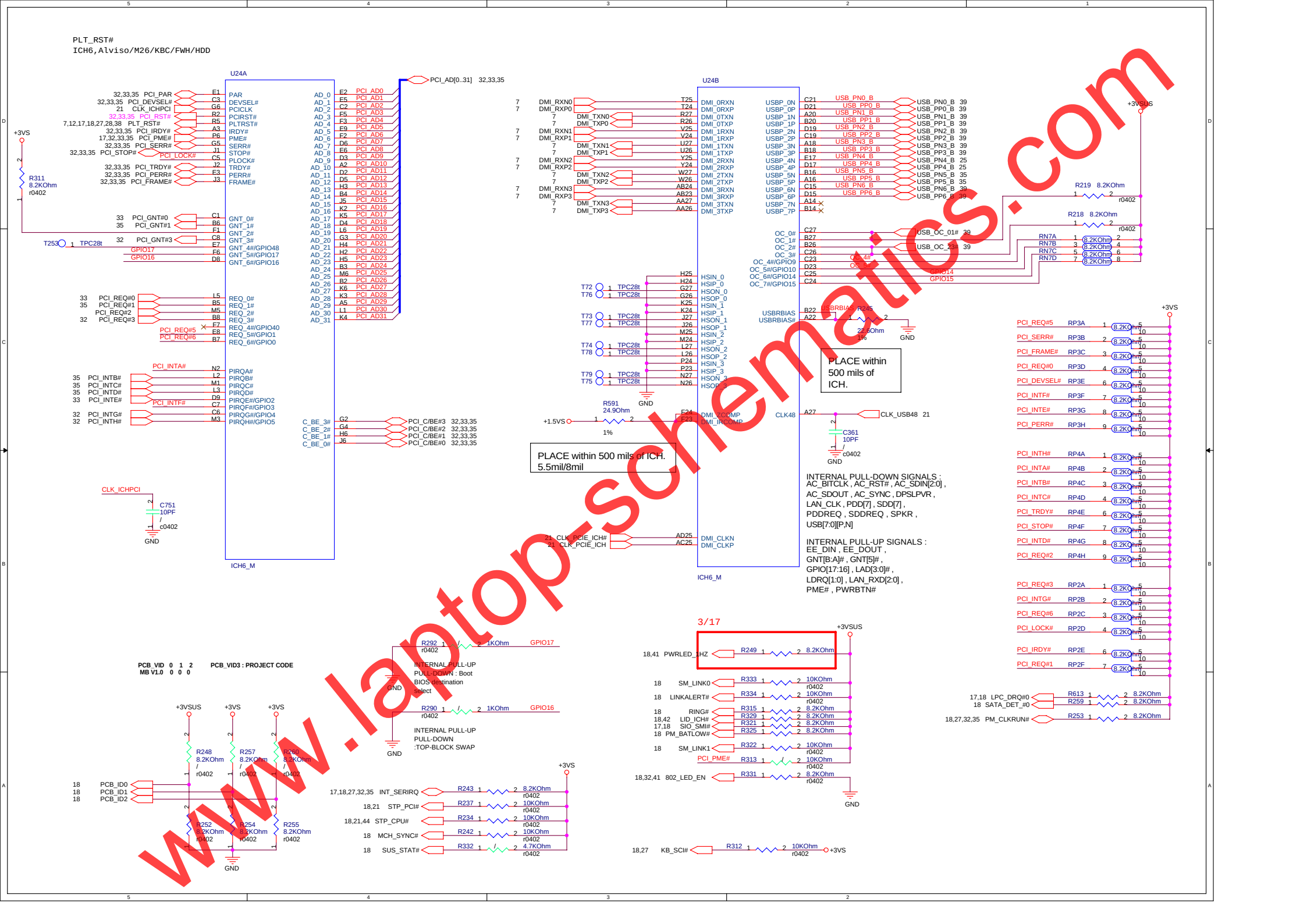

VGA output
TV OUT
NV44M-V / 43M
DACA_VDD-- 3.3V +/- 5% Imax=80mA
DACB_VDD-- 3.3V +/- 5% Imax= 110mA
DACB_RSET 86.6 Ohm 1% (HDTV)
DACB_RSET 69 Ohm 1% (TV)
50 OHM IMPEDANCE
DACC_xxxx ONLY IN NV43
IFPD_xxx ONLY IN NV43
www.laptop-schematics.com

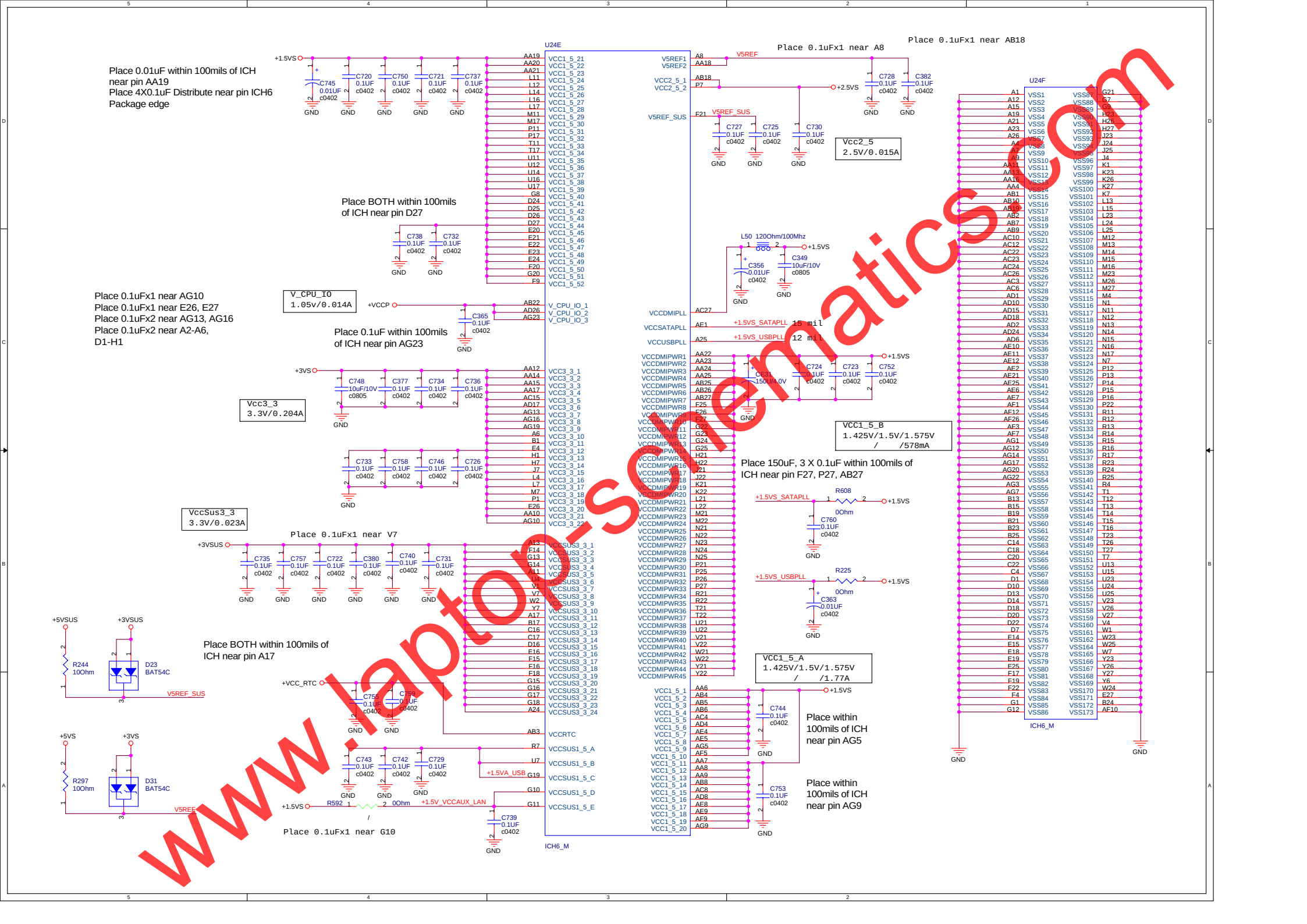


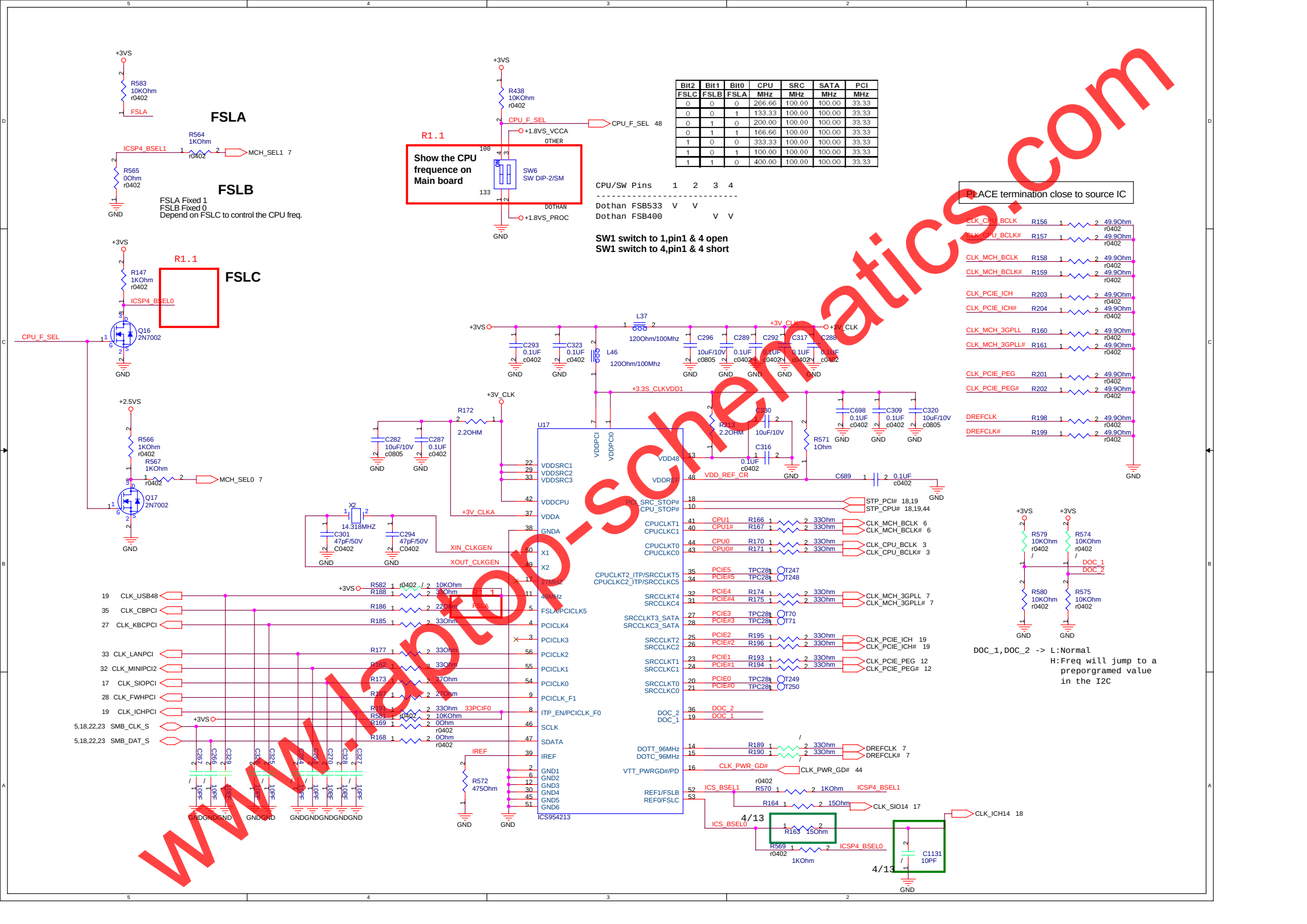



R1.1 2005/03/14
Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC
U24C
ICH6_M
U24D
ICH6_M
PLACE WITHIN 500mils of ICH6 ball
INTERNAL PULL-UP PULL-DOWN : RESERVED
INTERNAL PULL-DOWN PULL-UP : NO REBOOT
TP_3 INTERNAL PULL-UP PULL-DOWN : PCI Express Port chain test
* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2" from the series resistor
DELAY 18~25ms
RTC CMOS CLEAR
Q48 2N7002
Q43 2N7002
www.laptop-schematics.com

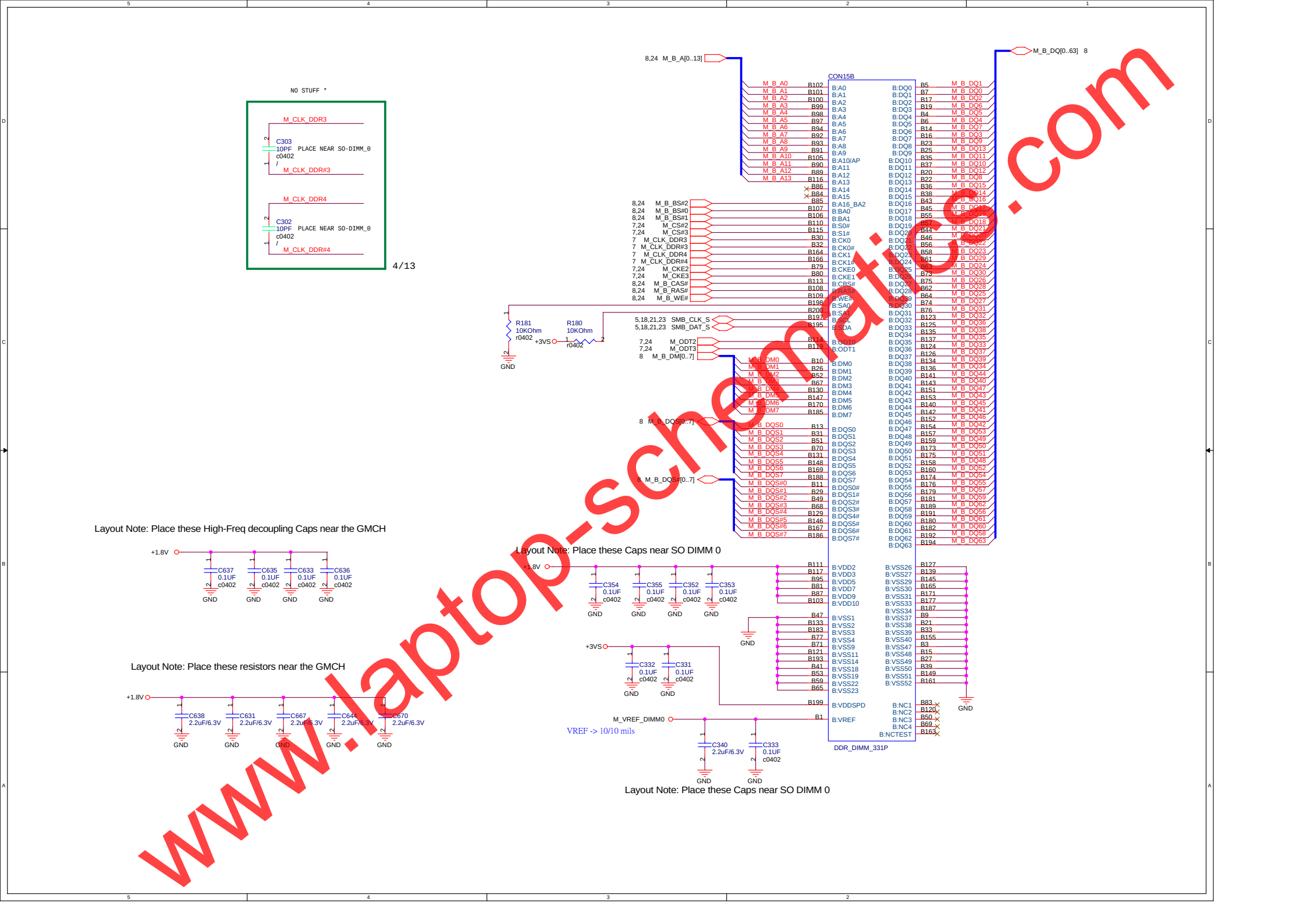
PLT_RST#
ICH6,Alviso/M26/KBC/FWH/HDD

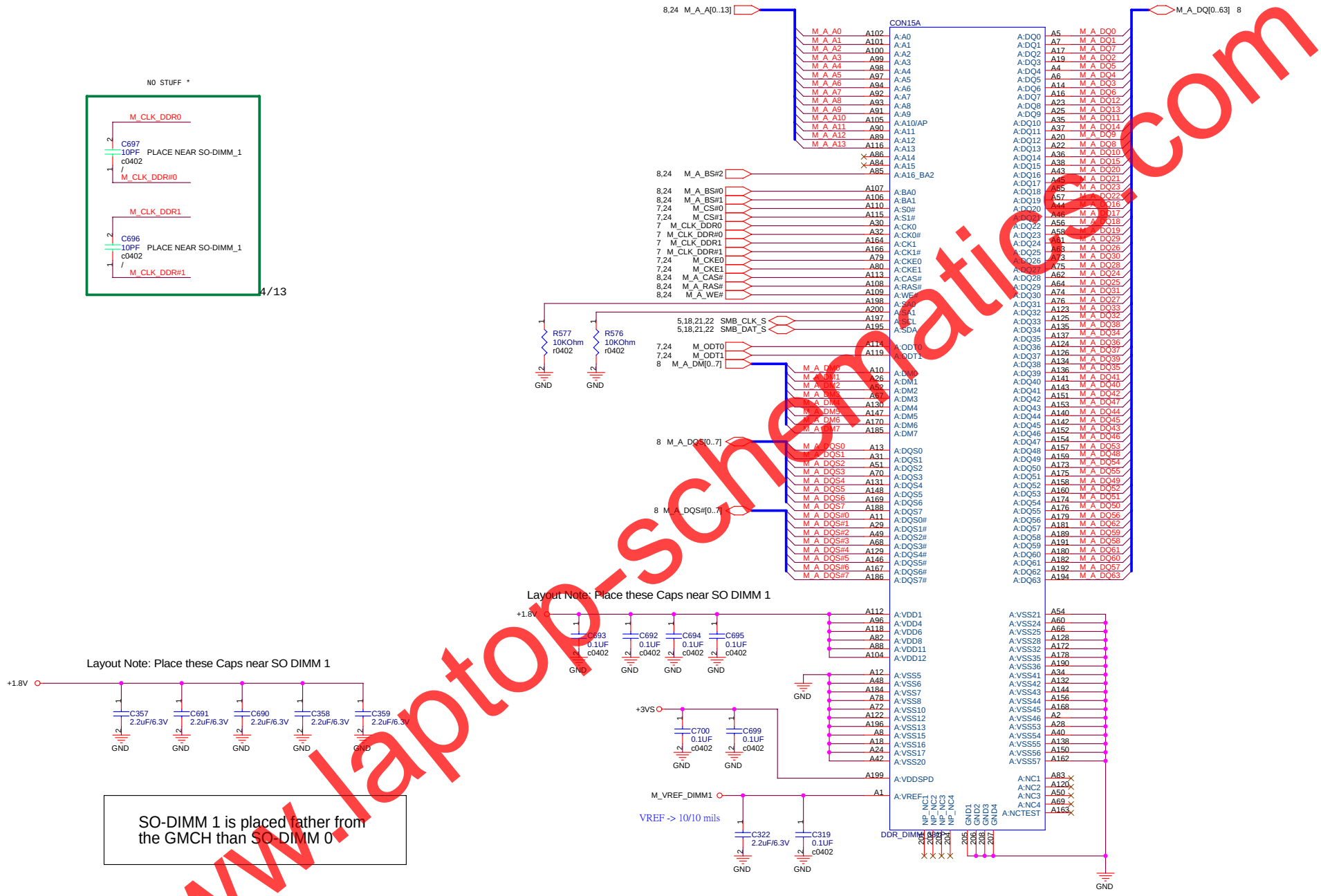


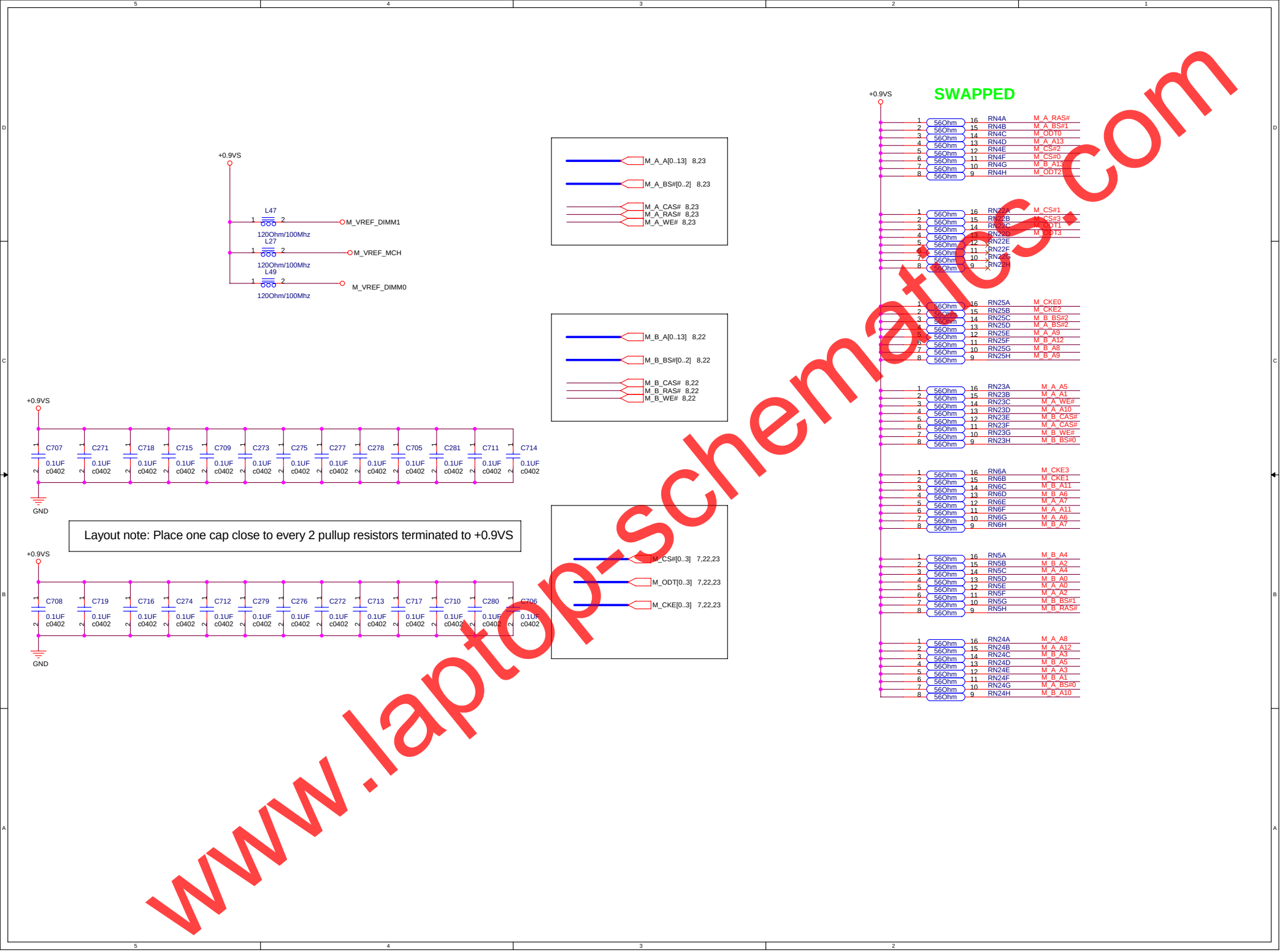

Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1
V_CPU_IO 1.05v/0.014A
Place 0.1uF within 100mils of ICH near pin AG23
Vcc3_3 3.3V/0.204A
VccSus3_3 3.3V/0.023A
Place 0.1uFx1 near V7
Place BOTH within 100mils of ICH near pin A17
Place 0.1uFx1 near G10
Place 0.1uFx1 near A8
Place 0.1uFx1 near AB18
Vcc2_5 2.5V/0.015A
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
VCC1_5_B 1.425V/1.5V/1.575V / /578mA
VCC1_5_A 1.425V/1.5V/1.575V / /1.77A
Place within 100mils of ICH near pin AG5
Place within 100mils of ICH near pin AG9
U24E
U24F
ICH6_M
www.laptop-schematics.com



Bit2	Bit1	Bit0	CPU	SRC	SATA	PCI
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	266.66	100.00	100.00	33.33
0	0	1	133.33	100.00	100.00	33.33
0	1	0	200.00	100.00	100.00	33.33
0	1	1	166.66	100.00	100.00	33.33
1	0	0	333.33	100.00	100.00	33.33
1	0	1	100.00	100.00	100.00	33.33
1	1	0	400.00	100.00	100.00	33.33

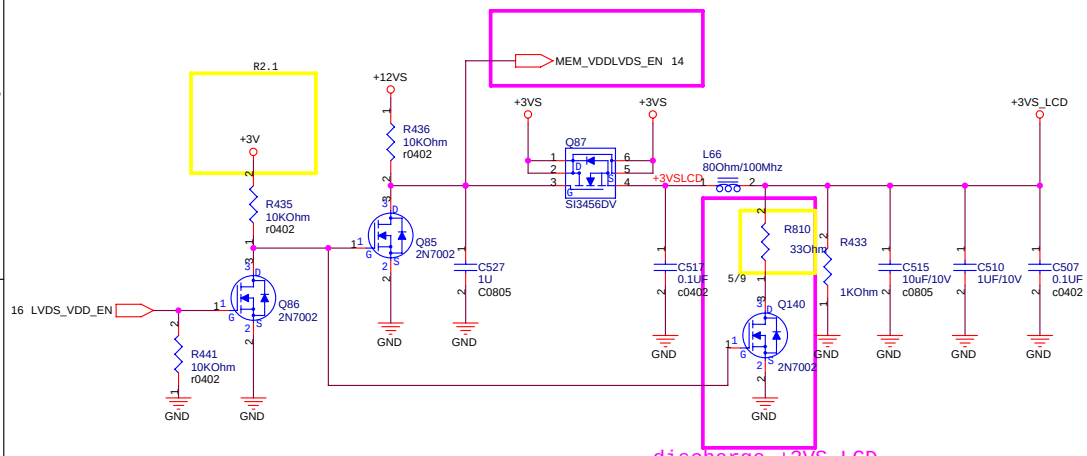






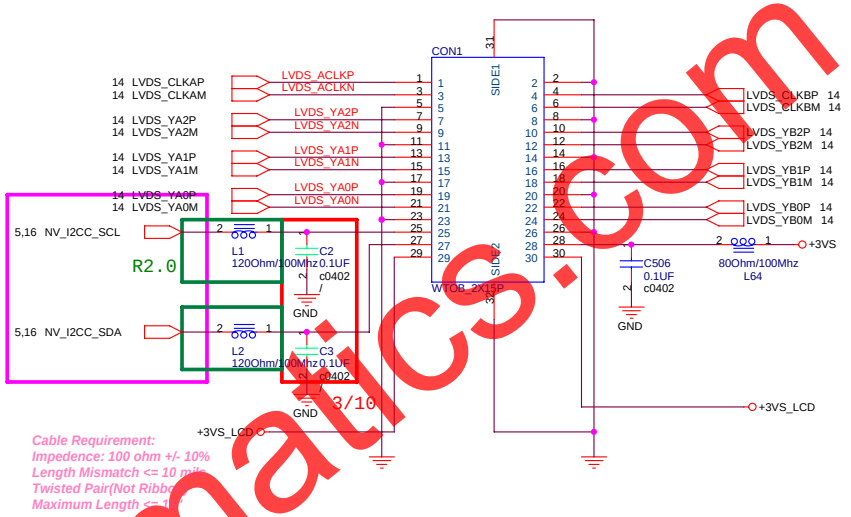
LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)



discharge +3VS_LCD

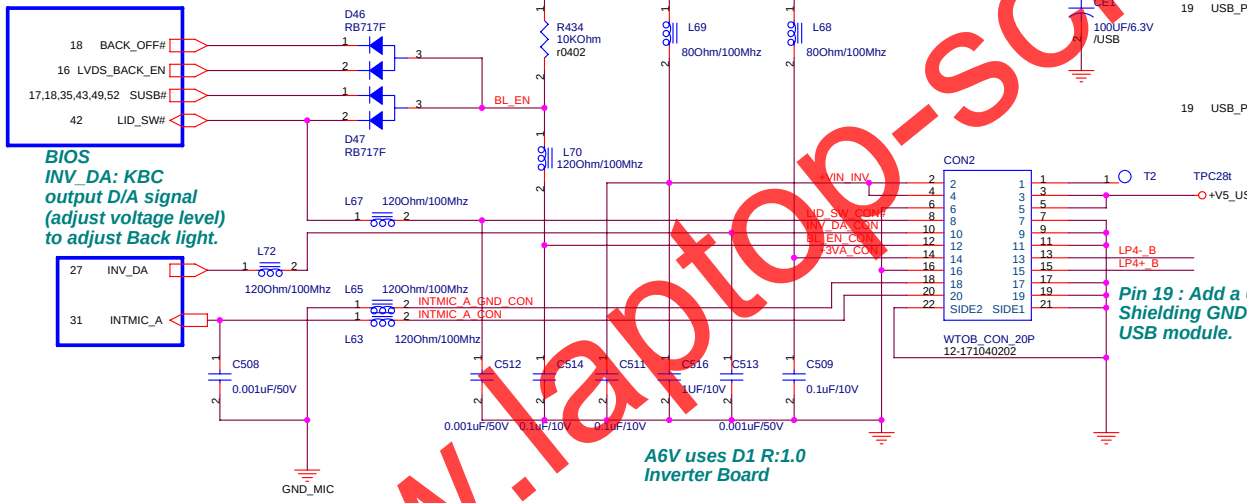
LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 14"

INVERTER Interface

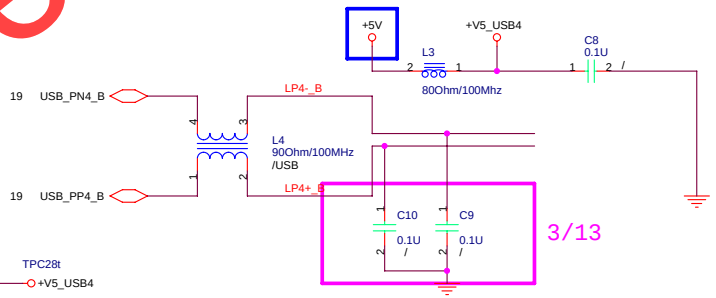
BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.



BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

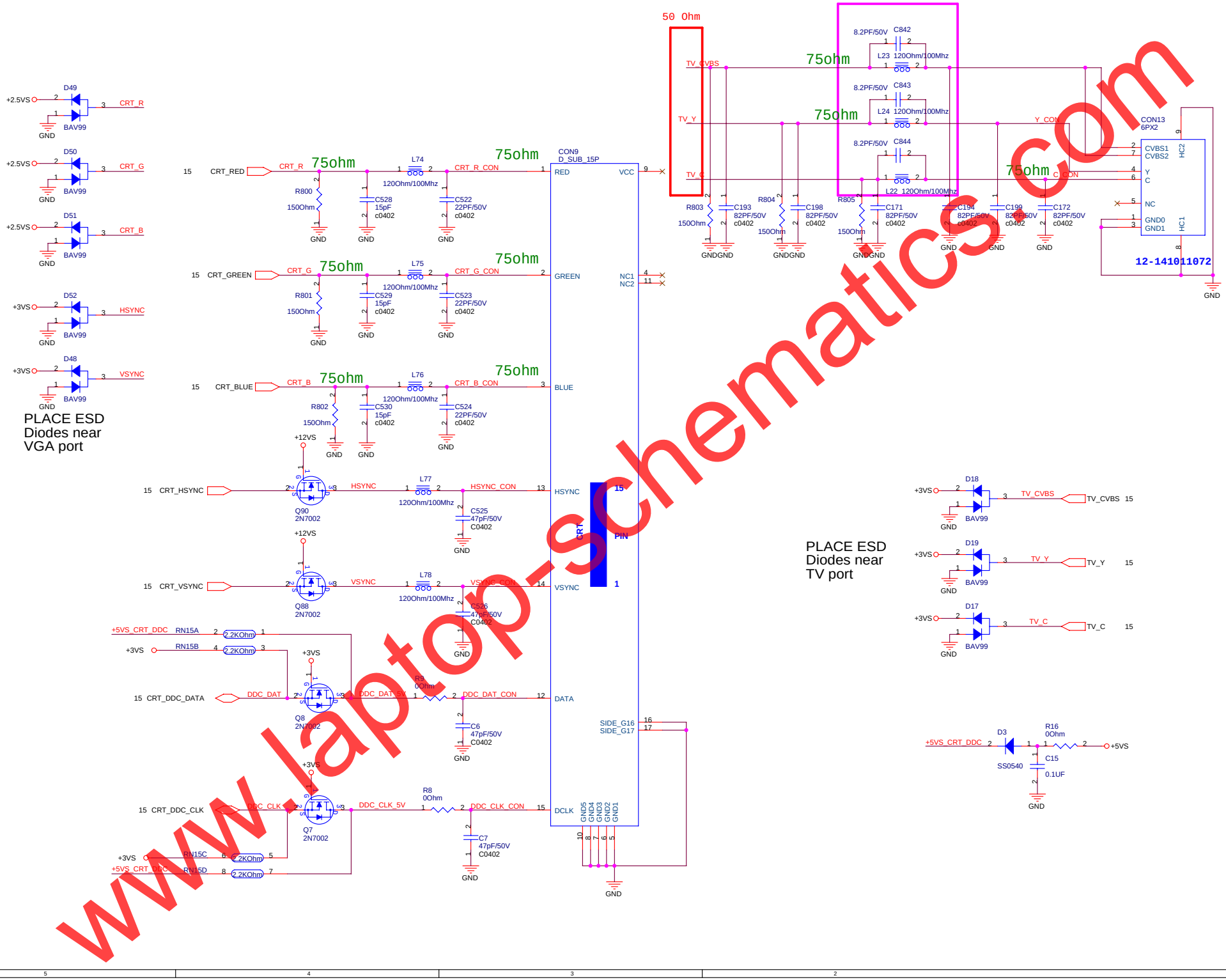
A6V uses D1 R:1.0 Inverter Board

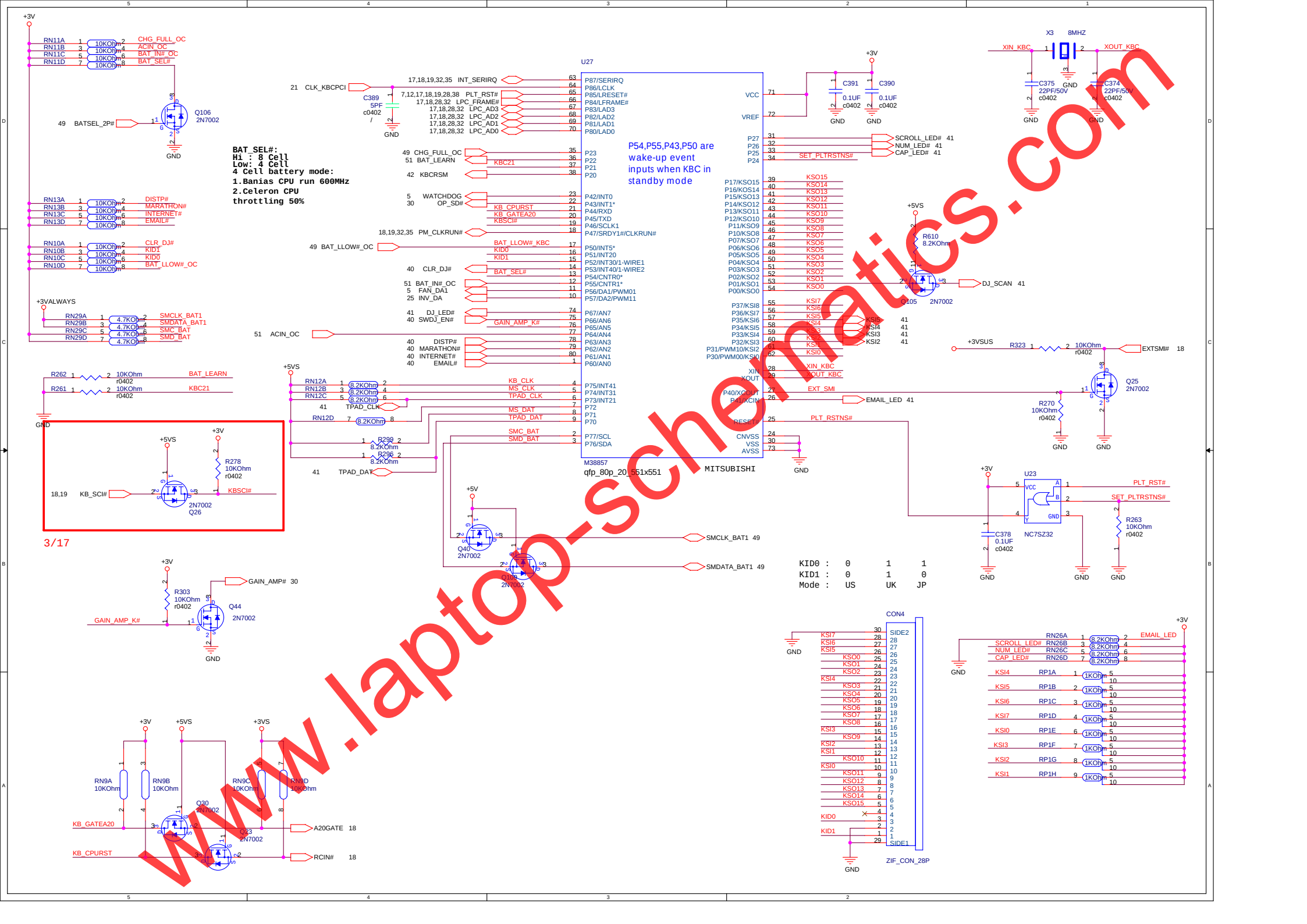
Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



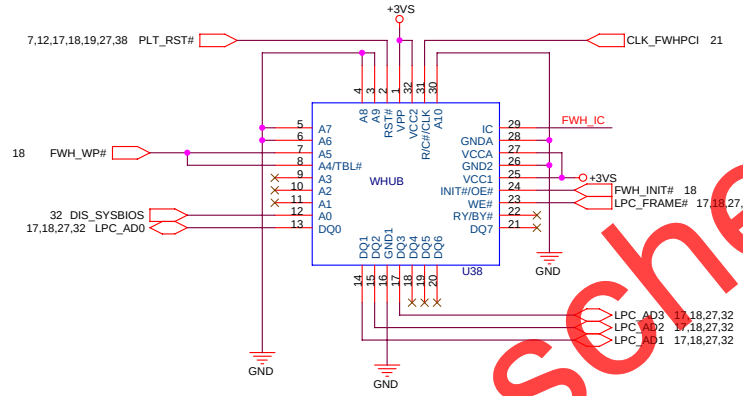
USB PORT 4 for USB CAMERA

A6V doesn't support USB WLAN function!


50 Ohm
75ohm
CON9
D_SUB_15P
CON13
6PX2
12-141011072
PLACE ESD
Diodes near
VGA port
PLACE ESD
Diodes near
TV port
CRT
PIN
15
1
www.laptop-schematics.com

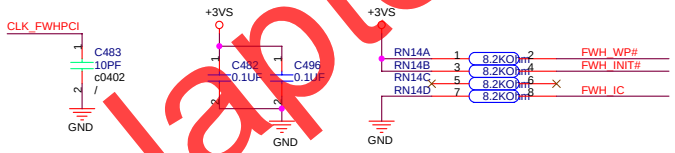

BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
U27
M38857
qfp_80p_20_551x551
MITSUBISHI
3/17
KID0 : 0 1 1
KID1 : 0 1 0
Mode : US UK JP
X3 8MHZ
CON4
ZIF_CON_28P
www.laptop-schematics.com

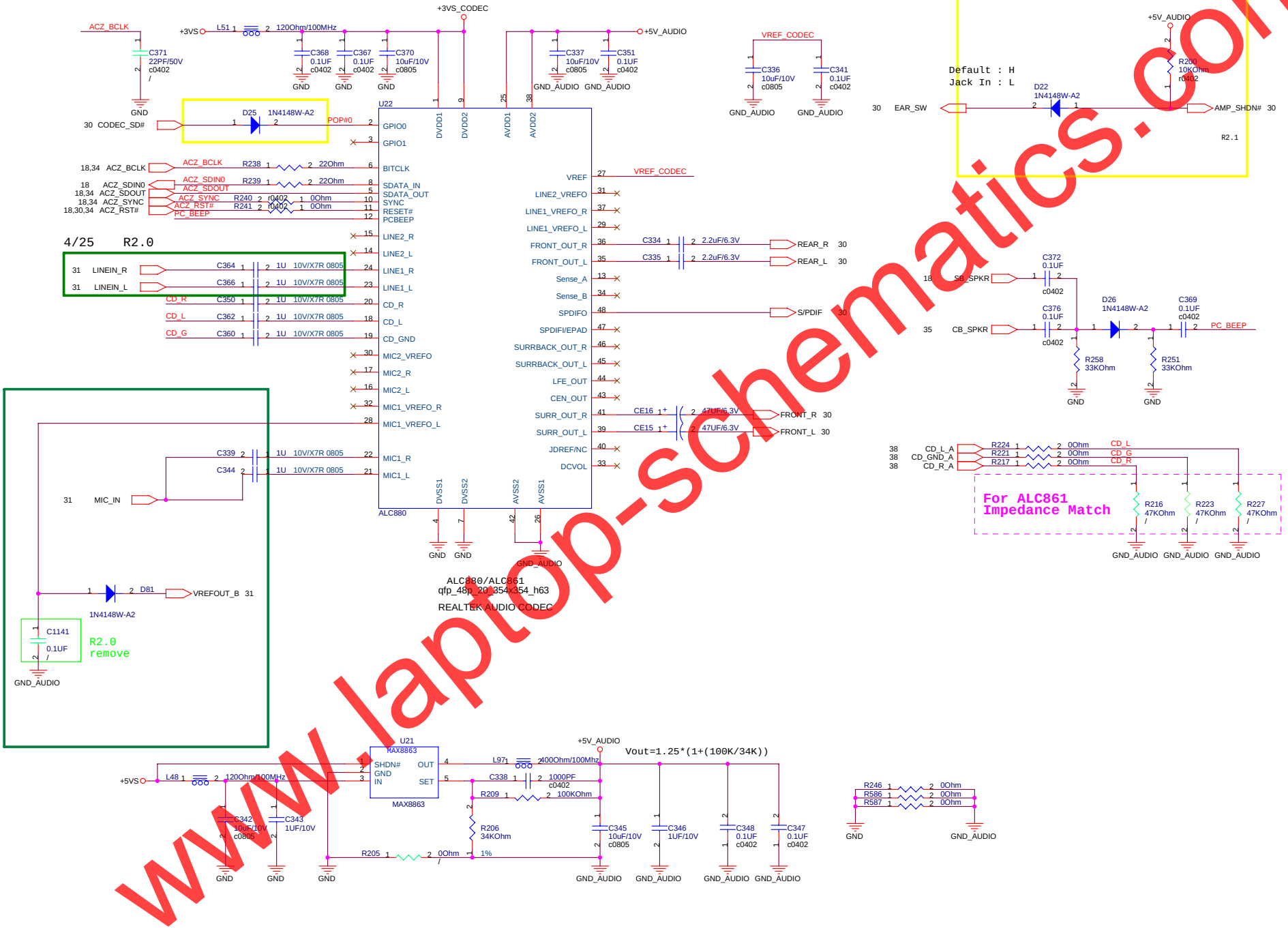
FWH

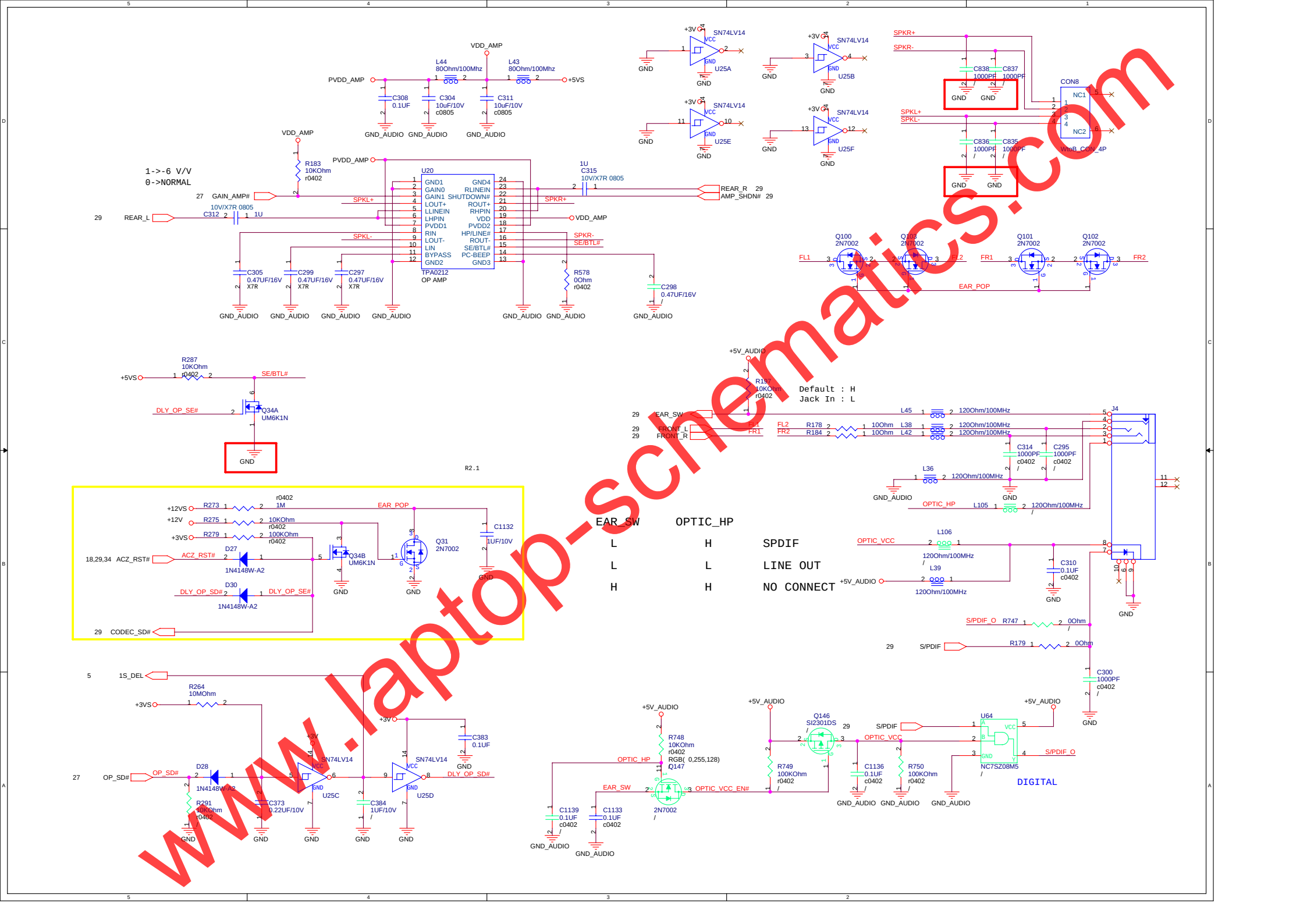


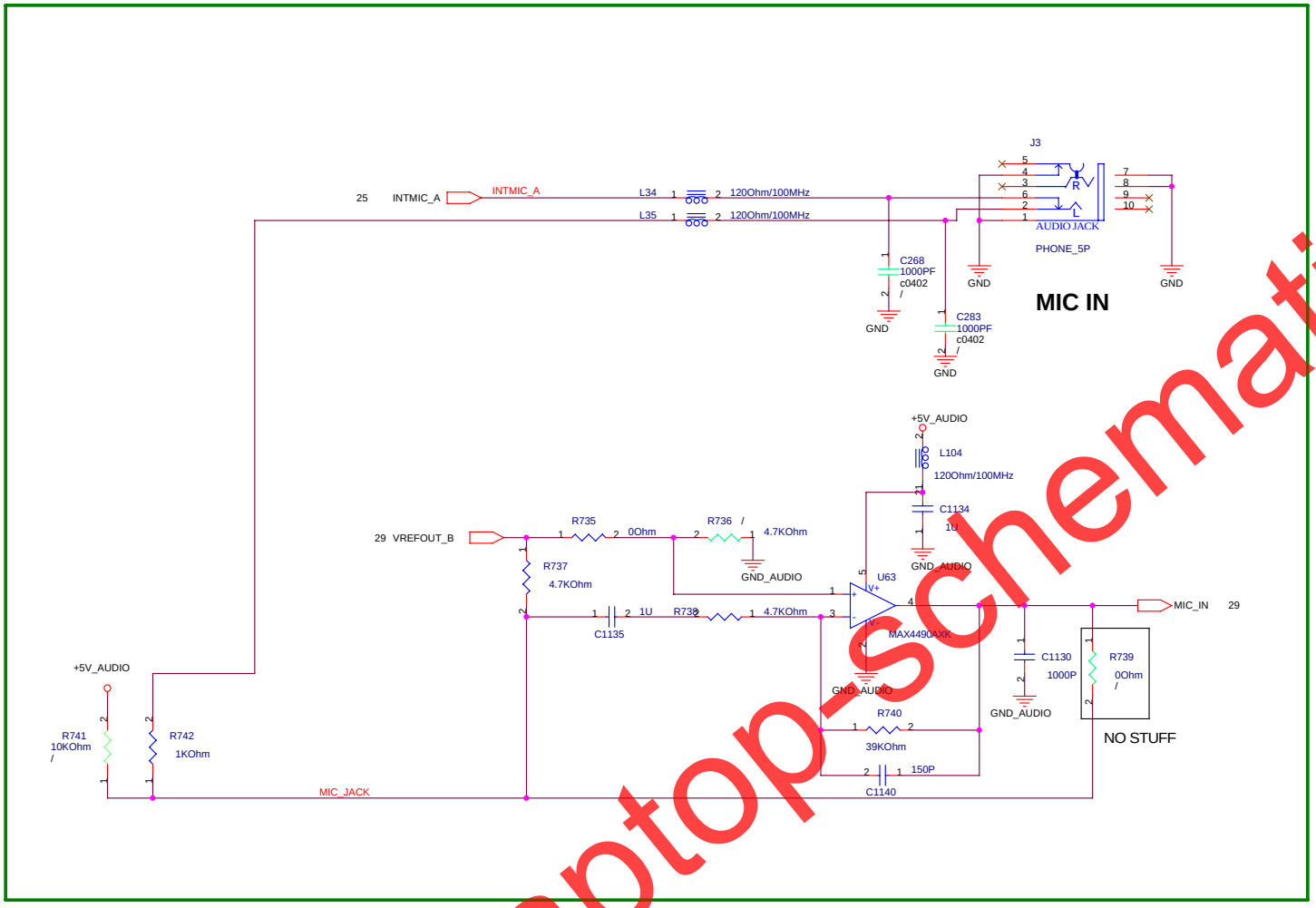
PLCC32 Socket Part Number :
12-043000321

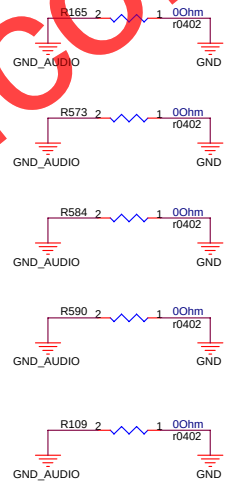
SST FWH/LPC Part Number :
05-001017122(燒)

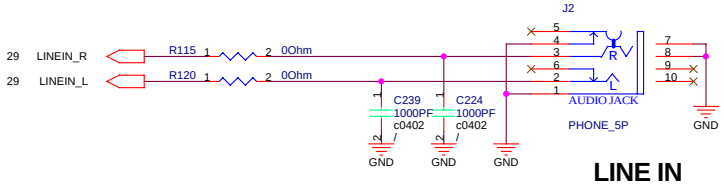




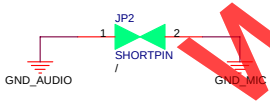


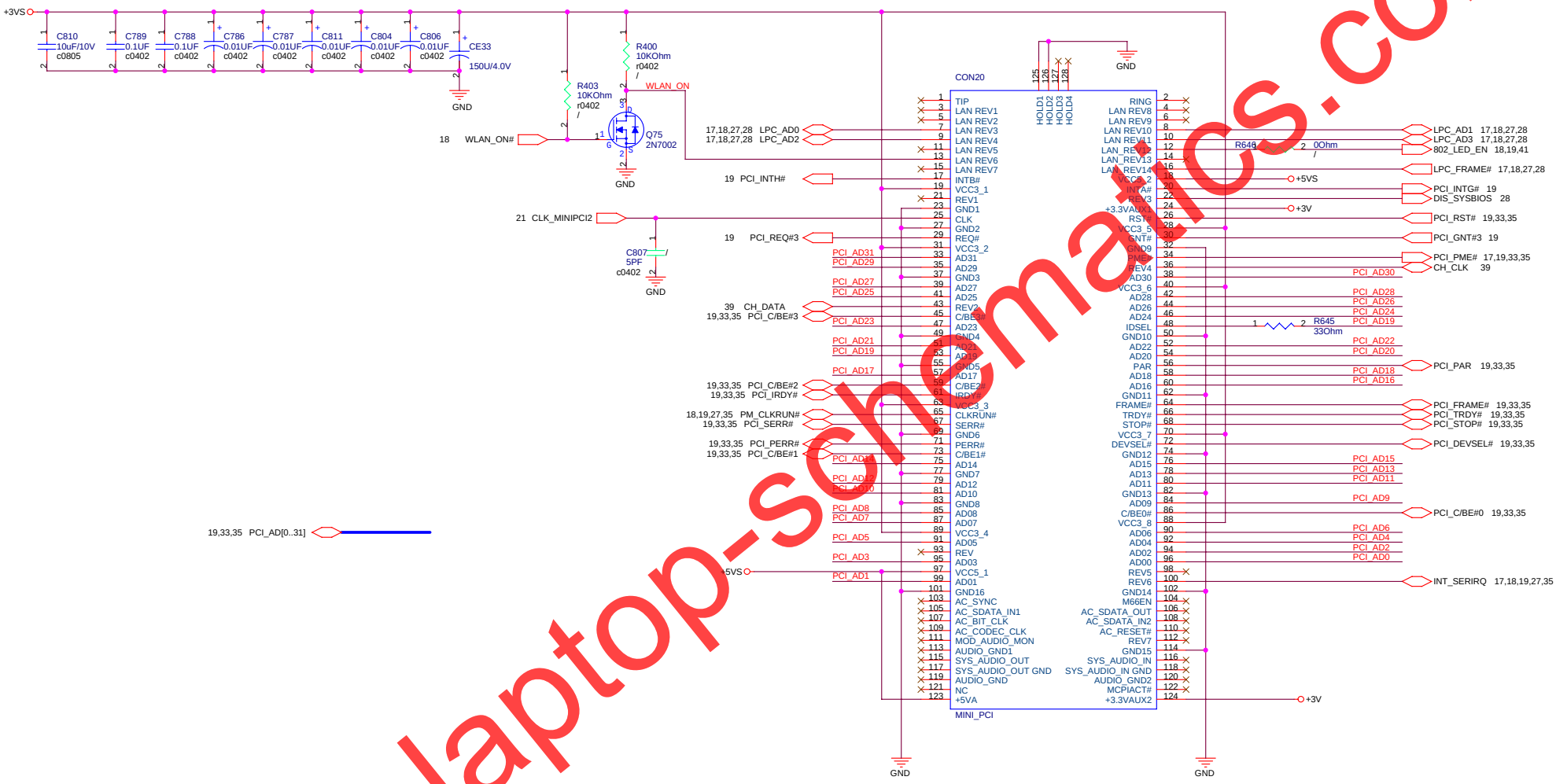


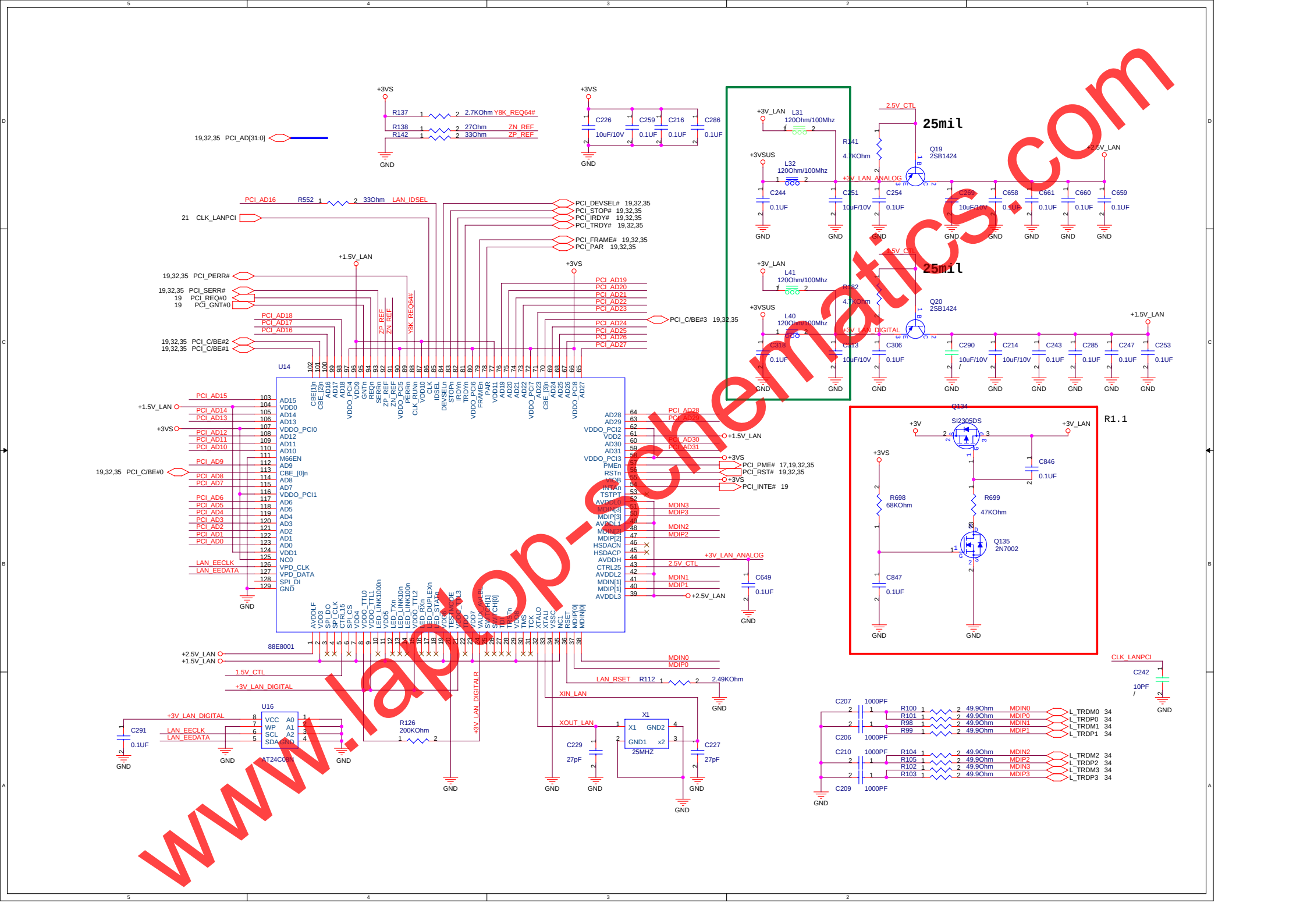


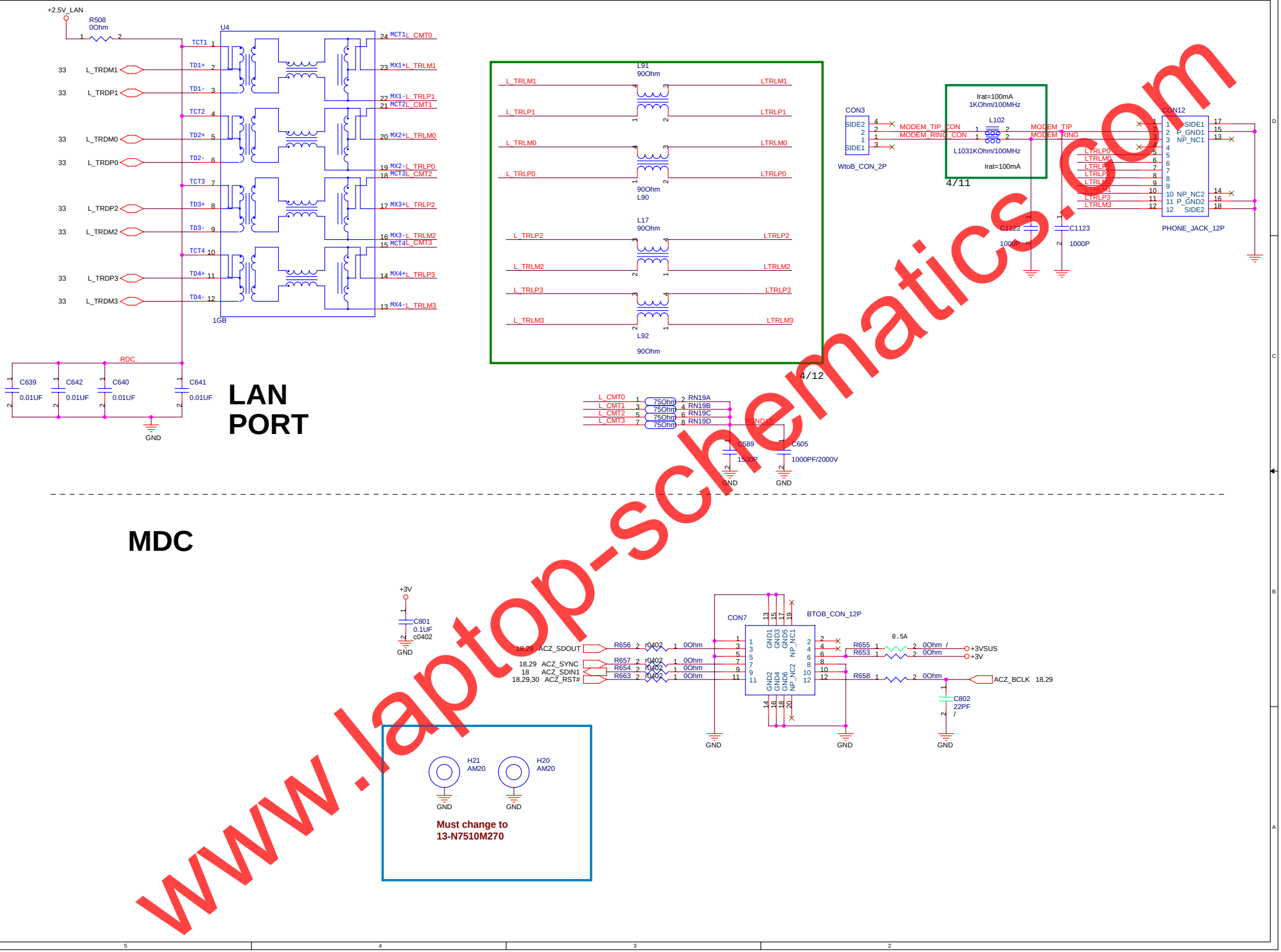


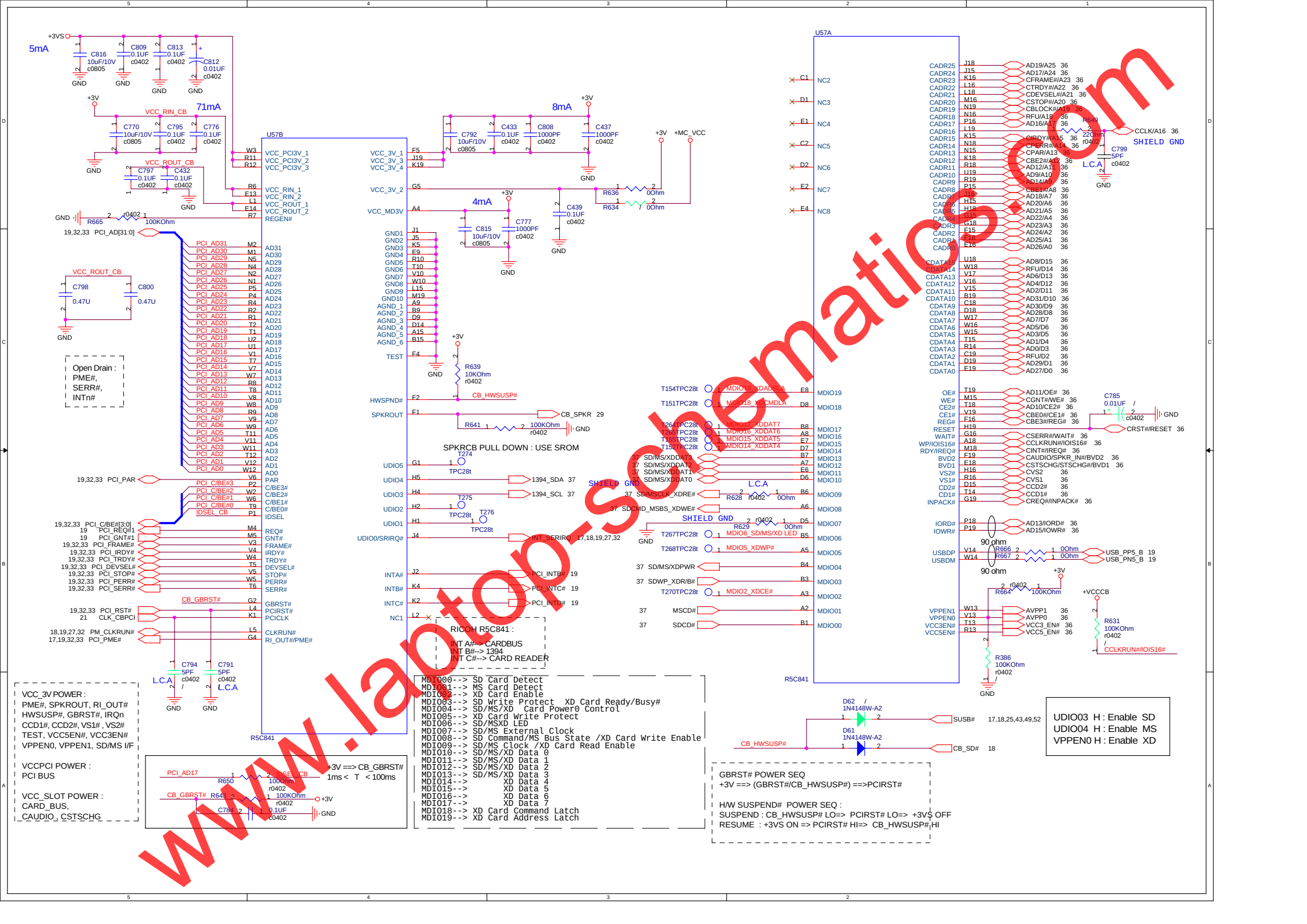
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

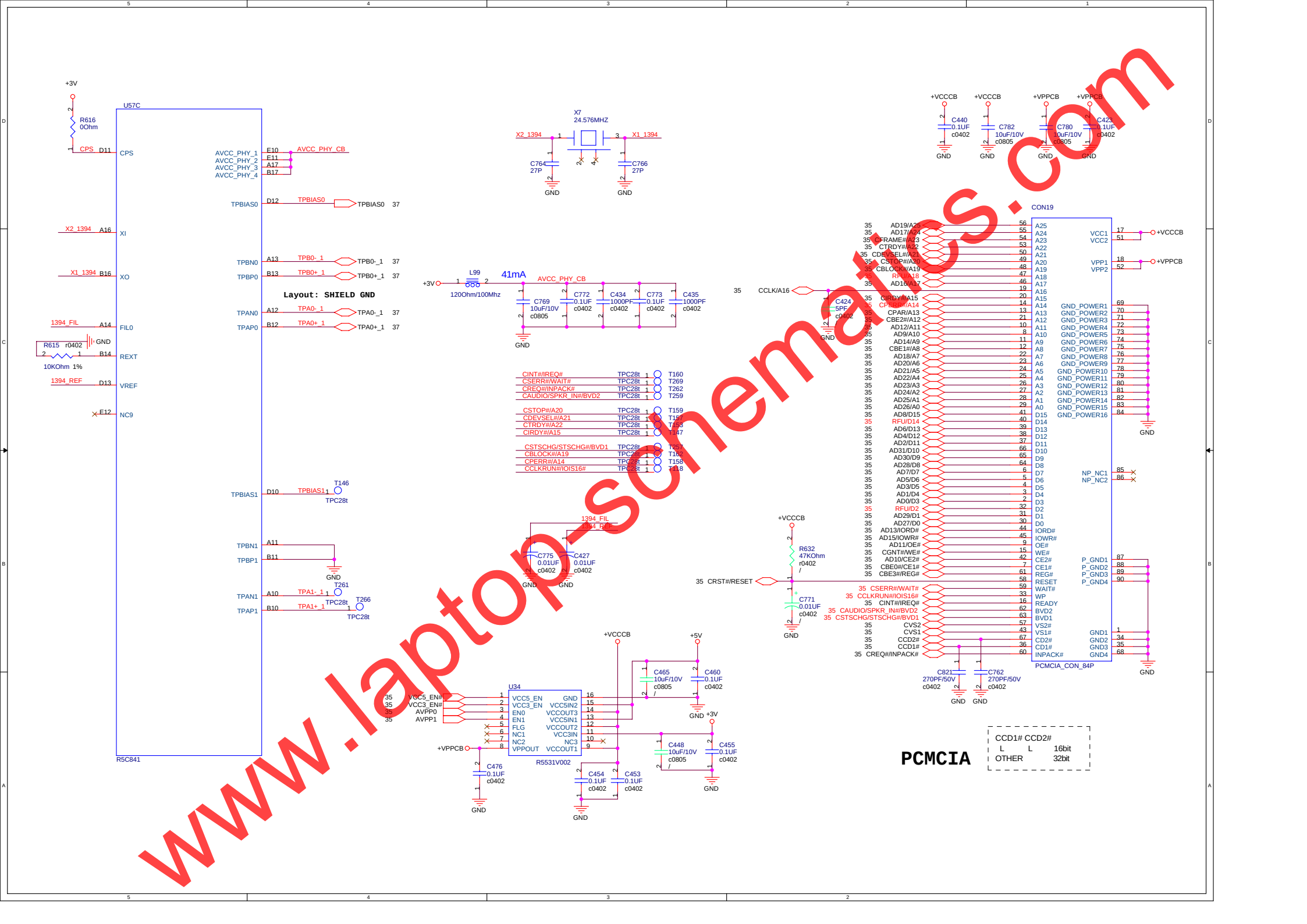


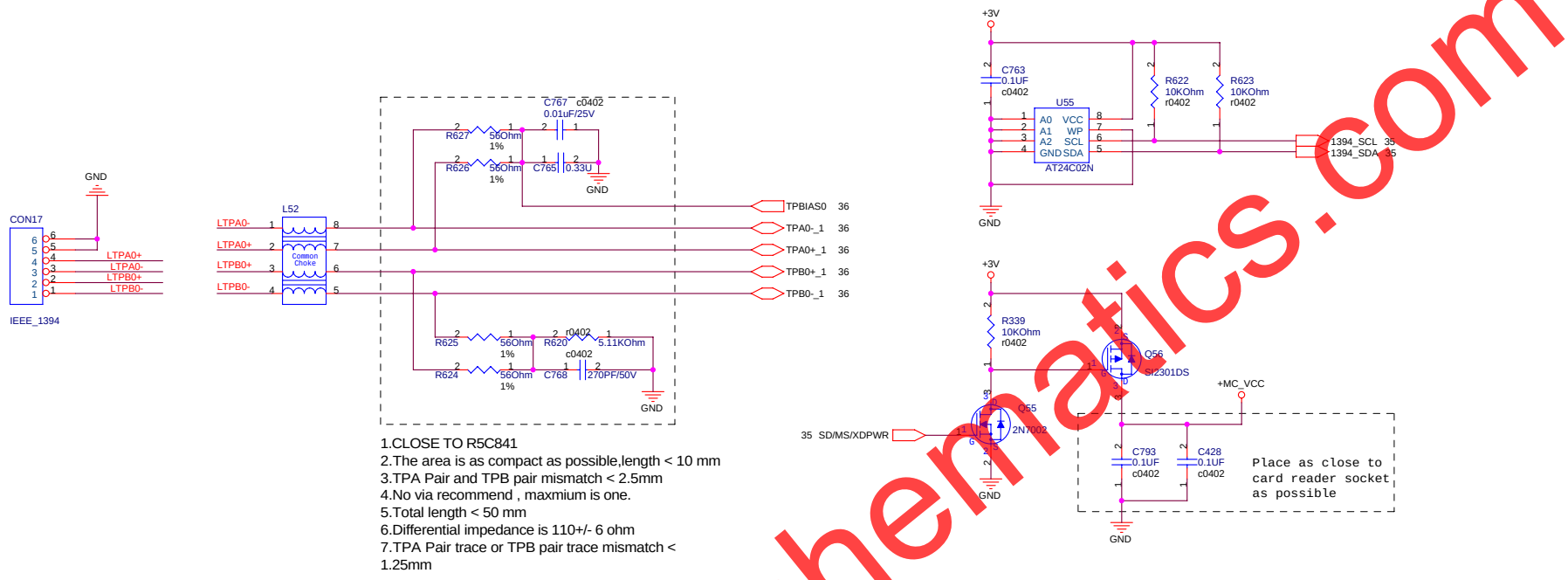




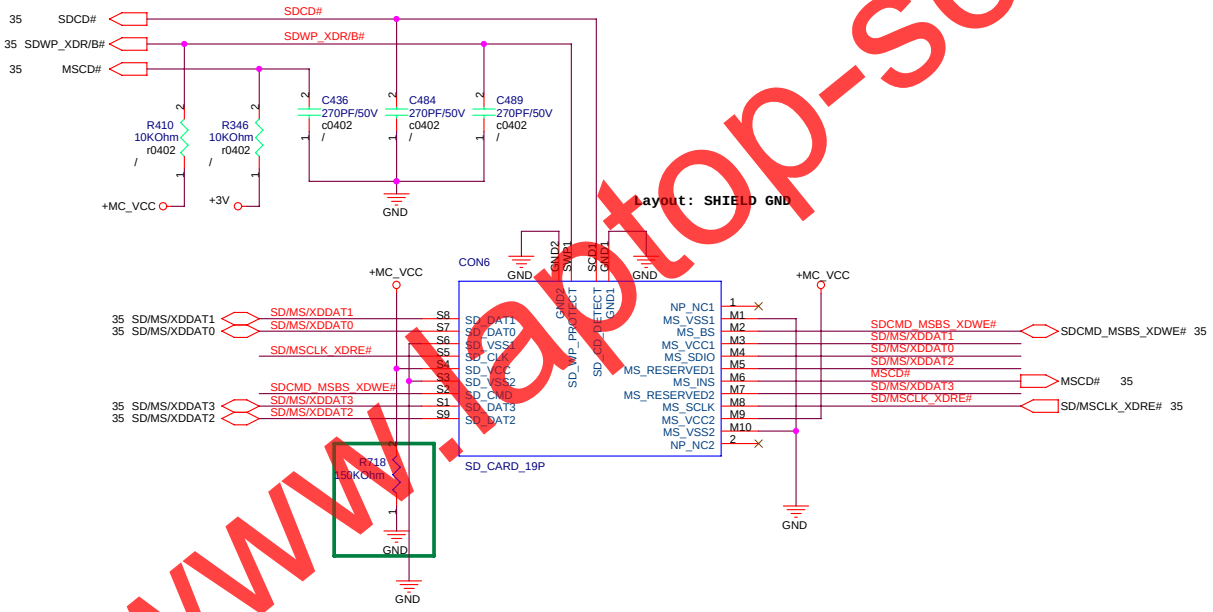


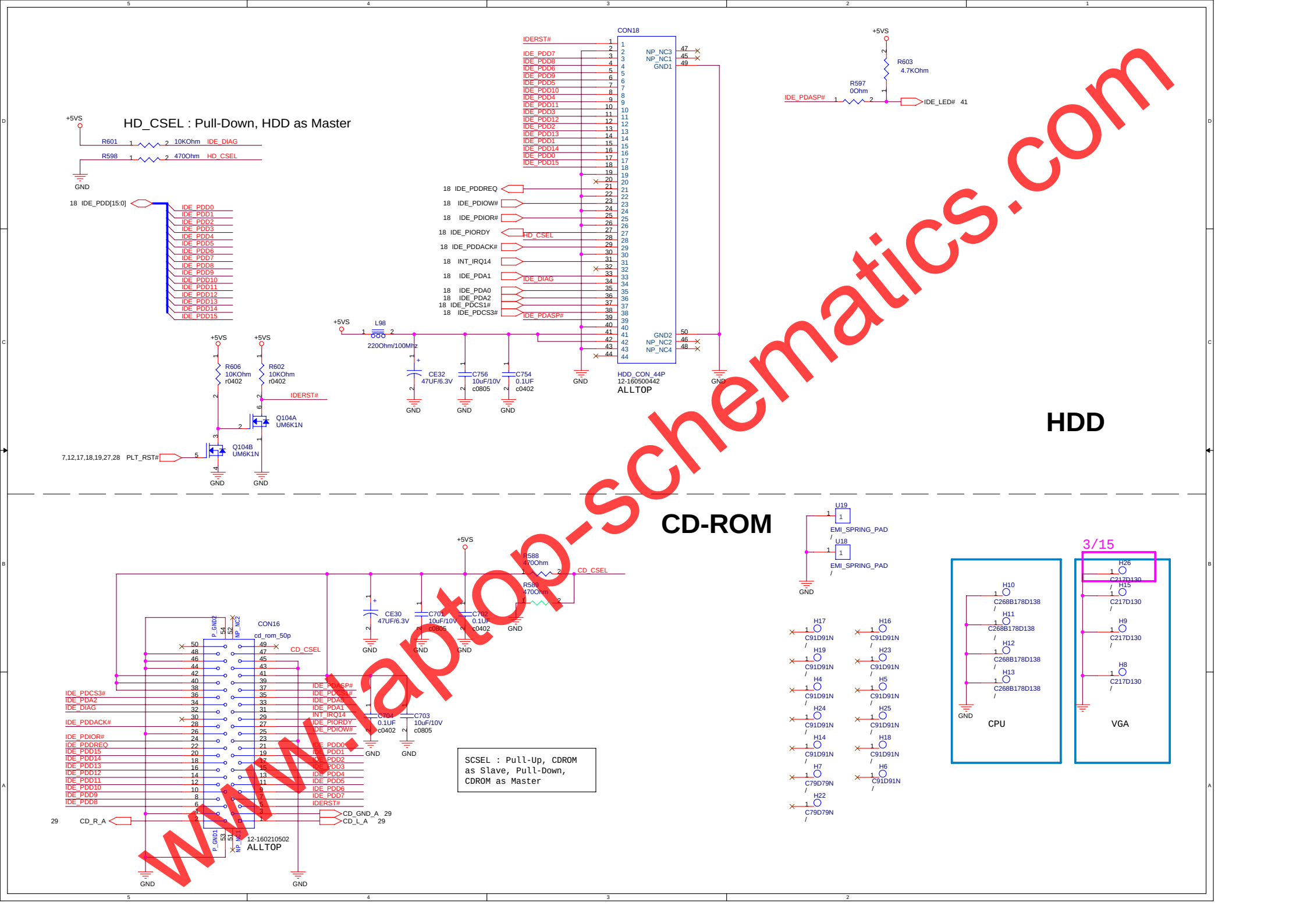

5mA
71mA
8mA
4mA
U57B
U57A
R5C841
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms< T <100ms
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP#,HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
SHIELD GND
L.C.A
www.laptop-schematics.com


U57C
R5C841
Layout: SHIELD GND
X7
24.576MHZ
L99
120Ohm/100Mhz
41mA
U34
R5531V002
CON19
PCMCIA_CON_84P
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
www.laptop-schematics.com

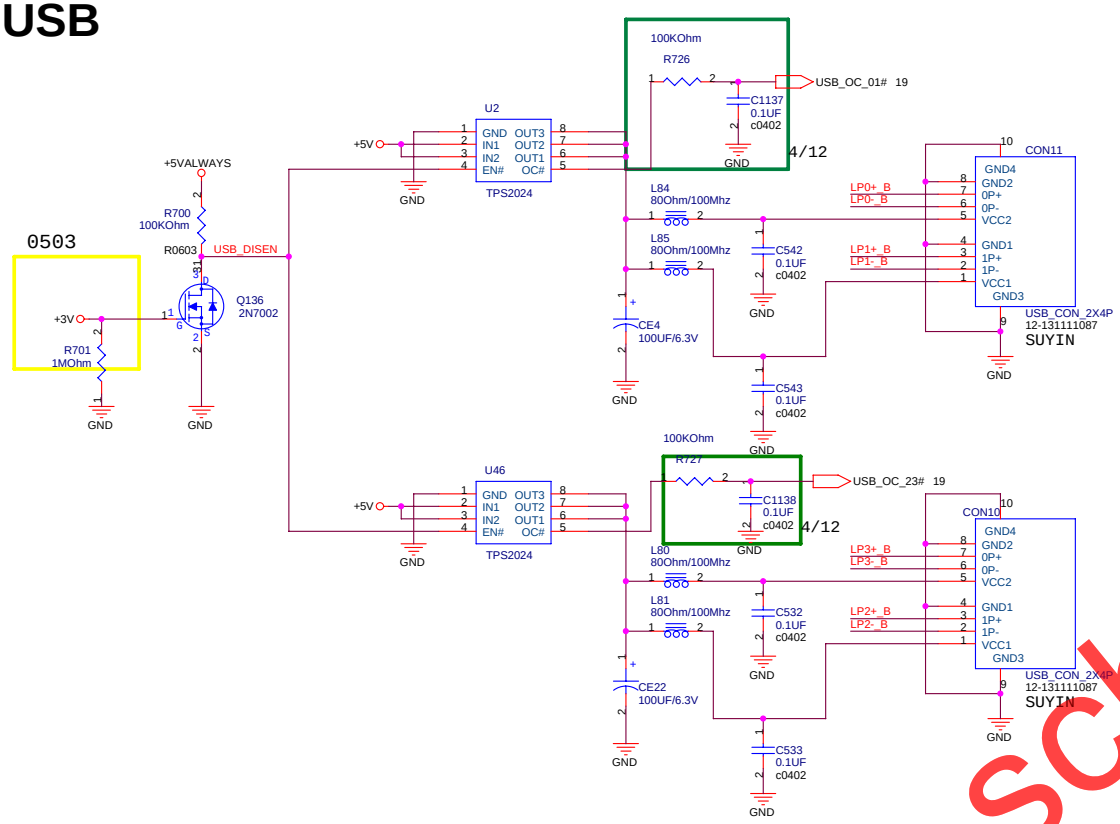


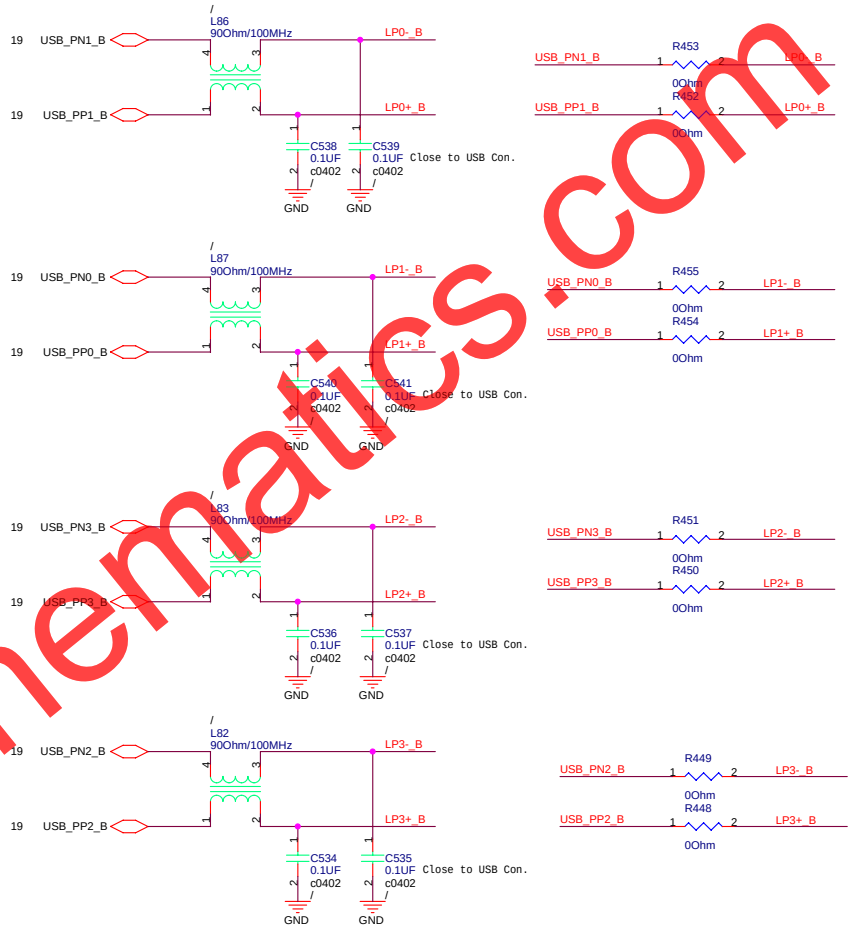
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm



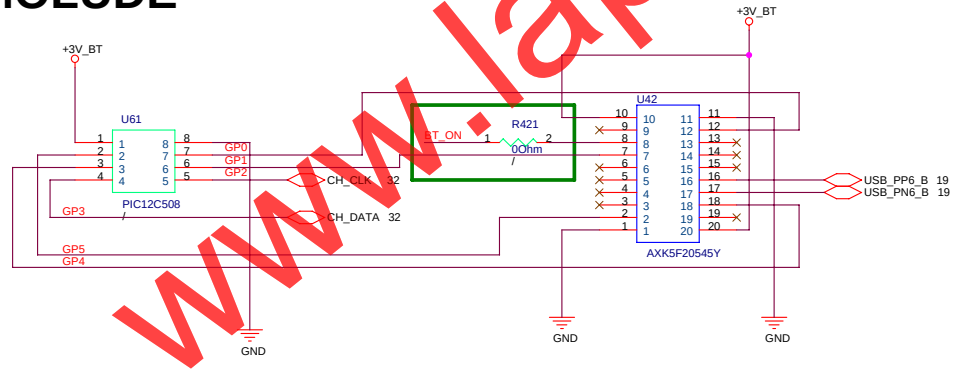


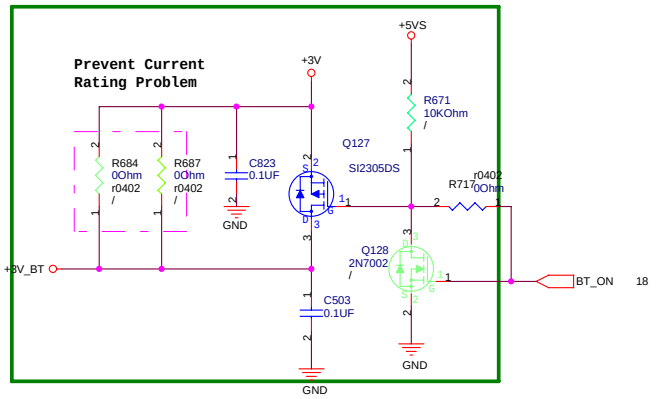
USB



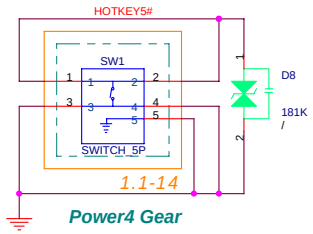


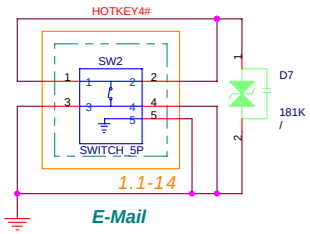
BLUE TOOTH MOLUDE

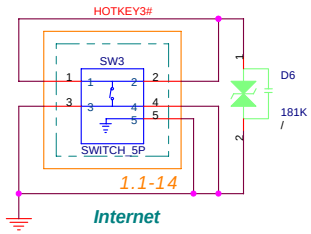


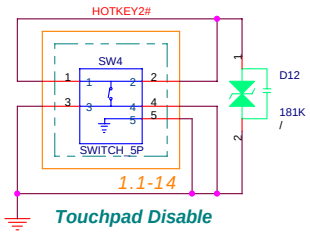


FUNCTION KEY

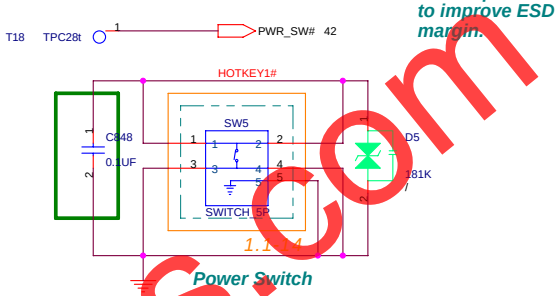


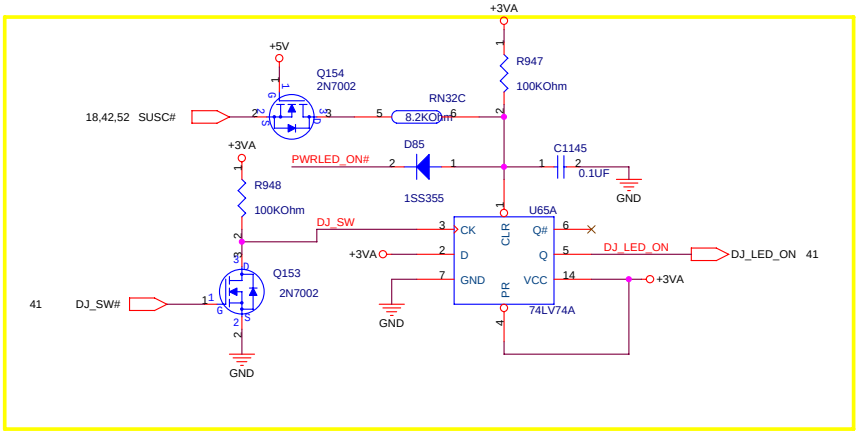




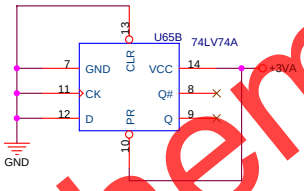


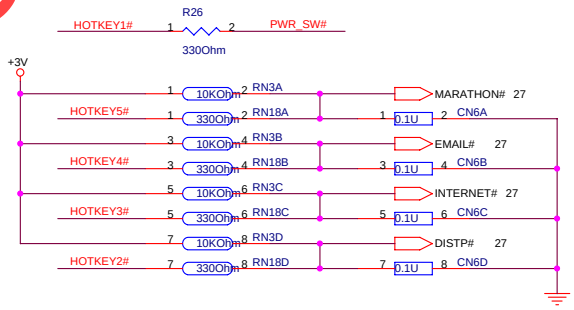
Uses 5-pin switch to improve ESD margin.

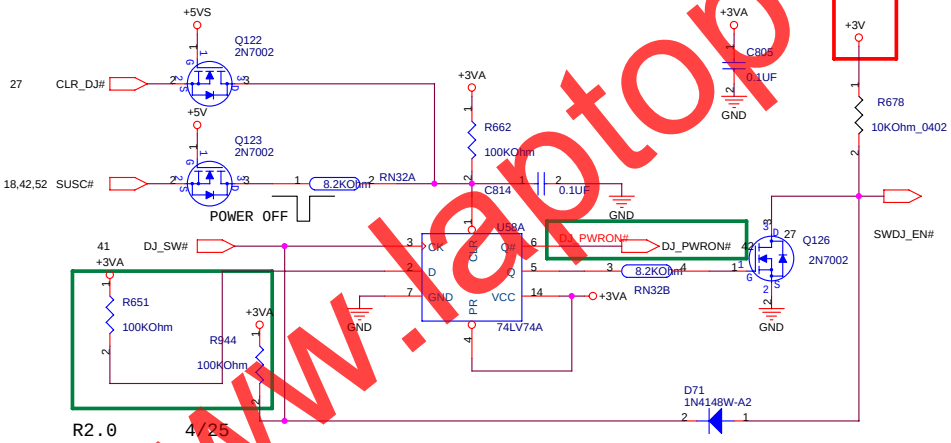




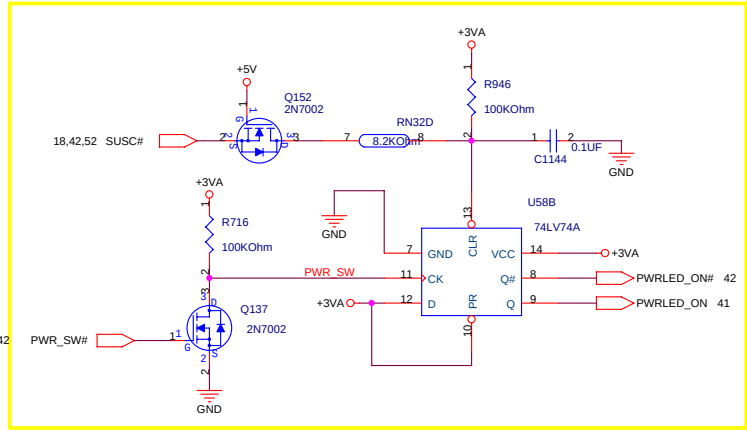
5/4

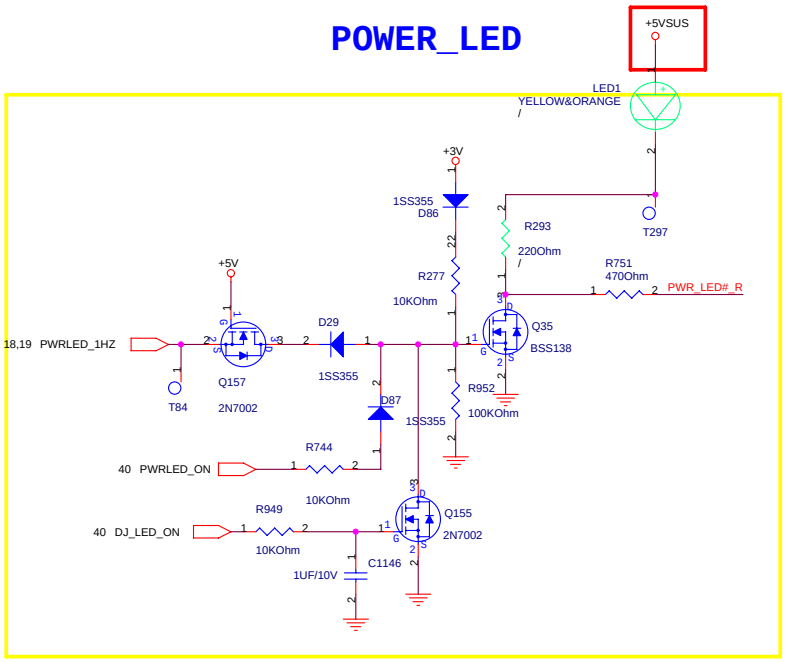




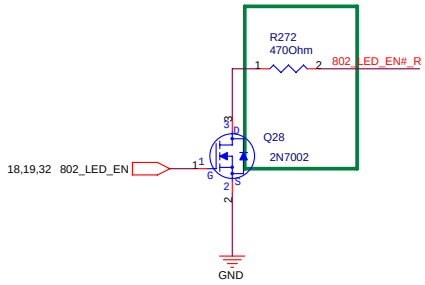


5/4



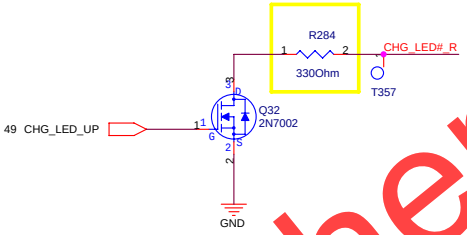


R2.0

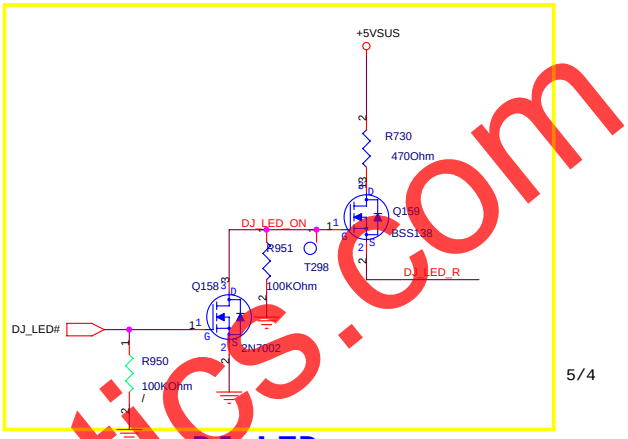


802_LED

5/3 R2.0

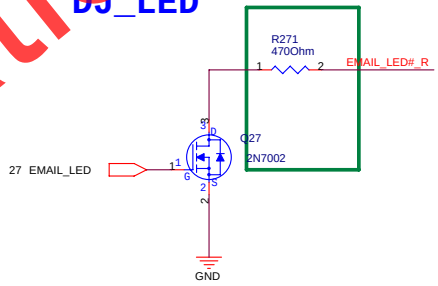


CHG_LED



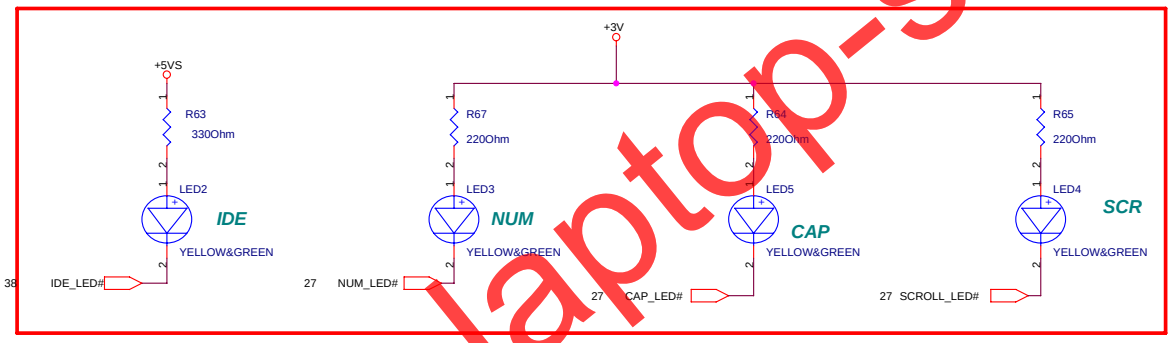
5/4

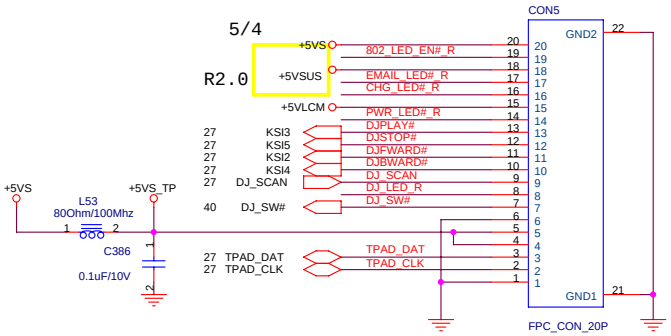
DJ_LED

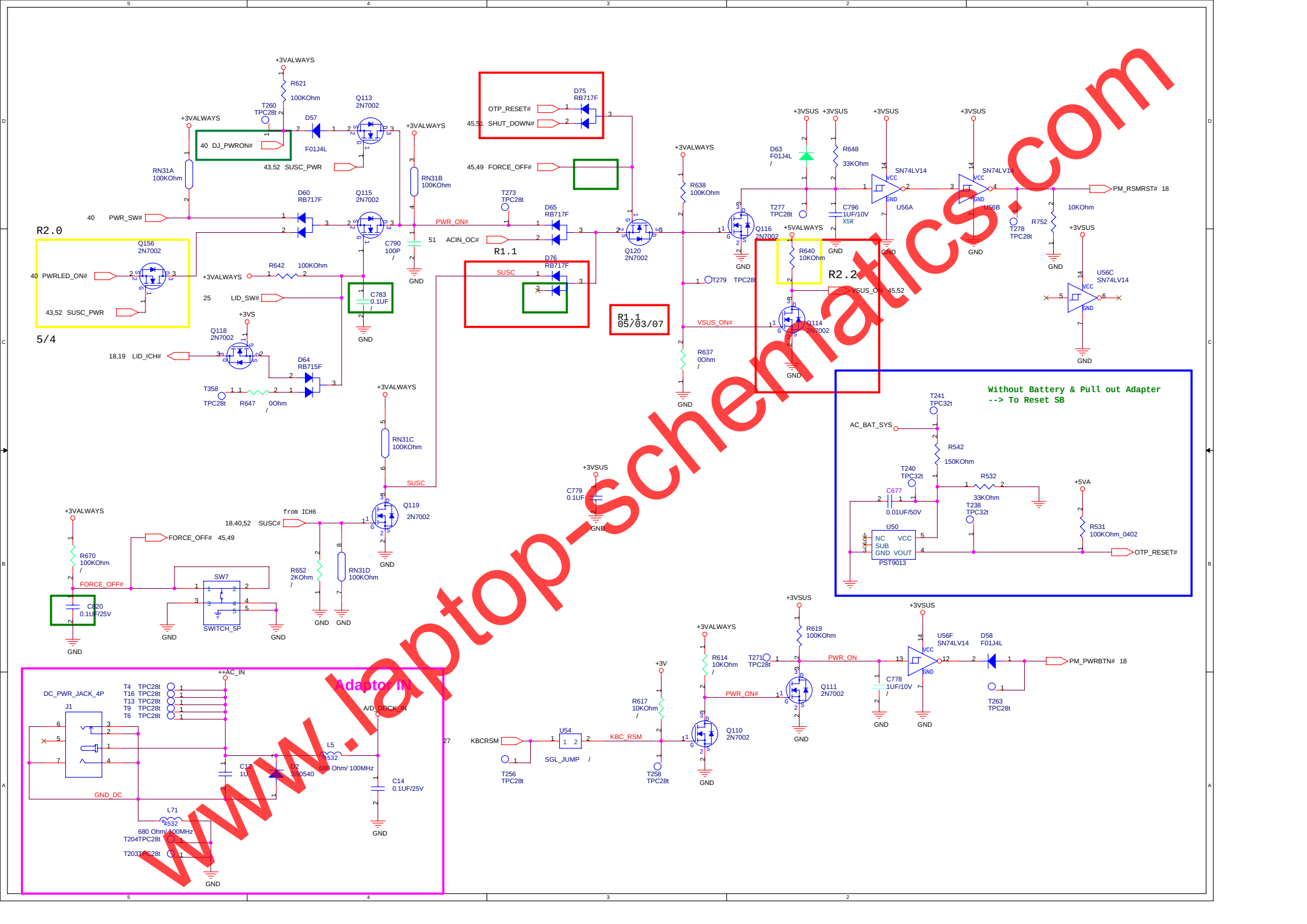


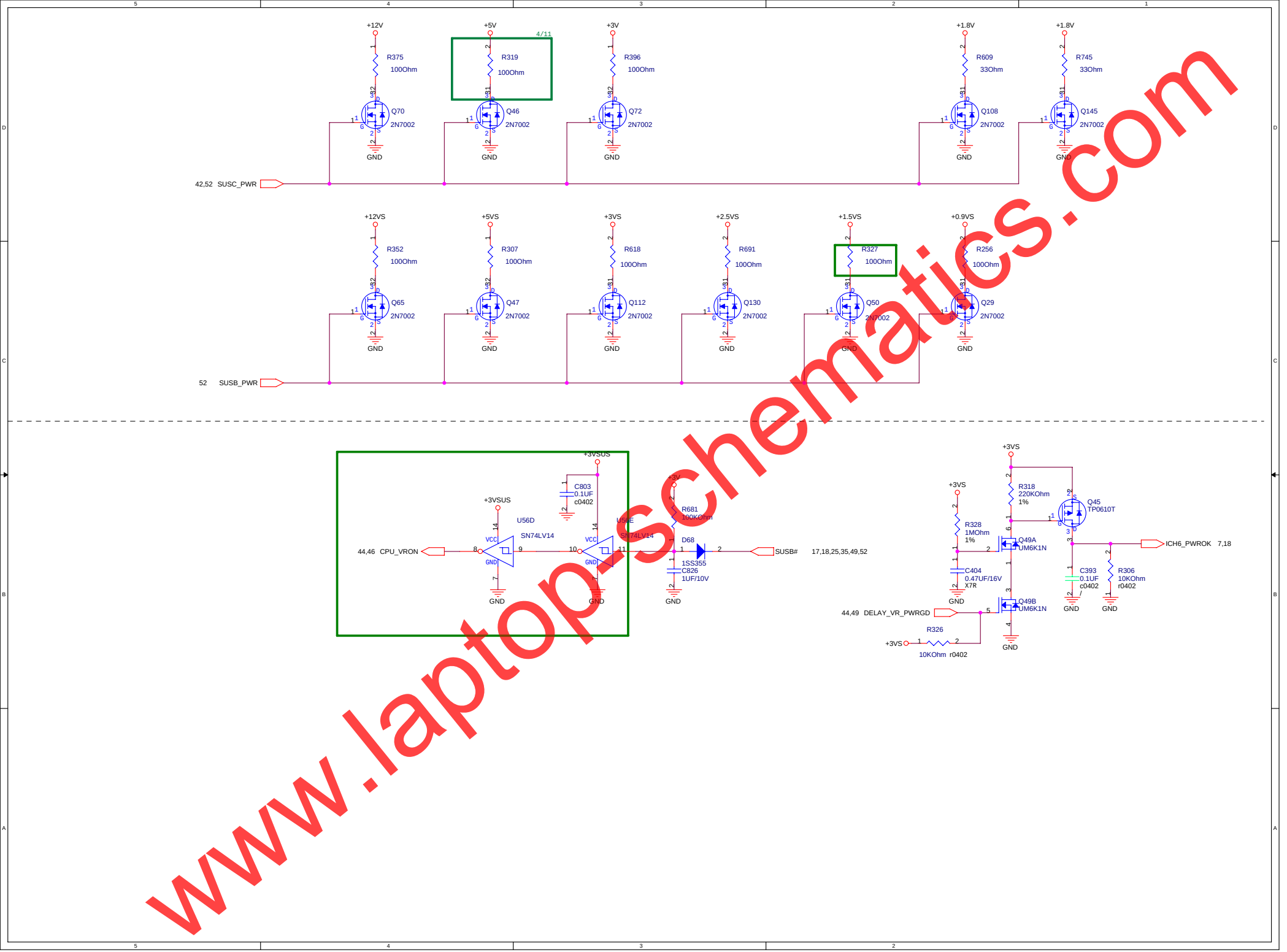
EMAIL_LED

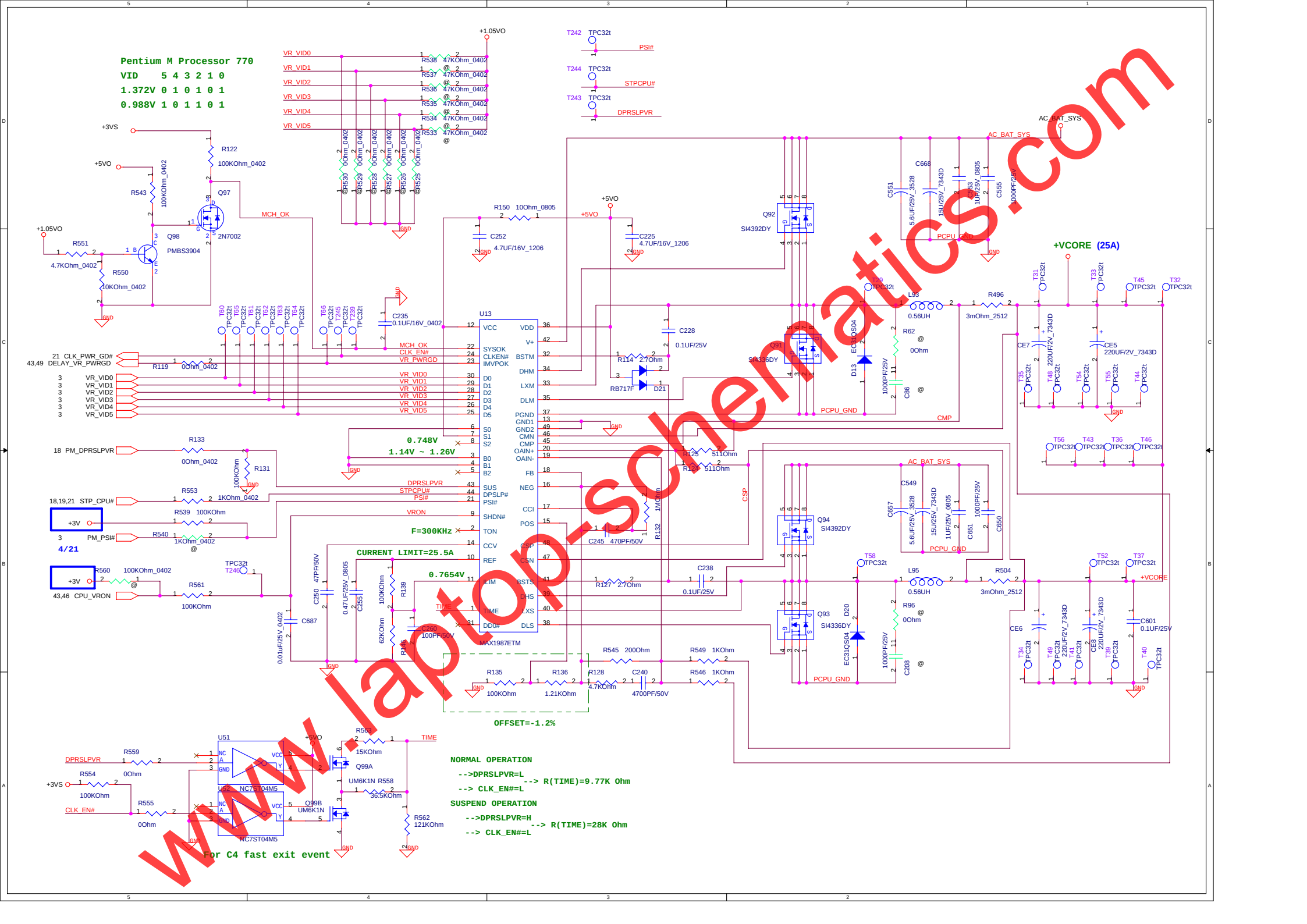
R1.1

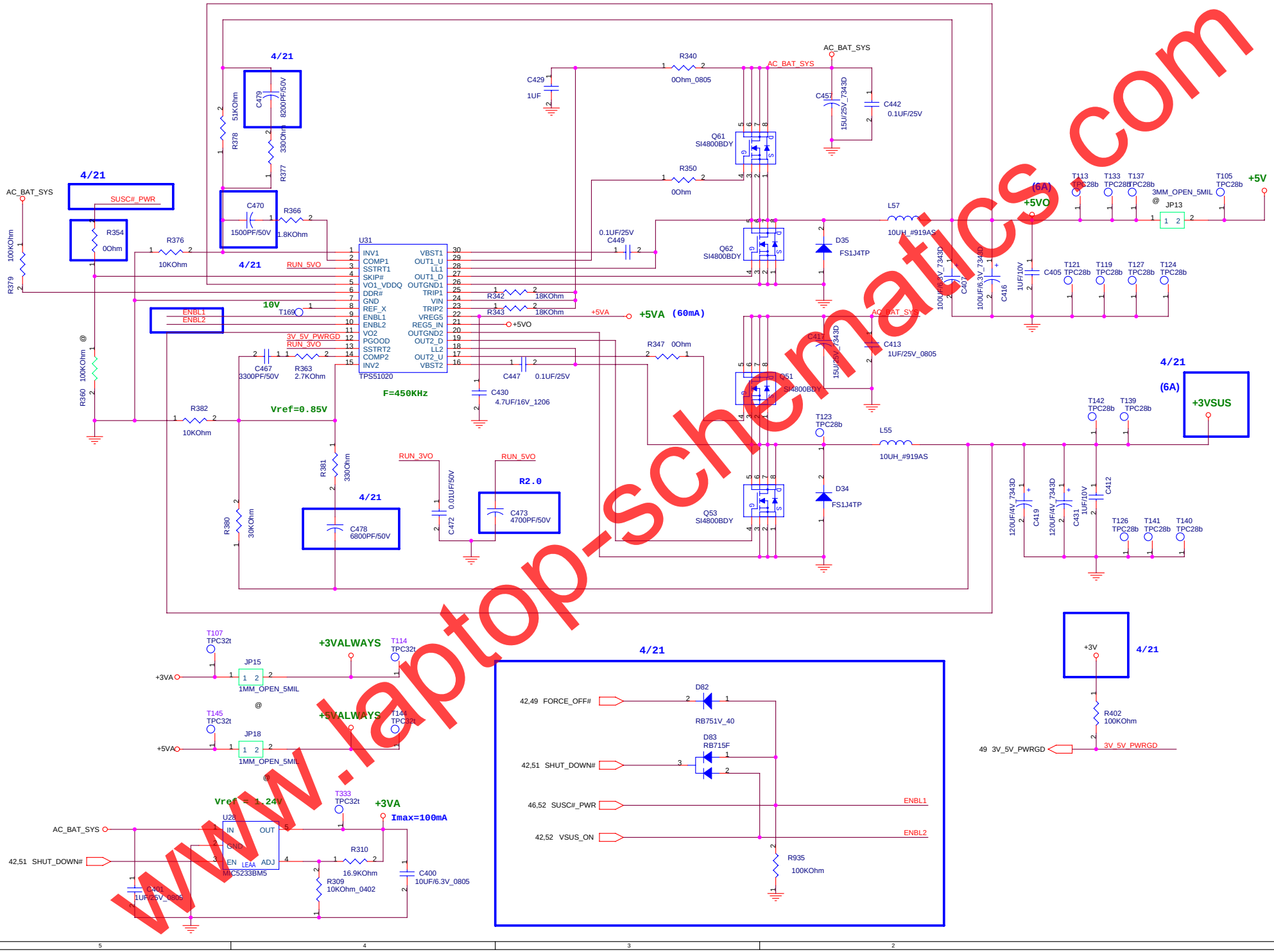


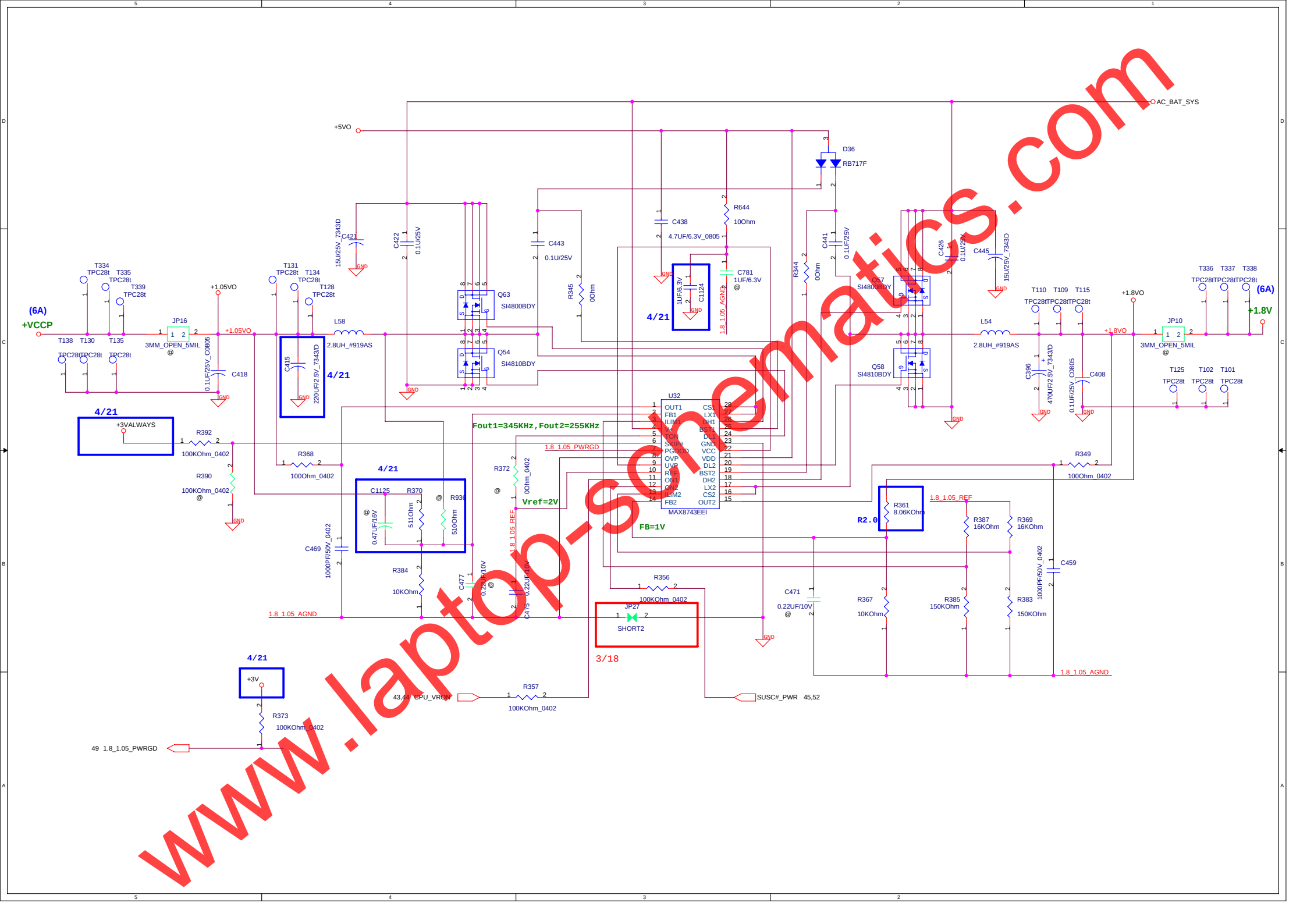


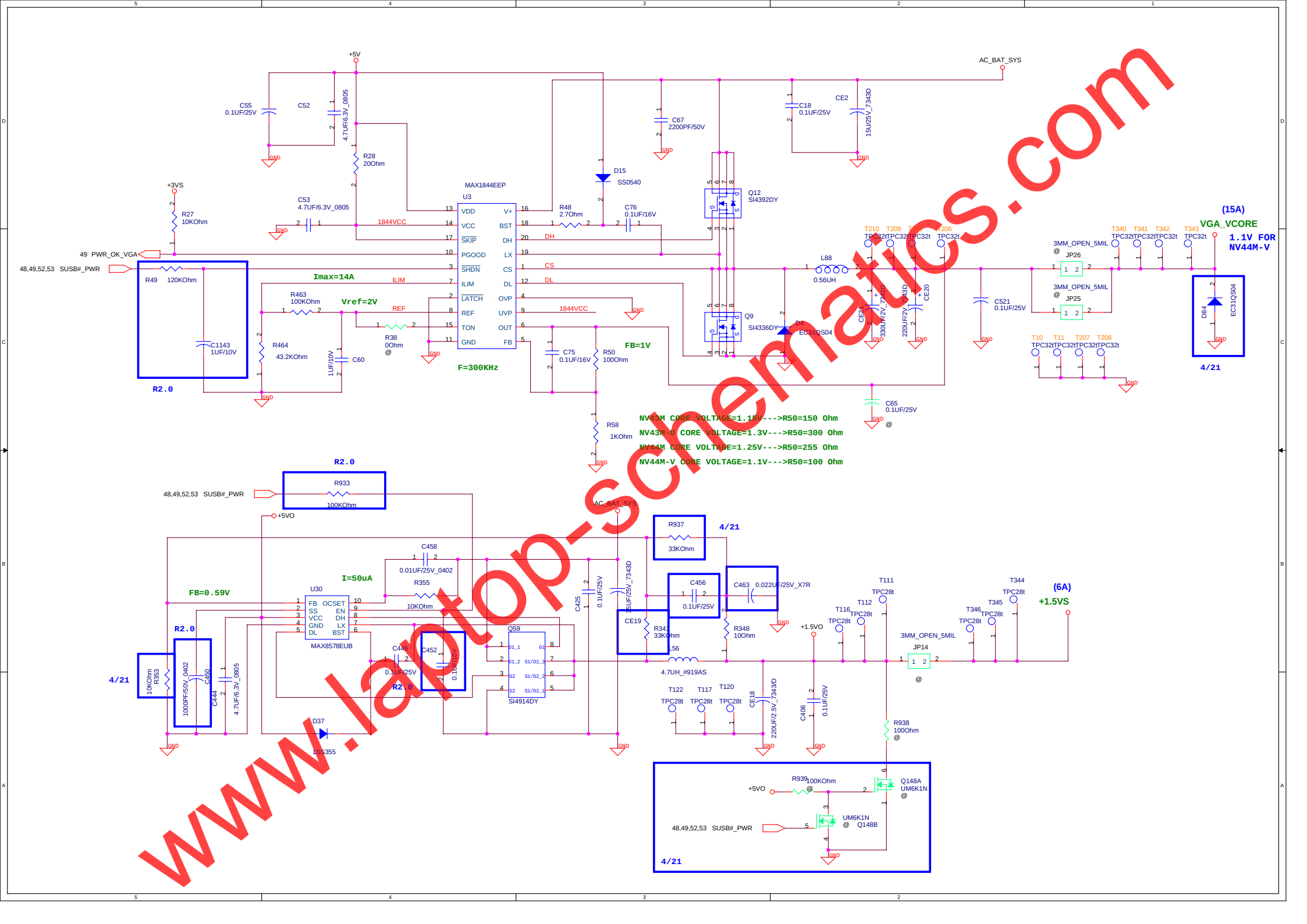


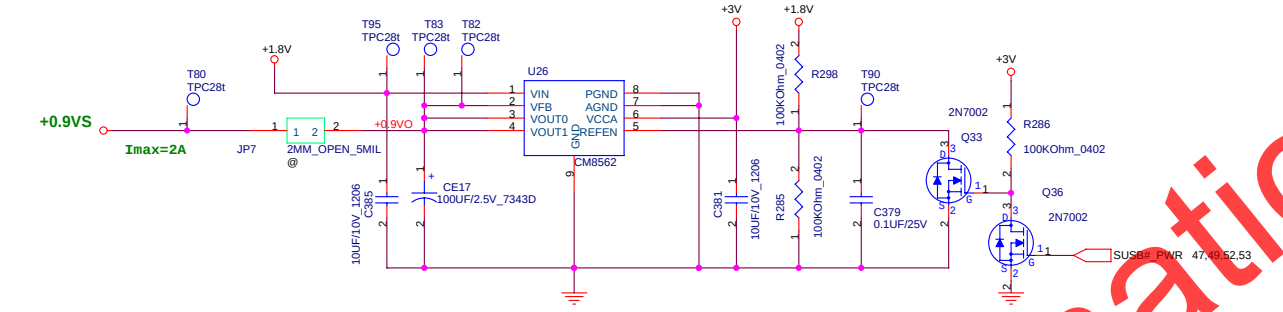


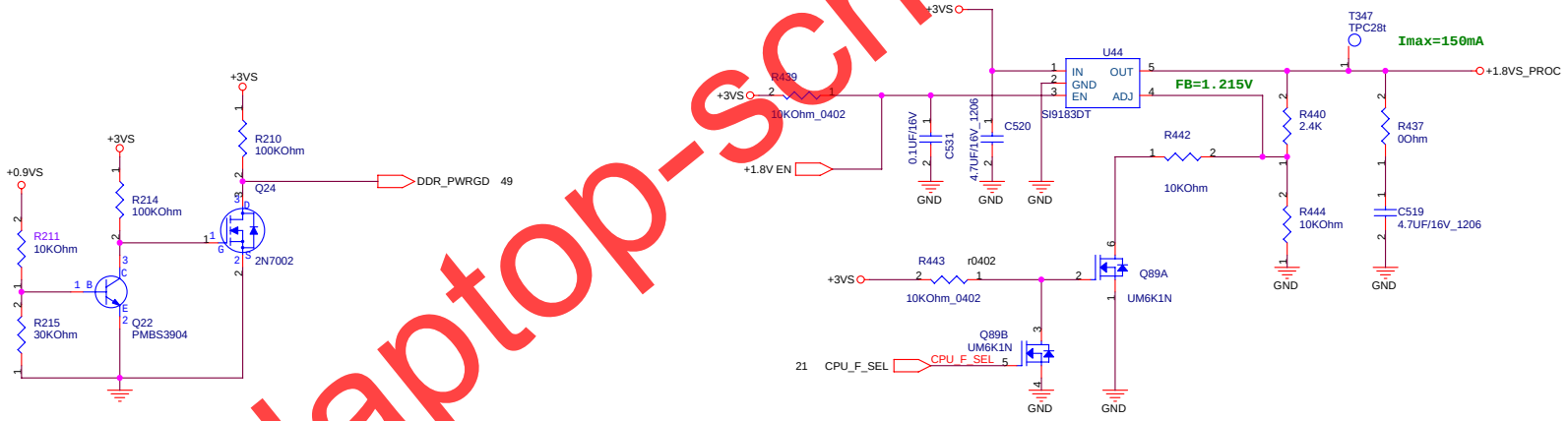

Pentium M Processor 770
VID 5 4 3 2 1 0
1.372V 0 1 0 1 0 1
0.988V 1 0 1 1 0 1
+1.05VO
+3VS
+5VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
R538 47KOhm_0402
R537 47KOhm_0402
R536 47KOhm_0402
R535 47KOhm_0402
R534 47KOhm_0402
R533 47KOhm_0402
R530 0Ohm_0402
R529 0Ohm_0402
R528 0Ohm_0402
R527 0Ohm_0402
R526 0Ohm_0402
R525 0Ohm_0402
T242 TPC32t
PSI#
T244 TPC32t
STPCPU#
T243 TPC32t
DPRSLPVR
R122 100KOhm_0402
R543 100KOhm_0402
Q97
MCH_OK
Q98 2N7002
R551 4.7KOhm_0402
PMBS3904
R550 10KOhm_0402
R150 10Ohm_0805
C252 4.7UF/16V_1206
C225 4.7UF/16V_1206
C235 0.1UF/16V_0402
U13
MAX1987ETM
VCC
VDD
V+
BSTM
DHM
LXM
DLM
PGND
GND1
GND2
CMN
CMP
OAIN+
OAIN-
FB
NEG
CCI
POS
CSP
CSN
BSTS
DHS
LXS
DLS
SYSOK
CLKEN#
IMVPOK
D0
D1
D2
D3
D4
D5
S0
S1
S2
B0
B1
B2
SUS
DPSLP#
PSI#
SHDN#
TON
CCV
REF
ILIM
TIME
DD0#
C228 0.1UF/25V
R114 2.7Ohm
RB717F
D21
Q92 SI4392DY
Q91 SI4336DY
EC31QS04
D13
1000PF/25V
C86
R62 0Ohm
C551 5.6UF/25V_3528
C668 15U/25V_7343D
C553 1UF/25V_0805
C555 1000PF/25V
AC_BAT_SYS
PCPU_GND
L93 0.56UH
R496 3mOhm_2512
+VCORE (25A)
CE7 220UF/2V_7343D
CE5 220UF/2V_7343D
R133 0Ohm_0402
R131 100KOhm
R553 1KOhm_0402
R539 100KOhm
R540 1KOhm_0402
4/21
R560 100KOhm_0402
R561 100KOhm
R125 511Ohm
R124 511Ohm
R132 1MOhm
C245 470PF/50V
R127 2.7Ohm
C238 0.1UF/25V
Q94 SI4392DY
Q93 SI4336DY
C657 5.6UF/25V_3528
C549 15U/25V_7343D
C651 1UF/25V_0805
C650 1000PF/25V
L95 0.56UH
R504 3mOhm_2512
R96 0Ohm
C208
CE6 220UF/2V_7343D
CE8 220UF/2V_7343D
C601 0.1UF/25V
C250 47PF/50V
C255 0.47UF/25V_0805
R139 100KOhm
R140 62KOhm
C260 100PF/50V
C687 0.01UF/25V_0402
R135 100KOhm
R136 1.21KOhm
R128 4.7KOhm
C240 4700PF/50V
R545 200Ohm
R549 1KOhm
R546 1KOhm
0.748V
1.14V ~ 1.26V
F=300KHz
CURRENT LIMIT=25.5A
0.7654V
OFFSET=-1.2%
U51 NC7ST04M5
U52 NC7ST04M5
R559 0Ohm
R554 100KOhm
R555 0Ohm
R563 15KOhm
Q99A
UM6K1N R558 36.5KOhm
Q99B UM6K1N
R562 121KOhm
NORMAL OPERATION
-->DPRSLPVR=L --> R(TIME)=9.77K Ohm
--> CLK_EN#=L
SUSPEND OPERATION
-->DPRSLPVR=H --> R(TIME)=28K Ohm
--> CLK_EN#=L
For C4 fast exit event
www.laptop-schematics.com





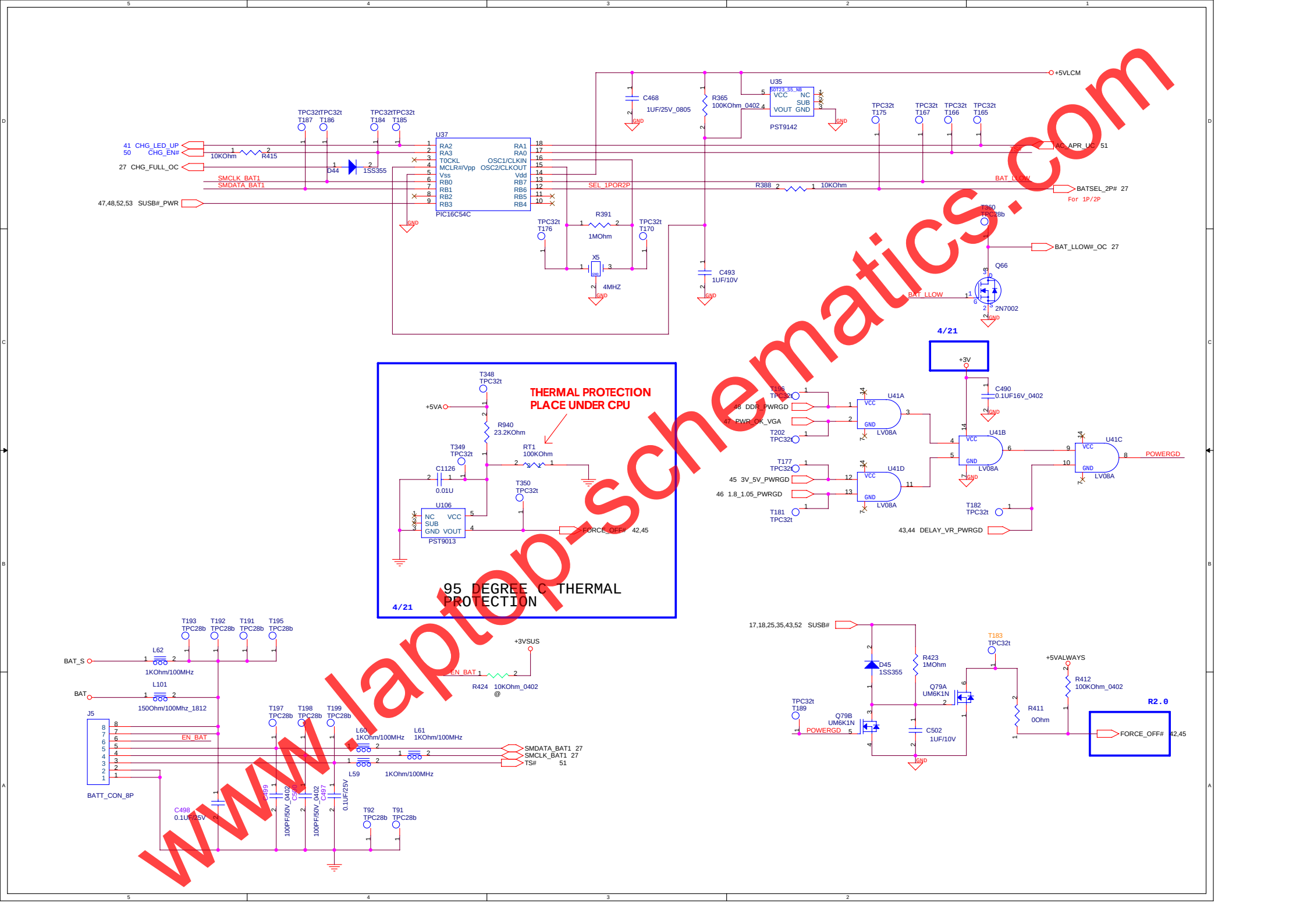


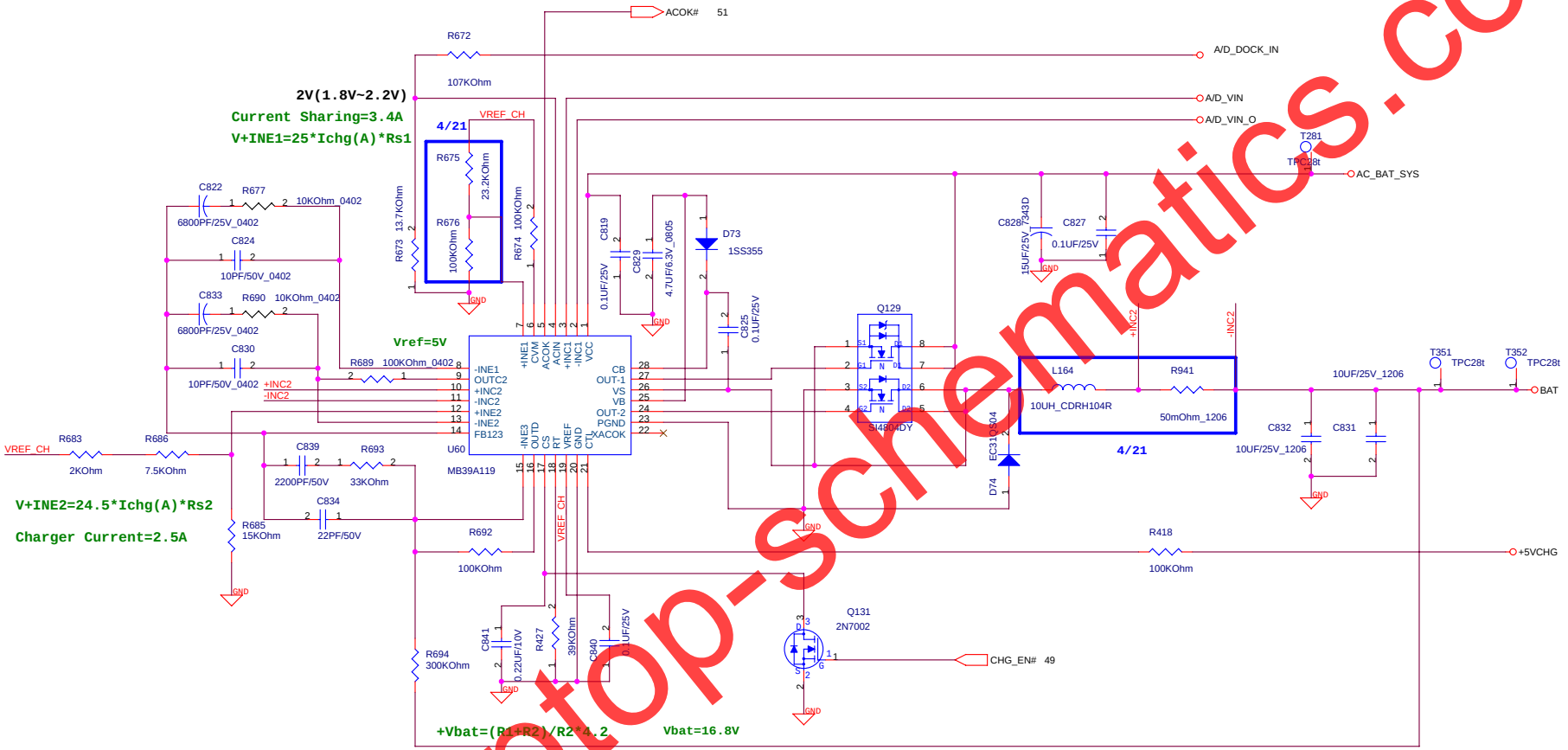


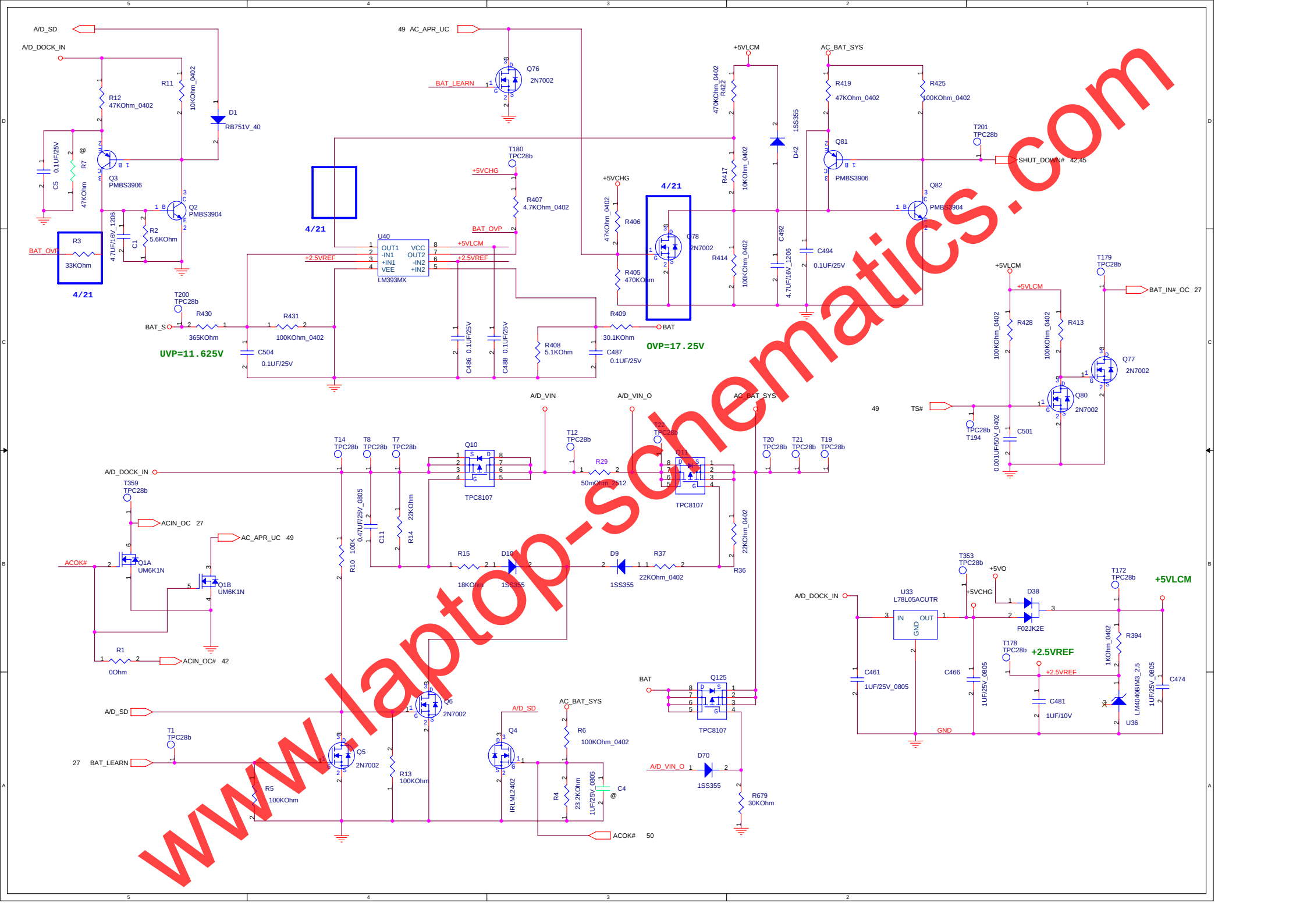


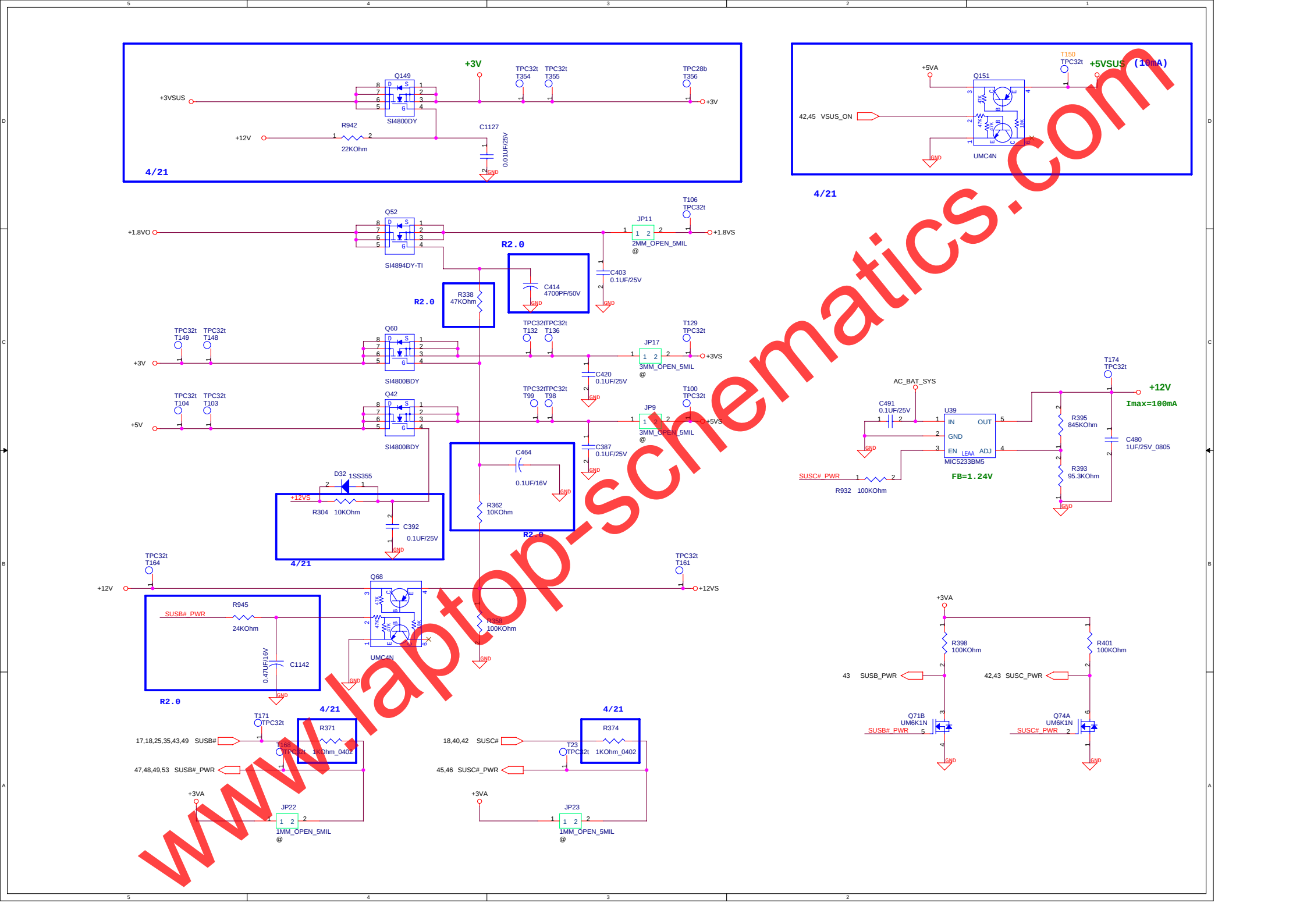
CPU_F_SEL-->H, OUT=1.5V (FSB=533MHz)

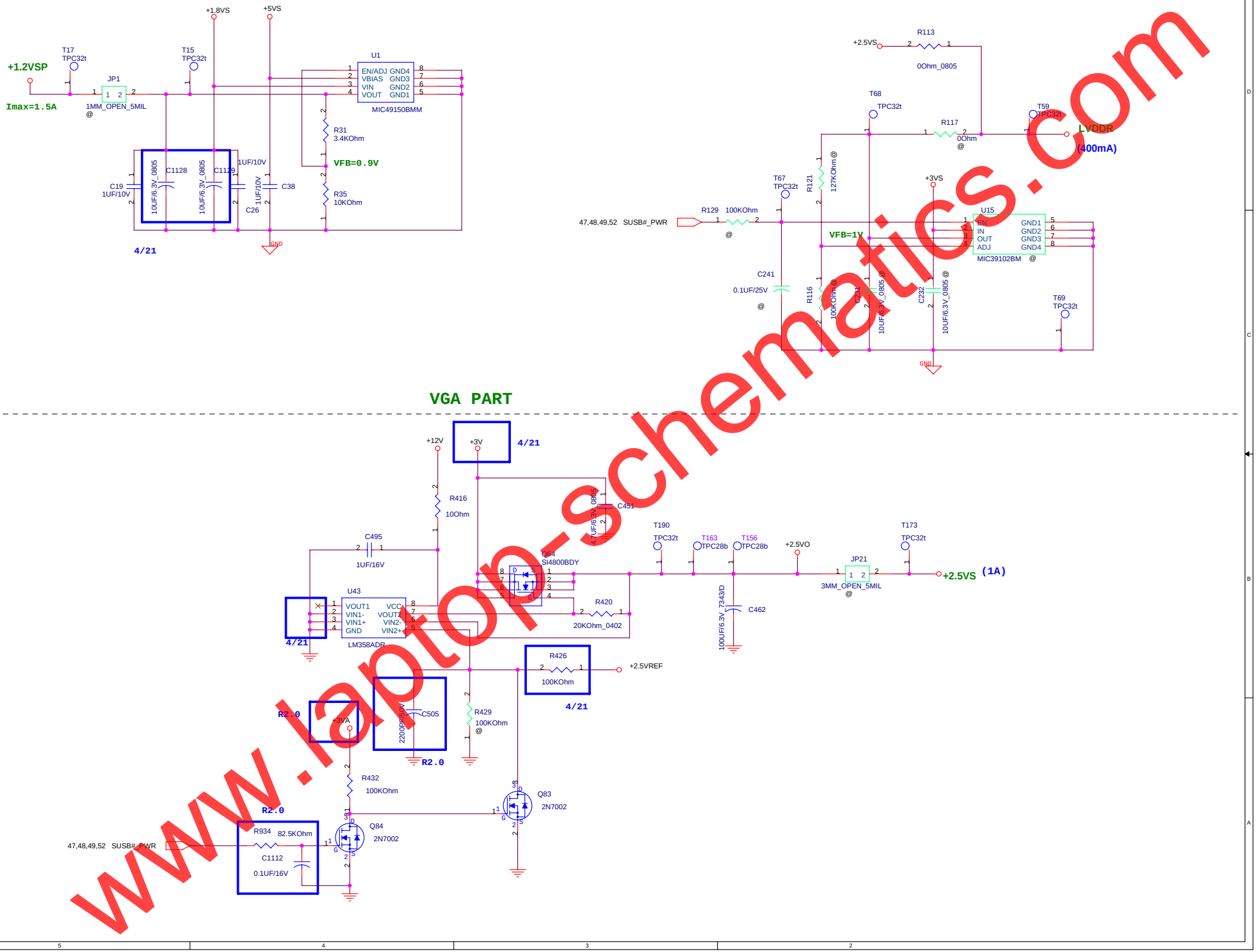
CPU_F_SEL-->L, OUT=1.8V (FSB=400MHz)

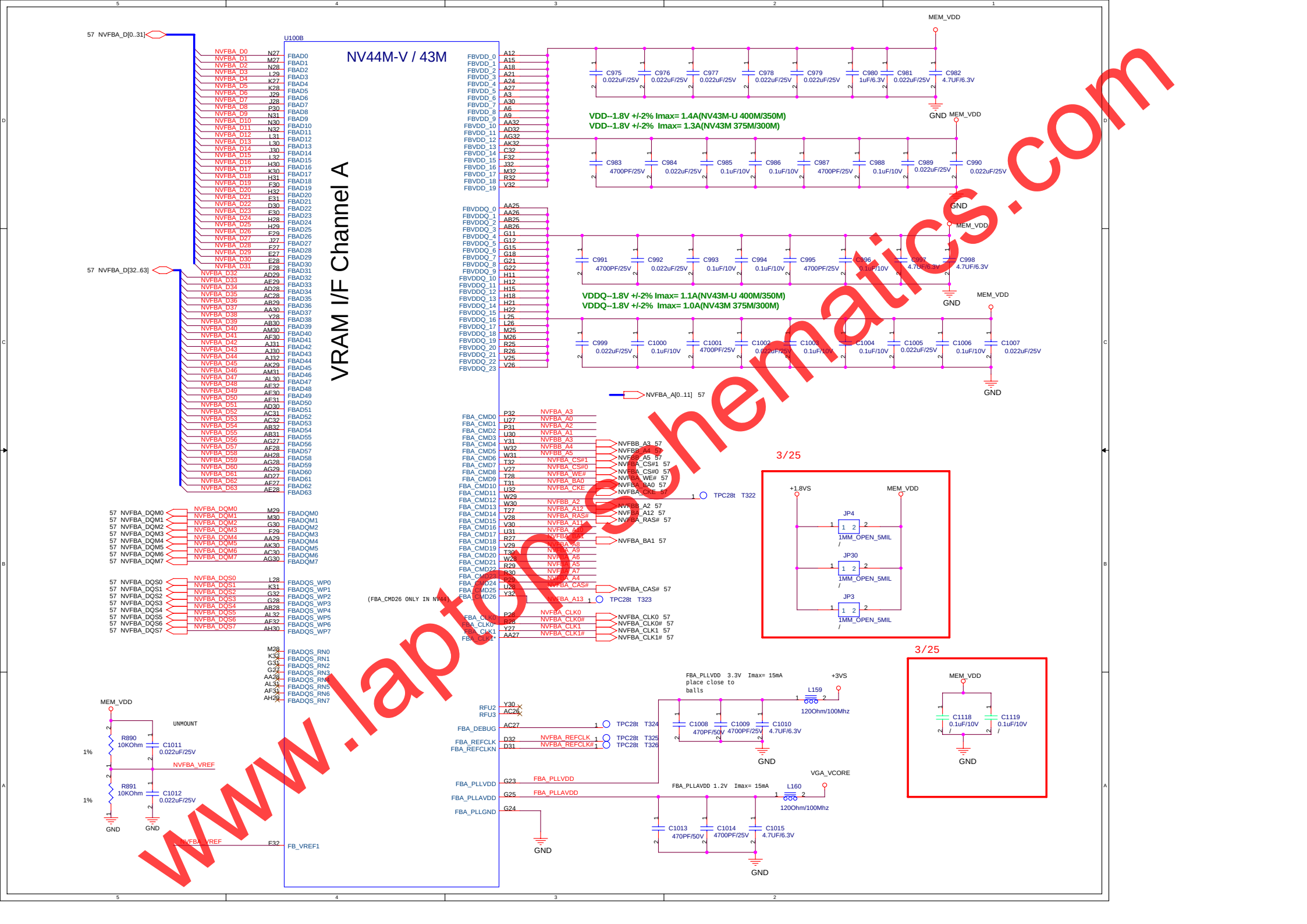


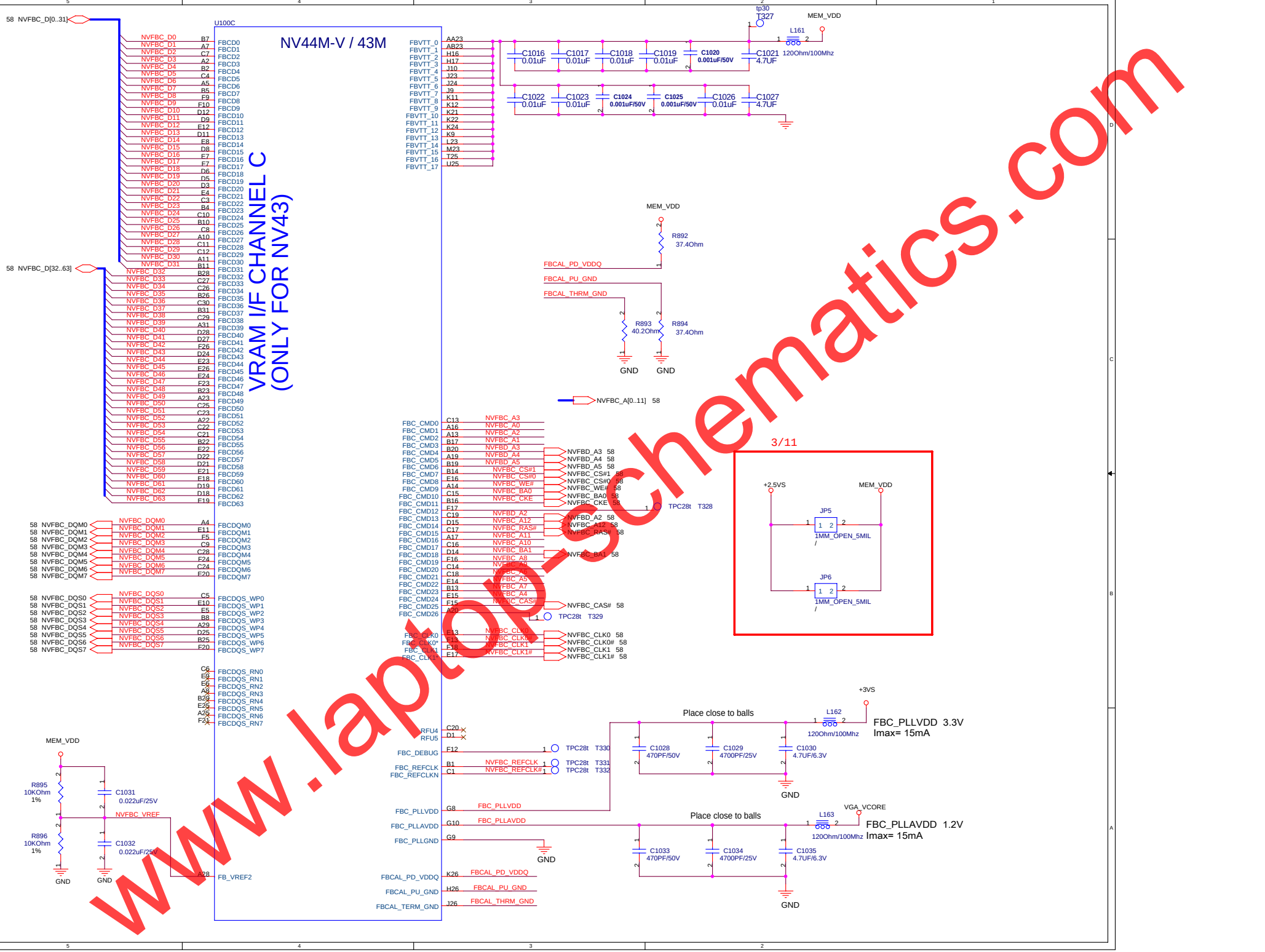


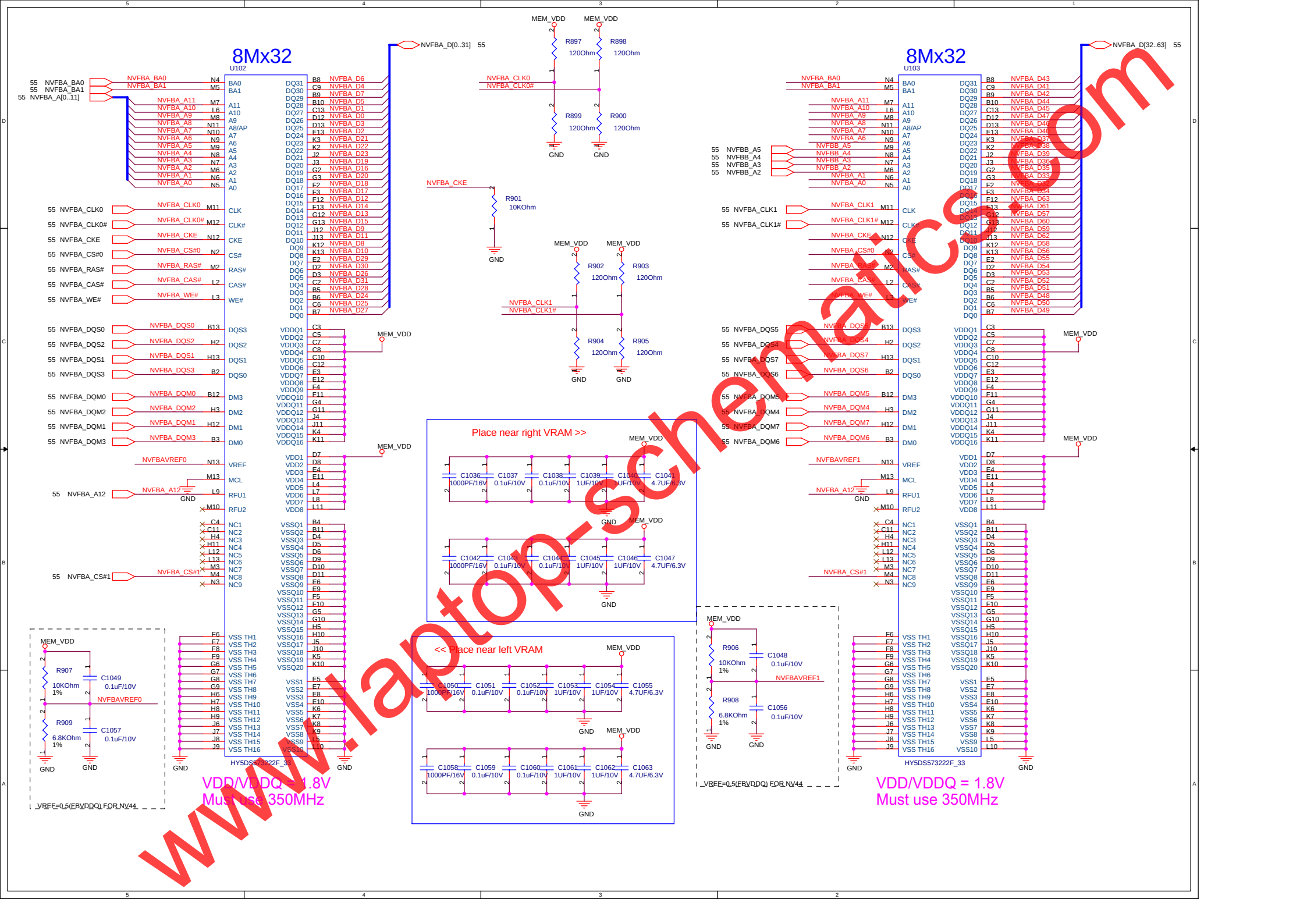


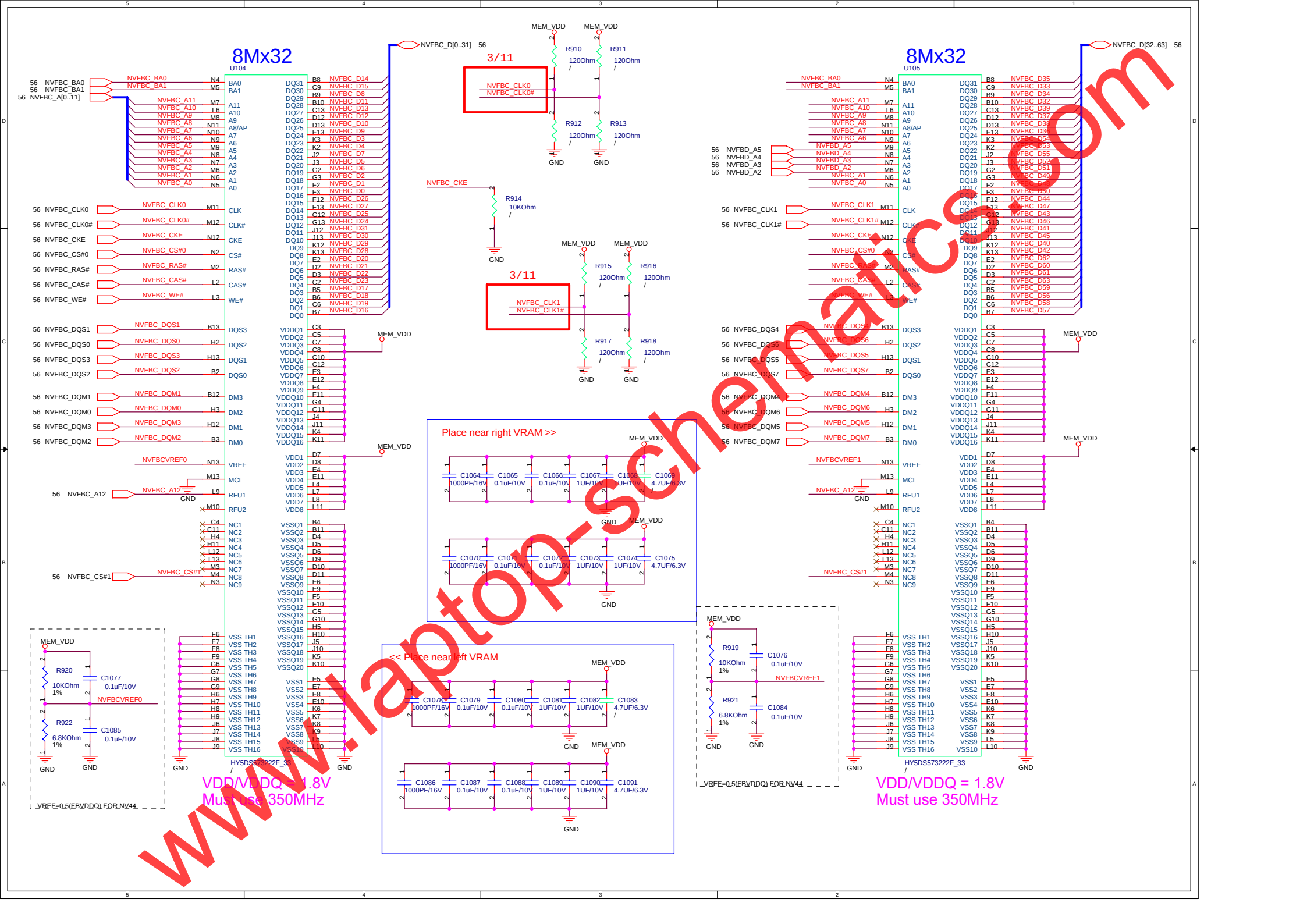








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U104
8Mx32
U105
3/11
3/11
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<< Place near left VRAM
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