Compal Confidential

QBL60 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-04-25

LA-7552P REV: 1.0

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/25	Deciphered Date	2012/04/25
Title	Cover Page		
Size B	Document Number QBL60 LA-7552P		Rev 1.0
Date: Monday, April 25, 2011	Sheet 1 of 53		

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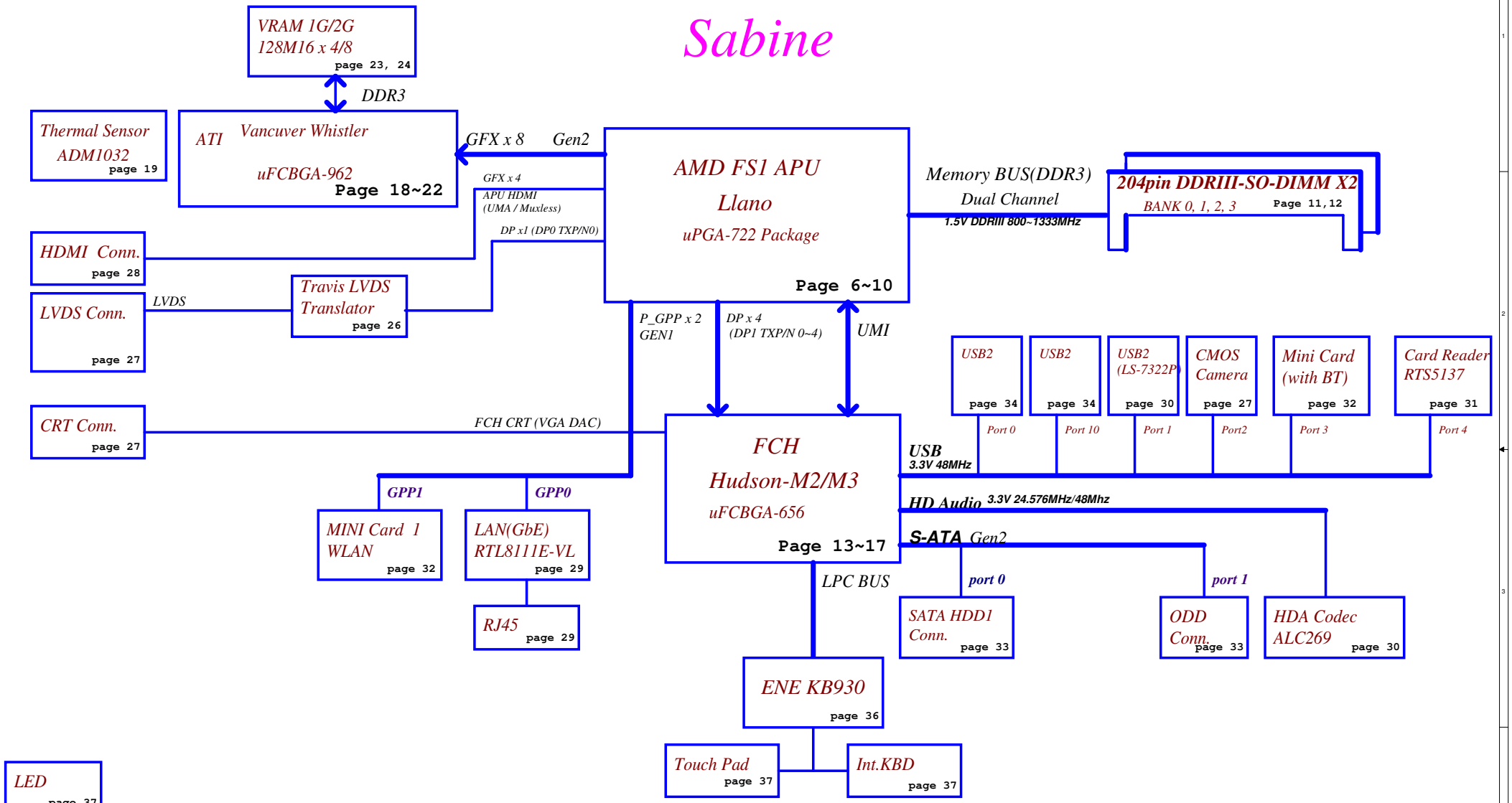
Model Name : QBL60



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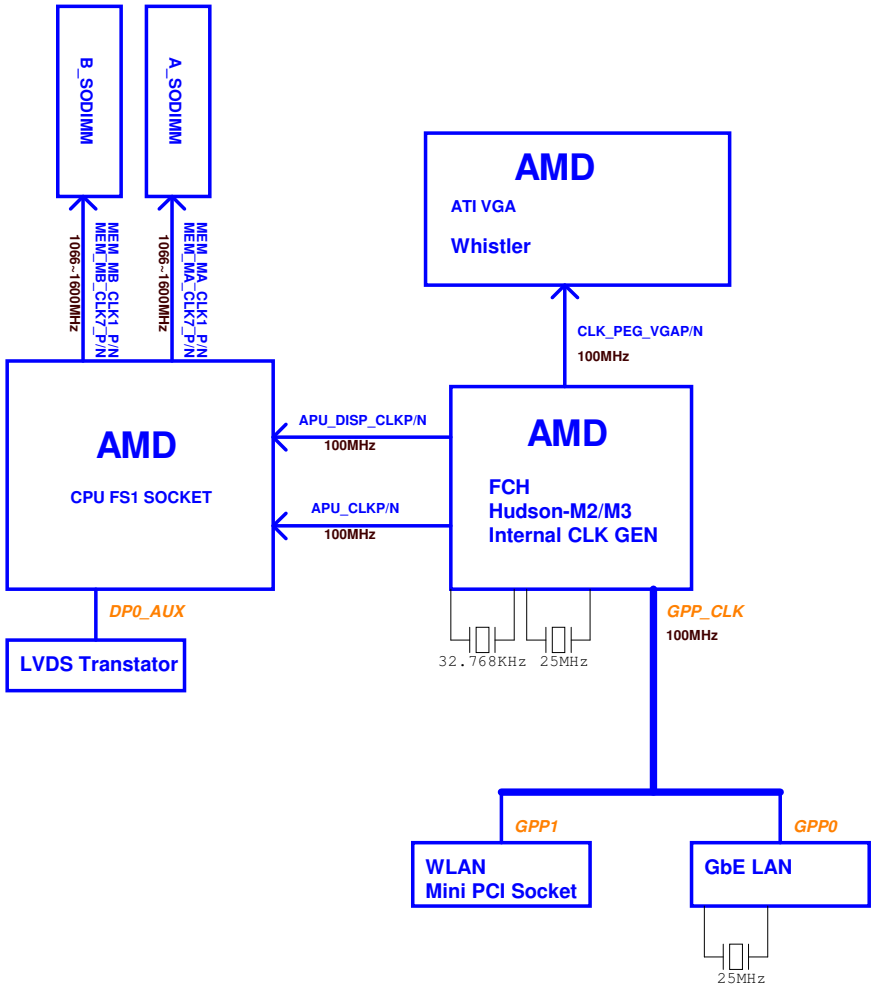
Title: Block Diagrams			
Size: B	Document Number: QBL60 LA-7552P		Rev: 1.0
Date: Monday, April 25, 2011	Sheet 2 of 53		

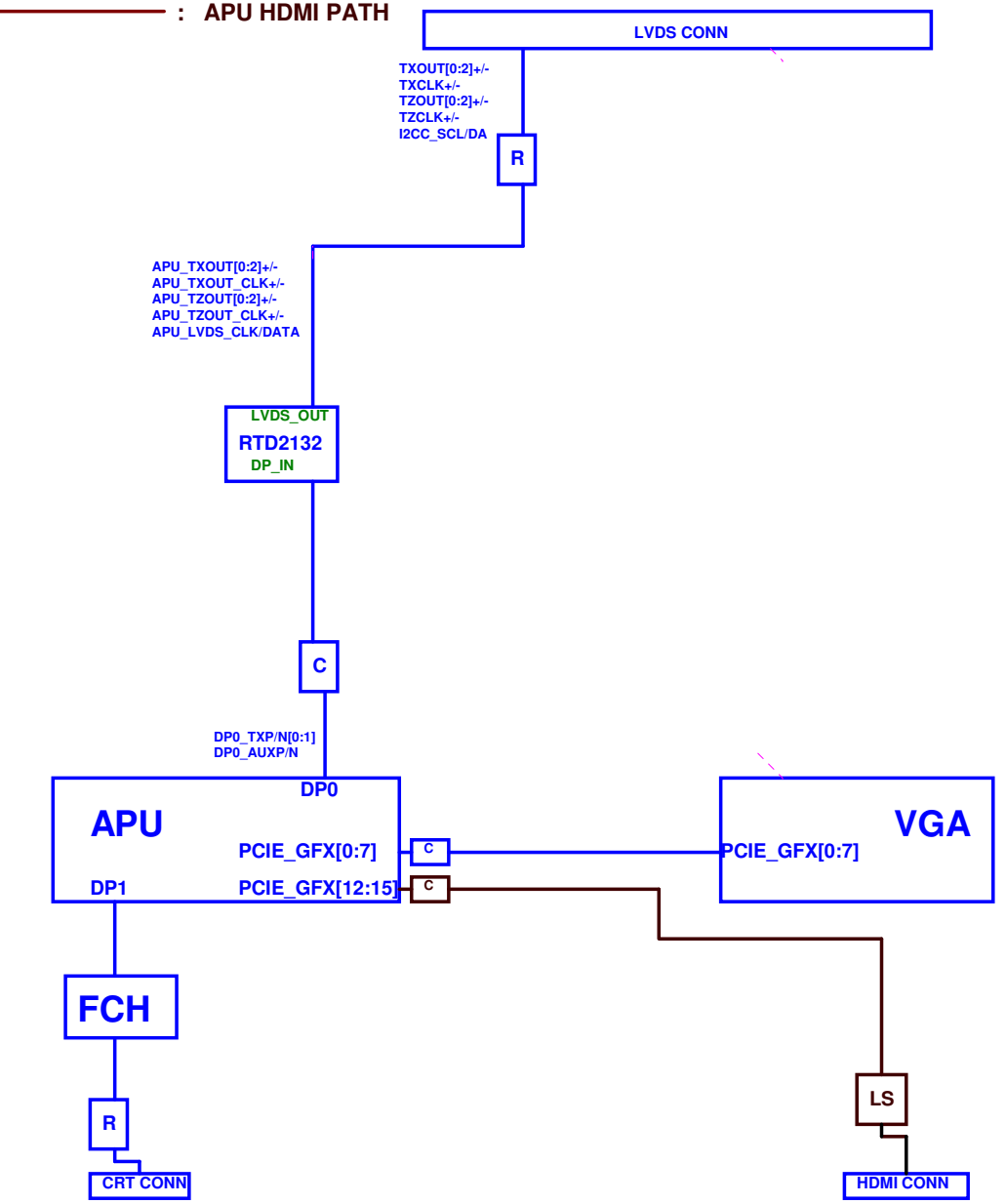
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Title	CLOCK / DISPLAY DISTRIBUTION	
Size: Custom	Document Number: QBL60 LA-7552P	Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043ID0

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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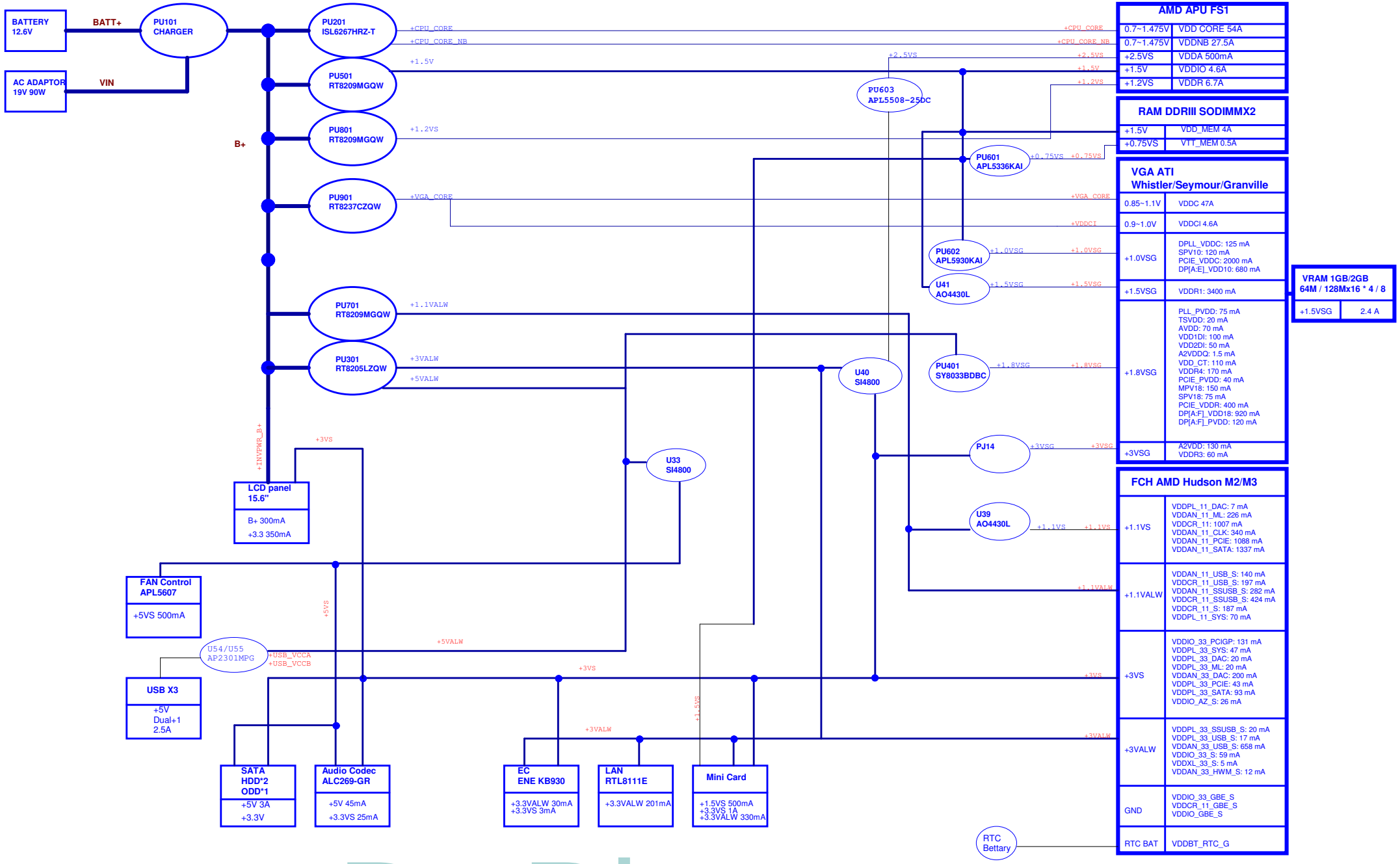

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Title	POWER DELIVERY CHART		
Size	Document Number		Rev
Custom	QBL60 LA-7552P		1.0
Date:	Monday, April 25, 2011	Sheet	5 of 53

18 PCIE_GTX_C_FRX_P[0..7]
18 PCIE_GTX_C_FRX_N[0..7]

PCIE_FTX_C_GRX_P[0..7] 18
PCIE_FTX_C_GRX_N[0..7] 18

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

JCPU1A — CONN@ — PCI EXPRESS — GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C917	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C918	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C919	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C920	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C921	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C922	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2
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PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C924	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3
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PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C926	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C927	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5	U6	P_GFX_RXN5	P_GFX_TXN5	V5	PCIE_FTX_GRX_N5	C928	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N5
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PCIE_GTX_C_FRX_N6	U9	P_GFX_RXN6	P_GFX_TXN6	U3	PCIE_FTX_GRX_N6	C930	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7	T7	P_GFX_RXP7	P_GFX_TXP7	T2	PCIE_FTX_GRX_P7	C931	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C932	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N7
	R5	P_GFX_RXP8	P_GFX_TXP8	T4					
	R6	P_GFX_RXN8	P_GFX_TXN8	T5					
	R8	P_GFX_RXP9	P_GFX_TXP9	R2					
	R9	P_GFX_RXN9	P_GFX_TXN9	R3					
	P7	P_GFX_RXP10	P_GFX_TXP10	P2					
	P8	P_GFX_RXN10	P_GFX_TXN10	P1					
	N5	P_GFX_RXP11	P_GFX_TXP11	P4					
	N6	P_GFX_RXN11	P_GFX_TXN11	P5					
	N8	P_GFX_RXP12	P_GFX_TXP12	N2	PCIE_FTX_GRX_P12				
	N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12				
	M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13				
	M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13				
	L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14				
	L6	P_GFX_RXN14	P_GFX_TXN14	M5	PCIE_FTX_GRX_N14				
	L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15				
	L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15				

For UMA Mux.

To HDMI

2 1 0 CK

GPP

29 PCIE_DTX_C_FRX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_DRX_P0	C950	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29	
29 PCIE_DTX_C_FRX_N0	AC6	P_GPP_RXN0	P_GPP_TXN0	AD5	PCIE_FTX_DRX_N0	C951	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29	
32 PCIE_DTX_C_FRX_P1	AC8	P_GPP_RXP1	P_GPP_TXP1	AC2	PCIE_FTX_DRX_P1	C952	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32	
32 PCIE_DTX_C_FRX_N1	AC9	P_GPP_RXN1	P_GPP_TXN1	AC3	PCIE_FTX_DRX_N1	C953	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N1 32	
	AB7	P_GPP_RXP2	P_GPP_TXP2	AB2					
	AB8	P_GPP_RXN2	P_GPP_TXN2	AB1					
	AA5	P_GPP_RXP3	P_GPP_TXP3	AB4					
	AA6	P_GPP_RXN3	P_GPP_TXN3	AB5					

GLAN

WLAN

UMI-LINK

13 UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C956	0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13
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13 UMI_MTX_C_FRX_N3	AD7	P_UMI_RXN3	P_UMI_TXN3	AD2	UMI_FTX_MRX_N3	C963	0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13

+1.2VS — R539 1 2 196_0402_1% — P_ZVDDP K5 — P_ZVDDP

P_ZVSS K4 — R540 1 2 196_0402_1% — P_ZVSS

AMD_TOPEDO_FS-1

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

C935 1 2 0.1U_0402_16V4Z

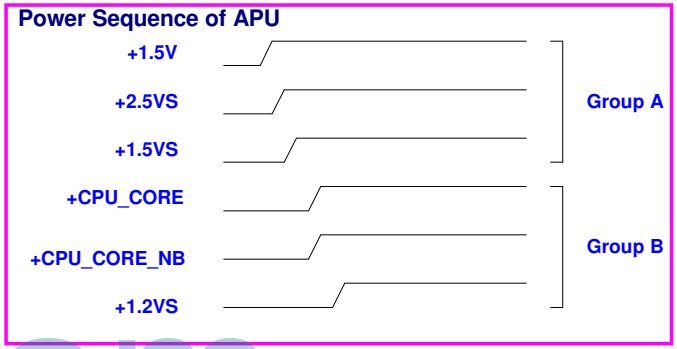
+3VS — R535 1 2 31.6K_0402_1% — R536 1 2 30K_0402_1%

8,14 APU_SID — APU_SID — Q9 BSH111 1N_SOT23-3 — EC_SMB_DA — R537 0_0402_5% — EC_SMB_DA2 19,36

8,14 APU_SIC — APU_SIC — Q10 BSH111 1N_SOT23-3 — EC_SMB_CK — R538 0_0402_5% — EC_SMB_CK2 19,36

To EC

Power Sequence of APU



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Title: AMD FS1 PCIE / UMI / TSI

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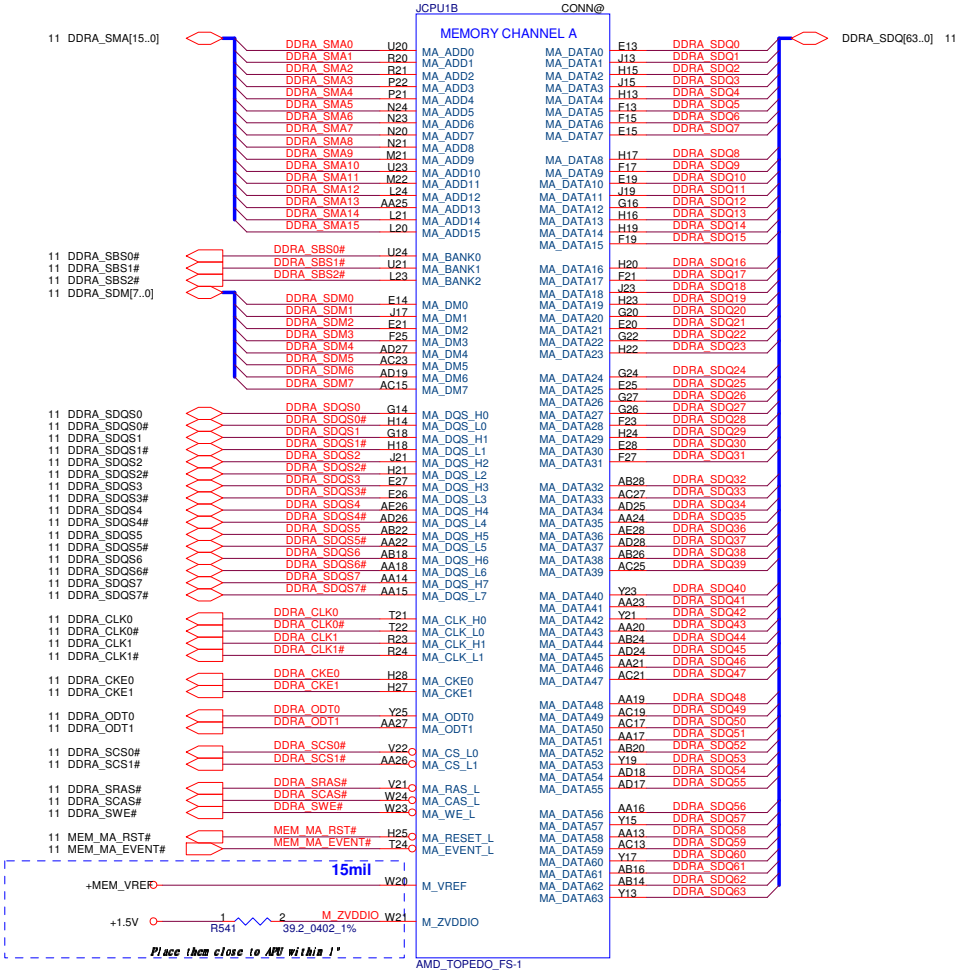

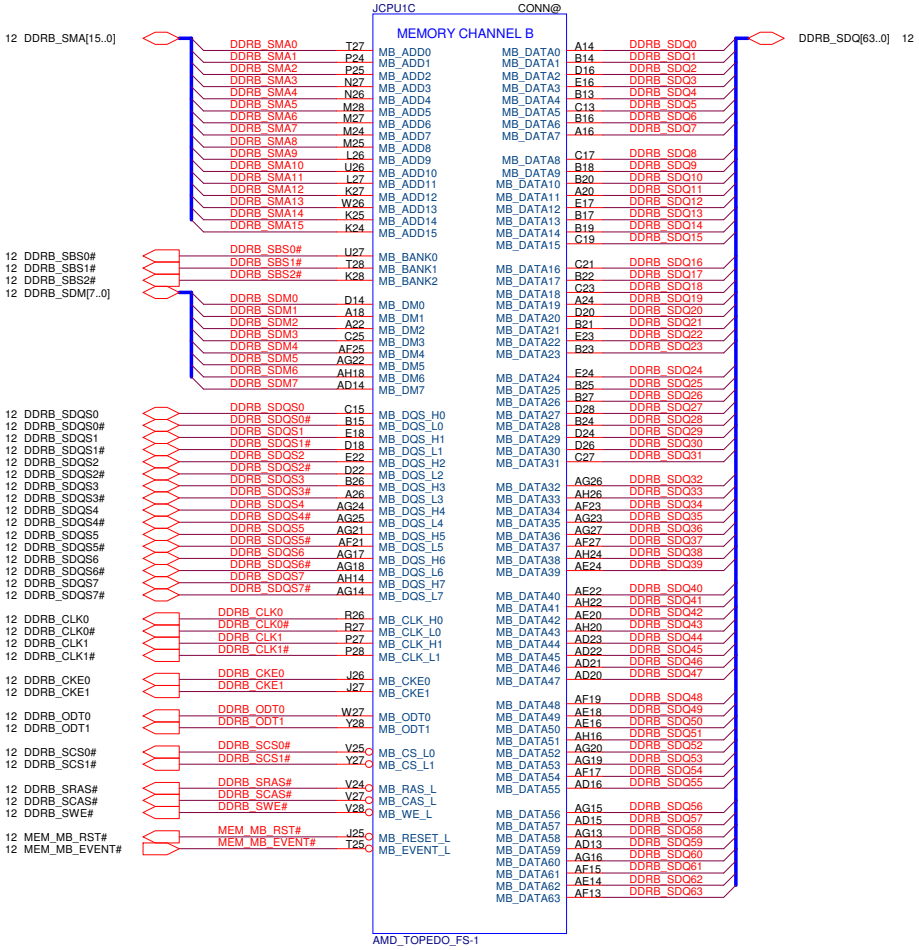

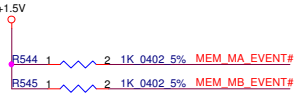

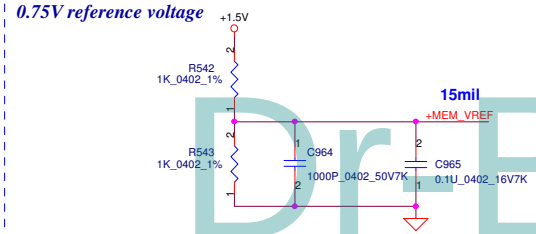

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Compal Electronics, Inc.

Title: AMD FS1 DDRIII I/F

Size	Document Number	Rev
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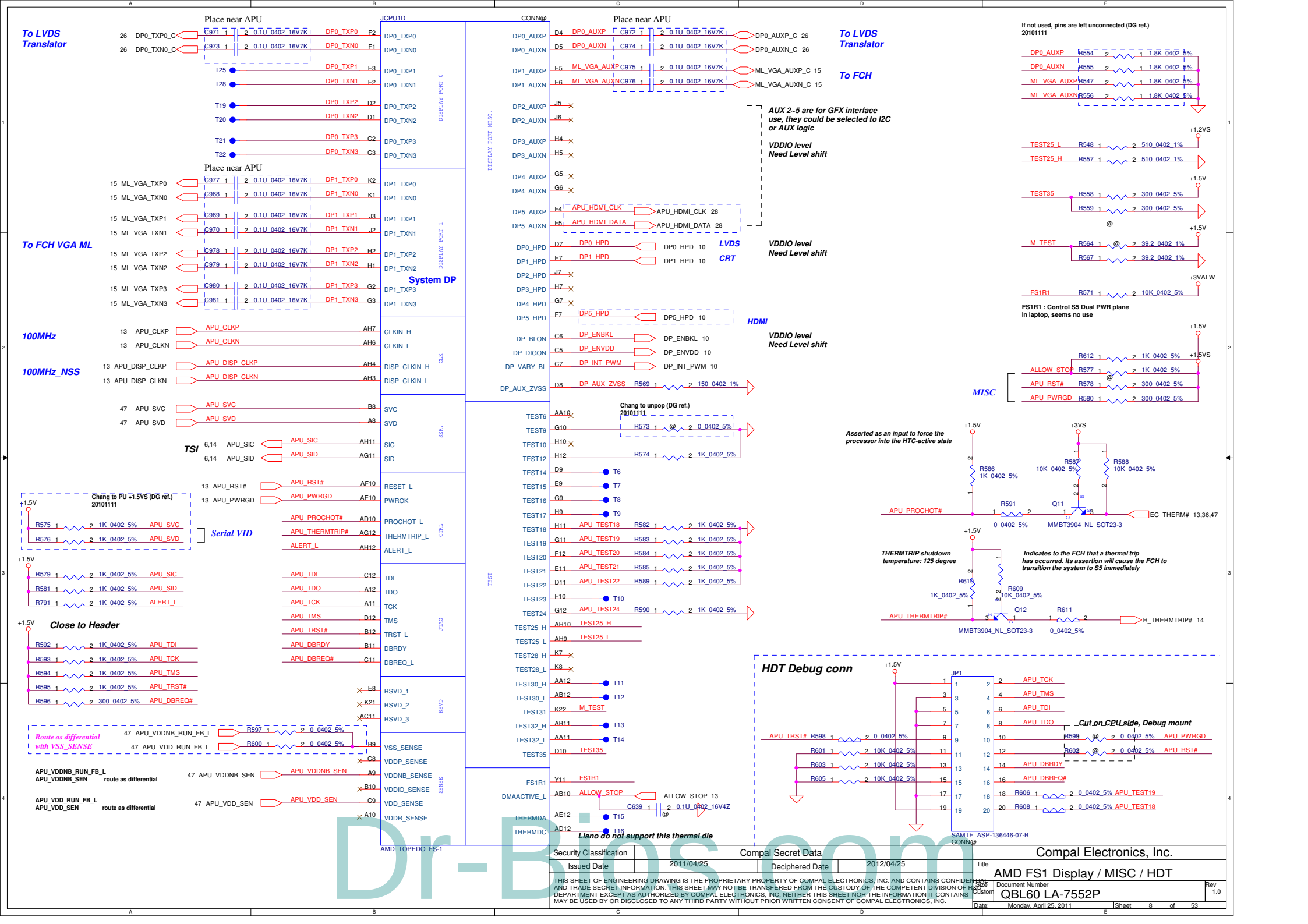

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Compal Electronics, Inc.

Title: AMD FS1 Display / MISC / HDT

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

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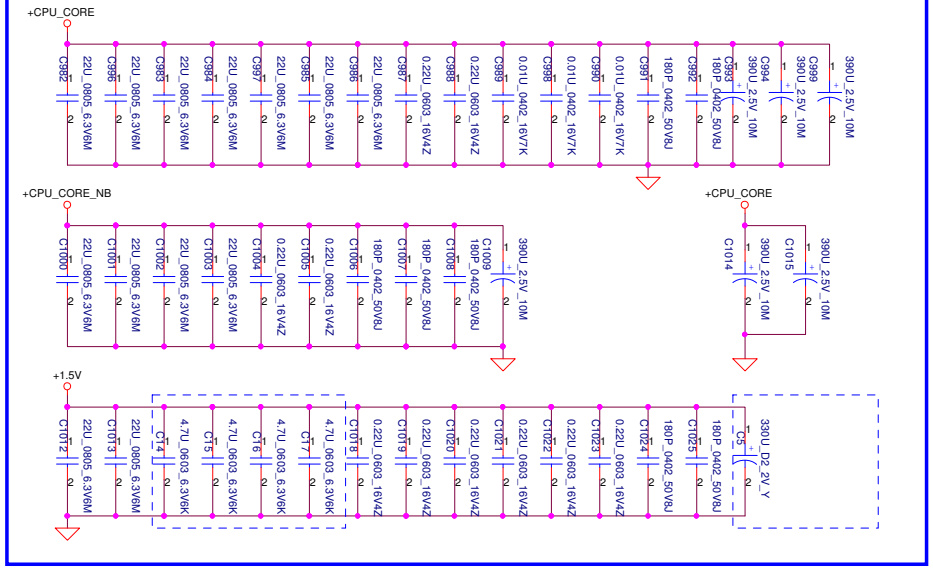
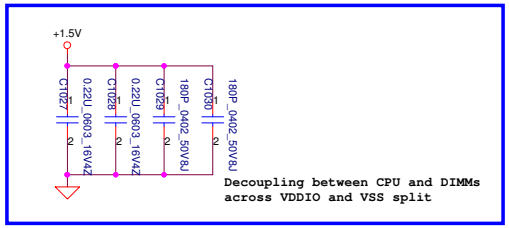
Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

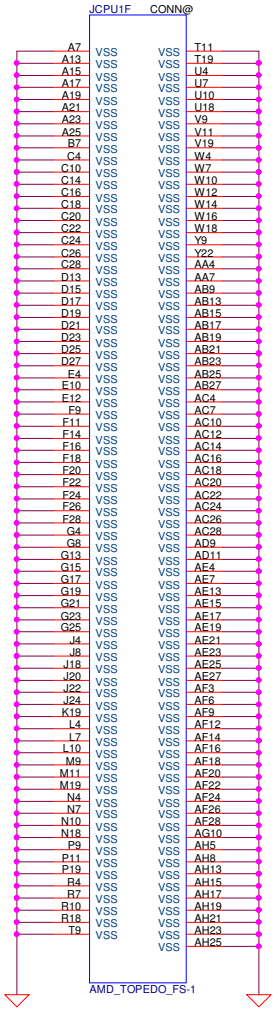
CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

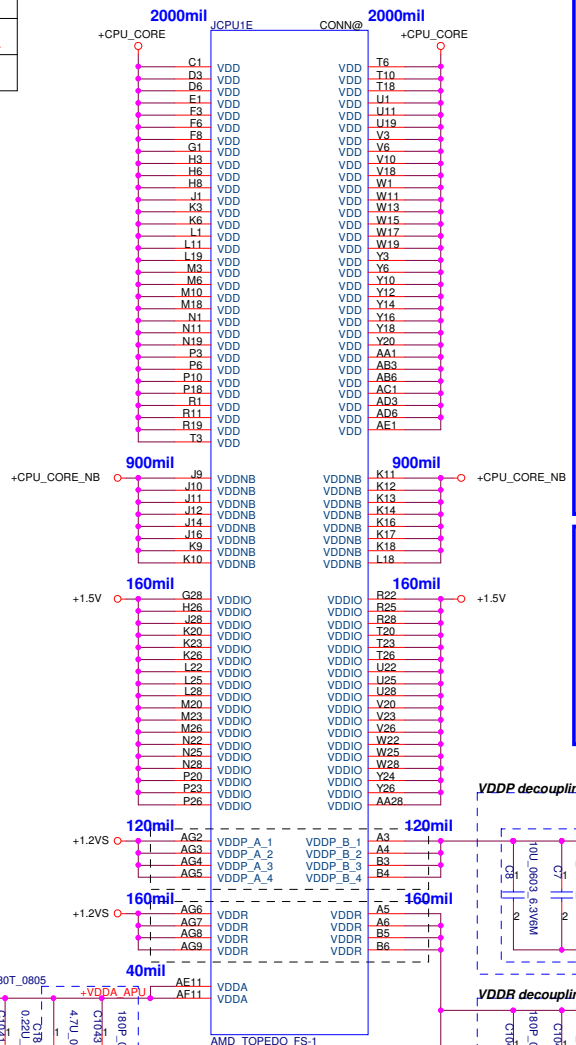
CPU BOTTOM SIDE DECOUPLING

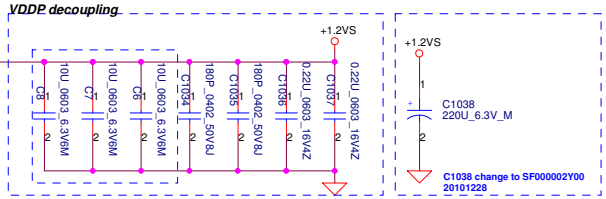




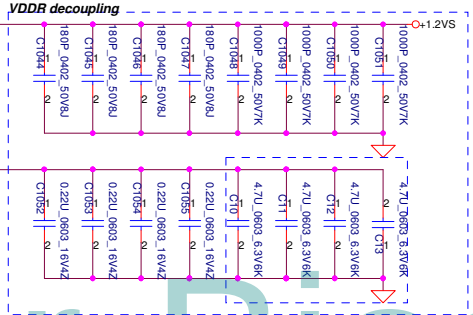
Decoupling between CPU and DIMMs across VDDIO and VSS split

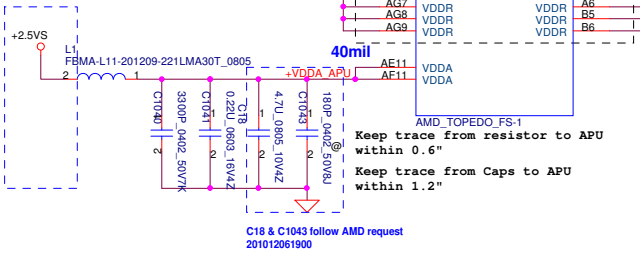






C1038 change to SF000002Y00
20101228





Keep trace from resistor to APU within 0.6"

Keep trace from Caps to APU within 1.2"

C18 & C1043 follow AMD request
201012061900

Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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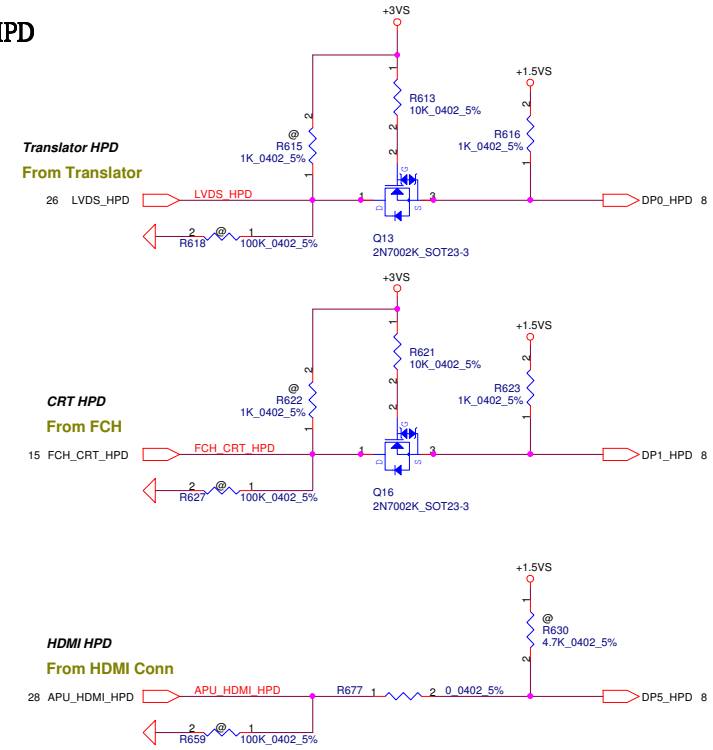
Compal Electronics, Inc.

Title: AMD FS1 PWR / GND

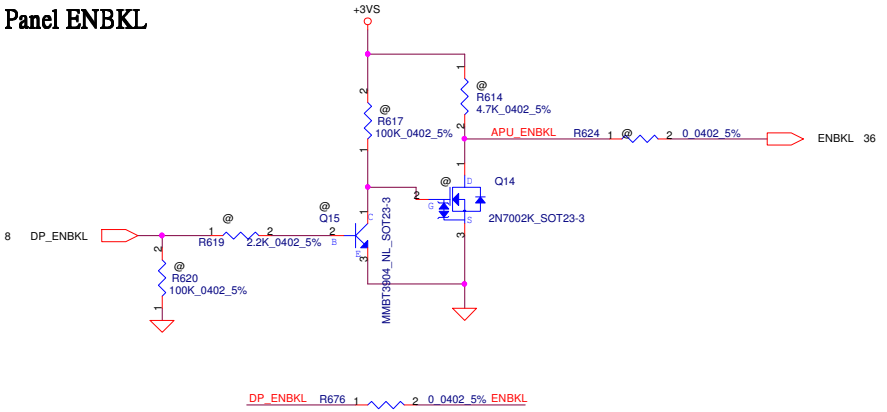
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 9 of 53

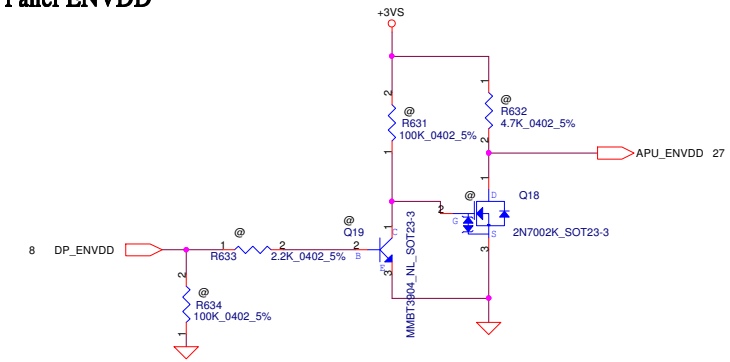
HPD



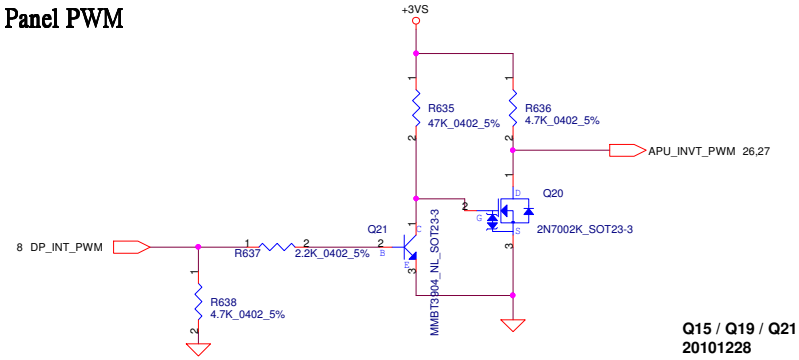
Panel ENBKL



Panel ENVDD



Panel PWM



Q15 / Q19 / Q21 change to SB000006A00 20101228

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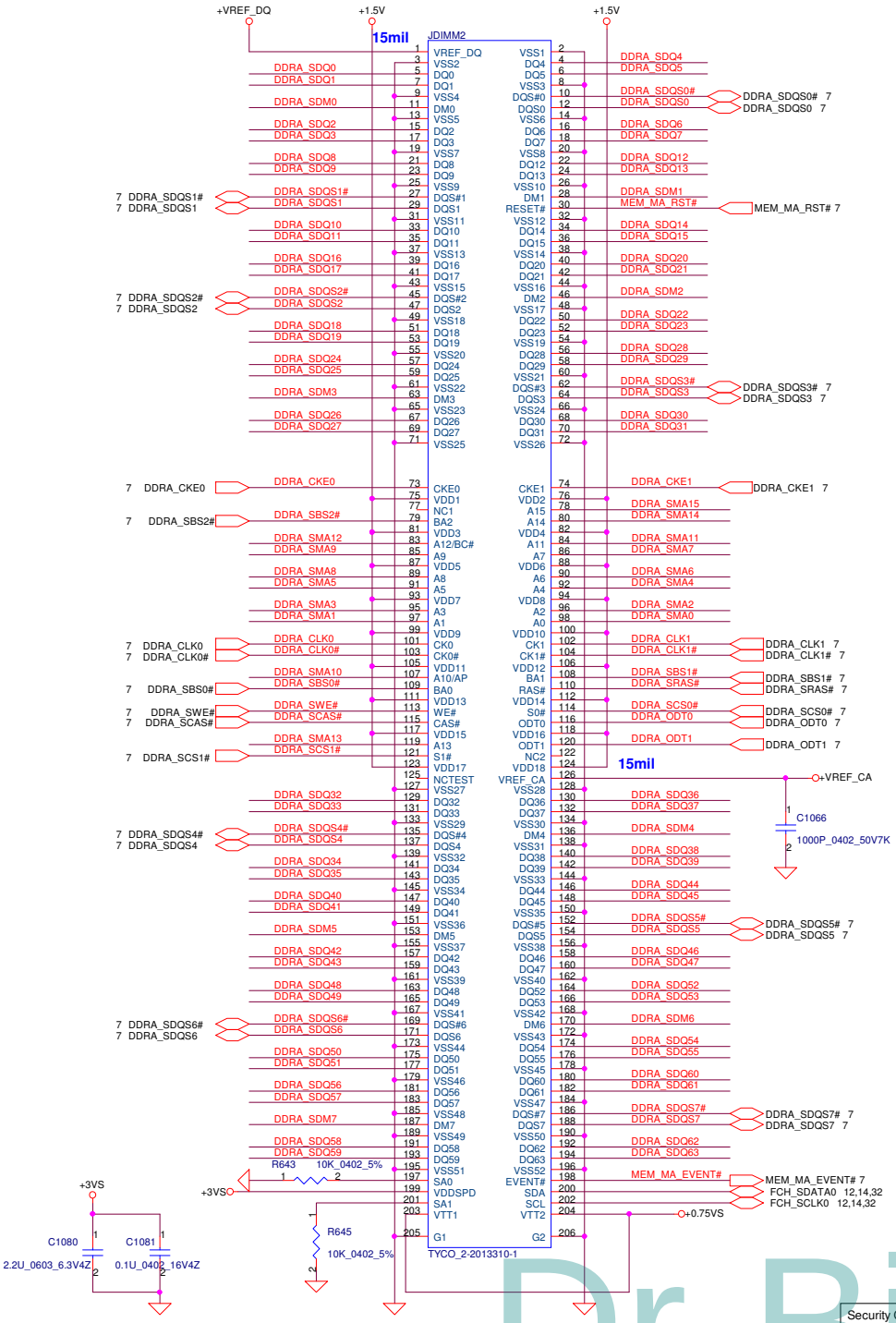
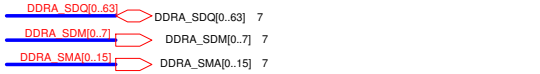
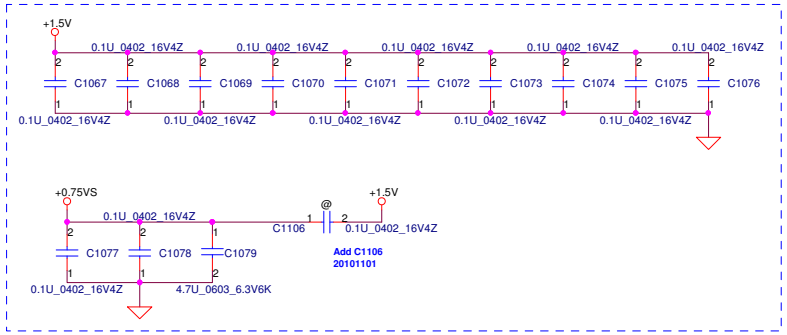
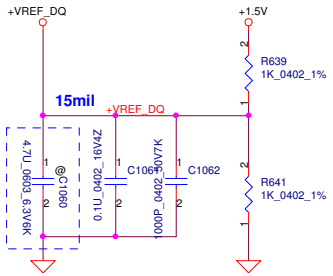
Title	AMD FS1 Singal Level Shifter		
Size	Document Number		Rev
Custom	QBL60 LA-7552P		1.0
Date:	Monday, April 25, 2011	Sheet 10 of 53	

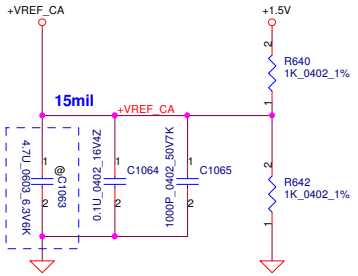




Place near DIMM1







DIMM_A STD H:9.2mm

<Address: 00>

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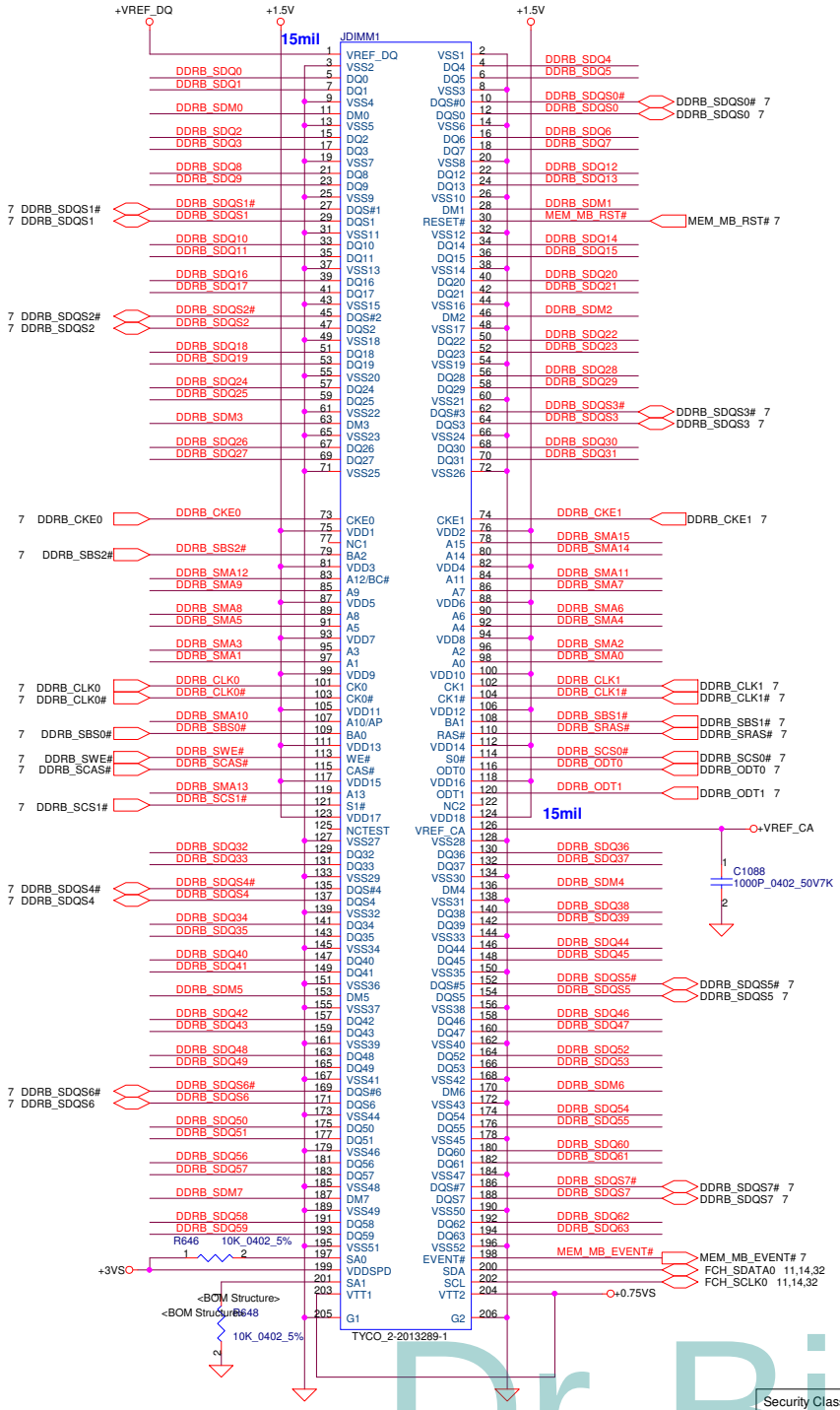
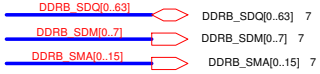
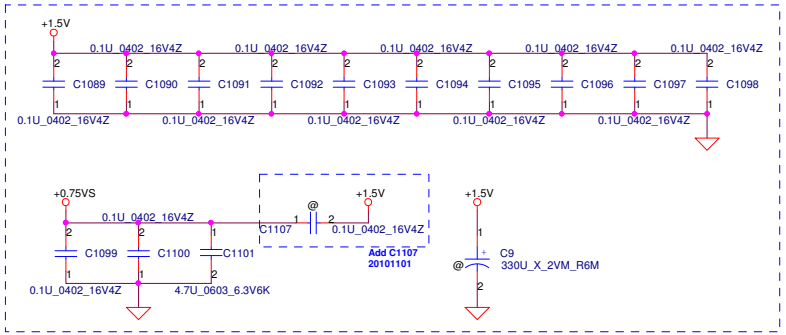
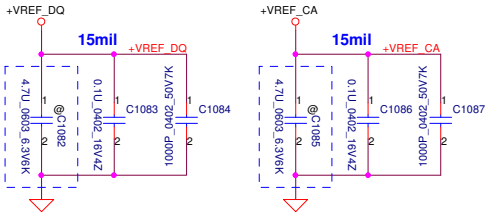
Compal Electronics, Inc.			
Title	DDRIII SO-DIMM 1		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
Date: Monday, April 25, 2011	Sheet 11 of 53		





Place near DIMM2





DIMM_B STD H:5.2mm

<Address: 01>

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Compal Electronics, Inc.			
Title	DDRIII SO-DIMM 2		
Size	Document Number		Rev
Custom	QBL60 LA-7552P		1.0
Date:	Monday, April 25, 2011	Sheet	12 of 53

PCI Host Bus Reset (To EC)

For "EXT" CLK mode, input to PCIE,

SS

NSS

APU DISP

APU

VGA

GLAN

WLAN

SS

GPP Port0 For USB30 on SUS/B
GPP Port1 For USB30 on M/B 20101103

For PCIE device reset on FS1 (GLAN,WLAN)

Level shift to ISL6267

Q38 change to SB000006A00 20101228

RTC BATT Conn.

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC

DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

for Clear CMOS

Close to HUDSON-M2

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Compal Electronics, Inc.	
Title	Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC
Size: Custom	Document Number: QBL60 LA-7552P
Rev	1.0
Date: Monday, April 25, 2011	Sheet 13 of 53

PCIE_RST2 : Reset PCIE device on Hudson2

U25D

HUDSON-2

THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

VGA_PD: Support MLDAC power save if connect
0: MLDAC power on
1: MLDAC power off

Modify 2010212-AMD request

Modify 2010212-AMD request

Modify 20101111

Modify 2010212-AMD request

For FCH internal debug use

Project SKU ID		
GPIO189 (use VGA)	L(NO) R44	H(YES) R43
GPIO190 (use PX)	L(NO) R46	H(YES) R45
GPIO191	L(15") R48	H(17") R47

Add Project ID Table 201011301600

HUDSON-M2_FCBGA656
M2@

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

USB1

Hudson-M2/M3 EHCI CTL DEV 19, Fn 2

CardReder

Hudson-M2/M3 EHCI CTL DEV 18, Fn 2

WLAN(BT)

CMOS

USB3

USB2

Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

On board USB Conn

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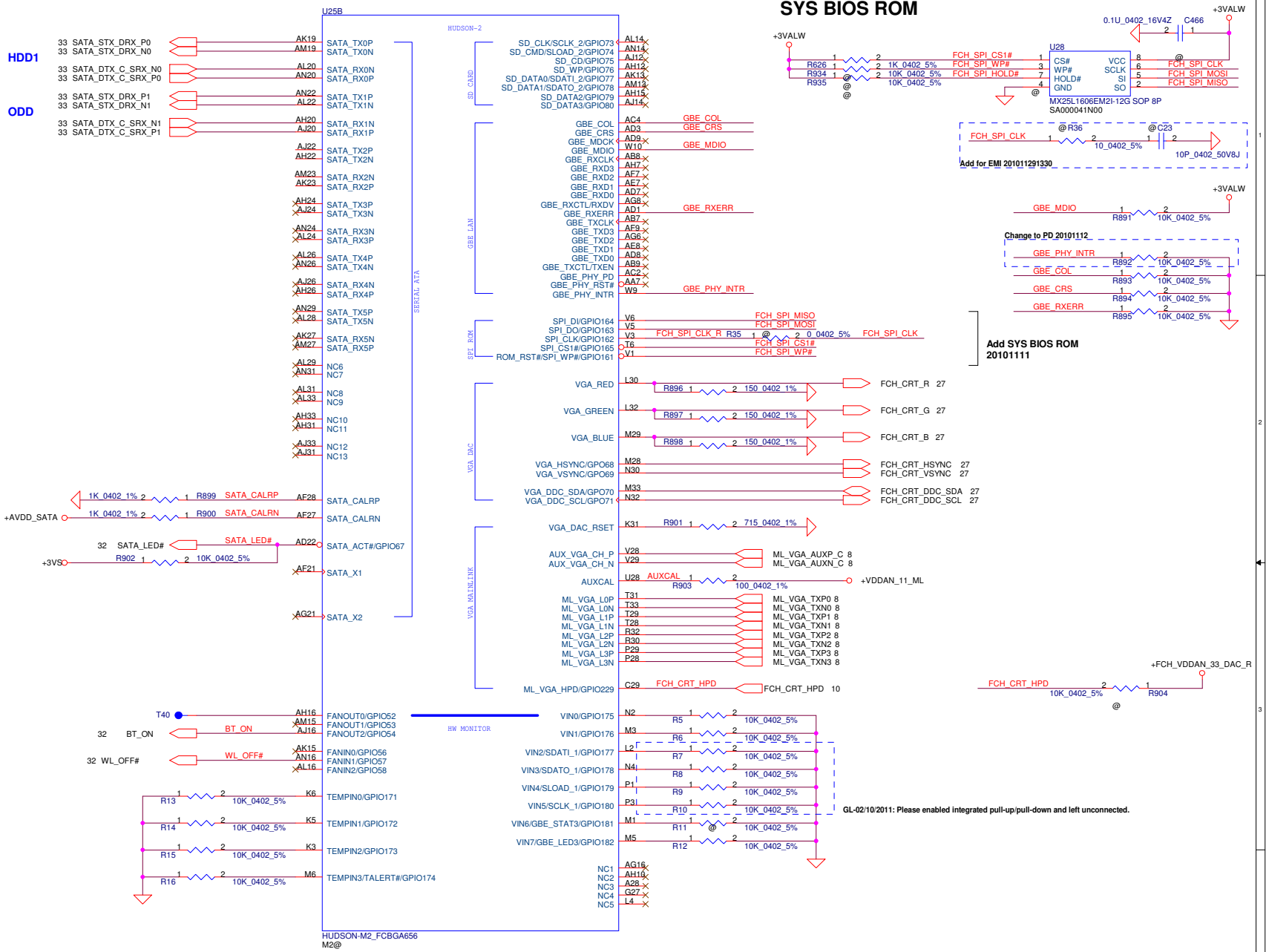
Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 14 of 53

SYS BIOS ROM



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Compal Electronics, Inc.			
Title	Hudson-M2/M3-SATA/GBE/HWM		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
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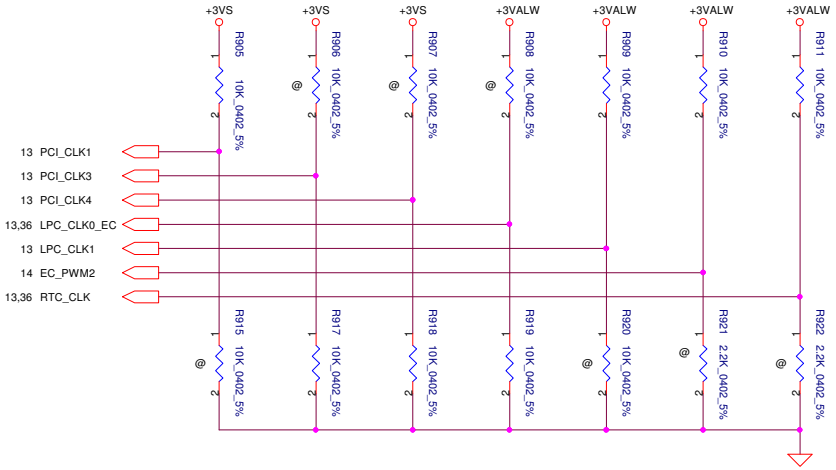
STRAP PINS

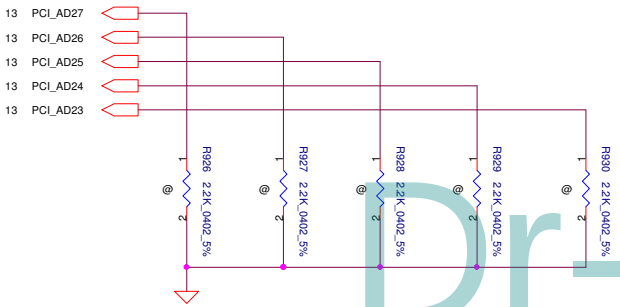
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

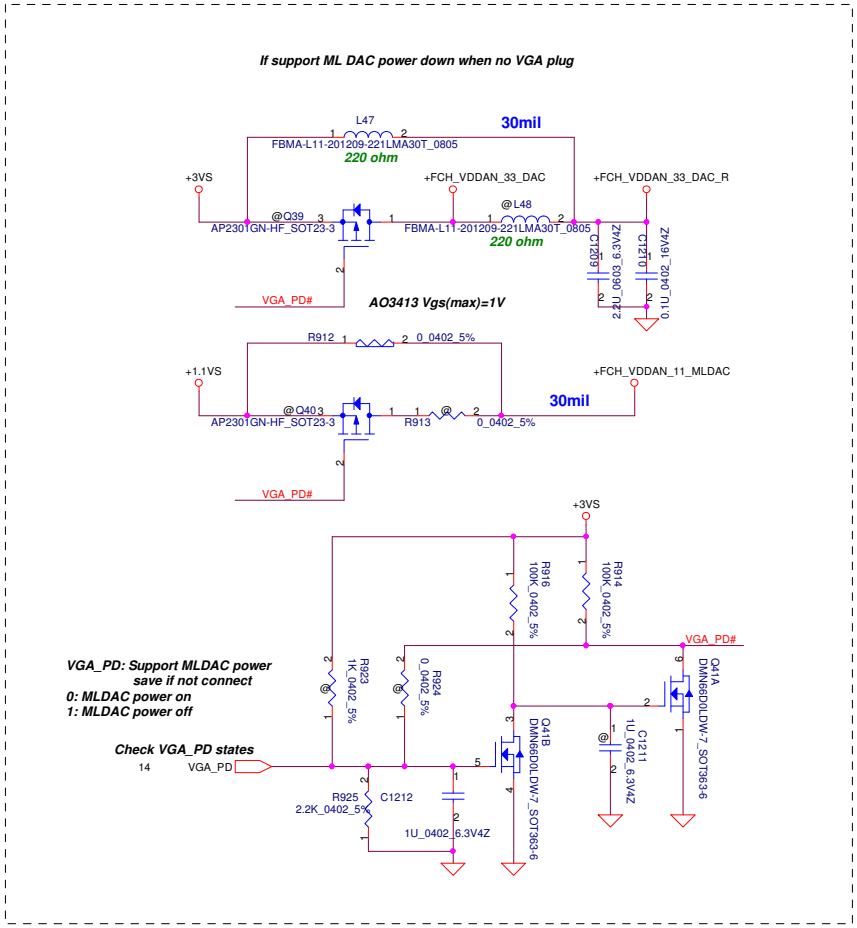


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Compal Electronics, Inc.	
Title	Hudson-M2/M3-STRAP
Size: Custom	Document Number: QBL60 LA-7552P
Rev	1.0
Date: Monday, April 25, 2011	Sheet 16 of 53

C1218 / C1219 / C1247 Change to SE00000I10
20101228

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB outputs

For A11: Cap = 1nF
For A12, Cap = DNI

R1242 change to 2.2uf-AMD request 20110212

Change to 0ohm-AMD request 20110212

change to four 1uf-AMD request 20110212

For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S Connected to VSS.

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

Connected to VSS through a dedicated via.

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Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 17 of 53

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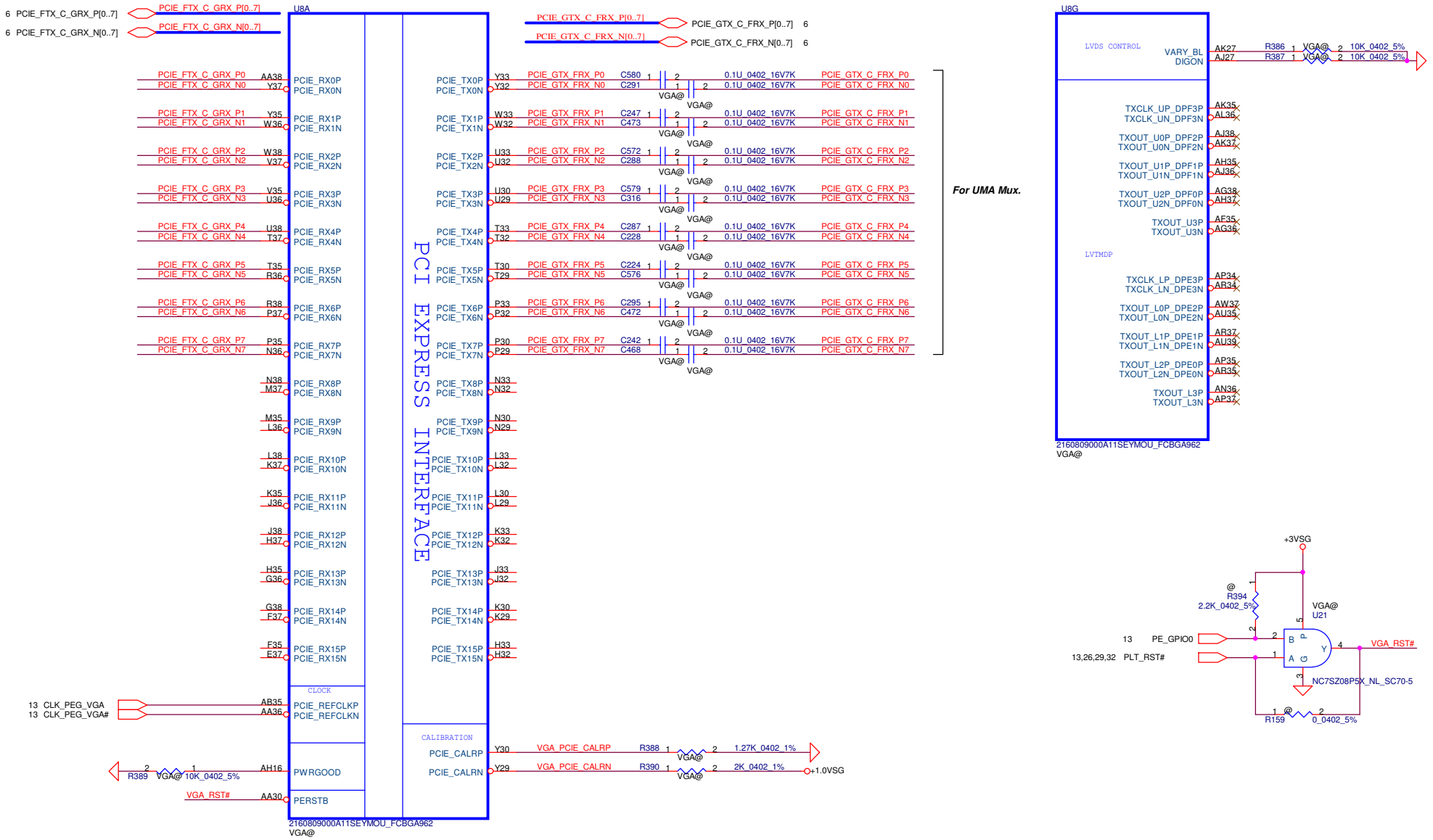
GFX PCIE LANE REVERSAL

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need



For UMA Mux.

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Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 18 of 53

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 128 MB 000 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

External VGA Thermal Sensor

U9 VGA@ ADM1032ARMZ-2REEL_MSOP8

VRAM ID

VRAM Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA000045330 64M16x8 K4W1G1646G-BC11	0	0	0	0
Samsung SA000047QA0 128M16x8 K4W2G1646C-HC11	0	0	0	1
Hynix SA000041S60 64M16x8 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16x8 H5TQ2G63BFR-11C	0	1	0	1

GPIO5 fast-power reduction:
HW control will casue display disturb should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N

GPIO7 Controls backlight on/off.
Active High ,need external PD
If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device
ON(1)/OFF(0) inter PD

Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

For ATI Cross fire
no use can NC

SM010030010
200ma 120ohm@100mhz DCR 0.2

Future ASIC call MLPS
OLD ASIC is Fan PWM

120ohm/0.3A

AMD ref:120ohm/0.3A

SM010030010
AMD ref:120ohm/0.3A
200ma 120ohm@100mhz DCR 0.2

NC on Whistler and Seymour

Back compatibility(Manhattan)

Whistler and Seymour
Except A2VSSQ change to TSVSSQ, others are NC

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

GPIO8 Serial-ROM output from ROM, GPIO9 Serial-ROM input to ROM. GPIO10 Serial-ROM clock to ROM. GPIO22 erternal BIOS-ROM enable	if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD if GPIO22 Low ,GPIO 11-13->CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010
GPIO8,GPIO9,GPIO10 no use can NC GPIO22 Enable need 3K PH ,no use must NC	

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 19 of 53

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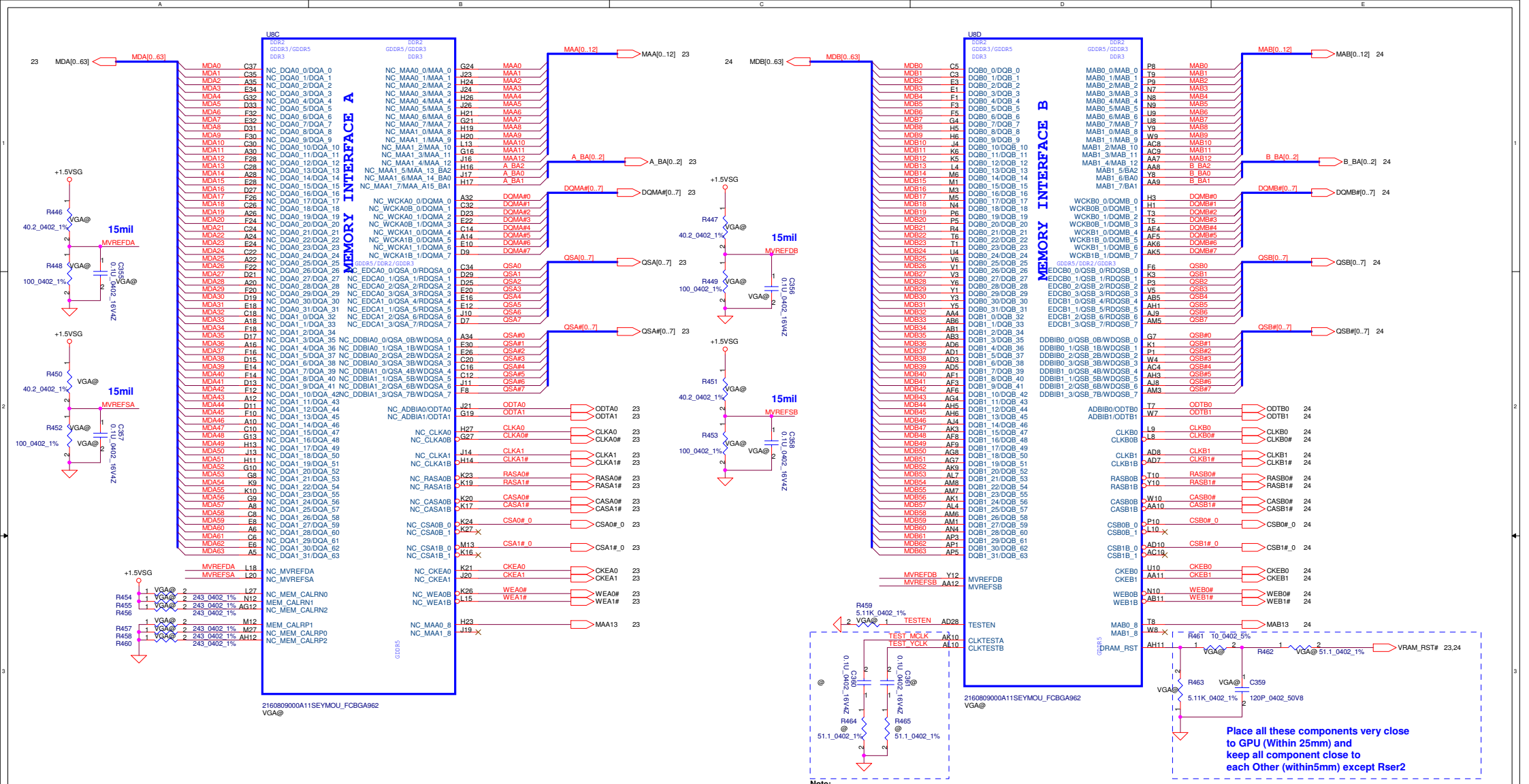

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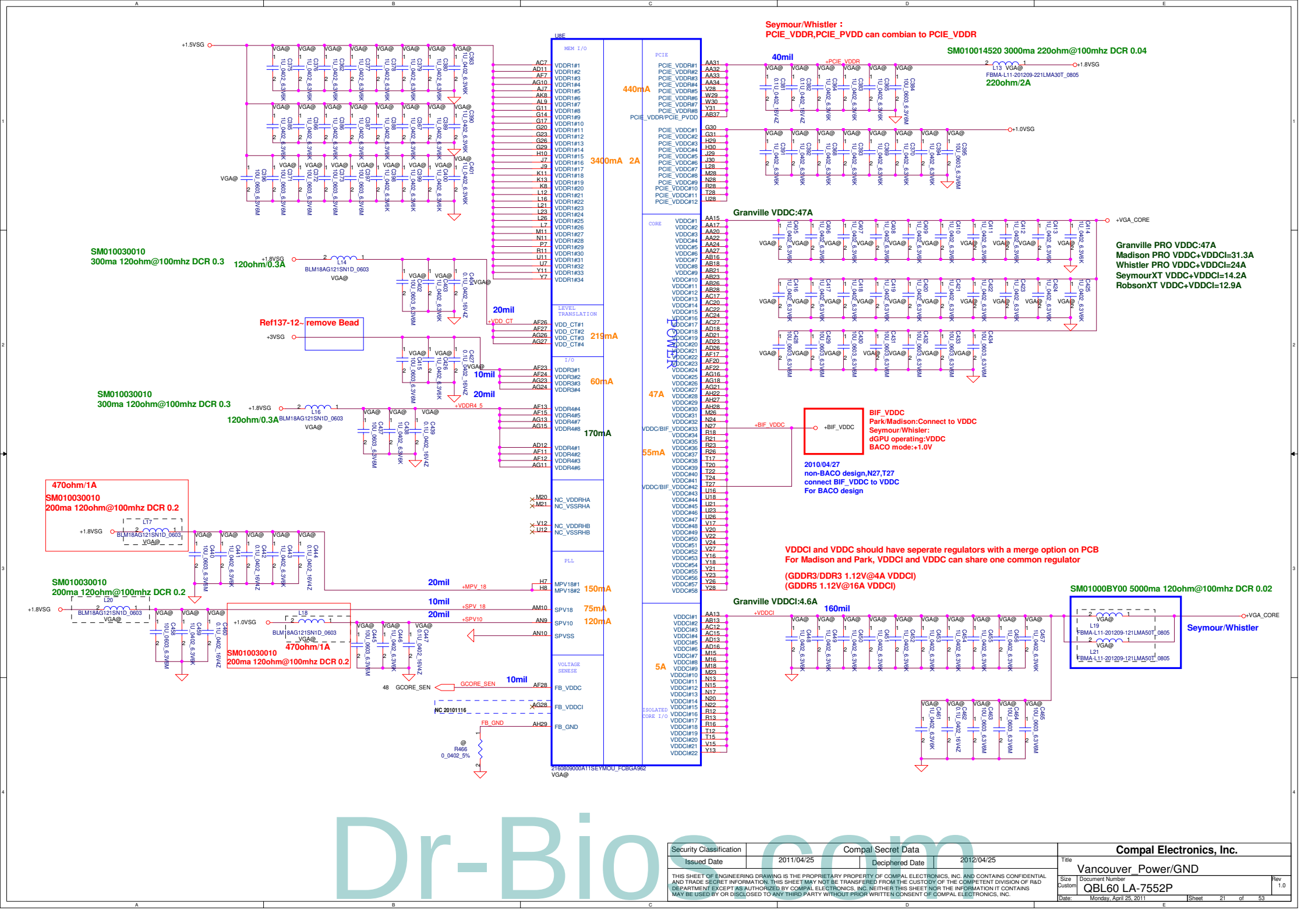
Compal Electronics, Inc.

Title: Vancouver_Memory

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 20 of 53



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Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size	Document Number	Rev
Custom	QBL60 LA-7552P	1.0

Date: Monday, April 25, 2011 | Sheet 21 of 53

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

PCIE_VSS#1 … PCIE_VSS#35

GND

GND#1 … GND#98

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW39

2160809000A11SEYMOU_FCBGA962
VGA@

REF137-13 update

U8H

DP C/D POWER

Manhatann:300mA
Seymour:150mA

20mil +DPABCD_VDD18 AP20 AP21
DPCD/DPC_VDD18#1 DPCD/DPC_VDD18#2

20mil +DPABCD_VDD10 AP13 AT13
DPCD/DPC_VDD10#1 DPCD/DPC_VDD10#2

DP/DPC_VSSR#1 AN17
DP/DPC_VSSR#2 AP16
DP/DPC_VSSR#3 AP17
DP/DPC_VSSR#4 AW14
DP/DPC_VSSR#5 AW16

20mil +DPABCD_VDD18 AP22 AP23
DPCD/DPD_VDD18#1 DPCD/DPD_VDD18#2

Manhatann:220mA
Seymour:110mA

20mil +DPABCD_VDD10 AP14 AP15
DPCD/DPD_VDD10#1 DPCD/DPD_VDD10#2

DP/DPD_VSSR#1 AN19
DP/DPD_VSSR#2 AP18
DP/DPD_VSSR#3 AP19
DP/DPD_VSSR#4 AW20
DP/DPD_VSSR#5 AW22

R467 150_0402_1% VGA@ AW18

DPCD_CALR

DP E/F POWER

DP mode:300mA
LVDS mode:440mA

20mil +DPEF_VDD18 AH34 AJ34
DPEF/DPE_VDD18#1 DPEF/DPE_VDD18#2

20mil +DPEF_VDD10 AL33 AM33
DPEF/DPE_VDD10#1 DPEF/DPE_VDD10#2

DP/DPE_VSSR#1 AN34
DP/DPE_VSSR#2 AP39
DP/DPE_VSSR#3 AR39
DP/DPE_VSSR#4 AU37

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L26 MBK1608221YZF_2P
+1.8VSG VGA@
FootPrint
C478 10U_0603_6.3V6M
C479 1U_0402_6.3V6K
C480 0.1U_0402_16V4Z

DP mode:220mA
LVDS mode:240mA

20mil +DPEF_VDD18 AF34 AG34
DPEF/DPF_VDD18#1 DPEF/DPF_VDD18#2

20mil +DPEF_VDD10 AK33 AK34
DPEF/DPF_VDD10#1 DPEF/DPF_VDD10#2

DP/DPF_VSSR#1 AF39
DP/DPF_VSSR#2 AH39
DP/DPF_VSSR#3 AK39
DP/DPF_VSSR#4 AL34
DP/DPF_VSSR#5 AM34

R470 VGA@ 150_0402_1% AM39

DPEF_CALR

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L27 MBK1608221YZF_2P
+1.0VSG VGA@
FootPrint
C481 10U_0603_6.3V6M
C482 1U_0402_6.3V6K
C483 0.1U_0402_16V4Z

PX_EN PX_EN 25,36

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

DP A/B POWER

20mil +DPABCD_VDD18 AN24 AP24
DPAB/DPA_VDD18#1 DPAB/DPA_VDD18#2
300mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23 MBK1608221YZF_2P
+1.8VSG VGA@
FootPrint
C469 10U_0603_6.3V6M
C470 0.1U_0402_16V4Z
C471 1U_0402_6.3V6K

20mil +DPABCD_VDD10 AP31 AP32
DPAB/DPA_VDD10#1 DPAB/DPA_VDD10#2

DP/DPA_VSSR#1 AN27
DP/DPA_VSSR#2 AP27
DP/DPA_VSSR#3 AP28
DP/DPA_VSSR#4 AW24
DP/DPA_VSSR#5 AW26

20mil +DPABCD_VDD18 AP25 AP26
DPAB/DPB_VDD18#1 DPAB/DPB_VDD18#2

20mil +DPABCD_VDD10 AW33 AP33
DPAB/DPB_VDD10#1 DPAB/DPB_VDD10#2
220mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L25 MBK1608221YZF_2P
+1.0VSG VGA@
FootPrint
C475 0.1U_0402_16V4Z
C476 1U_0402_6.3V6K
C477 10U_0603_6.3V6M

DP/DPB_VSSR#1 AN29
DP/DPB_VSSR#2 AP29
DP/DPB_VSSR#3 AP30
DP/DPB_VSSR#4 AW30
DP/DPB_VSSR#5 AW32

R468 150_0402_1% VGA@ AW28

DPAB_CALR

DP PLL POWER

20mA 10mil +DPABCD_VDD18 AU28 AV27
DPAB_VDD18/DPA_PVDD
DP_VSSR/DPA_PVSS

20mA 10mil +DPABCD_VDD18 AV29 AR28
DPAB_VDD18/DPB_PVDD
DP_VSSR/DPB_PVSS

20mA 10mil +DPABCD_VDD18 AU18 AV17
DPCD_VDD18/DPC_PVDD
DP_VSSR/DPC_PVSS

20mA 10mil +DPABCD_VDD18 AV19 AR18
DPCD_VDD18/DPD_PVDD
DP_VSSR/DPD_PVSS

20mA 10mil +DPEF_VDD18 AM37 AN38
DPEF_VDD18/DPE_PVDD
DP_VSSR/DPE_PVSS

20mA 10mil +DPEF_VDD18 AL38 AM35
DPEF_VDD18/DPF_PVDD
DP_VSSR/DPF_PVSS

2160809000A11SEYMOU_FCBGA962
VGA@

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

DP-Bios.com

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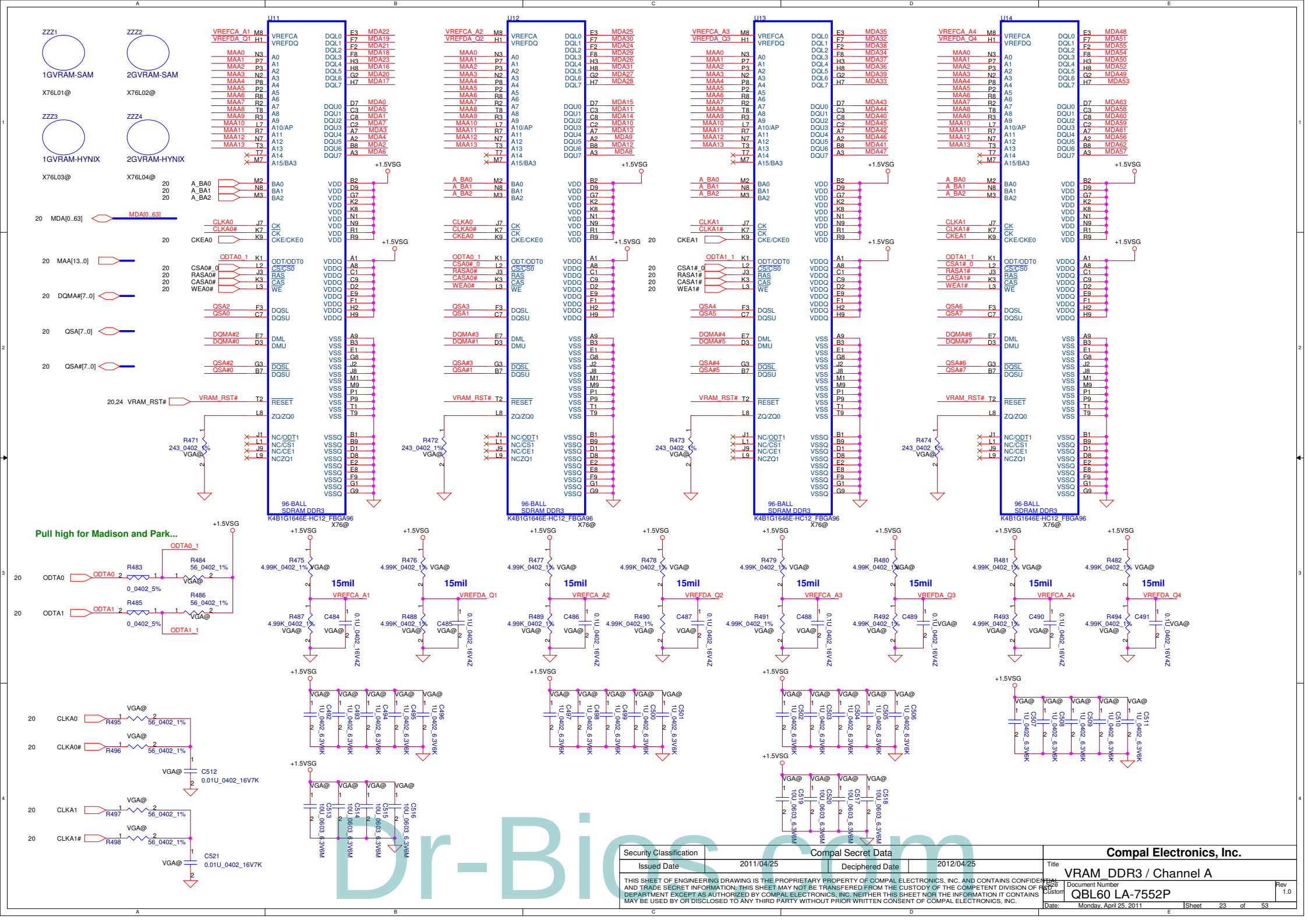
Title: Vancouver_Power/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 22 of 53


ZZZ1
1GVRAM-SAM
X76L01@
ZZZ2
2GVRAM-SAM
X76L02@
ZZZ3
1GVRAM-HYNIX
X76L03@
ZZZ4
2GVRAM-HYNIX
X76L04@
U11
U12
U13
U14
96-BALL SDRAM DDR3
K4B1G1646E-HC12_FBGA96
X76@
+1.5VSG
VRAM_RST#
Pull high for Madison and Park...
15mil
Security Classification
Compal Secret Data
Issued Date
2011/04/25
Deciphered Date
2012/04/25
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Title
VRAM_DDR3 / Channel A
Size
Custom
Document Number
QBL60 LA-7552P
Rev
1.0
Date:
Monday, April 25, 2011
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of
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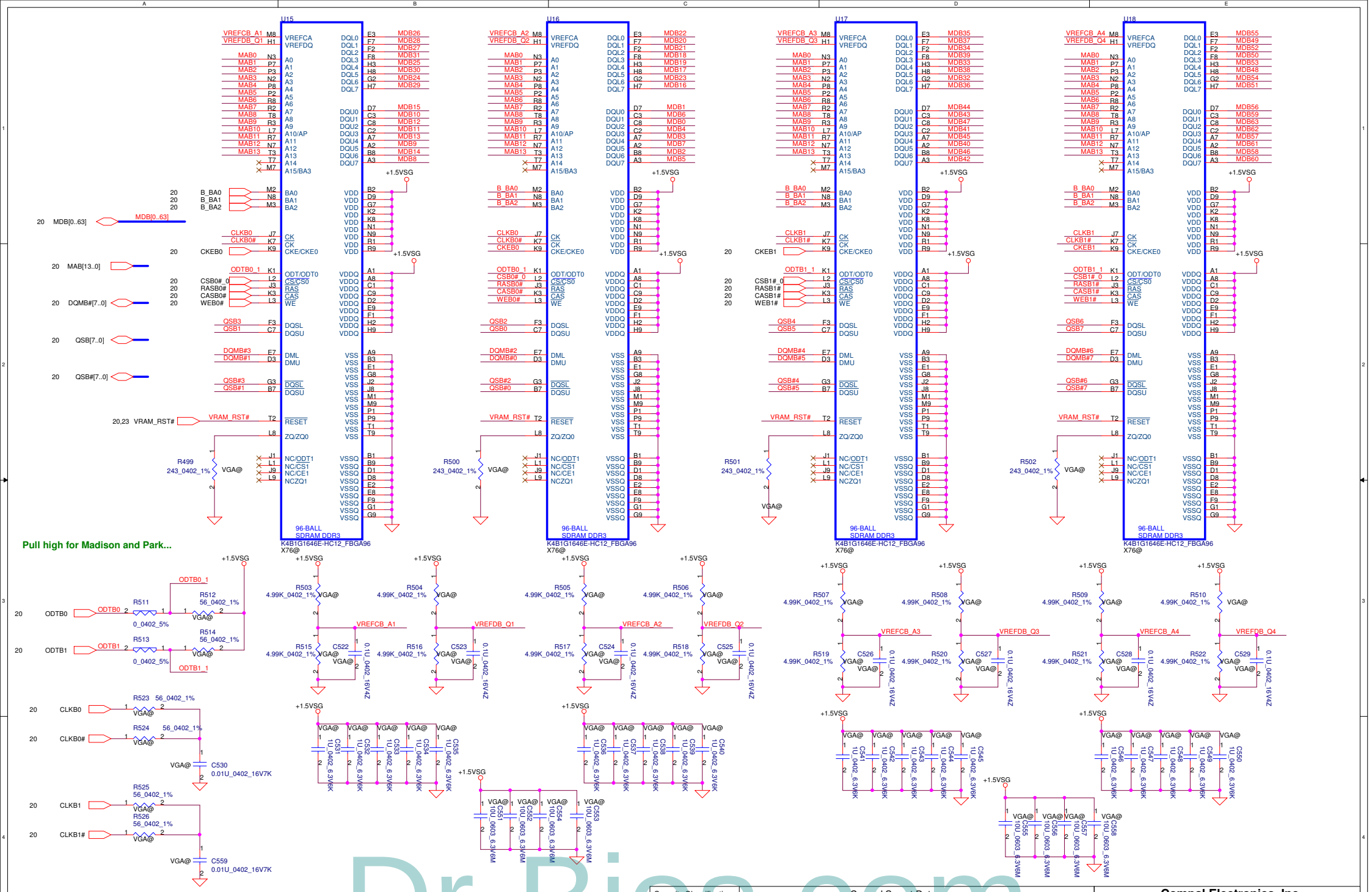

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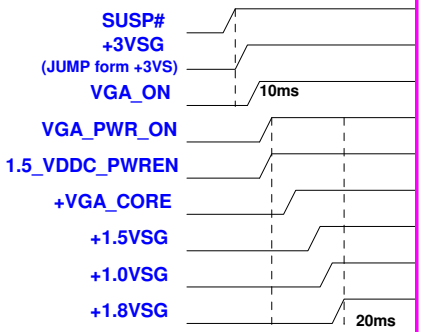
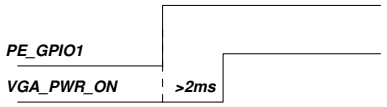
Title	VRAM_DDR3 / Channel B		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
Date: Monday, April 25, 2011	Sheet 24 of 53		

Power Sequence of Whistler and Seymour

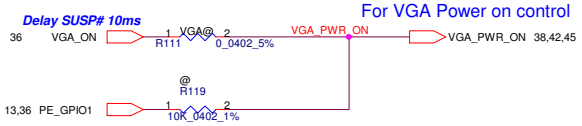


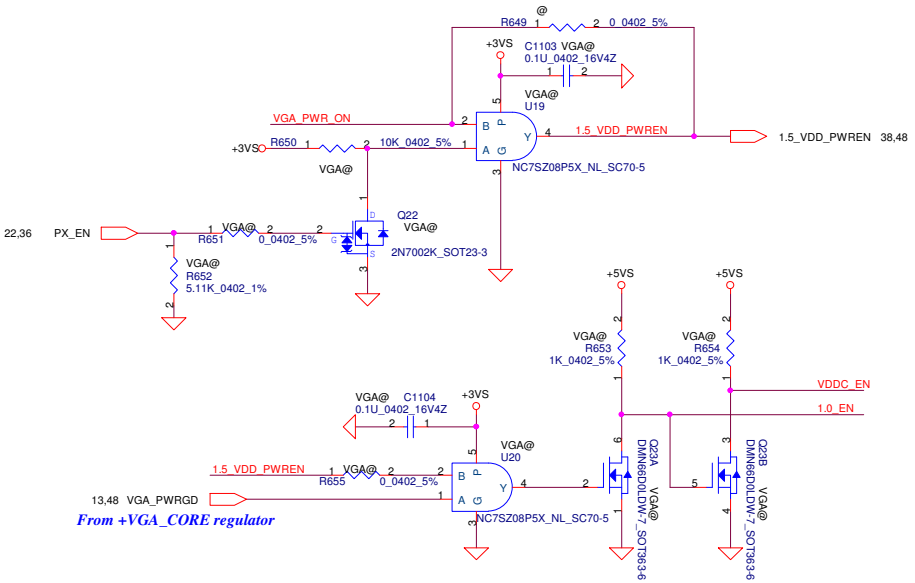
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

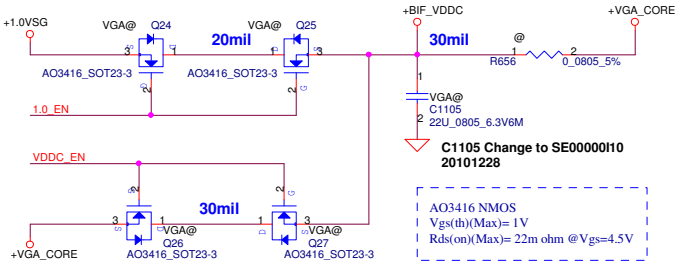


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN







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Issued Date	2011/04/25	Deciphered Date	2012/04/25
Title	VGA power sequence and BACO		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
Date: Monday, April 25, 2011	Sheet 25 of 53		

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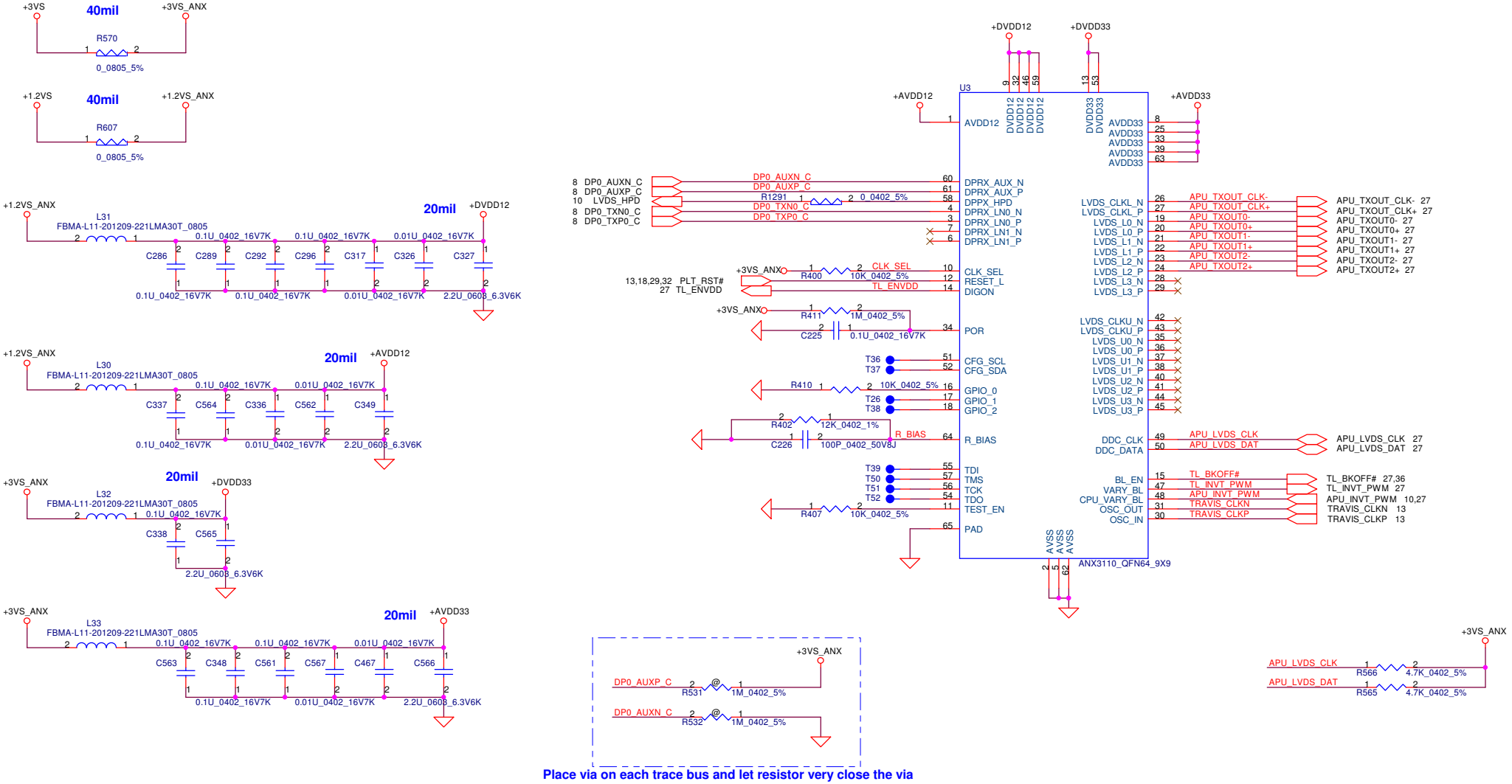

Place via on each trace bus and let resistor very close the via

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Compal Electronics, Inc.

Title: ***LVDS Translator-ANX3110***

Size	Document Number	Rev
Custom	QBL60 LA-7552P	1.0

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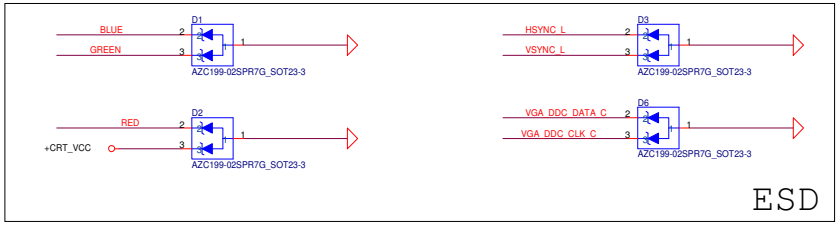
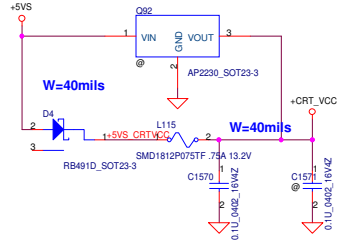
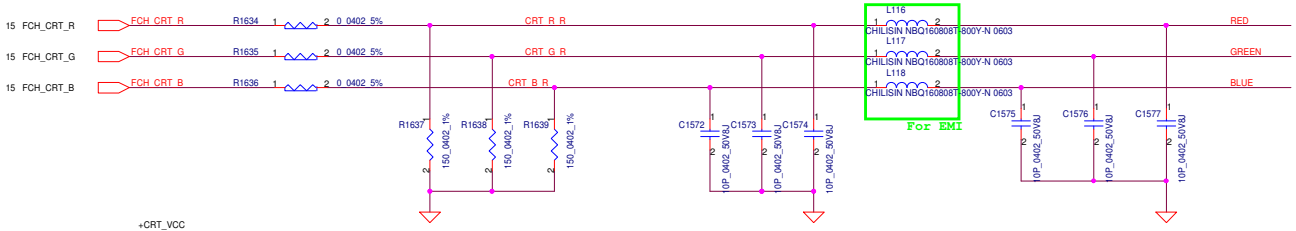
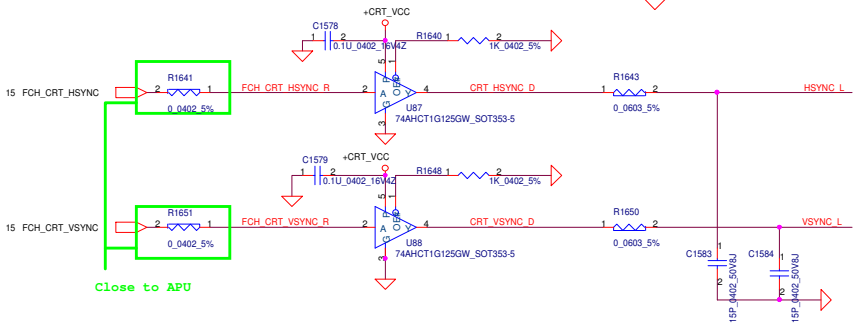
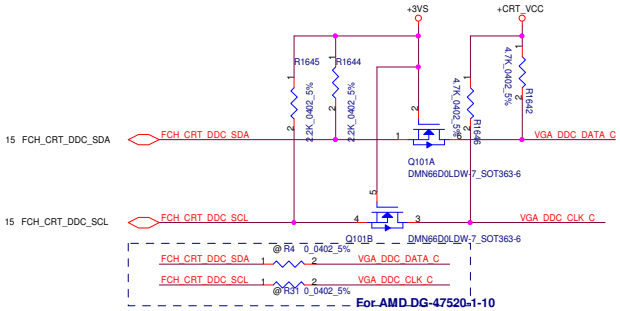
CRT

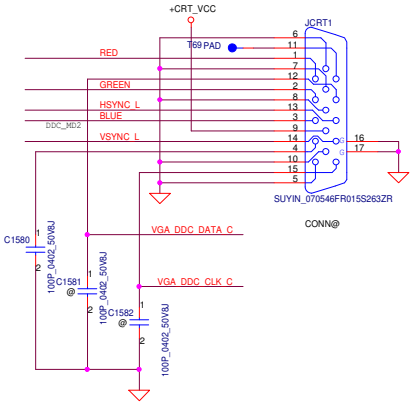




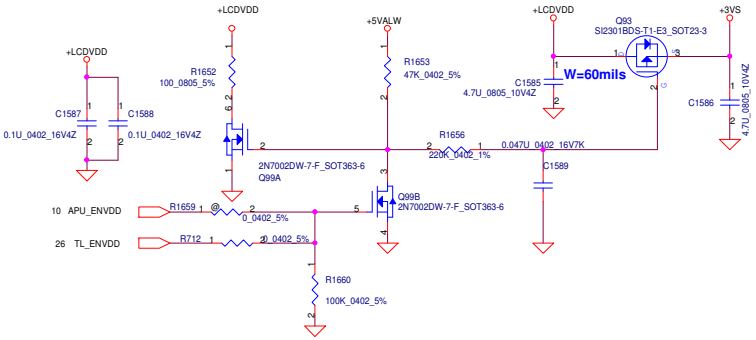


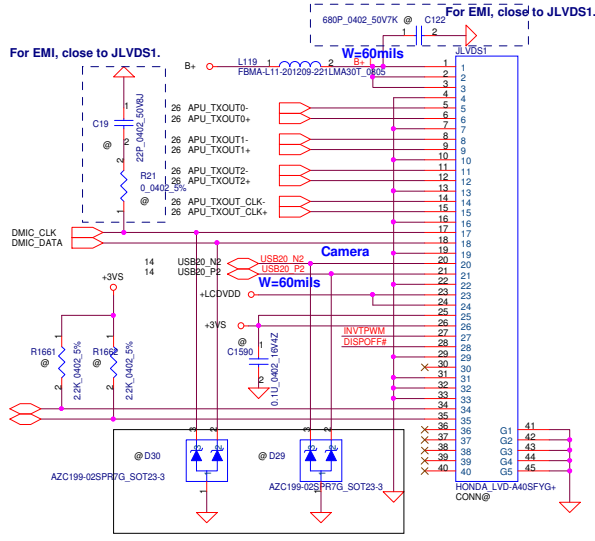




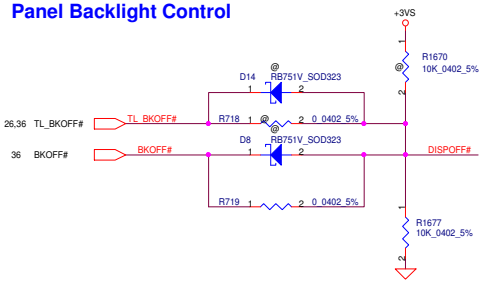


Panel LCDVDD Control

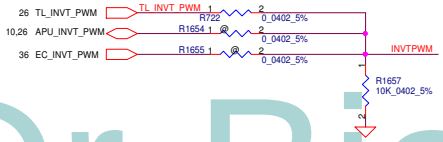




Panel Backlight Control



Panel PWM Control



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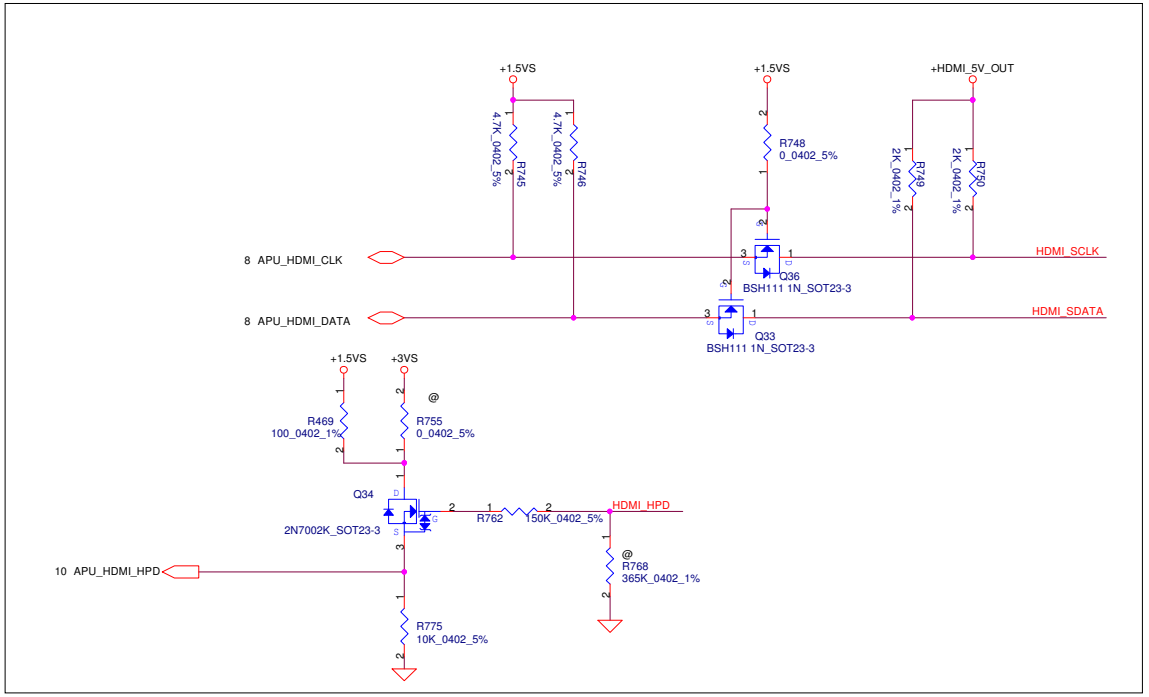
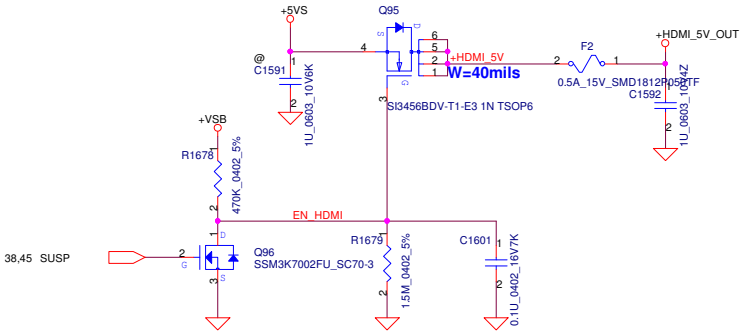
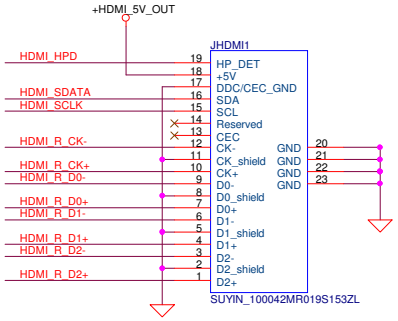
Title	P10-LVDS/CRT CONN		
Size C	Document Number QBL60 LA-7552P		Rev 1.0
Date: Monday, April 25, 2011	Sheet 27 of 53		



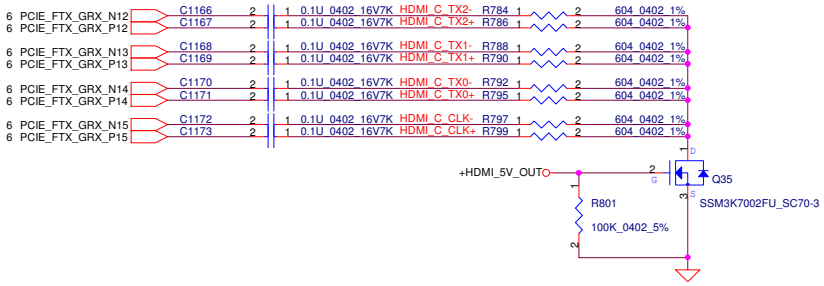


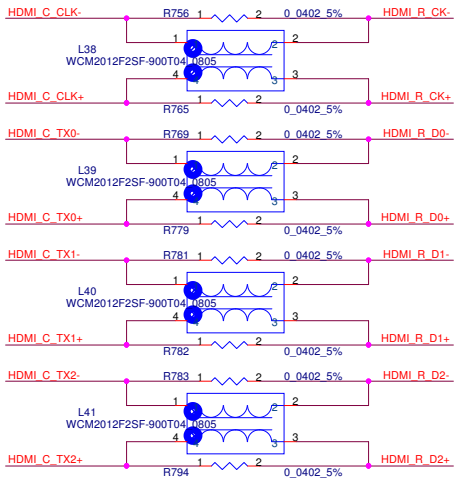


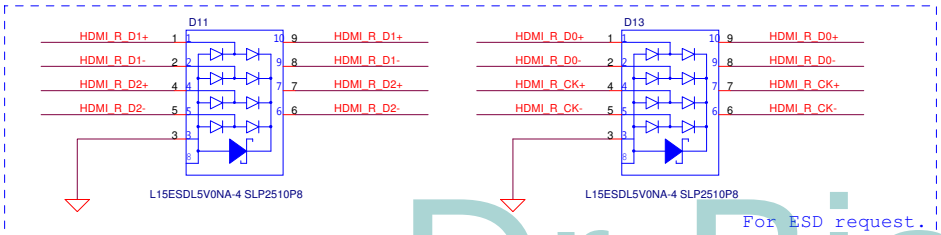
From APU

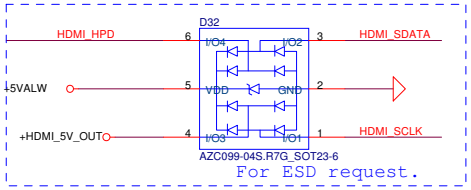
Near the connector

UMA use 604 ohm
VGA use 499 ohm









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Compal Electronics, Inc.

Title: HDMI Connector

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0

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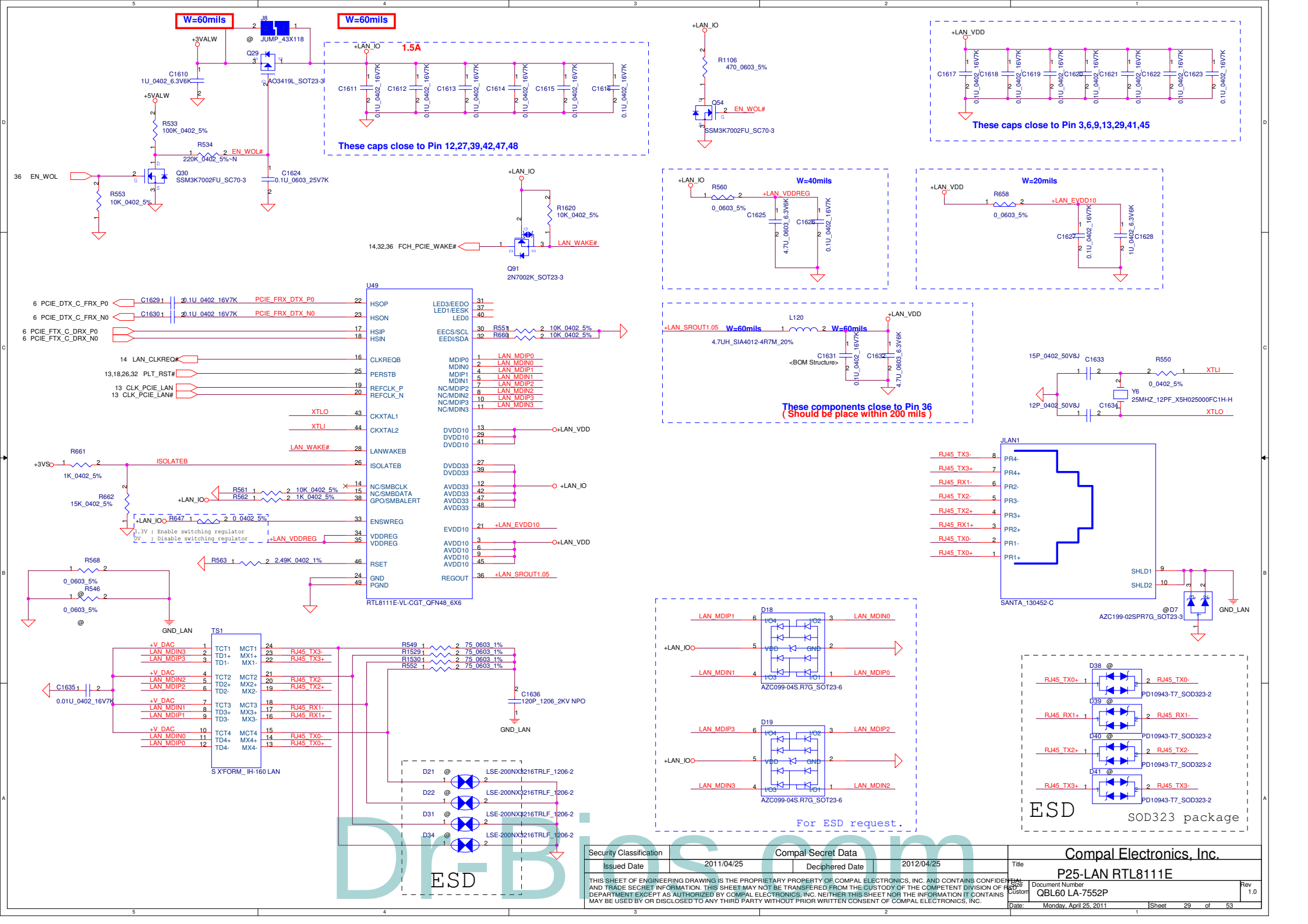

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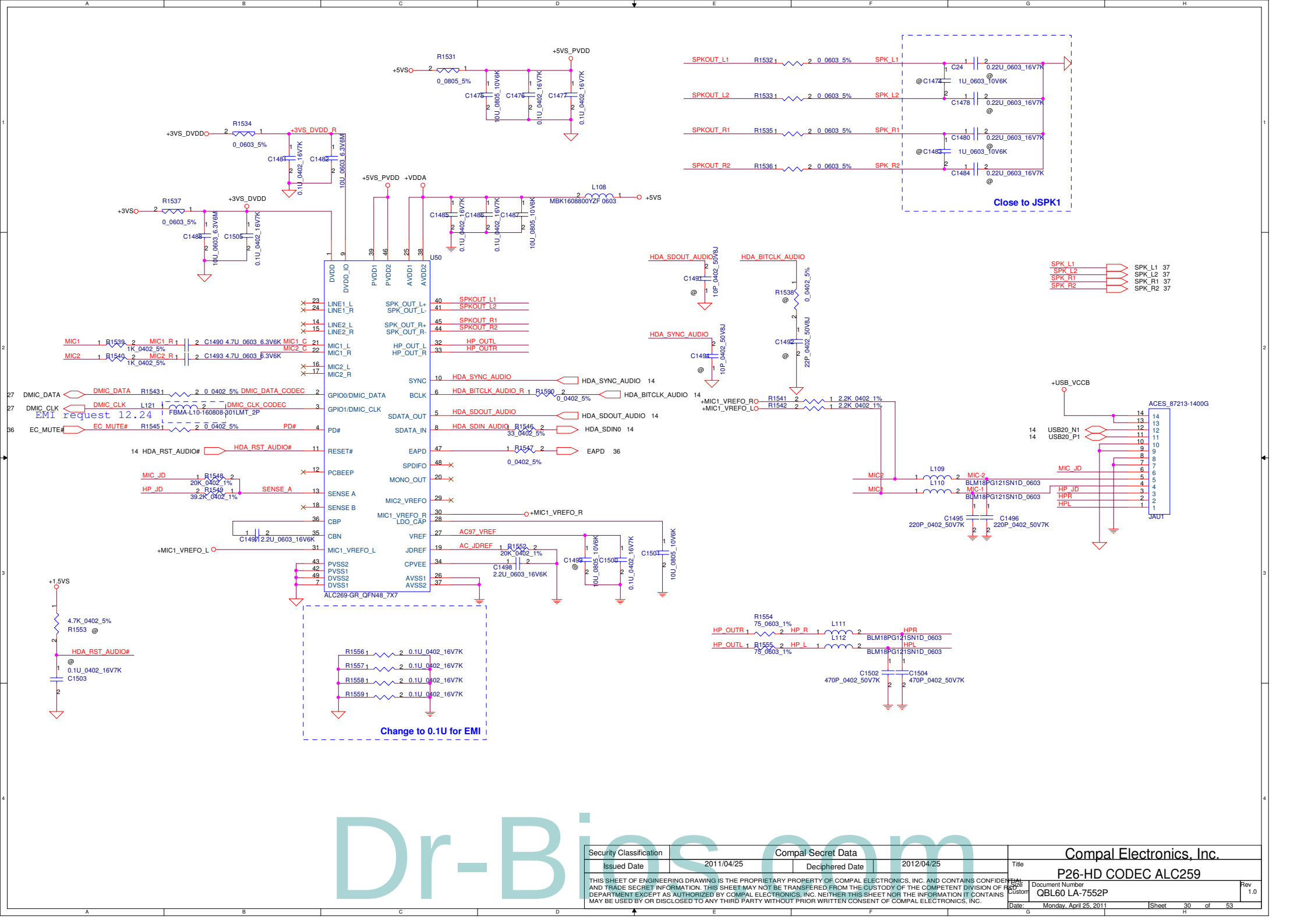
ALC269-GR_QFN48_7X7
U50
Close to JSPK1
Change to 0.1U for EMI
EMI request 12.24
ACES_87213-1400G
JAU1
Compal Electronics, Inc.
P26-HD CODEC ALC259
QBL60 LA-7552P
Security Classification
Compal Secret Data
Issued Date
2011/04/25
Deciphered Date
2012/04/25
Monday, April 25, 2011
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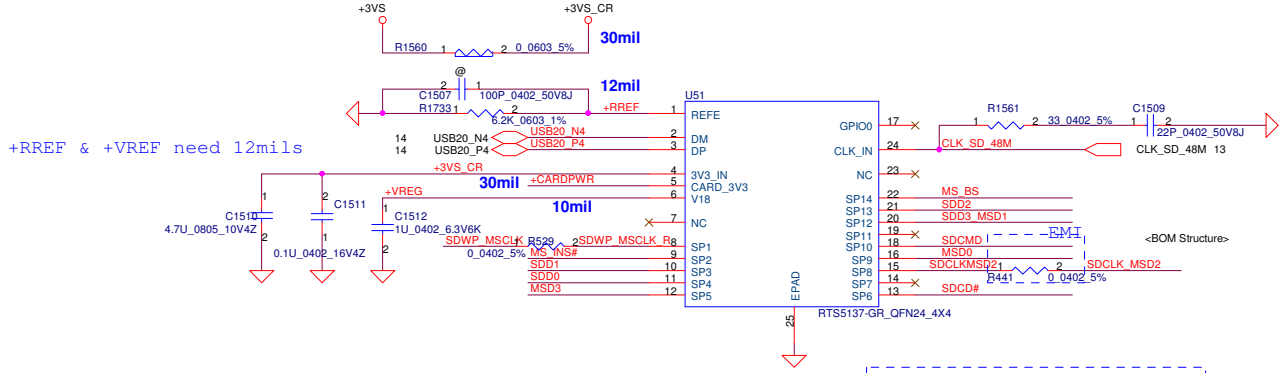
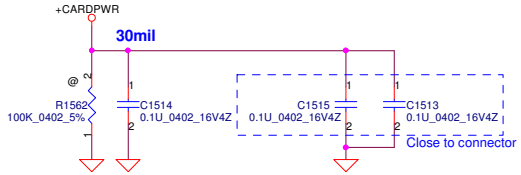
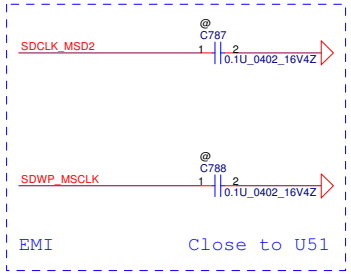
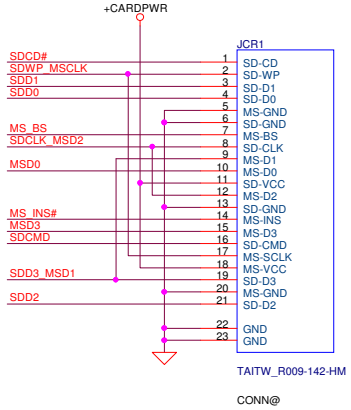
Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector







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Compal Electronics, Inc.			
Title	P27-RTS5137 Media Card Controller		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
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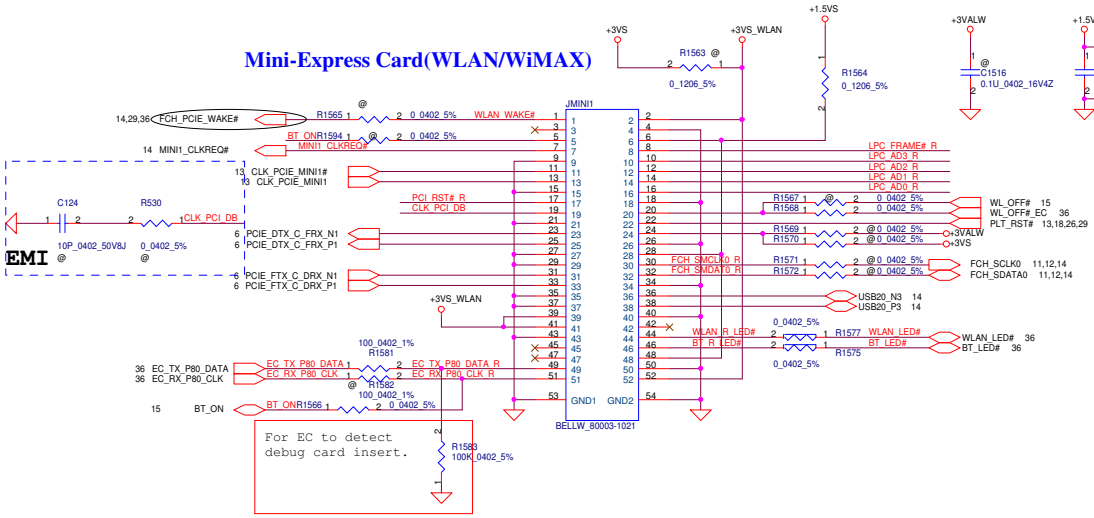
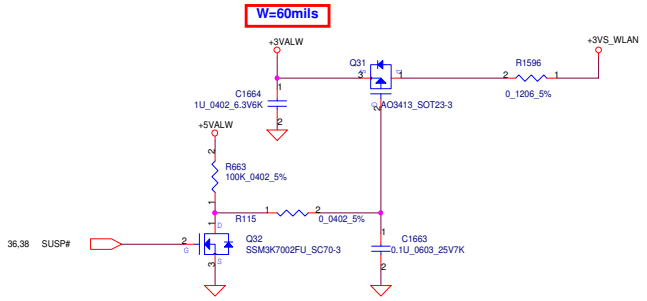
Mini-Express Card for WLAN/WiMAX(Half)

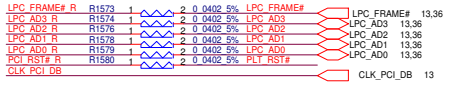
Mini-Express Card(WLAN/WiMAX)



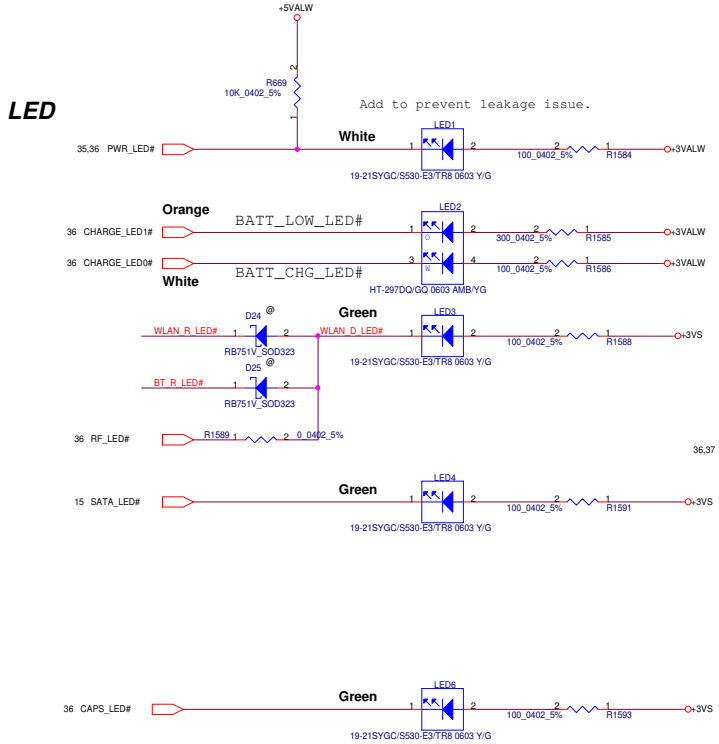
W=60mils

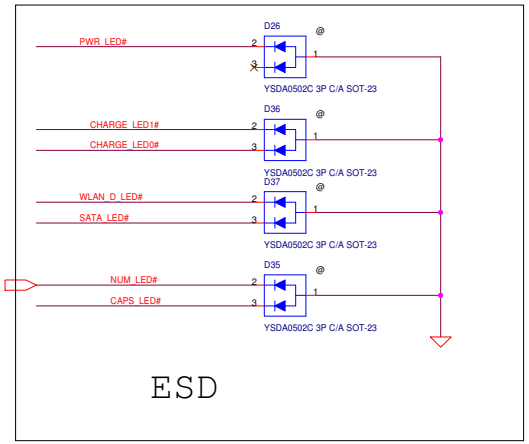


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



LED





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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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Compal Electronics, Inc.			
Title	P28-Mini PCIE/LED		
Size	Document Number		Rev
	QBL60 LA-7552P		1.0
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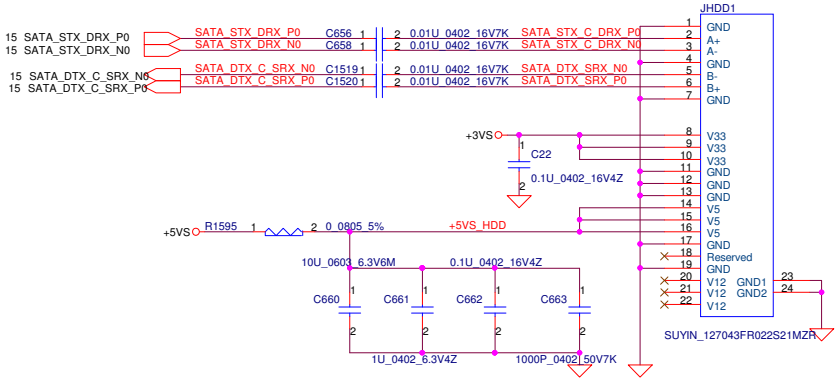
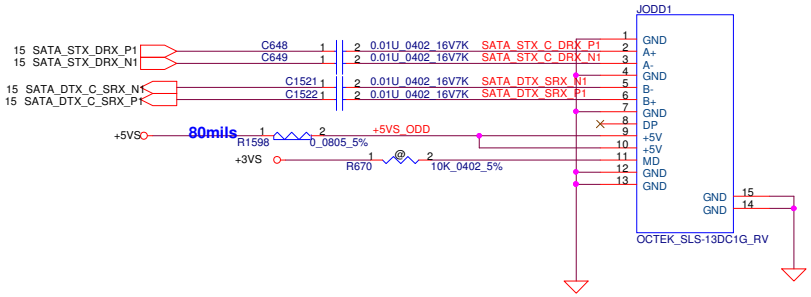
SATA HDD Conn.



SATA ODD FFC Conn.



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Compal Electronics, Inc.

Title: P29-HDD & ODD CONN

Size	Document Number	Rev
B	QBL60 LA-7552P	1.0

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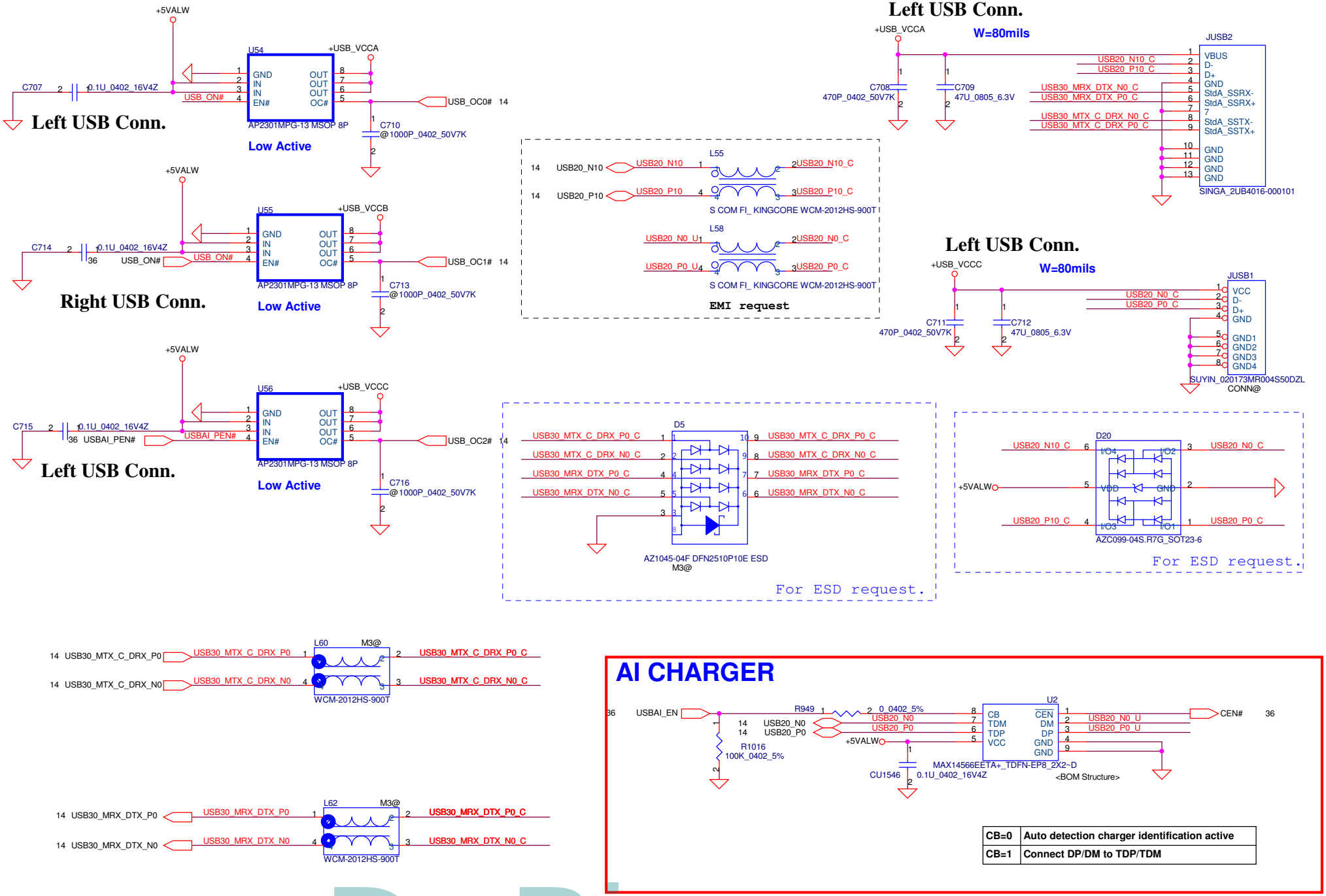

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/25	Deciphered Date	2012/04/25
Title	P32-USB/BT/USBsub		
Size	Custom	Document Number	QBL60 LA-7552P
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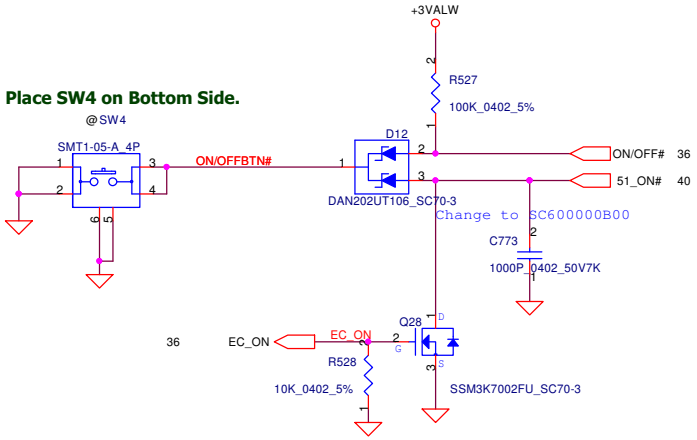
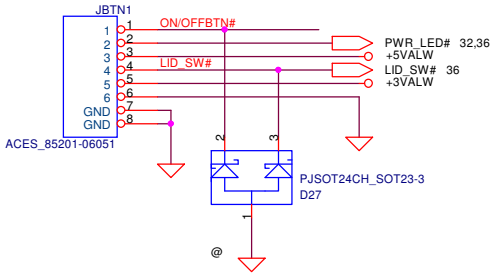
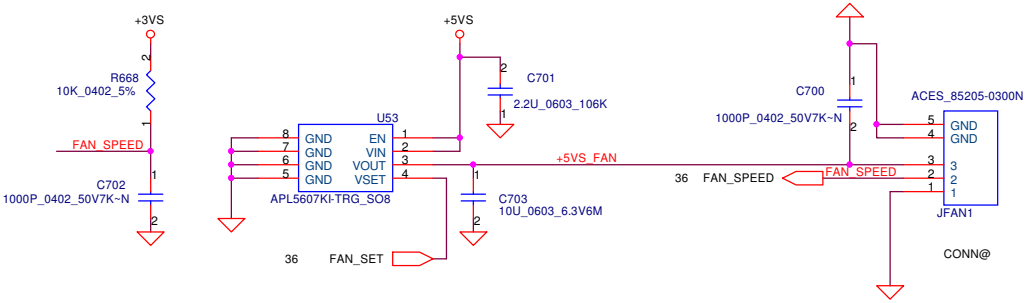
ON/OFF switch **Power Button**

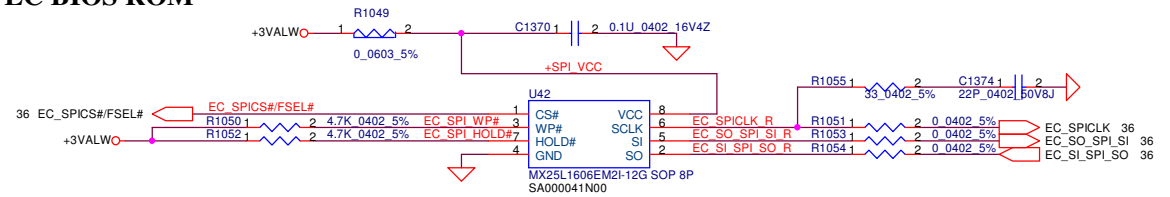




Fan Control Circuit



EC BIOS ROM



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Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size: B | Document Number: QBL60 LA-7552P | Rev: 1.0

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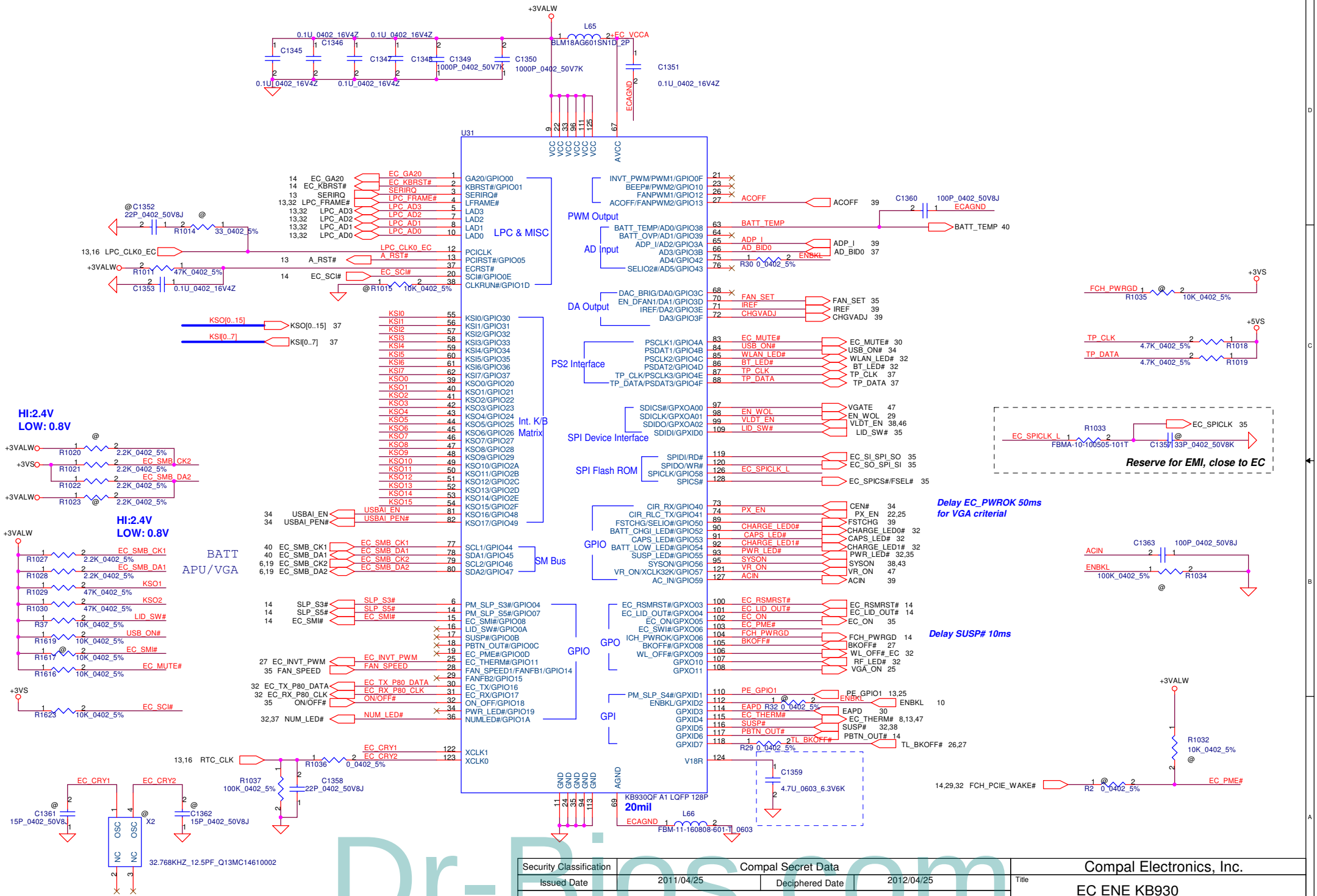

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Compal Electronics, Inc.			
Title	EC ENE KB930		
Size B	Document Number QBL60 LA-7552P		Rev 1.0
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INT_KBD Conn.

KSI[0..7] KSI[0..7] 36
KSO[0..15] KSO[0..15] 36

KSO2	C1543	1 2	@100P_0402_50V8J	KSO1	C1544	1 2	@100P_0402_50V8J	KSO7	24	KSO15	1
KSO15	C1546	1 2	@100P_0402_50V8J	KSO7	C1545	1 2	@100P_0402_50V8J	KSO0	23	KSO7	2
KSO6	C1547	1 2	@100P_0402_50V8J	KSI2	C1548	1 2	@100P_0402_50V8J	KSI1	22	KSO0	3
KSO8	C1549	1 2	@100P_0402_50V8J	KSO5	C1550	1 2	@100P_0402_50V8J	KSI7	21	KSI1	4
KSO13	C1551	1 2	@100P_0402_50V8J	KSI3	C1552	1 2	@100P_0402_50V8J	KSO9	20	KSI7	5
KSO12	C1553	1 2	@100P_0402_50V8J	KSO14	C1554	1 2	@100P_0402_50V8J	KSI6	19	KSI2	6
KSO11	C1555	1 2	@100P_0402_50V8J	KSI7	C1556	1 2	@100P_0402_50V8J	KSI5	18	KSI3	7
KSO10	C1557	1 2	@100P_0402_50V8J	KSI6	C1558	1 2	@100P_0402_50V8J	KSO3	17	KSI4	8
KSO3	C1559	1 2	@100P_0402_50V8J	KSI5	C1560	1 2	@100P_0402_50V8J	KSI4	16	KSI5	9
KSO4	C1561	1 2	@100P_0402_50V8J	KSI4	C1562	1 2	@100P_0402_50V8J	KSI2	15	KSI6	10
KSI0	C1563	1 2	@100P_0402_50V8J	KSO9	C1564	1 2	@100P_0402_50V8J	KSO1	14	KSO9	11
KSO0	C1565	1 2	@100P_0402_50V8J	KSI1	C1566	1 2	@100P_0402_50V8J	KSI3	13	KSI7	12
								KSI0	12	KSO5	13
								KSO13	11	KSO3	14
								KSO5	10	KSO4	15
								KSO2	9	KSO8	16
								KSO4	8	KSO6	17
								KSO8	7	KSO11	18
								KSO6	6	KSO10	19
								KSO11	5	KSO12	20
								KSO10	4	KSO14	21
								KSO12	3	KSO15	22
								KSO14	2		23
								KSO15	1		24

ACES_88514-02401-071
26 GND2
25 GND1
JKB1

Pin define

CONN PIN define need double check

+1.5VSG
VGA@ C374 330U_2.5V_M

+CPU_CORE
C569 330U@ 2.5V_Y

+CPU_CORE_NB
C1010 C1011 390U_2.5V_10M

+VGA_CORE
C435 C436 C474 C560 VGA@ 390U_2.5V_10M

ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R10 PR	100K	46.4K	1.045V
3	Reserve	100K	56.2K	1.187V

Analog Board ID definition

+3VALW
Ra R1024 100K_0402_5%
AD_BID0 AD_BID0 36
Rb R1026 46.4K_0402_1%

To TP/B Conn.

+5VS
C1567 0.1U_0402_16V4Z
36 TP_CLK
36 TP_DATA
C1568 100P_0402_50V8J
C1569 100P_0402_50V8J
GND GND
JTP1 ACES_88514-00601-071
D17 D28
YSDA0502C 3P C/A SOT-23
YSDA0502C 3P C/A SOT-23
Reserve for ESD

SW5 NTC010-BB1G-C100C
SW/L
SW6 NTC010-BB1G-C100C
SW/R

Place SW5 for TP Left switch.
Place SW6 for TP Right switch.

ZZZ
PCB

30 SPK_L1
30 SPK_L2
30 SPK_R1
30 SPK_R2
JSPK1 ACES_88266-04001
D9 D10 PJMBZ6V8_SOT23-3

32,36 NUM_LED#
Green
LED5 19-21SYGC/S530-E3/TR8 0603 Y/G
100_0402_5% R1592
+3VS

FD1 FD2 FD3 FD4 FIDUCIAL_C40M80

H1 H3 H9 H11 H13 H_3P0
H14 H15 H20 H22 H_3P0
H5 H6 H7 H10 H23 H_3P8
H16 H17 H18 H19 H_4P2
H2 H_6P2X3P2
H8 H_3P0
H24 H_3P2
H25 H_3P3

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Issued Date	2011/04/25	Deciphered Date	2012/04/25
Title	P33-Other IO/USB (right)		
Size Custom	Document Number QBL60 LA-7552P		Rev 1.0
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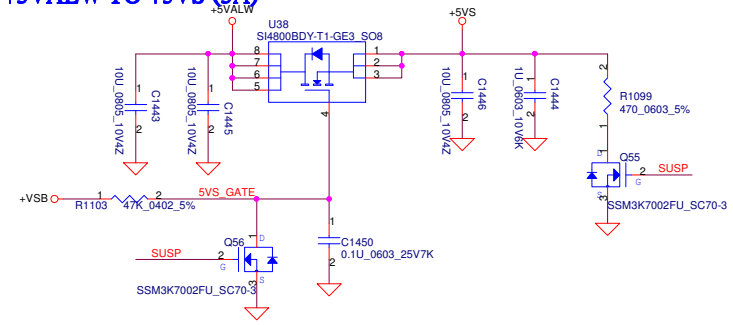
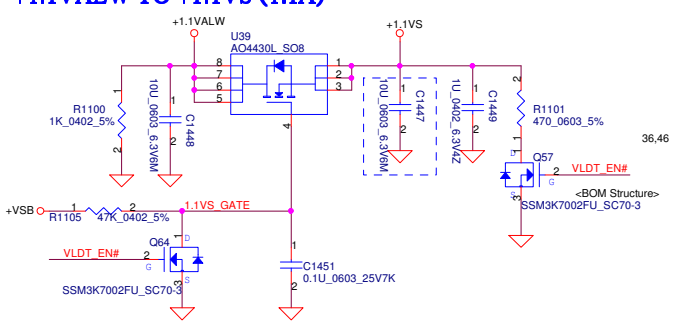
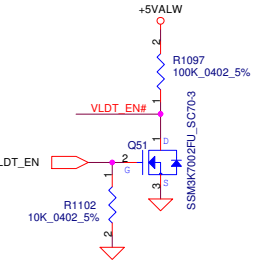
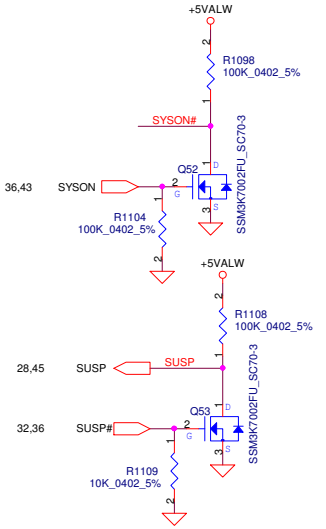
+5VALW TO +5VS (5A)



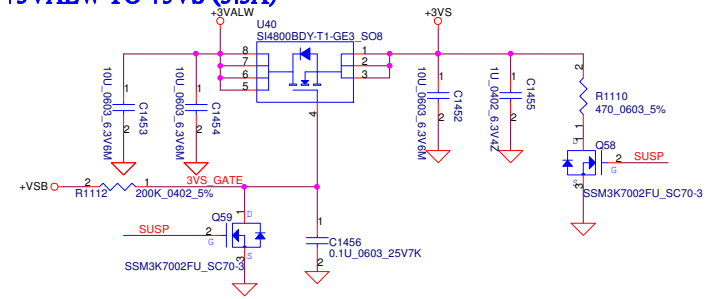
+1.1VALW TO +1.1VS (1.1A)



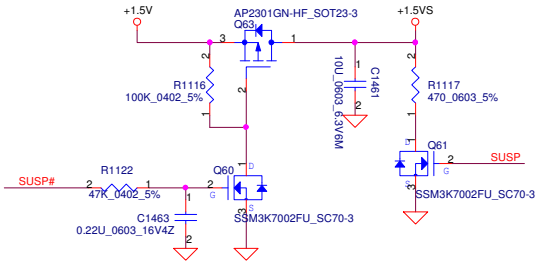




+3VALW TO +3VS (3.3A)

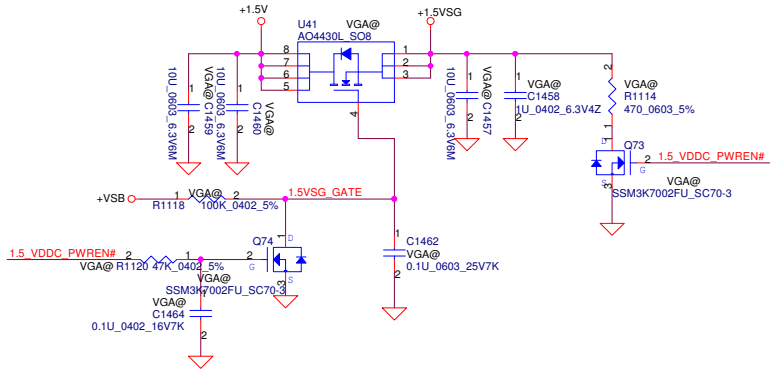


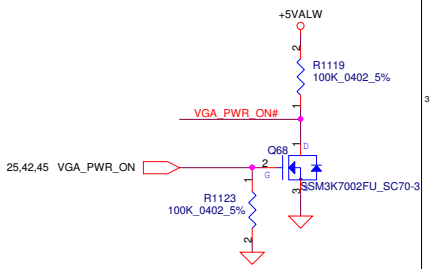
+1.5V TO +1.5VS (1.5A)



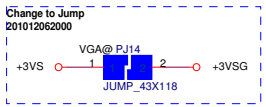
VGA Power

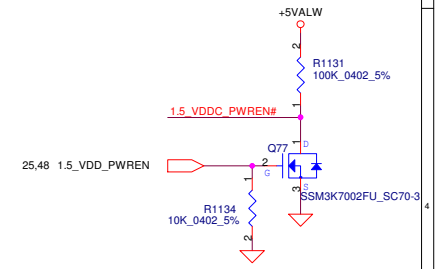
+1.5V to +1.5VSG (1.5A)

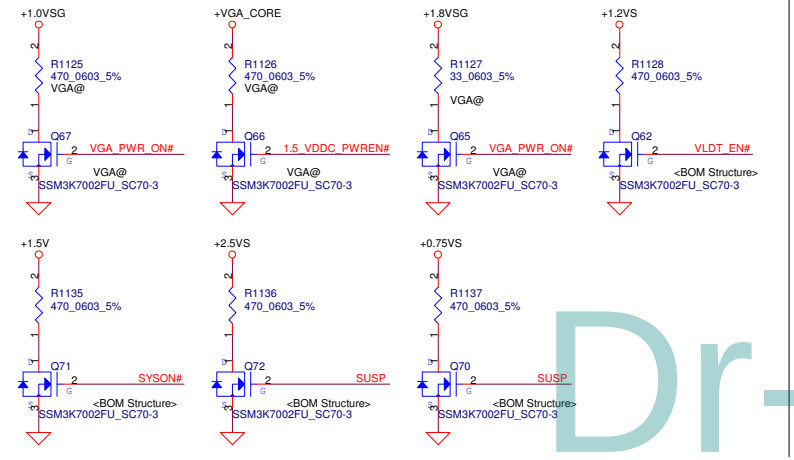




+3VS to +3VSG (3.3A)







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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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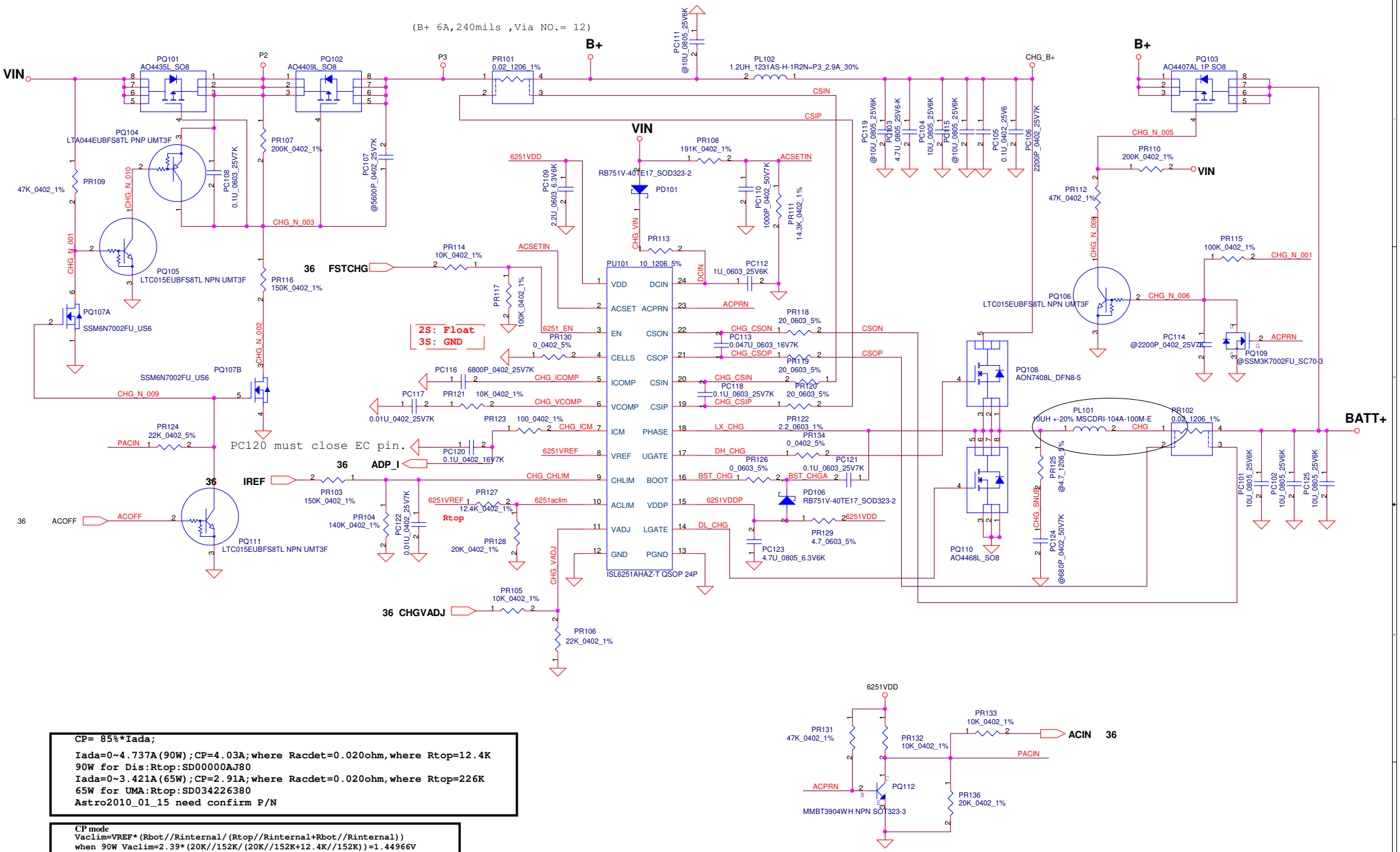
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: QBL60 LA-7552P | Rev: 1.0

Date: Monday, April 25, 2011 | Sheet 38 of 53



CP= 85%*Iada;

Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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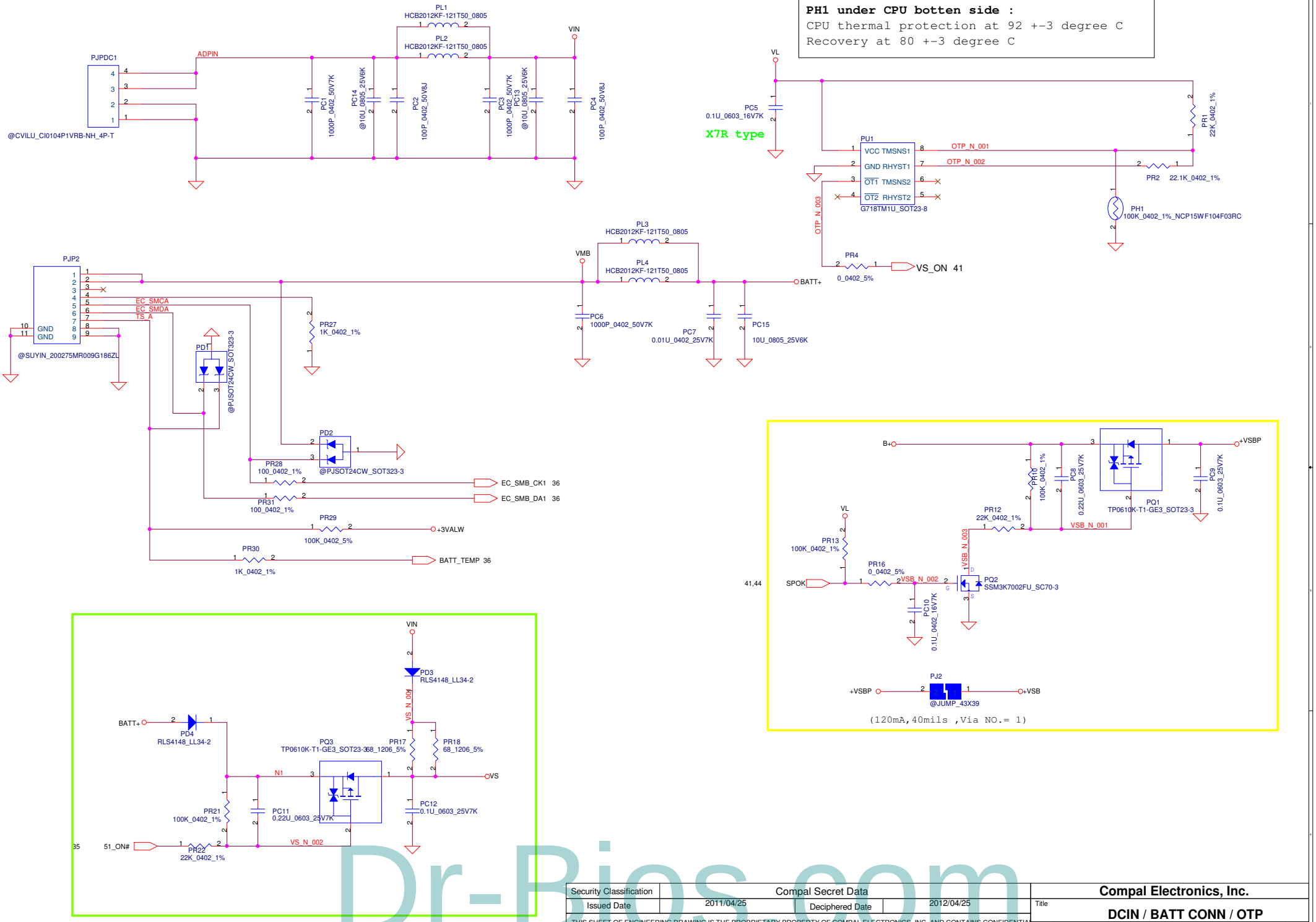
Compal Electronics, Inc.			
Title: CHARGER			
Size	Document Number: NCL61 LA-6321P M/B		Rev: 1.0
Date: Monday, April 25, 2011		Sheet 39 of 53	

PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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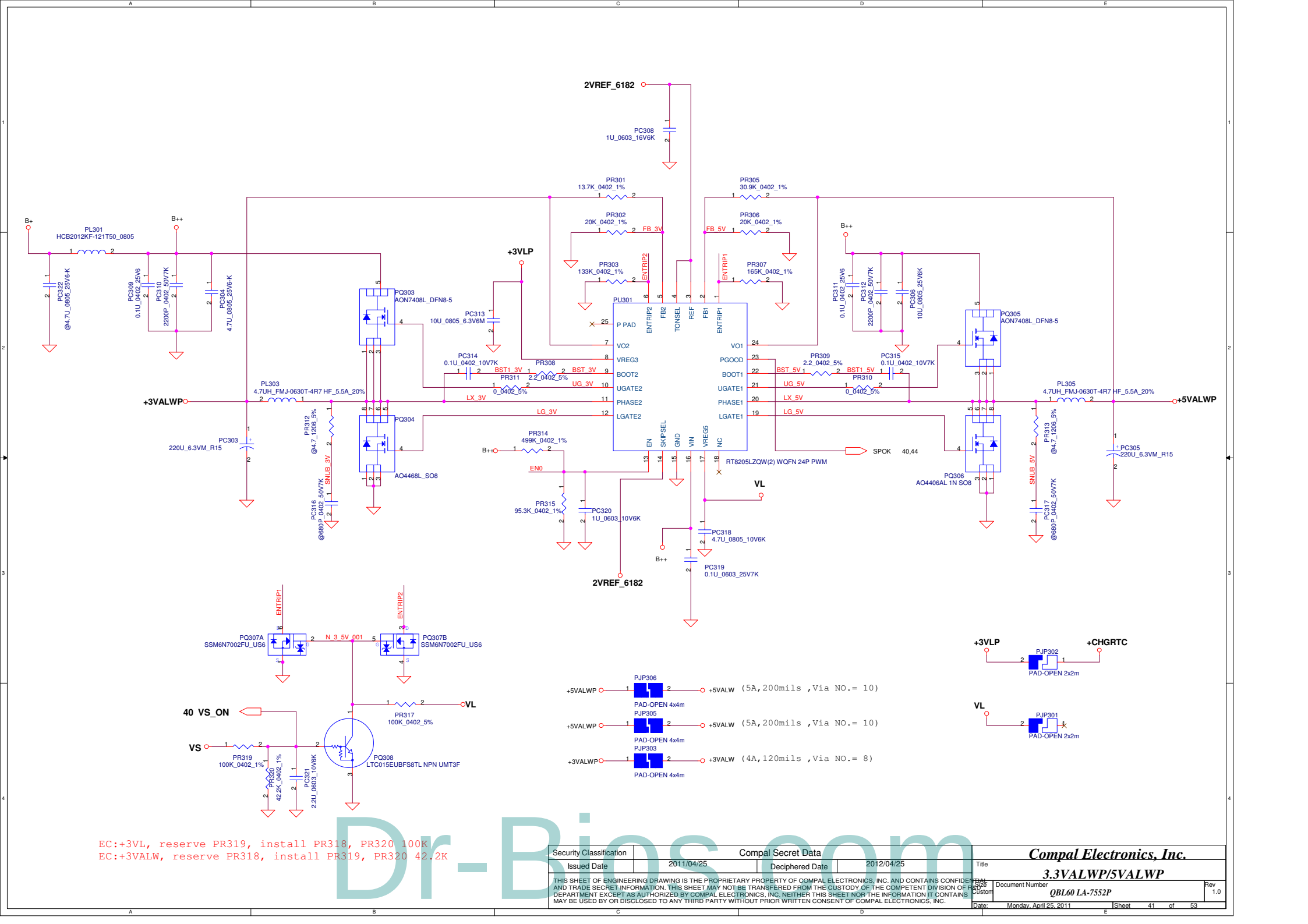
Compal Electronics, Inc.			
Title	DCIN / BATT CONN / OTP		
Size	Document Number	NCL61 LA-6321P M/B	Rev 1.0
Date: Monday, April 25, 2011	Sheet 40 of 53		



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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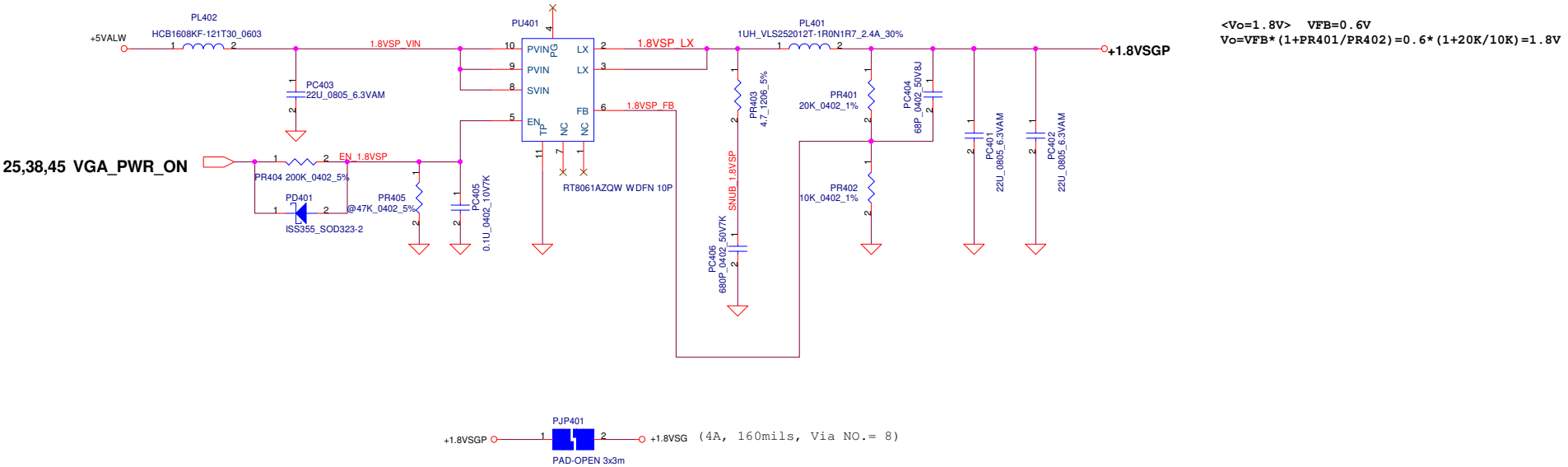
Compal Electronics, Inc.			
Title: 3.3VALWP/5VALWP			
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
Date: Monday, April 25, 2011	Sheet 41 of 53		



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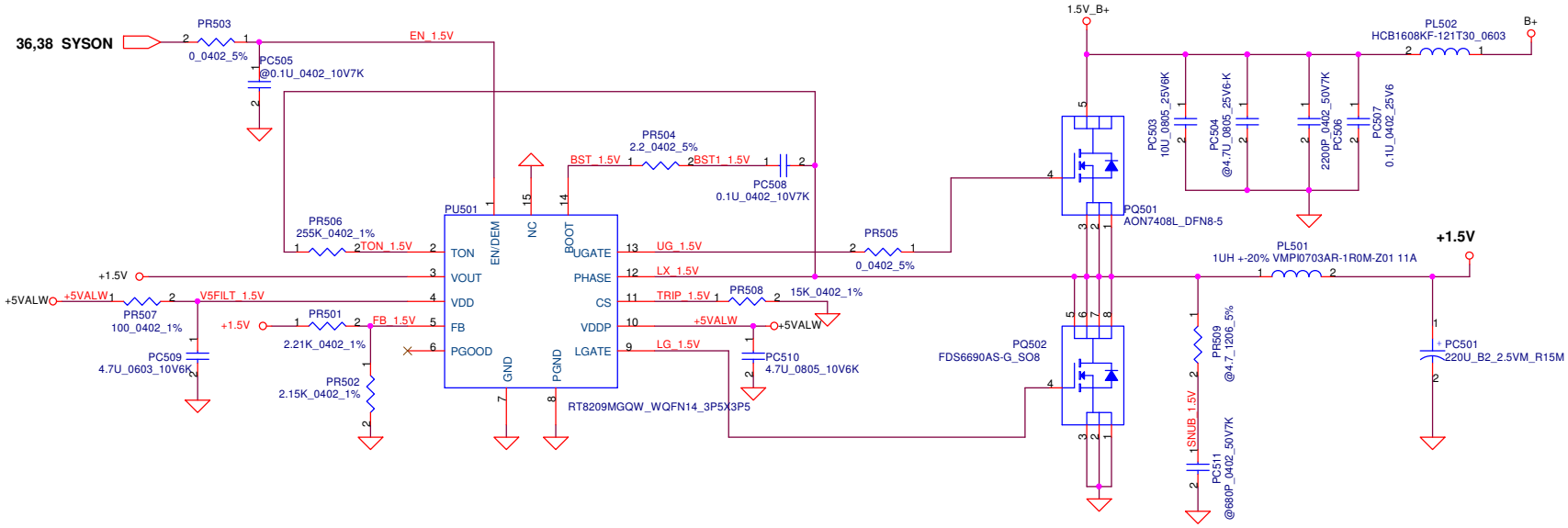
Compal Electronics, Inc.			
Title	+1.8VSGP		
Size	Document Number	NCL61 LA-6321P M/B	Rev 1.0
Date: Monday, April 25, 2011	Sheet 42 of 53		



(8A,320mils ,Via NO.= 16)

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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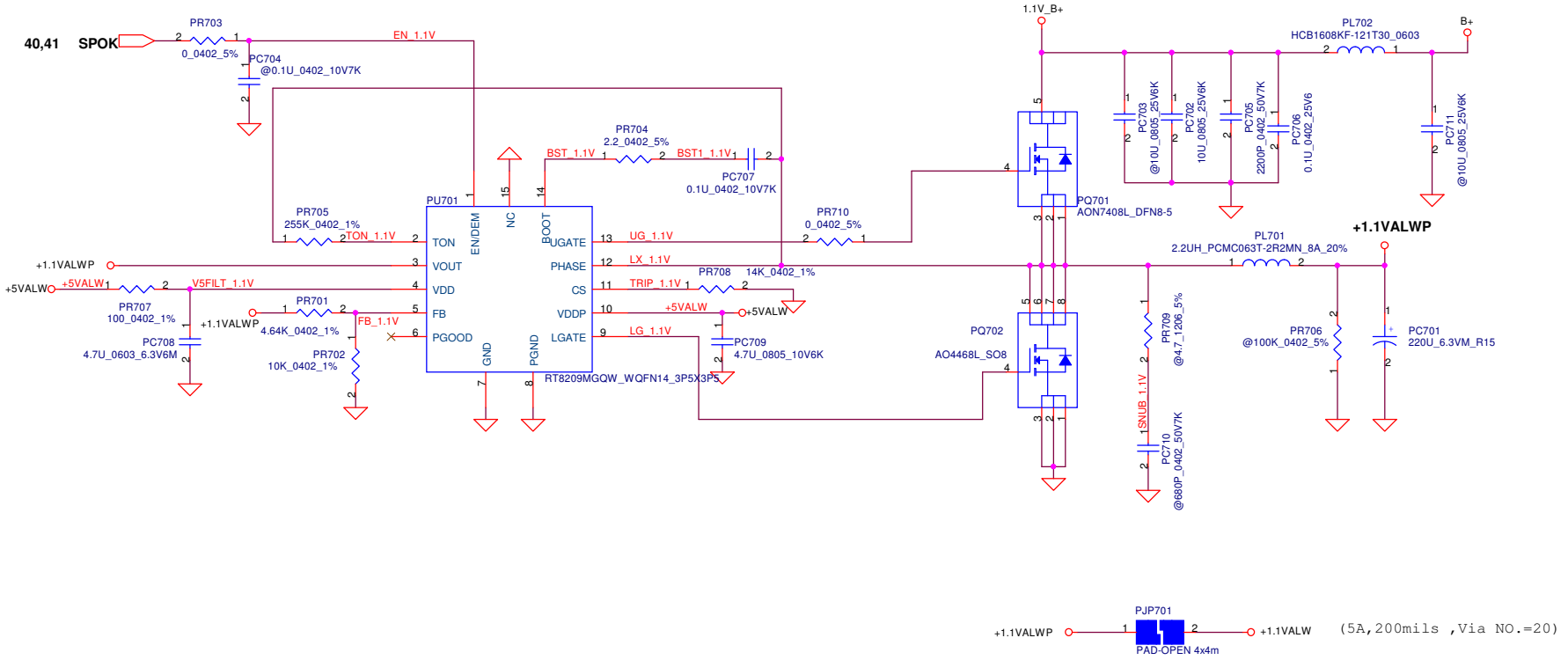
Compal Electronics, Inc.			
Title	+1.5VP		
Size	Document Number		Rev
	QBL60 LA-7552P		1.0
Date:	Monday, April 25, 2011	Sheet	43 of 53



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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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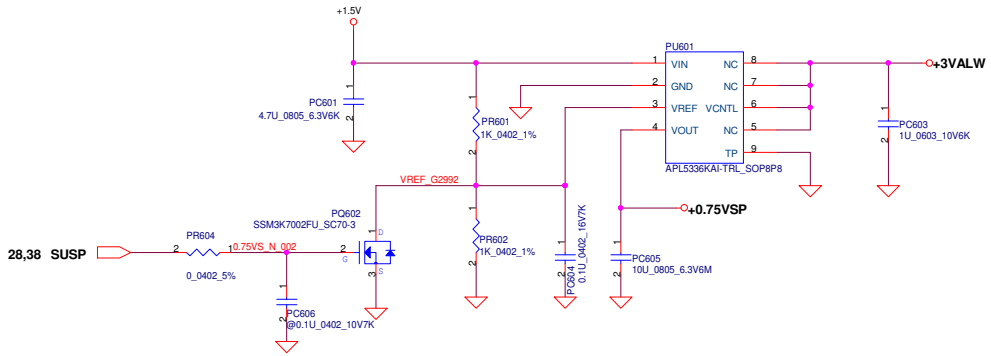
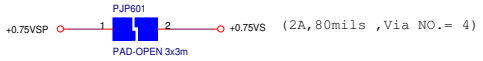
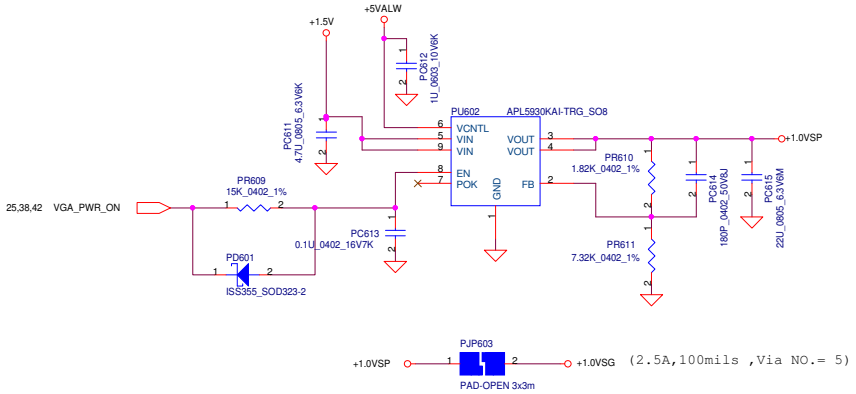
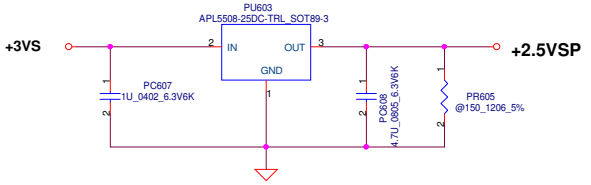
Compal Electronics, Inc.			
Title: PWR+1.1VALWP			
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 1.0
Date: Monday, April 25, 2011	Sheet 44 of 53		









Security Classification	Compal Secret Data		
Issued Date	2011/04/25	Deciphered Date	2012/04/25

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Compal Electronics, Inc.

Title: **PWR 0.75VSP/1.0VSP/2.5VSP**

Size	Document Number	Rev
	QBL60 LA-7552P	1.0

Date: Monday, April 25, 2011 | Sheet 45 of 53

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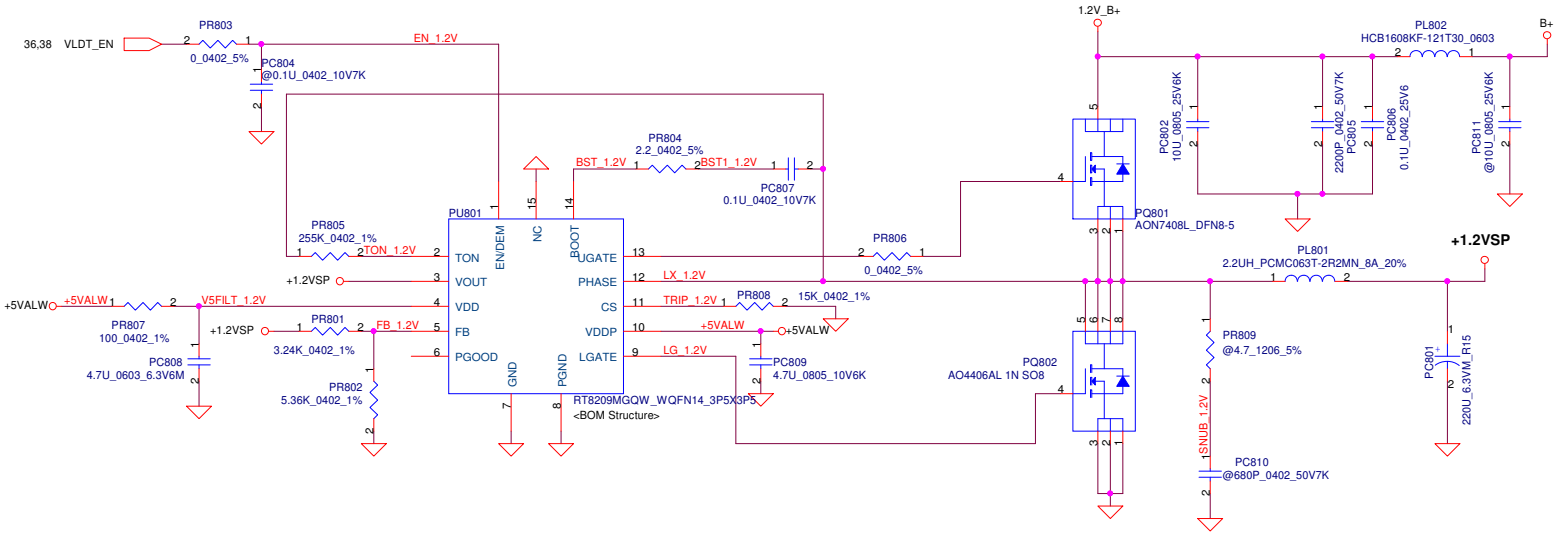

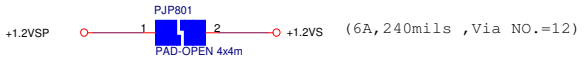

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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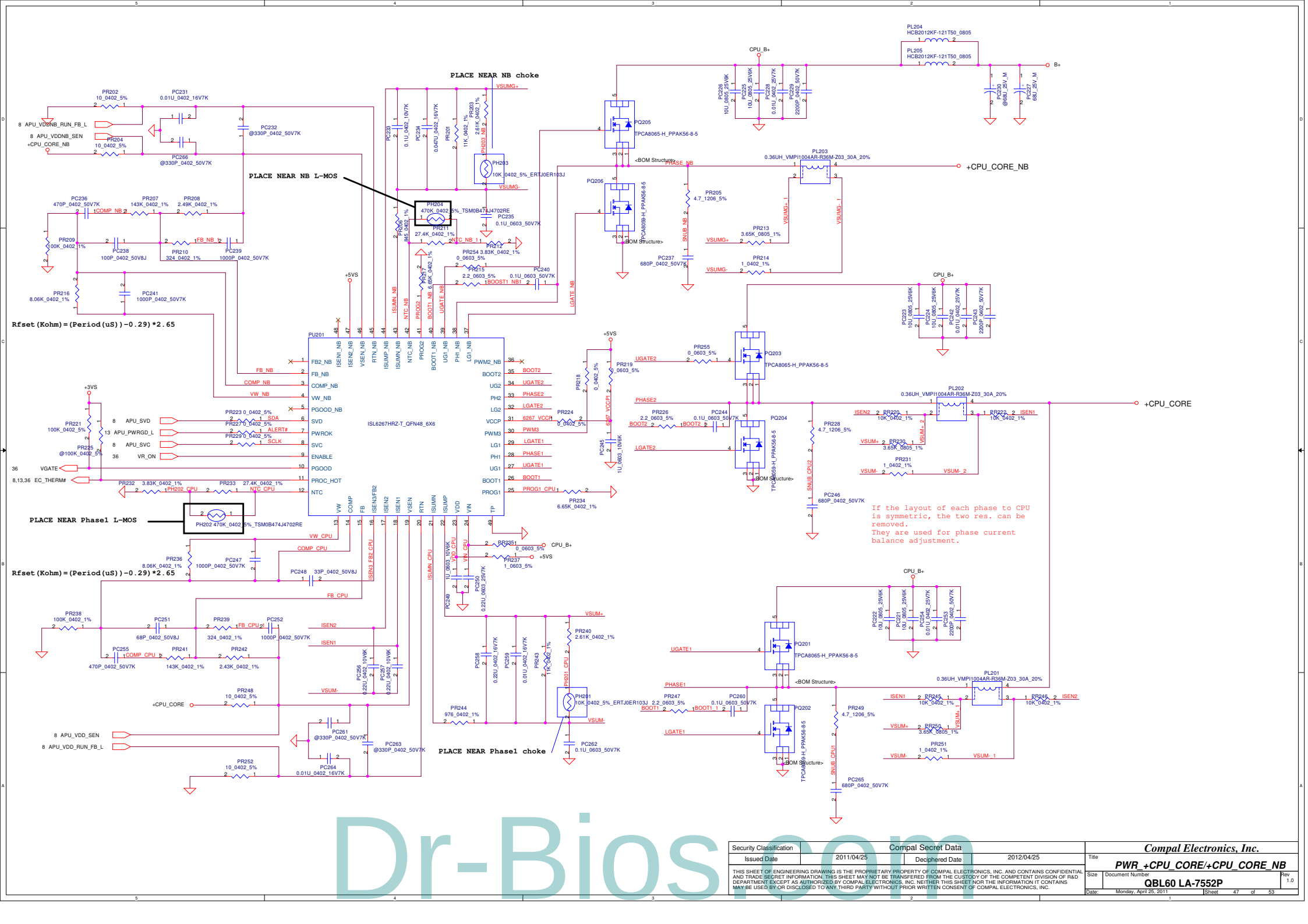
Compal Electronics, Inc.			
Title	+1.2VSP		
Size	Document Number	NCL61 LA-6321P M/B	Rev 1.0
Date: Monday, April 25, 2011	Sheet 46 of 53		



Security Classification	Compal Secret Data		
Issued Date	2011/04/25	Deciphered Date	2012/04/25

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Compal Electronics, Inc.	
Title	PWR_+CPU_CORE/+CPU_CORE_NB
Size	Document Number: QBL60 LA-7552P
Rev	1.0
Date:	Monday, April 25, 2011
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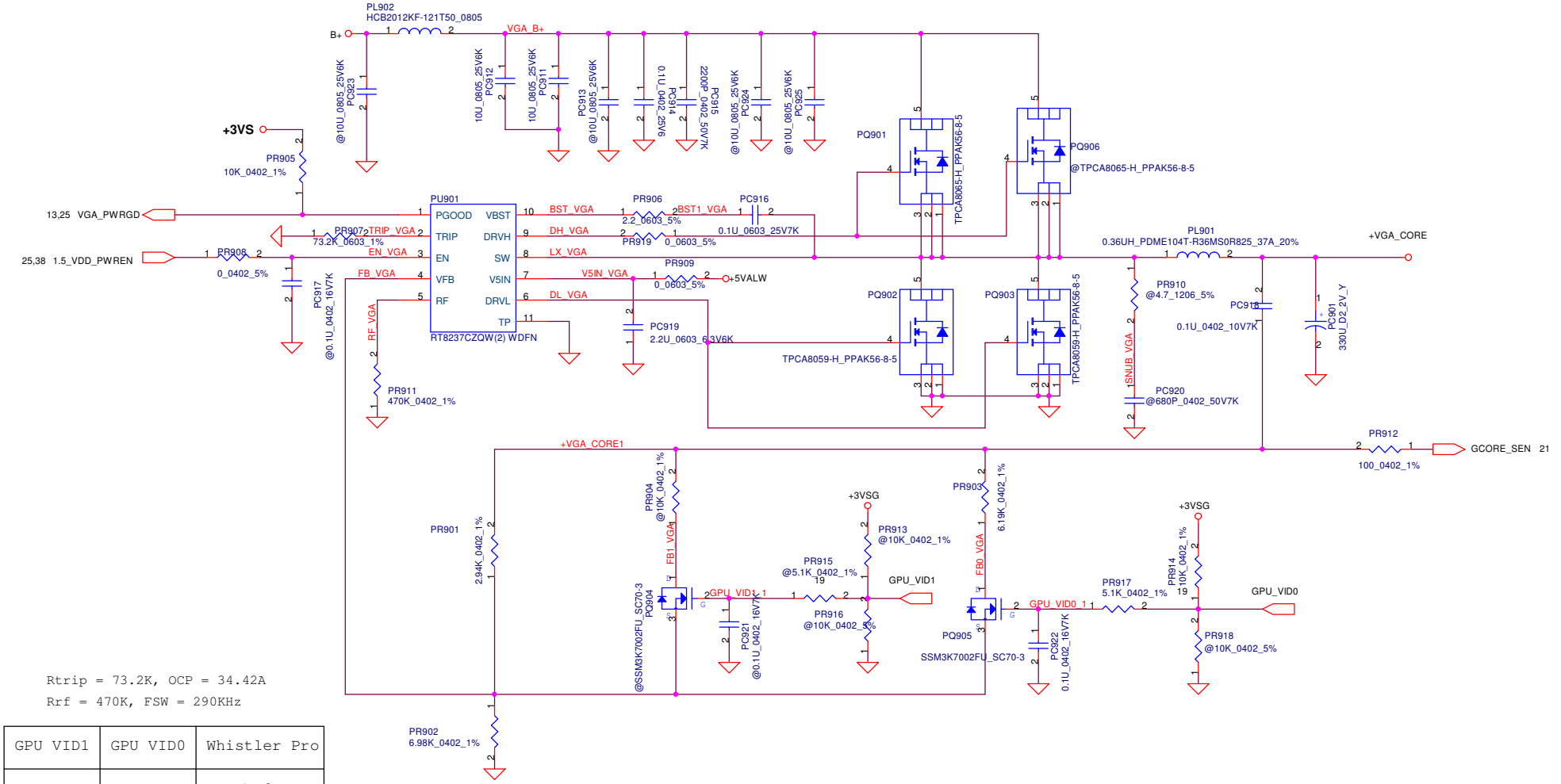

Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

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Issued Date	2011/04/25	Deciphered Date	2012/04/25

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Compal Electronics, Inc.		
Title: VGA_CORE		
Size	Document Number: QBL60 LA-7552P	Rev: 1.0
Date: Monday, April 25, 2011	Sheet 48 of 53	

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

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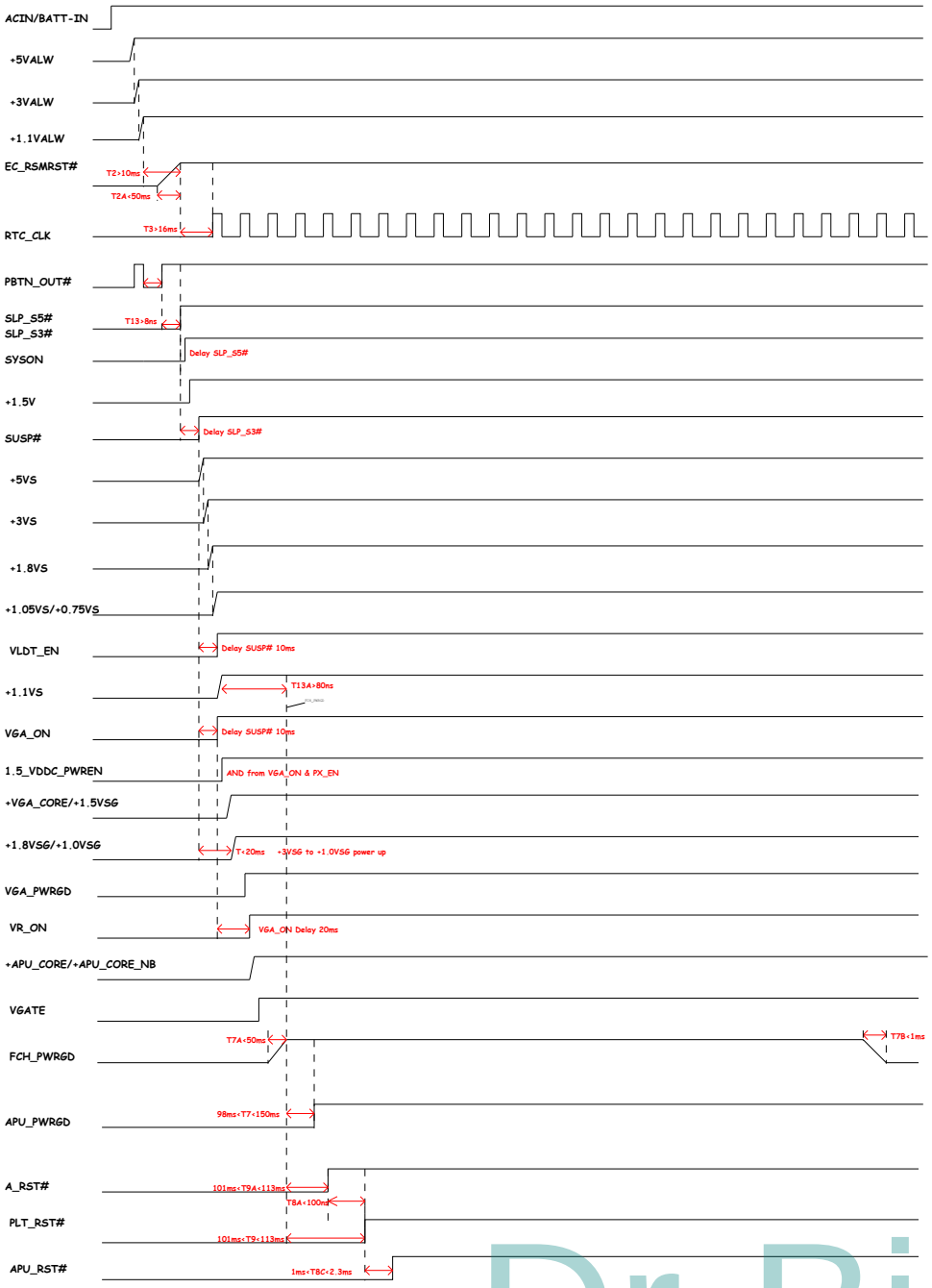
POWER SEQUENCE



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Security Classification	Compal Secret Data		
Issued Date	2011/04/05	Deciphered Date	2012/04/05

Power Sequence

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Size	Document Number	Rev
	QBL60 LA-7852P	1.0
Date: Monday, Dec 31, 2012	Sheet 46 of 53	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD reuqest	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

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Issued Date: 2011/04/25 Deciphered Date: 2012/04/25

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Compal Electronics, Inc.
Title: HW-PIR1
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 1.0
Date: Monday, April 25, 2011 | Sheet 51 of 53

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI reuqest	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uf	03/29	ER
2		For share ROM reuqest	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI reuqest	0.2	PG#34	D5 change to SC300001Y00	03/29	ER
4		For +3VS leakage from CRT	0.21	PG#27	Add Q101,R1644,R1645 Del R4,R31	03/31	ER
5		For Crystal EA	0.21	PG#13	Y4 change to SJ100007N00 (32.768KHZ 7PF)	03/31	ER
6		For HDMI EA	0.21	PG#34	D32.5 change to connect +5VALW from +5VS	03/31	ER
7		For EMC team requirement (ISN).	0.22	PG#29	Change C1636 from 1000pF to 120pF.	04/19	PR
8		For Thermal team recommend.	0.22	PG#19	Add R78, R79 and reserve R80, R82.	04/19	PR
9		Reserve PX_EN signal.	0.22	PG#36	Reserve PX_EN in EC pin 74.	04/19	PR
10		Follow ME BOM.	0.22	PG#11 PG#12	Swap the location of JDIMM1 & JDIMM2.	04/19	PR
11		Don't use for MP.	0.22	PG#35	Unstuff SW4.	04/19	PR
12		Update Board ID for PR (R1.0).	0.22	PG#37	Change R1026 to 46.4K ohm.	04/19	PR
13		DFM team requirement.	0.22	PG#35	Delete SW3.	04/19	PR
14		DMC team requirement.	0.23	PG#29	Reserve D7 between GND_LAN and GND.	04/21	PR
15		Don't use for MP.	0.23	PG#29	Unstuff C1193.	04/21	PR
16		Key Part list is updated from the customer.	0.23	PG#4	Update U25 (M3-FCH) P/N to SA000043ID0 (S IC 218-0755042 A13 02G050005815 T88!)	04/21	PR
17		Key Part list is updated from the customer.	0.23	PG#13	Update U25 (M2-FCH) P/N to SA000042C80 (S IC 218-0755046 A13 02G050005814 T88!)	04/21	PR
18		Update TS1 as ER build Memo.	0.23	PG#29	Change TS1 from SP050005L00 to SP050006F00. (S X'FORM_ IH-160 LAN)	04/21	PR
19		For VGA Sequence.	0.23	PG#38	Change R1127 from 470 ohm to 33 ohm.	04/21	PR
20		Prevent the leakage from CRT monitor.	0.23	PG#27	Add R1644, R1645, Q101 and Del R4, R31.	04/21	PR
21		DFB team requirement.	0.23	PG#34	Del R664~R667 and R672~R675.	04/21	PR
22		ESD team requirement.	0.23	PG#34	Change D5 from SC300001D00 (YSCLAMP0524P SLP2510P8) to SC300001Y00 (AZ1045-04F DFN2510P10E ESD).	04/21	PR
23		DMC team requirement.	0.23	PG#29	Change the ground of D21, D22, D31, D34 and H8. from GND_LAN to LAN.	04/22	PR
24		DMC team requirement.	0.23	PG#19	Add R83, R84.	04/22	PR
25		DMC team requirement.	1.0	PG#13	Change R657 from 22 ohm to 33 ohm.	04/25	PR
26		DMC team requirement.	1.0	PG#13	Stuff R1561 to 33 ohm and C1509 to 22pF.	04/25	PR
27							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Reduce the component count for MP.	1.0		Change below the footprints from 0 ohm to R short.	04/25	PR

Reference	Value	Source Part	Source Library	Page
R537	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P06-FS1 PCIE/UMI/TSI
R538	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P06-FS1 PCIE/UMI/TSI
R591	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 Display/MISC/...
R598	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 Display/MISC/...
R606	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 Display/MISC/...
R608	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 Display/MISC/...
R611	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 Display/MISC/...
R81	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P14-HUDSON-M2 GPI...
R912	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P16-HUDSON-M2 STR...
R1145	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R1148	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R19	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R20	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R22	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R23	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R24	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R25	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R26	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R27	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R28	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R937	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R938	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R941	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R945	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUDSON-M2 Pow...
R483	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P23-VRAM_DDR3 / CH...
R485	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P23-VRAM_DDR3 / CH...
R511	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P24-VRAM_DDR3 / CH...
R513	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P24-VRAM_DDR3 / CH...
R1291	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P26-LVDS Translator-A...
R570	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P26-LVDS Translator-A...
R607	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P26-LVDS Translator-A...
R1634	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R1635	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R1636	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R1641	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R1643	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R1650	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R1651	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVDS CONN / CRT...
R560	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN Realtek RTL81...
R647	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN Realtek RTL81...
R658	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN Realtek RTL81...
R1531	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P30-HD AUDIO CODEC...
R1534	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P30-HD AUDIO CODEC...
R1537	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P30-HD AUDIO CODEC...
R1560	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P31-RTS5137 Media C...
R1573	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1574	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1575	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1576	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1577	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1578	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1579	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1580	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini-Card / LED
R1595	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P33-HDD & ODD CONN
R1598	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P33-HDD & ODD CONN
R1049	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P35-FAN / PBTN / EC R...

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Compal Electronics, Inc.
Title: HW-PIR3
Size: Custom
Document Number: QBL60 LA-7552P
Rev: 1.0
Date: Monday, April 25, 2011
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