Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-16

LA-7552P REV: 0.03

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.		
Title: Cover Page		
Size: B	Document Number: QBL60 LA-7552P	Rev: 0.03
Date: Tuesday, February 22, 2011	Sheet 1 of 49	

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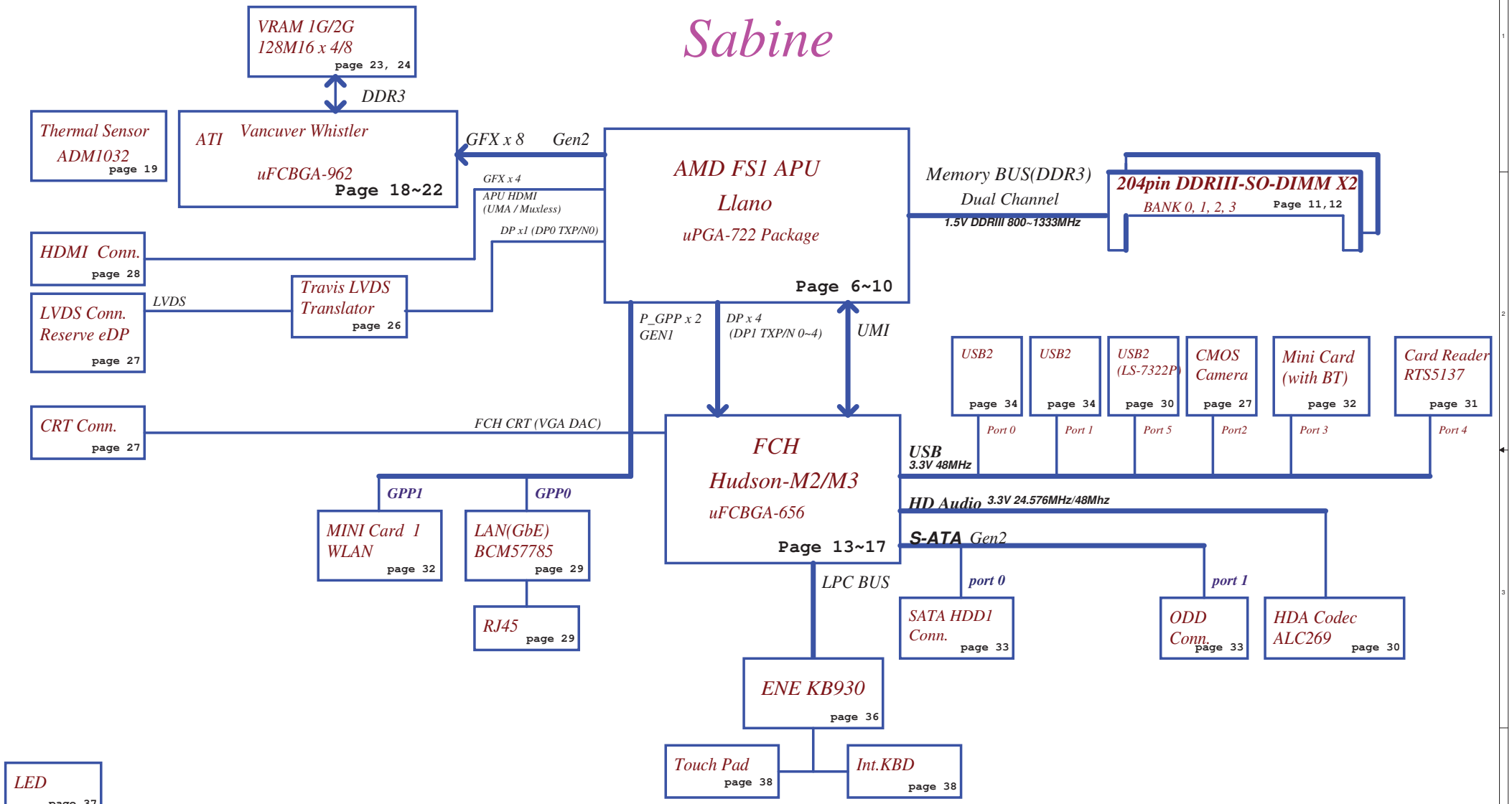
Model Name : QBL60



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: B	Document Number: QBL60 LA-7552P		Rev: 0.03
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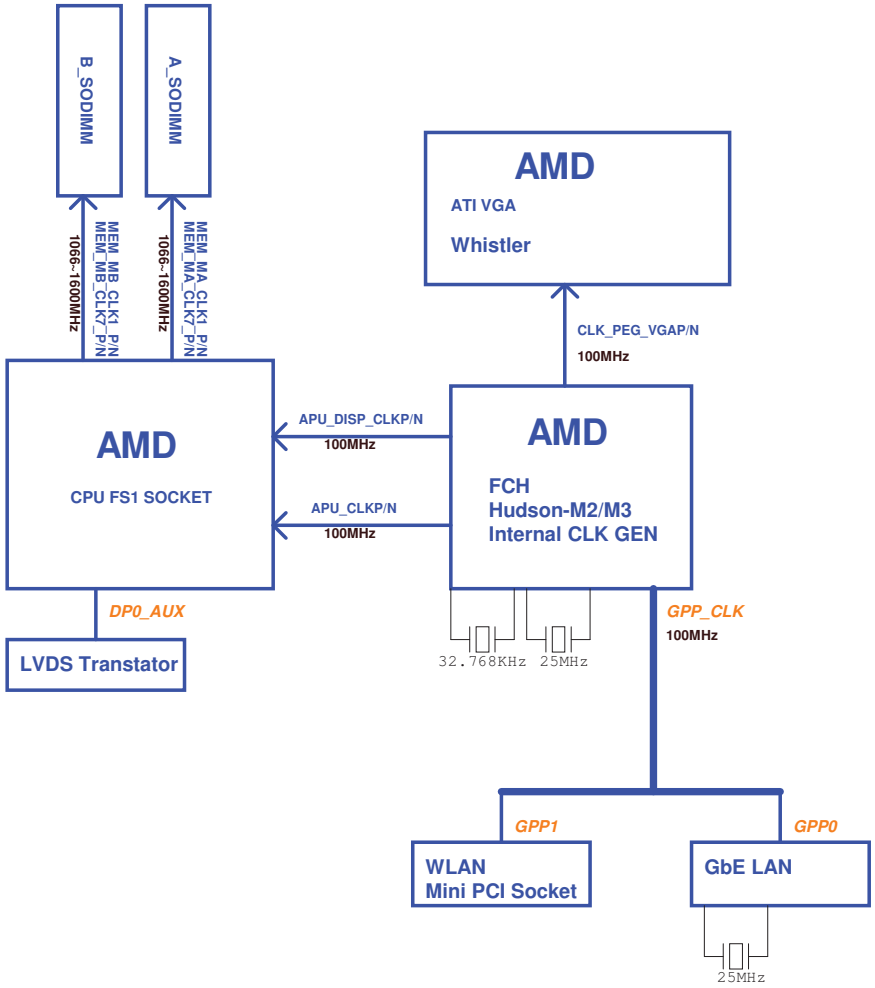
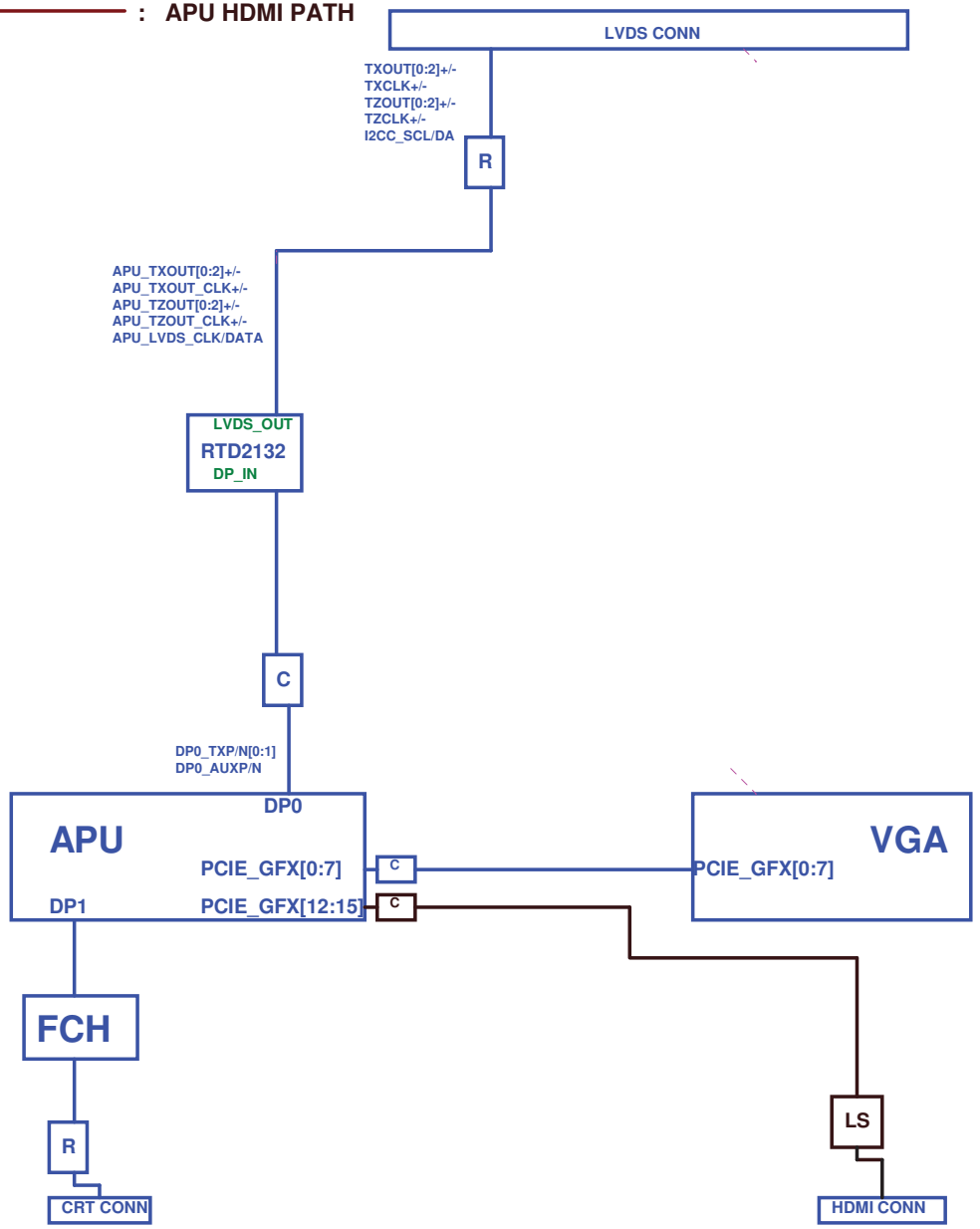
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Title	CLOCK / DISPLAY DISTRIBUTION		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.03
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043I90

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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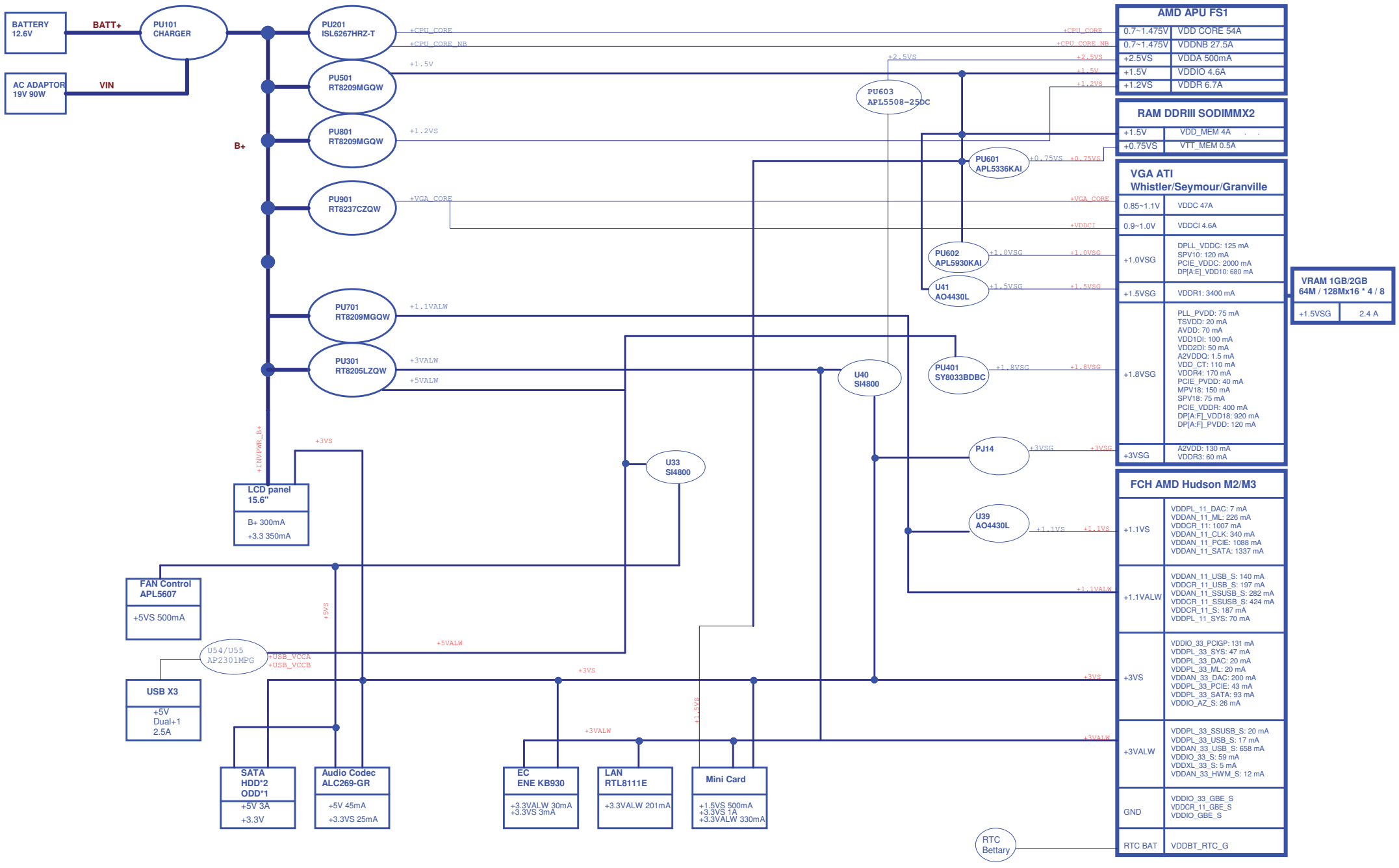

Security Classification	Compal Secret Data		
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Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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18 PCIE_GTX_C_FRX_P[0..7]
18 PCIE_GTX_C_FRX_N[0..7]

PCIE_FTX_C_GRX_P[0..7] 18
PCIE_FTX_C_GRX_N[0..7] 18

JCPU1A — CONN@ — PCI EXPRESS — GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C917	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C918	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C919	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C920	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C921	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C922	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3	W8	P_GFX_RXP3	P_GFX_TXP3	W2	PCIE_FTX_GRX_P3	C923	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C924	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4	V7	P_GFX_RXP4	P_GFX_TXP4	V2	PCIE_FTX_GRX_P4	C925	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C926	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C927	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5	U6	P_GFX_RXN5	P_GFX_TXN5	V5	PCIE_FTX_GRX_N5	C928	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6	U8	P_GFX_RXP6	P_GFX_TXP6	U2	PCIE_FTX_GRX_P6	C929	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6	U9	P_GFX_RXN6	P_GFX_TXN6	U3	PCIE_FTX_GRX_N6	C930	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7	T7	P_GFX_RXP7	P_GFX_TXP7	T2	PCIE_FTX_GRX_P7	C931	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C932	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N7
	R5	P_GFX_RXP8	P_GFX_TXP8	T4					
	R6	P_GFX_RXN8	P_GFX_TXN8	T5					
	R8	P_GFX_RXP9	P_GFX_TXP9	R2					
	R9	P_GFX_RXN9	P_GFX_TXN9	R3					
	P7	P_GFX_RXP10	P_GFX_TXP10	P2					
	P8	P_GFX_RXN10	P_GFX_TXN10	P1					
	N5	P_GFX_RXP11	P_GFX_TXP11	P4					
	N6	P_GFX_RXN11	P_GFX_TXN11	P5					
	N8	P_GFX_RXP12	P_GFX_TXP12	N2	PCIE_FTX_GRX_P12				
	N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12				
	M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13				
	M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13				
	L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14				
	L6	P_GFX_RXN14	P_GFX_TXN14	M5	PCIE_FTX_GRX_N14				
	L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15				
	L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15				

For UMA Mux.

2 / 1 / 0 / CK — *To HDMI*

GPP

29 PCIE_DTX_C_FRX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_DRX_P0	C950	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29	*GLAN*
29 PCIE_DTX_C_FRX_N0	AC6	P_GPP_RXN0	P_GPP_TXN0	AD5	PCIE_FTX_DRX_N0	C951	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29	
32 PCIE_DTX_C_FRX_P1	AC8	P_GPP_RXP1	P_GPP_TXP1	AC2	PCIE_FTX_DRX_P1	C952	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32	*WLAN*
32 PCIE_DTX_C_FRX_N1	AC9	P_GPP_RXN1	P_GPP_TXN1	AC3	PCIE_FTX_DRX_N1	C953	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N1 32	
	AB7	P_GPP_RXP2	P_GPP_TXP2	AB2					
	AB8	P_GPP_RXN2	P_GPP_TXN2	AB1					
	AA5	P_GPP_RXP3	P_GPP_TXP3	AB4					
	AA6	P_GPP_RXN3	P_GPP_TXN3	AB5					

UMI-LINK

13 UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C956	0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13	
13 UMI_MTX_C_FRX_N0	AF7	P_UMI_RXN0	P_UMI_TXN0	AF2	UMI_FTX_MRX_N0	C957	0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 13	
13 UMI_MTX_C_FRX_P1	AE6	P_UMI_RXP1	P_UMI_TXP1	AF5	UMI_FTX_MRX_P1	C958	0.1U_0402_16V7K	UMI_FTX_C_MRX_P1 13	
13 UMI_MTX_C_FRX_N1	AE5	P_UMI_RXN1	P_UMI_TXN1	AF4	UMI_FTX_MRX_N1	C959	0.1U_0402_16V7K	UMI_FTX_C_MRX_N1 13	
13 UMI_MTX_C_FRX_P2	AE9	P_UMI_RXP2	P_UMI_TXP2	AE3	UMI_FTX_MRX_P2	C960	0.1U_0402_16V7K	UMI_FTX_C_MRX_P2 13	
13 UMI_MTX_C_FRX_N2	AE8	P_UMI_RXN2	P_UMI_TXN2	AE2	UMI_FTX_MRX_N2	C961	0.1U_0402_16V7K	UMI_FTX_C_MRX_N2 13	
13 UMI_MTX_C_FRX_P3	AD8	P_UMI_RXP3	P_UMI_TXP3	AD1	UMI_FTX_MRX_P3	C962	0.1U_0402_16V7K	UMI_FTX_C_MRX_P3 13	
13 UMI_MTX_C_FRX_N3	AD7	P_UMI_RXN3	P_UMI_TXN3	AD2	UMI_FTX_MRX_N3	C963	0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13	

+1.2VS — R539 1 2 P_ZVDDP 196_0402_1%

P_ZVDDP	K5	K4	P_ZVSS

P_ZVSS — R540 1 2 196_0402_1%

AMD_TOPEDO_FS-1

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

C935 1 2 0.1U_0402_16V4Z

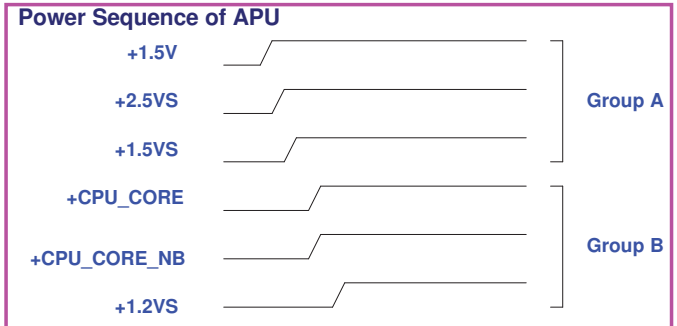
+3VS — R535 1 2 31.6K_0402_1% — R536 1 2 30K_0402_1%

Q9
8,14 APU_SID — APU_SID — EC_SMB_DA — R537 1 2 0_0402_5% — EC_SMB_DA2 19,26,36
BSH111 1N_SOT23-3

Q10
8,14 APU_SIC — APU_SIC — EC_SMB_CK — R538 1 2 0_0402_5% — EC_SMB_CK2 19,26,36
BSH111 1N_SOT23-3

To EC

Power Sequence of APU



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Compal Electronics, Inc.

Title: AMD FS1 PCIE / UMI / TSI

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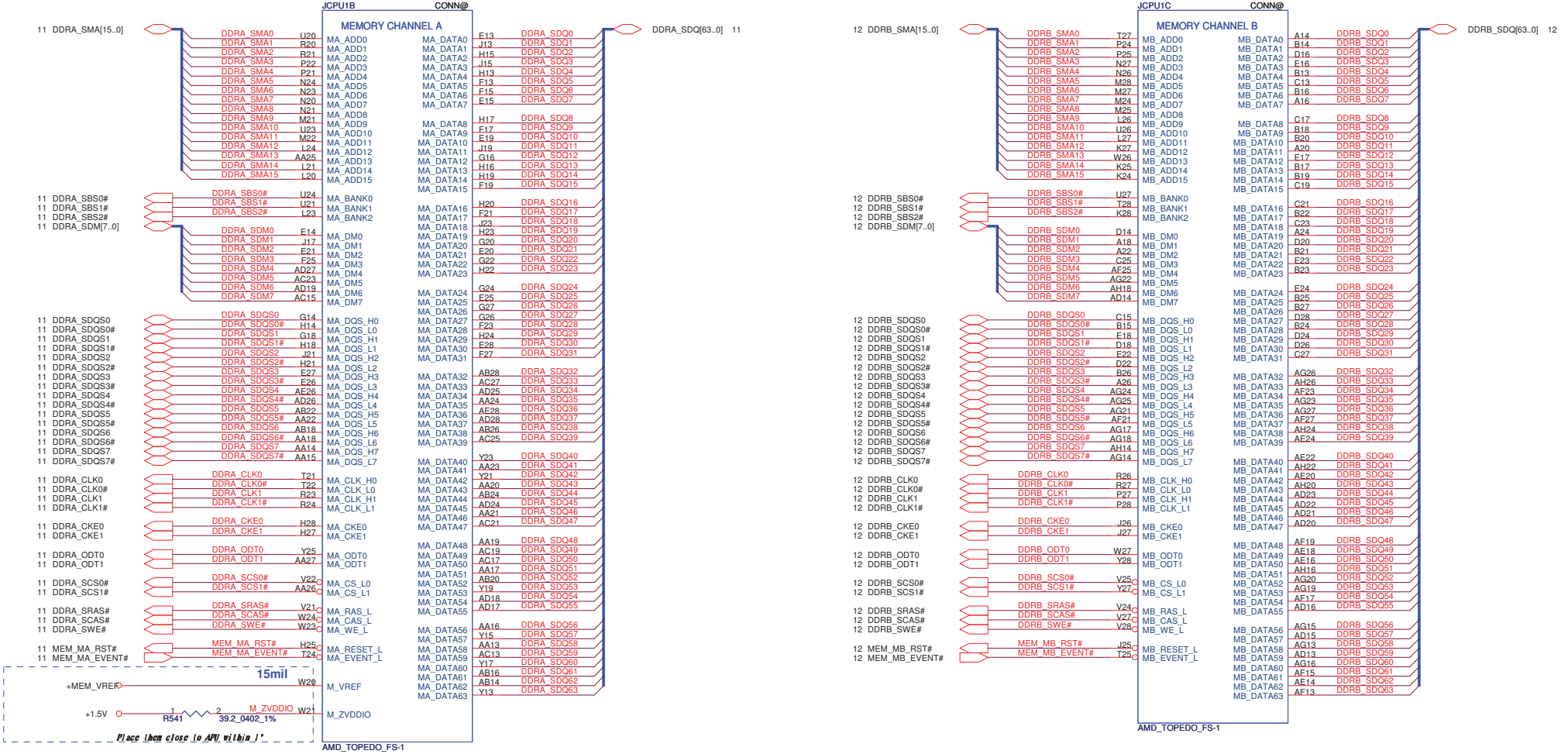
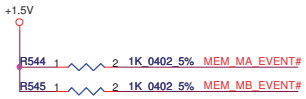
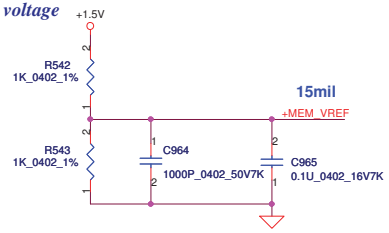


EVENT# pull high



0.75V reference voltage



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: AMD FS1 DDRIII I/F

Size	Document Number	Rev
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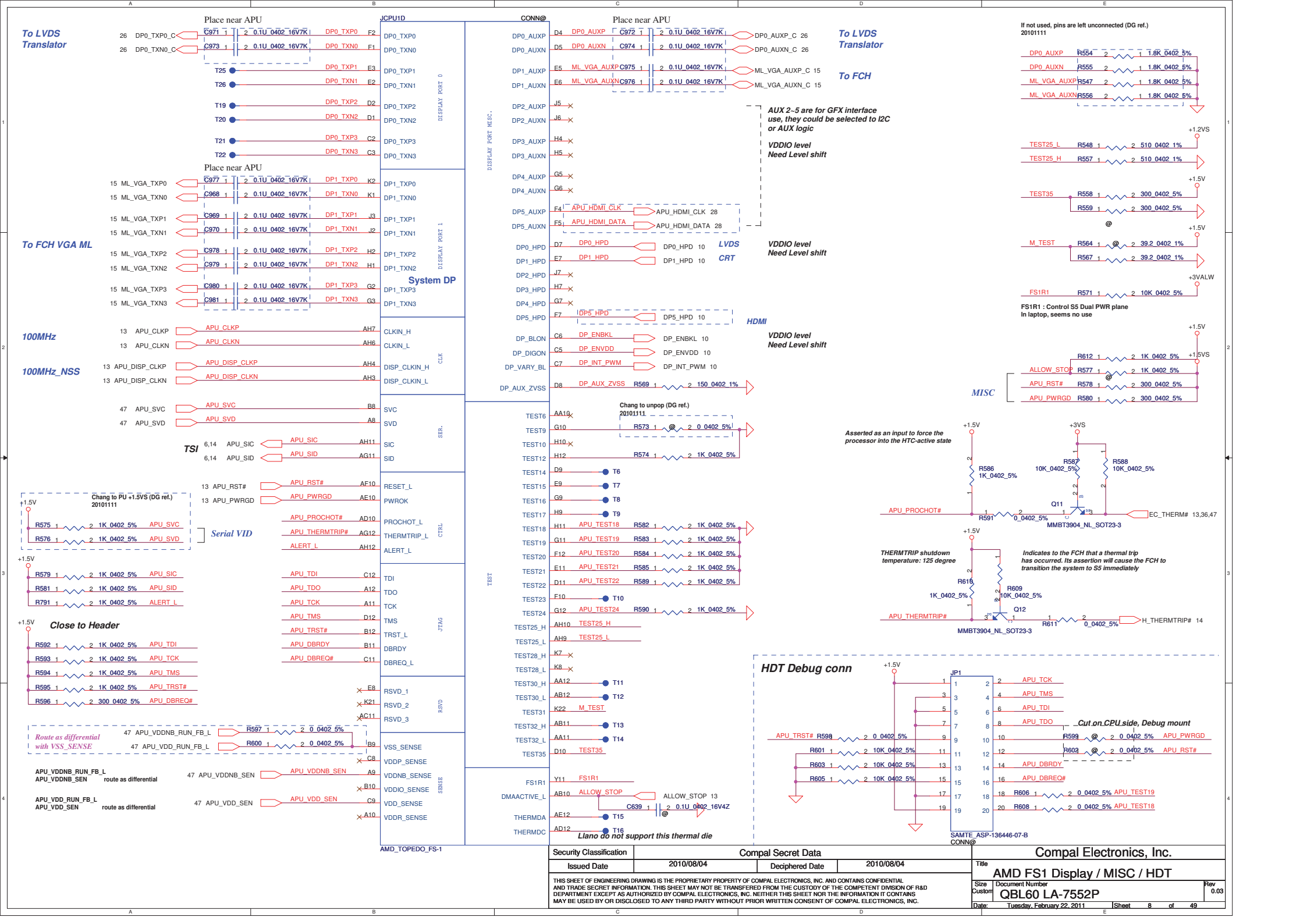

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: AMD FS1 Display / MISC / HDT

Size	Document Number	Rev
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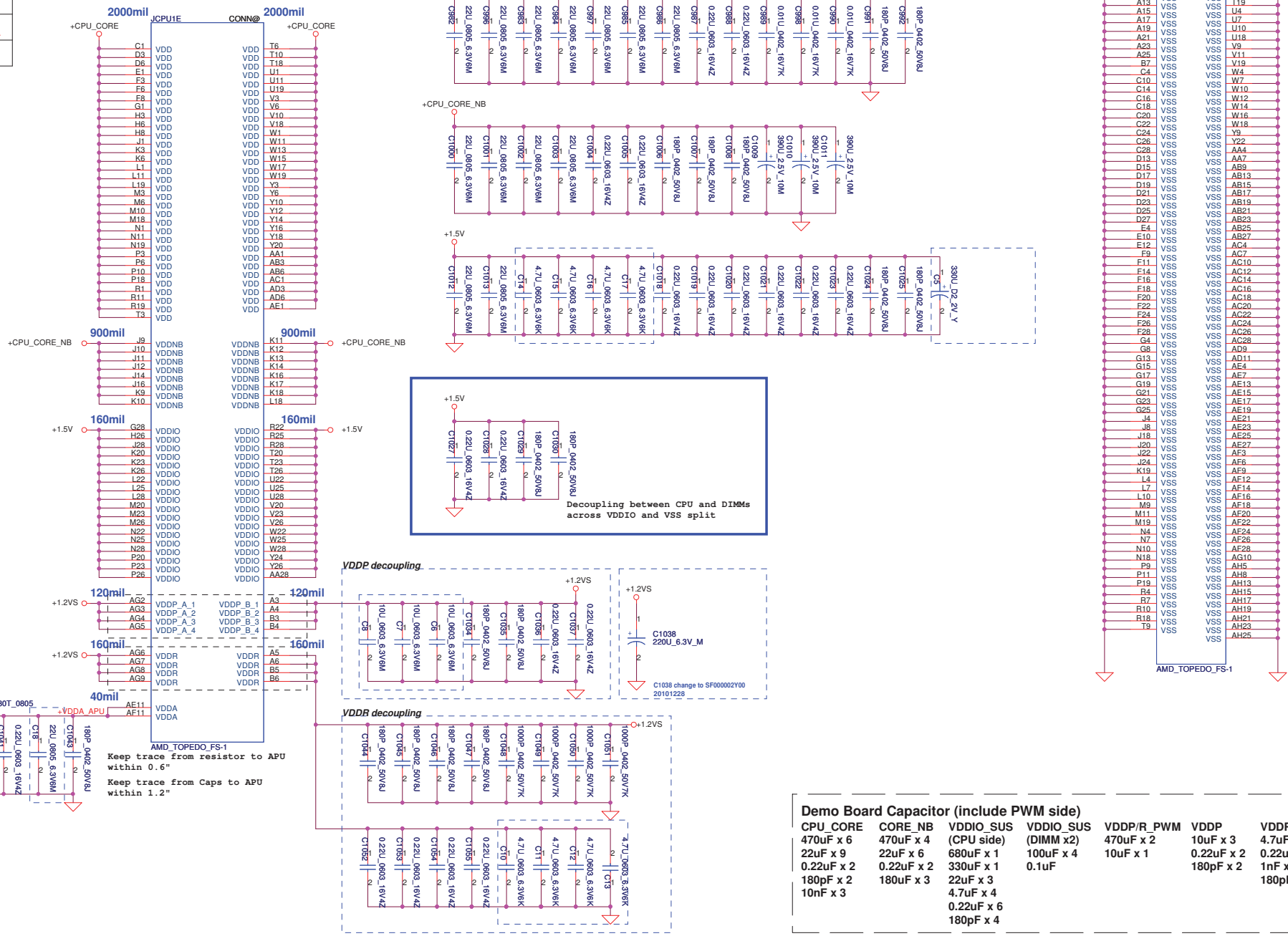
CPU BOTTOM SIDE DECOUPLING

Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11



Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: AMD FS1 PWR / GND

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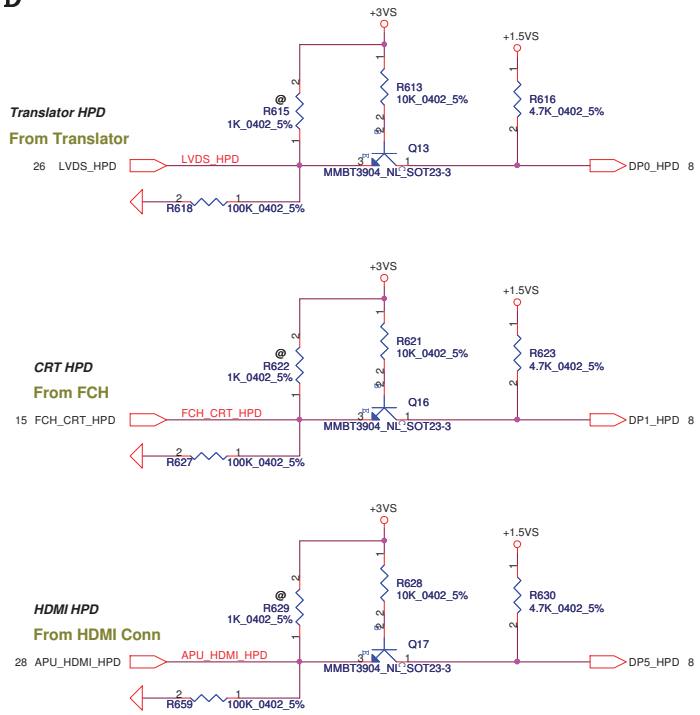
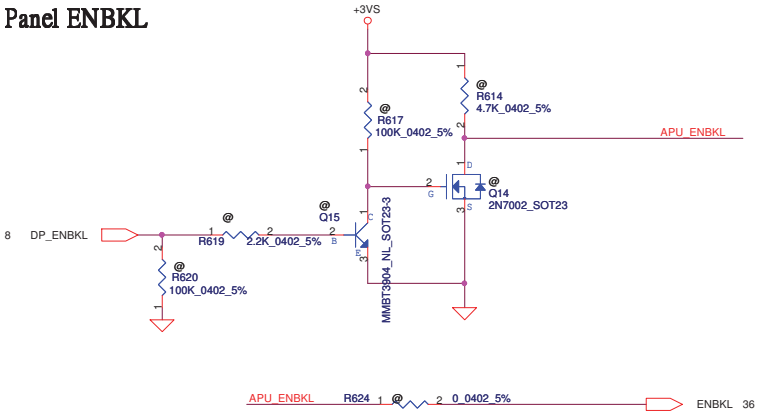
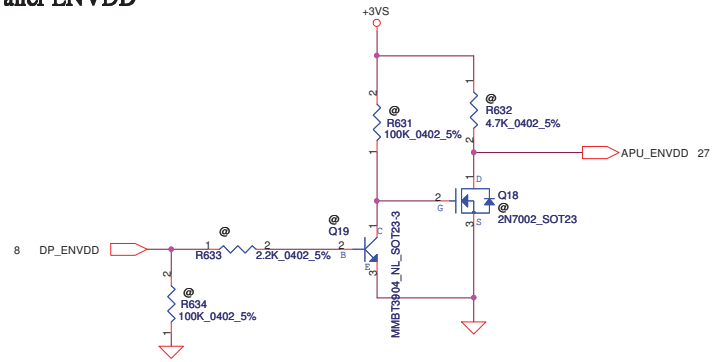
HPD



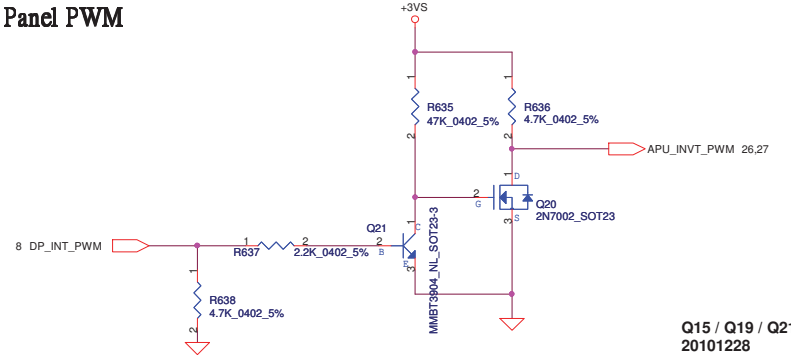
Panel ENBKL



Panel ENVDD



Panel PWM



Q15 / Q19 / Q21 change to SB000006A00 20101228

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Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title	AMD FS1 Singal Level Shifter		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.03
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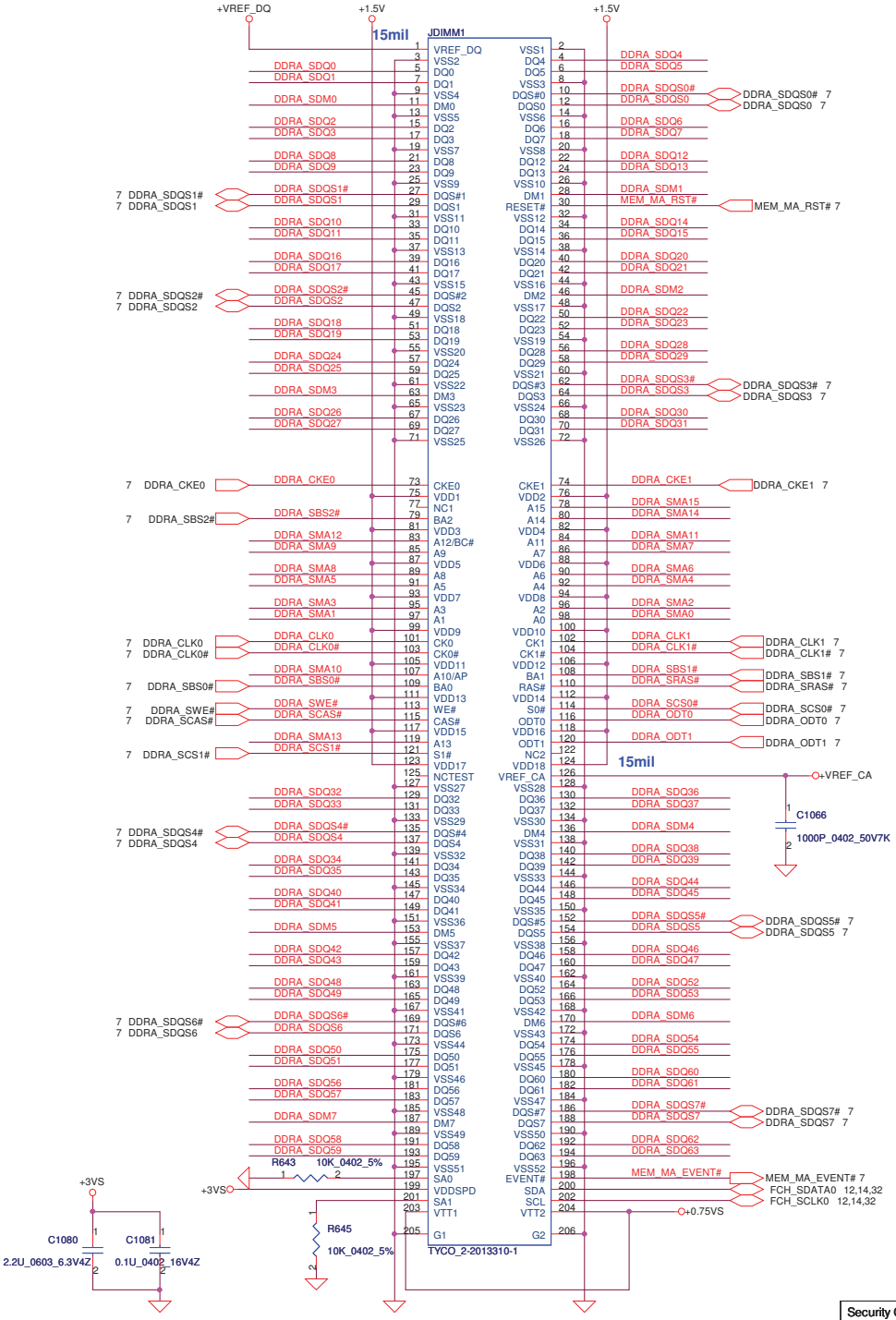
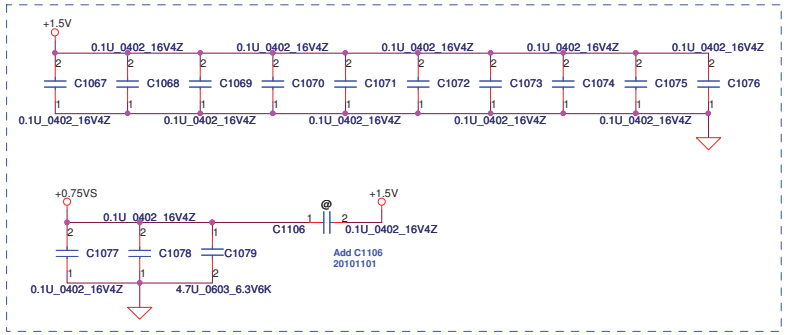
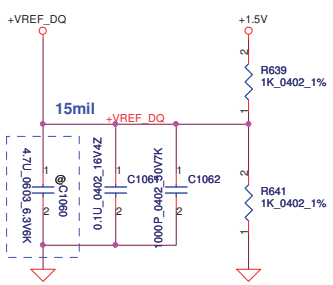
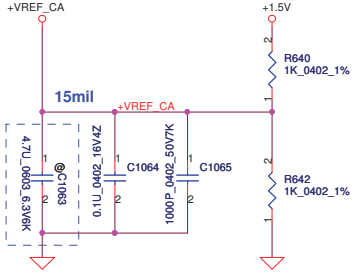


DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 7
DDRA_SDM[0..7] → DDRA_SDM[0..7] 7
DDRA_SMA[0..15] → DDRA_SMA[0..15] 7

Place near DIMM1







DIMM_A STD H:9.2mm

<Address: 00>

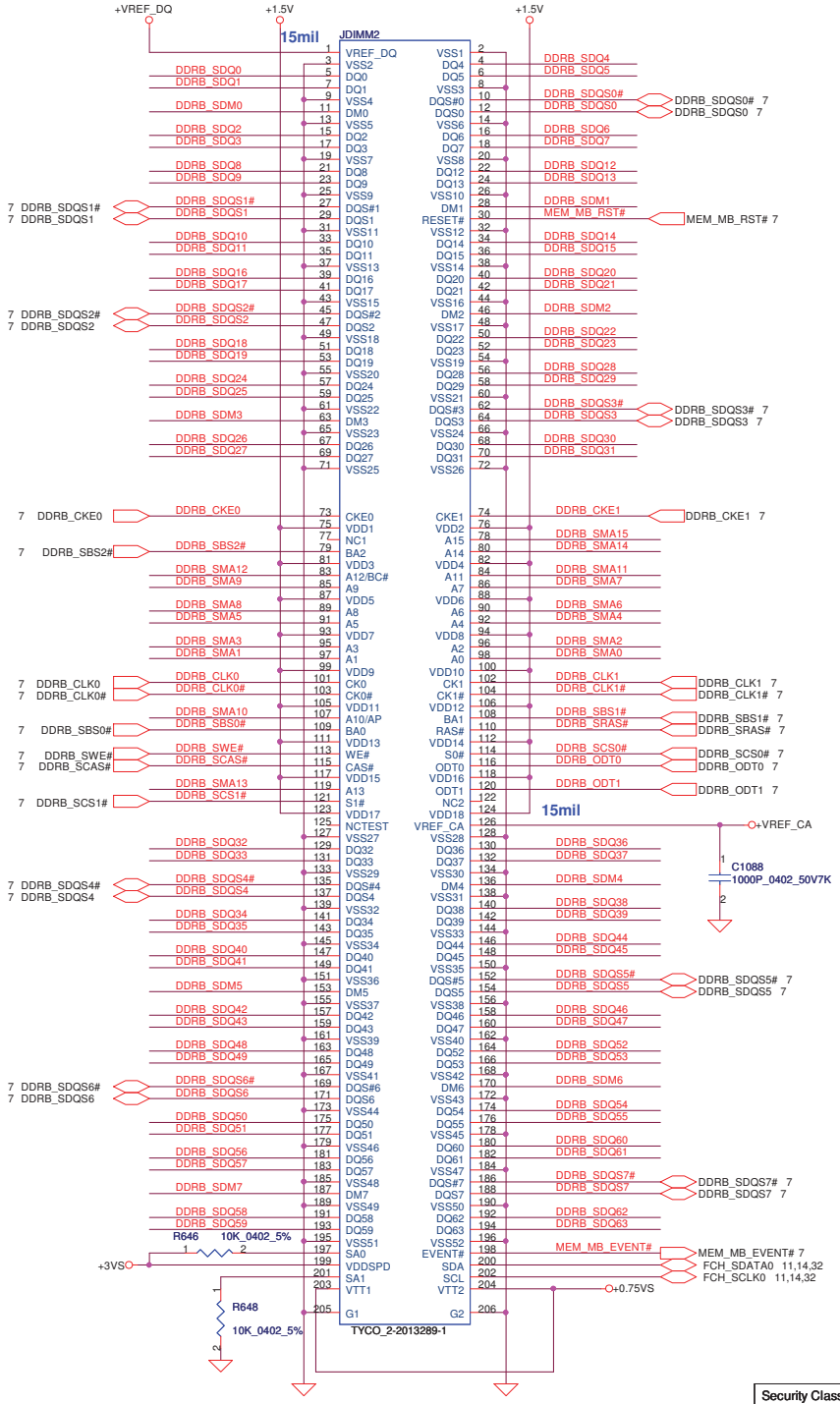
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

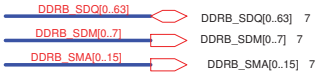
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 11 of 49

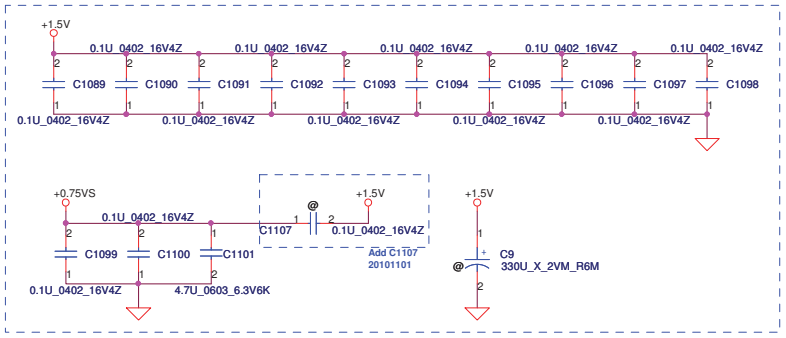


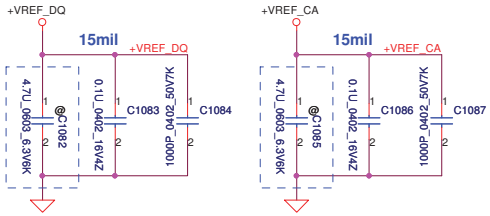
DIMM_B STD H:5.2mm

<Address: 01>



Place near DIMM2





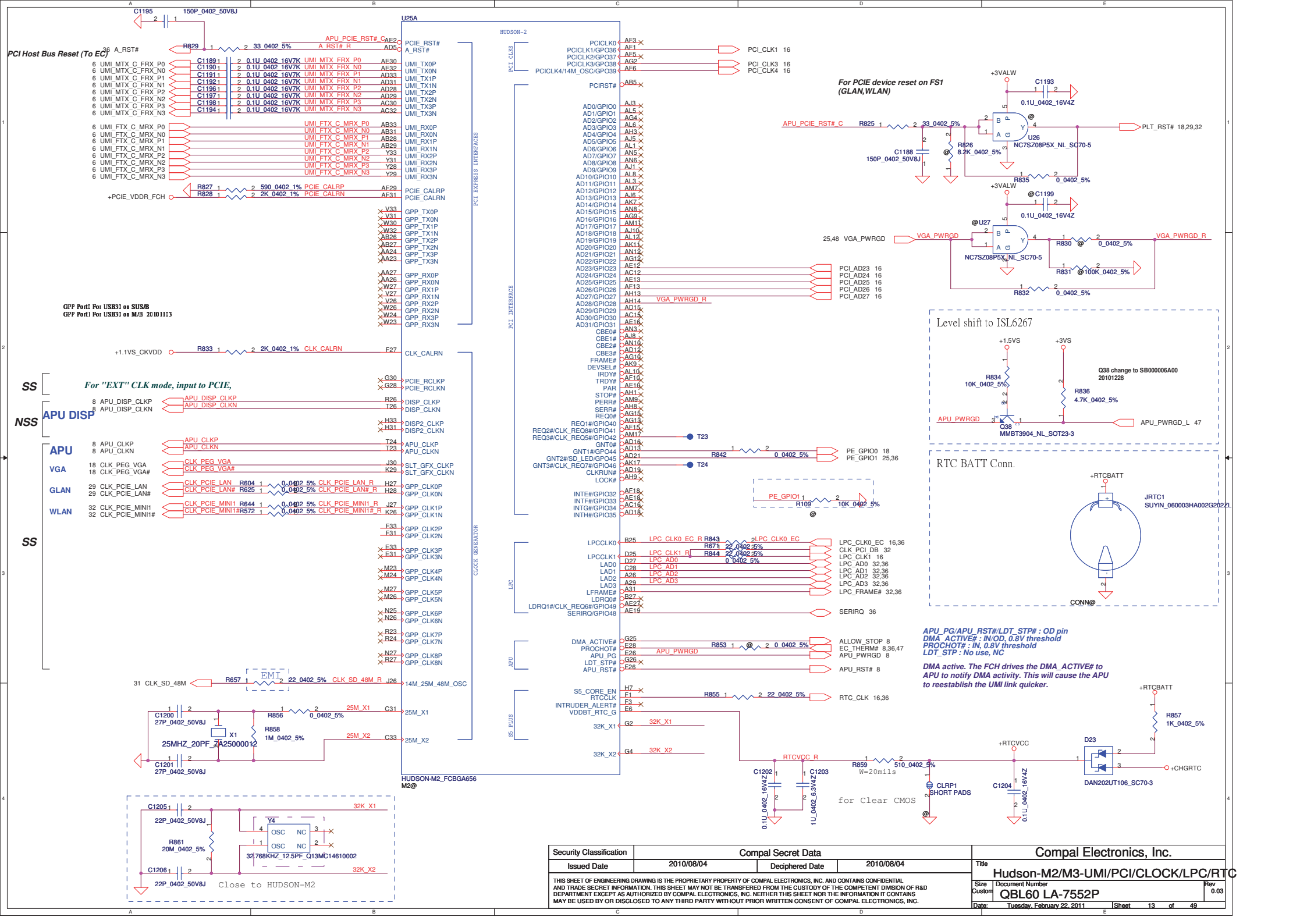
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 | Sheet 12 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 13 of 49

PCIE_RST2 : Reset PCIE device on Hudson2

U25D

HUDSON-2

36 EC_LID_OUT# — EC_LID_OUT# — AB6 PCIE_RST2#/PCI_PME#/GEVENT4#
R2 RI#/GEVENT22#
W7 SPI_CS3#/GBE_STAT1/GEVENT21#
36 SLP_S3# — T3 SLP_S3#
36 SLP_S5# — W2 SLP_S5#
36 PBTN_OUT# — J4 PWR_BTN#
36 FCH_PWRGD — N7 PWR_GOOD

TEST0 — T9 TEST0
TEST1 — T10 TEST1/TMS
TEST2 — V9 TEST2

36 EC_GA20 — AE22 GA20IN/GEVENT0#

36 EC_KBRST# — AG19 KBRST#/GEVENT1#
36 EC_SCI# — R9 LPC_PME#/GEVENT3#
36 EC_SMI# — C26 LPC_SMI#/GEVENT23#
T5 LPC_PD#/GEVENT5#
+3VALW — R18 10K_0402_5% — SYS_RESET# — U4 SYS_RESET#/GEVENT19#
29,32,36 FCH_PCIE_WAKE# — FCH_PCIE_WAKE# — K1 WAKE#/GEVENT8#
V7 IR_RX1/GEVENT20#
8 H_THERMTRIP# — R10 THRMTRIP#/SMBALERT#/GEVENT2#
+3VS — R862 10K_0402_5% — AF19 WD_PWRGD

36 EC_RSMRST# — U2 RSMRST#

ACPI / WAKE UP EVENTS

THERMTRIP:
Need level shift from +3VALW to +1.5V

AG24 CLK_REQ4#/SATA_IS0#/GPIO64
AE24 CLK_REQ3#/SATA_IS1#/GPIO63
AE26 SMARTVOLT1/SATA_IS2#/GPIO50
29 LAN_CLKREQ# — R81 0_0402_5% — LAN_CLKREQ# 1 — AF22 CLK_REQ0#/SATA_IS3#/GPIO60
Modify 2010212-AMD request
AH17 SATA_IS4#/FANOUT3/GPIO55
AG18 SATA_IS5#/FANIN3/GPIO59
AF24 SPKR/GPIO66
11,12,32 FCH_SCLK0 — FCH_SCLK0 — R873 10K_0402_5% — AD26 SCL0/GPIO43
11,12,32 FCH_SDATA0 — FCH_SDATA0 — AD25 SDA0/GPIO47
FCH_SCLK1 — T7 SCL1/GPIO227
FCH_SDATA1 — R7 SDA1/GPIO228
32 MINI1_CLKREQ# — MINI1_CLKREQ# — AG25 CLK_REQ2#/FANIN4/GPIO62
AG22 CLK_REQ1#/FANOUT4/GPIO61
J2 IR_LED#/LLB#/GPIO184
16 VGA_PD — VGA_PD — AG26 SMARTVOLT2/SHUTDOWN#/GPIO51
V8 DDR3_RST#/GEVENT7#/VGA_PD
W8 GBE_LED0/GPIO183
Y6 SPI_HOLD#/GBE_LED1/GEVENT9#
V10 GBE_LED2/GEVENT10#
AA8 GBE_STAT0/GEVENT11#
T29 — AF25 CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#

GPIO

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain
VGA_PD: Support MLDAC power save if connect
0: MLDAC power on
1: MLDAC power off

M7 BLINK/USB_OC7#/GEVENT18#
R8 USB_OC6#/IR_TX1/GEVENT6#
T1 USB_OC5#/IR_TX0/GEVENT17#
P6 USB_OC4#/IR_RX0/GEVENT16#
F5 USB_OC3#/AC_PRES/TDO/GEVENT15#
T28 — P5 USB_OC2#/TCK/GEVENT14#
34 USB_OC1# — USB_OC1# — J7 USB_OC1#/TDI/GEVENT13#
34 USB_OC0# — USB_OC0# — T8 USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#

USB OC

30 HDA_BITCLK_AUDIO — R866 33_0402_5% — HDA_BITCLK — AB3 AZ_BITCLK
30 HDA_SDOUT_AUDIO — R867 33_0402_5% — HDA_SDOUT — AB1 AZ_SDOUT
30 HDA_SDIN0 — HDA_SDIN0 — AA2 AZ_SDIN0/GPIO167
HDA_SDIN1 — Y5 AZ_SDIN1/GPIO168
T31 — Y3 AZ_SDIN2/GPIO169
T35 — Y1 AZ_SDIN3/GPIO170
30 HDA_SYNC_AUDIO — R868 33_0402_5% — HDA_SYNC — AD6 AZ_SYNC
30 HDA_RST_AUDIO# — R869 33_0402_5% — HDA_RST# — AE4 AZ_RST#

HD AUDIO

+3VALW
R55 100K_0402_5% — USB_OC0#
R54 100K_0402_5% — USB_OC1#
R871 10K_0402_5% — H_THERMTRIP#
R874 2.2K_0402_5% — FCH_SCLK1
R876 2.2K_0402_5% — FCH_SDATA1
R877 10K_0402_5% — EC_LID_OUT#
R878 10K_0402_5% — FCH_PCIE_WAKE#
@ Modify 2010212-AMD request

+3VS
R880 2.2K_0402_5% — FCH_SCLK0
R881 2.2K_0402_5% — FCH_SDATA0
R882 8.2K_0402_5% — MINI1_CLKREQ#
@ Modify 2010212-AMD request

R940 8.2K_0402_5% — LAN_CLKREQ# 1
Modify 20101111

R884 2.2K_0402_5% — EC_RSMRST#
R885 @ 10K_0402_5% — HDA_BITCLK
R886 @ 10K_0402_5% — HDA_SDIN0
R888 @ 10K_0402_5% — HDA_SDIN1

+3VALW
R47 8.2K_0402_5% — R45 8.2K_0402_5% — R43 8.2K_0402_5%
R48 8.2K_0402_5% — R46 8.2K_0402_5% — R44 8.2K_0402_5%
FCH_GPIO189
FCH_GPIO190
FCH_GPIO191

Project SKU ID		
GPIO189 (use VGA)	L(NO) R44	H(YES) R43
GPIO190 (use PX)	L(NO) R46	H(YES) R45
GPIO191	L(15") R48	H(17") R47

Add Project ID Table
201011301600

T27 — K19 PS2_DAT/SDA4/GPIO187
J19 PS2_CLK/CEC/SCL4/GPIO188
J21 SPI_CS2#/GBE_STAT2/GPIO166

FCH_GPIO189 — D21 PS2KB_DAT/GPIO189
FCH_GPIO190 — C20 PS2KB_CLK/GPIO190
FCH_GPIO191 — D23 PS2M_DAT/GPIO191
C22 PS2M_CLK/GPIO192

EMBEDDED CTRL

F21 KSO_0/GPIO209
E20 KSO_1/GPIO210
F20 KSO_2/GPIO211
A22 KSO_3/GPIO212
E18 KSO_4/GPIO213
A20 KSO_5/GPIO214
J18 KSO_6/GPIO215
H18 KSO_7/GPIO216
G18 KSO_8/GPIO217
B21 KSO_9/GPIO218
K18 KSO_10/GPIO219
D19 KSO_11/GPIO220
A18 KSO_12/GPIO221
C18 KSO_13/GPIO222
B19 KSO_14/GPIO223
B17 KSO_15/GPIO224
A24 KSO_16/GPIO225
D17 KSO_17/GPIO226

HUDSON-M2_FCBGA656
M2@

USB MISC

USBCLK/14M_25M_48M_OSC — G8
USB_RCOMP — B9 — USB_RCOMP — R863 11.8K_0402_1%

USB 1.1

USB_FSD1P/GPIO186 — H1
USB_FSD1N — H3
USB_FSD0P/GPIO185 — H6
USB_FSD0N — H5

USB 2.0

USB_HSD13P — H10
USB_HSD13N — G10
USB_HSD12P — K10
USB_HSD12N — J12
USB_HSD11P — G12
USB_HSD11N — F12
USB_HSD10P — K12 — USB20_P10 — USB20_P10 34
USB_HSD10N — K13 — USB20_N10 — USB20_N10 34 — USB1
USB_HSD9P — B11
USB_HSD9N — D11
USB_HSD8P — E10
USB_HSD8N — F10
USB_HSD7P — C10
USB_HSD7N — A10
USB_HSD6P — H9
USB_HSD6N — G9
USB_HSD5P — A8
USB_HSD5N — C8
USB_HSD4P — F8 — USB20_P4 — USB20_P4 31 — CardReder
USB_HSD4N — E8 — USB20_N4 — USB20_N4 31
USB_HSD3P — C6 — USB20_P3 — USB20_P3 32 — WLAN(BT)
USB_HSD3N — A6 — USB20_N3 — USB20_N3 32
USB_HSD2P — C5 — USB20_P2 — USB20_P2 27 — CMOS
USB_HSD2N — A5 — USB20_N2 — USB20_N2 27
USB_HSD1P — C1 — USB20_P1 — USB20_P1 30 — USB3
USB_HSD1N — C3 — USB20_N1 — USB20_N1 30
USB_HSD0P — E1 — USB20_P0 — USB20_P0 34 — USB2
USB_HSD0N — E3 — USB20_N0 — USB20_N0 34

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2

USB 3.0

USBSS_CALRP — C16 — USBSS_CALRP — R864 1K_0402_1% — M3@
USBSS_CALRN — A16 — USBSS_CALRN — R865 1K_0402_1% — M3@ — +FCH_VDD_11_SSUSB_S
USB_SS_TX3P — A14
USB_SS_TX3N — C14
USB_SS_RX3P — C12
USB_SS_RX3N — A12
USB_SS_TX2P — D15
USB_SS_TX2N — B15
USB_SS_RX2P — E14
USB_SS_RX2N — F14
USB_SS_TX1P — F15
USB_SS_TX1N — G15
USB_SS_RX1P — H13
USB_SS_RX1N — G13
USB_SS_TX0P — J16 — USB30_MTX_DRX_P0 — C39 0.1U_0402_16V7K — M3@ — USB30_MTX_C_DRX_P0 34
USB_SS_TX0N — H16 — USB30_MTX_DRX_N0 — C37 0.1U_0402_16V7K — M3@ — USB30_MTX_C_DRX_N0 34
USB_SS_RX0P — J15 — USB30_MRX_DTX_P0 — USB30_MRX_DTX_P0 34
USB_SS_RX0N — K15 — USB30_MRX_DTX_N0 — USB30_MRX_DTX_N0 34

On board USB Conn
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

SCL2/GPIO193 — H19 — R870 10K_0402_5%
SDA2/GPIO194 — G19 — R872 10K_0402_5%
SCL3_LV/GPIO195 — G22 — APU_SIC — APU_SIC 6,8
SDA3_LV/GPIO196 — G21 — APU_SID — APU_SID 6,8
EC_PWM0/EC_TIMER0/GPIO197 — F22
EC_PWM1/EC_TIMER1/GPIO198 — H22
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 — J22 — EC_PWM2 — EC_PWM2 16
EC_PWM3/EC_TIMER3/GPIO200 — H21

KSI_0/GPIO201 — K21
KSI_1/GPIO202 — K22
KSI_2/GPIO203 — F22
KSI_3/GPIO204 — F24
KSI_4/GPIO205 — E24
KSI_5/GPIO206 — B23
KSI_6/GPIO207 — C24
KSI_7/GPIO208 — F18

+3VALW — *For FCH internal debug use*
R887 @ 2.2K_0402_5% — TEST0
R889 @ 2.2K_0402_5% — TEST1
R890 @ 2.2K_0402_5% — TEST2

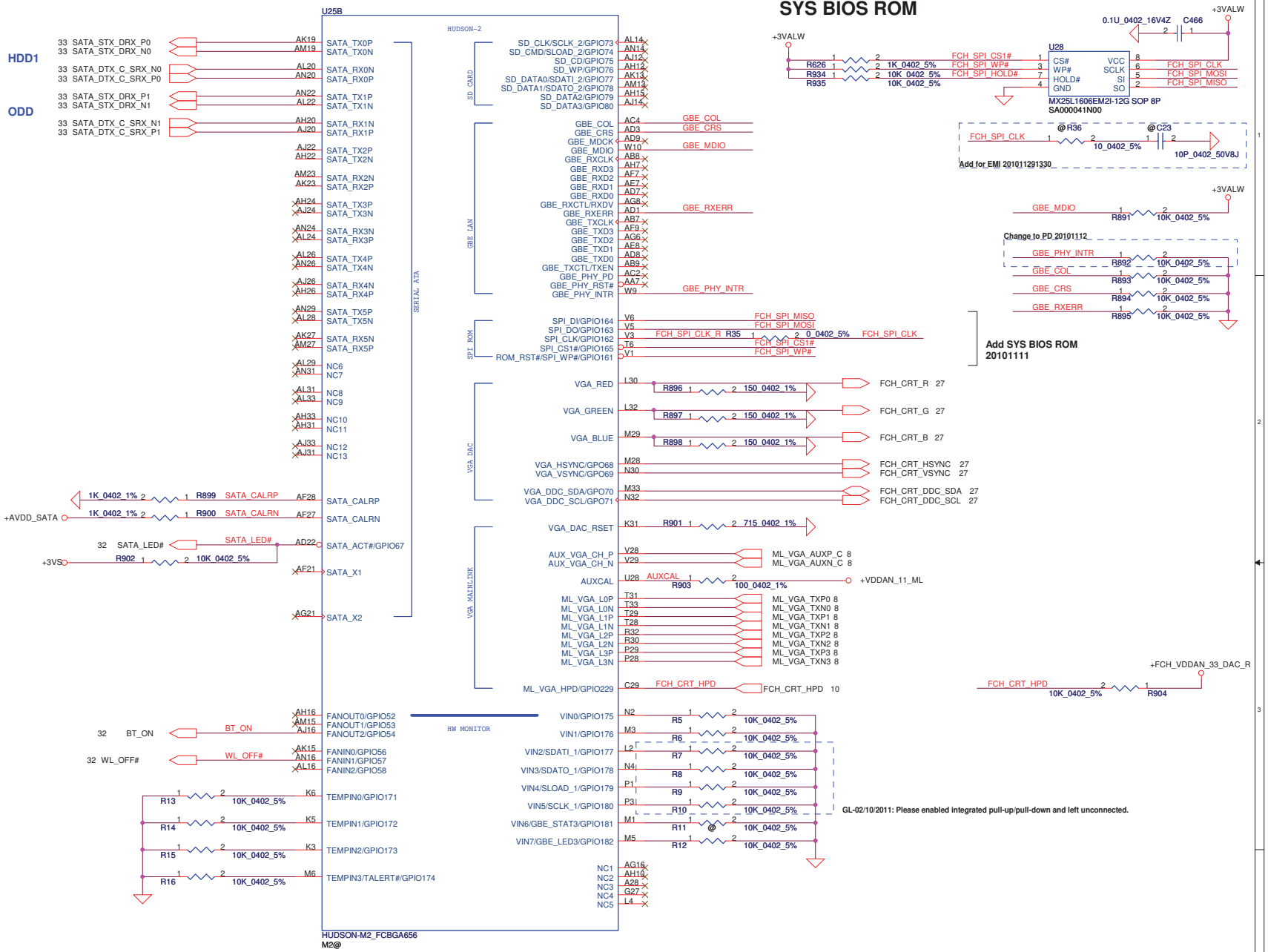
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 14 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

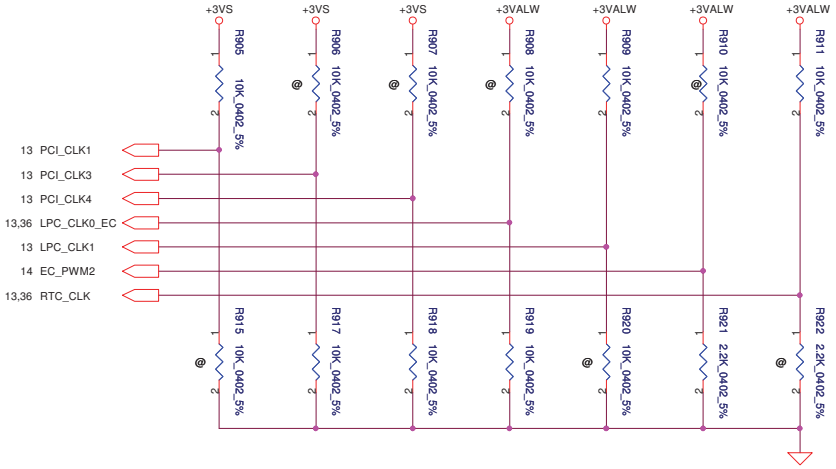
Title: Hudson-M2/M3-SATA/GBE/HWM

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 15 of 49

STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

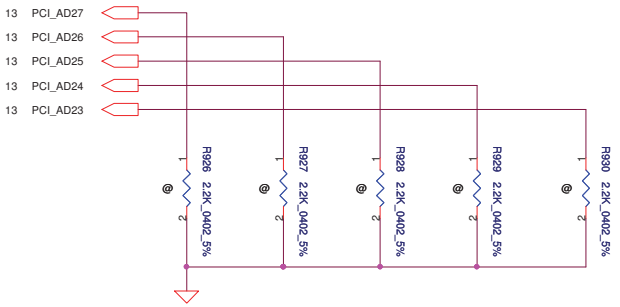


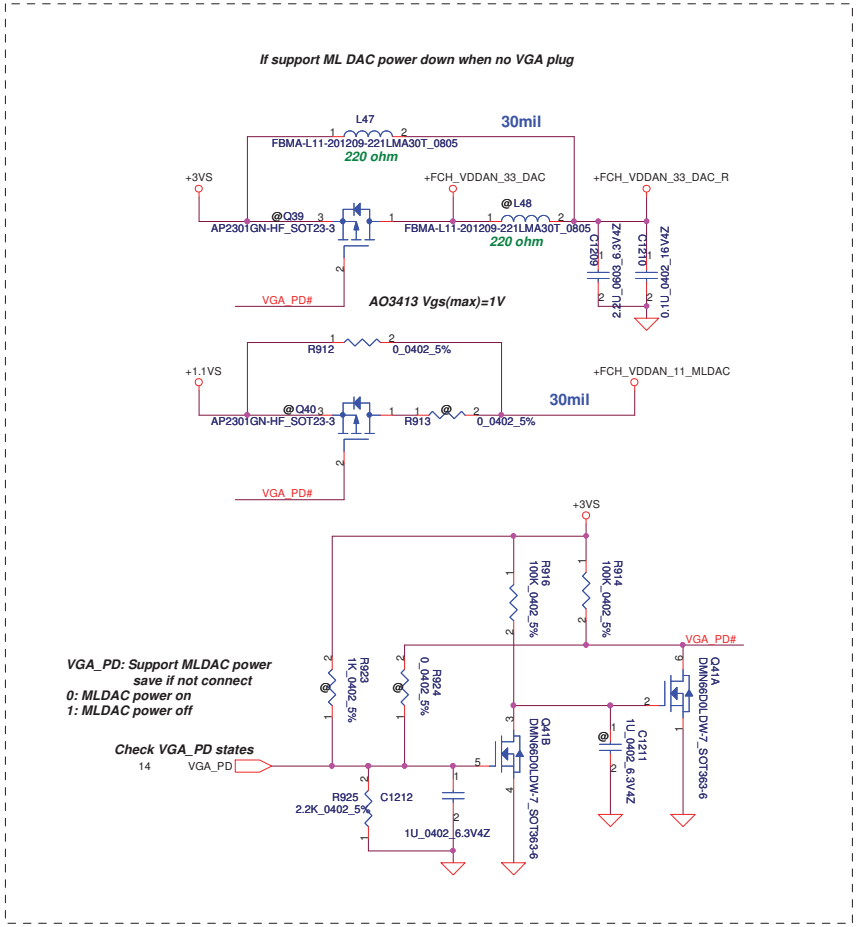
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26

	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 16 of 49

C1218 / C1219 / C1247 Change to SE00000I10
20101228

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB outputs

For A11: Cap = 1nF
For A12, Cap = DNI

R1242 change to 2.2uf-AMD request 20110212

change to 0ohm-AMD request 20110212

change to four 1uf-AMD request 20110212

For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S Connected to VSS.

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

Connected to VSS through a dedicated via.

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

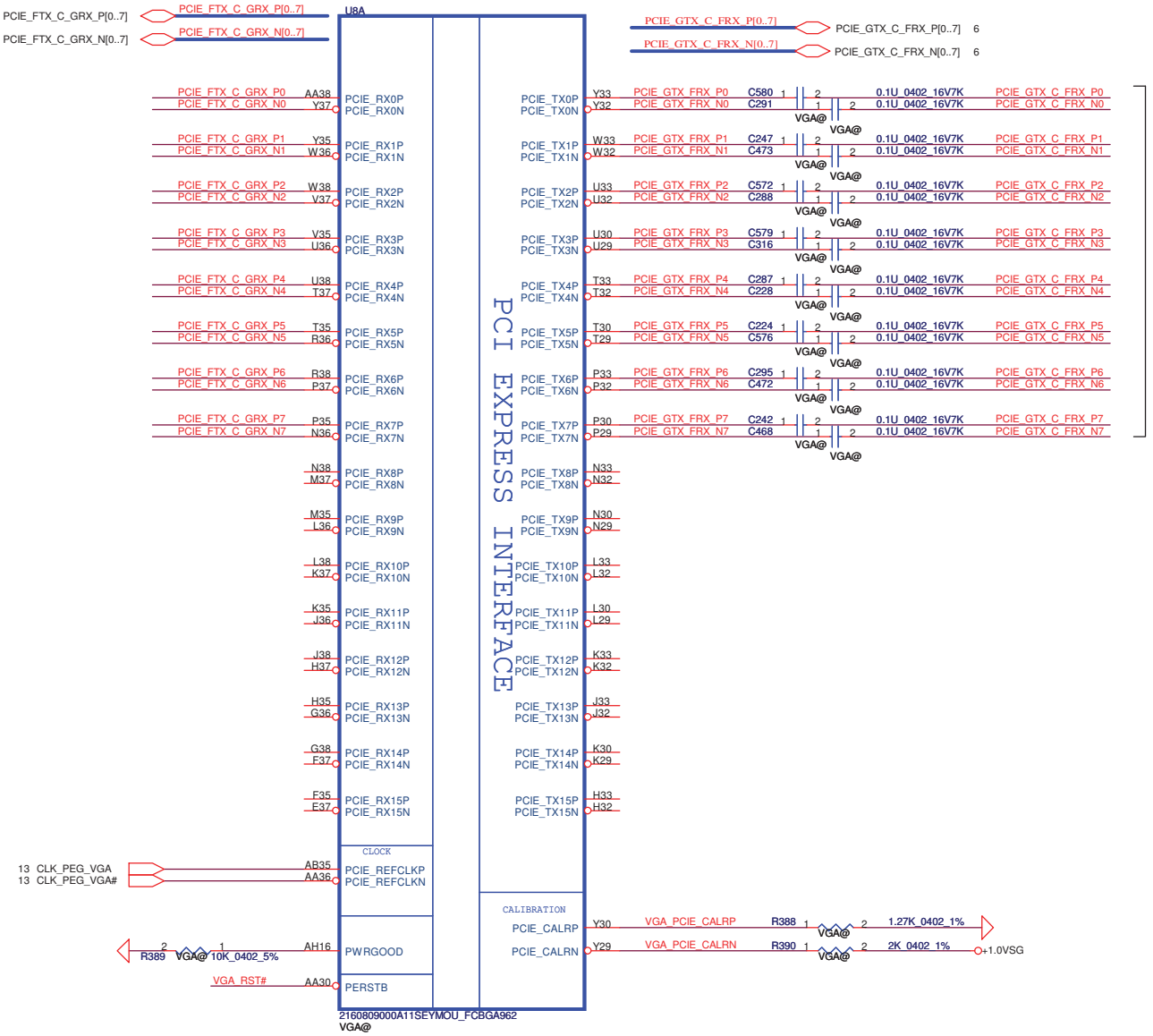
Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 17 of 49

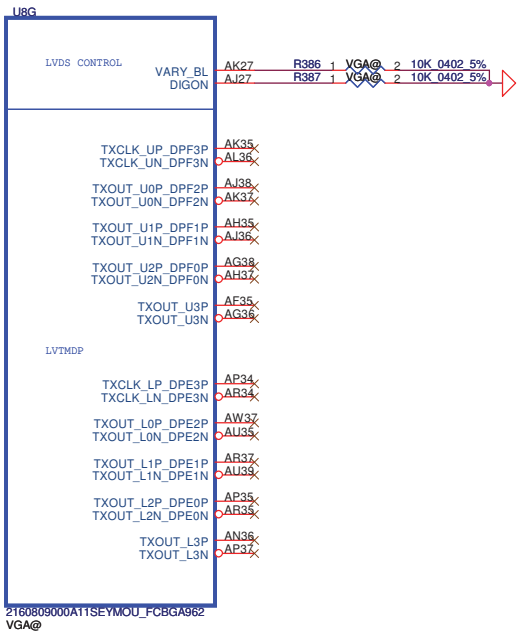
GFX PCIE LANE REVERSAL

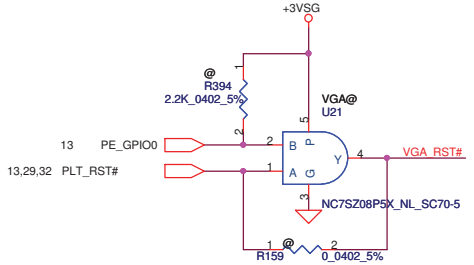


For UMA Mux.

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need





Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 | Sheet 18 of 49

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

VRAM ID

GPIO5 fast-power reduction:
HW control will casue display disturb should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N,

GPIO7 Controls backlight on/off.
Active High ,need external PD
If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device
ON(1)/OFF(0) inter PD

Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

For ATI Cross fire
no use can NC

SM010030010
200ma 120ohm@100mhz DCR 0.2

Future ASIC call MLPS.
OLD ASIC is Fan PWM

120ohm/0.3A

External VGA Thermal Sensor

ADM1032ARMZ-2REEL_MSOP8

Q8A DMN66D0LDW-7_SOT363-6

Q8B DMN66D0LDW-7_SOT363-6

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

GPIO8 Serial-ROM output from ROM.	if GPIO22 High ,GPIO 11-13->CFG[0:2]
GPIO9 Serial-ROM input to ROM.	Config ROM type ,GPU has internal PD
GPIO10 Serial-ROM clock to ROM.	if GPIO22 Low ,GPIO 11-13->CFG[0:2]
GPIO22 erternal BIOS-ROM enable	Config Primary memory-aperture size
	CFG[3:0]
GPIO8,GPIO9,GPIO10 no use can NC	128MB 000
GPIO22	256MB 001 *
Enable need 3K PH ,no use must NC	64MB 010

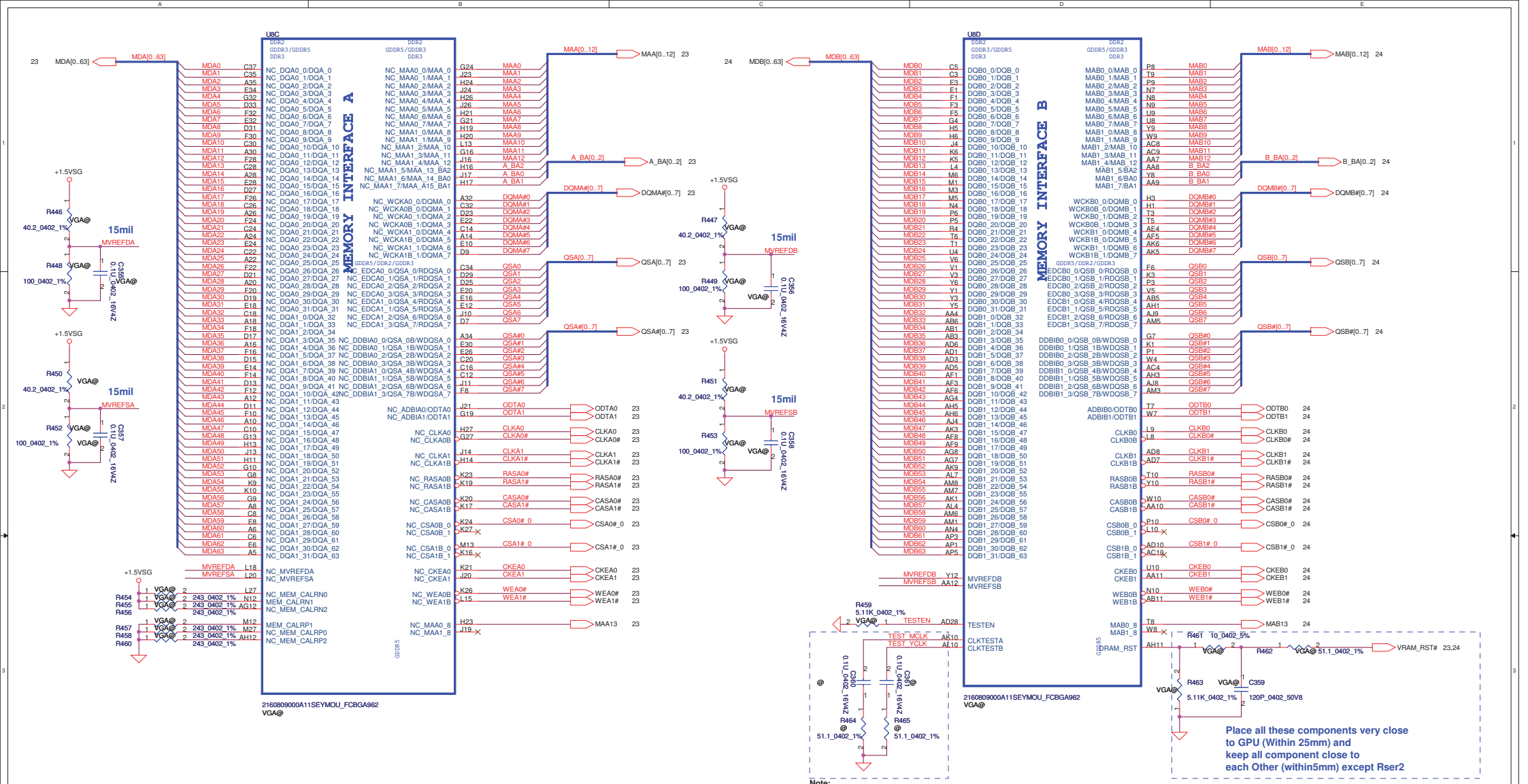
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 19 of 49



Note:
route 50ohms single-ended
and 100ohms diff
and keep short
REF137-03 suggest

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within5mm) except Rser2

Park&Seymour is single channel for memory (channel B only)

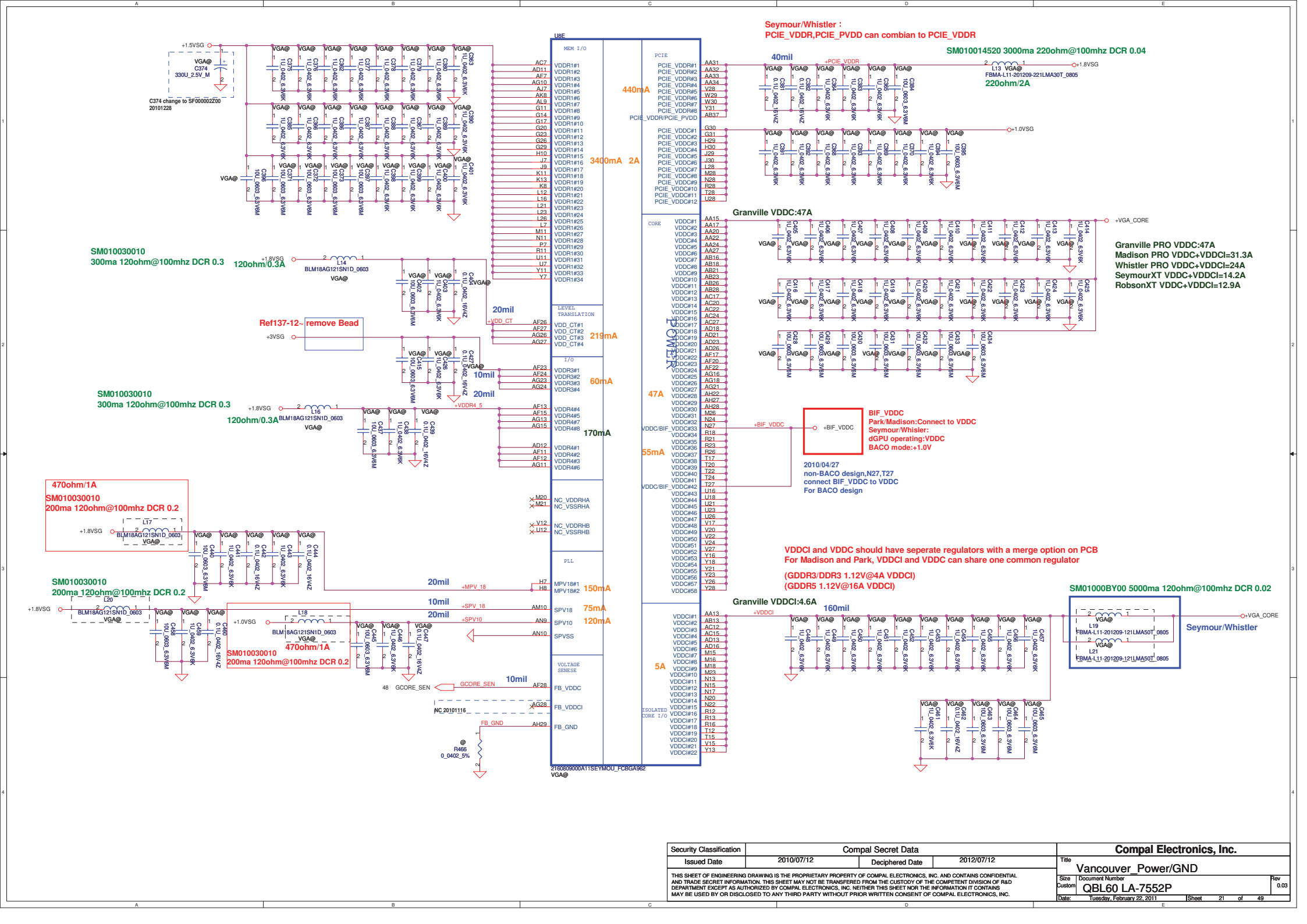
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Memory

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 | Sheet 20 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title	Vancouver_Power/GND	
Size: Custom	Document Number: QBL60 LA-7552P	Rev: 0.03
Date: Tuesday, February 22, 2011	Sheet 21 of 49	

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

GND

216080900 0A11SEYMOU_FCBGA962
VGA@

REF137-13 update

U8H

Manhatann:300mA
Seymour:150mA

Manhatann:220mA
Seymour:110mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
FootPrint

DP mode:300mA
LVDS mode:440mA

DP mode:220mA
LVDS mode:240mA

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

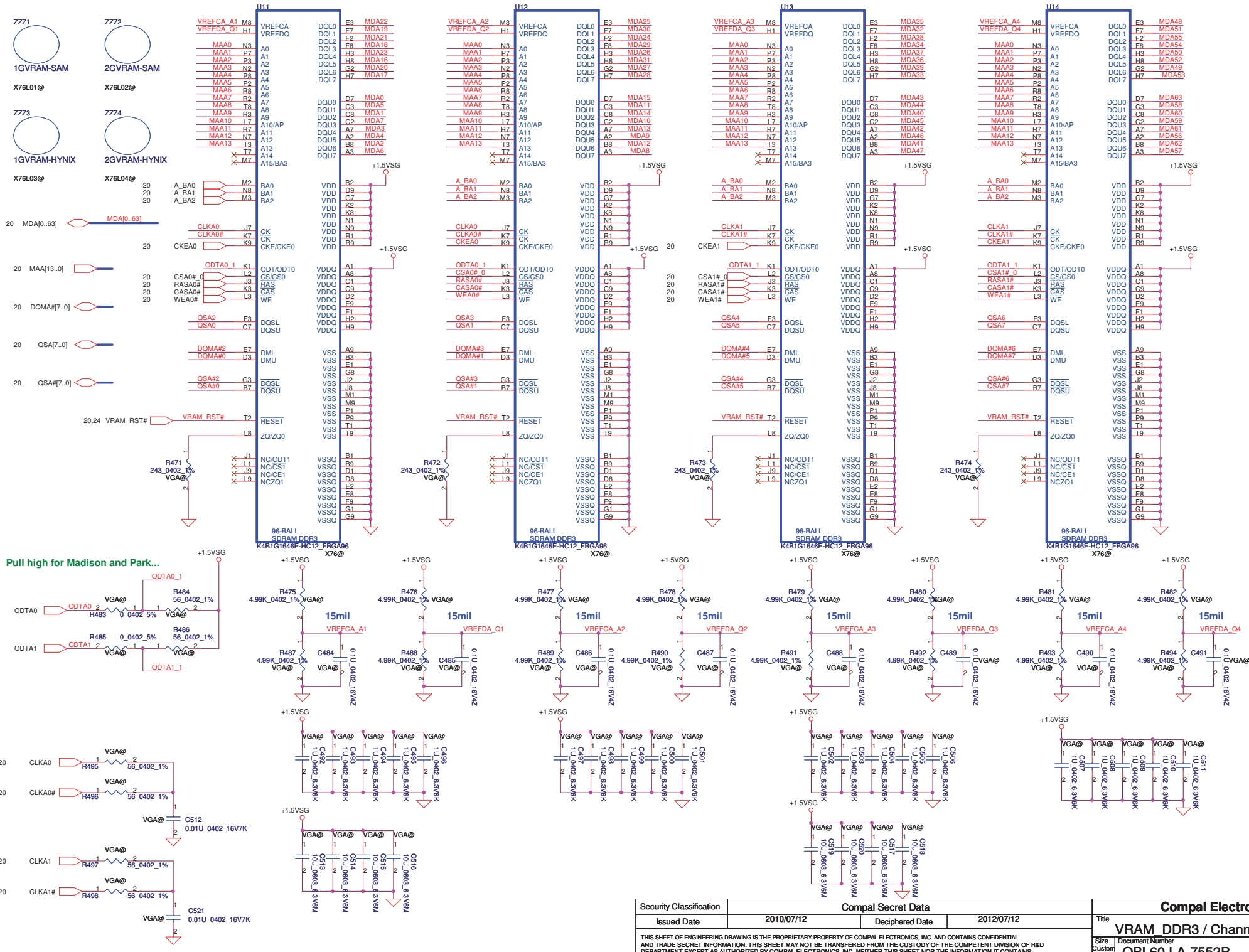
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 22 of 49



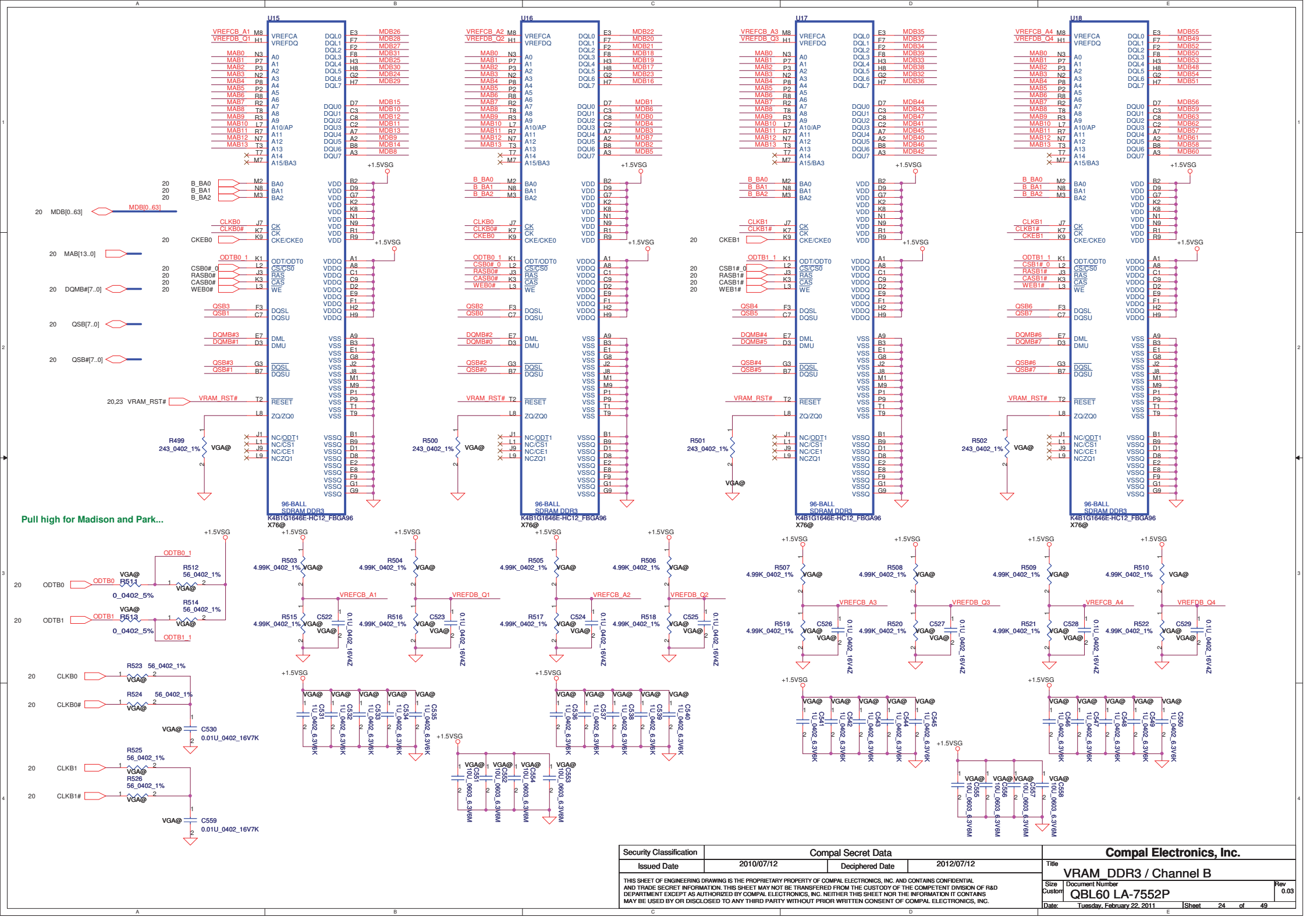
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 | Sheet 23 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

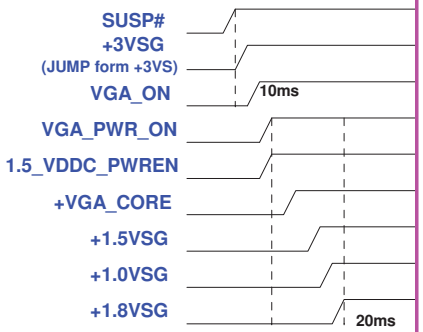
Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

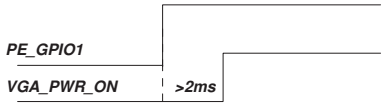
Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 | Sheet 24 of 49

Power Sequence of Whistler and Seymour

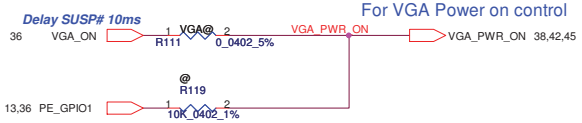


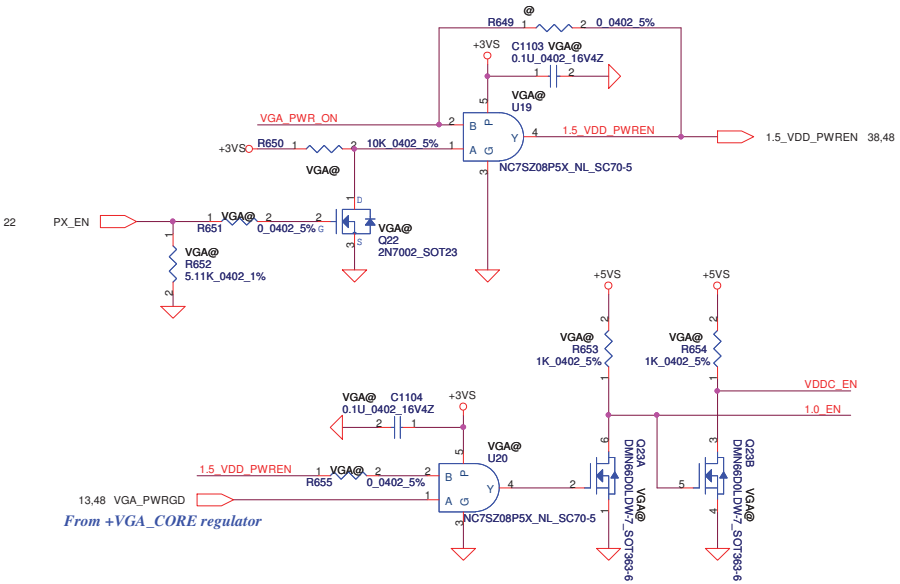
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

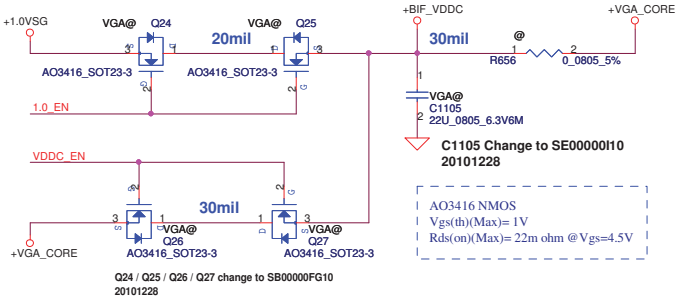


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN





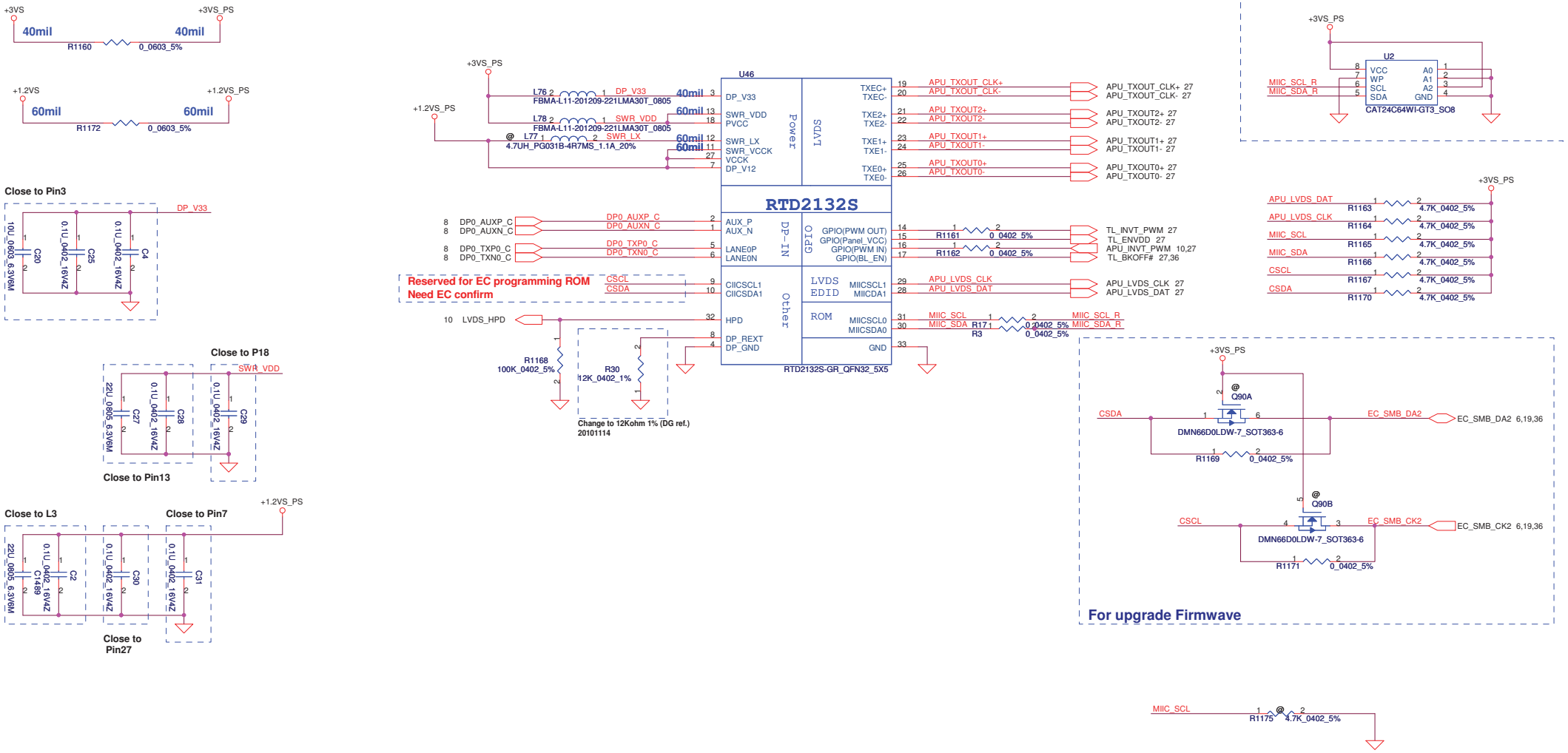


Compal Electronics, Inc.

Title: VGA power sequence and BACO

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 25 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title: LVDS Translator - RTD2132S

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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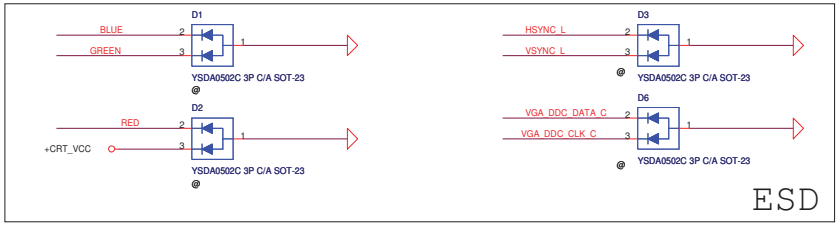
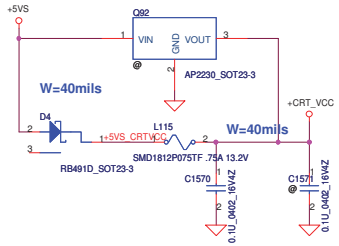
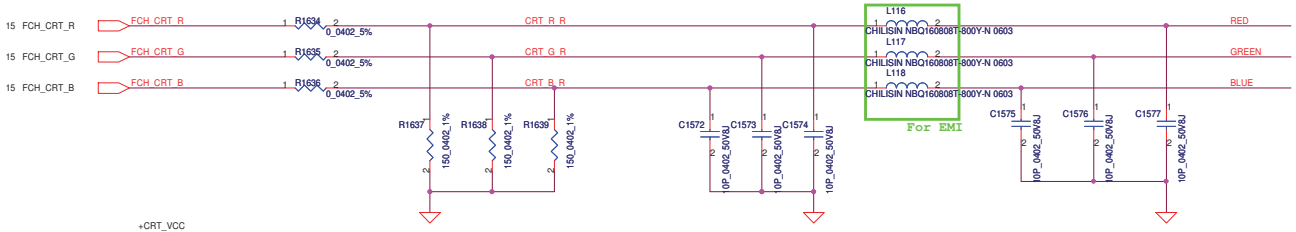
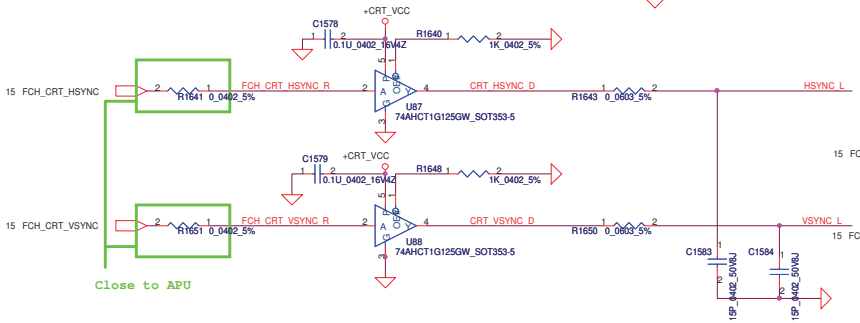
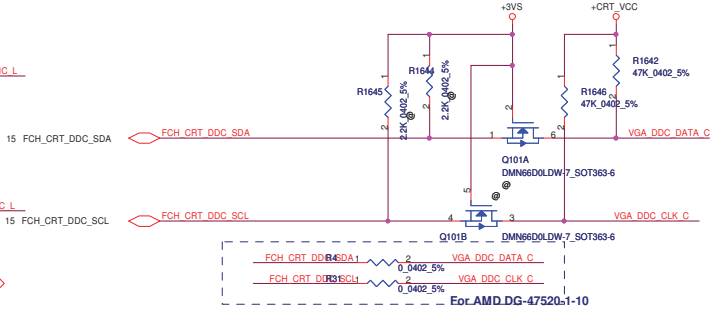
CRT

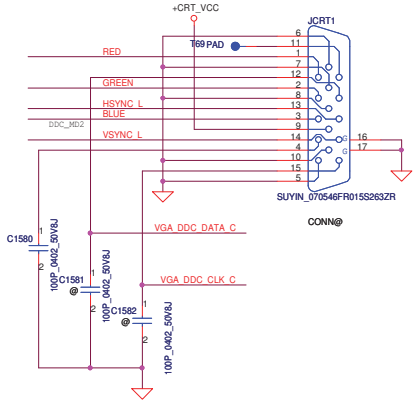




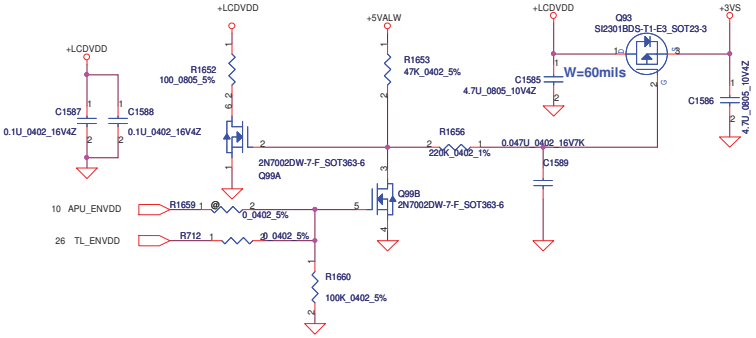


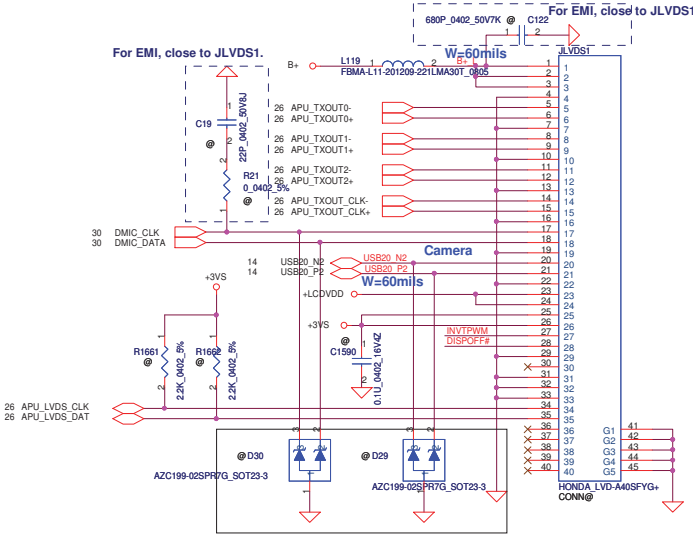




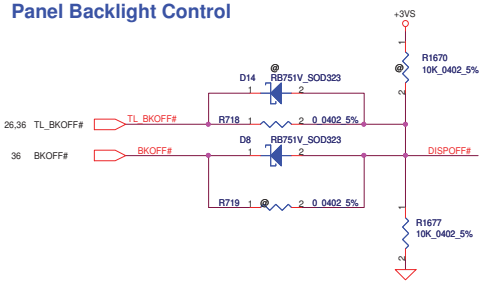


Panel LCDVDD Control

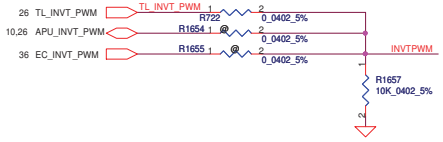




Panel Backlight Control



Panel PWM Control



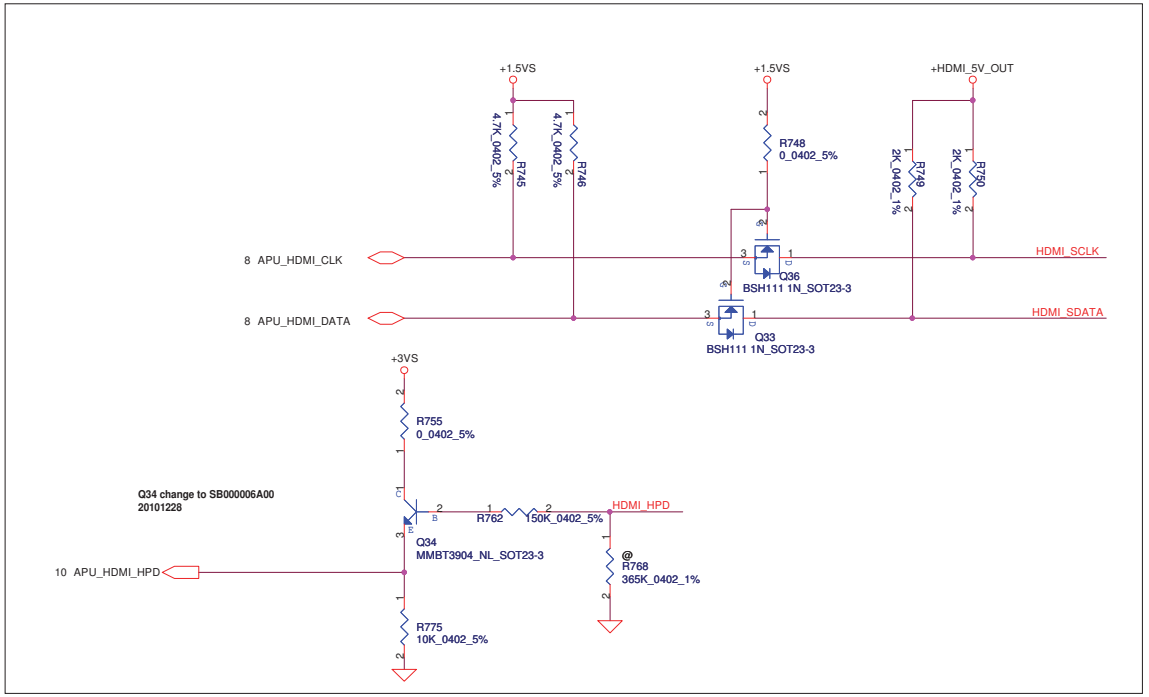
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

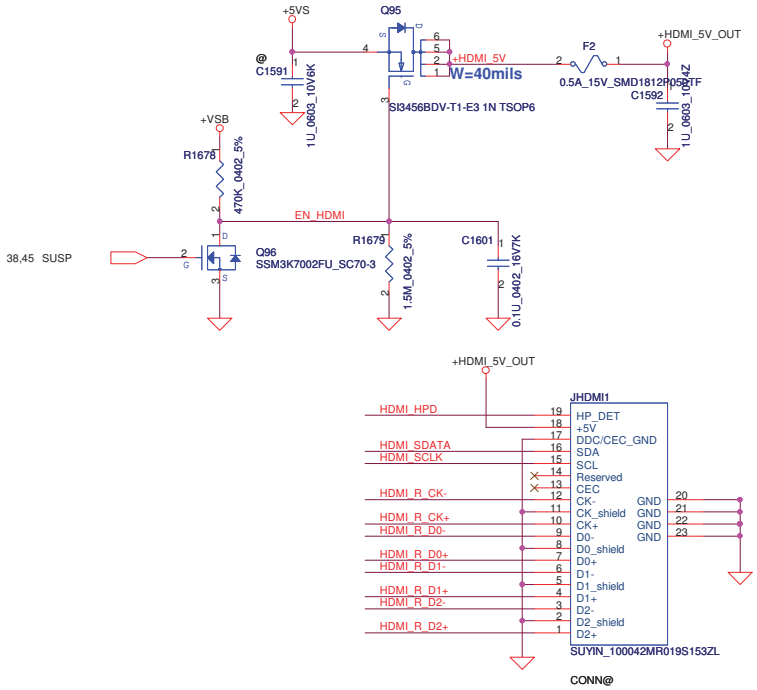
Compal Electronics, Inc.

Title: P10-LVDS/CRT CONN

Size	Document Number	Rev
C	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 27 of 49

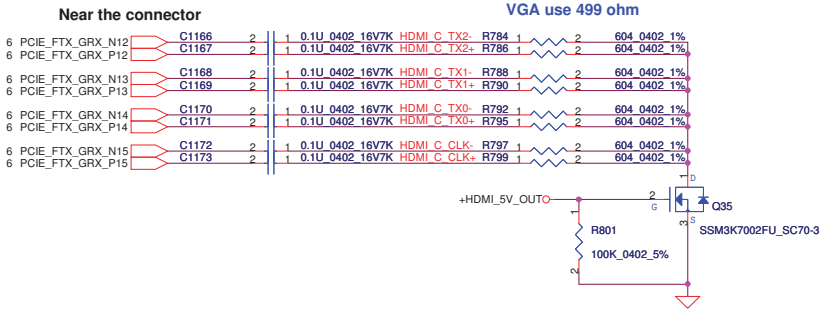


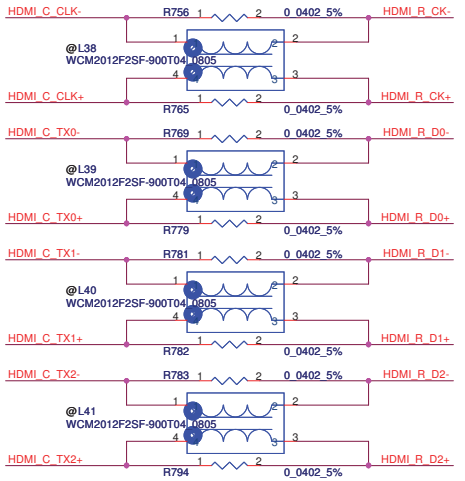


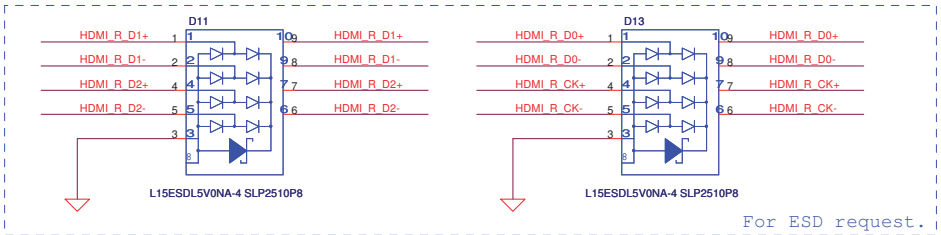
From APU

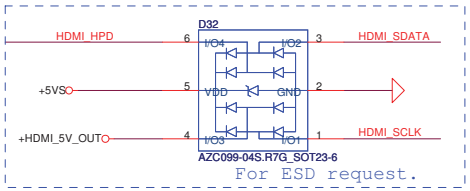
Near the connector

UMA use 604 ohm
VGA use 499 ohm









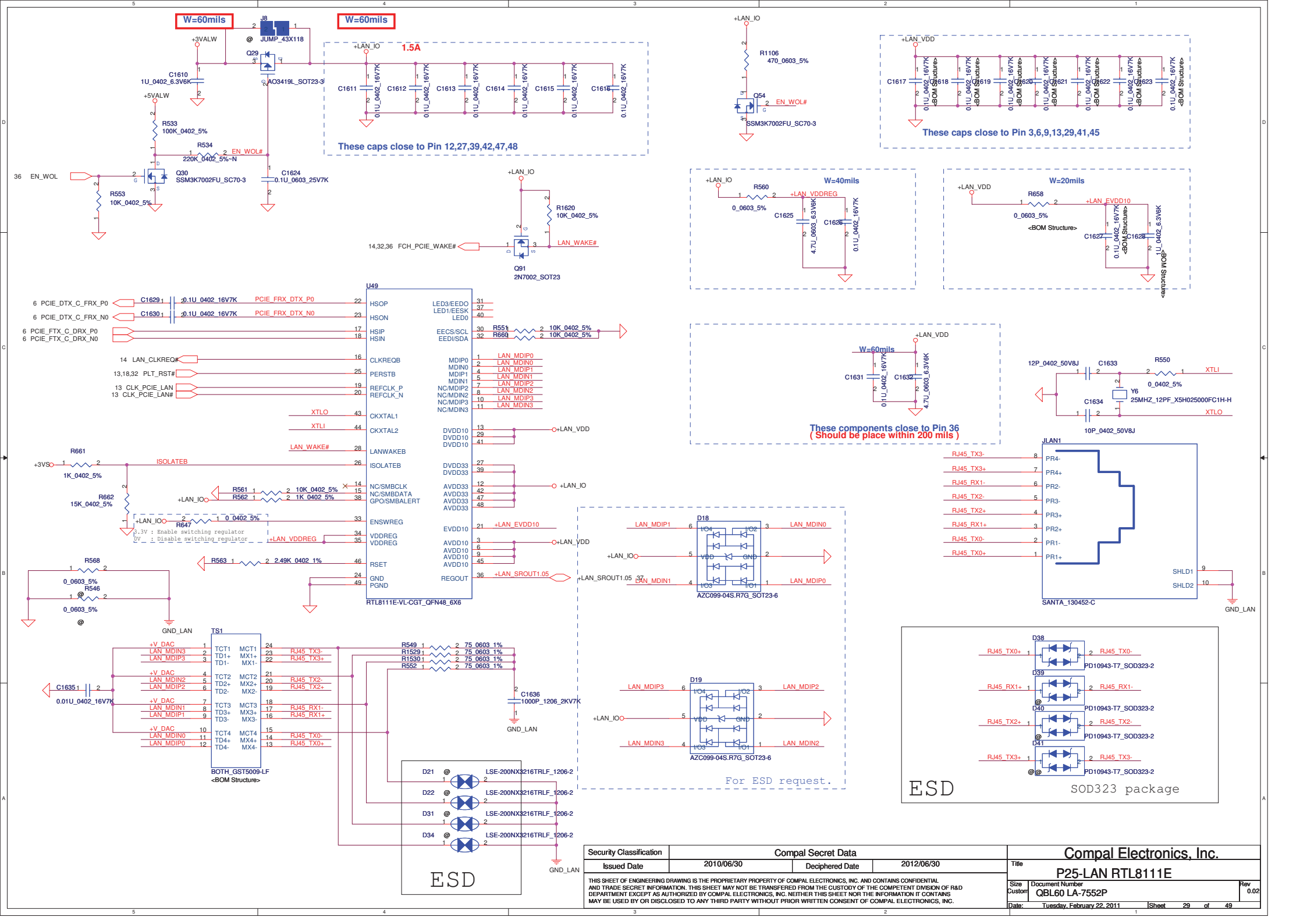
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 28 of 49



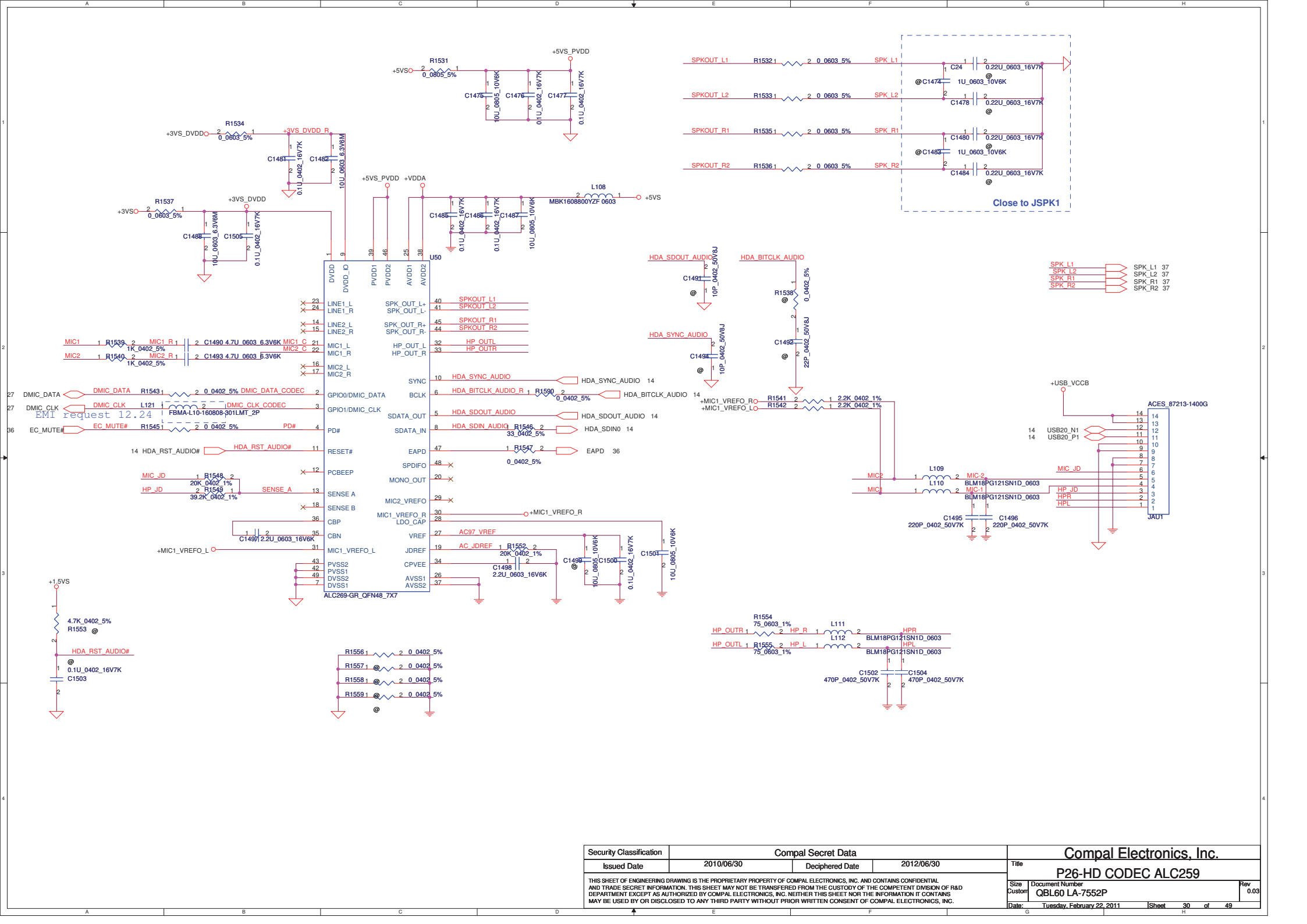
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P25-LAN RTL8111E

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.02

Date: Tuesday, February 22, 2011 | Sheet 29 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

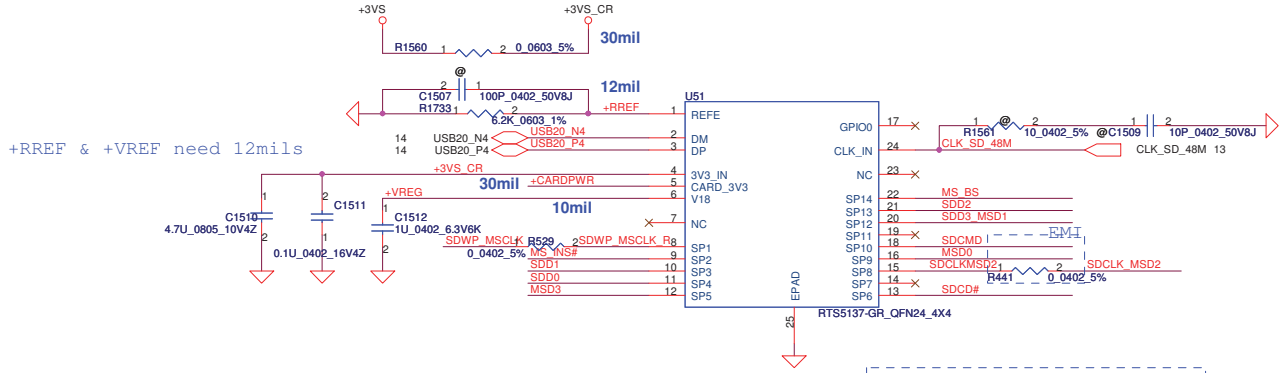
Compal Electronics, Inc.

Title: P26-HD CODEC ALC259

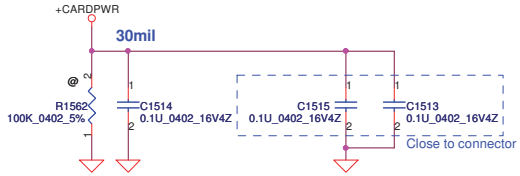
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

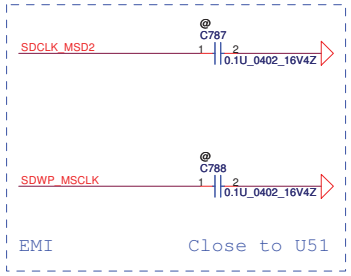
Date: Tuesday, February 22, 2011 | Sheet 30 of 49

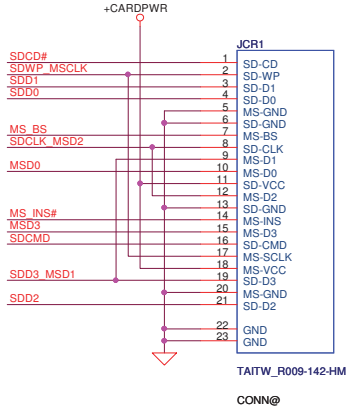
Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector







Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

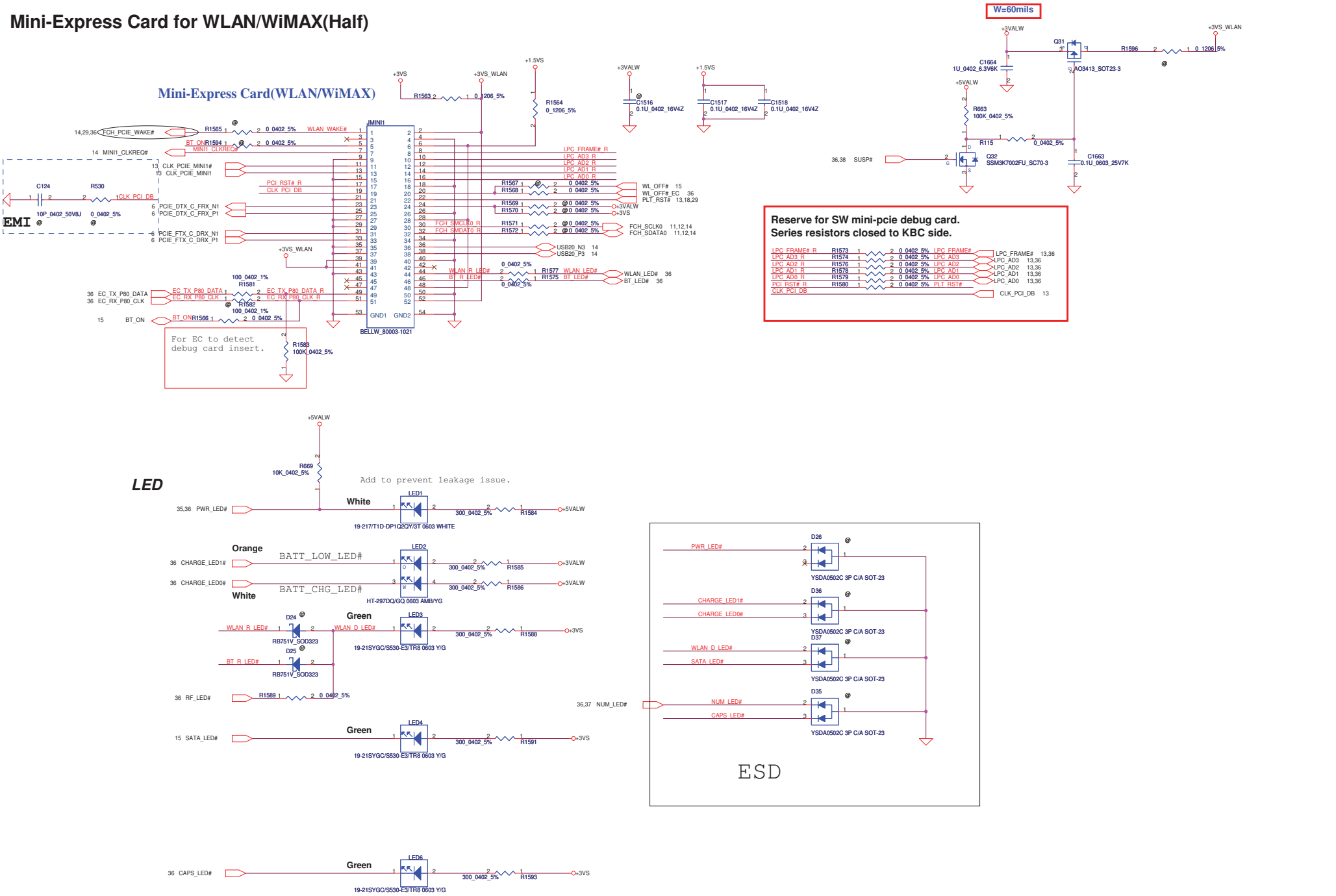
Compal Electronics, Inc.

Title: P27-RTS5137 Media Card Controller

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 31 of 49

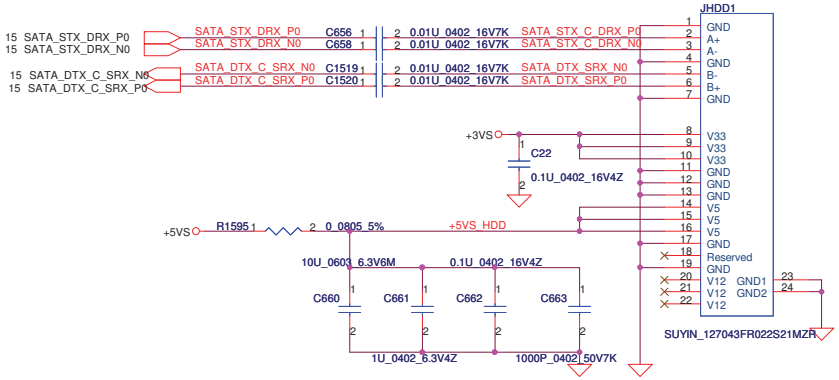
Mini-Express Card for WLAN/WiMAX(Half)



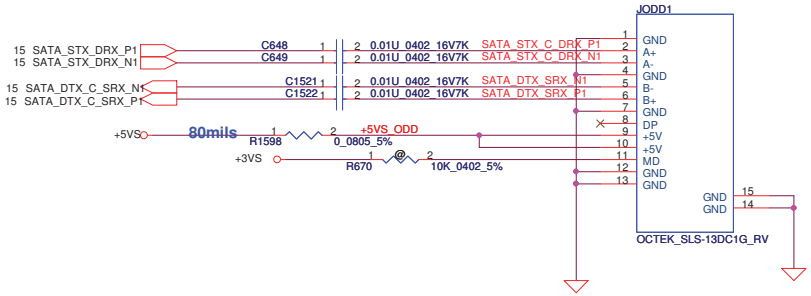
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.			
Title	P28-Mini PCIE/LED		
Size	Document Number		Rev
	QBL60 LA-7552P		0.03
Date: Tuesday, February 22, 2011	Sheet 32 of 49		

SATA HDD Conn.



SATA ODD FFC Conn.



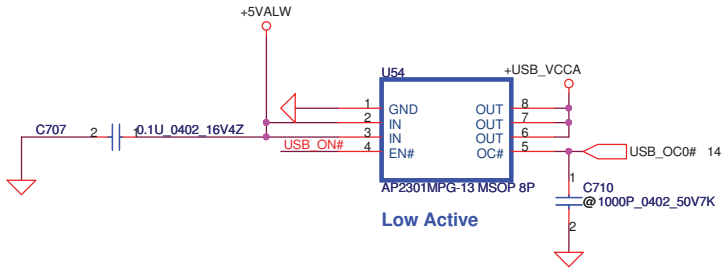
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

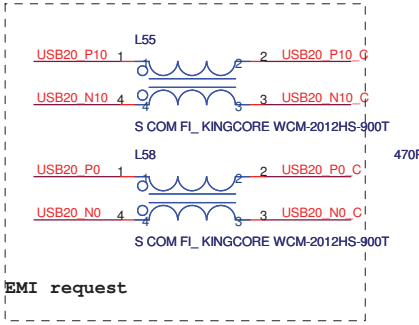
Compal Electronics, Inc.

Title: P29-HDD & ODD CONN

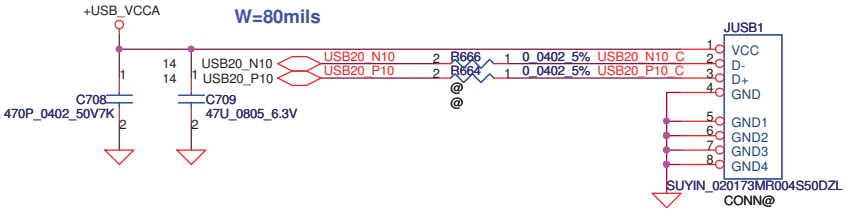
Size: B | Document Number: QBL60 LA-7552P | Rev: 0.03

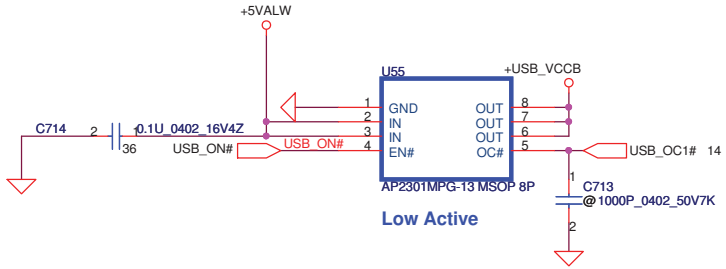
Date: Tuesday, February 22, 2011 | Sheet 33 of 49



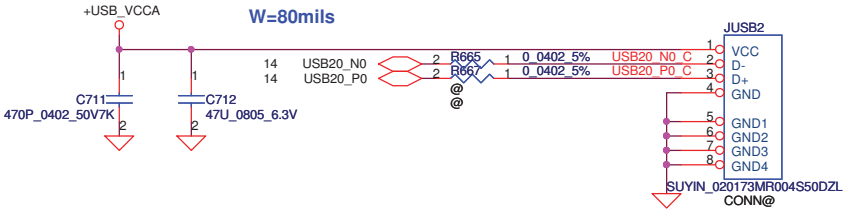


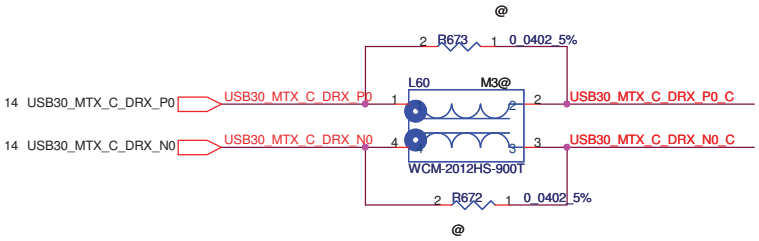
Left USB Conn.

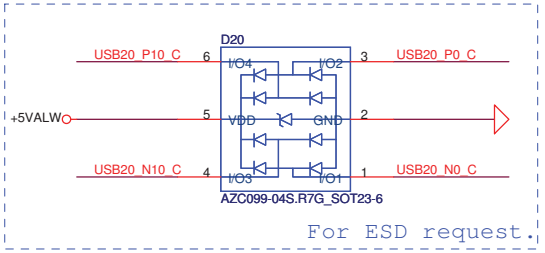


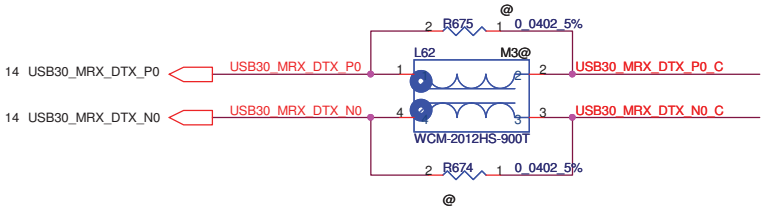


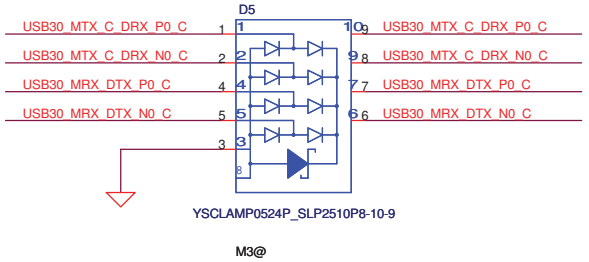
Left USB Conn.











Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

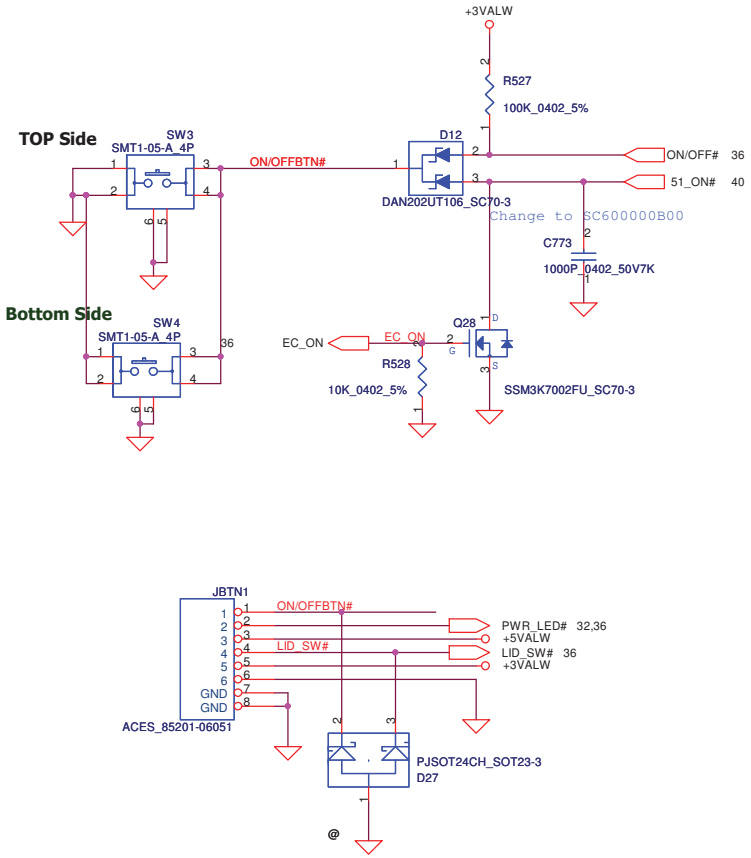
Compal Electronics, Inc.

Title: P32-USB/BT/USBsub

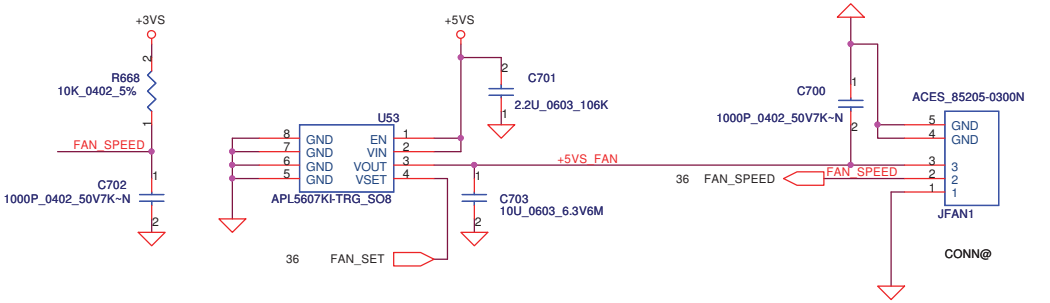
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 34 of 49

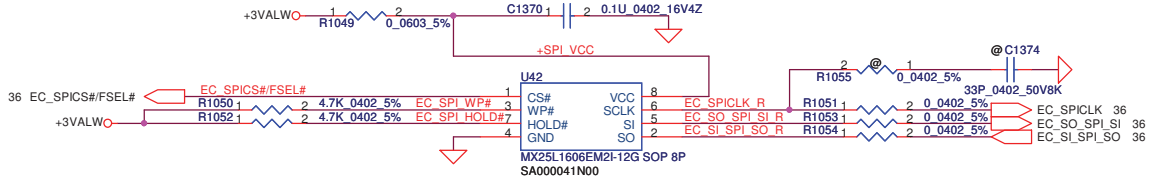
ON/OFF switch **Power Button**



Fan Control Circuit



EC BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size: B | Document Number: QBL60 LA-7552P | Rev: 0.03

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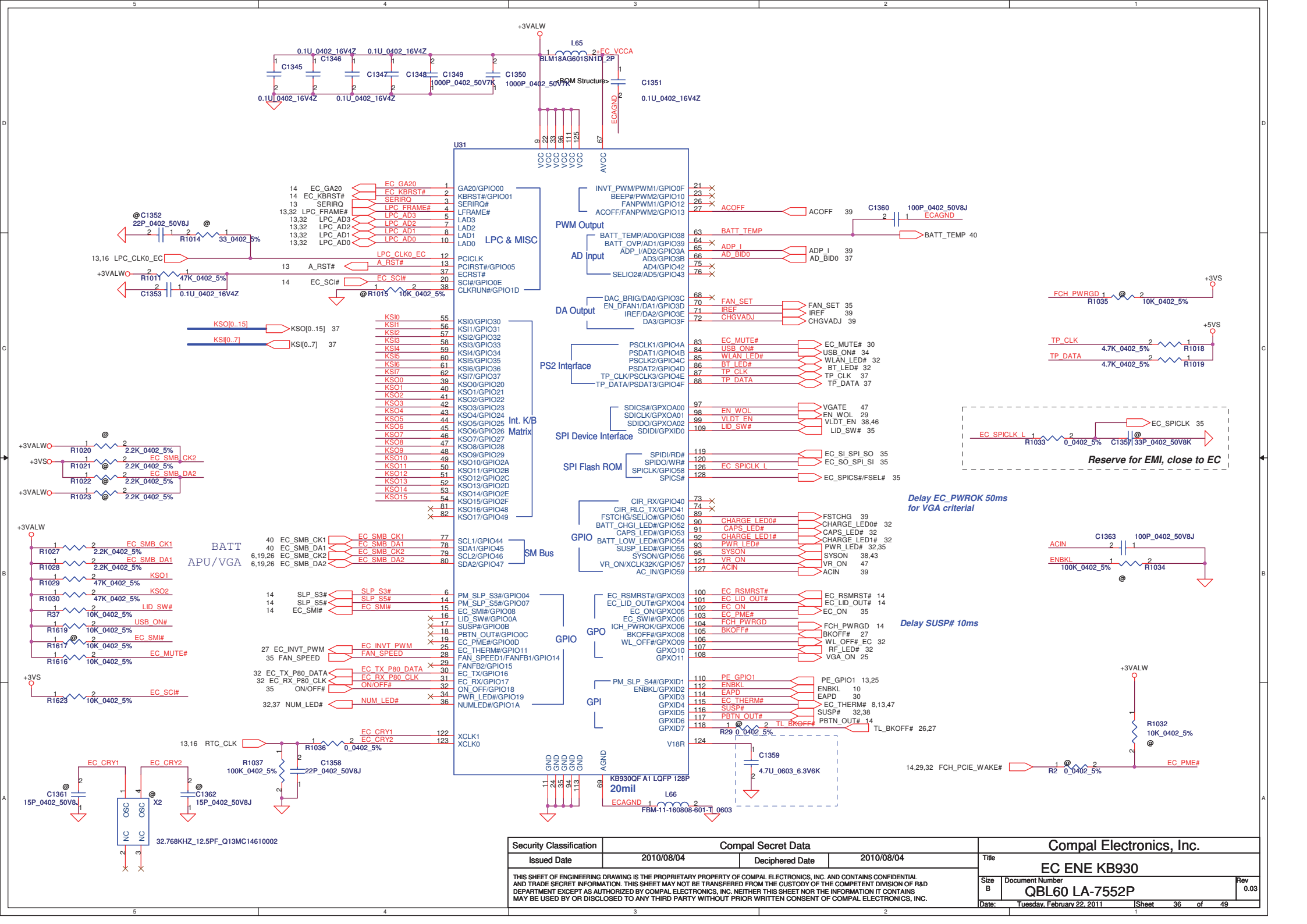


Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

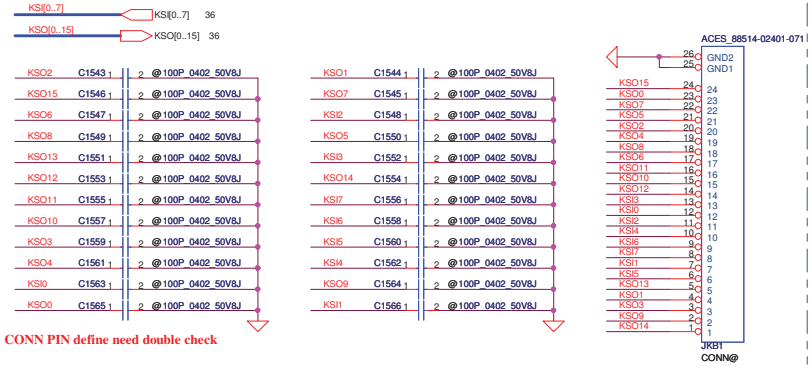
Compal Electronics, Inc.

Title: EC ENE KB930

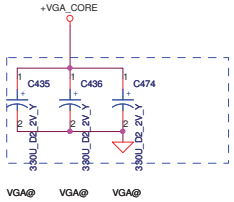
Size	Document Number	Rev
B	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 36 of 49

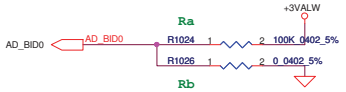
INT_KBD Conn.



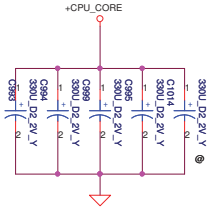
CONN PIN define need double check



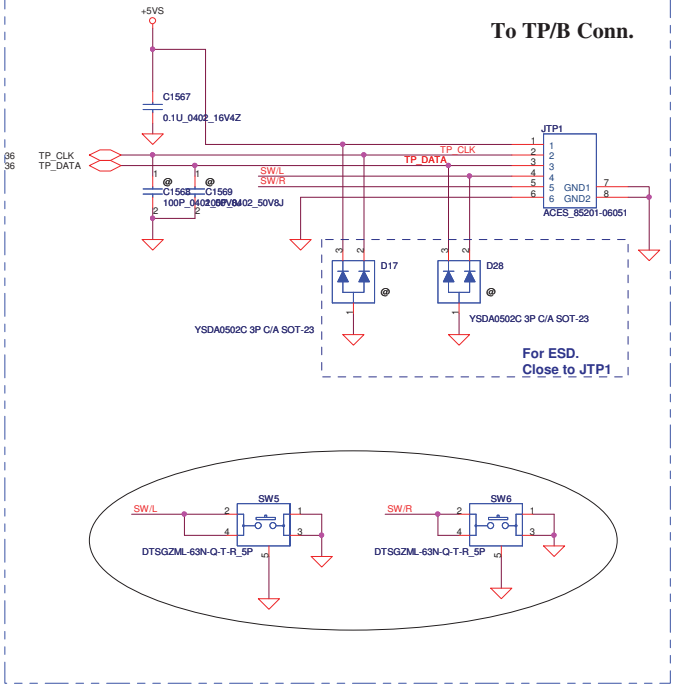
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V

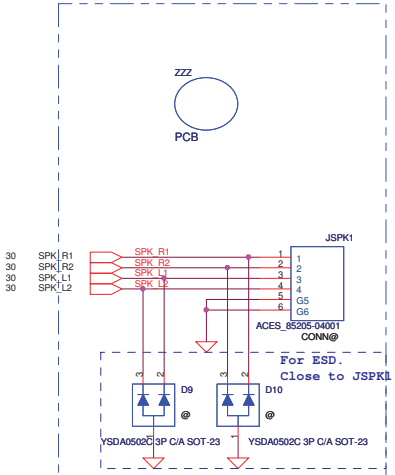


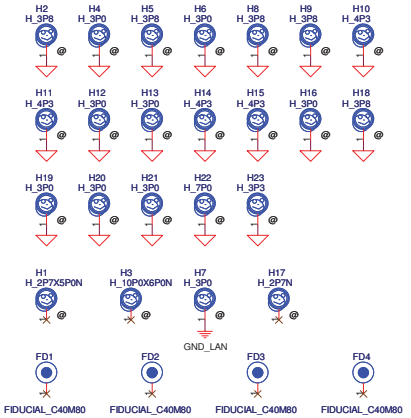
P9 FS1 PWR/GND

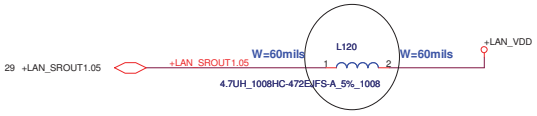


To TP/B Conn.

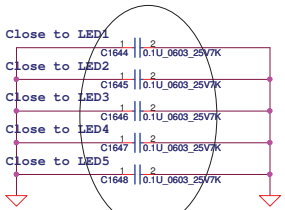








These components close to Pin 36
(Should be place within 200 mils)



For ESD.
Cap to LED gap is 1.2mm.

Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P33-Other IO/USB (right)

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 0.02

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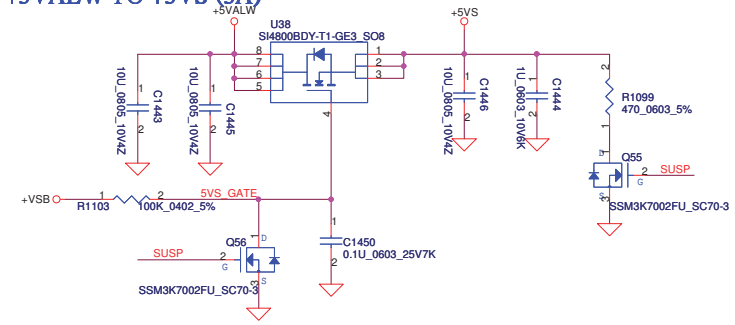
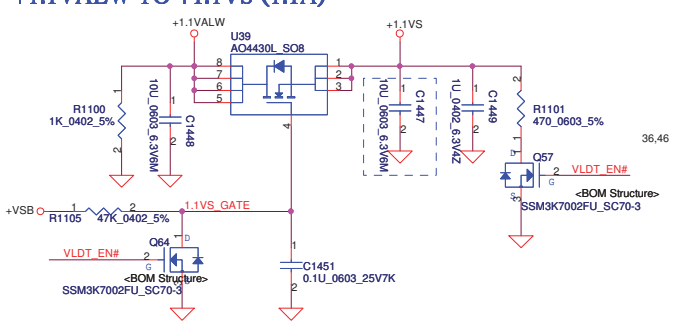
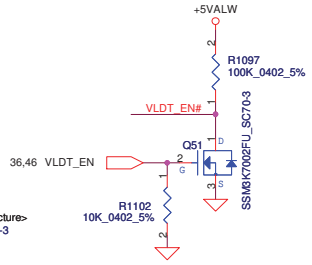
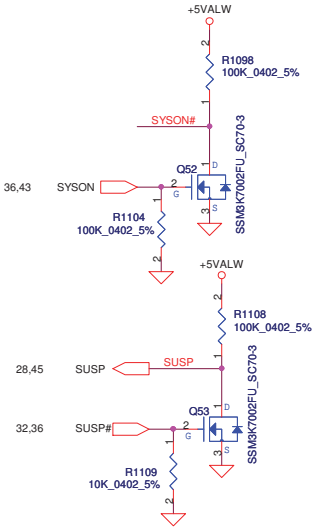
+5VALW TO +5VS (5A)



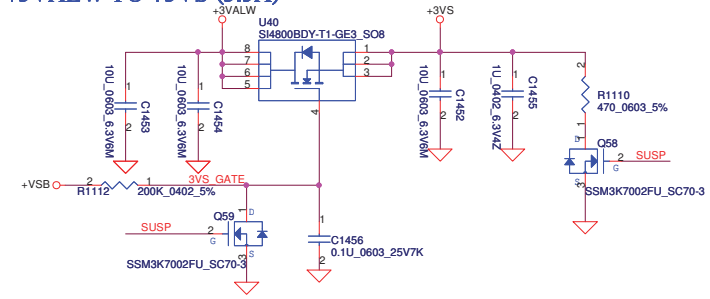
+1.1VALW TO +1.1VS (1.1A)



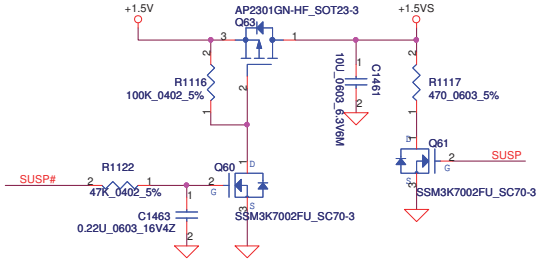




+3VALW TO +3VS (3.3A)

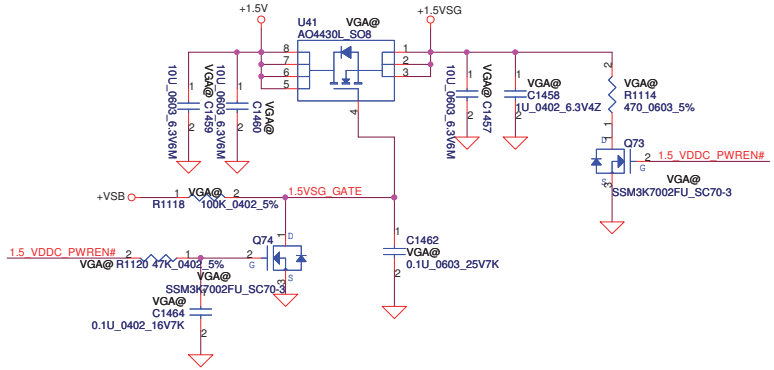


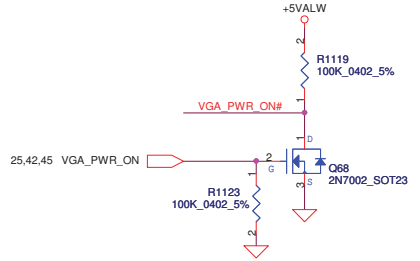
+1.5V TO +1.5VS (1.5A)



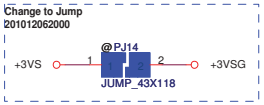
VGA Power

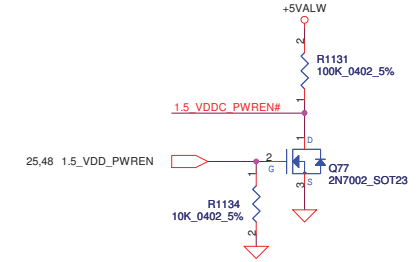
+1.5V to +1.5VSG (1.5A)

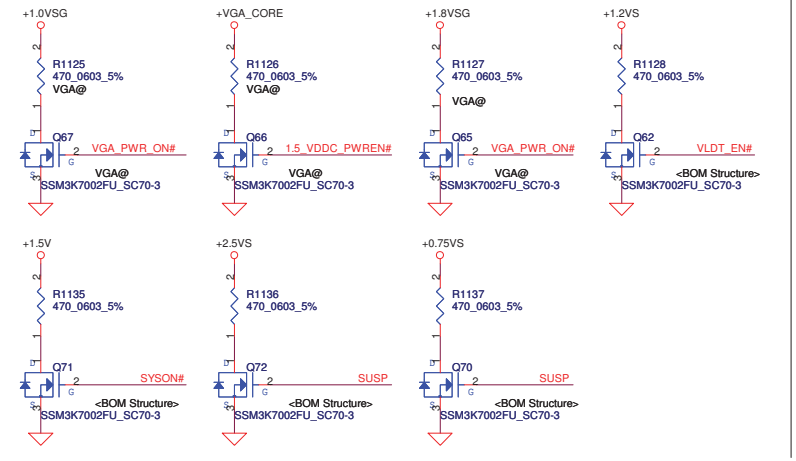




+3VS to +3VSG (3.3A)







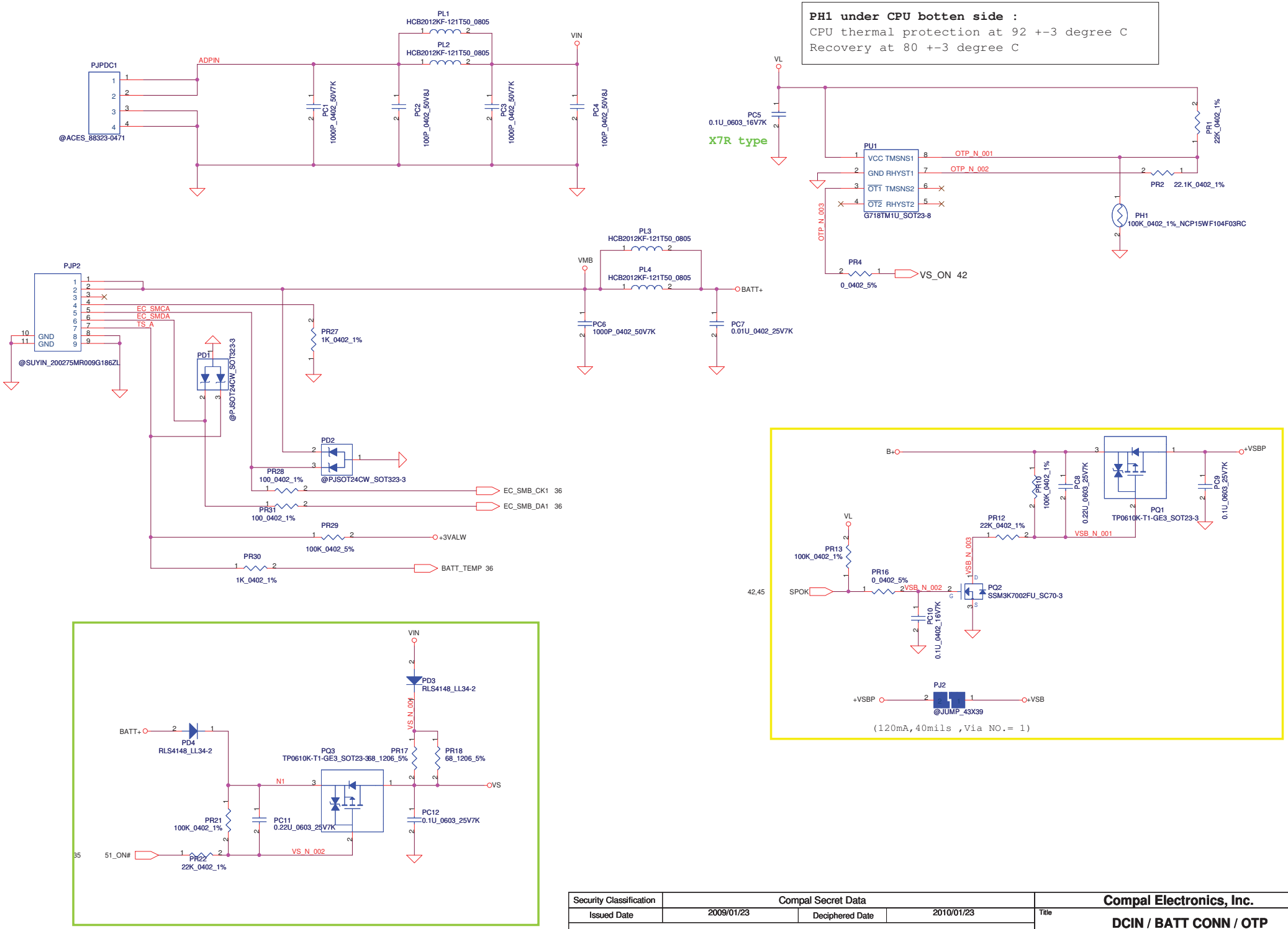
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 Sheet 38 of 49



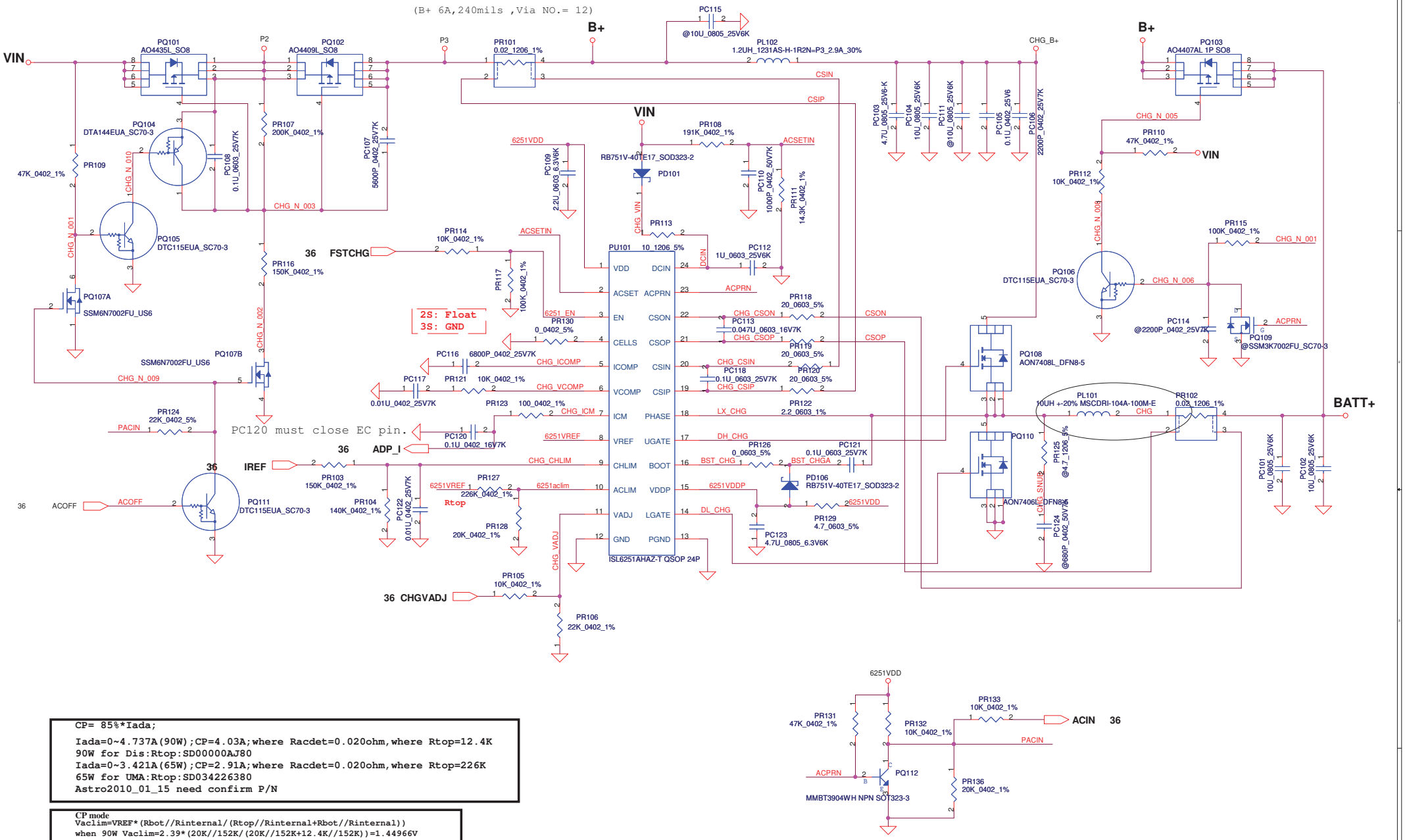
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Tuesday, February 22, 2011 | Sheet 40 of 44



CP= 85%*Iada;

Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

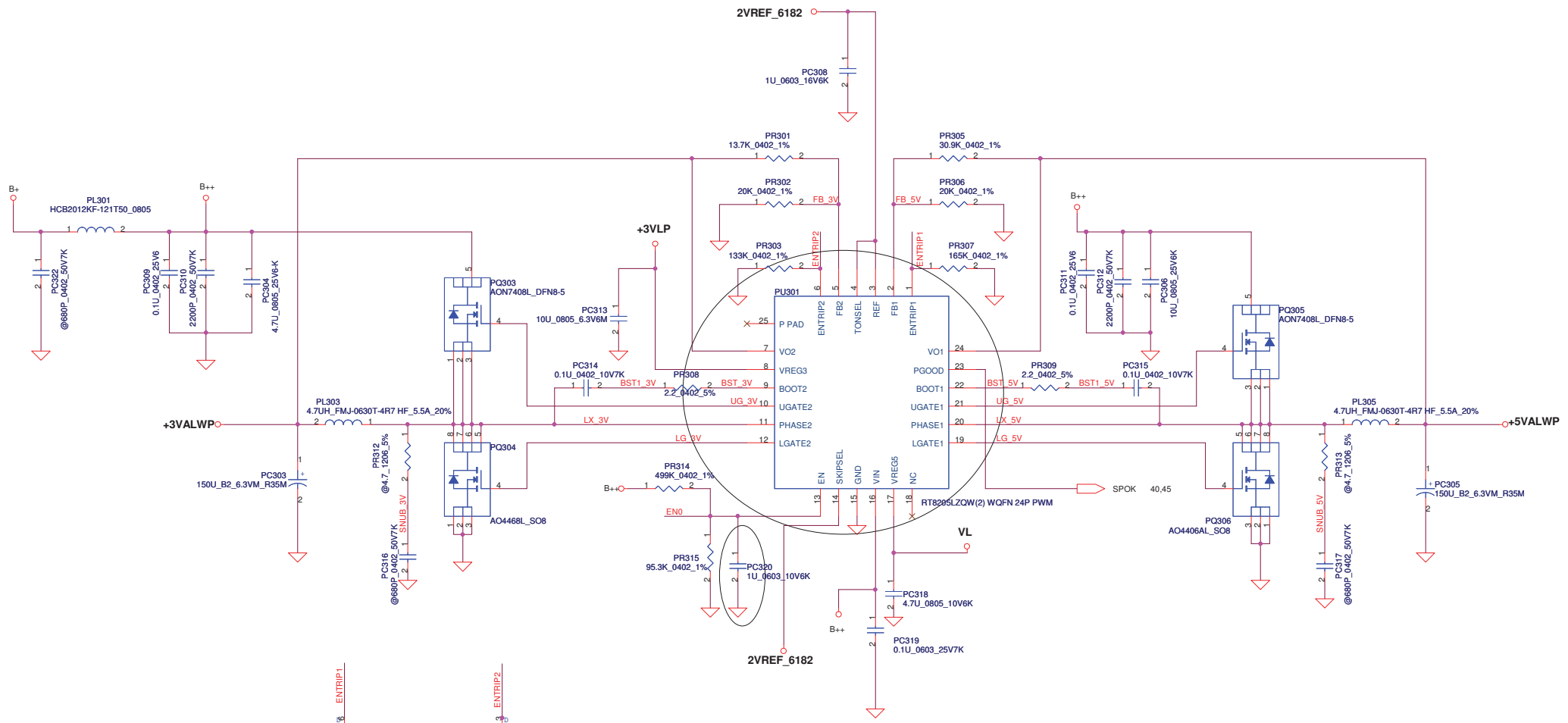
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: NCL61 LA-6321P M/B | Rev: 0.1

Date: Tuesday, February 22, 2011 | Sheet 41 of 44



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

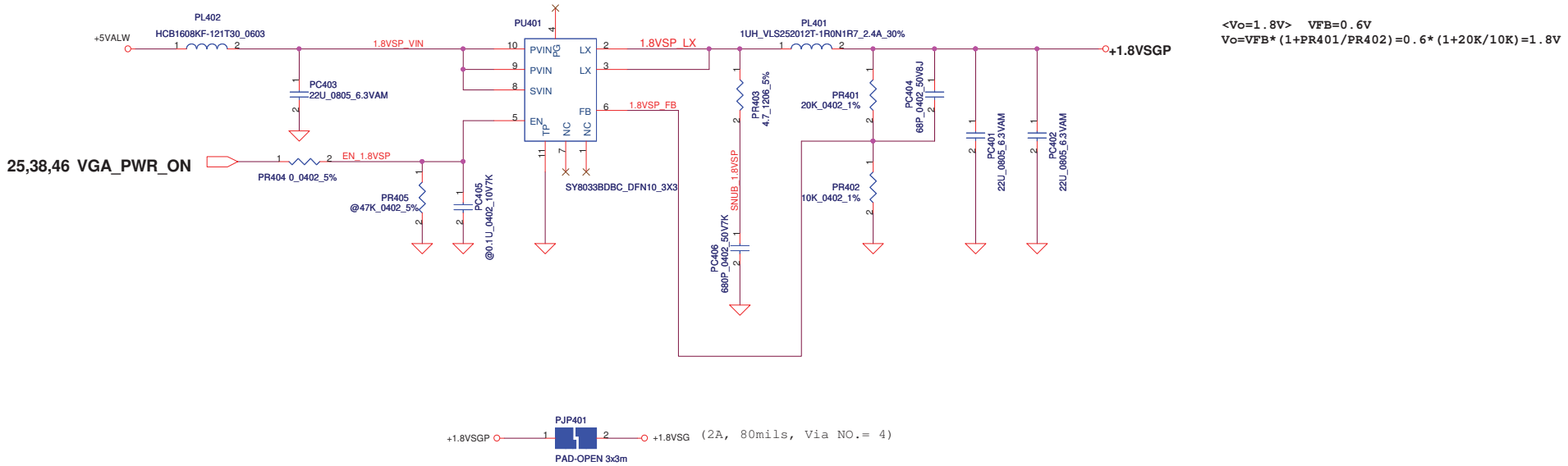
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: 3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	LAXXXX	0.1

Date: Tuesday, February 22, 2011 | Sheet 42 of 44



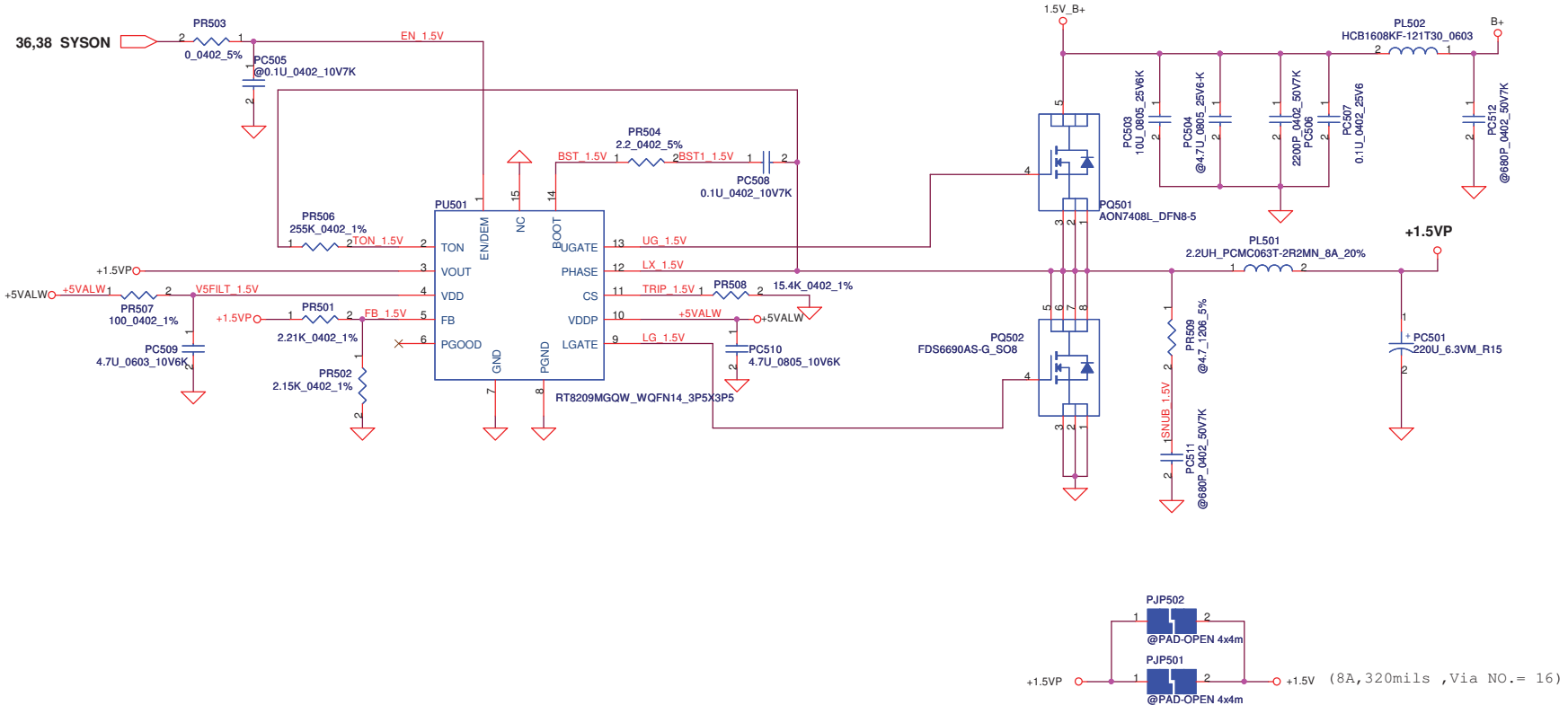
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.8VSGP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Tuesday, February 22, 2011 | Sheet 43 of 44



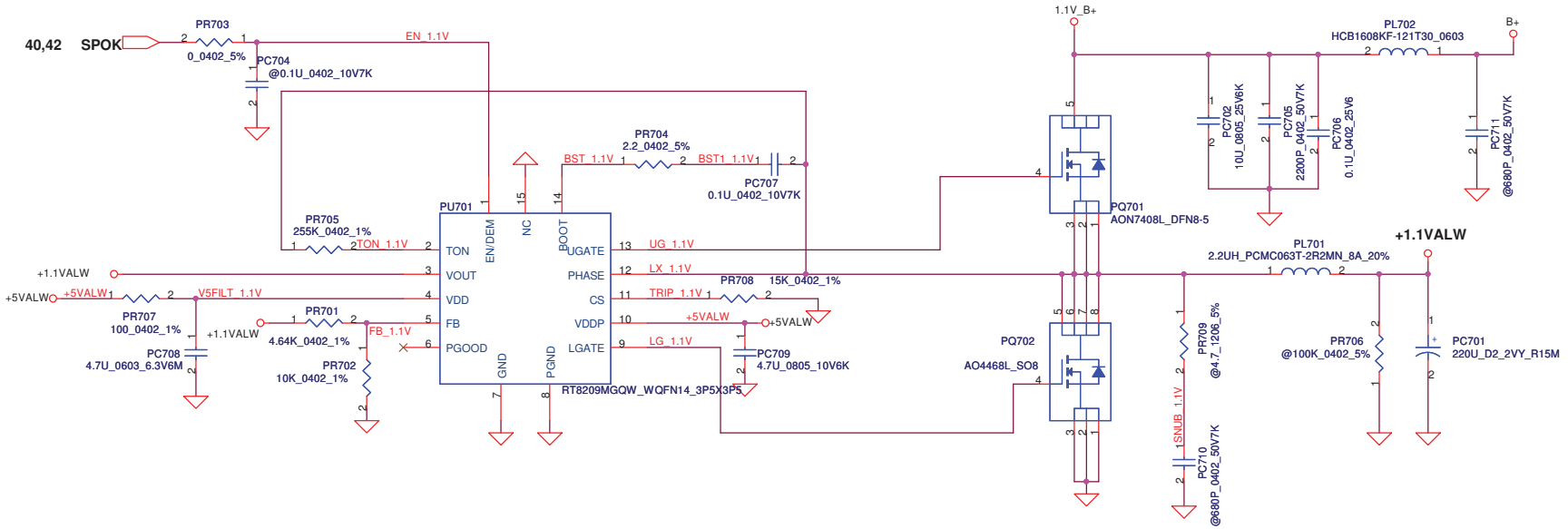
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	LAXXXX	0.1

Date: Tuesday, February 22, 2011 | Sheet 44 of 44



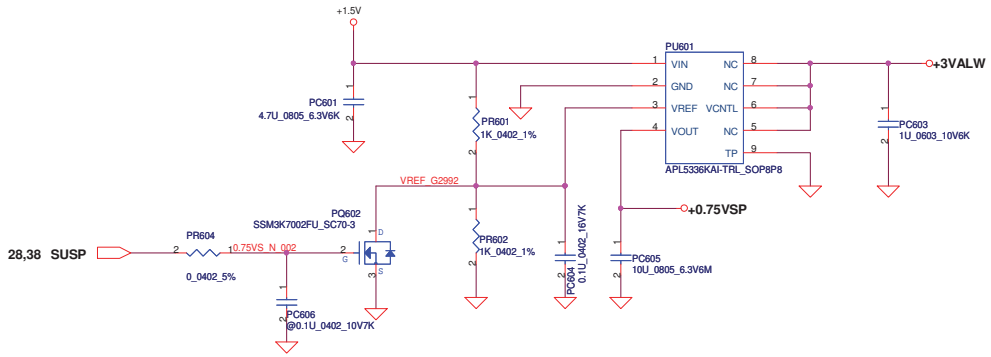
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

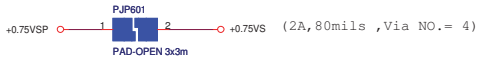
Compal Electronics, Inc.

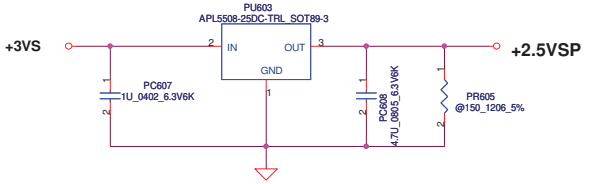
Title: PWR+1.1VALWP

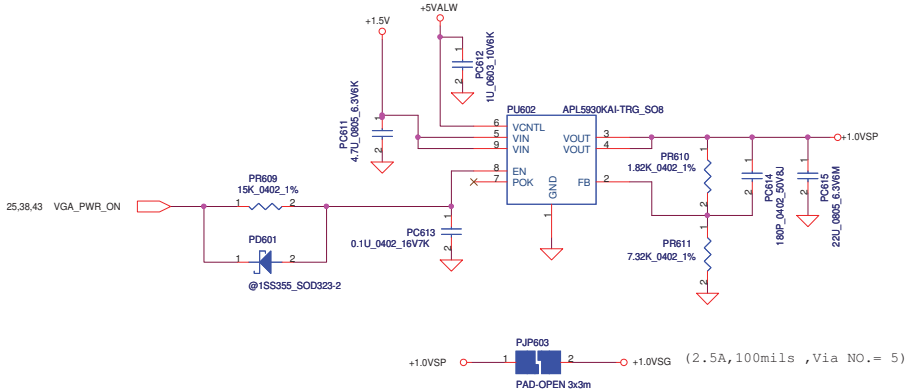
Size: Custom | Document Number: LAXXXX | Rev: 0.1

Date: Tuesday, February 22, 2011 | Sheet 45 of 44









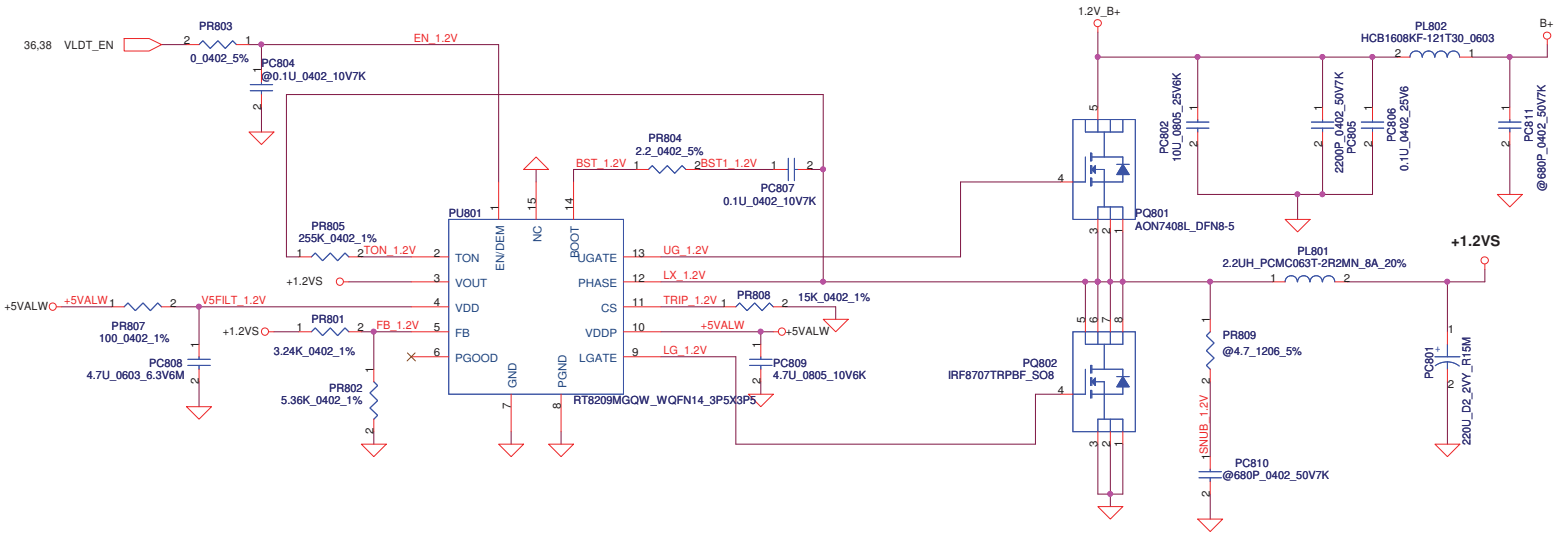
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **PWR 0.75VSP/1.0VSP/2.5VSP**

Size	Document Number	Rev
	LAXXXX	0.1

Date: Tuesday, February 22, 2011 | Sheet 46 of 44



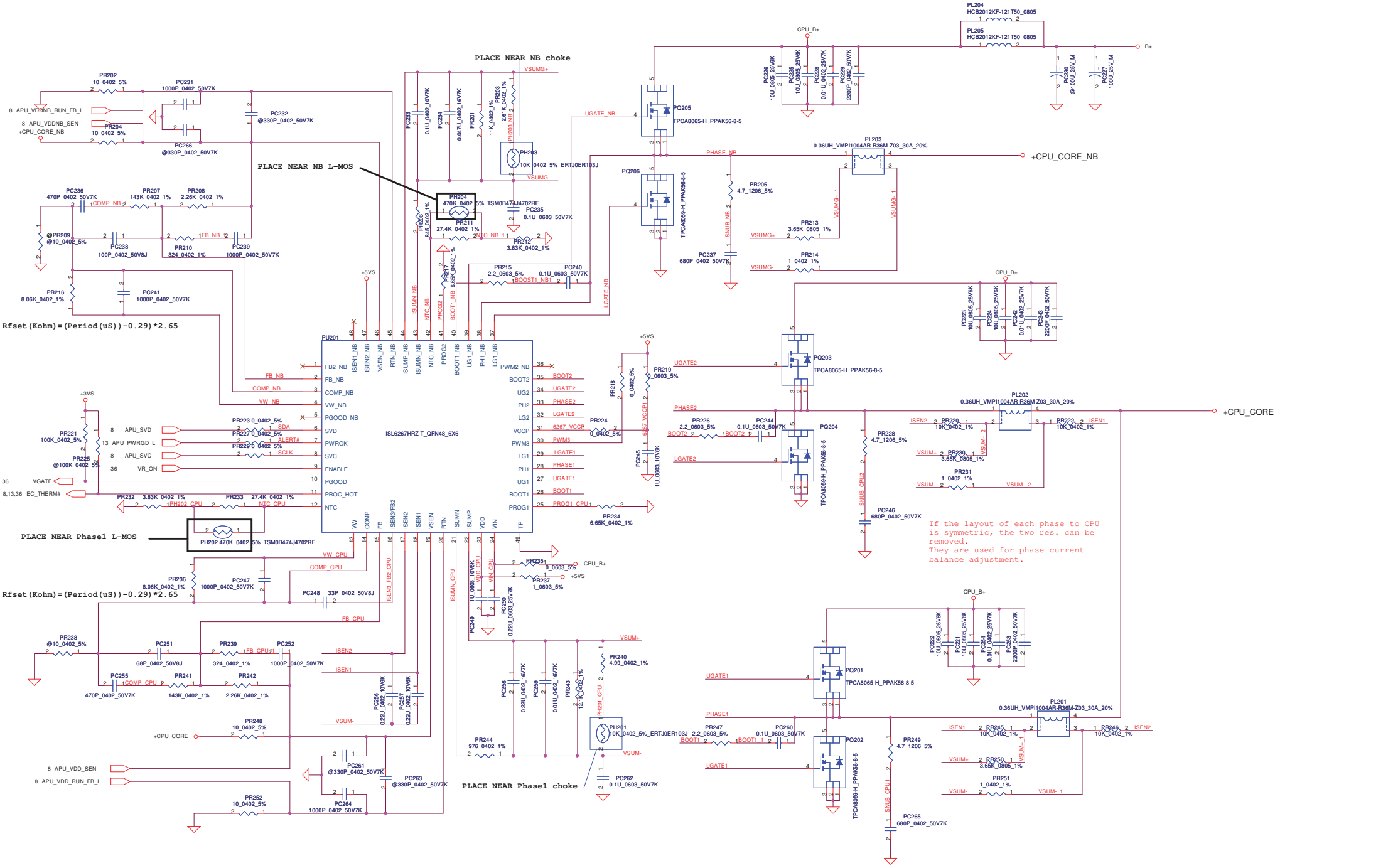
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.2VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

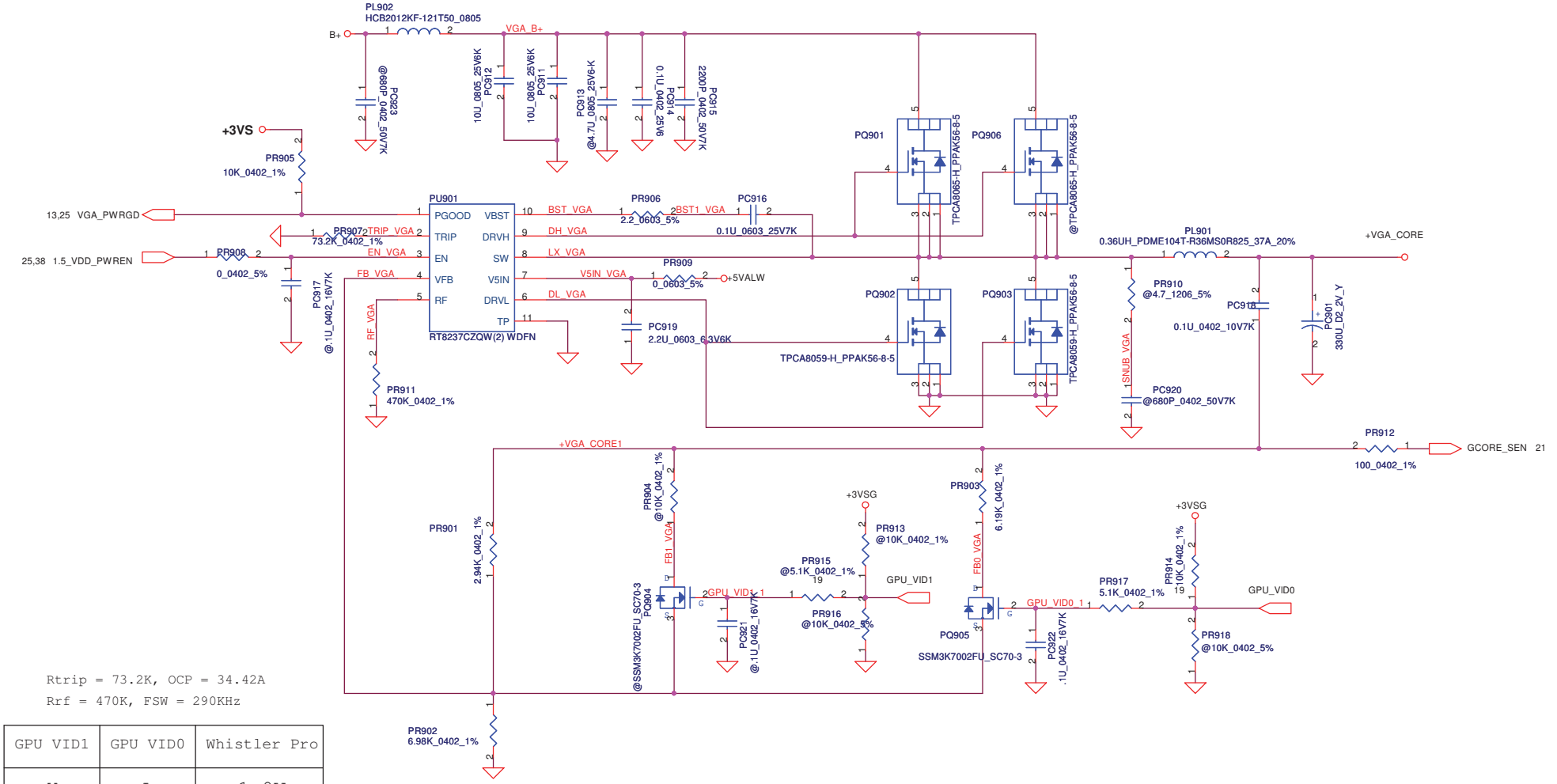
Date: Tuesday, February 22, 2011 | Sheet 47 of 44



Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/11/11

Compal Electronics, Inc.

Title	PWR_+CPU_CORE/+CPU_CORE_NB	
Size	Document Number: PEQAE LA-7291P M/B	Rev: 0.1
Date: Tuesday, February 22, 2011	Sheet 48 of 1	



Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: VGA_CORE

Size | Document Number: LAXXXX | Rev: 0.1

Date: Tuesday, February 22, 2011 | Sheet 49 of 44

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					