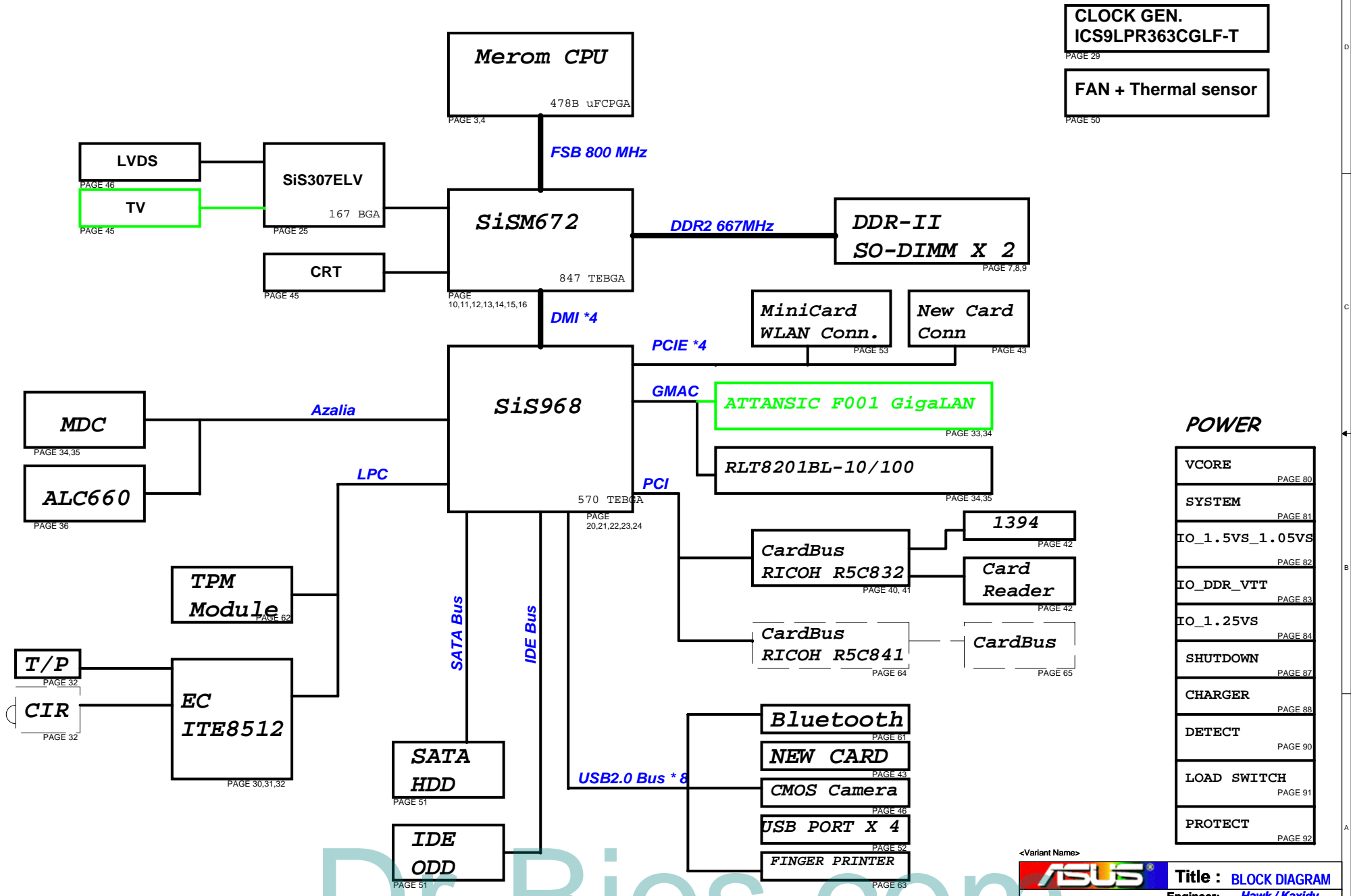


X51C Main BD. R1.0 BLOCK DIAGRAM



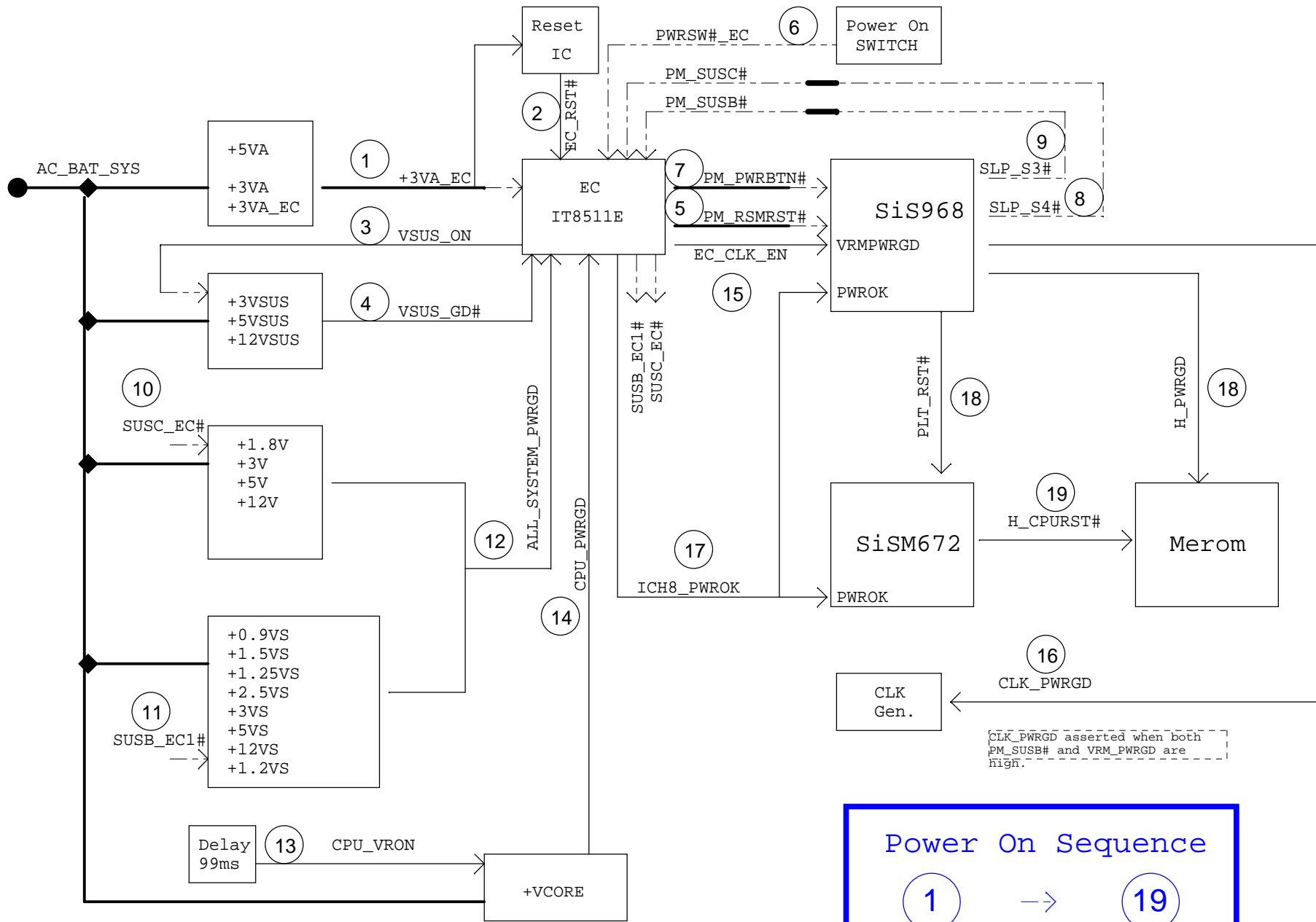
CLOCK GEN.
ICS9LPR363CGLF-T
PAGE 29

FAN + Thermal sensor
PAGE 50

POWER

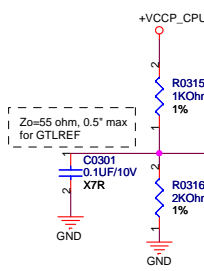
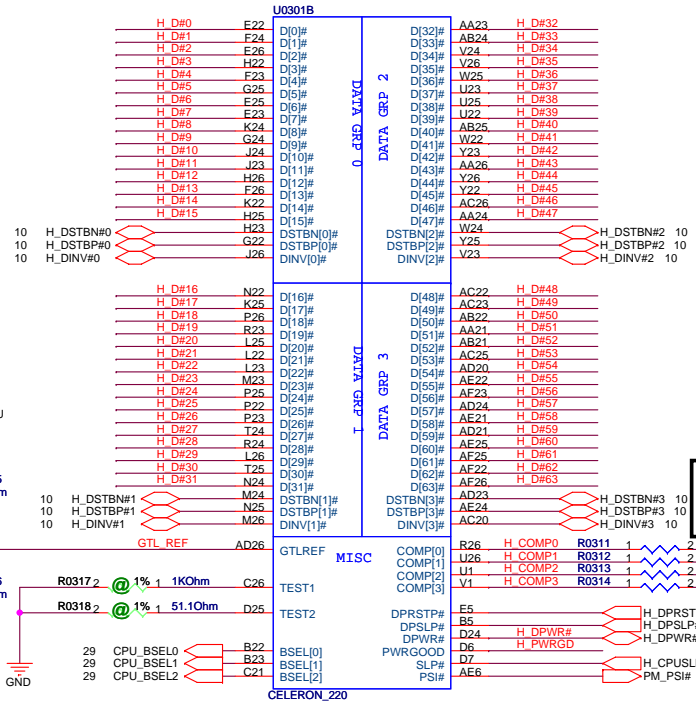
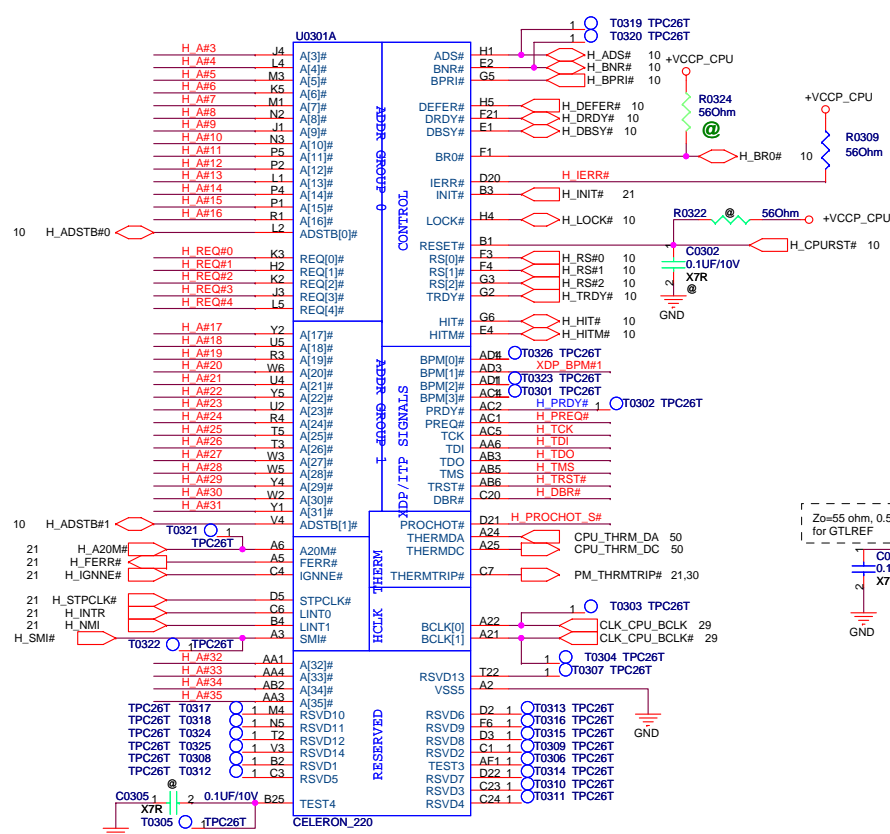
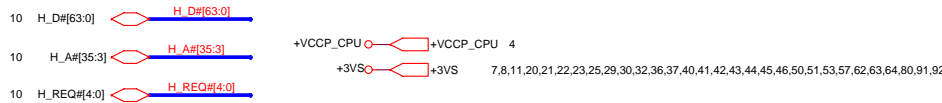
VCORE	PAGE 80
SYSTEM	PAGE 81
IO_1.5VS_1.05VS	PAGE 82
IO_DDR_VTT	PAGE 83
IO_1.25VS	PAGE 84
SHUTDOWN	PAGE 87
CHARGER	PAGE 88
DETECT	PAGE 90
LOAD SWITCH	PAGE 91
PROTECT	PAGE 92

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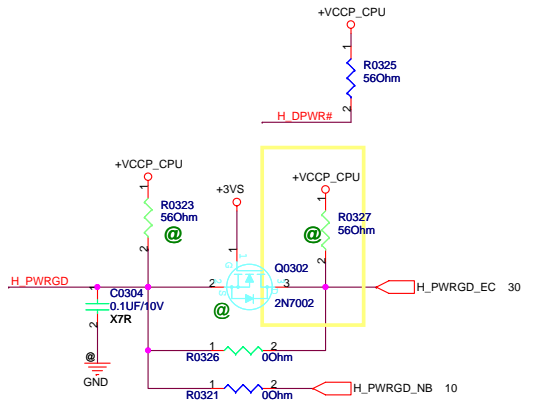
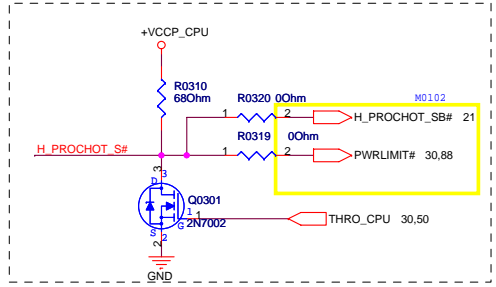
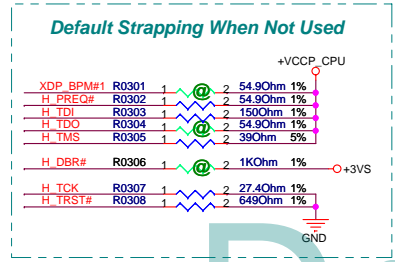


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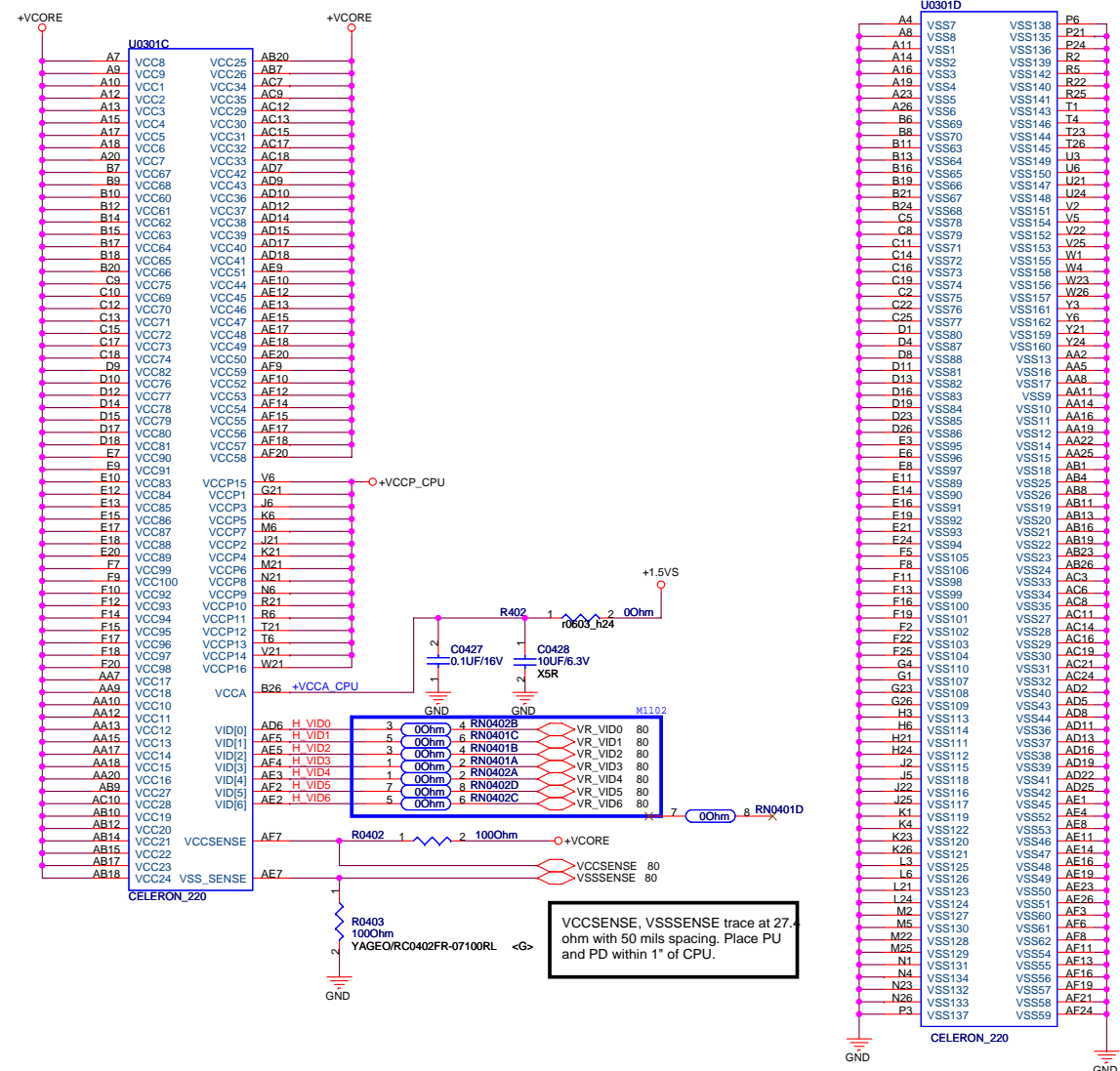
ASUS		Title : PowerOn sequence	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Monday, August 13, 2007	Sheet	2	of 94



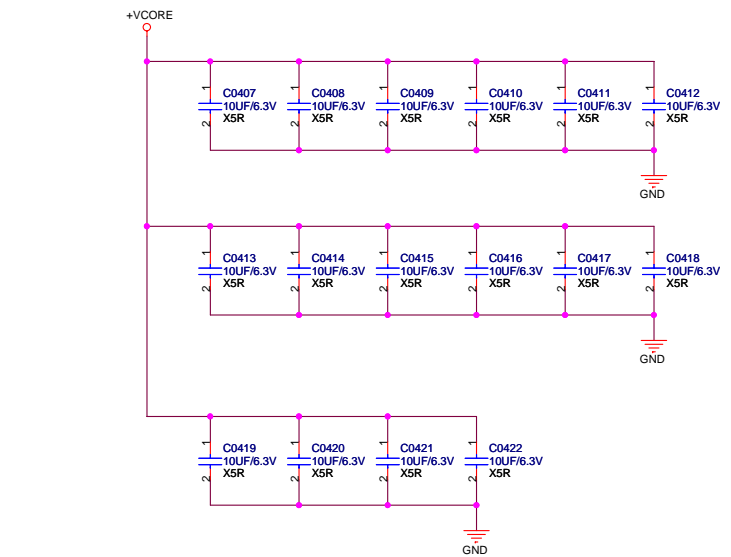
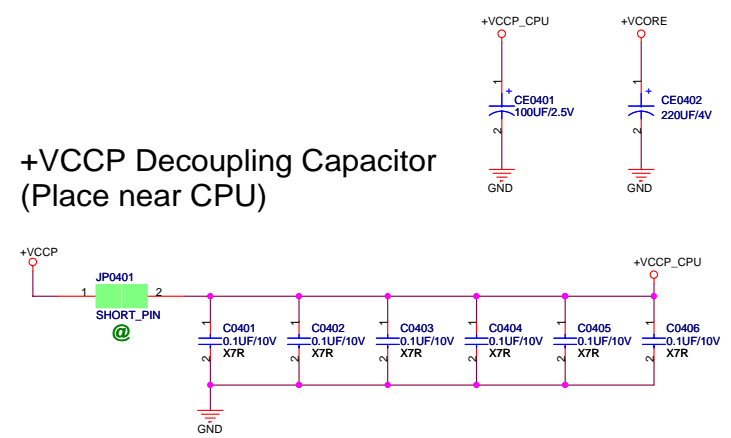
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5'.
 Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5'.



<Variant Name>
ASUS Title: MEROM CPU (1)
 ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy
 Size Project Name
 Custom T12C
 Date: Wednesday, February 27, 2008 Sheet 3 of 94
 Rev 1.1



+VCCP Decoupling Capacitor (Place near CPU)



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



<Variant Name>


		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	5 of 94

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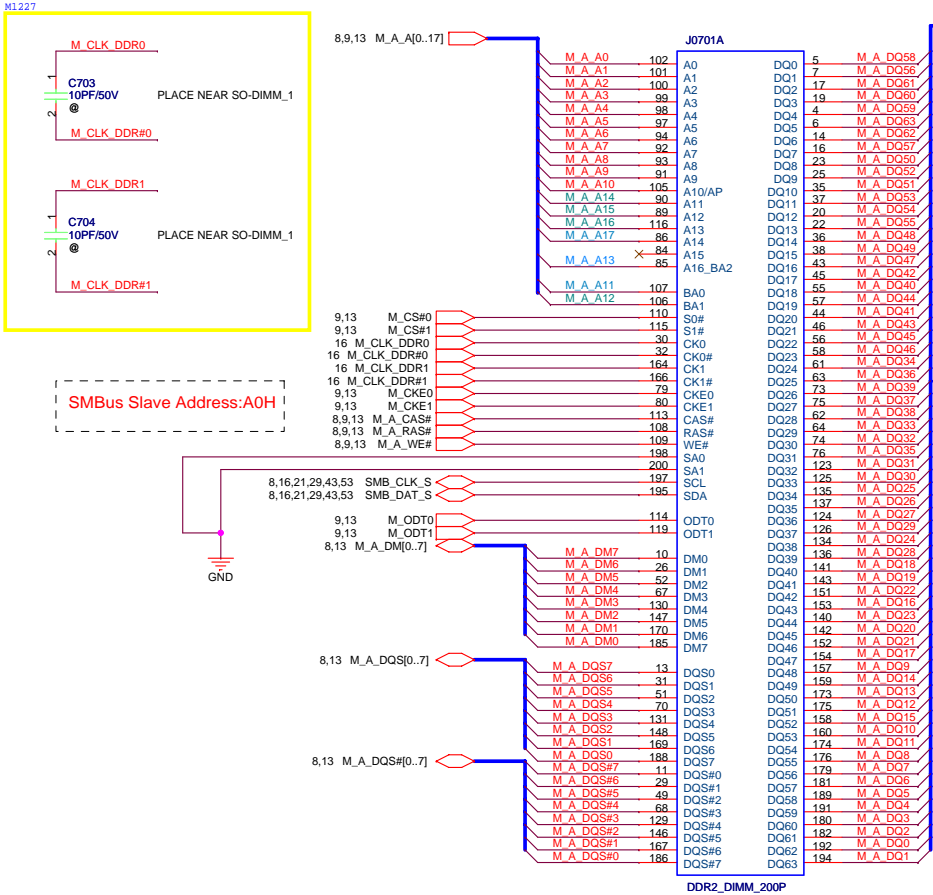


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<Variant Name>

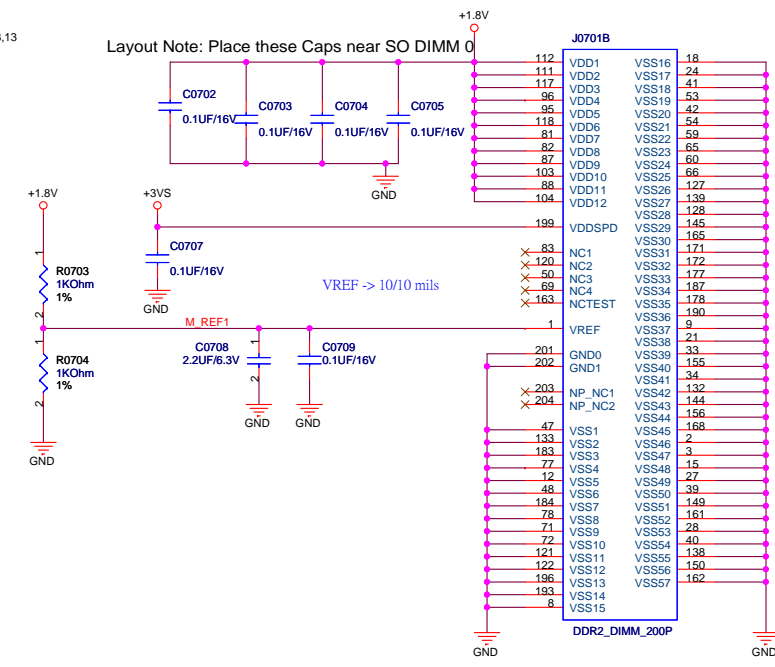
		Title : NULL
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 6 of 94

P/N: 12G025022004
(T12F) 4.0mm, STD

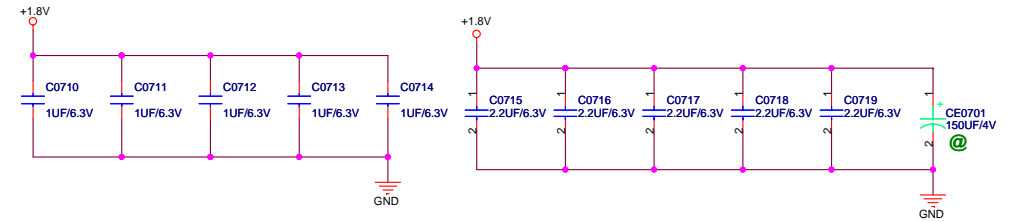


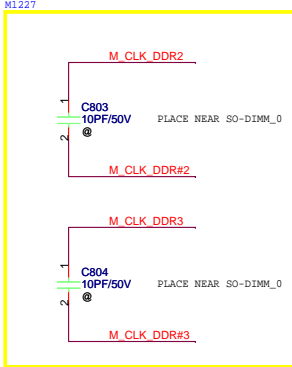
SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

Layout Note: Place these Caps near SO DIMM 0



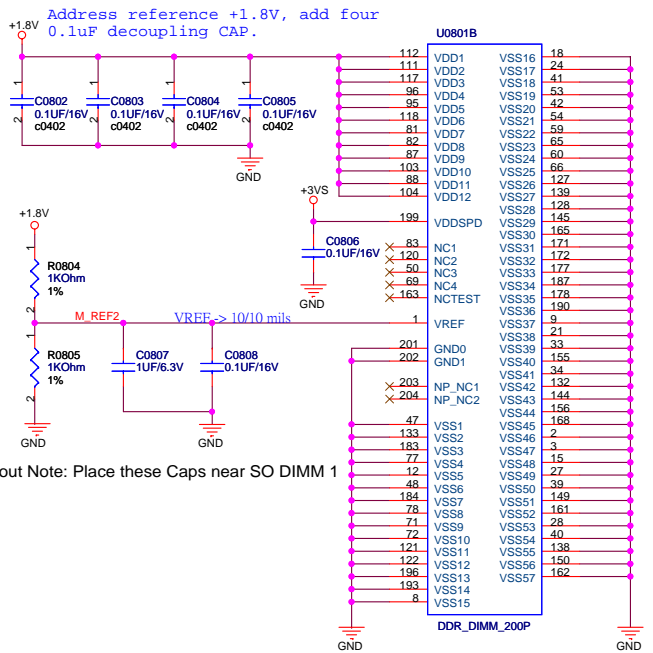
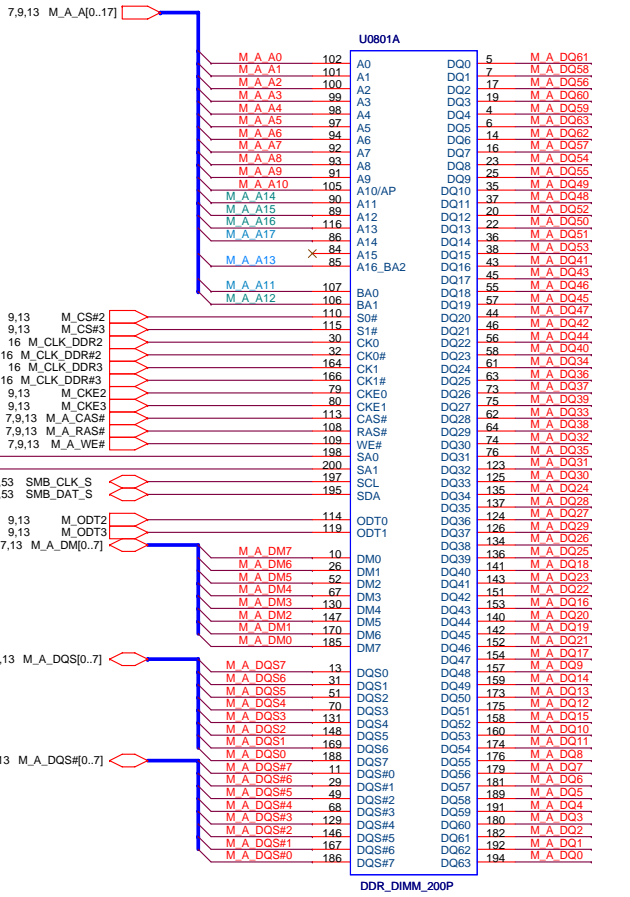
Layout Note: Place these Caps near SO DIMM 0





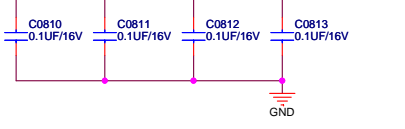
7,13 M_A_DQ[0..63] \leftrightarrow M_A DQ[0..63]

P/N: 12G025C22000 S:12G025C22004 (T12F) 9.2mm, STD

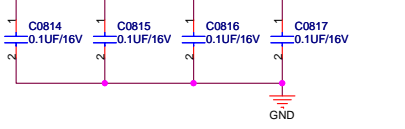


Layout Note: Place these Caps near SO DIMM 1

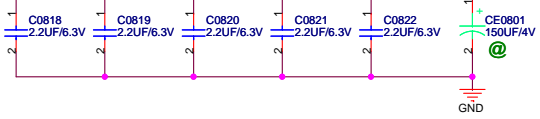
Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these CAPs near the SO DIMM1



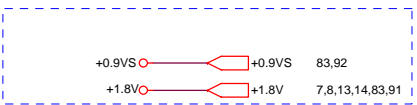
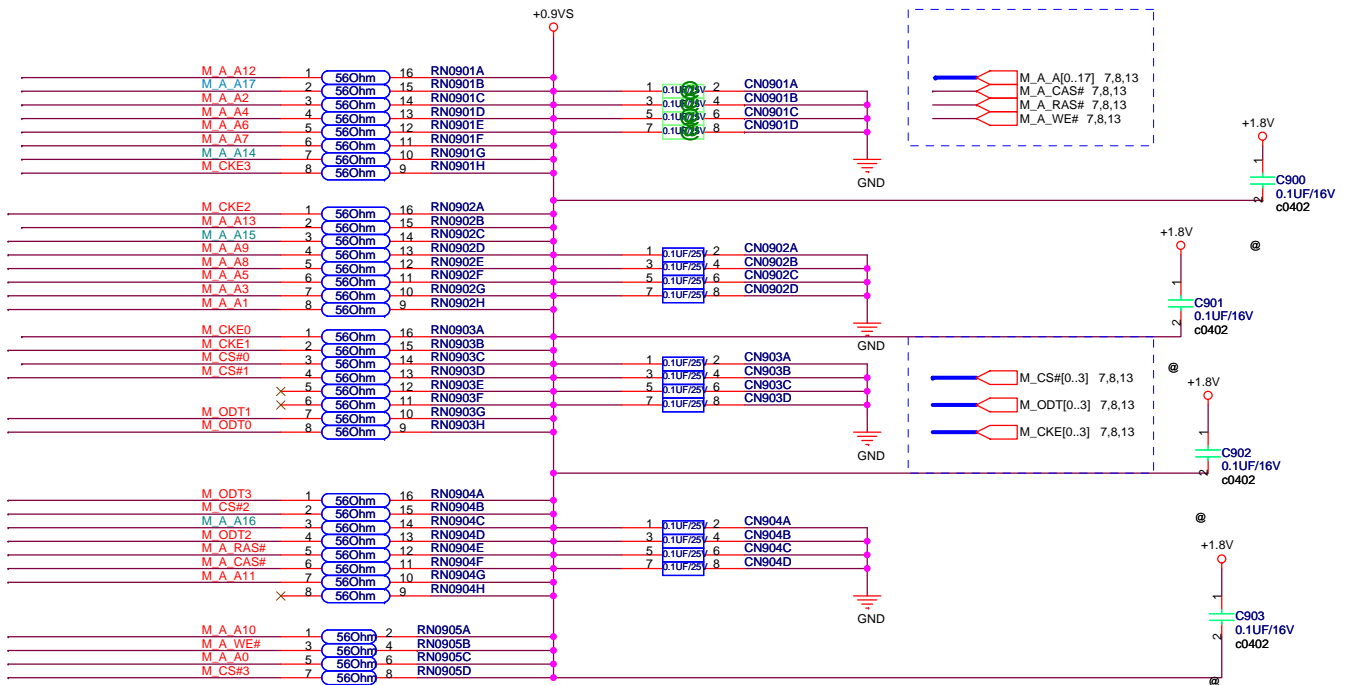
<Variant Name>

ASUS Title : **DDR2 SO-DIMM_1**

ASUSTeK COMPUTER INC Engineer: **Hawk / Kaxidy**

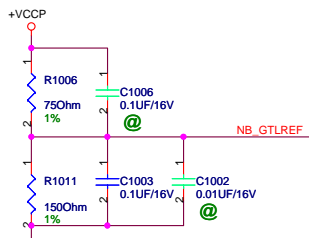
Size Project Name
 Custom **T12C** Rev 1.1

Date: **Wednesday, February 27, 2008** Sheet 8 of 94

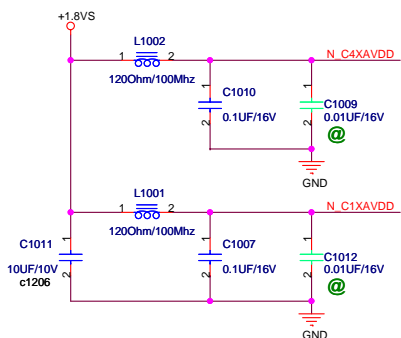
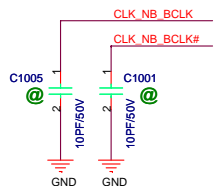


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

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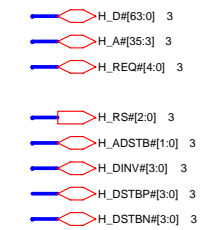
Layout Note:
0.1uF should be placed 100mils or less from NB pin.



Total Power mW (Max)		
1.8VS	N_C1XAVDD	10mA
	N_C4XAVDD	1.2mA

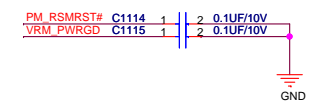
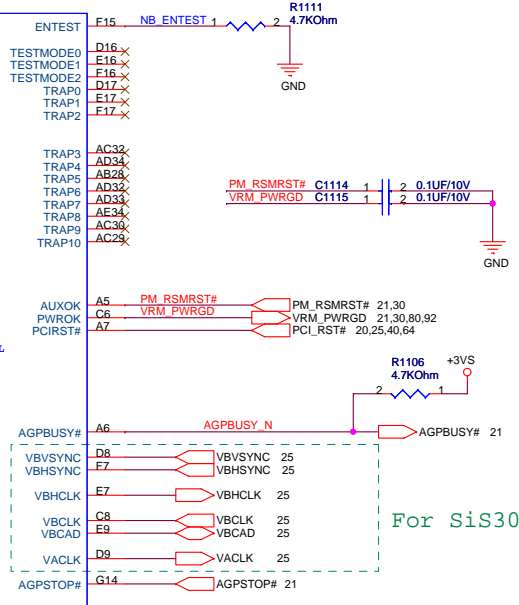
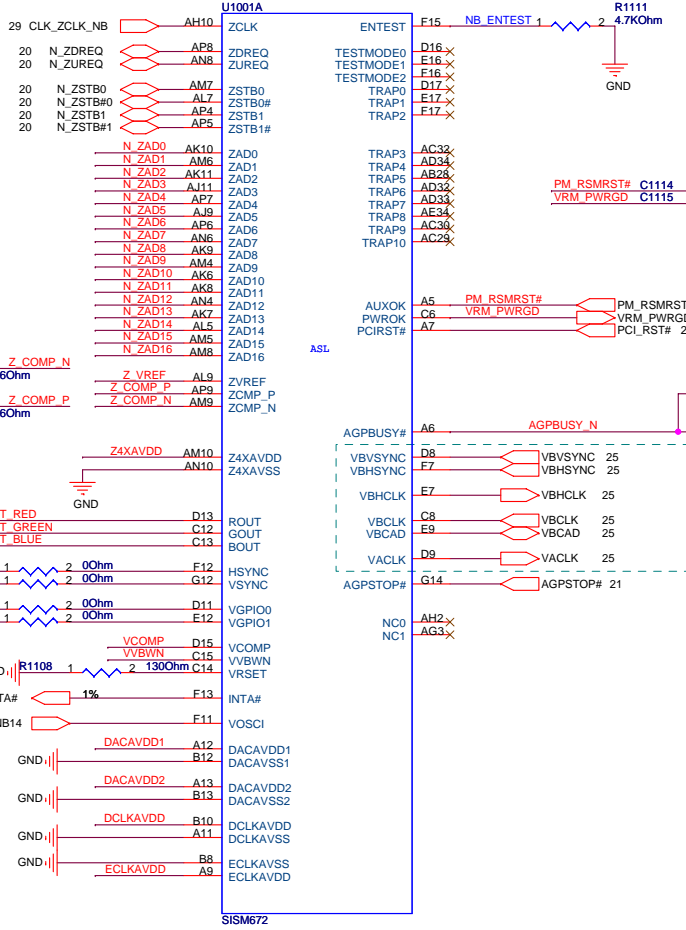
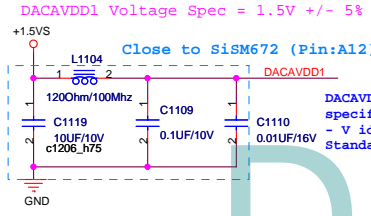
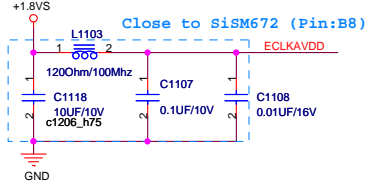
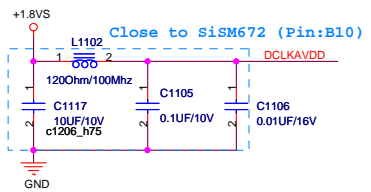
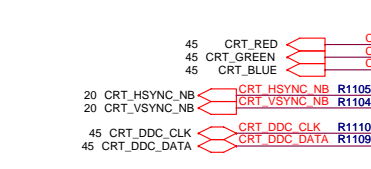
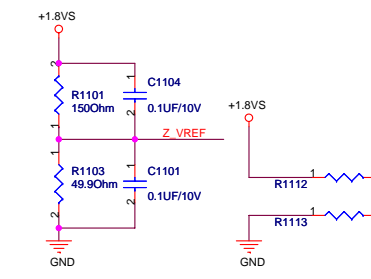
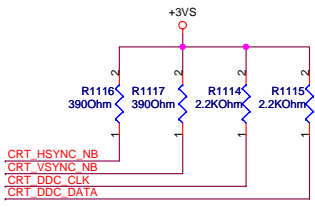
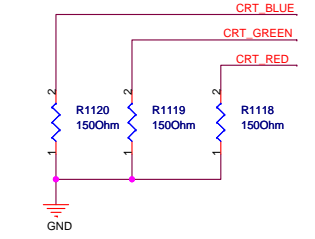
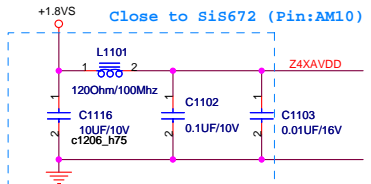
U1001C

C1XAVDD	B16	H0#	H D#0
C1XAVSS	C17	HD1#	M30 H D#1
C4XAVDD	A17	HD2#	M28 H D#2
C4XAVSS	B18	HD3#	L30 H D#3
HVREF1	W24	HD4#	L29 H D#4
HVREF2	U24	HD5#	K28 H D#5
HVREF3	R24	HD6#	K31 H D#6
HVREF4	N24	HD7#	K30 H D#7
HVREF5	L21	HD8#	H31 H D#8
PCREQ#	R34	HD9#	G34 H D#9
EDRDY#	P32	HD10#	H32 H D#10
NC2	E21	HD11#	G32 H D#11
CPUCLK	F18	HD12#	K32 H D#12
CPUCLK#	G18	HD13#	F34 H D#13
HLOCK#	L32	HD14#	F32 H D#14
DEFER#	P31	HD15#	H28 H D#15
HTRDY#	F21	HD16#	H28 H D#16
CPURST#	P28	HD17#	J30 H D#17
CPUPWRGD	N30	HD18#	G29 H D#18
BPR#	P33	HD19#	J29 H D#19
BREQ#	K34	HD20#	G29 H D#19
RS0#	M31	HD21#	G30 H D#20
RS1#	K33	HD22#	F30 H D#21
RS2#	M34	HD23#	D33 H D#22
ADS#	N34	HD24#	D33 H D#22
HITM#	N32	HD25#	B32 H D#23
HIT#	M33	HD26#	B32 H D#23
DRDY#	L34	HD27#	C34 H D#24
DBSY#	M32	HD28#	D31 H D#25
BNR#	M32	HD29#	A31 H D#26
H REQ#0	T34	HD30#	A32 H D#27
H REQ#1	R30	HD31#	C31 H D#28
H REQ#2	R29	HD32#	B30 H D#29
H REQ#3	R32	HD33#	C30 H D#30
H REQ#4	P34	HD34#	A30 H D#31
H ADSTB#0	U34	HD35#	D28 H D#32
H ADSTB#1	AA34	HD36#	D28 H D#32
H A#3	T32	HD37#	G29 H D#33
H A#4	T28	HD38#	E28 H D#34
H A#5	T31	HD39#	E27 H D#35
H A#6	T33	HD40#	C27 H D#36
H A#7	T30	HD41#	G26 H D#37
H A#8	U32	HD42#	E26 H D#38
H A#9	U30	HD43#	D26 H D#39
H A#10	V34	HD44#	B26 H D#40
H A#11	U29	HD45#	A26 H D#41
H A#12	V33	HD46#	A26 H D#41
H A#13	V32	HD47#	C26 H D#42
H A#14	V28	HD48#	C26 H D#42
H A#15	V31	HD49#	G22 H D#43
H A#16	W34	HD50#	E23 H D#44
H A#17	Y33	HD51#	E25 H D#45
H A#18	W32	HD52#	E25 H D#45
H A#19	W30	HD53#	G24 H D#46
H A#20	W30	HD54#	D22 H D#47
H A#21	Y34	HD55#	C22 H D#48
H A#22	Y28	HD56#	E22 H D#49
H A#23	W29	HD57#	C23 H D#50
H A#24	Y32	HD58#	B24 H D#51
H A#25	Y30	HD59#	A24 H D#52
H A#26	Y31	HD60#	E23 H D#53
H A#27	AA32	HD61#	E23 H D#53
H A#28	AA30	HD62#	A23 H D#54
H A#29	AA29	HD63#	A22 H D#55
H A#30	AB33		B22 H D#56
H A#31	AB34		
H A#32	AB32		
H A#33	AC34		
H A#34	AB30		
H A#35	AB31		



N_ZAD[16:0] 20

+1.8VS +1.8VS 10,13,14,16,20,21,22,23,25,91
 +3VS +3VS 3,7,8,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,
 +1.5VS +1.5VS 4,43,53,57,83



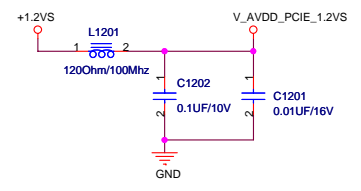
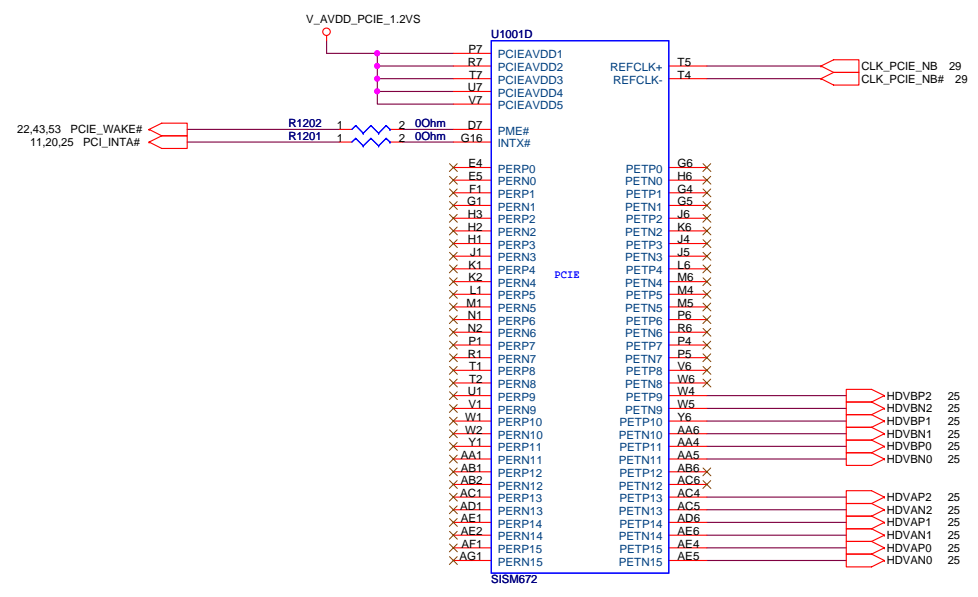
For SiS307 Only

Total Power mW(Max)		
1.8VS	Z4XAVDD	10mA
1.8VS	DCLKAVDD	5mA
1.8VS	ECLKAVDD	5mA
1.5VS	DACA VDD1	73mA
1.8VS	DACA VDD2	73mA

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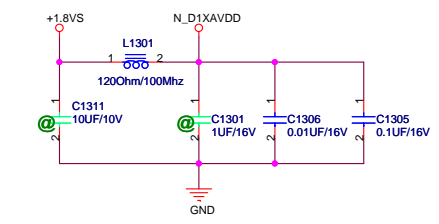
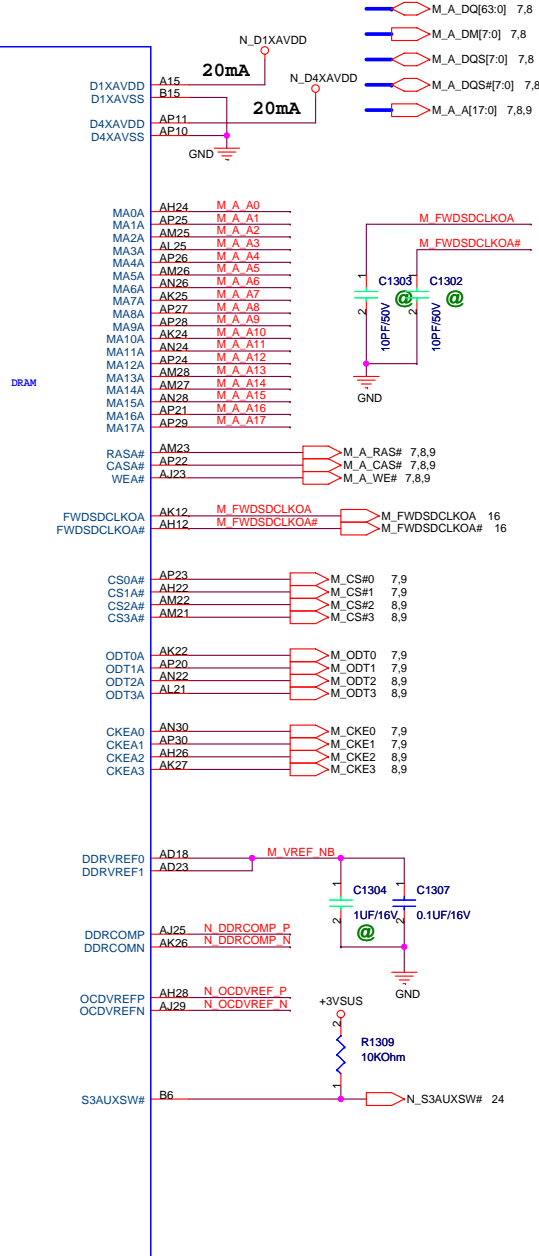
+1.2VS \rightarrow +1.2VS 14.83,91

Total Power mW(Max)		
1.2V	V_AVDD_PCIE_1.2V	190mA

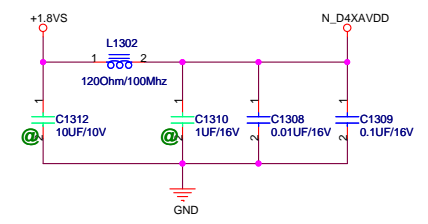


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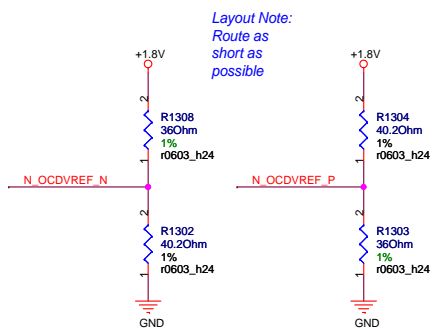
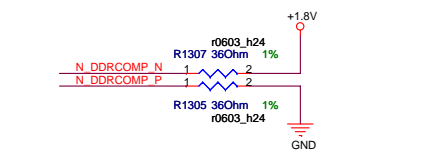
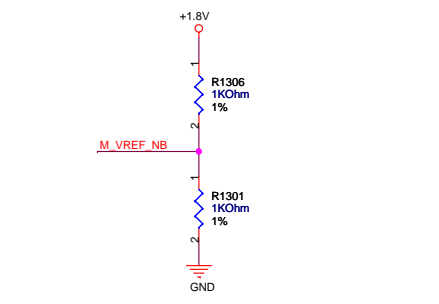
U1001B	
M A D00	AD31
M A D01	AD30
M A D02	AG34
M A D03	AE29
M A D04	AE32
M A D05	AF34
M A D06	AF31
M A D07	AE30
M A DM0	AD28
M A DQ50	AF32
M A DQS#0	AF33
M A DQ8	AF28
M A DQ9	AJ34
M A DQ10	AH31
M A DQ11	AC30
M A DQ12	AF30
M A DQ13	AG32
M A DQ14	AJ32
M A DQ15	AJ31
M A DM1	AH34
M A DQ51	AH32
M A DQS#1	AH33
M A DQ16	AK34
M A DQ17	AH30
M A DQ18	AL32
M A DQ19	AM33
M A DQ20	AK32
M A DQ21	AG29
M A DQ22	AL34
M A DQ23	AL31
M A DM2	AJ30
M A DQ52	AK33
M A DQS#2	AL34
M A DQ24	AM32
M A DQ25	AP32
M A DQ26	AP31
M A DQ27	AM29
M A DQ28	AK30
M A DQ29	AK29
M A DQ30	AJ27
M A DQ31	AK28
M A DM3	AK32
M A DQ53	AM30
M A DQS#3	AM31
M A DQ32	AK20
M A DQ33	AK20
M A DQ34	AM19
M A DQ35	AJ19
M A DQ36	AN20
M A DQ37	AJ21
M A DQ38	AP19
M A DQ39	AH20
M A DM4	AK21
M A DQ54	AK19
M A DQS#4	AL19
M A DQ40	AK18
M A DQ41	AJ17
M A DQ42	AK17
M A DQ43	AP16
M A DQ44	AH18
M A DQ45	AP18
M A DQ46	AN18
M A DQ47	AP17
M A DM5	AM18
M A DQ55	AL17
M A DQS#5	AM17
M A DQ48	AN16
M A DQ49	AK16
M A DQ50	AN14
M A DQ51	AJ15
M A DQ52	AP15
M A DQ53	AM16
M A DQ54	AK15
M A DQ55	AP14
M A DM6	AH16
M A DQ56	AL15
M A DQS#6	AM15
M A DQ56	AL13
M A DQ57	AM13
M A DQ58	AM12
M A DQ59	AJ13
M A DQ60	AM14
M A DQ61	AK14
M A DQ62	AN12
M A DQ63	AH14
M A DM7	AK13
M A DQ67	AP12
M A DQS#7	AP13



+3VSUS	+3VSUS	21,22,23,24,30,33,35,43,53,81,83,92
+1.8VS	+1.8VS	10,11,14,16,20,21,22,23,25,91
+1.8V	+1.8V	7,8,9,14,83,91



Total Power mW(Max)		
1.8VS	N_D1XAVDD	7mA
1.8VS	N_D4XAVDD	10mA



Layout Note:
Route as short as possible



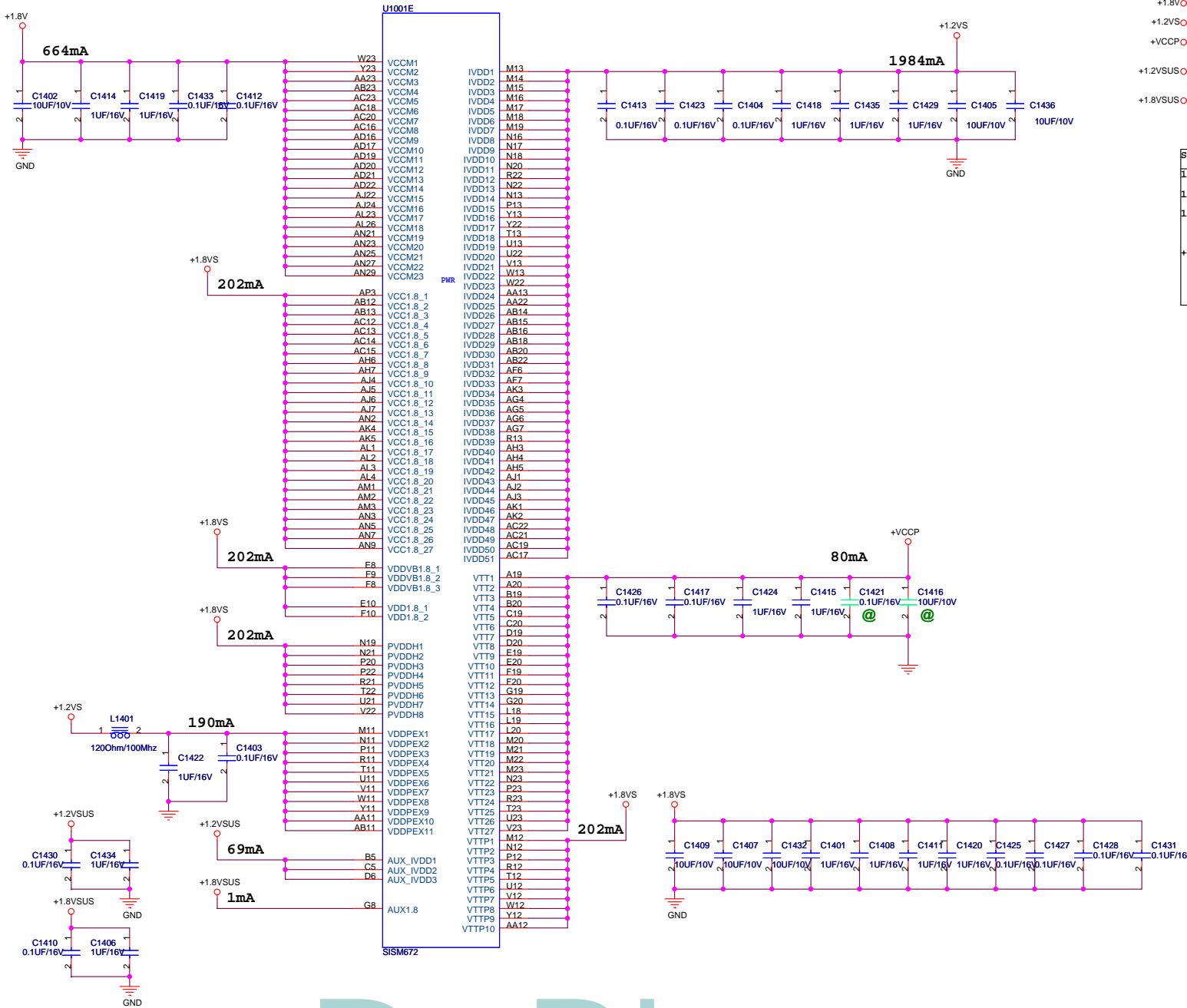
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ASUS Title : NB-SISM672 (DDR2)

ASUSTeK COMPUTER INC. NB Engineer: Hawk / Kaxidy

Size	Project Name	Rev
Custom	T12C	1.1

Date: Friday, August 17, 2007 Sheet 13 of 94



- +1.8VS ○ ○ +1.8VS 10,11,13,16,20,21,22,23,25,91
- +1.8V ○ ○ +1.8V 7,8,9,13,83,91
- +1.2VS ○ ○ +1.2VS 12,83,91
- +VCCP ○ ○ +VCCP 4,10,21,23,29,57,83,92
- +1.2VSUS ○ ○ +1.2VSUS 82
- +1.8VSUS ○ ○ +1.8VSUS 21,22,23,82

SiSM672 Total Power 4664mW (3D Mode)		
1.2VS	+1.2VS_NB	1984mA
1.8V	VCCM1-23	64mA
1.8VS	VCC1.8/VDDVB1.8/ VDDL.8/PVDDH/VTTP	202mA
+VCCP	VTT1-27	80mA
	VDDPEX1-11	190mA

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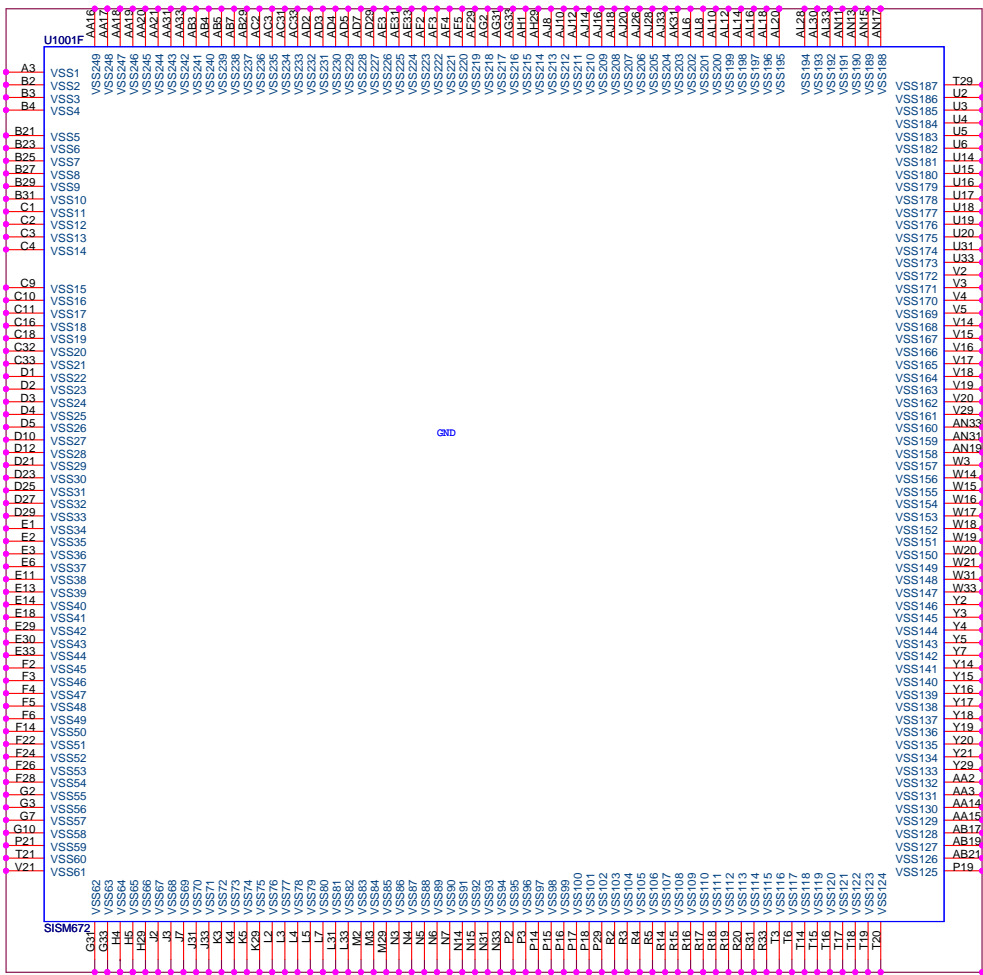
<Variant Name>

ASUS Title : NB_SiS672 (PWR)

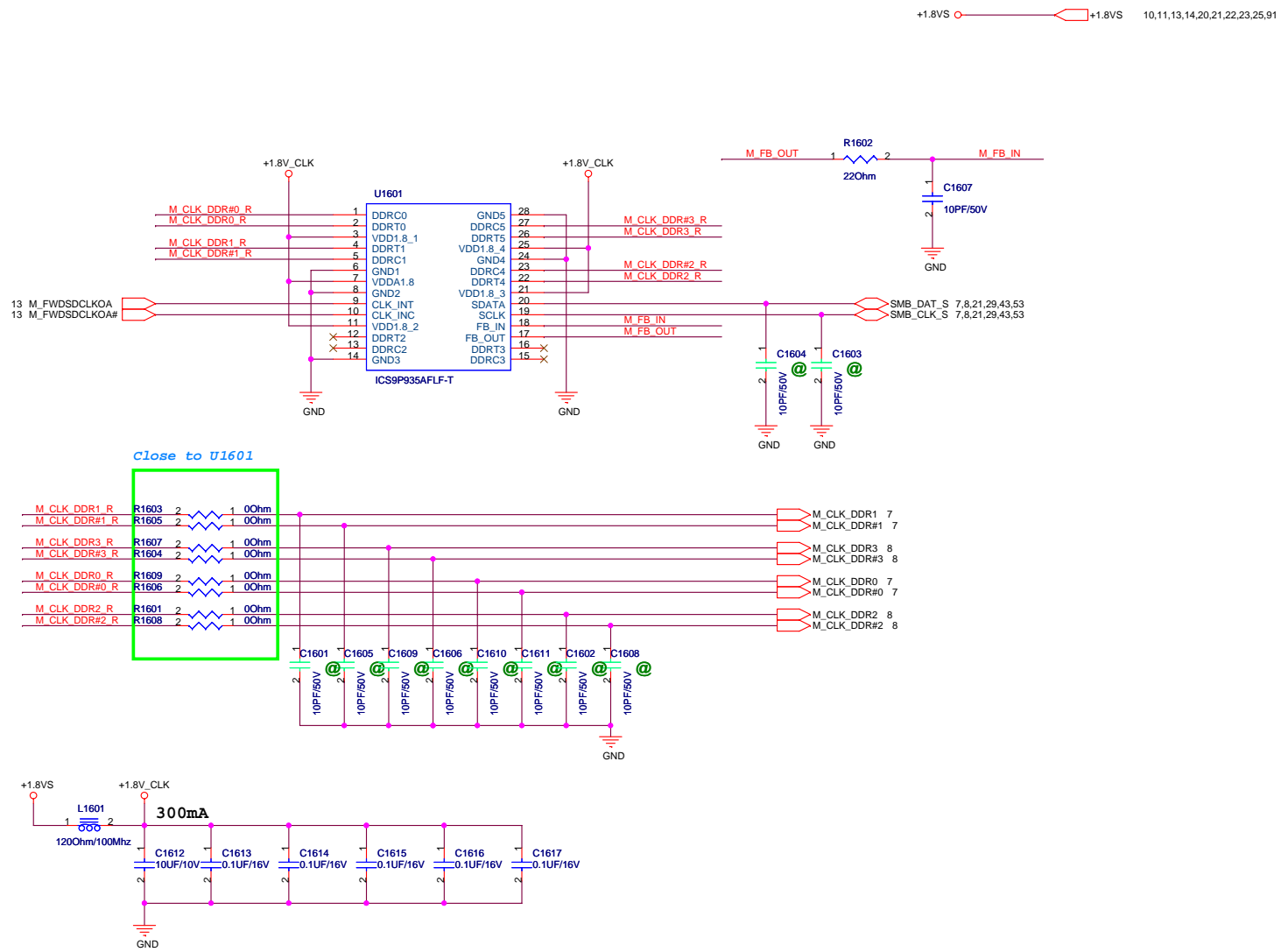
ASUSTek COMPUTER INC. NB Engineer: Hawk / Kaxidy

Size	Project Name	Rev
Custom	T12C	1.1

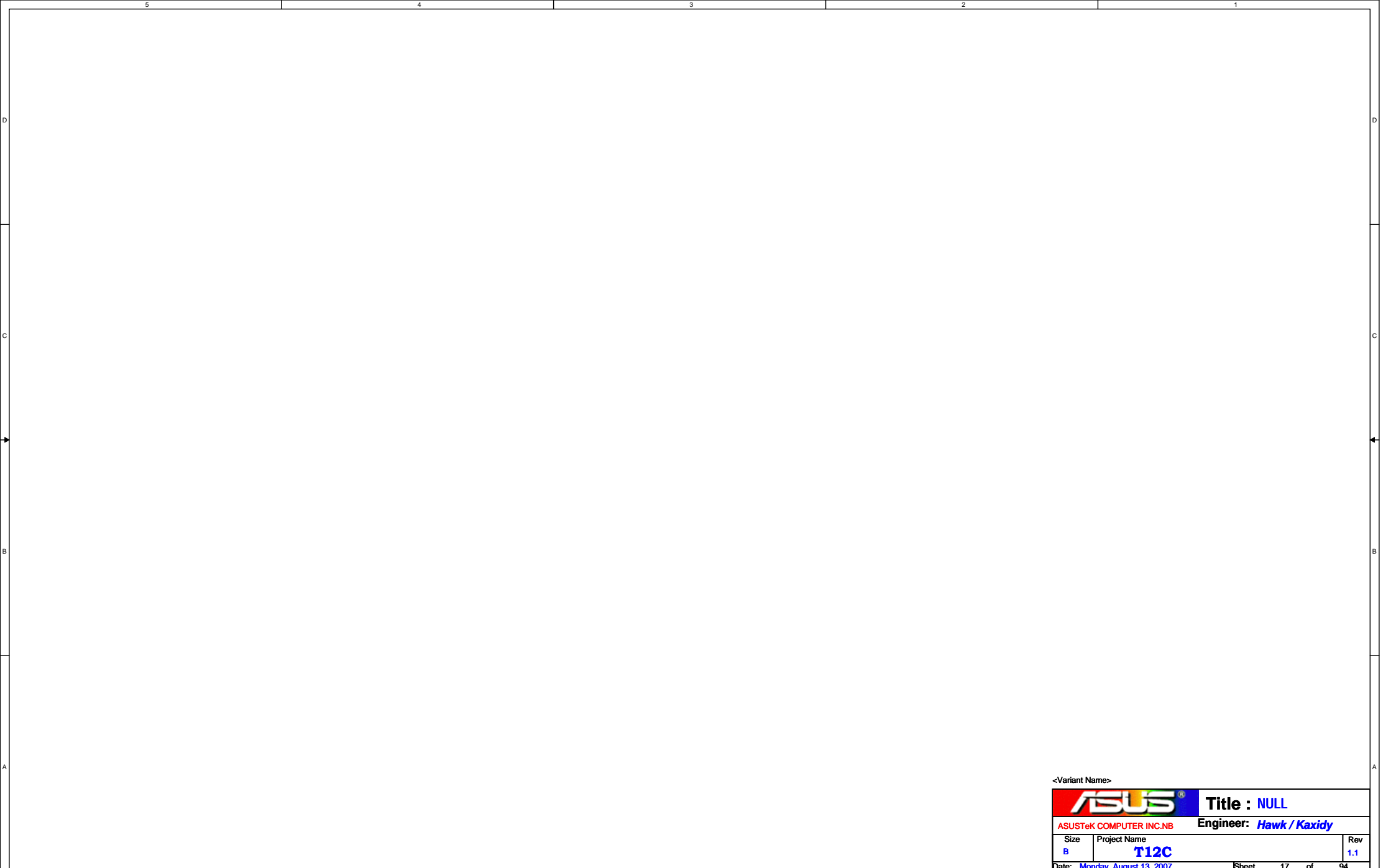
Date: Friday, August 17, 2007 Sheet 14 of 94




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<Variant Name>		
		Title : NULL
ASUSTeK COMPUTER INC.NB		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
B	T12C	1.1
Date: Monday, August 13, 2007	Sheet	17 of 94

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<Variant Name>


		Title : NULL	
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	18 of 94

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<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	19 of 94

5

4

3

2

1

A

A

B

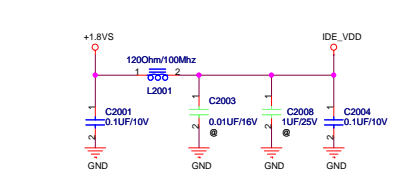
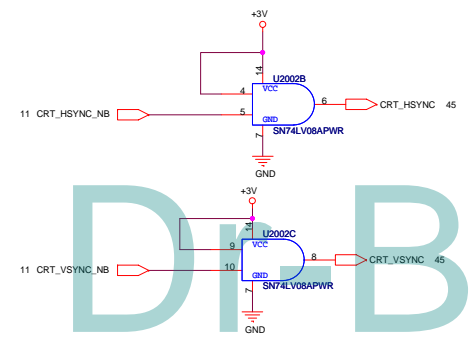
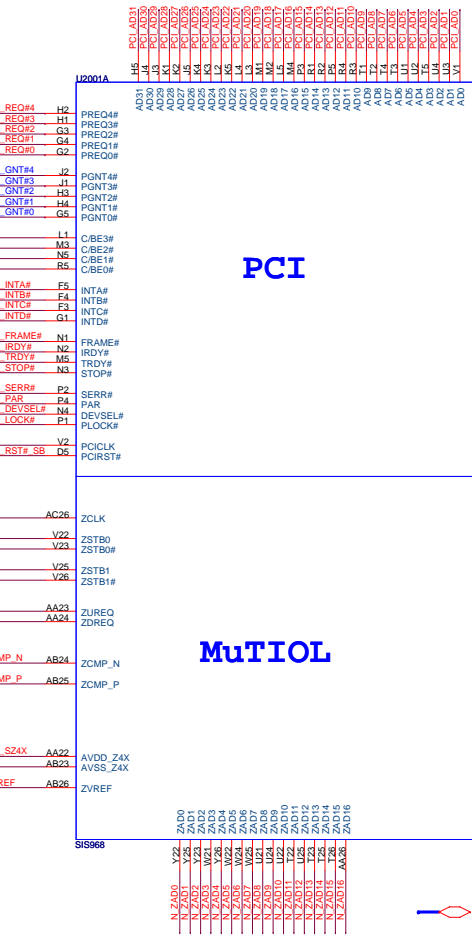
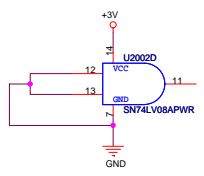
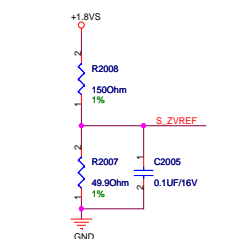
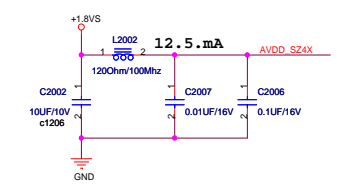
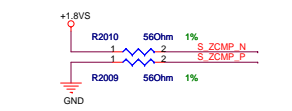
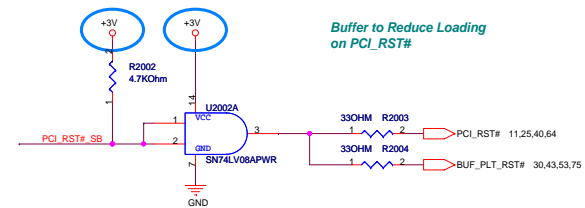
B

C

C

D

D



+1.8VS	10,11,13,14,16,21,22,23,25,91
+3VS	3,7,8,11,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
+3VO	23,35,40,46,53,57,61,62,64,65,91

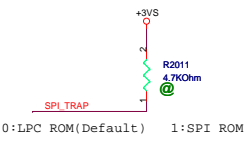
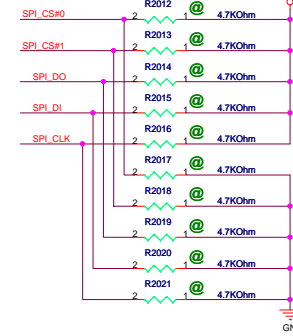
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PCI_REQ#1	R2026	2	1	8.2kOhm
PCI_REQ#2	R2027	2	1	8.2kOhm
PCI_REQ#3	R2028	2	1	8.2kOhm
PCI_REQ#4	R2029	2	1	8.2kOhm
PCI_GNT#0	R2030	2	1	8.2kOhm
PCI_GNT#1	R2031	2	1	8.2kOhm
PCI_GNT#2	R2032	2	1	8.2kOhm
PCI_GNT#3	R2033	2	1	8.2kOhm
PCI_GNT#4	R2034	2	1	8.2kOhm

PCI_INT#	RP2001A	1	8.2kOhm
PCI_INTB	RP2001B	2	8.2kOhm
PCI_INTA	RP2001C	3	8.2kOhm
PCI_INTD	RP2001D	4	8.2kOhm
RP2001E	6	8.2kOhm	
RP2001F	7	8.2kOhm	
RP2001G	8	8.2kOhm	
RP2001H	9	8.2kOhm	

PCI_LOCK#	RN2001A	1	4.7kOhm
PCI_SERR#	RN2001B	3	4.7kOhm
PCI_DEVSEL#	RN2001C	5	4.7kOhm
PCI_FRAME#	RN2001D	7	4.7kOhm

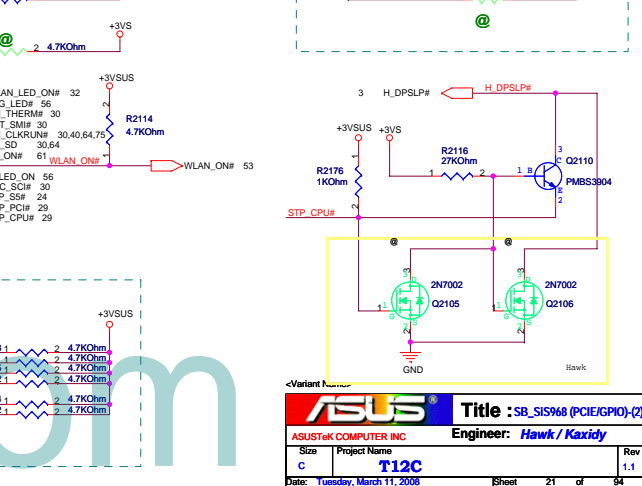
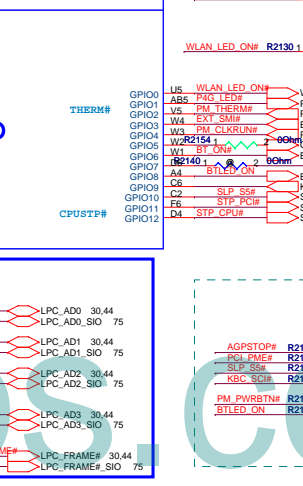
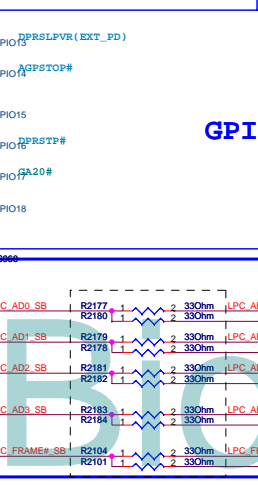
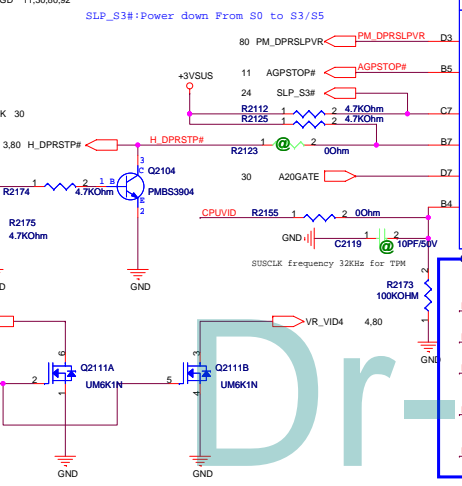
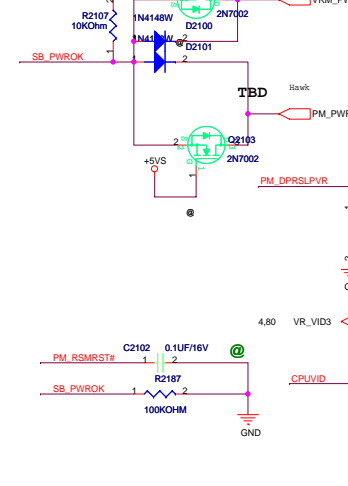
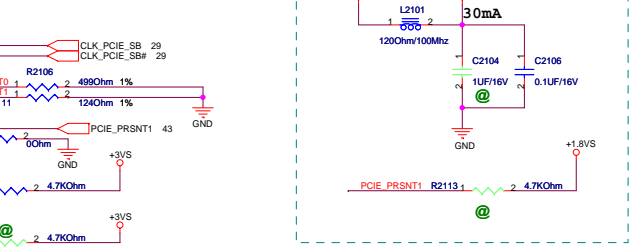
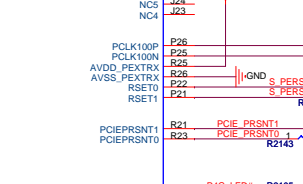
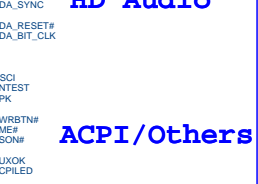
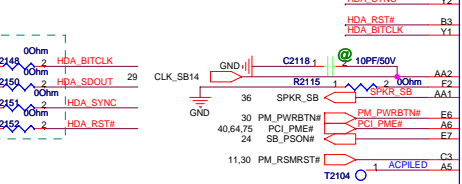
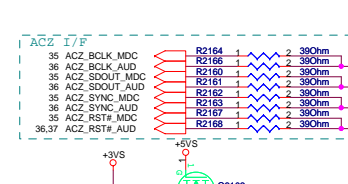
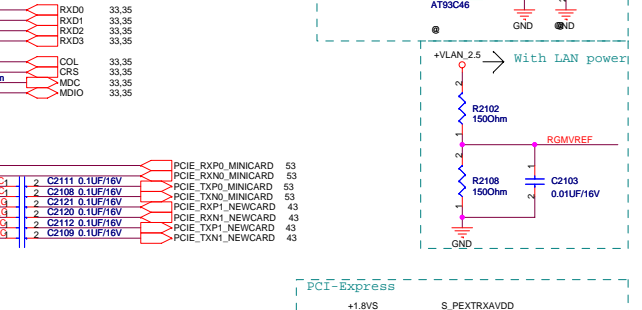
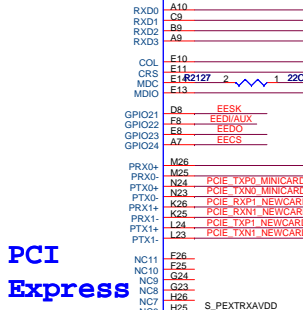
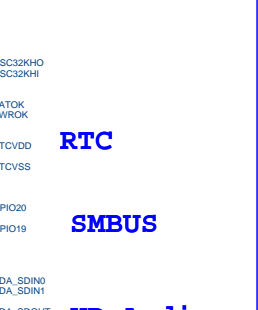
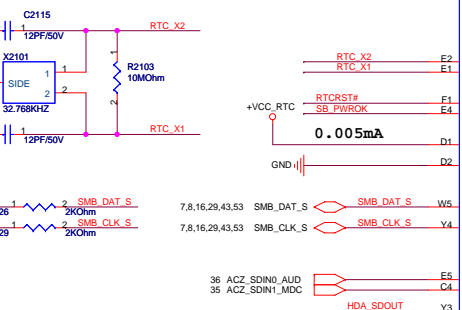
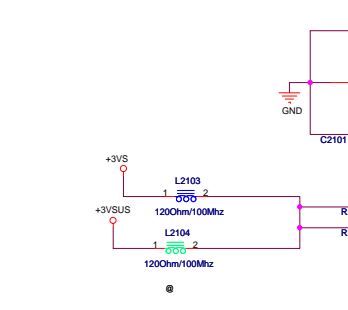
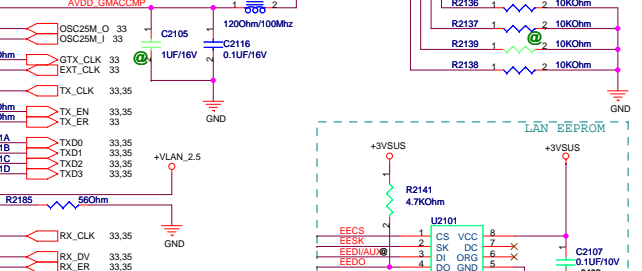
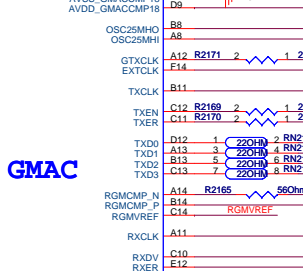
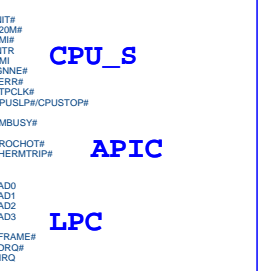
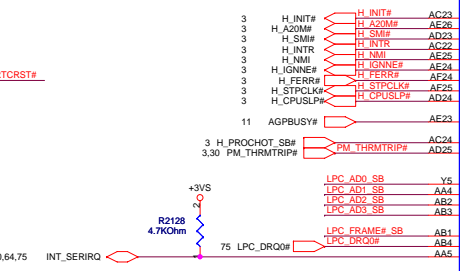
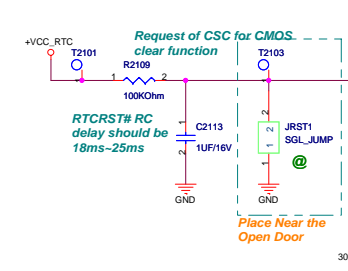
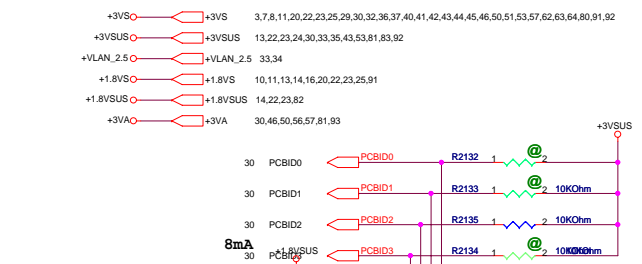
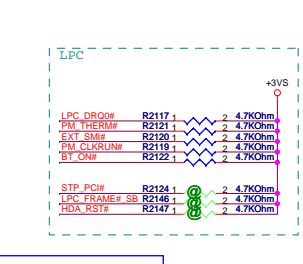
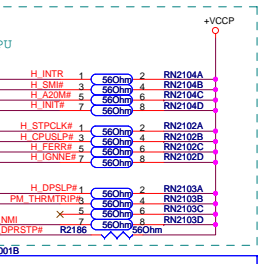
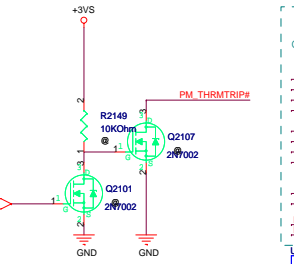
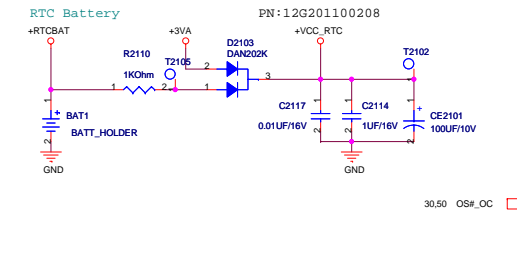
PCI_IRDY#	RN2002A	1	4.7kOhm
PCI_TRDY#	RN2002B	3	4.7kOhm
PCI_STOP#	RN2002C	5	4.7kOhm
PCI_PERR#	RN2002D	7	4.7kOhm

IDE_PIORDY	RN2003C	5	4.7kOhm
IDE_PODREQ	RN2003A	1	4.7kOhm
INT_IRGT4	RN2003B	3	4.7kOhm
IDE_PDD7	RN2003D	7	4.7kOhm

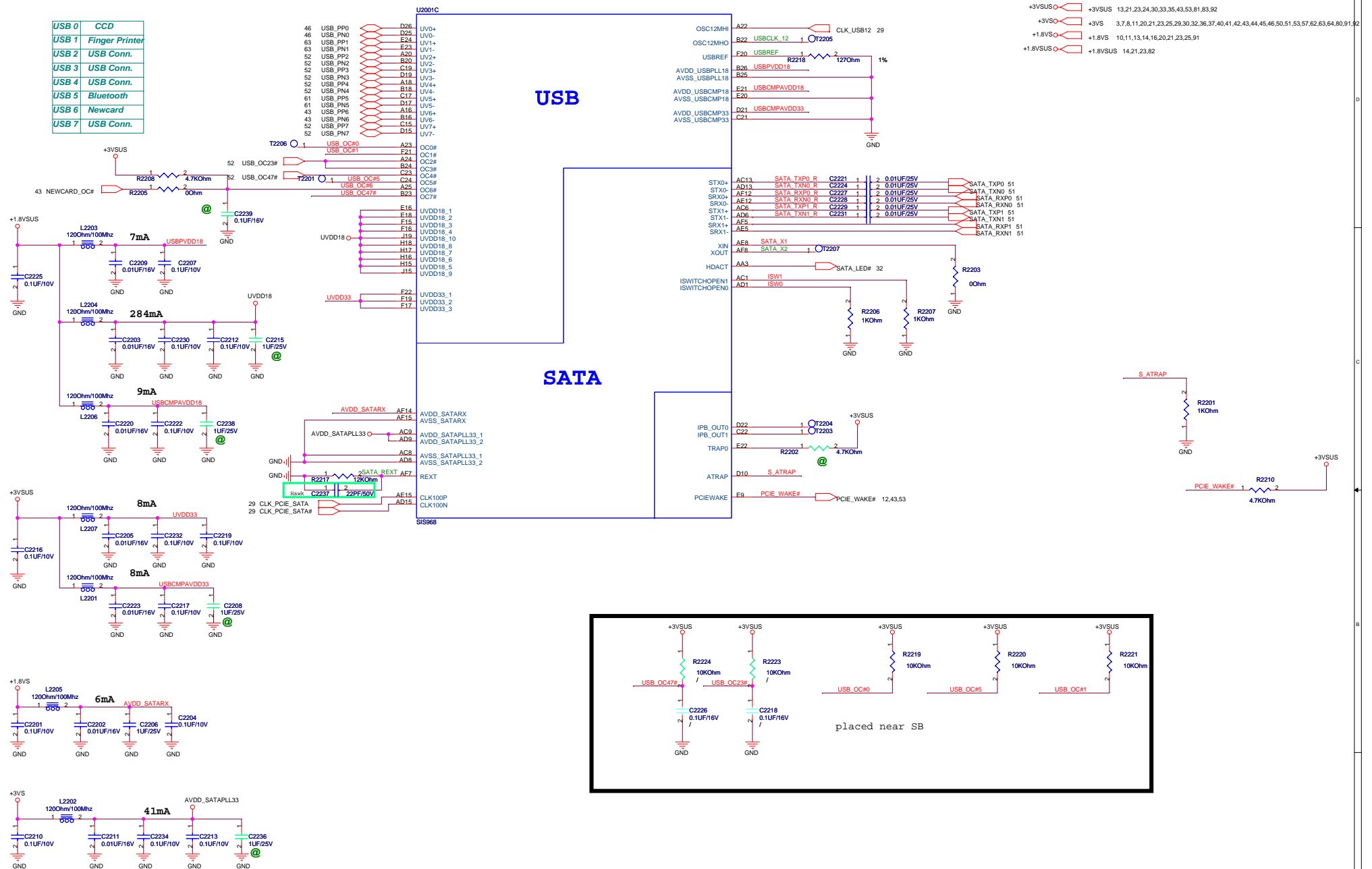


0:LPC ROM(Default) 1:SPI ROM

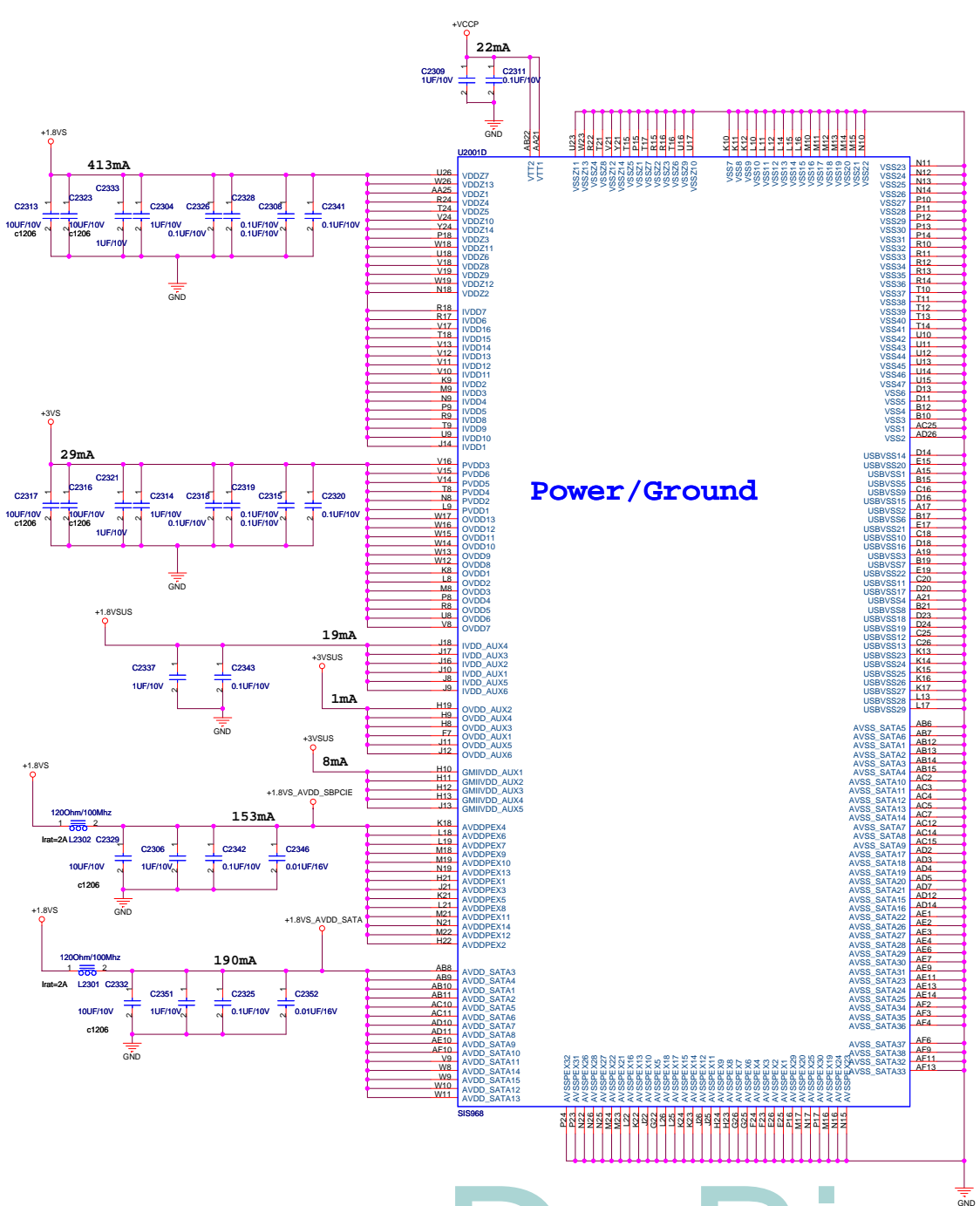




USB 0	CCD
USB 1	Finger Printer
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB Conn.
USB 5	Bluetooth
USB 6	Newcard
USB 7	USB Conn.

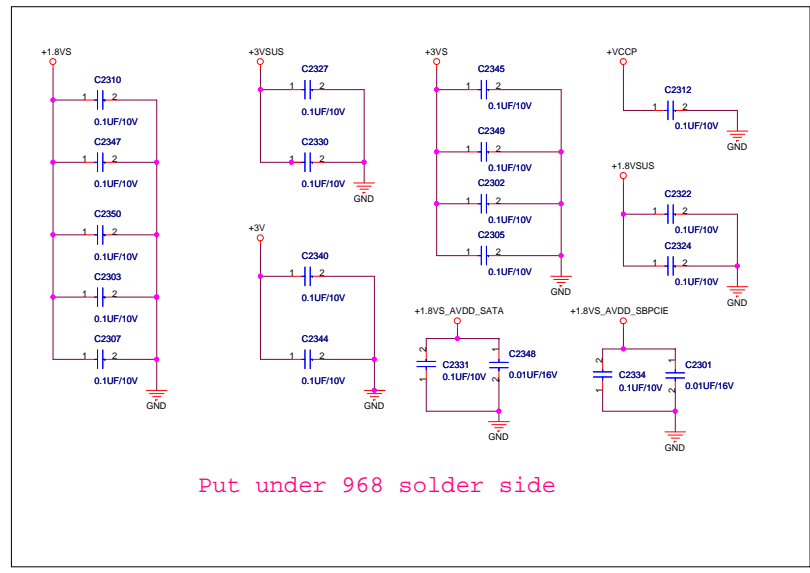
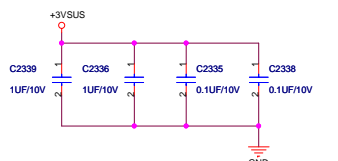


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Power /Ground

- +3VSUS ○ +3VSUS 13,21,22,24,30,33,35,43,53,81,83,92
- +1.8VSUS ○ +1.8VSUS 14,21,22,82
- +1.8VS ○ +1.8VS 10,11,13,14,16,20,21,22,25,91
- +3VS ○ +3VS 3,7,8,11,20,21,22,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
- +3V ○ +3V 20,35,40,46,53,57,61,62,64,65,91
- +VCCP ○ +VCCP 4,10,14,21,29,57,83,92

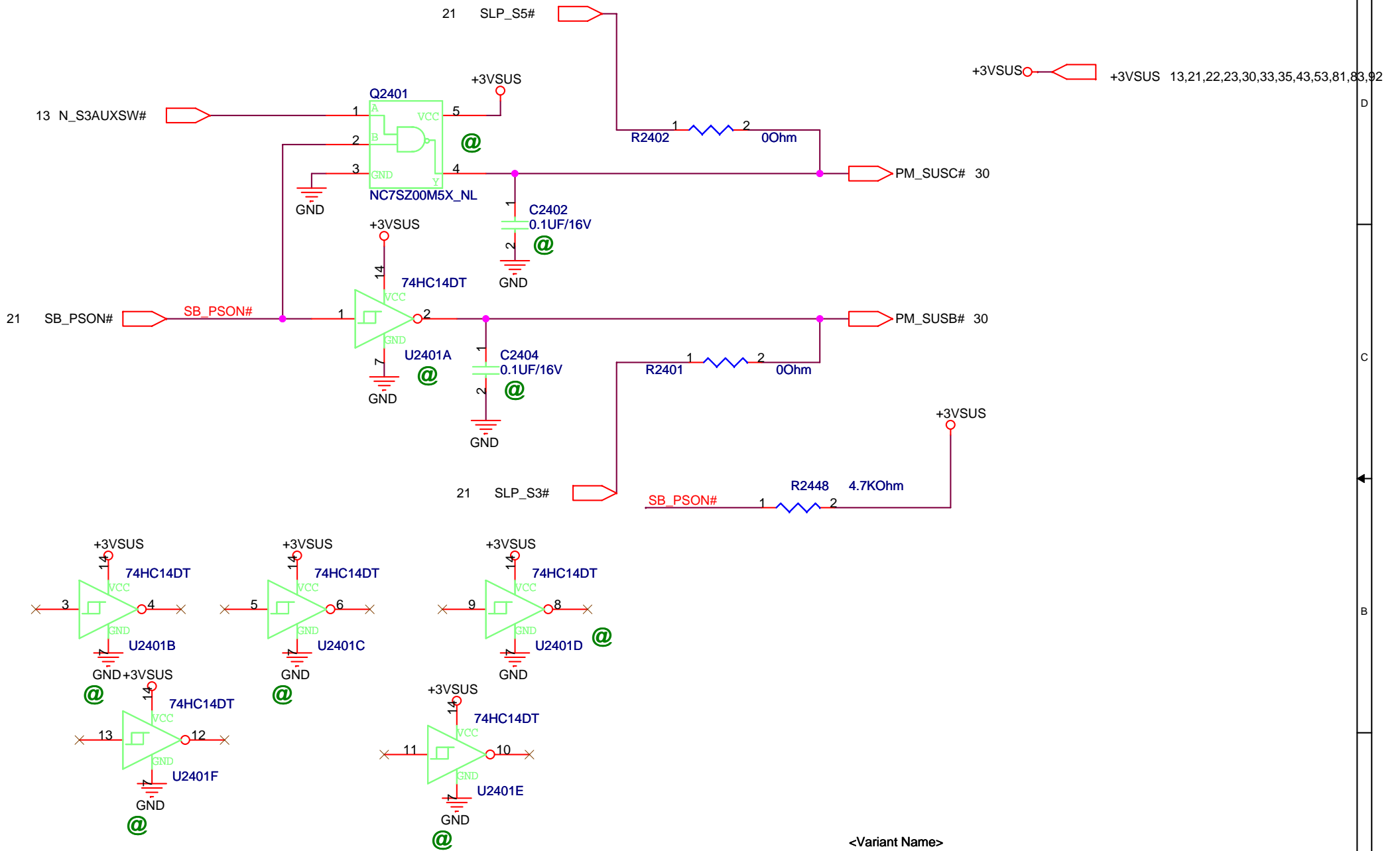


Put under 968 solder side

SIS968

- P24 AVSSPE_X30
- P23 AVSSPE_X1
- M24 AVSSPE_X26
- M23 AVSSPE_X27
- M25 AVSSPE_X22
- M22 AVSSPE_X21
- L22 AVSSPE_X16
- L21 AVSSPE_X15
- L20 AVSSPE_X10
- L19 AVSSPE_X9
- L18 AVSSPE_X17
- K23 AVSSPE_X15
- K21 AVSSPE_X12
- H24 AVSSPE_X11
- H23 AVSSPE_X8
- G25 AVSSPE_X7
- G24 AVSSPE_X6
- E24 AVSSPE_X3
- E23 AVSSPE_X1
- M17 AVSSPE_X25
- M16 AVSSPE_X29
- M15 AVSSPE_X19
- M14 AVSSPE_X24
- M13 AVSSPE_X3
- M12 AVSSPE_X3
- M11 AVSSPE_X3
- M10 AVSSPE_X3
- M9 AVSSPE_X3
- M8 AVSSPE_X3
- M7 AVSSPE_X3
- M6 AVSSPE_X3
- M5 AVSSPE_X3
- M4 AVSSPE_X3
- M3 AVSSPE_X3
- M2 AVSSPE_X3
- M1 AVSSPE_X3
- M0 AVSSPE_X3





<Variant Name>


		Title : Si968 (STRAPING)
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Friday, August 17, 2007		Sheet 24 of 94

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<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC .NB		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: <i>Monday, August 13, 2007</i>		Sheet	26 of 94
			1




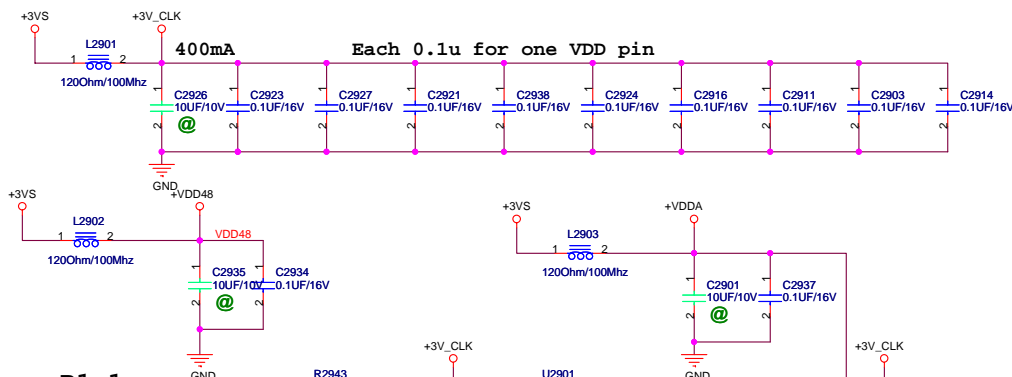
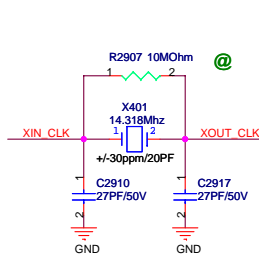
<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size	Project Name	Rev
A	T12C	1.1
Date: <i>Monday, August 13, 2007</i>		Sheet 27 of 94

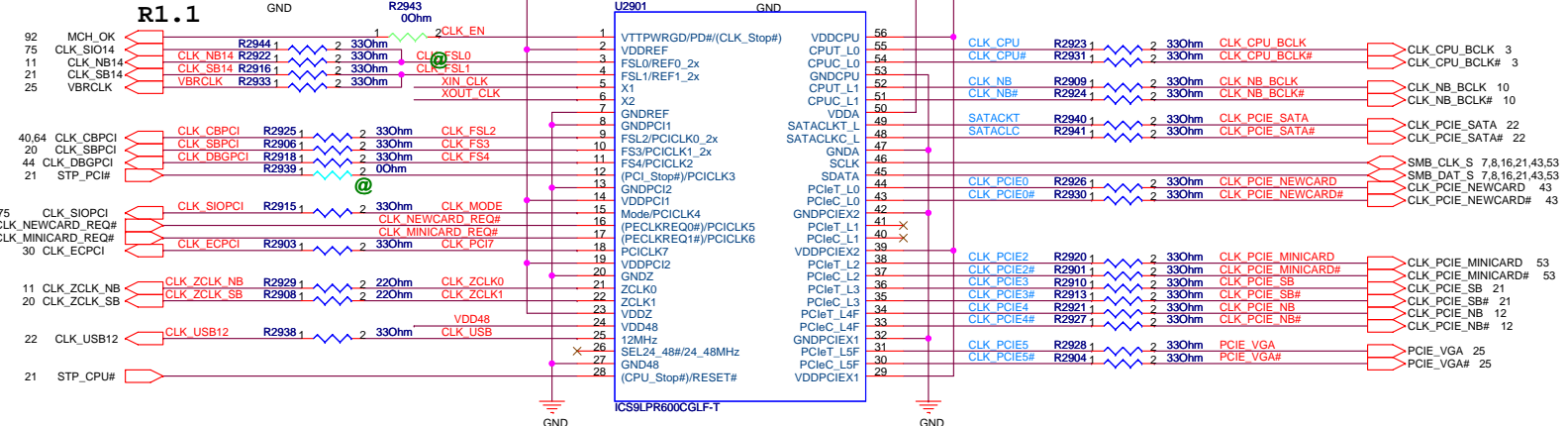
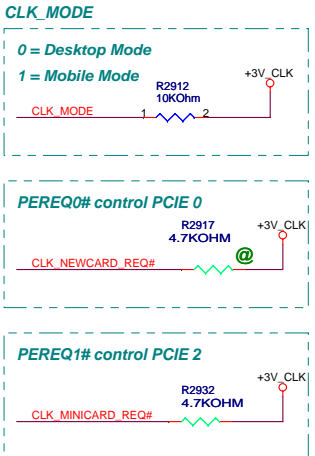
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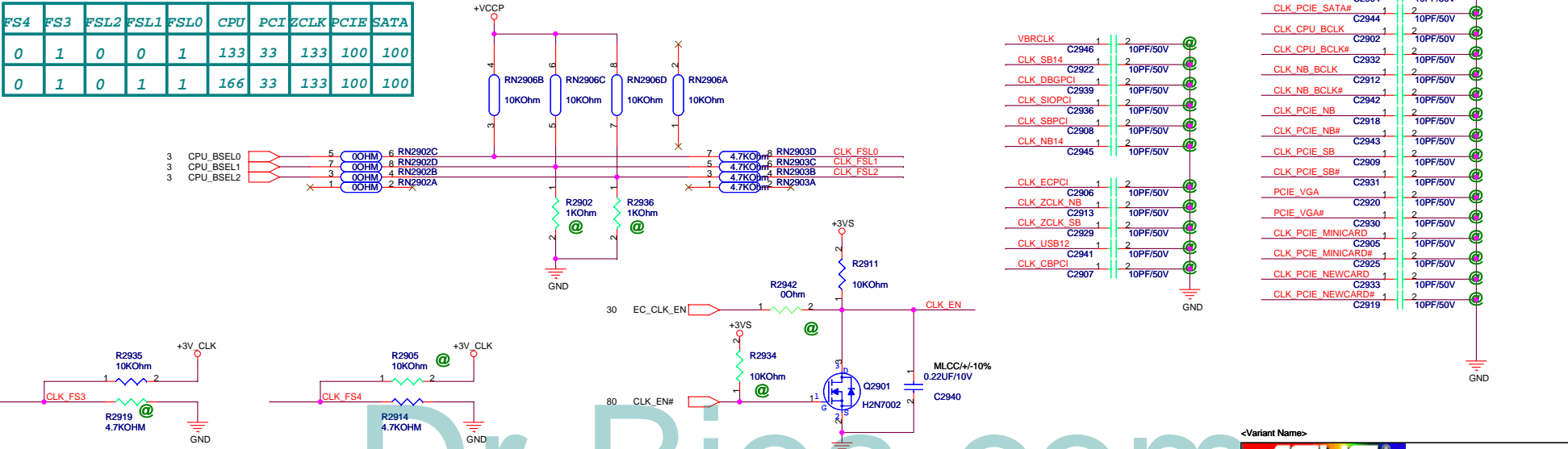
<Variant Name>		Title : NULL	
		Engineer: Hawk / Kaxidy	
ASUSTeK COMPUTER INC	Project Name	Size	Rev
Custom	T12C		1.1
Date: Monday, August 13, 2007	Sheet	28	of 94



+3VS 3,7,8,11,20,21,22,23,25,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
 +VCCP 4,10,14,21,23,57,83,82



FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



<Variant Name>
ASUS Title : **CLOCK GEN**
 ASUSTeK COMPUTER INC Engineer: **Hawk / Kaxidy**
 Size Project Name
 Custom **T12C**
 Date: **Friday, March 07, 2008** Sheet 29 of 94
 Rev 1.1

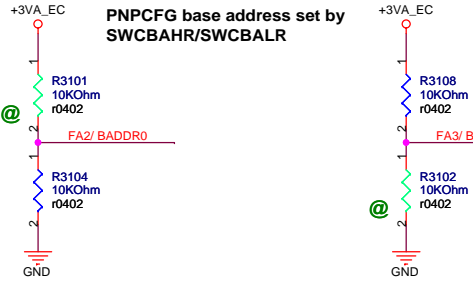
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EC Hardware Strap

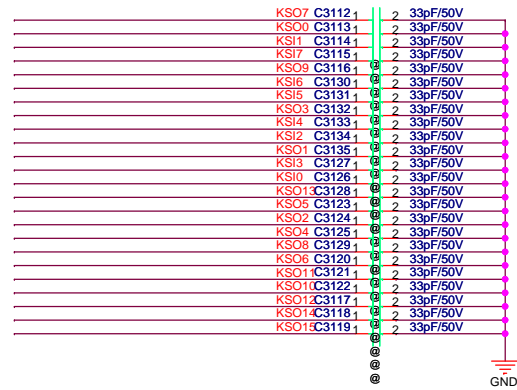
Strap value sampled after VSTBY power up reset

+3VA_ECO <- +3VA_EC 30,46

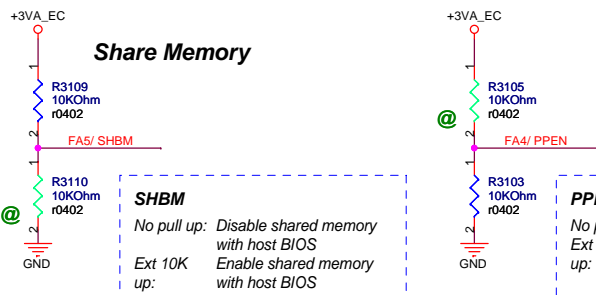
PNPCFG base address set by SWCBAHR/SWCBALR



BADDR[1:0]
 No pull up: The register pair to access PNPCFG is 002Eh and 002Fh.
 Ext 10K up on BADDR0: The register pair to access PNPCFG is 004Eh and 004Fh.
 Ext 10K up on BADDR1: The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.



Share Memory

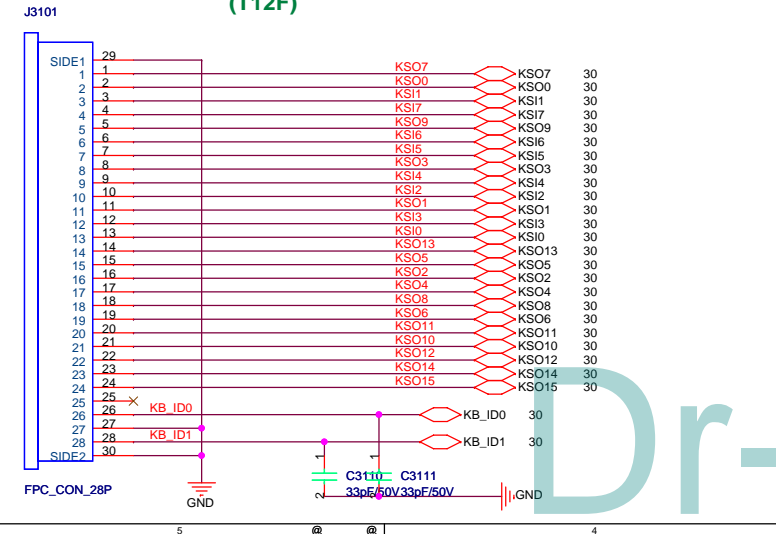


SHBM
 No pull up: Disable shared memory with host BIOS
 Ext 10K up: Enable shared memory with host BIOS

PPEN
 No pull up: Normal
 Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.

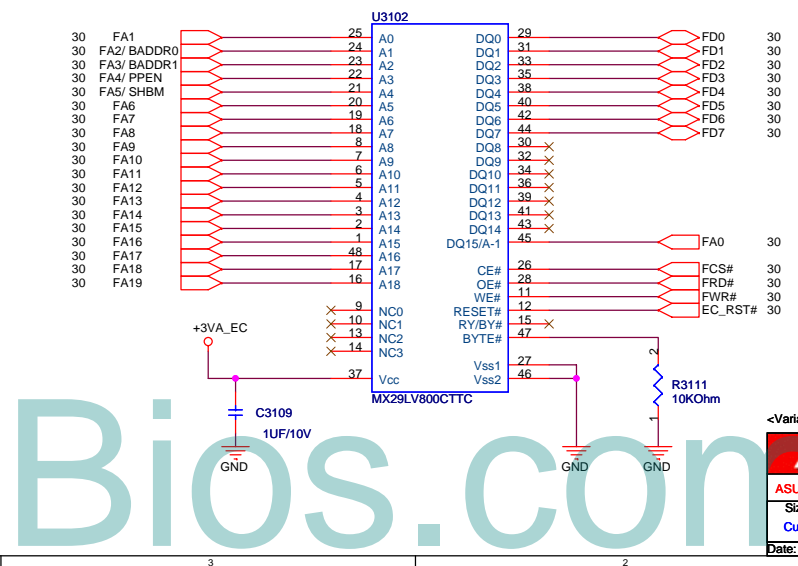
Keyboard Conn.

P/N: 12G182402806 (T12F)



For 8M bits SPI ROM

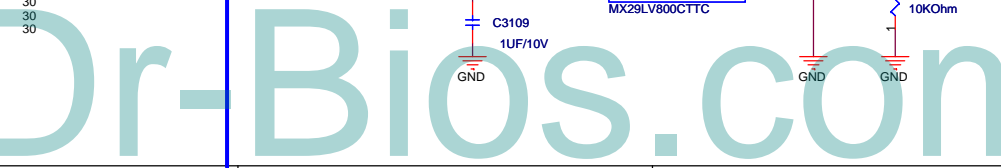
8M TSOP



<Variant Name>

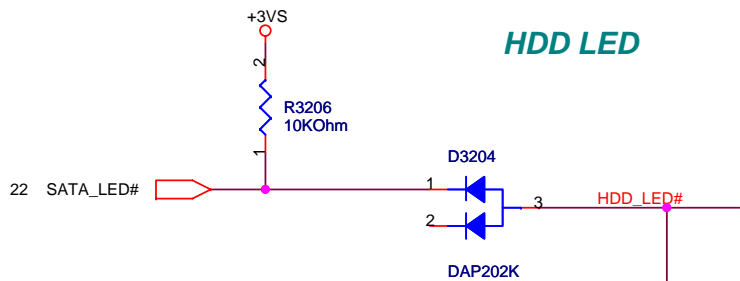
ASUS Title: EC-ITE8511(2)
 ASUSTeK COMPUTER INC.ETD Engineer: Hawk / Kaxidy

Size	Project Name	Rev
Custom	T12C	1.1
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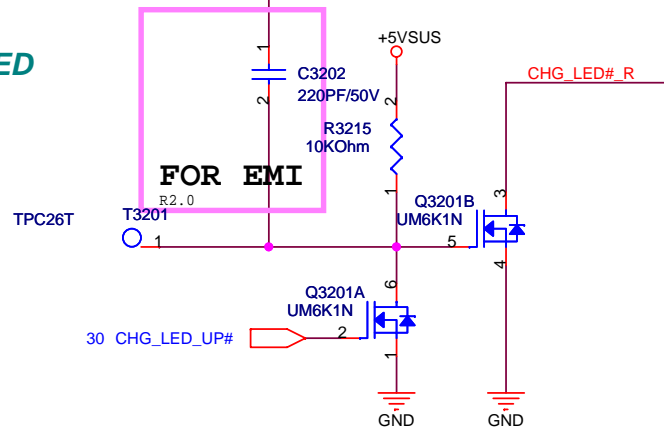


Touchpad

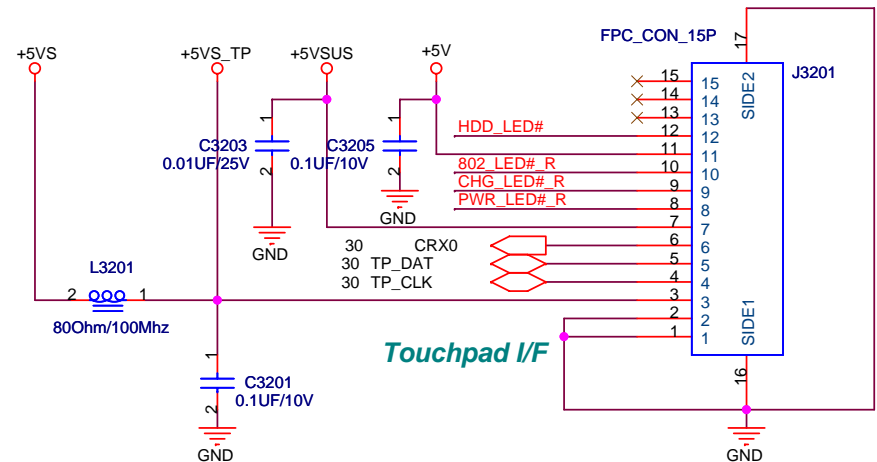
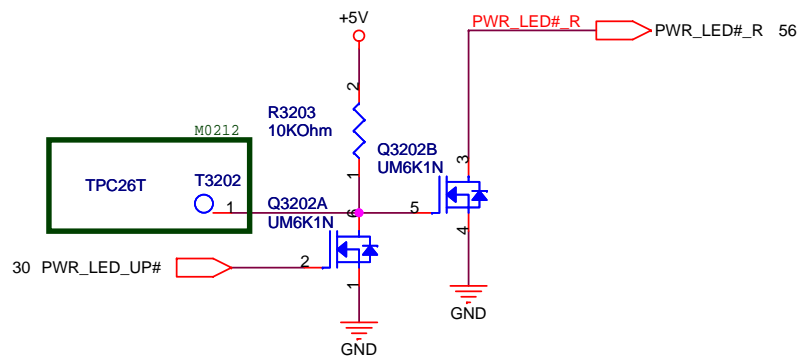
- +5VSUS ○ +5VSUS 33,81
 - +5VS ○ +5VS 21,30,36,37,38,45,50,51,56,57,80,91
 - +3VS ○ +3VS 3,7,8,11,20,21,22,23,25,29,30,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
 - +5V ○ +5V 37,46,52,56,57,65,91
- I2G183101506**
T12



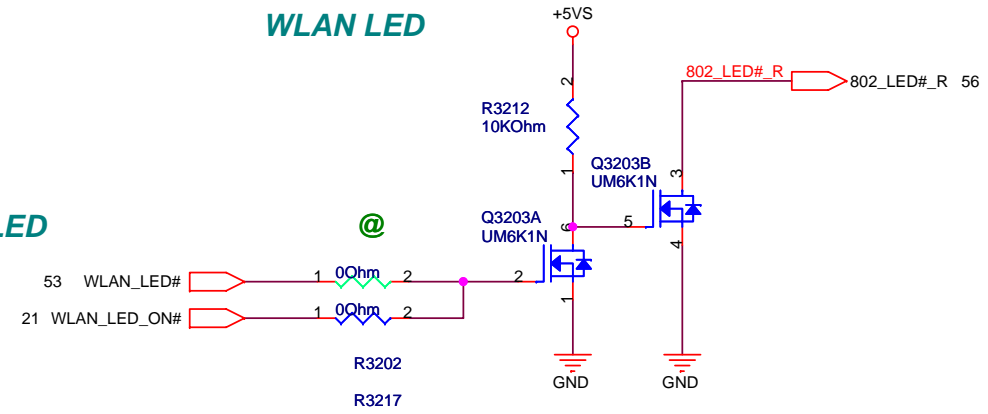
CHARGE LED



POWER LED



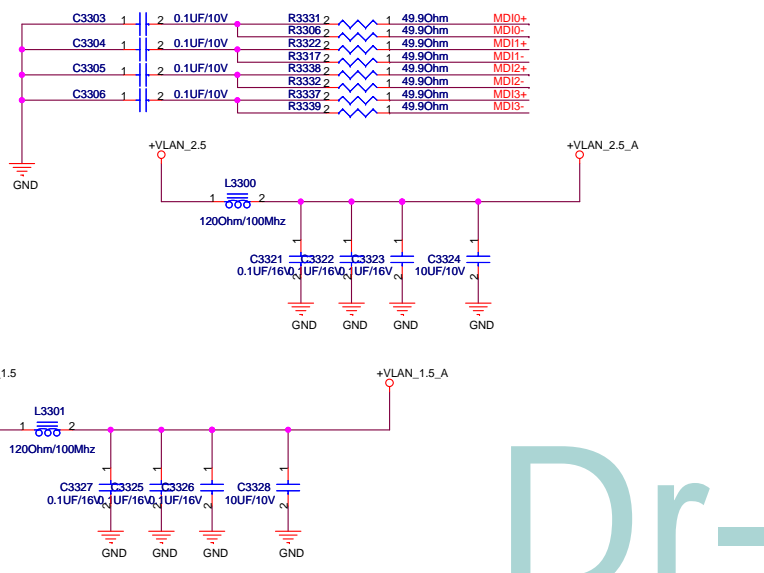
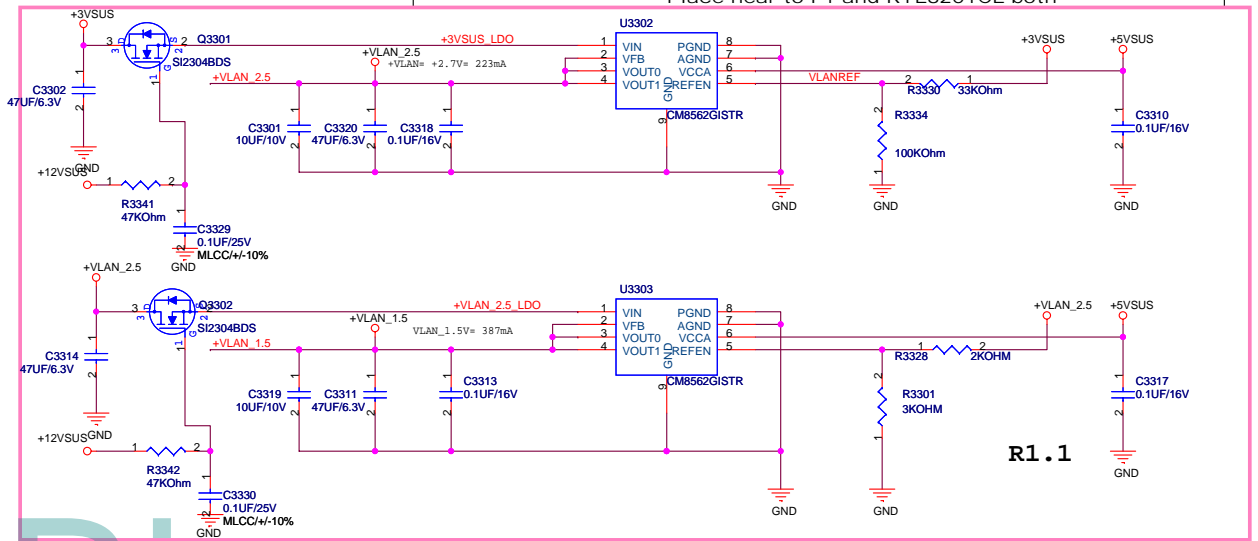
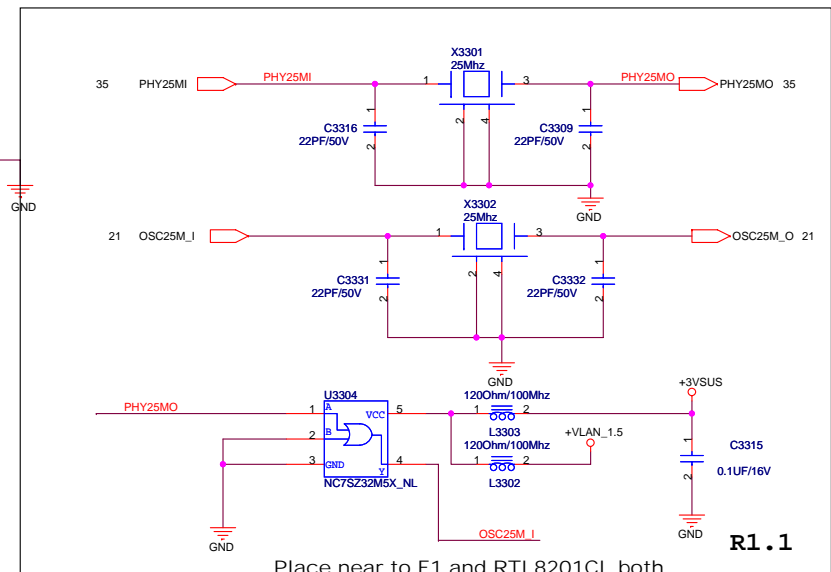
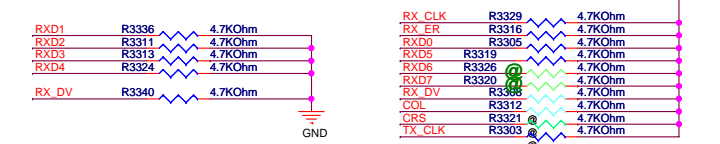
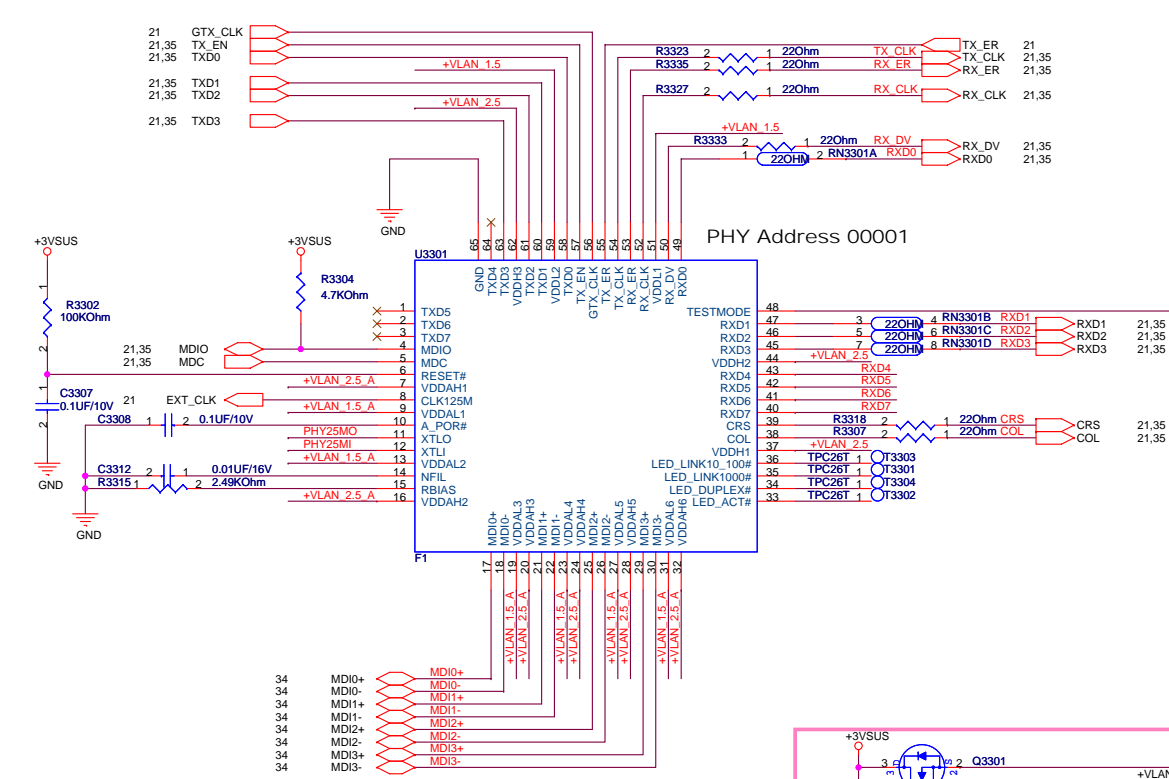
WLAN LED



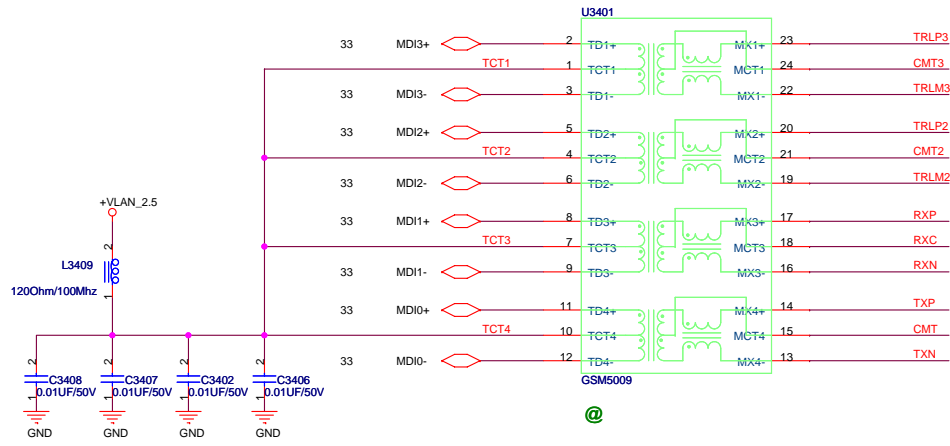
<Variant Name>

ASUS		Title : TouchPad
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
Custom	T12C	1.1
Date: Tuesday, March 04, 2008		Sheet 32 of 94

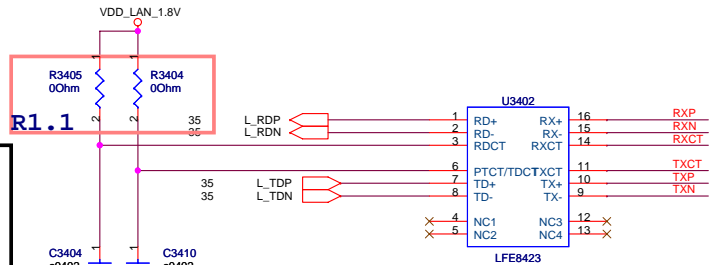
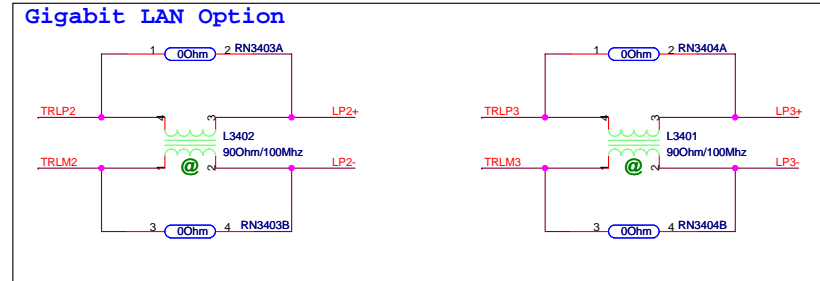
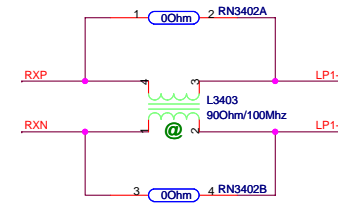
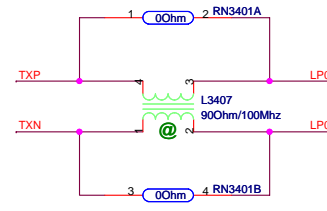
VDD_LAN_1.8V	VDD_LAN_1.8V	34,35
+VLAN_2.5	+VLAN_2.5	21,34
+3VSUS	+3VSUS	13,21,22,23,24,30,35,43,53,81,83,92
+5VSUS	+5VSUS	32,81
+5V0	+5V	32,37,46,52,56,57,65,91



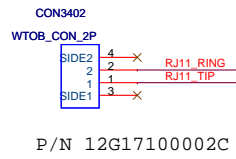
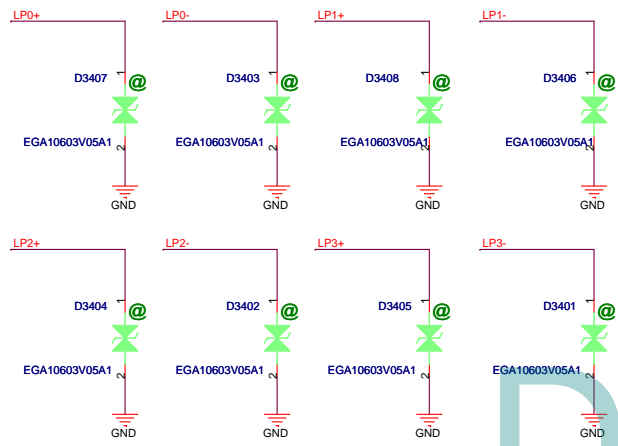
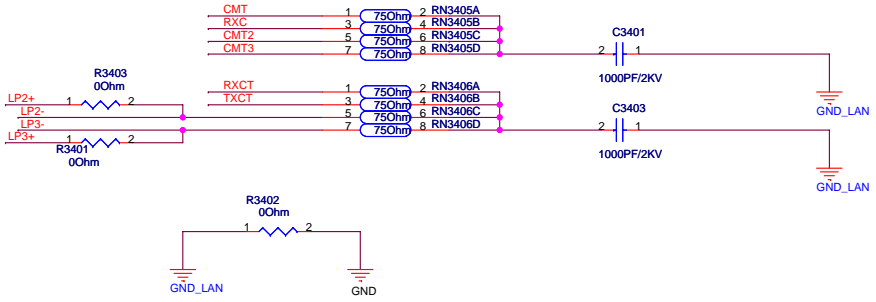
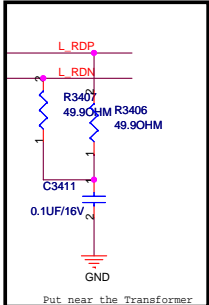
Dr-Bios.com



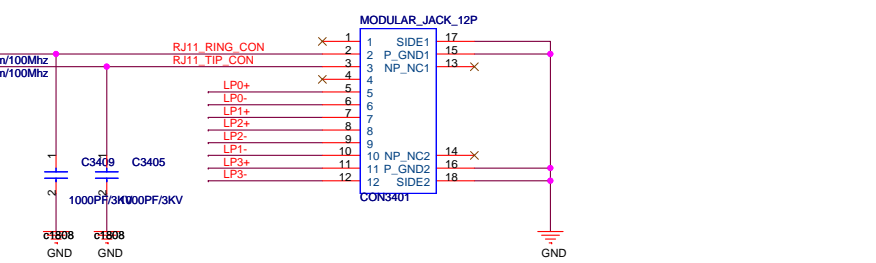
VDD_LAN_1.8V \rightarrow VDD_LAN_1.8V 35
 +VLAN_2.5 \rightarrow +VLAN_2.5 21,33



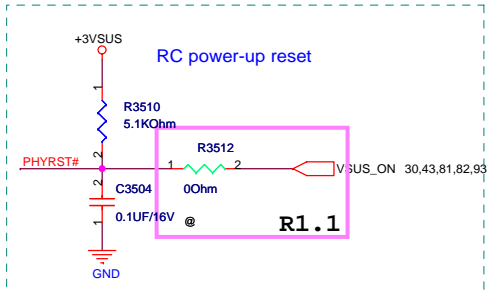
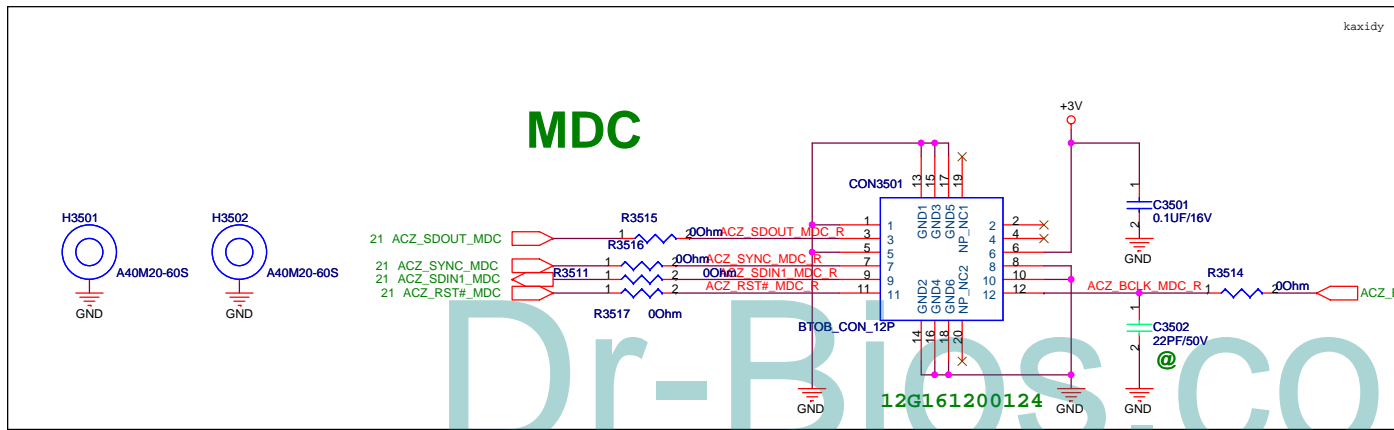
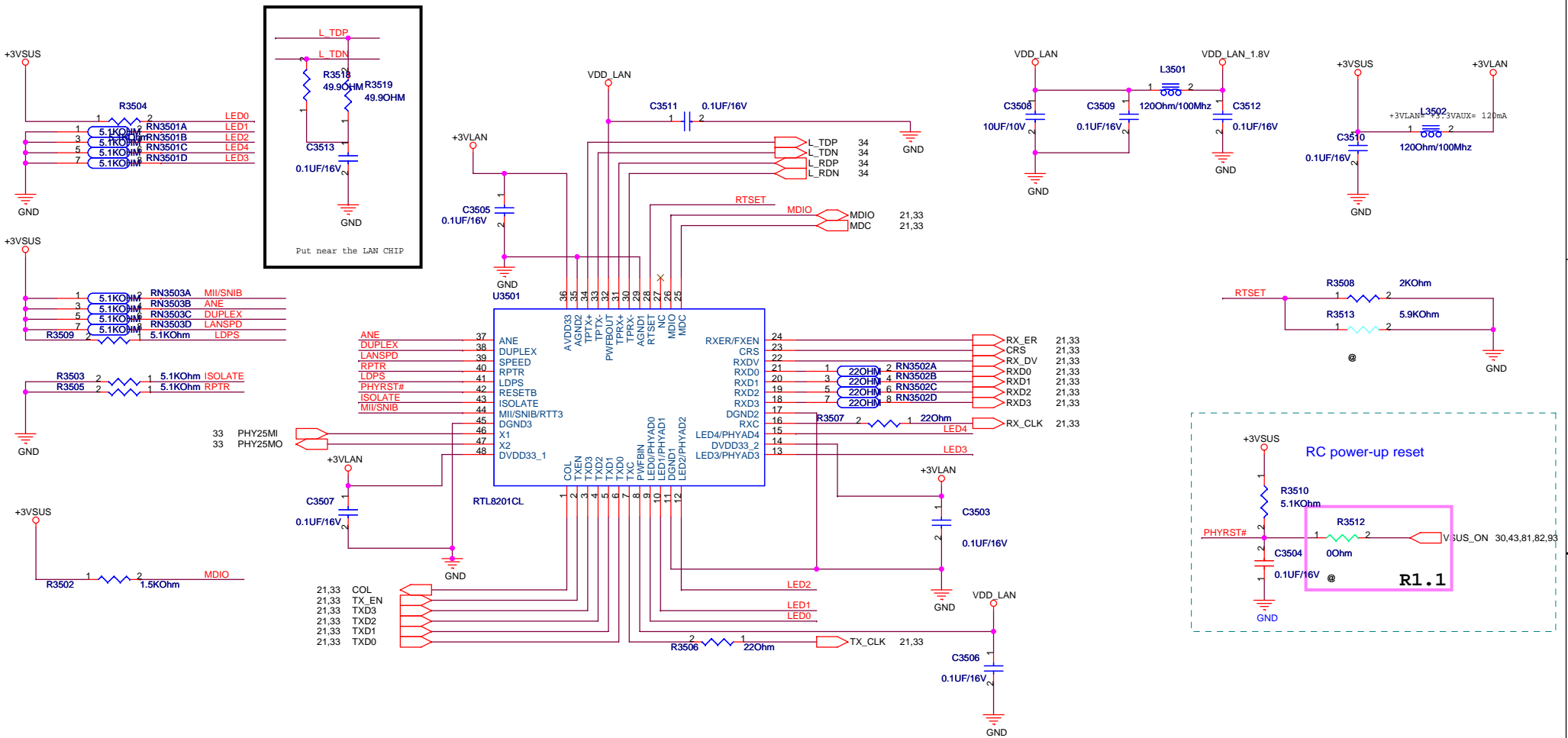
U3402 place under U3401
 Co-lay 10/100 BOM Option



P/N 12G17100002C



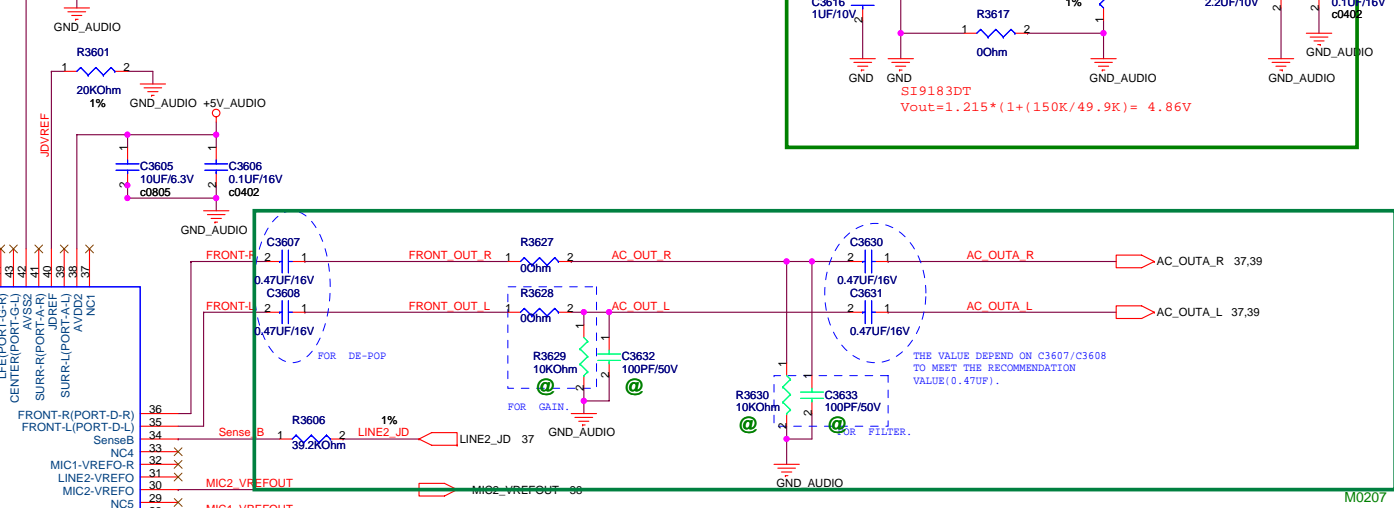
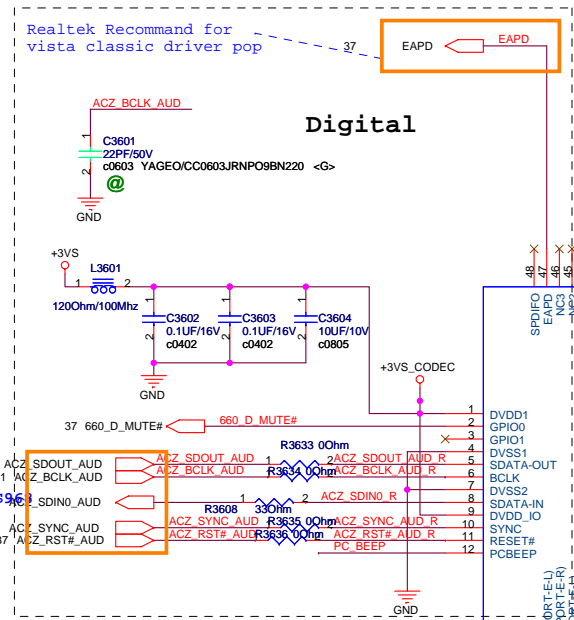
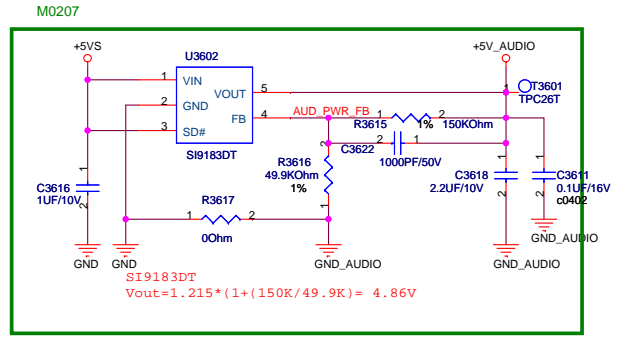
Dr-Bios.com



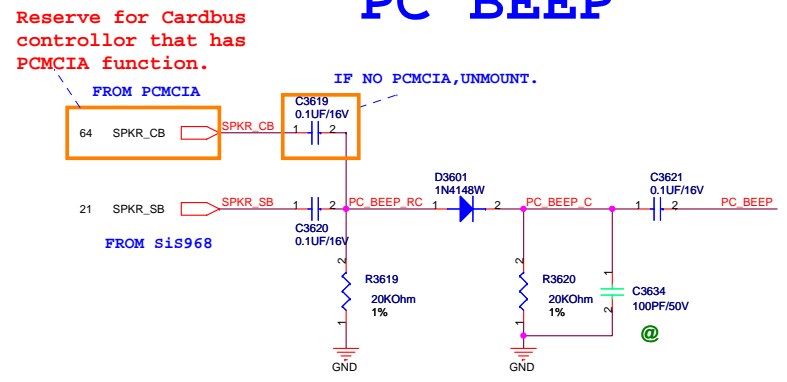
+5VS \rightarrow +5VS 21,30,32,37,38,45,50,51,56,57,80,91
 +5V_AUDIO \rightarrow +5V_AUDIO 38

AUDIO POWER

CODEC ALC660 REV:D



PC BEEP



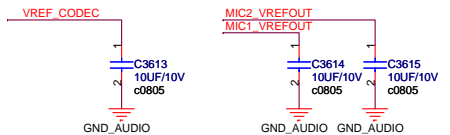
FROM S1996

Reserve for Cardbus controller that has PCMCIA function.

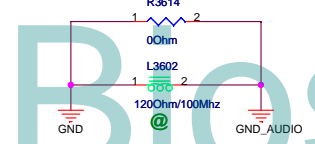
FROM PCMCIA

IF NO PCMCIA, UNMOUNT.

FROM S1998

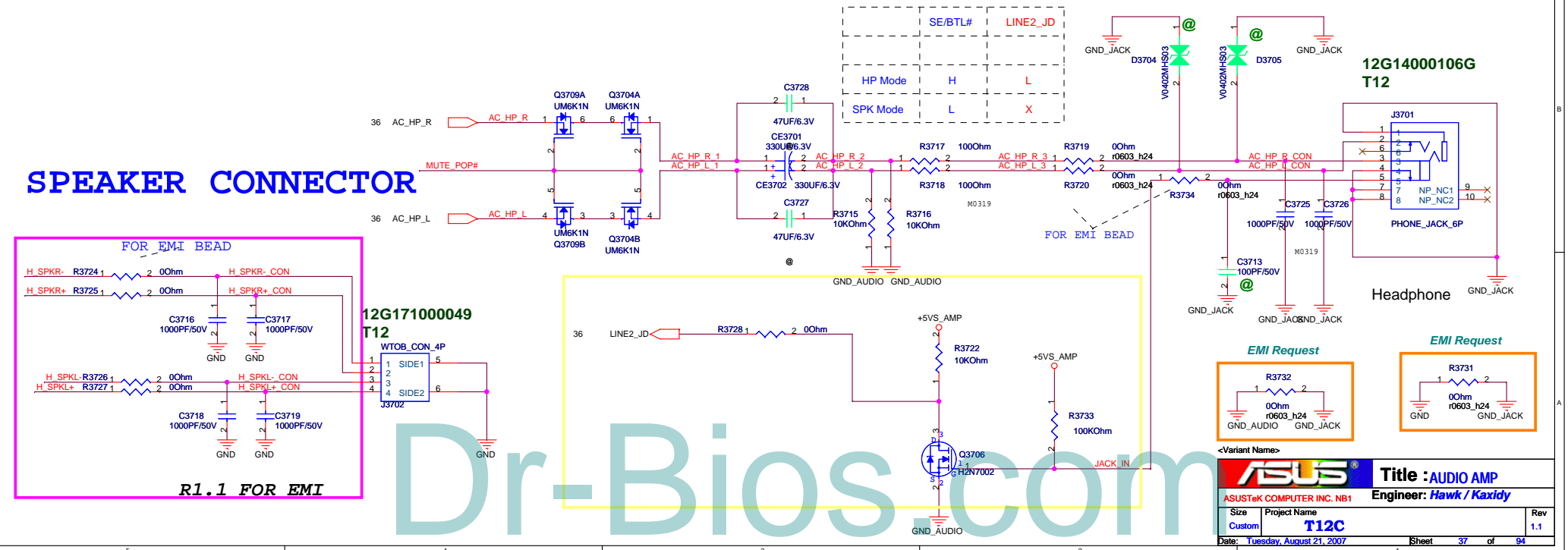
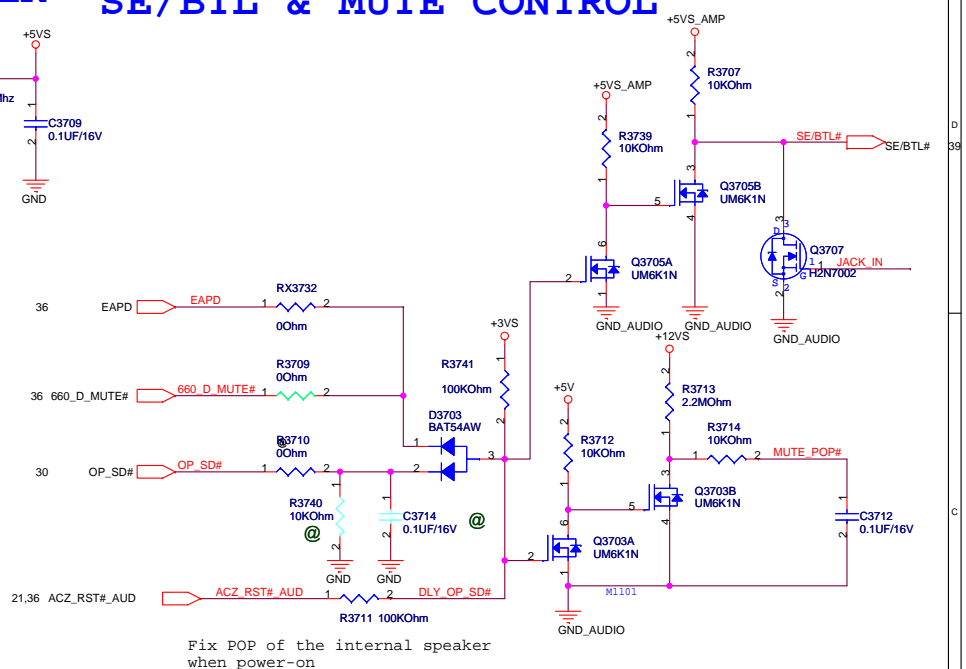
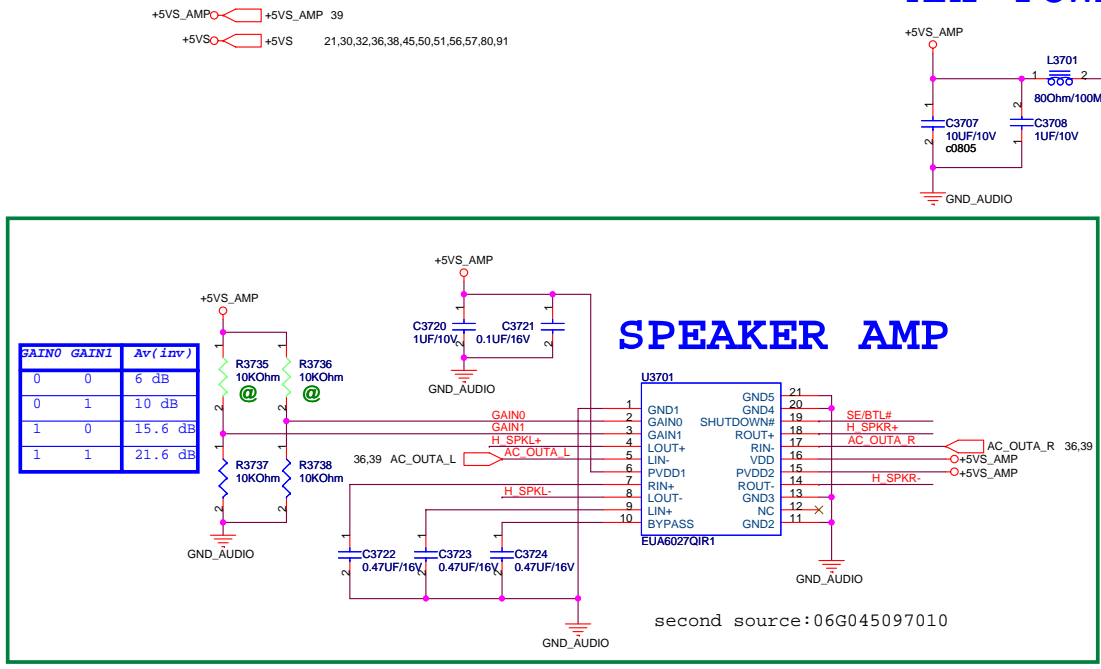


For EMI



Input impedance: 64K ohm (Typical)

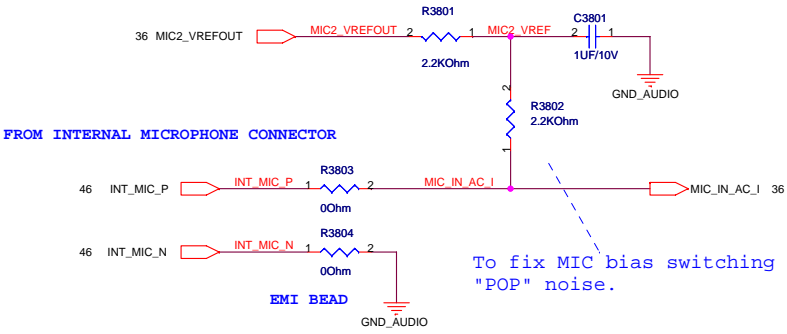
AMP POWER SE/BTL & MUTE CONTROL



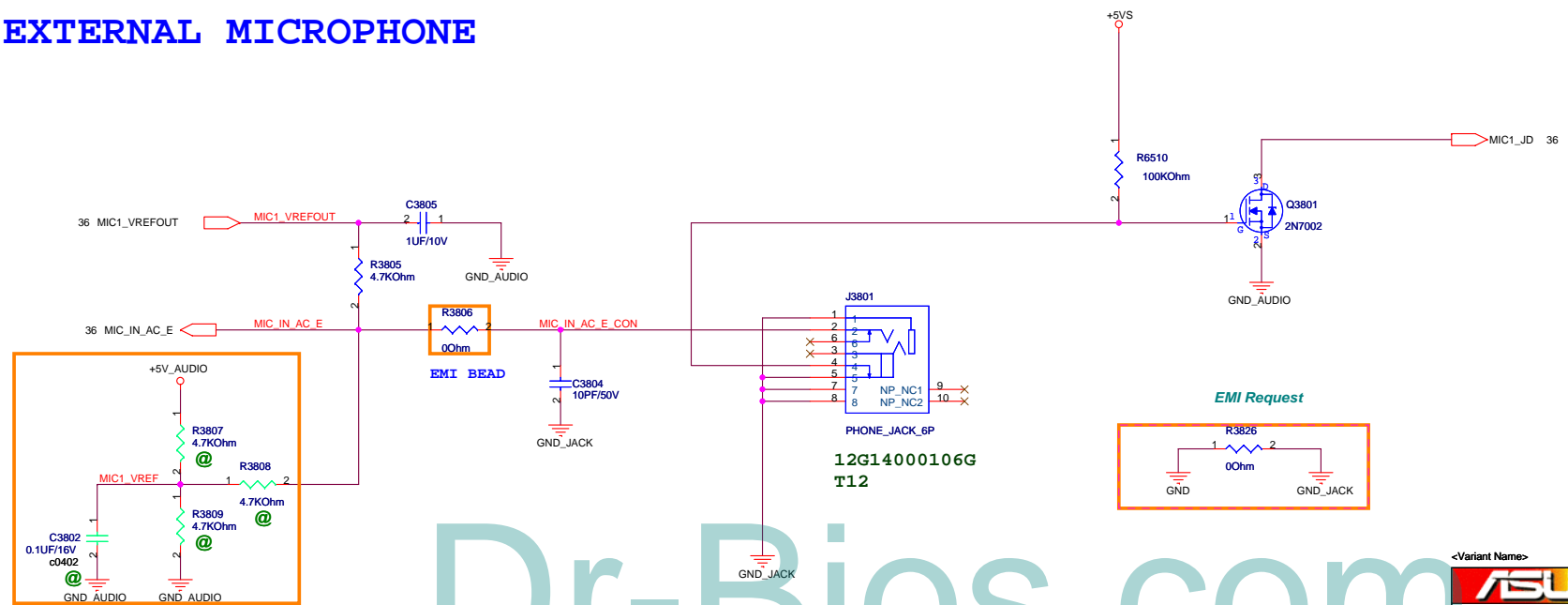
Dr-Bios.com

INTERNAL MICROPHONE

+5V_AUDIO ○ +5V_AUDIO 36
 +5VS ○ +5VS 21,30,32,36,37,45,50,51,56,57,80,91



EXTERNAL MICROPHONE

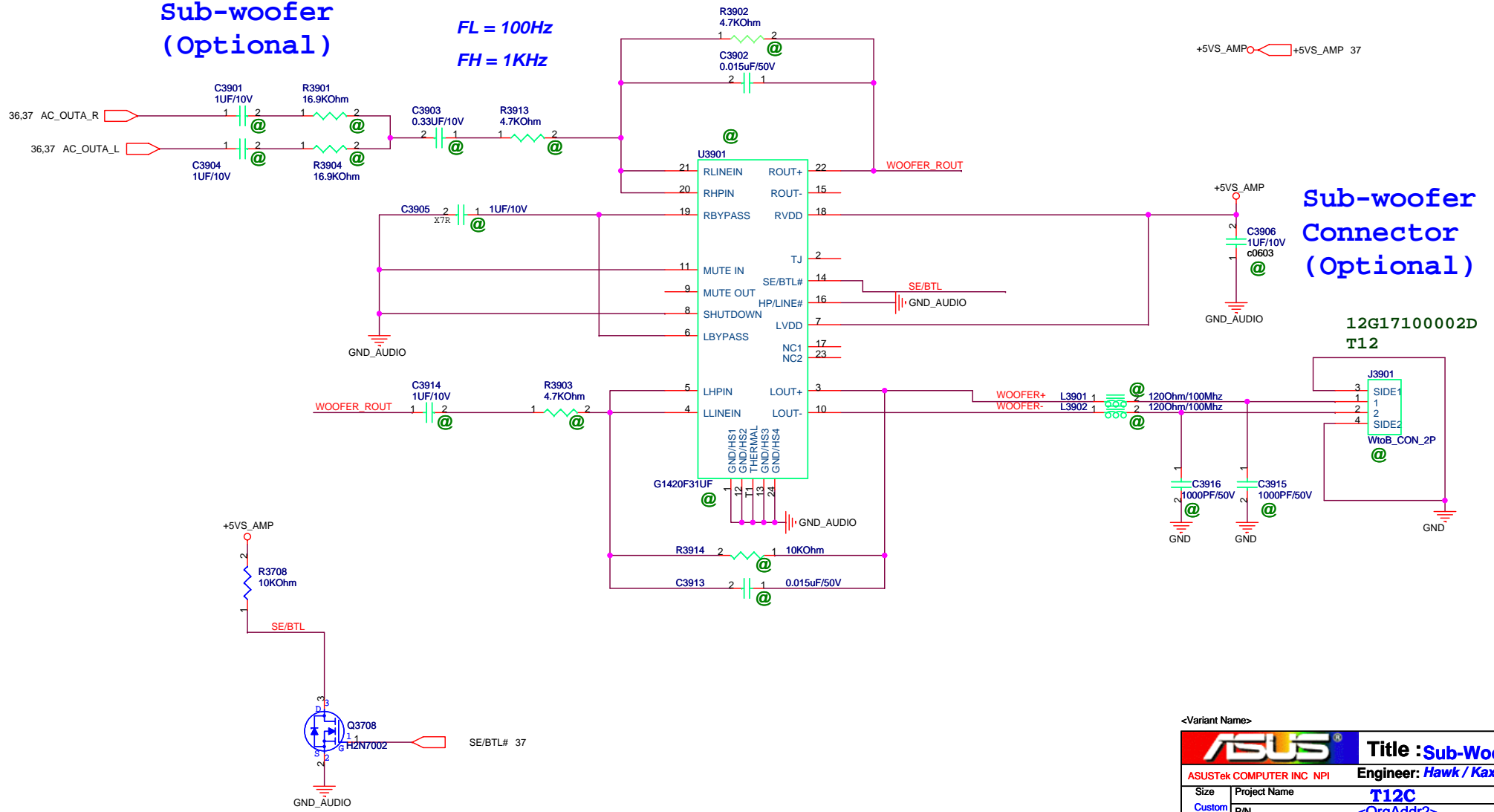


Reserved the external MIC bias(T filter).

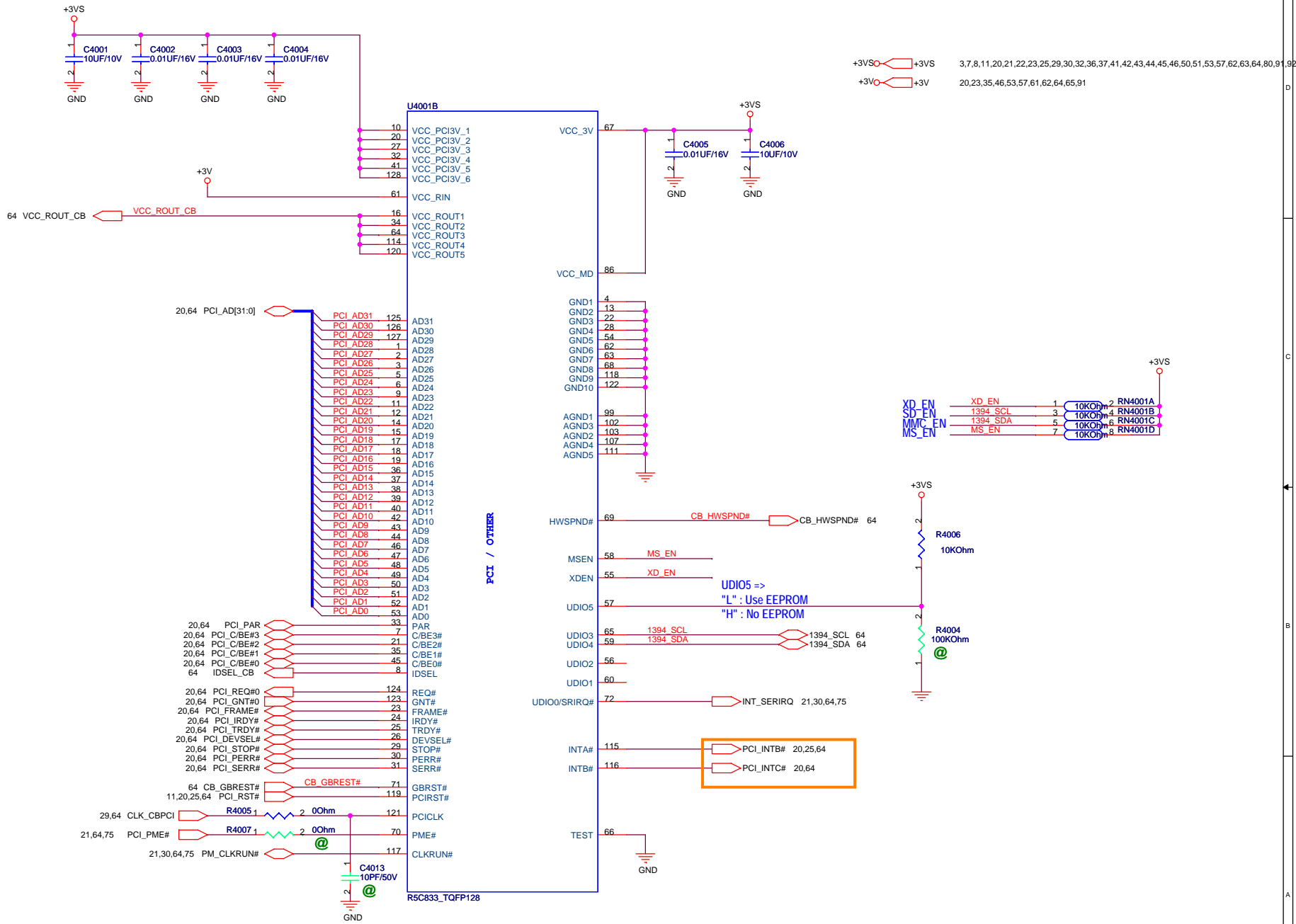
Dr-Bios.com

Sub-woofer (Optional)

FL = 100Hz
FH = 1KHz



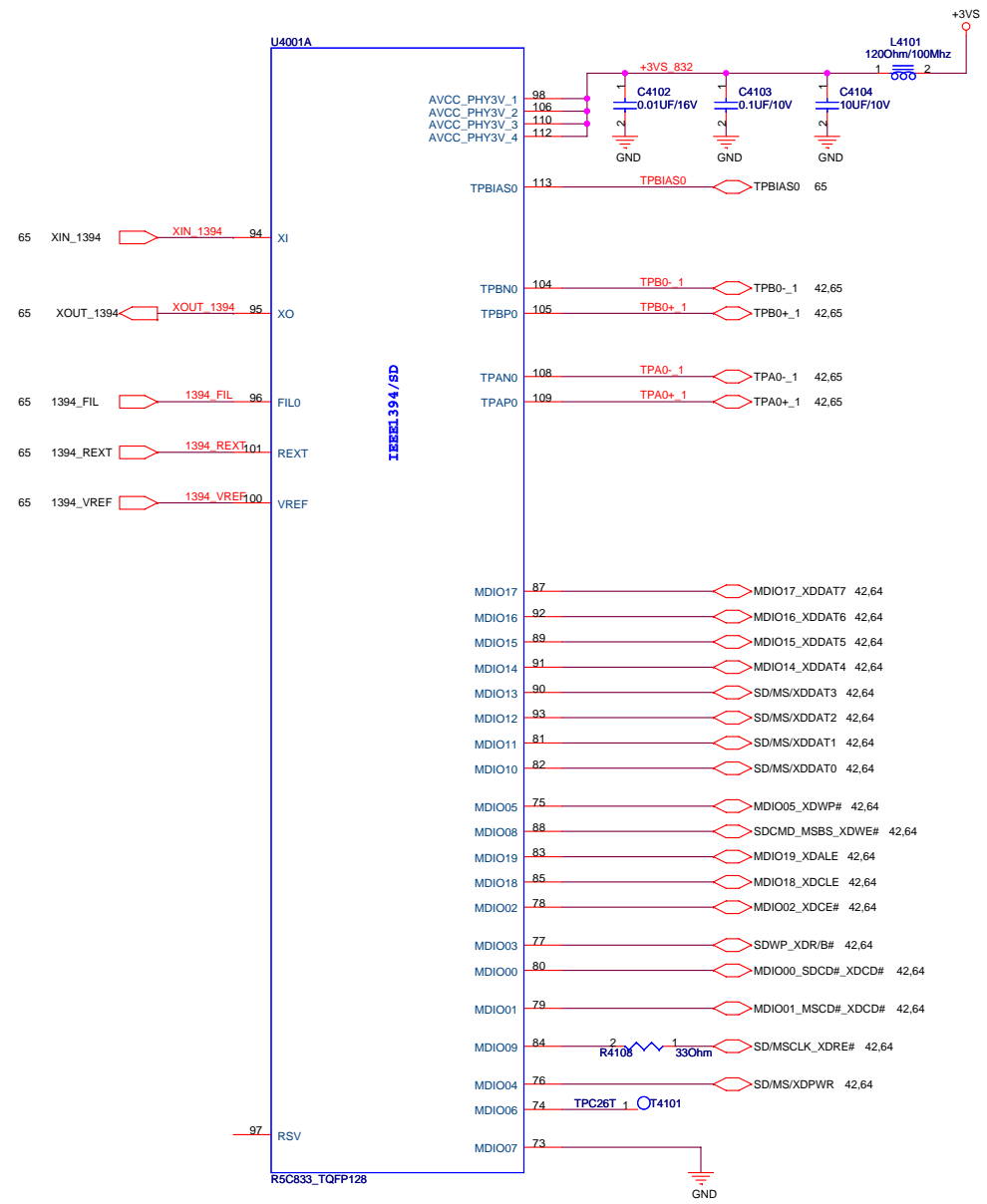
ASUS		Title : Sub-Woofier	
ASUSTek COMPUTER INC NPI		Engineer: Hawk / Kaxidy	
Size	Project Name	T12C	Rev
Custom	P/N	<OrgAddr2>	1.1
Date: Friday, August 17, 2007		Sheet 39 of 94	



Dr-Bios.com

<Variant Name>

ASUS		Title : CARDBUS R5C832 (1)	
ASUSTek COMPUTER INC		Engineer: Arthur & Bruce	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Tuesday, March 04, 2008	Sheet	40	of 94



+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92

```

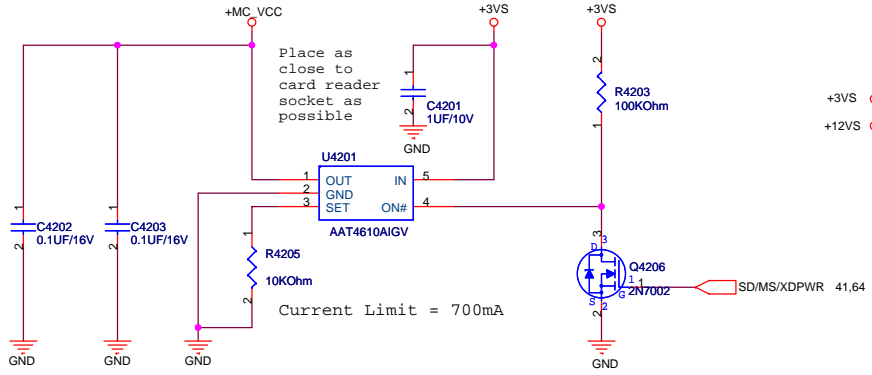
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
           MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
  
```

```

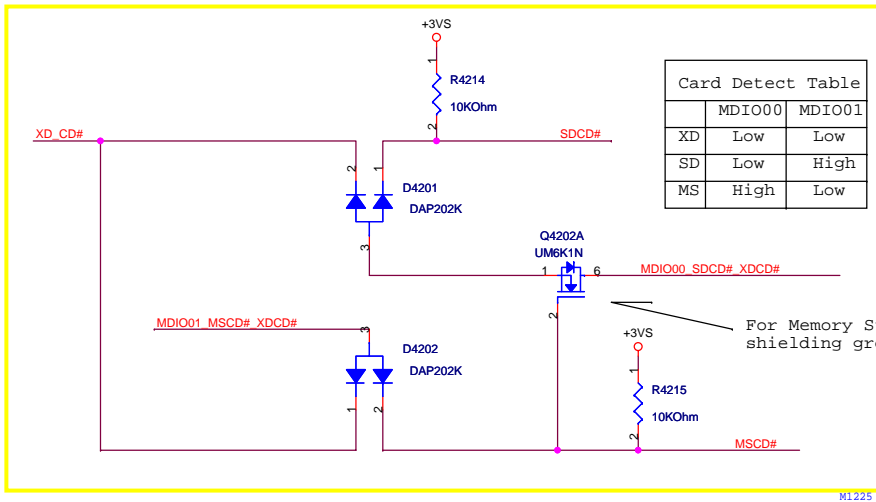
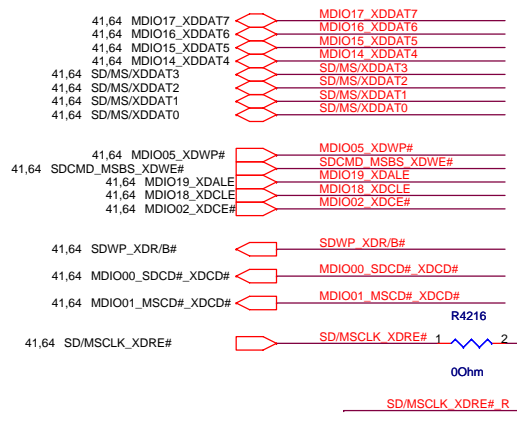
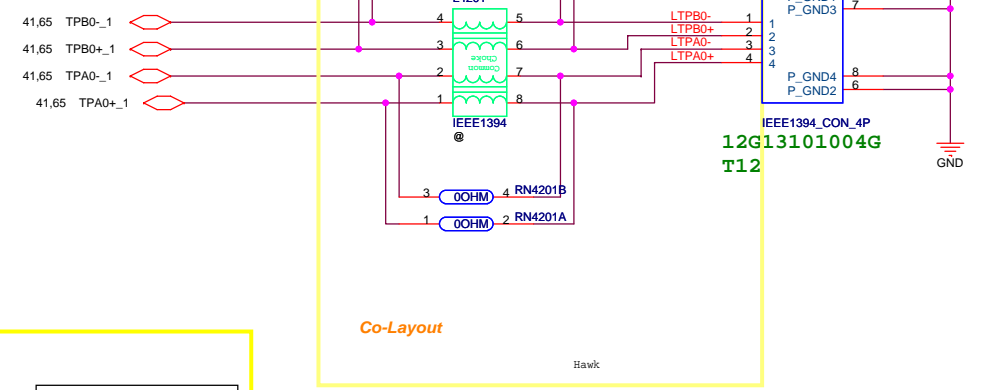
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
  
```

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<Variant Name>		ASUS		Title: R5C832 (2)	
ASUSTeK COMPUTER INC		Engineer: Arthur & Bruce			
Size: Custom	Project Name: T12C			Rev: 1.1	
Date: Friday, August 17, 2007	Sheet: 41	of 94			



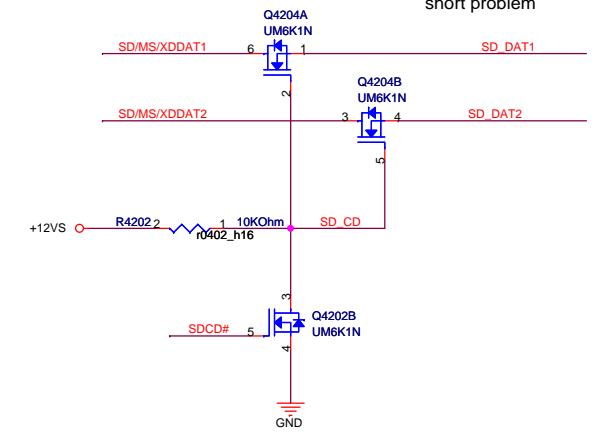
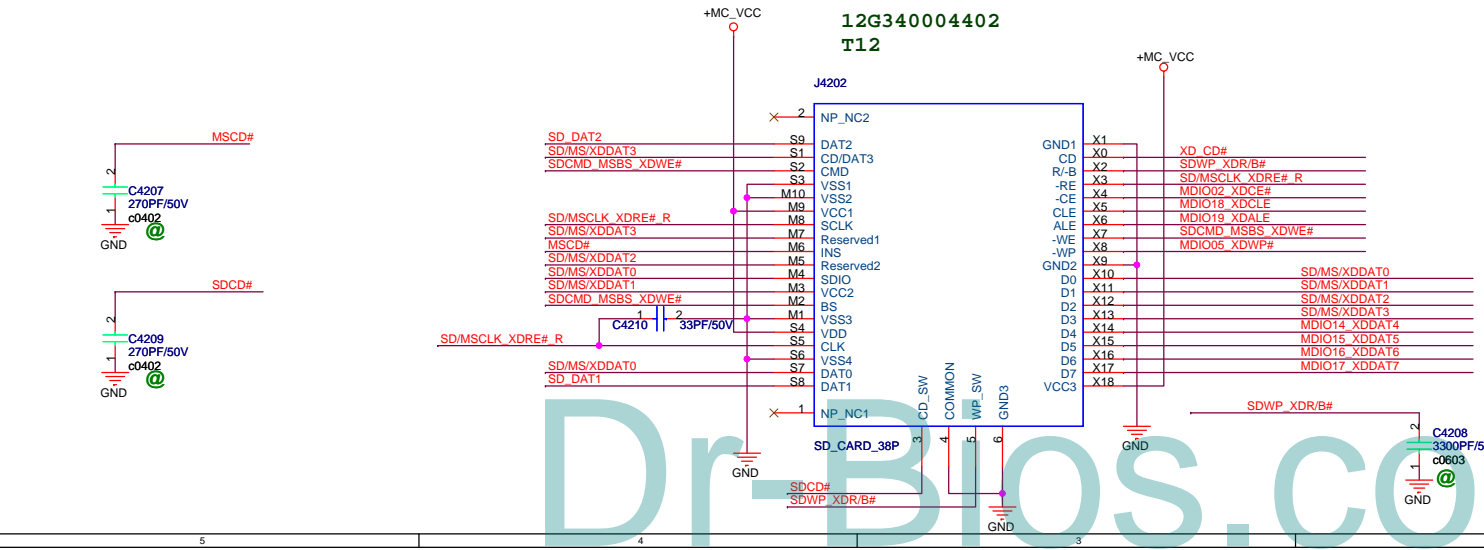
+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,43,44,45,46,50,51,53,57,62,63,64,80,91,92
 +12VS 37,46,83,91



Co-Layout

Hawk

Solve MS Duo Adaptor short problem



<Variant Name>

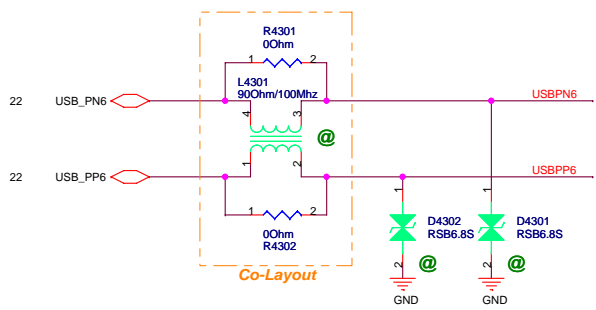
Title : 1394 & CardReader CON

ASUSTek COMPUTER INC Engineer: Arthur & Bruce

Size	Project Name	Rev
Custom	T12C	1.1

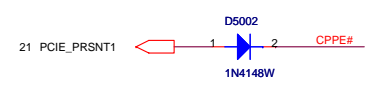
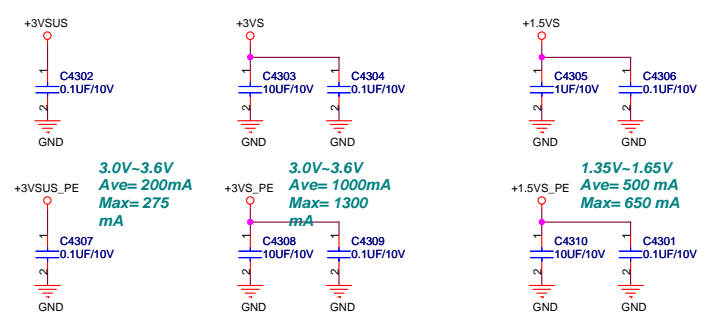
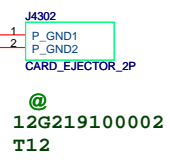
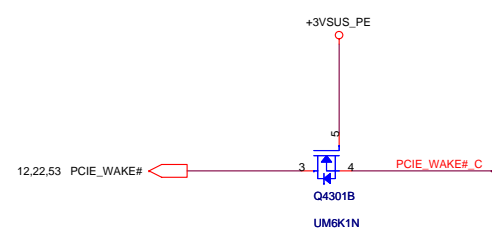
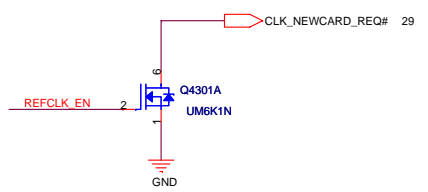
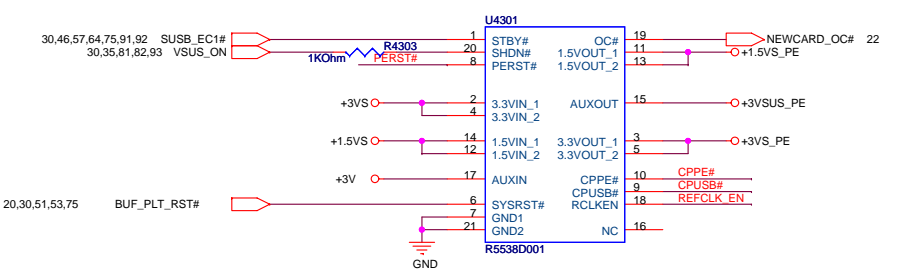
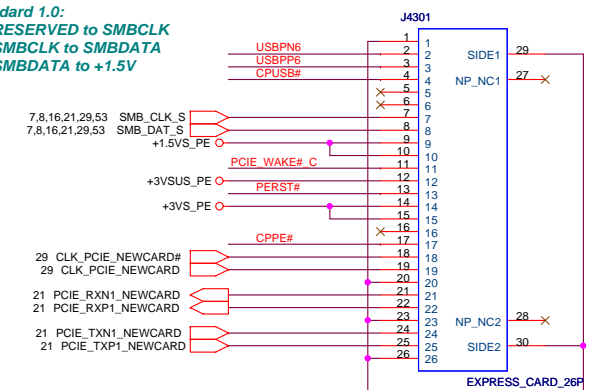
Date: Friday, March 07, 2008 Sheet 42 of 94

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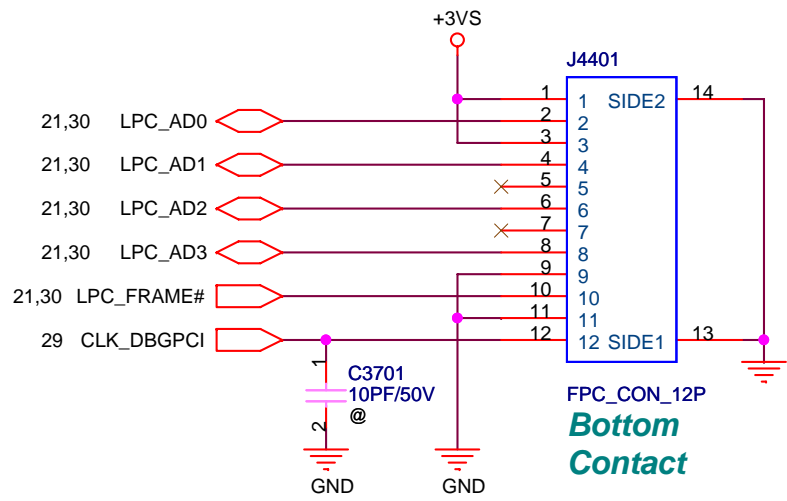
!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

NewCard Header



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ASUS		Title : NEWCARD	
ASUSTeK COMPUTER INC. ETD		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Tuesday, March 11, 2008	Sheet	43	of 94

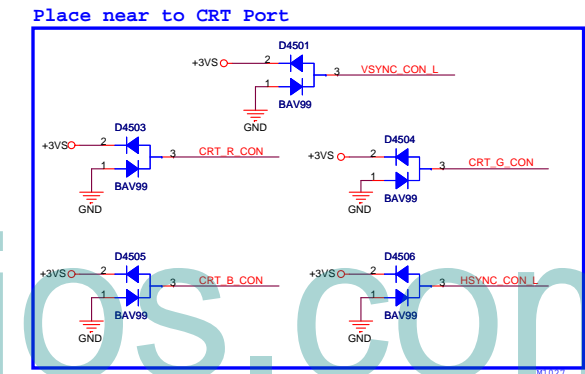
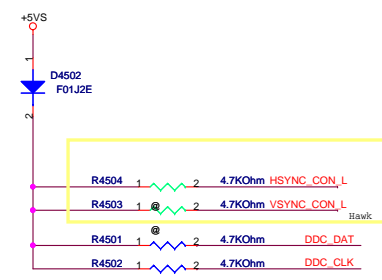
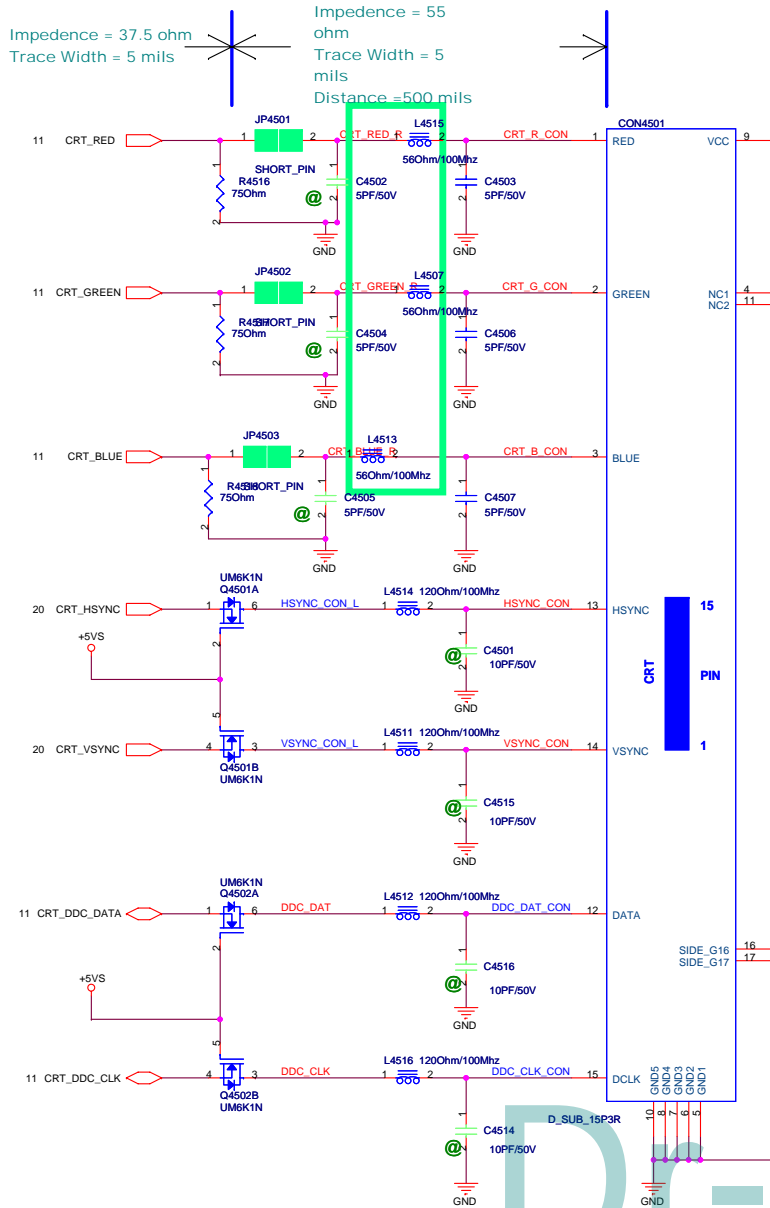


<Variant Name>

		Title :DEBUG	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>	
Size A	Project Name T12C	Rev 1.1	
Date: Tuesday, February 26, 2008		Sheet	44 of 94

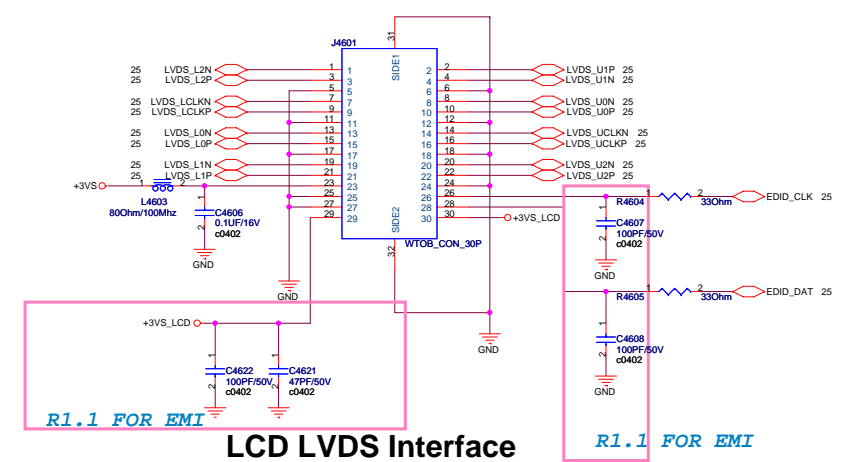
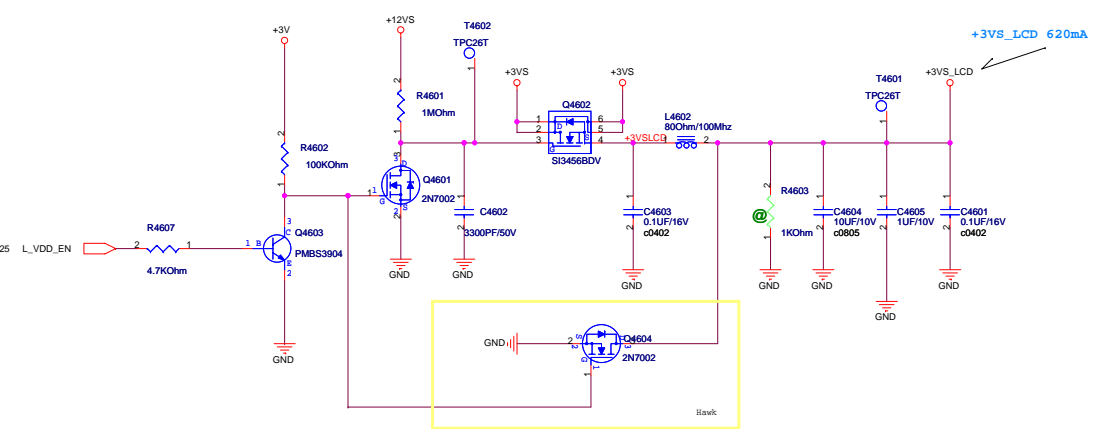
Dr-Bios.com

CRT Connector



+5VS 21,30,32,36,37,38,50,51,56,57,80,91
+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,46,50,51,53,57,62,63,64,80,91,92

Dr-Bios.com



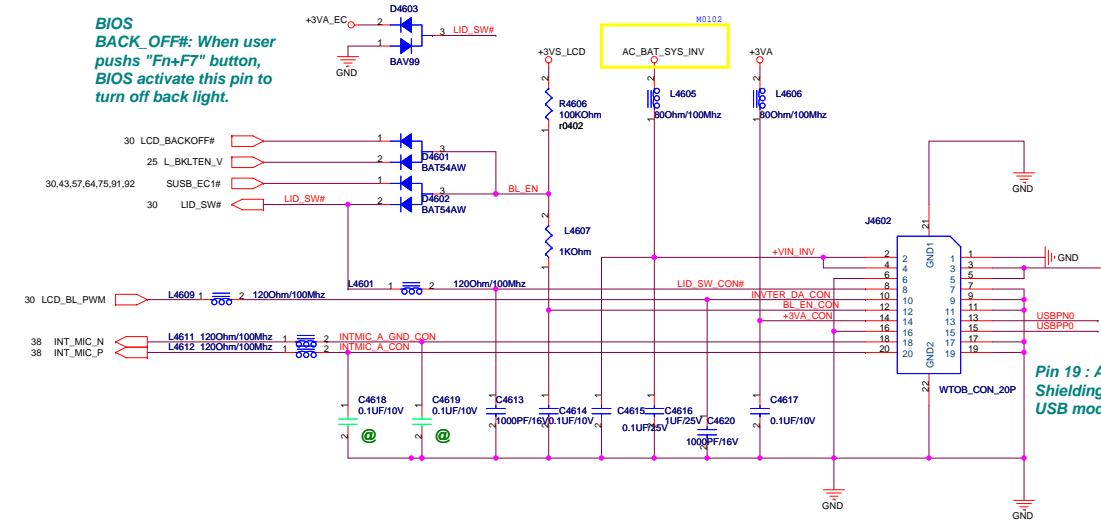
R1.1 FOR EMI

LCD LVDS Interface

R1.1 FOR EMI

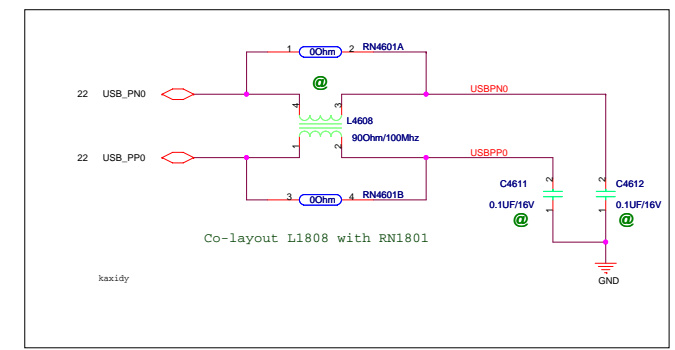
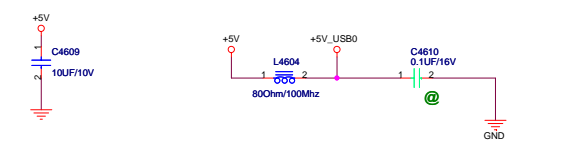
Layout note: close to connector

BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.



Digital Camera 150mA

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.




Co-layout L1808 with RN1801

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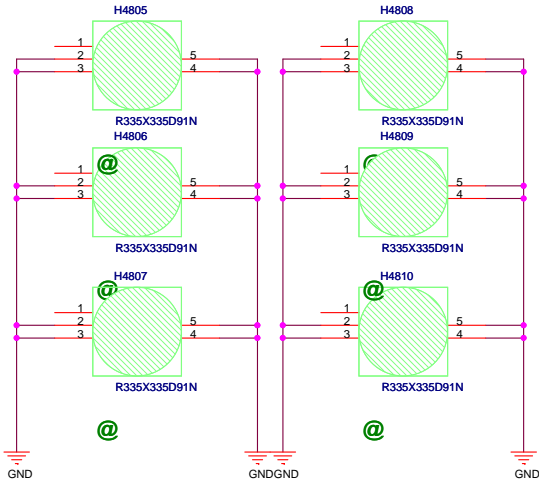


Dr-Bios.com

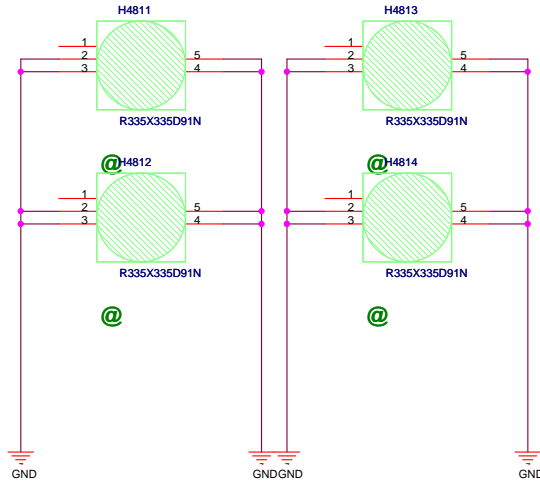
<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	47 of 94
			1

A Hole / TOP Side



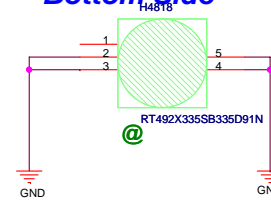
A Hole / Bottom Side



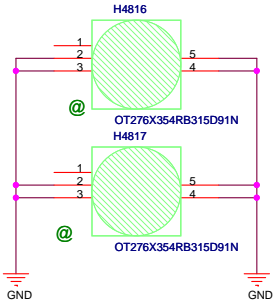
Drill Hole for Fix



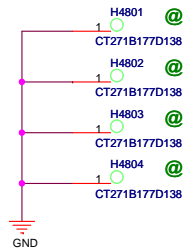
A Hole Special / Bottom Side



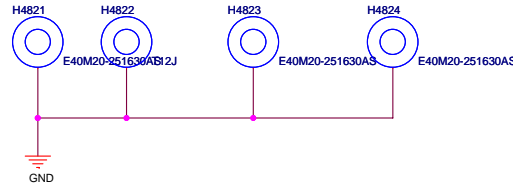
E Hole for Main board fix



F Hole for CPU



銅柱 Hole for VGA 13GNJ510M170-1




Dr-Bios.com

ASUS		Title :SREW HOLE	
ASUSTek COMPUTER INC NPI		Engineer: Hawk / Kaxidy	
Size	Project Name	T12C	Rev
Custom	P/N	<OrgAddr2>	1.1
Date: Monday, August 13, 2007		Sheet	48 of 94

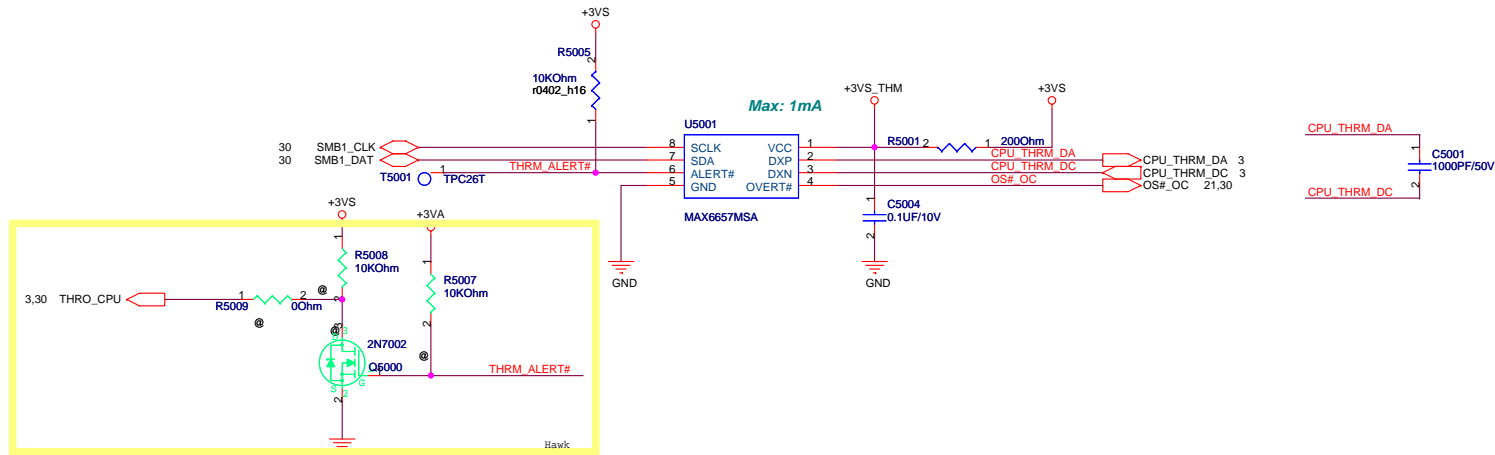


Dr-Bios.com

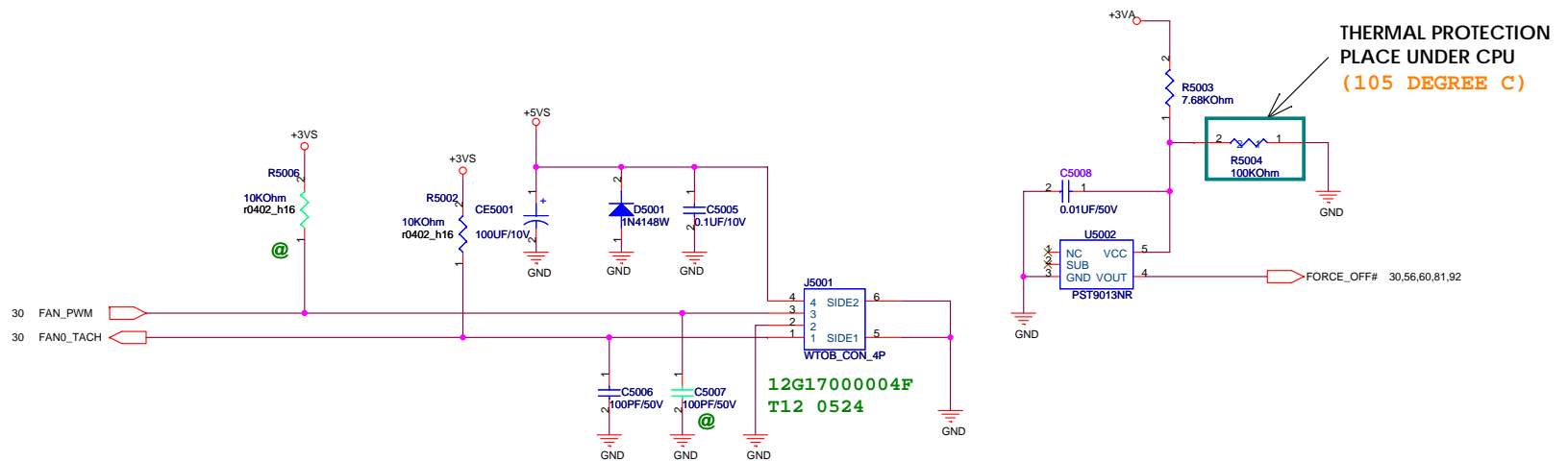
<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: <i>Monday, August 13, 2007</i>		Sheet	49 of 94
			1

Thermal Sensor



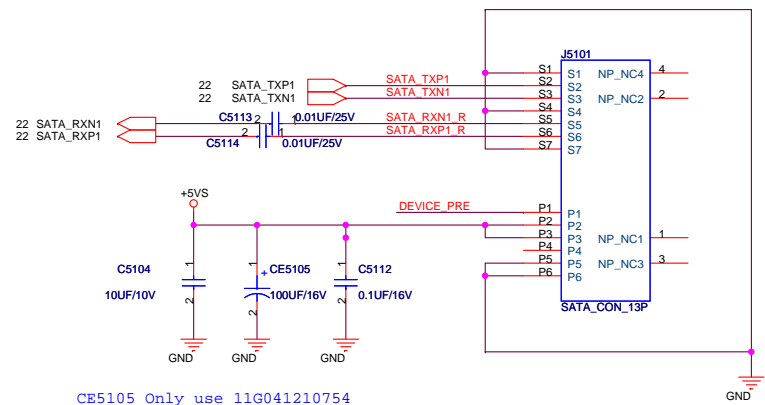
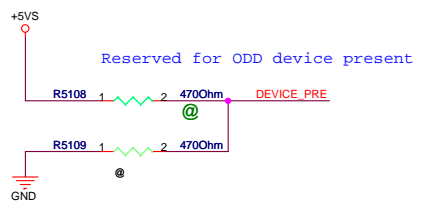
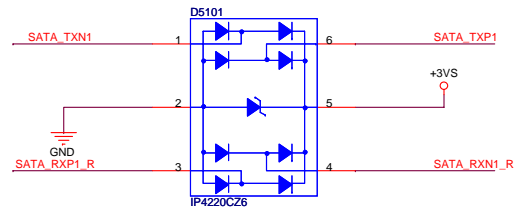
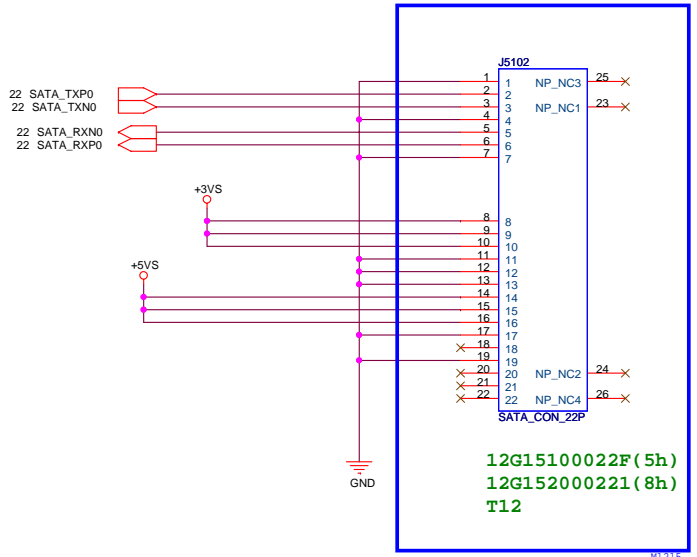
DC FAN Control



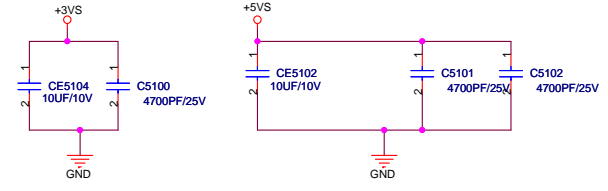
Dr-Bios.com

SATA HDD

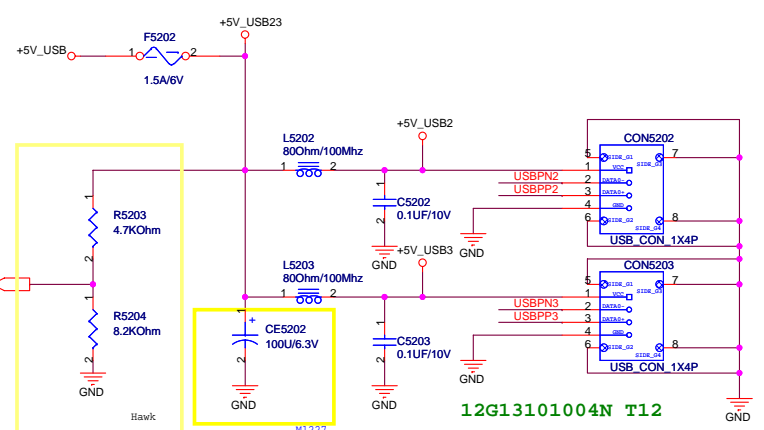
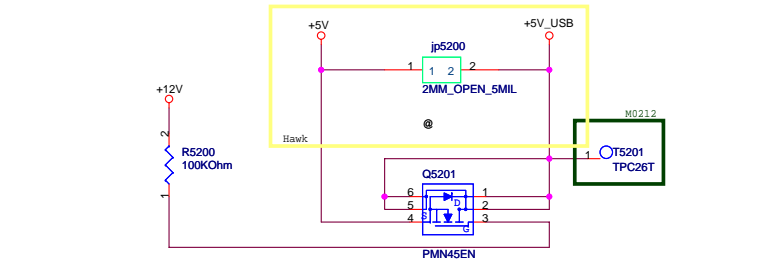
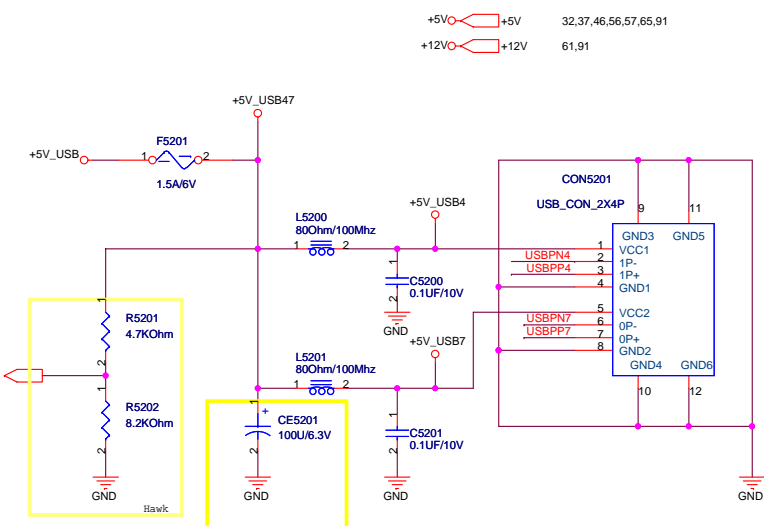
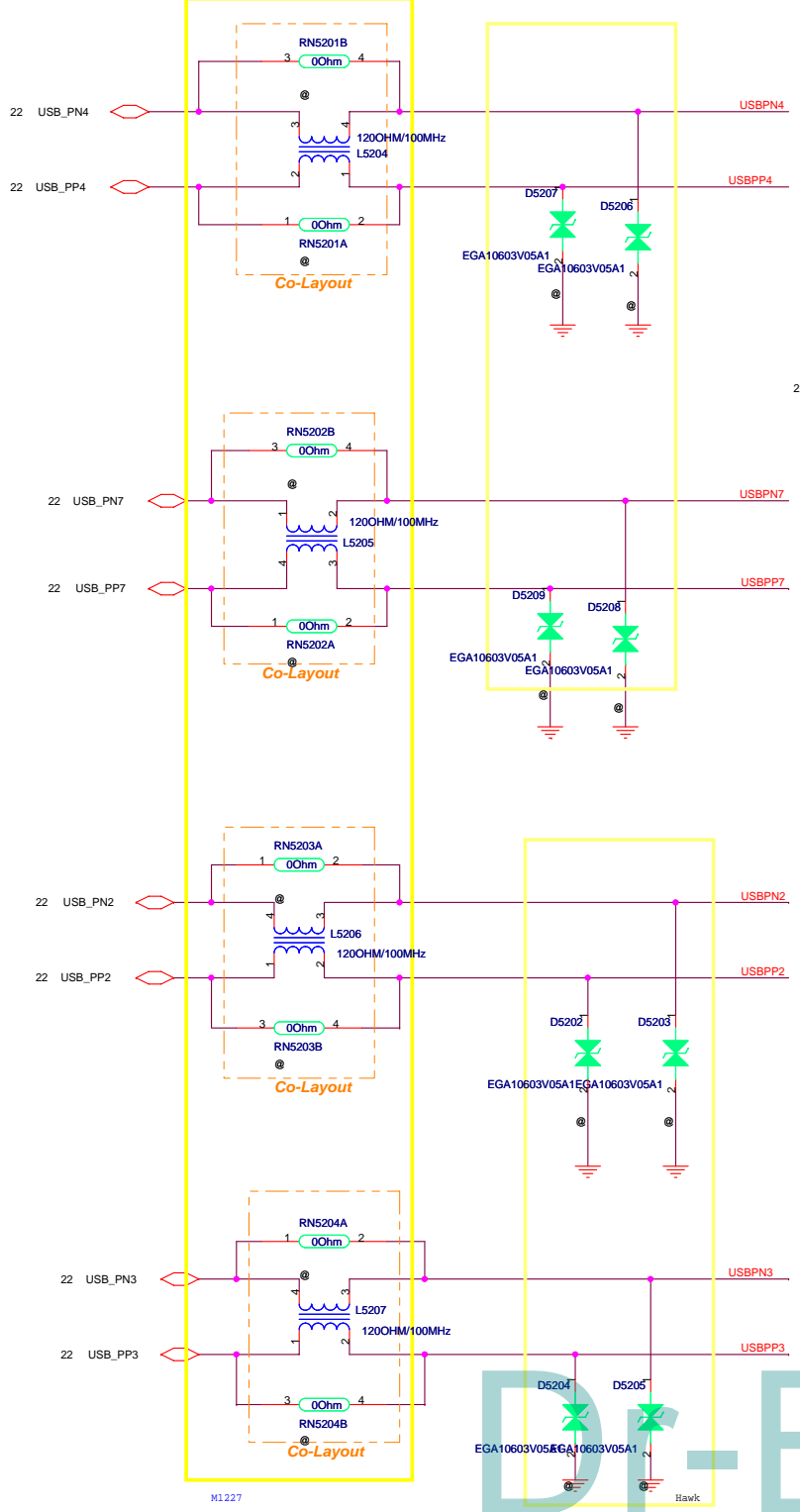
+3VS +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,53,57,62,63,64,80,91,92
 +5VS +5VS 21,30,32,36,37,38,45,50,56,57,80,91



CE5105 Only use 11G041210754



Dr-Bios.com

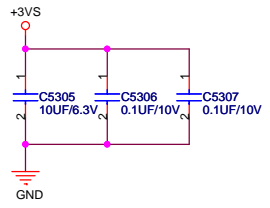
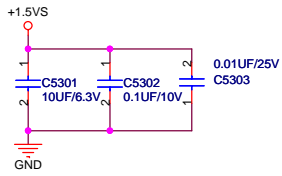


+5V 32,37,46,56,57,65,91
+12V 61,91

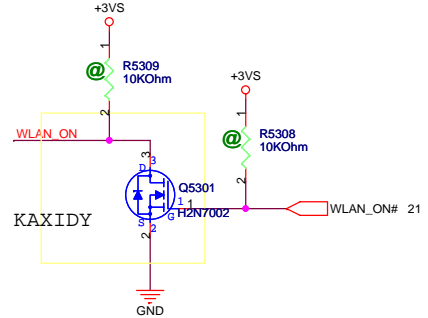
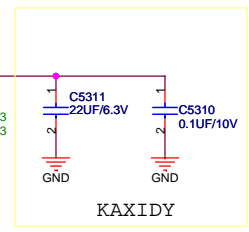
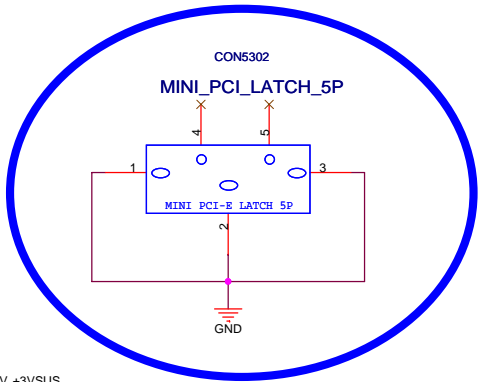
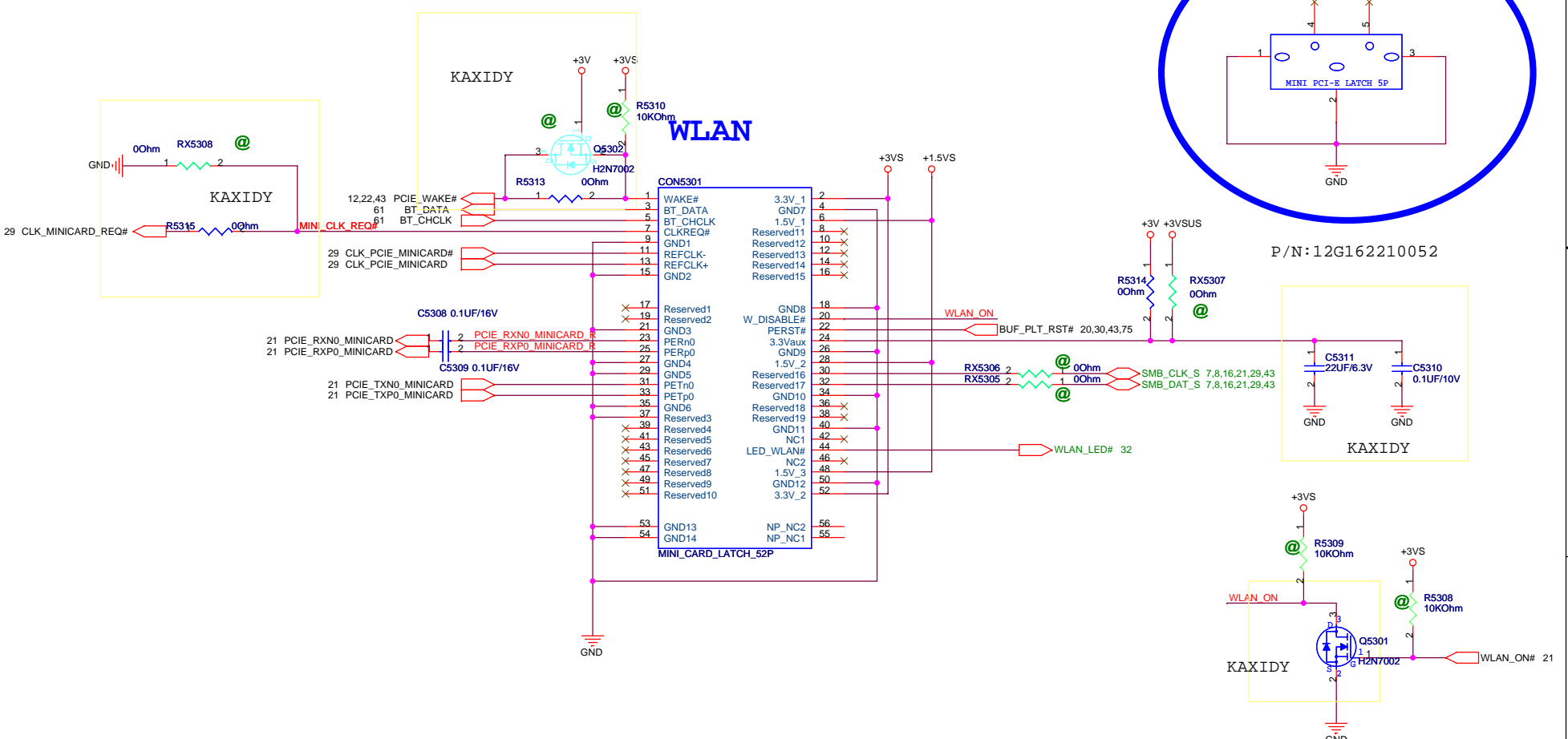
12G13101004N T12

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ASUS		Title :USB CONN X 4	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Friday, August 17, 2007	Sheet	52	of 94



+3VS	+3VS	3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,57,62,63,64,80,91,92
+3V	+3V	20,23,35,40,46,57,61,62,64,65,91
+1.5VS	+1.5VS	4,11,43,57,83




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<Variant Name>		ASUS Title : MINICARD	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Friday, March 07, 2008		Sheet	53 of 94




<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: <i>Monday, August 13, 2007</i>		Sheet	54 of 94
			1

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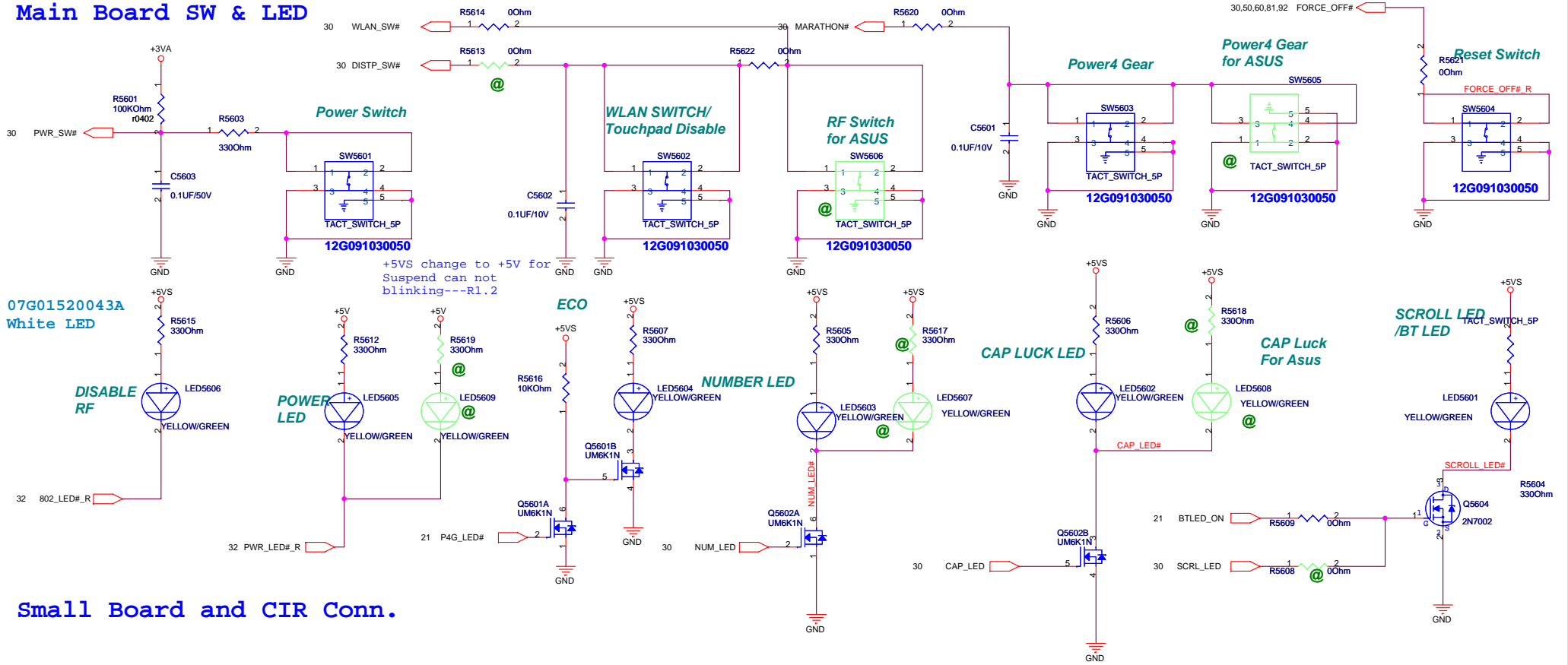
<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: <i>Monday, August 13, 2007</i>		Sheet	55 of 94

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+5V +5V 32,37,46,52,57,65,91
 +5VS +5VS 21,30,32,36,37,38,45,50,51,57,80,91
 +3VA +3VA 21,30,46,50,57,81,93

Main Board SW & LED









Small Board and CIR Conn.

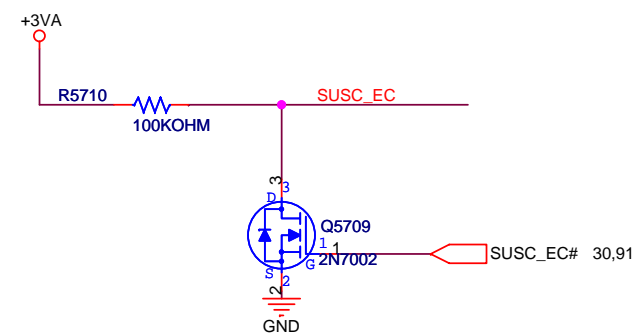
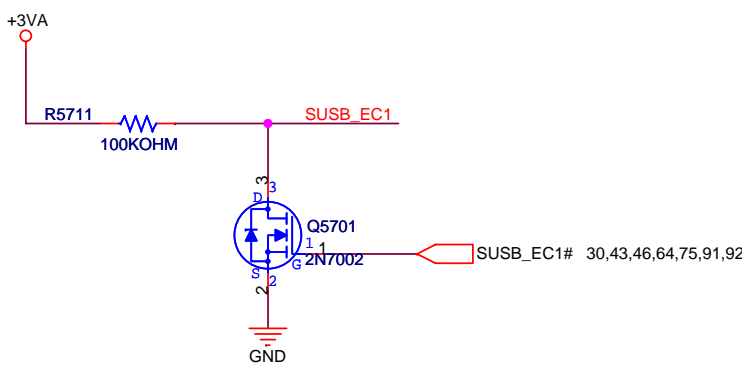
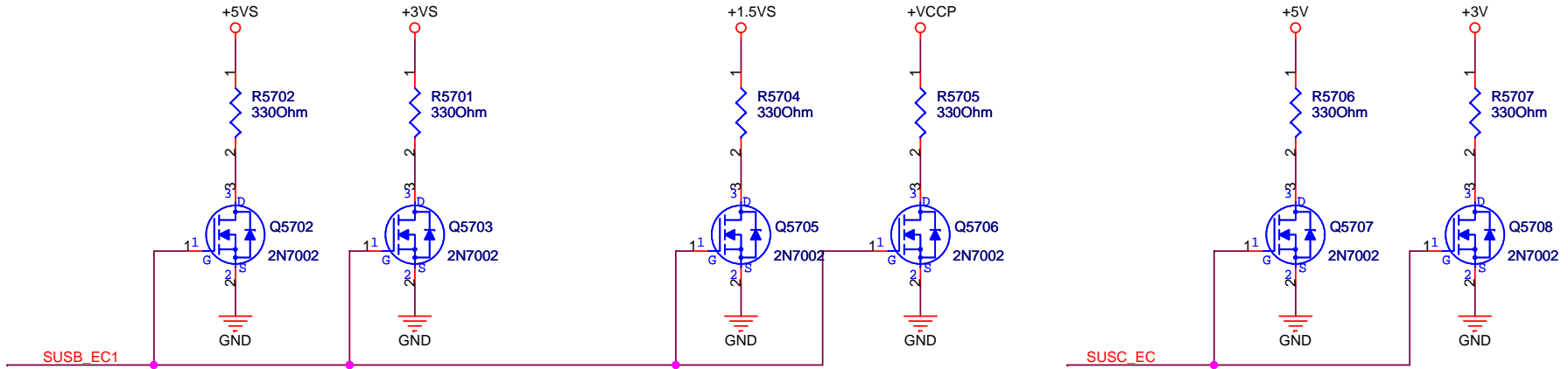
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<Variant Name>

ASUS Title : LED/SWITCH
 ASUSTek COMPUTER INC Engineer: Hawk / Kaxidy

Size	Project Name	Rev
Custom	T12C	1.1
Date: Friday, March 07, 2008	Sheet	56 of 94

- +3V  +3V 20,23,35,40,46,53,61,62,64,65,91
- +5V  +5V 32,37,46,52,56,65,91
- +VCCP  +VCCP 4,10,14,21,23,29,83,92
- +1.5VS  +1.5VS 4,11,43,53,83
- +3VS  +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,62,63,64,80,91,92
- +5VS  +5VS 21,30,32,36,37,38,45,50,51,56,80,91




		Title :DISCHARGE	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>	
Size Custom	Project Name T12C		Rev 1.1
Date: Tuesday, March 04, 2008		Sheet	57 of 94

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<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 58 of 94

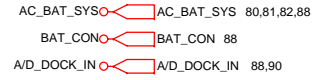
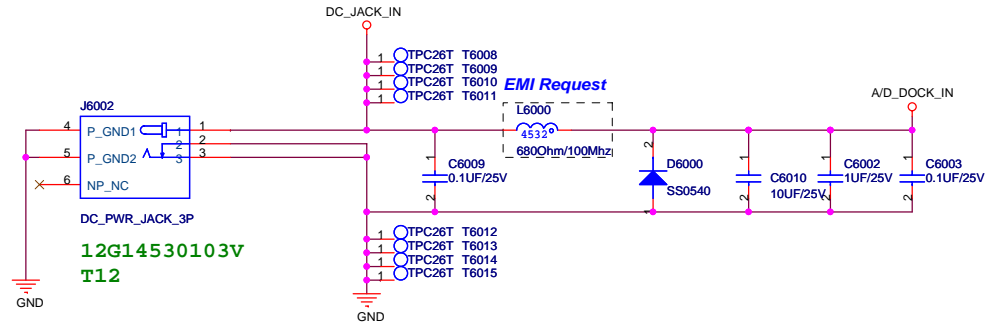


<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	59 of 94

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DC-IN



For Battery

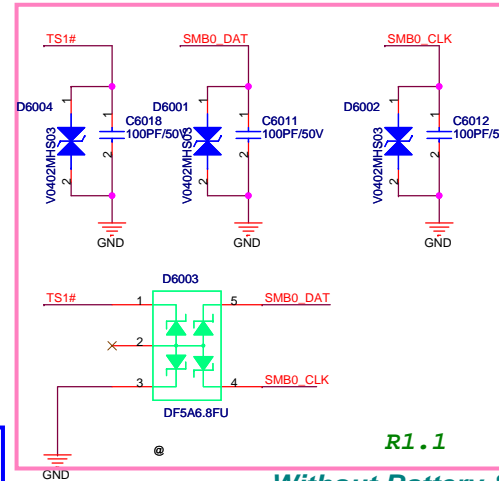
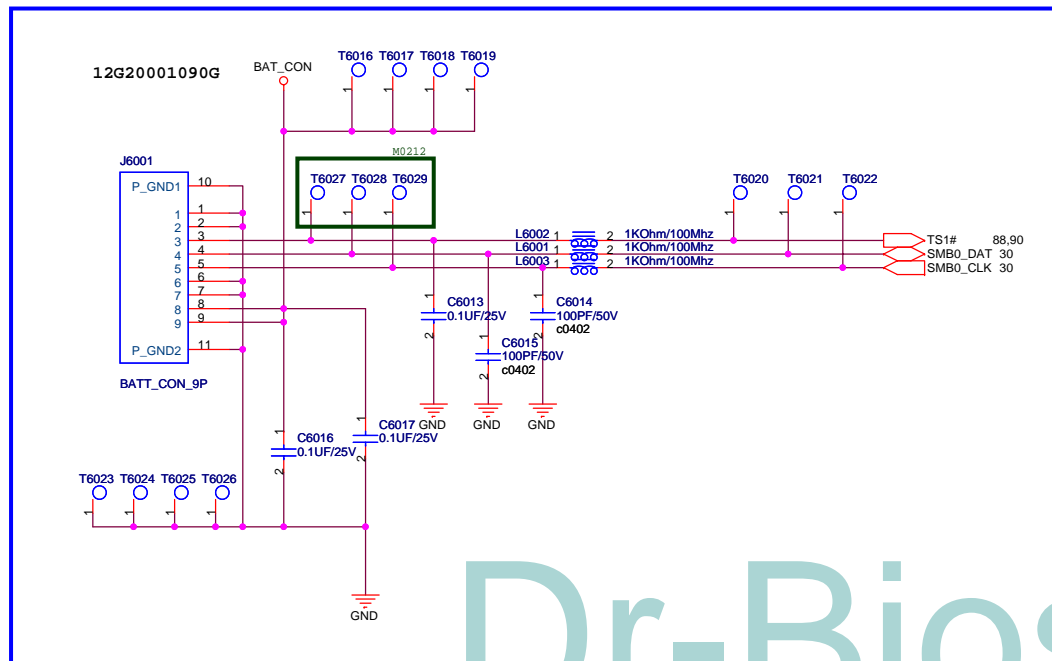
Single Battery

BAT1_CNT1#, BAT1_CNT2#,
 BAT2_CNT1#, BAT2_CNT2#
 don't connect to Battery
 Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
 BAT2_CNT1#, BAT2_CNT2#
 must connect to Battery
 Connector.

Battery Connector

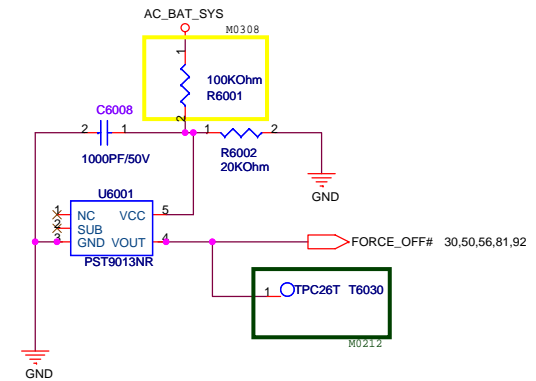


Note:

When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

Without Battery & Pull out Adapter

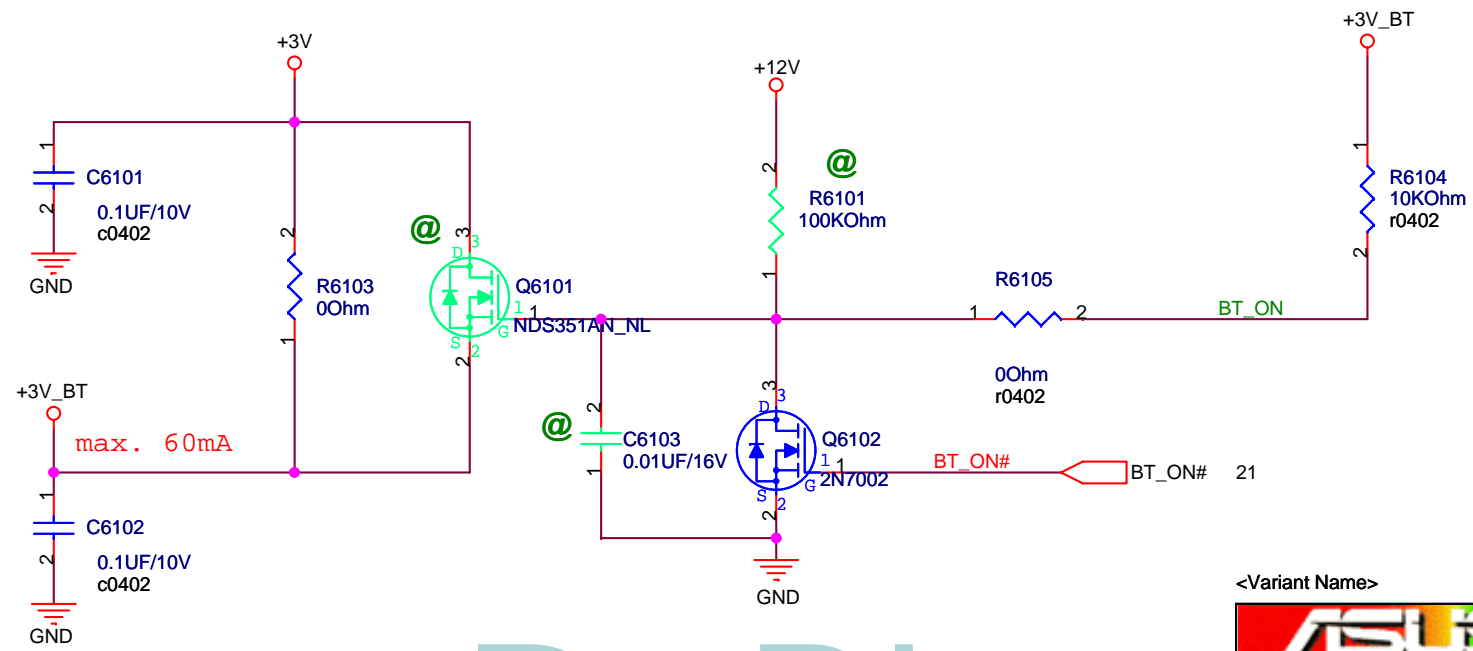
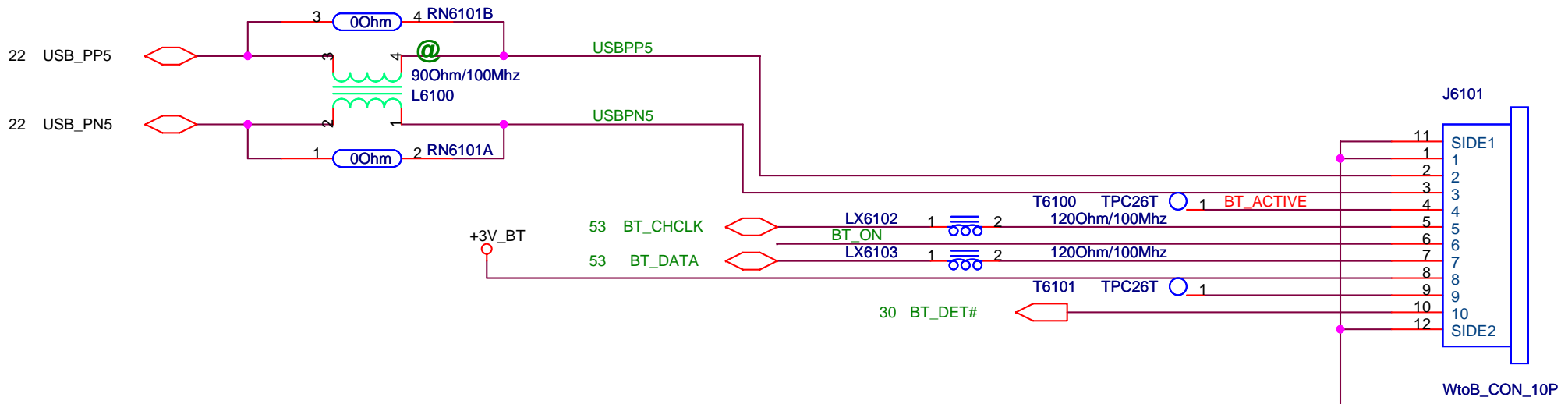


<Variant Name>

ASUS		Title : DCIN/Batt conn.	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Friday, August 17, 2007	Sheet	60	of 94

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BLUETOOTH CONNECTOR




<Variant Name>

		Title : Blue Tooth
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Friday, August 17, 2007		Sheet 61 of 94

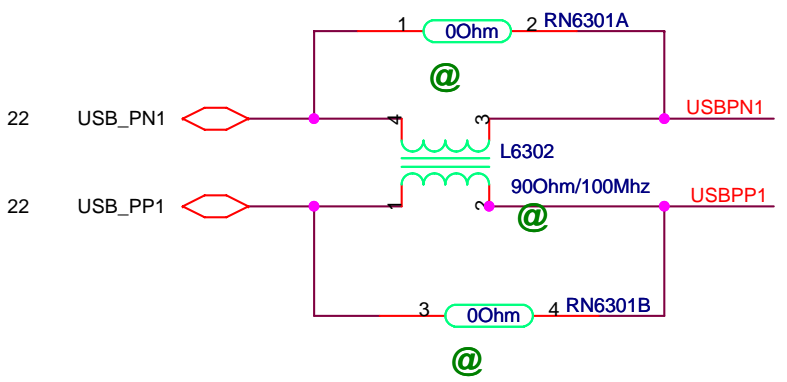
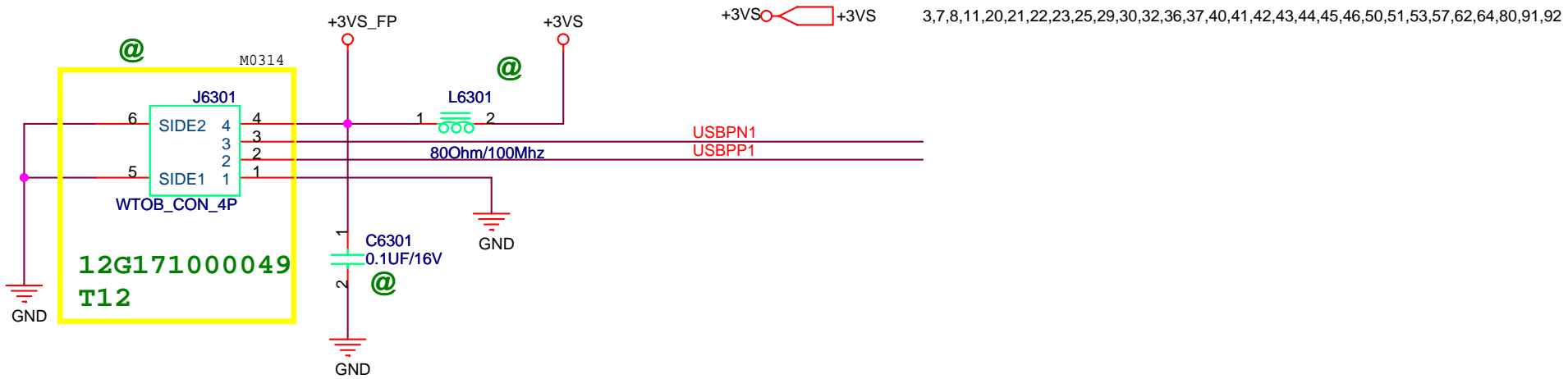
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TPM Connector

<Variant Name>

		Title : TPM
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
A	T12C	1.1
Date: Tuesday, March 04, 2008		Sheet 62 of 94

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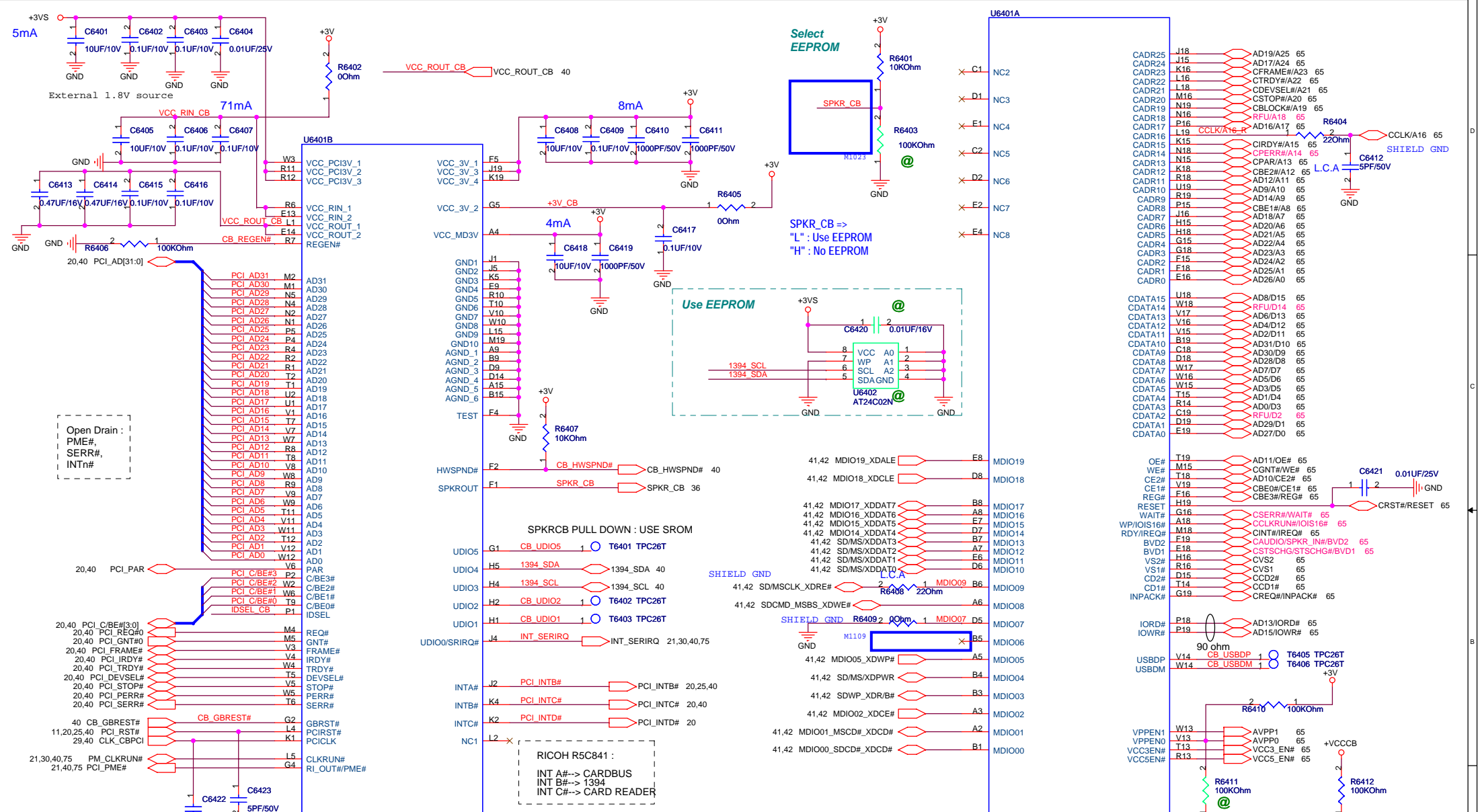


+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,64,80,91,92

<Variant Name>

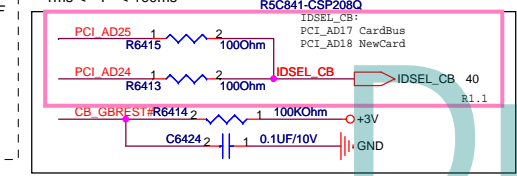
ASUS		Title :Finger Print	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>	
Size A	Project Name T12C	Rev 1.1	
Date: Friday, August 17, 2007		Sheet 63 of 94	

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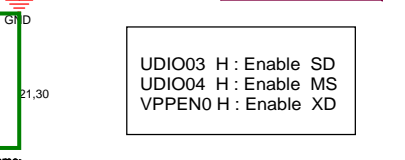
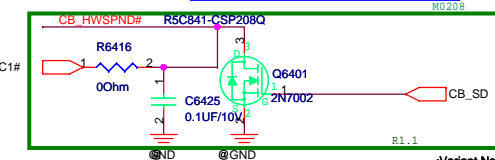


Open Drain :
PME#,
SERR#,
INTn#

VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC3EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F



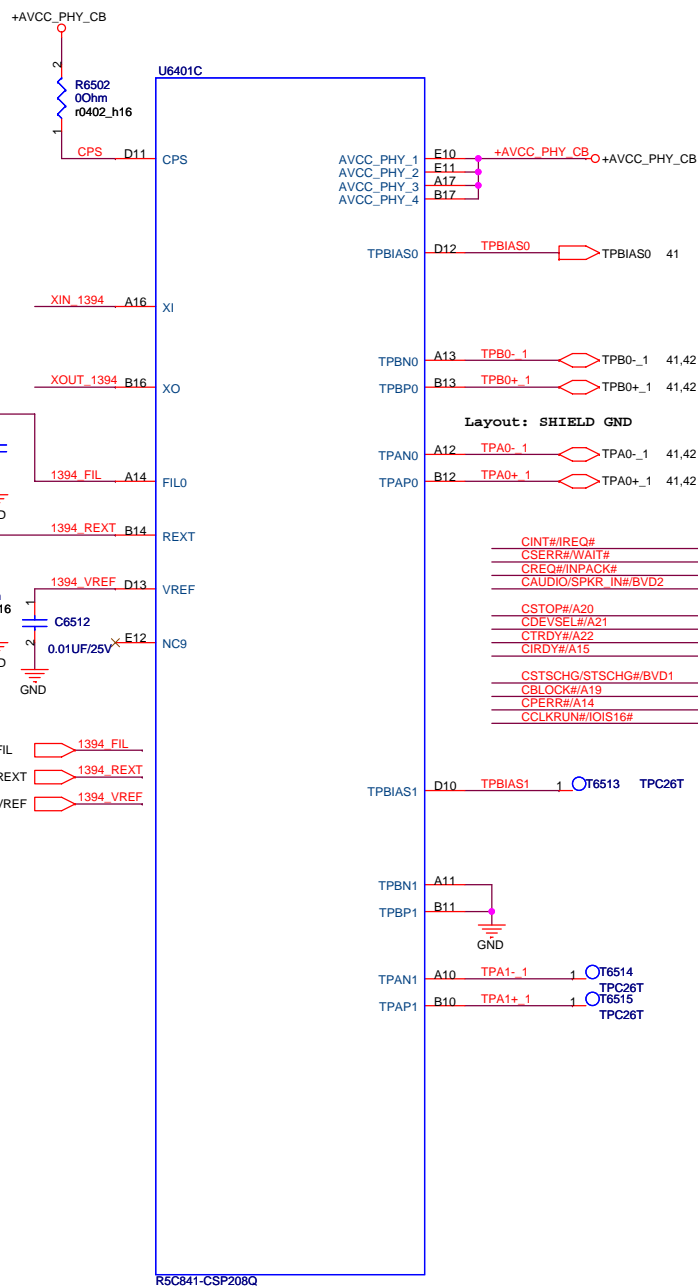
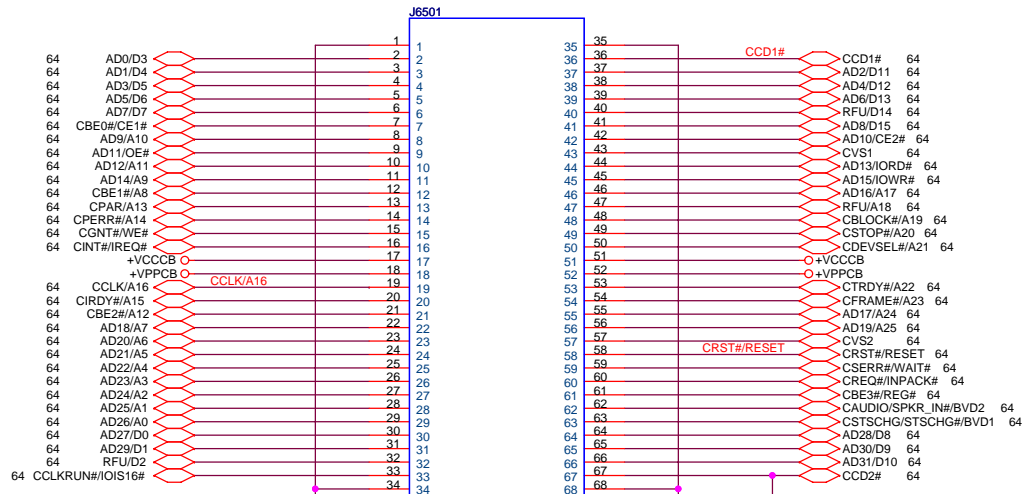
RICOH R5C841 :
INT A#-> CARDBUS
INT B#-> 1394
INT C#-> CARD READER



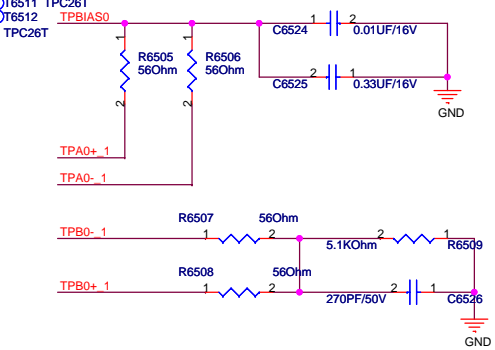
ASUS Title : **RICOH R5C841**
ASUSTek COMPUTER INC Engineer : **Hawk / Kaxidy**
Size Project Name
Custom **T12C**
Date: **Tuesday, March 04, 2008** Sheet **64** of **94**

PCMCIA SOCKET

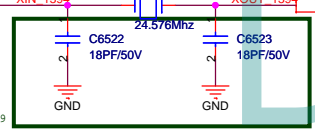
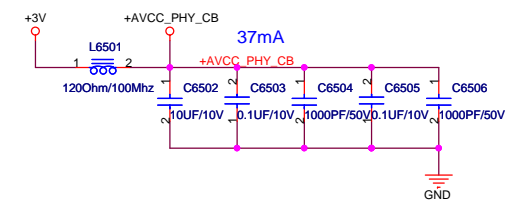
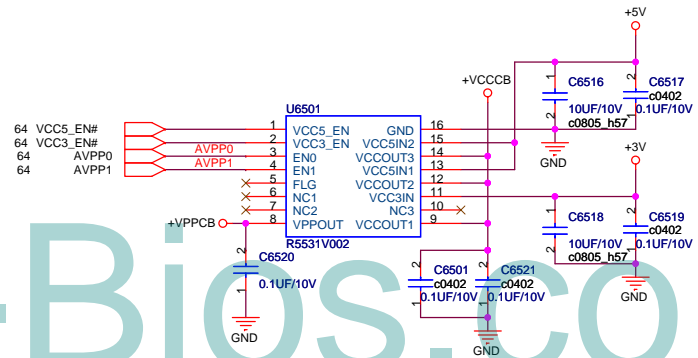
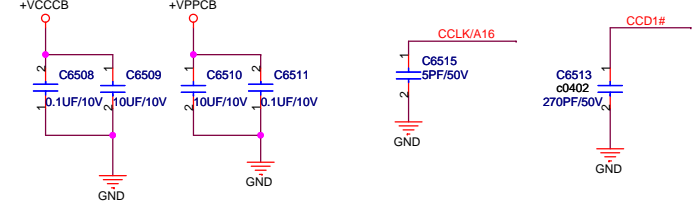
CCD1# CCD2#
L L 16bit
OTHER 32bit



- Layout: SHIELD GND
- CINT#/WREQ# 1 T6502 TPC26T
 - CSERR#/WAIT# 1 T6503 TPC26T
 - CREQ#/INPACK# 1 T6504 TPC26T
 - AUDIO/SPKR_IN#/BVD2 1 T6505 TPC26T
 - CSTOP#/A20 1 T6506 TPC26T
 - CDEVSEL#/A21 1 T6507 TPC26T
 - CTRDY#/A22 1 T6508 TPC26T
 - CIRDY#/A15 1 T6509 TPC26T
 - CSTSCHG#/STSCHG#/BVD1 1 T6501 TPC26T
 - CBLOCK#/A19 1 T6510 TPC26T
 - CPERR#/A14 1 T6511 TPC26T
 - CCLKRUN#/IOIS16# 1 T6512 TPC26T



12G160420683



ASUS Logo

Title: CARBUS SOCKET
Engineer: Hawk / Kaxidy

ASUSTeK COMPUTER INC	Project Name	Rev 1.1
A3	T12C	
Date: Friday, August 17, 2007	Sheet 65 of 94	

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<Variant Name>		ASUS®		Title : eSATA	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy			
Size	Project Name			Rev	
Custom	T12C			1.1	
Date:	Monday, August 13, 2007	Sheet	66	of	94

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD15	2	D
1394 (R5C841)	AD17	1	B
CARD READER (R5C841)	AD17	1	C
CARDBUS (R5C841)	AD17	1	D
1394 (R5C832)	AD18	1	B
CARD READER (R5C832)	AD18	1	C


SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)
SDVO to DVI (SIL1362A)	0111000x (70)

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		Title :RESOURCE
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size Custom	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007	Sheet 67 of 94	




<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size	Project Name	Rev
A	T12C	1.1
Date: <i>Monday, August 13, 2007</i>		Sheet 68 of 94

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<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size	Project Name	Rev
A	T12C	1.1
Date: <i>Monday, August 13, 2007</i>		Sheet 69 of 94

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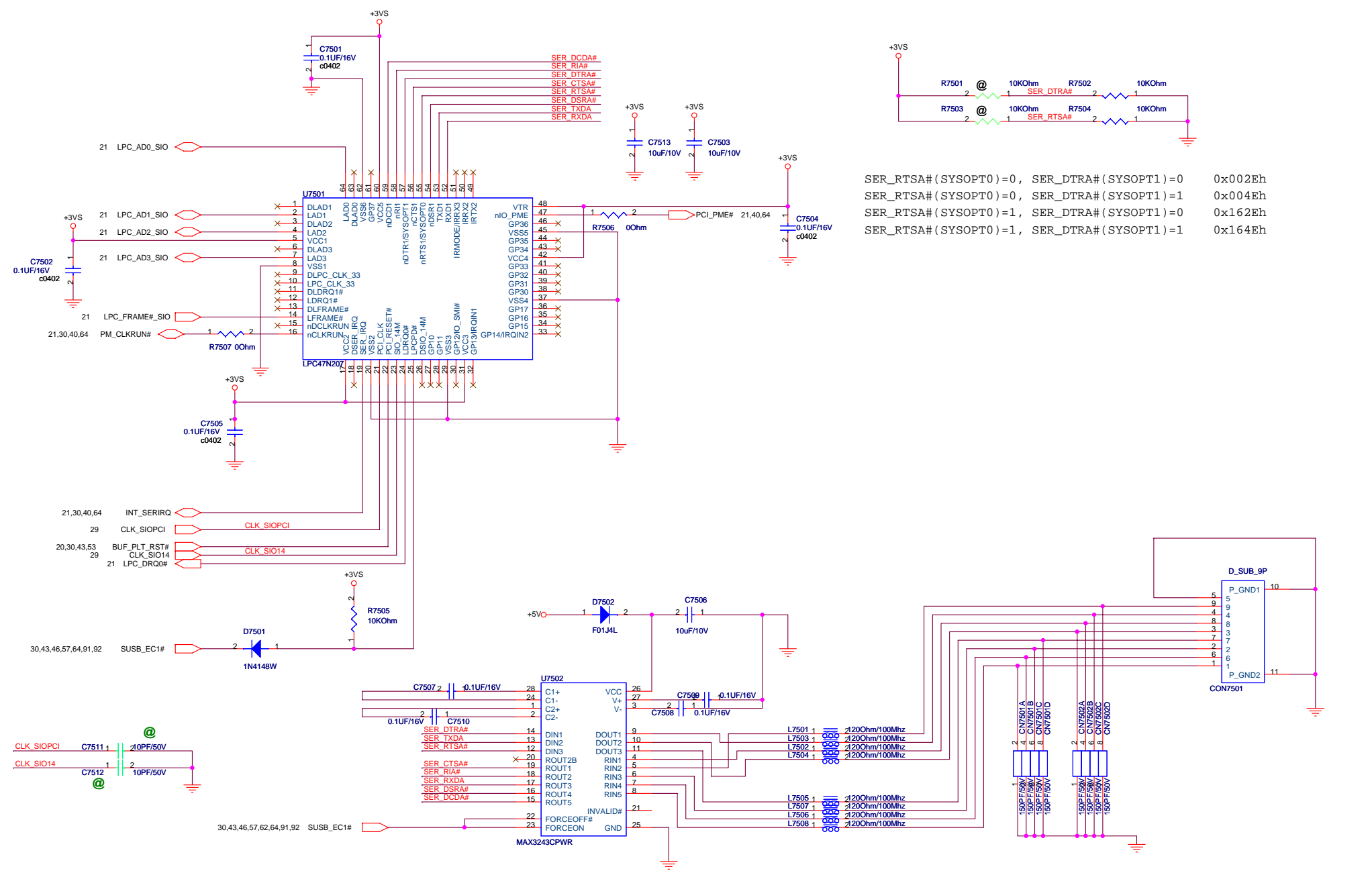
	5	4	3	2	1
D					
C					
B					
A					

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<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: <i>Monday, August 13, 2007</i>		Sheet	70 of 94

	5	4	3	2	1
D					
C					
B					
A					



```

SER_RTSA#(SYSOPT0)=0, SER_DTRA#(SYSOPT1)=0 0x002Eh
SER_RTSA#(SYSOPT0)=0, SER_DTRA#(SYSOPT1)=1 0x004Eh
SER_RTSA#(SYSOPT0)=1, SER_DTRA#(SYSOPT1)=0 0x162Eh
SER_RTSA#(SYSOPT0)=1, SER_DTRA#(SYSOPT1)=1 0x164Eh

```

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		Title : Null	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Date:	Rev
Custom	T12C	Tuesday, February 26, 2008	1.1
Date: Tuesday, February 26, 2008		Sheet	76 of 94

Change Note:


R1.1 :

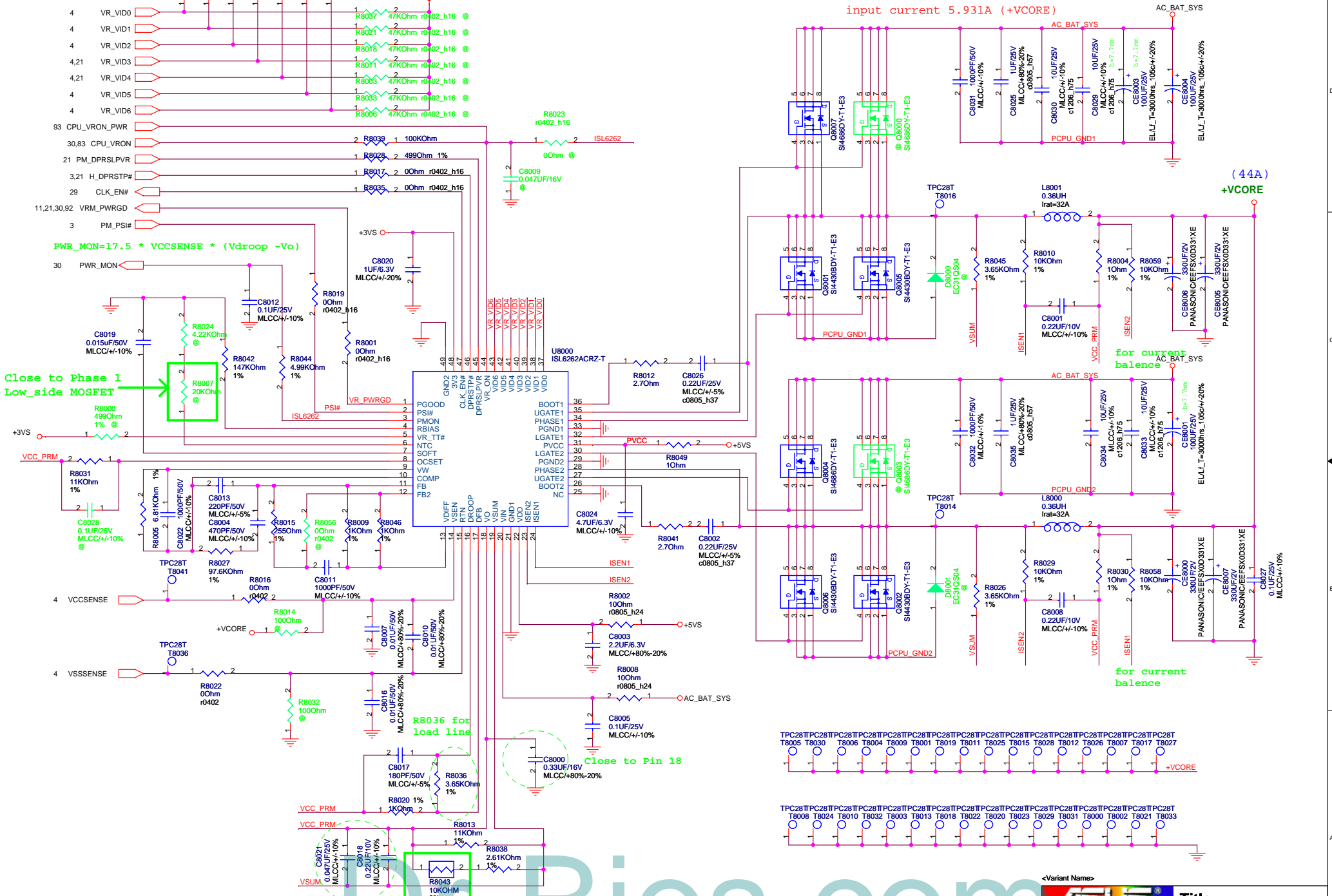
1. Reserve LVDS Up and Low channel of VGA side.
2. Change R3404 R3405 to 0ohm for LAN disconnect issue.
3. Change U3302 U3303 for new part.
4. Add D6004/D6003 for optional
5. Add R3114,R3115
6. Add Q3301,Q3302,R3341,R3342, C3329,C3330
7. Change IDSEL_CB to AD24/AD25. p64
8. add R6416 to CB_HWSPND#. P65
9. add Q3709 for depop issue. P37
9. change Q9203 TO Q3705B for ref error.

R2.0 :

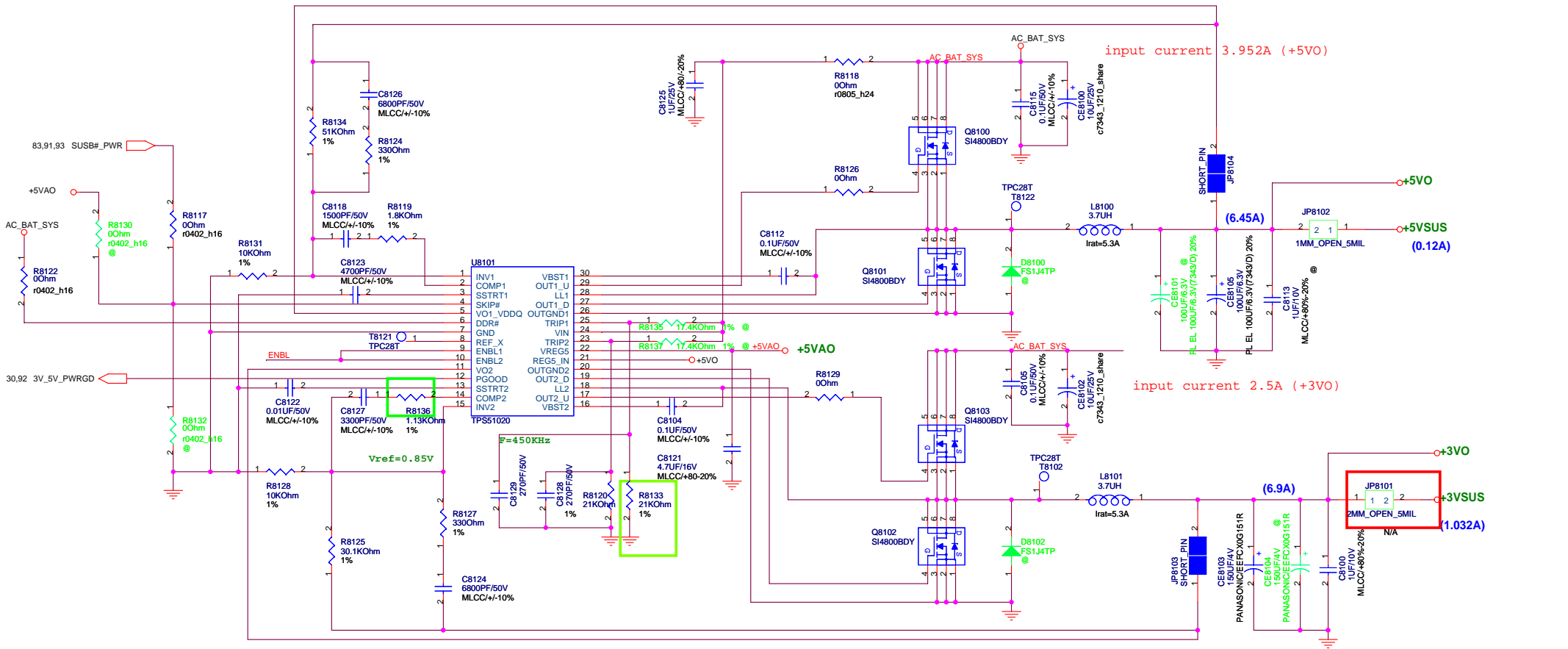
1. Add C3202/C4210 /R4216 for EMI
2. Add R4607 and change Q4603 for LCD VCC
3. Add C2530,C2545,C2546,C2547,C2548,C2549,C2550,C2551,C2552,C2553,C2554,C2555

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<Variant Name>		
 Title : NULL		
ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy		
Size	Project Name	Rev
Custom	T12C	1.1
Date: Friday, August 17, 2007		Sheet 79 of 94



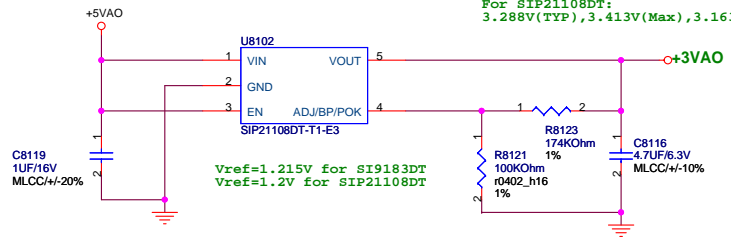
ASUS
Title :POWER_VCORE
 ASUSTeK COMPUTER INC. NB Engineer: **Tanner Zhang**
 Size Project Name
 Custom T12C
 Date: Tuesday, March 11, 2008 Sheet 80 of 94
 Rev 1.1



input current 3.952A (+5V0)

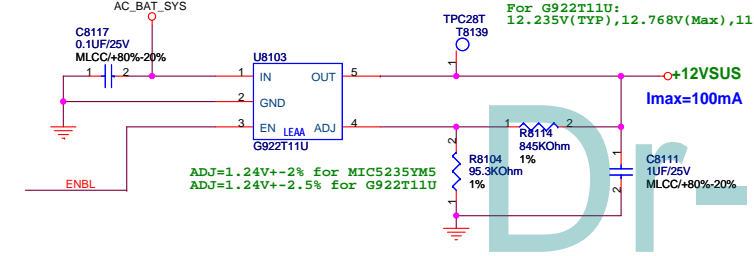
input current 2.5A (+3V0)

+3VAO
BOM need add second source:
SI9183 (06G007055114)

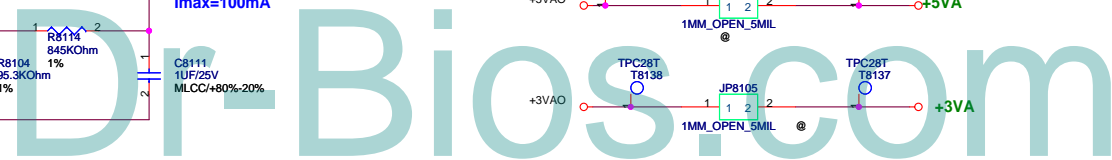
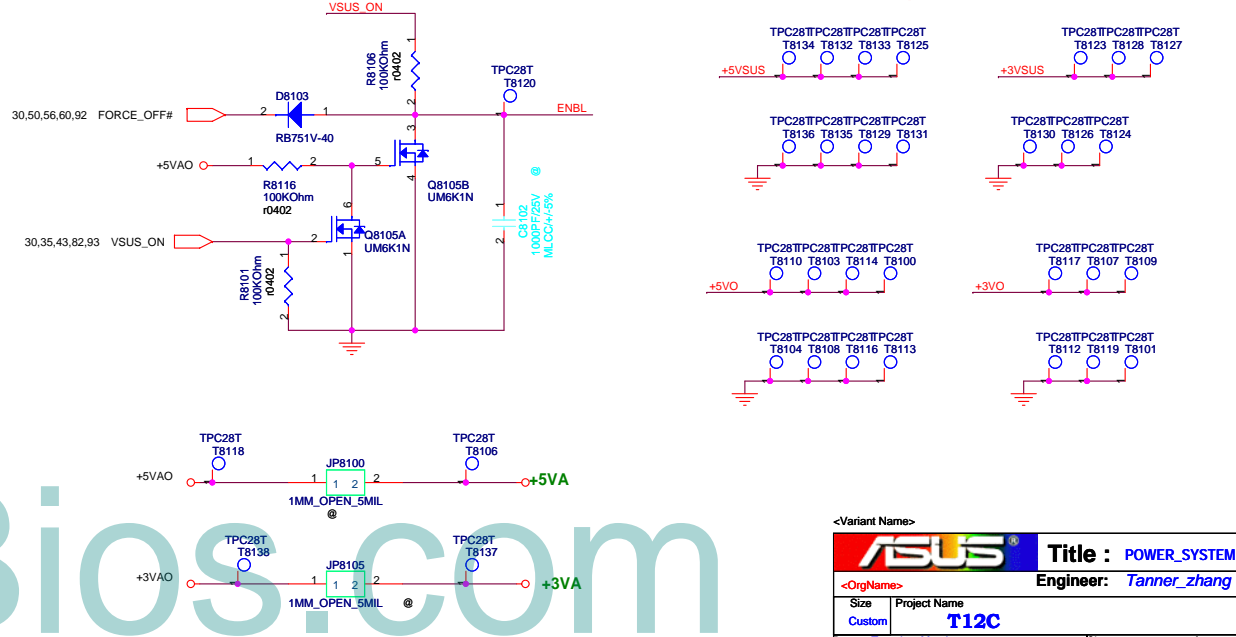


For SI9183DT:
3.329V(TYP), 3.473V(Max), 3.178V(min)
For SIP21108DT:
3.288V(TYP), 3.413V(Max), 3.163V(min)

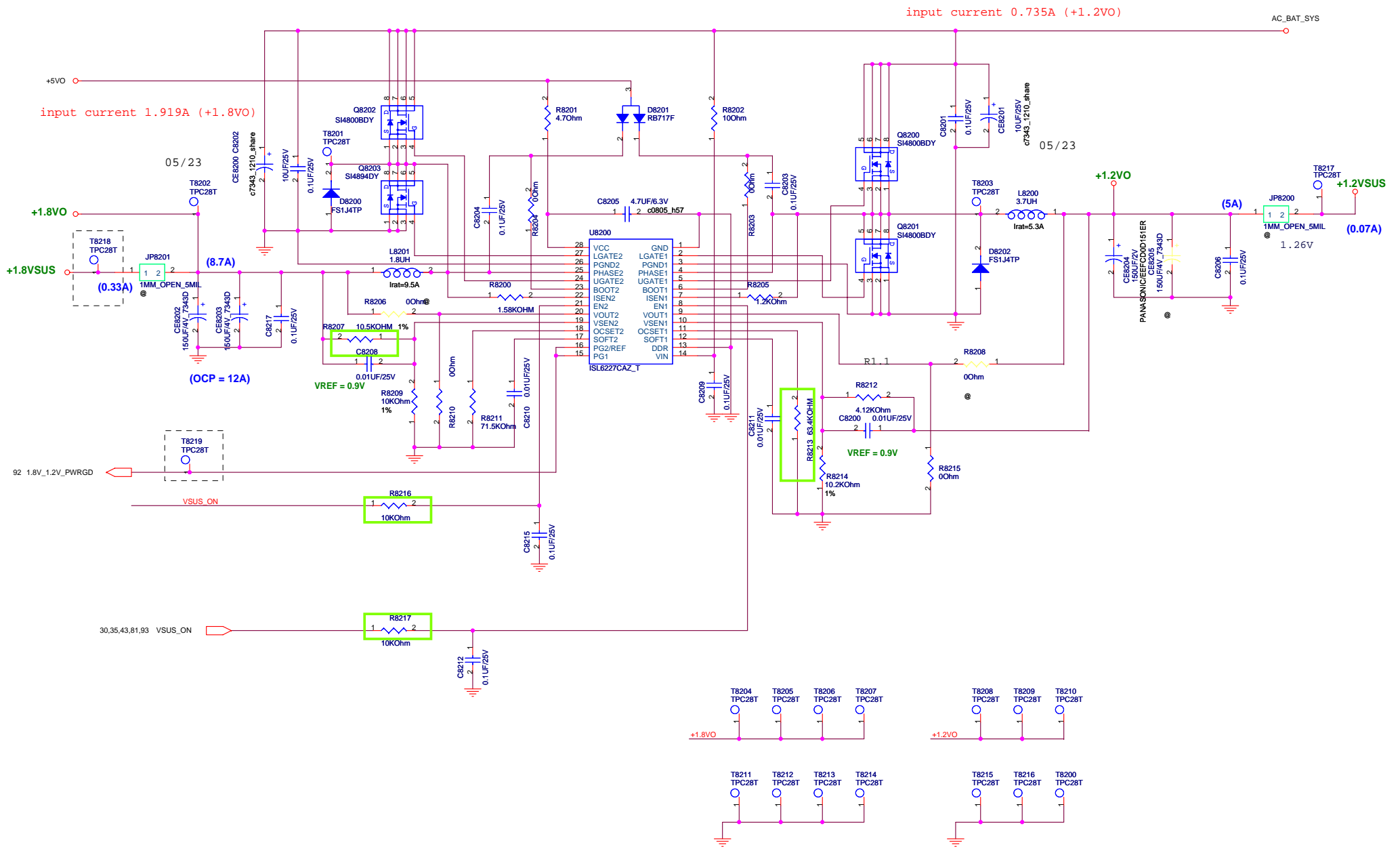
+12VSUS
BOM need add second source:
MIC5235YM5 (06G007137020)



For MIC5235YM5:
12.235V(TYP), 12.706V(Max), 11.777V(min)
For G922T11U:
12.235V(TYP), 12.768V(Max), 11.717V(min)



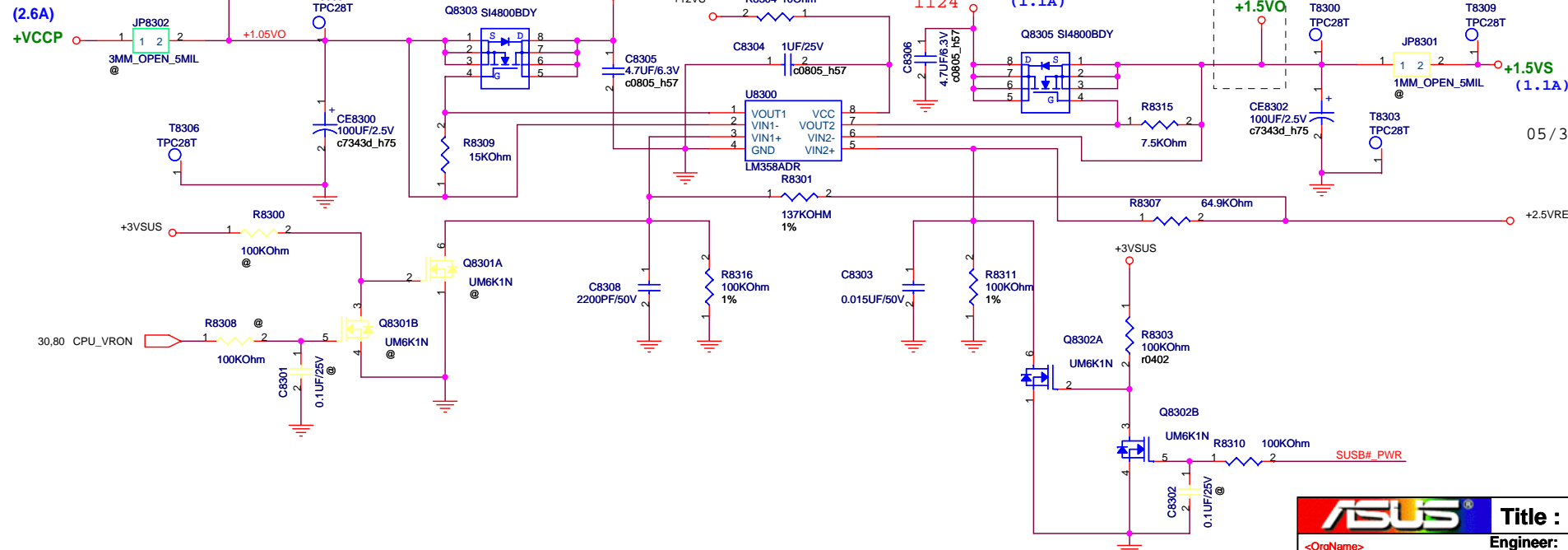
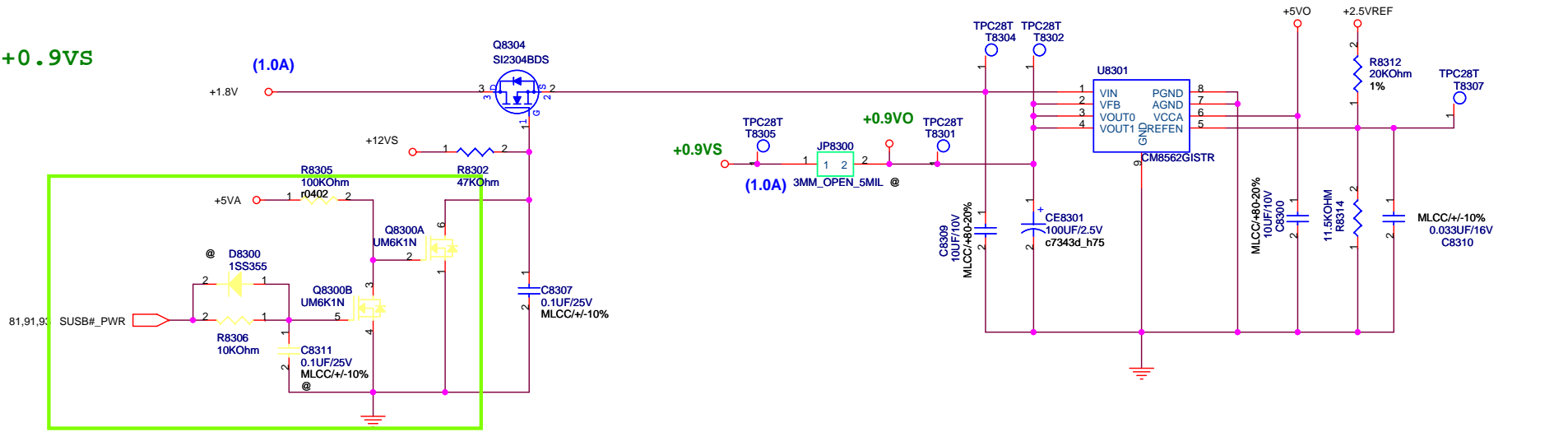
ASUS		Title : POWER_SYSTEM
-<OrigName>		Engineer: Tanner_zhang
Size	Project Name	Rev
Custom	T12C	1.0
Date: Tuesday, March 11, 2008	Sheet	81 of 94



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ASUS		Title : 1.8V&1.2V	
-<OrigName>		Engineer: Tanner	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Tuesday, March 11, 2008	Sheet 82	of 94	

+0.9VS

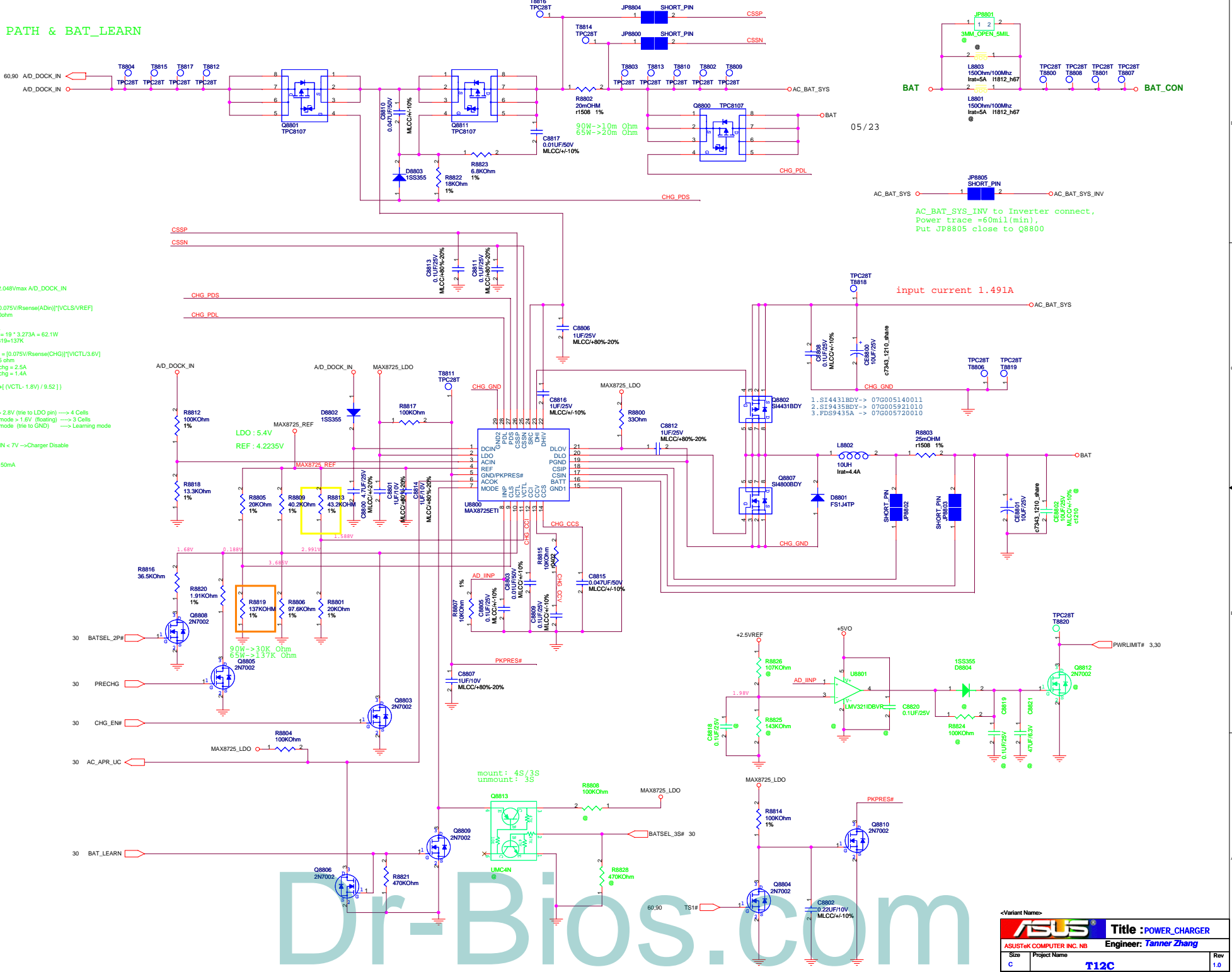


		Title : 1.05V & +0.9VS	
<OrgName>		Engineer: Tanner_zhang	
Size	Project Name		Rev
B	T12C		1.1
Date: Tuesday, March 11, 2008		Sheet	83 of 94

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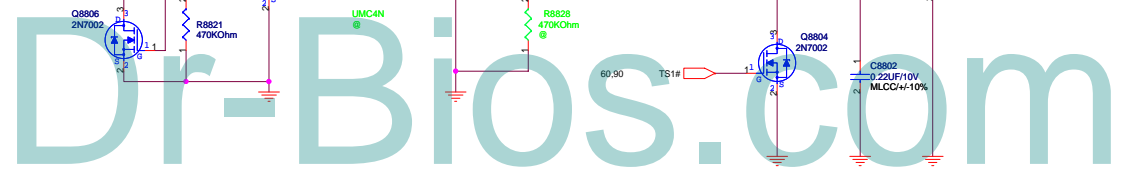
POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Adapter lin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
 Rsense(ADin)=0.010ohm
 VCLS=3.685V
 => lin(max)=3.273A
 => Constant Power = 19 / 3.273A = 62.1W
 => R8805=20K, R8819=137K
 Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
 Rsense(CHG)=0.025ohm
 VICTL= 3V => Ichg = 2.5A
 Vbatt = 1.68V => Ichg = 1.4A
 Vbatt = Cell * (Vref - (VICTL - 1.8V) / 9.52)
 VCTL = 1.588V
 => Vbatt = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells
 2.0 > Vmode = 1.5V (floating) ----> 3 Cells
 0.8 > Vmode (tie to GND) ----> Learning mode
 VICTL < 0.8V or DCIN < 7V -> Charger Disable
 Precharge current=150mA




AC_BAT_SYS_INV to Inverter connect,
 Power Trace =60mil(min),
 Put JP8805 close to Q8800

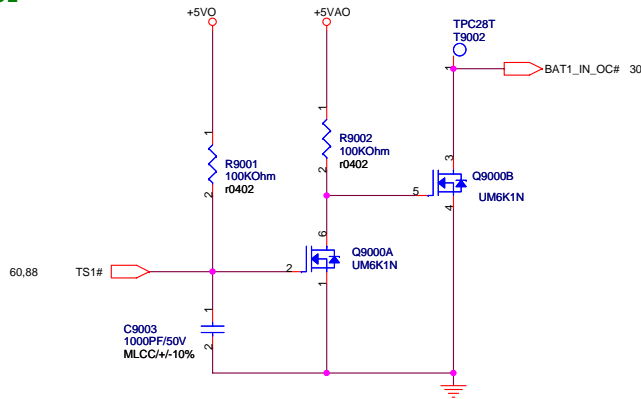
input current 1.491A



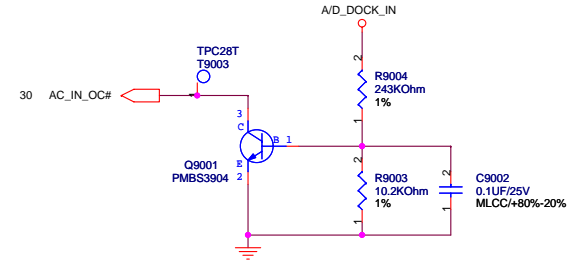
Dr-Bios.com

<Variant Name>		
		Title : <i>N/A</i>
<OrgName>		Engineer: <i>Tanner</i>
Size	Project Name	Rev
Custom	T12C	1.0
Date: <i>Tuesday, March 11, 2008</i>		
Sheet 89 of 94		

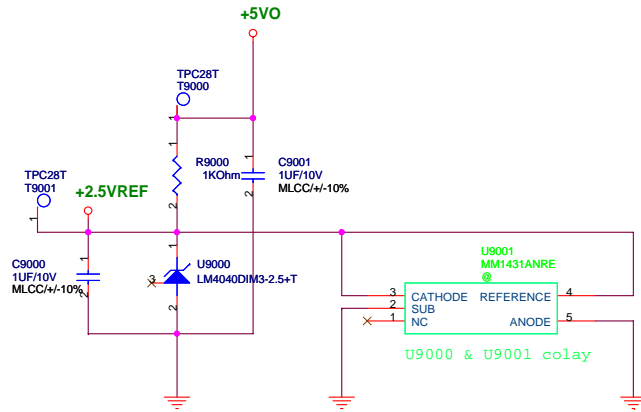
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



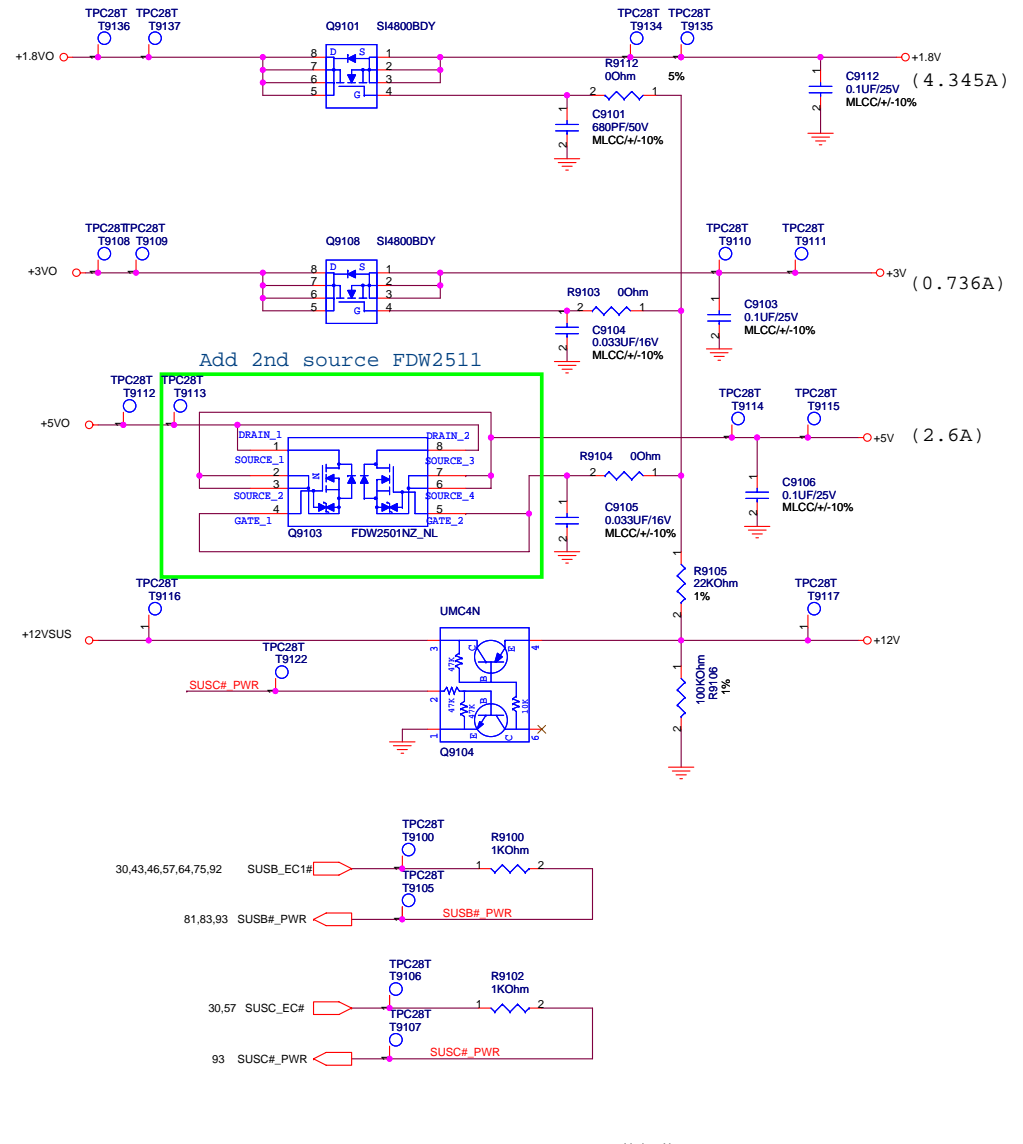
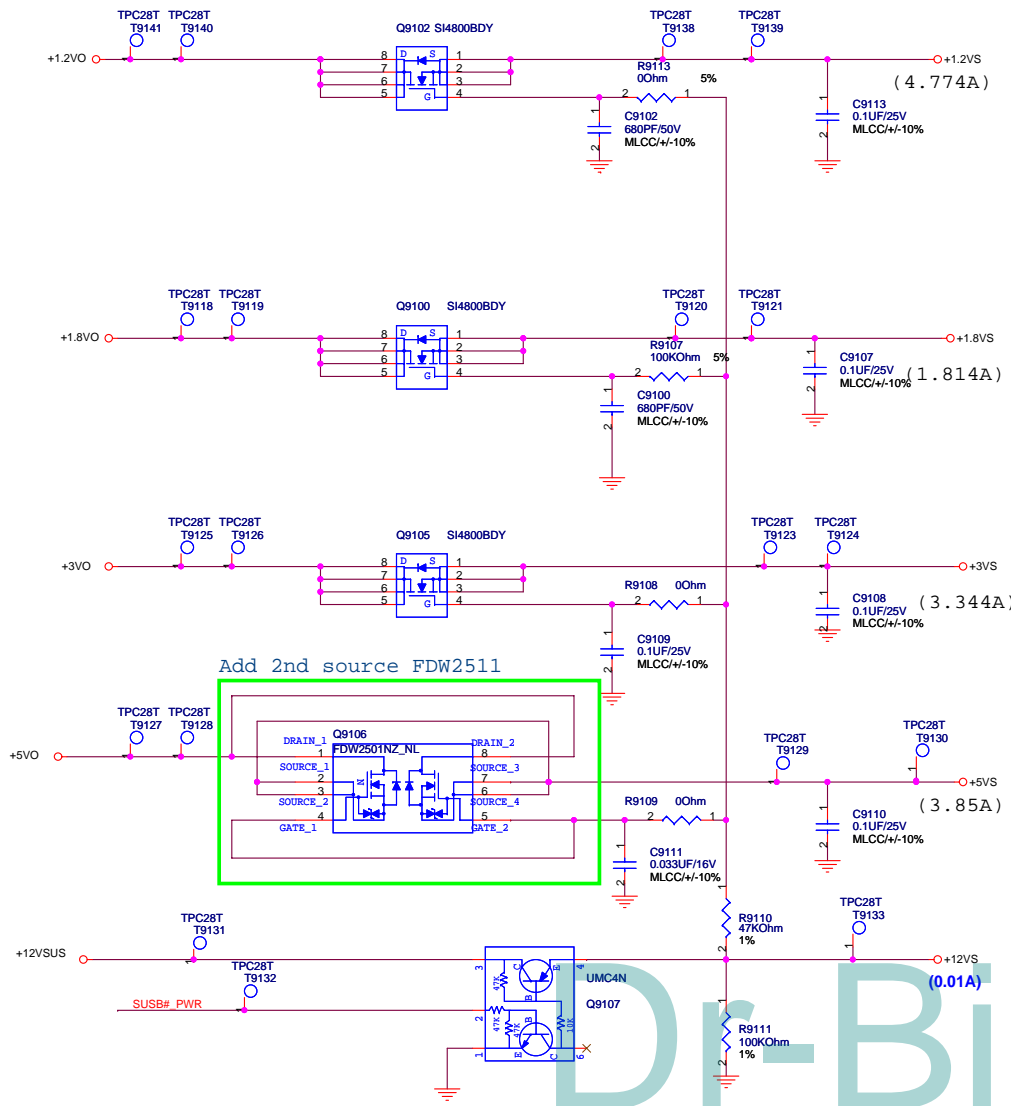
U9000 Main source change to 06G006002414(tolerance:1%).
 Add second source 06G006002610 (tolerance:1%),
 06G006002412 (tolerance:0.2%) and
 06G006002020 (tolerance:0.2%)



<Variant Name>		ASUS		Title :POWER_DETECT	
<OrgName>		Engineer: tanner			
Size	Project Name	Rev			
Custom	T12C	1.0			
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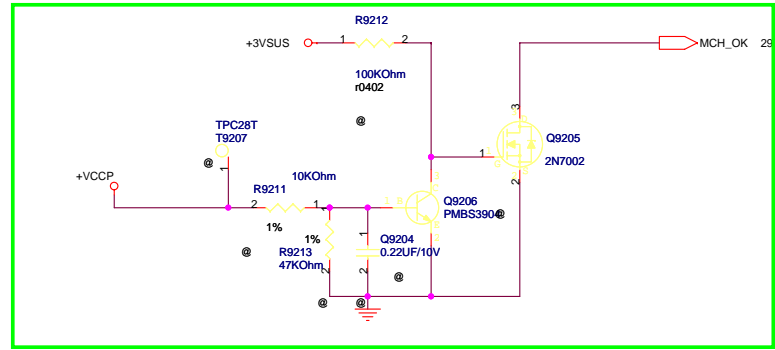
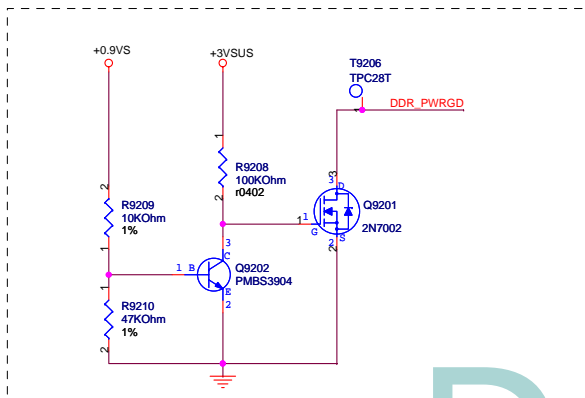
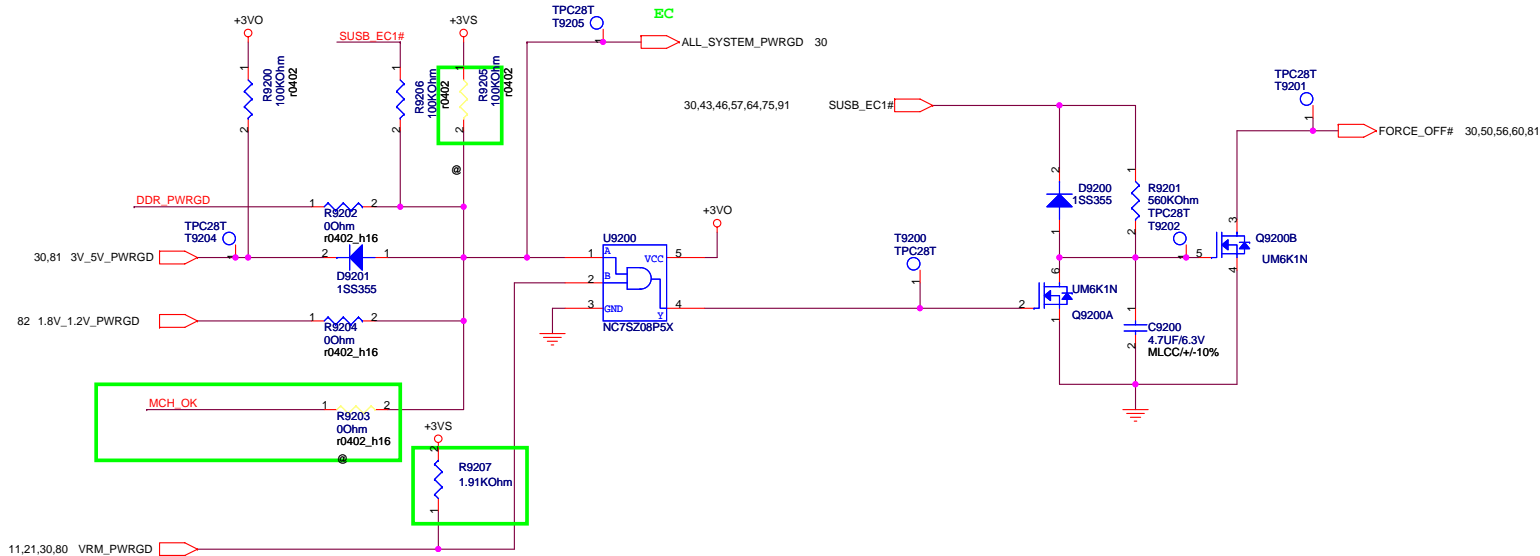
SUSC#_STAGE POWER

SUSB#_STAGE POWER

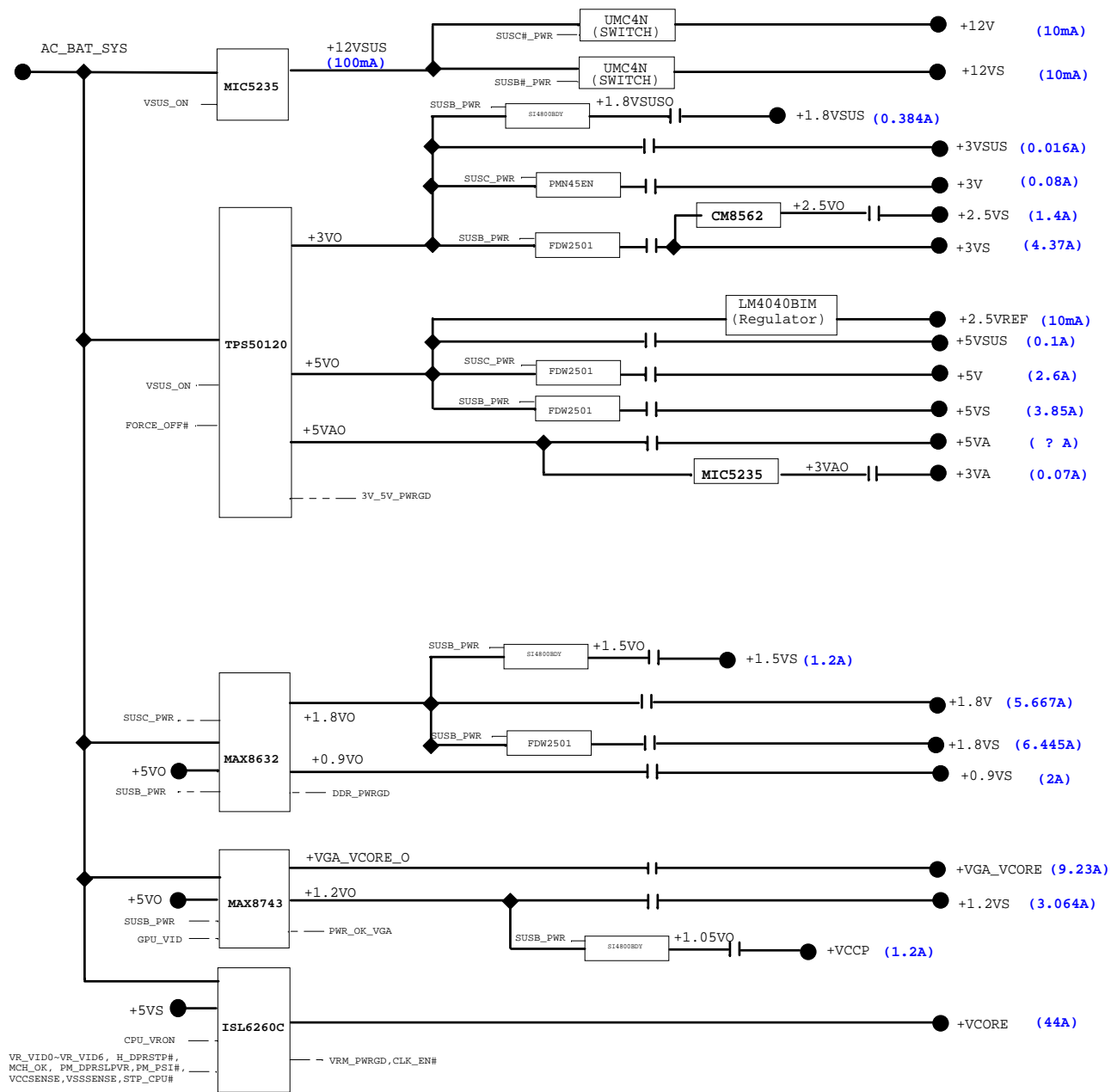


-Variant Name-		ASUS Title : POWER_LOAD SWITCH	
-OrgName-		Engineer: Tanner	
Size	Project Name	Rev	
Custom	T12C	1.0	
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POWER GOOD DETECTOR



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