



PCB
Part Number = DA6000M700

Compal Confidential

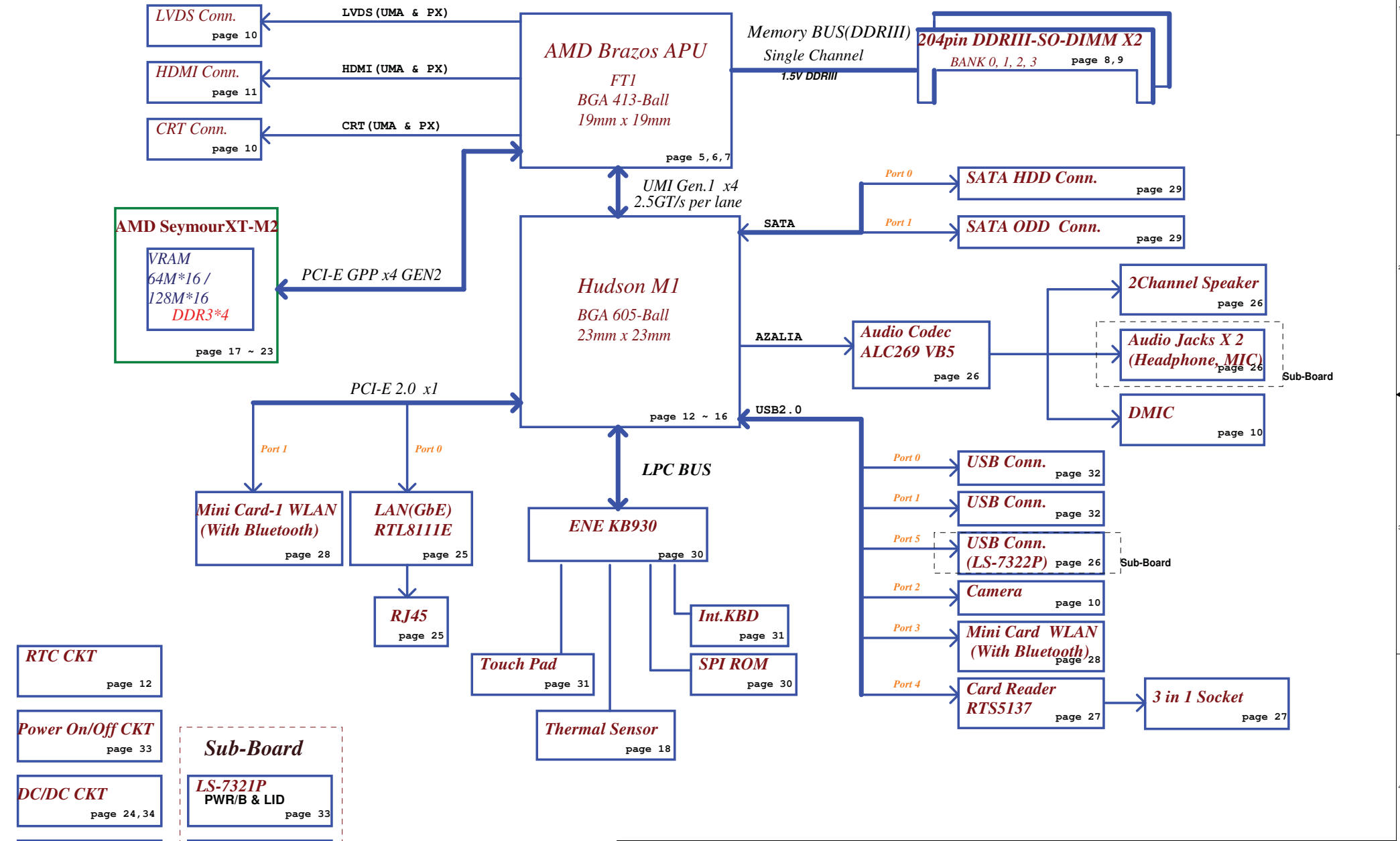
PBL50 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + DGPU Seymour XT-M2

2011-02-15

REV: 0.22

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

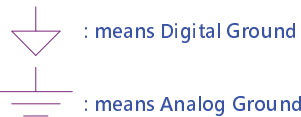
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE PU Rail	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930 +3VALW	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V +3VS	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH +3VS	V	X	X	V	V	X
FCH_SIC FCH_SID	FCH +3VALW	X	X	V Reserve	X	X	X

SCL0, SDA0 (Primary SMBUS in the S0 domain)
 SCL1, SDA1 (Secondary SMBUS supporting ASF)
 SCL2, SDA2 (Primary SMBUS in the S5 domain)
 SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
 SCL4, SDA4 (Primary SMBUS in the S5 domain)

Symbol Note :



FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

10G@ : 1.0G CPU (C50)
 15G@ : 1.5G CPU (E240)
 16G@ : 1.6G CPU (E350)
 UMA@ : APU output.
 VGA@ : GPU used.
 LS@ : Level shift used.
 X76@ : VRAM.

X76@L01: Samsung 1G
 X76@L02: Hynix 1G
 X76@L03: Samsung 512M
 X76@L04: Hynix 512M

DIS M/B BOM Config

L01: 16G@/VGA@/LS@ --X76@L04
 L02: 16G@/UMA@/LS@
 L03: 15G@/VGA@/LS@ --X76@L03
 L04: 15G@/UMA@/LS@
 L05: 16G@/VGA@/LS@ --X76@L01
 L06: 15G@/VGA@/LS@ --X76@L02
 L07: 10G@/UMA@/LS@

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Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
2. VDDR3 should ramp-up before or simultaneously with VDDC.
3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VSG)

PCIE_VDDC(1.0V)

VDDR1(1.5VSG)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

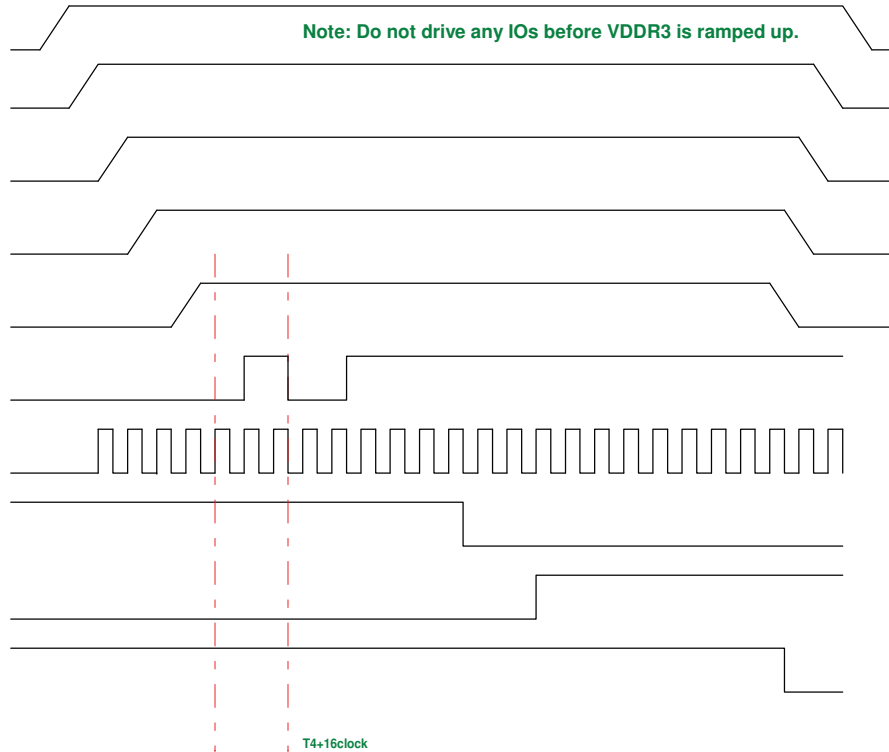
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset



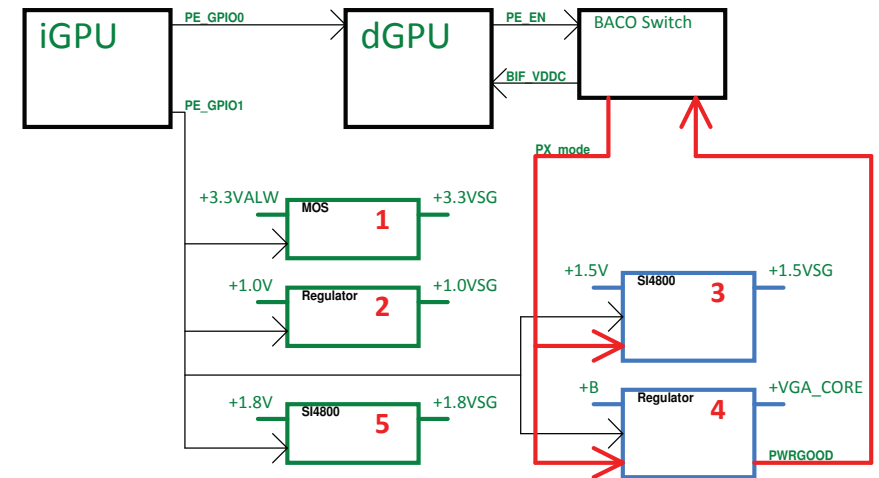
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

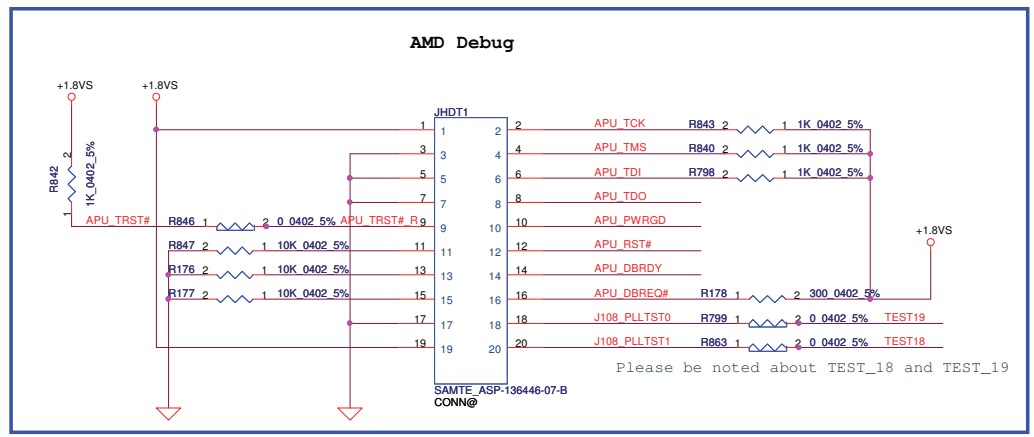
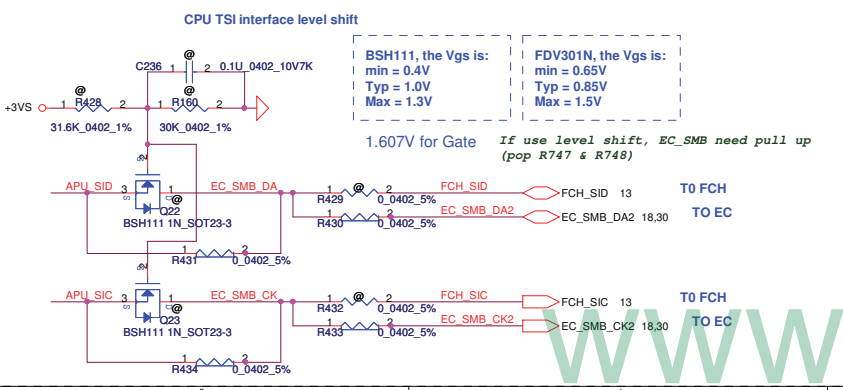
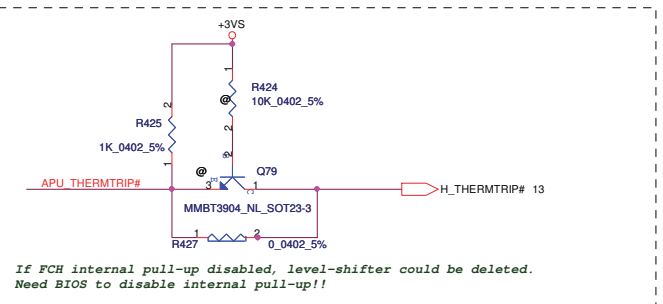
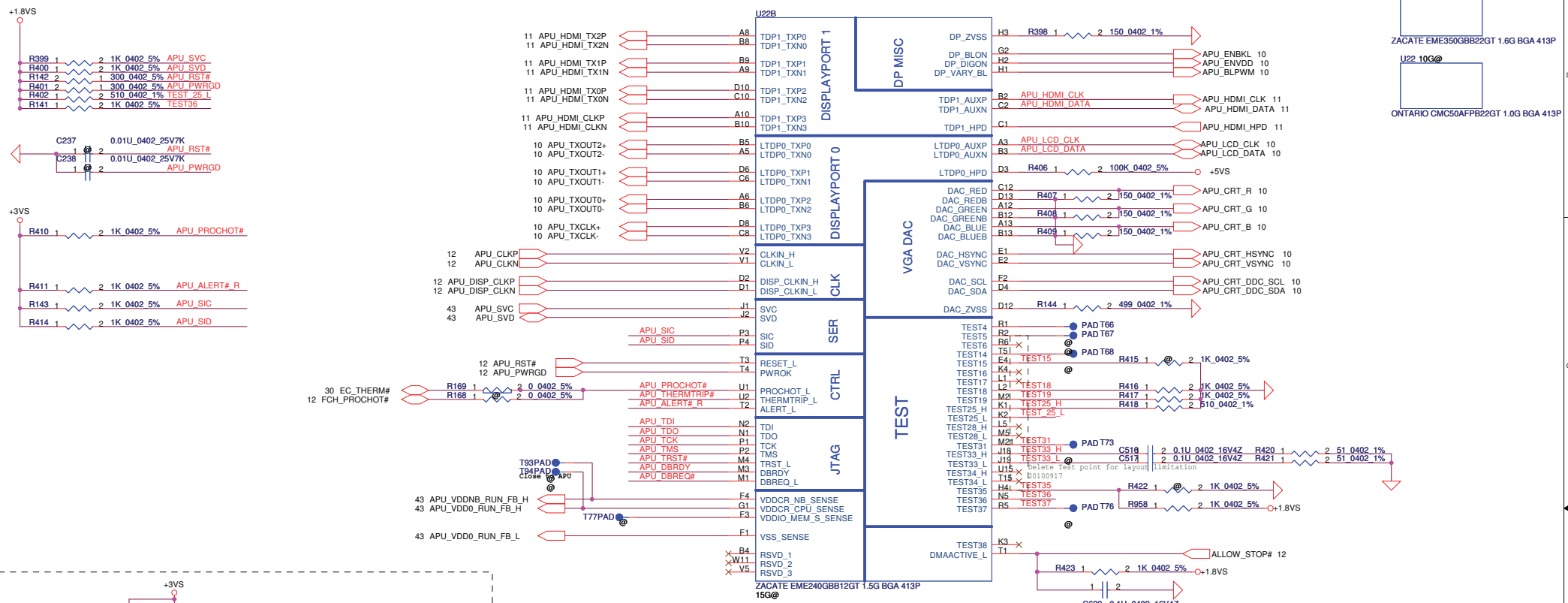
BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

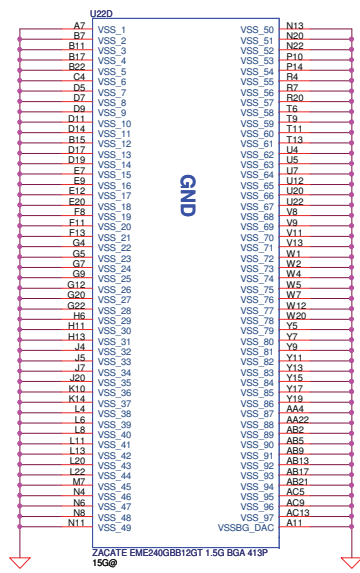
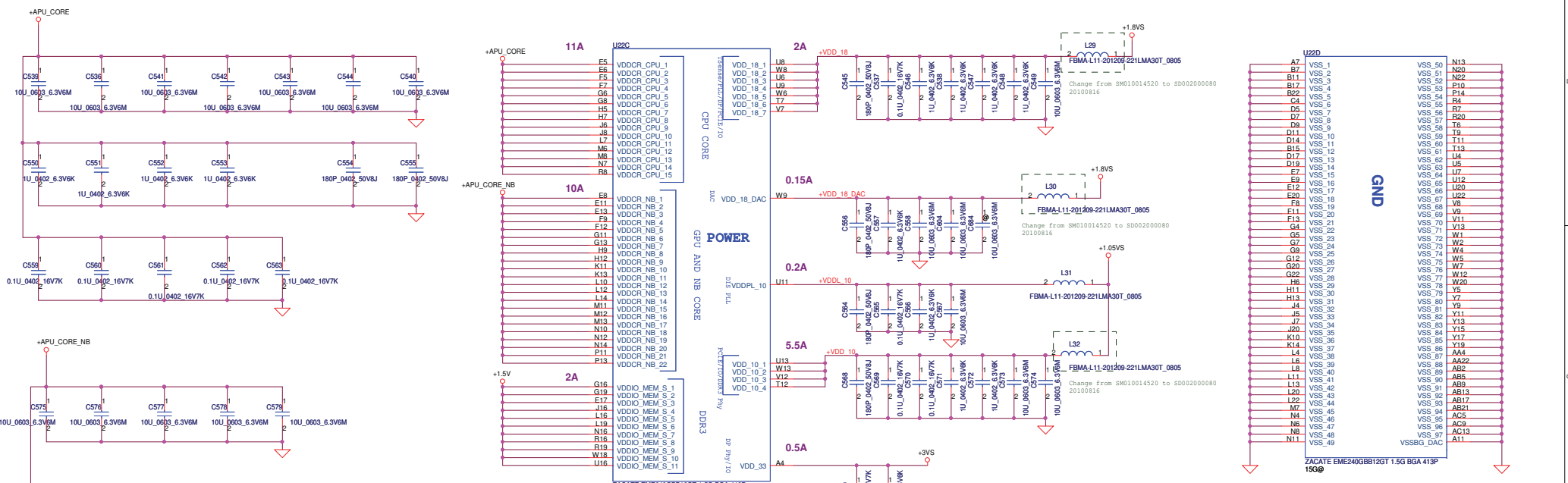
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1D1, A2VDDQ, VDD2D1, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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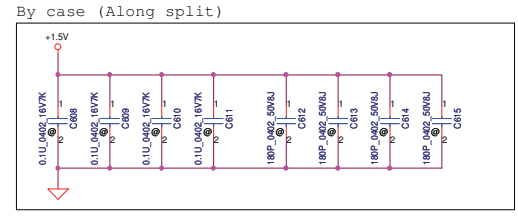
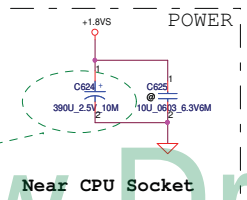
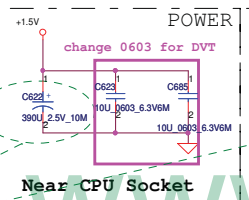
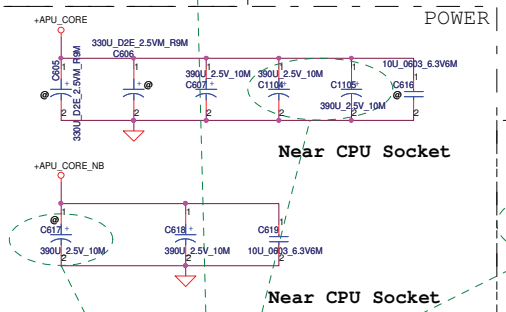
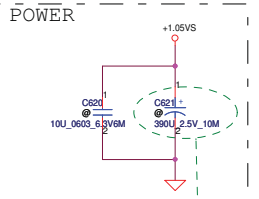


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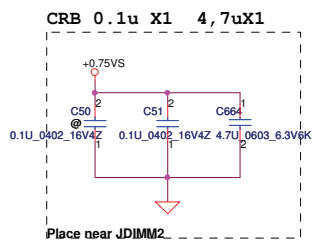
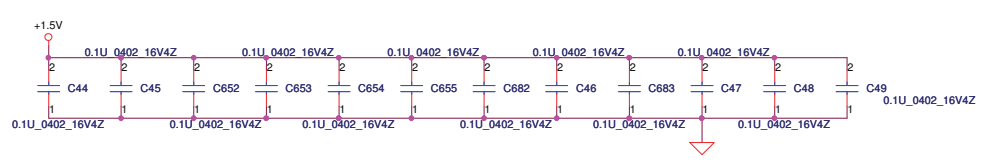
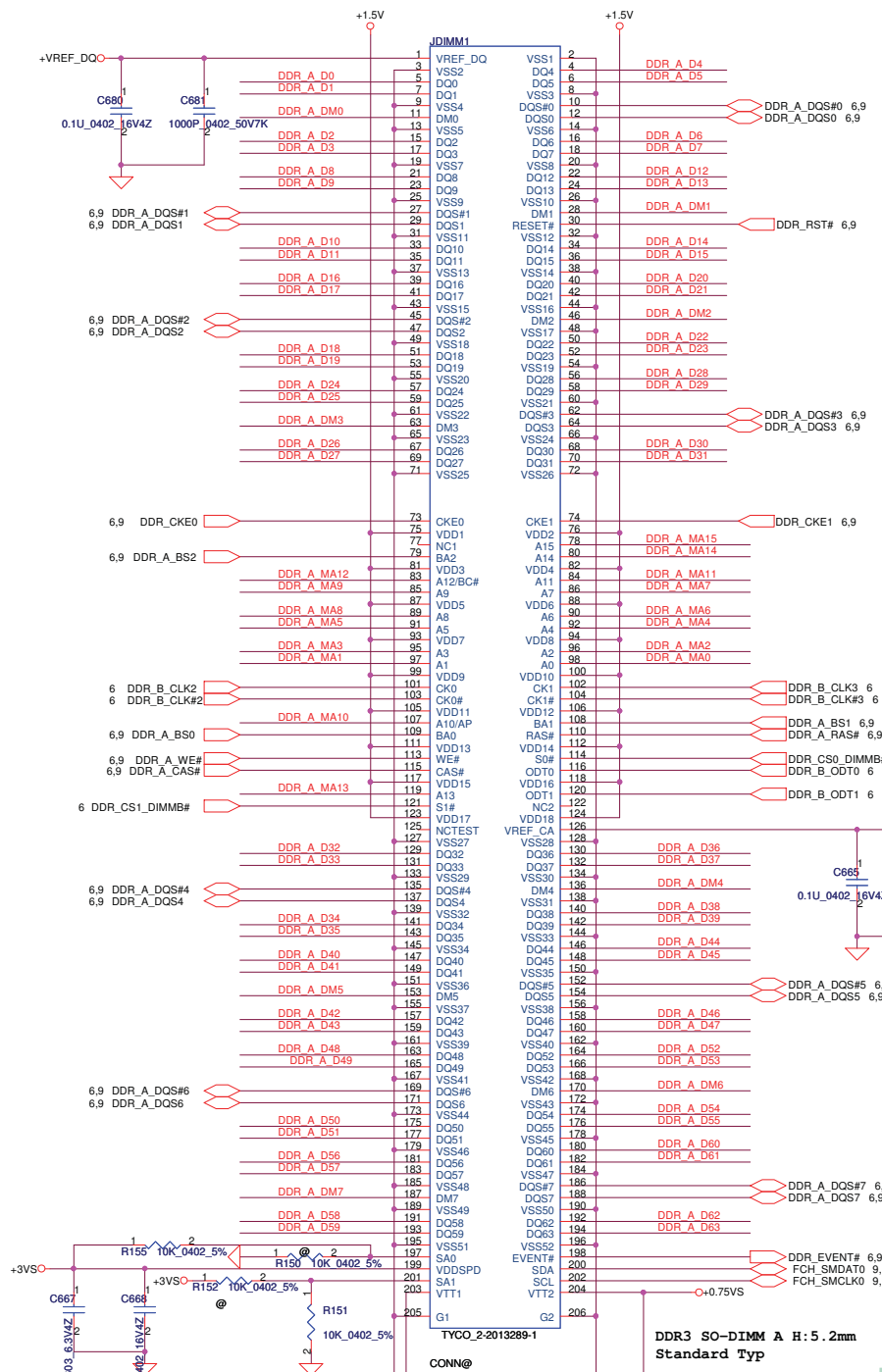


Power Cap. Summary

- APU**
 - S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 ---->+APU_CORE (Qty : 3) Unpop:2
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE (Qty : 2)
- APU_CORE_NB**
 - S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+APU_CORE_NB (Qty : 1)
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE_NB (Qty : 1)
- 1.5V**
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5V (Qty : 1)
- 1.05VS**
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.05VS (Qty : 1)
- 1.8VS**
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.8VS (Qty : 1)
- DDR3 Socket**
 - S POLY C 330U 2V M X LESR6M SX H1.9 ---->+1.5V (Qty : 1)
- FCH**
 - S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+1.1VS (Qty : 1) UMA unpop
- GPU**
 - S POLY C 330U 2V M X LESR6M SX H1.9 ---->+VGA_CORE (Qty : 2) Unpop:1
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+VGA_CORE (Qty : 1)
- 1.5VSG**
 - S A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5VSG (Qty : 1)
- USB**
 - S A-P_CAP 220U 6.3V M C45 R17M SVPE H4.4 ---->+USB_VCCA (Qty : 1)



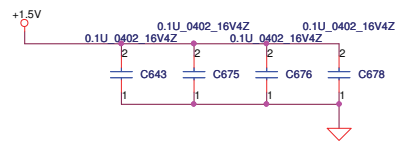
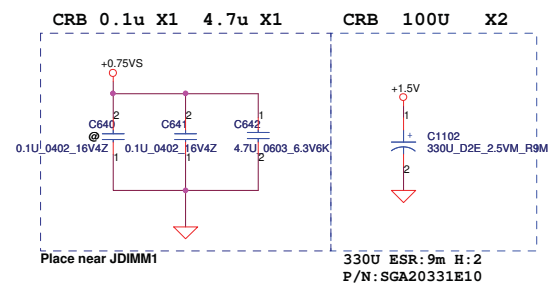
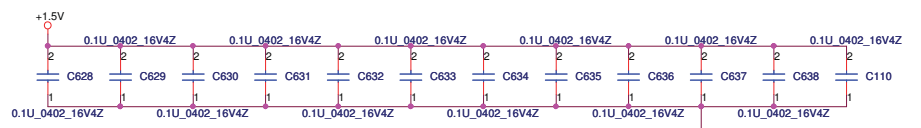
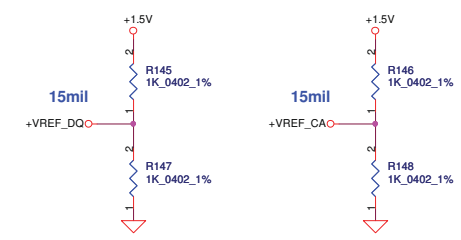
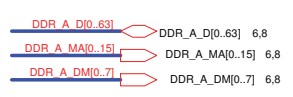
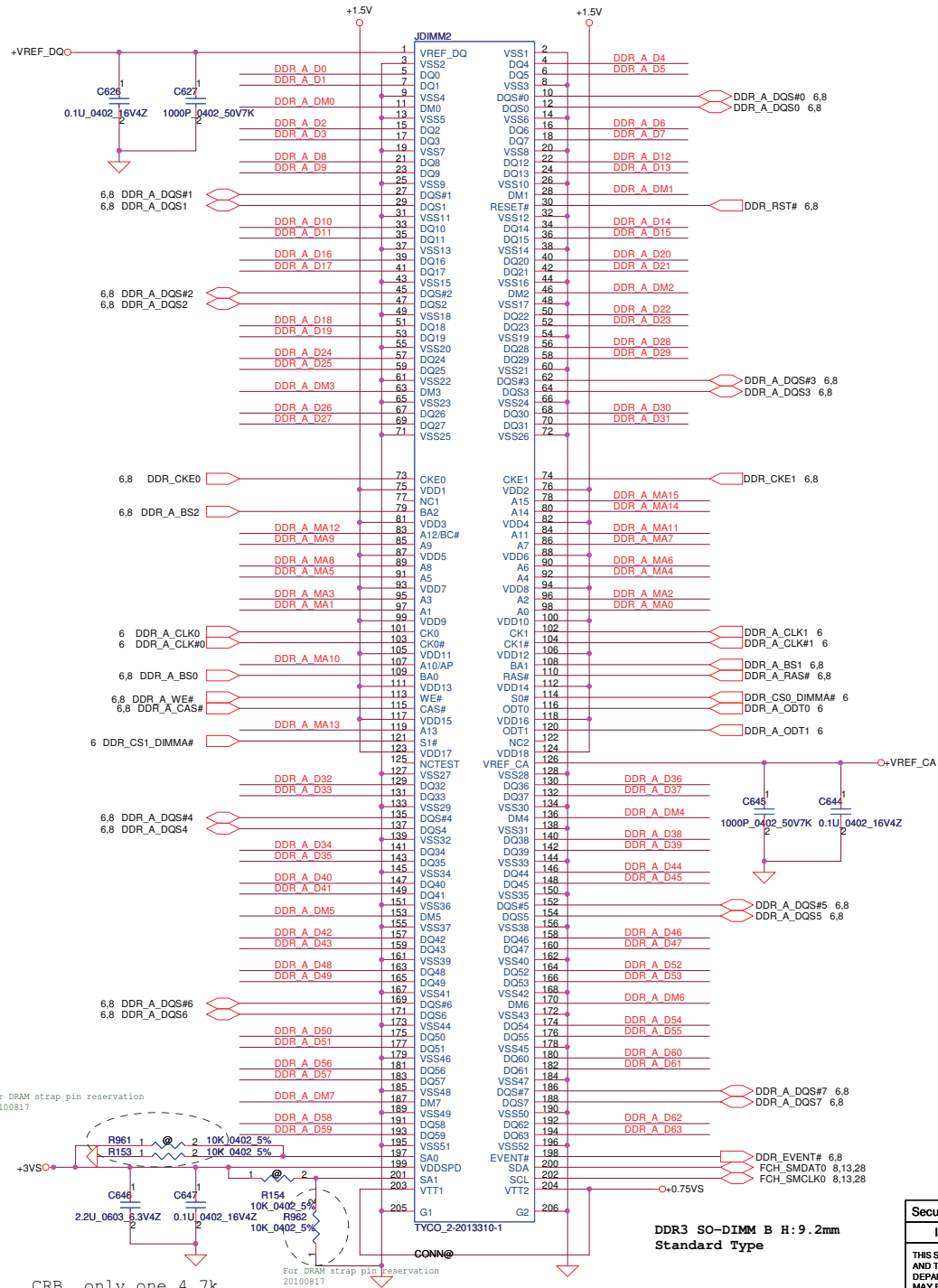
$(390\mu F \ 2.5V \ 6.3x5.7 \ ESR10m) * 1 = (SF000002000)$



Place near JDIMM2

DDR3 SO-DIMM A H:5.2mm
Standard Typ

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For DRAM strap pin reservation
20100817

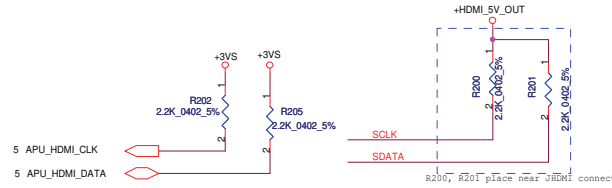
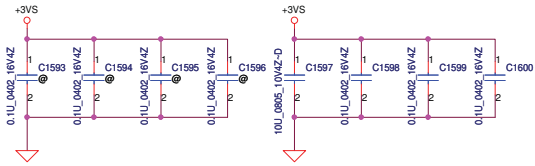
For DRAM strap pin reservation
20100817

DDR3 SO-DIMM B H:9.2mm
Standard Type

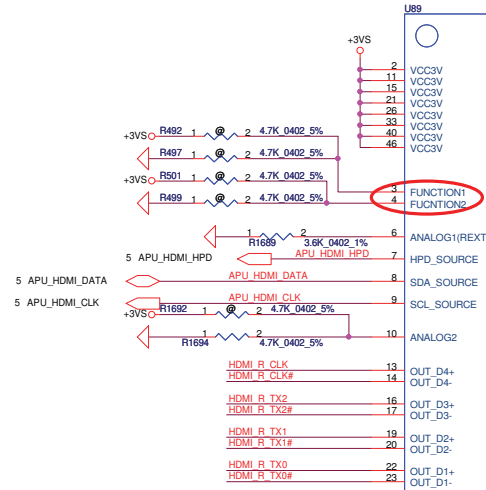
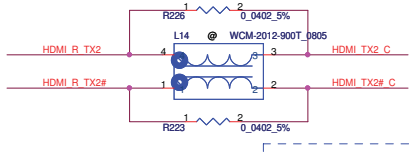
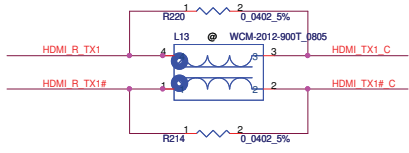
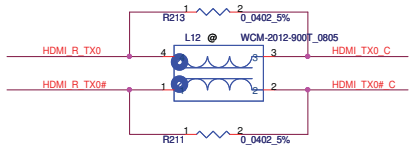
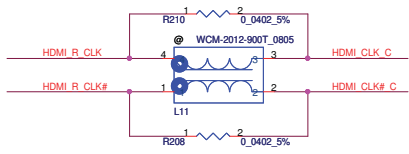
CRB only one 4.7k

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close to U10VCC (+3VS) pins (one Pin one Capacitor)

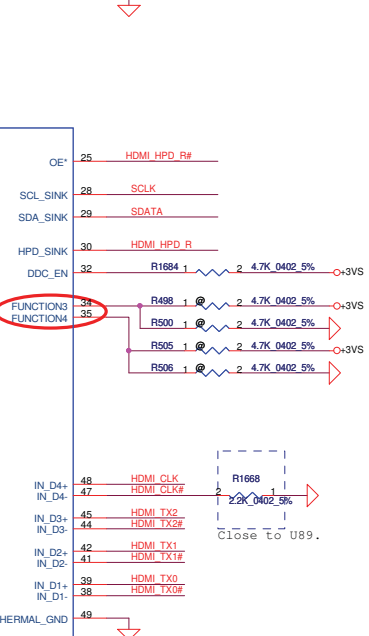
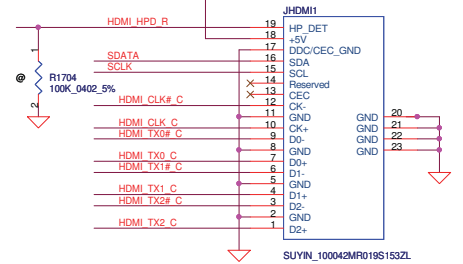
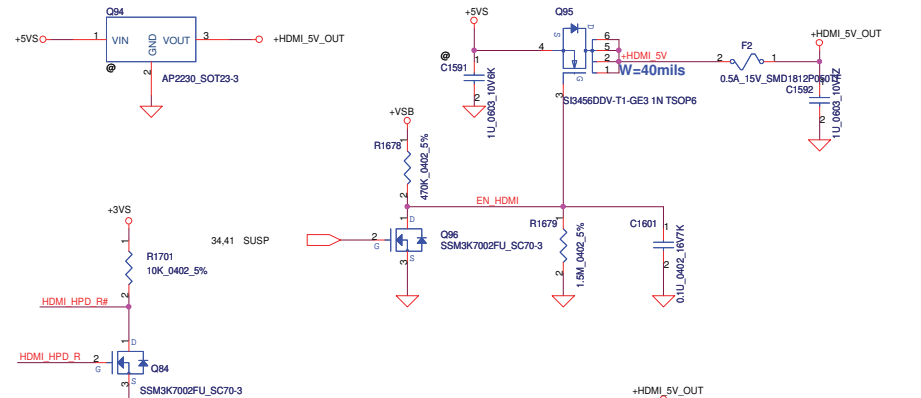
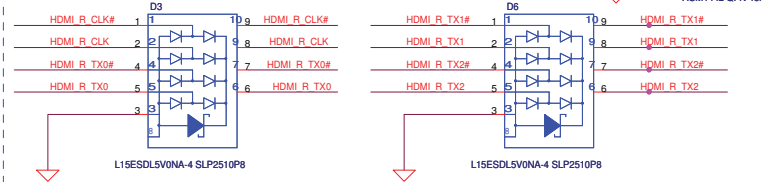


5 APU_HDMI_CLKP	C1802	1	2	0.1U 0402 16V7K	HDMI_CLK
5 APU_HDMI_CLKN	C1803	1	2	0.1U 0402 16V7K	HDMI_CLK#
5 APU_HDMI_TX0P	C1804	1	2	0.1U 0402 16V7K	HDMI_TX0
5 APU_HDMI_TX0N	C1805	1	2	0.1U 0402 16V7K	HDMI_TX0#
5 APU_HDMI_TX1P	C1806	1	2	0.1U 0402 16V7K	HDMI_TX1
5 APU_HDMI_TX1N	C1807	1	2	0.1U 0402 16V7K	HDMI_TX1#
5 APU_HDMI_TX2P	C1808	1	2	0.1U 0402 16V7K	HDMI_TX2
5 APU_HDMI_TX2N	C1809	1	2	0.1U 0402 16V7K	HDMI_TX2#

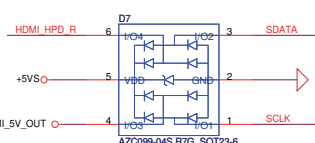


Trace AS Short PASS

ASM1442 QFN 48P



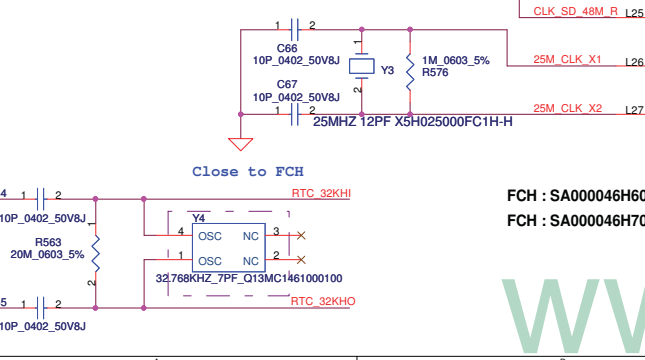
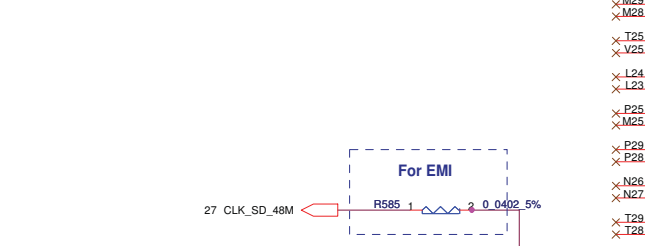
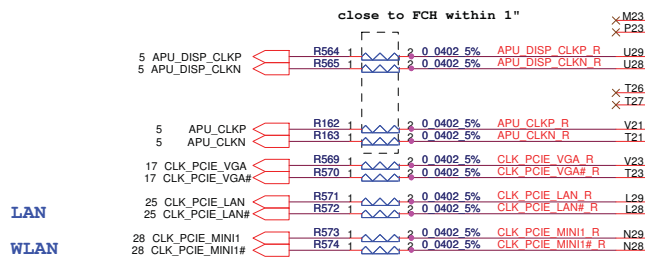
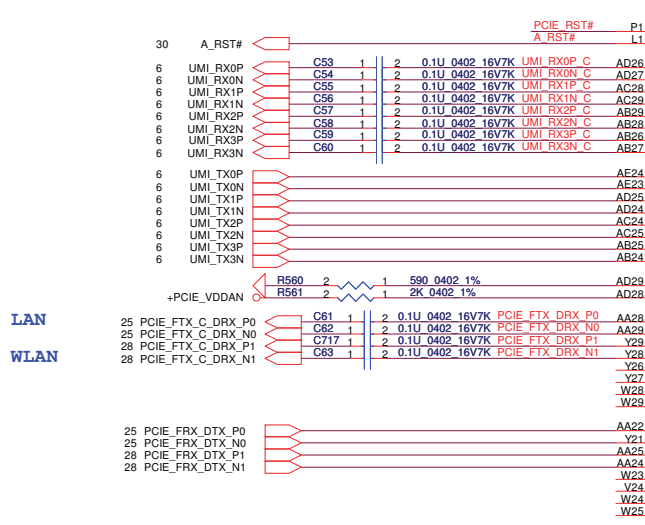
Close to U89.



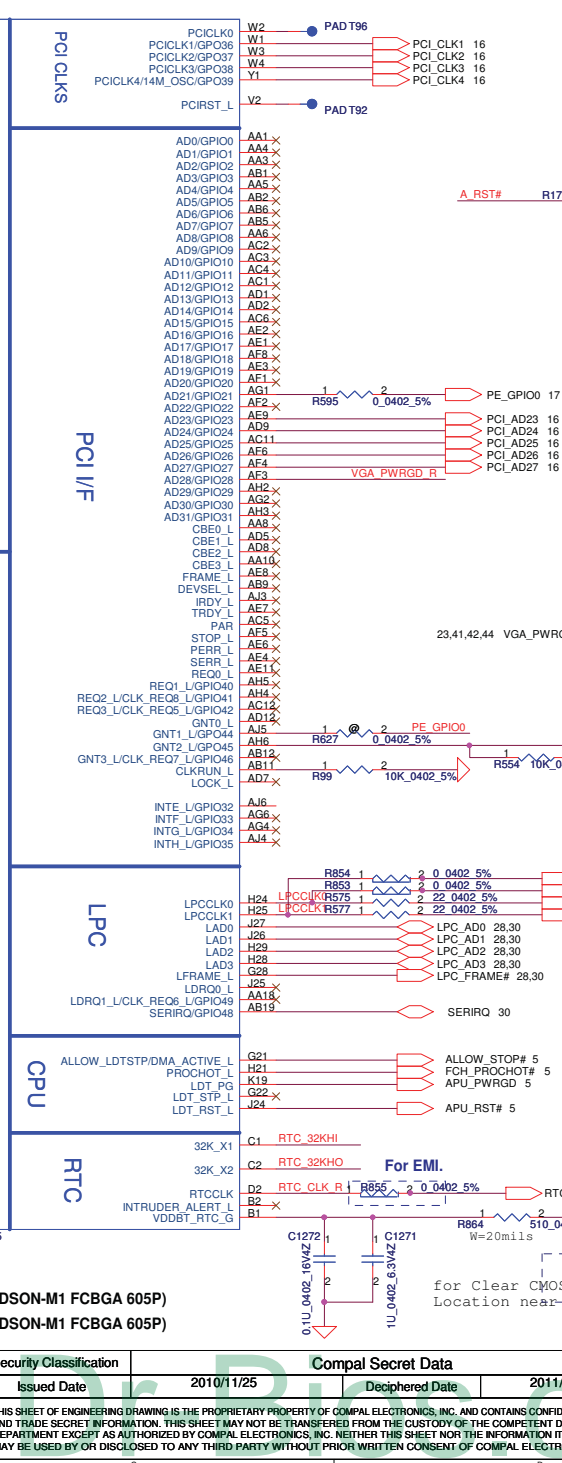
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				P11-HDMI CONN	
				Size Document Number	
				LA7321P PBL50	
				Date: Wednesday, February 16, 2011	
				Sheet 11 of 46	

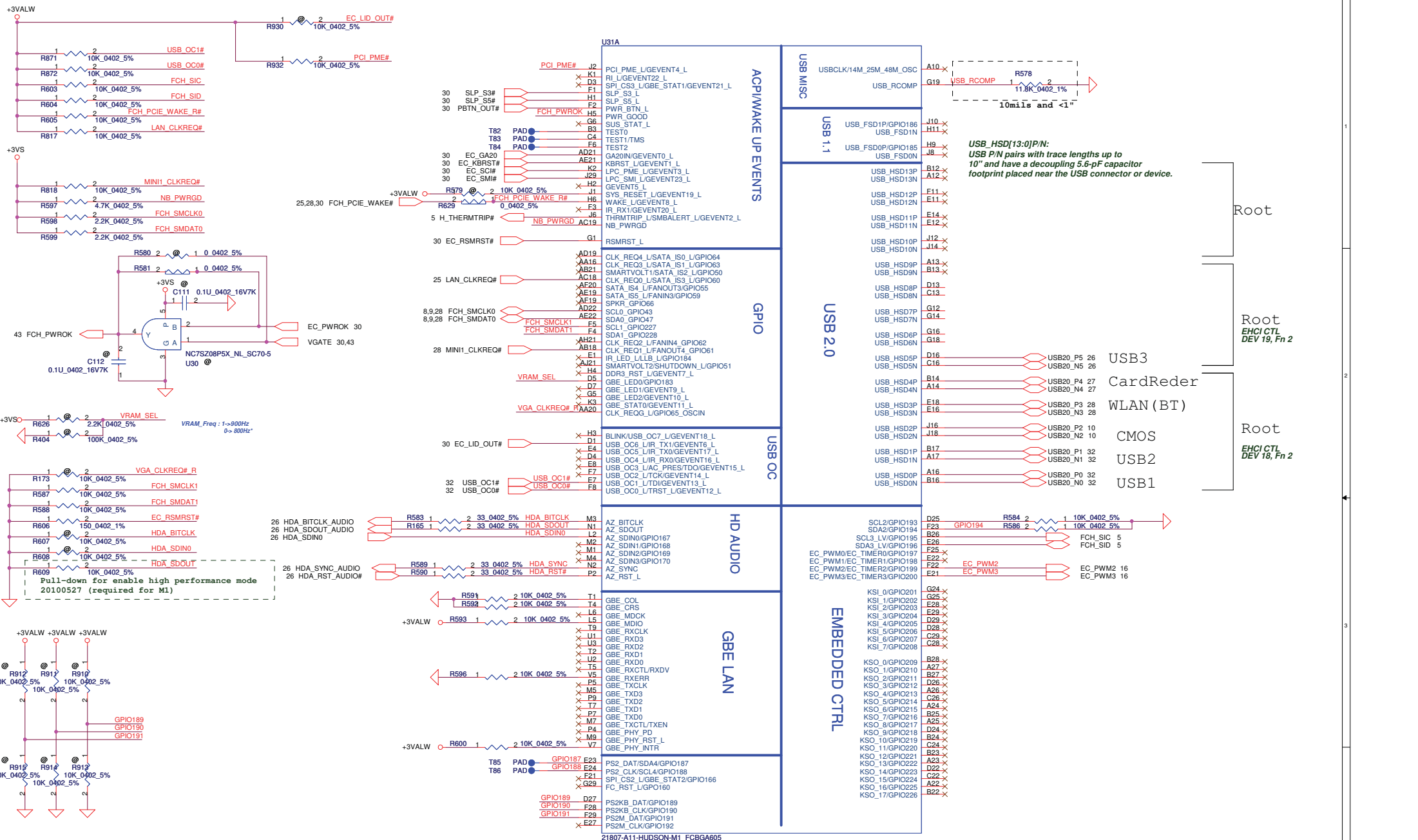
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For ESD request.



FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)
 FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)





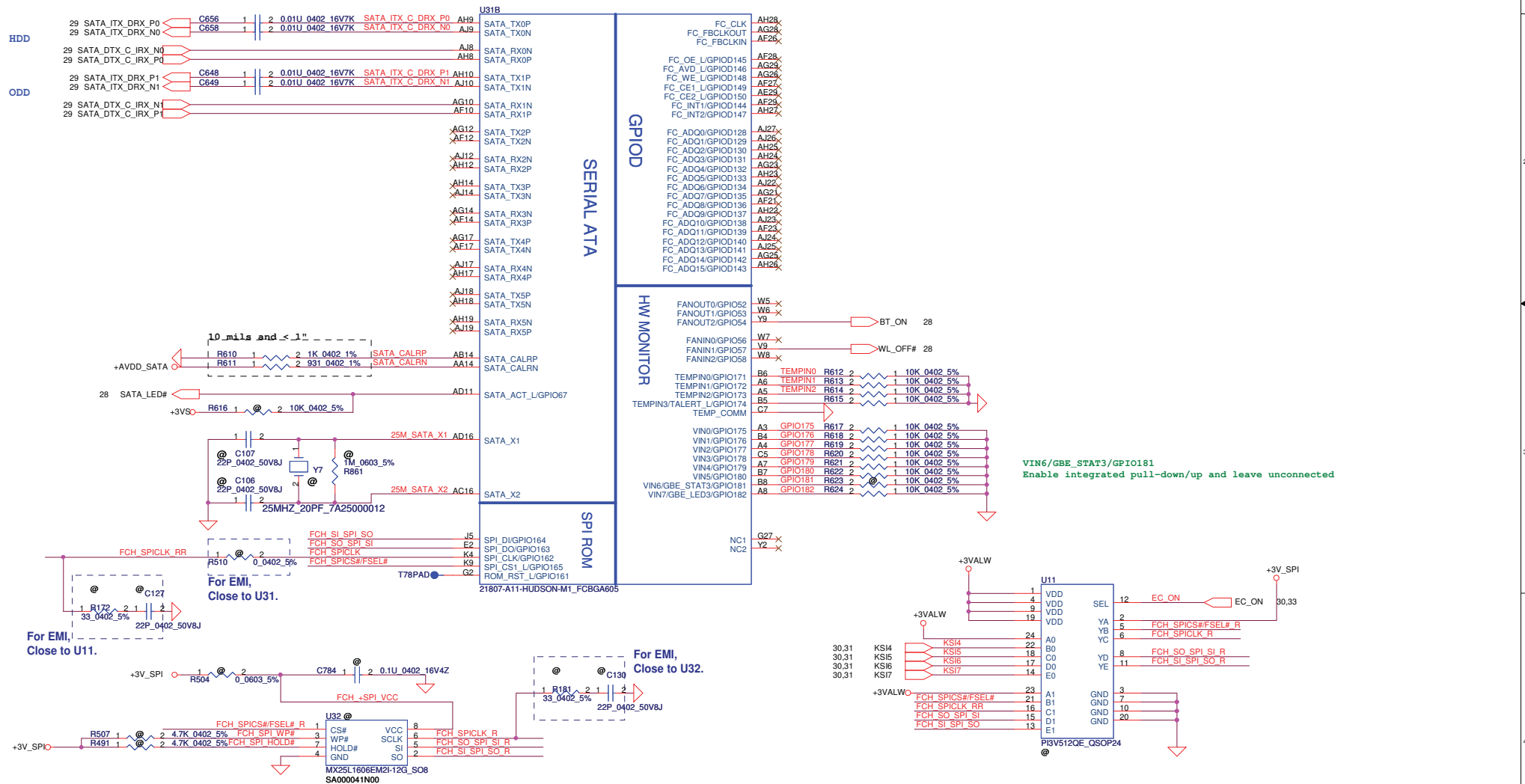
SKU_ID (GPIO189)	SKU_ID: 1→VGA* 0→UMA	GPIO	189	190	191
PX_FN (GPIO190)	PX_Function: 1→PX Enable* 0→PX Disable	UMA	0	0	1
PX_SEL (GPIO191)	PX_SEL: 1→PX 3.0* 0→PX 4.0	DISO	1	0	1
		PX3.0	1	1	1
		PX4.0	1	1	0

Do not Use In PBL50/60/70

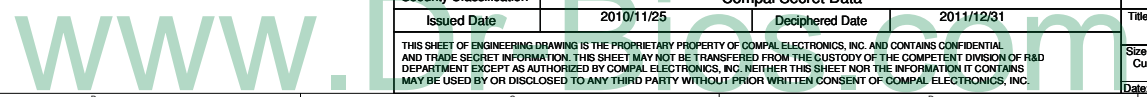
Security Classification	Compal Secret Data	
Issued Date	2010/11/25	Deciphered Date
		2011/12/31

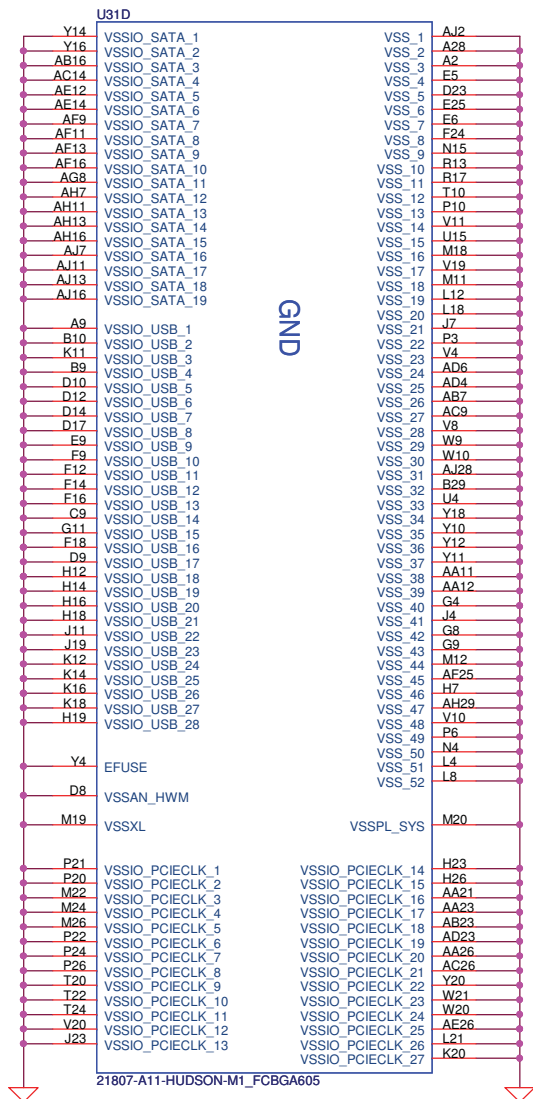
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Compal Electronics, Inc.		
Title		
P13-FCH HDA/USB/ACPI		
Size	Document Number	Rev
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Date:	Thursday, February 17, 2011	E Sheet 13 of 46



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Size	Document Number	Date	Wednesday, February 16, 2011	Rev 0.22
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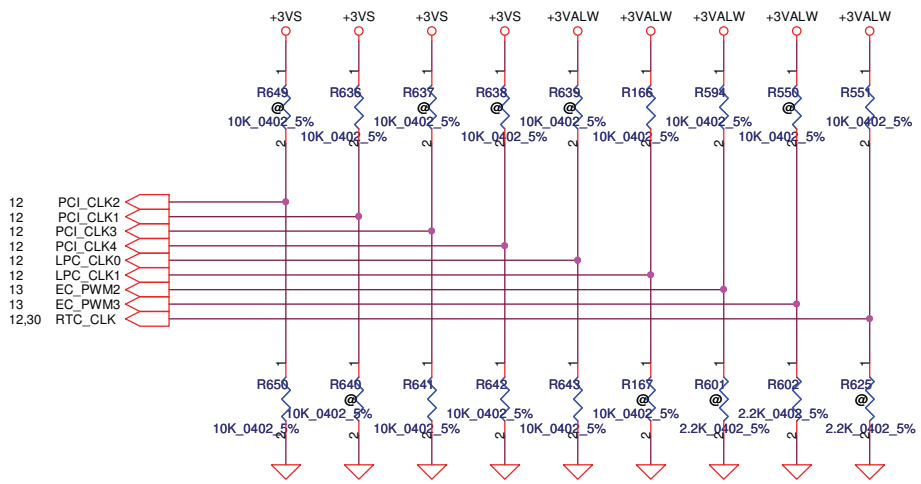


21807-A11-HUDSON-M1_FCBGA605

REQUIRED STRAPS

Check Internal PU/PD

PULL HIGH	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2	EC_PWM3
	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED Mode DEFAULT	LPC ROM (H,L) *	
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)	

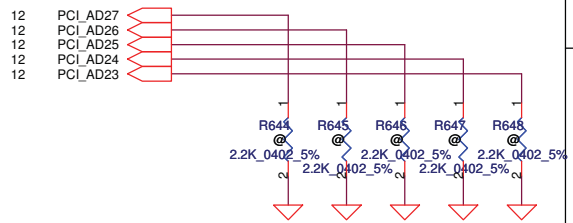


DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

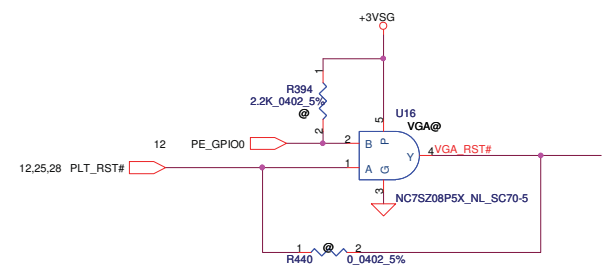
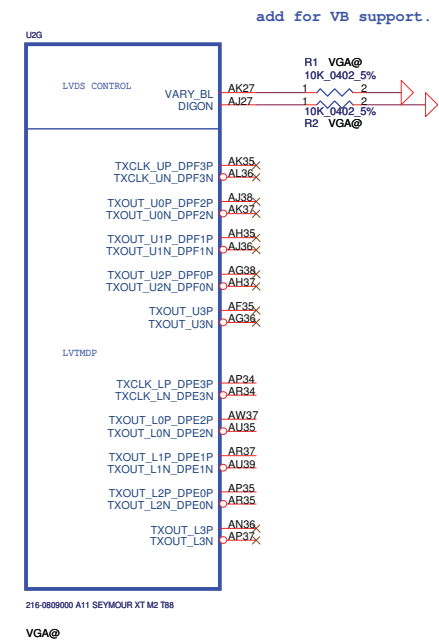
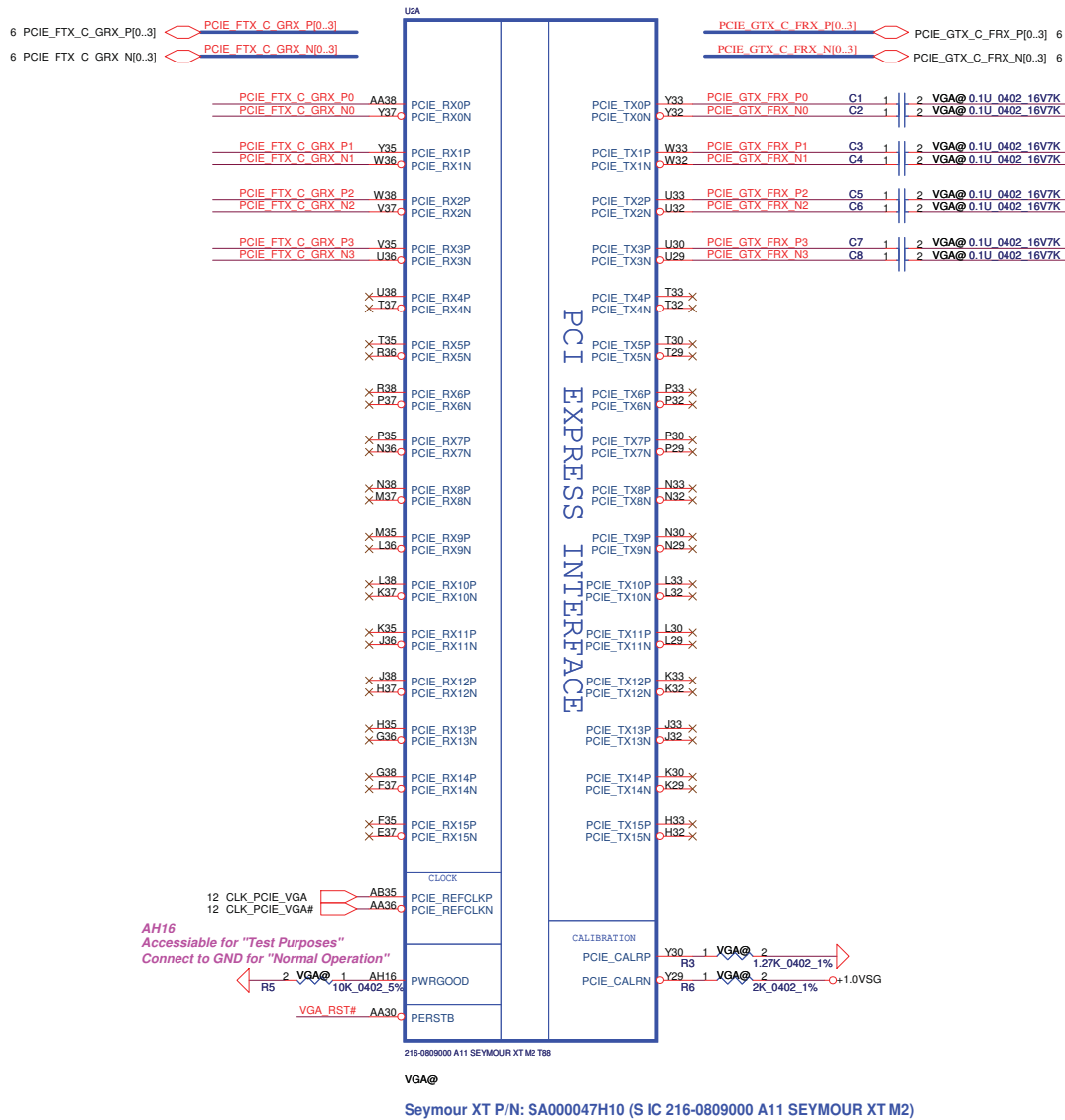
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function check default



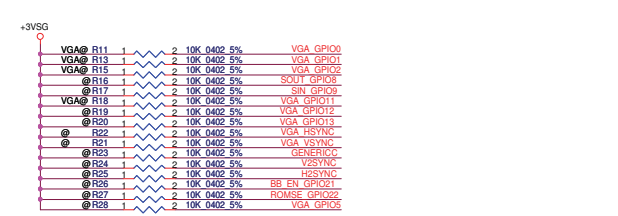
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/11/25	Deciphered Date	2011/12/31	Title P16-FCH-VSS/Strap		
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GFX PCIE LANE REVERSAL



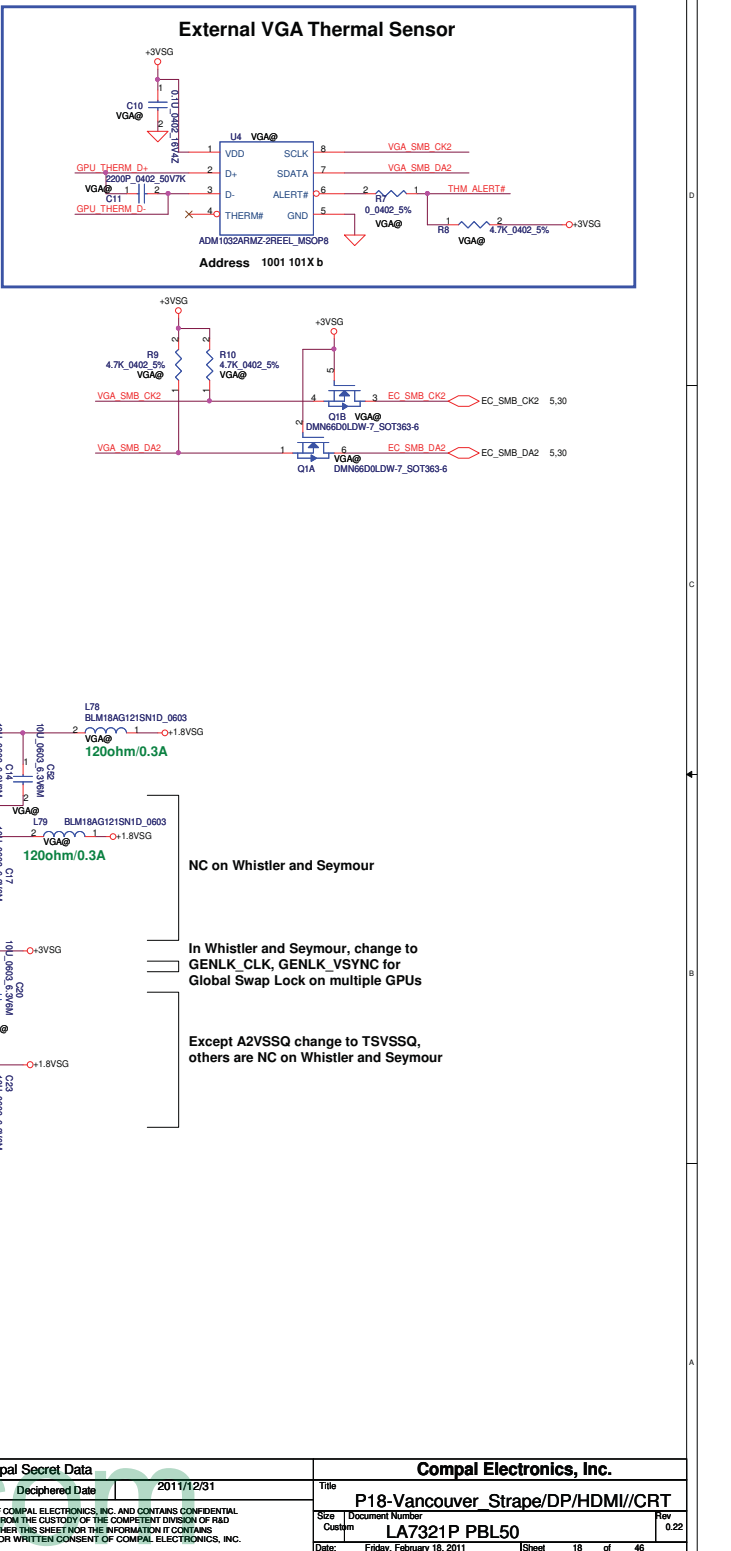
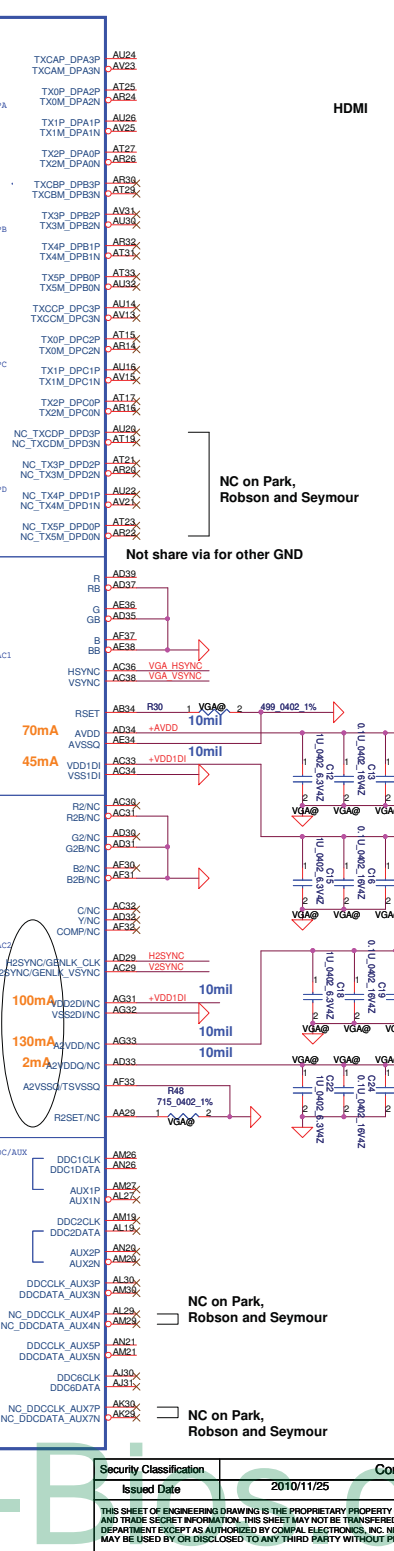
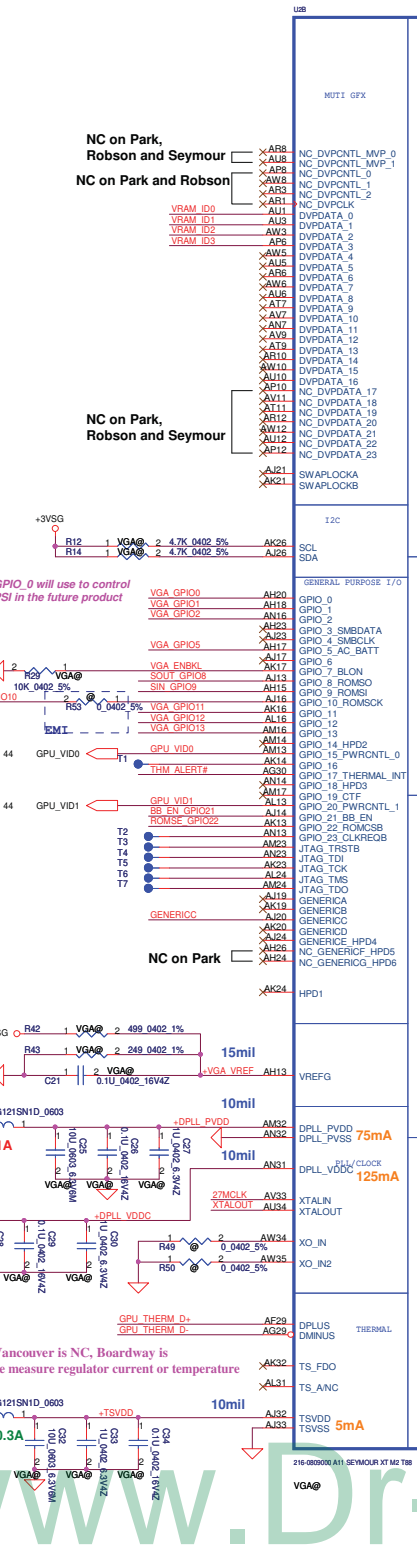
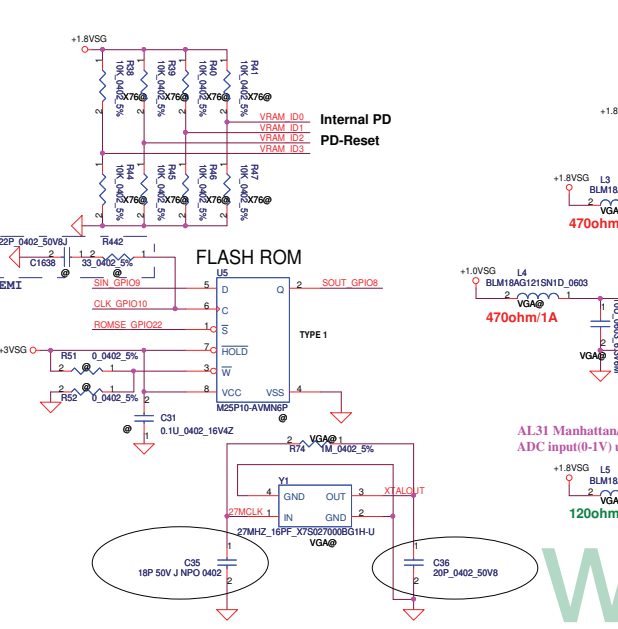
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Strap Name	Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9 VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13, 12, 11 (config 2, 1, 0) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2 0: Advertises the PCIe device as 2.5 GT/s capable at power-on 1: Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI
	GPIO8 GPIO21 GENERIC0 GPIO5	



Seymour(XT)

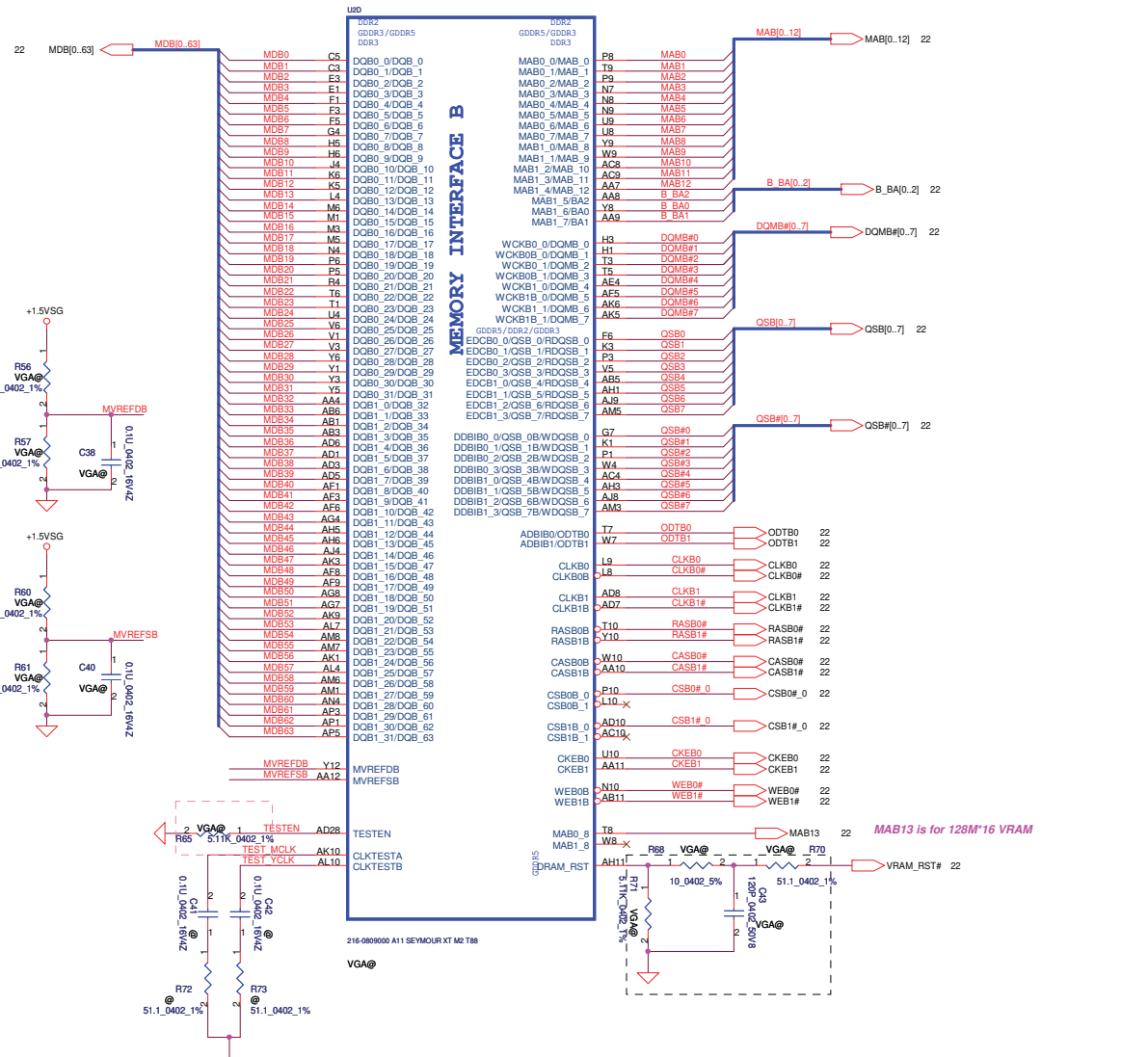
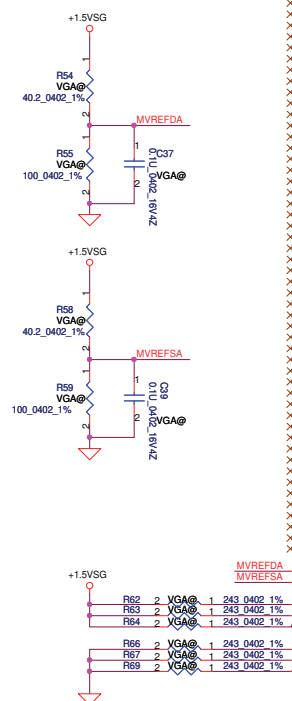
VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung 1G	X76L01	0	0	0	1
Hynix 1G	X76L02	0	1	0	1
Samsung 512M	X76L03	0	0	0	0
Hynix 512M	X76L04	0	1	0	0



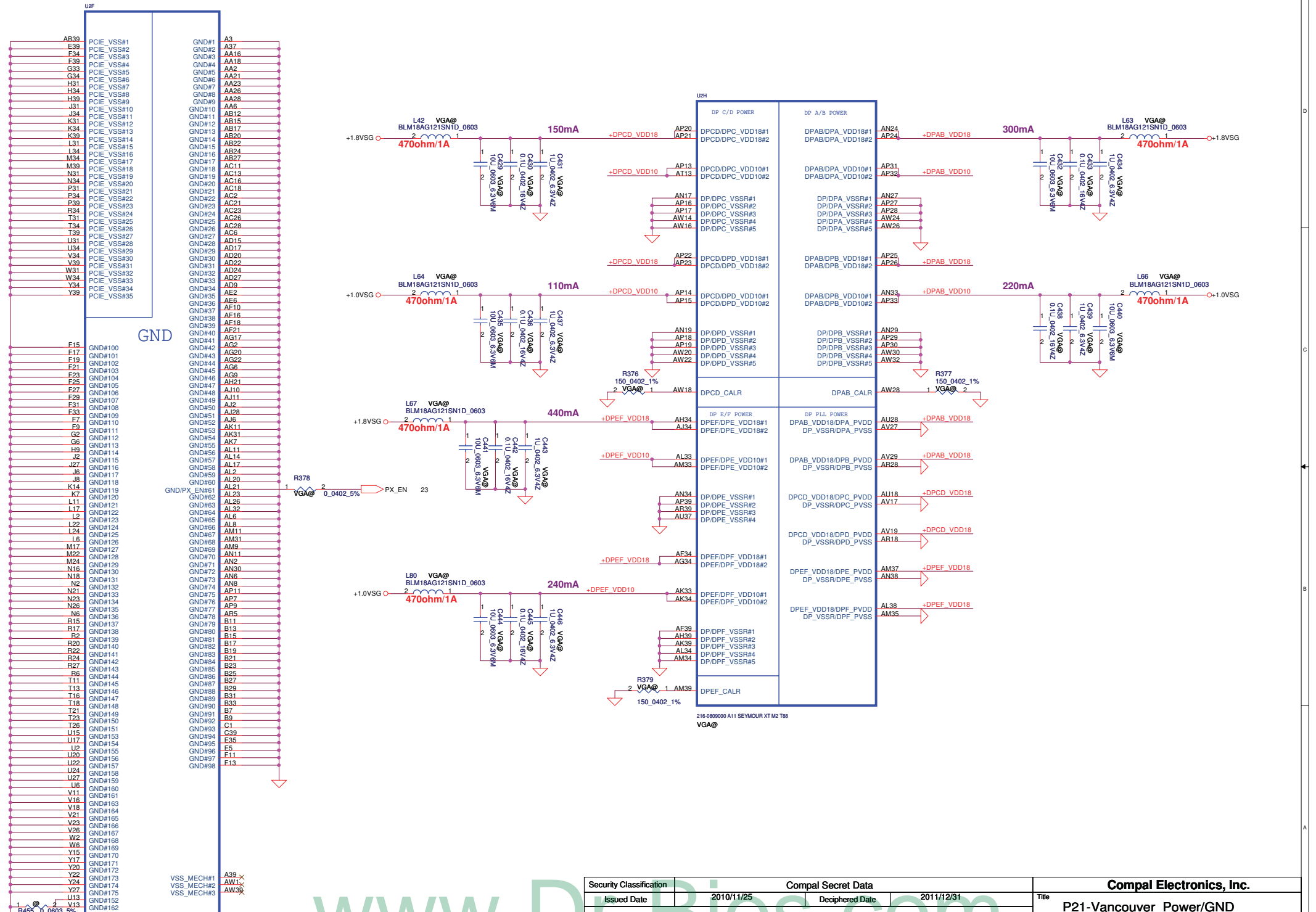
Robson, Seymour only support single channel memory (channel B only)

DDR2 GDDR3/GDDR5 DDR3		DDR2 GDDR3/GDDR3 DDR3	
C37	NC_DDA0_0/DDA_0	NC_MAA0_0/MAA_0	J23
C36	NC_DDA0_1/DDA_1	NC_MAA0_1/MAA_1	J24
A35	NC_DDA0_2/DDA_2	NC_MAA0_2/MAA_2	H24
E34	NC_DDA0_3/DDA_3	NC_MAA0_3/MAA_3	J24
C33	NC_DDA0_4/DDA_4	NC_MAA0_4/MAA_4	H36
D33	NC_DDA0_5/DDA_5	NC_MAA0_5/MAA_5	J26
F32	NC_DDA0_6/DDA_6	NC_MAA0_6/MAA_6	H21
C32	NC_DDA0_7/DDA_7	NC_MAA0_7/MAA_7	G21
D31	NC_DDA0_8/DDA_8	NC_MAA1_0/MAA_8	H19
F30	NC_DDA0_9/DDA_9	NC_MAA1_1/MAA_9	H20
A30	NC_DDA0_10/DDA_10	NC_MAA1_2/MAA_10	G16
C29	NC_DDA0_11/DDA_11	NC_MAA1_3/MAA_11	H13
F28	NC_DDA0_12/DDA_12	NC_MAA1_4/MAA_12	H16
C28	NC_DDA0_13/DDA_13	NC_MAA1_5/MAA_13_BA2	H16
A28	NC_DDA0_14/DDA_14	NC_MAA1_6/MAA_14_BA0	H17
E28	NC_DDA0_15/DDA_15	NC_MAA1_7/MAA_15_BA1	H17
D27	NC_DDA0_16/DDA_16		
F26	NC_DDA0_17/DDA_17	NC_WCKA0_0/DCMA_0	C32
C26	NC_DDA0_18/DDA_18	NC_WCKA0_1/DCMA_1	D23
A26	NC_DDA0_19/DDA_19	NC_WCKA0_2/DCMA_2	E22
E24	NC_DDA0_20/DDA_20	NC_WCKA0B_1/DCMA_3	C14
C24	NC_DDA0_21/DDA_21	NC_WCKA1_0/DCMA_4	A14
A24	NC_DDA0_22/DDA_22	NC_WCKA1B_0/DCMA_5	E10
E24	NC_DDA0_23/DDA_23	NC_WCKA1_1/DCMA_6	D9
C22	NC_DDA0_24/DDA_24	NC_WCKA1B_1/DCMA_7	
A22	NC_DDA0_25/DDA_25	NC_EDCA0_0/OSA_0/RDOSA_0	C34
F22	NC_DDA0_26/DDA_26	NC_EDCA0_1/OSA_1/RDOSA_1	D21
A20	NC_DDA0_27/DDA_27	NC_EDCA0_2/OSA_2/RDOSA_2	D25
C20	NC_DDA0_28/DDA_28	NC_EDCA0_3/OSA_3/RDOSA_3	E20
F20	NC_DDA0_29/DDA_29	NC_EDCA1_0/OSA_4/RDOSA_4	E16
D18	NC_DDA0_30/DDA_30	NC_EDCA1_1/OSA_5/RDOSA_5	H12
E18	NC_DDA0_31/DDA_31	NC_EDCA1_2/OSA_6/RDOSA_6	J10
C18	NC_DDA0_32/DDA_32	NC_EDCA1_3/OSA_7/RDOSA_7	D7
A18	NC_DDA1_1/DDA_33		
F18	NC_DDA1_2/DDA_34	NC_DDBIA0_0/OSA_0B/WDOSA_0	A34
C17	NC_DDA1_3/DDA_35	NC_DDBIA0_1/OSA_1B/WDOSA_1	E30
A16	NC_DDA1_4/DDA_36	NC_DDBIA0_2/OSA_2B/WDOSA_2	E26
E16	NC_DDA1_5/DDA_37	NC_DDBIA0_3/OSA_3B/WDOSA_3	C20
C15	NC_DDA1_6/DDA_38	NC_DDBIA0_4/OSA_4B/WDOSA_4	C16
A14	NC_DDA1_7/DDA_39	NC_DDBIA1_0/OSA_5B/WDOSA_5	H14
F14	NC_DDA1_8/DDA_40	NC_DDBIA1_1/OSA_6B/WDOSA_6	H14
D13	NC_DDA1_9/DDA_41	NC_DDBIA1_2/OSA_7B/WDOSA_7	J11
E12	NC_DDA1_10/DDA_42		
C12	NC_DDA1_11/DDA_43	NC_ADBIA0_0/ODTA0	J21
A12	NC_DDA1_12/DDA_44	NC_ADBIA1_0/ODTA1	G19
F12	NC_DDA1_13/DDA_45		
D11	NC_DDA1_14/DDA_46	NC_CLKA0	H27
E10	NC_DDA1_15/DDA_47	NC_CLKA0B	G27
C10	NC_DDA1_16/DDA_48		
A10	NC_DDA1_17/DDA_49	NC_CLKA1	J14
F10	NC_DDA1_18/DDA_50	NC_CLKA1B	H14
C09	NC_DDA1_19/DDA_51		
A09	NC_DDA1_20/DDA_52	NC_RASA0B	K23
F09	NC_DDA1_21/DDA_53	NC_RASA1B	K19
D09	NC_DDA1_22/DDA_54		
E09	NC_DDA1_23/DDA_55	NC_CASA0B	K20
C09	NC_DDA1_24/DDA_56	NC_CASA1B	K17
A09	NC_DDA1_25/DDA_57		
F09	NC_DDA1_26/DDA_58	NC_CSA0B_0	K24
D09	NC_DDA1_27/DDA_59	NC_CSA0B_1	K27
E09	NC_DDA1_28/DDA_60		
C09	NC_DDA1_29/DDA_61	NC_CSA1B_0	M13
A09	NC_DDA1_30/DDA_62	NC_CSA1B_1	K16
F09	NC_DDA1_31/DDA_63		
C08	NC_MVREFDA	NC_CKEA0	K21
A08	NC_MVREFSA	NC_CKEA1	J20
F08		NC_WEA0B	K26
D08		NC_WEA1B	L15
E08			
C08		NC_MAA0_8	H23
A08		NC_MAA1_8	J19

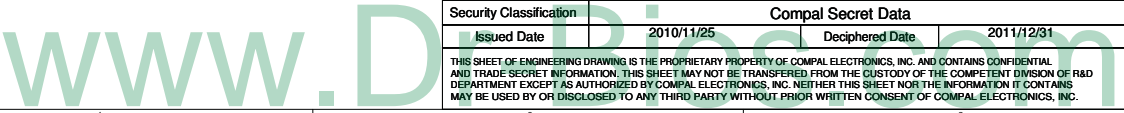
MEMORY INTERFACE A



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Title			Compal Electronics, Inc.
Sno			P19-Vancouver_Memory
CusNm			LA7321P PBL50
Date:	Tuesday, February 15, 2011	Sheet	19 of 46

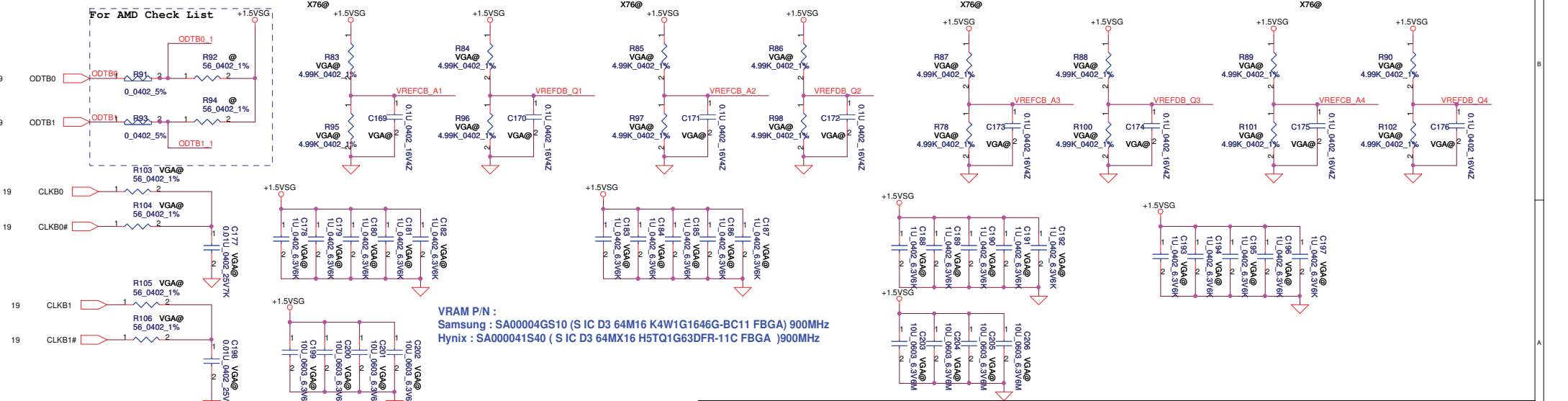
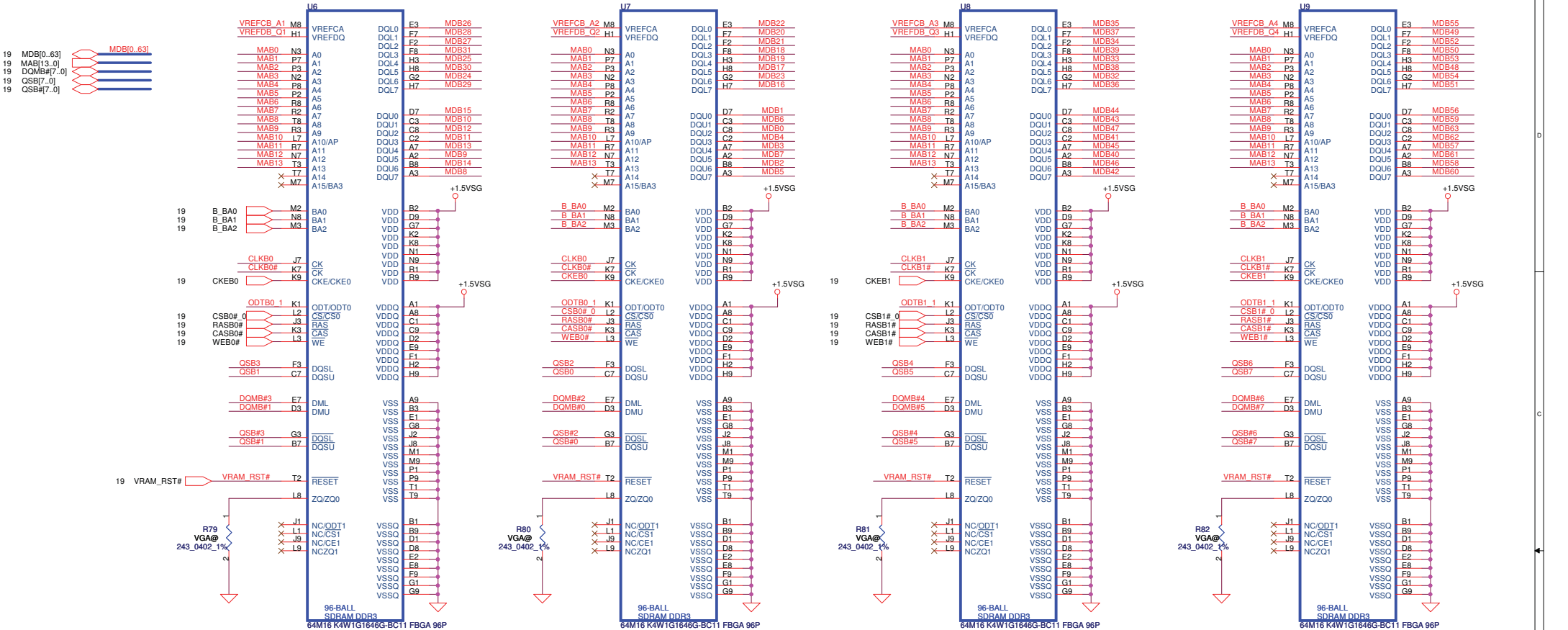


216-0809000 A11 SEYMOUR XT M2 T88
 VGA@



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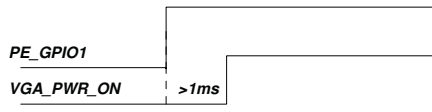
Compal Electronics, Inc.			
Title: P21-Vancouver Power/GND			
Size: Custom	Document Number: LA7321P PBL50	Rev: 0.22	
Date: Tuesday, February 15, 2011	Sheet: 21	of	46



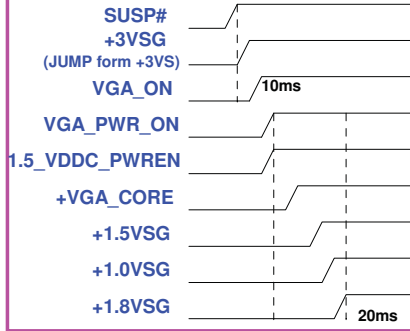
VRAM P/N :
 Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA) 900MHz
 Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA)900MHz

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For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON



Power Sequence of Whistler and Seymour

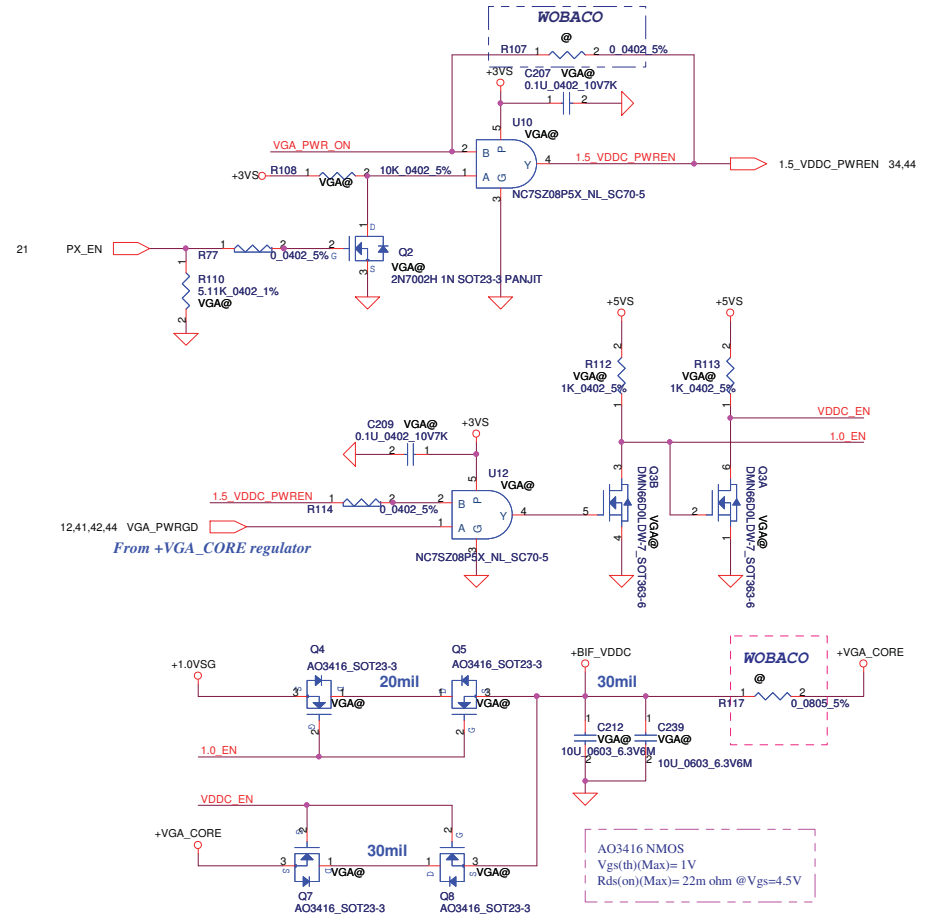


VGA Muxless with BACO Status Mapping table

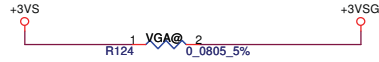
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

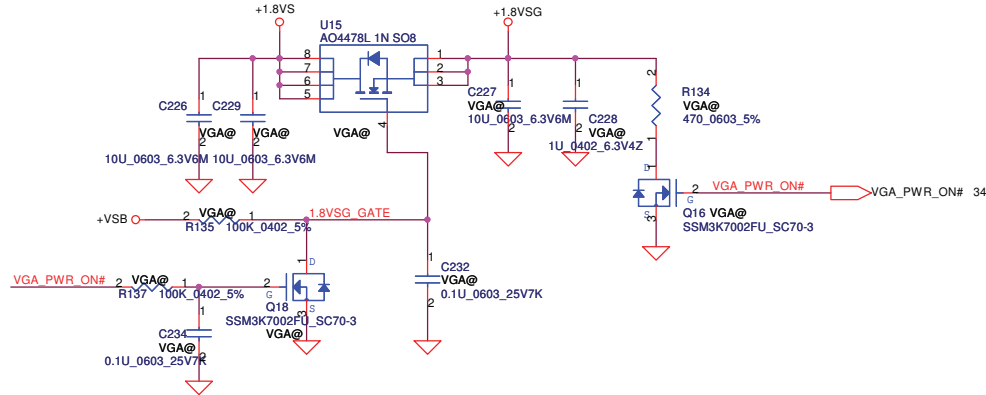
VGA_PWR_ON source signal	Graville	Whistler and Seymour
INT_VGAPWR_ON	VGA_PWR_ON	SUSP#
+3.3VSG	VGA_PWR_ON	VGA_PWR_ON
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN



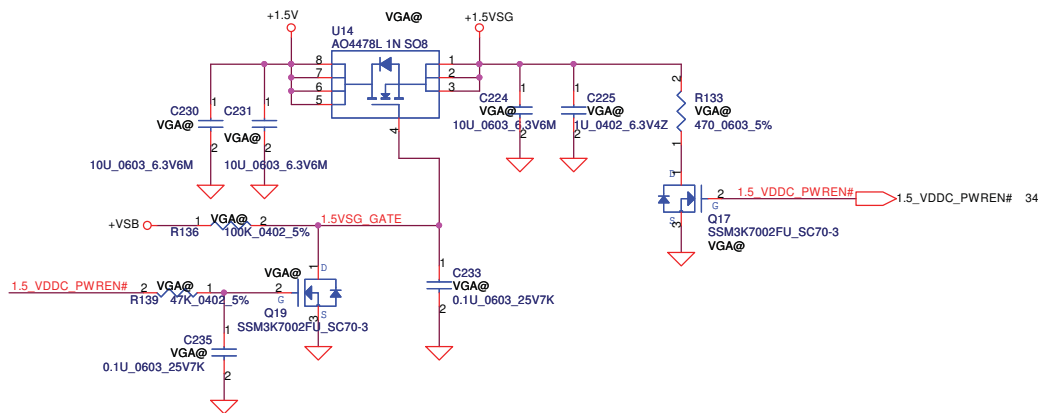
+3.3VS TO +3.3VSG



+1.8VS TO +1.8VSG

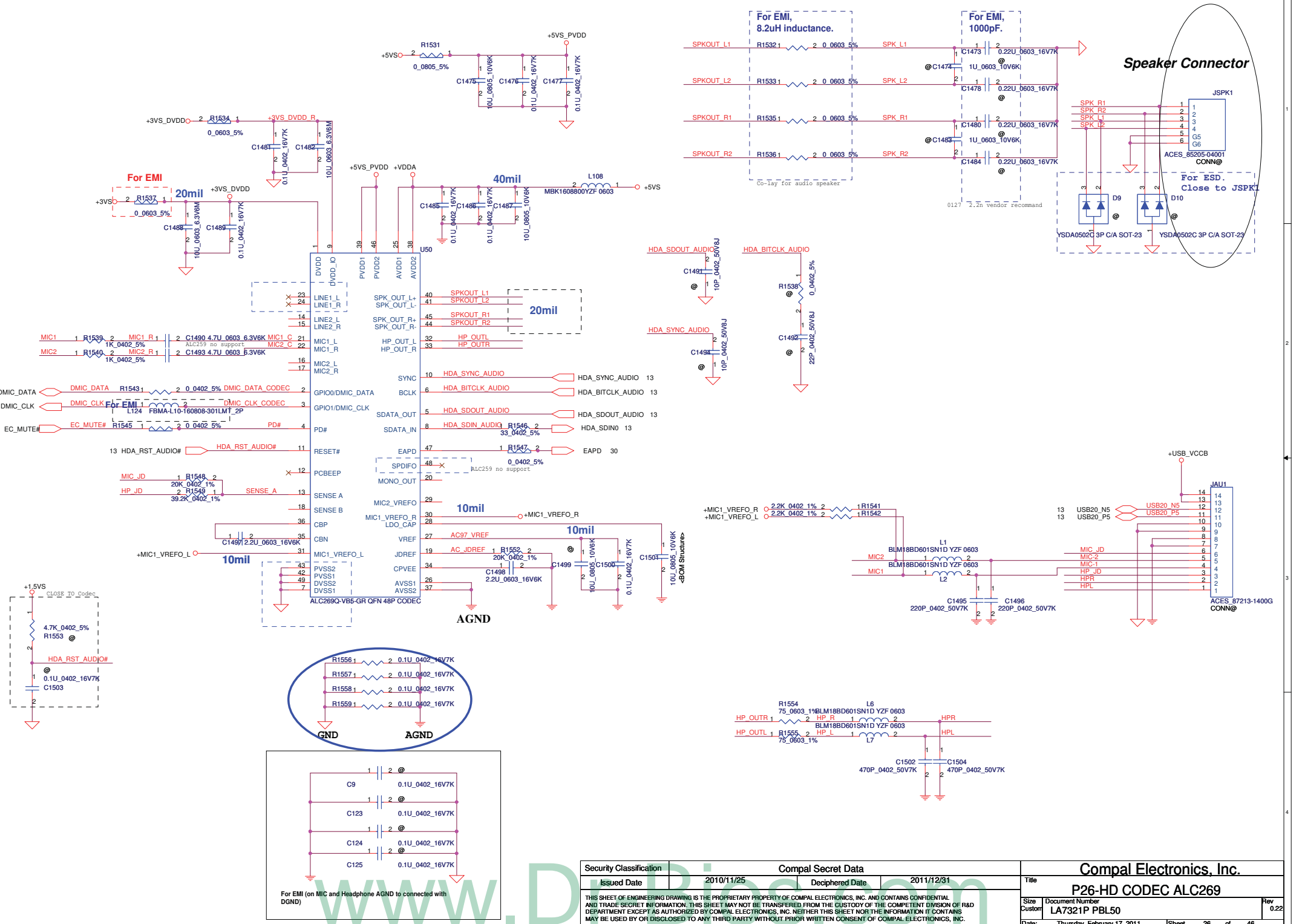


+1.5V TO +1.5VSG



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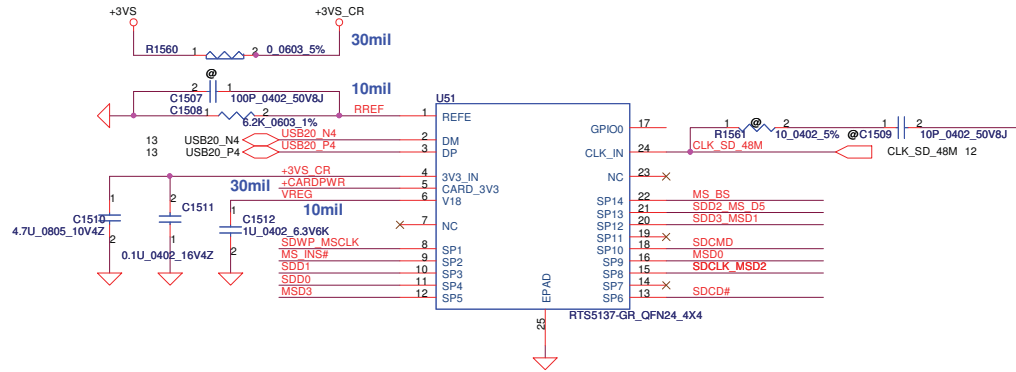


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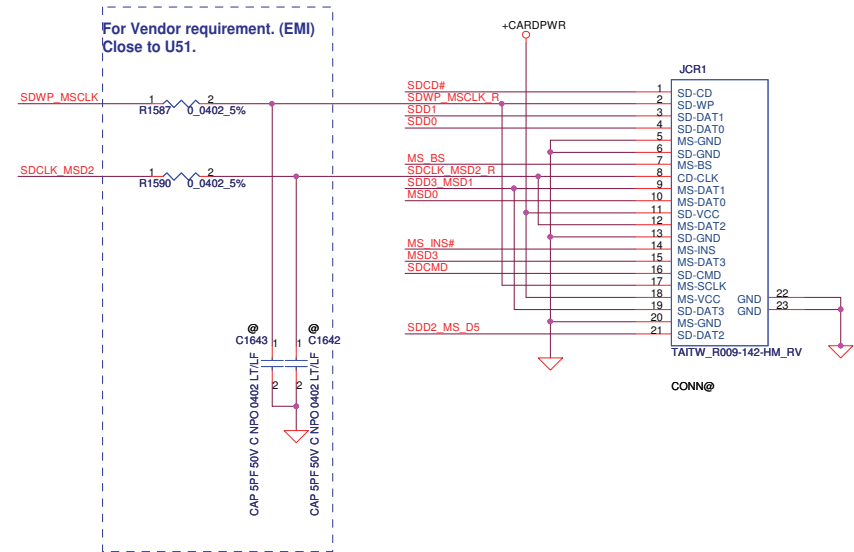
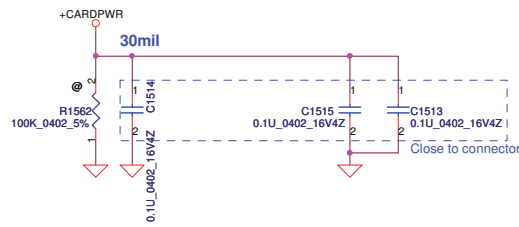
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Size		P26-HD CODEC ALC269	
Customer	Document Number	Rev	
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Card Reader RTS5137 (only SD/MMC/MS function)



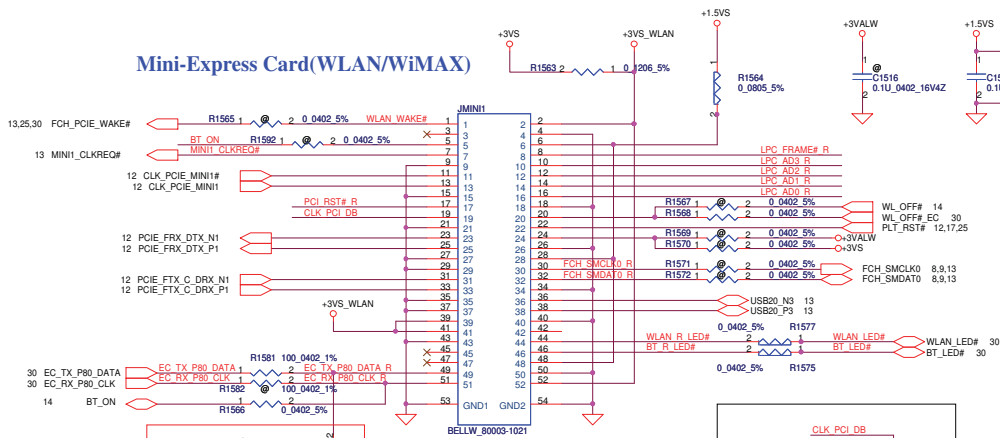
Card Reader Connector



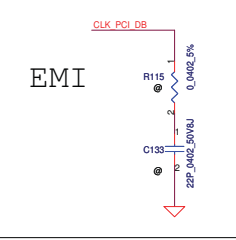
Security Classification	Compal Secret Data	
Issued Date	2010/11/25	Deciphered Date
		2011/12/31
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Compal Electronics, Inc.		
Title		
P27-RTS5137 Media Card Controller		
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Mini-Express Card for WLAN/WiMAX(Half)

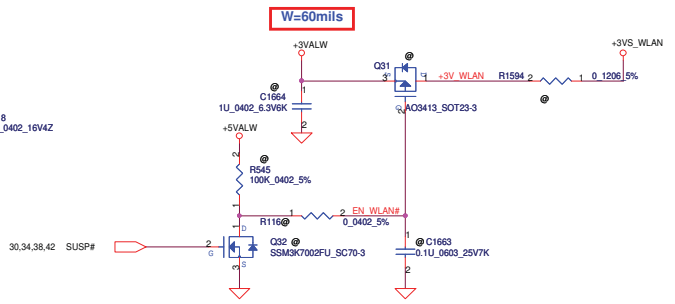


For EC to detect debug card insert.

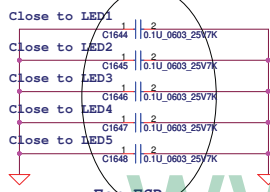
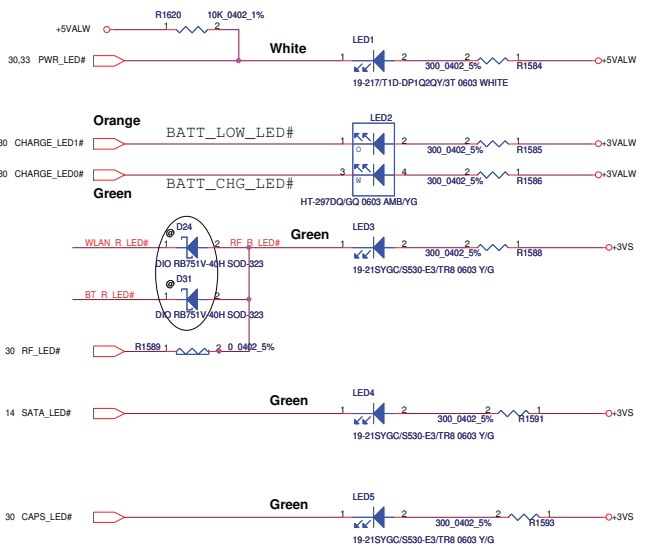


Reserve for SW mini-pcie debug card. Series resistors closed to KBC side.

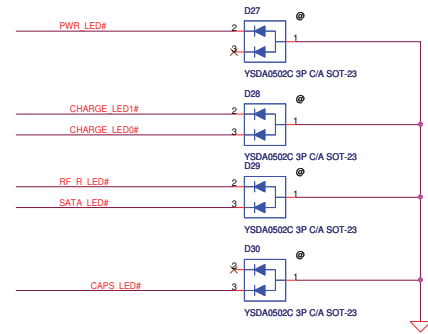
LPC_FRAME# R	R1673	1	0.0402 5%	LPC_FRAME#	12,30
LPC_AD3 R	R1674	1	0.0402 5%	LPC_AD3	12,30
LPC_AD2 R	R1675	1	0.0402 5%	LPC_AD2	12,30
LPC_AD1 R	R1676	1	0.0402 5%	LPC_AD1	12,30
LPC_AD0 R	R1677	1	0.0402 5%	LPC_AD0	12,30
PLT_RST#	R1678	1	0.0402 5%	PLT_RST#	12,17,25
CLK_PCIE_DB	R1679	1	0.0402 5%	CLK_PCIE_DB	12



LED

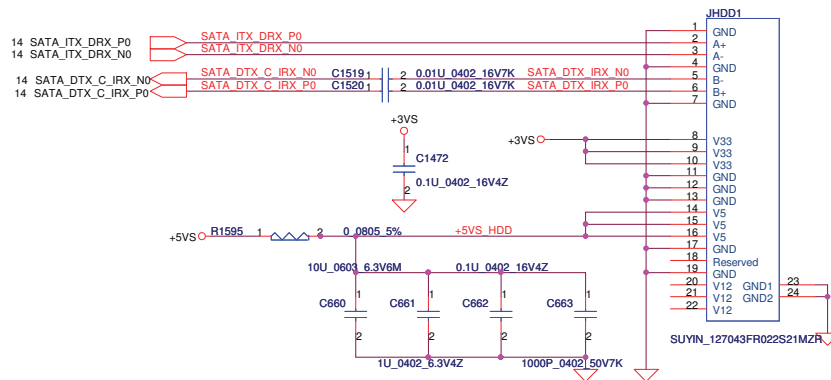


For ESD
Cap to LED gap is 1.2mm.

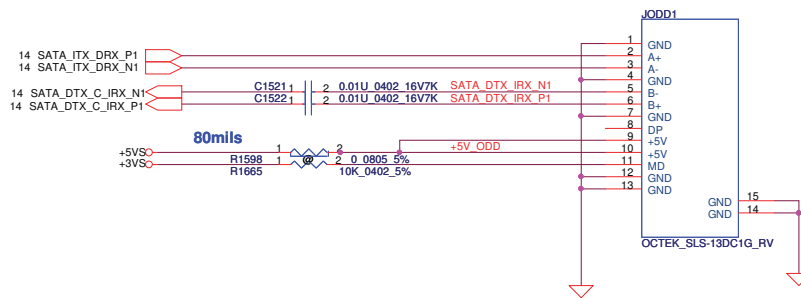


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SATA HDD Conn.

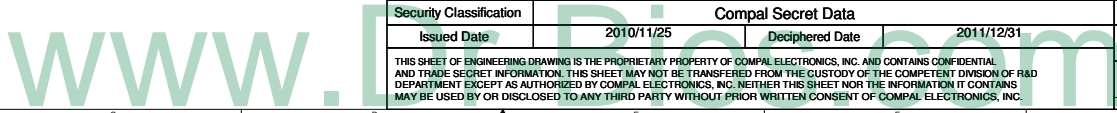


SATA ODD FFC Conn.

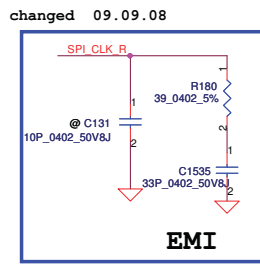
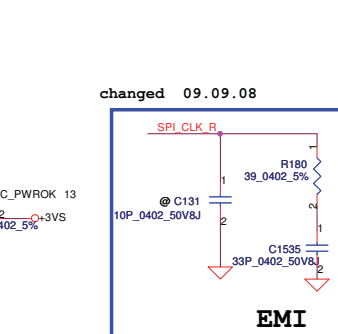
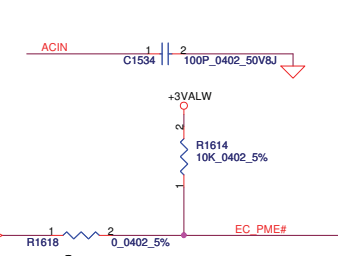
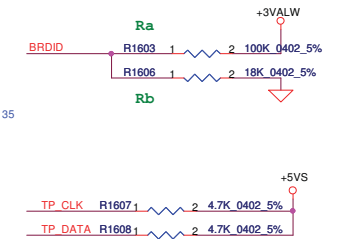
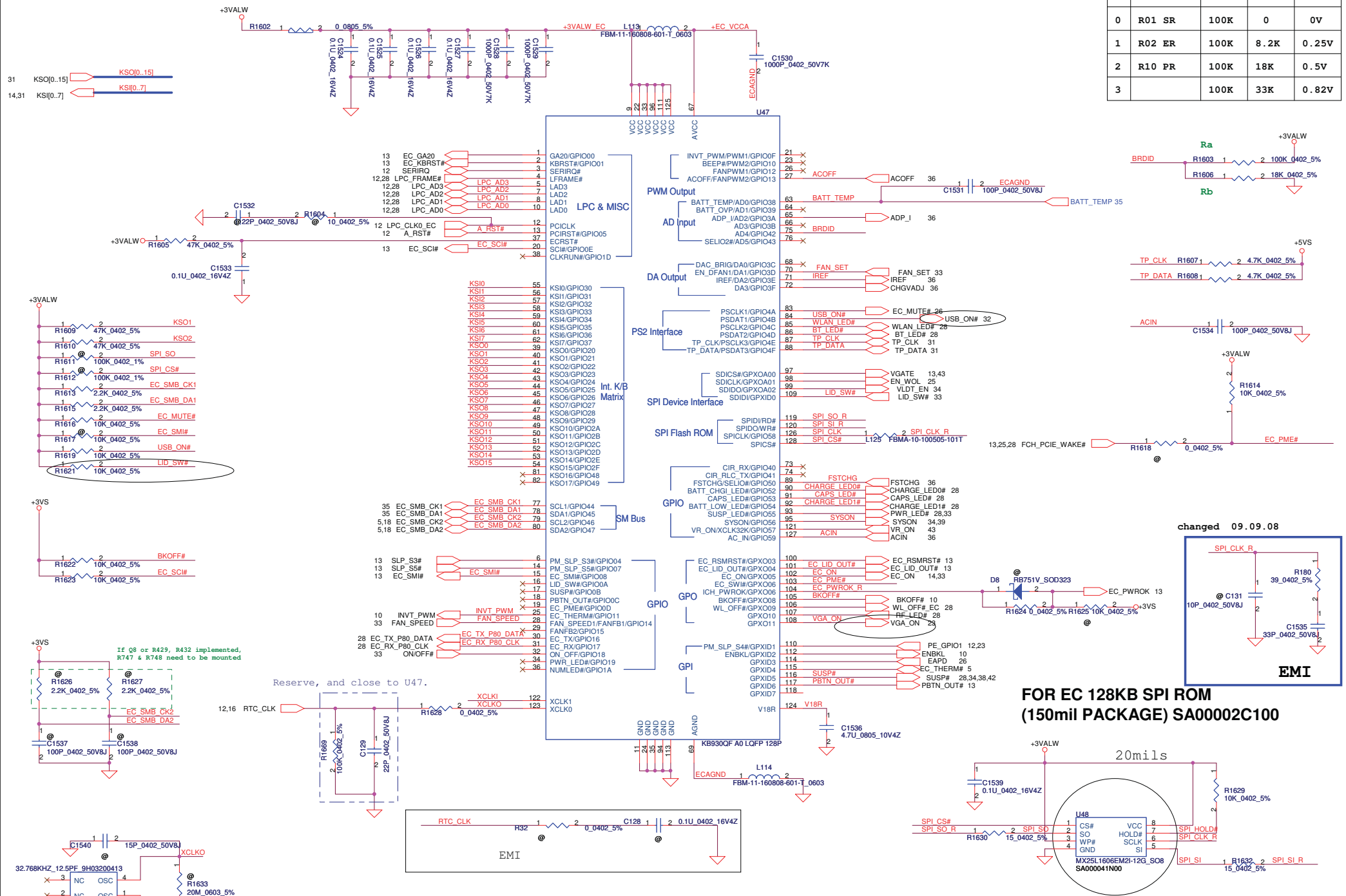


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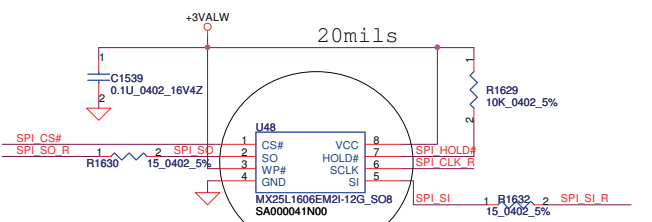
Compal Electronics, Inc. P29-HDD & ODD CONN		
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 PR	100K	18K	0.5V
3		100K	33K	0.82V



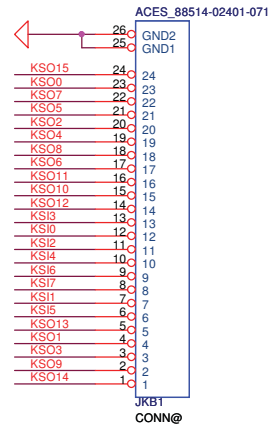
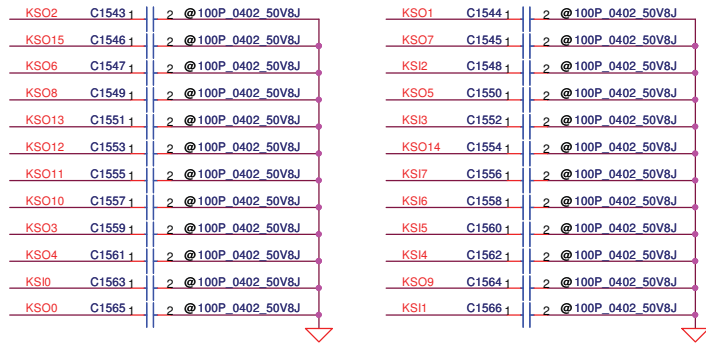
FOR EC 128KB SPI ROM (150mil PACKAGE) SA00002C100



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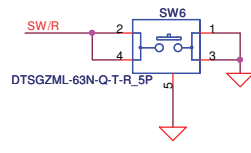
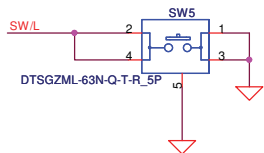
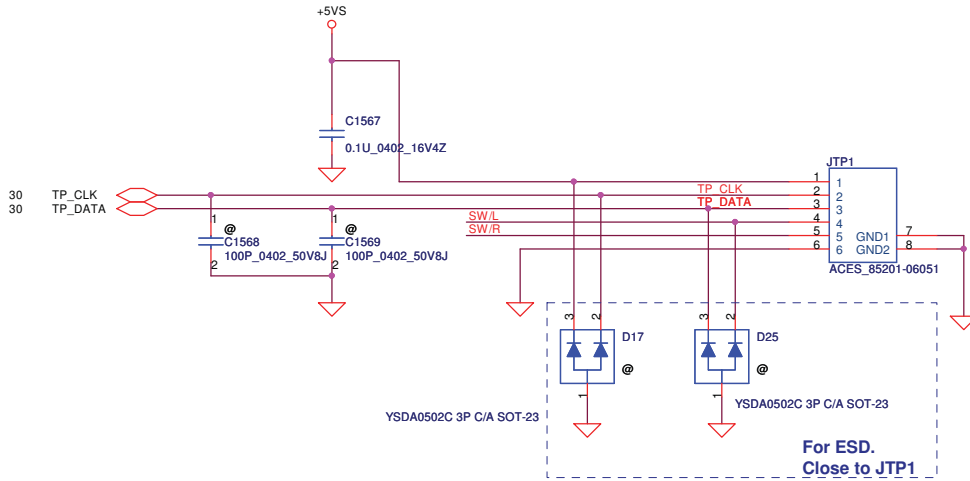
INT_KBD Conn.

KS[0..7] 14,30
 KSO[0..15] 30



CONN PIN define need double check

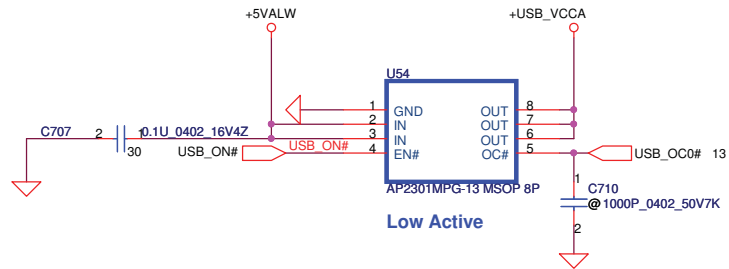
To TP/B Conn.



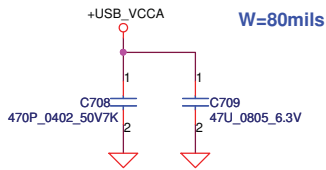
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WWW

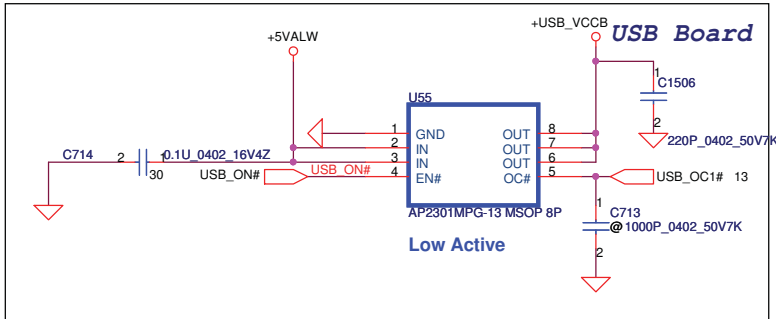
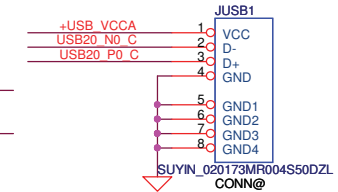
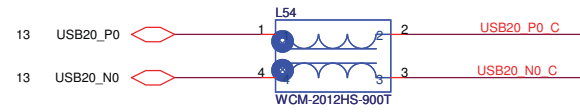
Left USB1 Conn.



Low Active

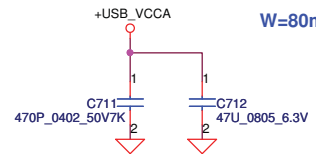


W=80mils

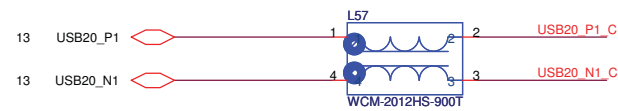


Low Active

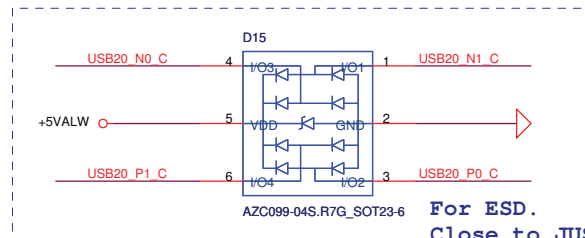
Left USB2 Conn.



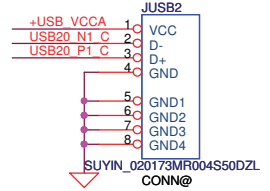
W=80mils



EMI request

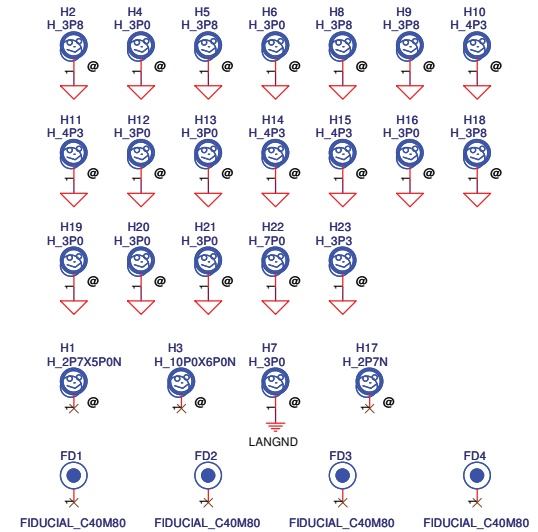
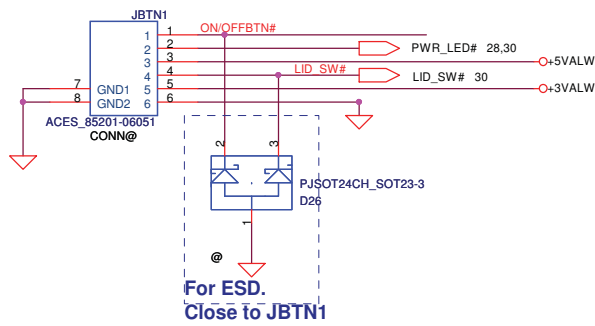
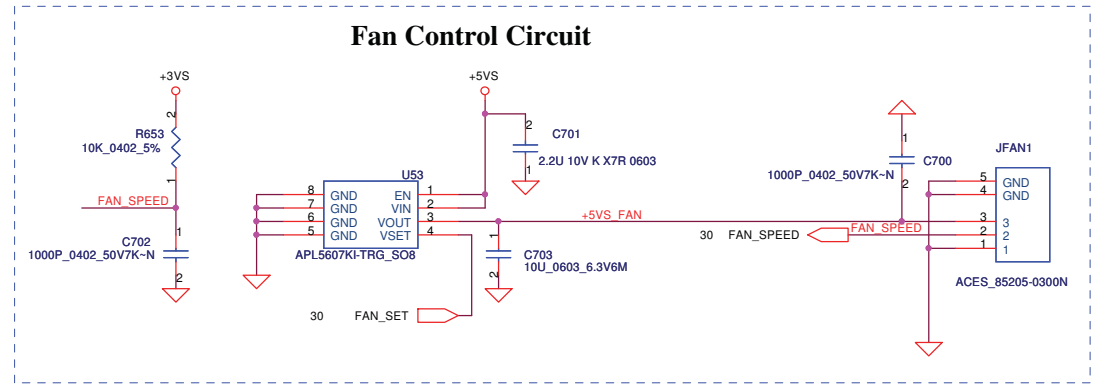
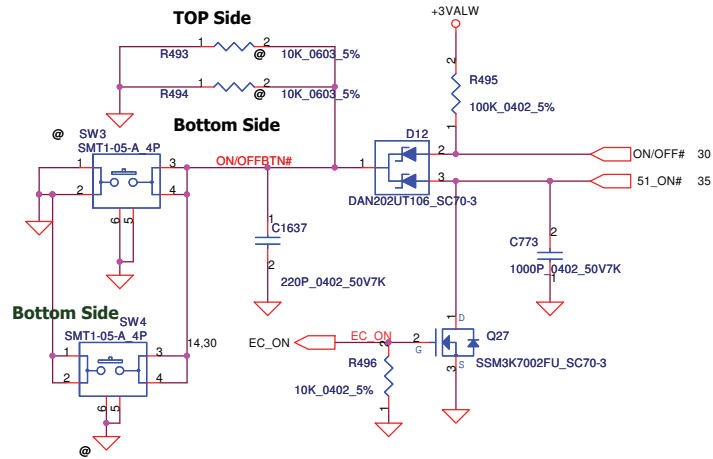


For ESD. Close to JUSB1, JUSB2



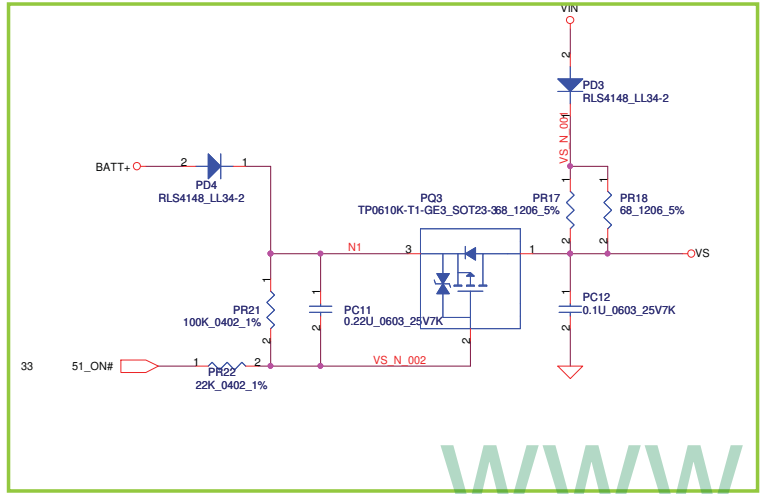
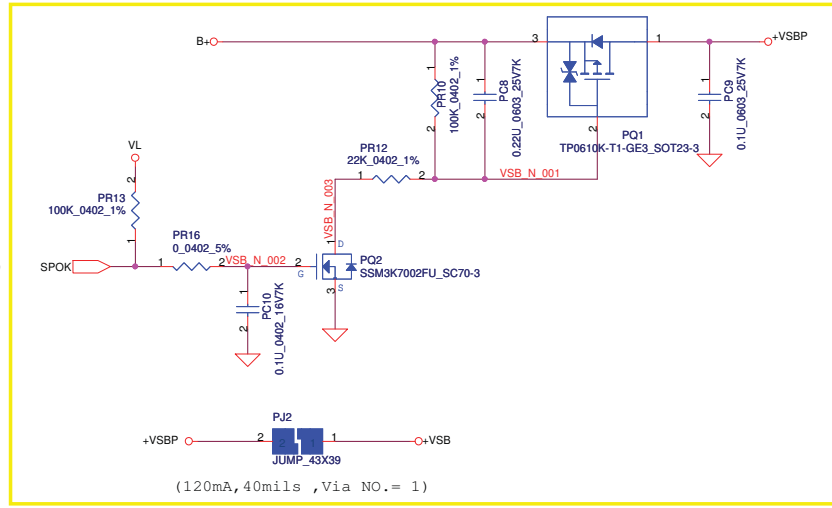
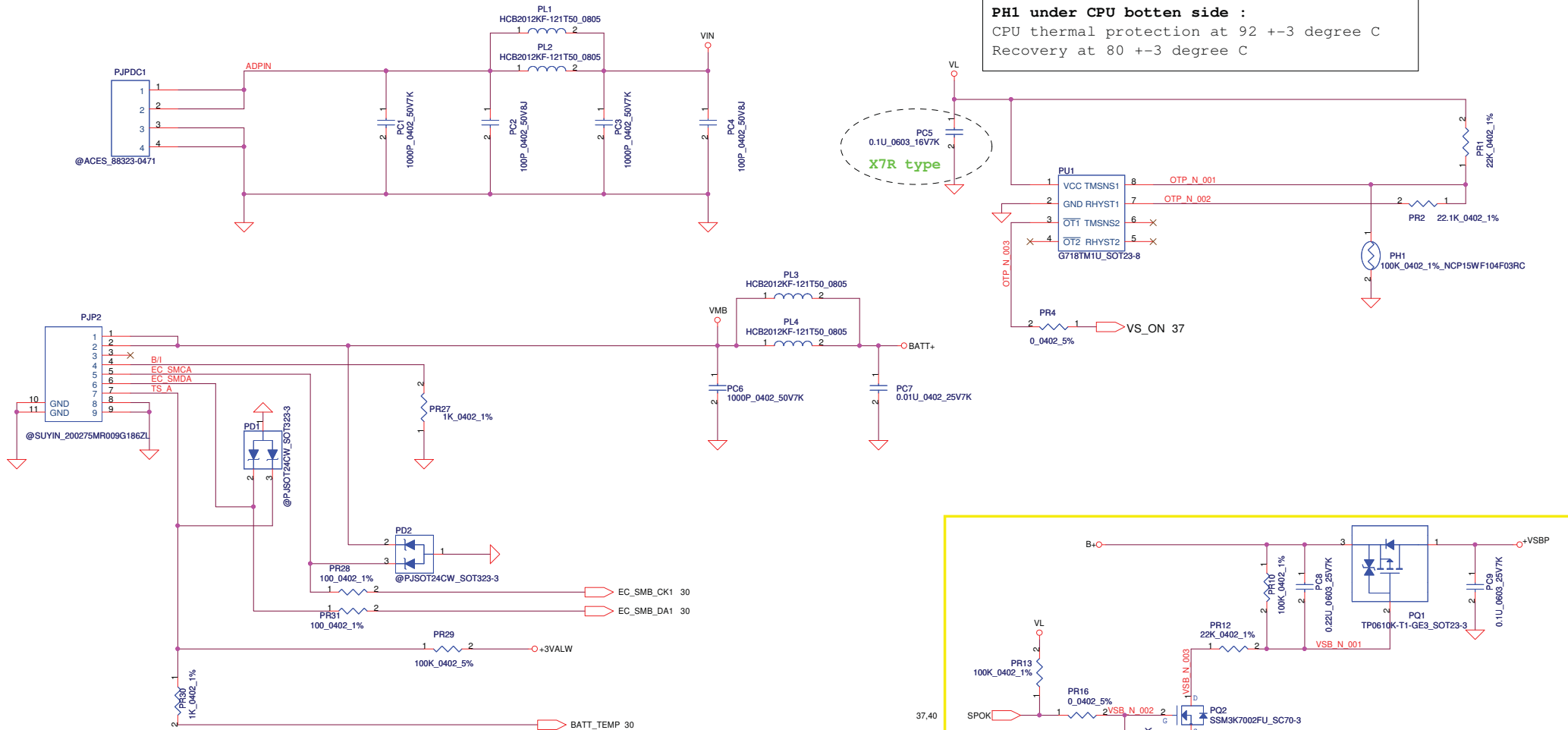
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ON/OFF switch **Power Button**

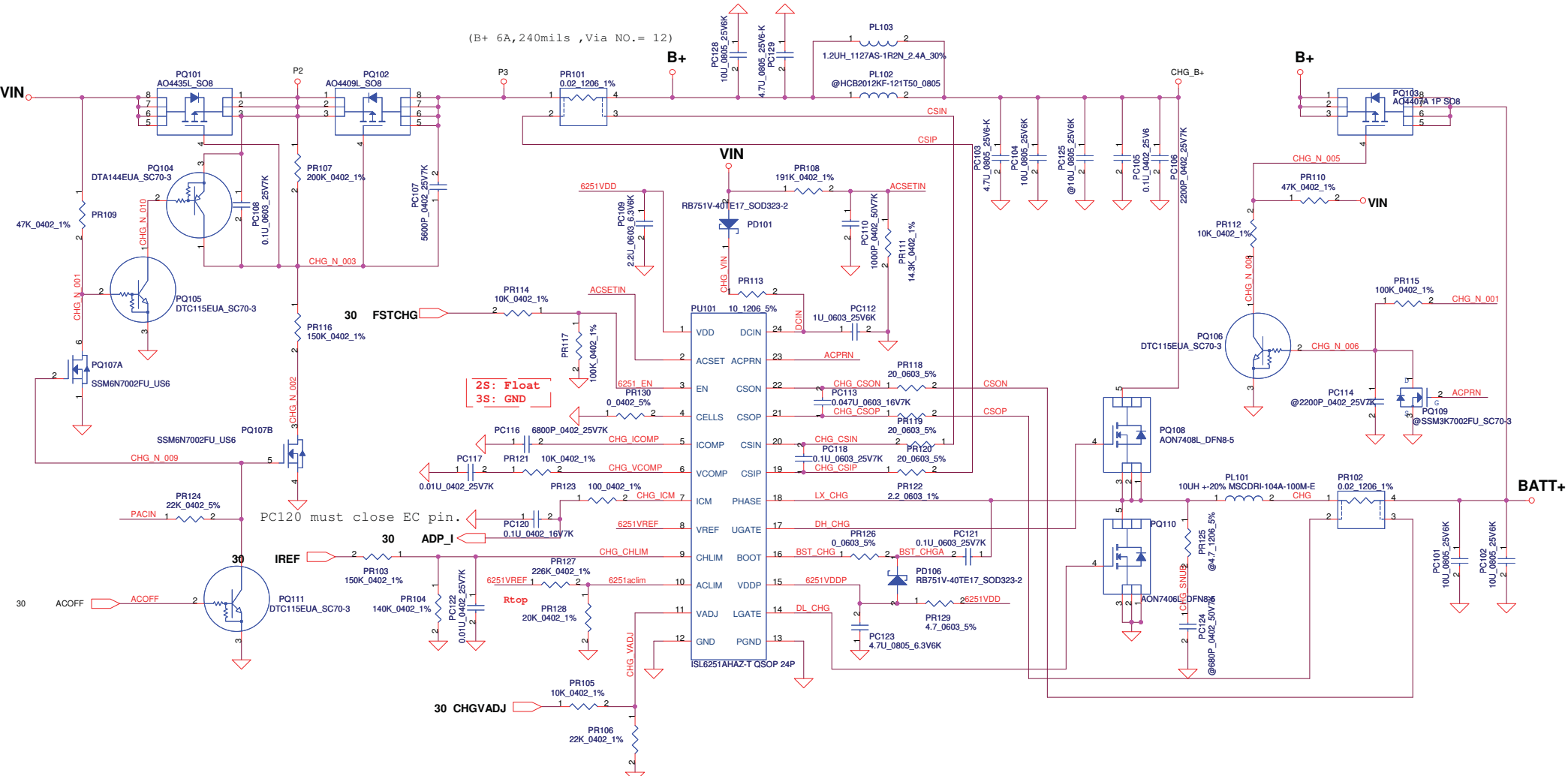


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PH1 under CPU botten side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C



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(B+ 6A, 240mils, Via NO.= 12)

2S: Float
3S: GND

PC120 must close EC pin.

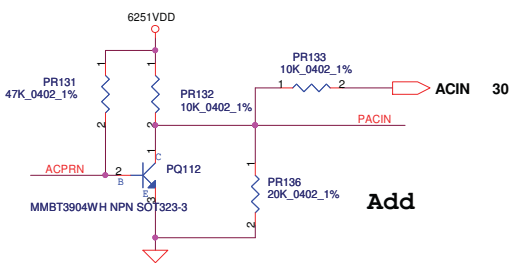
30 CHGVADJ

CP= 85%*Iada;
 Iada=0~4.737A (90W); CP=4.03A; where Racdet=0.020ohm, where Rtop=12.4K
 90W for Dis: Rtop: SD00000AJ80
 Iada=0~3.421A (65W); CP=2.91A; where Racdet=0.020ohm, where Rtop=226K
 65W for UMA: Rtop: SD034226380
 Astro2010_01_15 need confirm P/N

CP mode
 $V_{acli} = V_{REF} * (R_{bot} / (R_{int} + R_{top} / (R_{int} + R_{bot})))$
 when 90W $V_{acli} = 2.39 * (20K / (152K + (20K / (152K + 12.4K / (152K)))) = 1.44966V$
 when 65W $V_{acli} = 2.39 * (20K / (152K + (20K / (152K + 226K / (152K)))) = 0.38914V$
 $I_{input} = (1 / Racdet) * (0.05 * V_{acli} / V_{REF} + 0.05)$
 when 90W, $I_{input} = (1 / 0.02) * (0.05 * 1.44966 / 2.39 + 0.05) = 4.02A$
 when 65W, $I_{input} = (1 / 0.02) * (0.05 * 0.38914 / 2.39 + 0.05) = 2.92A$

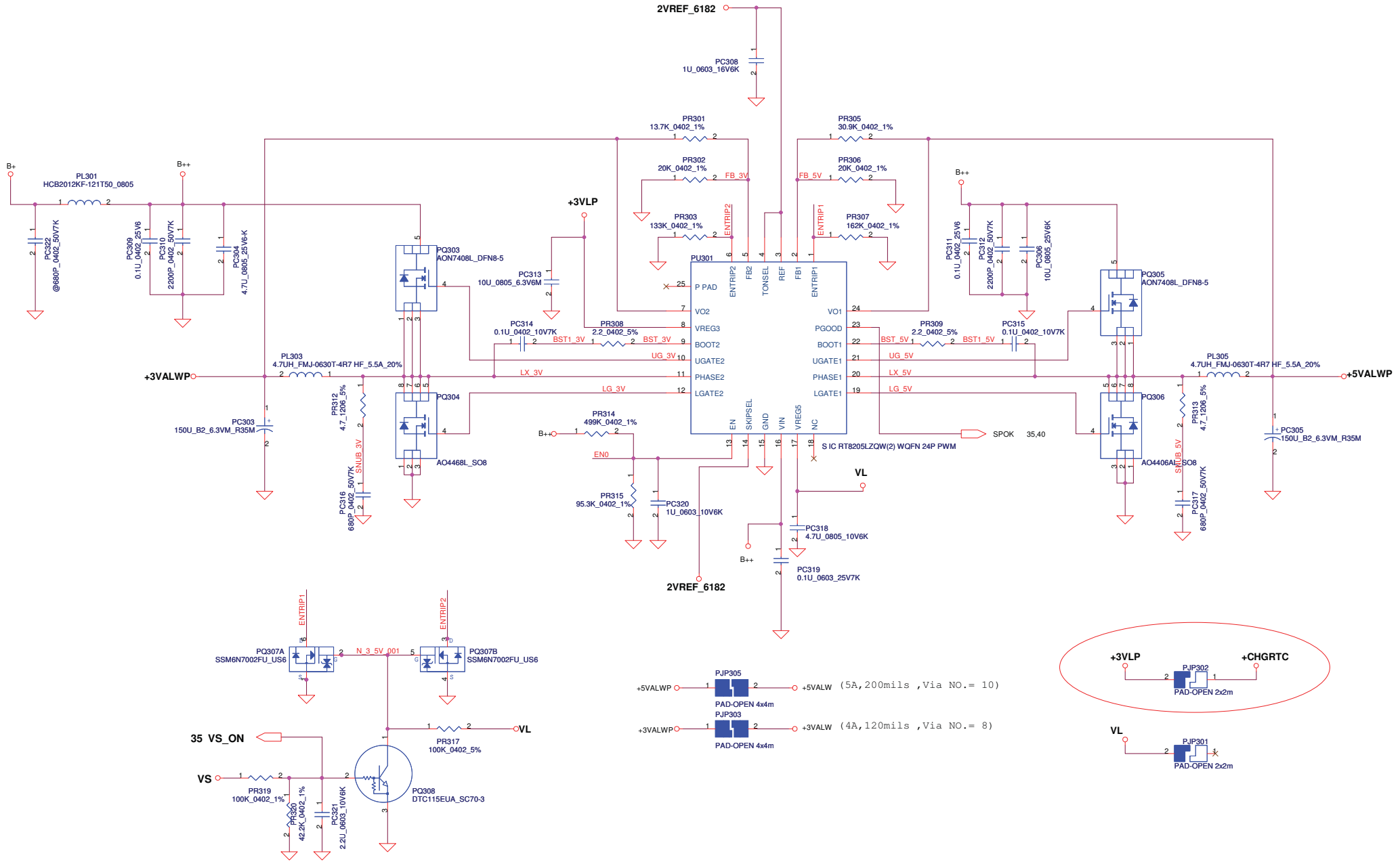
CC=0.25A~3A
 IREF=1.016*Icharge
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V

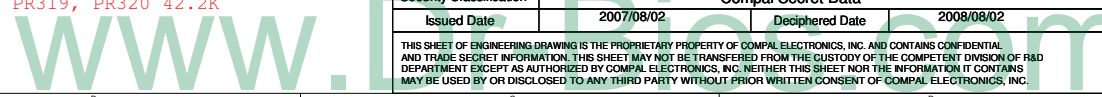


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Title			
CHARGER			
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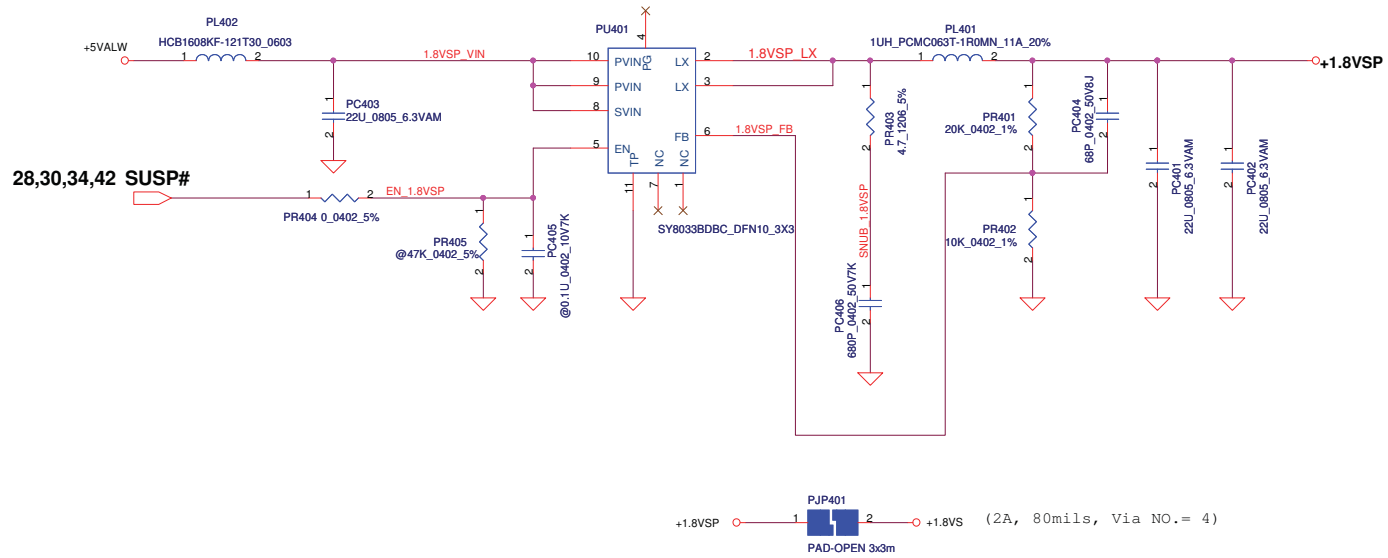


EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K



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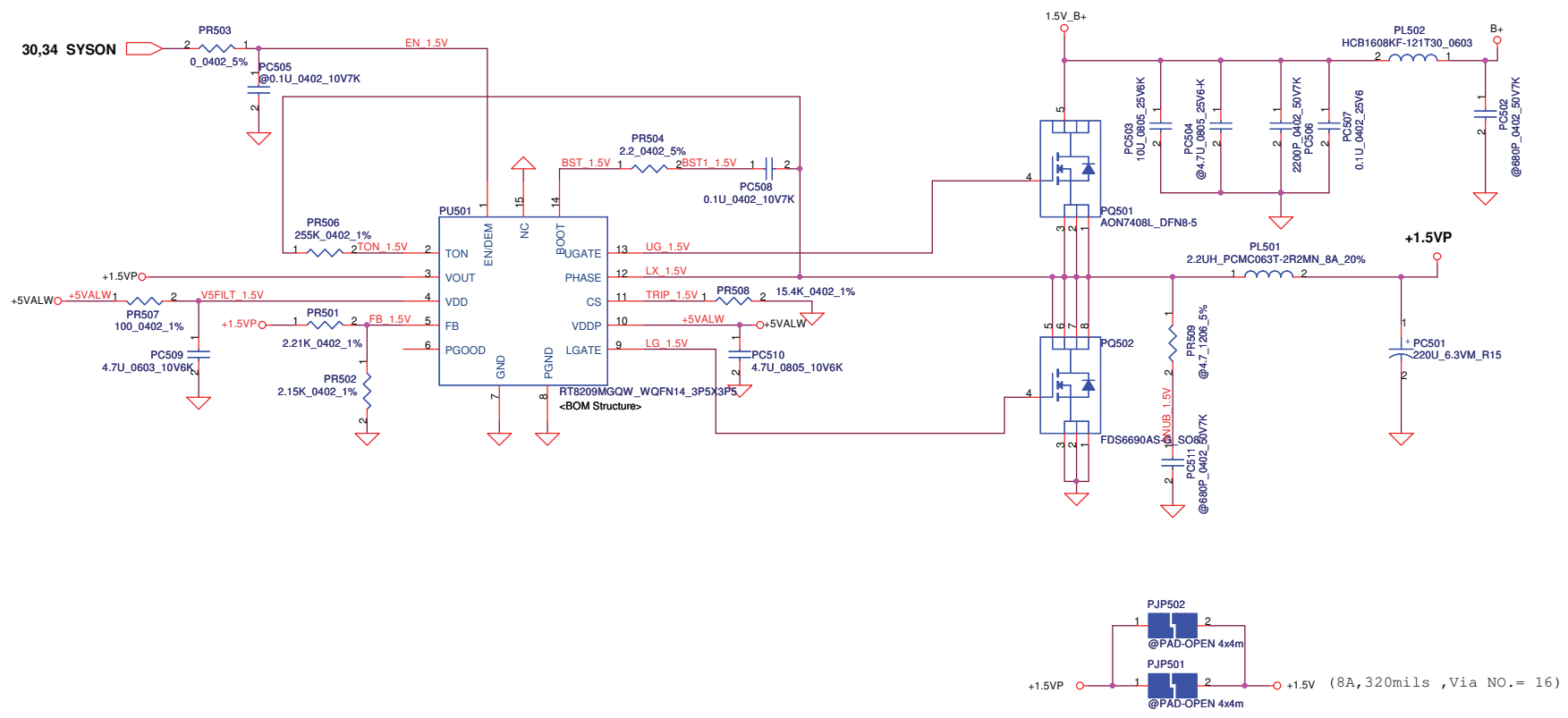
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Title		
3.3VALWP/5VALWP		
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$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$

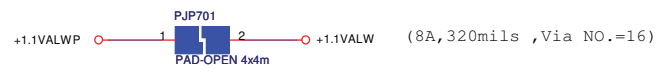
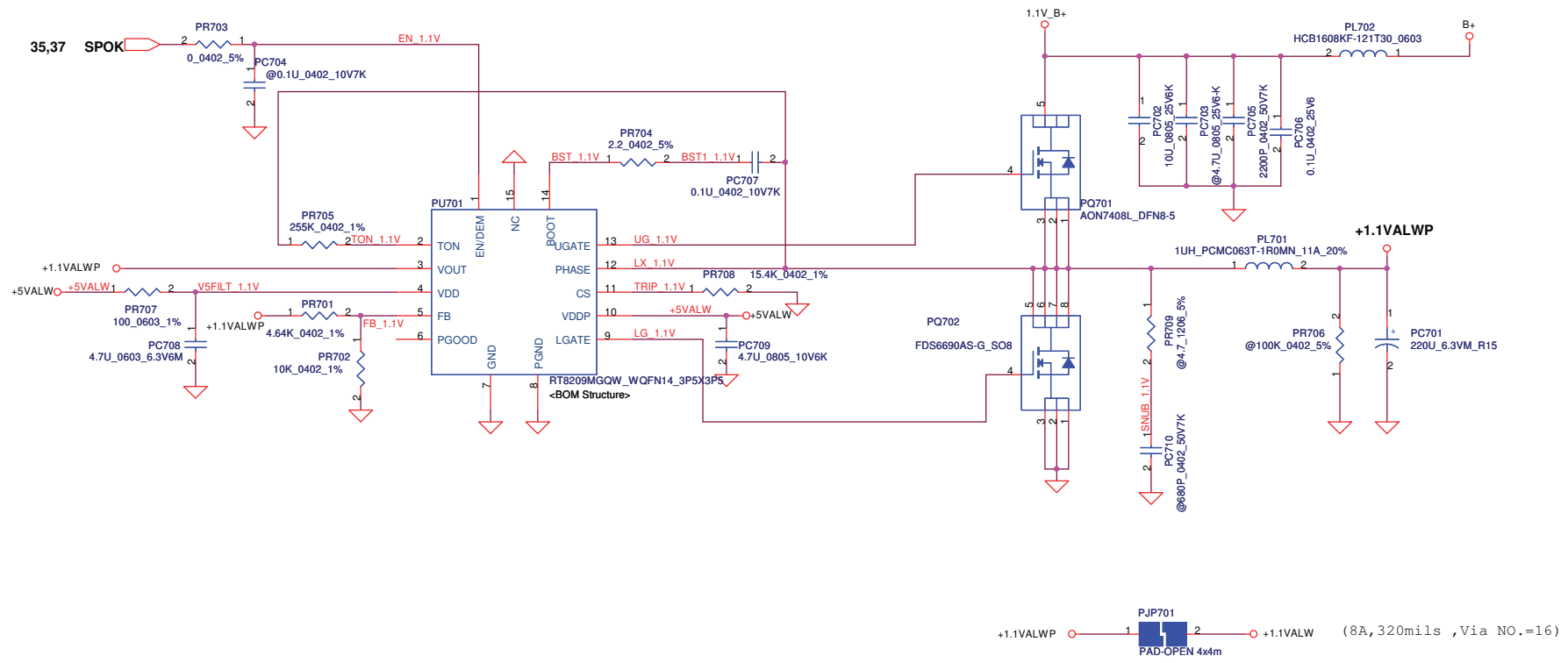
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Title		
+1.8VSP		
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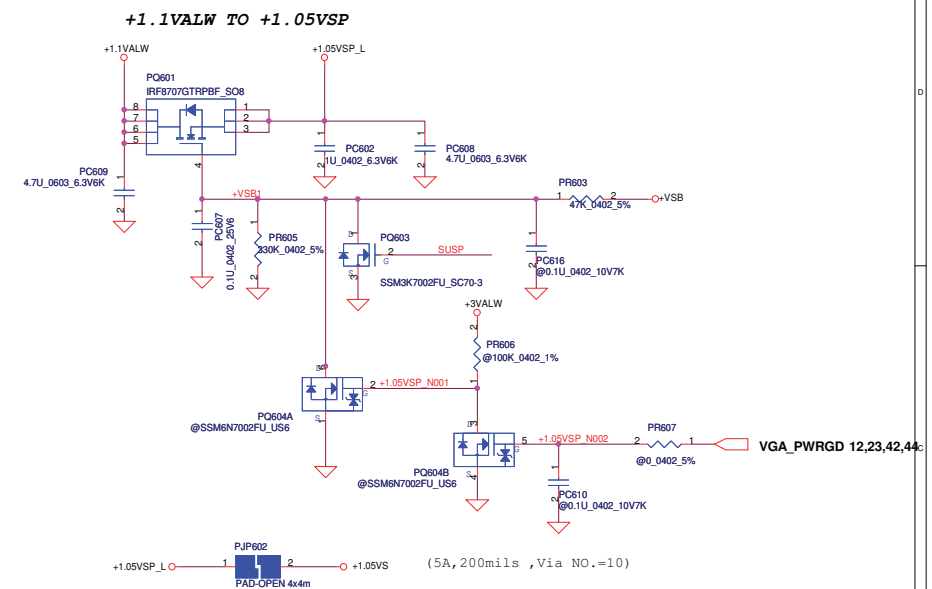
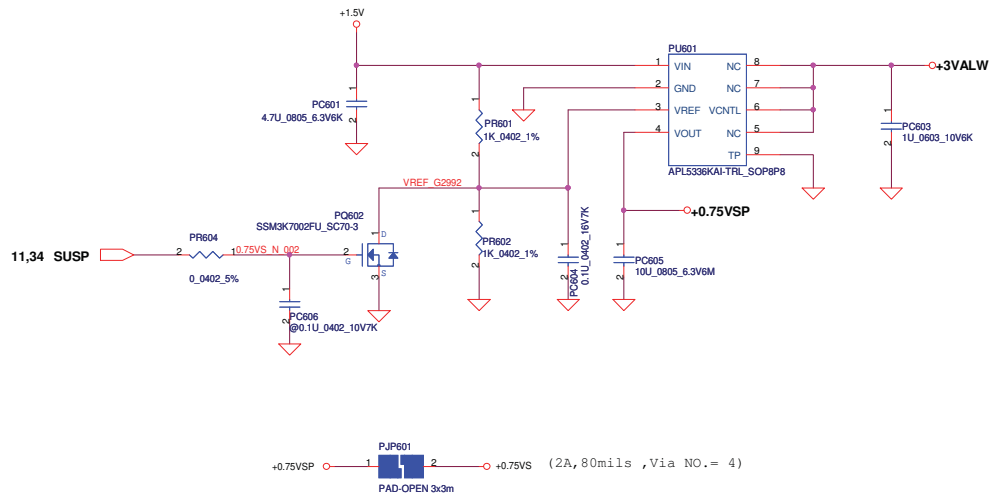


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				Document Number	LAXXXX
				Date	Wednesday, February 16, 2011
				Sheet	39 of 44

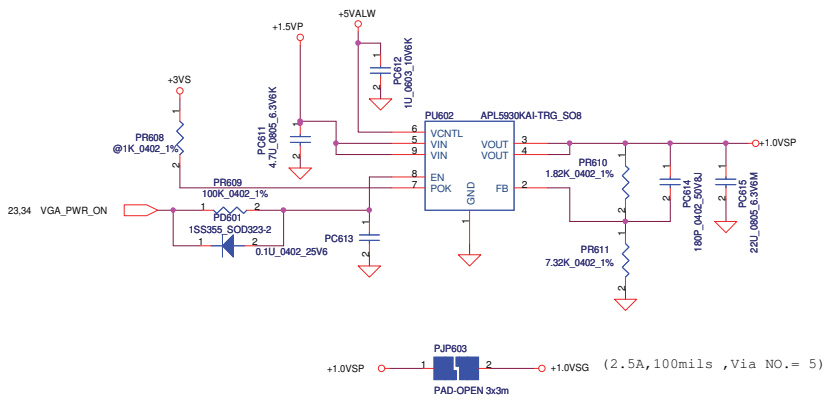
WWW



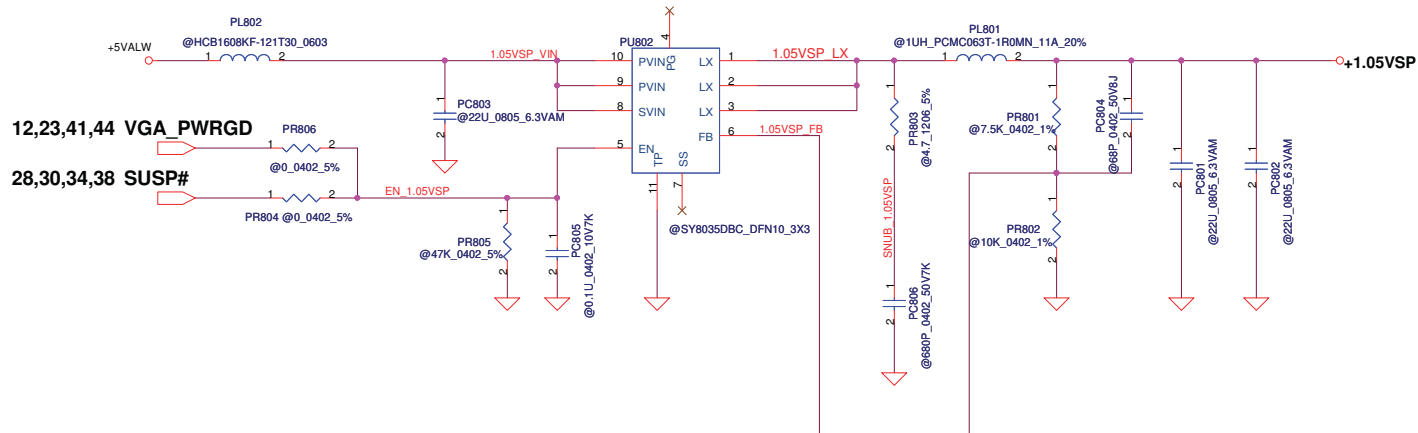
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR+1.1VALWP
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Date:	Wednesday, February 16, 2011	Sheet	40 of 44	Rev	0.22



Need to confirm with HW power sequence.



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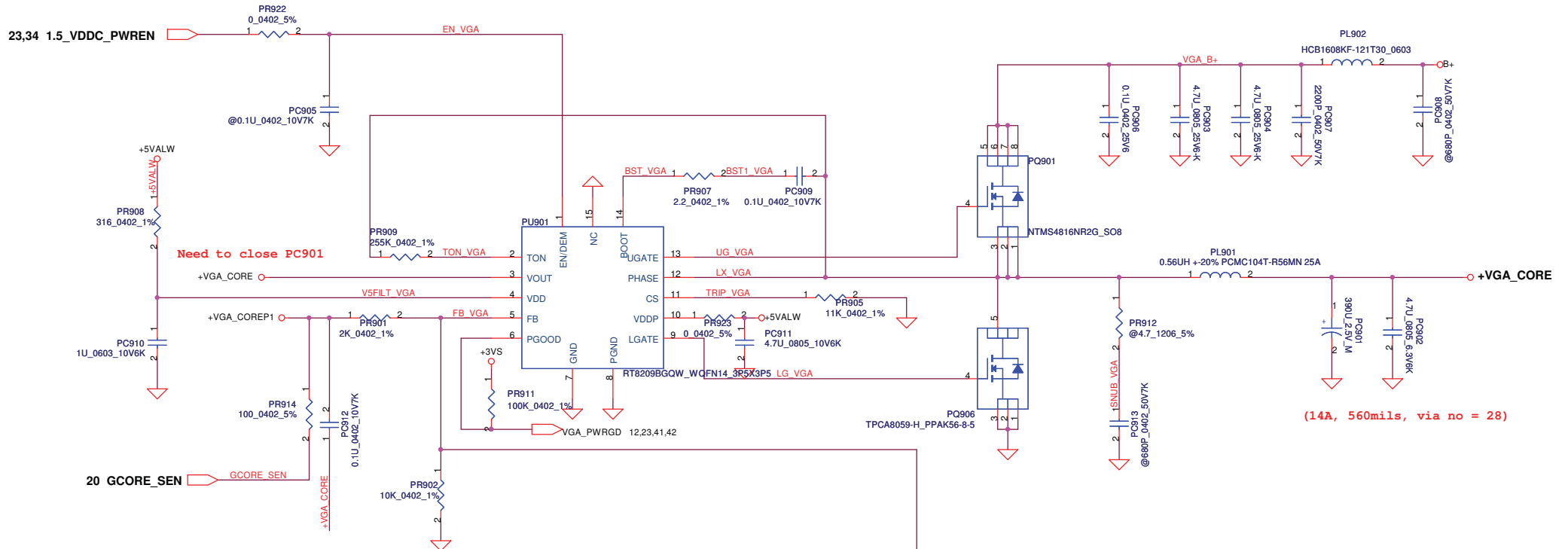
12,23,41,44 VGA_PWRGD

28,30,34,38 SUSP#



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Issued Date	2009/01/23	Deciphered Date	2010/01/23
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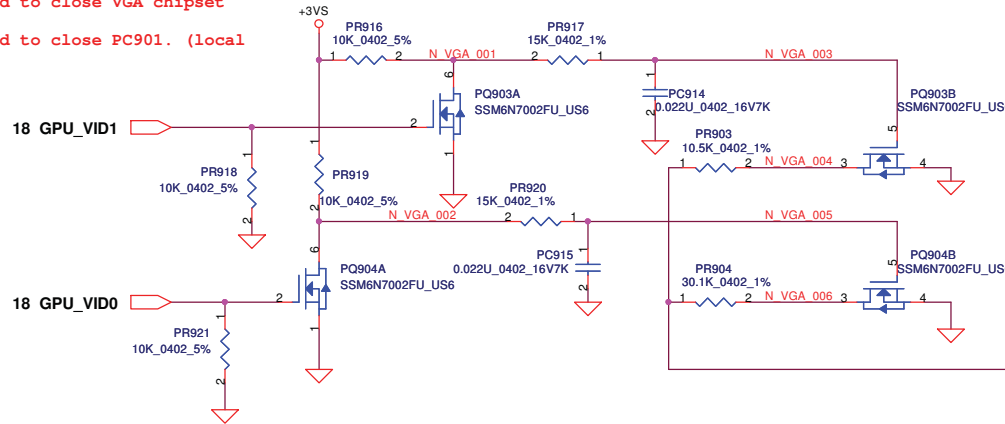
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Title +1.8VSP		
Size	Document Number NCL61 LA-6321P M/B	Rev 0.22
Date:	Tuesday, February 15, 2011	Sheet 42 of 44



Need to close PC901

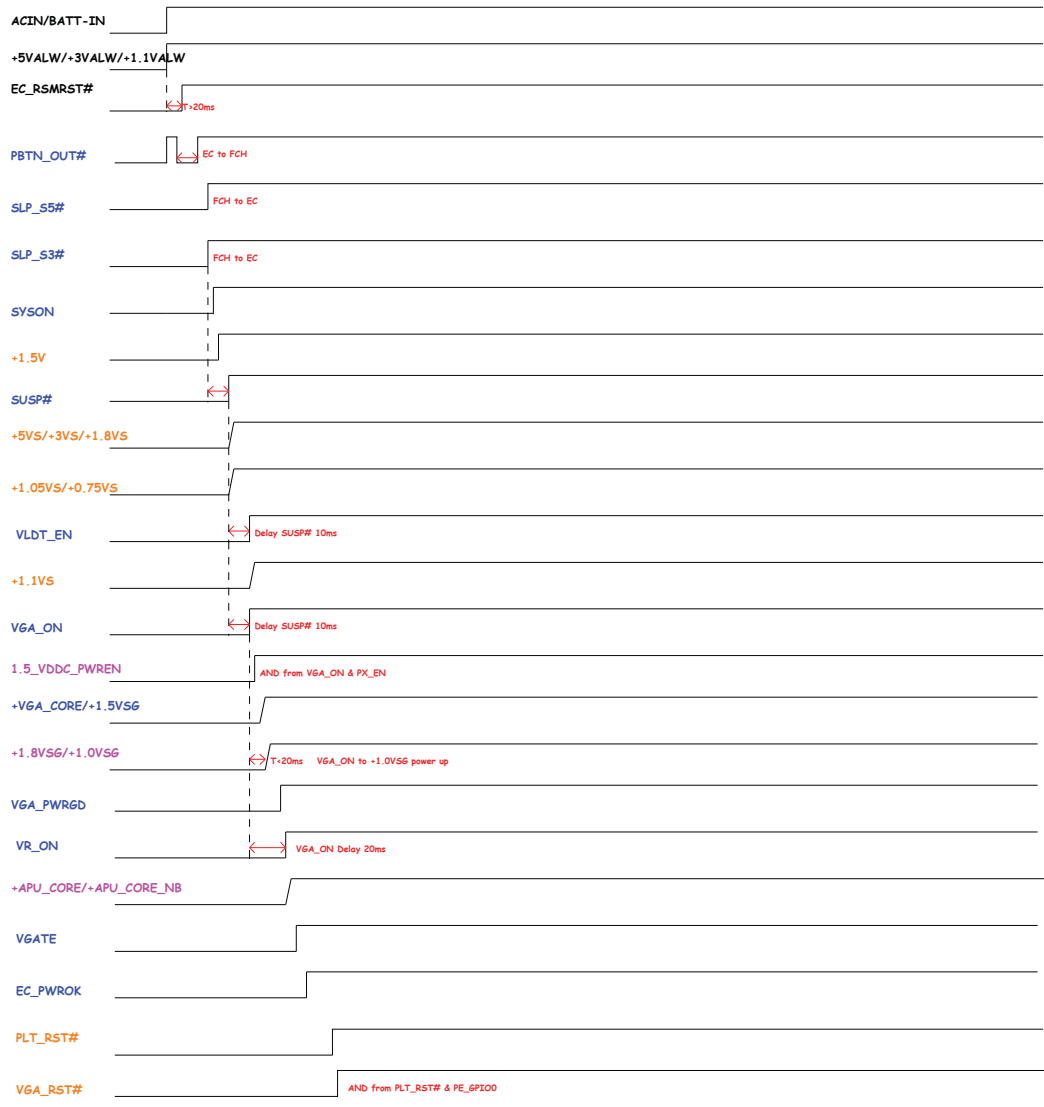
(14A, 560mils, via no = 28)

PR914 pin2 trace need to close VGA chipset MLCC. (remote sense)
 PC912 pin1 trace need to close PC901. (local sense.)



GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

POWER SEQUENCE



Rev. 1.0	2019/10/25	Control Board Date	2019/10/25
Rev. 1.0	2019/10/25	Control Board Date	2019/10/25
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P30	KB930	2010/12/16	COMPAL	Power button no function.	Add R1621 pull up to +3VALW.	0.12
2	P31	TP button	2010/12/16	COMPAL	SWS,SW6 footprint error	Modify SWS,SW6 symbol.	0.12
3	F33	Fan Connector	2010/12/16	COMPAL	Fan no function.	Modify Fan connector pin define.	0.12
4	P35 ~ P44	Power schematic update	2010/12/16	COMPAL		Power schematic update	0.12
5	P30	KB930	2010/12/17	COMPAL	Modify board ID for ER phase.	Change R1606 from 0 ohm to 8.2K ohm.	0.12
6	P5	FCH THERMTRIP	2010/12/17	COMPAL	Modify BOM structure of thermtrip circuit. For FCH spec.	Change Q79 and R424 to unpop and change R427 to pop.	0.12
7							
8	P30	KB930	2010/12/17	COMPAL	Vendor's recommend for XCLK0 signal.	Add R1669 and C129.	0.12
9	P14	FCH SPI	2010/12/21	COMPAL	Add U11 circuit for flash BIOS crisis circuit.	Add U11 circuit.	0.12
10	P8	DDR3 80-DIMM1	2010/12/21	COMPAL	Reserve R155,R152 for DDR3 DIMM1. (SA)		0.12
11	F33	Screw hole	2010/12/22	COMPAL	Thermal issue, modify H22.	Modify H22 to 7.0.	0.13
12	P35 ~ P44	Power schematic update	2010/12/22	COMPAL		Power schematic update	0.13
13	F12	FCH RTC	2010/12/23	COMPAL	Customer requirement for clear CMOS	Change R865 to Jump.	0.13
14	P28	WLAN & LED	2010/12/23	COMPAL	For ESD solution on LED.	Add C1644-C1648.	0.13
15	P26	Audio Codec	2010/12/24	COMPAL	For EMI solution on DMIC CLK.	Change R1544 to L124.	0.13
16	P30	KB930	2010/12/24	COMPAL	For EMI solution on SPI CLK.	Change R1631 to L125 and pop R180 and C1535.	0.13
17	P14	FCH SPI	2010/12/24	COMPAL		Modify Crisis circuit.	0.13
18	P10	CRT	2010/12/24	COMPAL	For ESD solution on CRT.	Pop D1,D2,D16,D18	0.13
19	P35 ~ P44	Power schematic update	2010/12/24	COMPAL		Power schematic update	0.13
20	P25	LAN	2010/12/24	COMPAL		Reserve J1 jump for LAN power.	0.13
21	P14	FCH SPI	2010/12/25	COMPAL	For EMI requirement.	Reserve R181,C130 close to U32.	0.13
22	P25	LAN	2010/12/27	COMPAL	For LAN power discharge.	Add R1113,Q62.	0.13
23	P25	LAN	2010/12/27	COMPAL	Prevent LAN wake up signal fo floating.	Add R553 pull down to GND.	0.13
24	P25	LAN	2010/12/27	COMPAL	For ESD requirement.	Change R549,R1529,R1530,R552 to 0603 size.	0.13
25	P34	DC to DC	2010/12/27	COMPAL	For Power sequence.	Change R1103 from 100K to 47K.	0.13
26	P11	HDMI	2010/12/28	COMPAL	For EMI requirement.	Modify L11-L14 circuit and remove un-LS circuit.	0.13
27	P12,18,25	Crystal	2010/12/29	COMPAL	For Vendor recommend.	Modify C35,C66,C67,C1633,C1634.	0.2
28	P26	Audio Codec	2010/12/30	COMPAL	For EMI Requirement.	Unpop R1556,R1557,R1558,R1559.	0.2
29	P30	KB930	2010/12/31	COMPAL	Change ROM footprint.	Change U48 footprint.	0.2
30	P16	FCH Strap	2010/12/31	COMPAL	Change FCH Strap for SPI-ROM	Pop R594,R602; Unpop R601,R550.	0.2
31	P18	Seymour Strap	2011/01/10	COMPAL	For AMD requirement.	Unpop R21,R22.	0.21
32	P34	DC to DC	2011/01/11	COMPAL	For +1.8VS discharge issue.	Add Q81,R1138.	0.21
33	P13	FCH HDA/USB/ACPI	2011/02/11	COMPAL	For RSMRST pluse issue	Change R606 from 2.2k ohm to 150 ohm	0.22
34	P30	EC	2011/02/11	COMPAL	For MB Board ID	Change R1606 to 18K	0.22
35	P10	CRT	2011/02/11	COMPAL	For CRT EA AND EMI	Change L116, L117, L118 TO 80 ohm	0.22
36	P25	LAN	2011/02/11	COMPAL	For EMI request	Change D36, D37, D38, D39 footprint	0.22
37	P18	VGA	2011/02/15	COMPAL	For S3 can't resume issue	ADD R74 (1M ohm) on Y1's cap	0.22
38	P25	LAN	2011/02/15	COMPAL	Follow vendor recommend to change Crystal's cap value	Change C1633 to 15P, C1634 to 12P	0.22
39	P30	EC	2011/02/16	COMPAL	For EMI requirement	Change R180 to 39 ohm, C1535 to 33P	0.23
40	P25	LAN	2011/02/16	COMPAL	For EMI requirement	Change T81 to IH-160	0.23
41	P26	AUDIO	2011/02/17	COMPAL	For EMI requirement	Change R1556, R1557, R1558, R1559 to 0.1u caps	0.23
42	P34	DC-DC	2011/02/17	COMPAL	For EMI requirement	ADD C1505, C1523 on +5VALW	0.23
43	P32	USB	2011/02/17	COMPAL	For EMI requirement	ADD C1506 on +USB_VCCB	0.23
44	P33	PHRBTN	2011/02/17	COMPAL	For EMI requirement	ADD C1603 on ON/OFFBTN#	0.23
45	P25	LAN	2011/02/18	COMPAL	For EMI requirement	Stuff R546, R548	0.23
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