



Part Number = DA6000M700

# Compal Confidential

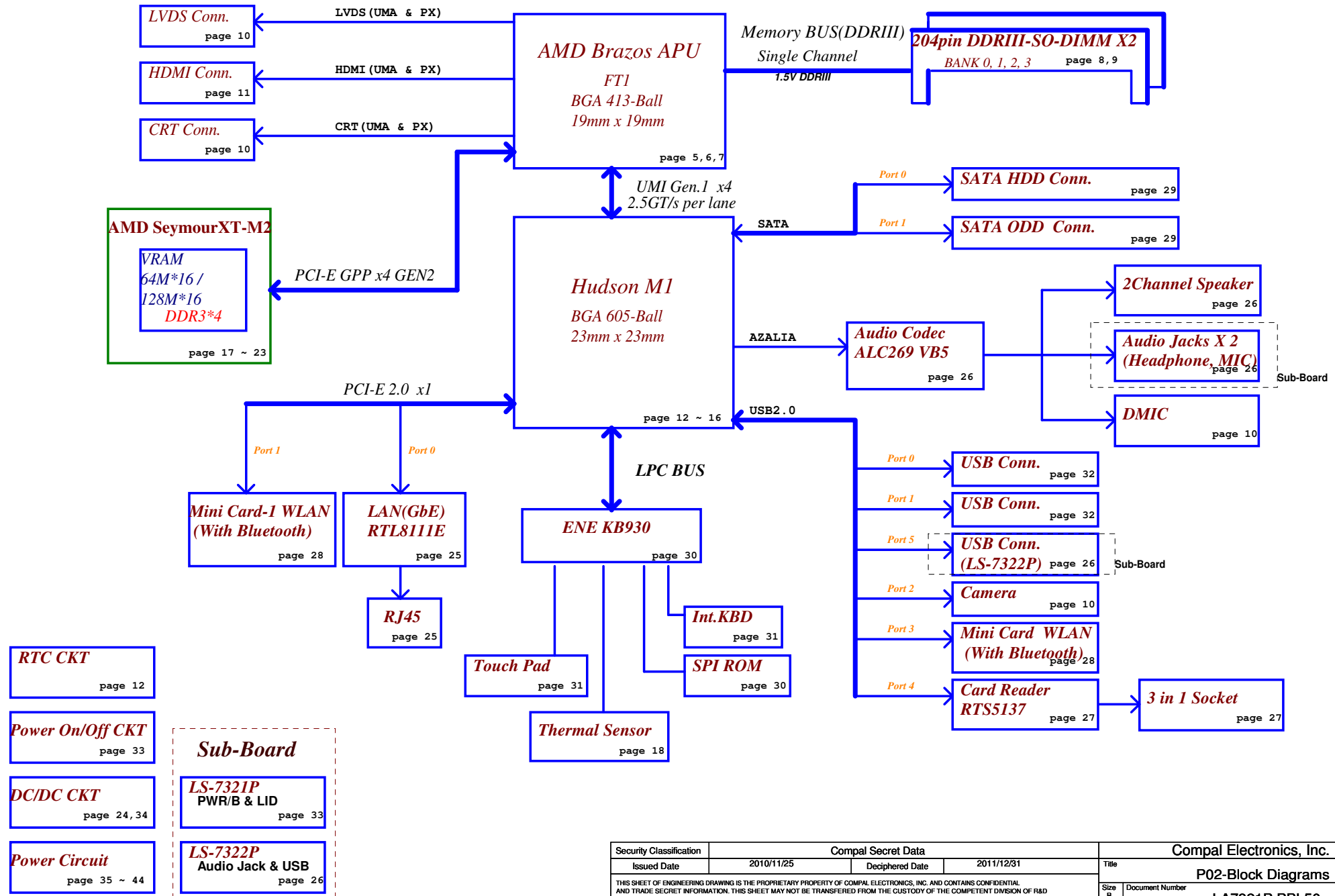
## PBL50 Schematics Document

### AMD APU Zacate-FT1 + FCH Hudson-M1 + DGPU Seymour XT-M2

2011-02-15

REV: 0.22

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE PU Rail	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930 +3VALW	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V +3VS	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH +3VS	V	X	X	V	V	X
FCH_SIC FCH_SID	FCH +3VALW	X	X	V Reserve	X	X	X

SCL0, SDA0 (Primary SMBUS in the S0 domain)  
 SCL1, SDA1 (Secondary SMBUS supporting ASF)  
 SCL2, SDA2 (Primary SMBUS in the S5 domain)  
 SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)  
 SCL4, SDA4 (Primary SMBUS in the S5 domain)

### Symbol Note :



: means Digital Ground



: means Analog Ground

## FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

## Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

## FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

## BOM Structure

10G@ : 1.0G CPU (C50)  
 15G@ : 1.5G CPU (E240)  
 16G@ : 1.6G CPU (E350)  
 UMA@ : APU output.  
 VGA@ : GPU used.  
 LS@ : Level shift used.  
 X76@ : VRAM.

X76@L01: Samsung 1G  
 X76@L02: Hynix 1G  
 X76@L03: Samsung 512M  
 X76@L04: Hynix 512M

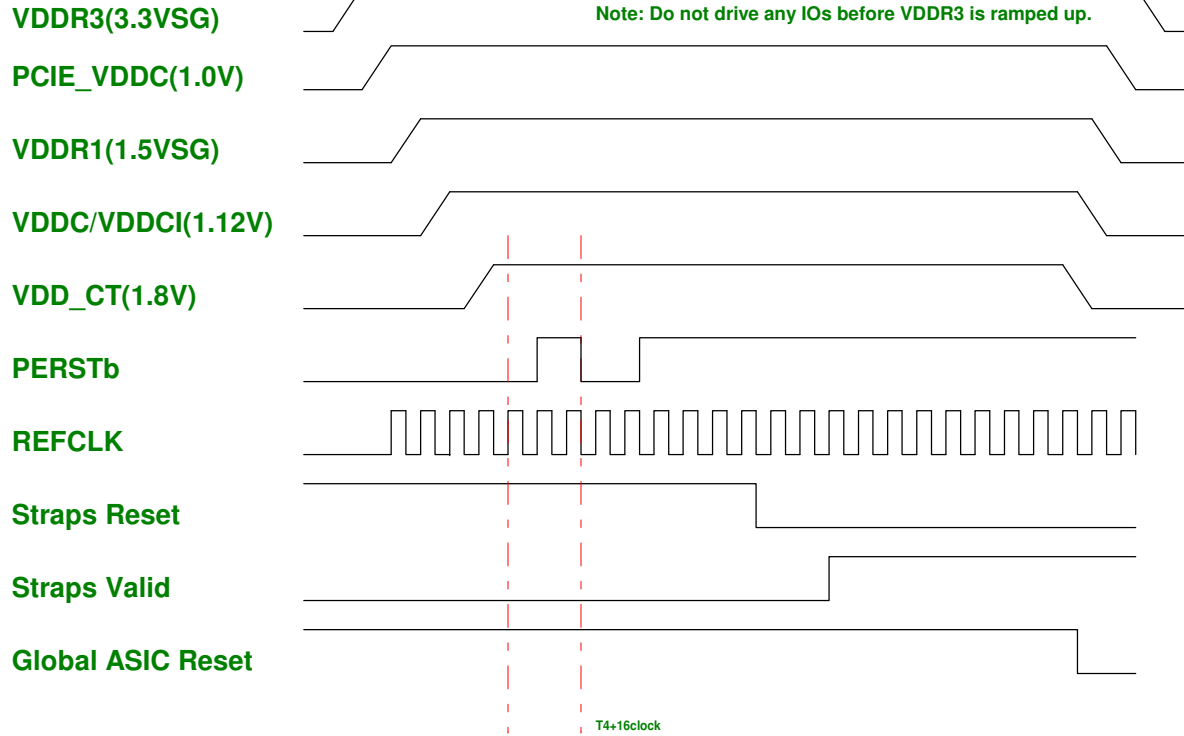
### DIS M/B BOM Config

L01: 16G@/VGA@/LS@ --X76@L04  
 L02: 16G@/UMA@/LS@  
 L03: 15G@/VGA@/LS@ --X76@L03  
 L04: 15G@/UMA@/LS@  
 L05: 16G@/VGA@/LS@ --X76@L01  
 L06: 15G@/VGA@/LS@ --X76@L02  
 L07: 10G@/UMA@/LS@

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				P03-Notes List		
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## Power-Up/Down Sequence

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDR3 should ramp-up before or simultaneously with VDDC.
- For LVDS, DPx\_VDD10 should ramp-up before DPx\_VDD18 and the PCIe Reference clock should begin before DPx\_VDD18. For power-down, DPx\_VDD18 should ramp-down before DPx\_VDD10.
- The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD\_CT starts to ramp-up (or vice versa).)



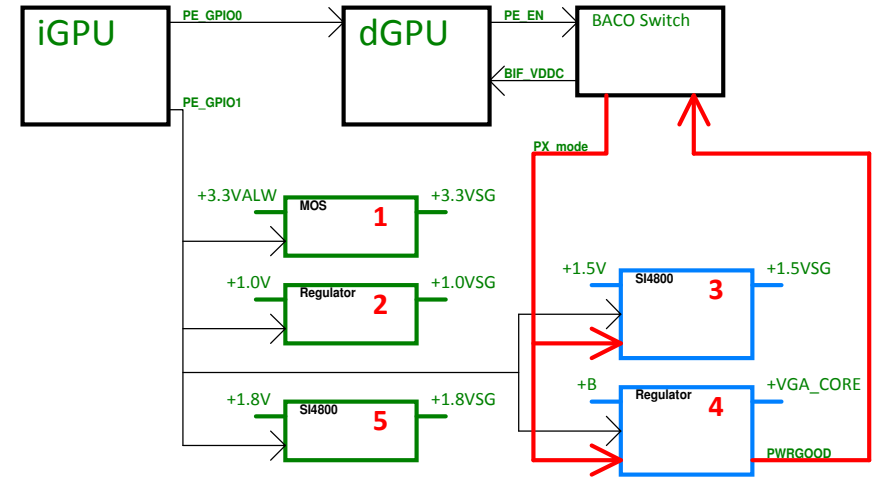
## Without BACO option :

PE\_GPIO0 : Low -> Reset dGPU ; High ->Normal operation  
 PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

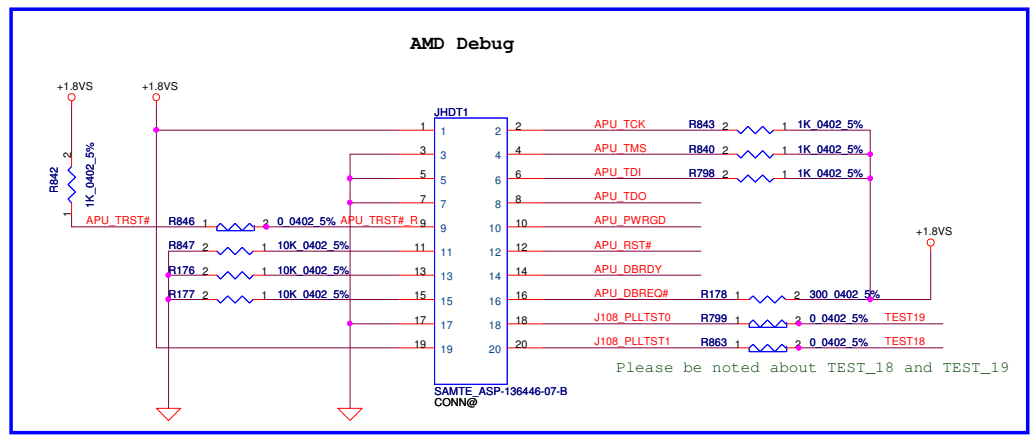
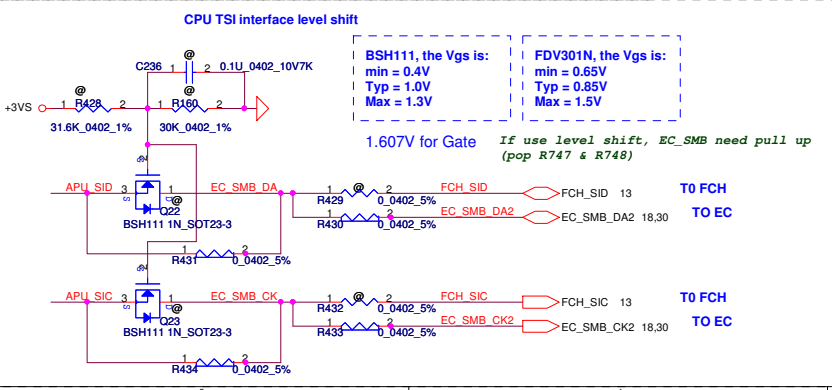
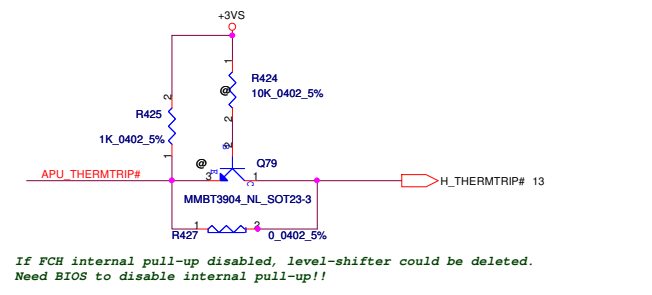
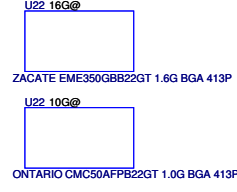
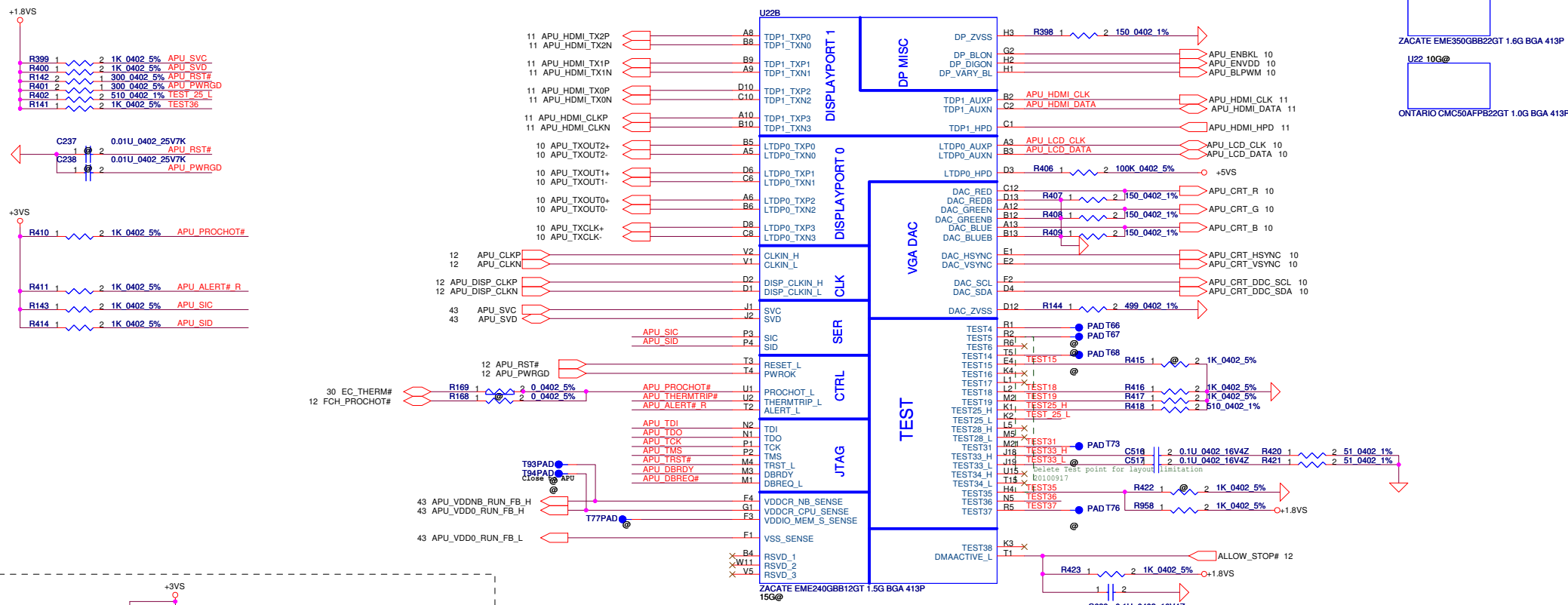
## BACO option :

PE\_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)  
 PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



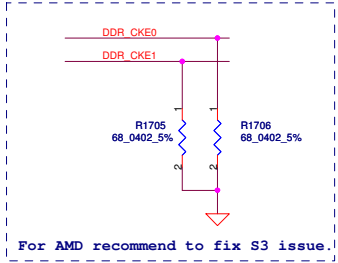
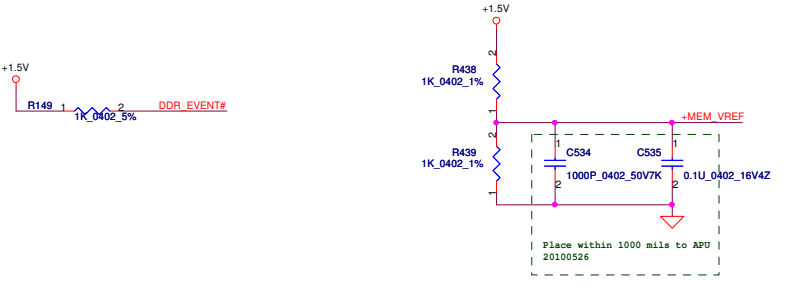
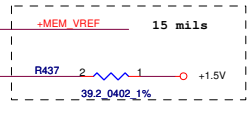
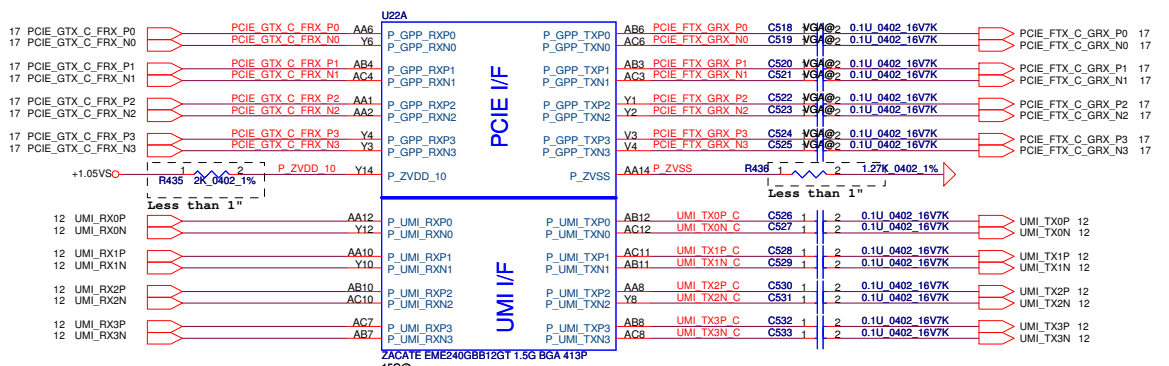
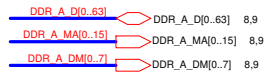
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			P05-FT1 CTRL/DP/CRT	
			Rev 0.22	

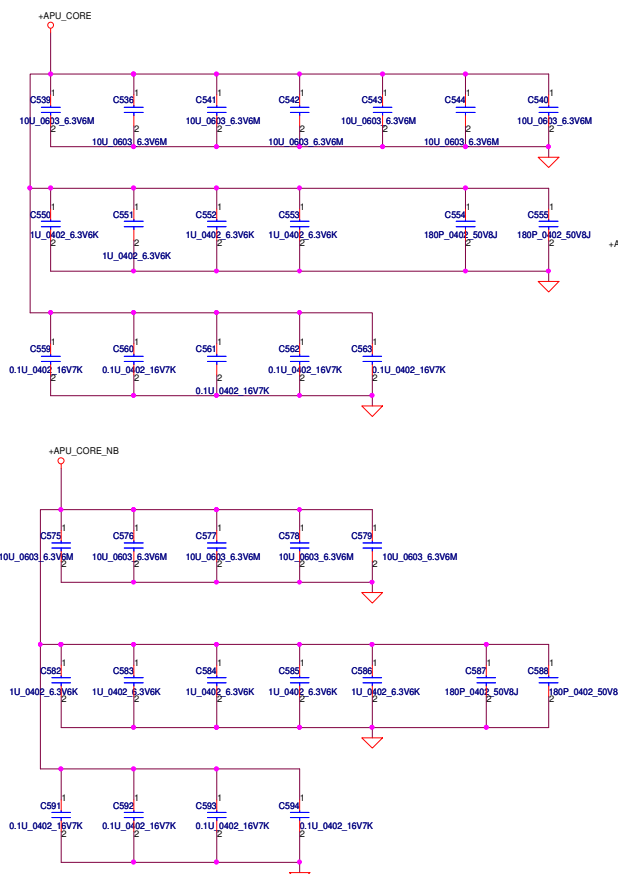
DDR A MA0	R17	M_ADD0	B14	DDR A D0									
DDR A MA1	H19	M_ADD1	A15	DDR A D1									
DDR A MA2	J17	M_ADD2	A17	DDR A D2									
DDR A MA3	H18	M_ADD3	D18	DDR A D3									
DDR A MA4	G17	M_ADD4	A14	DDR A D4									
DDR A MA5	G17	M_ADD5	C14	DDR A D5									
DDR A MA6	H15	M_ADD6	C16	DDR A D6									
DDR A MA7	F18	M_ADD7	D16	DDR A D7									
DDR A MA8	F19	M_ADD8	C18	DDR A D8									
DDR A MA9	E19	M_ADD9	A19	DDR A D9									
DDR A MA10	T19	M_ADD10	B21	DDR A D10									
DDR A MA11	F17	M_ADD11	D20	DDR A D11									
DDR A MA12	E18	M_ADD12	A18	DDR A D12									
DDR A MA13	W17	M_ADD13	B18	DDR A D13									
DDR A MA14	E16	M_ADD14	A21	DDR A D14									
DDR A MA15	G15	M_ADD15	C20	DDR A D15									
8.9 DDR A_BS0	R18	M_BANK0	C23	DDR A D16									
8.9 DDR A_BS1	T18	M_BANK1	D23	DDR A D17									
8.9 DDR A_BS2	F16	M_BANK2	F23	DDR A D18									
DDR A DM0	D15	M_DM0	F22	DDR A D19									
DDR A DM1	B19	M_DM1	C22	DDR A D20									
DDR A DM2	D21	M_DM2	D22	DDR A D21									
DDR A DM3	H22	M_DM3	F20	DDR A D22									
DDR A DM4	P23	M_DM4	F21	DDR A D23									
DDR A DM5	V23	M_DM5	H21	DDR A D24									
DDR A DM6	AB20	M_DM6	H23	DDR A D25									
DDR A DM7	AA16	M_DM7	K22	DDR A D26									
8.9 DDR_A_DQS0	DDR A DQS0	A16	M_DOS_L0	PCIE GTX C FRX P0	AA6	P_GPP_RXP0	P_GPP_TXP0	AB6	PCIE_FTX_GRX_P0	C518	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0
8.9 DDR_A_DQS#0	DDR A DQS#0	B16	M_DOS_L1	PCIE GTX_C_FRX_N0	Y6	P_GPP_RXN0	P_GPP_TXN0	AC6	PCIE_FTX_GRX_N0	C519	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0
8.9 DDR_A_DQS1	DDR A DQS1	B20	M_DOS_L1	PCIE GTX_C_FRX_P1	AB4	P_GPP_RXP1	P_GPP_TXP1	AB3	PCIE_FTX_GRX_P1	C520	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1
8.9 DDR_A_DQS#1	DDR A DQS#1	A20	M_DOS_L1	PCIE GTX_C_FRX_N1	AA1	P_GPP_RXN1	P_GPP_TXN1	AC3	PCIE_FTX_GRX_N1	C521	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1
8.9 DDR_A_DQS2	DDR A DQS2	E22	M_DOS_L2	PCIE GTX C FRX P2	AA1	P_GPP_RXP2	P_GPP_TXP2	Y1	PCIE_FTX_GRX_P2	C522	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2
8.9 DDR_A_DQS#2	DDR A DQS#2	E22	M_DOS_L2	PCIE GTX_C_FRX_N2	AA2	P_GPP_RXN2	P_GPP_TXN2	Y2	PCIE_FTX_GRX_N2	C523	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2
8.9 DDR_A_DQS3	DDR A DQS3	J22	M_DOS_L2	PCIE GTX C FRX P3	Y4	P_GPP_RXP3	P_GPP_TXP3	V3	PCIE_FTX_GRX_P3	C524	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P3
8.9 DDR_A_DQS#3	DDR A DQS#3	J22	M_DOS_L2	PCIE GTX_C_FRX_N3	Y3	P_GPP_RXN3	P_GPP_TXN3	V4	PCIE_FTX_GRX_N3	C525	VGA@2	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3
8.9 DDR_A_DQS4	DDR A DQS4	P22	M_DOS_L3										
8.9 DDR_A_DQS#4	DDR A DQS#4	P22	M_DOS_L3										
8.9 DDR_A_DQS5	DDR A DQS5	V22	M_DOS_L4										
8.9 DDR_A_DQS#5	DDR A DQS#5	V22	M_DOS_L4										
8.9 DDR_A_DQS6	DDR A DQS6	AC20	M_DOS_H6										
8.9 DDR_A_DQS#6	DDR A DQS#6	AC21	M_DOS_H6										
8.9 DDR_A_DQS7	DDR A DQS7	AB16	M_DOS_H7										
8.9 DDR_A_DQS#7	DDR A DQS#7	AC16	M_DOS_L7										
9 DDR_A_CLK0	DDR A CLK0	M17	M_CLK_L0										
9 DDR_A_CLK#0	DDR A CLK#0	M16	M_CLK_L0										
9 DDR_A_CLK1	DDR A CLK1	M19	M_CLK_H1										
9 DDR_A_CLK#1	DDR B CLK#1	M18	M_CLK_L1										
8 DDR_B_CLK2	DDR B CLK#2	N19	M_CLK_L2										
8 DDR_B_CLK#2	DDR B CLK#2	L18	M_CLK_H3										
8 DDR_B_CLK3	DDR B CLK#3	L17	M_CLK_L3										
8.9 DDR_RST#	DDR_RST#	L23	M_RESET_L										
8.9 DDR_EVENT#	DDR_EVENT#	N17	M_EVENT_L										
8.9 DDR_CKE0	DDR_CKE0	F15	M_CKE0										
8.9 DDR_CKE1	DDR_CKE1	E15	M_CKE1										
9 DDR_A_ODT0	DDR A ODT0	W19	M0_ODT0										
9 DDR_A_ODT1	DDR A ODT1	V15	M0_ODT1										
8 DDR_B_ODT0	DDR B ODT0	U19	M1_ODT0										
8 DDR_B_ODT1	DDR B ODT1	W15	M1_ODT1										
9 DDR_CS0_DIMM#	DDR_CS0_DIMM#	T17	M0_CS_L0										
9 DDR_CS1_DIMM#	DDR_CS1_DIMM#	W16	M0_CS_L1										
8 DDR_CS0_DIMM#	DDR_CS0_DIMM#	U17	M1_CS_L0										
8 DDR_CS1_DIMM#	DDR_CS1_DIMM#	V16	M1_CS_L1										
8.9 DDR_A_RAS#	DDR A RAS#	U18	M_RAS_L										
8.9 DDR_A_CAS#	DDR A CAS#	V19	M_CAS_L										
8.9 DDR_A_WE#	DDR A WE#	V17	M_WE_L										

DDR SYSTEM MEMORY

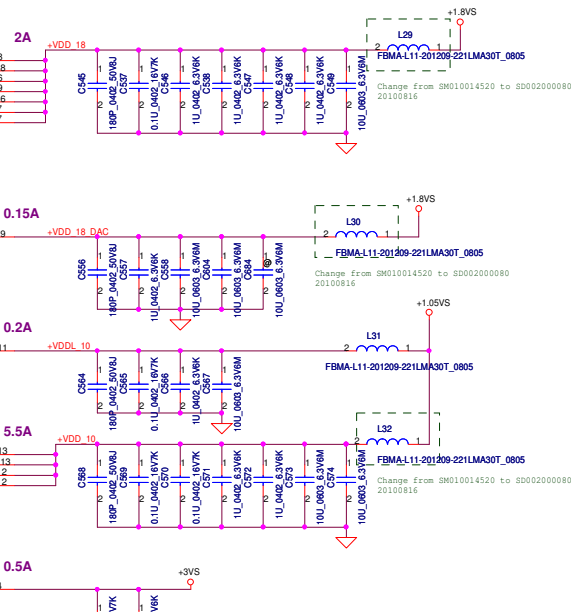


For AMD recommend to fix S3 issue.

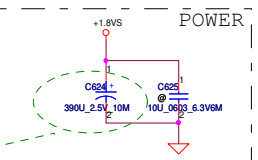
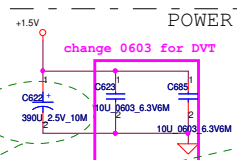
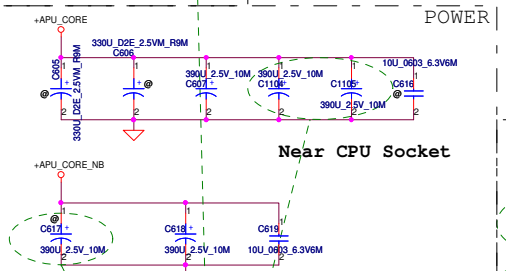
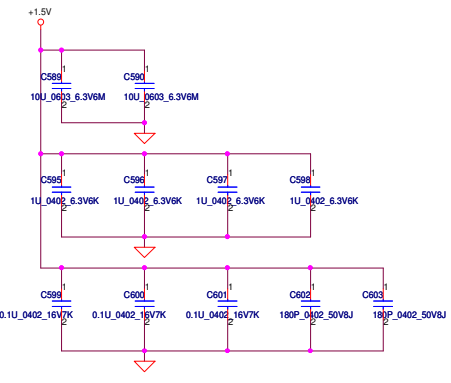
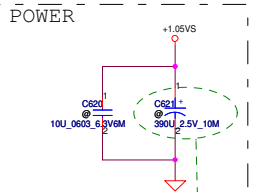
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Pin	Signal
E5	VDDCR_CPU_1
E6	VDDCR_CPU_2
E7	VDDCR_CPU_3
F6	VDDCR_CPU_4
F7	VDDCR_CPU_5
G6	VDDCR_CPU_6
G7	VDDCR_CPU_7
H6	VDDCR_CPU_8
H7	VDDCR_CPU_9
J8	VDDCR_CPU_10
L7	VDDCR_CPU_11
M6	VDDCR_CPU_12
M7	VDDCR_CPU_13
N7	VDDCR_CPU_14
R8	VDDCR_CPU_15
E8	VDDCR_NB_1
E11	VDDCR_NB_2
E12	VDDCR_NB_3
F9	VDDCR_NB_4
F12	VDDCR_NB_5
G11	VDDCR_NB_6
G13	VDDCR_NB_7
H9	VDDCR_NB_8
H12	VDDCR_NB_9
K11	VDDCR_NB_10
K13	VDDCR_NB_11
L10	VDDCR_NB_12
L12	VDDCR_NB_13
M11	VDDCR_NB_14
M14	VDDCR_NB_15
M12	VDDCR_NB_16
M15	VDDCR_NB_17
N10	VDDCR_NB_18
N12	VDDCR_NB_19
N14	VDDCR_NB_20
P11	VDDCR_NB_21
P13	VDDCR_NB_22
Q18	VDDIO_MEM_S_1
Q19	VDDIO_MEM_S_2
J16	VDDIO_MEM_S_3
L16	VDDIO_MEM_S_4
L19	VDDIO_MEM_S_5
N16	VDDIO_MEM_S_6
R19	VDDIO_MEM_S_7
R18	VDDIO_MEM_S_8
W18	VDDIO_MEM_S_9
W18	VDDIO_MEM_S_10
W18	VDDIO_MEM_S_11



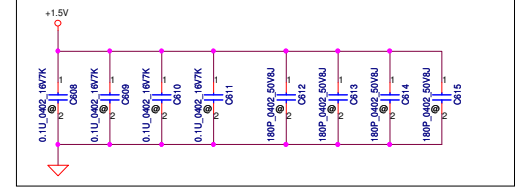
Pin	Signal
A7	VSS_1
B7	VSS_2
B11	VSS_3
B17	VSS_4
B22	VSS_5
C4	VSS_6
D5	VSS_7
D7	VSS_8
D11	VSS_9
D11	VSS_10
B15	VSS_11
D17	VSS_12
D17	VSS_13
D19	VSS_14
E7	VSS_15
E9	VSS_16
E12	VSS_17
E20	VSS_18
F8	VSS_19
F13	VSS_20
G4	VSS_21
G5	VSS_22
G7	VSS_23
G9	VSS_24
G12	VSS_25
G20	VSS_26
G22	VSS_27
H1	VSS_28
H11	VSS_29
H13	VSS_30
M4	VSS_31
M4	VSS_32
J5	VSS_33
J7	VSS_34
K10	VSS_35
K14	VSS_36
L4	VSS_37
L4	VSS_38
L6	VSS_39
L8	VSS_40
L11	VSS_41
L13	VSS_42
L23	VSS_43
L29	VSS_44
M7	VSS_45
N4	VSS_46
N6	VSS_47
N8	VSS_48
N11	VSS_49
N13	VSS_50
N20	VSS_51
N22	VSS_52
P10	VSS_53
P14	VSS_54
R4	VSS_55
R7	VSS_56
R20	VSS_57
R9	VSS_58
T9	VSS_59
T11	VSS_60
T13	VSS_61
U4	VSS_62
U5	VSS_63
U7	VSS_64
U12	VSS_65
U22	VSS_66
V8	VSS_67
V8	VSS_68
V11	VSS_69
V13	VSS_70
W1	VSS_71
W2	VSS_72
W4	VSS_73
W4	VSS_74
W7	VSS_75
W7	VSS_76
W12	VSS_77
W20	VSS_78
Y5	VSS_79
Y7	VSS_80
Y9	VSS_81
Y11	VSS_82
Y13	VSS_83
Y15	VSS_84
Y17	VSS_85
Y19	VSS_86
AA4	VSS_87
AA22	VSS_88
AA2	VSS_89
AB5	VSS_90
AB5	VSS_91
AB9	VSS_92
AB13	VSS_93
AB17	VSS_94
AC5	VSS_95
AC9	VSS_96
AC13	VSS_97
AC13	VSS_98
AC13	VSS_99
AC13	VSS_100



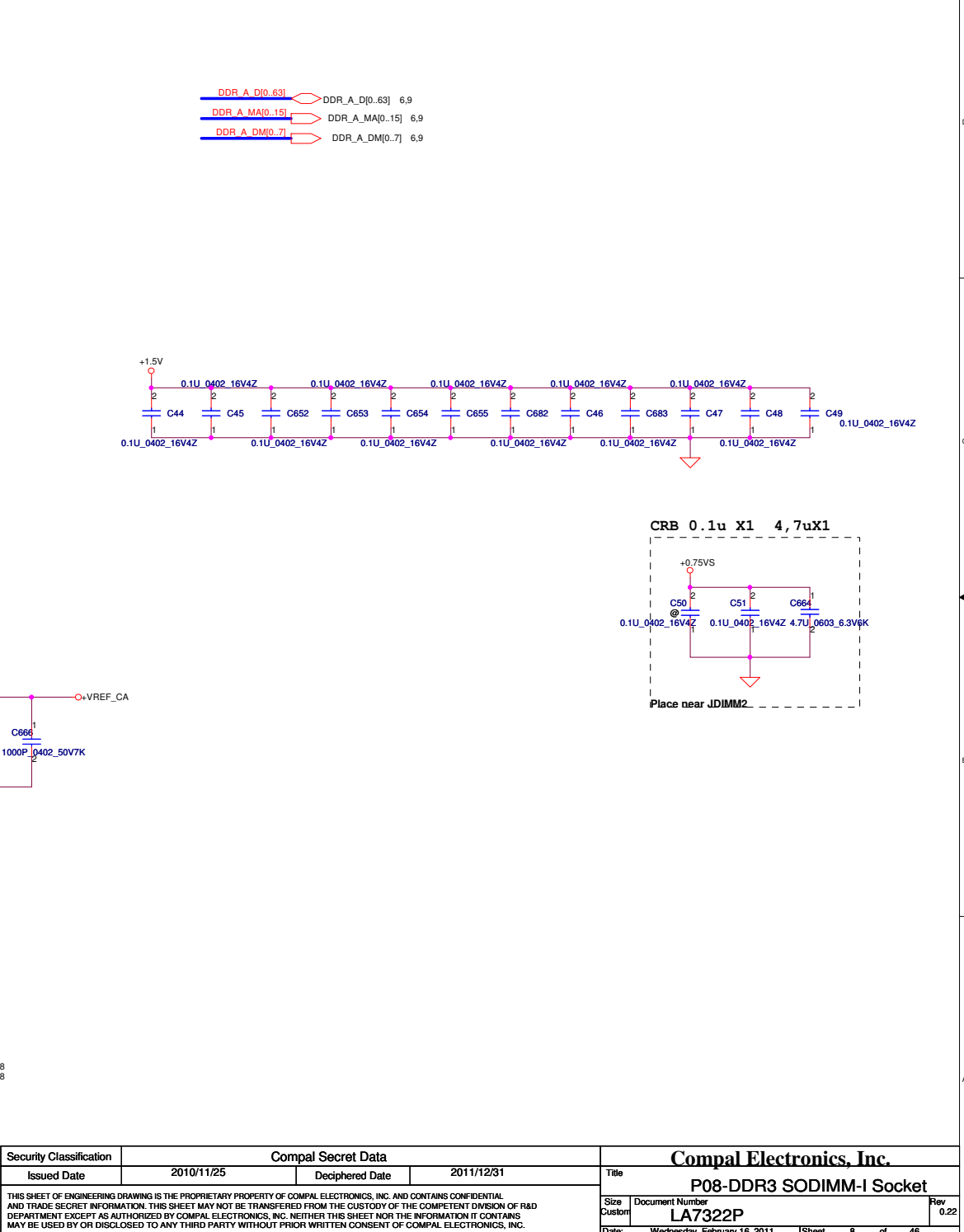
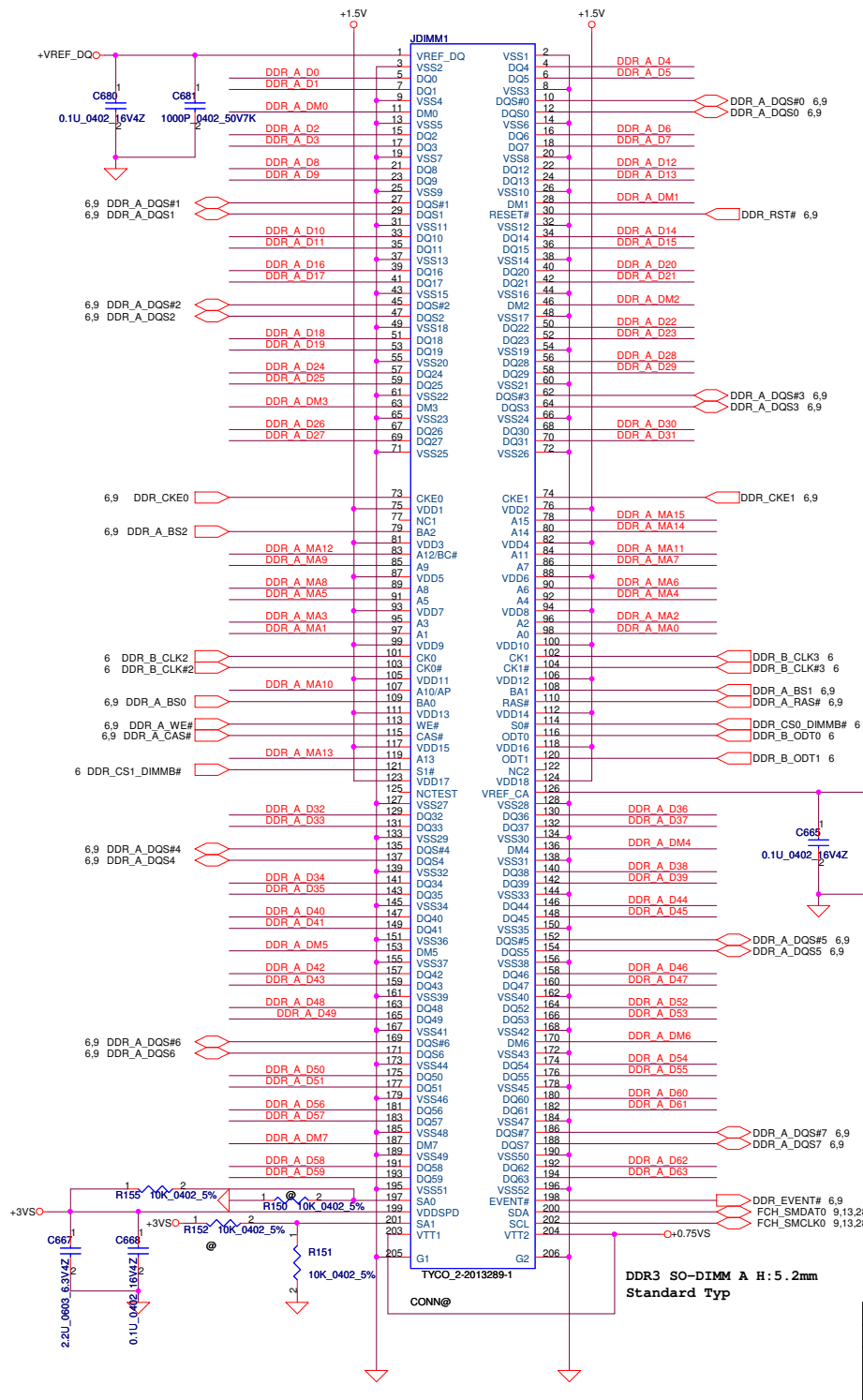
**Power Cap. Summary**

- APU**
  - S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 ---->+APU\_CORE(Qty : 3) Unpop:2
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU\_CORE(Qty : 2) +APU\_CORE
  - S POLY C 330U 2.5V Y D2 LESR9M EEF5 H1.9 ---->+APU\_CORE\_NB(Qty : 1)
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU\_CORE\_NB(Qty : 1) +APU\_CORE\_NB
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5V(Qty : 1) +1.5V
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.05VS(Qty : 1) +1.05VS
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.8VS(Qty : 1) +1.8VS
- DDR3 Socket**
  - S POLY C 330U 2V M X LESR6M SX H1.9 ---->+1.5V(Qty : 1) +1.5V
- FCH**
  - S POLY C 330U 2.5V Y D2 LESR9M EEF5 H1.9 ---->+1.1VS(Qty : 1) UMA unpop +1.1VS
- GPU**
  - S POLY C 330U 2V M X LESR6M SX H1.9 ---->+VGA\_CORE(Qty : 2) Unpop:1
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+VGA\_CORE(Qty : 1) +GPU\_CORE
  - S A-P\_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5VSG(Qty : 1) +1.5VSG
- USB**
  - S A-P\_CAP 220U 6.3V M C45 R17M SVPE H4.4 ---->+USB\_VCCA(Qty : 1) +USB\_VCCA

By case (Along split)

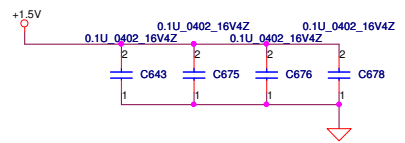
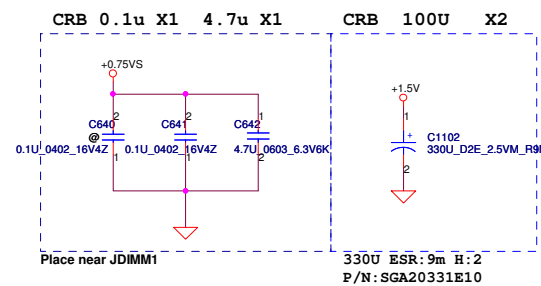
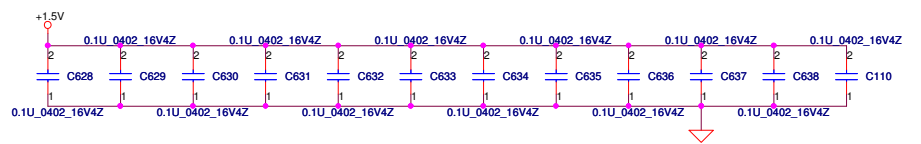
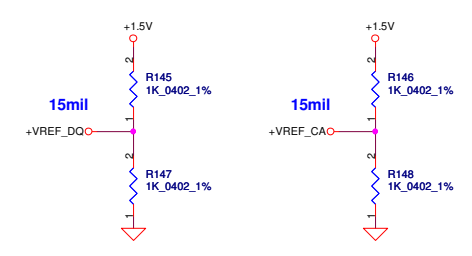
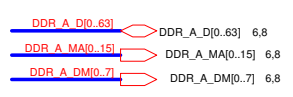
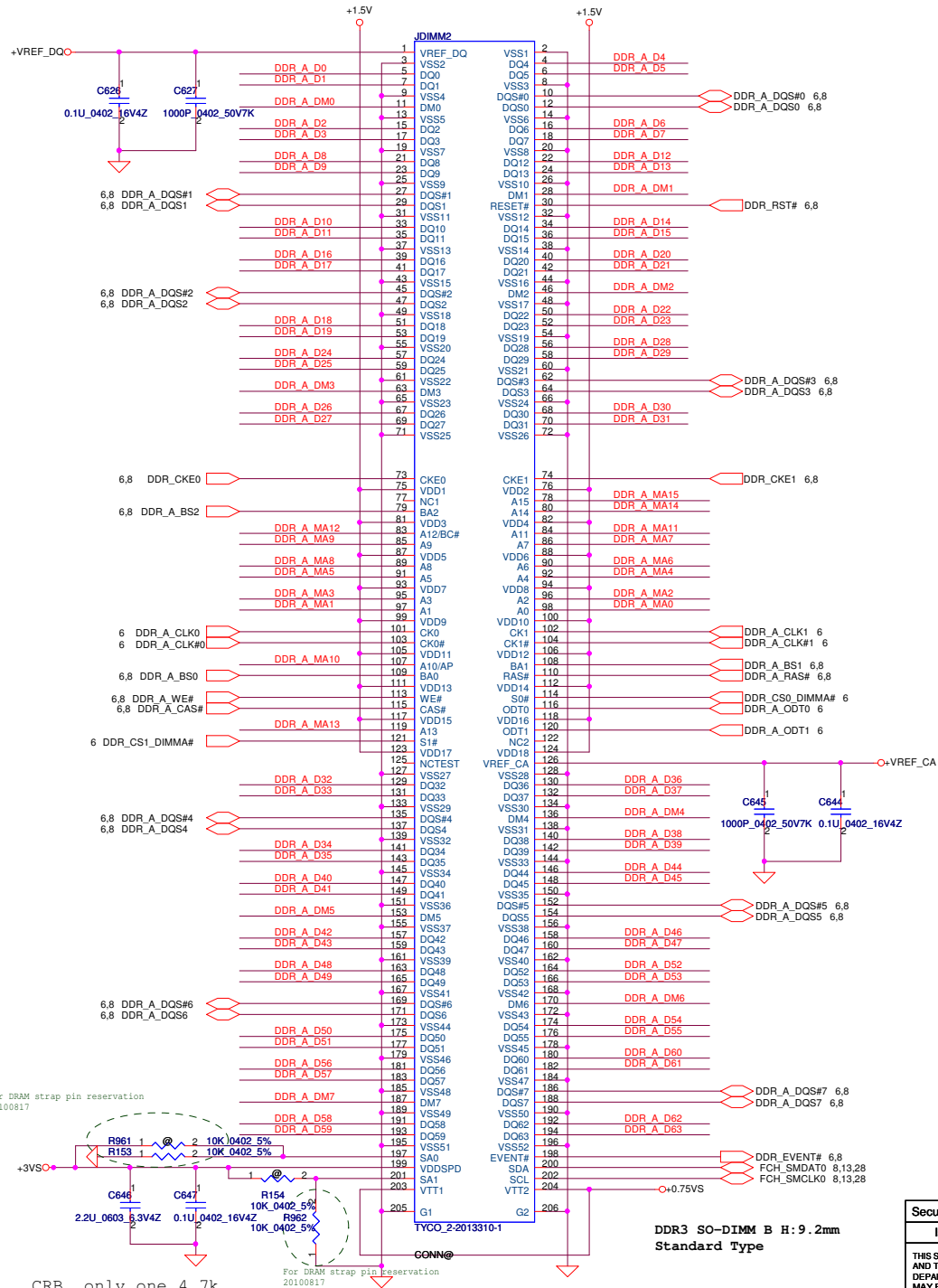


$(390\mu F \cdot 2.5V \cdot 6.3 \times 5.7 \cdot ESR10m) * 1 = (SF000002000)$



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				P08-DDR3 SODIMM-I Socket	
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Custom	Document Number	LA7322P		0.22	
Date:	Wednesday, February 16, 2011	Sheet	8	of	46





For DRAM strap pin reservation  
20100817

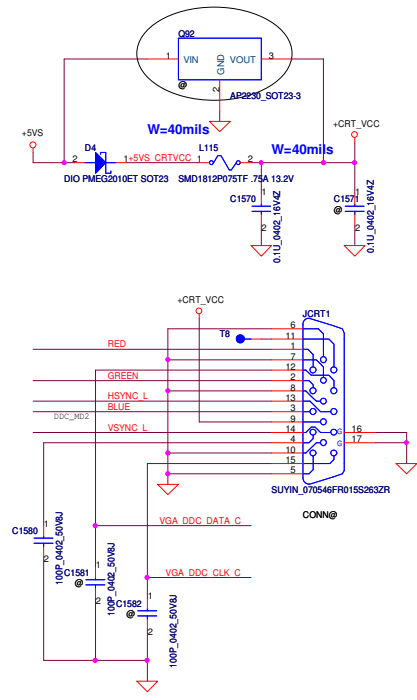
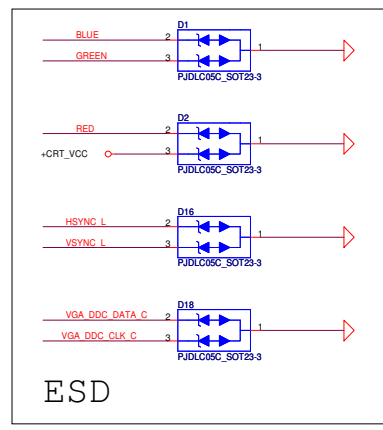
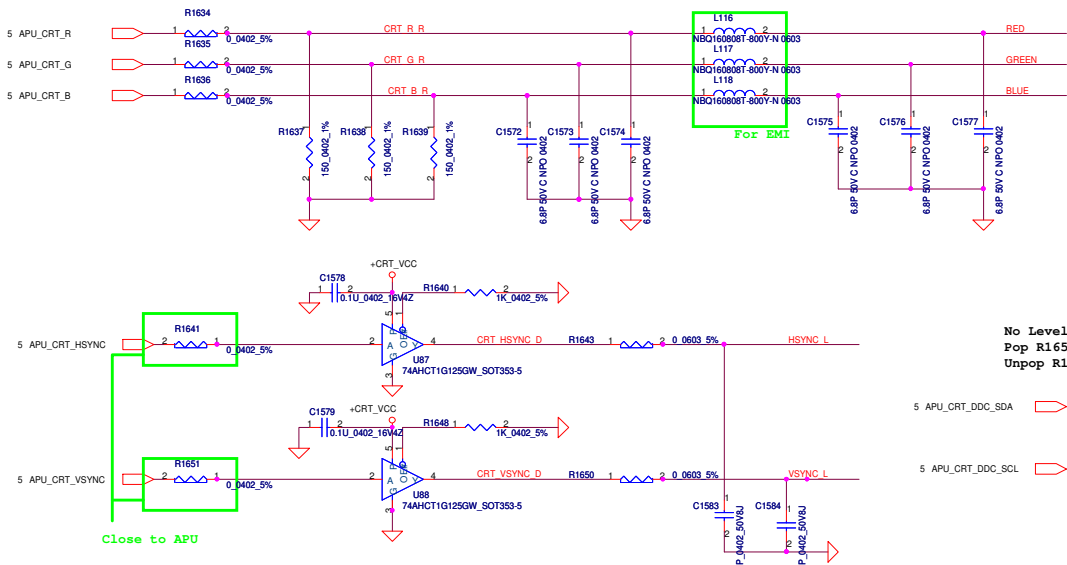
For DRAM strap pin reservation  
20100817

DDR3 SO-DIMM B H:9.2mm  
Standard Type

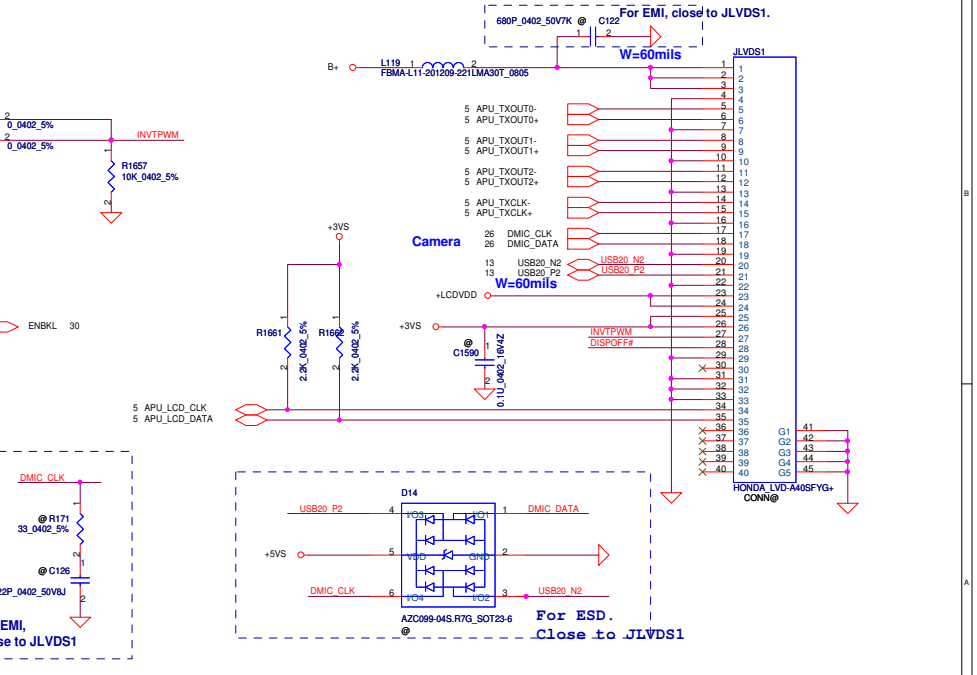
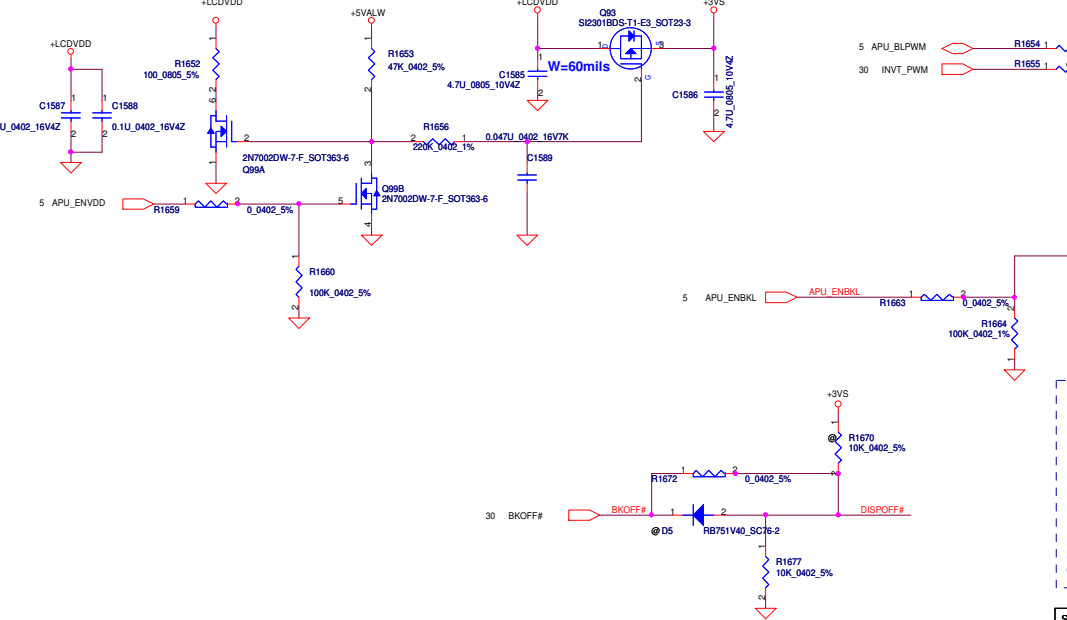
CRB only one 4.7k

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				LA7322P	0.22	
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# CRT

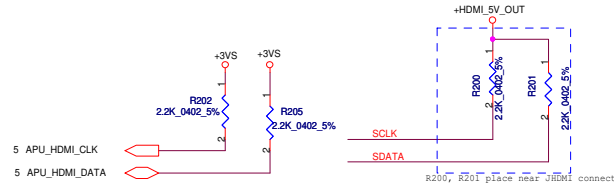
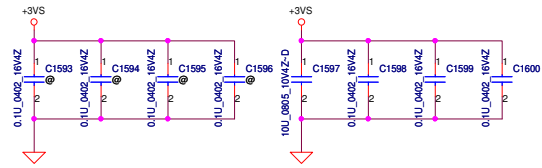


# LCD POWER CIRCUIT

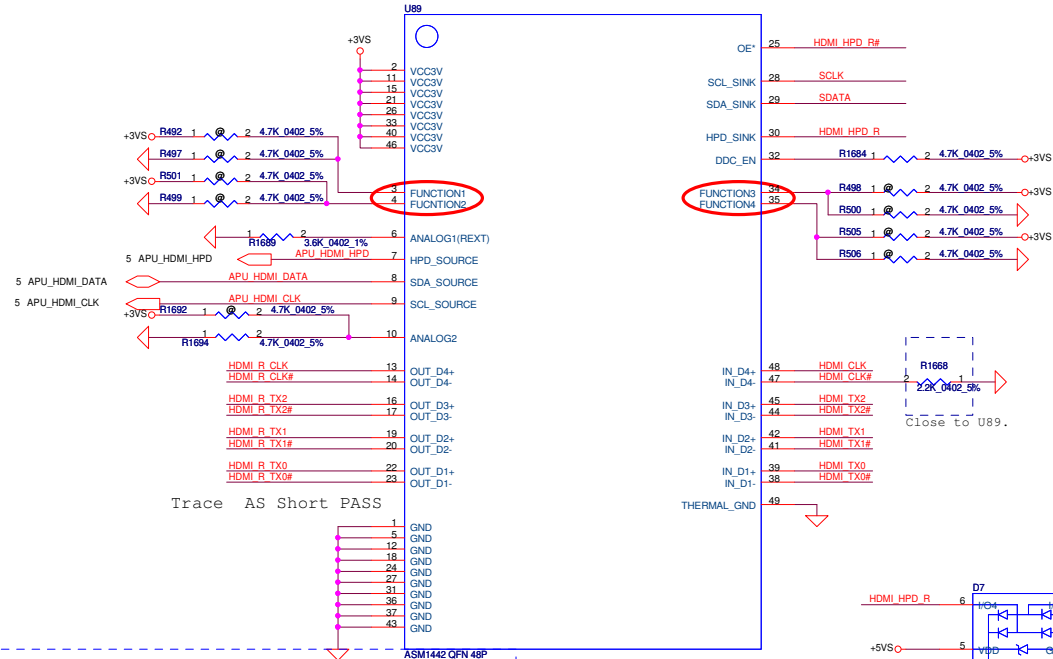
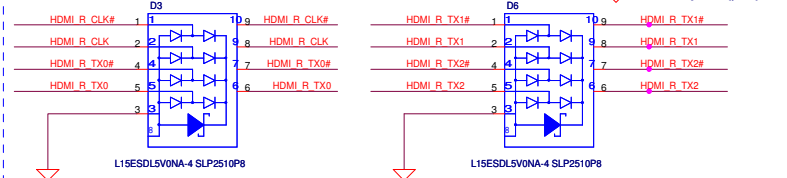
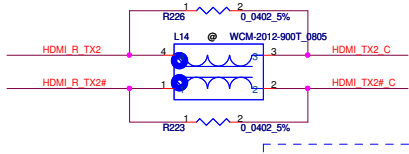
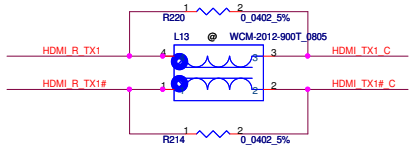
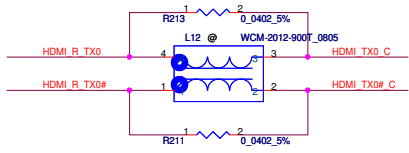
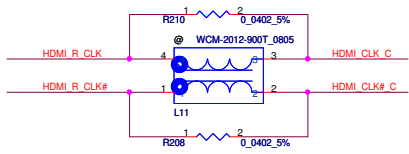


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Size	Document Number	Rev		
C	LA7321P PBL50	0.22		
Date:	Thursday, February 17, 2011	Sheet	10	of 46

close to U10VCC (+3VS) pins (one Pin one Capacitor)

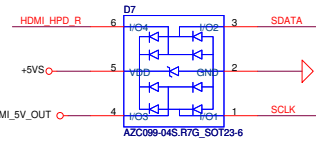
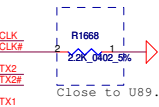
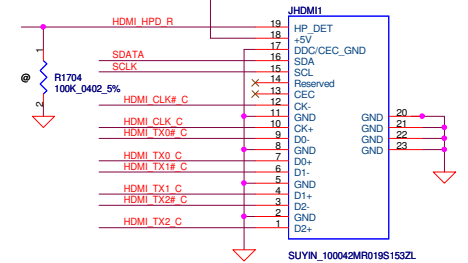
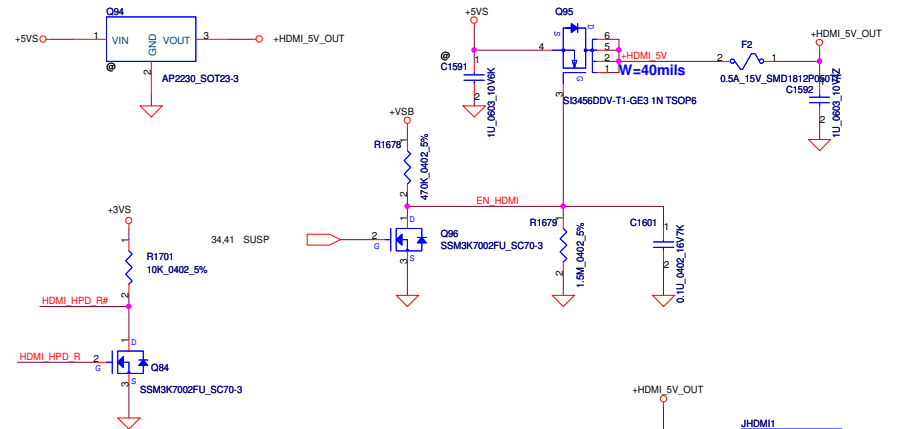


5 APU_HDMI_CLKP	C1802 1	2	0.1U 0402 16V7K	HDMI_CLK
5 APU_HDMI_CLKN	C1803 1	2	0.1U 0402 16V7K	HDMI_CLK#
5 APU_HDMI_TX0P	C1804 1	2	0.1U 0402 16V7K	HDMI_TX0
5 APU_HDMI_TX0N	C1805 1	2	0.1U 0402 16V7K	HDMI_TX0#
5 APU_HDMI_TX1P	C1806 1	2	0.1U 0402 16V7K	HDMI_TX1
5 APU_HDMI_TX1N	C1807 1	2	0.1U 0402 16V7K	HDMI_TX1#
5 APU_HDMI_TX2P	C1808 1	2	0.1U 0402 16V7K	HDMI_TX2
5 APU_HDMI_TX2N	C1809 1	2	0.1U 0402 16V7K	HDMI_TX2#



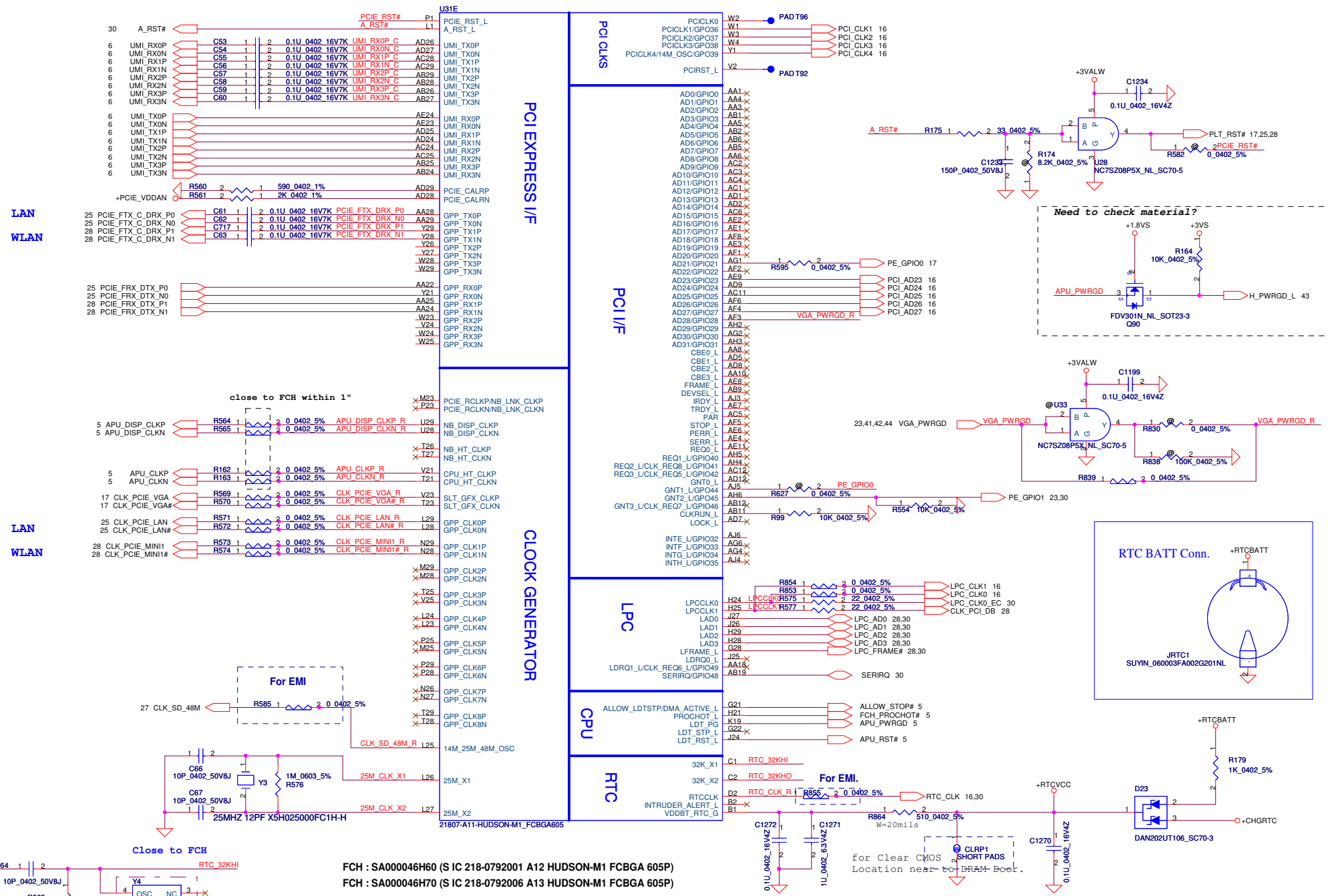
Trace AS Short PASS

ASM1442 QFN 48P



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Date:	Wednesday, February 16, 2011	Sheet	11	of 46	

For ESD request.

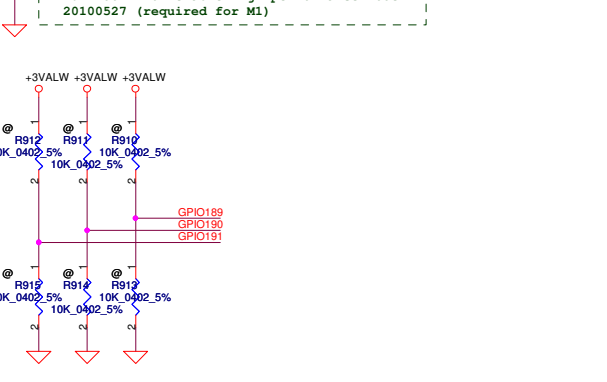
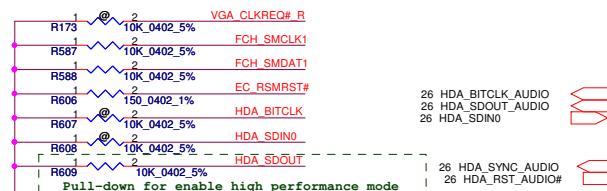
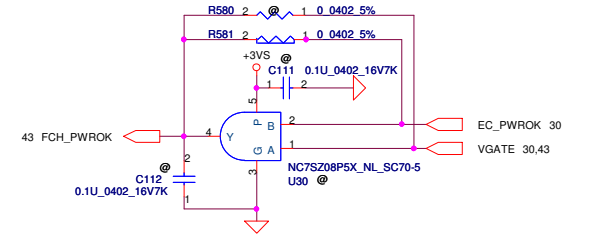
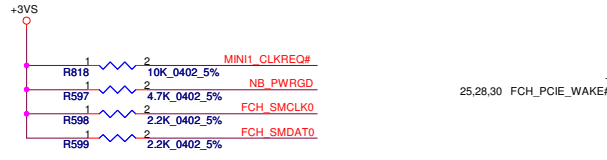
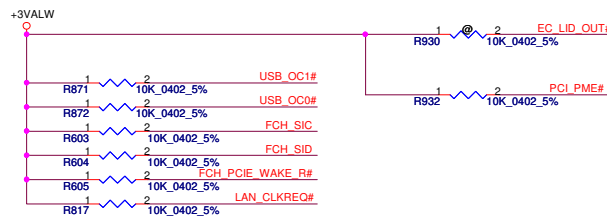


FCH : SA000046H60 (S IC 218-0792001 A13 HUDSON-M1 FCBGA 605P)  
 FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

Security Classification	Compal Secret Data	
Issued Date	2010/1/25	Deciphered Date
		2011/12/31

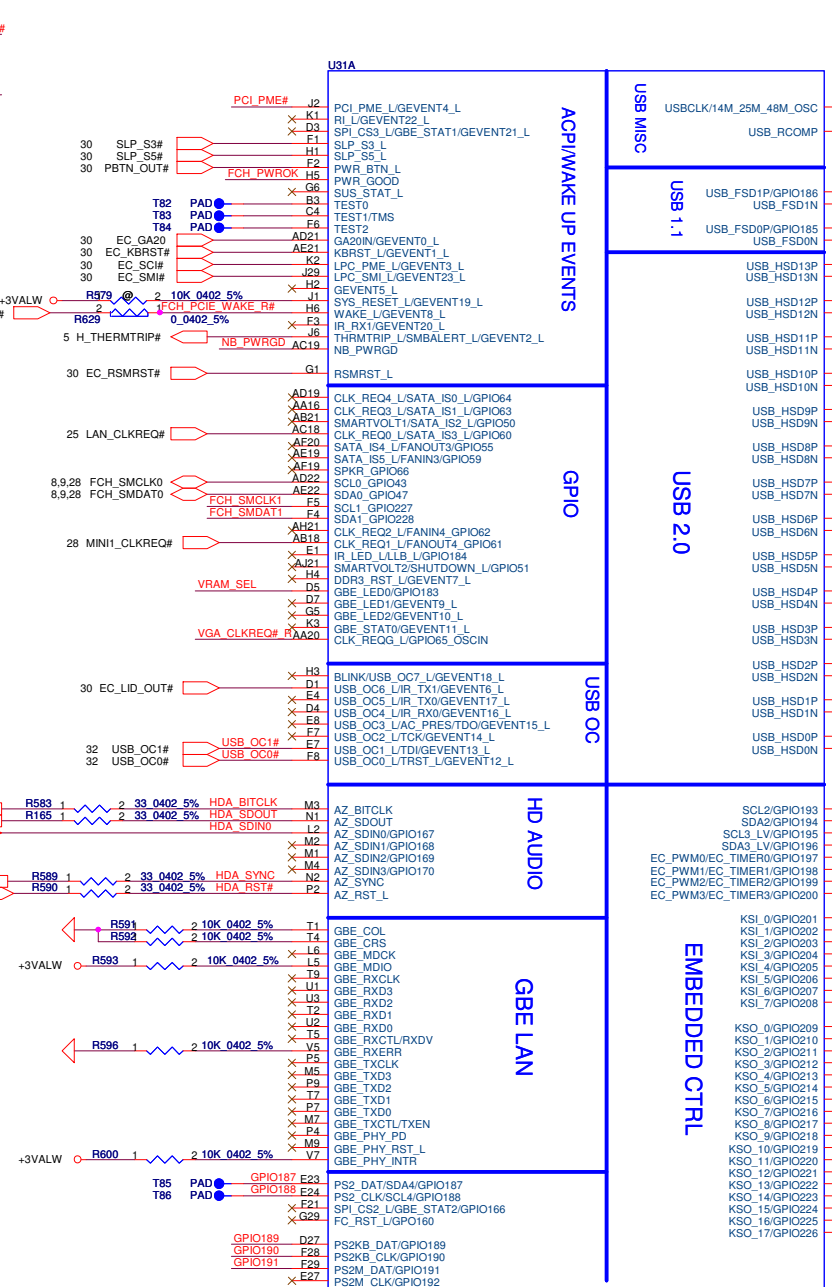
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P12-FCH PCIE/PCI/ACPI/LPC/RTC		
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SKU_ID (GPIO189)	SKU_ID : 1->VGA* 0->UMA	GPIO	189	190	191
PX_FN (GPIO190)	PX_Function : 1->PX Enable* 0->PX Disable	UMA	0	0	1
PX_SEL (GPIO191)	PX_SEL : 1->PX 3.0* 0->PX 4.0	DISO	1	0	1
		PX3.0	1	1	1
		PX4.0	1	1	0

Do not Use In PBL50/60/70

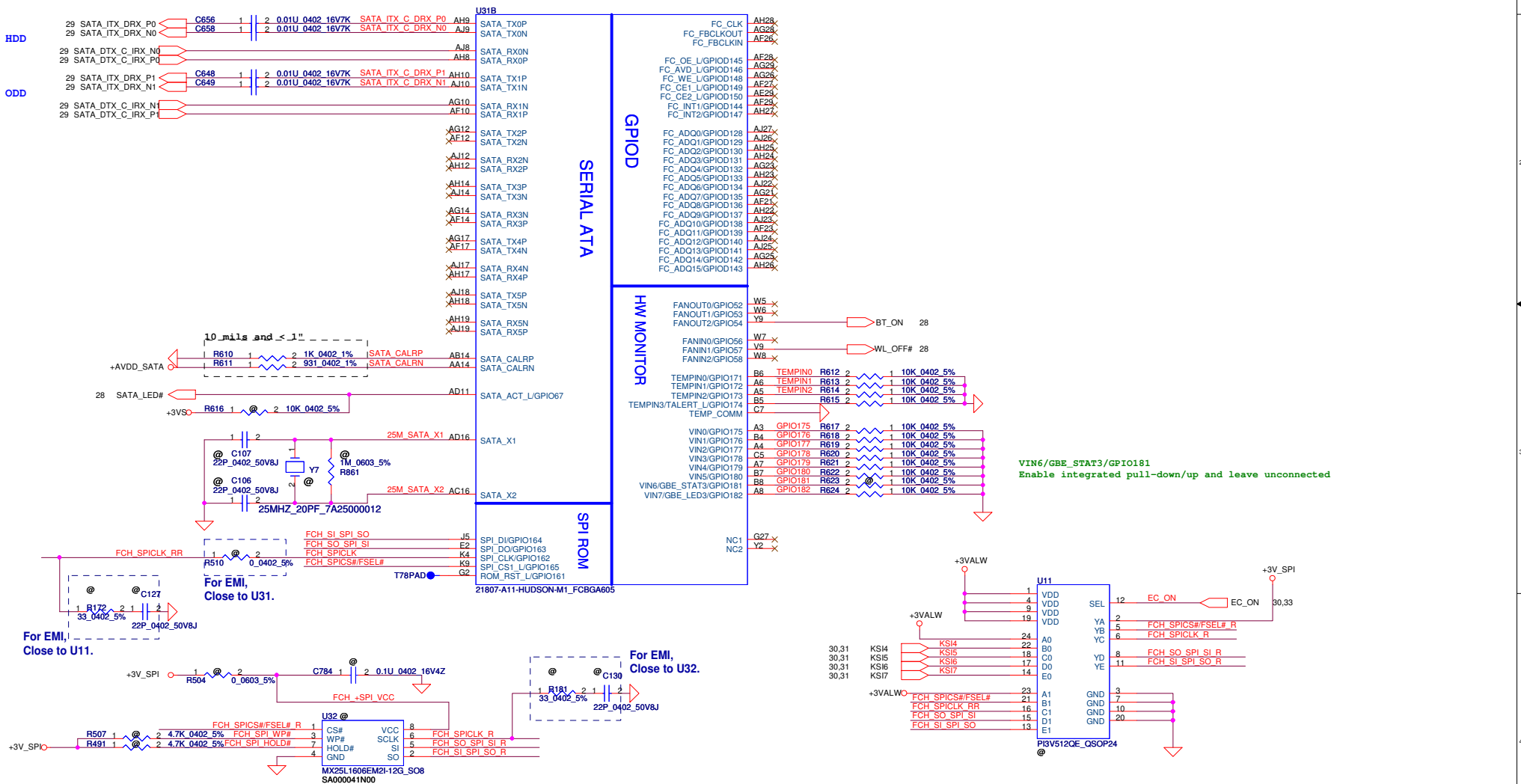


21807-A11-HUDSON-M1\_FCBGA605

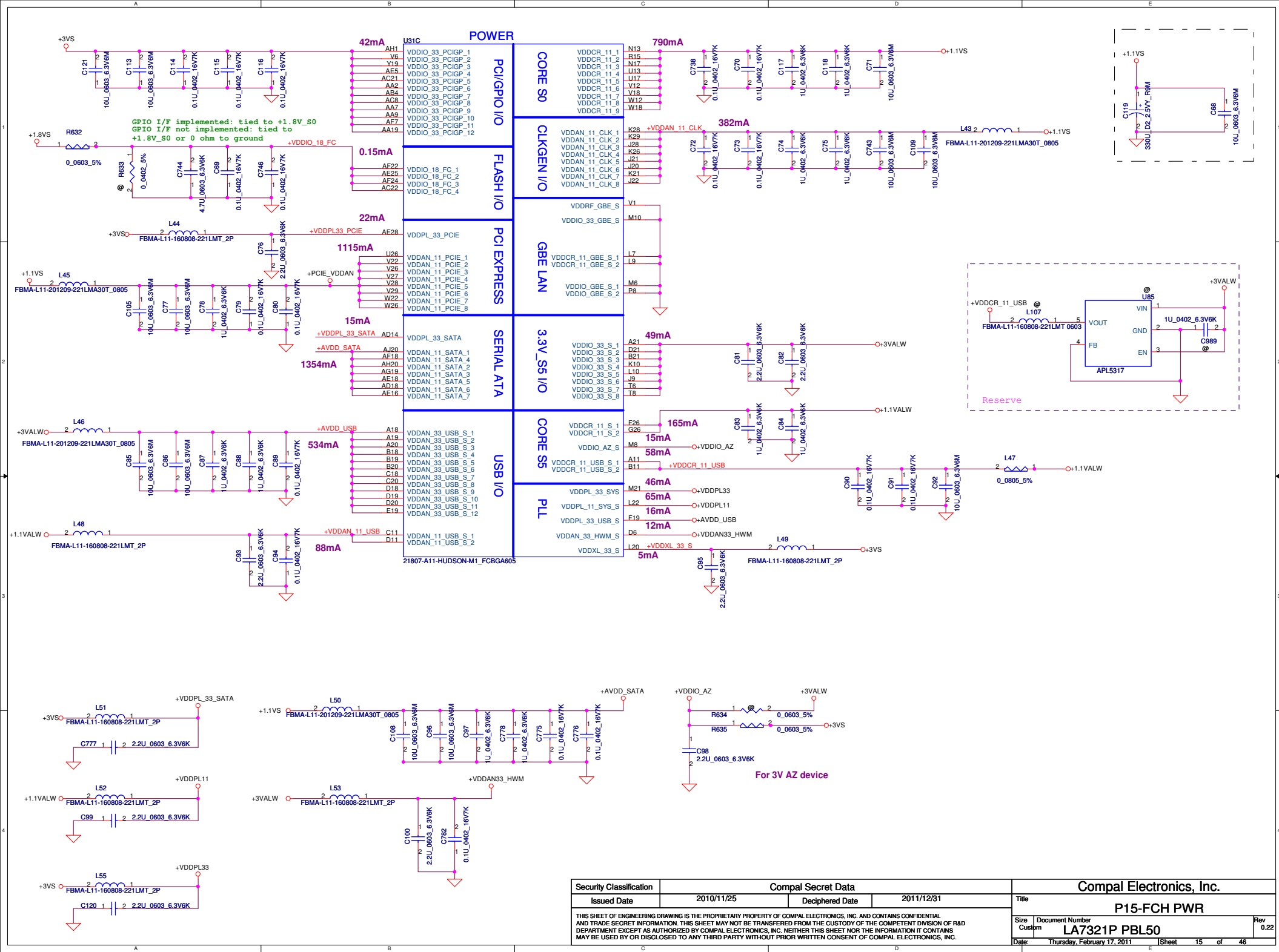
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Issued Date	2010/11/25	Deciphered Date
		2011/12/31

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Title			
P13-FCH HDA/USB/ACPI			
Size	Document Number	Rev	
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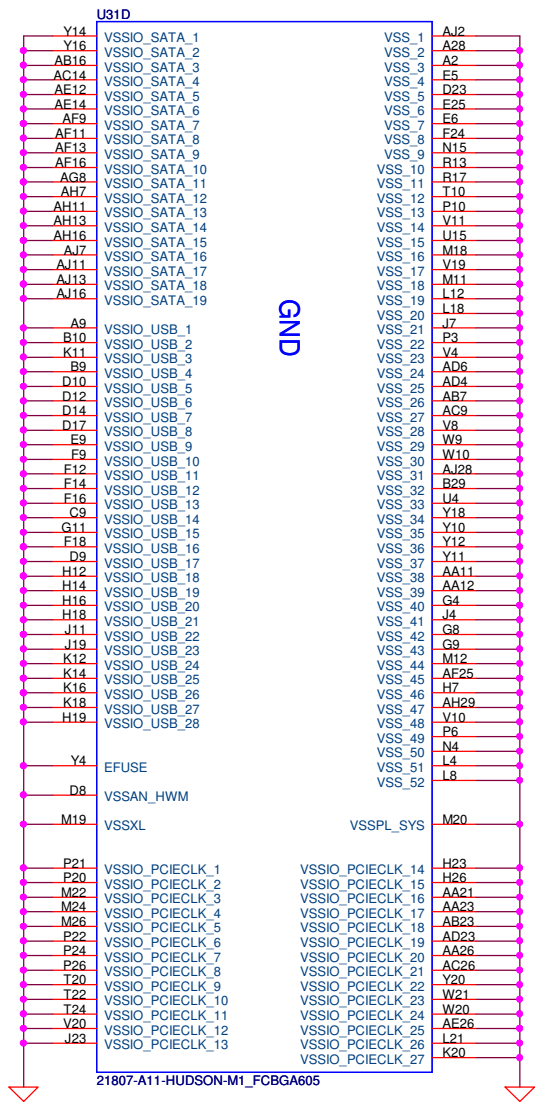


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				P14-FCH-SATA/SPI		
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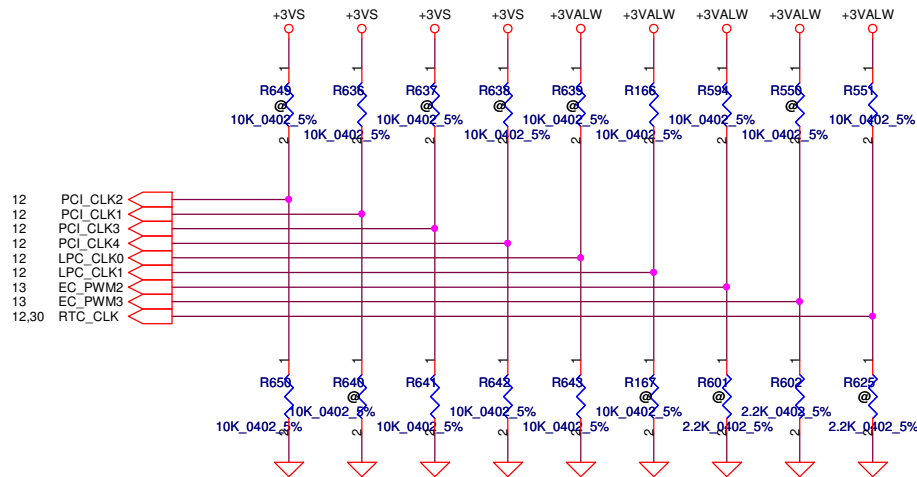
Compal Electronics, Inc.			
<b>P15-FCH PWR</b>			
Title	Document Number	Rev	
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# REQUIRED STRAPS

Check Internal PU/PD

PULL HIGH	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2  DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	Internal EC ENABLE	Internal CLKGEN Mode  DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L)  *
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP  DEFAULT	Fusion CLOCK Mode  DEFAULT	Internal EC DISABLE  DEFAULT	External CLKGEN Mode  ENABLED	S5 PLUS MODE ENABLED	SPI ROM(L,H)



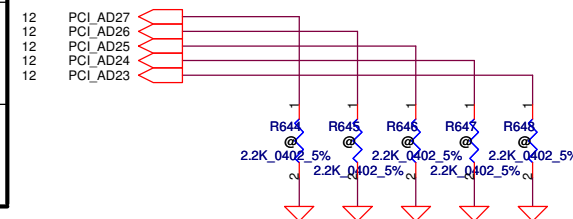
# DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

PULL HIGH	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
	USE internal PLL generated PLL CLK  DEFAULT	ILA AUTORUN Disabled  DEFAULT	Selects FC PLL  DEFAULT	Disable I2C ROM  DEFAULT	Required Setting  DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

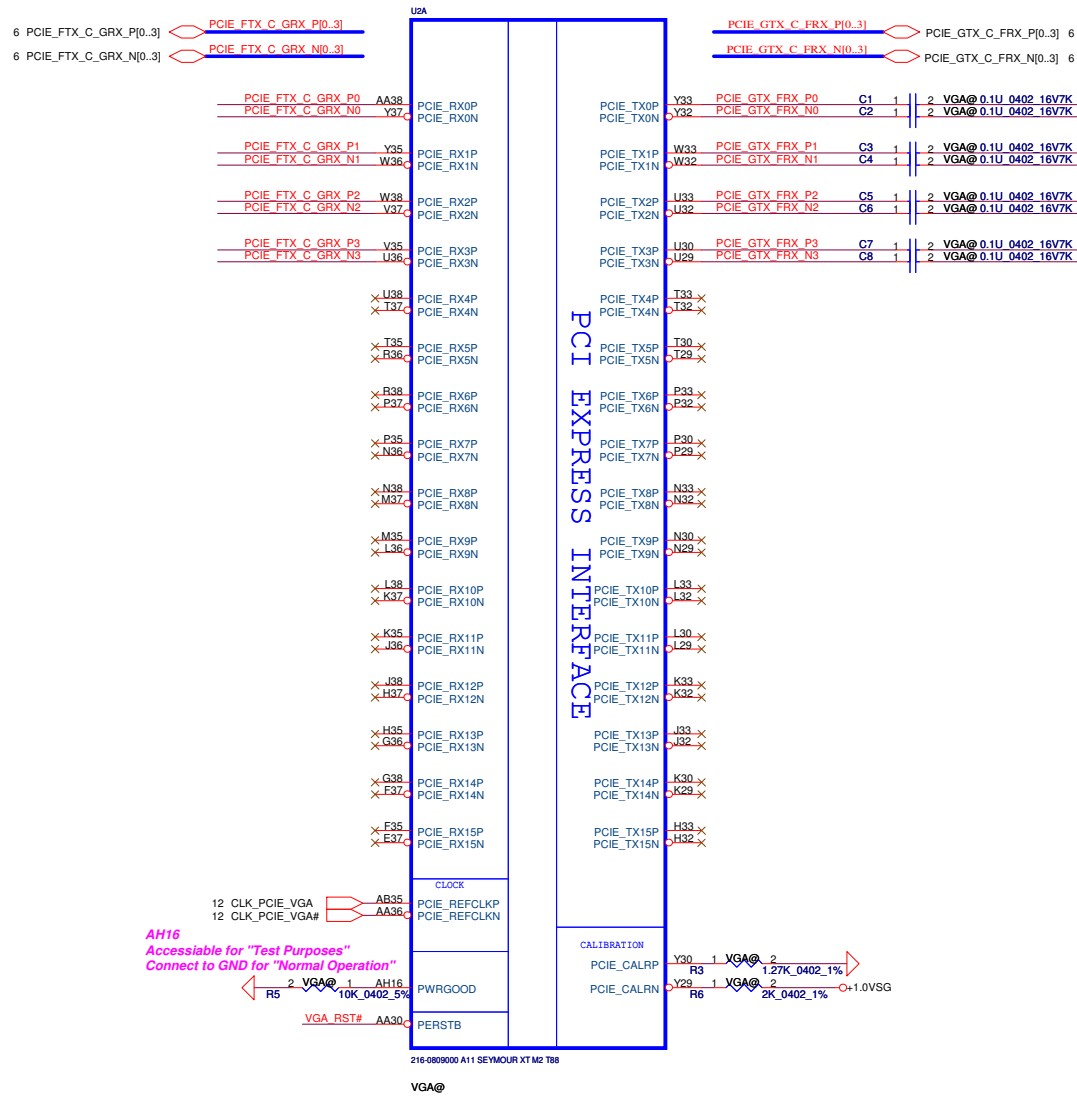
check default



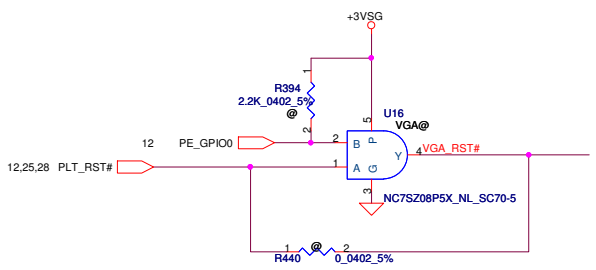
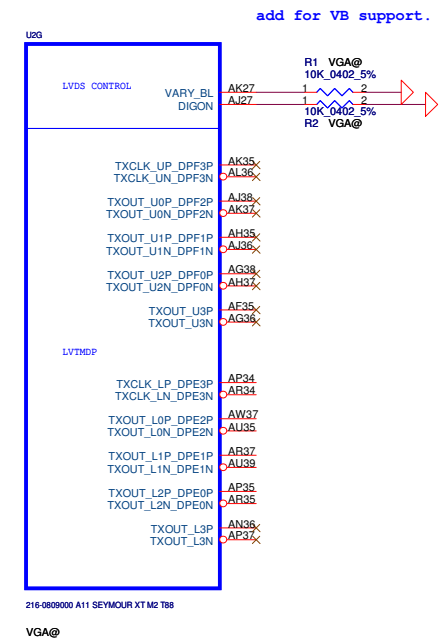
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/11/25	Deciphered Date	2011/12/31	Title P16-FCH-VSS/Strap		
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				Date: Wednesday, February 16, 2011	Sheet 16	of 46



# GFX PCIE LANE REVERSAL

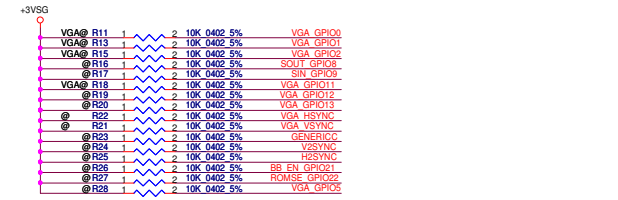
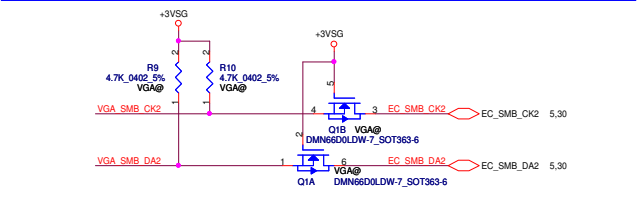
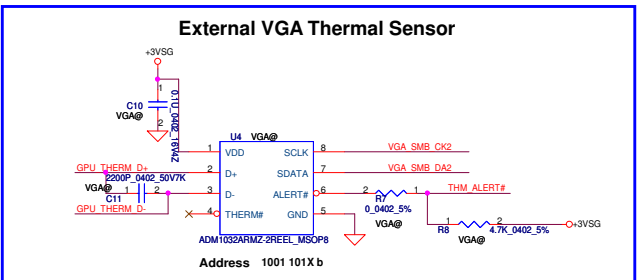


Seymour XT P/N: SA000047H10 (S IC 216-0809000 A11 SEYMOUR XT M2)



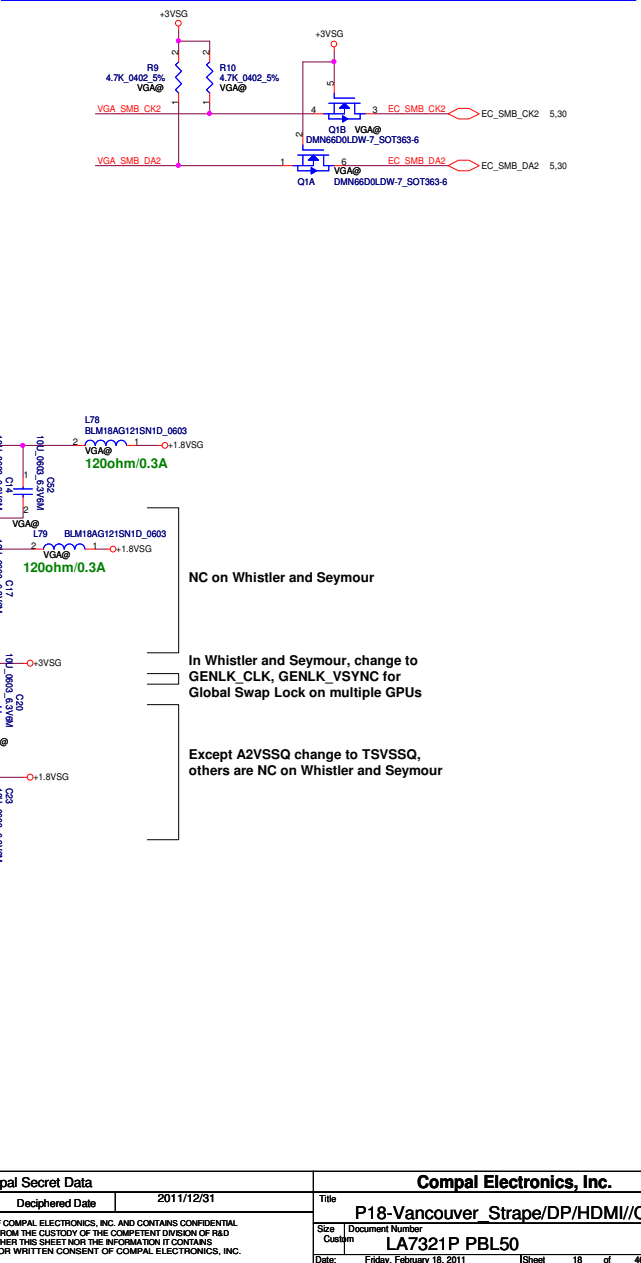
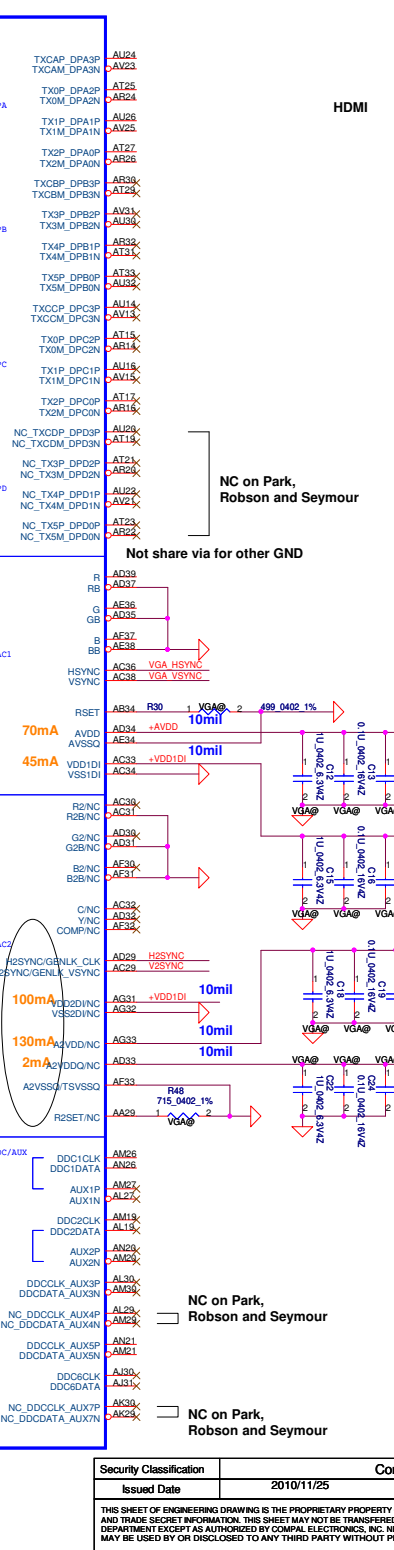
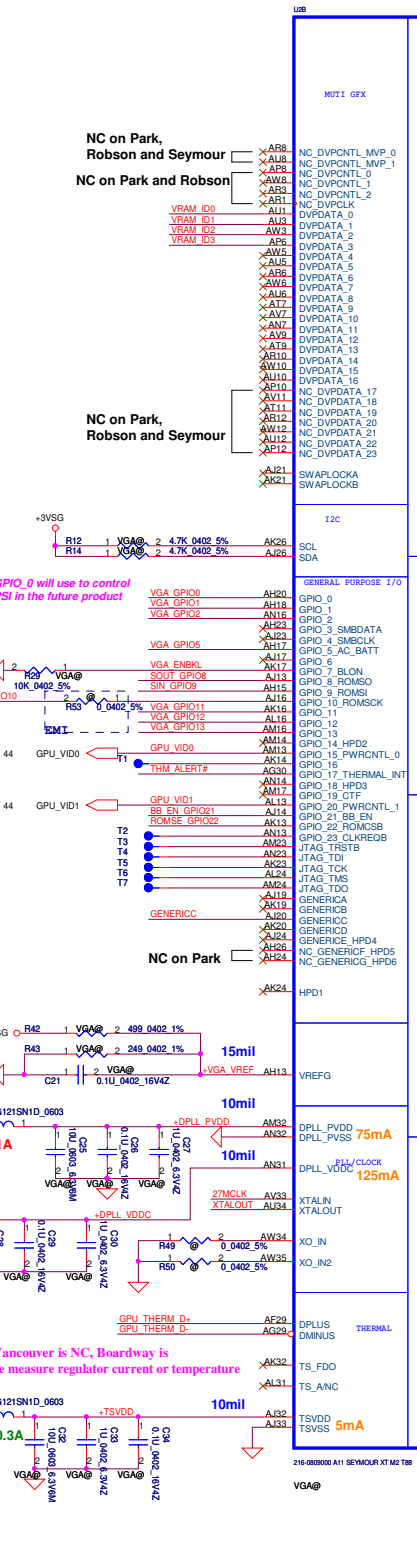
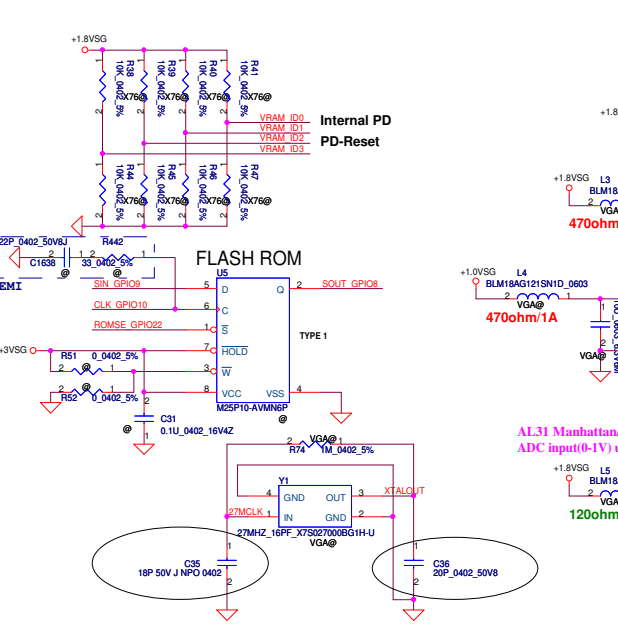
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Strap Name	Pin	Straps description <all internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) - a) If BIOS_ROM_EN = 1, then Config[3:0] defines memory apertures 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	HSYNC GENLK_CLK GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

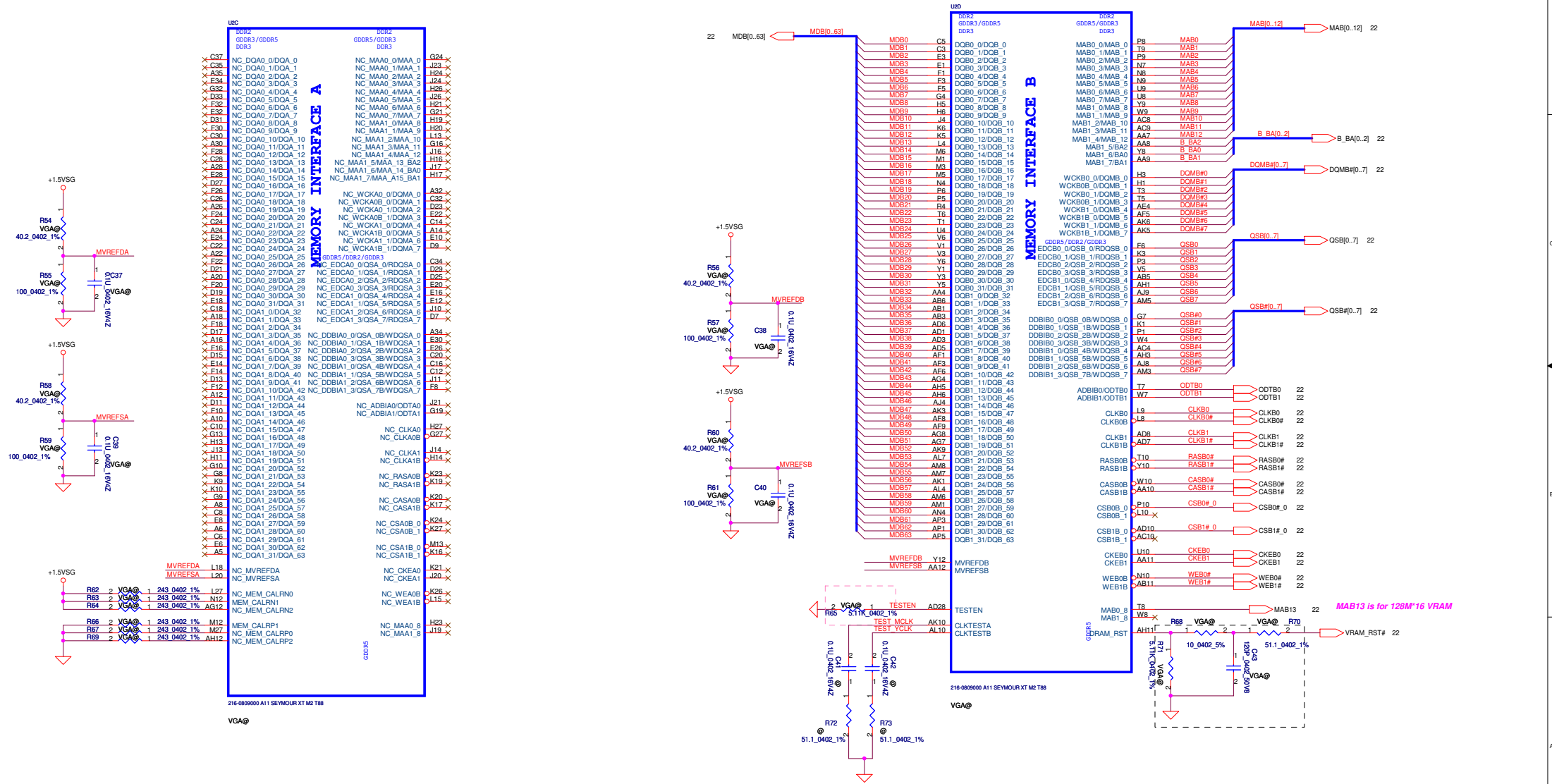


**Seymour(XT)**

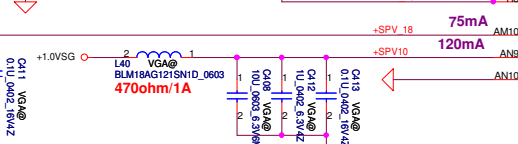
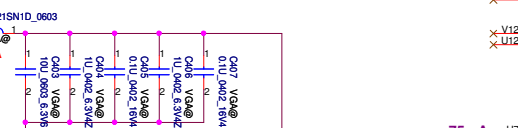
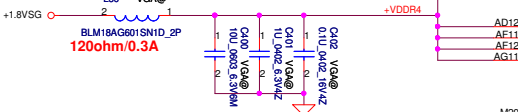
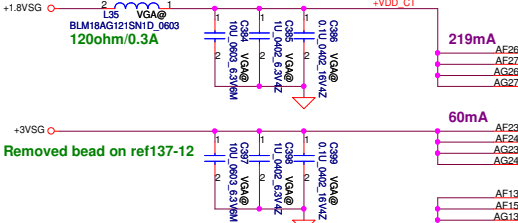
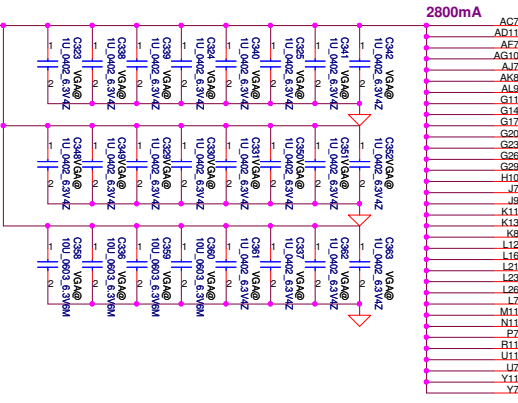
VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung 1G	X76L01	0	0	0	1
Hynix 1G	X76L02	0	1	0	1
Samsung 512M	X76L03	0	0	0	0
Hynix 512M	X76L04	0	1	0	0



# Robson, Seymour only support single channel memory (channel B only)

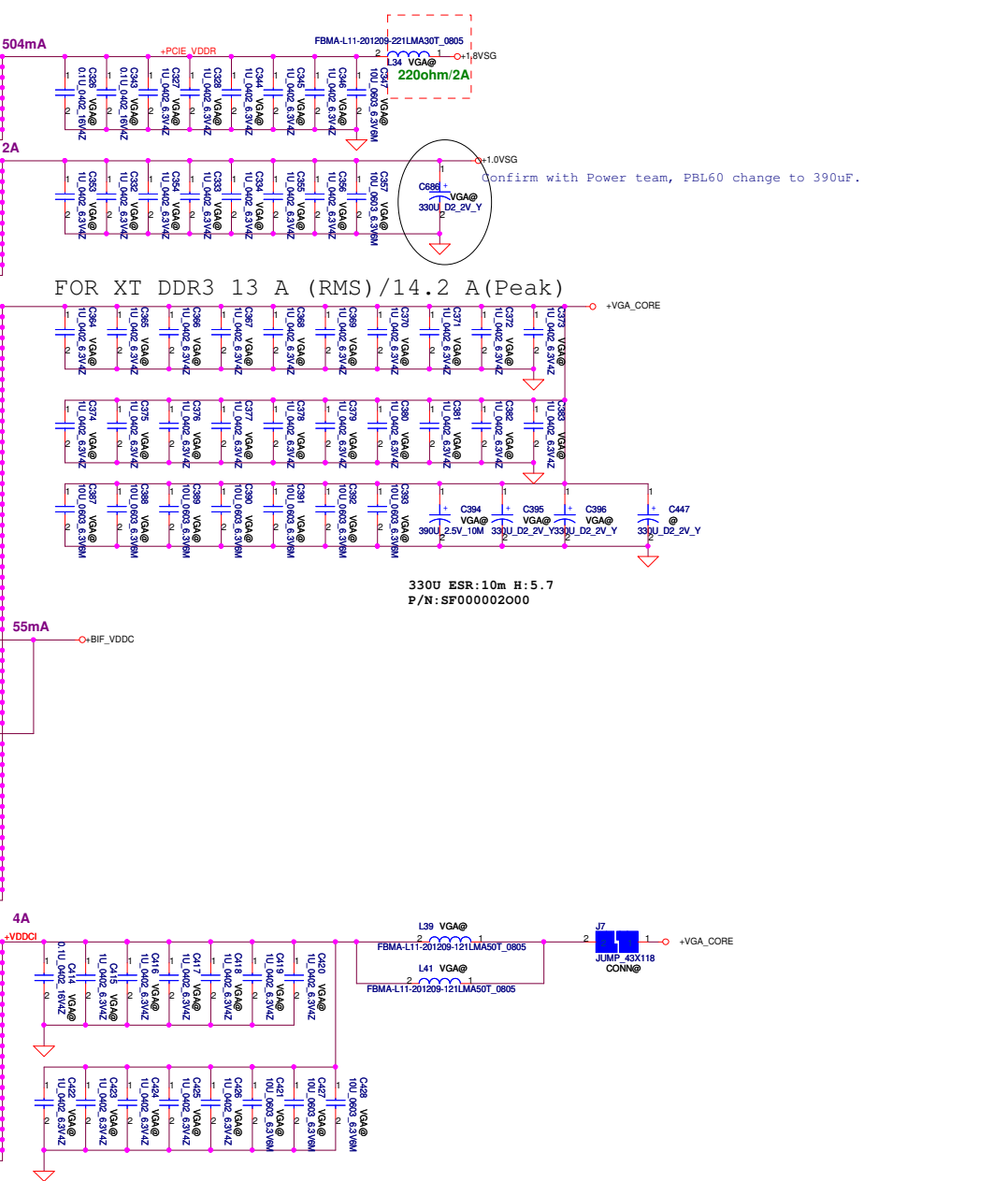


390U ESR:10m H:5.7  
P/N:SF000002000

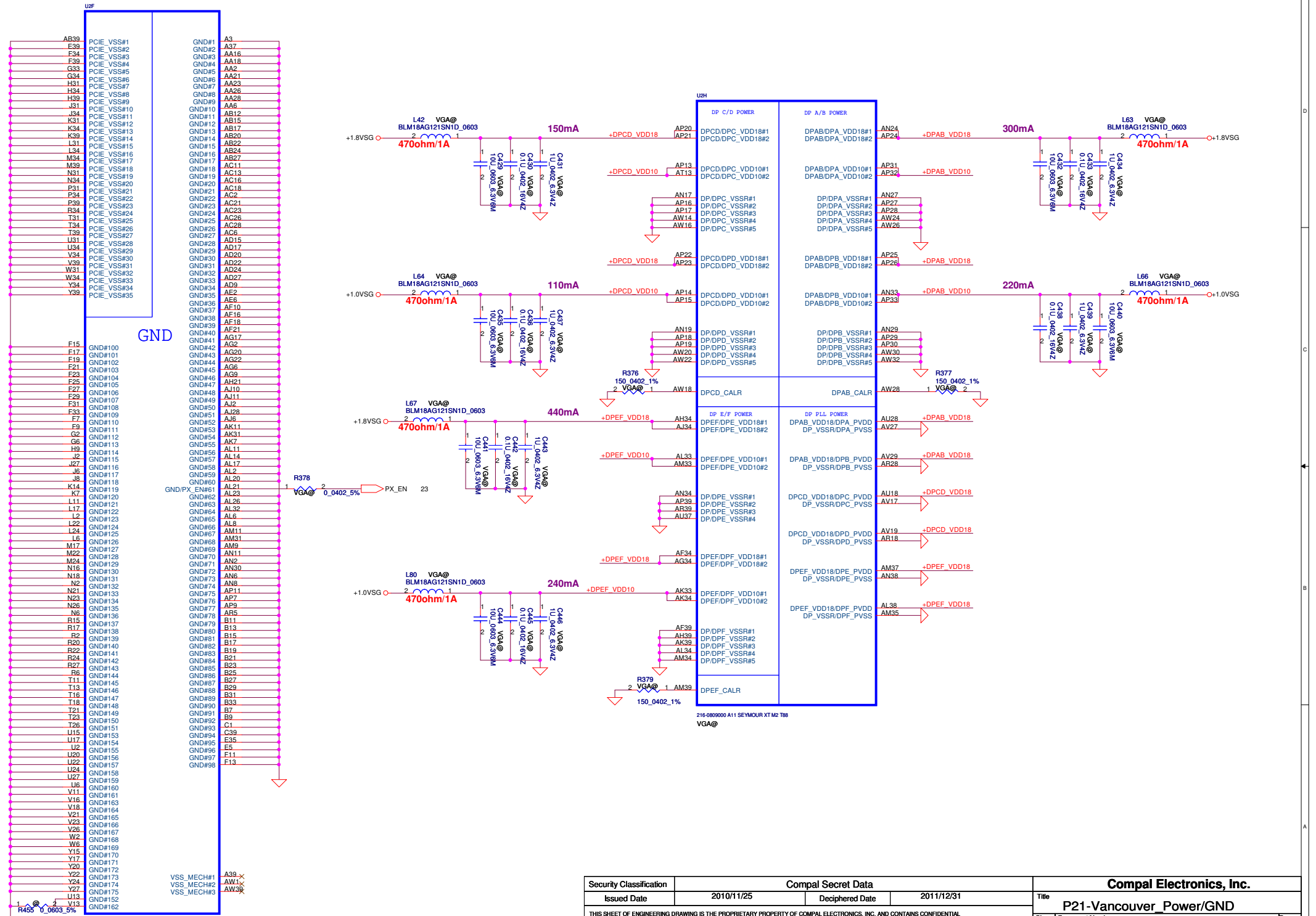


MEM I/O	AC7 VDDR1#1 AD11 VDDR1#2 AF7 VDDR1#3 AG10 VDDR1#4 AK8 VDDR1#5 AL9 VDDR1#6 AG19 VDDR1#7 G11 VDDR1#8 G17 VDDR1#9 G20 VDDR1#10 G23 VDDR1#11 G26 VDDR1#12 G29 VDDR1#13 G32 VDDR1#14 H10 VDDR1#15 I7 VDDR1#16 J6 VDDR1#17 K11 VDDR1#18 K13 VDDR1#19 K8 VDDR1#20 L12 VDDR1#21 L16 VDDR1#22 L23 VDDR1#23 L24 VDDR1#24 L28 VDDR1#25 L17 VDDR1#26 M11 VDDR1#27 N11 VDDR1#28 L5 VDDR1#29 R17 VDDR1#30 R11 VDDR1#31 U11 VDDR1#32 Y11 VDDR1#33 Y7 VDDR1#34
LEVEL TRANSLATION	AF26 VDD_CT#1 AF27 VDD_CT#2 AG26 VDD_CT#3 AG27 VDD_CT#4
I/O	AF23 VDDR3#1 AF24 VDDR3#2 AG23 VDDR3#3 AG24 VDDR3#4 AF13 VDDR4#4 AF15 VDDR4#5 AG13 VDDR4#7 AG15 VDDR4#8 AD12 VDDR4#1 AF11 VDDR4#2 AF12 VDDR4#3 AG11 VDDR4#6
PLL	NC_VDDRHA NC_VSSRHA NC_VDDRHB NC_VSSRHB
MPV	MPV1#1 MPV1#2
SPV	SPV18 SPV10 SPVSS
VOLTAGE SENSE	GCORE_SEN GCORE_SEN
FB	FB_VDDC FB_VDDCI FB_GND

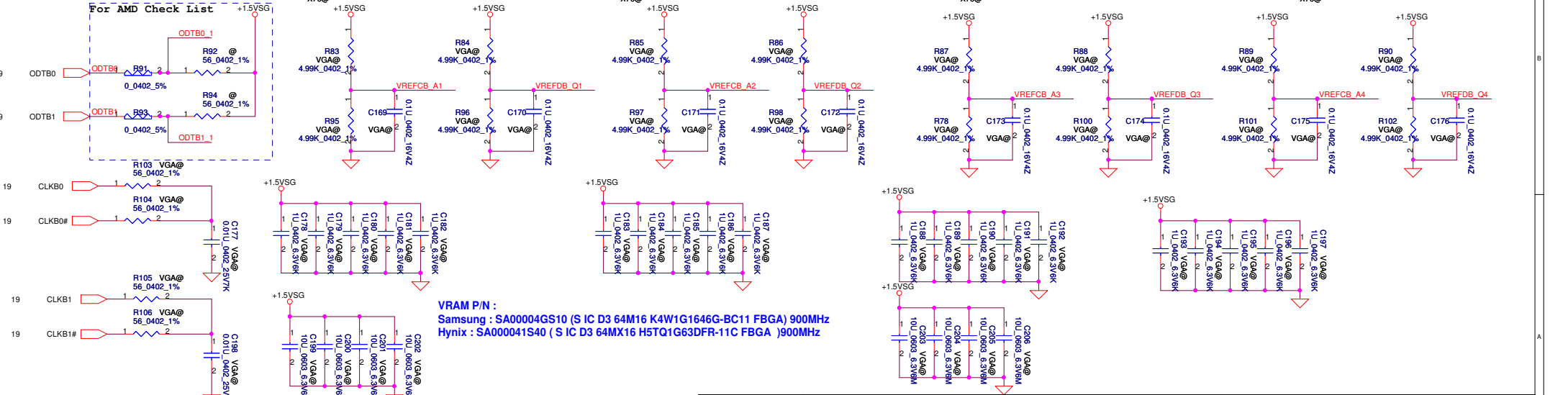
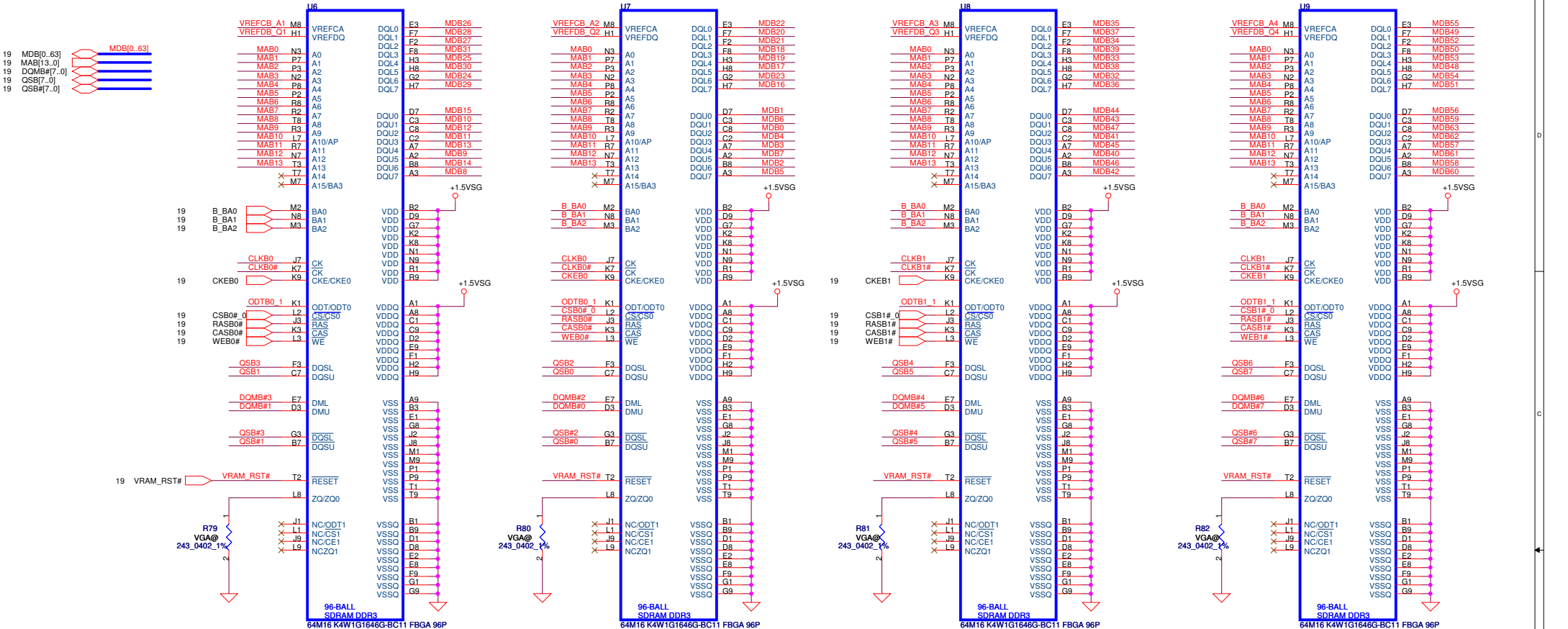
PCIE	AA31 PCIE_VDDR#1 AA32 PCIE_VDDR#2 AA33 PCIE_VDDR#3 AA34 PCIE_VDDR#4 V28 PCIE_VDDR#5 V29 PCIE_VDDR#6 W30 PCIE_VDDR#7 Y31 PCIE_VDDR#8 AB37 PCIE_VDDR#9 G30 PCIE_VDDC#1 G31 PCIE_VDDC#2 G32 PCIE_VDDC#3 H30 PCIE_VDDC#4 H39 PCIE_VDDC#5 J30 PCIE_VDDC#6 L28 PCIE_VDDC#7 L28 PCIE_VDDC#8 M28 PCIE_VDDC#9 N28 PCIE_VDDC#10 R28 PCIE_VDDC#11 T28 PCIE_VDDC#12 U28
CORE	AA15 VDDC#1 AA20 VDDC#2 AA21 VDDC#3 AA22 VDDC#4 AA24 VDDC#5 AA27 VDDC#6 AB18 VDDC#7 AB18 VDDC#8 AB21 VDDC#9 AB23 VDDC#10 AB26 VDDC#11 AC17 VDDC#12 AC20 VDDC#13 AC22 VDDC#14 AC24 VDDC#15 AC27 VDDC#16 AD18 VDDC#17 AD23 VDDC#18 AD26 VDDC#19 AE17 VDDC#20 AE22 VDDC#21 AE22 VDDC#22 AG16 VDDC#23 AG16 VDDC#24 AG16 VDDC#25 AG16 VDDC#26 AG21 VDDC#27 AG21 VDDC#28 AH28 VDDC#29 AH28 VDDC#30 M26 VDDC#31 N24 VDDC#32 N24 VDDC#33 R18 VDDC#34 R21 VDDC#35 R23 VDDC#36 R26 VDDC#37 R26 VDDC#38 T17 VDDC#39 T20 VDDC#40 T22 VDDC#41 T24 VDDC#42 T27 VDDC#43 U16 VDDC#44 U18 VDDC#45 U21 VDDC#46 U26 VDDC#47 V17 VDDC#48 V20 VDDC#49 V22 VDDC#50 V24 VDDC#51 V24 VDDC#52 V27 VDDC#53 Y18 VDDC#54 Y18 VDDC#55 Y21 VDDC#56 Y26 VDDC#57 Y26 VDDC#58 Y28
VDDC#BIF	VDDC#32 VDDC#33 VDDC#34 VDDC#35 VDDC#36 VDDC#37 VDDC#38 VDDC#39 VDDC#40 VDDC#41 VDDC#42 VDDC#43 VDDC#44 VDDC#45 VDDC#46 VDDC#47 VDDC#48 VDDC#49 VDDC#50 VDDC#51 VDDC#52 VDDC#53 VDDC#54 VDDC#55 VDDC#56 VDDC#57 VDDC#58
ISOLATED CORE I/O	AA18 VDDCI#1 AB13 VDDCI#2 AC12 VDDCI#3 AC15 VDDCI#4 AD13 VDDCI#5 AD16 VDDCI#6 M15 VDDCI#7 M16 VDDCI#8 M16 VDDCI#9 M18 VDDCI#10 M23 VDDCI#11 N13 VDDCI#12 N15 VDDCI#13 N17 VDDCI#14 N20 VDDCI#15 N22 VDDCI#16 R12 VDDCI#17 R13 VDDCI#18 R16 VDDCI#19 R16 VDDCI#20 T15 VDDCI#21 V15 VDDCI#22 Y13



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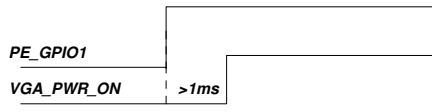
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Date:	Tuesday, February 15, 2011	Sheet	21	of	46



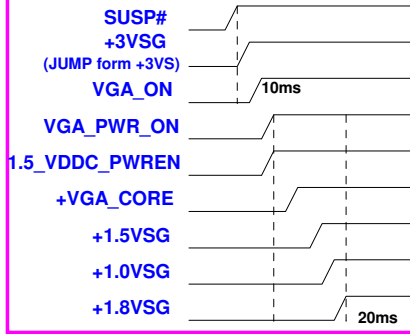
**VRAM P/N :**  
 Samsung : SA00004GS10 ( S IC D3 64M16 K4W1G1646G-BC11 FBGA ) 900MHz  
 Hynix : SA00004S40 ( S IC D3 64MX16 H5TQ1G63DFR-11C FBGA ) 900MHz

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For PX sequence, >1mS delay is required between PE\_GPIO1 and VGA\_PWR\_ON

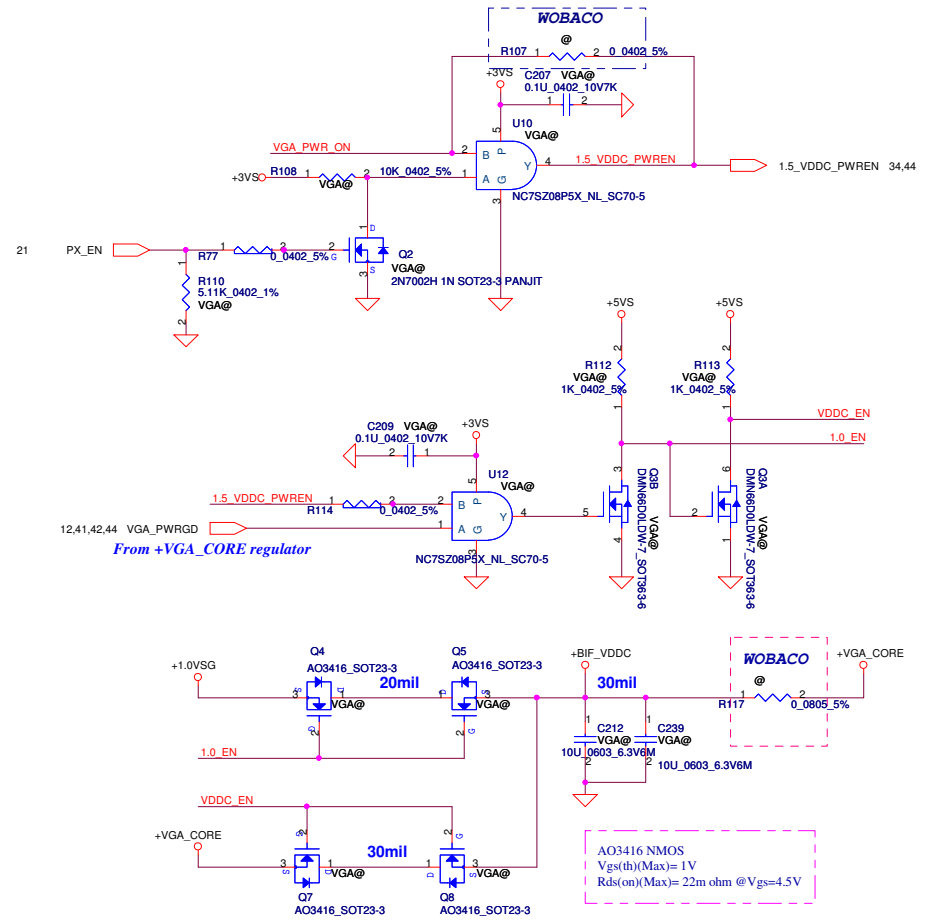
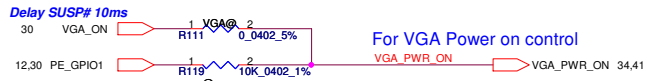


**Power Sequence of Whistler and Seymour**

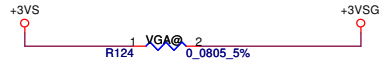


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

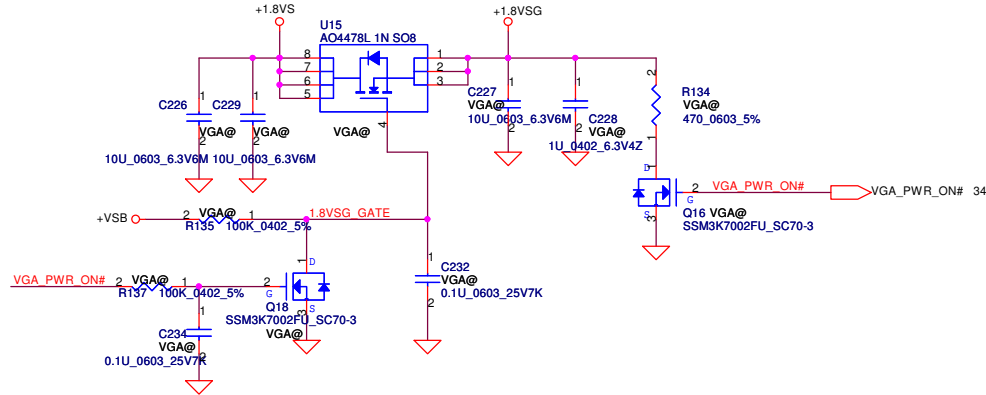
VGA Power Enable Signal Mapping table		
VGA_PWR_ON source signal	Graville	Whistler and Seymour
INT_VGAPWR_ON	VGA_PWR_ON	SUSP#
+3.3VSG	VGA_PWR_ON	VGA_PWR_ON
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN



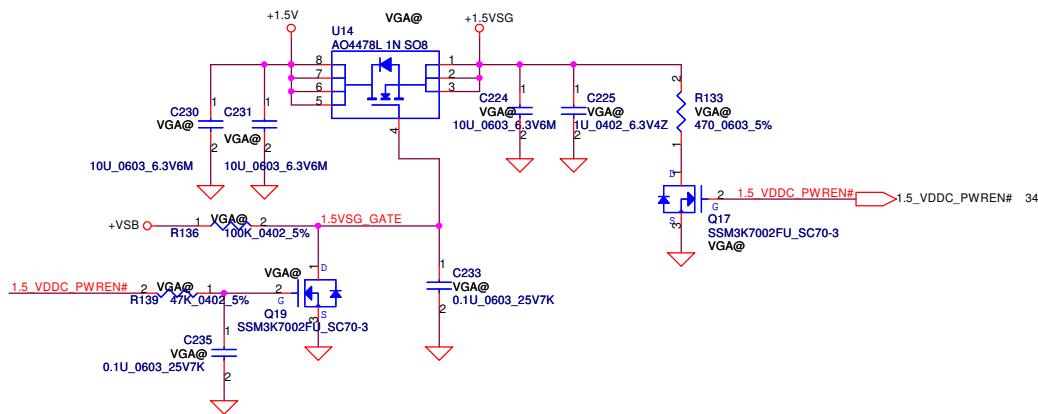
**+3.3VS TO +3.3VSG**



**+1.8VS TO +1.8VSG**



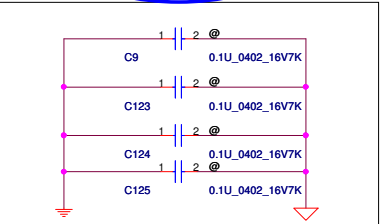
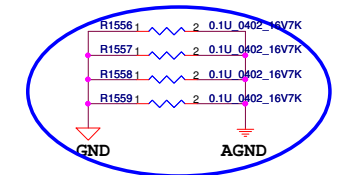
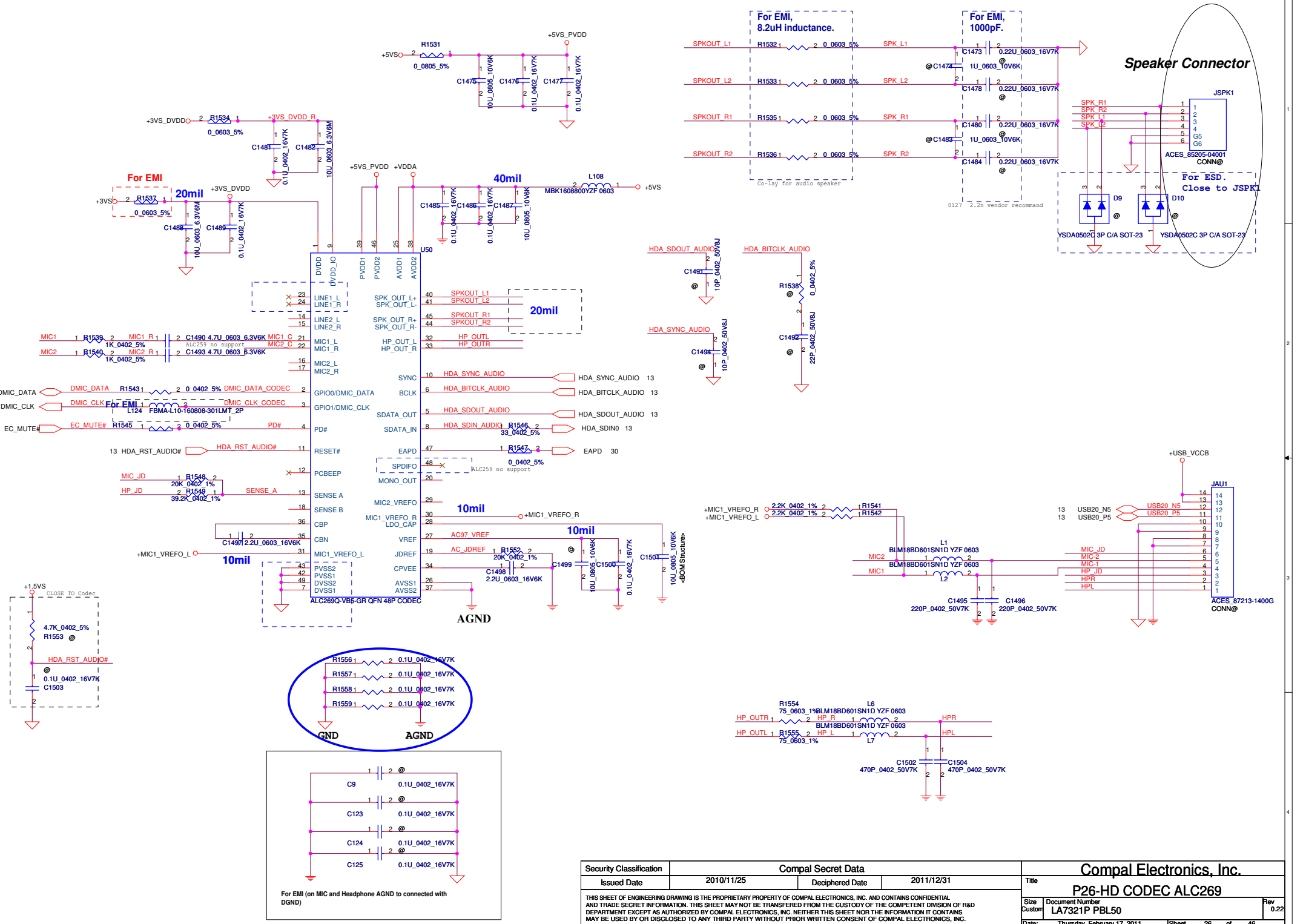
**+1.5V TO +1.5VSG**



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Size	Custom	Document Number	LA7321P PBL50	Rev	0.22
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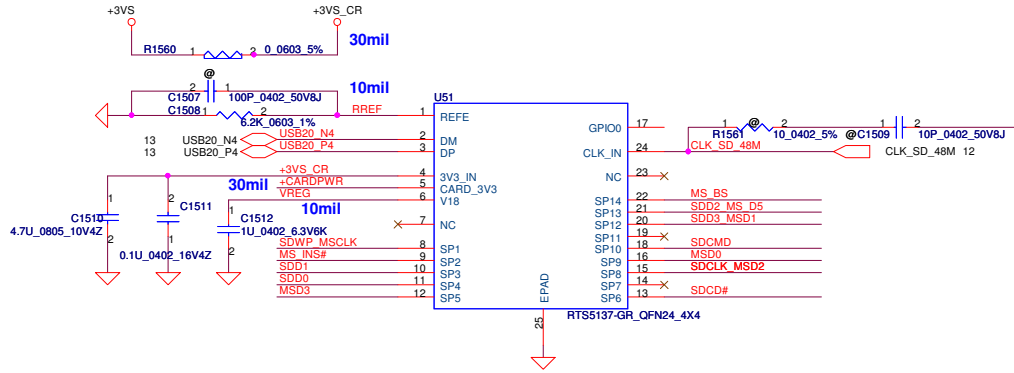




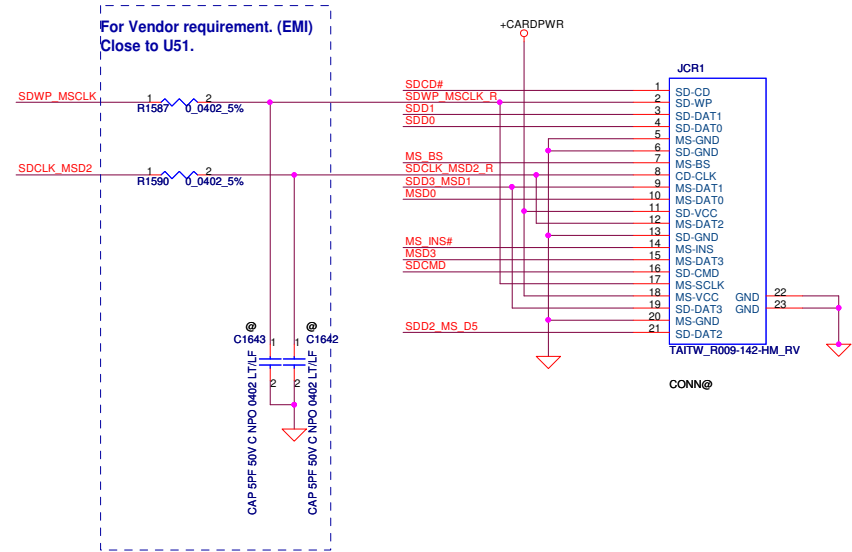
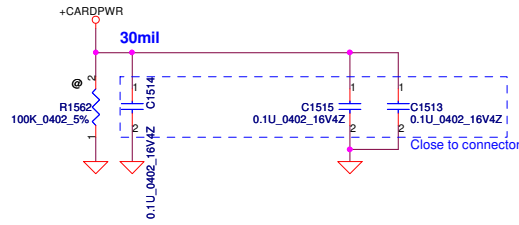
For EMI (on MIC and Headphone AGND to connected with DGND)

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Size	Document Number	Rev			
Custom	LA7321P PBL50	0.22			
Date:	Thursday, February 17, 2011	Sheet	26	of 46	

# Card Reader RTS5137 (only SD/MMC/MS function)

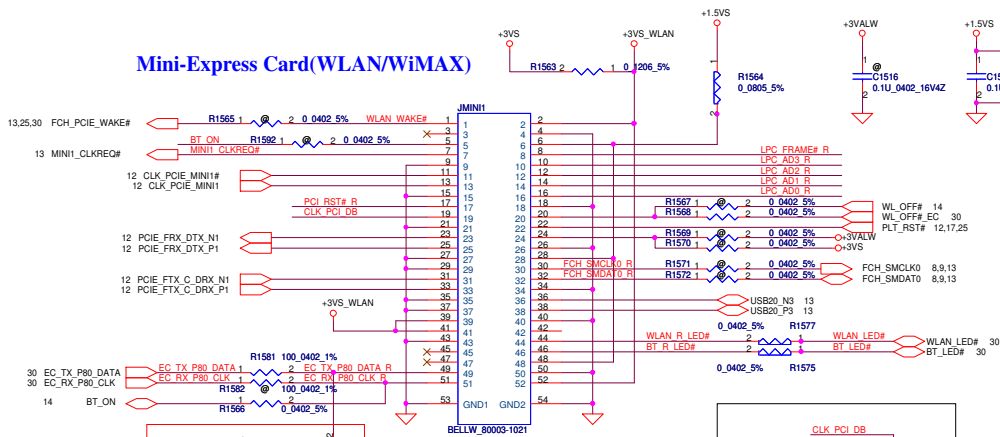


# Card Reader Connector



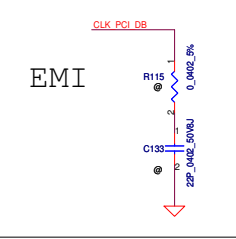
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				Rev 0.22

# Mini-Express Card for WLAN/WiMAX(Half)



## Mini-Express Card(WLAN/WiMAX)

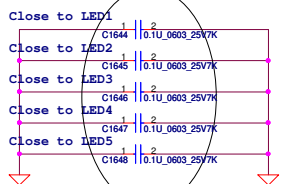
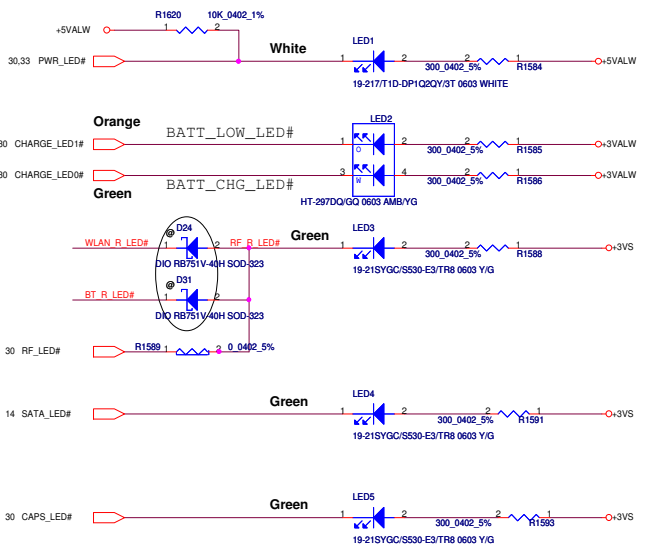
For EC to detect debug card insert.



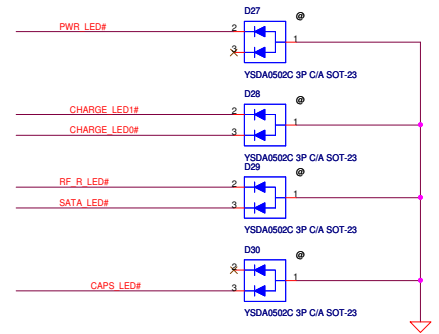
**Reserve for SW mini-pcie debug card. Series resistors closed to KBC side.**

LPC_FRAME# R	R1573	1	2	0.0402_5%	LPC_FRAME#	12,30
LPC_AD3# R	R1574	1	2	0.0402_5%	LPC_AD3	12,30
LPC_AD2# R	R1575	1	2	0.0402_5%	LPC_AD2	12,30
LPC_AD1# R	R1576	1	2	0.0402_5%	LPC_AD1	12,30
LPC_AD0# R	R1577	1	2	0.0402_5%	LPC_AD0	12,30
PLT_RST#	R1578	1	2	0.0402_5%	PLT_RST#	12,17,25
CLK_PCIE_DB	R1580	1	2	0.0402_5%	CLK_PCIE_DB	12

## LED

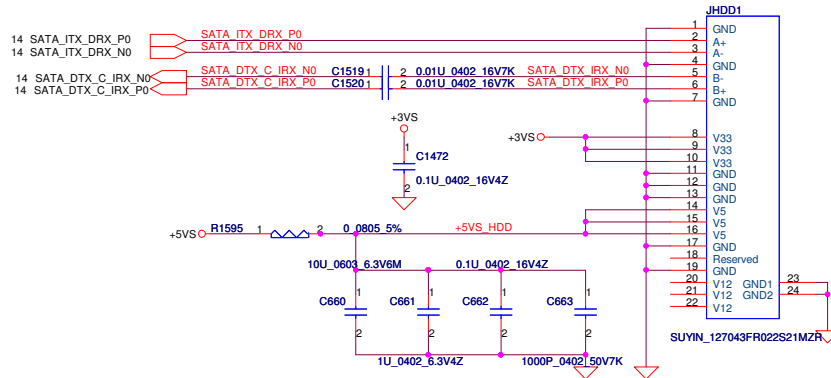


For ESD.  
Cap to LED gap is 1.2mm.

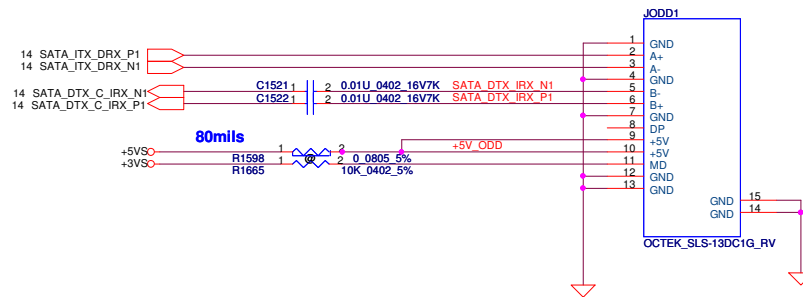


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Date:	Friday, February 18, 2011	Sheet:	28	of 46

### SATA HDD Conn.

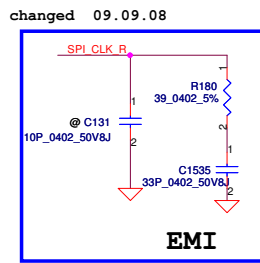
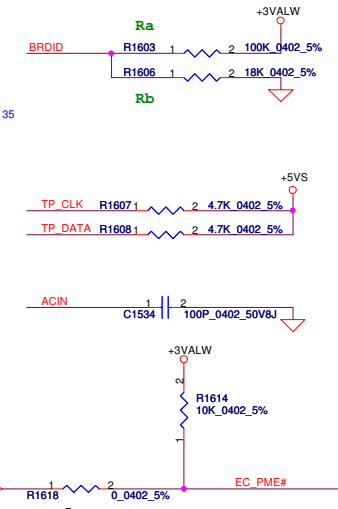
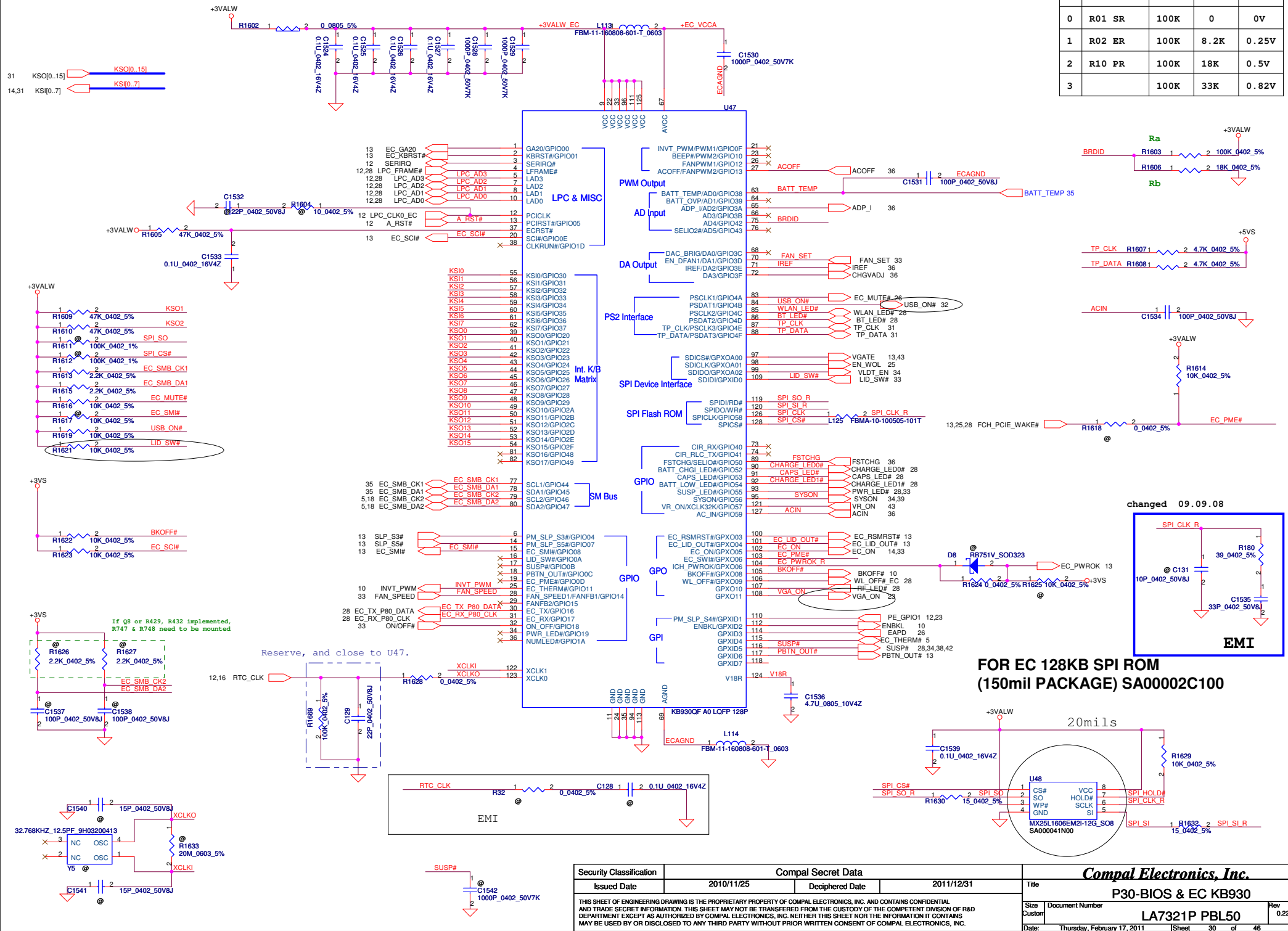


### SATA ODD FFC Conn.

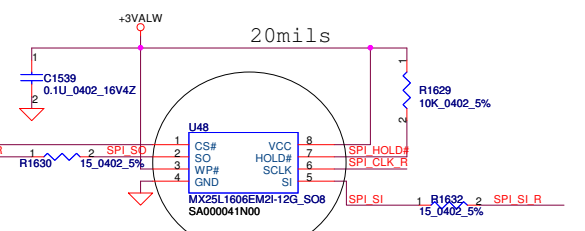


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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 PR	100K	18K	0.5V
3		100K	33K	0.82V

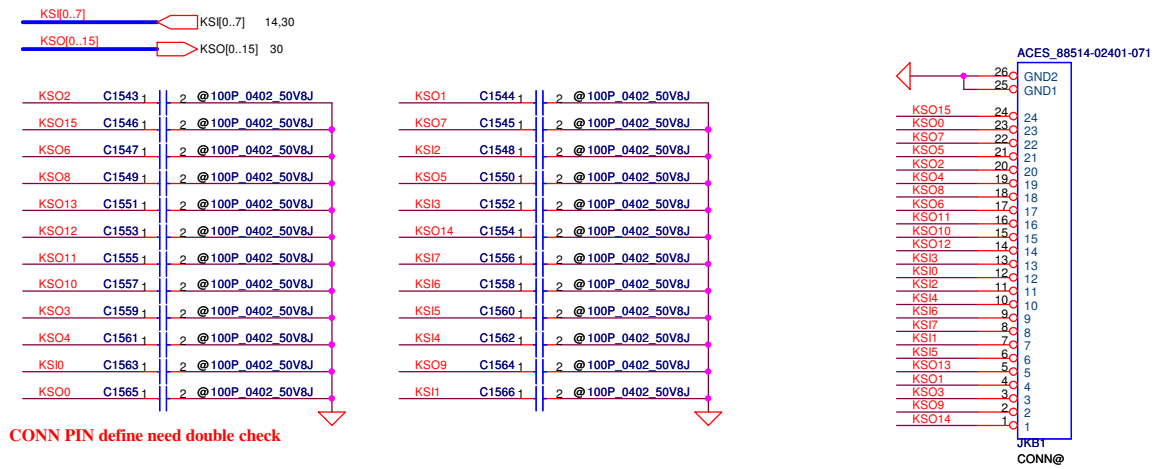


**FOR EC 128KB SPI ROM (150mil PACKAGE) SA00002C100**



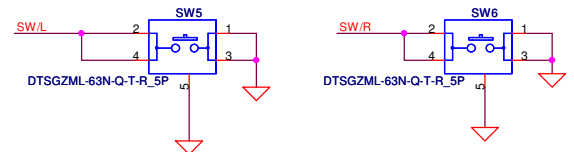
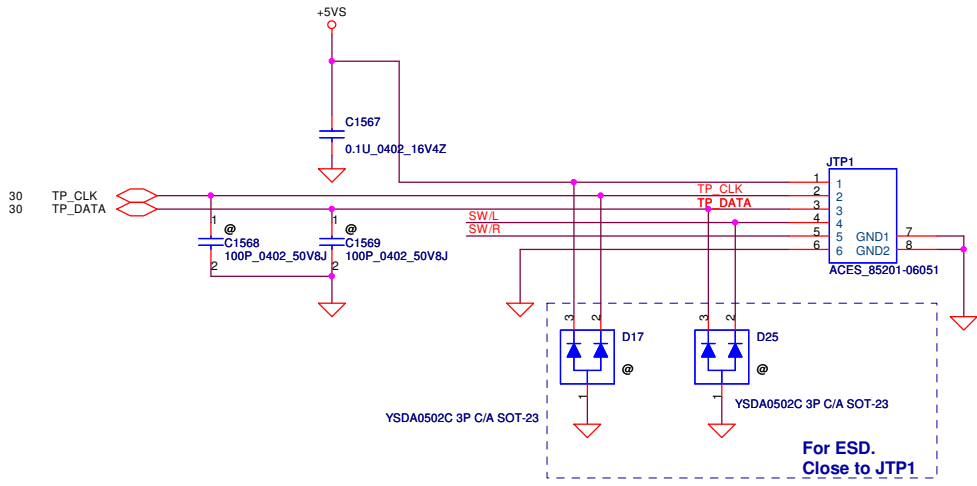
Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/25	Deciphered Date	2011/12/31	P30-BIOS & EC KB930	
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Size	Document Number	Date		Rev	
	LA7321P PBL50	Thursday, February 17, 2011		0.22	
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### INT\_KBD Conn.



CONN PIN define need double check

### To TP/B Conn.

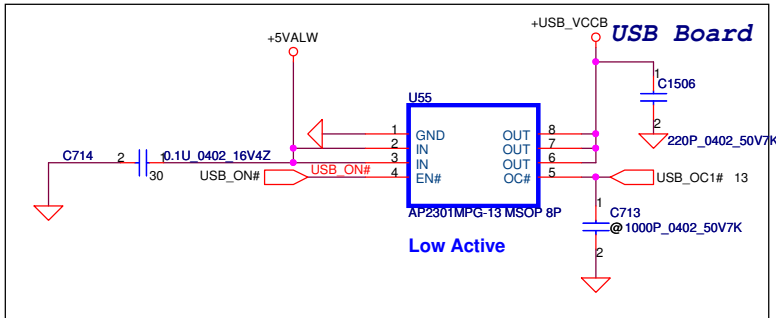
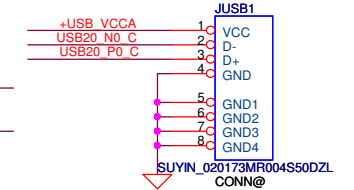
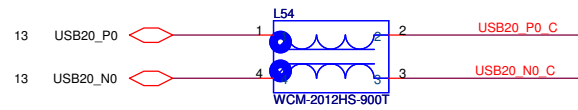
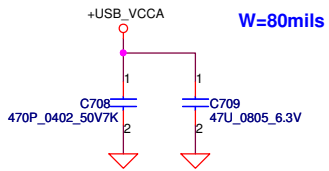
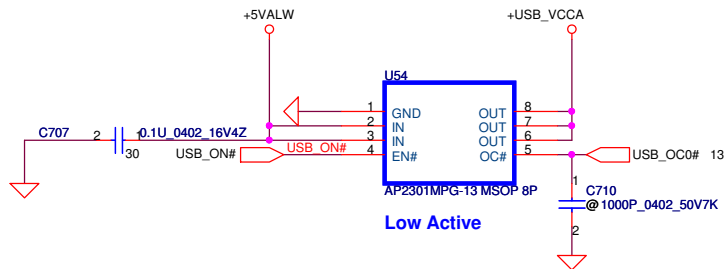


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				B	0.22
				Date:	Sheet
				Tuesday, February 15, 2011	31 of 46

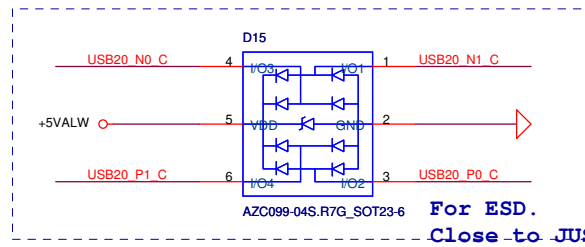
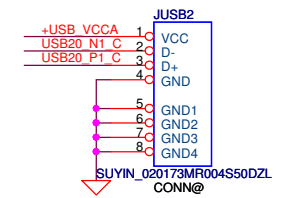
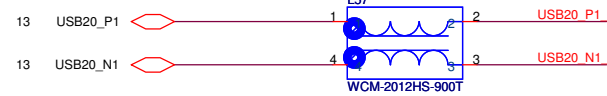
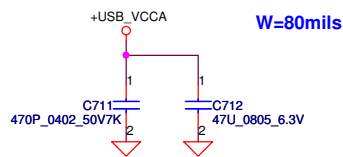
Compal Electronics, Inc.

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### Left USB1 Conn.



### Left USB2 Conn.

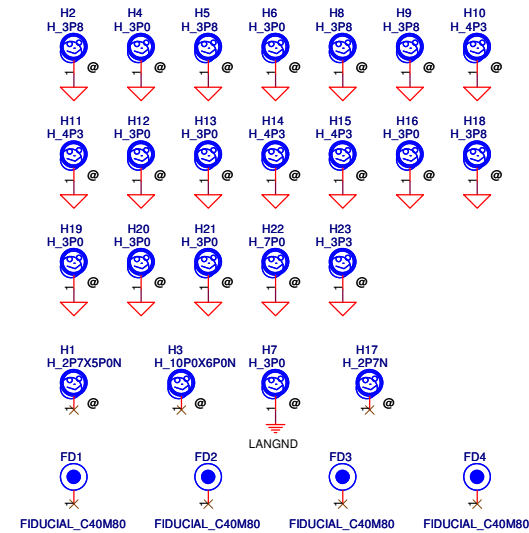
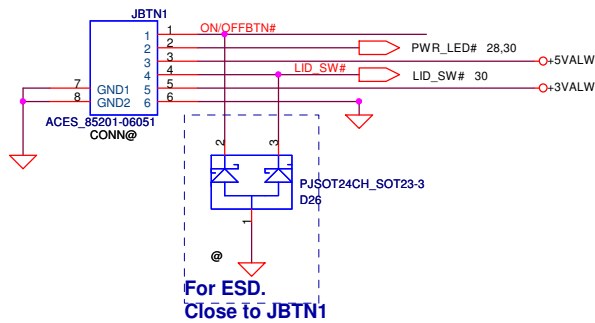
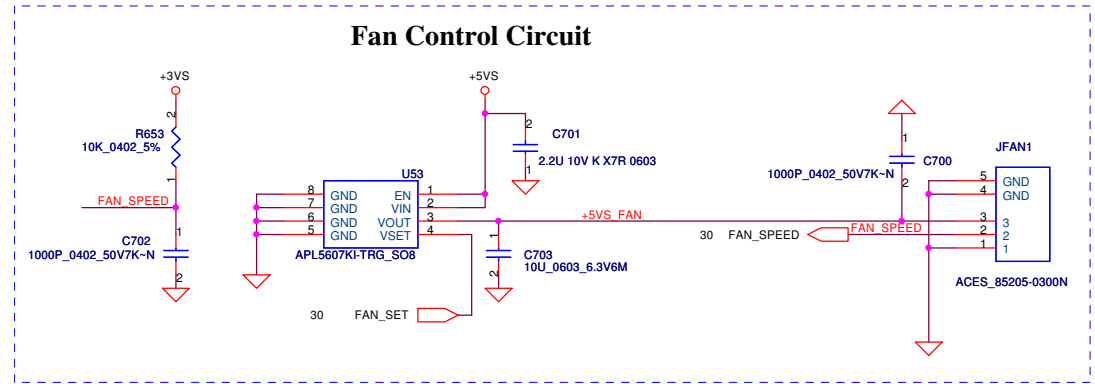
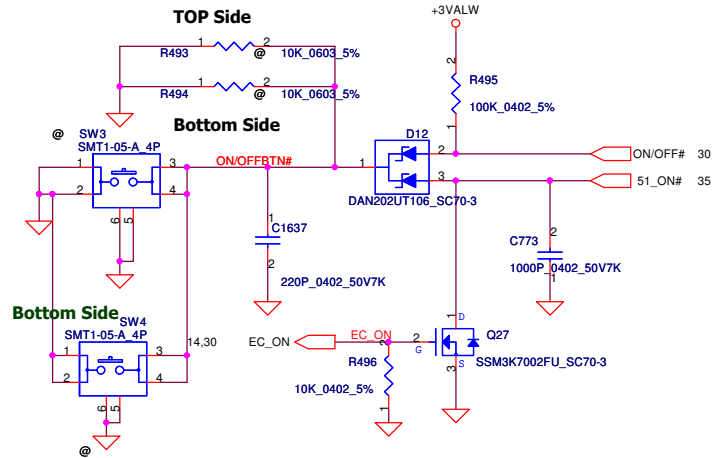


EMI request

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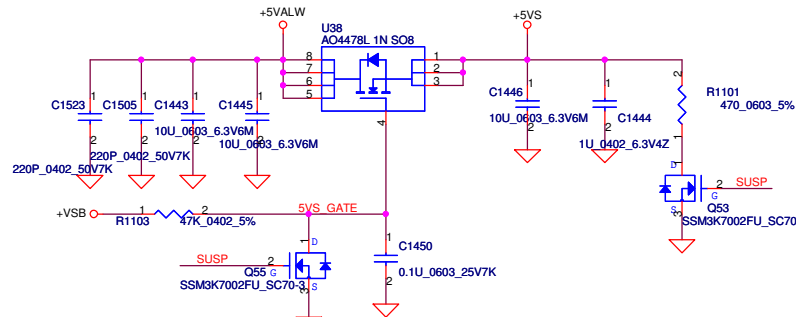


# ON/OFF switch Power Button

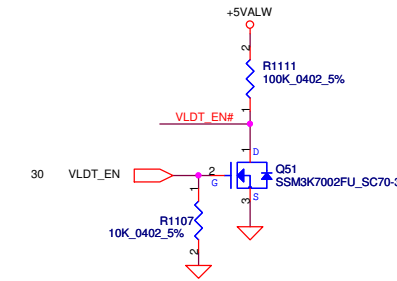
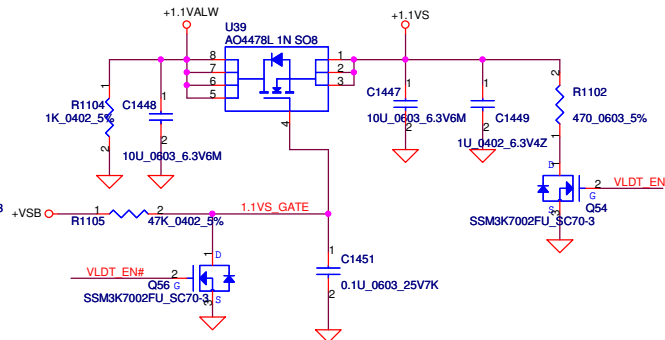


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Issued Date	2010/11/25	Deciphered Date	2011/12/31	P33-Other IO/USB (right)
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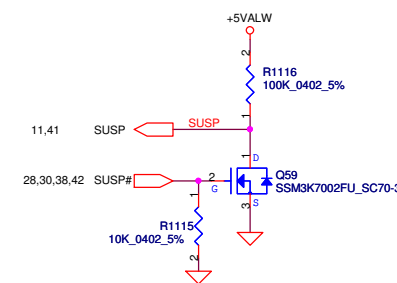
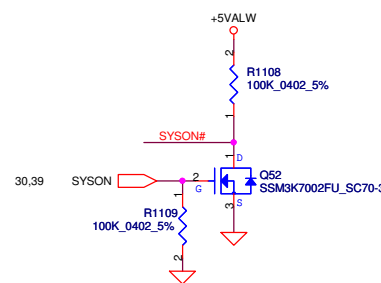
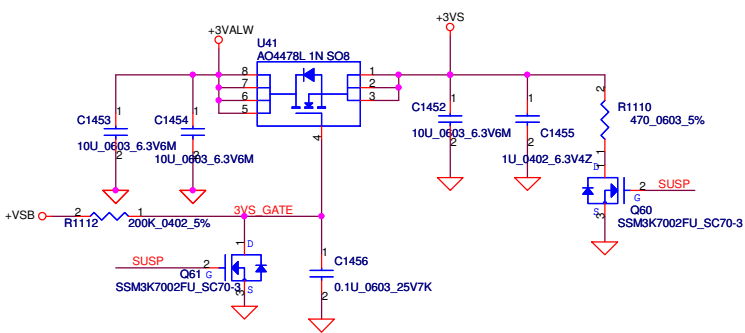
**+5VALW TO +5VS**



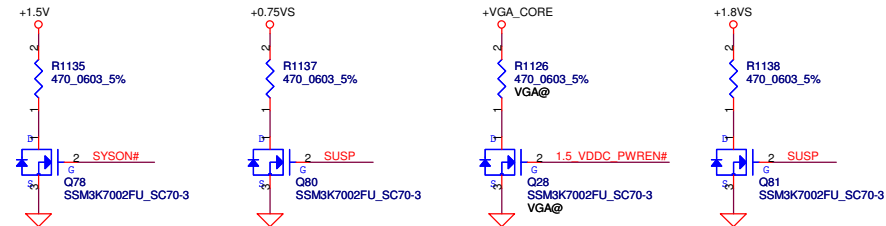
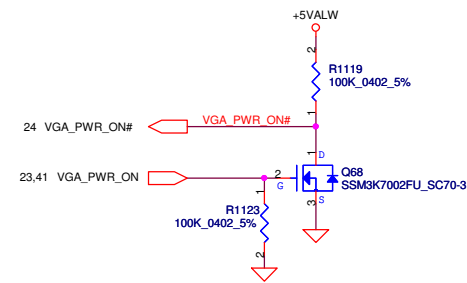
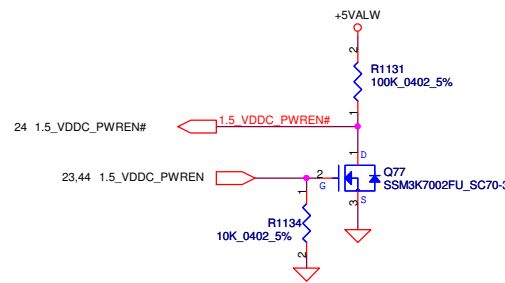
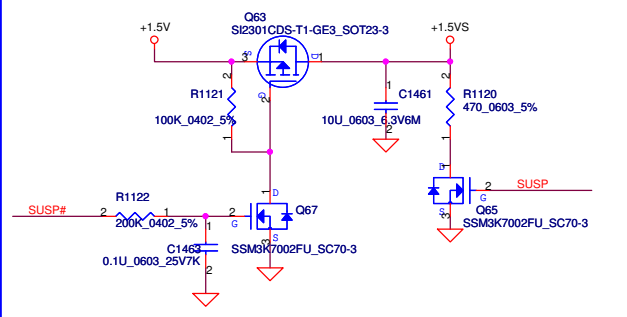
**+1.1VALW TO +1.1VS**



**+3VALW TO +3VS**

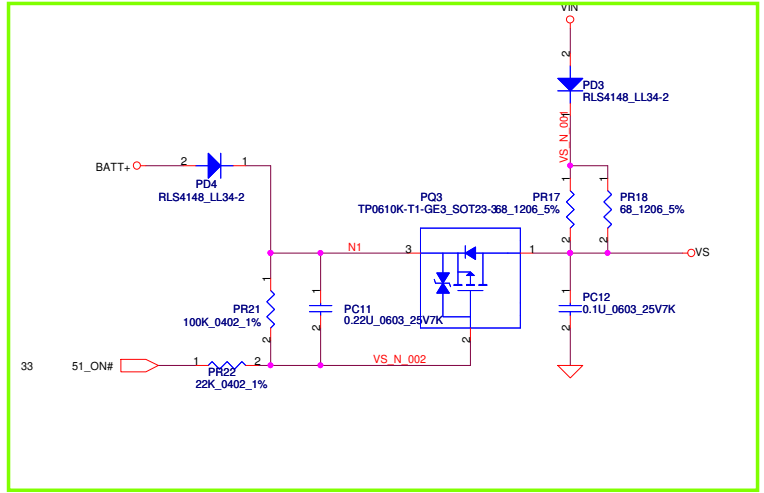
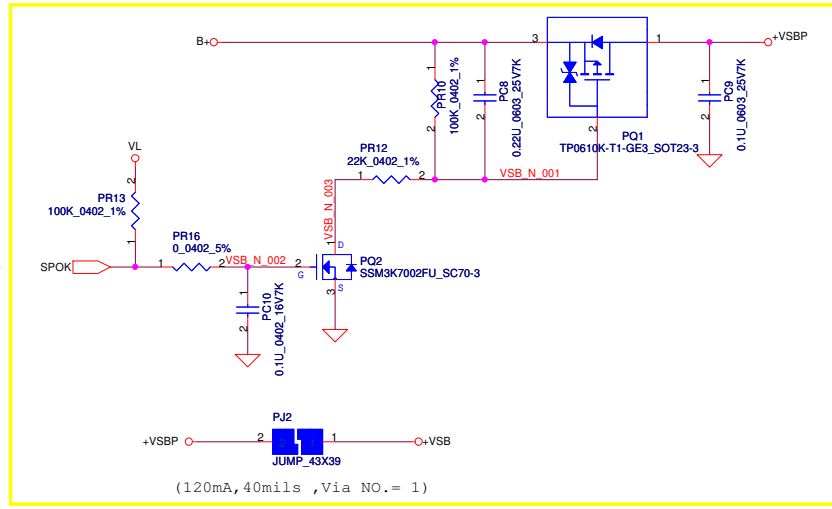
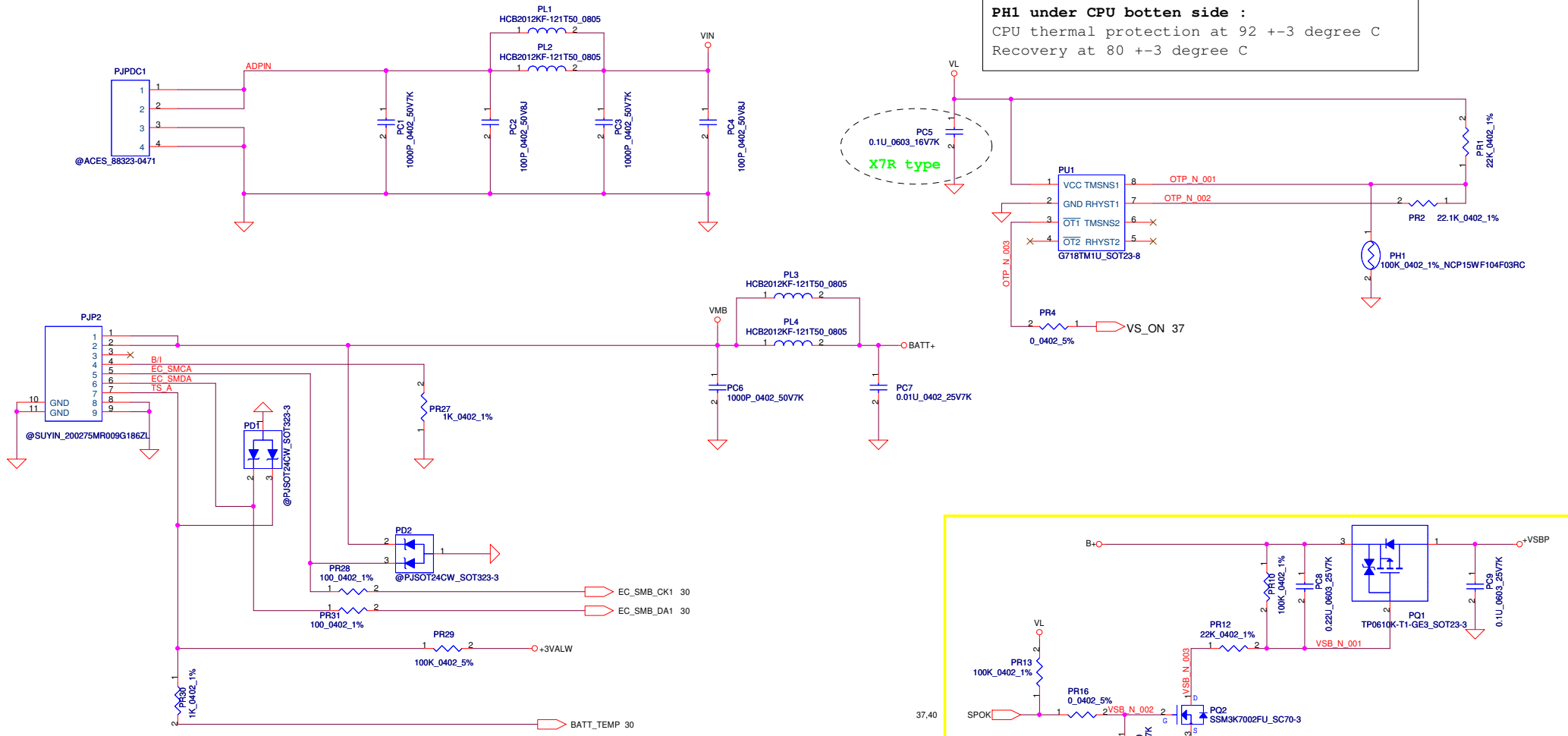


**+1.5VS**

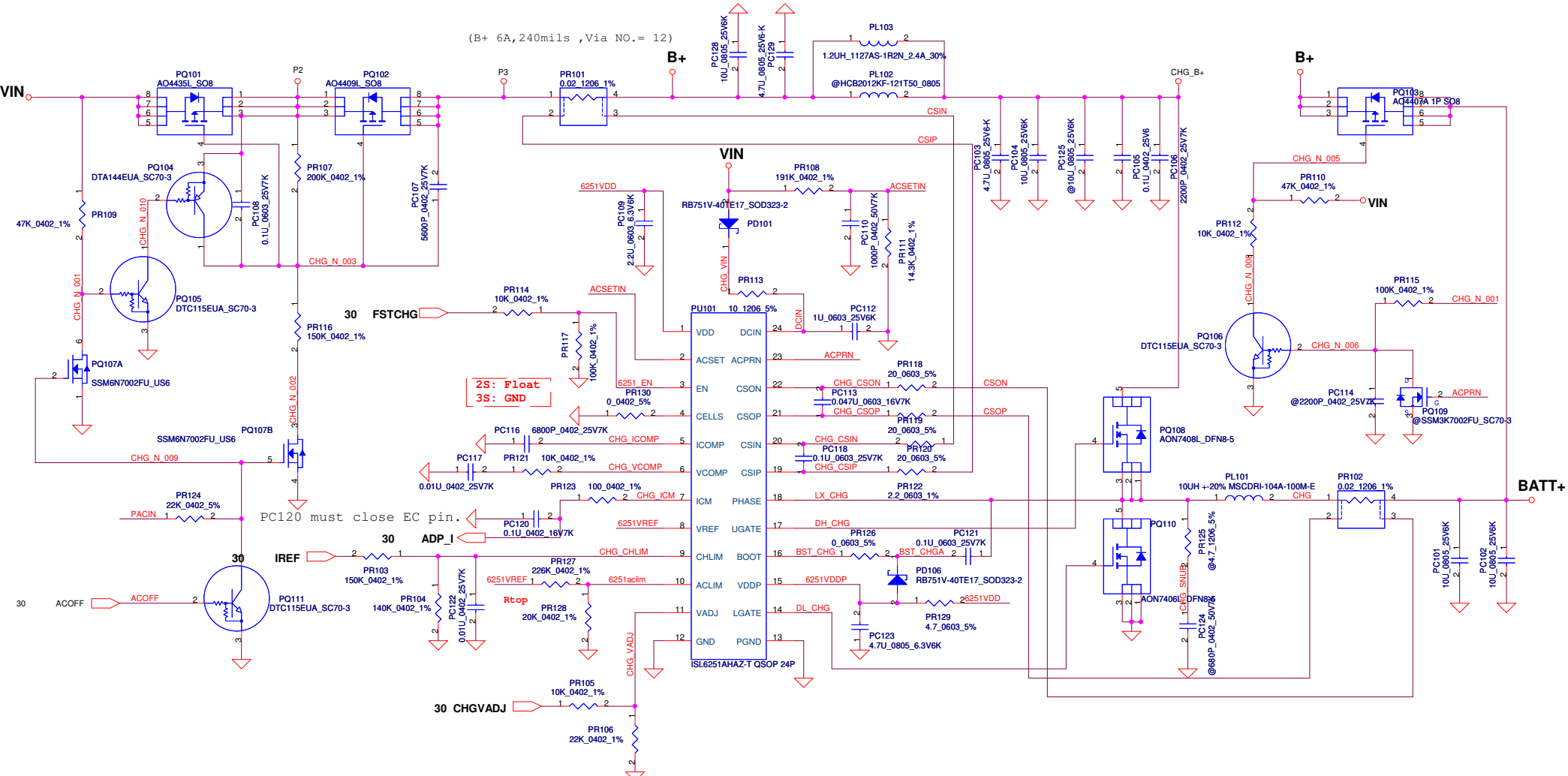


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				P34-DC Interface	
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**PH1 under CPU botten side :**  
 CPU thermal protection at 92 +/-3 degree C  
 Recovery at 80 +/-3 degree C



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(B+ 6A, 240mils, Via NO.= 12)

2S: Float  
3S: GND

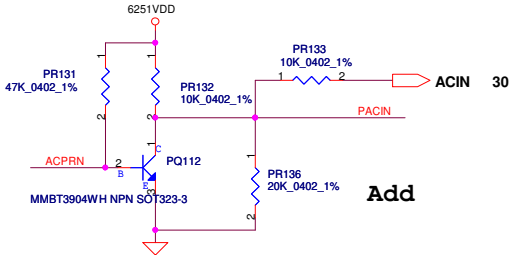
PC120 must close EC pin.

CP= 85%\*I<sub>ada</sub>;  
 I<sub>ada</sub>=0~4.737A (90W); CP=4.03A; where R<sub>acdet</sub>=0.020ohm, where R<sub>top</sub>=12.4K  
 90W for Dis: R<sub>top</sub>:SD00000AJ80  
 I<sub>ada</sub>=0~3.421A (65W); CP=2.91A; where R<sub>acdet</sub>=0.020ohm, where R<sub>top</sub>=226K  
 65W for UMA: R<sub>top</sub>:SD034226380  
 Astro2010\_01\_15 need confirm P/N

CP mode  
 $V_{aclim} = V_{REF} * (R_{bot} / (R_{internal} / (R_{top} / (R_{internal} + R_{bot} / R_{internal})))$   
 when 90W  $V_{aclim} = 2.39 * (20K / (152K / (20K / (152K + 12.4K / 152K))) = 1.44966V$   
 when 65W  $V_{aclim} = 2.39 * (20K / (152K / (20K / (152K + 226K / 152K))) = 0.38914V$   
 $I_{input} = (1 / R_{acdet}) * ((0.05 * V_{aclim} / V_{REF} + 0.05))$   
 when 90W  $I_{input} = (1 / 0.02) * (0.05 * 1.44966 / 2.39 + 0.05) = 4.02A$   
 when 65W  $I_{input} = (1 / 0.02) * (0.05 * 0.38914 / 2.39 + 0.05) = 2.92A$

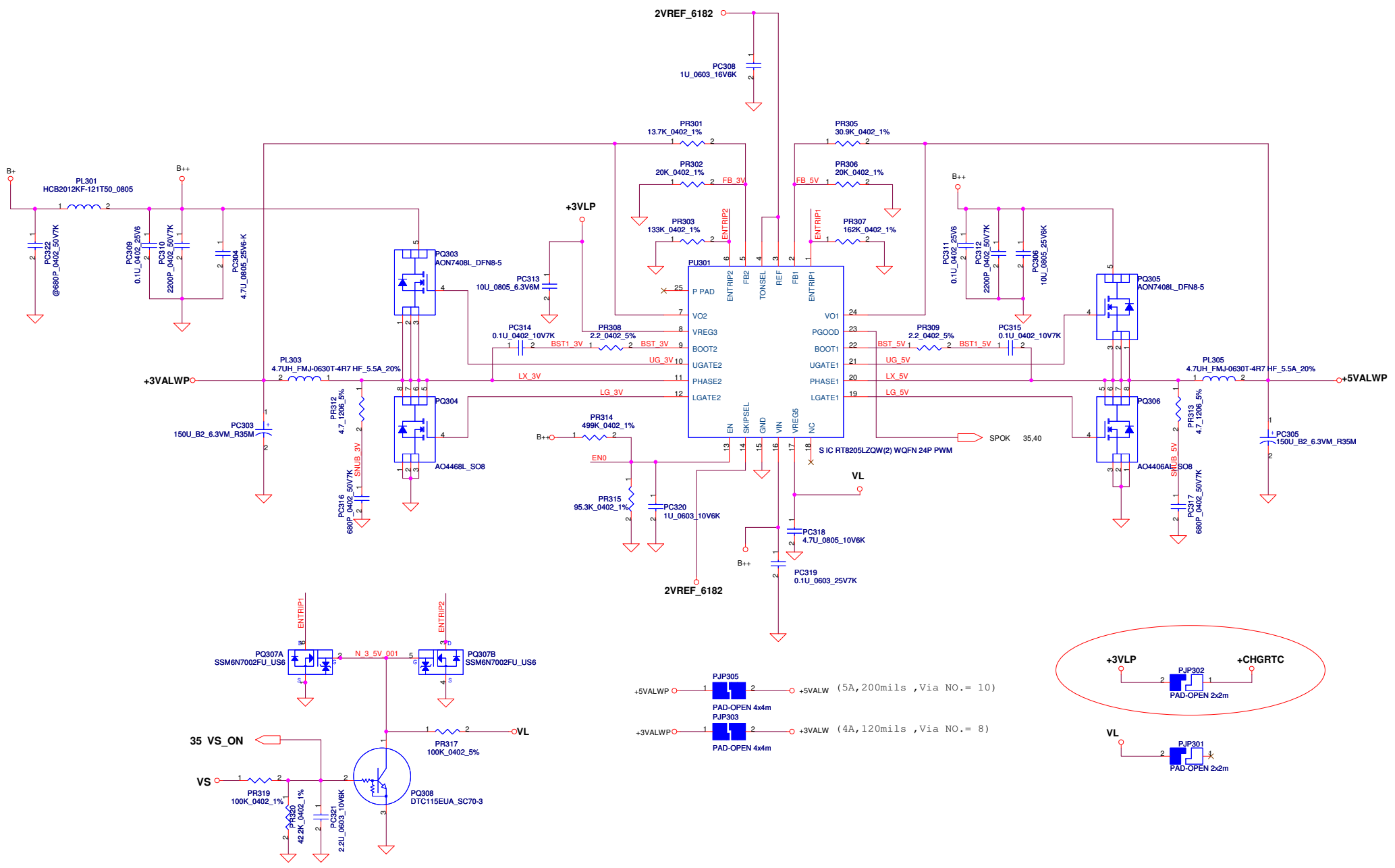
CC=0.25A~3A  
 IREF=1.016\*I<sub>charge</sub>  
 IREF=0.254V~3.048V  
 VCHLIM need over 95mV

CHGVADJ=(V <sub>cell</sub> -4)/0.10627	
V <sub>cell</sub>	CHGVADJ
4V	0V
4.2V	1.882V



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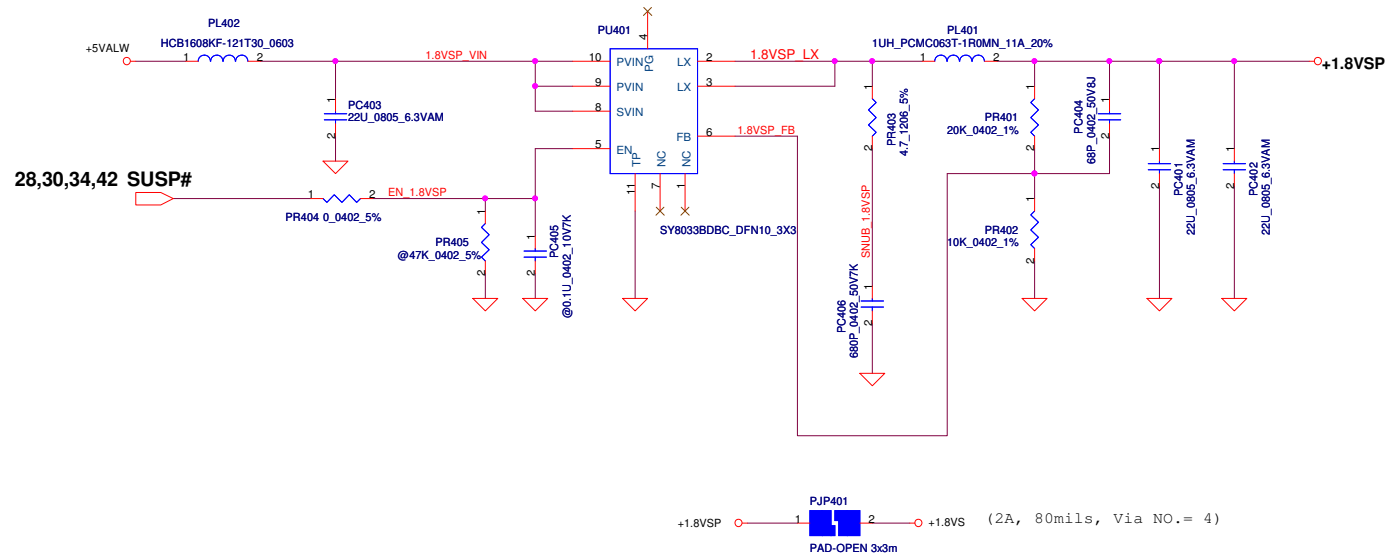
Compal Electronics, Inc.			
Title <b>CHARGER</b>			
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EC:+3VL, reserve PR319, install PR318, PR320 100K  
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

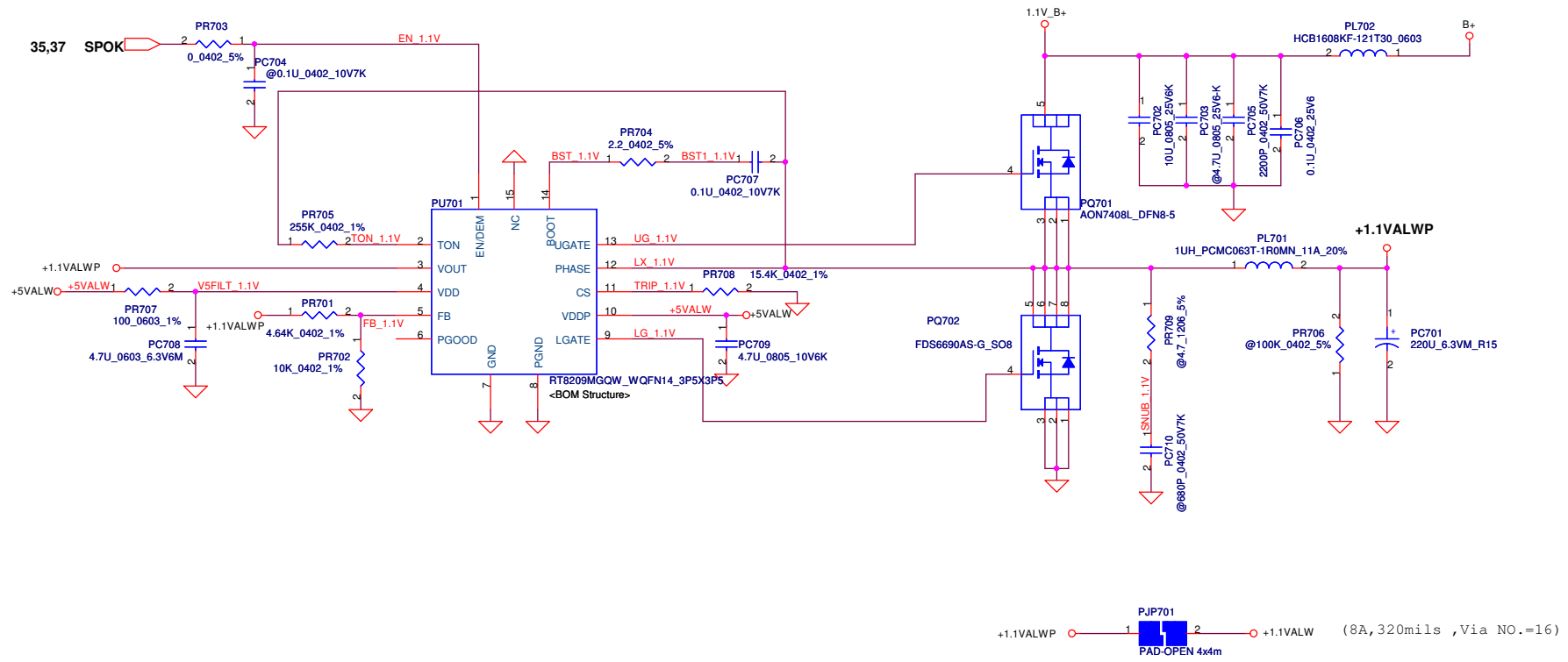
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Issued Date	2007/08/02	Deciphered Date	2008/08/02
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Compal Electronics, Inc.			
<b>3.3VALWP/5VALWP</b>			
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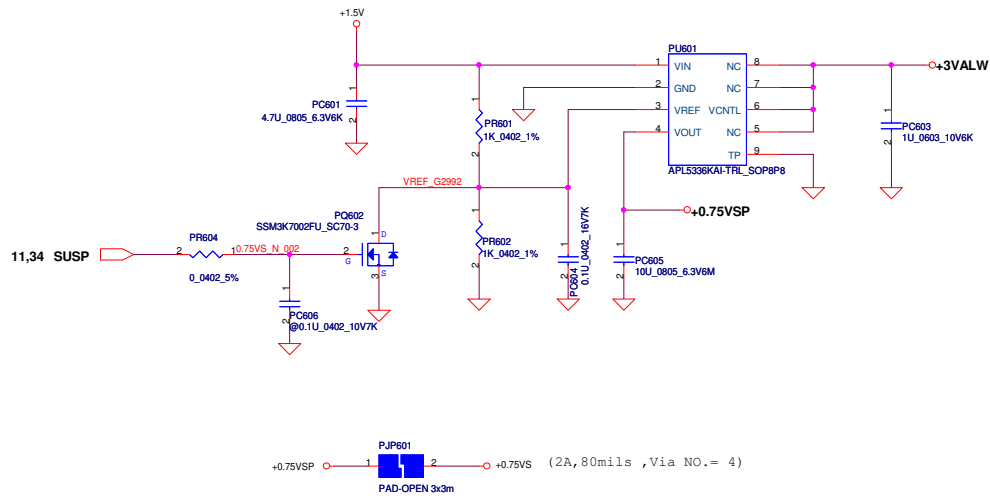
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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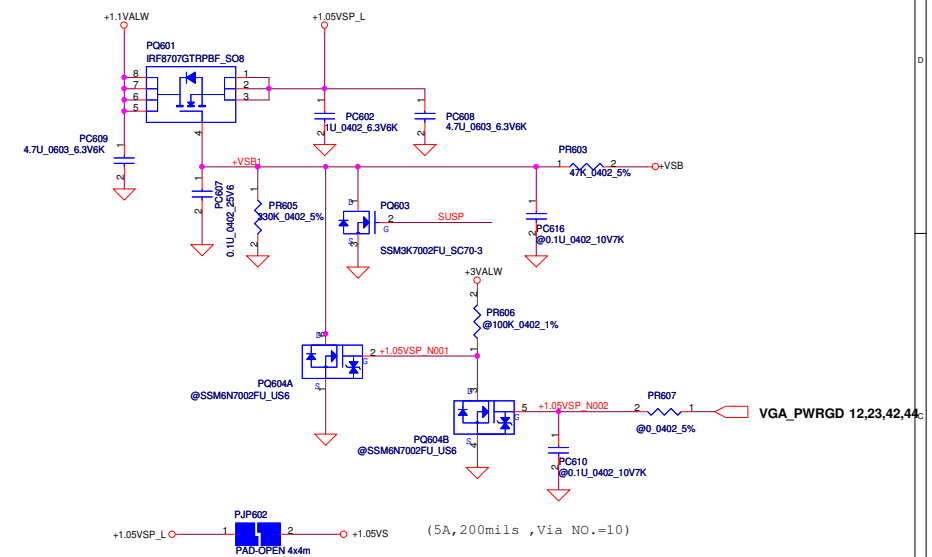
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	<b>PWR+1.1VALWP</b>
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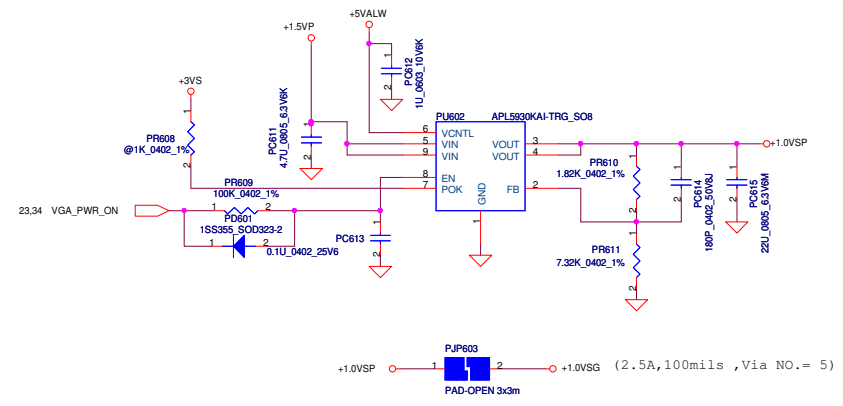
+0.75VSP (2A, 80mils, Via NO. = 4)

**+1.1VALW TO +1.05VSP**



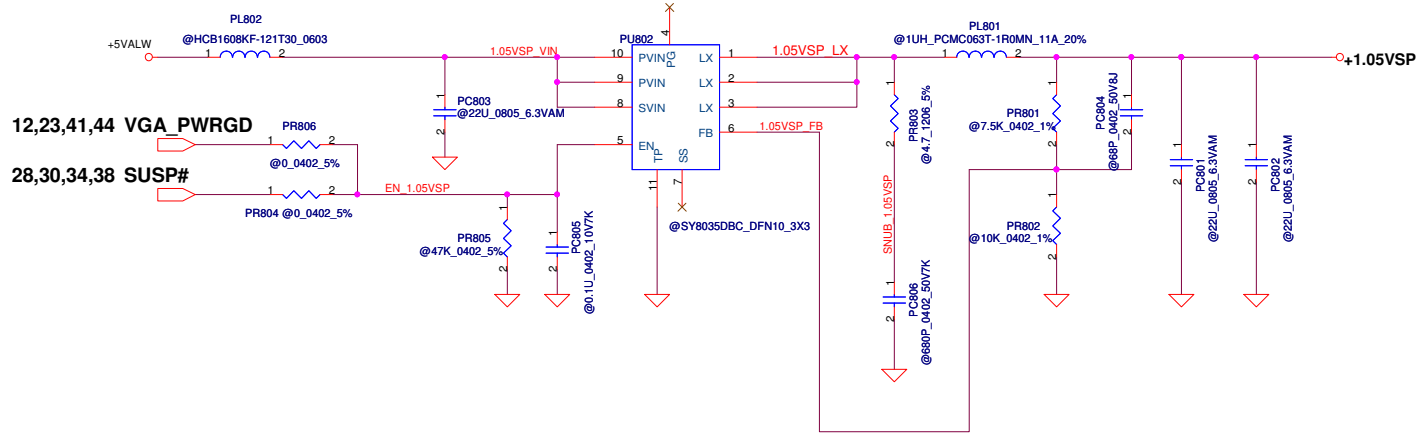
+1.05VSP (5A, 200mils, Via NO.=10)

Need to confirm with HW power sequence.



+1.0VSP (2.5A, 100mils, Via NO. = 5)

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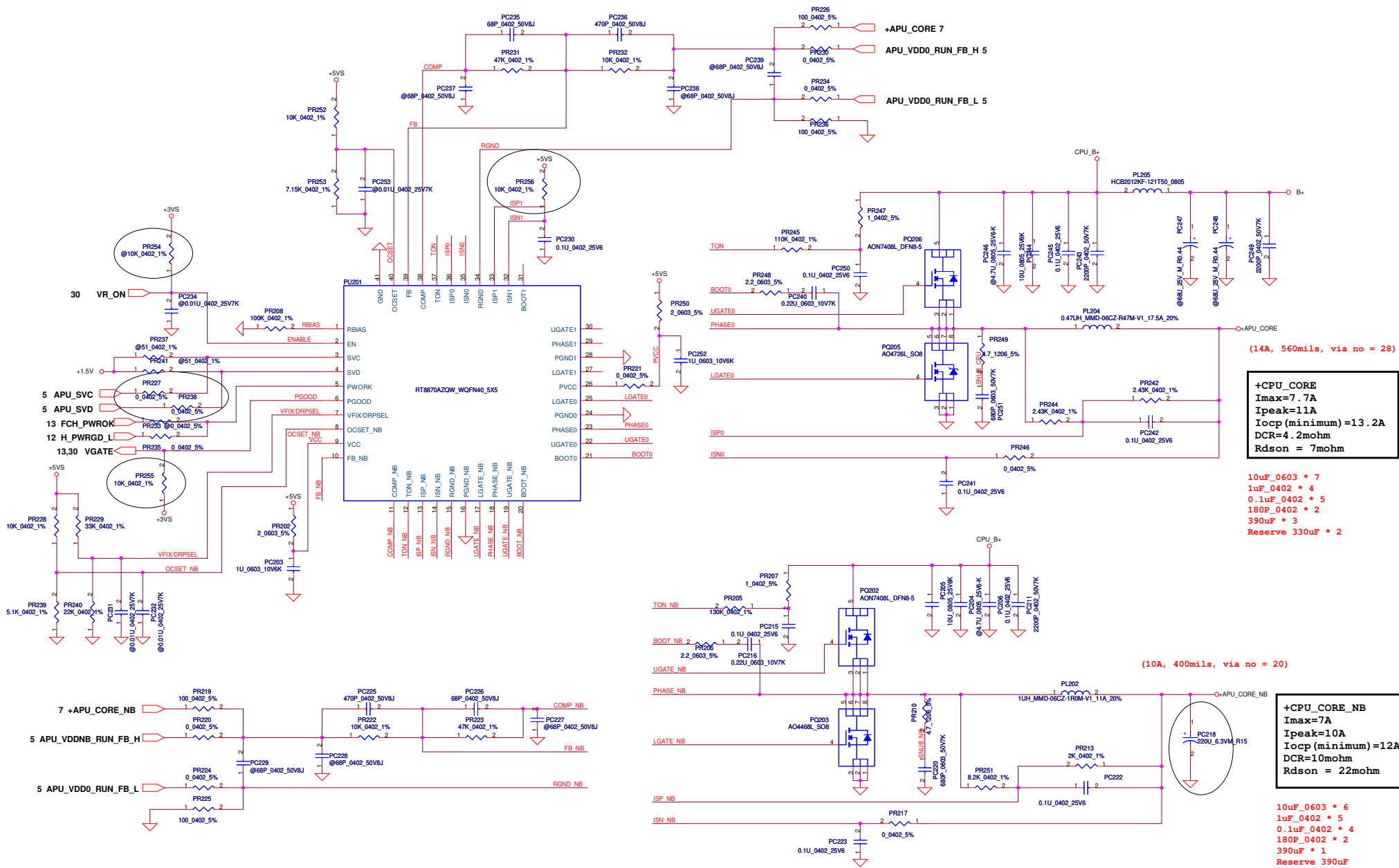


12,23,41,44 VGA\_PWRGD

28,30,34,38 SUSP#



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	NCL61 LA-6321P M/B			0.22	
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(14A, 560mils, via no = 28)

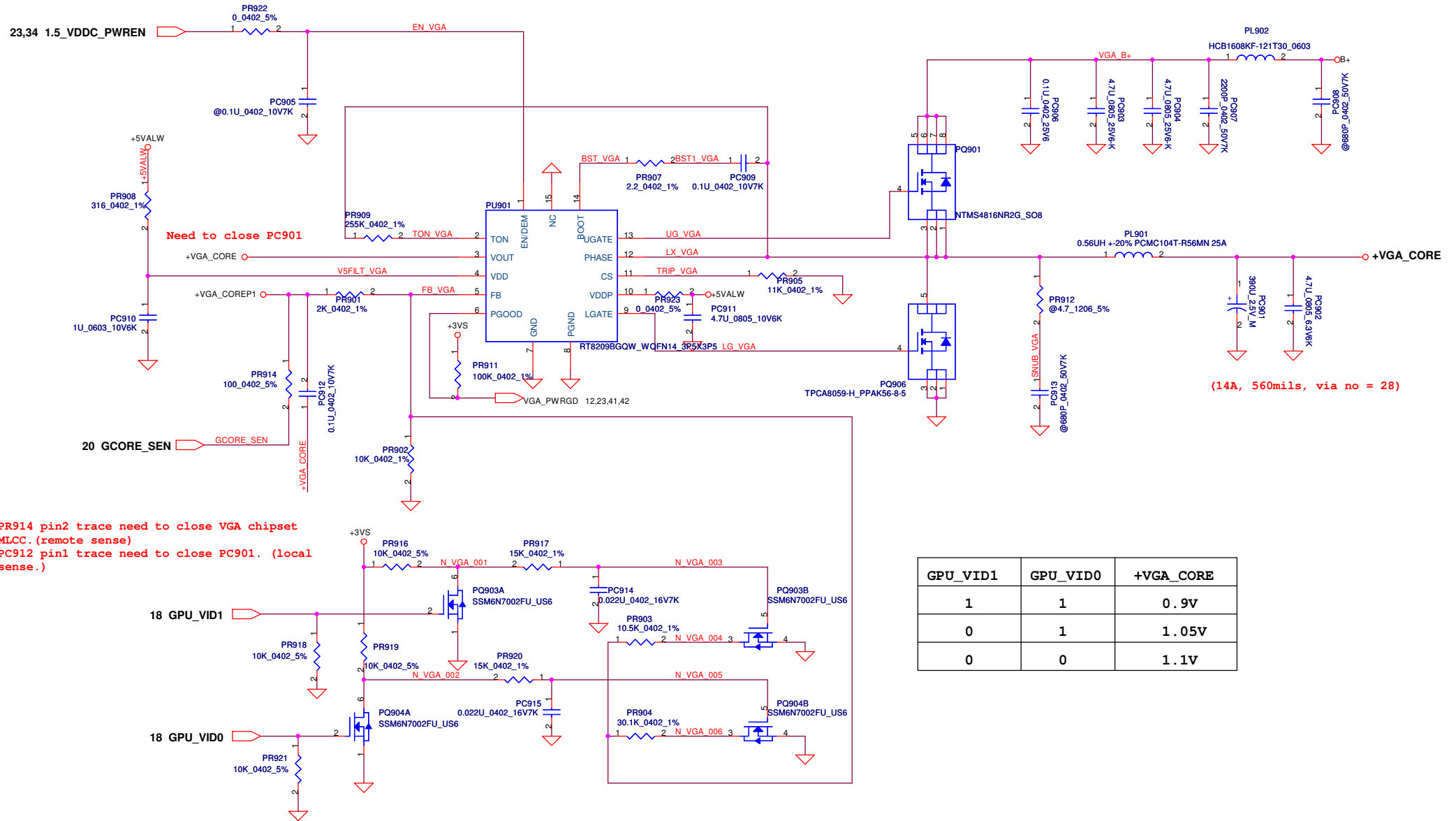
**+CPU\_CORE**  
 I<sub>max</sub>=7.7A  
 I<sub>peak</sub>=11A  
 I<sub>ocp</sub>(minimum)=13.2A  
 DCR=4.2mohm  
 R<sub>dson</sub> = 7mohm

10uF\_0603 \* 7  
 1uF\_0402 \* 4  
 0.1uF\_0402 \* 5  
 180P\_0402 \* 2  
 390uF \* 3  
 Reserve 330uF \* 2

(10A, 400mils, via no = 20)

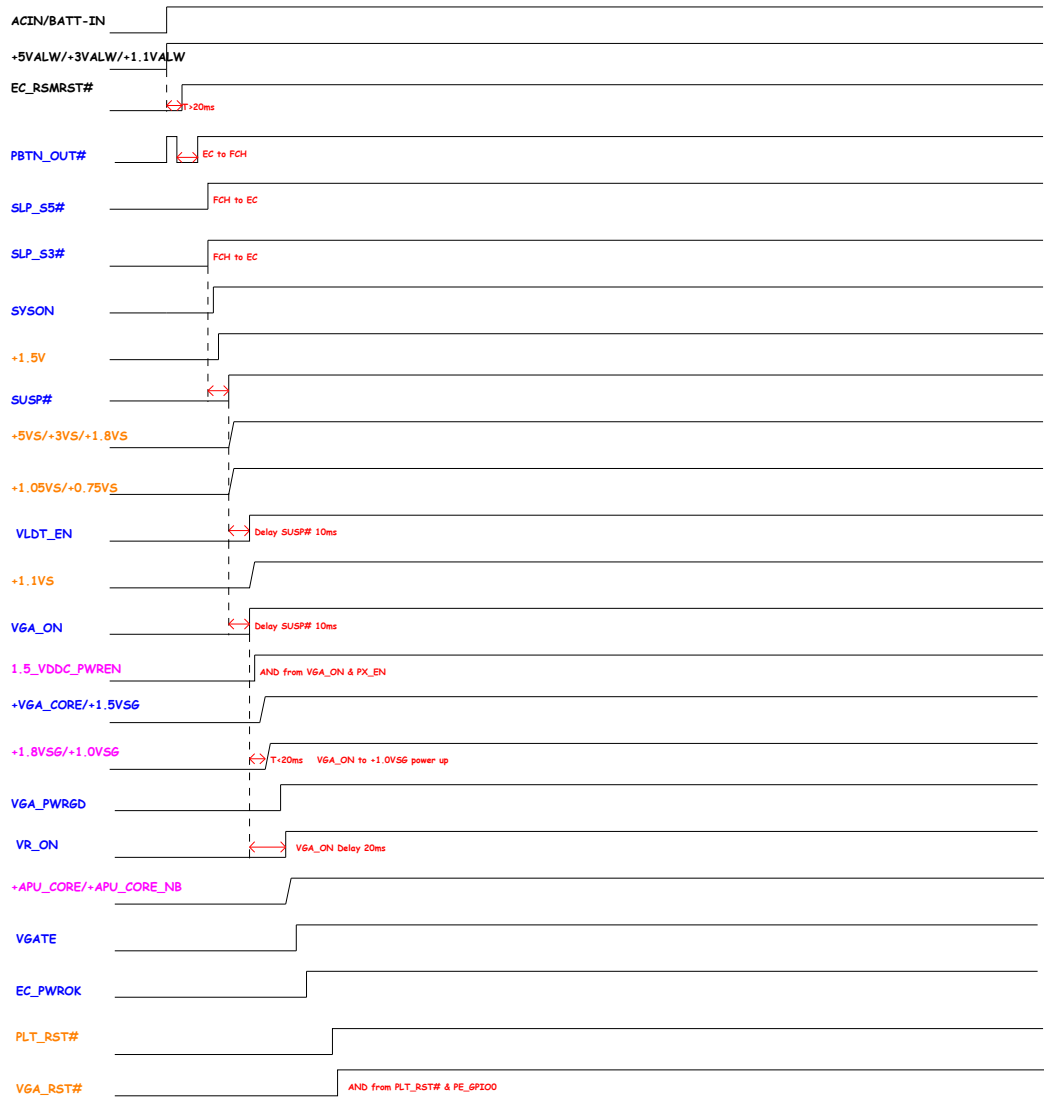
**+CPU\_CORE\_NB**  
 I<sub>max</sub>=7A  
 I<sub>peak</sub>=10A  
 I<sub>ocp</sub>(minimum)=12A  
 DCR=10mohm  
 R<sub>dson</sub> = 22mohm

10uF\_0603 \* 6  
 1uF\_0402 \* 5  
 0.1uF\_0402 \* 4  
 180P\_0402 \* 2  
 390uF \* 1  
 Reserve 390uF



GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

# POWER SEQUENCE



Security Classification		Control Release Date	
Classified	2011/05	Declassified	2019/01
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	F30	KB930	2010/12/16	COMPAL	Power button no function.	Add R1621 pull up to +3VALW.	0.12
2	F31	TP button	2010/12/16	COMPAL	SWS, SW6 footprint error	Modify SWS, SW6 symbol.	0.12
3	F33	Fan Connector	2010/12/16	COMPAL	Fan no function.	Modify Fan connector pin define.	0.12
4	F35 ~ P44	Power schematic update	2010/12/16	COMPAL		Power schematic update	0.12
5	F30	KB930	2010/12/17	COMPAL	Modify board ID for ER phase.	Change R1606 from 0 ohm to 8.2K ohm.	0.12
6	F5	FCH THERMTRIP	2010/12/17	COMPAL	Modify BOM structure of thermtrip circuit. For FCH spec.	Change Q79 and R424 to unpop and change R427 to pop.	0.12
7							
8	F30	KB930	2010/12/17	COMPAL	Vendor's recommend for XCLK0 signal.	Add R1669 and C129.	0.12
9	F14	FCH SPI	2010/12/21	COMPAL	Add U11 circuit for flash BIOS crisis circuit.	Add U11 circuit.	0.12
10	F8	DDR3 80-DIMM1	2010/12/21	COMPAL	Reserve R155, R152 for DDR3 DIMM1. (SA)		0.12
11	F33	Screw hole	2010/12/22	COMPAL	Thermal issue, modify H22.	Modify H22 to 7.0.	0.13
12	F35 ~ P44	Power schematic update	2010/12/22	COMPAL		Power schematic update	0.13
13	F12	FCH RTC	2010/12/23	COMPAL	Customer requirement for clear CMOS	Change R865 to Jump.	0.13
14	F28	WLAN & LED	2010/12/23	COMPAL	For ESD solution on LED.	Add C1644-C1648.	0.13
15	F26	Audio Codec	2010/12/24	COMPAL	For EMI solution on DMIC CLK.	Change R1544 to L124.	0.13
16	F30	KB930	2010/12/24	COMPAL	For EMI solution on SPI CLK.	Change R1631 to L125 and pop R180 and C1535.	0.13
17	F14	FCH SPI	2010/12/24	COMPAL		Modify Crisis circuit.	0.13
18	F10	CRT	2010/12/24	COMPAL	For ESD solution on CRT.	Pop D1, D2, D16, D18	0.13
19	F35 ~ P44	Power schematic update	2010/12/24	COMPAL		Power schematic update	0.13
20	F25	LAN	2010/12/24	COMPAL		Reserve J1 jump for LAN power.	0.13
21	F14	FCH SPI	2010/12/25	COMPAL	For EMI requirement.	Reserve R181, C130 close to U32.	0.13
22	F25	LAN	2010/12/27	COMPAL	For LAN power discharge.	Add R1113, Q62.	0.13
23	F25	LAN	2010/12/27	COMPAL	Prevent LAN wake up signal fo floating.	Add R553 pull down to GND.	0.13
24	F25	LAN	2010/12/27	COMPAL	For ESD requirement.	Change R549, R1529, R1530, R552 to 0603 size.	0.13
25	F34	DC to DC	2010/12/27	COMPAL	For Power sequence.	Change R1103 from 100K to 47K.	0.13
26	F11	HDMI	2010/12/28	COMPAL	For EMI requirement.	Modify L11-L14 circuit and remove un-LS circuit.	0.13
27	F12, 18, 25	Crystal	2010/12/29	COMPAL	For Vendor recommend.	Modify C35, C66, C67, C1633, C1634.	0.2
28	F26	Audio Codec	2010/12/30	COMPAL	For EMI Requirement.	Unpop R1556, R1557, R1558, R1559.	0.2
29	F30	KB930	2010/12/31	COMPAL	Change ROM footprint.	Change U48 footprint.	0.2
30	F16	FCH Strap	2010/12/31	COMPAL	Change FCH Strap for SPI-ROM	Pop R594, R602; Unpop R601, R550.	0.2
31	F18	Seymour Strap	2011/01/10	COMPAL	For AMD requirement.	Unpop R21, R22.	0.21
32	F34	DC to DC	2011/01/11	COMPAL	For +1.8VS discharge issue.	Add Q81, R1138.	0.21
33	F13	FCH HDA/USB/ACPI	2011/02/11	COMPAL	For RSMRST pluse issue	Change R606 from 2.2k ohm to 150 ohm	0.22
34	F30	EC	2011/02/11	COMPAL	For MB Board ID	Change R1606 to 18K	0.22
35	F10	CRT	2011/02/11	COMPAL	For CRT EA AND EMI	Change L116, L117, L118 TO 80 ohm	0.22
36	F25	LAN	2011/02/11	COMPAL	For EMI request	Change D36, D37, D38, D39 footprint	0.22
37	F18	VGA	2011/02/15	COMPAL	For S3 can't resume issue	ADD R74 (1M ohm) on Y1's cap	0.22
38	F25	LAN	2011/02/15	COMPAL	Follow vendor recommend to change Crystal's cap value	Change C1633 to 15P, C1634 to 12P	0.22
39	F30	EC	2011/02/16	COMPAL	For EMI requirement	Change R180 to 39 ohm, C1535 to 33P	0.23
40	F25	LAN	2011/02/16	COMPAL	For EMI requirement	Change T81 to IH-160	0.23
41	F26	AUDIO	2011/02/17	COMPAL	For EMI requirement	Change R1556, R1557, R1558, R1559 to 0.1u caps	0.23
42	F34	DC-DC	2011/02/17	COMPAL	For EMI requirement	ADD C1505, C1523 on +5VALW	0.23
43	F32	USB	2011/02/17	COMPAL	For EMI requirement	ADD C1506 on +USB_VCCB	0.23
44	F33	PHRBTN	2011/02/17	COMPAL	For EMI requirement	ADD C1603 on ON/OFFBTN#	0.23
45	F25	LAN	2011/02/18	COMPAL	For EMI requirement	Stuff R546, R548	0.23
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Issued Date	2010/11/25	Deciphered Date	2011/12/31	Title	EE-PIR-1
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