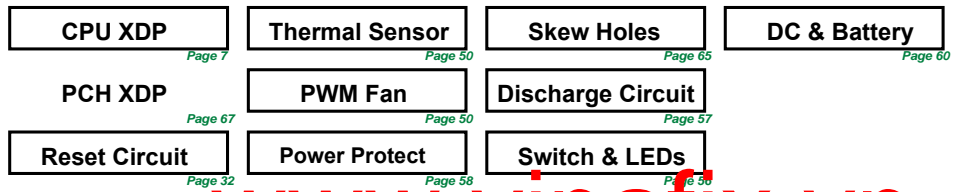
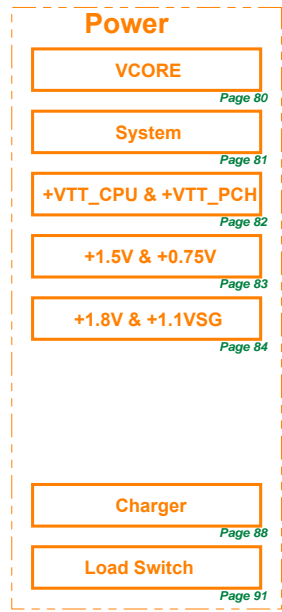
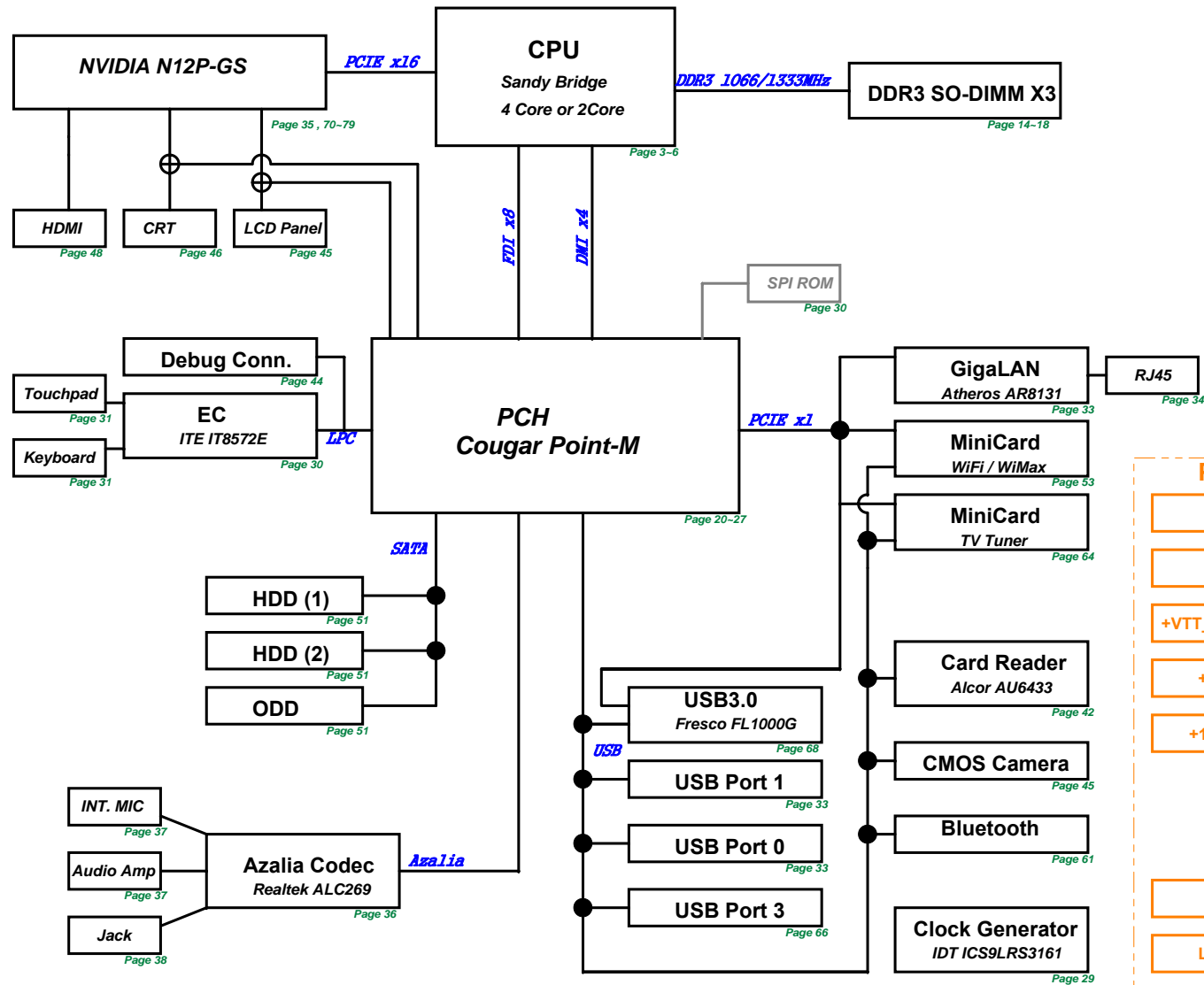


N73Sv Block Diagram

01. Block Diagram
02. System Setting
03. CPU_DMI, PEG, FDI, CLK, MISC
04. CPU_DDR3
05. CPU_CFG, RSVD, GND
06. CPU_PWR
07. CPU_XDP
14. DIM_DDR3 SO-DIMM 0 (for CFD)
16. DIM_DDR3 SO-DIMM 1
17. DIM_DDR3 SO-DIMM 3
18. DIM_CA/DQ Voltage
19. CPU_VID Controller
20. SB_Cougar SATA, HDA, RTC, LPC
21. SB_Cougar PCIE, CLK, SMB, PEG
22. SB_Cougar FDI, DMI, SYS_PWR
23. SB_Cougar DP, LVDS, CRT
24. SB_Cougar PCI, NVRAM, USB
25. SB_Cougar CPU, GPIO, MISC
26. SB_Cougar PWR, GND
27. SB_Cougar PWR, GND
28. SB_SPI ROM, SMBus
29. CLK_ICS9LRS3161
30. KBC_IT8572E
31. KBC_KB & TP
32. RST_Reset Circuit
33. LAN_AR8131
34. LAN_RJ45 Conn.
35. Hybrid switch
36. AUD_CODEEC ALC269
37. AUO_SPKR, Woofer, Mic
38. MIC & LINE IN
42. CB_AU6433
44. BUG_NewCard & LPC
45. CRT_LVDS & CMOS
46. CRT_D-Sub
48. CRT_HDMI
49. TV_TUNE
50. FAN_Thermal Sensor & Fan
51. XDD_HDD & ODD CON.
52. USB_USB Port
53. PCI_WiFi/WiMax
56. LED_LED & Switch
57. DSG_Discharge
58. PRO_Protect
60. DC_DC & BAT IN
61. BT_Bluetooth
64. TUN_TV Tuner
65. ME_W2B conn. & NUT
66. USB_USB Port
68. USB3.0_FRESCO
69. USB3.0 Port
70. VGA_N11P-GS Main (1)
71. VGA_N11P-GS Main (2)
72. VGA_N11P-GS VRAM CH_A
73. VGA_N11P-GS VRAM CH_C
74. VGA_N11P-GS Main (5)
75. VGA_N11P-GS Main (6)
76. VGA_N11P-GS Main (7)
77. VGA_N11P-GS Main (7)
78. VGA_SG Display Switch
79. VGA_SG PWR Switch
80. PWR_VCORE(NCP3218)
81. PWR_SYSTEM(RT8206A)
82. PWR_I/O_VCCP_PCH(RT8202A)
83. PWR_I/O_DDR(RT8202A+uP7711)
84. PWR_+1.8V_+1.1V(RT8015+LDO)
85. PWR_VGA_CORE(RT8202A)
86. PWR_RENDER_CORE(RT8152D)
88. PWR_CHARGER(MB39A132)
91. PWR_LOAD SWITCH
93. PWR_SIGNAL
94. PWR_Flowchart
95. Revision History



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PCH GPIO

PCH_IBEX GPIO	Use As	Signal Name	Int. & Ext Pull up / down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPI	NC_TP	EXT PU	+3VS
GPIO 07	GPI	USB3_SMI#	EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	INT PD	+3VSUS
GPIO 14	Native	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1_TV#	EXT PD	+3VS
GPIO 19	GPI	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2_WLAN#	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	-	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3_NEWCARD#	EXT PD	+3VSUS
GPIO 26	GPI	CLKREQ4_USB3#	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	-	+3VSUS
GPIO 29	Native		-	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT_PCH	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPI	SATA_CLK_REQ#_R	EXT PD	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PD	+3VS
GPIO 37	GPI	DGPU_PRSENT#	EXT PD	+3VS
GPIO 38	GPI	PCB_ID0	EXT PU / PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PU / PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	-	+3VSUS
GPIO 46	Native	NC_TP	-	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	DGPU_PWM_SELECT#_R	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PD	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU (Diode)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML1ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	GPO	EDID_SELECT#	INT TBD	+3VS
GPIO 67	Native	CLK_CR48	INT TBD	+3VS
GPIO 72	GPO	PM_BATLOW#	INT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC IT8572 GPIO

EC GPIO	Use As	Signal Name
GPA0	OD	PWR_LED#
GPA1	OD	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3	O	MUTE_LED#
GPA4	ALT	LCD_BL_PWM
GPA5	ALT	FAN_PWM
GPA6	ALT	VOLUME_LED#
GPA7	O	MEDIA_KEY_LED#
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT
GPB3	ALT	SMB0_CLK
GPB4	ALT	SMB0_DAT
GPB5	OD	A20GATE
GPB6	OD	RC_IN#
GPB7	O	PM_RSMRST#
GPC0		CLK_UC
GPC1	ALT	SMB1_CLK
GPC2	ALT	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	ALT	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	ALT	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	ALT	BUF_PLT_RST#
GPD3	OD	EXT_SCI#
GPD4	OD	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	ALT	FANO_TACH
GPD7	OD	EXP_GATE_LED#
GPE0	O	-
GPE1	I / PU	-
GPE2	I / PU	-
GPE3		-
GPE4	ALT	PWR_SW#
GPE5	ALT	CLK_OC#
GPE6	I	LID_SW#
GPE7	I	EXP_GATE#
GPF0	ALT	OS_LED#
GPF1	O	VSUS_ON
GPF2	I	VCCP_DV0
GPF3	I	VCCP_DV1
GPF4	ALT	TP_CLK
GPF5	ALT	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
PGP0	I	ME_SusPwrDnAck
PGP1	I	PM_SUSB#
PGP2		CLK_STRAP0
PGP6		CLK_STRAP1
GPH0	ALT	PM_CLKRUN#
GPH1		GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	OD	NUM_LED#
GPH6	OD	CAP_LED#
GPI0		HDMI_HPD
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5		-
GPI6		IDLE_HPD_INT#
GPI7		-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	ALT	VSET_EC
GPJ3	ALT	ISET_EC
GPJ4		CPU_DV0
GPJ5		CPU_DV1

Design IP Source: N73JF

SM BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
Clock Generator(ICS9LRS3197)	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
VID Controller(ASM8272)	0011011x (36)
EC Master (SMB1)	
SM-Bus Device	SM-Bus Address
CPU Thermal Sensor(G781)	1001100x (9A)
VGA Thermal IC(G781-1)	1001101x (9E)

PCI Express

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	USB 3.0
PCIE 5	Card Reader
PCIE 6	GLAN
PCIE 7	
PCIE 8	

USB Port

USB 0	USB Port 0
USB 1	USB Port 1
USB 2	USB Port 2
USB 3	USB Port 3
USB 4	Minicard TV Tuner
USB 5	NewCard
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	

SATA Port

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

Device Identification

CPU Thermal Sensor		
1st	06G023048011	G781F
2nd		

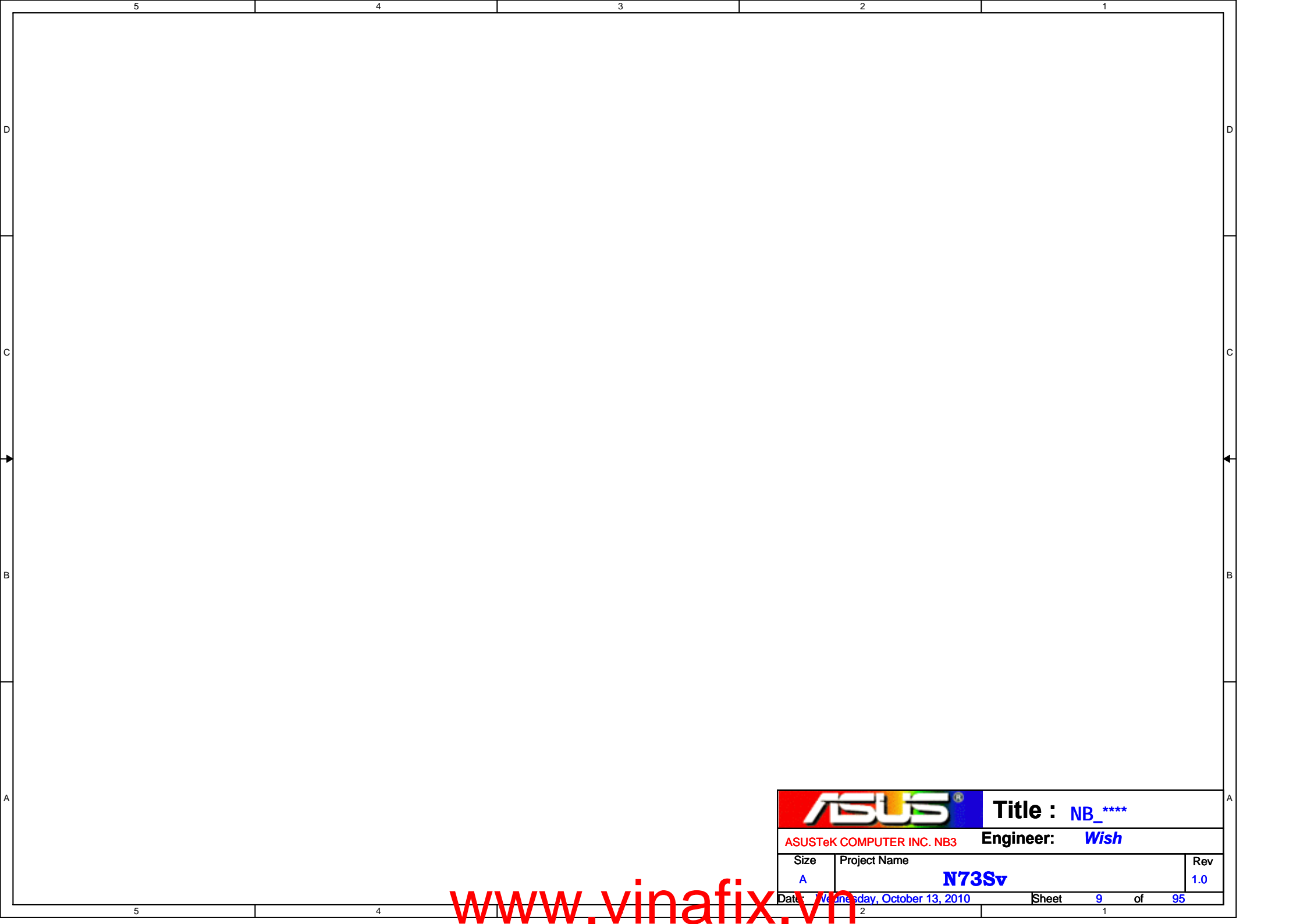
VGA Thermal Sensor		
1st	06G023048010	G781-1
2nd		

Clock Gen		
1st	06G011614010	ICS9LVS3161
2nd		

		Title : System Setting
ASUSTeK COMPUTER INC. NBS		Engineer: <i>Wish</i>
Size	Project Name	Rev
C	N73Sv	1.0
Date: Wednesday, October 13, 2010	Sheet	2 of 95

		Title : NB_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	8 of 95

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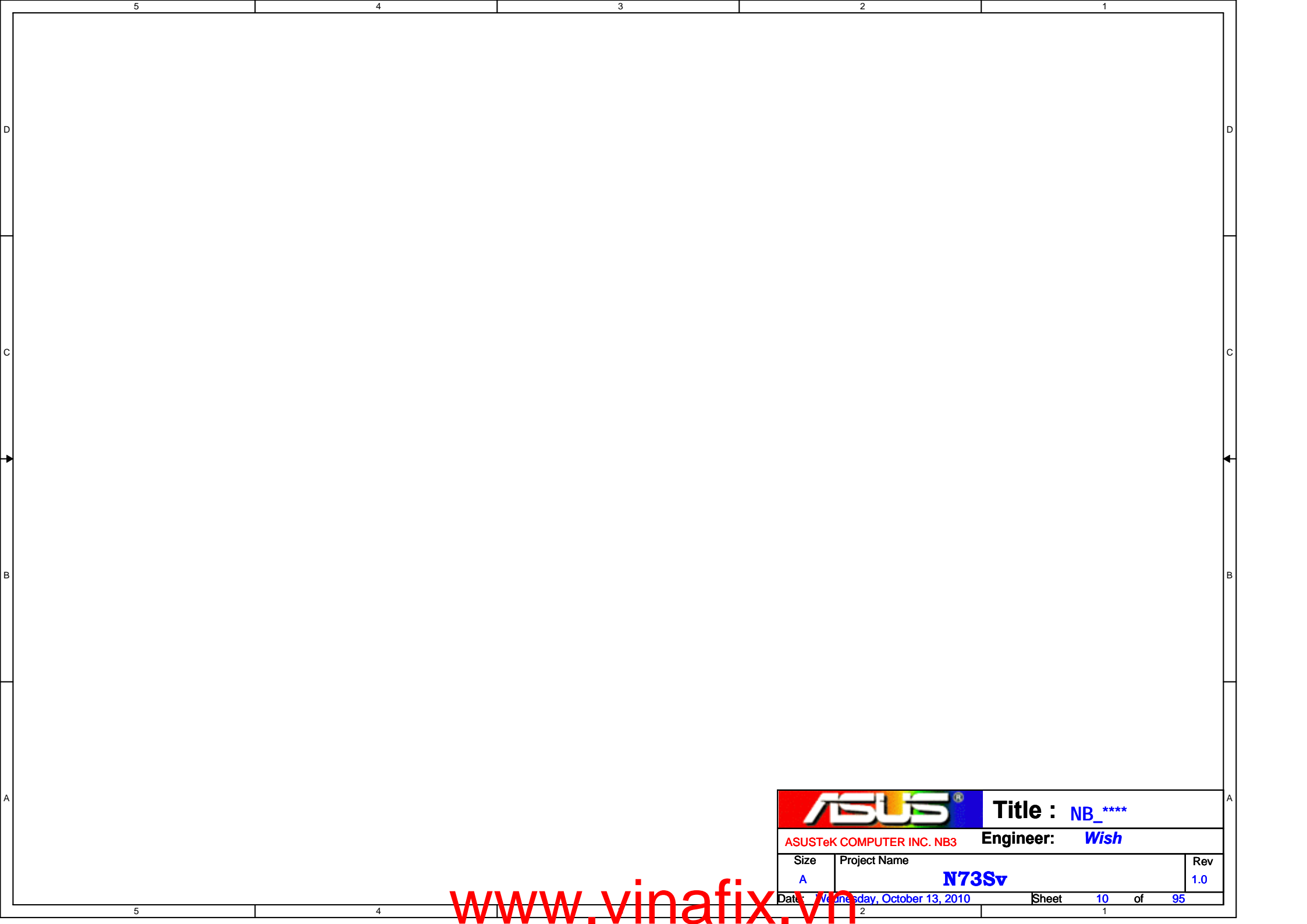
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ASUSTeK COMPUTER INC. NB3

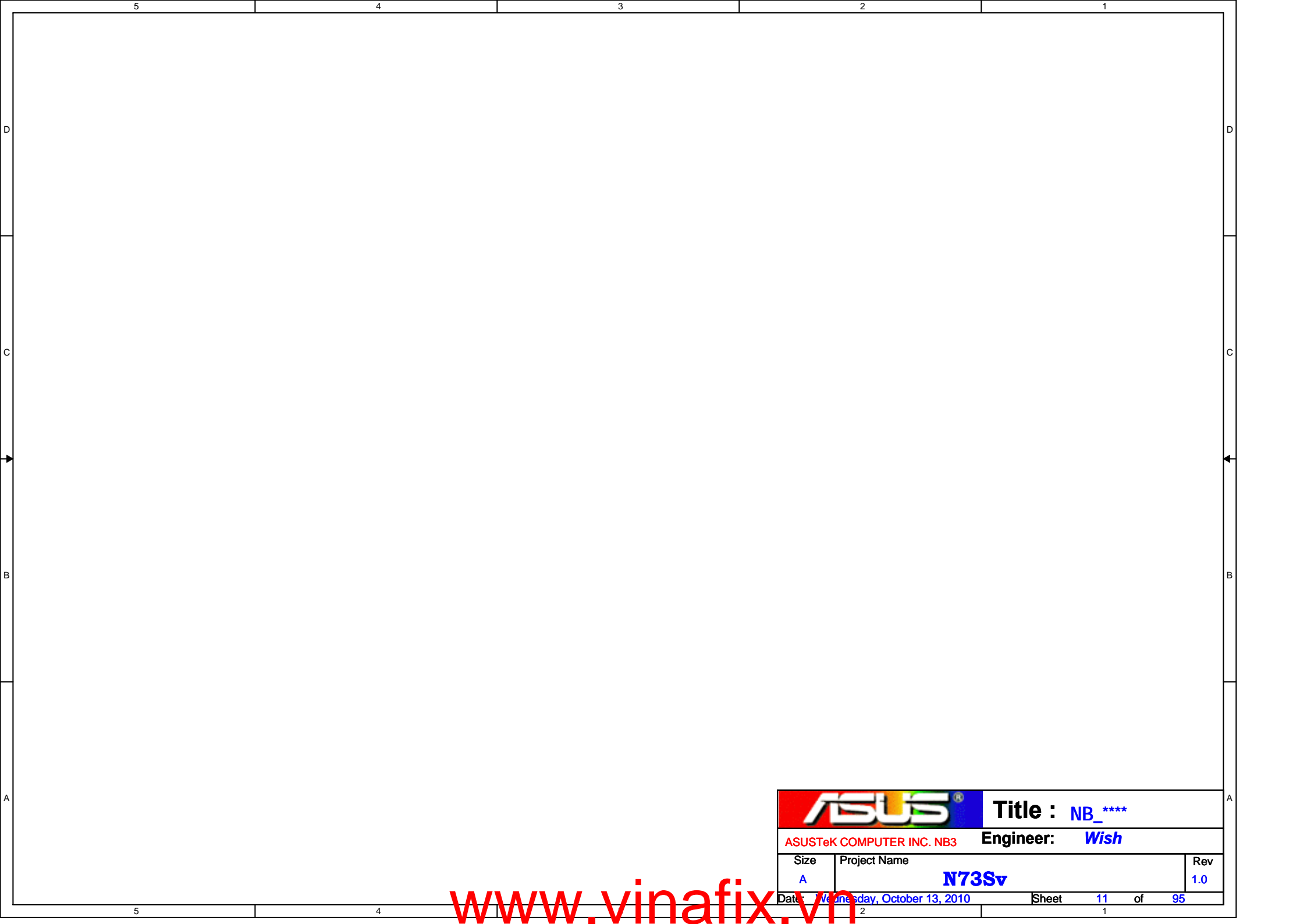
Engineer: *Wish*

Size	Project Name	Rev
A	N73Sv	1.0
Date: Wednesday, October 13, 2010	Sheet 9	of 95

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		Title : NB_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
A	N73Sv	1.0	
Date	Wednesday, October 13, 2010	Sheet	10 of 95



Title : NB_****

ASUSTeK COMPUTER INC. NB3

Engineer: *Wish*

Size	Project Name	Rev
A	N73Sv	1.0
Date: <i>Wednesday, October 13, 2010</i>	Sheet	11 of 95

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		Title : NB_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	12 of 95

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5

4

3

2

1

b

b

c

c

b

b

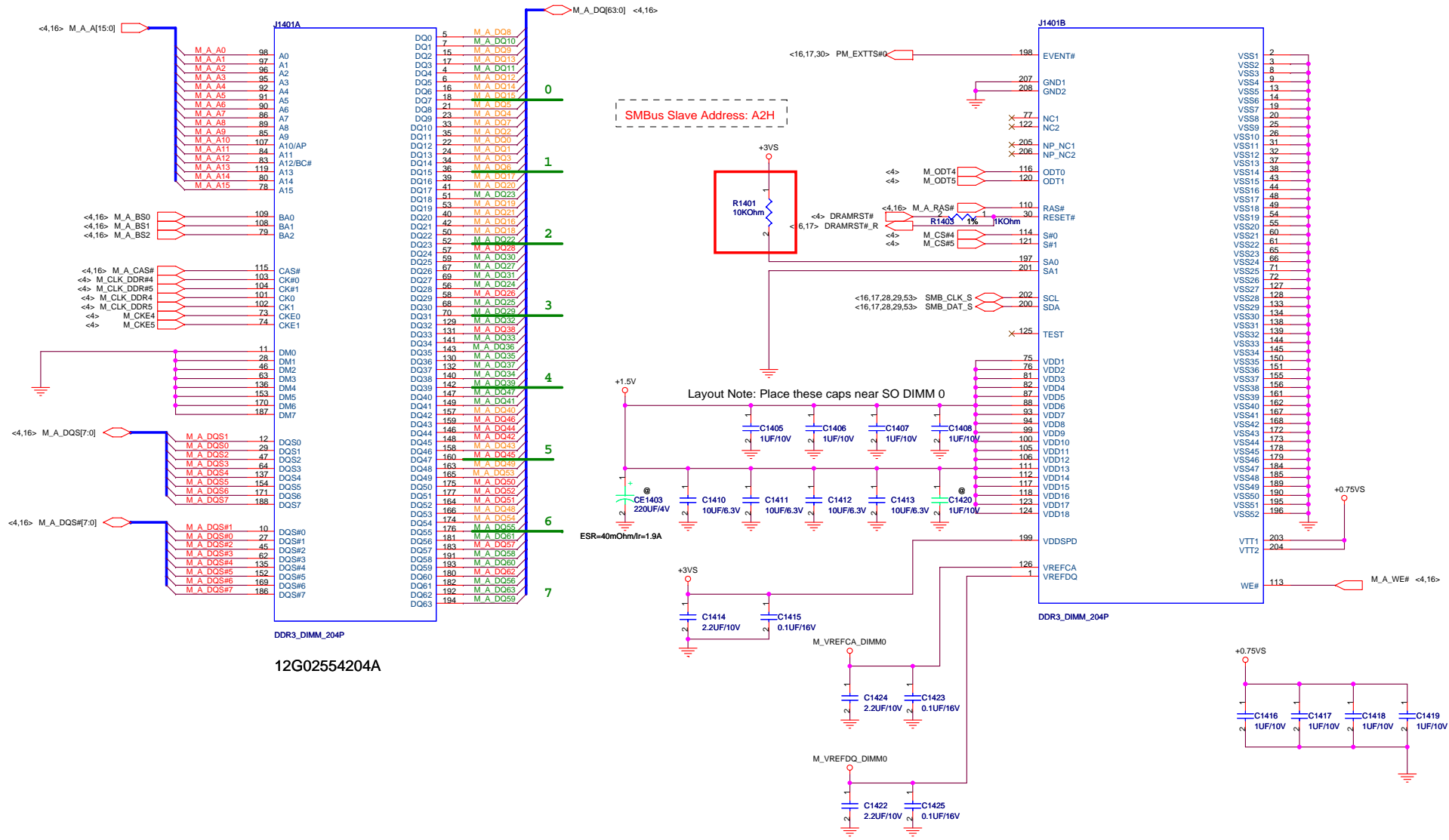
a


a

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		Title : NB_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	13 of 95

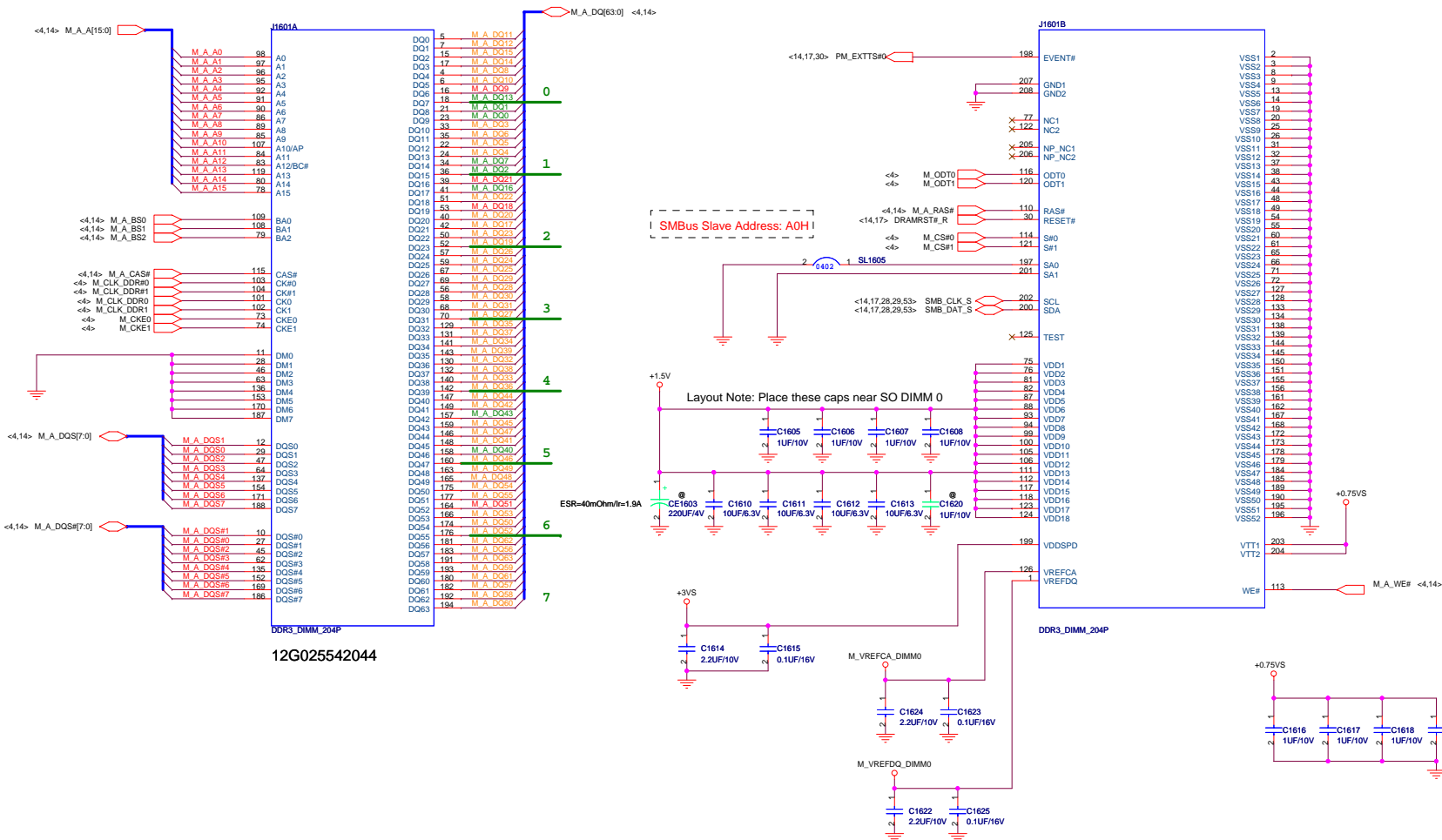
CH-A-4mm-TOP



		Title : DDR3_****	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	15 of 95

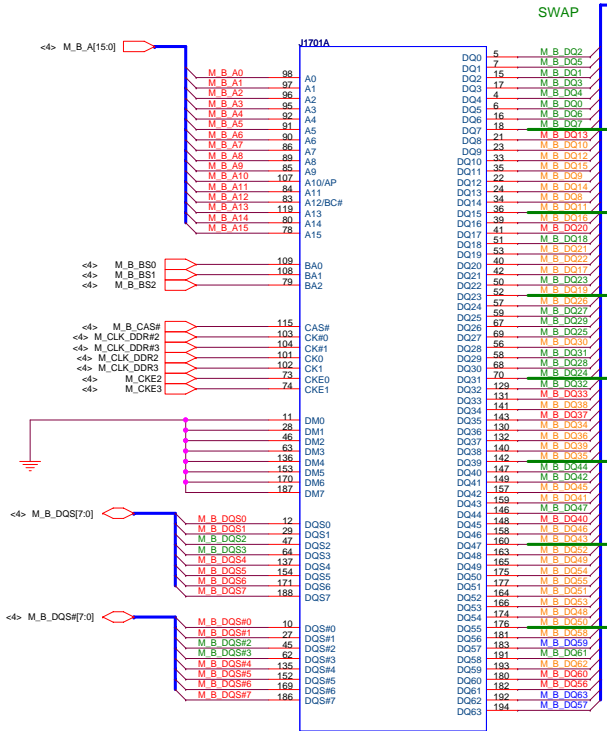
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CH-A-5. 2mm-BOT



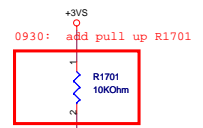
DDR3_DIMM_204P
12G025542044

CH-B-9.2mm-BOT

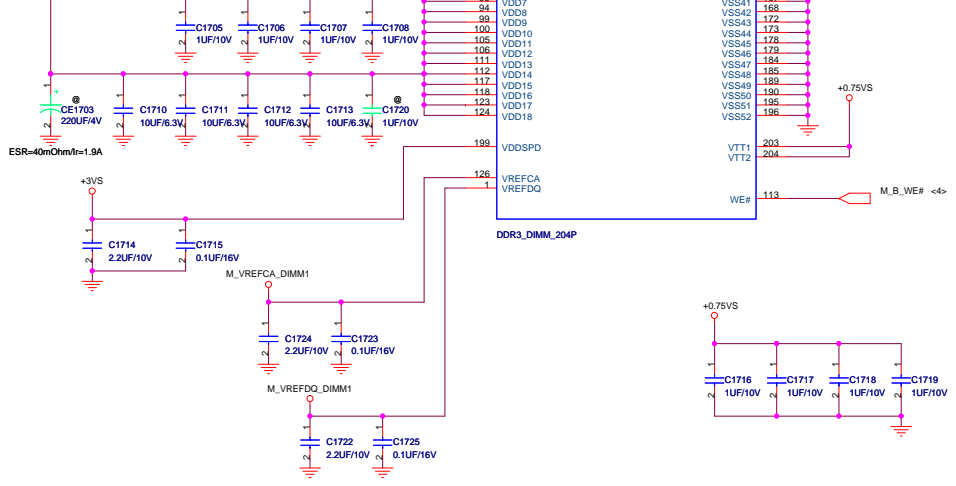


DDR3_DIMM_204P
12G02555204B

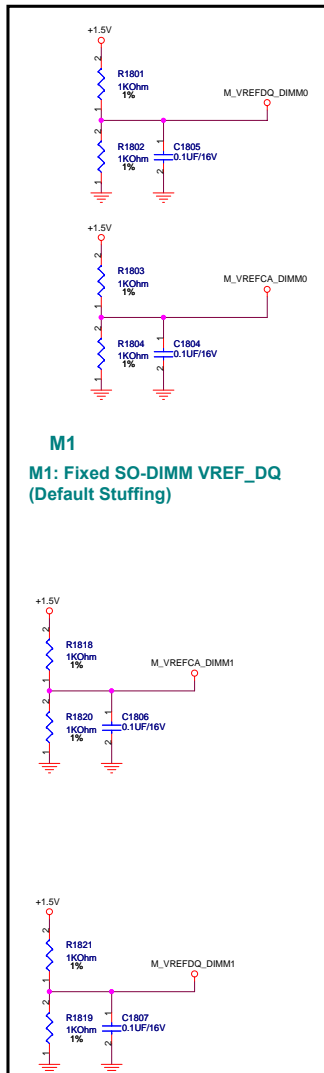
SMBus Slave Address: A4H



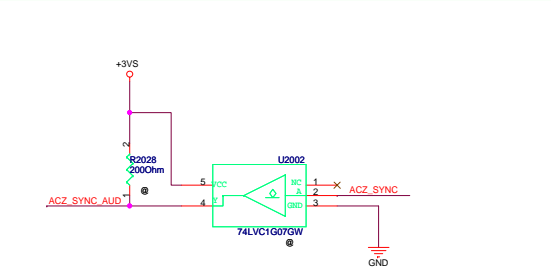
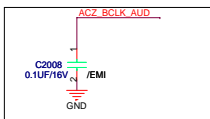
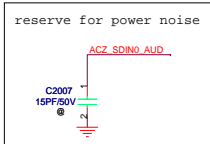
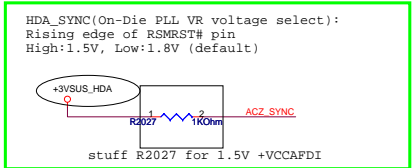
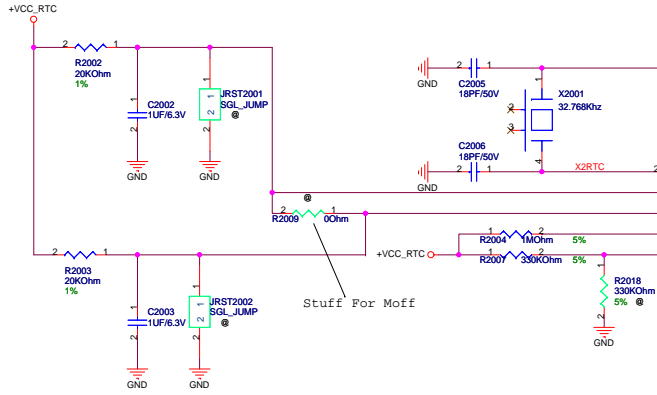
Layout Note: Place these caps near SO DIMM 1



For DDR3_VREF command & address.

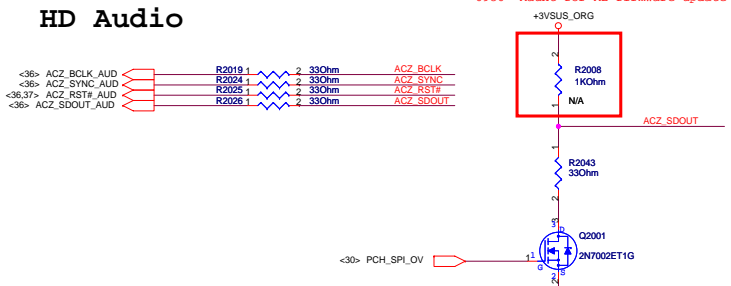


CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

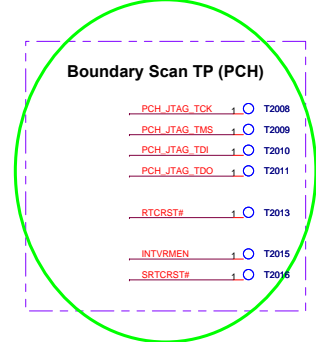
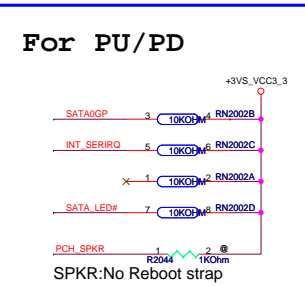
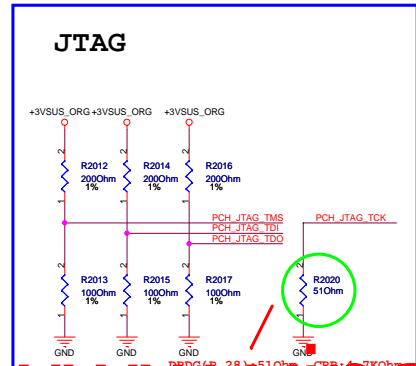


HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the VIHmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase.

ACZ_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V (2)
 ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V
 0930: Maunt for ME firmware update

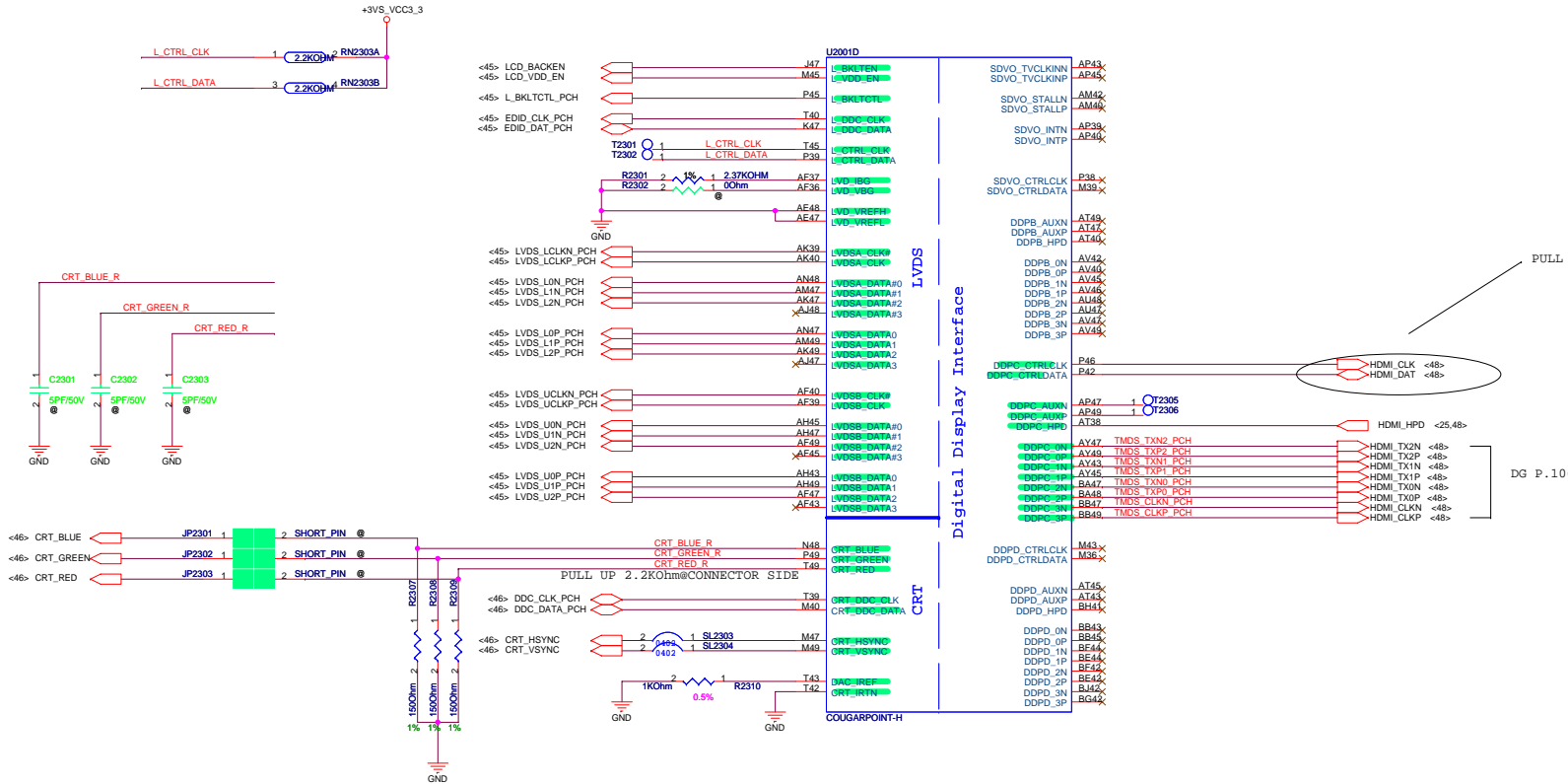


GPIO33 is a signal used for Flash Descriptor security Override/ME debug mode
 HIGH : Disable, LOW : Enable



PORT	STRAP	ENABLE PORT	DISABLE PORT
LVDS	L_DDC_DATA	Pull up to 3.3(V) with 2.2k Ohm	NC
PORT B	SDVO_CTRLDATA		
PORT C	DDPC_CTRLDATA		
PORT D	DDPD_CTRLDATA		

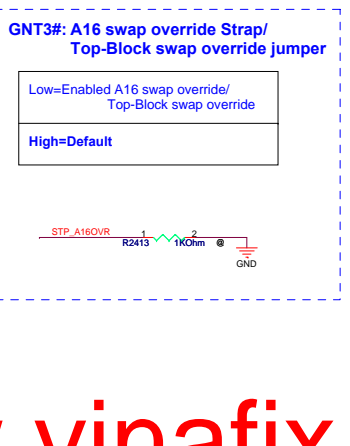
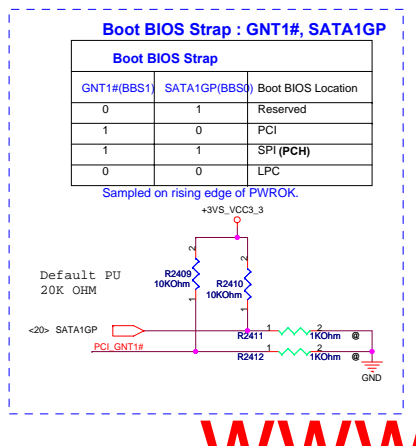
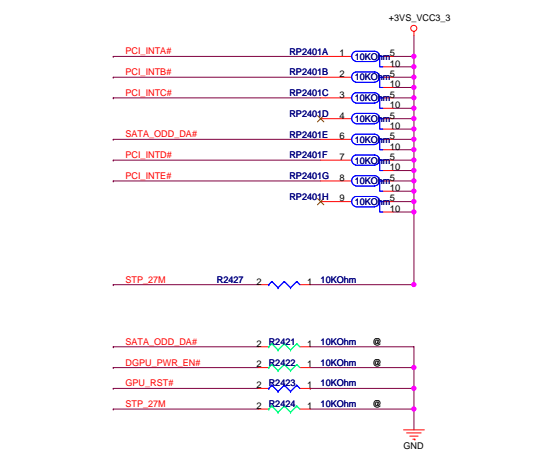
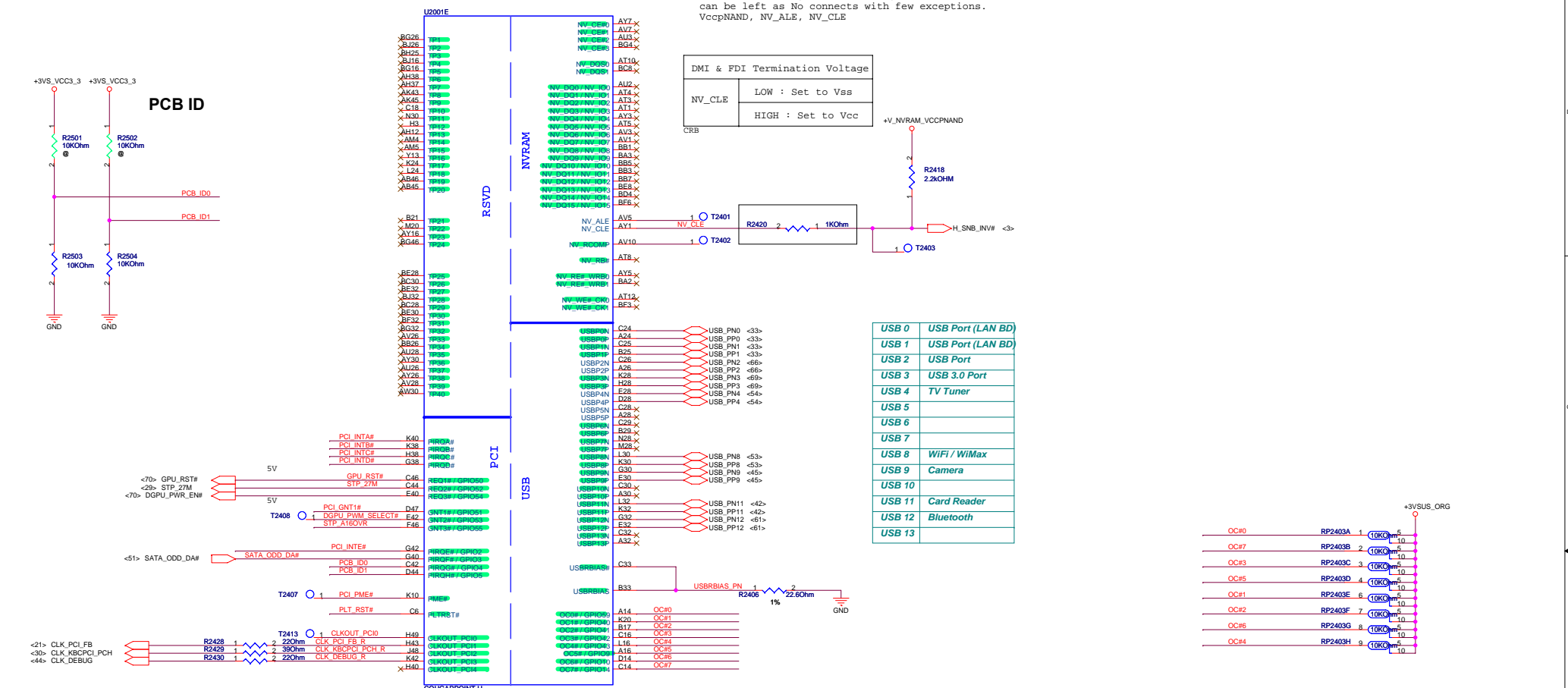
DG P.105,168

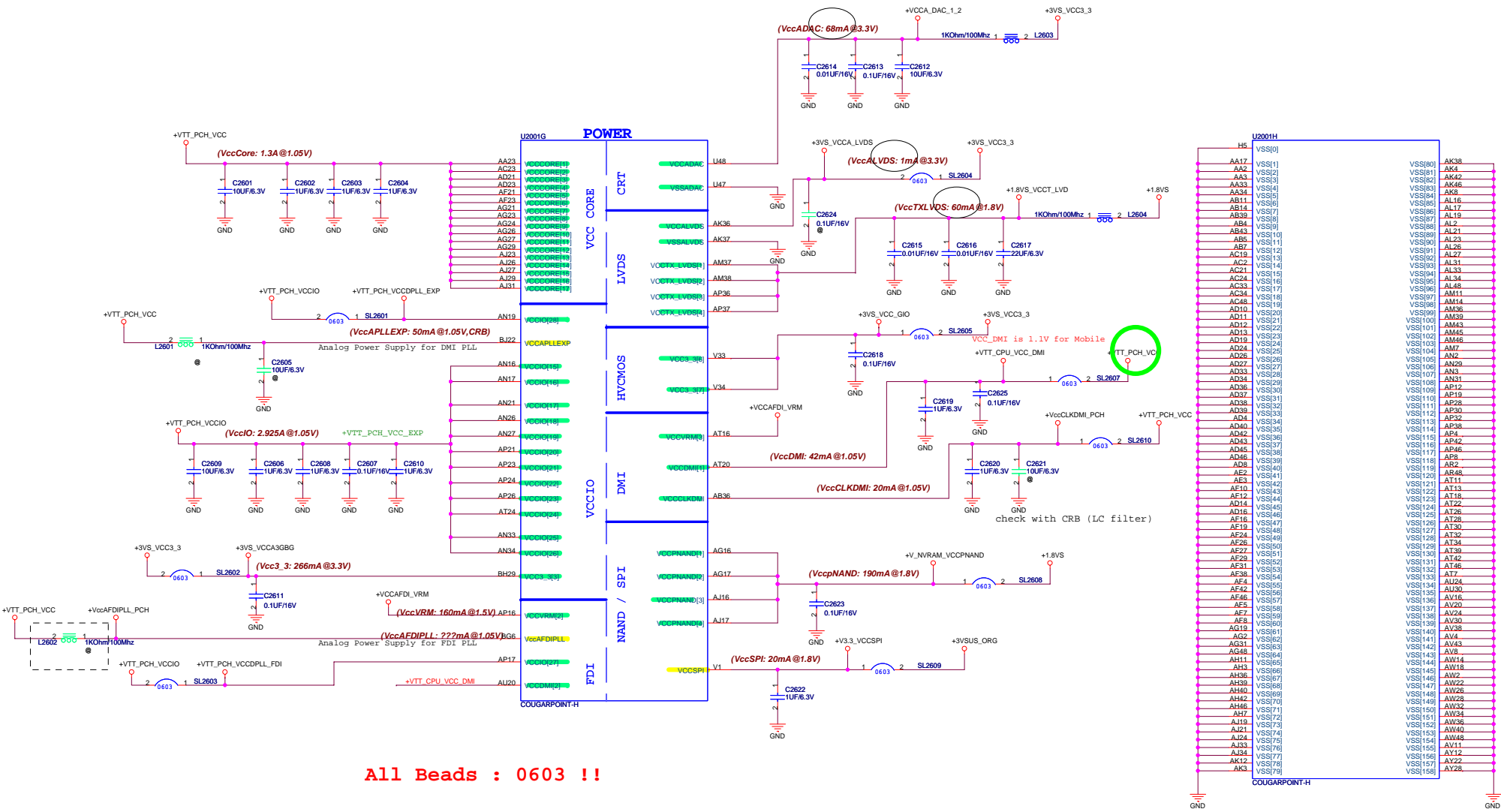


PULL UP 2.2kOhm @ CONNECTOR SIDE

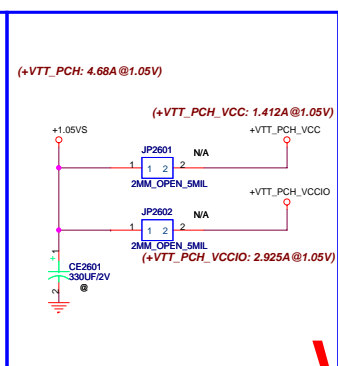
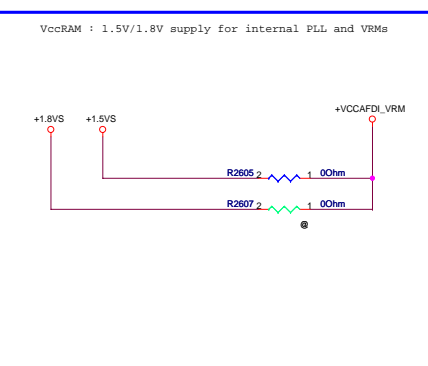
DG P.106

Tacoma Pass(NVRAM) Disabling and termination guidelines(DG R0.7 p.322)
 If the tacoma Pass interface is not used, the interface signals, including NV_RCOMP, can be left as No connects with few exceptions.
 VccpNAND, NV_ALE, NV_CLE



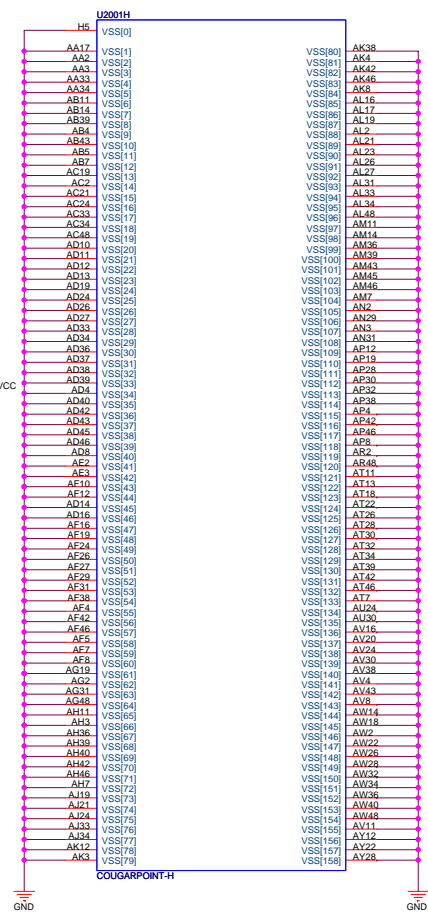


All Beads : 0603 !!



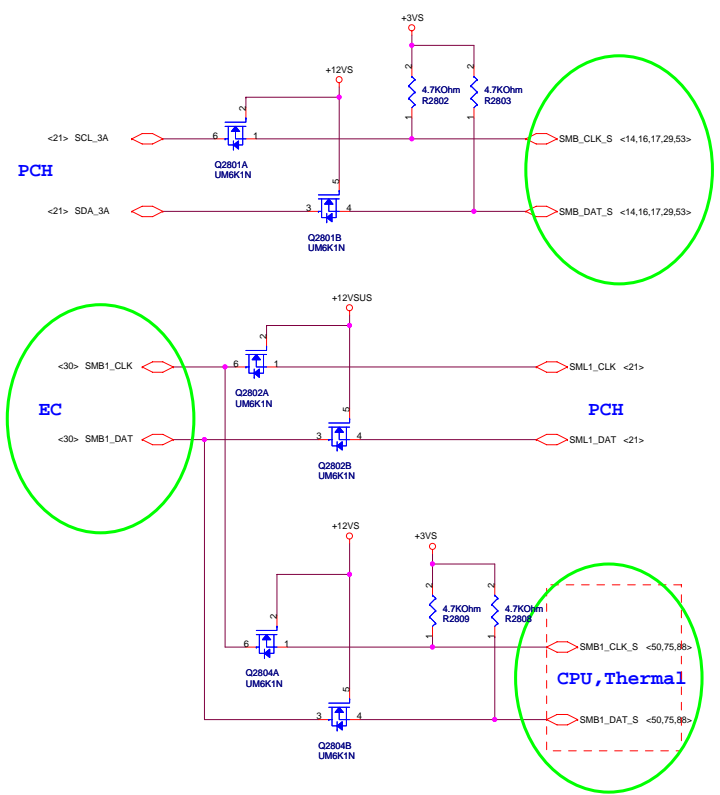
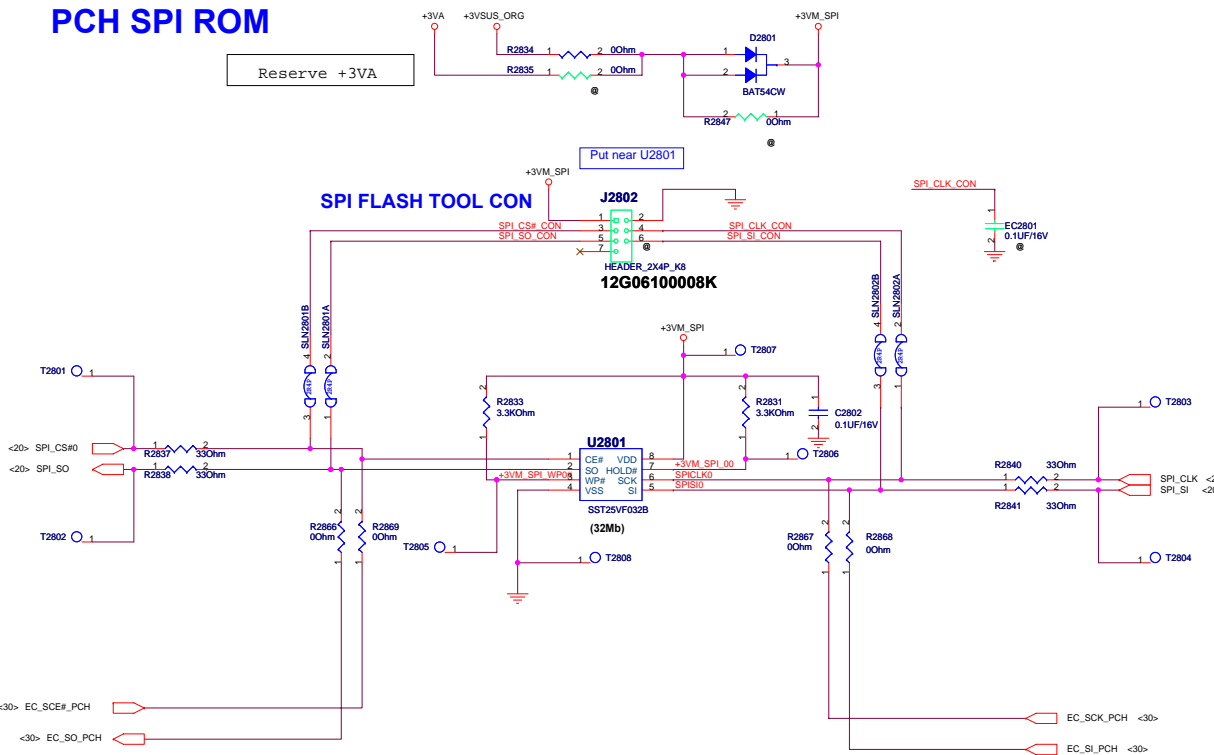
PCH ICC Description

+VTT	4.68A
+1.5VS	0.16A
+1.8VS	0.19A
+3VS	0.355A
+3VSUS	0.1A

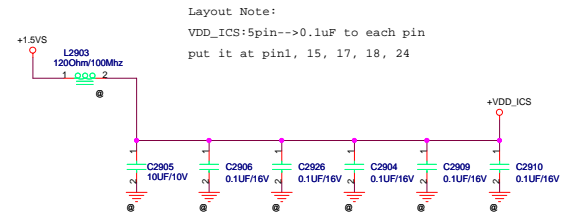
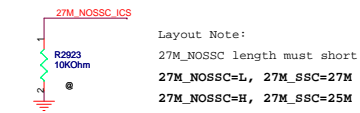
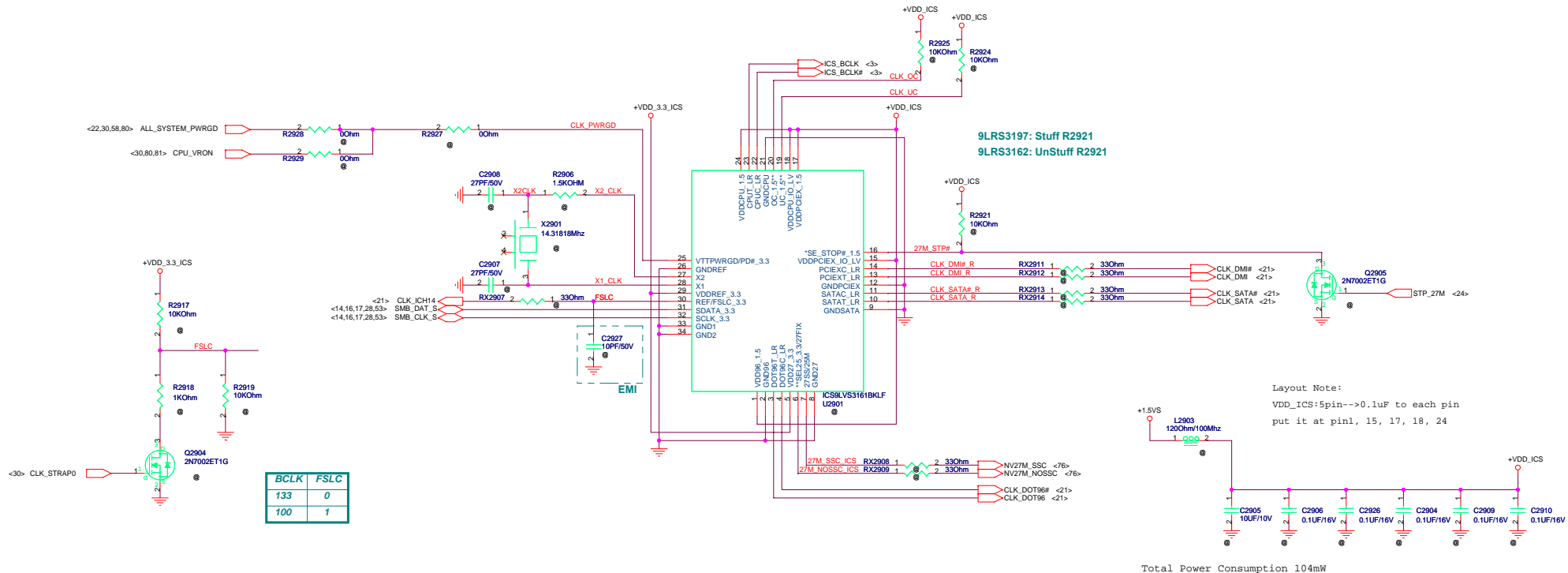


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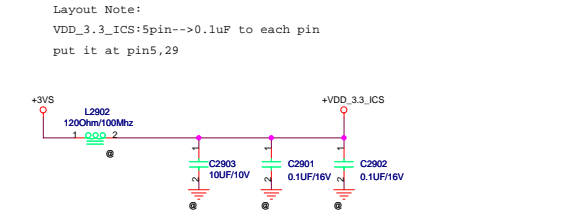
PCH SPI ROM

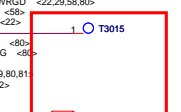
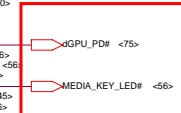
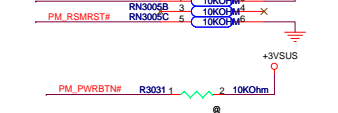
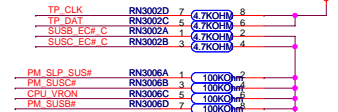
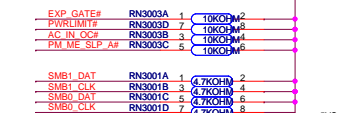
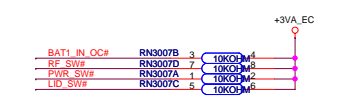
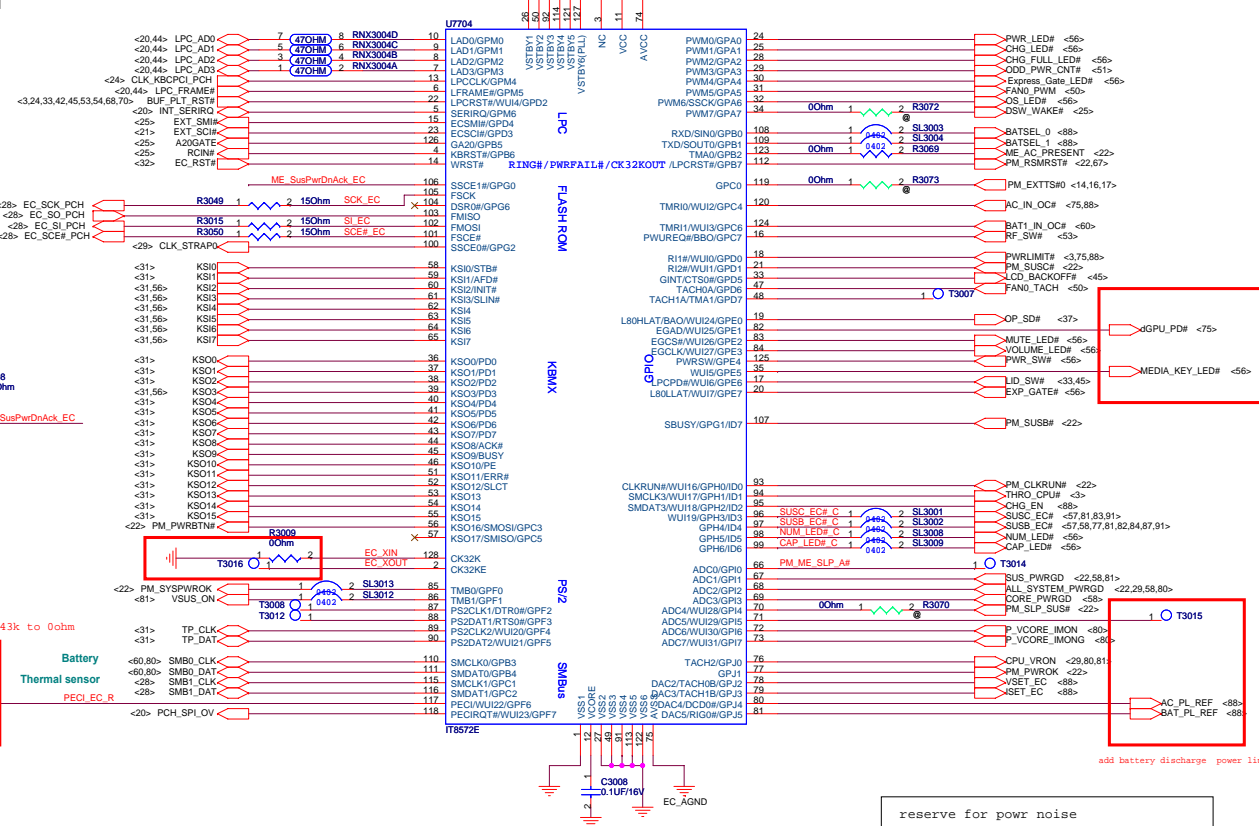
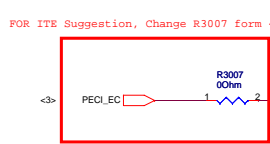
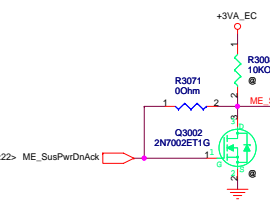
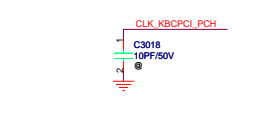
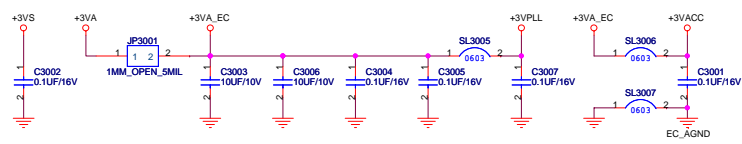
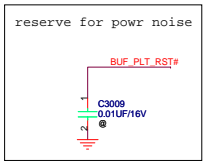


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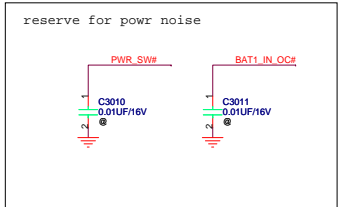


Total Power Consumption 104mW

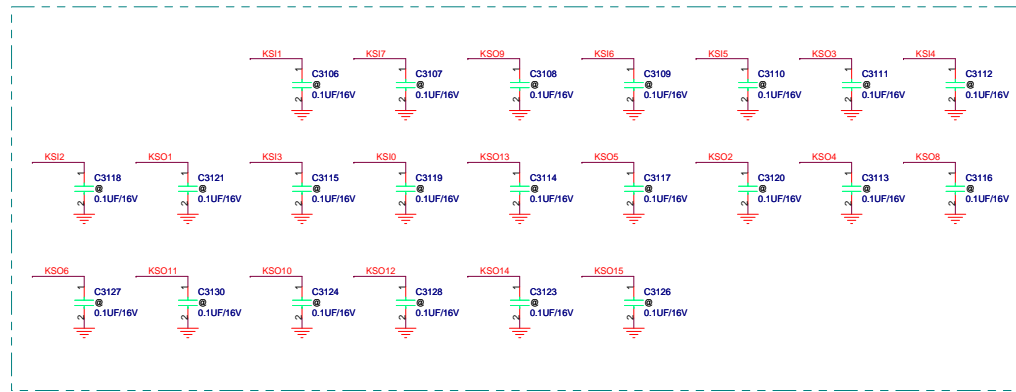
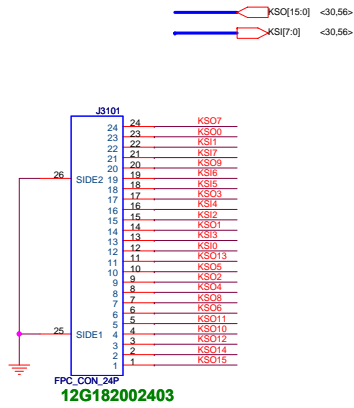




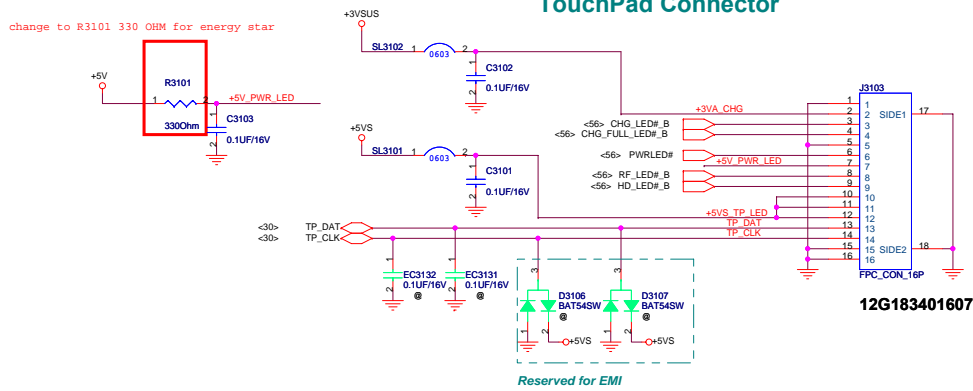
add battery discharge power limit circuit



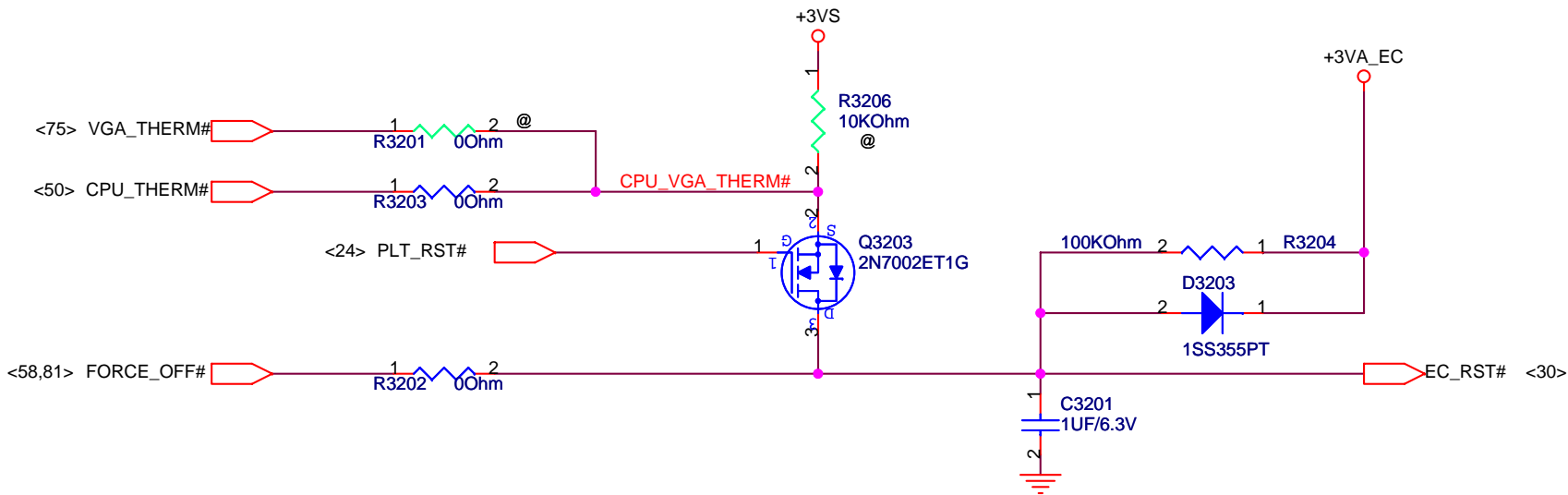
Keyboard Connector



TouchPad Connector

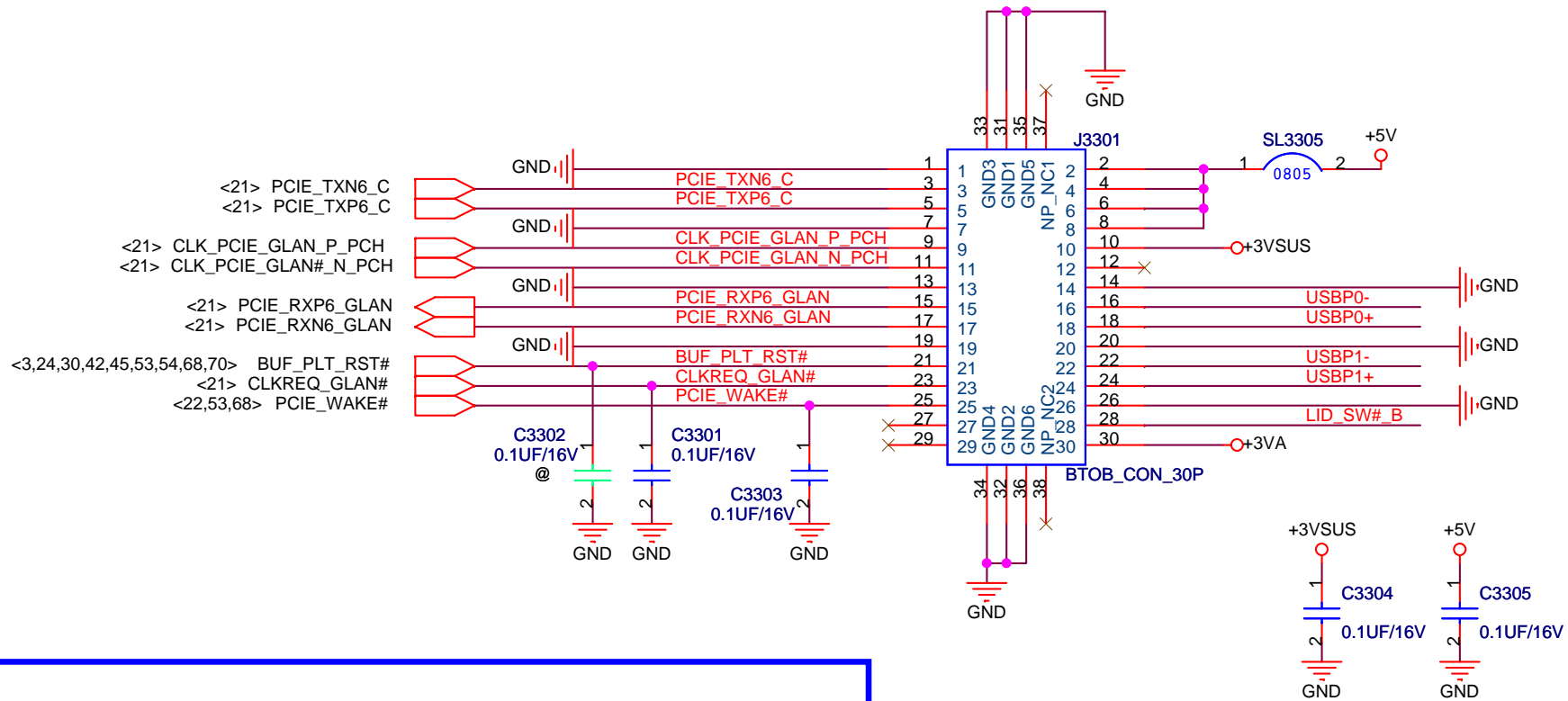


Main Board

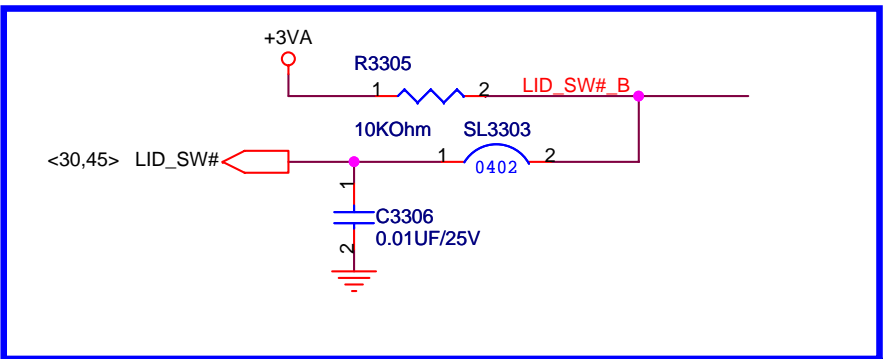
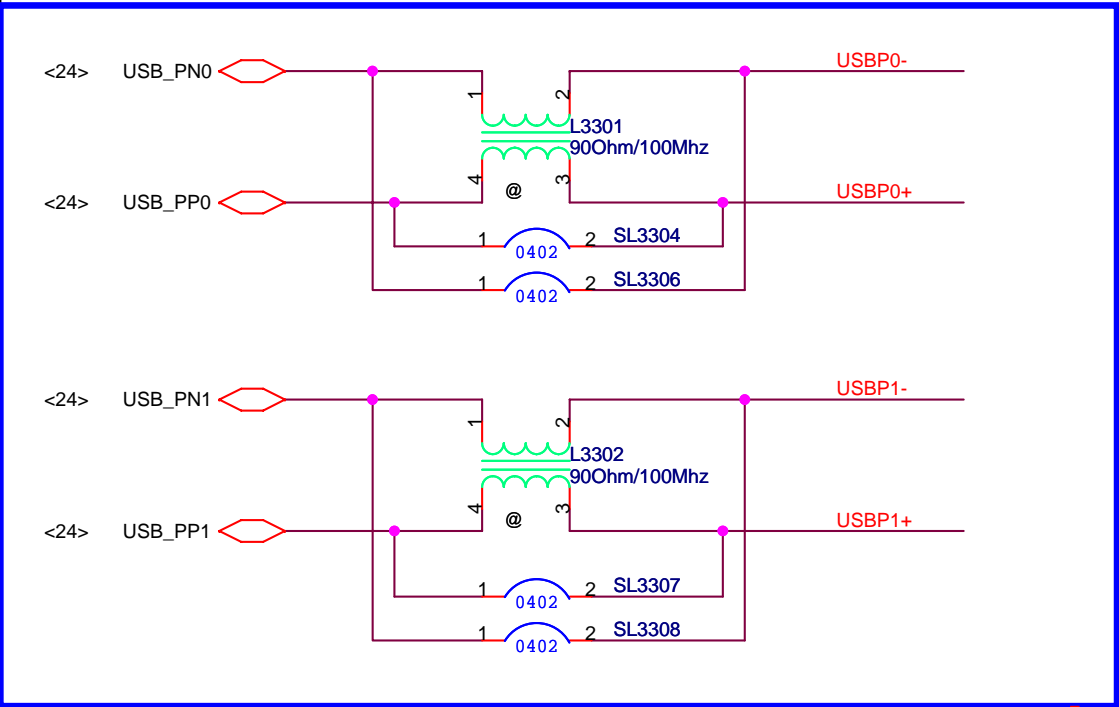


Check it! ITE說C3201可以不用加


		Title : RST_Reset Circuit	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size A	Project Name N73Sv	Rev 1.0	
Date: Wednesday, October 13, 2010		Sheet 32 of 95	



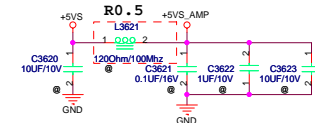
EMI RESERVE
recommand stuff



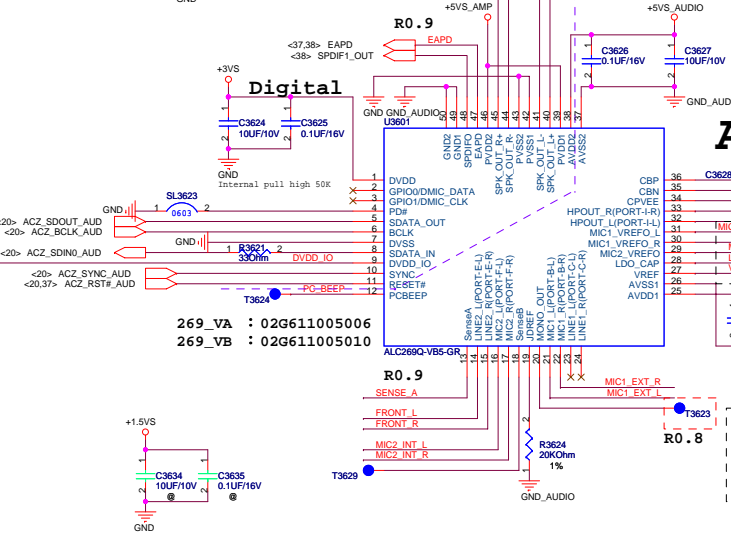
ASUS		Title : LAN_AR8131	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size A	Project Name N73Sv	Rev 1.0	
Date: Wednesday, October 13, 2010		Sheet 33 of 95	

		Title : LAN_RJ45 Conn.	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size	Project Name		Rev
B	N73Sv		1.0
Date: Wednesday, October 13, 2010		Sheet	34 of 95

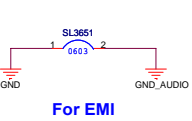
DIGITAL



The Power consumption is 0.18mA on S5



269_VA : 02G611005006
269_VB : 02G611005010

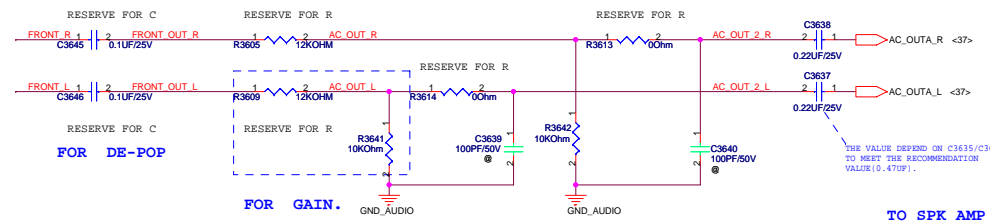
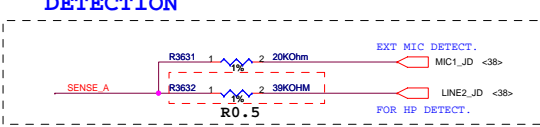
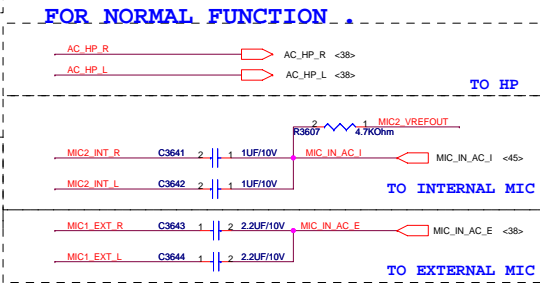
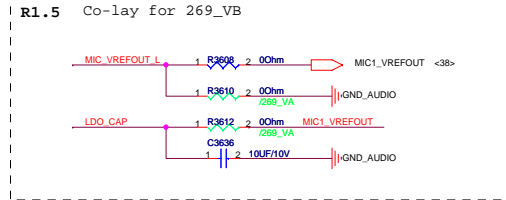
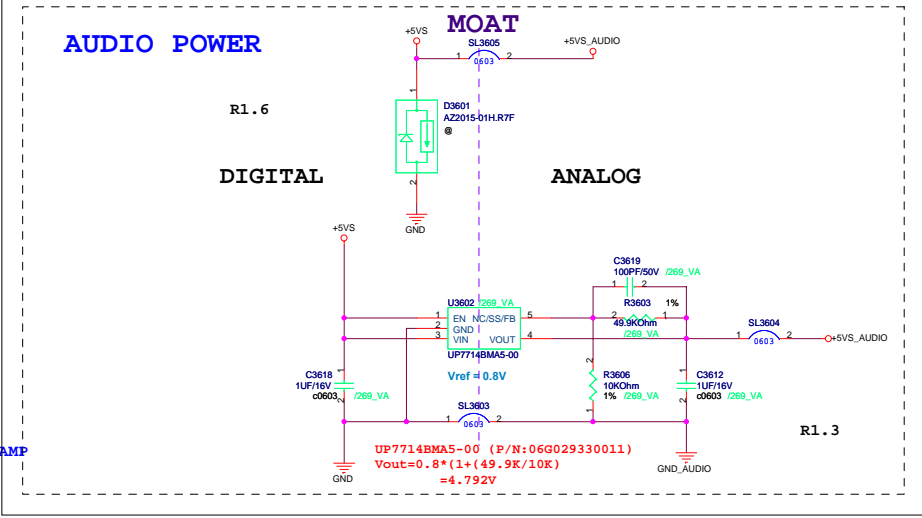


For EMI

MOAT

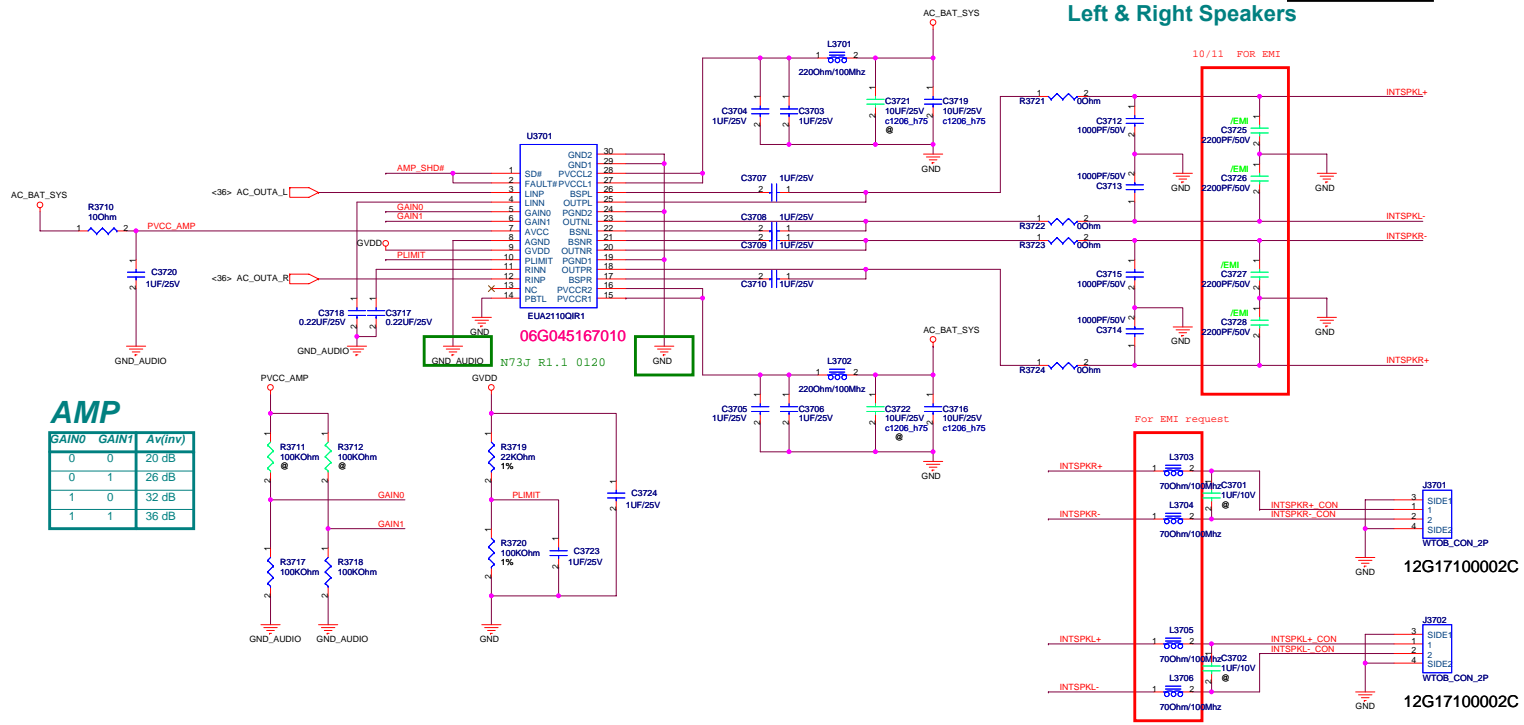
ANALOG

RealTek recommend change C3631 from 2.2uF to 1uF
New project : Please use the 1uF for VREF_CODEC
On going project : Please keep 2.2uF for VREF_CODEC if speaker have not S3 · S4 resume issue.



ASUS		Title : CODEC ALC269	
ASUSTeK COMPUTER INC. NB2		Engineer: Wish	
Size C	Project Name N735v	Rev 1.0	
Date: Wednesday, October 13, 2010	Sheet 36	of 95	

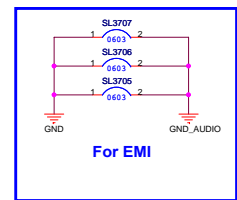
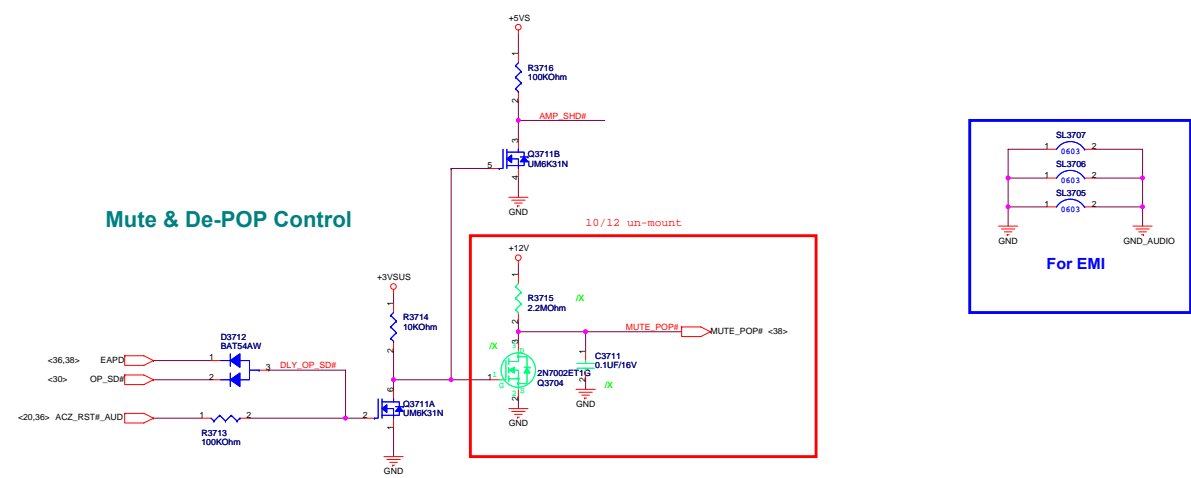
Left & Right Speakers



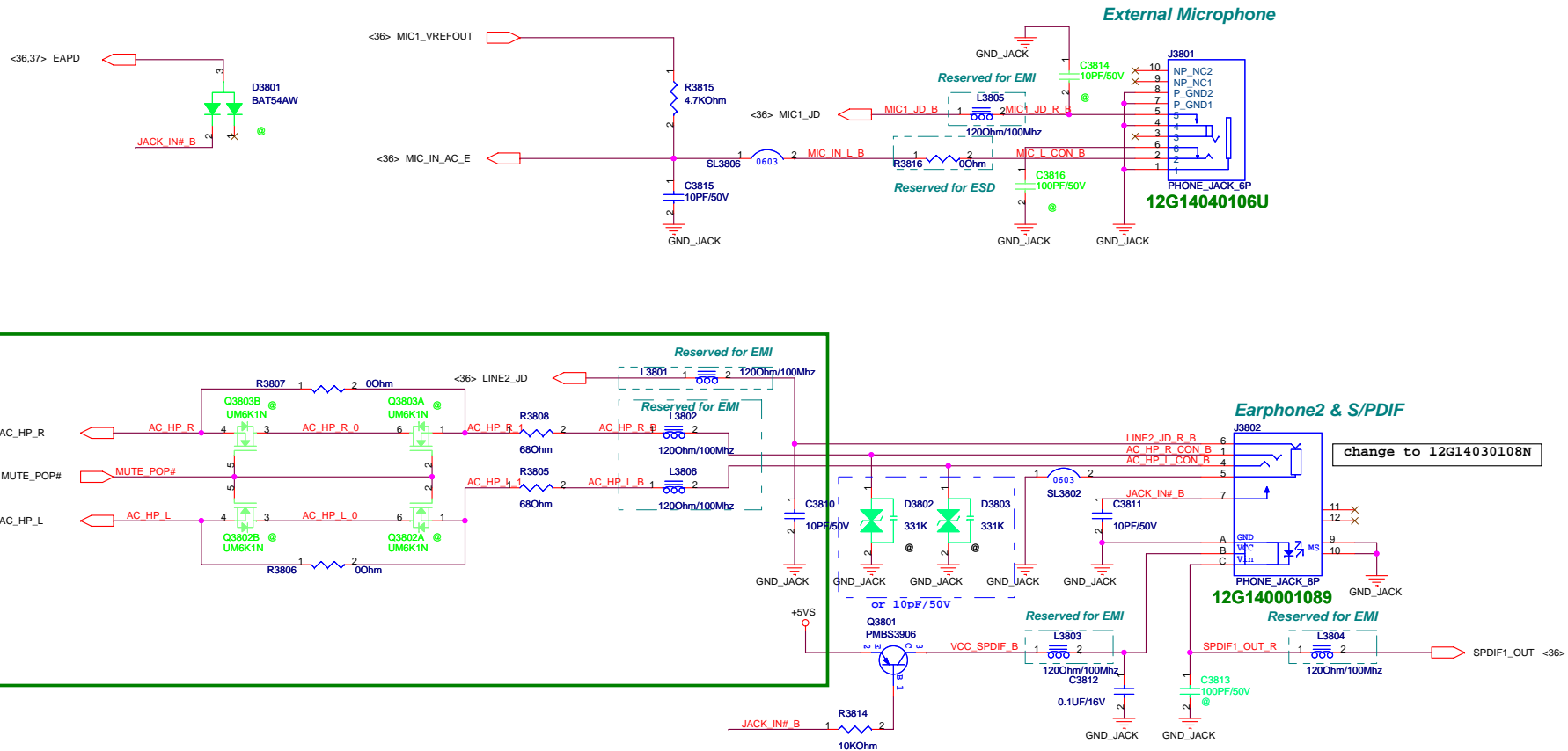
AMP

SAIN0	GAIN1	Av(inv)
0	0	20 dB
0	1	26 dB
1	0	32 dB
1	1	36 dB

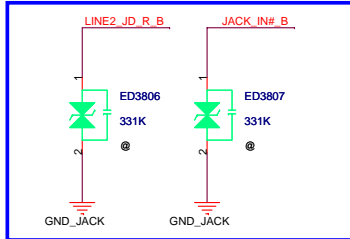
Mute & De-POP Control



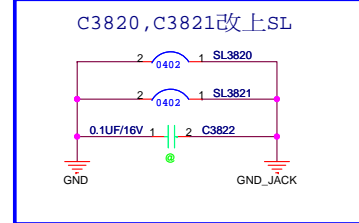
AUDIO



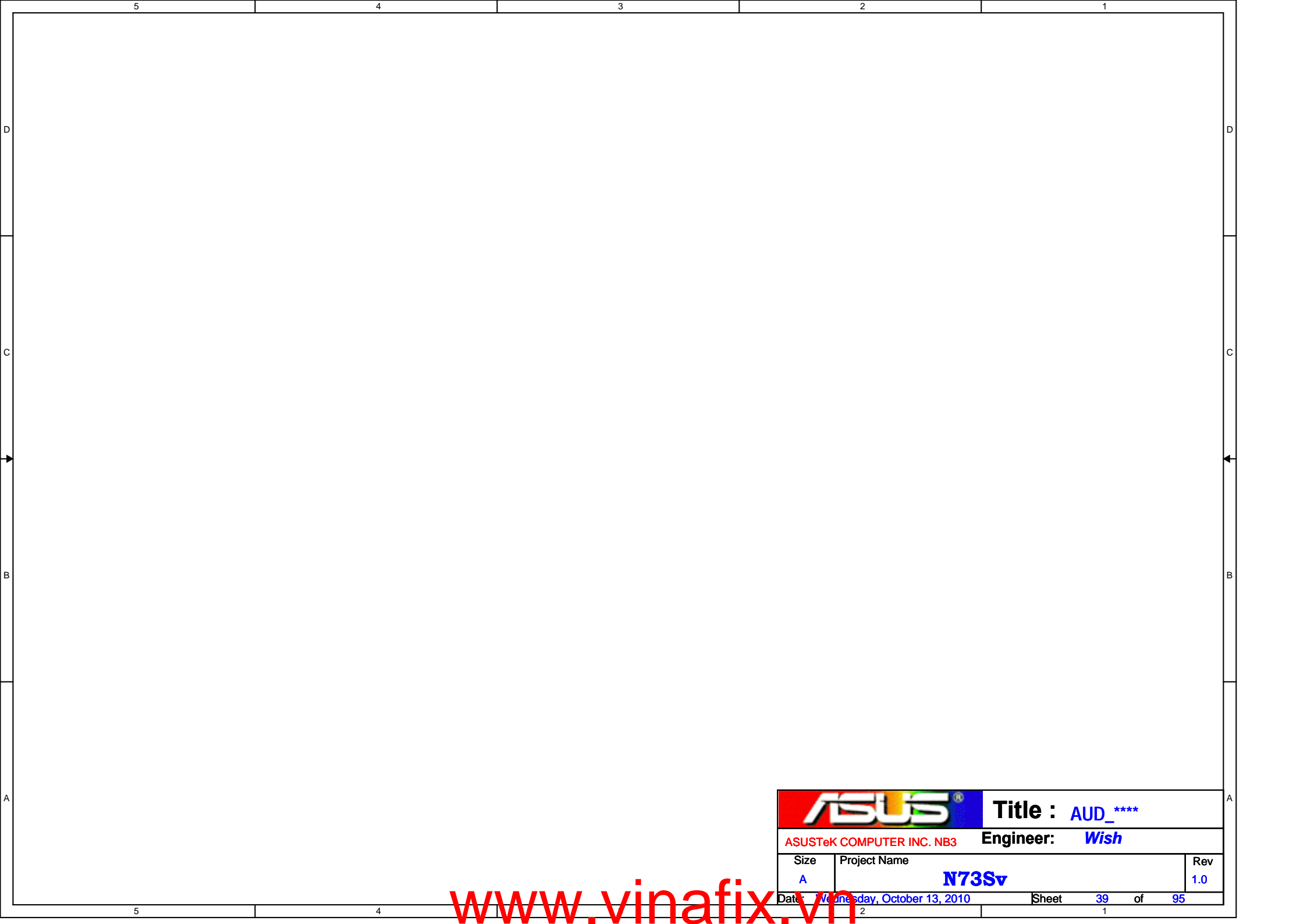
For EMI Reserve




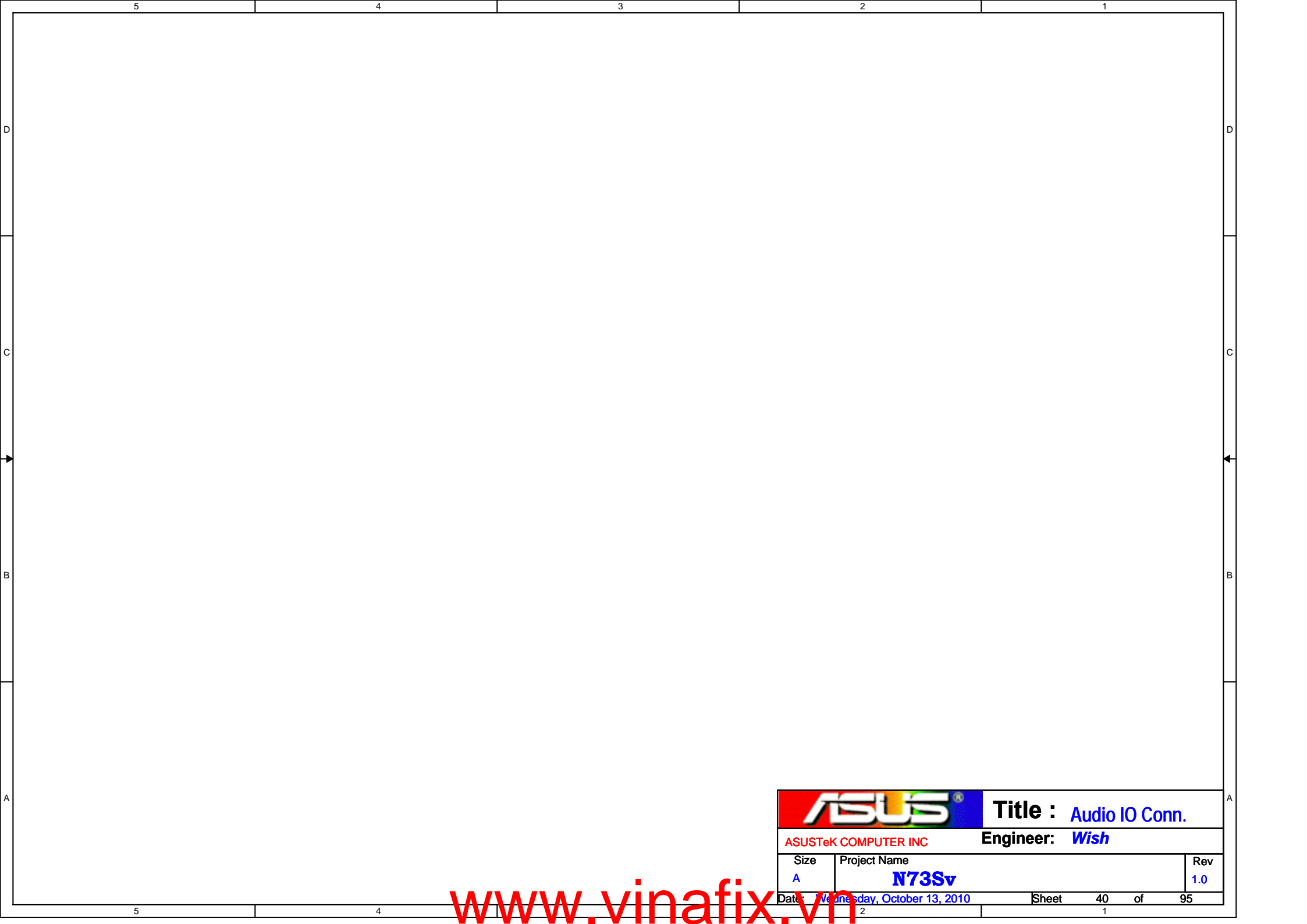
For EMI Reserve



<Variant Name>		ASUS		Title : MIC&LINE1	
ASUSTek COMPUTER INC. NB2		Engineer: Wish			
Size	Project Name	Rev			
Custom	N738v	1.0			
Date	Wednesday, October 13, 2010	Sheet	38	of 95	



		Title : AUD_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
A	N73Sv	1.0	
Date	Wednesday, October 13, 2010	Sheet	39 of 95



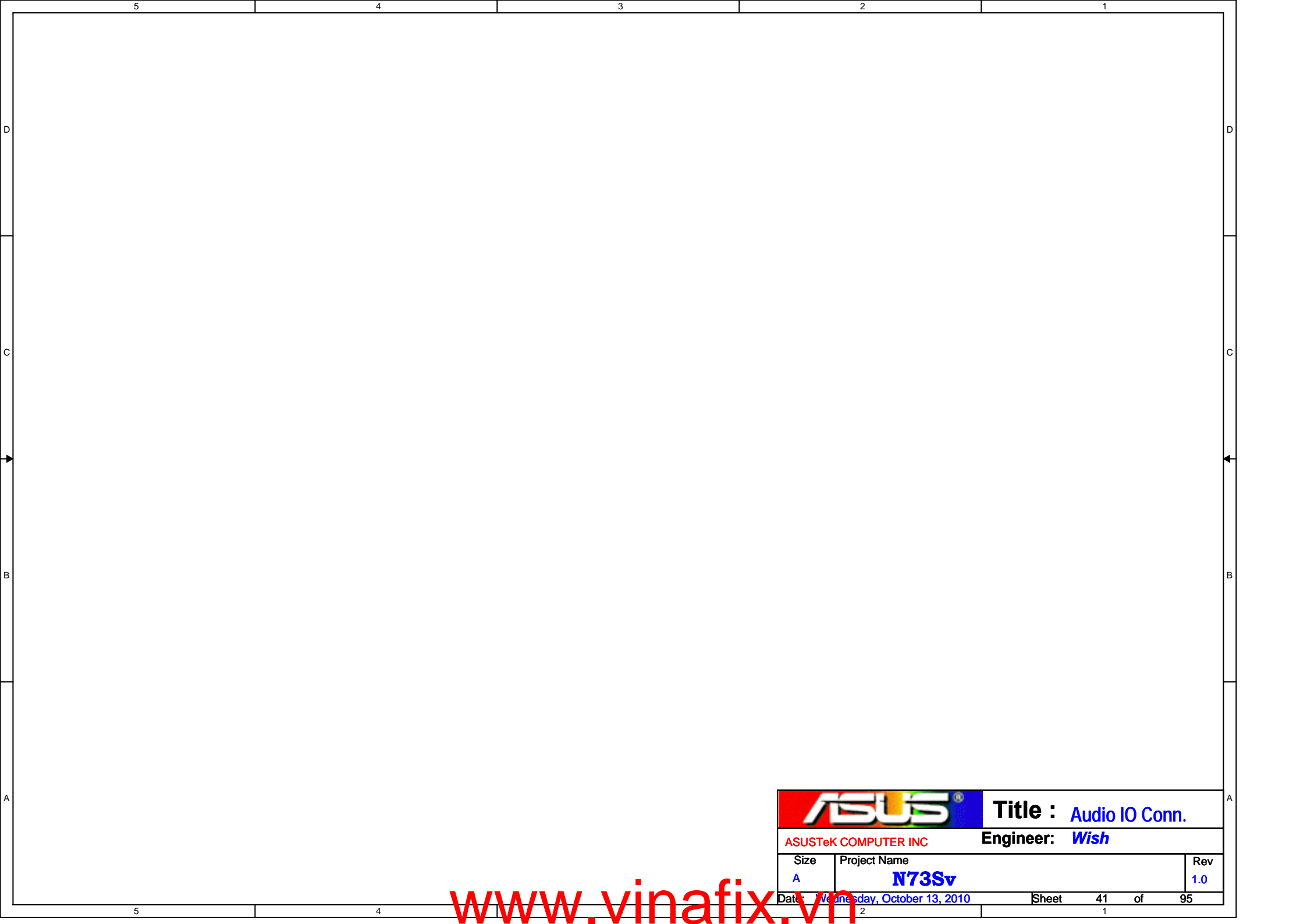
Title : Audio IO Conn.

ASUSTeK COMPUTER INC

Engineer: Wish

Size	Project Name	Rev
A	N73Sv	1.0
Date	Wednesday, October 13, 2010	Sheet 40 of 95

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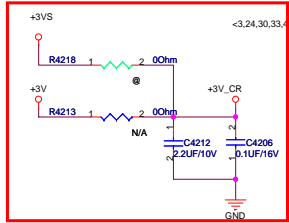
Title : Audio IO Conn.

ASUSTeK COMPUTER INC

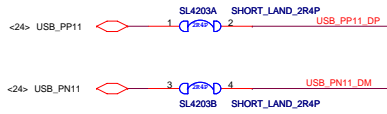
Engineer: Wish

Size	Project Name	Rev
A	N73Sv	1.0
Date: Wednesday, October 13, 2010	Sheet 41 of 95	

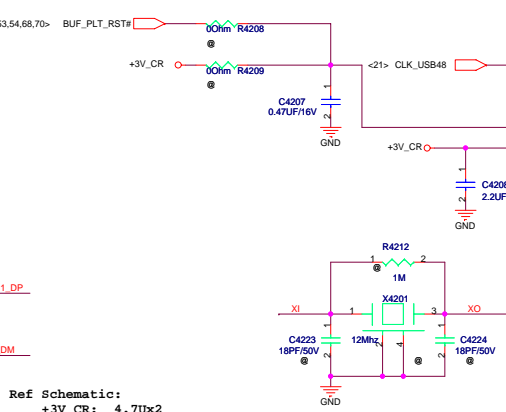
1009 reserve R4218 (+3VS) for energy star



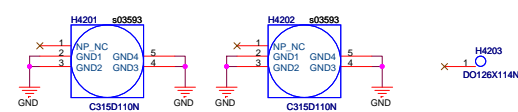
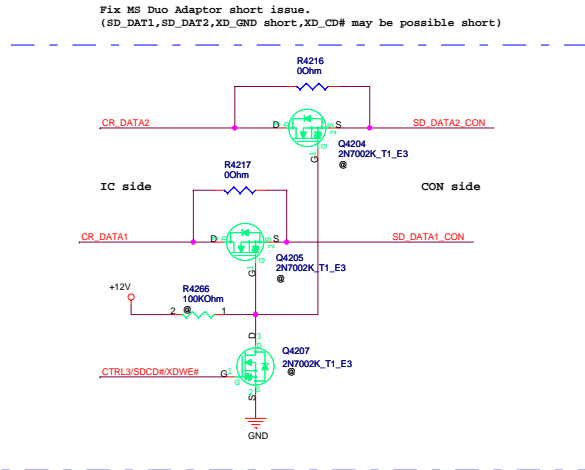
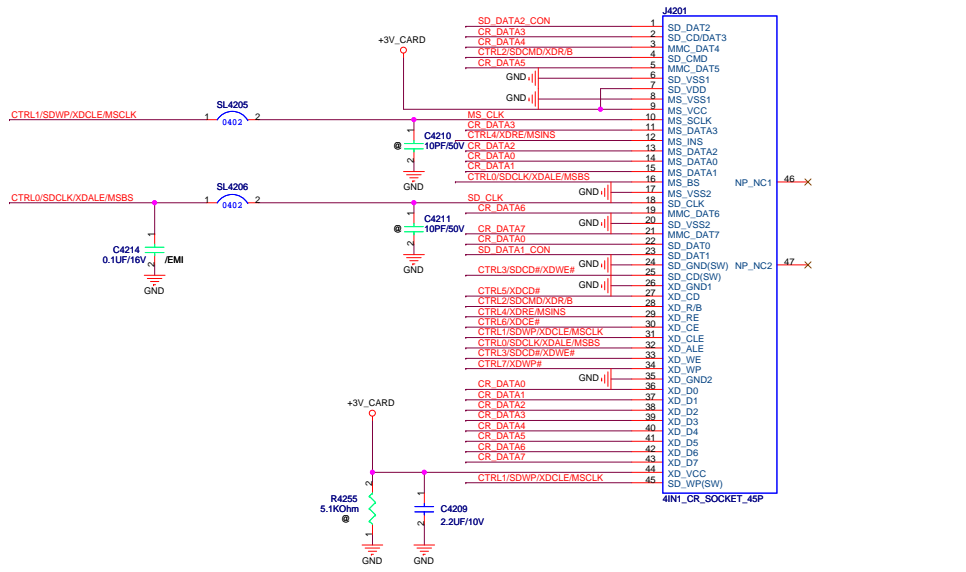
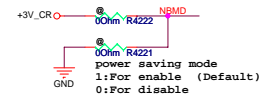
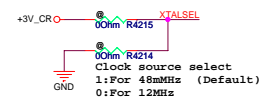
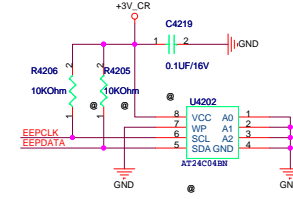
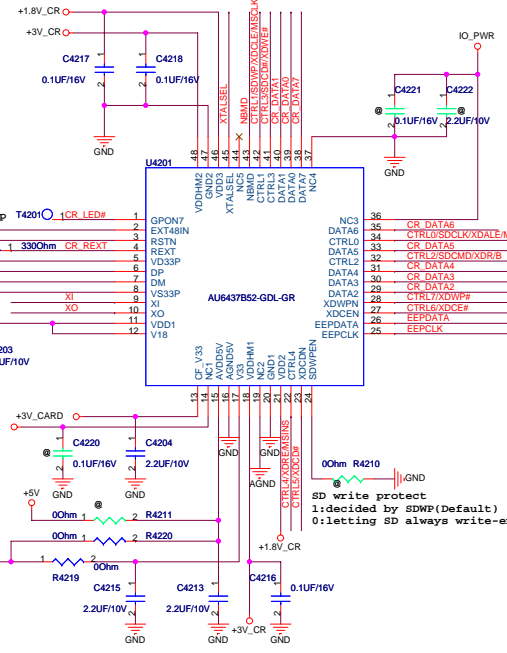
Reserve for Eye Diagram



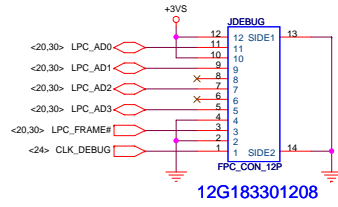
Pin2 has internal pu 75K to +3V.



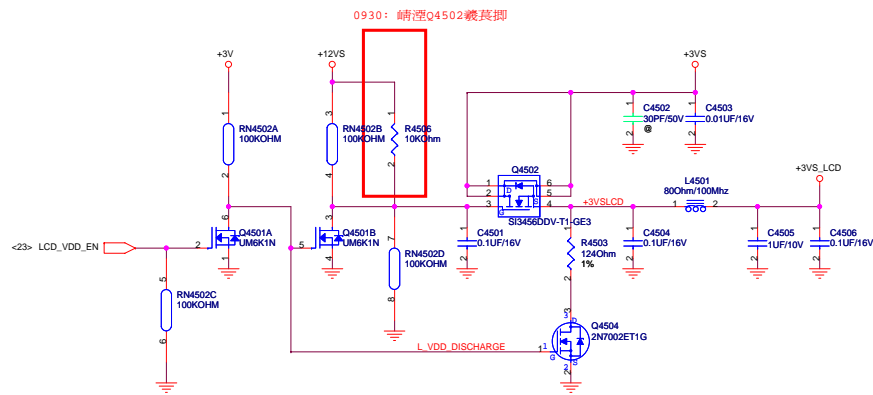
Ref Schematic:
+3V_CR: 4.7Ux2
0.1Ux1
+1.8V: 2.2Ux1
+3V_CARD: 4.7Ux1



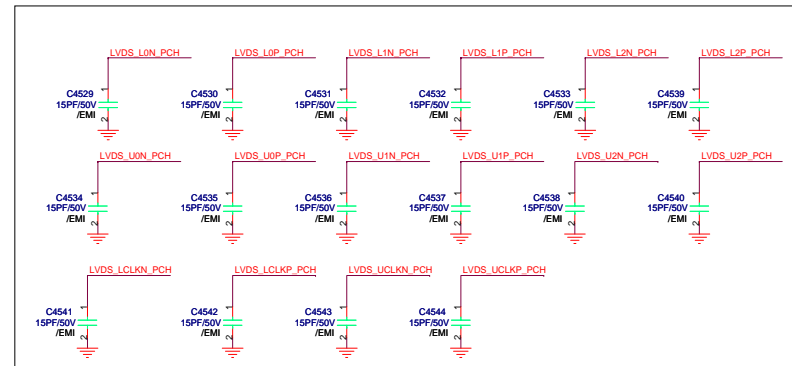
LPC Debug Port



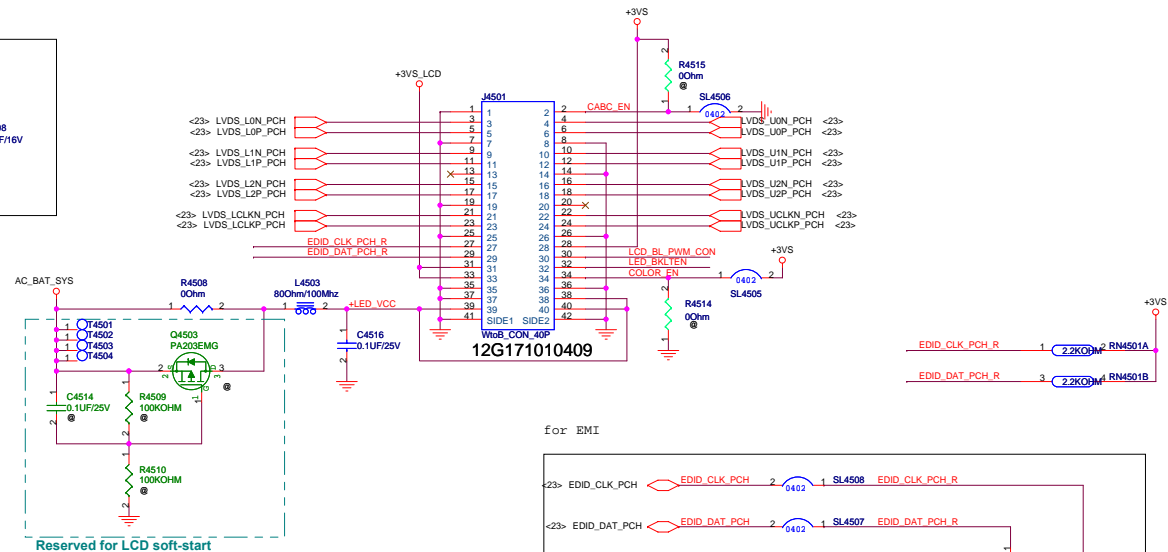
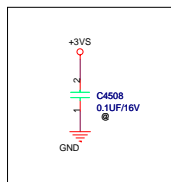
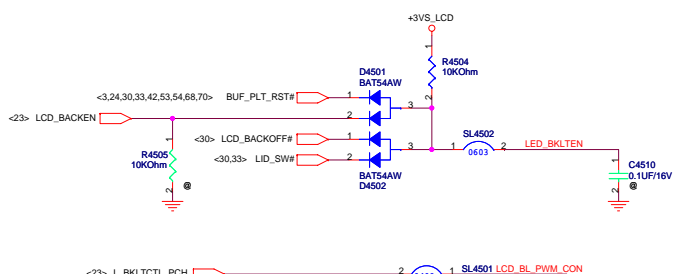
LCD Power



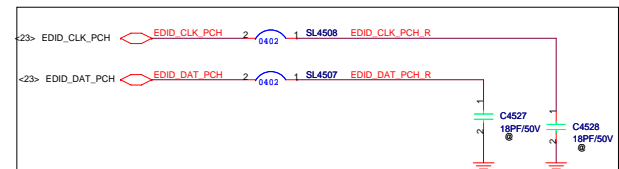
for EMI



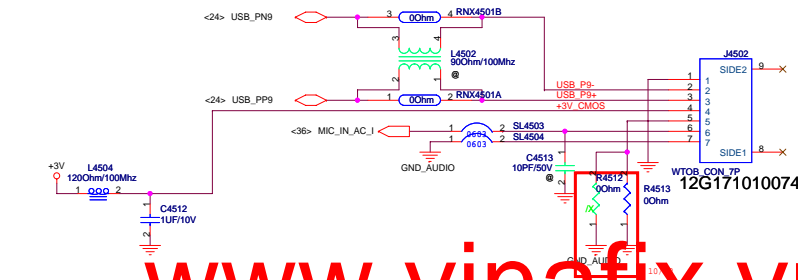
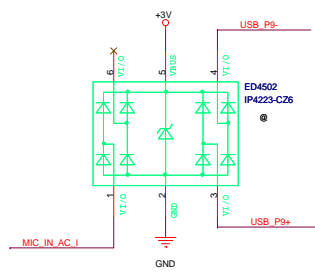
Panel Connector

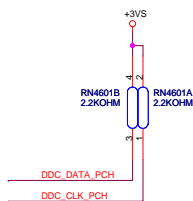
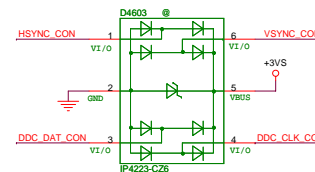
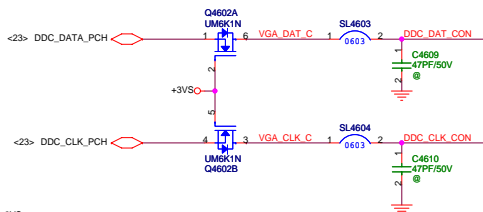
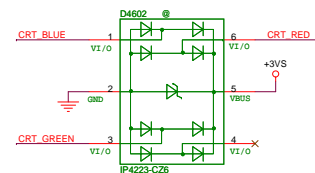
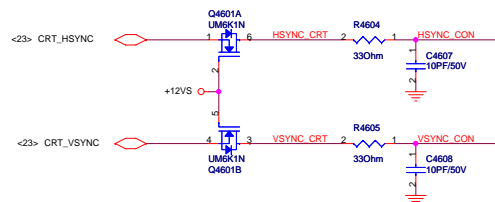
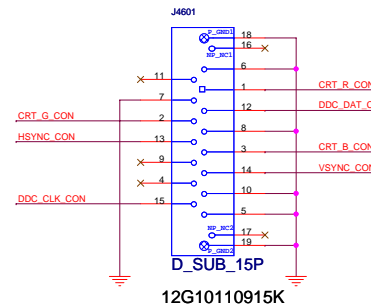
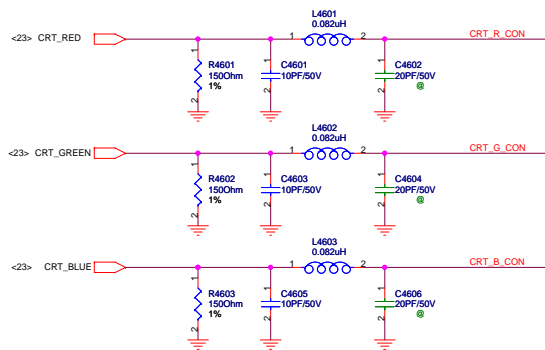



for EMI



CMOS & Int. Mic.

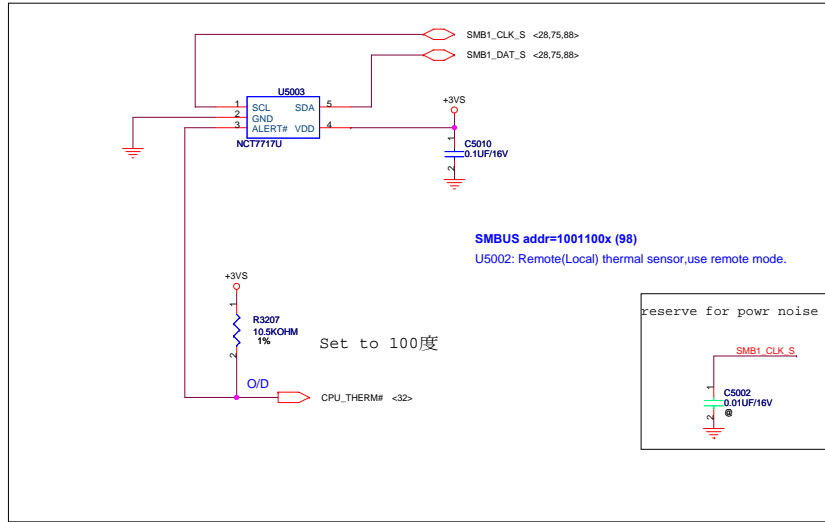




		Title : CRT_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
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CPU Thermal Sensor

change Thermal sensor solution

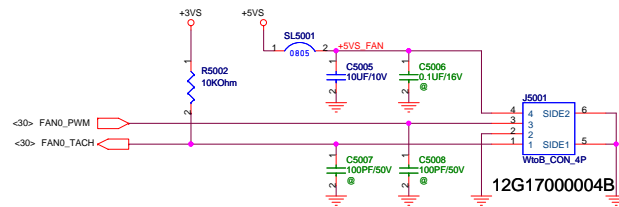


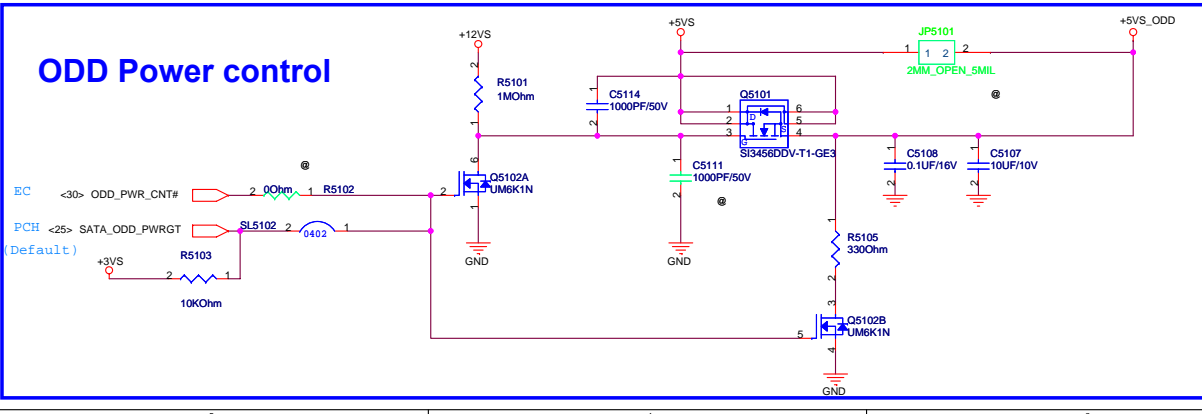
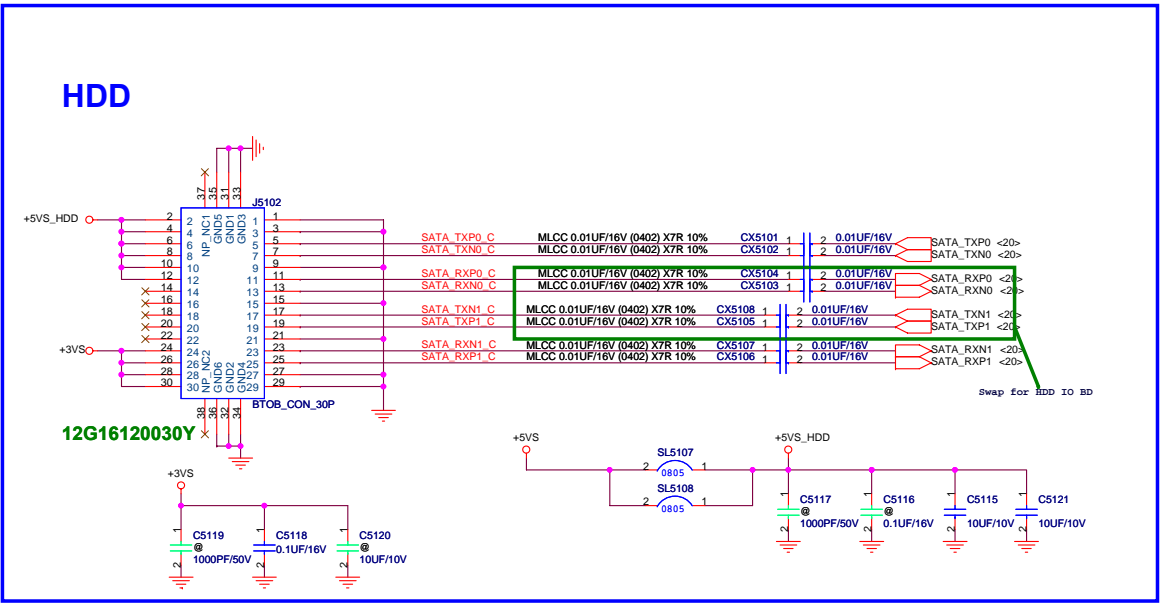
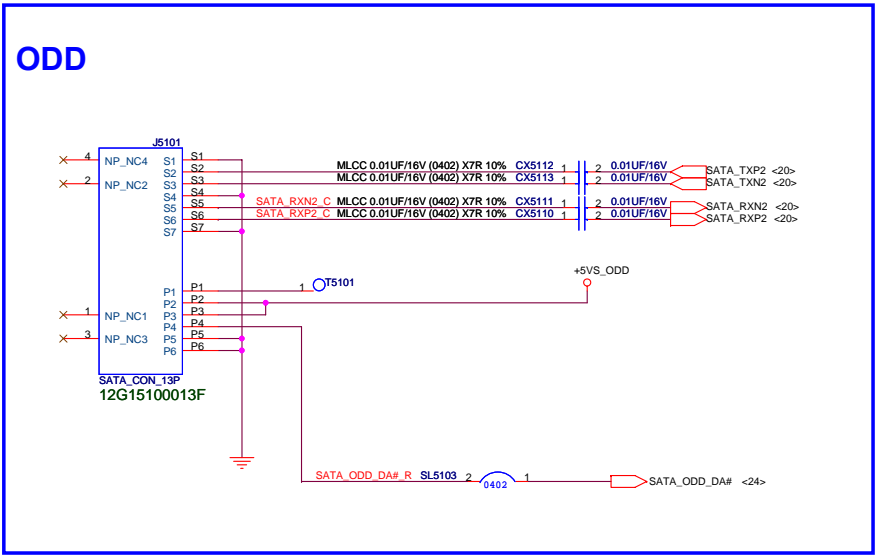
Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

Avoid FSB,Power


DC FAN Control

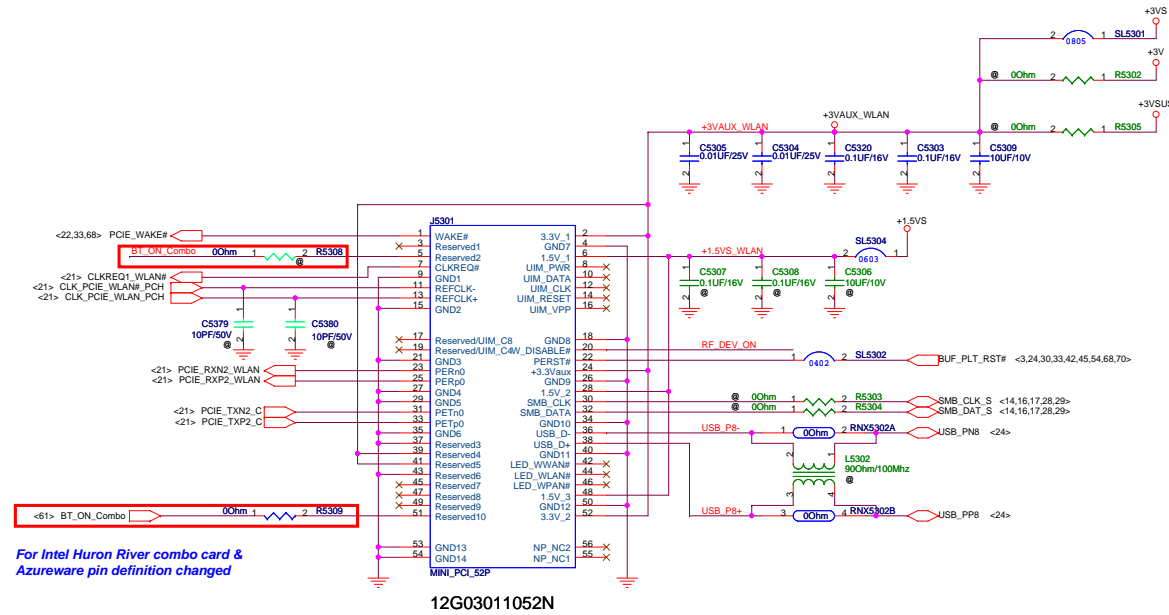




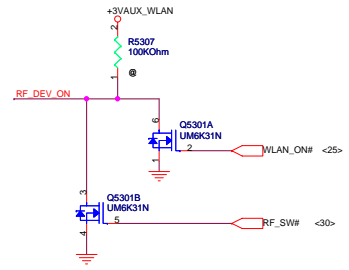
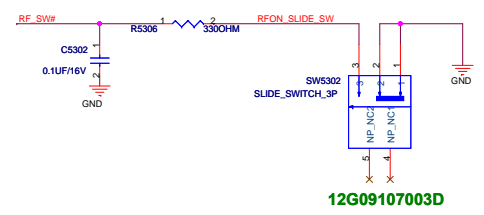
ASUS		Title : XDD_HDD & ODD Conn.
ASUSTeK COMPUTER INC. NB3		Engineer: Wish
Size	Project Name	Rev
Custom	N73Sv	1.0
Date: Wednesday, October 13, 2010		Sheet 51 of 95

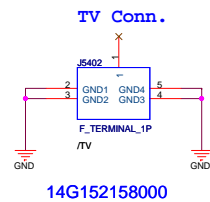
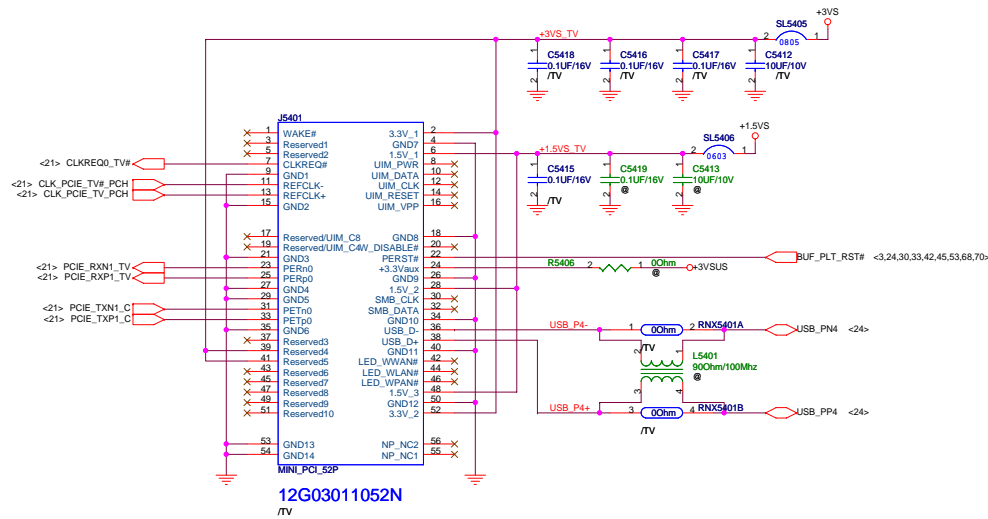
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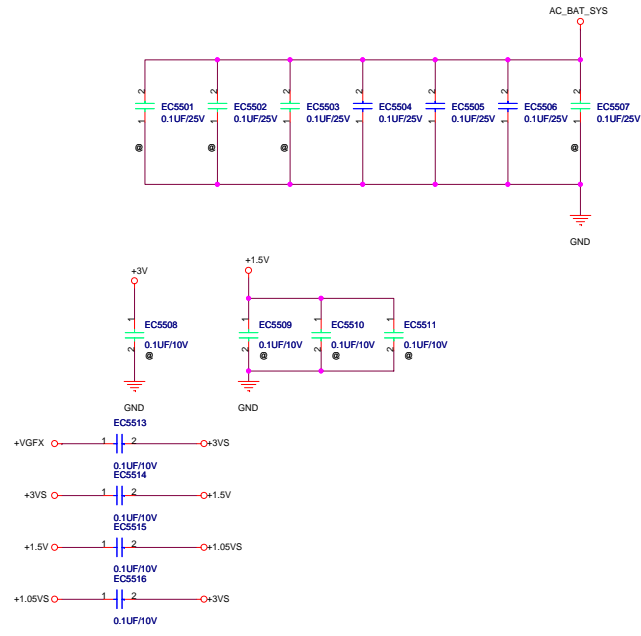
		Title : Empty	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	52 of 95



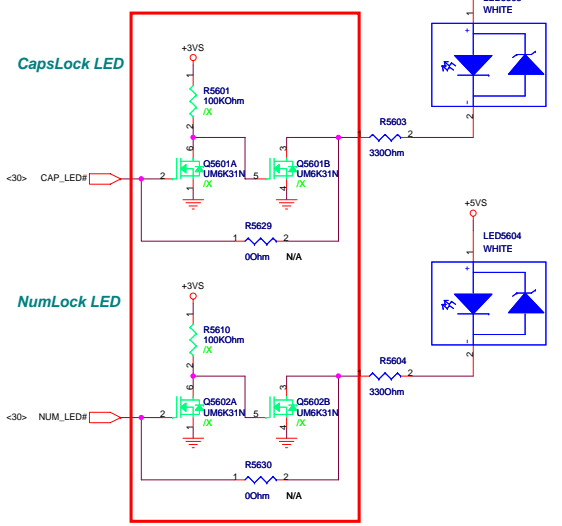
RF SWITCH



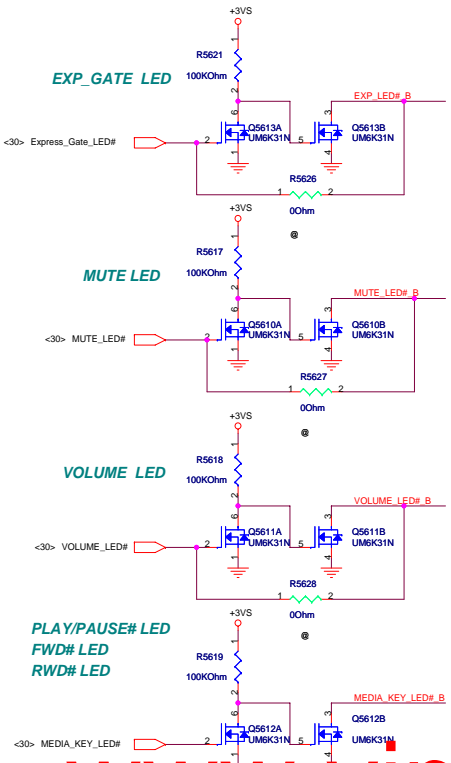
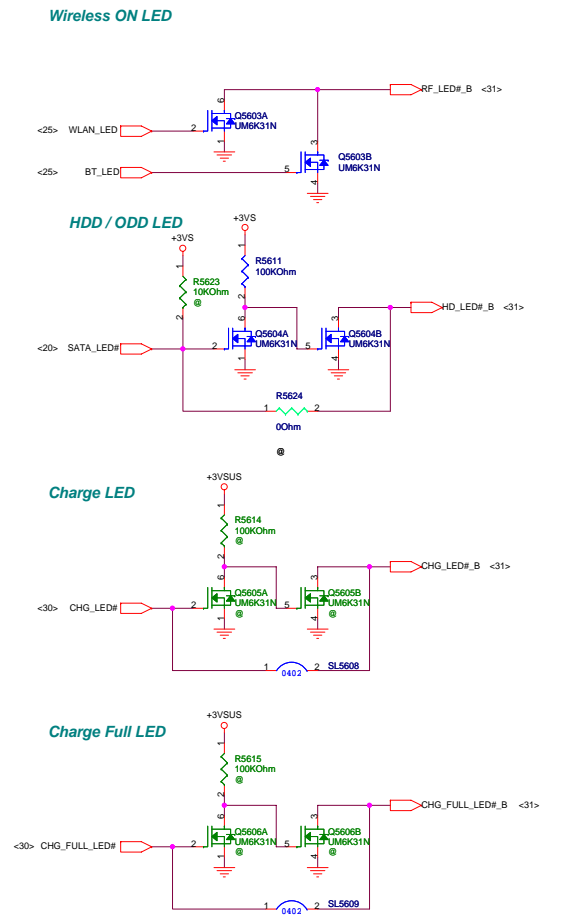
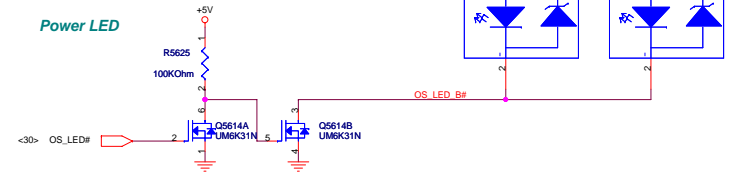
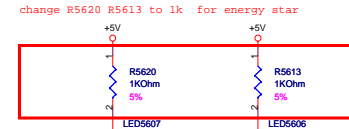
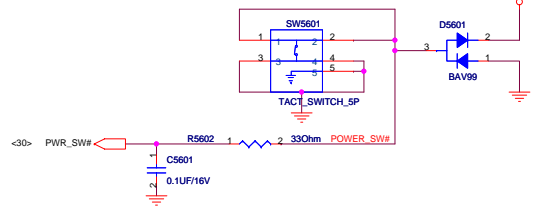
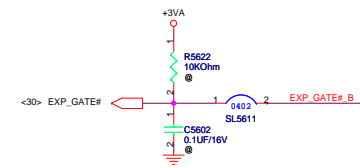
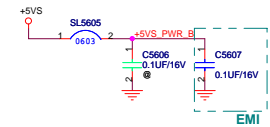
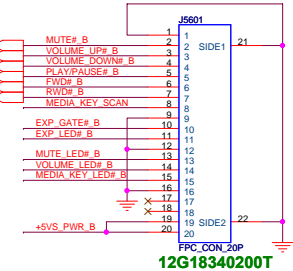
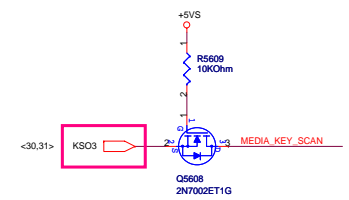
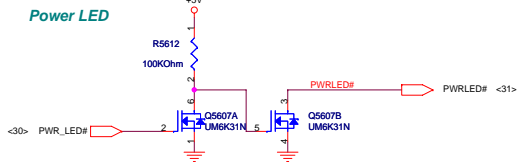




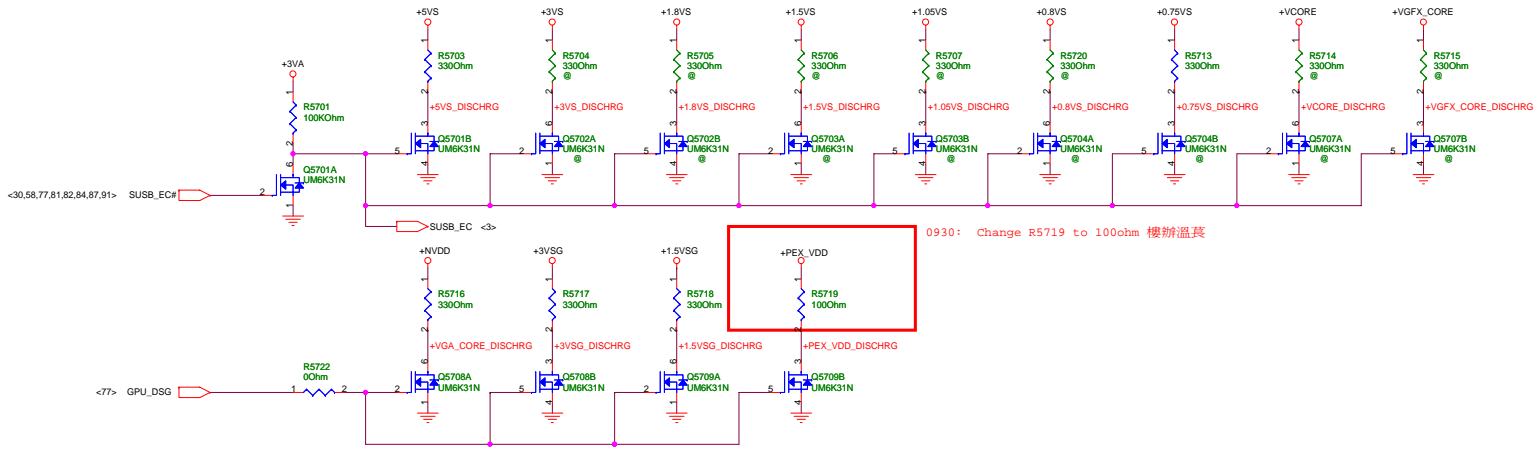
To Touchpad Board



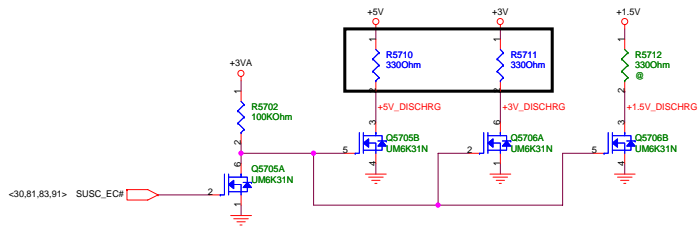
delete dGPU/iGPU LED

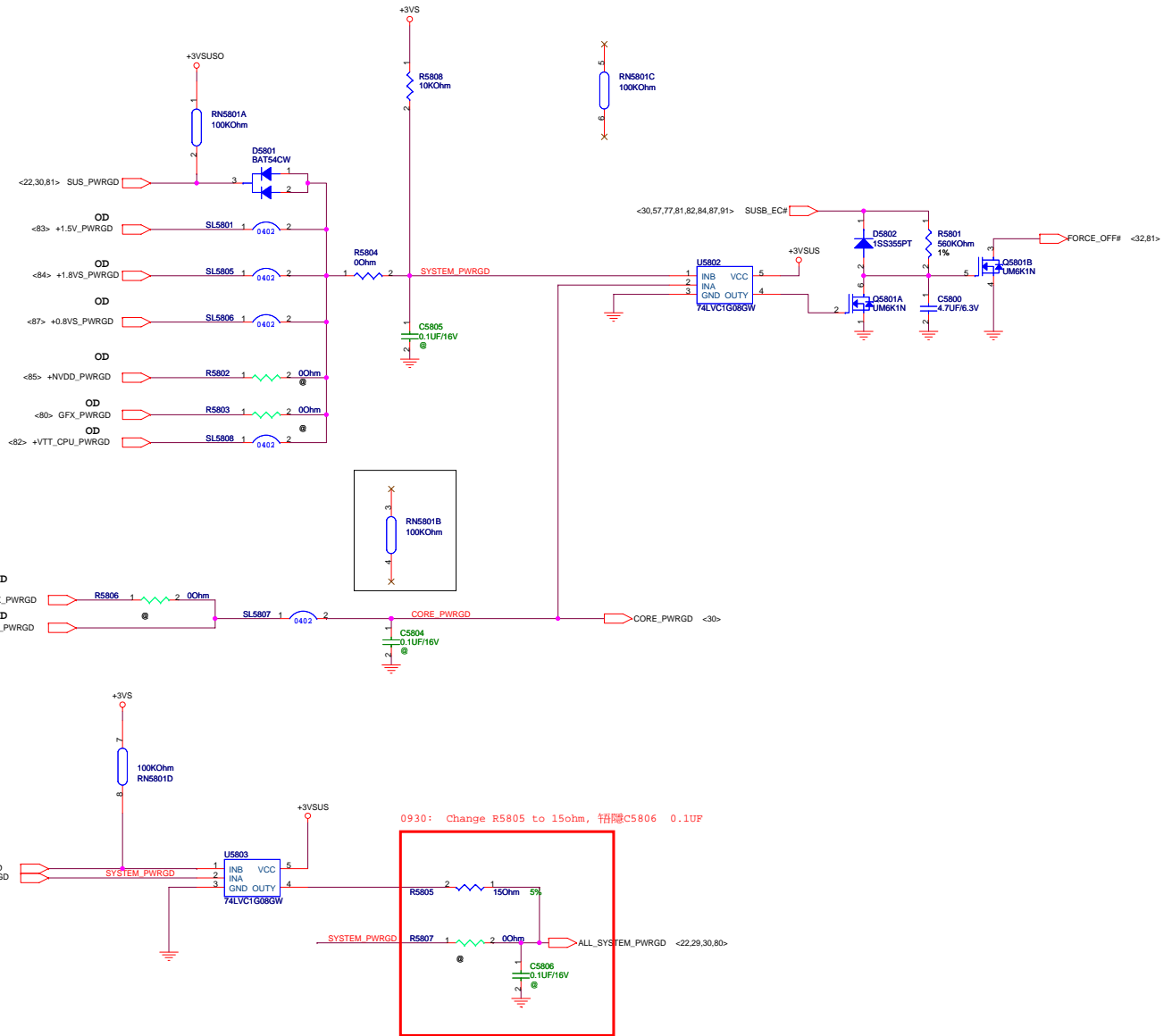


change R5620 R5613 to 1k for energy star



Stuff R5710 and R5711



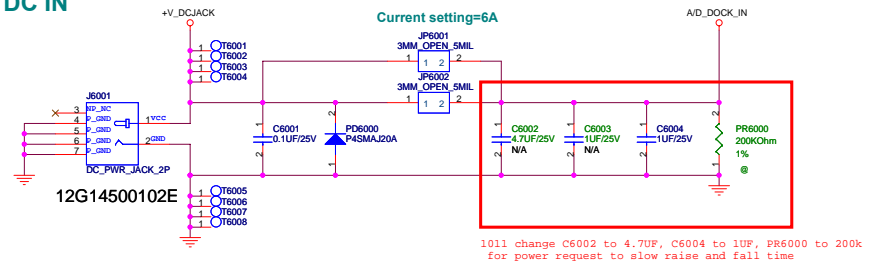


www.vinafix.vn

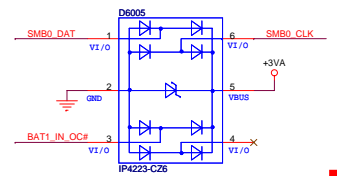
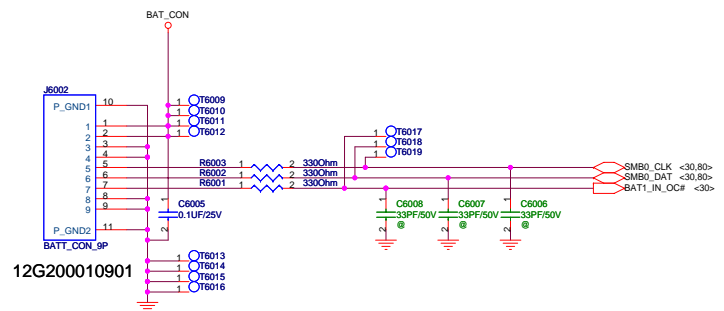
www.vinafix.vn

		Title : Dynamic Vcore Ctrl	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: <i>Wednesday, October 13, 2010</i>		Sheet	59 of 95

DC IN

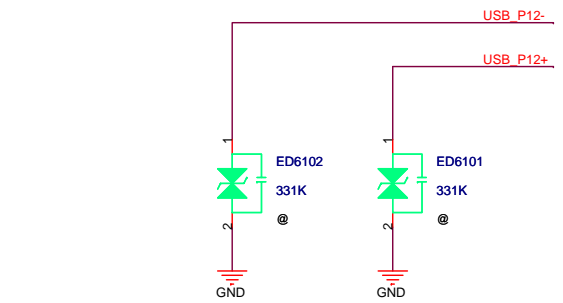


BAT IN

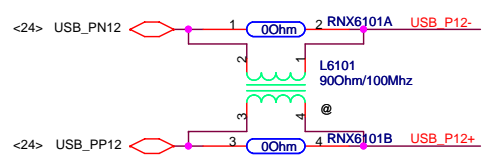
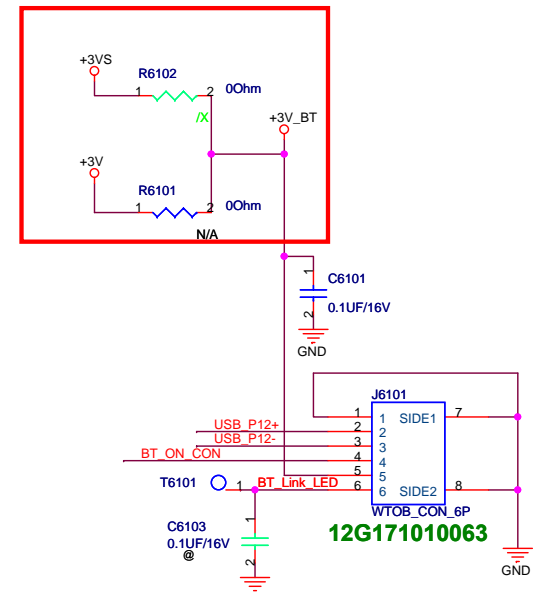


BLUETOOTH

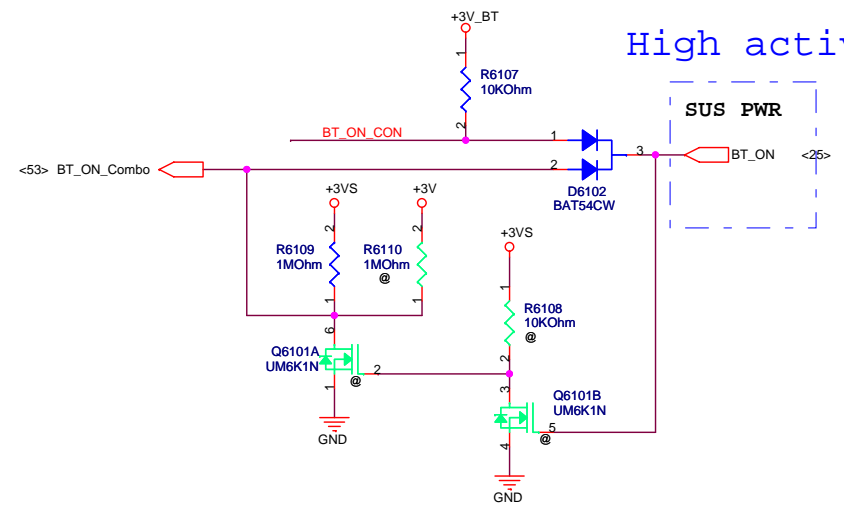
Reserve for EMI



10/12 Reserve R6102 For Energy Satr



High active



		Title : BT_Bluetooth	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size B	Project Name N73Sv	Date: Wednesday, October 13, 2010	Rev 1.0
Date: Wednesday, October 13, 2010		Sheet 61 of 95	

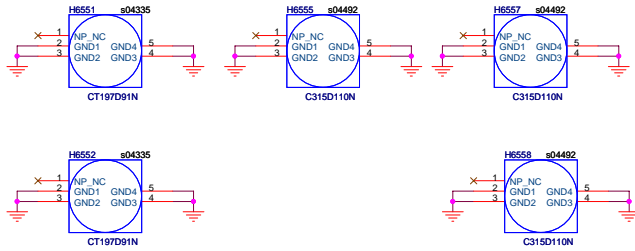
		Title : TPM_****	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	62 of 95

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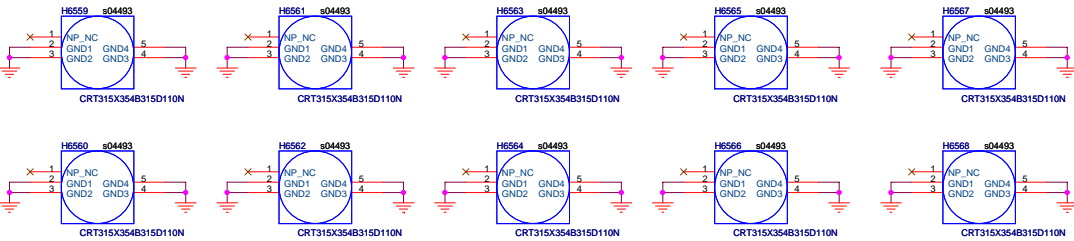
		Title : BAR_****	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
C	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	64 of 95

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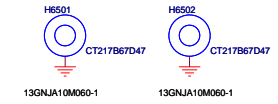
Screw D x 2 for ODD Screw E x 4



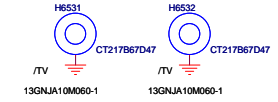
Screw F x 10



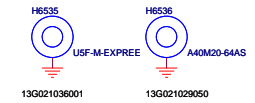
MiniCard (Wifi) Stand-Off HMC



MiniCard (TV) Stand-Off MC



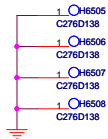
FAN Stand-Off



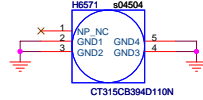
HDD Stand-Off



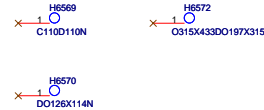
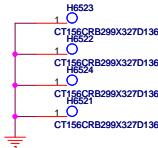
Screw B x 4 CPU Bracket

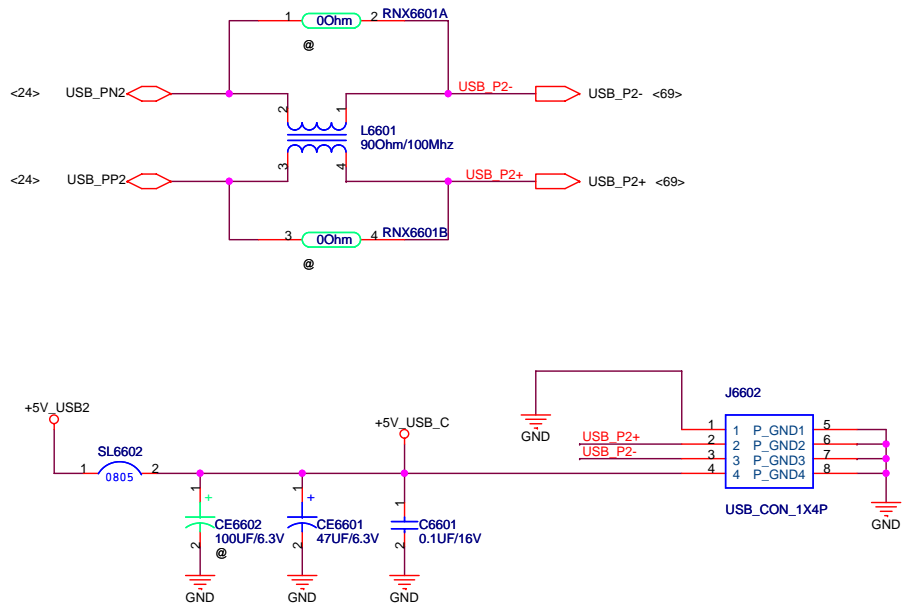


Screw H x 1

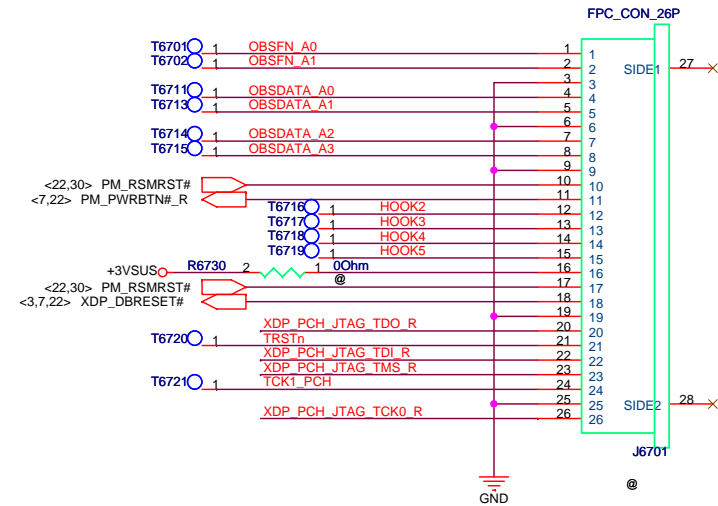
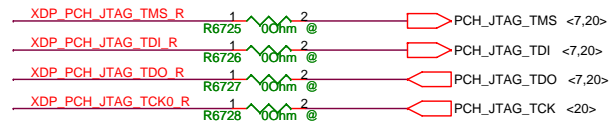


Screw C x 4 GPU Bracket

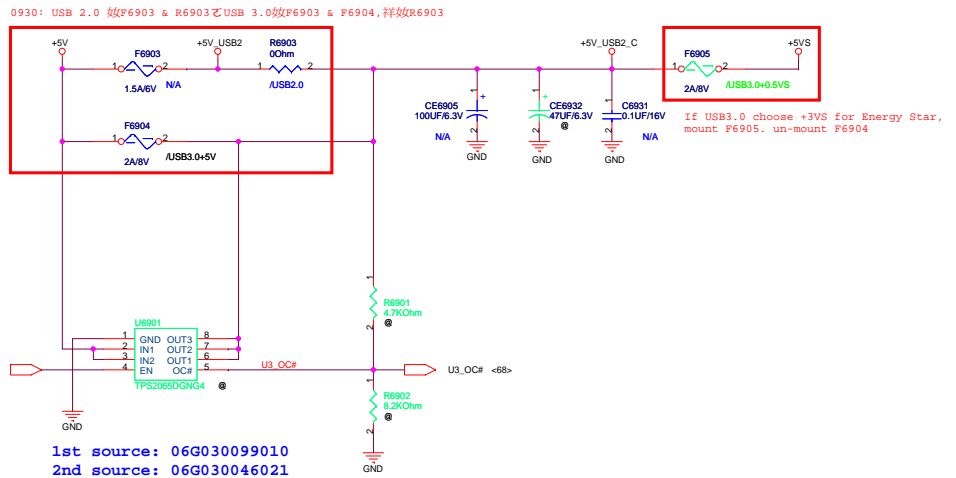
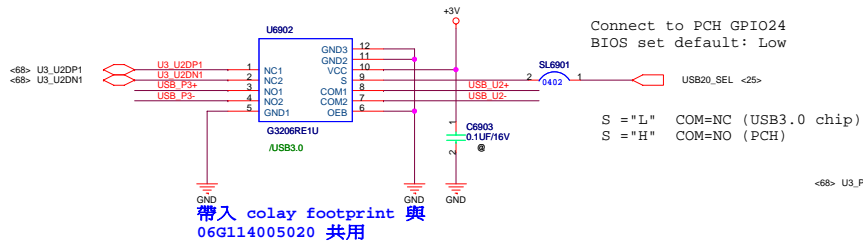




		Title : USB2.0 Port	
ASUSTeK COMPUTER INC. NB3		Engineer: Wish	
Size B	Project Name N73Sv		Rev 1.0
Date: Wednesday, October 13, 2010		Sheet 66 of 95	

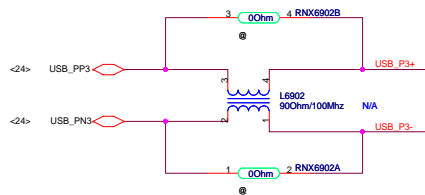


USB ports

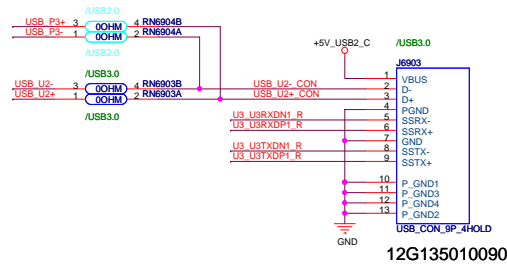
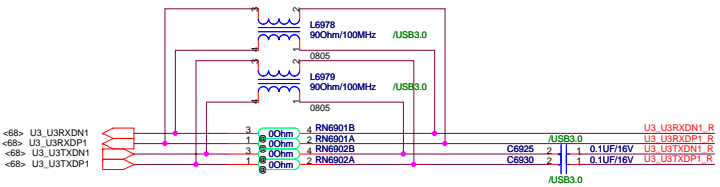


Fresco USB3.0 VBUS Control Circuit

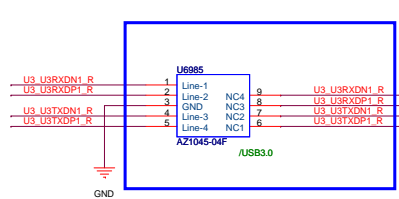
- Follow USB3.0 Logo 認證 (必要條件 : a. S3 Wake up; b. VBUS Control Circuit) 需搭配 Ver. E0 Fresco Chipset IC 才採PWR SW方式上件, 目前(Ver. D1)採Poly Fuse方式上件
1. Unmount R6819,U6901. Mount F6903,R6903,R6904 for Poly Fuse in Ver. D1 Fresco Chipset IC.
 2. Mount R6819,U6901. Unmount F6903,R6903,R6904 for PWR SW in Ver. E0 Fresco Chipset IC.



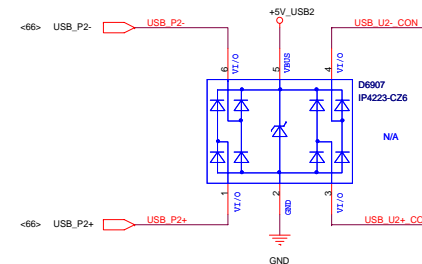
USB3.0 EMI-Protection



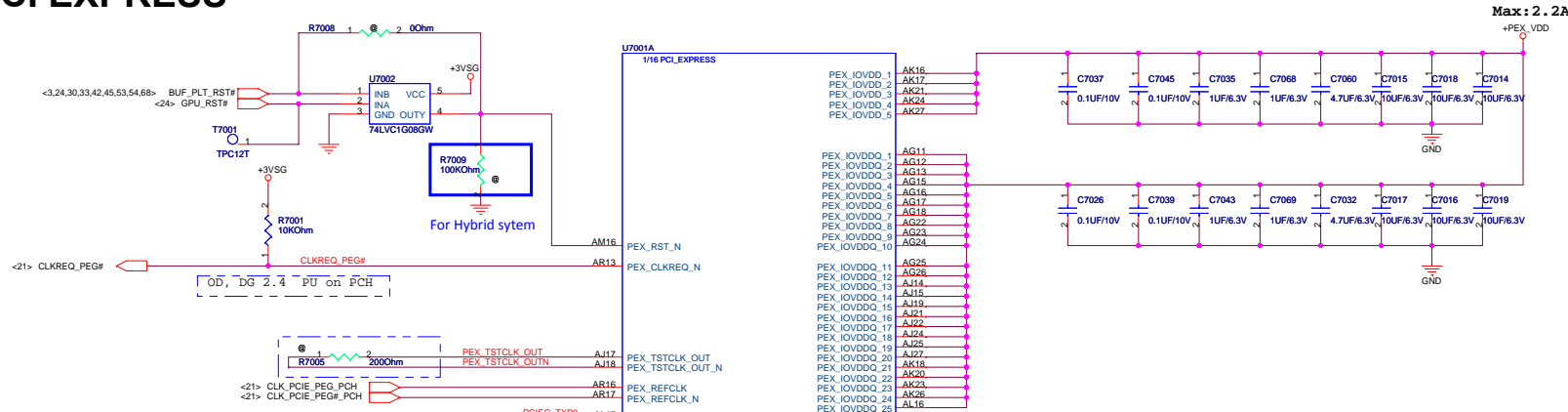
USB3.0/USB 2.0 ESD-Protection



走線請直接由 U1485 穿過至零件另一側之對應 pin
勿成分枝狀走線

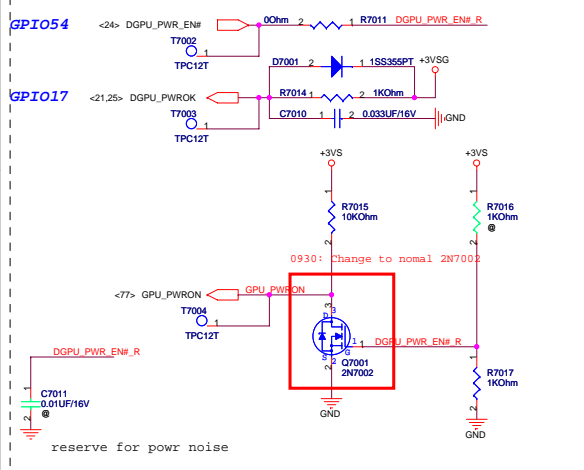


PCI EXPRESS



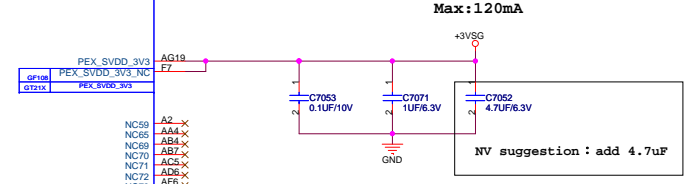
Max: 2.2 A

Control Signal from PCH

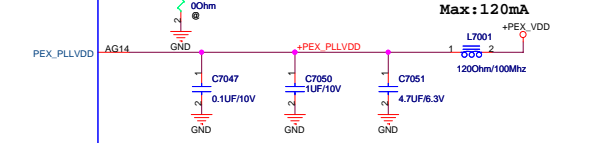
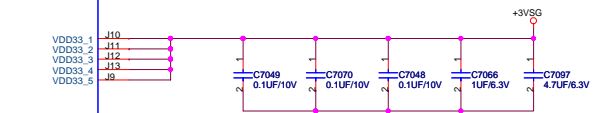


PCIEG_TXP0	AL17	PEX_TX0	AK16
PCIEG_TXN0	AM17	PEX_TX0_N	AK17
PCIEG_RXP0	AP17	PEX_RX0	AK21
PCIEG_RXN0	AN17	PEX_RX0_N	AK22
PCIEG_TXP1	AM18	PEX_TX1	AG12
PCIEG_TXN1	AM19	PEX_TX1_N	AG13
PCIEG_RXP1	AP19	PEX_RX1	AG14
PCIEG_RXN1	AN19	PEX_RX1_N	AG15
PCIEG_TXP2	AL19	PEX_TX2	AG16
PCIEG_TXN2	AK19	PEX_TX2_N	AG17
PCIEG_RXP2	AR19	PEX_RX2	AG18
PCIEG_RXN2	AN20	PEX_RX2_N	AG19
PCIEG_TXP3	AL20	PEX_TX3	AG20
PCIEG_TXN3	AM20	PEX_TX3_N	AG21
PCIEG_RXP3	AP20	PEX_RX3	AG22
PCIEG_RXN3	AN20	PEX_RX3_N	AG23
PCIEG_TXP4	AM21	PEX_TX4	AG24
PCIEG_TXN4	AM22	PEX_TX4_N	AG25
PCIEG_RXP4	AN22	PEX_RX4	AG26
PCIEG_RXN4	AP22	PEX_RX4_N	AG27
PCIEG_TXP5	AL22	PEX_TX5	AG28
PCIEG_TXN5	AK22	PEX_TX5_N	AG29
PCIEG_RXP5	AR22	PEX_RX5	AG30
PCIEG_RXN5	AN23	PEX_RX5_N	AG31
PCIEG_TXP6	AL23	PEX_TX6	AG32
PCIEG_TXN6	AM23	PEX_TX6_N	AG33
PCIEG_RXP6	AP23	PEX_RX6	AG34
PCIEG_RXN6	AN23	PEX_RX6_N	AG35
PCIEG_TXP7	AM24	PEX_TX7	AG36
PCIEG_TXN7	AM25	PEX_TX7_N	AG37
PCIEG_RXP7	AN25	PEX_RX7	AG38
PCIEG_RXN7	AP25	PEX_RX7_N	AG39
PCIEG_TXP8	AL25	PEX_TX8	AG40
PCIEG_TXN8	AK25	PEX_TX8_N	AG41
PCIEG_RXP8	AR25	PEX_RX8	AG42
PCIEG_RXN8	AN26	PEX_RX8_N	AG43
PCIEG_TXP9	AL26	PEX_TX9	AG44
PCIEG_TXN9	AM26	PEX_TX9_N	AG45
PCIEG_RXP9	AP26	PEX_RX9	AG46
PCIEG_RXN9	AN26	PEX_RX9_N	AG47
PCIEG_TXP10	AM27	PEX_TX10	AG48
PCIEG_TXN10	AM28	PEX_TX10_N	AG49
PCIEG_RXP10	AN28	PEX_RX10	AG50
PCIEG_RXN10	AP29	PEX_RX10_N	AG51
PCIEG_TXP11	AL28	PEX_TX11	AG52
PCIEG_TXN11	AK28	PEX_TX11_N	AG53
PCIEG_RXP11	AR28	PEX_RX11	AG54
PCIEG_RXN11	AN29	PEX_RX11_N	AG55
PCIEG_TXP12	AM29	PEX_TX12	AG56
PCIEG_TXN12	AM30	PEX_TX12_N	AG57
PCIEG_RXP12	AN30	PEX_RX12	AG58
PCIEG_RXN12	AP31	PEX_RX12_N	AG59
PCIEG_TXP13	AL30	PEX_TX13	AG60
PCIEG_TXN13	AK30	PEX_TX13_N	AG61
PCIEG_RXP13	AR31	PEX_RX13	AG62
PCIEG_RXN13	AN31	PEX_RX13_N	AG63
PCIEG_TXP14	AM31	PEX_TX14	AG64
PCIEG_TXN14	AM32	PEX_TX14_N	AG65
PCIEG_RXP14	AN32	PEX_RX14	AG66
PCIEG_RXN14	AP33	PEX_RX14_N	AG67
PCIEG_TXP15	AL32	PEX_TX15	AG68
PCIEG_TXN15	AK32	PEX_TX15_N	AG69
PCIEG_RXP15	AR34	PEX_RX15	AG70
PCIEG_RXN15	AN34	PEX_RX15_N	AG71

PCIEB_RXN15[0]	C7054	1	2	0.1UF/10V	PCIEG_TXN15
PCIEB_RXP15[0]	C7054	1	2	0.1UF/10V	PCIEG_TXP15
PCIEB_RXN14[0]	C7086	1	2	0.1UF/10V	PCIEG_TXN14
PCIEB_RXP14[0]	C7086	1	2	0.1UF/10V	PCIEG_TXP14
PCIEB_RXN13[0]	C7089	1	2	0.1UF/10V	PCIEG_TXN13
PCIEB_RXP13[0]	C7089	1	2	0.1UF/10V	PCIEG_TXP13
PCIEB_RXN12[0]	C7082	1	2	0.1UF/10V	PCIEG_TXN12
PCIEB_RXP12[0]	C7082	1	2	0.1UF/10V	PCIEG_TXP12
PCIEB_RXN11[0]	C7083	1	2	0.1UF/10V	PCIEG_TXN11
PCIEB_RXP11[0]	C7083	1	2	0.1UF/10V	PCIEG_TXP11
PCIEB_RXN10[0]	C7057	1	2	0.1UF/10V	PCIEG_TXN10
PCIEB_RXP10[0]	C7057	1	2	0.1UF/10V	PCIEG_TXP10
PCIEB_RXN9[0]	C7055	1	2	0.1UF/10V	PCIEG_TXN9
PCIEB_RXP9[0]	C7055	1	2	0.1UF/10V	PCIEG_TXP9
PCIEB_RXN8[0]	C7056	1	2	0.1UF/10V	PCIEG_TXN8
PCIEB_RXP8[0]	C7056	1	2	0.1UF/10V	PCIEG_TXP8
PCIEB_RXN7[0]	C7065	1	2	0.1UF/10V	PCIEG_TXN7
PCIEB_RXP7[0]	C7065	1	2	0.1UF/10V	PCIEG_TXP7
PCIEB_RXN6[0]	C7076	1	2	0.1UF/10V	PCIEG_TXN6
PCIEB_RXP6[0]	C7076	1	2	0.1UF/10V	PCIEG_TXP6
PCIEB_RXN5[0]	C7082	1	2	0.1UF/10V	PCIEG_TXN5
PCIEB_RXP5[0]	C7082	1	2	0.1UF/10V	PCIEG_TXP5
PCIEB_RXN4[0]	C7081	1	2	0.1UF/10V	PCIEG_TXN4
PCIEB_RXP4[0]	C7081	1	2	0.1UF/10V	PCIEG_TXP4
PCIEB_RXN3[0]	C7084	1	2	0.1UF/10V	PCIEG_TXN3
PCIEB_RXP3[0]	C7084	1	2	0.1UF/10V	PCIEG_TXP3
PCIEB_RXN2[0]	C7096	1	2	0.1UF/10V	PCIEG_TXN2
PCIEB_RXP2[0]	C7096	1	2	0.1UF/10V	PCIEG_TXP2
PCIEB_RXN1[0]	C7075	1	2	0.1UF/10V	PCIEG_TXN1
PCIEB_RXP1[0]	C7075	1	2	0.1UF/10V	PCIEG_TXP1
PCIEB_RXN0[0]	C7087	1	2	0.1UF/10V	PCIEG_TXN0
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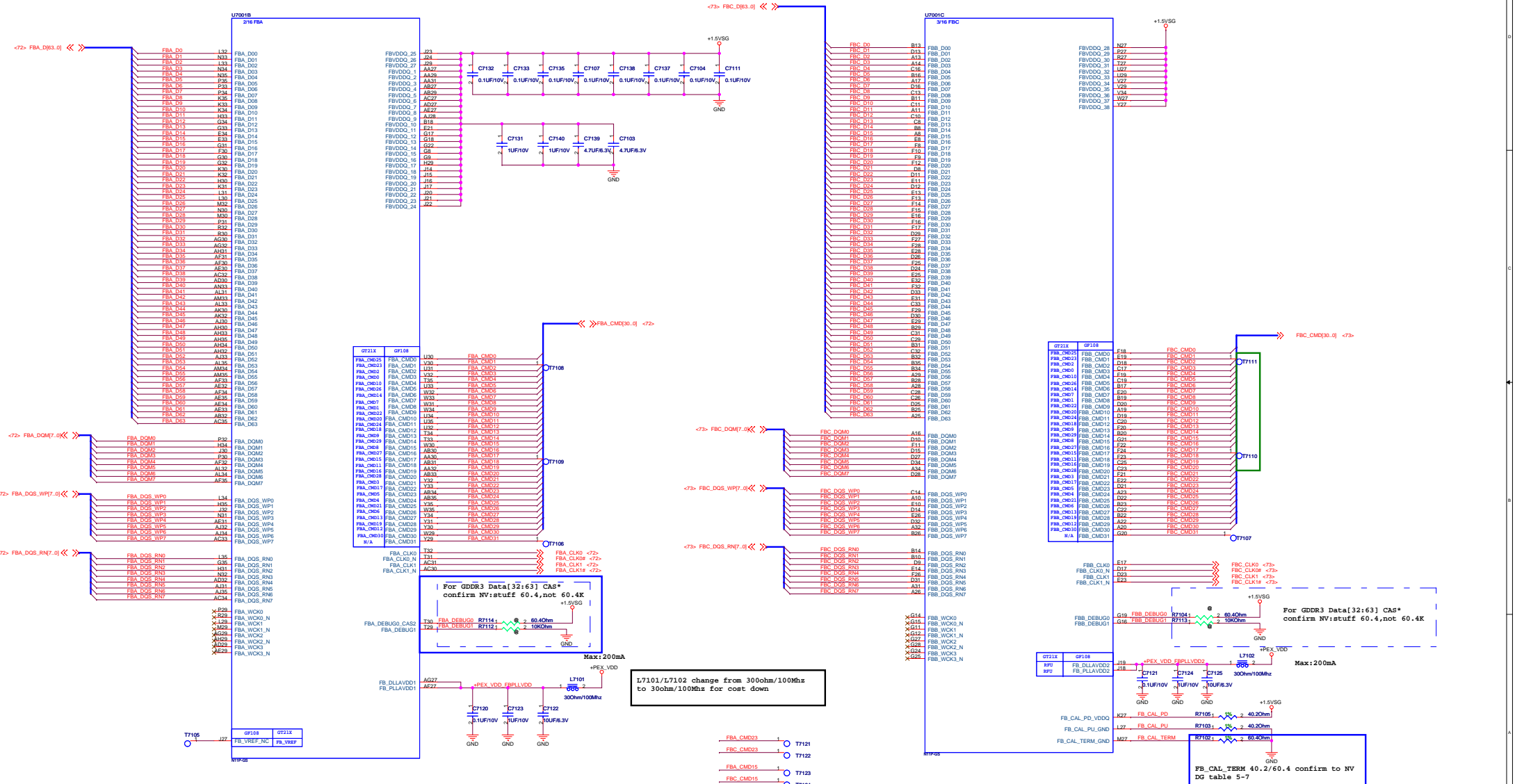
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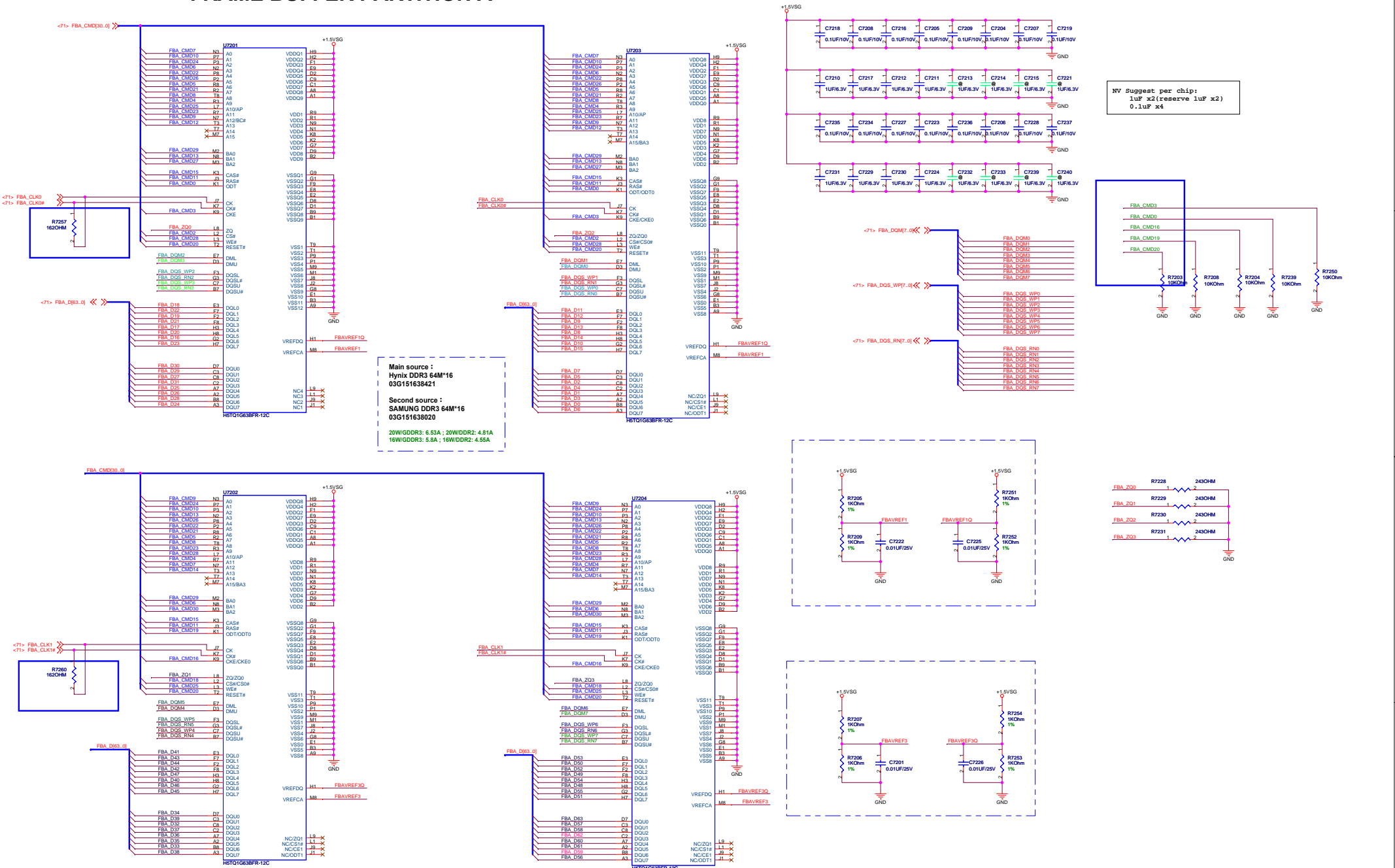
Max: 120mA

GPU MEMORY INTERFACE: PARTITION A

GPU MEMORY INTERFACE: PARTITION C

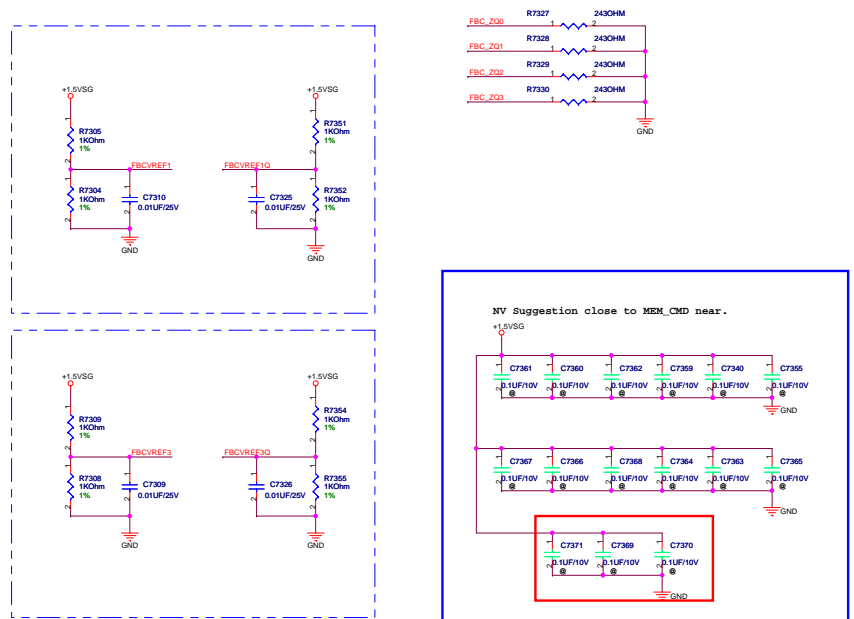
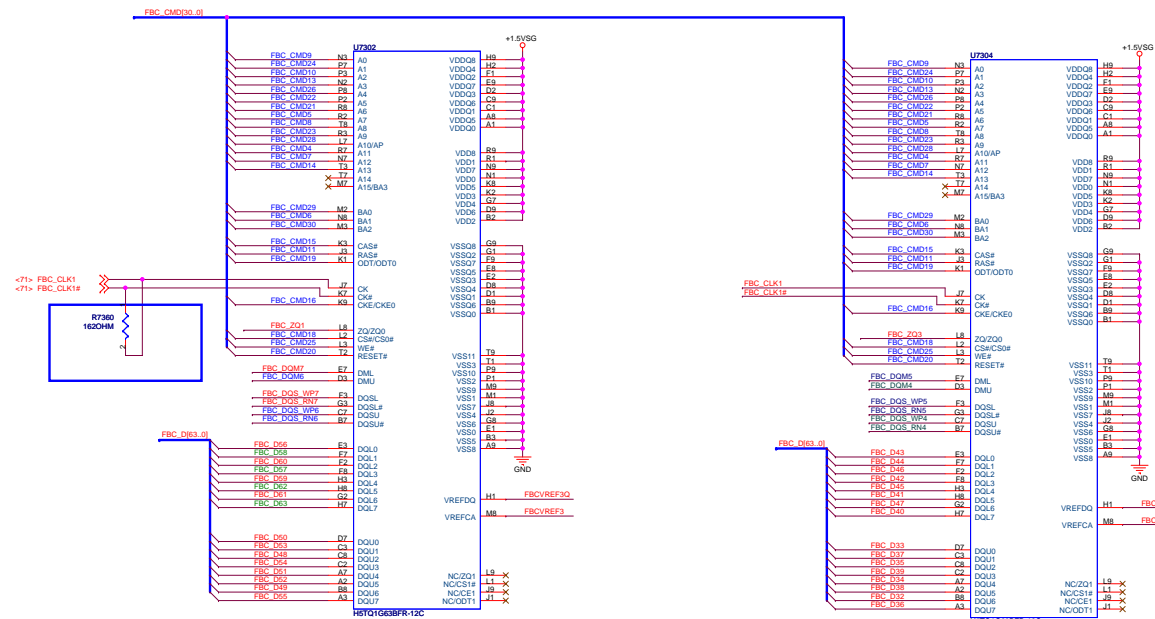
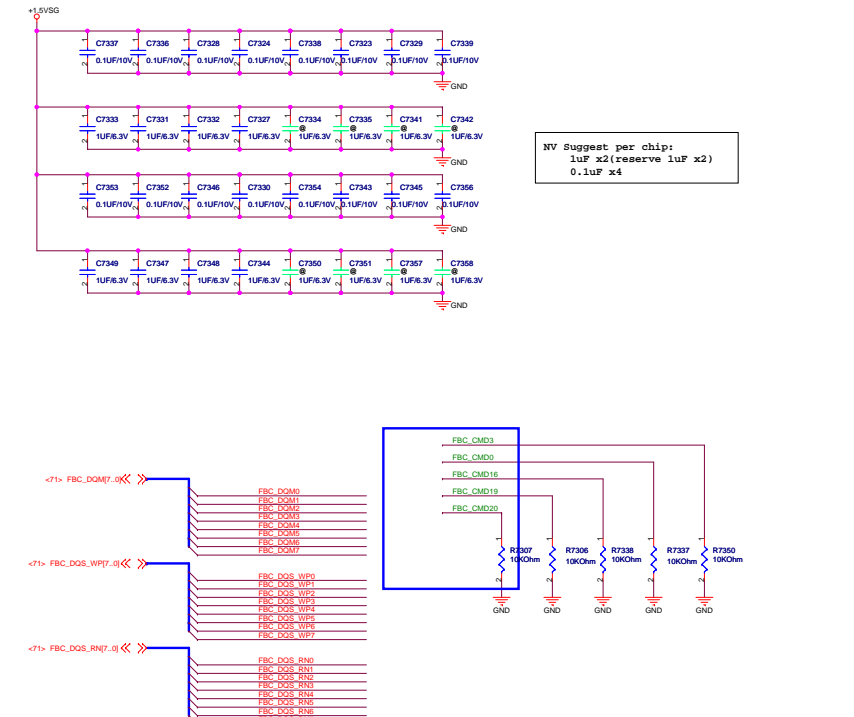
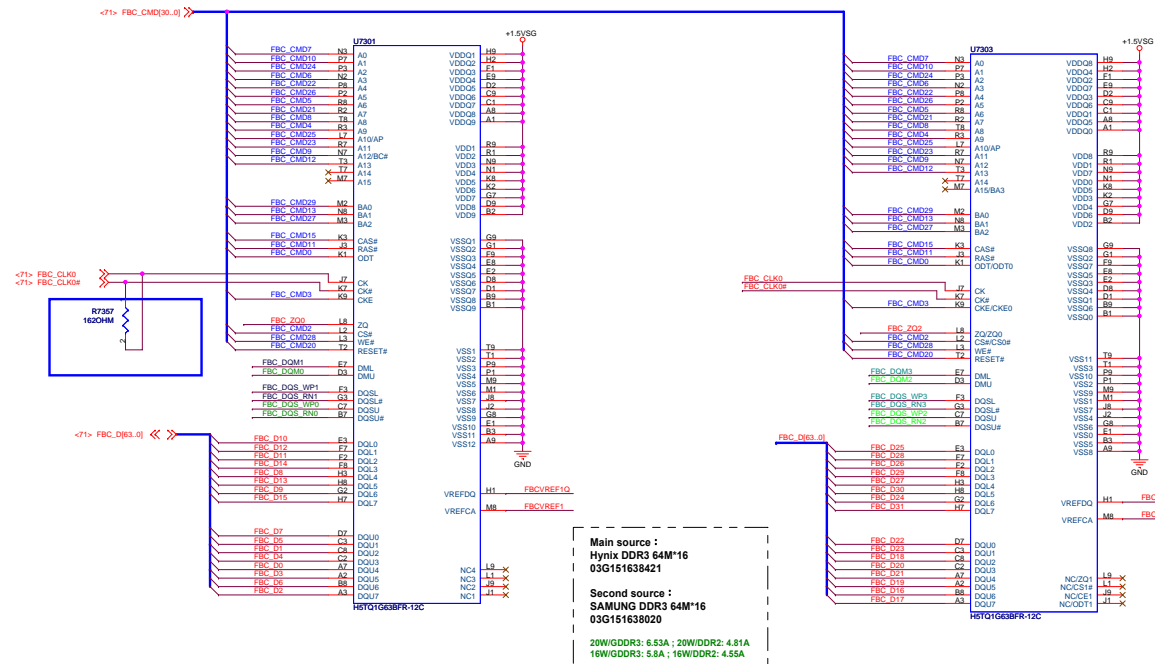


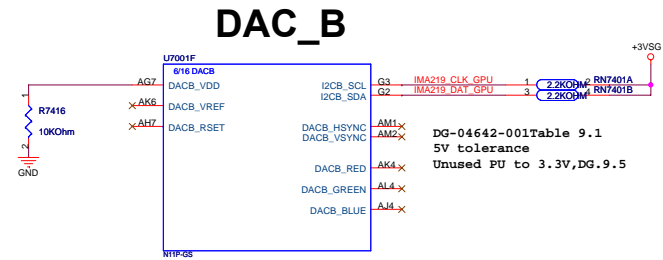
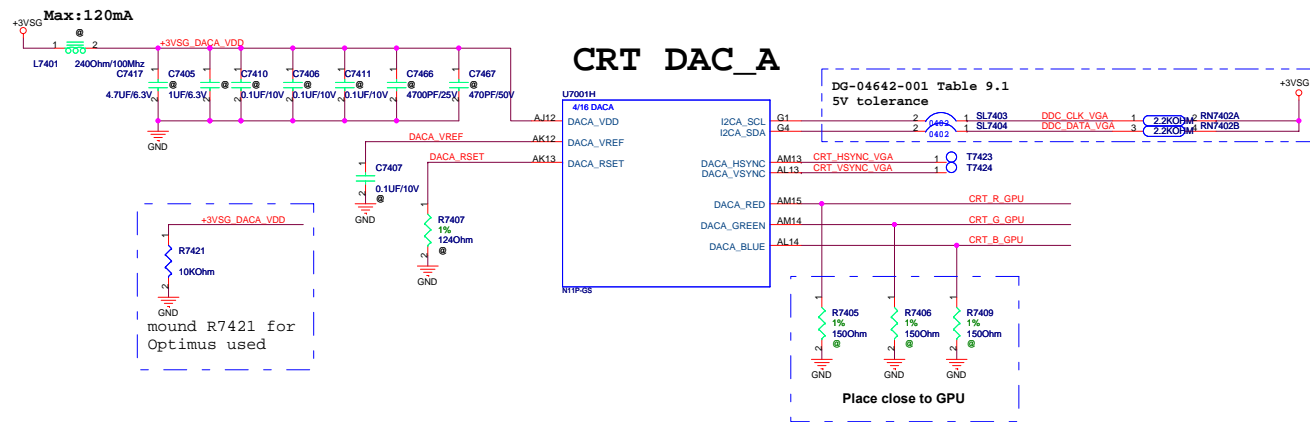
FRAME BUFFER PARTITION A



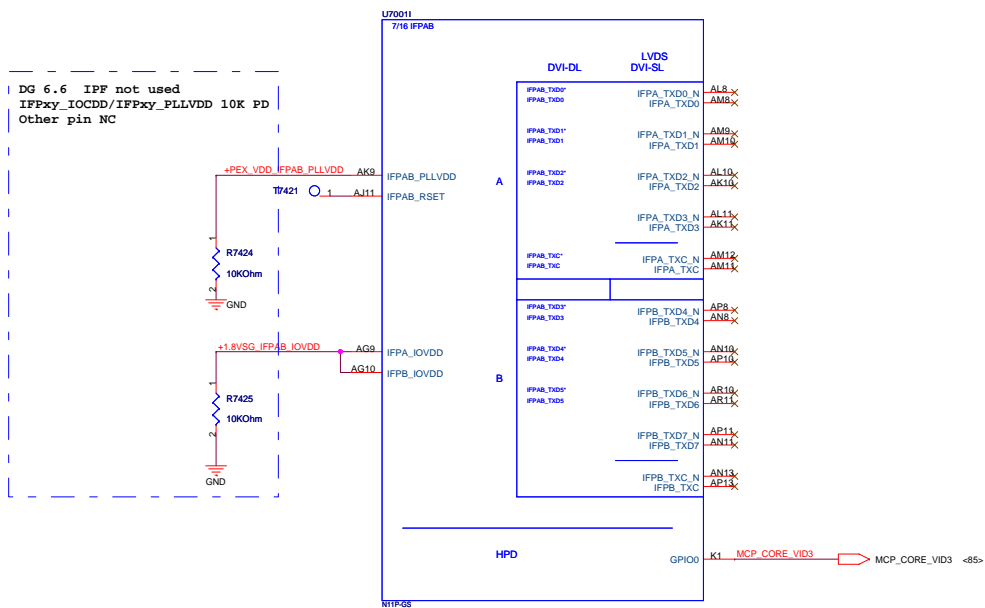
NV Suggest per chip:
1uF x2 (reserve 1uF x2)
0.1uF x4

FRAME BUFFER PARTITION C

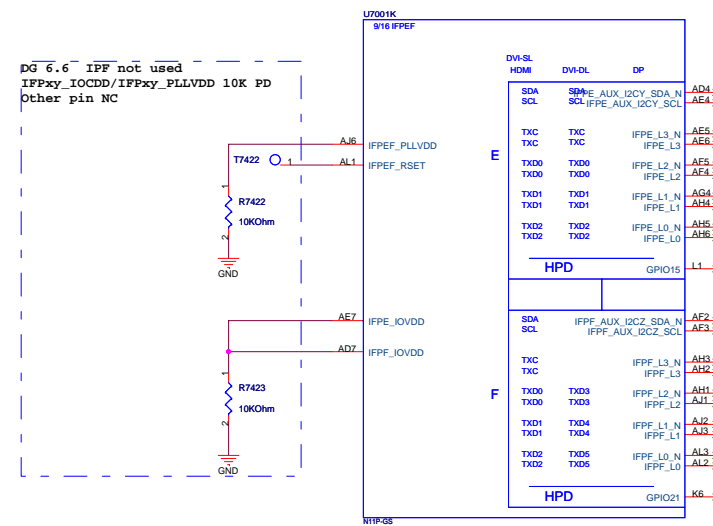




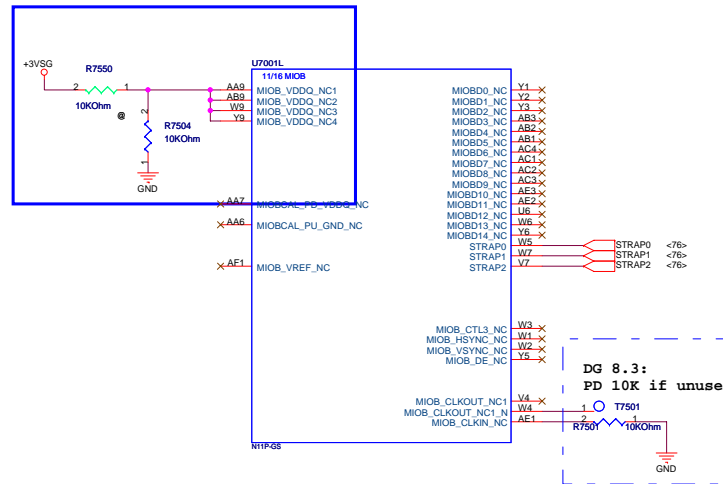
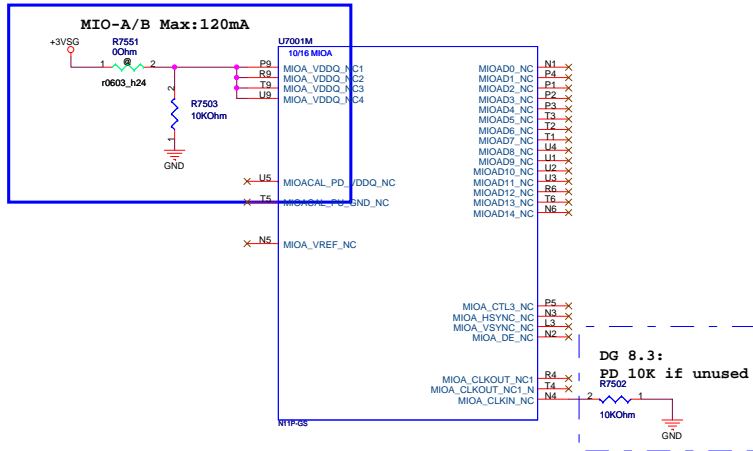
LVDS



IFP_E/F



MIO-A/B Max:120mA



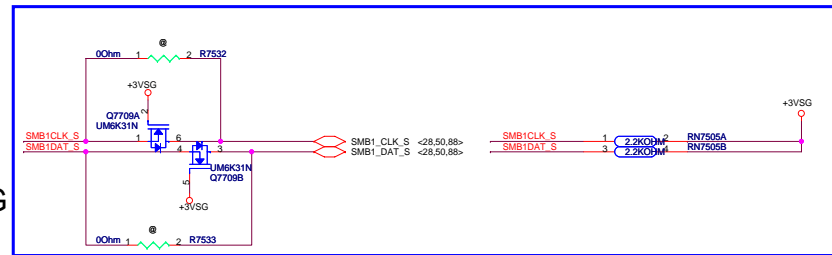
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	IFPC HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID 0
6	OUT	N/A	NVVD VID 1
7	OUT	N/A	NVVD VID 2
8	I/O	LOW	OVER THERMAL
9	I/O	LOW	THERMAL ALERT
10	OUT	N/A	FBVREF SELECT
11	I/O	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	MEM_VID/PWR Control
14	OUT	N/A	PWR Control

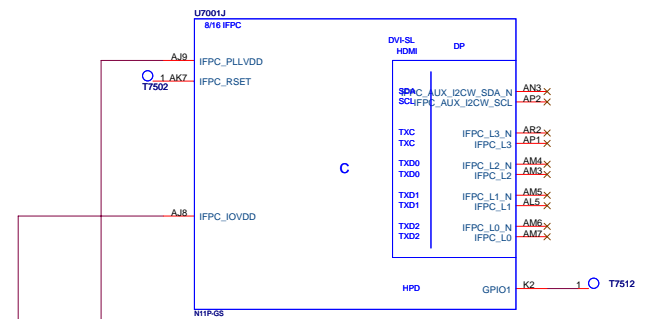
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
15	IN	N/A	IFPE HOTPLUG (HDMI)
16	OUT	N/A	FAN PWM CONTROL
17	IN	N/A	RESERVED
18	IN	N/A	RESERVED
19	IN	N/A	IFPD HOTPLUG
20	IN	N/A	RESERVED
21	IN	N/A	IFPF HOTPLUG
22	IN	N/A	SLI Swap Ready Signal
23	I/O	N/A	STEREO

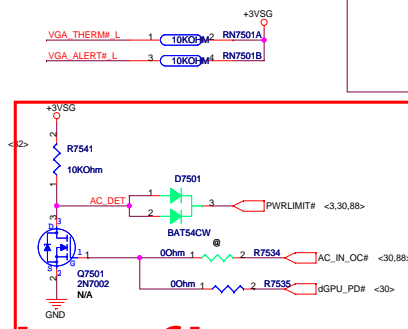
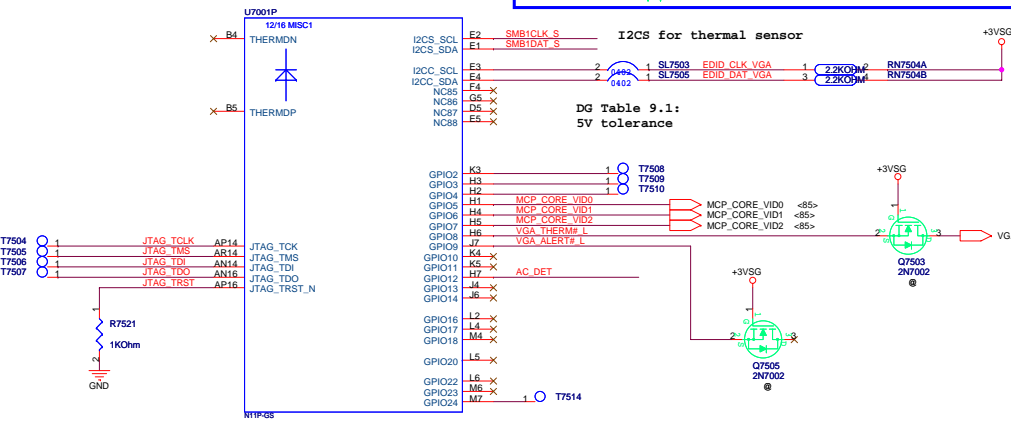
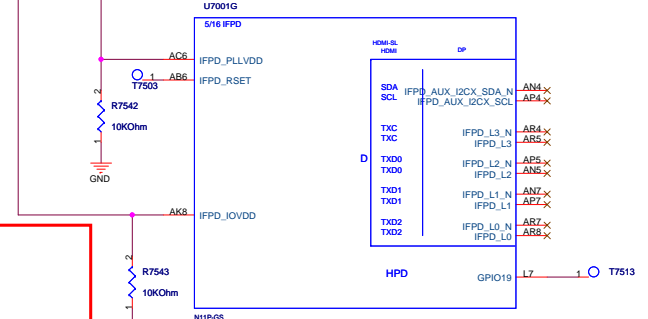
GPIO, TEMP SENSOR, JTAG I2C ADDRESS: 0x9AH

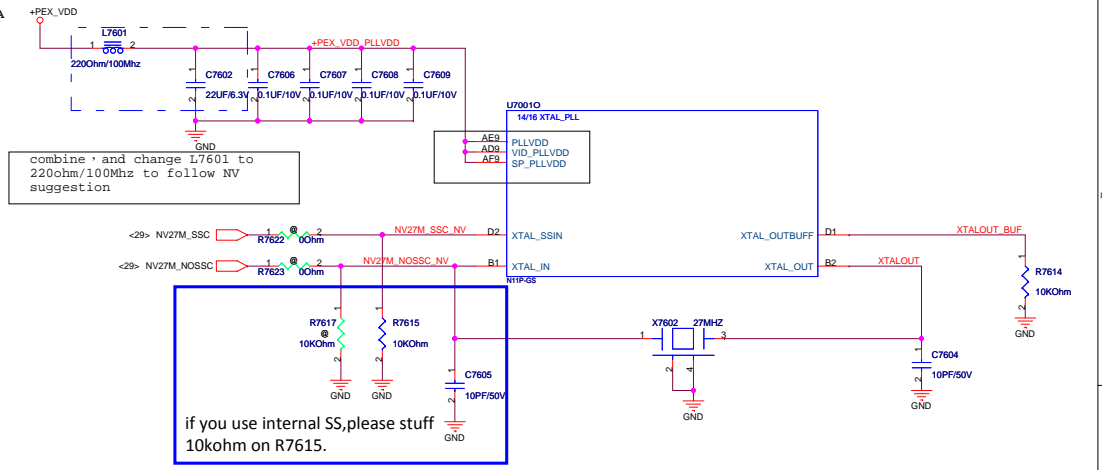
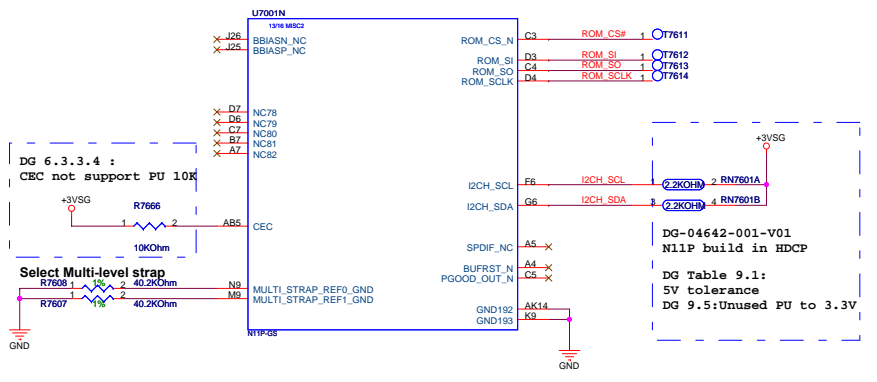


HDMI(link C)

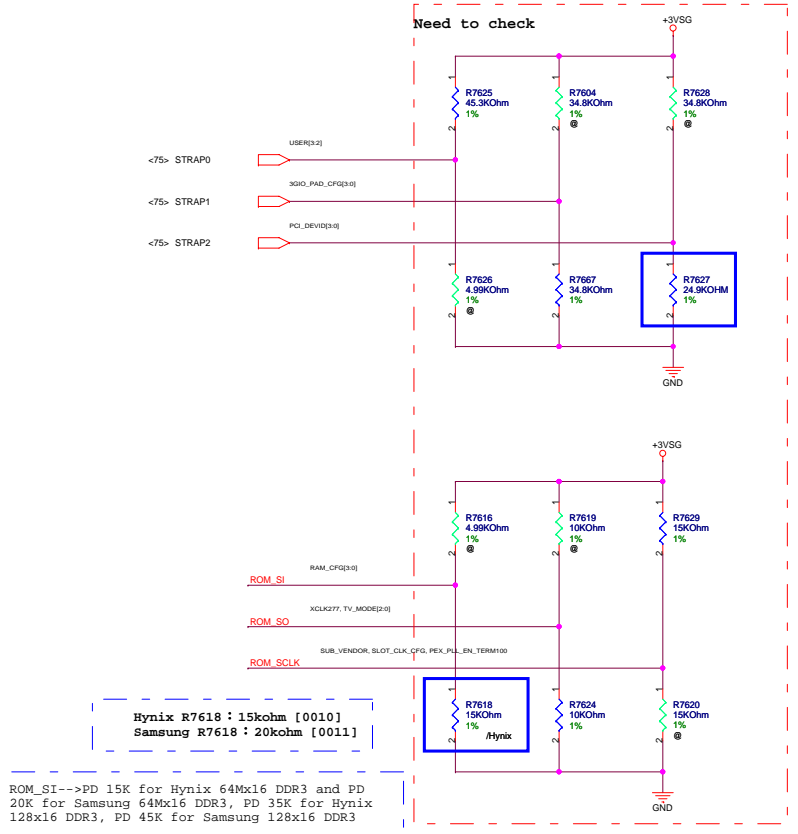


DVI(link D)





STRAPPING OPTIONS



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0

STRAP1

STRAP2

ROM_SO

ROM_SI

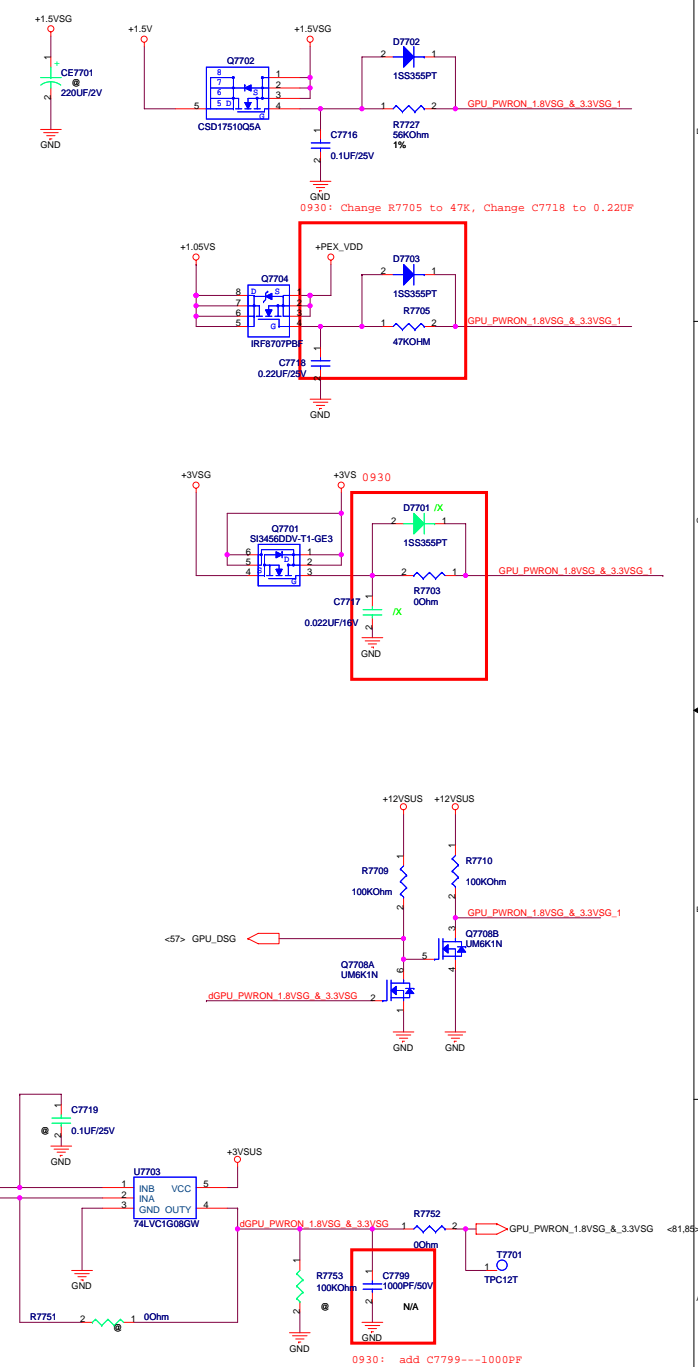
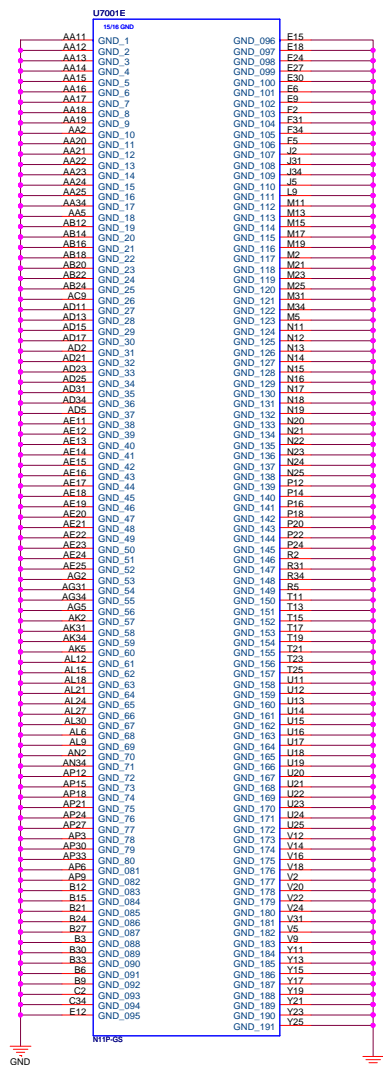
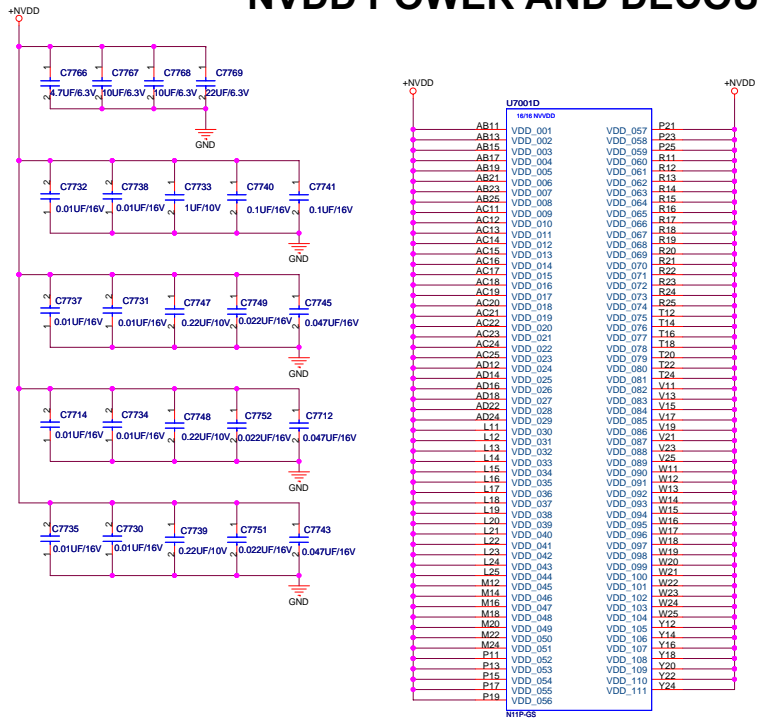
ROM_SCLK

USER_BIT0	
USER_BIT1	
USER_BIT2	
USER_BIT3	
3GIO_PADCFG_LUT_ADR0	
3GIO_PADCFG_LUT_ADR1	0x0: Desktop default (normal swing) - 5k PD 0x1: Mobile default (low swing) - 10k PD
3GIO_PADCFG_LUT_ADR2	
3GIO_PADCFG_LUT_ADR3	acc. to /hw/tesla_g98/manuals/dev_ext_devices.ref
PCI_DEVID_0	all 4 bits set by HW strapping
PCI_DEVID_1	0x0A35 : 30K ohm PD (N11P-GV1)
PCI_DEVID_2	
PCI_DEVID_3	
VGA_DEVICE	0:3D DEVICE 1:VGA DEVICE(default)
SMB_ALT_ADDR	0:0x9E(default) 0x1=10K PD
FB_OBAR_SIZE	0:256M(default)
XCLK_417	0: 277MHZ(Default)
RAM_CFG_0	1GB (8pcs.64Mx16)
RAM_CFG_1	RAM_CFG[3:0] Definitions
RAM_CFG_2	
RAM_CFG_3	
PEX_PLL_EN_TERM	0: Default
SLOT_CLK_CONFIG	1: GPU and MCH COMMON REFCLK 35K PU
SUB_VENDOR	0: VBIOS ROM is not present, default '1'
PCI_DEVID_4	0: 0x0A28(PCDEVID[4]=0) for MP, 0x0A3D(PCDEVID[4]=1) for ER


ROM_SI-->PD 15K for Hynix 64Mx16 DDR3 and PD 20K for Samsung 64Mx16 DDR3, PD 35K for Hynix 128x16 DDR3, PD 45K for Samsung 128x16 DDR3

1. N11P-GS->Device ID: 0x0DF0, please PD 5K for STRAP2, and PU 15K for ROM_SCLK
2. N12P-GS->Device ID: 0x0DF4, please PD 25K for STRAP2, and PU 15K for ROM_SCLK
3. N12P-GV->Device ID: TBD

NVDD POWER AND DECOUPLING NVDD GROUND



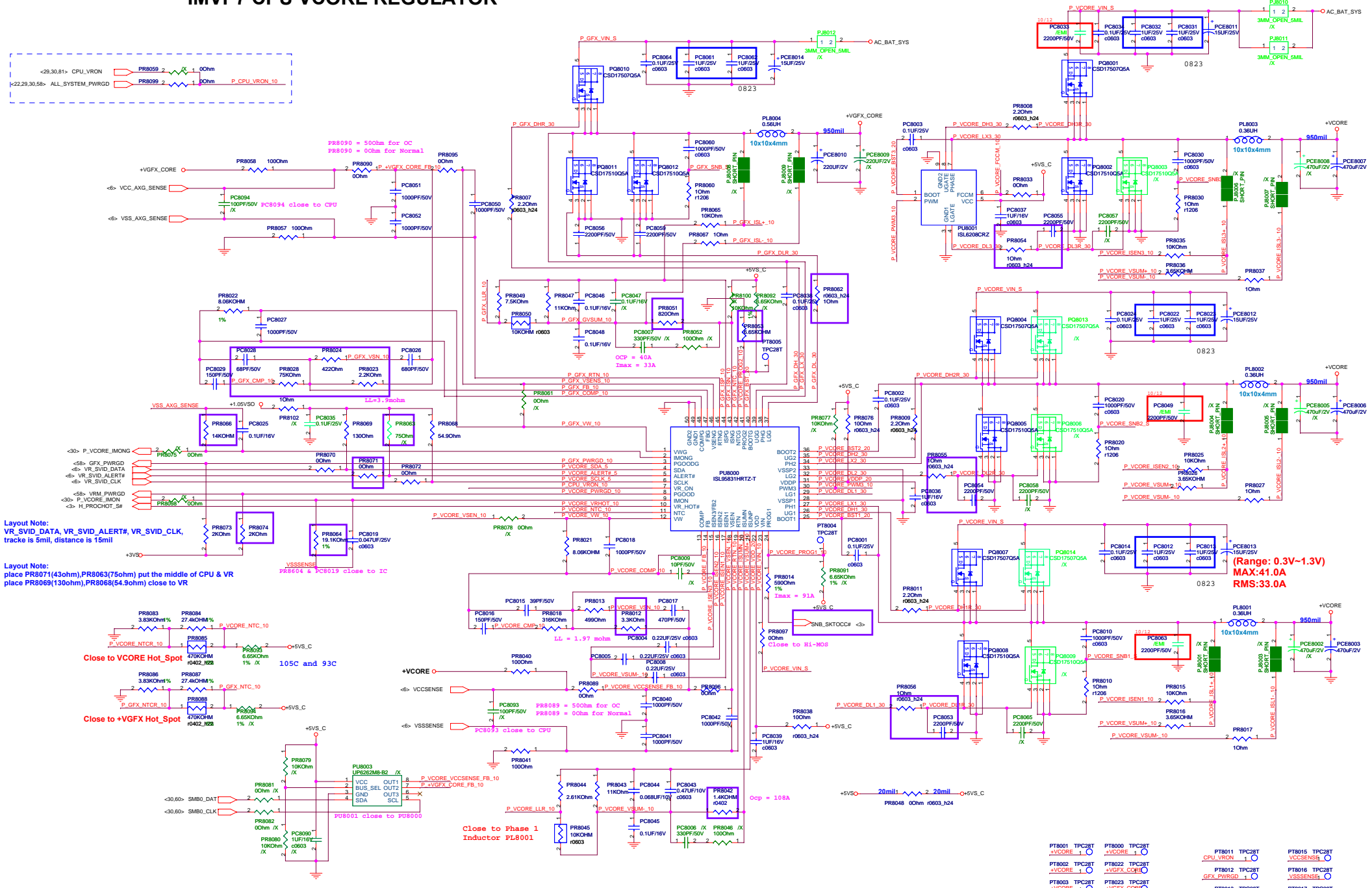


		Title : **	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>Wish</i>	
Size	Project Name	Rev	
Custom	N73Sv	1.0	
Date: Wednesday, October 13, 2010		Sheet	78 of 95

Rev	Date	Description
1.1	2010/08	<p>(1)Page3 & 20 & 70 : CPU socket P/N change to 12G011909893; PCH P/N as 02G010027100; GPU P/N change to 02G190018200; change VRAM to Hynix H5TQ1G63DFR-11C & SAMSUNG/K4W1G1646E-HC11</p> <p>(2)Page3/80 : link SNB_SKTOCC# to VRM controller</p> <p>(3)Page3 : reserve 0.01uF(C0335/C0336/C0337) for H_CPUPWRGD/PM_SYNC#/H_SNB_INV#</p> <p>(4)Page3/7 : un-link XDP_PREQ# to XDP for saving layout space, and add test point on XDP connector side.</p> <p>(5)Page6 : change +VDDQ power source from +1.5VS to +1.5V, so delete JP0601&JP0602</p> <p>(6)Page6/80 : add R0602 serial R & R0605 pull-up R for VR_SVID_ALERT#, and change PR8071 to 0ohm, un-mount PR8063</p> <p>(7)Page6 : un-mount CE0601 for factory DFM</p> <p>(8)Page26/27 : change SL0402 to SL0603 for SL2601/SL2602/SL2603/SL2702/SL2703/SL2708/SL2710/SL2711/SL2712/SL2717/SL2718/SL2719</p> <p>(9)Page29 : un-mount Clock Gen. & others interrelated components</p> <p>(10)Page30: 10.1 change net name from FAN_PWM to FAN0_PWM(page 50) 10.2 DSW_WAKE# changed to no function 10.3 PM_EXTTTS#0 changed to no function 10.4 changed net name from RFON_SW# to RF_SW#(page 53) 10.5 OP_SD# changed from GPC5 to GPE0, and VOLUME_LED# changed from GPE0 to GPE3 10.6 THRO_CPU change from GPE5 to GPH1, and changed net name from THRO_CPU to THRO_CPU#,and correct THRO_CPU# control, R0307 changed from 62ohm to 200ohm(page 3); 10.7 PM_SLP_SUS# changed to no function</p> <p>(11)Page33: delete +3VS power & SL3310 for LAN chip changed to AR8151</p> <p>(12)Page33: un-mount C3302 for BUF_PLT_RST# glitch issue</p> <p>(13)Page36 : change C3631 from 1UF/10V to 2.2UF/10V for EA test failed</p> <p>(14)Page36/20 : change DVDD_IO power source to +3VSUS, and then un-mount U2002 & R2028 and stuff R2024</p> <p>(15)Page37 : ex-change MUTE_POP# & AMP_SHD# MOS</p> <p>(16)Page42 : change the Card Reader chip to AU6437-GDL</p> <p>(17)Page44 : change J4401 to JDEBUG1 for BU request</p> <p>(18)Page46 : unstuff C4602/C4604/C4606 for EA test failed</p> <p>(19)Page68 : change FRESCO FL1000G (D1) TFBGA100 (MP) to FRESCO FL1000G (E0) TFBGA100 (ES)</p> <p>(20)Page66/69 : change CE6602 & CE6932 to c3528 size</p> <p>(21)Page76 : change R7627 value for N12P-GS and pay attention to R7618 value</p> <p>(22)Page77 : change Q7702 to CSD17507Q5A for high Rdson</p> <p>(23)Page77 : change R7703 to 0ohm</p> <p>(24)Page55 : mount stlitch Caps EC5513-EC5516, and delete EC5512</p> <p>(25)Page : change RNX4501 、 RNX5302 、 RNX5401 、 RNX6101 、 RNX6601 、 RNX6902 、 RN6901 、 RN6902 from 0402 size to 0603 size</p> <p>(26)Page6 : un-mount CE0601 for factory DFM</p> <p>(27)Page26 : reserve CE2601 for +1.05VS</p> <p>(28)Page68 : add R6801 for GPIO "USB3_SMI#"</p>

Rev	Date	Description
2.0	2010/09/30	<p>1: Page 69, USB 2.0 mount F6903 & R6903 USB 3.0 mount F6903 & F6904, un-mount R6903</p> <p>2 : Page 68, unmount R6813</p> <p>3 : Page 45, Mount R4506, increase Q4502 Vgs</p> <p>4 : Page 20, Mount R2008 for ME firmware update</p> <p>5 : Page 85, Change PR8556 to 91K, Change C7716 to 0.22UF and add D8501 for discharge</p> <p>6 : Page 20, Mount R2008 for ME firmware update</p> <p>7 : Page 77, Change R7705 to 47K, Change C7718 to 0.22UF</p> <p>8 : Page 6, R0617, R0618 Change to 1K</p> <p>9 : Page 82, Change PR8201 to 360K, Change PC8201 to 0.01UF</p> <p>10 : Page 77, Add C7799---1000PF</p> <p>11 : Page 58, Change R5805 to 15ohm, reserve C5806 0.1UF</p> <p>12 : Page 70, Change GPU to N12PLJ 02G190018204</p> <p>13 : Page 38, Change J3802 to 12G14030108N</p> <p>14 : Page 20, Change PCH to 02G010027500</p> <p>15 : Page 68, Change C6809 to 4.7UF</p> <p>16 : Page 57, Change R5719 to 100ohm for quick discharge</p> <p>17 : Page 17,14, add pull up R1701, R1401</p> <p>18 : Page 44, JDEBUG connector Power change to +3VS</p> <p>19 : Page 70/77, change U7002 & U7703 from NC7SZ08P5X_NL to 74LVC1G08GW for saving the variety of component.</p> <p>20 : Page 80, un-stuff PCE8008 , mount PCE8007</p>
	2010/10/06	<p>21 : Page 48, For EMI, mount L4801, L4802, L4803, L4804, un-mount RN4801, RN4802, RN4803, RN4804</p> <p>22 : Page 30, Change GPE1 to dGPU_PD#, Change GPE5 to MEDIA_KEY_LED#</p> <p>23 : Page 75, Add D7501 for PWRLIMIT#</p>
	2010/10/07	<p>24 : Page 56, For EC +3v reference, mount R5601 R5610 Q5601 Q5602--> change it back (2010/10/11)</p> <p>25 : Page 30, FOR ITE Suggestion, Change R3007 form 43k to 0ohm</p> <p>26 : Page 30, Change SL3010 to R3009 0ohm prevent EC version change.</p> <p>27 : Page 07, un-mount XDP: J0701, R0701, R0702 , R0703, R0704, R0705, RNX0702</p> <p>28 : Page 30, add battery discharge power limit circuit</p>
	2010/10/09	<p>29 : Page 06, change +1.5V to +1.5VS for energy star</p> <p>30 : Page 42, Reserve R4218 (+3VS) for energy star</p> <p>31 : Page 31, SL3101 change to R3101 330 OHM for energy star</p> <p>32 : Page 56, change R5620 R5613 to 1k for energy star</p> <p>32 : Page 68, Reserve +3VS for USB3.0 for energy star and remove JP6801 JP6802 JP6803</p>
	2010/10/11	<p>33 : Page 60, Change C6002 to 4.7UF, C6004 to 1UF, PR6000 to 200k for power request to slow raise and fall time</p> <p>34 : Page 91, Change PQ9113 to 07G005B19010 for large current</p> <p>35 : Page 37, Reserve C3725 C3726 C3727 C3728 FOR EMI</p>
	2010/10/12	<p>36 : Page 61, Reserve R6102 For Energy Star</p> <p>37 : Page 45, Add R4513 to change J4502 PIN5 from GND_AUDIO to GND</p> <p>38 : Page 60, mount C6002 C6003 for POWER suggestion</p> <p>39 : update power circuit for BOM</p> <p>40 : Page 37 Page 03, unmount R3715 Q3704 C3711 R0303</p>
	2010/10/13	<p>41 : Page 69, reserve R6905 for leakage, if USB3.0 choose +3VS for Energy Star, mount F6905 un-mount F6904</p> <p>42 : Page 03, Mount Q0302 R0335 For DRAMPWROK quick discharge</p> <p>43 : Page 69, Change F6904 F6905 from 07G012200130 to 07G014200020</p> <p>43 : Page 37, For EMI request, Change jump to bead (L3703, L3704, L3705, L3706)</p>

IMVP7 CPU VCORE REGULATOR



Layout Note:
VR_SVID_DATA, VR_SVID_ALERT#, VR_SVID_CLK, tracks is 5mil, distance is 15mil

Layout Note:
place PR8071(43ohm), PR8063(75ohm) put the middle of CPU & VR
place PR8069(130ohm), PR8068(54.9ohm) close to VR

Close to VCore Hot_Spot
105C and 93C

Close to +VGFx Hot_Spot

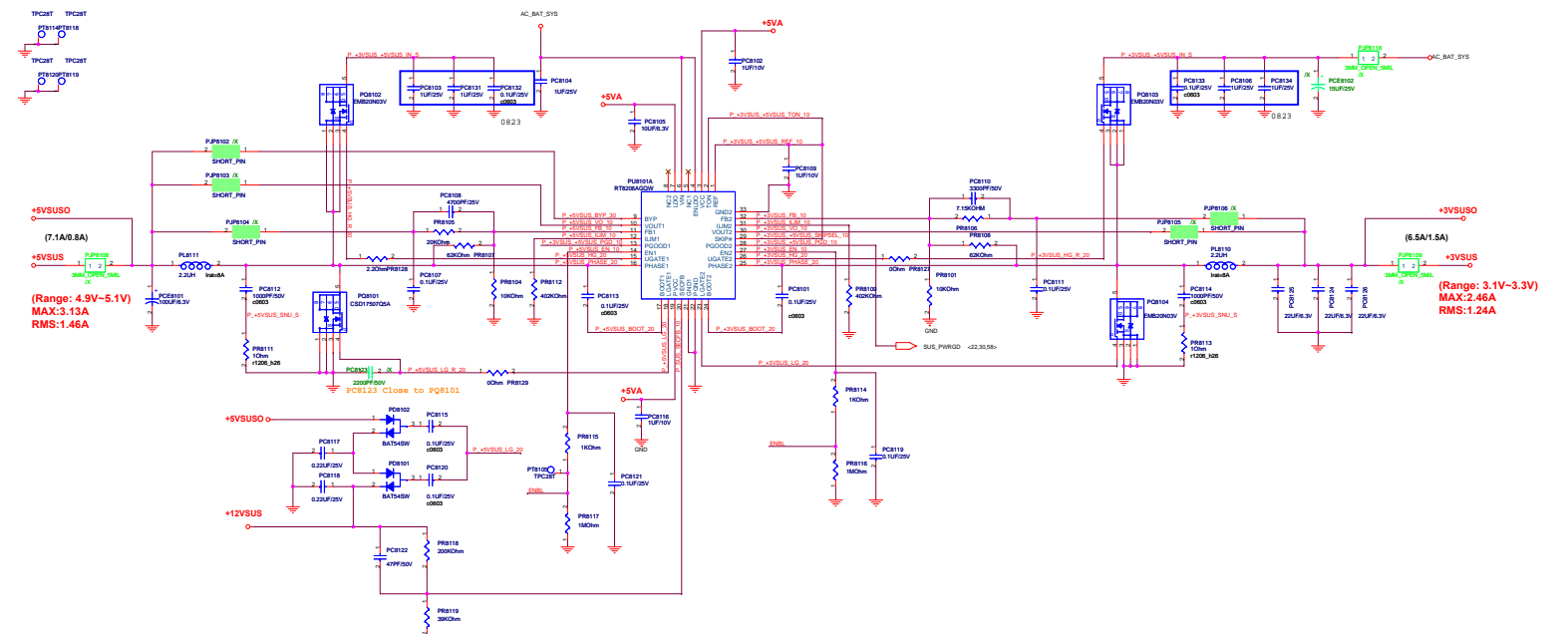
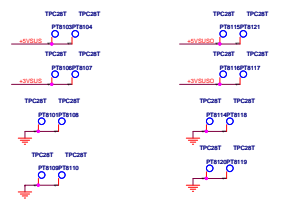
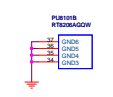
Close to Phase 1 Inductor PR8001

1. IP Current:
 $I_{in} = V_o / (0.75 \cdot V_{in}) = 3.9A$
2. Ripple Current:
Irripple=7A
3. Voltage & Current:
0.3V~1.3V ; 55A
4. ripple voltage:
 $I_{peak} = (V_{in} - V_o) / D(L / F_{sw}) = 8.8A$
 $ESR = 9 / 3 = 3mohm$
 $V = 26.4mV$
5. Frequency:
 $R_{fset} = (T - 0.29) \cdot 2.65$
Frequency= 300KHZ

For 35W CPU:
PR8014 = 5.62K for Vboot=0V/94A; PR8053 = 9.53K for 105C/25A
For 45W CPUs:
PR8014 = 590Ohm for Vboot=0V/91A; PR8053 = 6.65K for 105C/33A

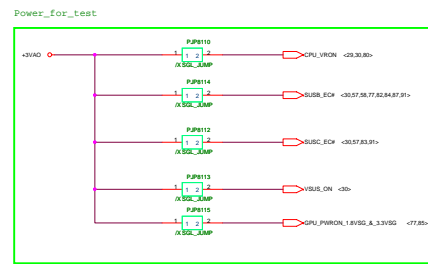
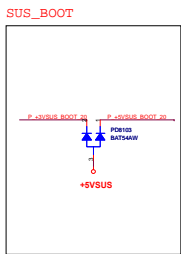
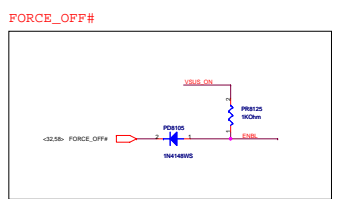
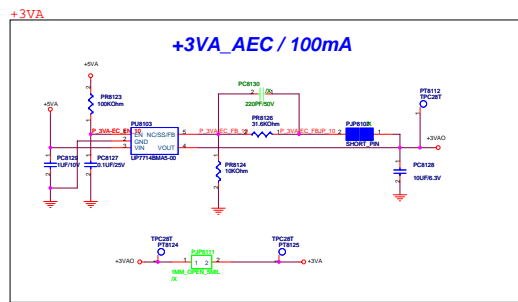
PT8001 TPC28T	PT8000 TPC28T	PT8011 TPC28T	PT8015 TPC28T
+VCore 1	+VCore 1	CPU_VRON 1	+VCCSENSE
VCC_AGS_SENSE	+VCore 1	PT8022 TPC28T	PT8016 TPC28T
GND 1	+VGFx_COR	+VCore 1	+VSENSE
PT8029 TPC28T	PT8024 TPC28T	PT8023 TPC28T	PT8017 TPC28T
GND 1	GND 1	+VCore 1	+VGFx_COR
PT8030 TPC28T	PT8028 TPC28T	PT8027 TPC28T	PT8021 TPC28T
GND 1	GND 1	GND 1	GND 1
PT8031 TPC28T	PT8025 TPC28T	PT8025 TPC28T	PT8021 TPC28T
+VCore 1	GND 1	GND 1	GND 1

ASUS
ASUSTeK COMPUTER INC. NBI
Title: +VCore
Engineer: VC
Size: Project Name
Custom: U535
Date: Wednesday, October 13, 2010
Sheet: 80 of 92



(7.1A/0.8A)
+5VSUS0
+5VSUS
(Range: 4.9V-5.1V)
MAX:3.13A
RMS:1.46A

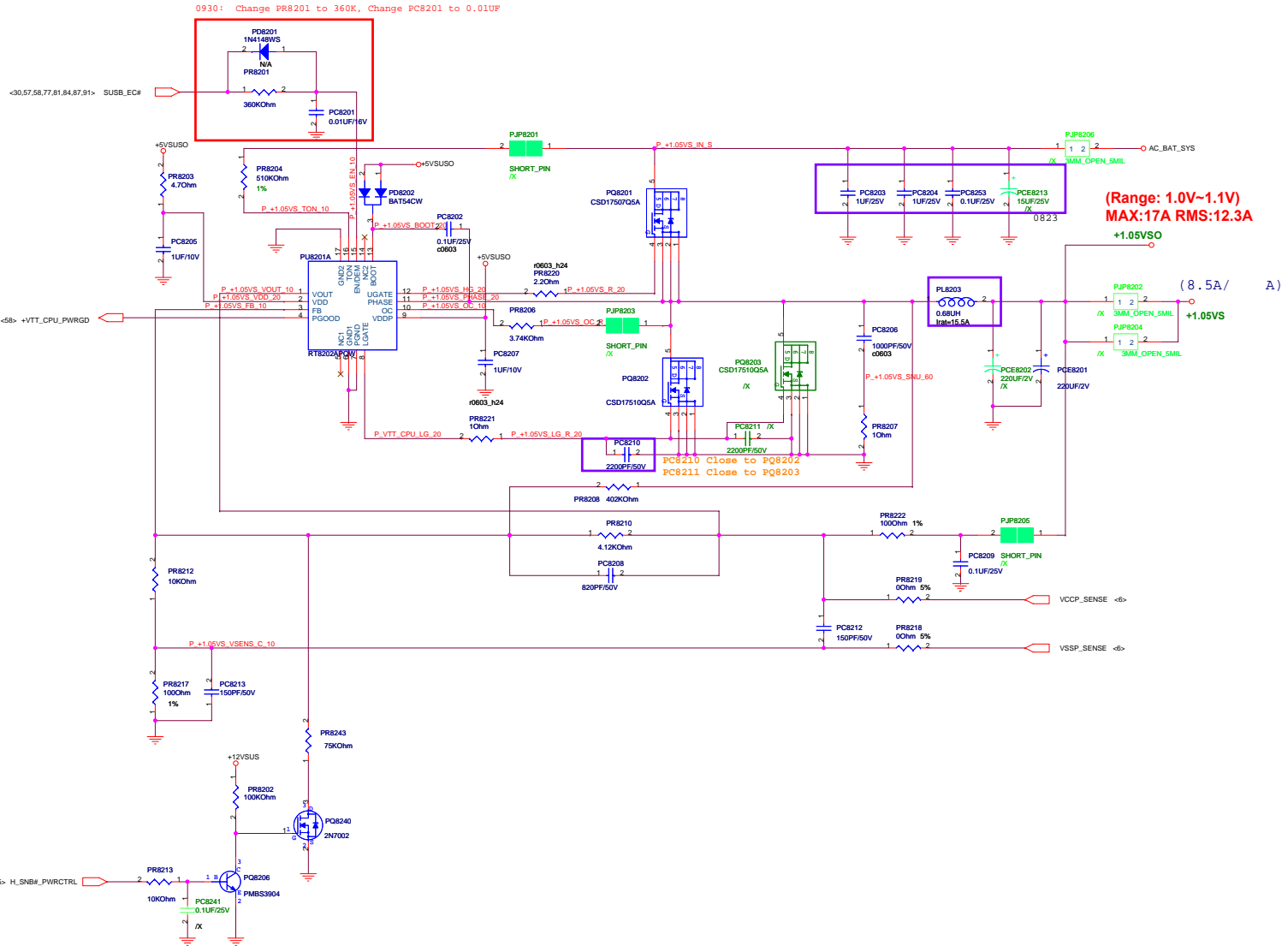
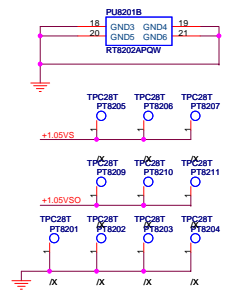
(6.5A/1.5A)
+3VSUS0
+3VSUS
(Range: 3.1V-3.3V)
MAX:2.46A
RMS:1.24A



Power information	
+5VSUS	
1. I/P Current:	
$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.082A$	
2. Ripple Current:	
$I_{rip} = 1.012A$	
$I_{spec} = 2.5A \times 1$	
pcs	
3. Dynamic:	
$I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 2.58A$	
ESR / 1 pcs = 15 mohm	
$\Delta V = 38.72mV$	
1. Voltage & Current:	
+5VSUS=5V@3.13A	
2. Frequency:	
fosc=300KHz	
3. OCP:	
Set PR8112=402Kohm	
locp=14A	

Power information	
+3VSUS	
1. I/P Current:	
$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.375A$	
2. Ripple Current:	
$I_{rip} = 1.152A$	
$I_{spec} = 2.5A \times 1$	
pcs	
3. Dynamic:	
$I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 1.55A$	
ESR / 1 pcs = 15mohm	
$\Delta V = 23.25mV$	
1. Voltage & Current:	
+3VSUS=3.3V@2.46A	
2. Frequency:	
fosc=375KHz	
3. OCP:	
Set PR8109=402Kohm	
locp=8.74A	

	Title: Power -5VSUS+3VSUS+12VSUS
ASUS Design Center	Engineer: ZHA-KUN, LIU
Rev: 1.0	Rev: 1.0
Doc Name: P61JLV	Doc No: P61JLV
Doc Date: 2014.08.14	Doc Ver: 1.0



Power Information

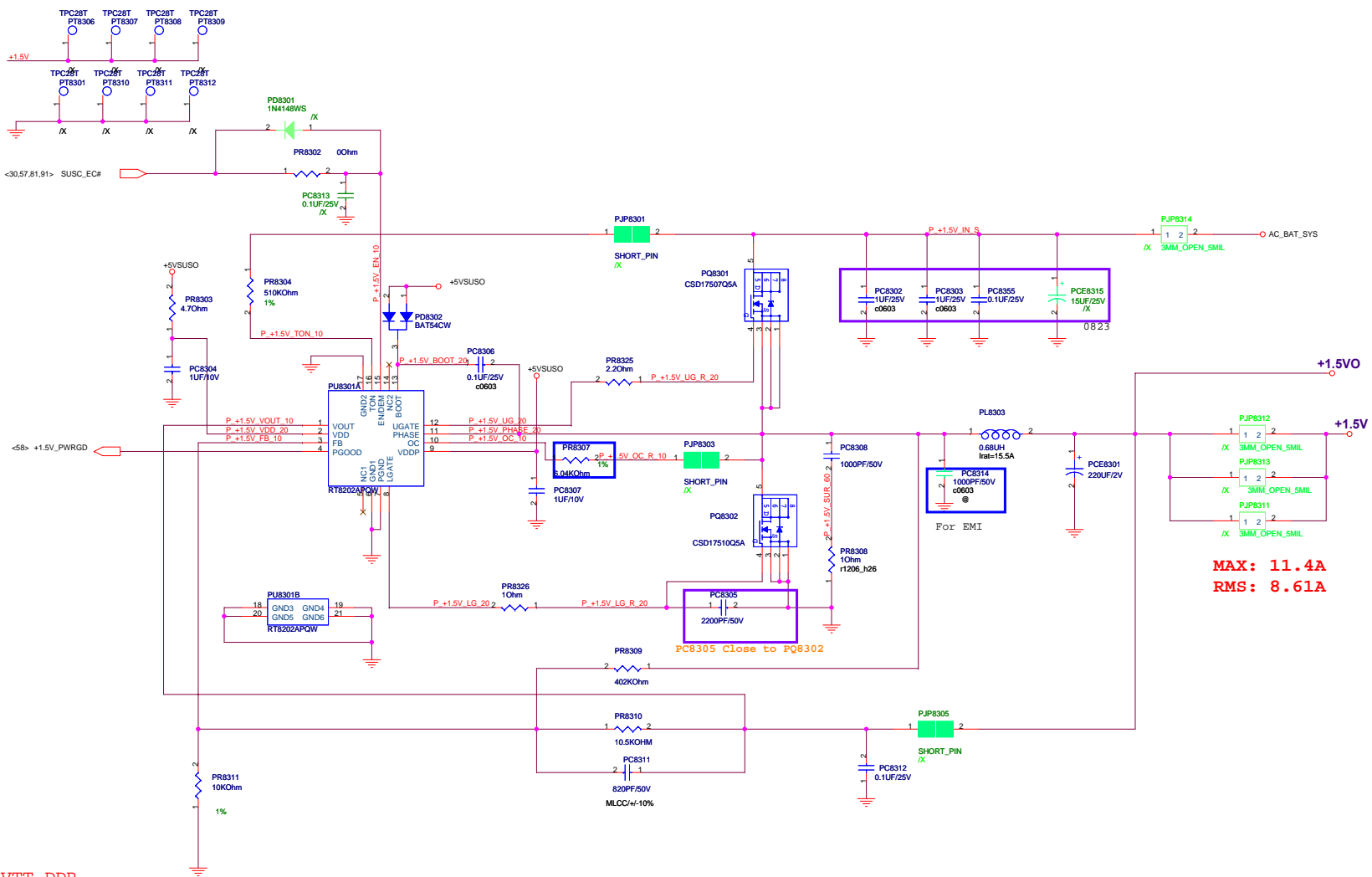
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.1A$
- Ripple Current:**
 $I_{ripple} = 5A$
- Dynamic:**
 $I_{peak} = 1.98A$
 $DCR = 3.3m\Omega$
 $V = 6.534mV$

1. Voltage & Current:
 +VTT_CPU: 1.05V@25A

2. Frequency:
 $T_{on} = 3.85 \mu s \cdot R_t / (V_{in} - 0.5) = 2.3 \mu s$
 $F_{frequency} = V_{out} / (V_{in} \cdot T_{on}) = 500KHZ$

3. OCP:
 Set PR8206 = 3.74KOhm
 $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)} = 27.2A$

H_VTTVID1	+VTT_CPU
1	1.05V
0	1.1V

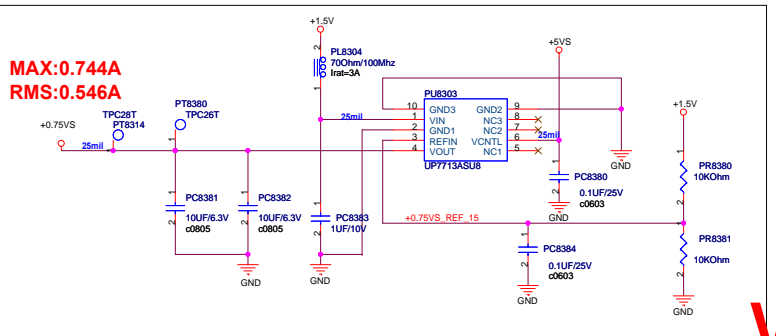


Power information

- I/P Current:**
 $I_{in} = V_o I_o / (0.75 * V_{in}) = 3.6A$
- Ripple Current:**
 Irrippl=5A
- Ripple voltage:**
 $I_{peak} = (v_{in} - v_o) * D / (L * F_{sw}) = 2.07A$
 $DCR = 10mohm$
 $V = 20.7mV$
- Voltage & Current:**
 1.5V: 16.45A
- Frequency:**
 $T_{on} = 3.85p * R_t(ON) / V_{in} - 0.05 = 0.3us$
 $Frequency = V_{out} / (V_{in} * T_{on}) = 500KHZ$
- SOCP:**
 Set OCP PR8307=4.7kohm
 $I_{ocp} = R_{ocp} * 20 / R_{ds(on)} = 17A$
- Soft start time:**
 Soft-Star duration is 1.35ms
- Inrush Current:**
 $C_{total} = 220uF$
 $I_{inrush} = 0.163A$

MAX: 11.4A
RMS: 8.61A

+VTT_DDR



www.vinafix.vn

1.8VS @ 0.7A

1. Dropout Voltage:

$\Delta V = 0.3V$ ($I_o = 2A$)

2. Current Limit:

$I_{limit} = 3A$

3. Continue Current:

$I_{cont} = 1A$

4. Power Dissipation:

$R_{thjc} = 250^{\circ}C/W$

$P_d = 0.4W$

5. EN Voltage:

$V_{rising} = 2V$

$V_{falling} = 0.8V$

6. Supply Voltage:

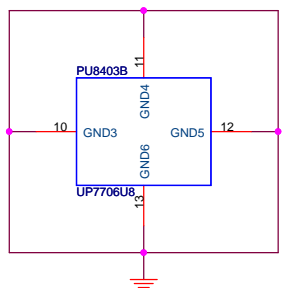
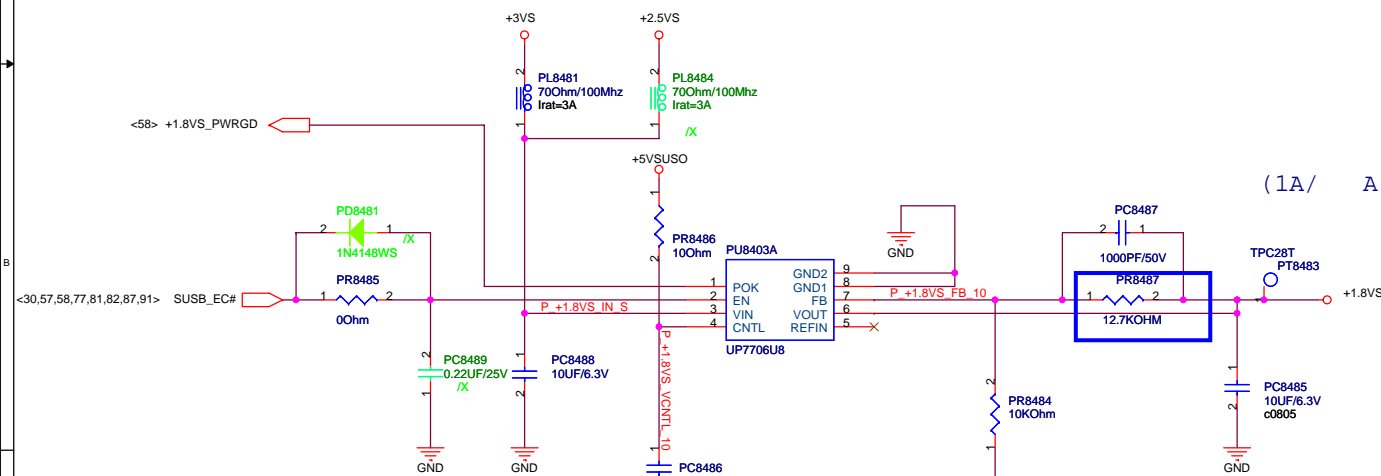
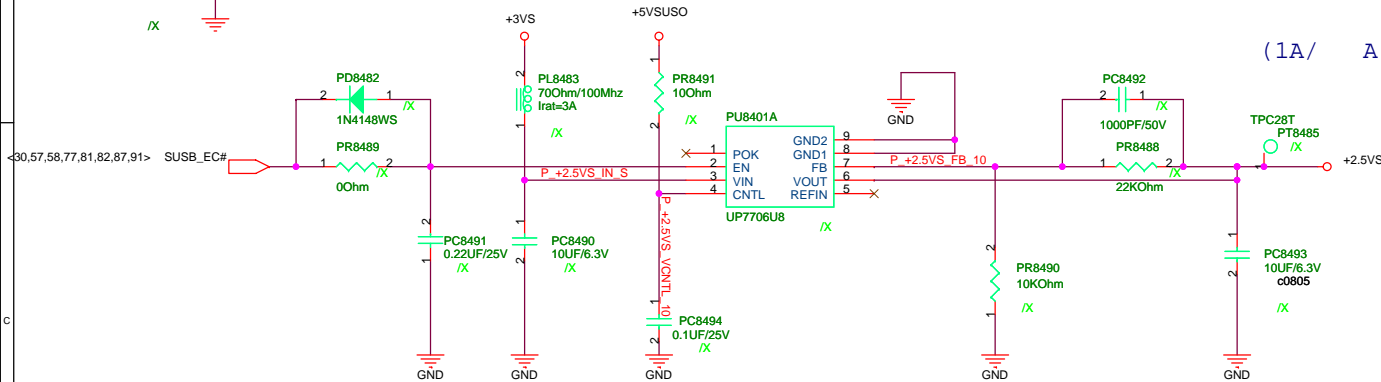
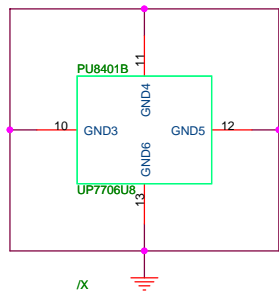
$V_{cc} = 3V$

7. Inrush current:

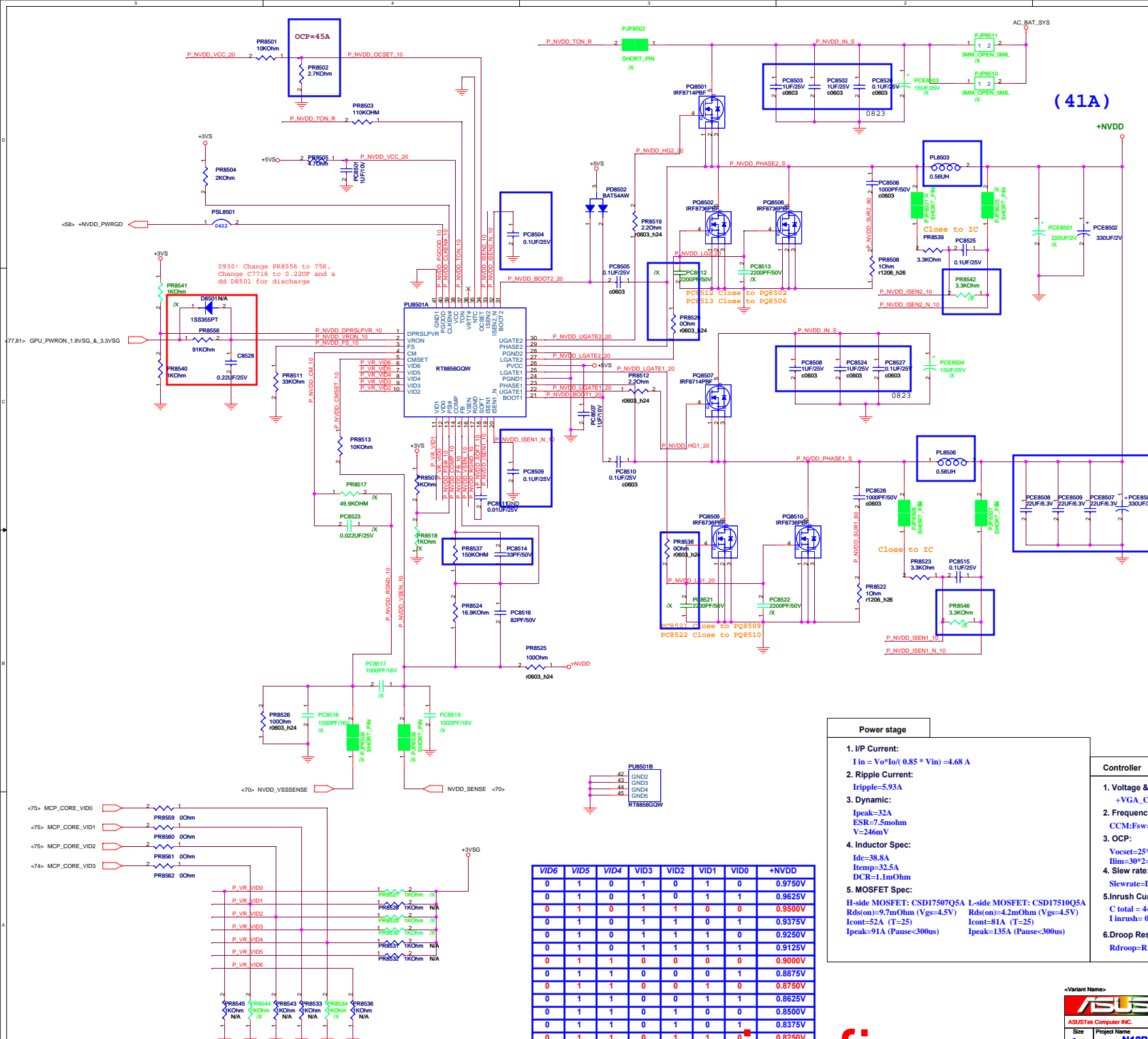
$T_{ss} = 400\mu s$

$C_{total} = 10\mu F$

$I_{inrush} = 0.063A$



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(41A)

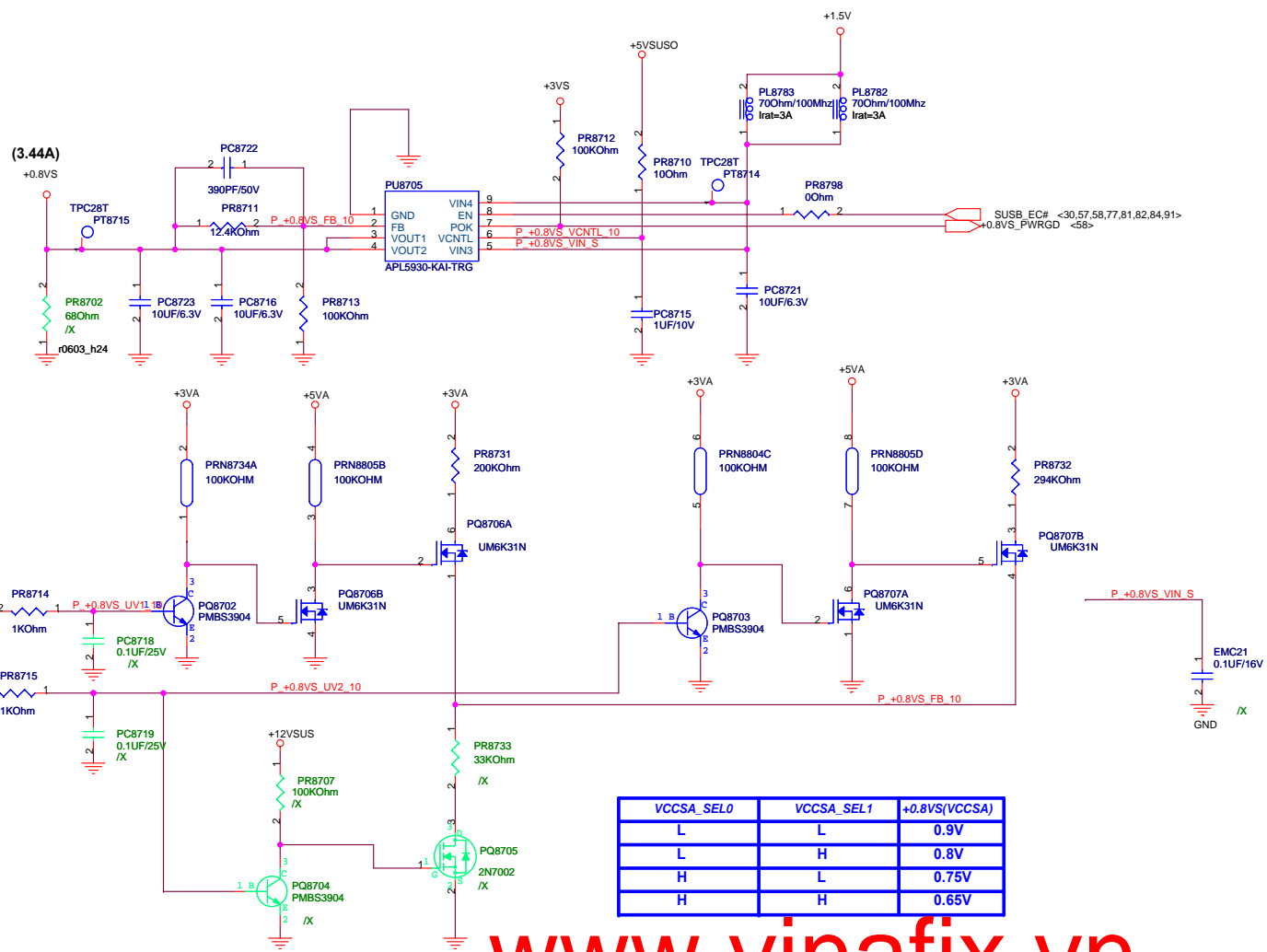
Power stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.85 \cdot V_{in}) = 4.68 \text{ A}$
- Ripple Current:**
 $I_{ripple} = 5.93 \text{ A}$
- Dynamic:**
 $I_{peak} = 32 \text{ A}$
 $E_{SR} = 7.5 \text{ mJ/mhm}$
 $V = 24 \text{ kV}$
- Inductor Spec:**
 $I_{dc} = 38.8 \text{ A}$
 $I_{temp} = 32.5 \text{ A}$
 $I_{cont} = 52 \text{ A (T=25)}$
 $I_{peak} = 91 \text{ A (Pause < 300us)}$
- MOSFET Spec:**
 $R_{ds(on)} = 9.7 \text{ m}\Omega$ ($V_{gs} = 4.5 \text{ V}$) $R_{ds(on)} = 4.2 \text{ m}\Omega$ ($V_{gs} = 4.5 \text{ V}$)
 $I_{cont} = 52 \text{ A (T=25)}$ $I_{cont} = 81 \text{ A (T=25)}$
 $I_{peak} = 91 \text{ A (Pause < 300us)}$ $I_{peak} = 135 \text{ A (Pause < 300us)}$

Controller

- Voltage & Current:**
 $+VGA_Core = 0.875 \text{ V/41A}$
- Frequency:**
 $CCM: F_{sw} = 300 \cdot 33 / R_{FS} = 300 \text{ KHZ}$
- OCP:**
 $V_{ocset} = 25 \cdot I_{lim} \cdot R_{sense}$
 $I_{lim} = 30 \cdot 2 = 60 \text{ A}$
- Slew rate:**
 $Slewrate = I_{ss} / PC7810 = 100 \mu\text{A} / 10 \text{ nF} = 10 \text{ mV/us}$
- Inrush Current:**
 $C_{total} = 440 \text{ nF}$
 $I_{inrush} = 0.3 \text{ A}$
- Droop Resistance:**
 $R_{droop} = R1/R2 \cdot 10^4 \cdot R_{sense} = 0.39 \text{ mohm}$

VID6	VID5	VID4	VID3	VID2	VID1	VID0	+NVDD
0	1	0	1	0	1	0	0.9750V
0	1	0	1	0	1	1	0.9625V
0	1	0	1	1	0	0	0.9500V
0	1	0	1	1	1	0	0.9375V
0	1	0	1	1	1	1	0.9250V
0	1	0	1	1	1	1	0.9125V
0	1	1	0	0	0	0	0.9000V
0	1	1	0	0	0	1	0.8875V
0	1	1	0	0	1	0	0.8750V
0	1	1	0	0	1	1	0.8625V
0	1	1	0	1	0	0	0.8500V
0	1	1	0	1	0	1	0.8375V
0	1	1	0	1	1	0	0.8250V



VCCSA_SEL0	VCCSA_SEL1	+0.8V(VCCSA)
L	L	0.9V
L	H	0.8V
H	L	0.75V
H	H	0.65V

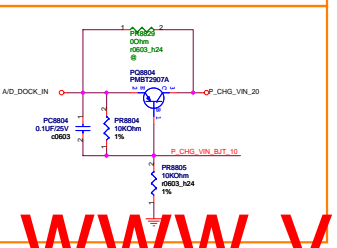
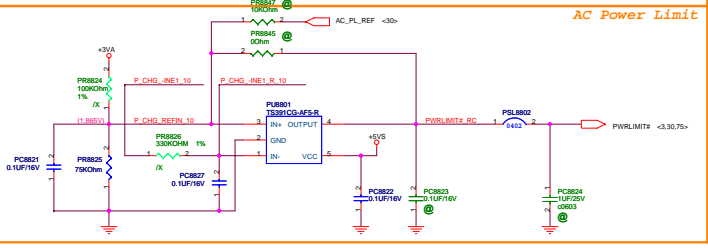
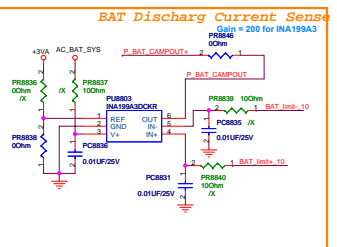
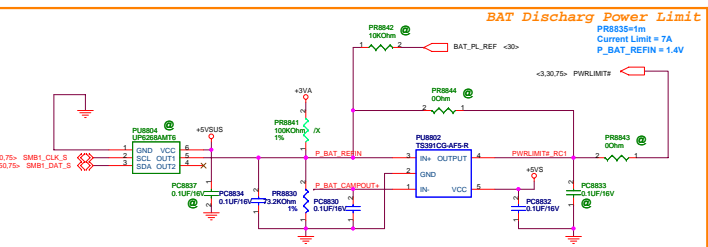
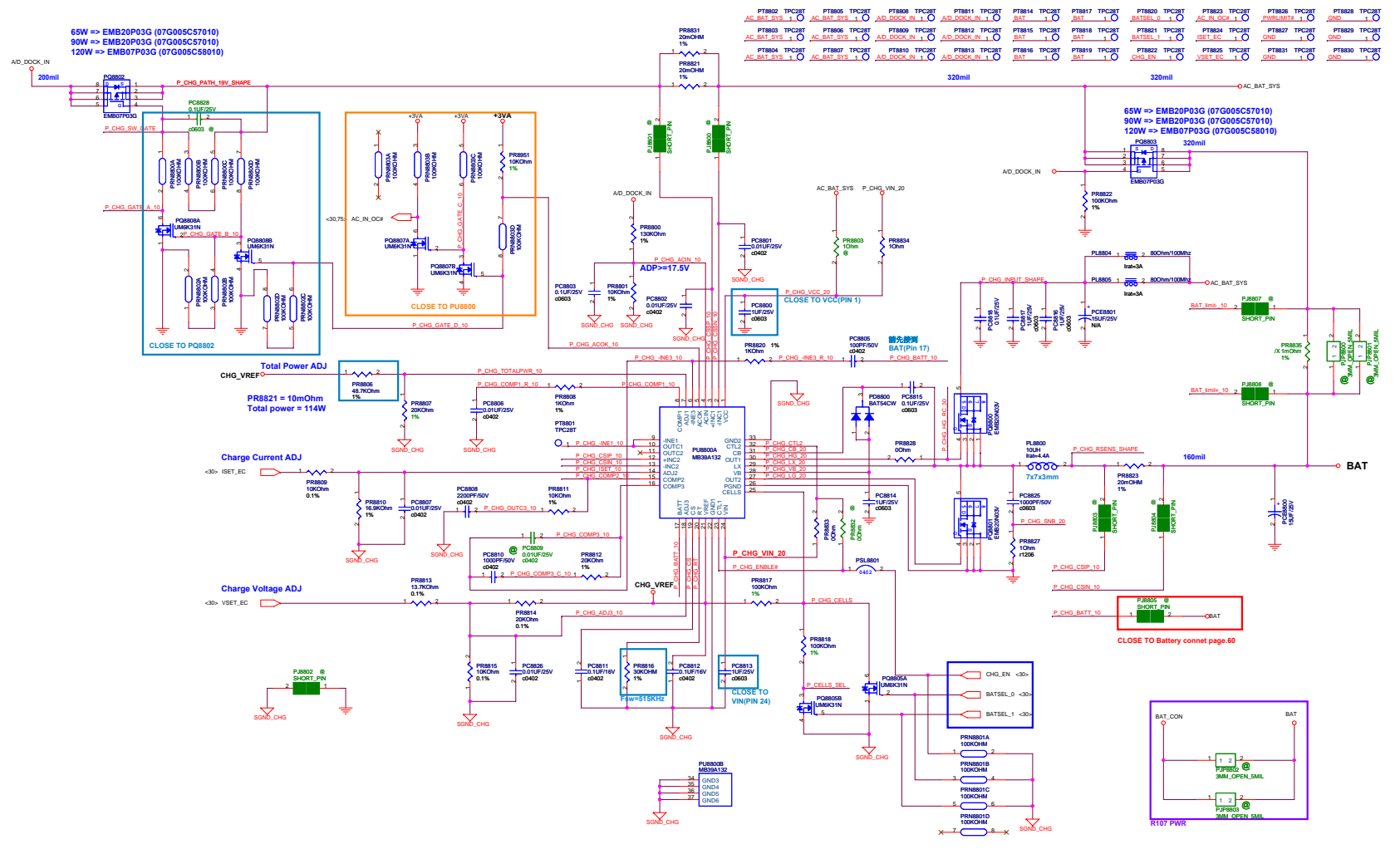
<Variant Name>

Title :

ASUSTeK COMPUTER INC **Engineer:**

Size	Project Name	Rev
Custom		1.0

Date: Wednesday, October 13, 2010 Sheet 87 of 92



Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
 Charger MAX1725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

5

4

3

2

1

D

D

C

C


B

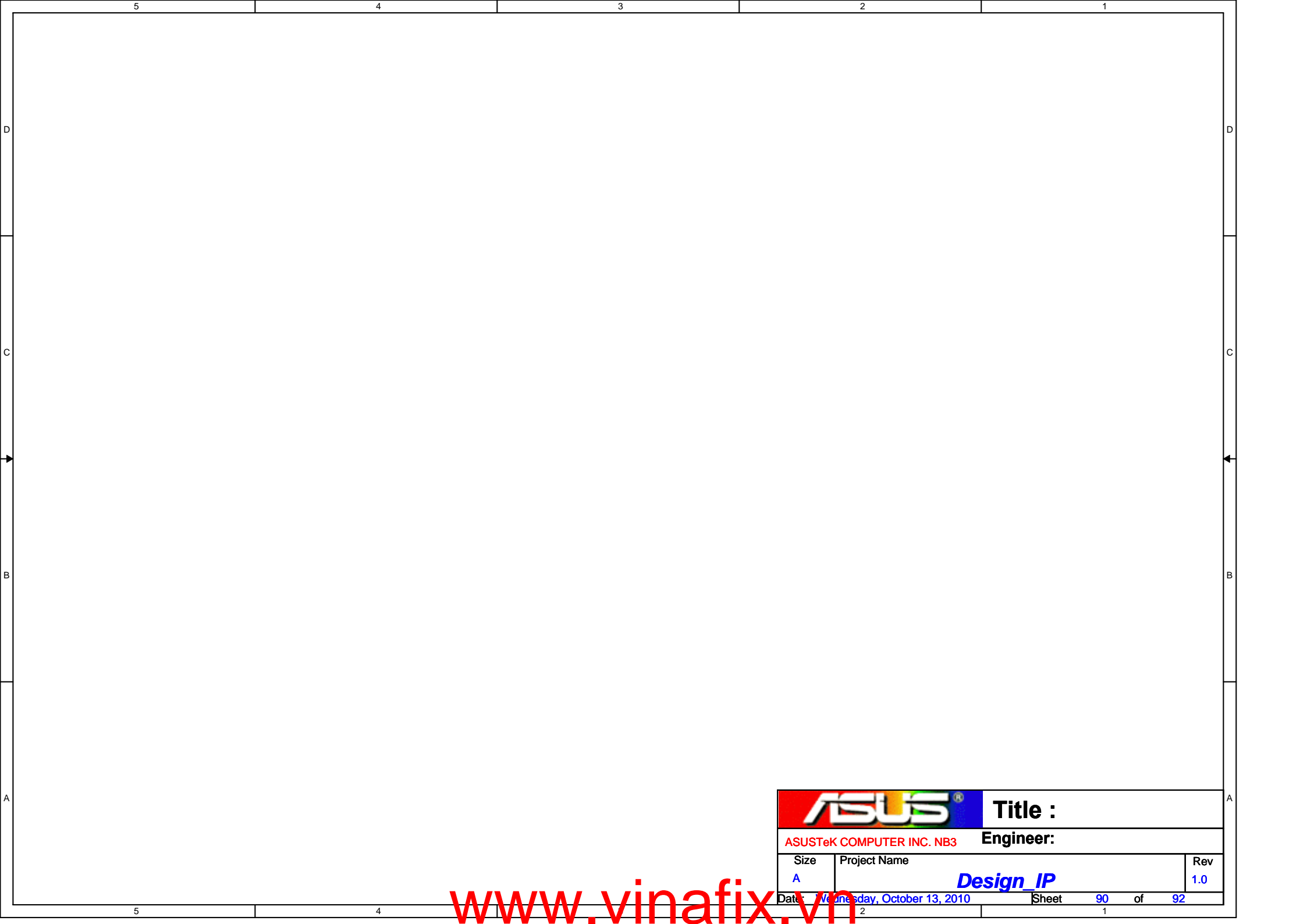
B

A

A

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		Title :	
ASUSTeK COMPUTER INC. NB3		Engineer:	
Size	Project Name	Rev	
Custom	<i>Design_IP</i>	1.0	
Date: Wednesday, October 13, 2010		Sheet	89 of 92



Title :

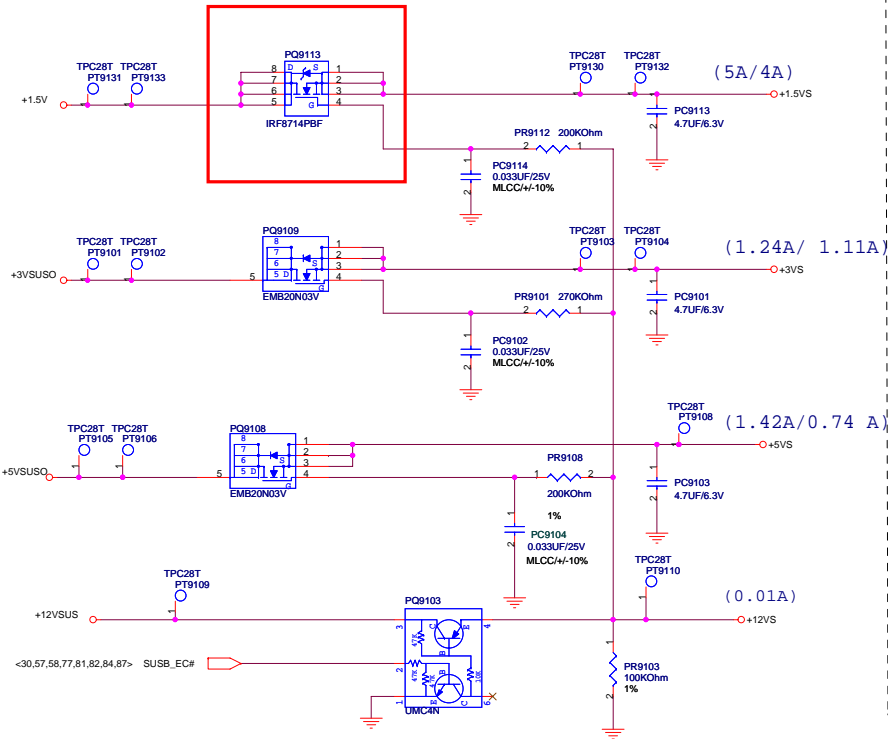
ASUSTeK COMPUTER INC. NB3

Engineer:

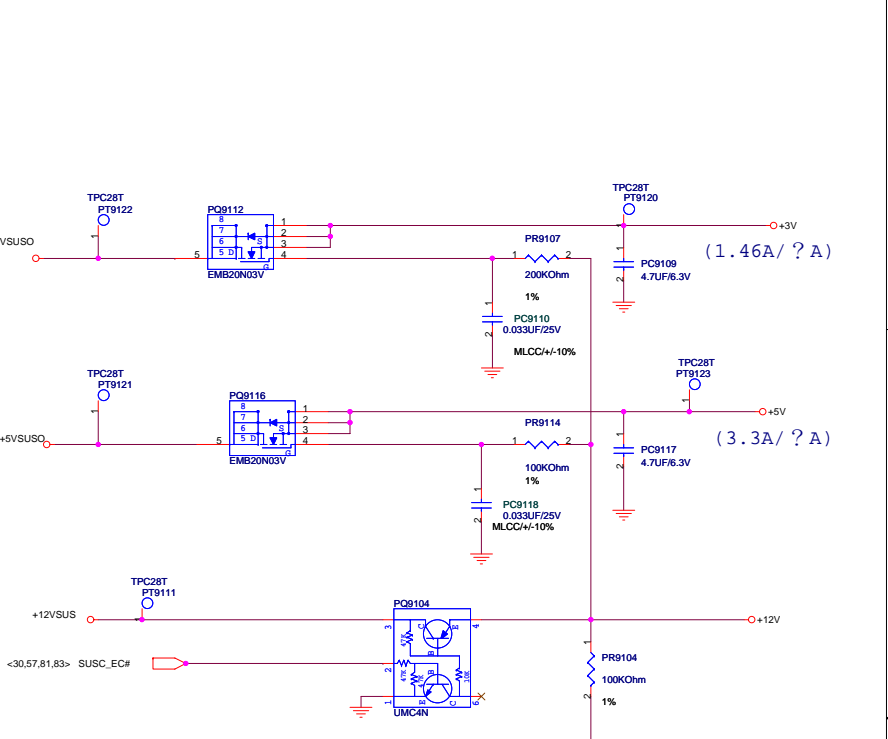
Size A	Project Name <i>Design_IP</i>	Rev 1.0
Date: Wednesday, October 13, 2010	Sheet 90 of 92	

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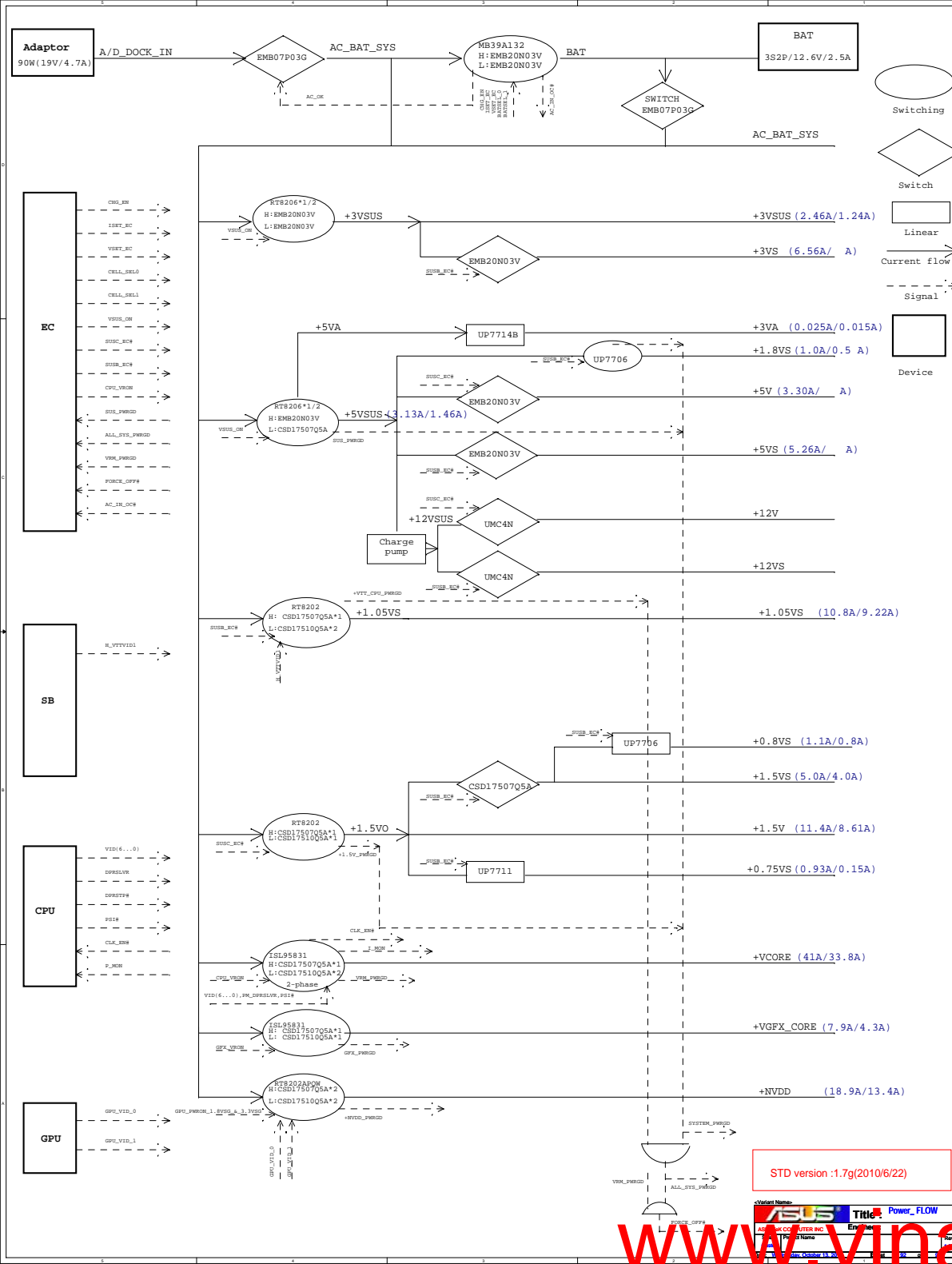
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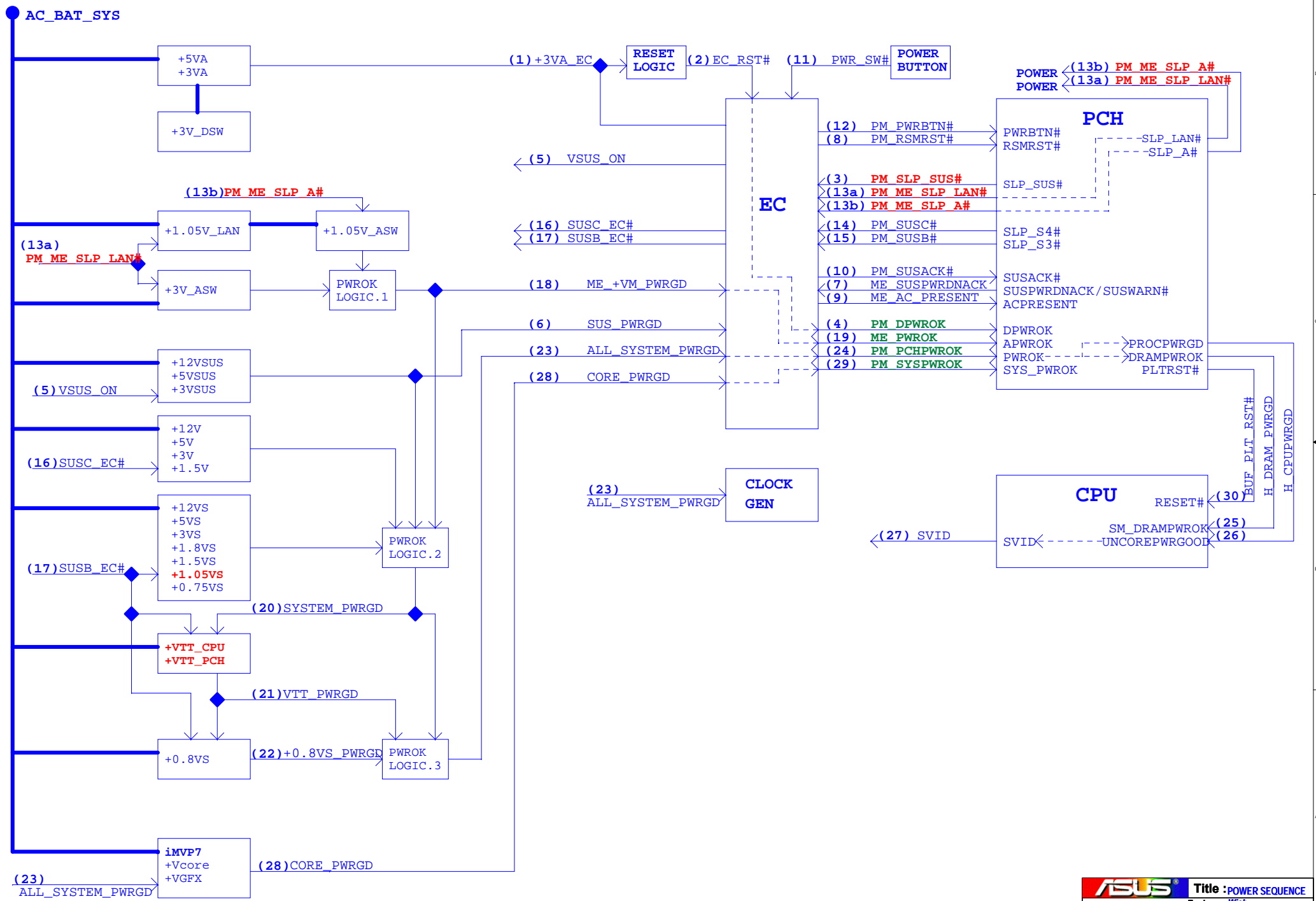
SUSC#_PWR POWER



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STD version :1.7g(2010/6/22)

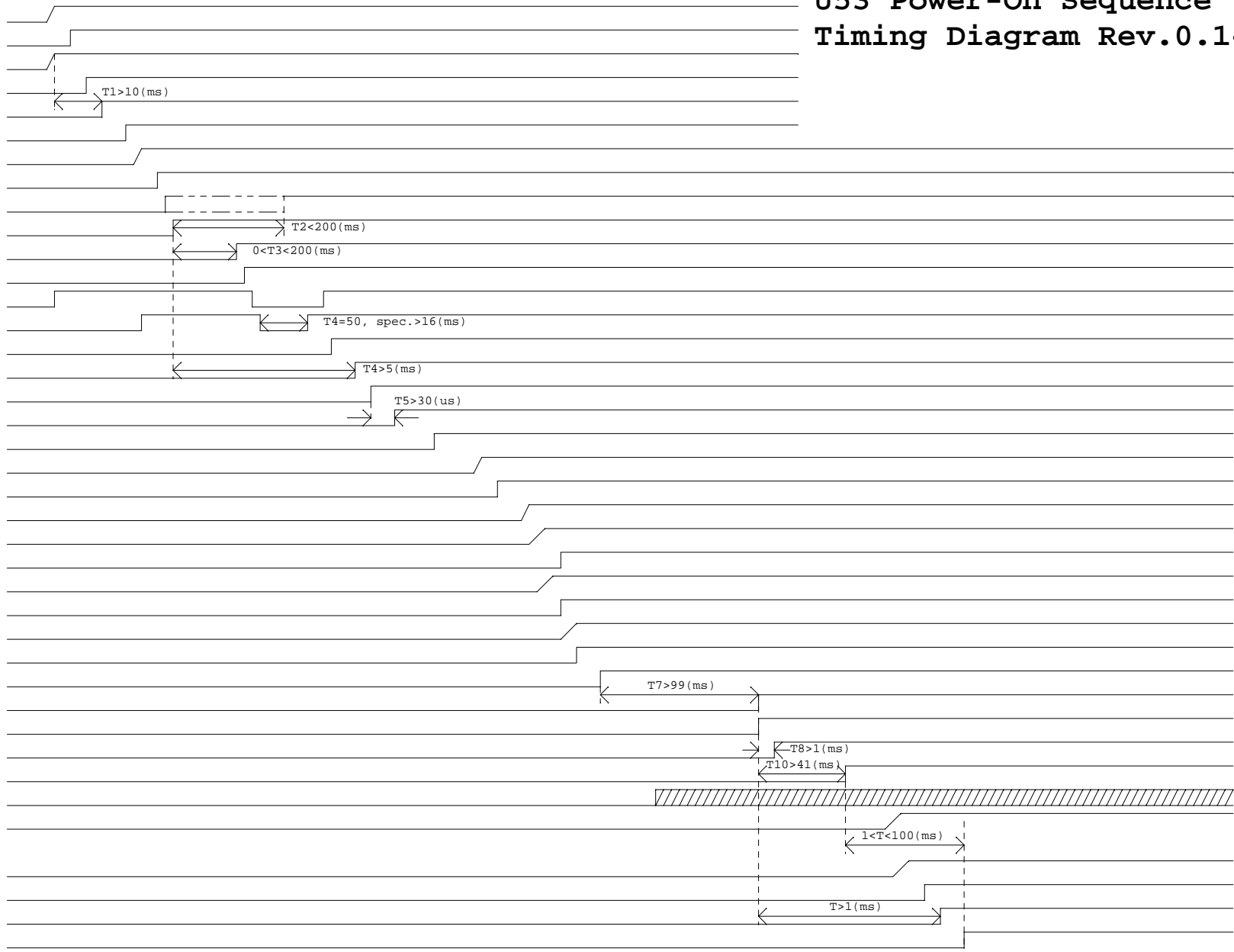


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U53 Power-On Sequence Timing Diagram Rev.0.14

AC-IN Mode

- 1 +3VA/+5VA/+3VA_EC
- 2 EC_RST#
VccDSW
- 3 PM_SLP_SUS#
- 4 PM_DPWROK
- 5 VSUS_ON
+3VSUS/+5VSUS
SUS_PWRGD
- 7 ME_SusPwrDnAck
- 8 PM_RSMRST#
- 9 ME_AC_PRESENT
- 10 PM_SUSACK#
- 11 PWR_SW#
- 12 PM_PWRBTN#
- 13(a) PM_ME_SLP_LAN#
- 13(b) PM_ME_SLP_A#
- 14 PM_SUSC#
- 15 PM_SUSB#
- 16 SUSC_EC#
+1.5V/+3V/+5V
- 17 SUSB_EC#
+0.8VS/+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS
+PEX_VDD/+1.5VSG/+1.8VSG/+3VSG/+NVDD
- 20 SYSTEM_PWRGD
+VTT_CPU
- 21 +VTT_CPU_PWRGD
+0.8VS
- 22 +0.8VS_PWRGD
- 23 ALL_SYSTEM_PWRGD
- 24 PM_PCHPWROK
- 25 PM_SYSPWROK
- 26 H_DRAM_PWRGD
- 27 H_CPUPWRGD
- 28 SVID
+Vcore
- +VccGFX
- 29 VRM_PWRGD
- 30 SUS_SATA#
- 31 BUF_PLT_RST#



U53 Power-On Sequence Timing Diagram Rev.0.14

DC-IN Mode

- 1 +3VA/+5VA/+3VA_EC
- 2 EC_RST#
VccDSW
- 3 PM_SLP_SUS#
- 4 PM_DPWROK
- 5 PWR_SW#
- 6 VSUS_ON
+3VSUS/+5VSUS
- 7 SUS_PWRGD
- 8 ME_SusPwrDnAck
- 9 PM_RSMRST#
- 10 ME_AC_PRESENT
- 11 PM_SUSACK#
- 12 PM_PWRBTN#
- 13(a) PM_ME_SLP_LAN#
- 13(b) PM_ME_SLP_A#
- 14 PM_SUSC#
- 15 PM_SUSB#
+105VM_LAN
+1.05VM/+3VM
- 16 SUSC_EC#
+1.5V/+3V/+5V
- 17 SUSB_EC#
+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS
- 18 ME_+VM_PWRGD
- 19 ME_PWROK
- 20 SYSTEM_PWRGD
+VTT_CPU
- 21 +VTT_CPU_PWRGD
+0.8VS
- 22 +0.8VS_PWRGD
- 23 ALL_SYSTEM_PWRGD
- 24 PM_PCHPWROK
- 25 H_DRAM_PWRGD
- 26 H_CPUPWRGD
- 27 SVID
+VCORE
+VccGFX
- 28 VRM_PWRGD
- 29 PM_SYSPWROK
- 30 BUF_PLT_RST#

