

PROJECT N10I

Revision 2008/04/24

Revision History

R1.0	S R	2008/01

Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	++VALWAYS#	++V	++VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

SMB Signals

Host	Name	Devices	Address
Chipset	SMBCK, SMBDA	ICH7-M ADT7473(Thermal) ICS954310(Clock Genertor) DDR2 SO-DIMM	0001 000X b 0101 110X b D2h A0h

PCI Devices

Bus#	Device#	Function#	REQ/GNT#	IDSEL	APIC Interrupts	Device Function
Bus0	Device00	Function0				Intel 945GMS Host Bridge
Bus0	Device02	Function0				VGA-Comptible Controller
Bus0	Device1C	Function0				PCI to PCI Bridge
Bus0	Device27	Function0			A#	Azalia Controller
Bus0	Device29	Function0			H#	Intel UHCI USB Cotroller
Bus0	Device29	Function1			D#	Intel UHCI USB Cotroller
Bus0	Device29	Function2			C#	Intel UHCI USB Cotroller
Bus0	Device29	Function3			A#	Intel UHCI USB Cotroller
Bus0	Device29	Function7			H#	Intel EHCI USB Cotroller
Bus0	Device31	Function1			C#	PATA
Bus0	Device31	Function2			B#	SATA
Bus5	Device08	Function0		AD17	B#	CarBus Brige

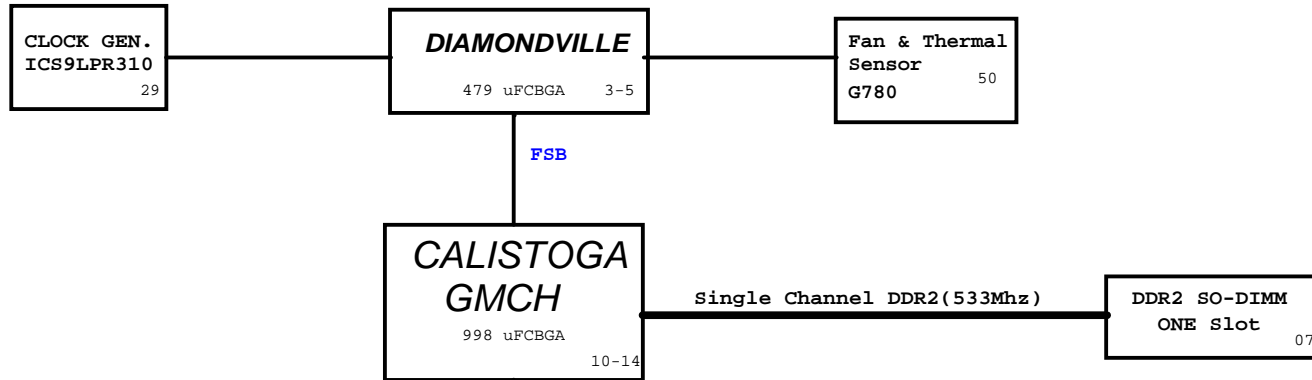
Voltage Rail

Net Name	Voltage	On During These ACPI States	Description
+3VAO,+3VA,+3VALWAYS_P	+3.3V	S0 - S5	Always ON.
+5VCHG	+5V		
+VCC_RTC	+5V		
+3VO,+3VSUS,+3VALWAYS	+3V	S0,S3,S4*,S5*	Power supply for ICH7M, RTL8111B.
+5VO,+5VSUS	+5V		
+1.8VO,+1.8V	+1.8V	S0 - S3	Power supply for 945GMS, DDRII, ICH7M, M38857 R5C801.
+3V	+3V		
+5V	+5V		
+1.05VO,+VCCP	+1.05V	S0	0.9V DDR2 termination voltage
+1.5VO,+1.5VS	+1.5V		
+0.9VO,+0.9VS	+0.9V		Core voltage for processor
+2.5VO,+2.5VS,VCCA3GBG	+2.5VS		
VCCALVDS, VCCSYN, VCCTXLVDS			
+3VS	+3V		
+5VS	+5V		
+VCORE_0,+VCORE	Variable		

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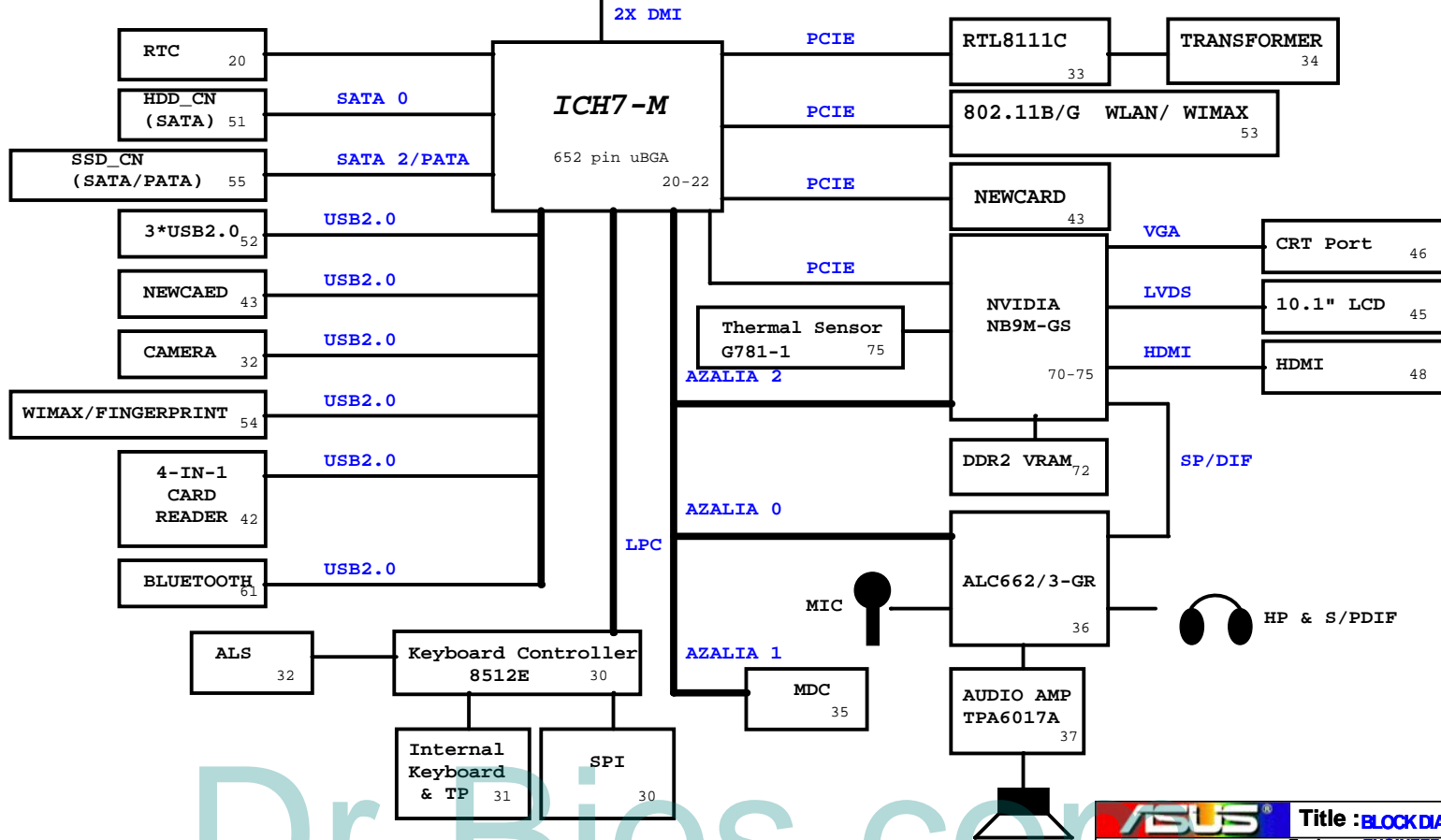
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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
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DIAMONDVILLE/CALISTOGA(945GSE) BLOCK DIAGRAM






POWER

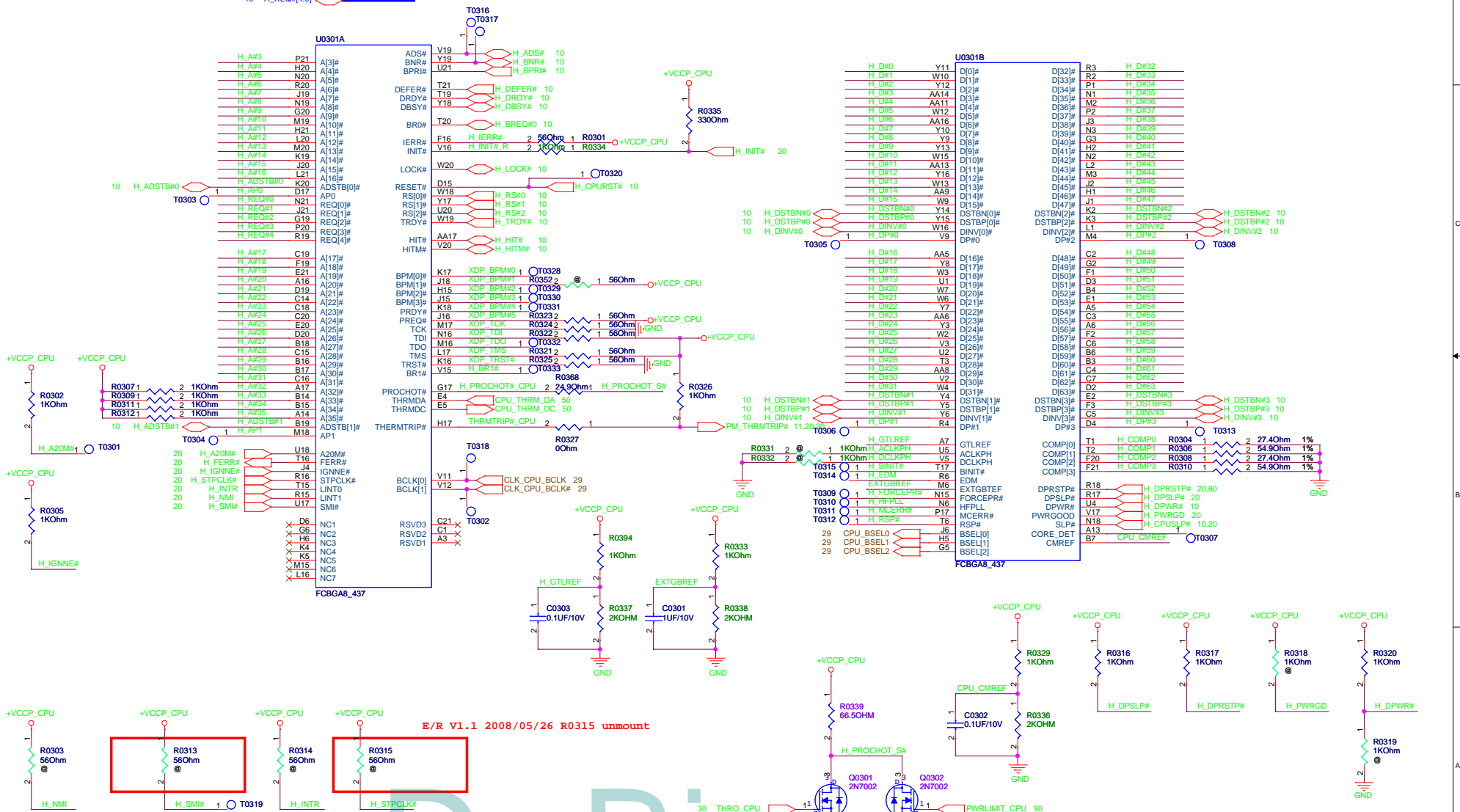
VCORE	80
SYSTEM	81
VCCP, +1.5VS	82
+1.8V, +0.9VS	83
+2.5VS, +3VA	84
+VGA_CORE, +1.1VS	85
EMPTY	86
EMPTY	87
CHARGER	88
EMPTY	89
POWER PROTECT	90
LOAD SWITCH	91
PROTECT SIGNAL	92
FLOW CHART	93
POWERON_DC(1)	94
POWERON_DC(2)	95
POWERON_AC(1)	96
POWERON_AC(2)	97



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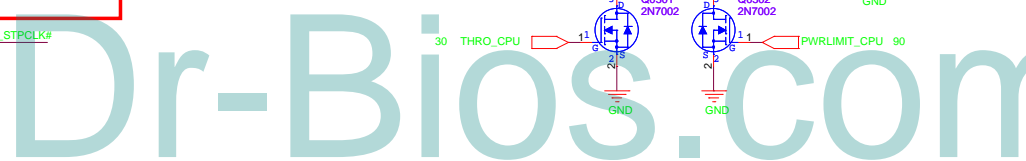
ASUS		Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size Custom	Project Name N10	Rev 1.0	
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10 H_D#(63:0)  H_D#(63:0)
 10 H_A#(35:3)  H_A#(35:3)
 10 H_REQ#(4:0)  H_REQ#(4:0)

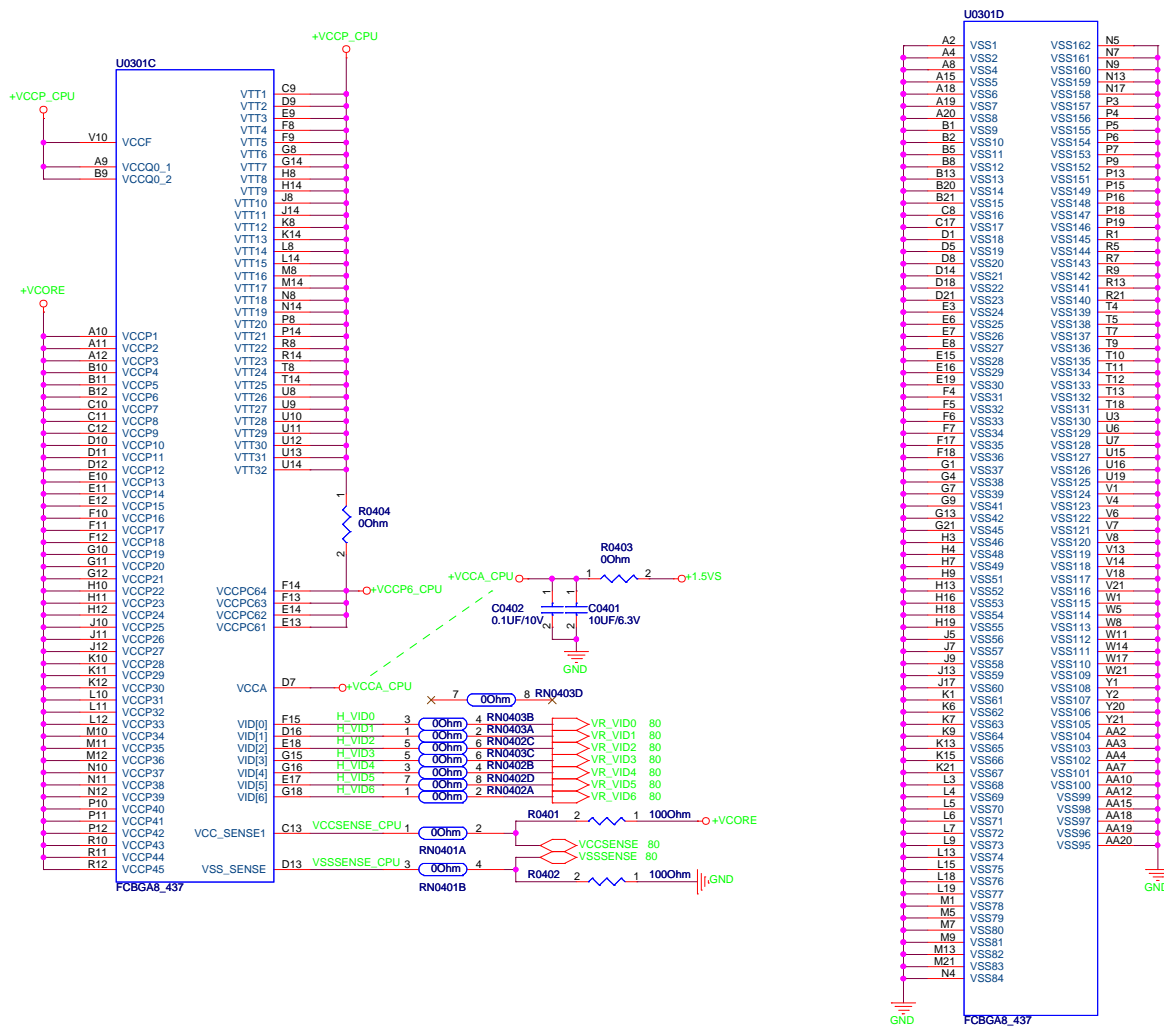


E/R V1.1 2008/05/26 R0313 unmount

E/R V1.1 2008/05/26 R0315 unmount

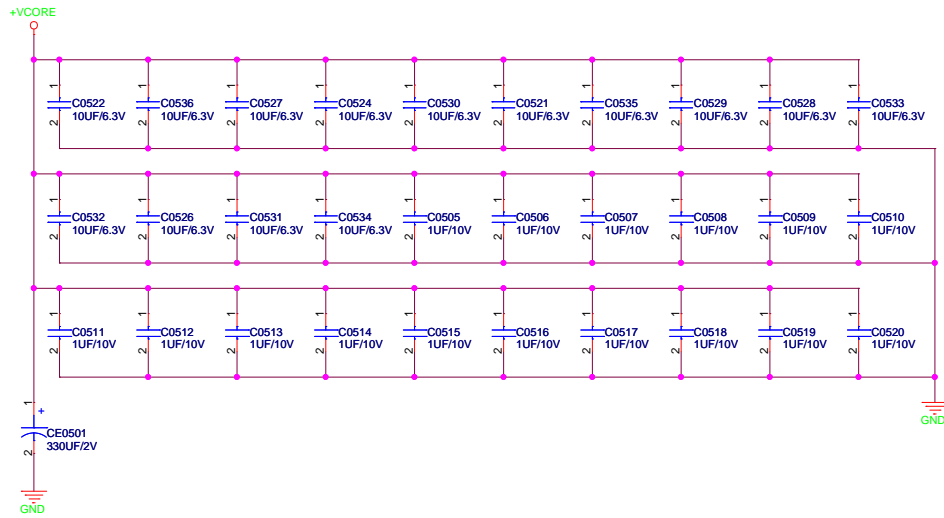


		Title : CPU(1)	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
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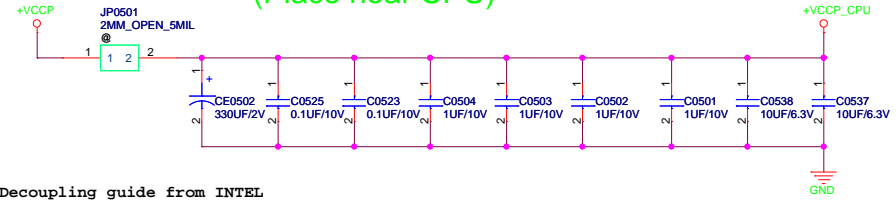


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ASUS		Title : CPU(2)	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
Custom	N10		1.0
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**+VCCP Decoupling Capacitor
(Place near CPU)**



Decoupling guide from INTEL

VCCORE	1uF/10V	* 16pcs for CPU
	10uF/6.3V	* 14pcs for CPU
	330uF/2V	* 1pcs for CPU
VCCP	0.1uF	* 2pcs for CPU
	1uF	* 4 pcs for CPU
	10uF	* 2 pcs for CPU
	330uF	* 1pcs for CPU

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5

4

3

2

1

D

D

C

C


B

B

A

A

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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
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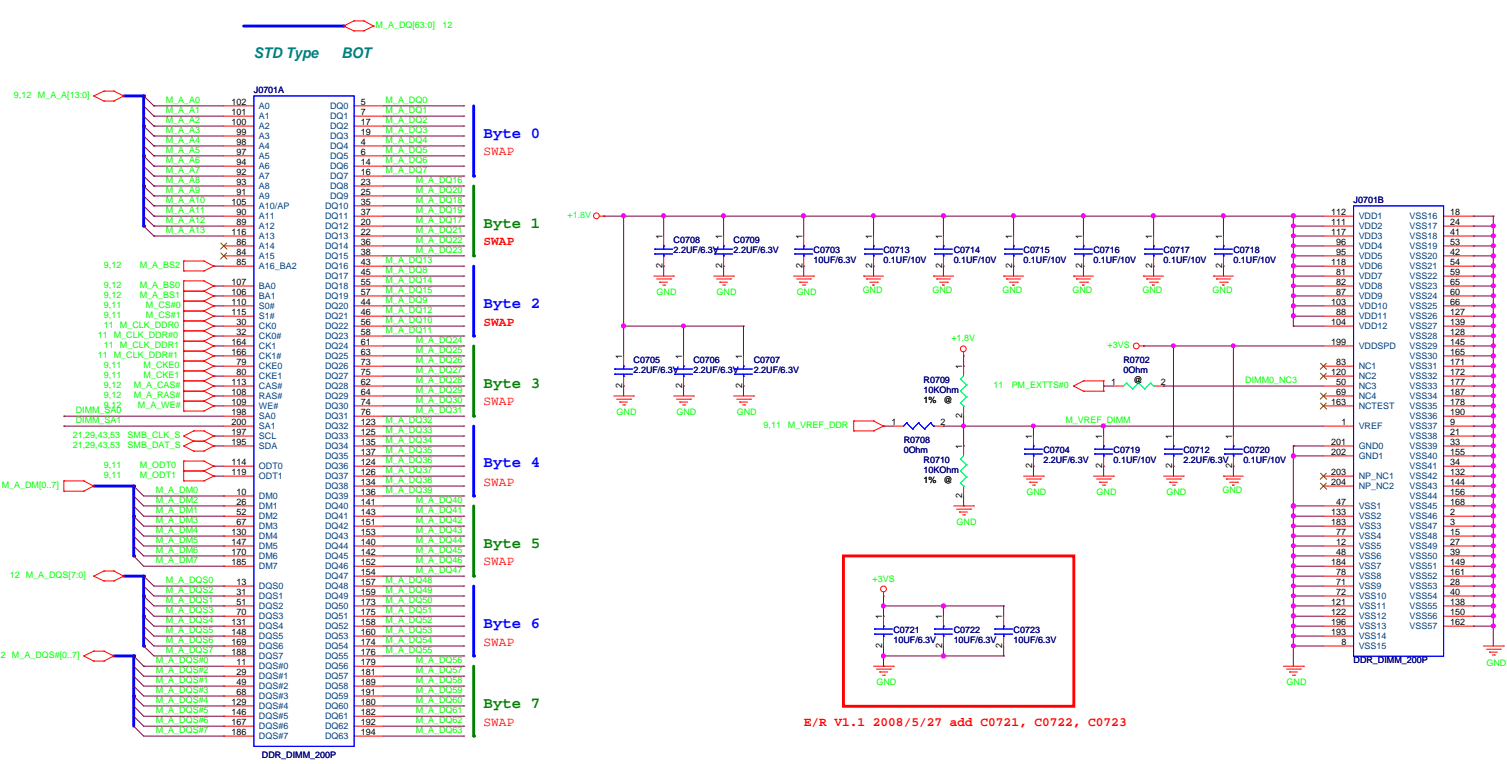
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4

3

2

1



E/R V1.1 2008/5/27 add C0721, C0722, C0723

5

4

3

2

1

D

D

C

C


B

B

A

A

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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
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Custom	N10	1.0	
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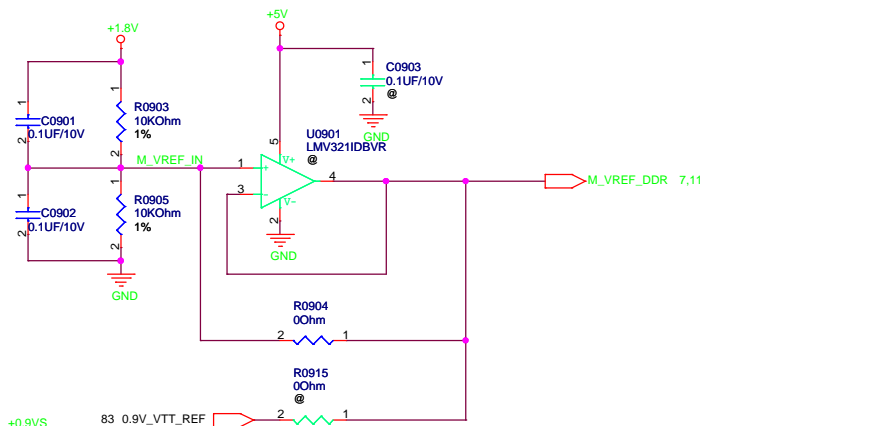
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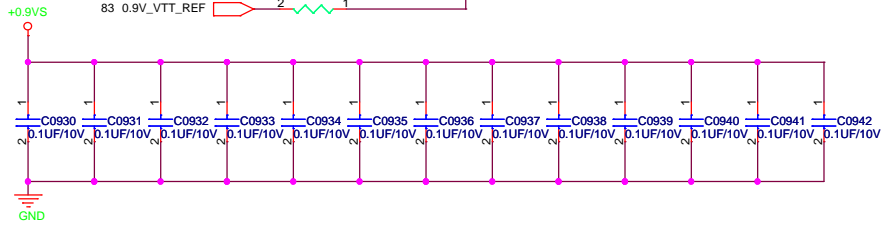
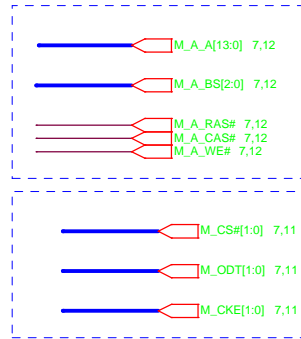
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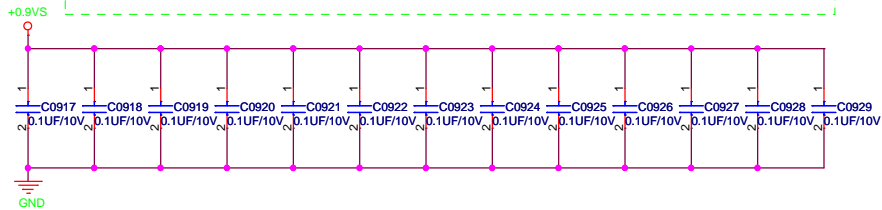
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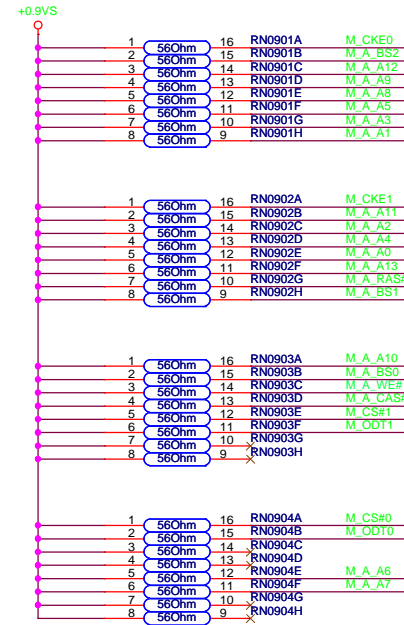
+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve SUSB# and SUSC#






Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



HAD SWAPED

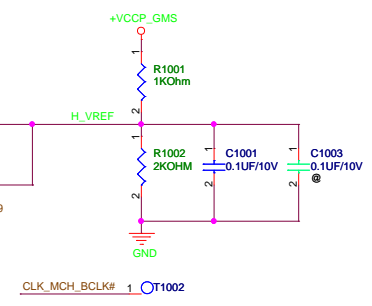
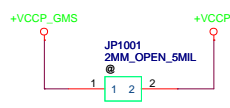
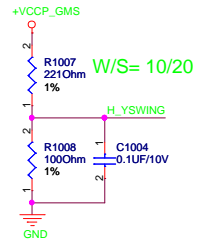
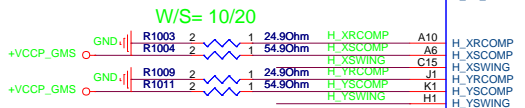
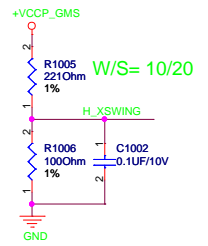


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 3 H_REQ#(4:0)  H_REQ#(4:0)
 3 H_D#(63:0)  H_D#(63:0)


U1001A				
H_D#0	C4	H_D#_0	F8	H_A#3
H_D#1	F6	H_D#_1	D12	H_A#4
H_D#2	H9	H_D#_2	C13	H_A#5
H_D#3	H6	H_D#_3	A6	H_A#6
H_D#4	F7	H_D#_4	E13	H_A#7
H_D#5	E3	H_D#_5	E12	H_A#8
H_D#6	C2	H_D#_6	J12	H_A#9
H_D#7	C3	H_D#_7	B13	H_A#10
H_D#8	K9	H_D#_8	A13	H_A#11
H_D#9	F5	H_D#_9	G13	H_A#12
H_D#10	J7	H_D#_10	A12	H_A#13
H_D#11	K7	H_D#_11	D14	H_A#14
H_D#12	H8	H_D#_12	F14	H_A#15
H_D#13	E5	H_D#_13	J13	H_A#16
H_D#14	K8	H_D#_14	E17	H_A#17
H_D#15	J8	H_D#_15	H15	H_A#18
H_D#16	J2	H_D#_16	G15	H_A#19
H_D#17	J3	H_D#_17	G14	H_A#20
H_D#18	N1	H_D#_18	A15	H_A#21
H_D#19	M5	H_D#_19	B18	H_A#22
H_D#20	K5	H_D#_20	B15	H_A#23
H_D#21	J5	H_D#_21	E14	H_A#24
H_D#22	H3	H_D#_22	H13	H_A#25
H_D#23	J4	H_D#_23	C14	H_A#26
H_D#24	N3	H_D#_24	A17	H_A#27
H_D#25	M4	H_D#_25	E15	H_A#28
H_D#26	M3	H_D#_26	H17	H_A#29
H_D#27	N8	H_D#_27	D17	H_A#30
H_D#28	N6	H_D#_28	G17	H_A#31
H_D#29	K3	H_D#_29		
H_D#30	N9	H_D#_30		
H_D#31	M1	H_D#_31		
H_D#32	V8	H_D#_32		
H_D#33	V9	H_D#_33		
H_D#34	T8	H_D#_34		
H_D#35	R6	H_D#_35		
H_D#36	R2	H_D#_36		
H_D#37	N5	H_D#_37		
H_D#38	N2	H_D#_38		
H_D#39	U7	H_D#_39		
H_D#40	R8	H_D#_40		
H_D#41	T4	H_D#_41		
H_D#42	T7	H_D#_42		
H_D#43	R3	H_D#_43		
H_D#44	T5	H_D#_44		
H_D#45	V6	H_D#_45		
H_D#46	V3	H_D#_46		
H_D#47	V2	H_D#_47		
H_D#48	W1	H_D#_48		
H_D#49	V2	H_D#_49		
H_D#50	W4	H_D#_50		
H_D#51	W7	H_D#_51		
H_D#52	V5	H_D#_52		
H_D#53	V5	H_D#_53		
H_D#54	V8	H_D#_54		
H_D#55	A8	H_D#_55		
H_D#56	V8	H_D#_56		
H_D#57	A9	H_D#_57		
H_D#58	A8	H_D#_58		
H_D#59	AB1	H_D#_59		
H_D#60	AB7	H_D#_60		
H_D#61	AB7	H_D#_61		
H_D#62	AA2	H_D#_62		
H_D#63	AB5	H_D#_63		

HOST

H_ADS#	F10	H_ADS#	H_ADS#_3
H_ADSTB#_0	C12	H_ADSTB#0	H_ADSTB#_3
H_ADSTB#_1	H16	H_ADSTB#1	H_ADSTB#1_3
H_VREF#	E2	H_VREF#	
H_BNR#	C7	H_BNR#	H_BNR#_3
H_BREQ#	G8	H_BREQ#0	H_BREQ#_3
H_CPURST#	B10	H_CPURST#	H_CPURST#_3
H_VREF#	E1	H_VREF#	
CLK_MCH_BCLK#	AA6	CLK_MCH_BCLK#	CLK_MCH_BCLK#_29
CLK_MCH_BCLK	AA5	CLK_MCH_BCLK	CLK_MCH_BCLK_29
H_DBSY#	C10	H_DBSY#	H_DBSY#_3
H_DEFER#	C6	H_DEFER#	H_DEFER#_3
H_DINV#_0	H5	H_DINV#0	H_DINV#_3
H_DINV#_1	J6	H_DINV#1	H_DINV#1_3
H_DINV#_2	T9	H_DINV#2	H_DINV#2_3
H_DINV#_3	U6	H_DINV#3	H_DINV#3_3
H_DPWR#	G7	H_DPWR#	H_DPWR#_3
H_DRDY#	E6	H_DRDY#	H_DRDY#_3
H_DSTBN#_0	F3	H_DSTBN#0	H_DSTBN#_3
H_DSTBN#_1	M8	H_DSTBN#1	H_DSTBN#1_3
H_DSTBN#_2	T1	H_DSTBN#2	H_DSTBN#2_3
H_DSTBN#_3	AA3	H_DSTBN#3	H_DSTBN#3_3
H_DSTBP#_0	F4	H_DSTBP#0	H_DSTBP#_3
H_DSTBP#_1	M7	H_DSTBP#1	H_DSTBP#1_3
H_DSTBP#_2	T2	H_DSTBP#2	H_DSTBP#2_3
H_DSTBP#_3	AB3	H_DSTBP#3	H_DSTBP#3_3
H_HIT#	C8	H_HIT#	H_HIT#_3
H_HITM#	B4	H_HITM#	H_HITM#_3
H_LOCK#	C5	H_LOCK#	H_LOCK#_3
H_REQ#_0	G9	H_REQ#0	
H_REQ#_1	E9	H_REQ#1	
H_REQ#_2	G12	H_REQ#2	
H_REQ#_3	B8	H_REQ#3	
H_REQ#_4	F12	H_REQ#4	
H_RS#_0	A5	H_RS#0	H_RS#0_3
H_RS#_1	B6	H_RS#1	H_RS#1_3
H_RS#_2	G10	H_RS#2	H_RS#2_3
H_CPOUSLP# GMCH	E8	H_CPOUSLP# GMCH	H_RS#2_3
H_TRDY#	E10	H_TRDY#	H_TRDY#_3



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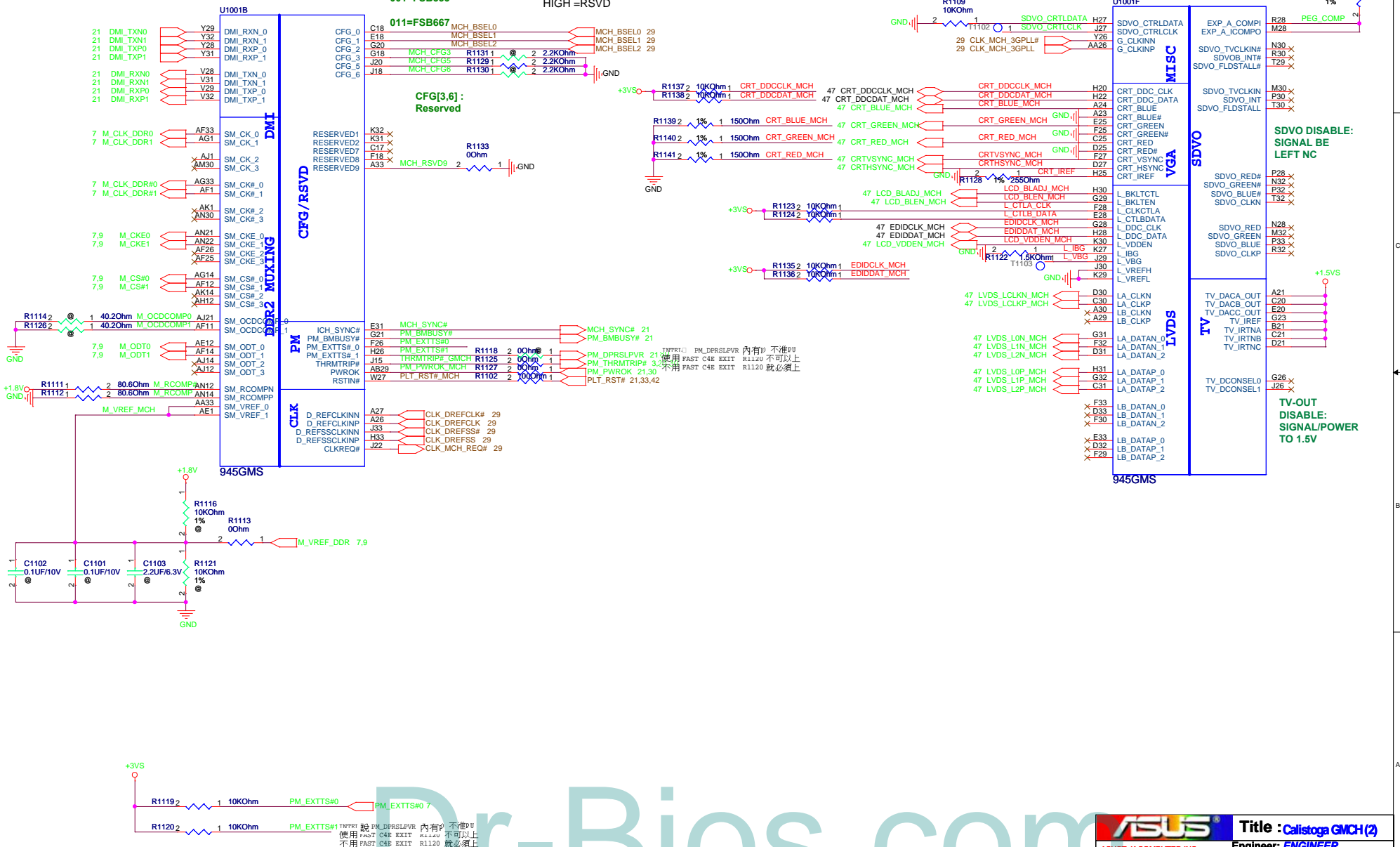
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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
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TX/RX of DMI is viewed from ICH7M

Lane Reversal of DMI is not supported in 945GMS

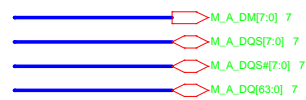
CFG2[2:0]:
001=FSB533

CFG5 : DMI STRAP
LOW = DMI X 2
HIGH =RSVD



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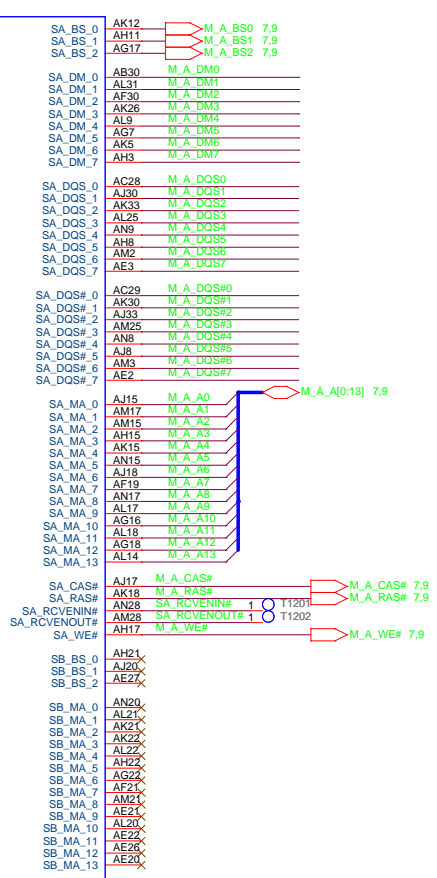
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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
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U1001C

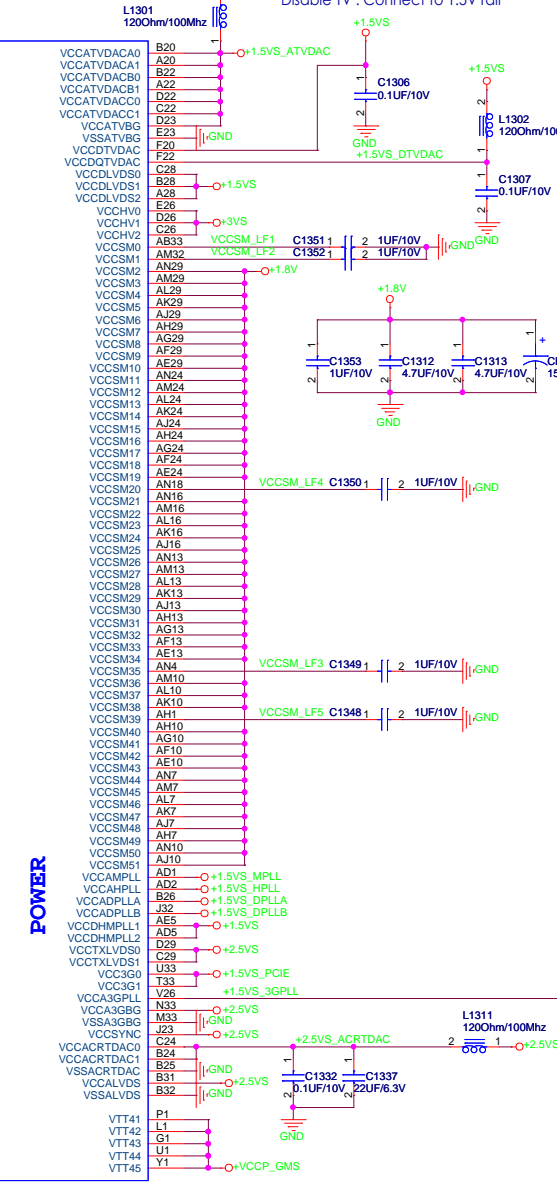
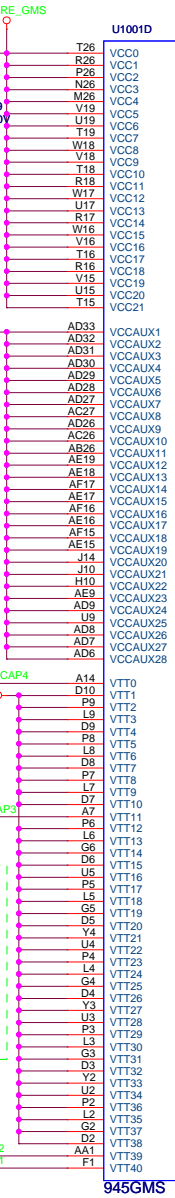
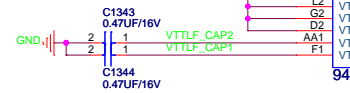
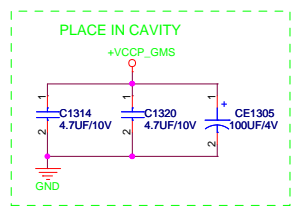
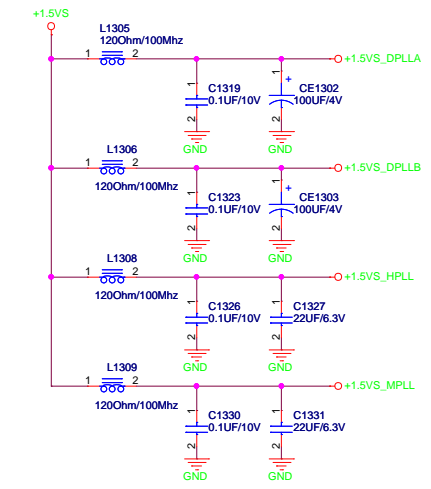
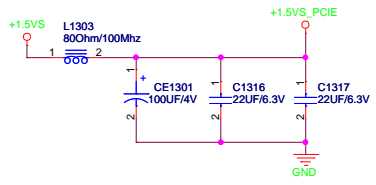
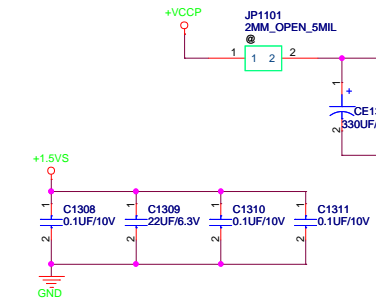
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	M_A_DQ3	AF32	SA_DQ_3
	M_A_DQ4	AC33	SA_DQ_4
	M_A_DQ5	AB32	SA_DQ_5
	M_A_DQ6	AE31	SA_DQ_6
	M_A_DQ7	AE31	SA_DQ_7
	M_A_DQ8	AH31	SA_DQ_8
	M_A_DQ9	AK31	SA_DQ_9
Byte 1	M_A_DQ10	AL28	SA_DQ_10
	M_A_DQ11	AK27	SA_DQ_11
	M_A_DQ12	AH30	SA_DQ_12
	M_A_DQ13	AL32	SA_DQ_13
	M_A_DQ14	AJ28	SA_DQ_14
	M_A_DQ15	AJ27	SA_DQ_15
	M_A_DQ16	AH32	SA_DQ_16
	M_A_DQ17	AF31	SA_DQ_17
Byte 2	M_A_DQ18	AH27	SA_DQ_18
	M_A_DQ19	AF28	SA_DQ_19
	M_A_DQ20	AJ32	SA_DQ_20
	M_A_DQ21	AC31	SA_DQ_21
	M_A_DQ22	AG28	SA_DQ_22
	M_A_DQ23	AG27	SA_DQ_23
	M_A_DQ24	AN27	SA_DQ_24
	M_A_DQ25	AM28	SA_DQ_25
Byte 3	M_A_DQ26	AJ26	SA_DQ_26
	M_A_DQ27	AJ25	SA_DQ_27
	M_A_DQ28	AL27	SA_DQ_28
	M_A_DQ29	AN26	SA_DQ_29
	M_A_DQ30	AH25	SA_DQ_30
	M_A_DQ31	AG26	SA_DQ_31
Byte 4	M_A_DQ32	AM12	SA_DQ_32
	M_A_DQ33	AL11	SA_DQ_33
	M_A_DQ34	AH9	SA_DQ_34
	M_A_DQ35	AK9	SA_DQ_35
	M_A_DQ36	AM11	SA_DQ_36
	M_A_DQ37	AK11	SA_DQ_37
	M_A_DQ38	AM8	SA_DQ_38
	M_A_DQ39	AK8	SA_DQ_39
	M_A_DQ40	AG9	SA_DQ_40
	M_A_DQ41	AF9	SA_DQ_41
	M_A_DQ42	AF8	SA_DQ_42
Byte 5	M_A_DQ43	AK6	SA_DQ_43
	M_A_DQ44	AF7	SA_DQ_44
	M_A_DQ45	AG11	SA_DQ_45
	M_A_DQ46	AJ6	SA_DQ_46
	M_A_DQ47	AH6	SA_DQ_47
	M_A_DQ48	AM6	SA_DQ_48
	M_A_DQ49	AK3	SA_DQ_49
	M_A_DQ50	AK3	SA_DQ_50
Byte 6	M_A_DQ51	AL2	SA_DQ_51
	M_A_DQ52	AM5	SA_DQ_52
	M_A_DQ53	AL5	SA_DQ_53
	M_A_DQ54	AJ3	SA_DQ_54
	M_A_DQ55	AJ2	SA_DQ_55
	M_A_DQ56	AG2	SA_DQ_56
	M_A_DQ57	AF3	SA_DQ_57
	M_A_DQ58	AE7	SA_DQ_58
	M_A_DQ59	AF6	SA_DQ_59
Byte 7	M_A_DQ60	AH8	SA_DQ_60
	M_A_DQ61	AG3	SA_DQ_61
	M_A_DQ62	AG5	SA_DQ_62
	M_A_DQ63	AF5	SA_DQ_63

DDR2 SYSTEM MEMORY



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		Title : Calistoga GMCH (3)	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
Custom	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	12 of 97

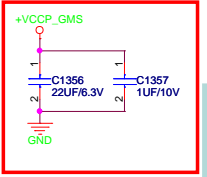
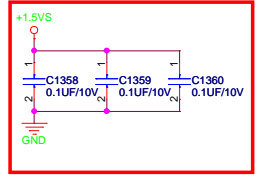


Close to Pin A28,B28,C28

Close to Pin C26,D26,E26

E/R V1.1 2008/5/28 add C1315, C1361, C1362

E/R V1.1 2008/5/28 add C1358, C1359, C1360



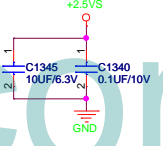
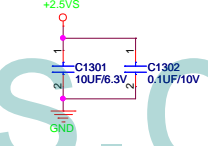
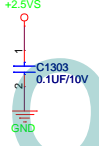
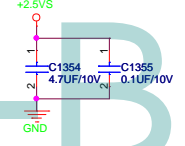
E/R V1.1 2008/5/28 add C1356, C1357

Close to Pin N33

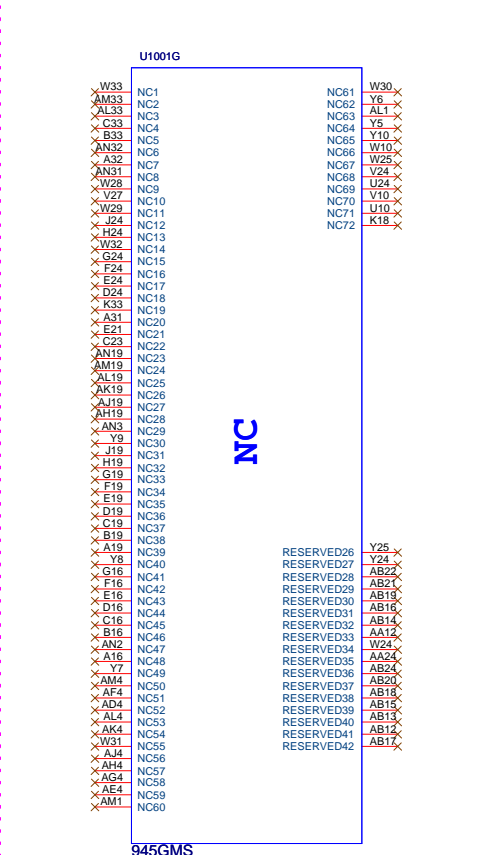
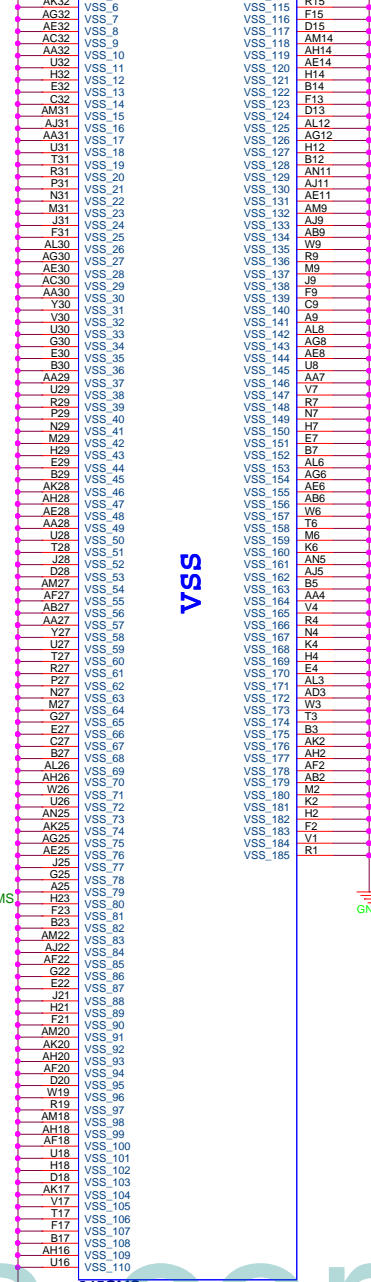
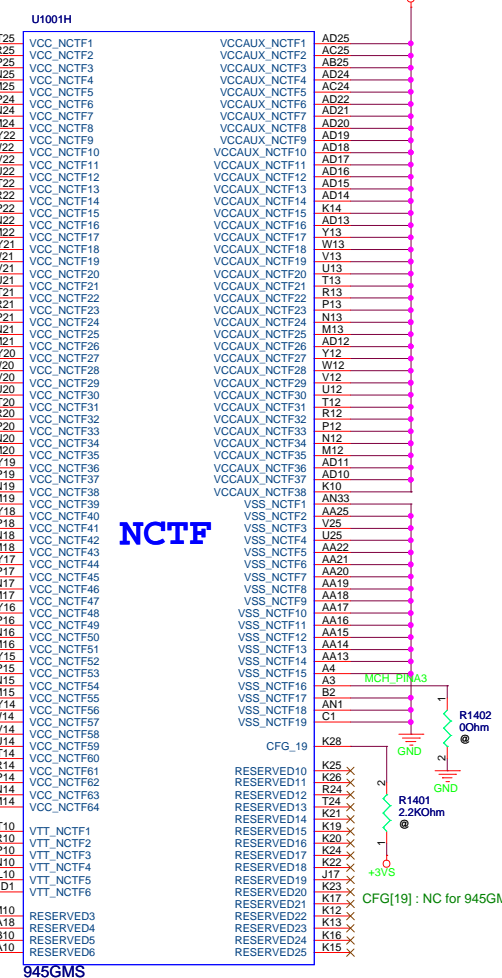
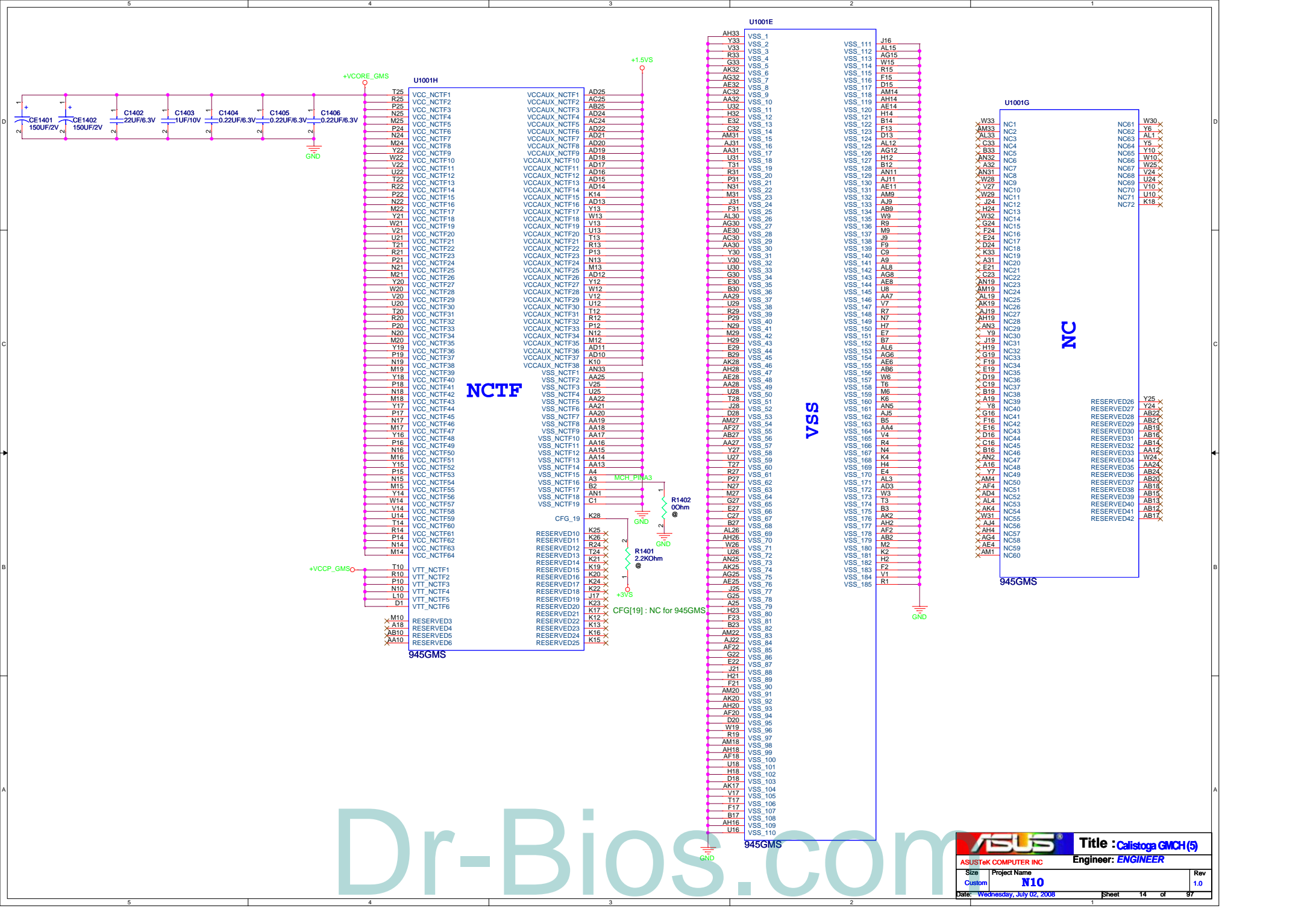
Close to Pin C29,D29

Close to Pin B31

Close to Pin J23



ASUS Title: Calistoga GMCH(4)
 ASUSTeK COMPUTER INC Engineer: ENGINEER
 Size: Project Name
 Custom: N10
 Date: Wednesday, July 02, 2008 Sheet 13 of 97



NCTF

VSS

NC


945GMS

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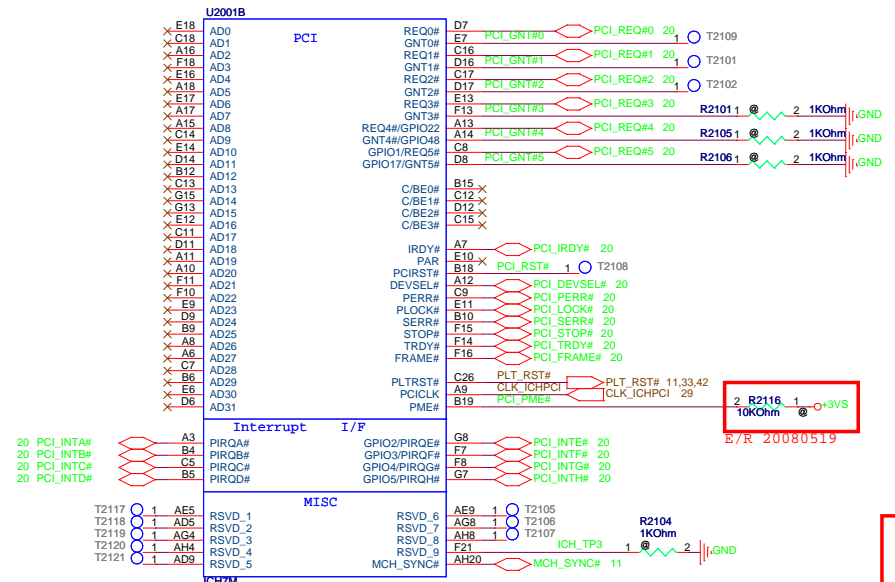
ASUS Title : Calistoga GMCH (5)
 ASUSTeK COMPUTER INC Engineer: ENGINEER
 Size: Custom Project Name: N10 Rev: 1.0
 Date: Wednesday, July 02, 2008 Sheet: 14 of 97



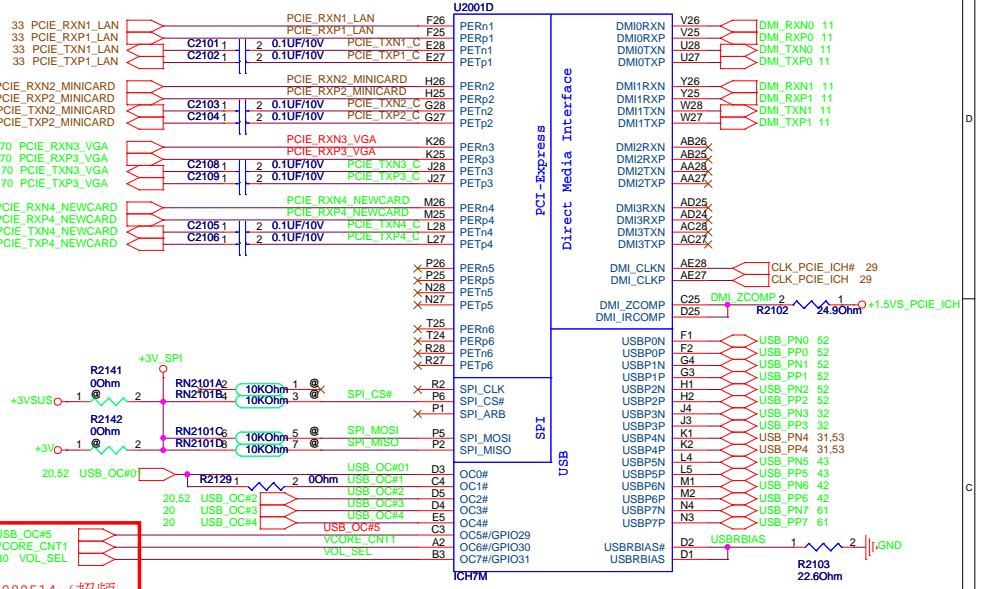
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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
A	N10		1.0
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			1

U2001B
 REQ0# D7 PCT_GNT#0 PCI_REQ#0 20 T2109
 REQ1# E7 PCT_GNT#0 PCI_REQ#1 20 T2101
 REQ2# C16 PCT_GNT#1 PCI_REQ#2 20 T2102
 REQ3# C17 PCT_GNT#2 PCI_REQ#3 20 R2101 10Kohm
 REQ4# C17 PCT_GNT#3 PCI_REQ#4 20 R2105 10Kohm
 REQ5# F13 PCT_GNT#4 PCI_REQ#5 20 R2106 10Kohm



TX/RX of DMI is viewed from ICH7M Lane Reversal of DMI is not supported in 945GMS

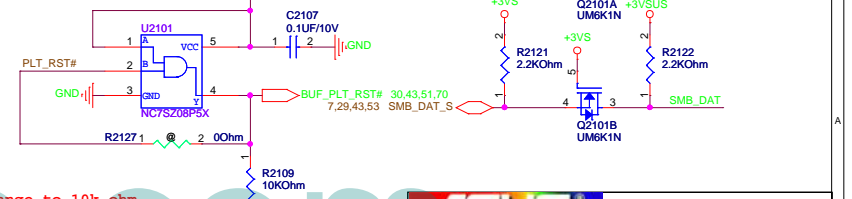
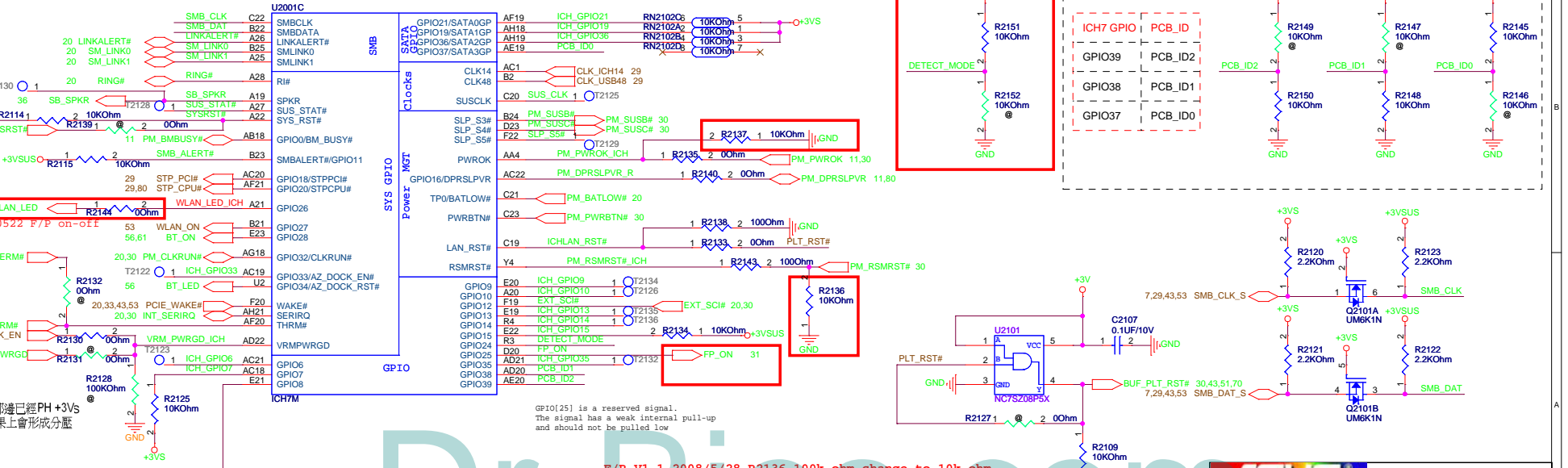


E/R V1.1 2008/5/28 R2137 100k ohm change to 10k ohm

P/R V2.0 2008/7/01 when mount R2151 --> N10J
 P/R V2.0 2008/7/01 when mount R2152 --> N10E

SPKR signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

SWAP

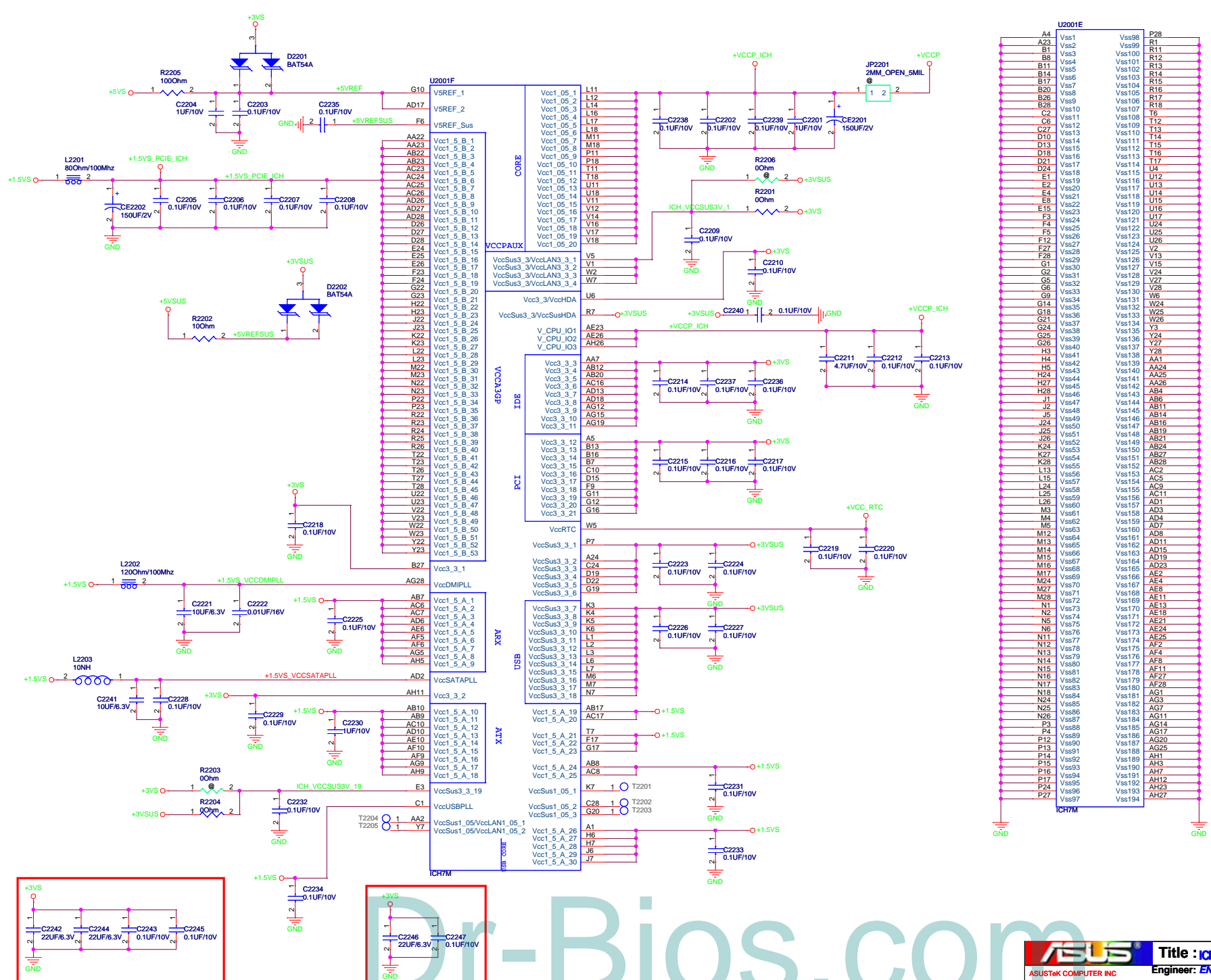


E/R V1.1 2008/5/28 R2136 100k ohm change to 10k ohm

P/R V2.0 2008/6/29 GPIO25 change to FP_ON

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ASUS ASUSTeK COMPUTER INC		Title : ICH7M2	Engineer: ENGINEER
Size Custom	Project Name N10	Date: Wednesday, July 02, 2008	Rev 1.0
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U2001E	
A4	Vss1
A23	Vss2
B1	Vss3
B8	Vss4
B11	Vss5
B14	Vss6
B17	Vss7
B20	Vss8
B28	Vss9
C6	Vss10
C27	Vss12
D10	Vss14
D13	Vss15
D18	Vss16
D21	Vss17
D24	Vss18
E1	Vss19
E2	Vss20
E4	Vss21
E8	Vss22
F3	Vss23
F4	Vss24
F5	Vss25
F12	Vss26
F27	Vss27
F28	Vss28
G1	Vss29
G2	Vss30
G5	Vss31
G6	Vss32
G8	Vss33
G14	Vss34
G18	Vss35
G36	Vss36
G37	Vss37
G41	Vss38
G25	Vss39
G26	Vss40
H5	Vss41
H4	Vss42
H5	Vss43
H24	Vss44
H27	Vss45
H28	Vss46
J1	Vss47
J5	Vss48
J4	Vss49
J25	Vss50
J26	Vss51
K24	Vss52
K27	Vss53
K28	Vss54
L13	Vss55
L15	Vss56
L24	Vss57
L25	Vss58
L26	Vss59
M3	Vss60
M4	Vss61
M5	Vss62
M12	Vss63
M13	Vss64
M14	Vss65
M15	Vss66
M16	Vss67
M17	Vss68
M24	Vss69
M27	Vss70
M28	Vss71
N1	Vss72
N2	Vss73
N5	Vss74
N6	Vss75
N6	Vss76
N11	Vss77
N14	Vss78
N13	Vss79
N14	Vss80
N16	Vss81
N18	Vss82
N17	Vss83
N24	Vss84
P3	Vss85
P4	Vss86
P12	Vss87
P13	Vss88
P14	Vss89
P15	Vss90
P16	Vss91
P17	Vss92
P24	Vss93
P27	Vss94
P27	Vss95
P27	Vss96
P27	Vss97
P28	Vss98
R1	Vss99
R11	Vss100
R12	Vss101
R13	Vss102
R14	Vss103
R15	Vss104
R16	Vss105
R17	Vss106
R18	Vss107
T6	Vss108
T12	Vss109
T13	Vss110
T14	Vss111
T15	Vss112
T16	Vss113
T17	Vss114
T18	Vss115
T19	Vss116
T20	Vss117
T21	Vss118
T22	Vss119
T23	Vss120
T24	Vss121
T25	Vss122
T26	Vss123
T27	Vss124
T28	Vss125
T29	Vss126
T30	Vss127
T31	Vss128
T32	Vss129
T33	Vss130
T34	Vss131
T35	Vss132
T36	Vss133
T37	Vss134
T38	Vss135
T39	Vss136
T40	Vss137
T41	Vss138
T42	Vss139
T43	Vss140
T44	Vss141
T45	Vss142
T46	Vss143
T47	Vss144
T48	Vss145
T49	Vss146
T50	Vss147
T51	Vss148
T52	Vss149
T53	Vss150
T54	Vss151
T55	Vss152
T56	Vss153
T57	Vss154
T58	Vss155
T59	Vss156
T60	Vss157
T61	Vss158
T62	Vss159
T63	Vss160
T64	Vss161
T65	Vss162
T66	Vss163
T67	Vss164
T68	Vss165
T69	Vss166
T70	Vss167
T71	Vss168
T72	Vss169
T73	Vss170
T74	Vss171
T75	Vss172
T76	Vss173
T77	Vss174
T78	Vss175
T79	Vss176
T80	Vss177
T81	Vss178
T82	Vss179
T83	Vss180
T84	Vss181
T85	Vss182
T86	Vss183
T87	Vss184
T88	Vss185
T89	Vss186
T90	Vss187
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T92	Vss189
T93	Vss190
T94	Vss191
T95	Vss192
T96	Vss193
T97	Vss194

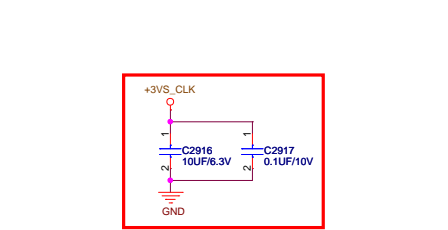
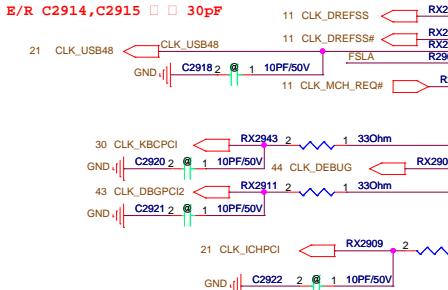
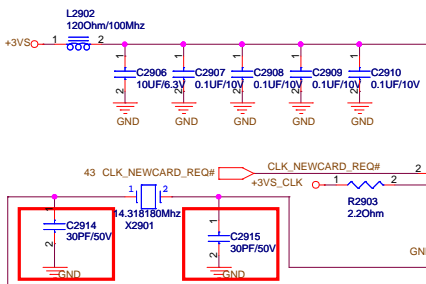
E/R V1.1 2008/5/28 add C2242, C2243, C2244, C2245

E/R V1.1 2008/5/28 add C2246, C2247

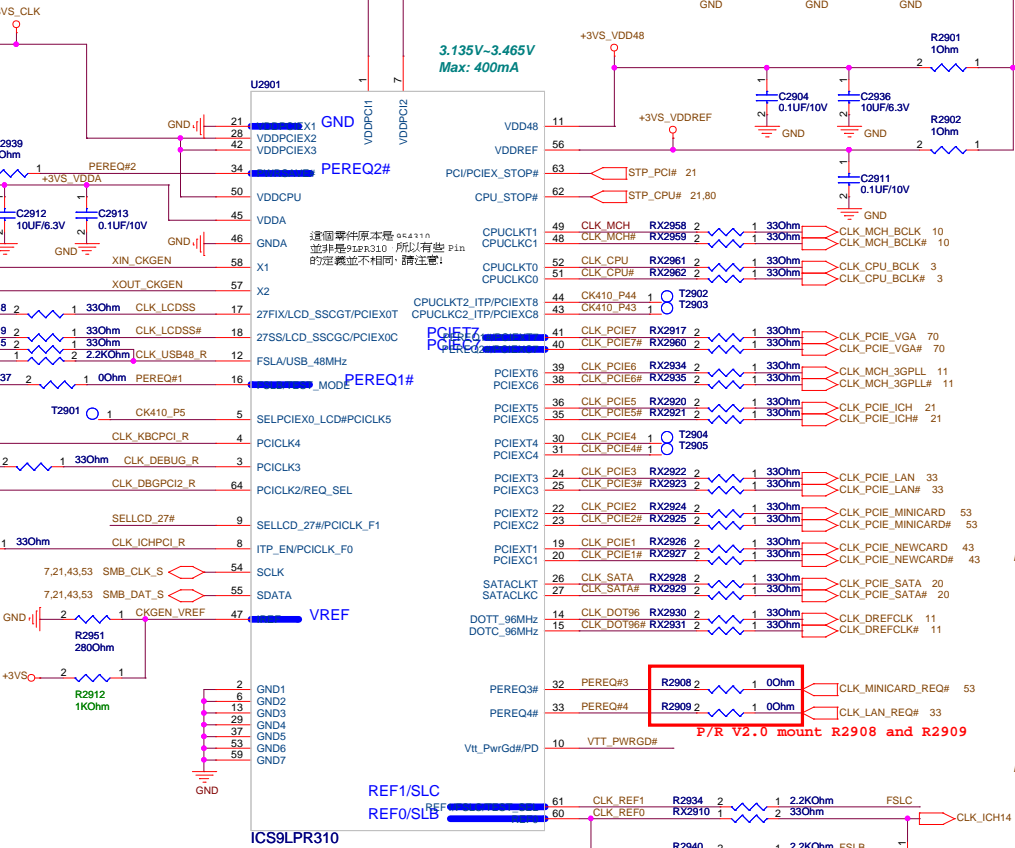
ASUS Title: ICH7M(3)
 ASUSTek COMPUTER INC Engineer: ENGINEER
 Size Project Name
 Custom **N10**
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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
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			1



E/R V1.1 2008/5/28 add C2916 C2917



PEREQ#1 0 = Enable control PCIEX6/0
1 = Disable PCIEX6/0 Controlled

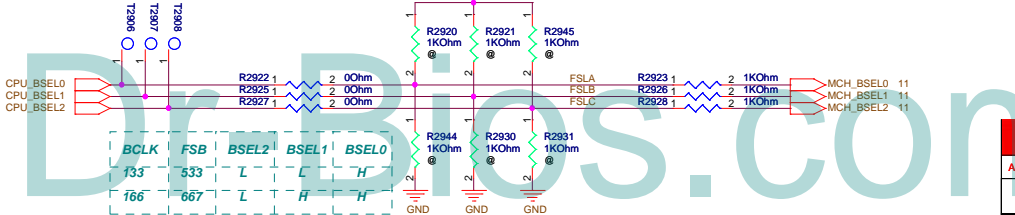
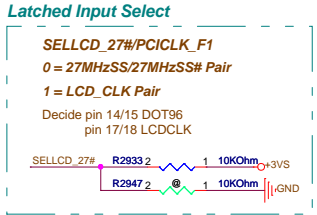
P/R V2.0 unmount R2913, R2916, R2918

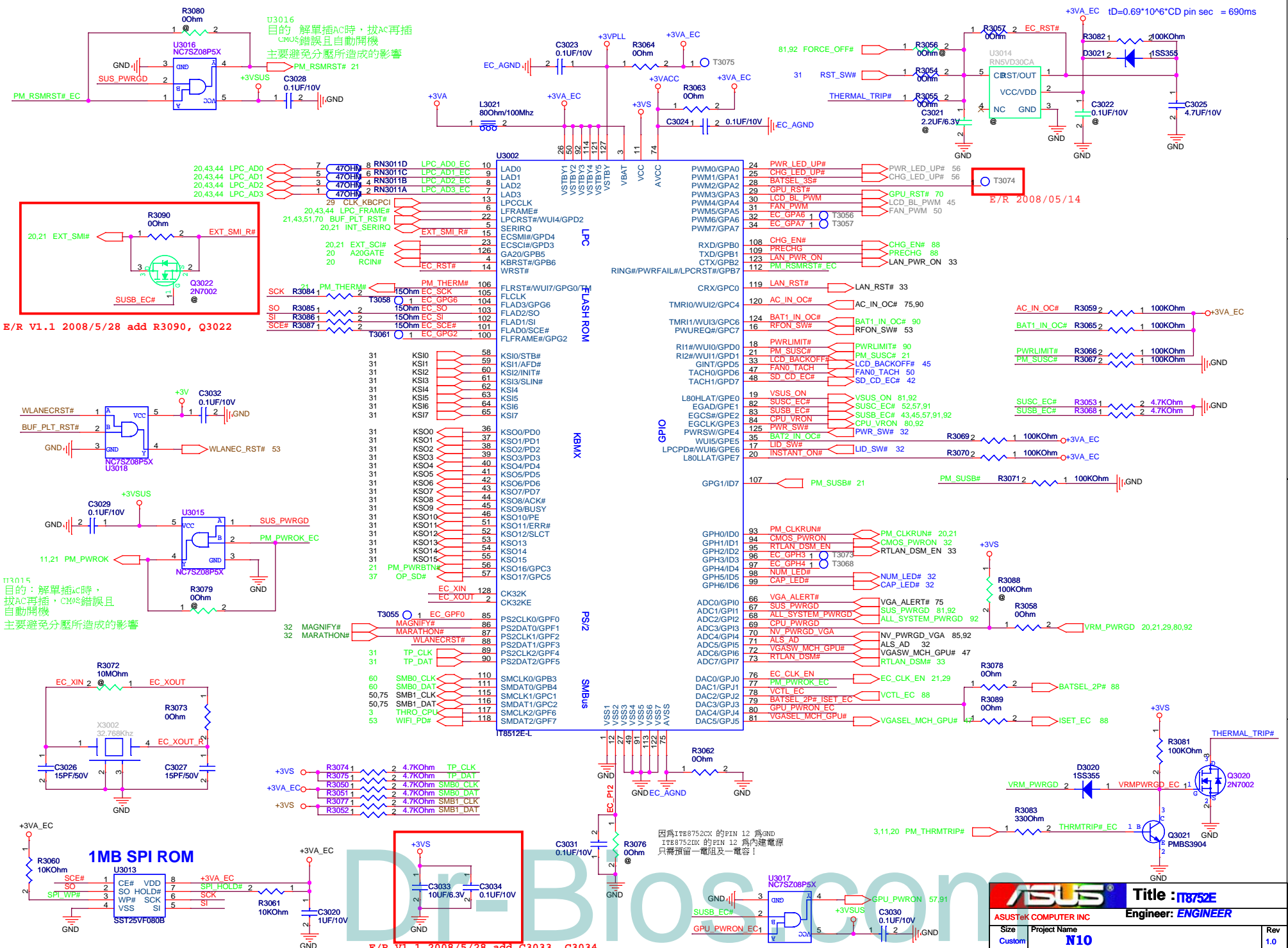
PEREQ#2 0 = Enable control PCIEX8/1
1 = Disable PCIEX8/1 Controlled

PEREQ#3 0 = Enable control PCIEX4/2
1 = Disable PCIEX4/2 Controlled

PEREQ#4 0 = Enable control PCIEX7/5/3
1 = Disable PCIEX7/5/3 Controlled

P/R V2.0 add R2932, unmount R2929





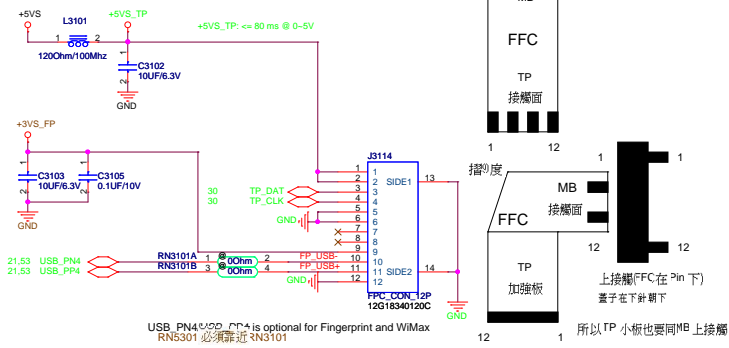
E/R V1.1 2008/5/28 add R3090, Q3022

E/R V1.1 2008/5/28 add C3033, C3034

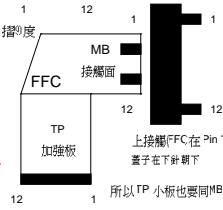
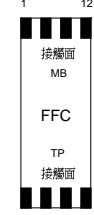
因為TP87520X的PIN 12 為GND
TP87520Z的PIN 12 為內建電容
只需預留一阻及一電容!

E/R 2008/05/14

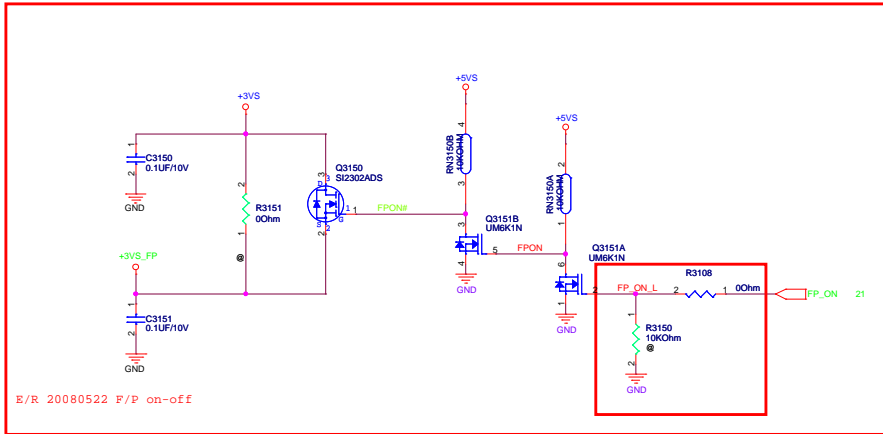
TOUCHPAD FPC



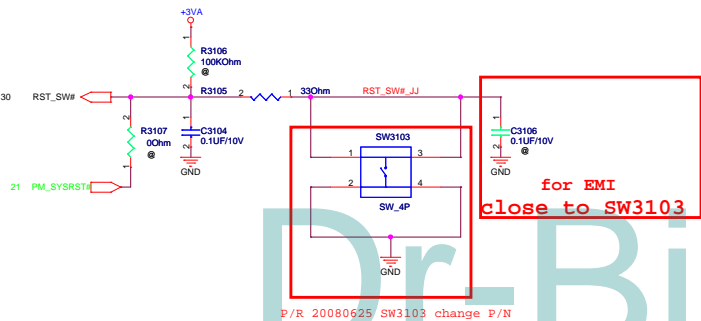
製作 FFC 時要提醒 PCB 標示 TP/MB 文字面以利組裝



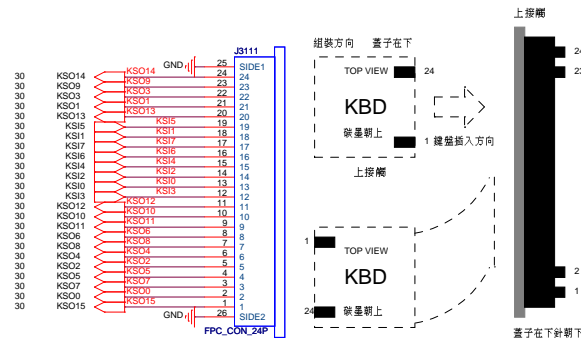
上接觸(FFC在Pin下)
蓋子在針朝下
所以TP小板也要同MB上接觸



RESET BUTTON



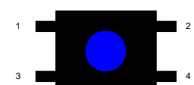
INTERNAL KEYBOARD



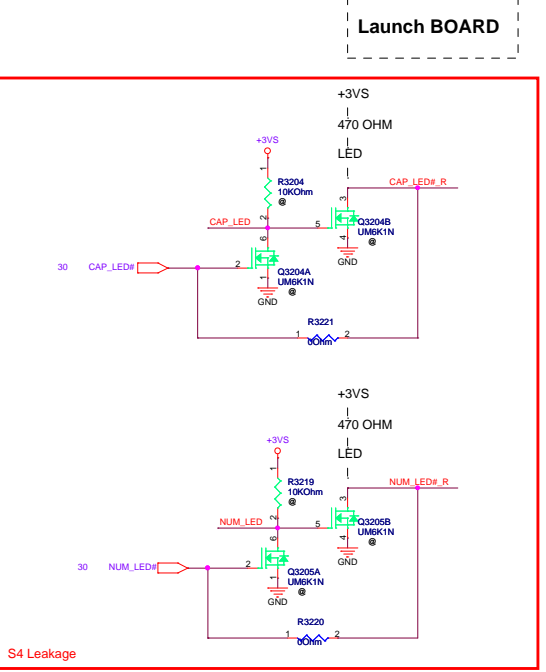
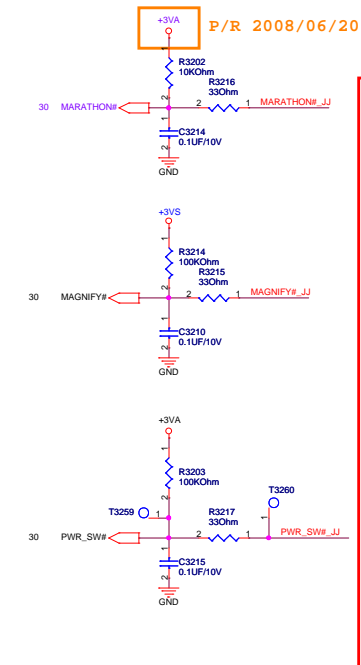
KSO14	D3101	1	2	EGAI0603V05A1@
KSO9	D3102	1	2	EGAI0603V05A1@
KSO3	D3103	1	2	EGAI0603V05A1@
KSO1	D3104	1	2	EGAI0603V05A1@
KSO13	D3105	1	2	EGAI0603V05A1@
KSI5	D3106	1	2	EGAI0603V05A1@
KSI1	D3107	1	2	EGAI0603V05A1@
KSI7	D3108	1	2	EGAI0603V05A1@
KSI6	D3109	1	2	EGAI0603V05A1@
KSI4	D3110	1	2	EGAI0603V05A1@
KSI2	D3111	1	2	EGAI0603V05A1@
KSI0	D3112	1	2	EGAI0603V05A1@
KSI3	D3113	1	2	EGAI0603V05A1@
KSO12	D3114	1	2	EGAI0603V05A1@
KSO10	D3115	1	2	EGAI0603V05A1@
KSO11	D3116	1	2	EGAI0603V05A1@
KSO6	D3117	1	2	EGAI0603V05A1@
KSO8	D3118	1	2	EGAI0603V05A1@
KSO4	D3119	1	2	EGAI0603V05A1@
KSO2	D3120	1	2	EGAI0603V05A1@
KSO5	D3121	1	2	EGAI0603V05A1@
KSO7	D3122	1	2	EGAI0603V05A1@
KSO0	D3123	1	2	EGAI0603V05A1@
KSO15	D3124	1	2	EGAI0603V05A1@

為使Layout 簡潔 ESD在BOM可改成同包裝0603電容

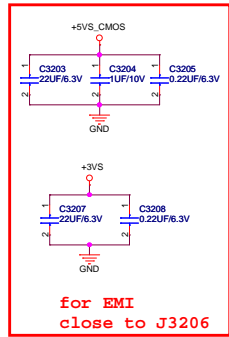
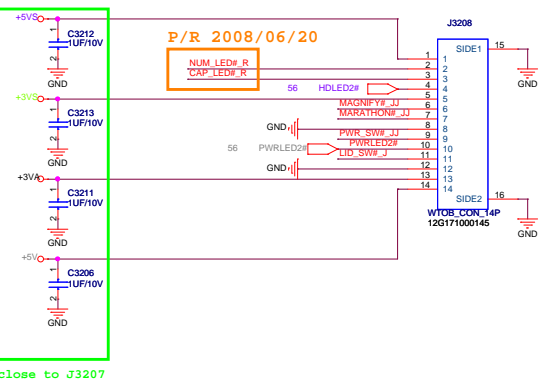
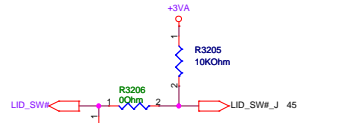
for EMI
close to J3111



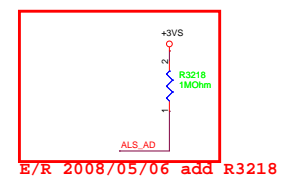
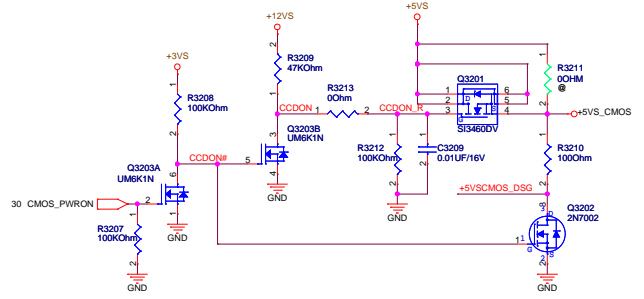
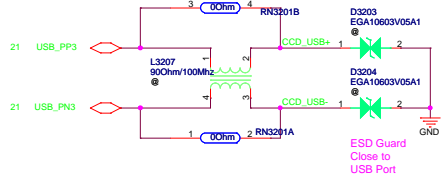
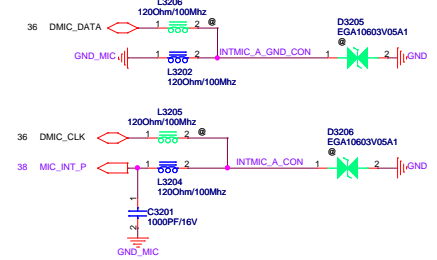
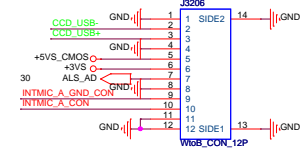
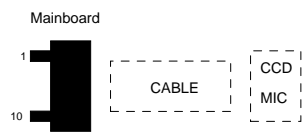
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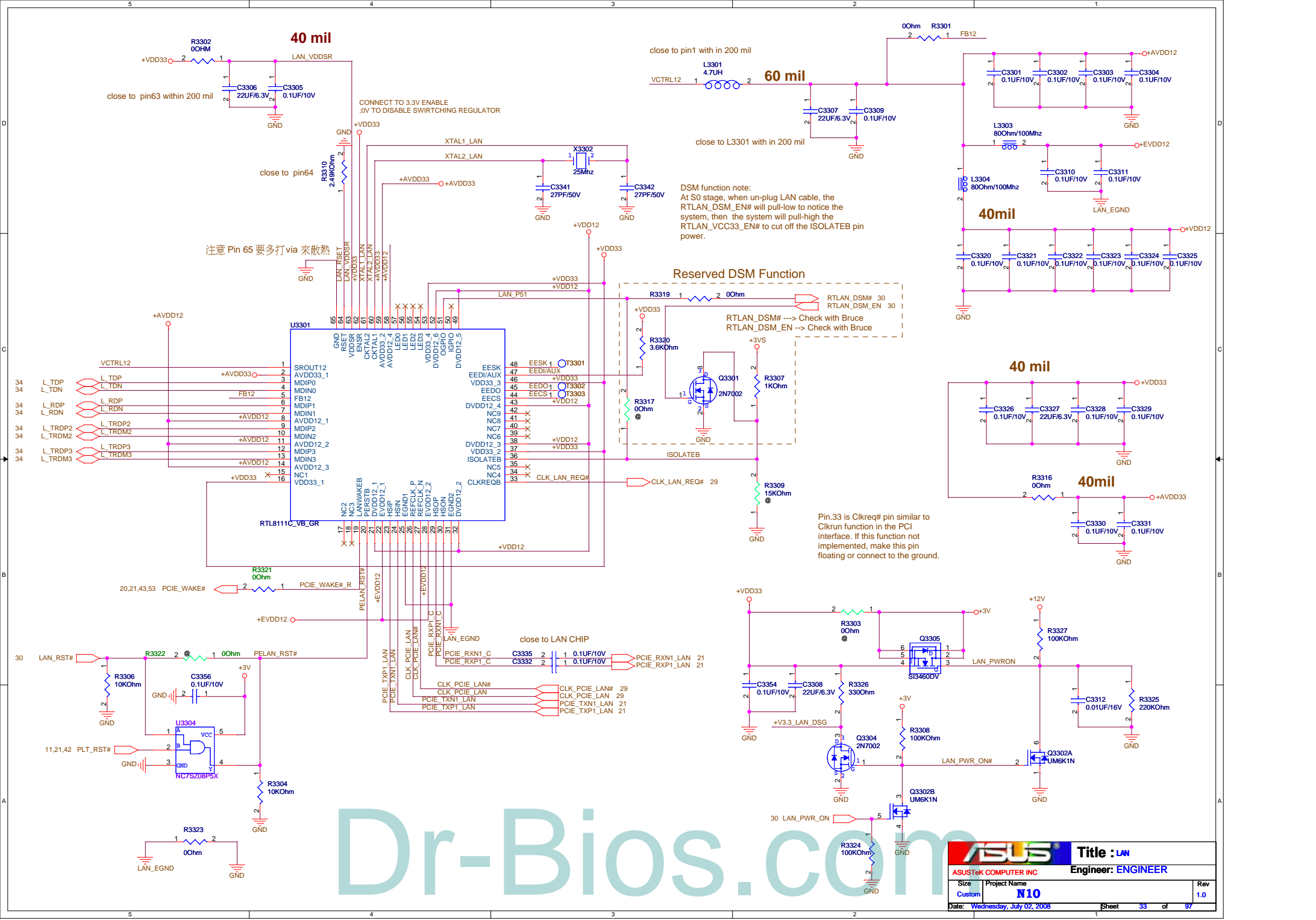
E/R 2008/05/06



CAMERA BOARD



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40 mil

60 mil

40mil

40 mil

40mil

Reserved DSM Function

DSM function note:
At S0 stage, when un-plug LAN cable, the
RTLAN_DSM_EN# will pull-low to notice the
system, then the system will pull-high the
RTLAN_VCC33_EN# to cut off the ISOLATEB pin
power.

Pin.33 is Clkreq# pin similar to
Clkrun function in the PCI
interface. If this function not
implemented, make this pin
floating or connect to the ground.

注意 Pin 65 要多打 via 來散熱

close to LAN CHIP

close to L3301 with in 200 mil

close to pin1 with in 200 mil

close to pin63 within 200 mil

close to pin64

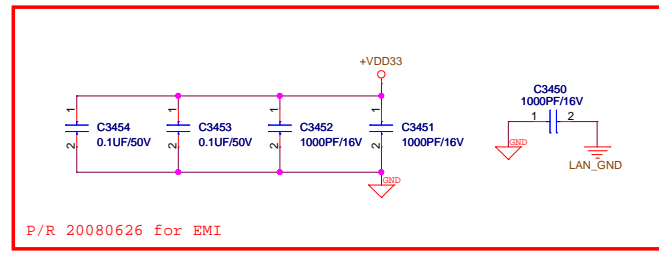
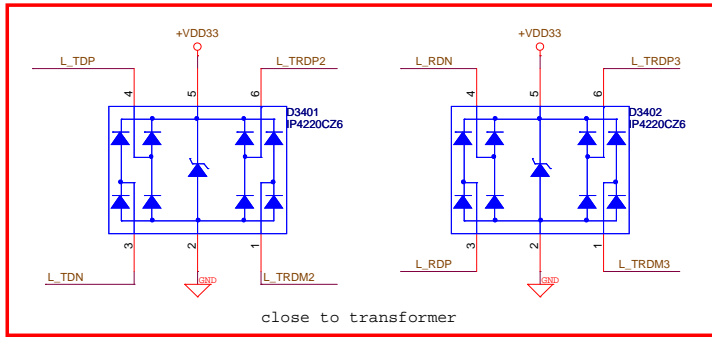
CONNECT TO 3.3V ENABLE
:0V TO DISABLE SWITCHING REGULATOR

close to LAN CHIP

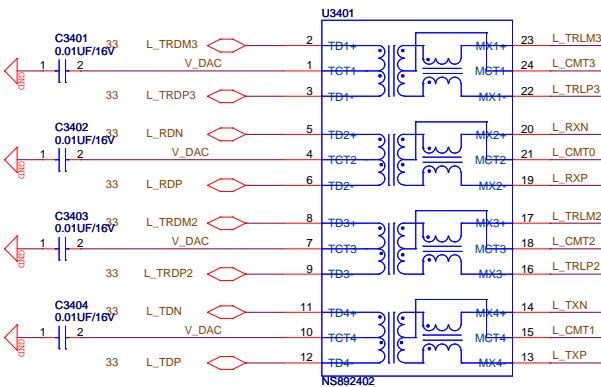
ASUS		Title : LAN
ASUSTeK COMPUTER INC		Engineer: ENGINEER
Size	Project Name	Rev
Custom	N10	1.0
Date: Wednesday, July 02, 2008		Sheet 33 of 97

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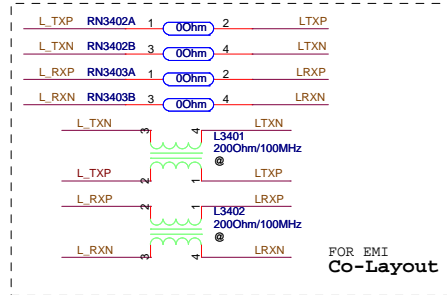
P/R 20080630 SWAP D3401(pin1, pin6) and D3402(pin3, pin4)



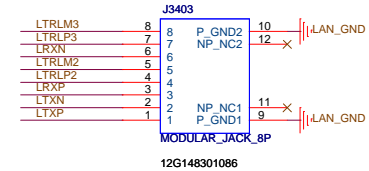
P/R 20080626 for EMI



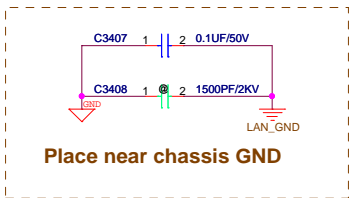
Transformer close to J3401



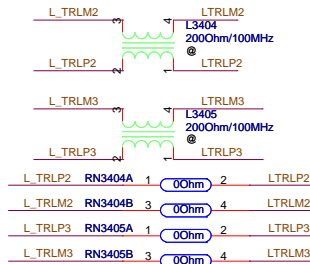
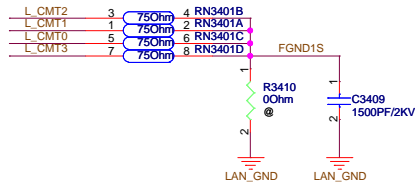
FOR EMI Co-Layout



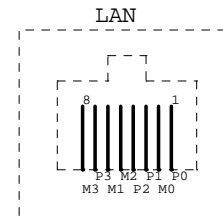
12G148301086



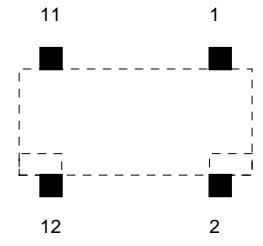
Place near chassis GND




FOR EMI Co-Layout



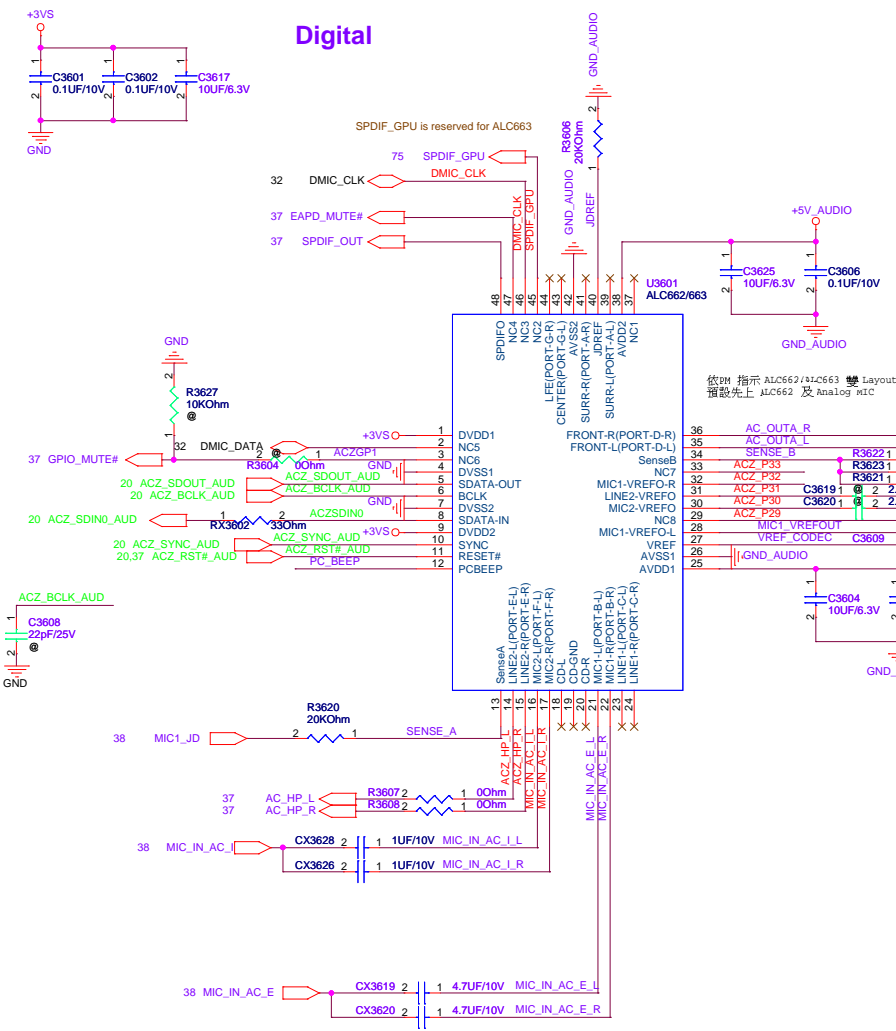
MDC



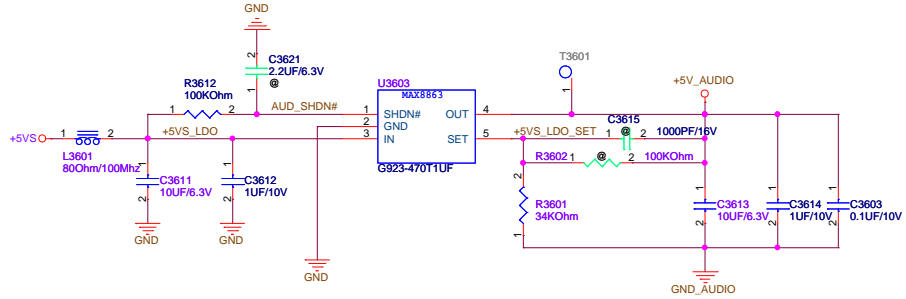
Dr-Bios.com

		Title : MDC	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size A	Project Name N10	Date: Wednesday, July 02, 2008	Rev 1.0
Date: Wednesday, July 02, 2008		Sheet	35 of 97

Digital

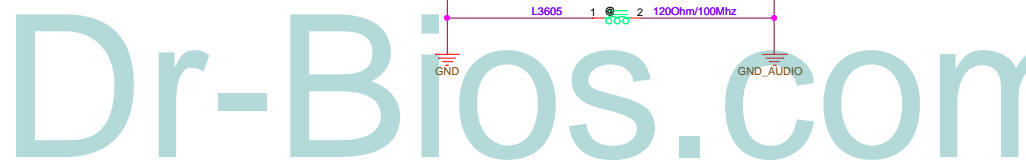
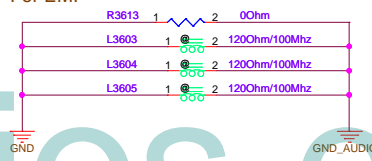


AUD_SHDN# For ALC663 power-on sequence

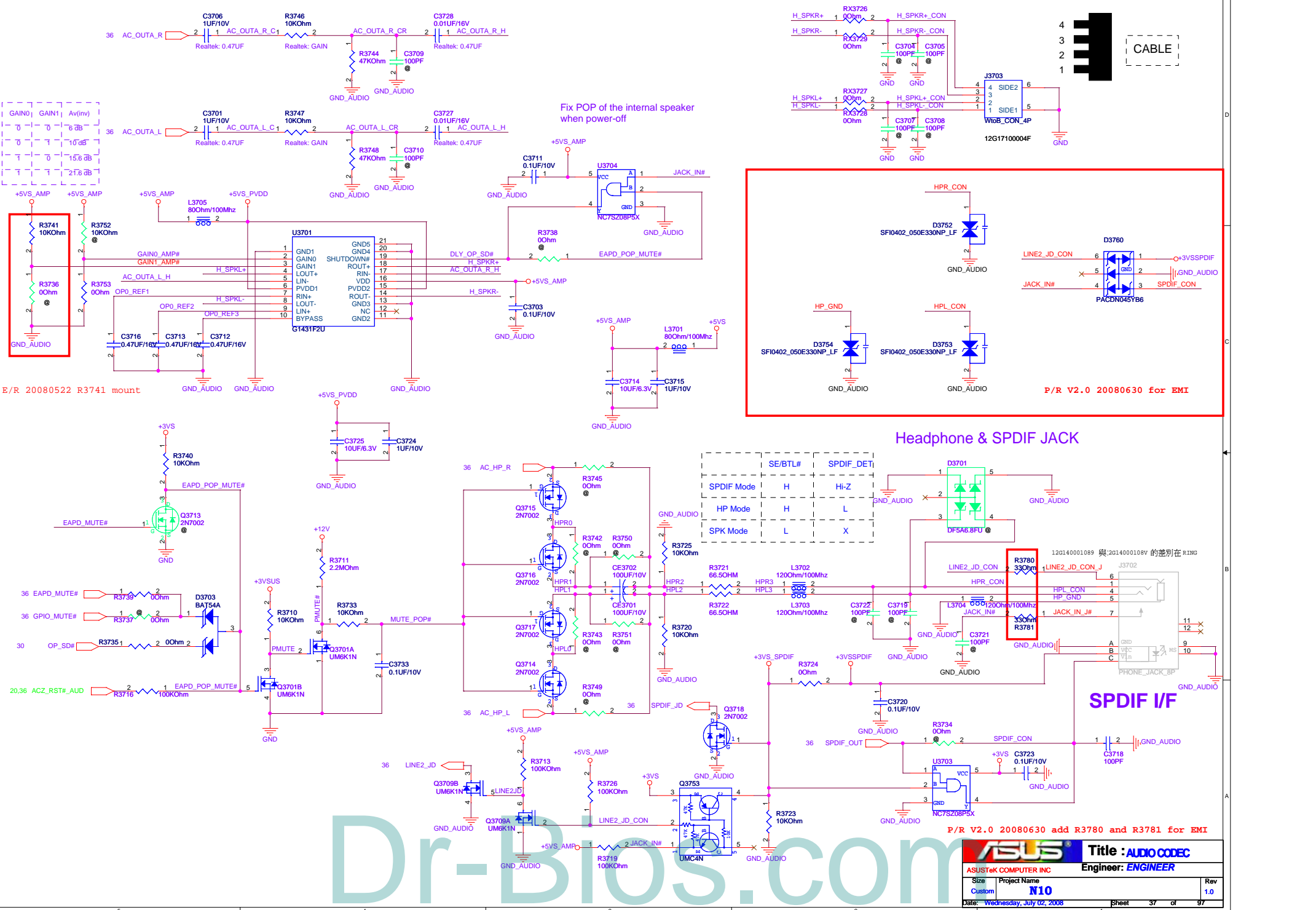


R3601 is 34KOHM(10G213340213010) for MAX8863
 R3601 is 0 OHM(10G213340213010) for GMT923

For EMI



ASUS		Title : AUDIO CODEC	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
Custom	N10		1.0
Date: Wednesday, July 02, 2008		Sheet 36	of 97



E/R 20080522 R3741 mount

Fix POP of the internal speaker when power-off

Headphone & SPDIF JACK

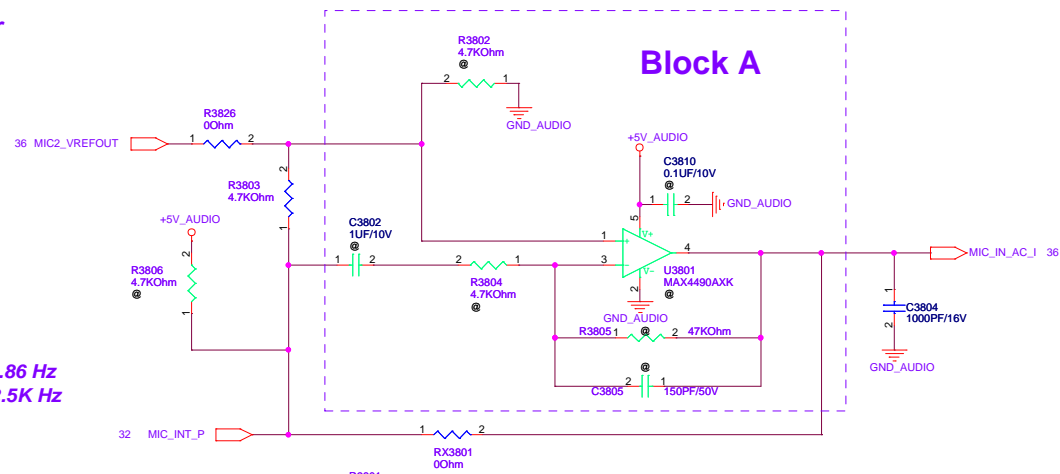
SPDIF I/F

P/R V2.0 20080630 add R3780 and R3781 for EMI

SE/BTL#	SPDIF_DET
SPDIF Mode	H Hi-Z
HP Mode	H L
SPK Mode	L X

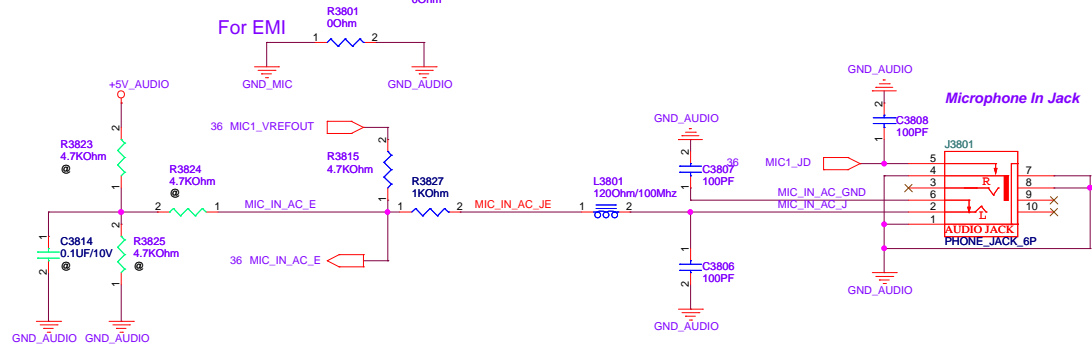
ASUS Title: AUDIO CODEC	
ASUS TeK COMPUTER INC	Engineer: ENGINEER
Size: Custom	Project Name: N10
Date: Wednesday, July 02, 2008	Rev: 1.0
Sheet 37 of 97	

Internal MIC Pre-Amplifier



(Microphone)FL = 33.86 Hz
 (Microphone)FH = 22.5K Hz

External MIC




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ASUS		Title : MICROPHONE	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
Date: Wednesday, July 02, 2008		Sheet	38 of 97



Dr-Bios.com

		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
A	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	39 of 97
			1

xD Pin-assignment

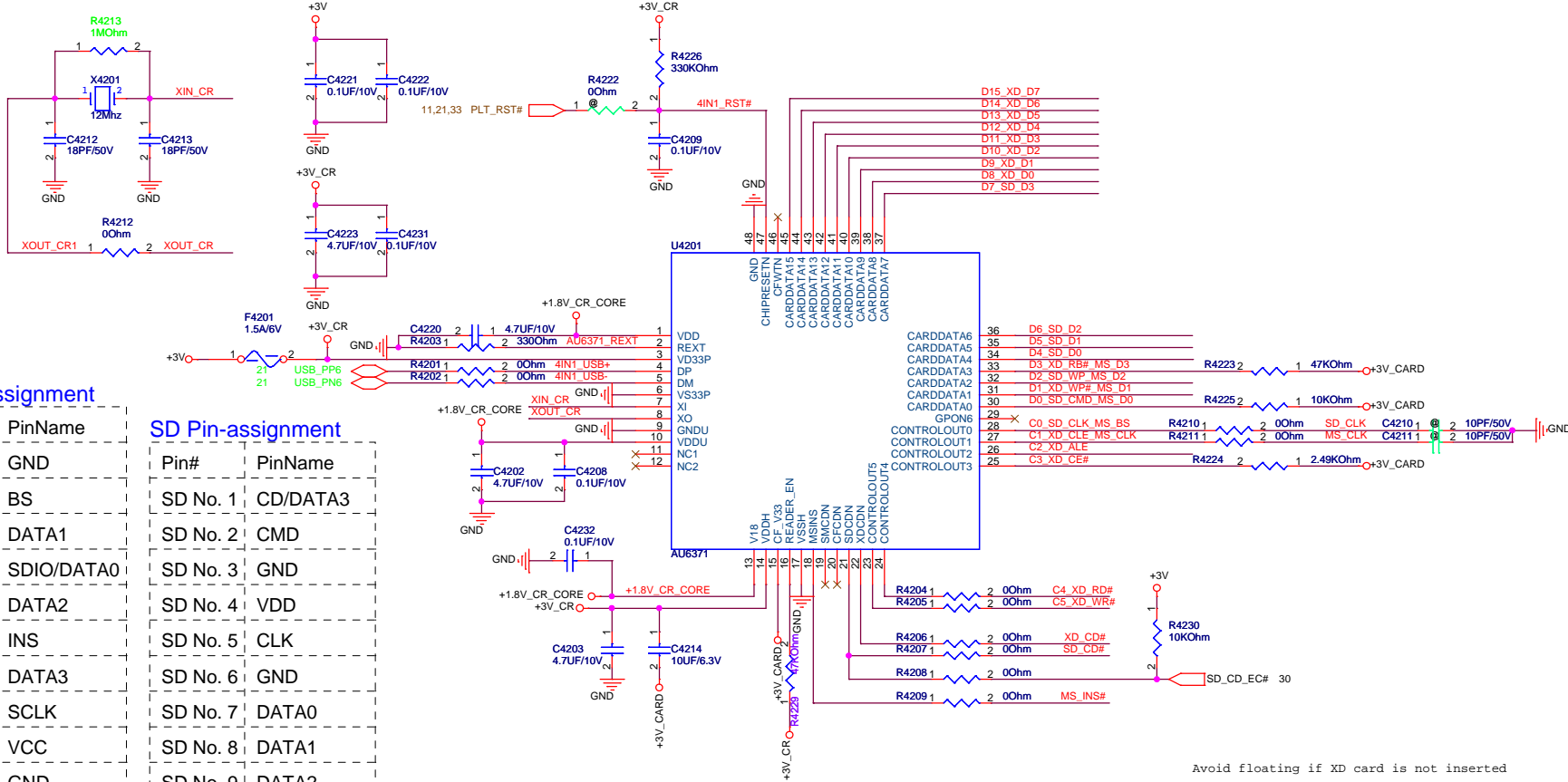
Pin#	PinName
Xd No. 0	CD
Xd No. 1	GND
Xd No. 2	R/-B
Xd No. 3	-RE
Xd No. 4	-CE
Xd No. 5	CLE
Xd No. 6	ALE
Xd No. 7	-WE
Xd No. 8	-WP
Xd No. 9	GND
Xd No.10	D0
Xd No.11	D1
Xd No.12	D2
Xd No.13	D3
Xd No.14	D4
Xd No.15	D5
Xd No.16	D6
Xd No.17	D7
Xd No.18	VCC

MS Pin-assignment

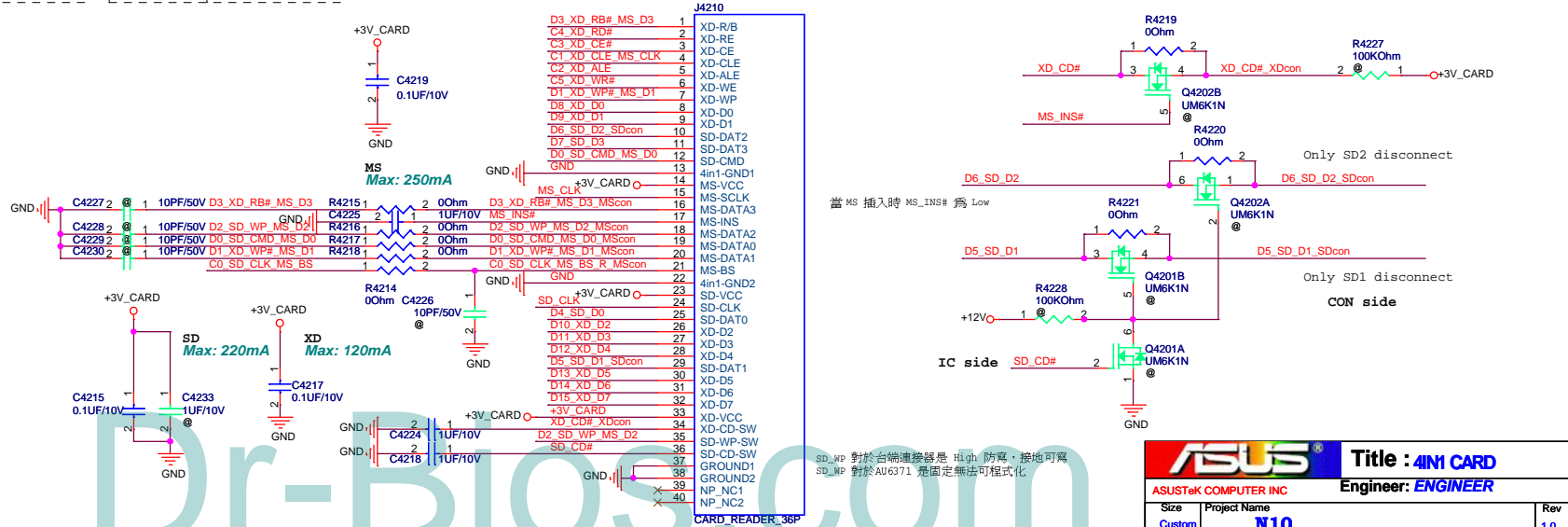
Pin#	PinName
MS No. 1	GND
MS No. 2	BS
MS No. 3	DATA1
MS No. 4	SDIO/DATA0
MS No. 5	DATA2
MS No. 6	INS
MS No. 7	DATA3
MS No. 8	SCLK
MS No. 9	VCC
MS No.10	GND

SD Pin-assignment

Pin#	PinName
SD No. 1	CD/DATA3
SD No. 2	CMD
SD No. 3	GND
SD No. 4	VDD
SD No. 5	CLK
SD No. 6	GND
SD No. 7	DATA0
SD No. 8	DATA1
SD No. 9	DATA2



Avoid floating if XD card is not inserted



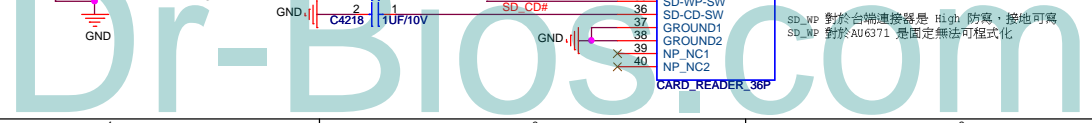
SD_WP 對於台端連接器是 High 防寫，接地可寫
SD_WP 對於AU6371 是固定無法程式化

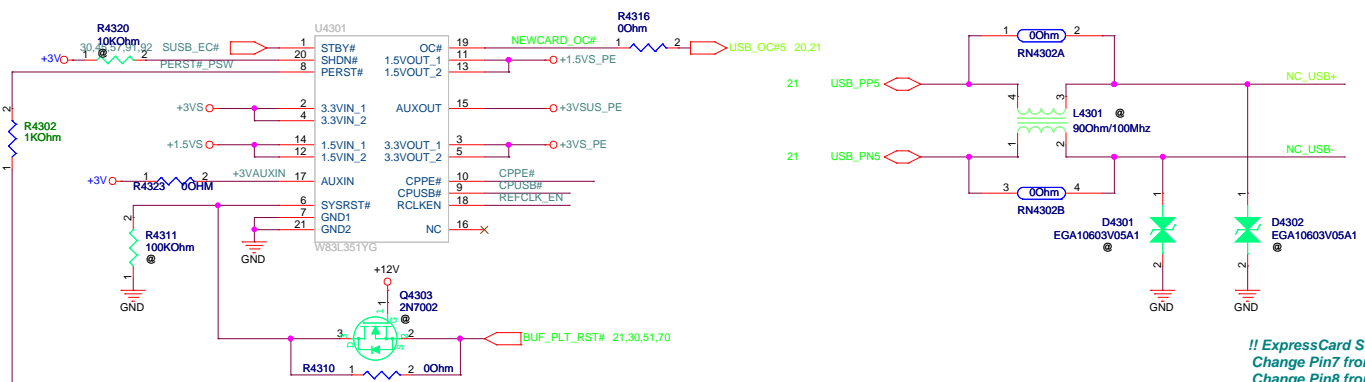
ASUSTeK COMPUTER INC

Engineer: ENGINEER

Title: 4in1 CARD

Size	Project Name	Rev
Custom	N10	1.0
Date: Wednesday, July 02, 2008	Sheet	42 of 97

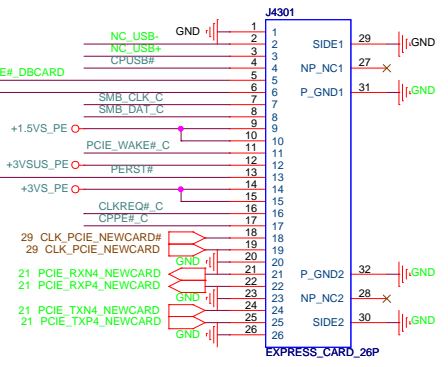
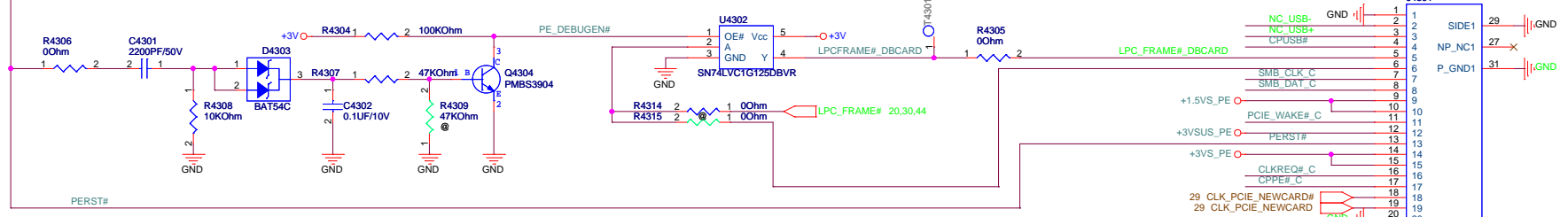




!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

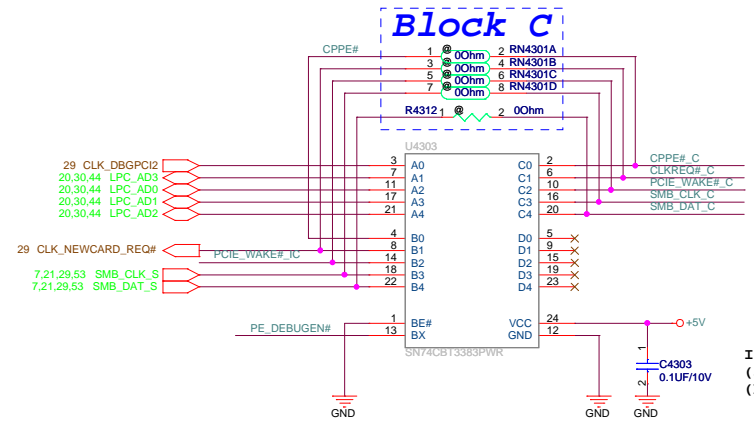
NewCard Header

Block A

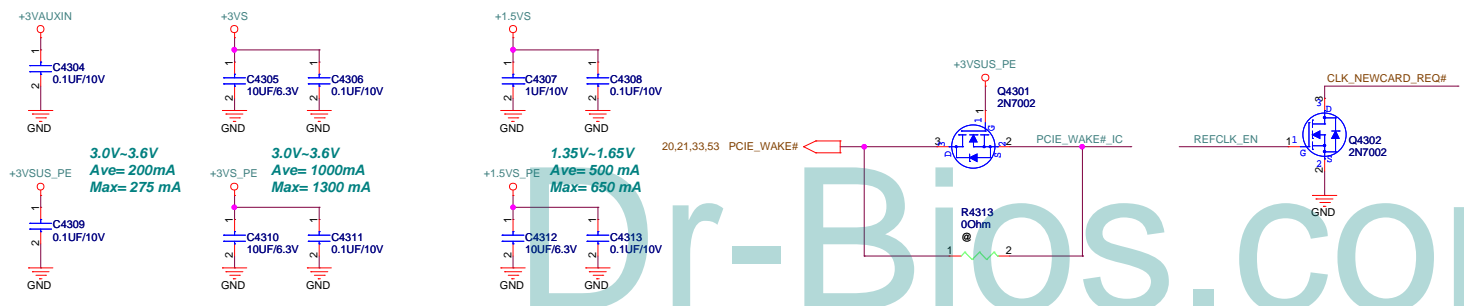


在編 ROM時 請將磁殼 12G21C20001X 加在 60 階

Block C

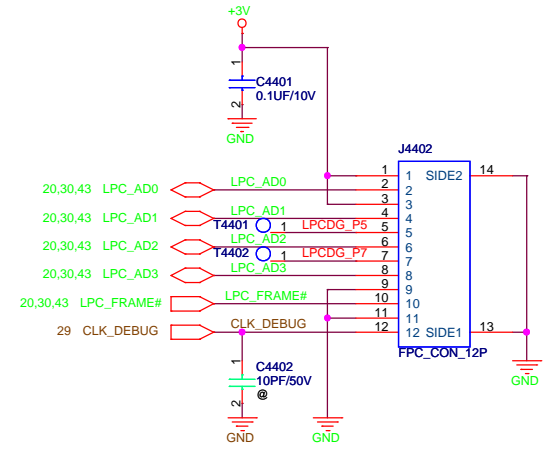



If don't support NewCard Debug Card,Pls do
 (a) DNI all components of block A
 (b) Mount Block C (RN1,R445)



ASUSTeK COMPUTER INC		Title : NEWCARD	
		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
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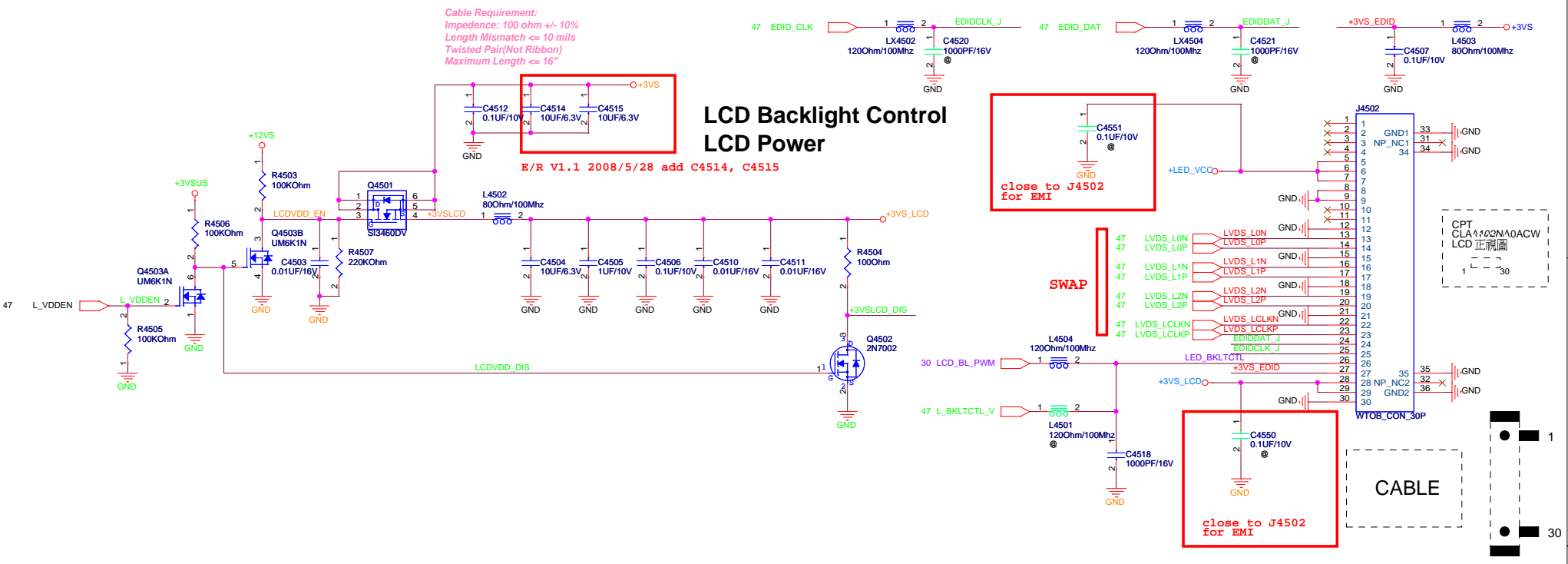
LPC DEBUG PORT



		Title : LPC DEBUG	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
B	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	44 of 97

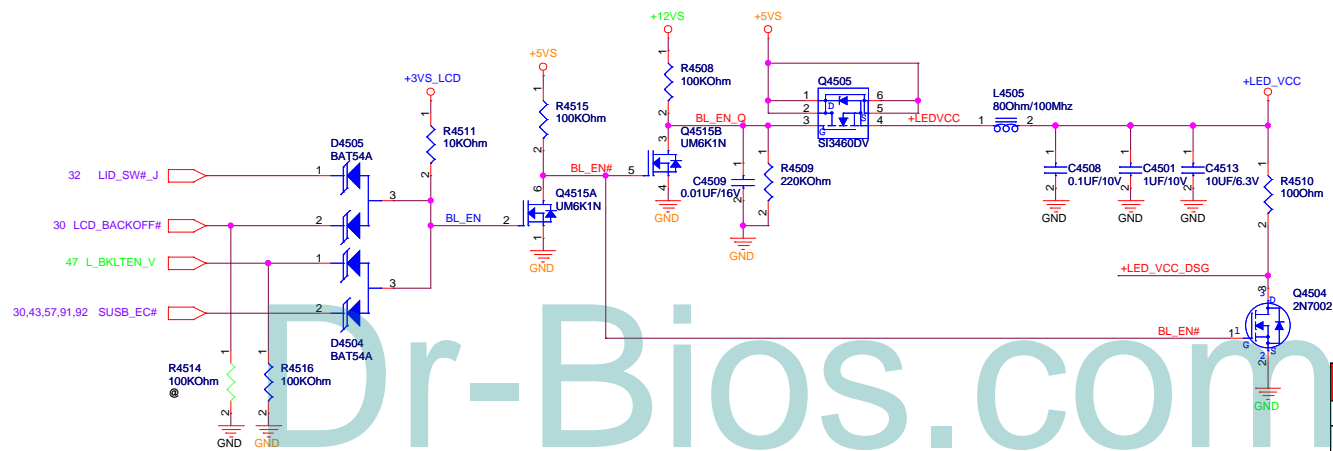
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LCD LVDS Interface



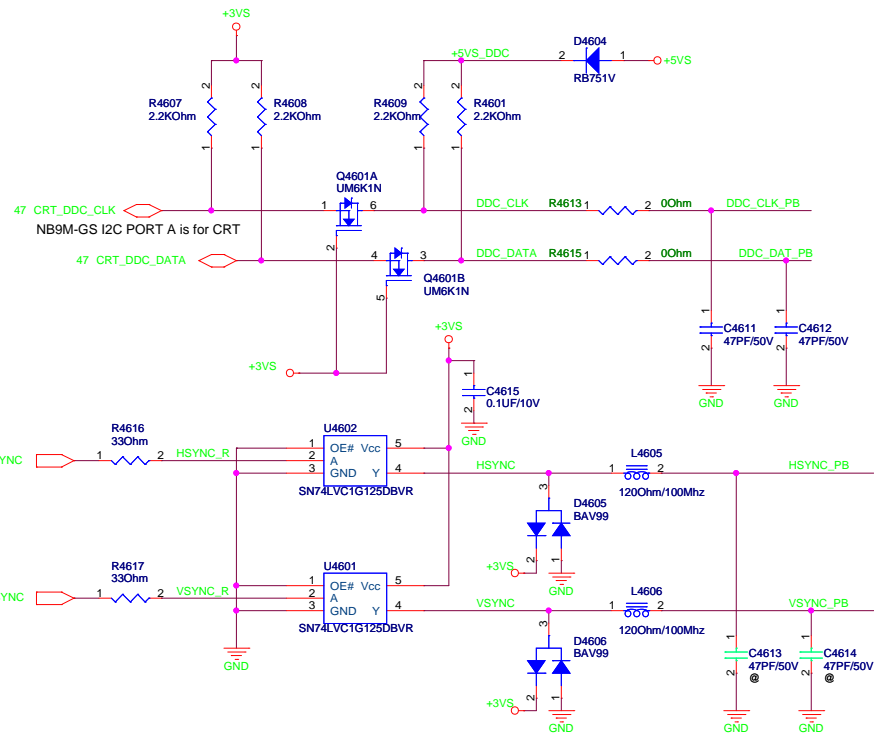
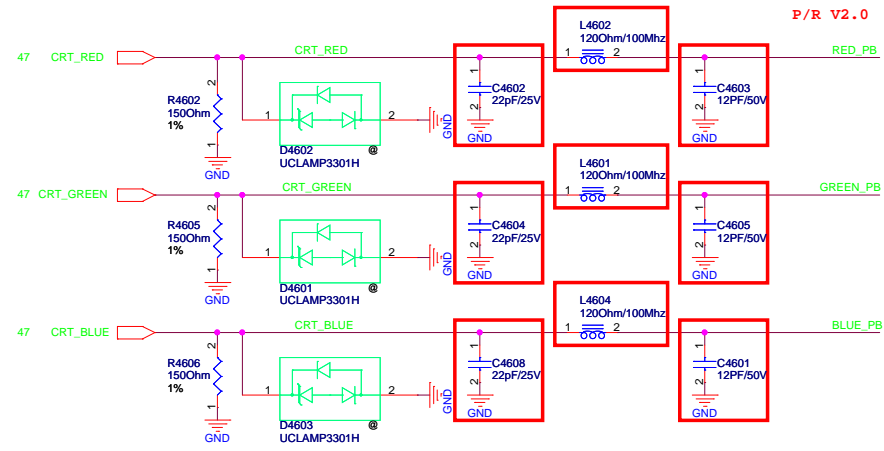
Backlight Interface

BIOS
 BACK_OFF#:When user push
 "Fn+F7" button, BIOS
 active this pin to turn
 off back light.

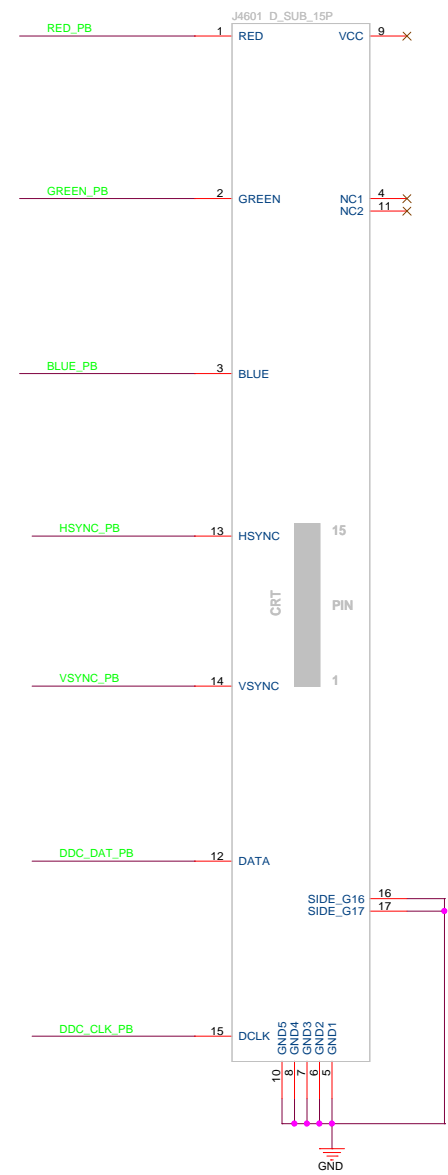


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P/R V2.0 L4601,L4602,L4604 change to P/N:09G023681002 (0.0680UH/300mA 0603 5%)
 P/R V2.0 C4601,C4602,C4603,C4604,C4605,C4608 change to P/N:11G232010004150 (10pF 0402)



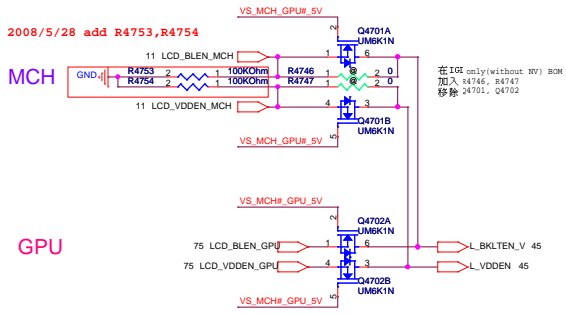
Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.



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LCD/BL Enable Switch

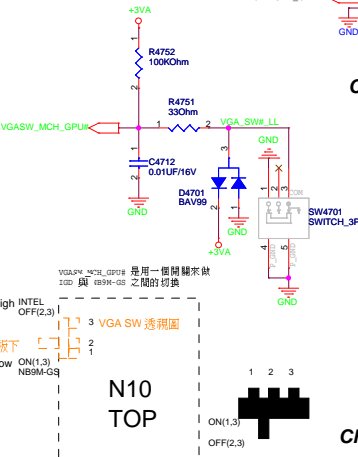
E/R V1.1 2008/5/28 add R4753,R4754



E/R V1.1 2008/5/28 add C4715

CRT RGB Switch

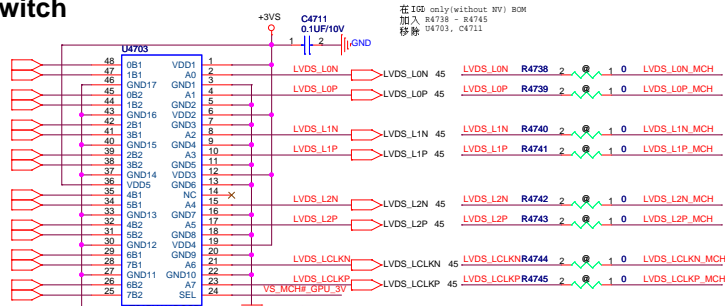
DAC_SEL
L: Dx=S1x (MCH)
H: Dx=S2x (GPU)



N10 TOP

P/R V2.0 2008/7/01 change +3VS to +3VA, amount R4718

LVDS Switch

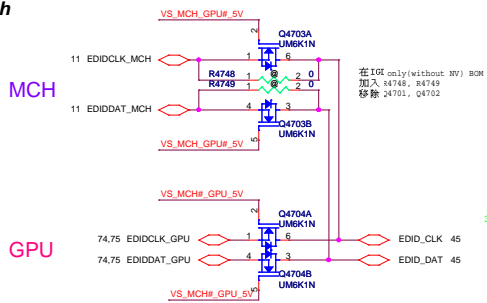


VS_MCH#_GPU#_3V
L: An=nB1 (MCH)
H: An=nB2 (GPU)

E/R V1.1 2008/5/28 add C4713, C4714

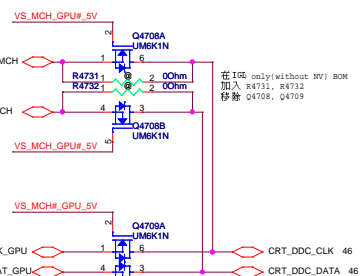
在 IIG only (without NV) BOM
加入 R4735, R4736, R4737
移除 U4702, C4710

EDID Switch



CRT DDC Switch

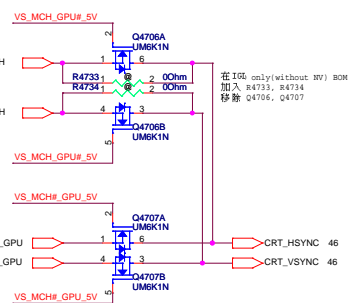
MCH



GPU

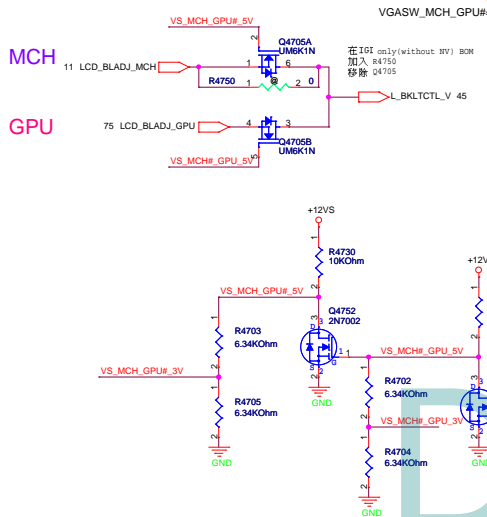
CRT SYNC Switch

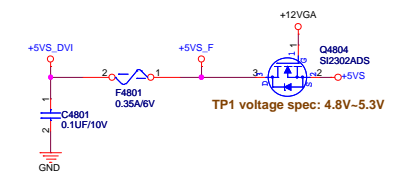
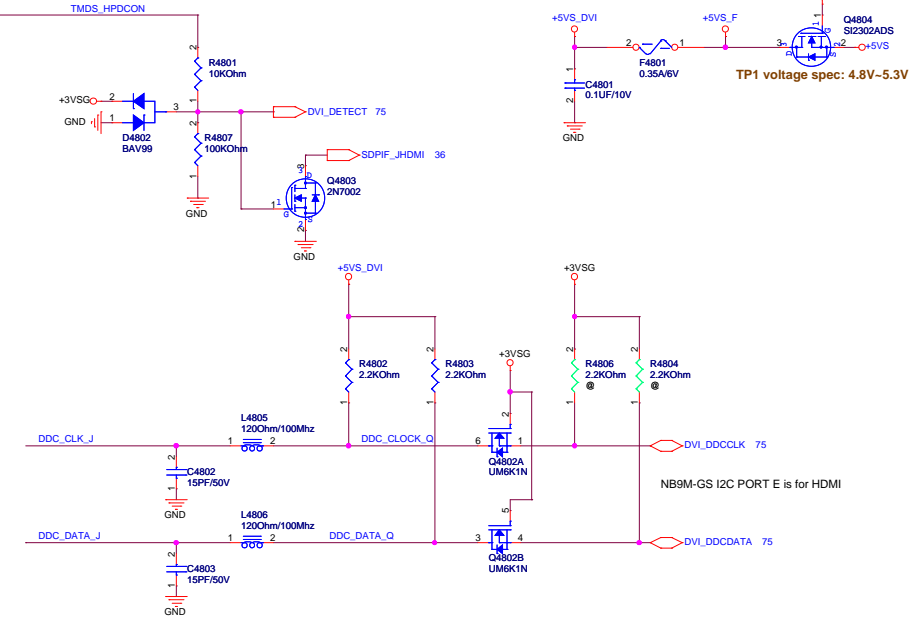
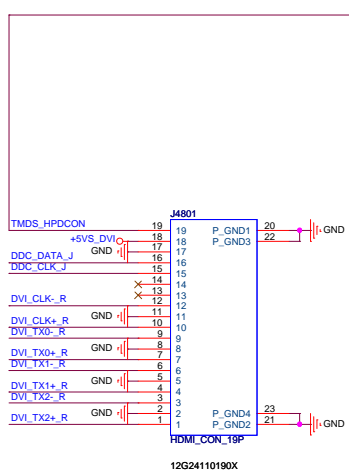
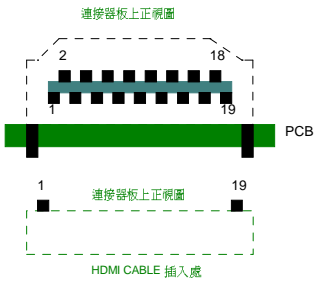
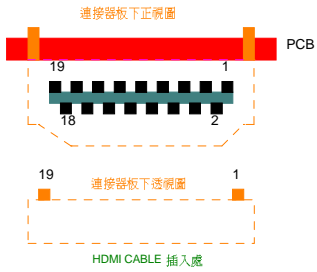
MCH



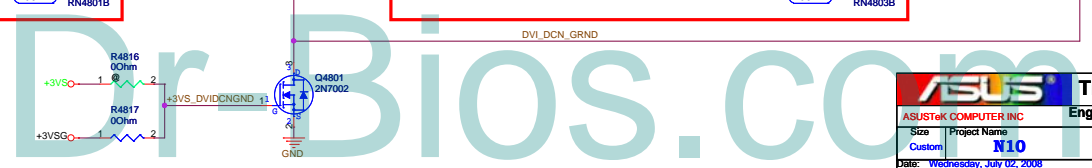
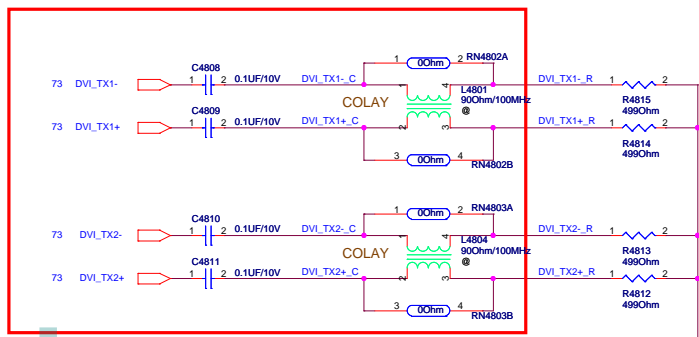
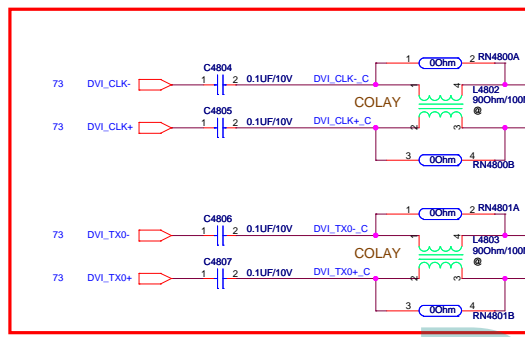
GPU

BL PWM Switch






E/R V1.1 20080526 for EMI



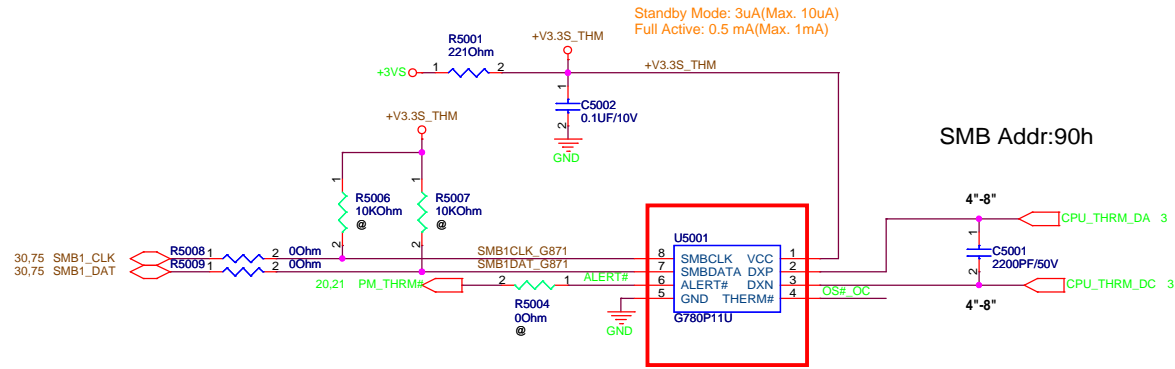
ASUS		Title : HDMI	
ASUSTek COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
Date: Wednesday, July 02, 2008	Sheet	48	of 97



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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
A	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	49 of 97
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Thermal Sensor



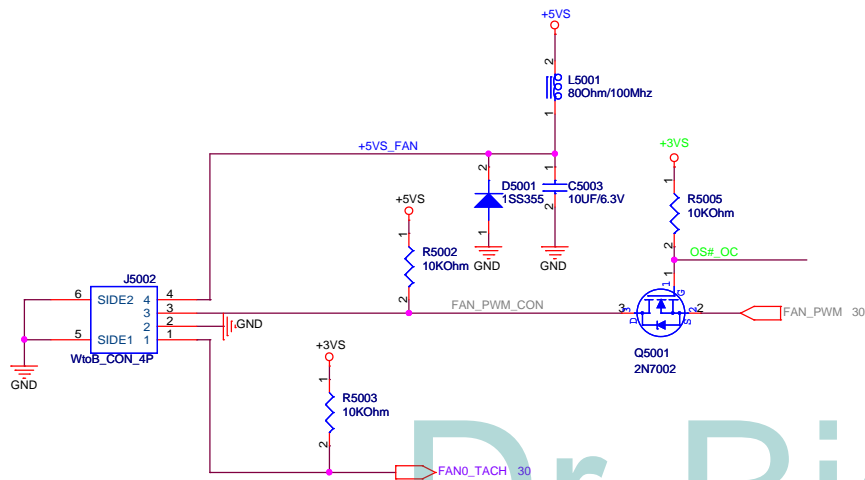
U5001 於30M變更>/N:06G023064020 E/R 2008/05/19

Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
12 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
12 mils
-----OTHER SIGNALS

Avoid BPSB,Power

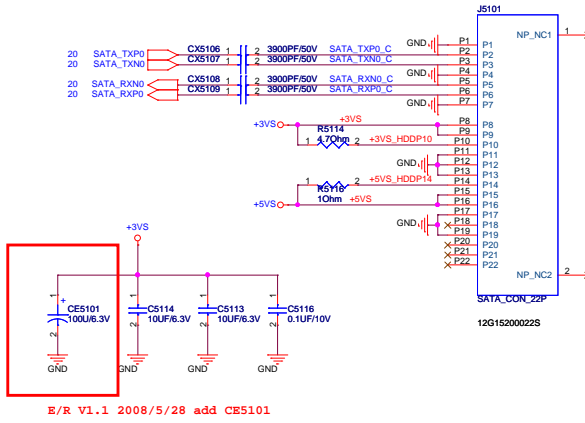
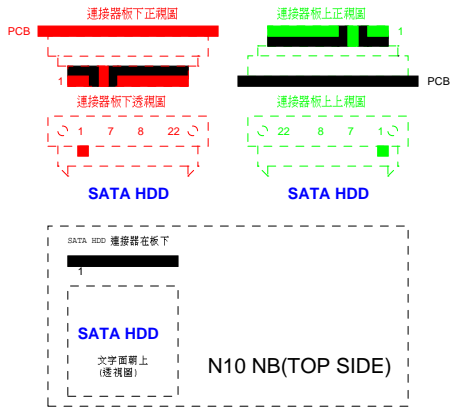
FAN connector



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SATA HDD

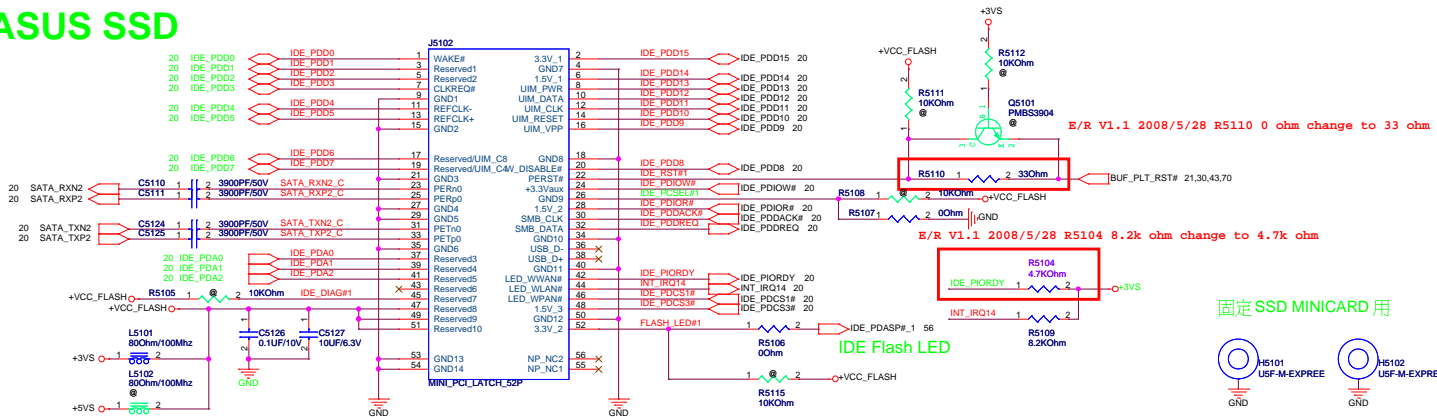
J5101 變更 P/N: 12G15200022S (DIP)



E/R H5103, H5104 Delete

E/R V1.1 2008/5/28 add C5101

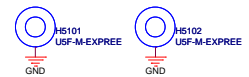
ASUS SSD



E/R V1.1 2008/5/28 R5110 0 ohm change to 33 ohm

E/R V1.1 2008/5/28 R5104 8.2k ohm change to 4.7k ohm

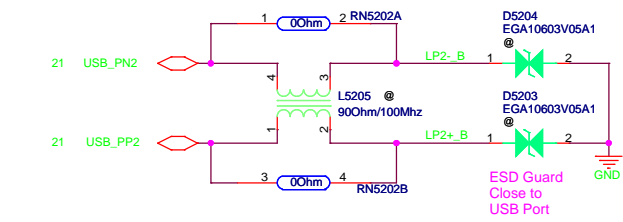
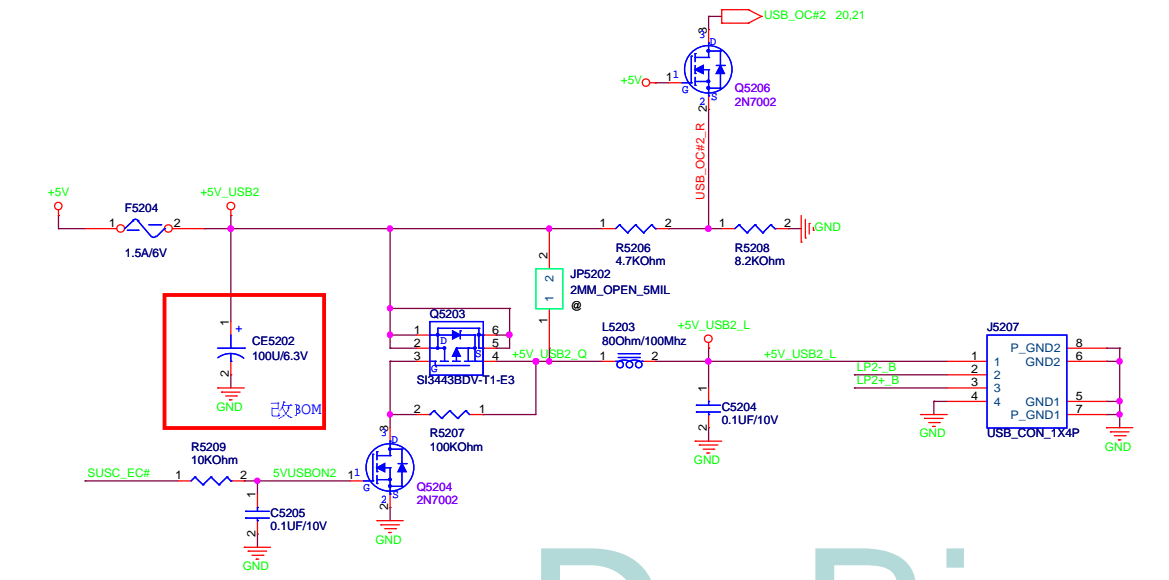
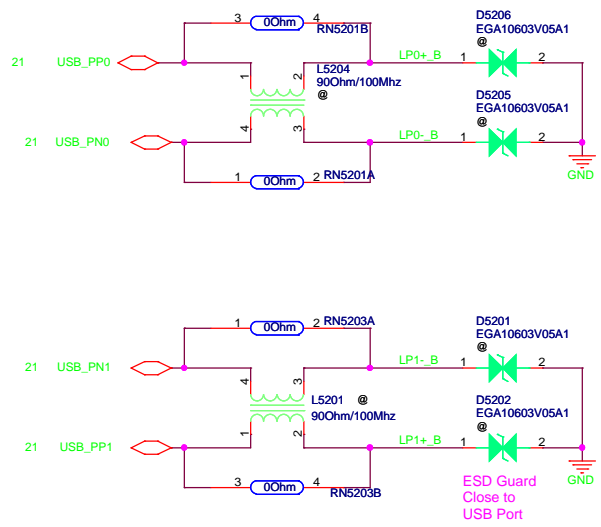
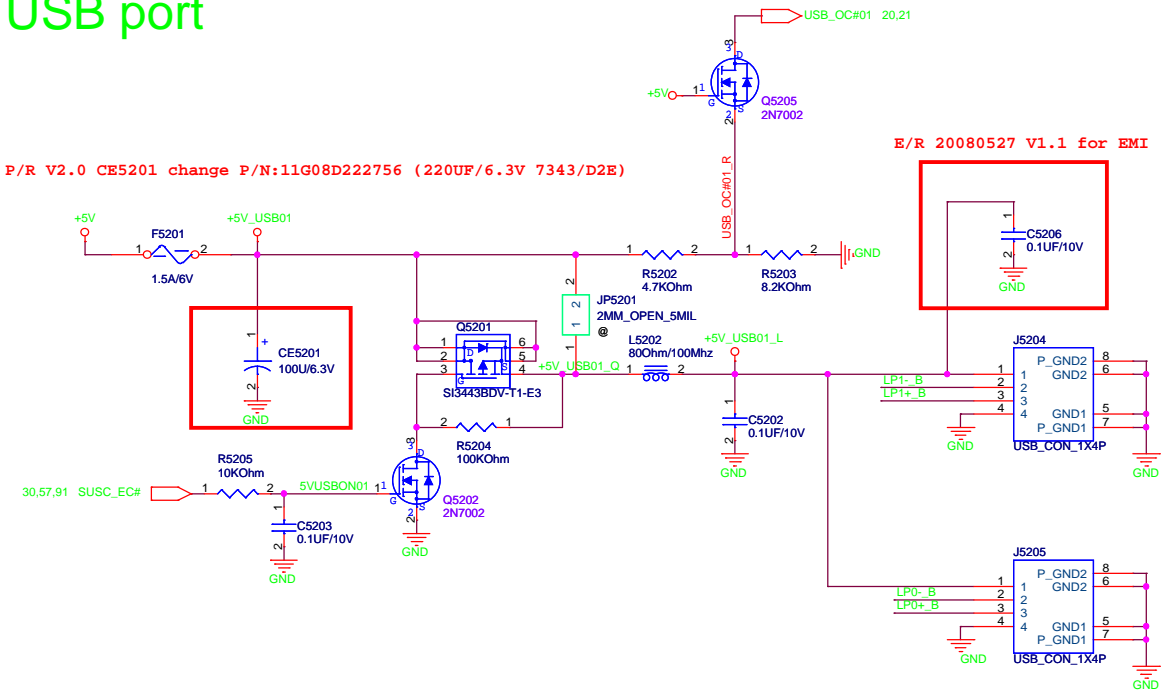
固定 SSD MINICARD 用



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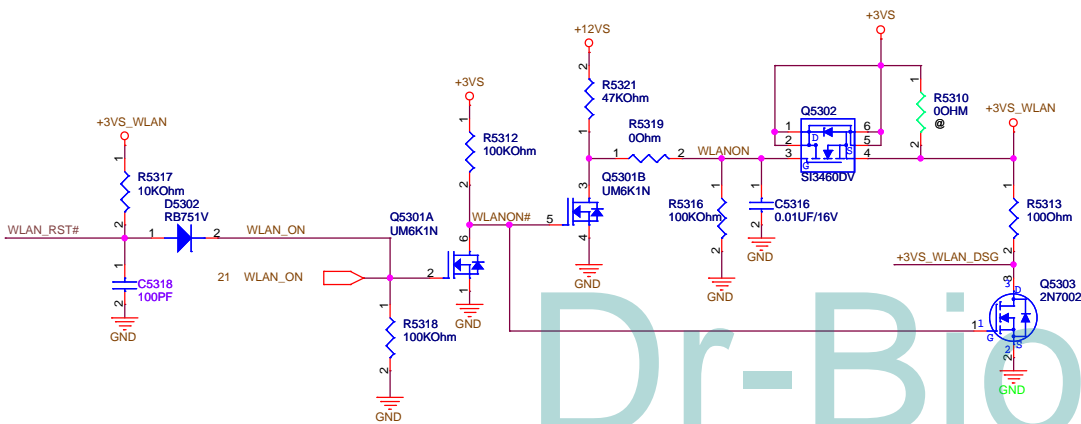
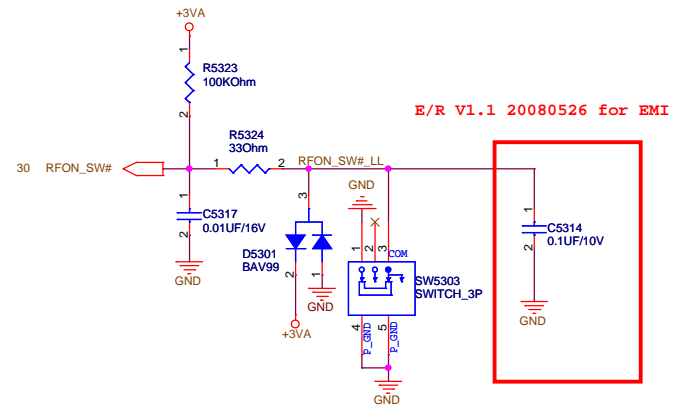
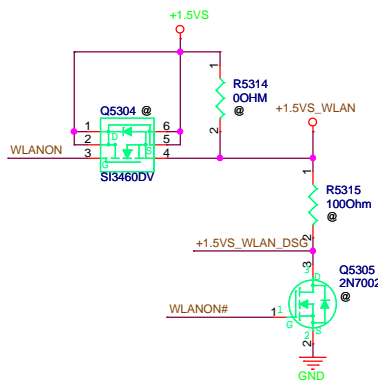
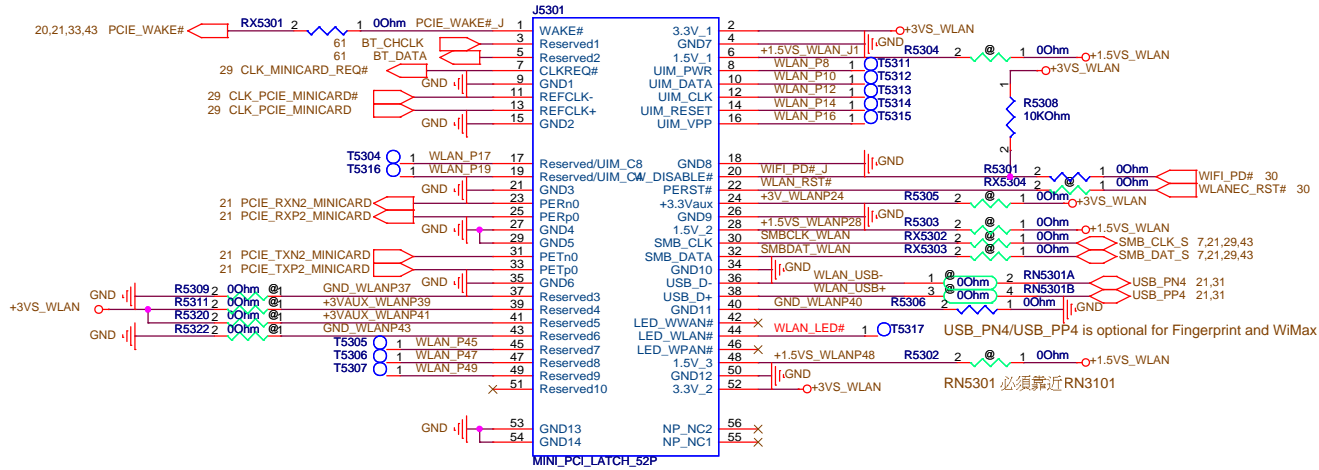
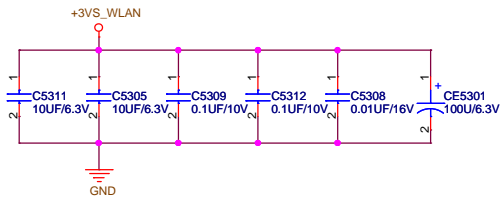
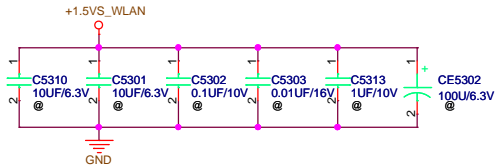
USB port

P/R V2.0 CE5201 change P/N:11G08D222756 (220UF/6.3V 7343/D2E)



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ASUS		Title : USB CONN	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
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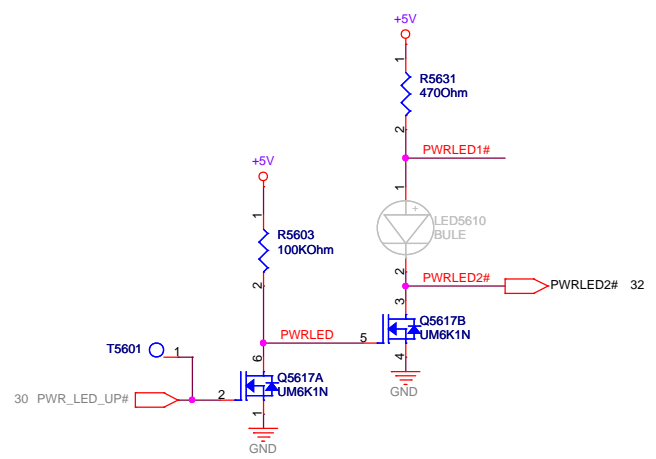


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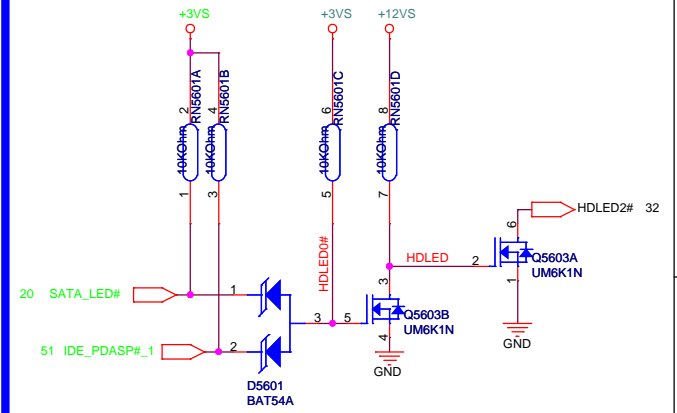
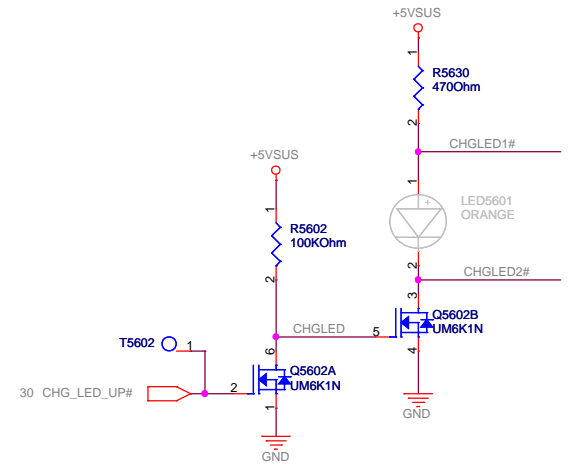
Dr-Bios.com

		Title : EMPTY
ASUSTek COMPUTER INC		Engineer: ENGINEER
Size Custom	Project Name N10	Rev 1.0
Date: Wednesday, July 02, 2008		Sheet 54 of 87

POWER LED

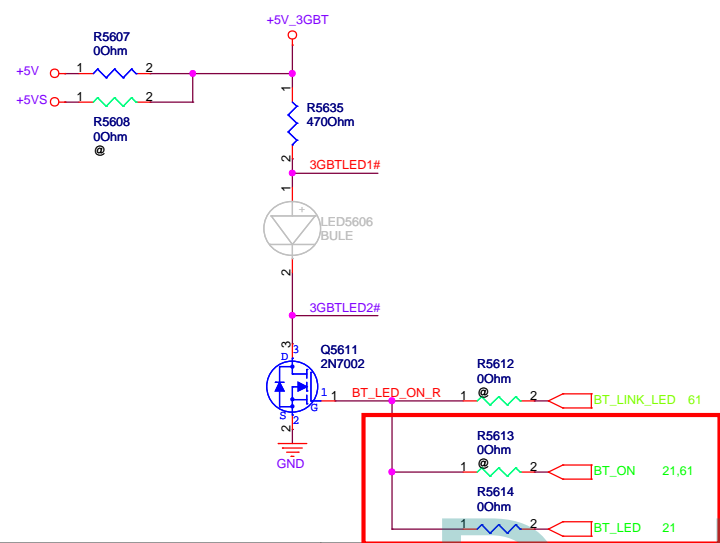


CHARGE LED

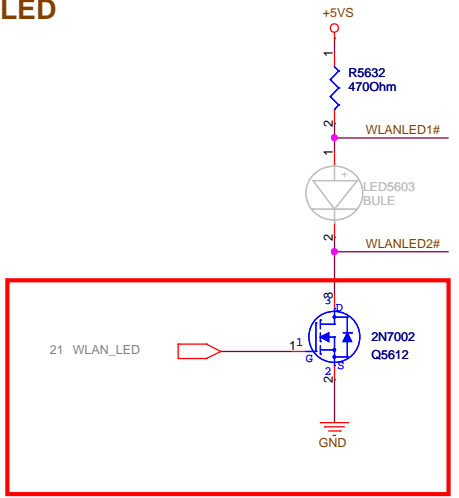


BT LED

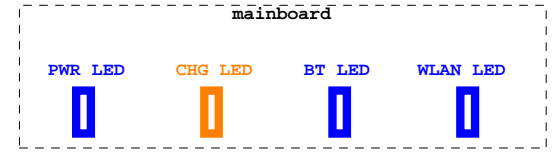
P/R V2.0 2008/6/29 R5613 unmount, R5614 mount



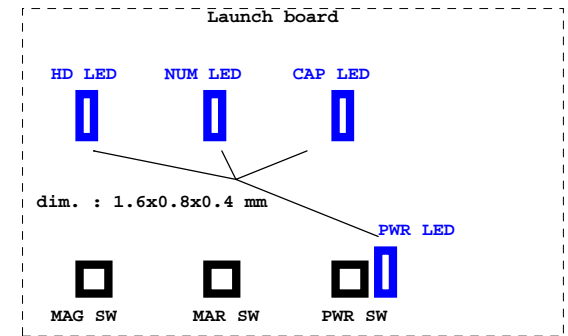
WLAN LED



P/R V2.0 2008/6/29 mount Q5612

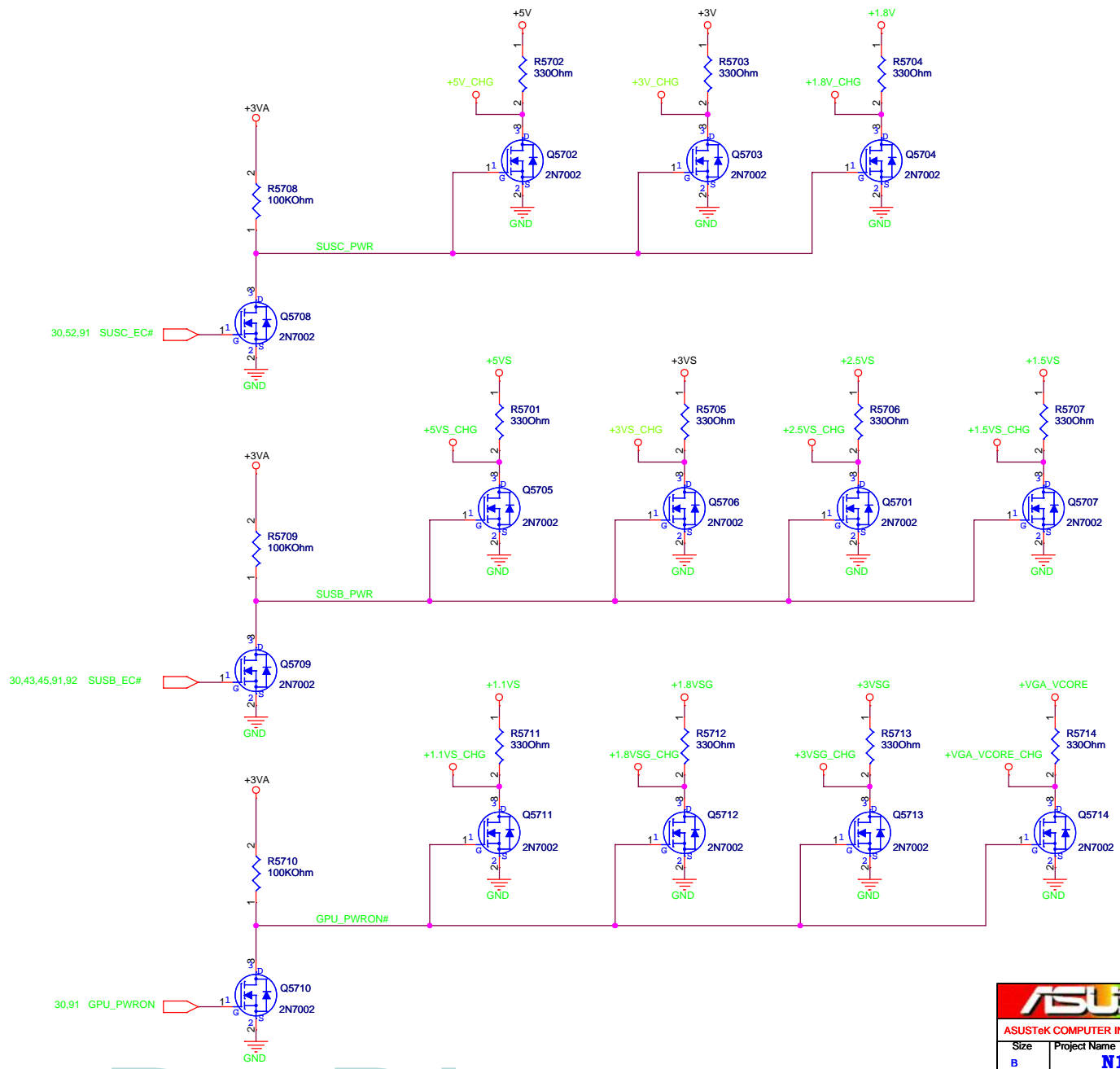


dim. : 3x1.6x1.6 mm



dim. : 1.6x0.8x0.4 mm

ASUS		Title : LED	
ASUSTek COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
B	N10		1.0
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ASUS		Title : Discharge Circuit	
ASUSTek COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
B	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	57 of 97

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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
B	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	58 of 97

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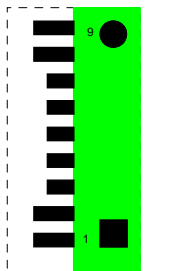
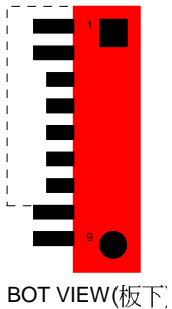


		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
B	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	59 of 97

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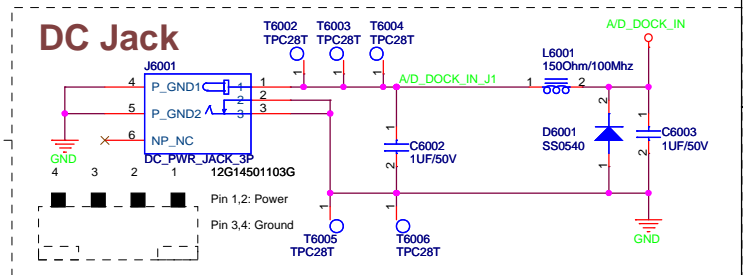
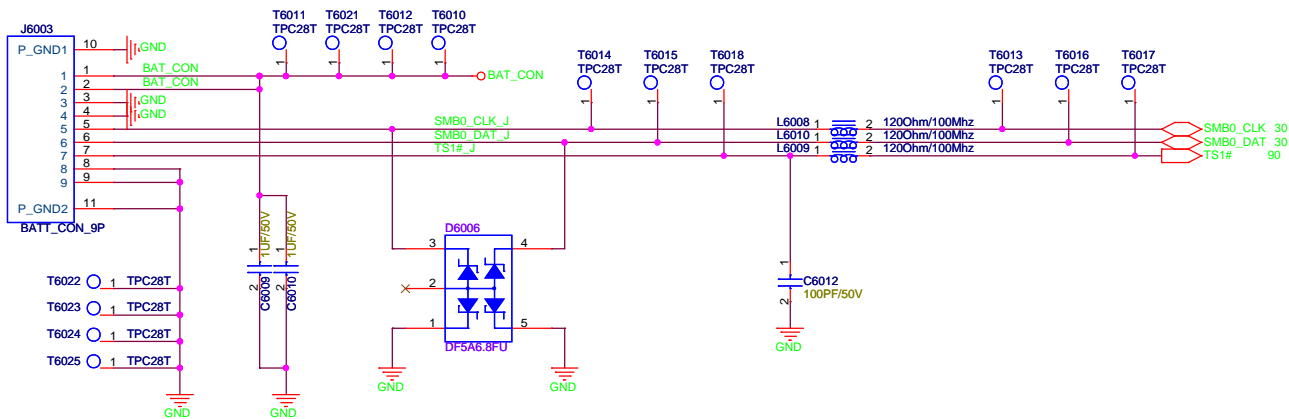
BAT1 JACK

Pin	Signal
1	P+
2	P+
3	CNT1
4	CNT2
5	SMBC
6	SMBD
7	ID
8	GND
9	GND

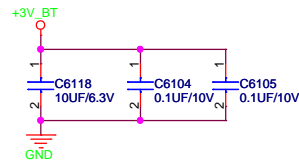
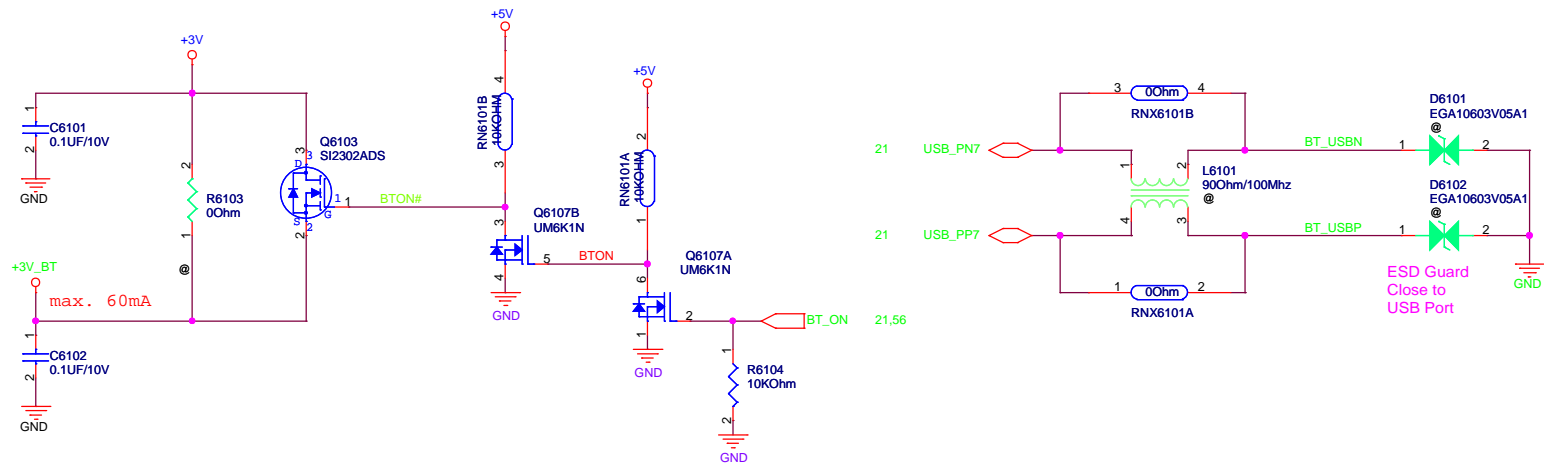


TOP VIEW (板上)

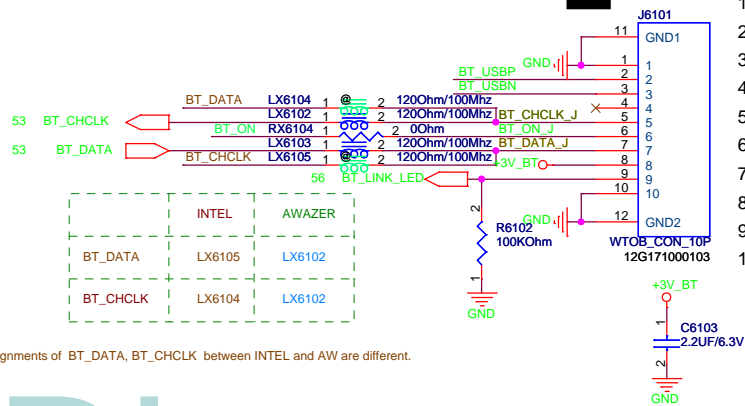
主電池上視圖



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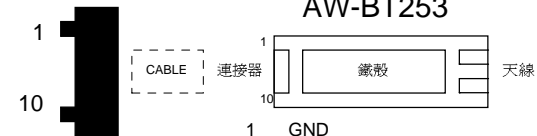


Bluetooth Module



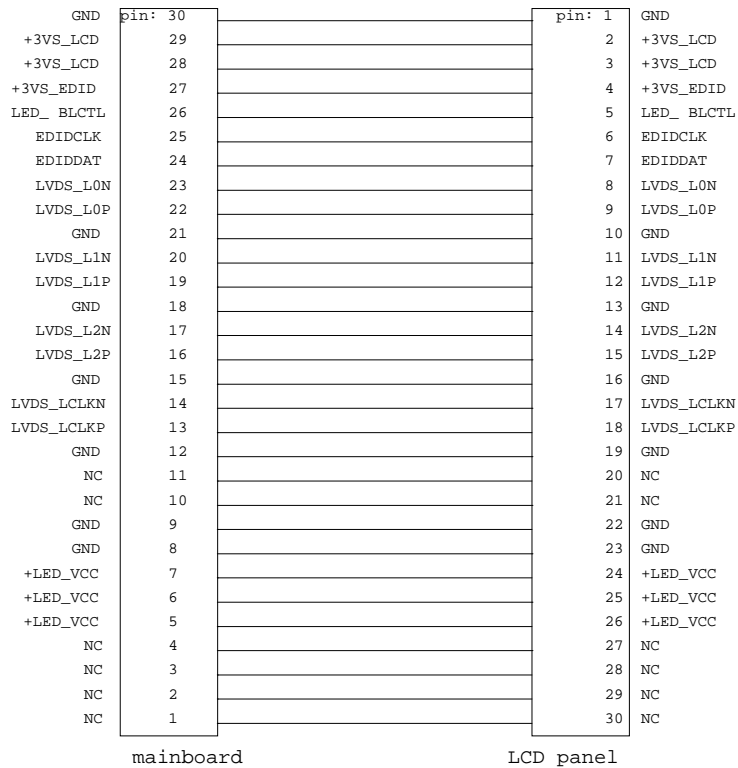
Pin-assignments of BT_DATA, BT_CHCLK between INTEL and AW are different.

AW-BT253



- 1 GND
- 2 USB+
- 3 USB-
- 4 NC
- 5 BT_PRI/CH_CLK
- 6 HW_DIS#
- 7 CH_DAT
- 8 +3.3V
- 9 LED
- 10 GND

ASUS		Title : BLUETOOTH	
ASUSTek COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
B	N10		1.0
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5

4

3

2

1

D

D

C

C


B

B

A

A

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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
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5

4

3

2

1

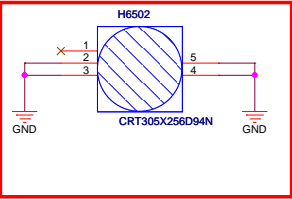
PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

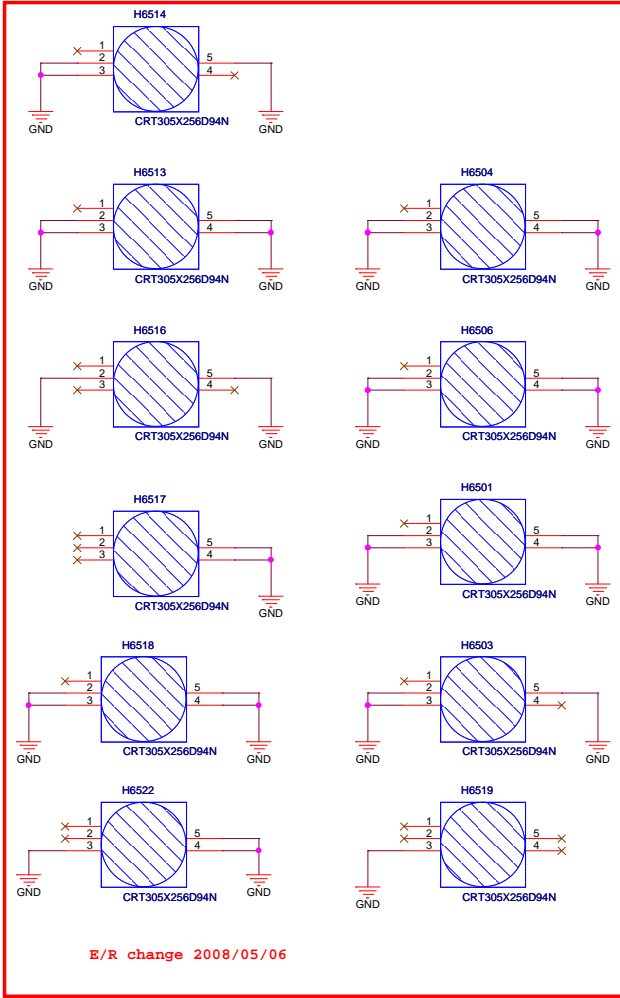
IC	REFERENCE	VENID	DEVID	VERSION	MARK
NB9M-GS			0x06E9		Current Version: A2

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A+E

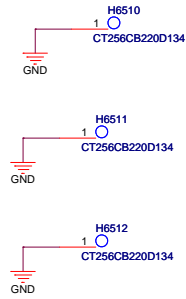


A+B

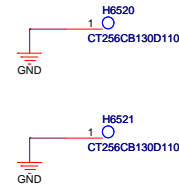


E/R change 2008/05/06

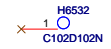
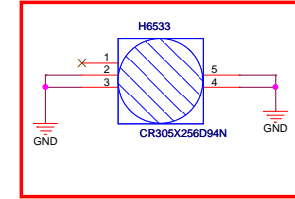
G+H



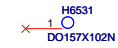
D



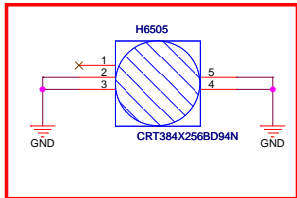
A+A



L



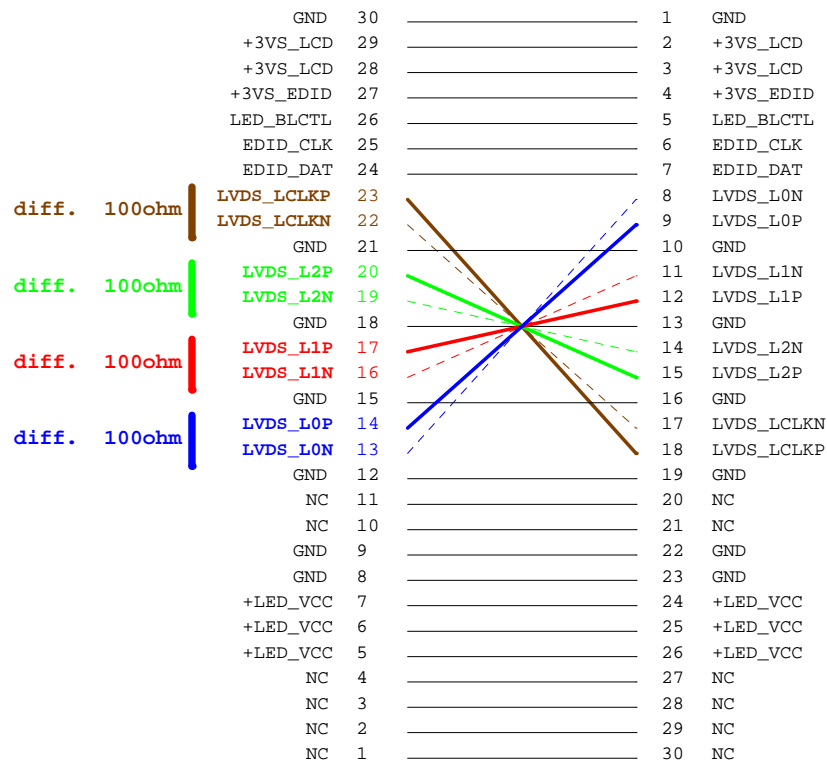
O+B



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ASUS		Title : MESKEWOLE	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
Date: Wednesday, July 02, 2008		Sheet	65 of 97

LVDS CABLE (WTB)

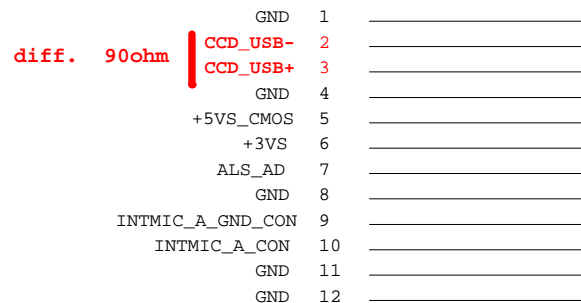


MAINBOARD CONNECT

LCD PANEL CONNECT

P/N: 12G171040305

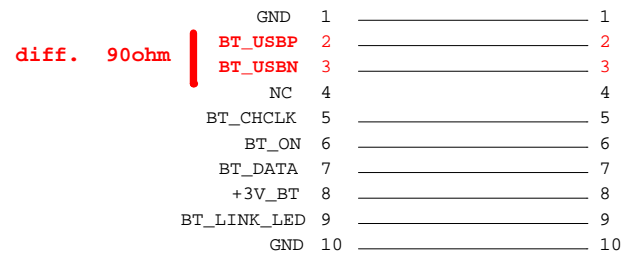
MIC., CCD, ALS CABLE(WTB)



MAINBOARD CONNECT

P/N: 12G171000124

BLUETOOTH CABLE(WTB)



MAINBOARD CONNECT

BlueTooth

P/N: 12G171000103

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LAUNCH CABLE(WTB)

+5V	14	_____	14	+5V
+3VA	13	_____	13	+3VA
GND	12	_____	12	GND
LID_SW#	11	_____	11	LID_SW#
PWRLED#	10	_____	10	PWRLED#
PWR_SW#	9	_____	9	PWR_SW#
GND	8	_____	8	GND
MARATHON_SW#	7	_____	7	MARATHON_SW#
MAGNIFY_SW#	6	_____	6	MAGNIFY_SW#
+3VS	5	_____	5	+3VS
HDLED#	4	_____	4	HDLED#
NUM_LED#	3	_____	3	NUM_LED#
CAP_LED#	2	_____	2	CAP_LED#
+5VS	1	_____	1	+5VS

MAINBOARD CONNECT

P/N: 12G171000145

LAUNCH BOARD CONNECT

P/N: 12G171030140

MODEM CABLE(WTB)

RING 1	_____	RING
TIP 2	_____	TIP

MAINBOARD CONNECT

MODEM CONNECT

FINGER-PRINTER CABLE(FFC)

GND	12	_____	12	GND
FP_USB+	11	_____	11	FP_USB+
FP_USB-	10	_____	10	FP_USB-
+3VS	9	_____	9	+3VS
NC	8	_____	8	NC
NC	7	_____	7	NC
GND	6	_____	6	GND
GND	5	_____	5	GND
TP_CLK	4	_____	4	TP_CLK
TP_DAT	3	_____	3	TP_DAT
+5VS_TP	2	_____	2	+5VS_TP
+5VS_TP	1	_____	1	+5VS_TP

MAINBOARD CONNECT

P/N: 12G18340120C

下接觸

FINGER-PRINTER BOARD CONNECT

P/N: 12G18340120C

下接觸

Touch-Pad CABLE(FFC)

+5VS	12	_____	12	+5VS
+5VS	11	_____	11	+5VS
TP_DAT	10	_____	10	TP_DAT
TP_CLK	9	_____	9	TP_CLK
GND	8	_____	8	GND
GND	7	_____	7	GND
NC	6	_____	6	NC
NC	5	_____	5	NC
NC	4	_____	4	NC
SWL	3	_____	3	SWL
SWR	2	_____	2	SWR
NC	1	_____	1	NC

FINGER-PRINTER BOARD CONNECT

P/N: 12G183301208


上接觸

Touch-Pad BOARD CONNECT

上接觸

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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
Date: Wednesday, July 02, 2008		Sheet	68 of 97

D

D

C

C


B

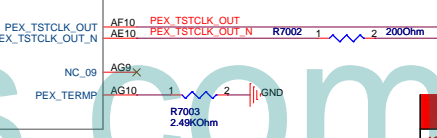
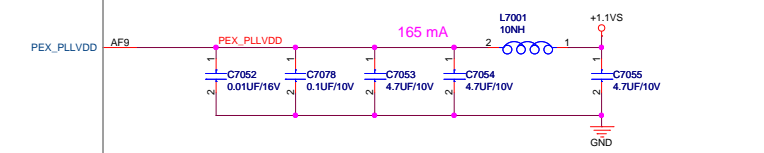
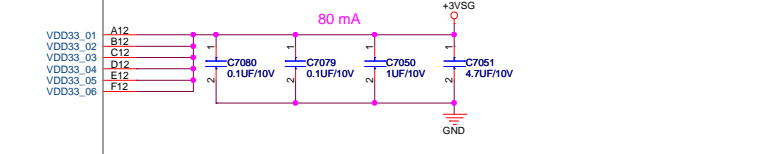
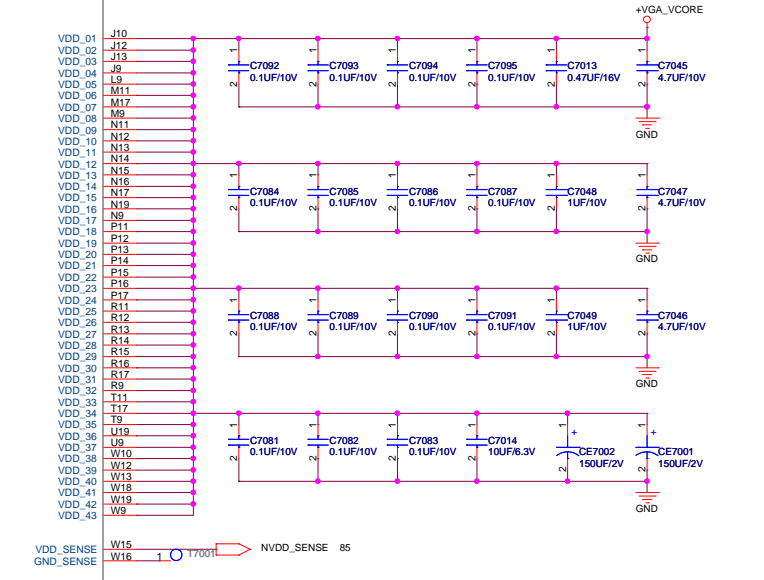
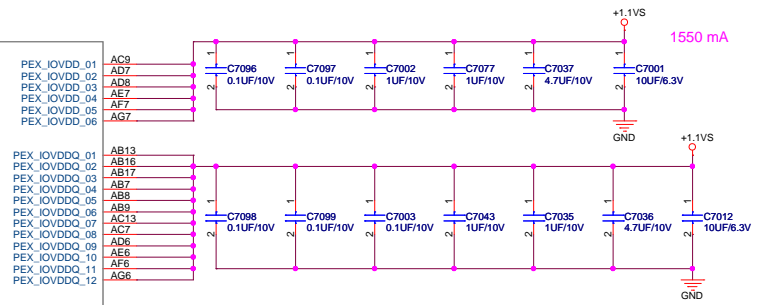
B

A

A

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		Title : HISTORY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
A	N10		1.0
Date: Wednesday, July 02, 2008		Sheet	69 of 97
		2	1



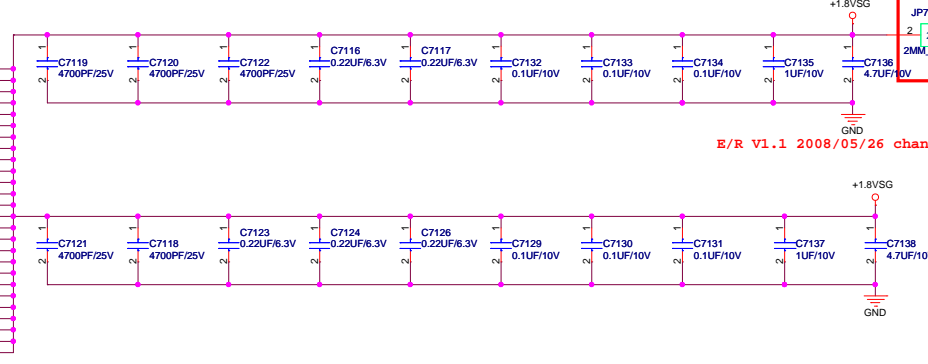
ASUS		Title : NB9MGS_PCIE	
ASUSTek COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10	1.0	
Date: Wednesday, July 02, 2008		Sheet	70 of 97

72 FBAD0[0..63]
 72 FBAD0M[0..7]
 72 FBADQ5[0..7]
 72 FBARDQ5[0..7]

BYTE 0
 BYTE 1
 BYTE 2
 BYTE 3
 BYTE 4
 BYTE 5
 BYTE 6
 BYTE 7

2/13 FRAME_BUFFER
 U7001B
 FBA_D0 D21 FBA_D0
 FBA_D1 D22 FBA_D1
 FBA_D2 D23 FBA_D2
 FBA_D3 D24 FBA_D3
 FBA_D4 D25 FBA_D4
 FBA_D5 D26 FBA_D5
 FBA_D6 D27 FBA_D6
 FBA_D7 D28 FBA_D7
 FBA_D8 D29 FBA_D8
 FBA_D9 D30 FBA_D9
 FBA_D10 D31 FBA_D10
 FBA_D11 D32 FBA_D11
 FBA_D12 D33 FBA_D12
 FBA_D13 D34 FBA_D13
 FBA_D14 D35 FBA_D14
 FBA_D15 D36 FBA_D15
 FBA_D16 D37 FBA_D16
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 FBA_D63 D84 FBA_D63
 FBA_DQM0 D23 FBA_DQM0
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 FBA_DQM6 D41 FBA_DQM6
 FBA_DQM7 D44 FBA_DQM7
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 FBA_DQS_WP2 A19 FBA_DQS_WP2
 FBA_DQS_WP3 I22 FBA_DQS_WP3
 FBA_DQS_WP4 I22 FBA_DQS_WP4
 FBA_DQS_WP5 AA24 FBA_DQS_WP5
 FBA_DQS_WP6 AA26 FBA_DQS_WP6
 FBA_DQS_WP7
 FBA_DQS_RN0 B24 FBA_DQS_RN0
 FBA_DQS_RN1 D25 FBA_DQS_RN1
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 FBA_DQS_RN3 A18 FBA_DQS_RN3
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 FBVDDQ_02 B13 FBVDDQ_02
 FBVDDQ_03 C13 FBVDDQ_03
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 FBVDDQ_06 F13 FBVDDQ_06
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 FBVDDQ_10 F16 FBVDDQ_10
 FBVDDQ_11 F17 FBVDDQ_11
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 FBVDDQ_20 L19 FBVDDQ_20
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 FBVDDQ_23 M19 FBVDDQ_23
 FBVDDQ_24 N22 FBVDDQ_24
 FBVDDQ_25 U22 FBVDDQ_25
 FBVDDQ_26 Y22 FBVDDQ_26
 FBA_CMD0 F26 FBA_CMD0
 FBA_CMD1 J24 FBA_CMD1
 FBA_CMD2 F26 FBA_CMD2
 FBA_CMD3 M23 FBA_CMD3
 FBA_CMD4 N27 FBA_CMD4
 FBA_CMD5 M27 FBA_CMD5
 FBA_CMD6 K26 FBA_CMD6
 FBA_CMD7 J25 FBA_CMD7
 FBA_CMD8 J27 FBA_CMD8
 FBA_CMD9 G23 FBA_CMD9
 FBA_CMD10 G26 FBA_CMD10
 FBA_CMD11 J23 FBA_CMD11
 FBA_CMD12 M25 FBA_CMD12
 FBA_CMD13 K27 FBA_CMD13
 FBA_CMD14 G26 FBA_CMD14
 FBA_CMD15 L24 FBA_CMD15
 FBA_CMD16 K23 FBA_CMD16
 FBA_CMD17 K24 FBA_CMD17
 FBA_CMD18 G22 FBA_CMD18
 FBA_CMD19 H22 FBA_CMD19
 FBA_CMD20 H22 FBA_CMD20
 FBA_CMD21 M26 FBA_CMD21
 FBA_CMD22 J24 FBA_CMD22
 FBA_CMD23 F27 FBA_CMD23
 FBA_CMD24 J26 FBA_CMD24
 FBA_CMD25 G27 FBA_CMD25
 FBA_CMD26 K22 FBA_CMD26
 FBA_CMD27 M24 FBA_CMD27
 FBA_CMD28 J22 FBA_CMD28
 NC_11 X
 NC_12 X
 FBA_CLK0 F24 FBA_CLK0
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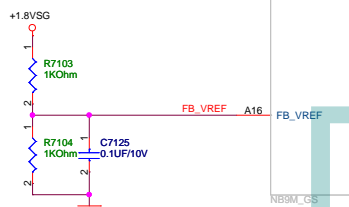
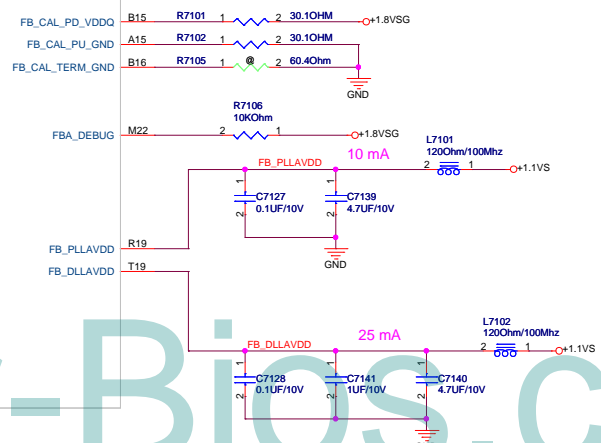
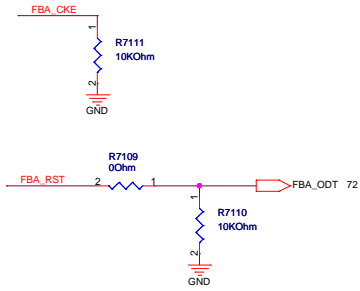


E/R V1.1 2008/05/26 change 3mm to 2mm

COMMAND BUS MAPPING

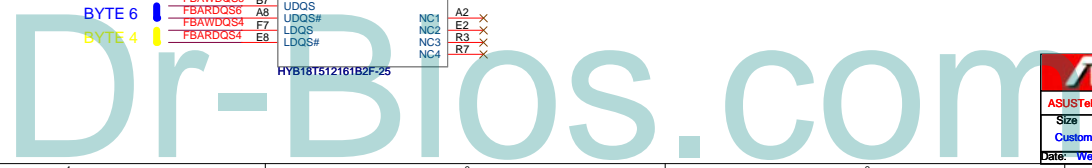
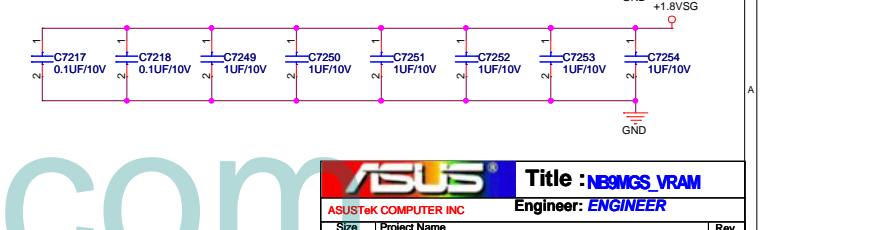
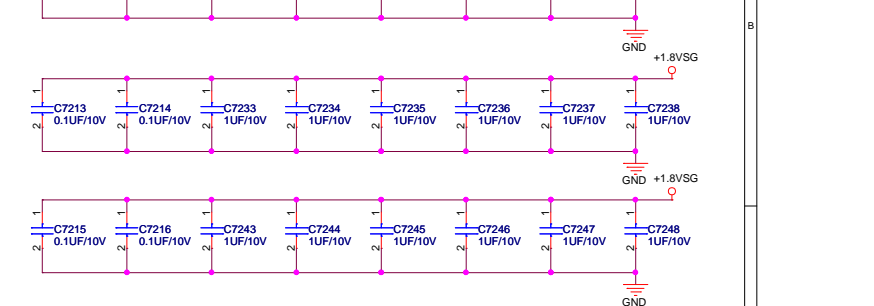
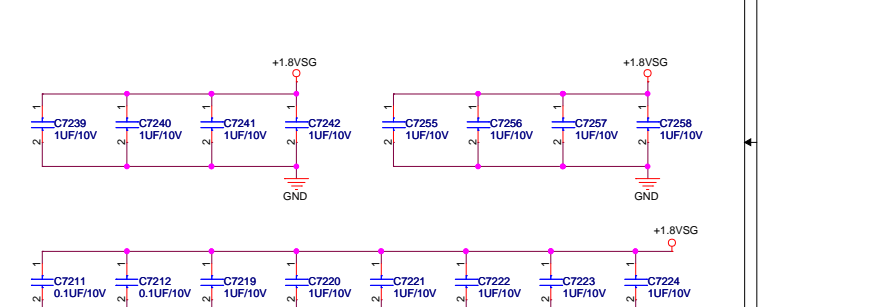
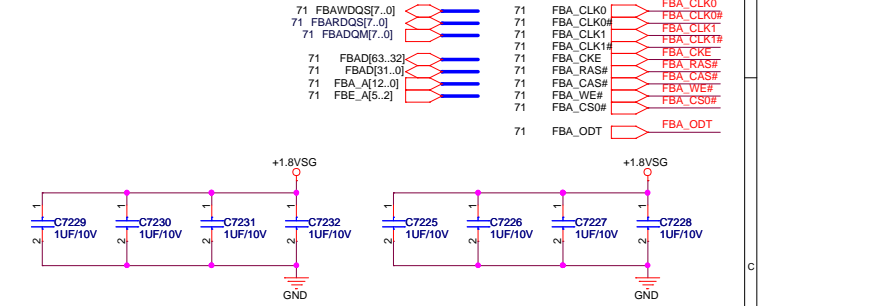
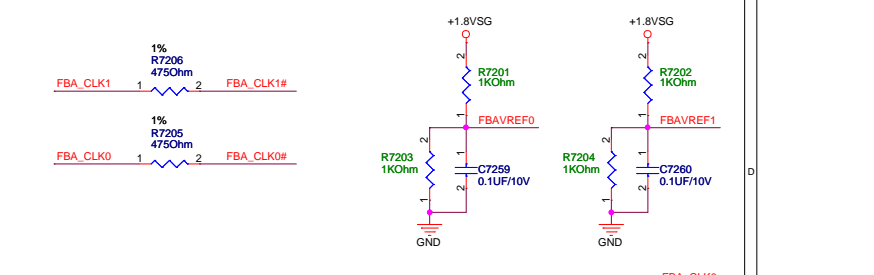
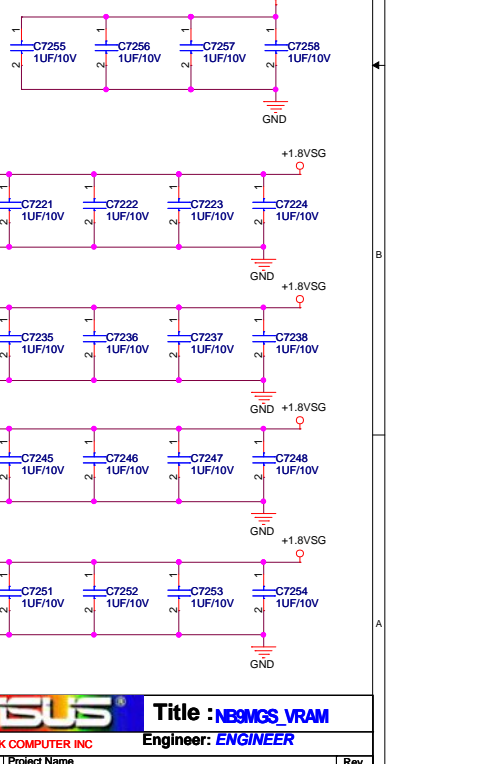
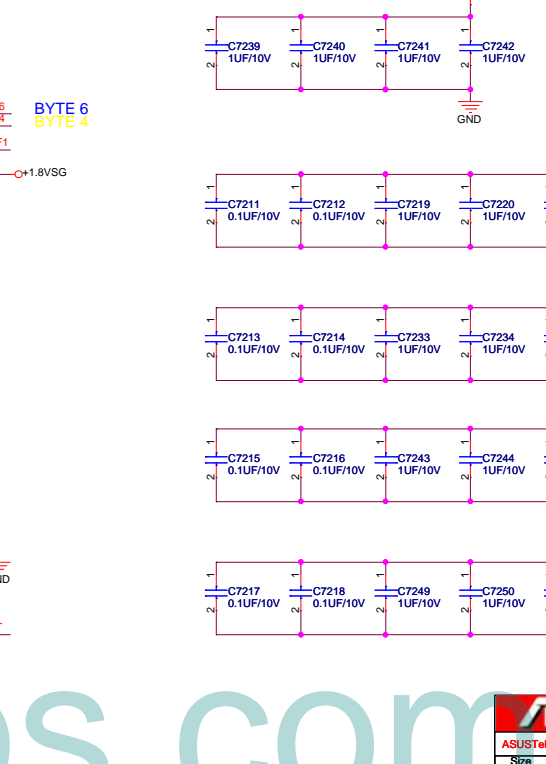
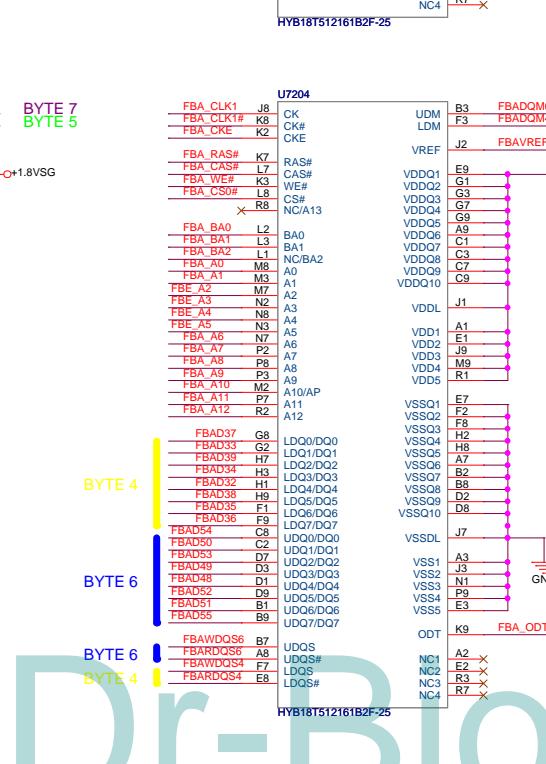
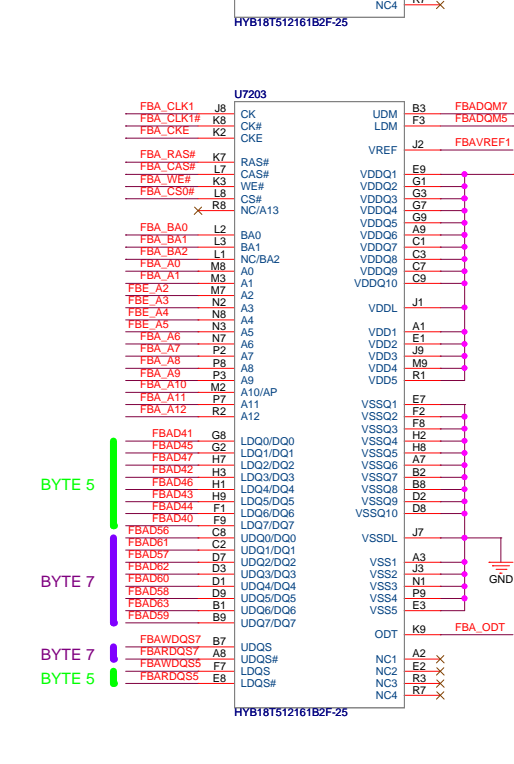
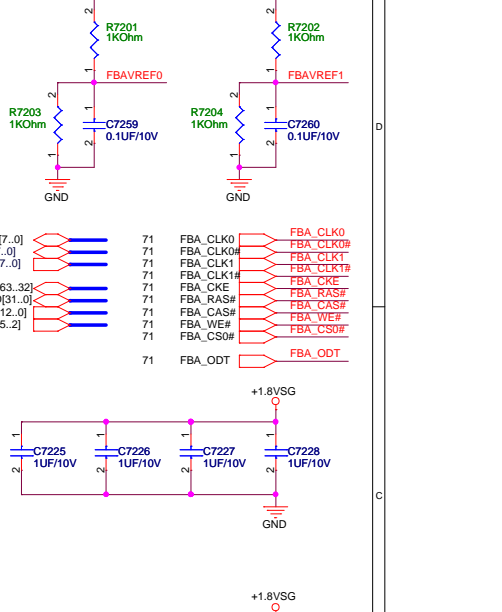
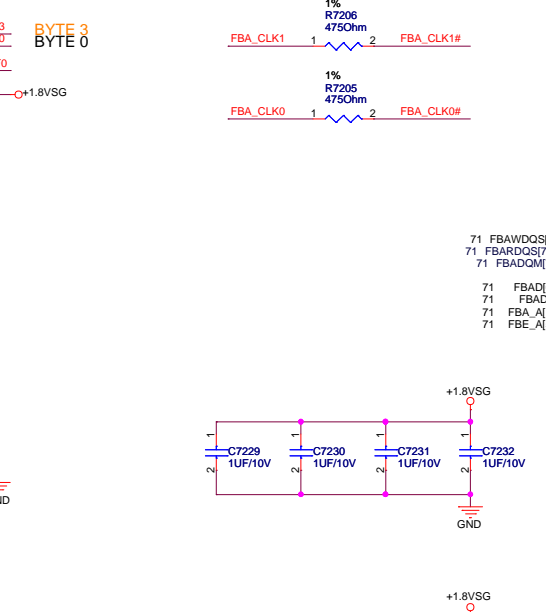
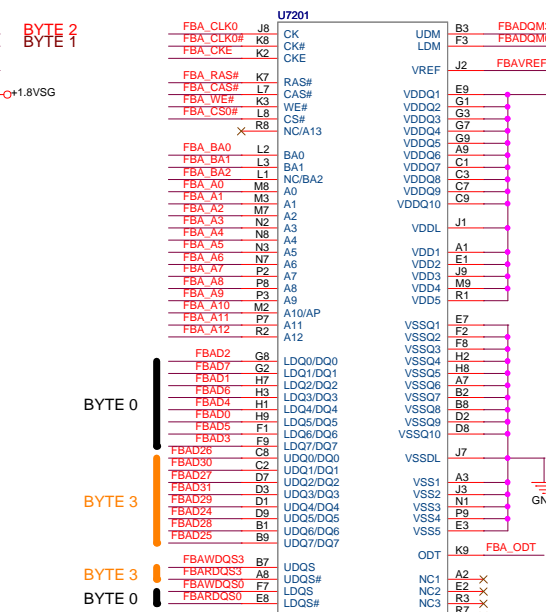
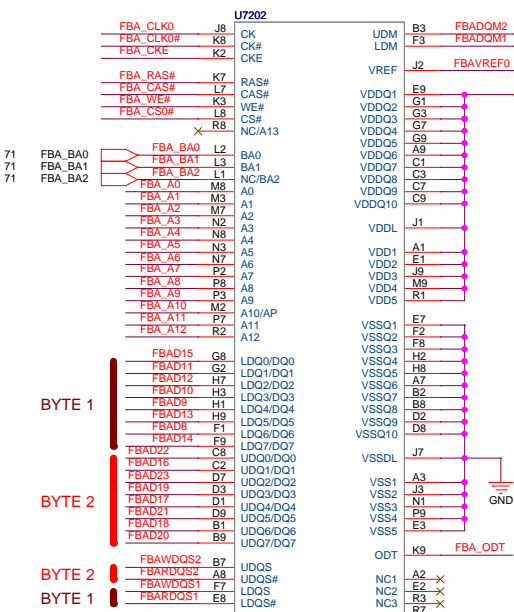
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CM00	A0	NC
CM01	A0	NC
CM02	A2	NC
CM03	A1	A1
CM04	NC	A3
CM05	NC	A4
CM06	NC	A5
CM07	CS1*	CS0*
CM08	CS0*	CS0*
CM09	WE*	WE*
CM10	BA0	BA0
CM11	OE*	OE*
CM12	RSTODT	RSTODT
CM13	NC	A2
CM14	A12	A12
CM15	RA0*	RA0*
CM16	A11	A11
CM17	AA0	AA0
CM18	BA1	BA1
CM19	AB	AB
CM20	AG	AG
CM21	AA	AA
CM22	AA	NC
CM23	A7	A7
CM24	AA	NC
CM25	CAS*	CAS*
CM26	A13	A13
CM27	BA2	BA2
CM28	RFU0	RFU0
CM29	RFU1	RFU1
CM30	RFU2	RFU2

Note: CS1* not used for single rank



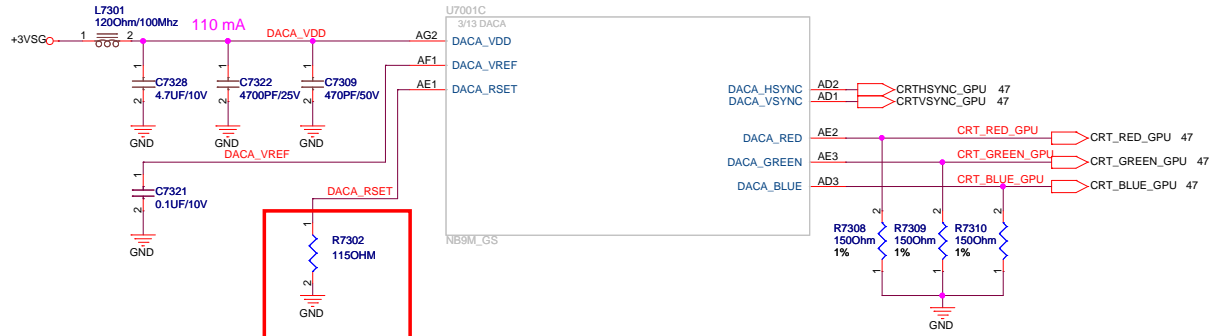
NB9M_CS

ASUS Title : NB9MCS_FB
 ASUSTek COMPUTER INC Engineer: ENGINEER
 Size Project Name
 Custom N10
 Date: Wednesday, July 02, 2008 Sheet 71 of 97
 Rev 1.0



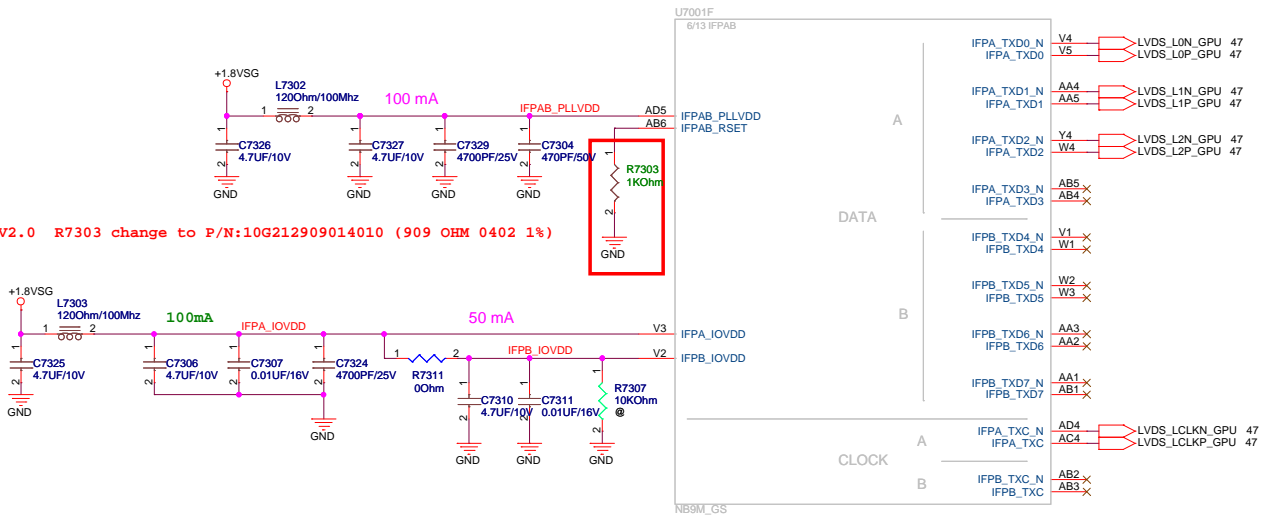
ASUS Title: **NBSMGS VRAM**
 ASUSTeK COMPUTER INC Engineer: **ENGINEER**
 Size: Custom Project Name: **N10** Rev: 1.0
 Date: Wednesday, July 02, 2008 Sheet: 72 of 97

VGA

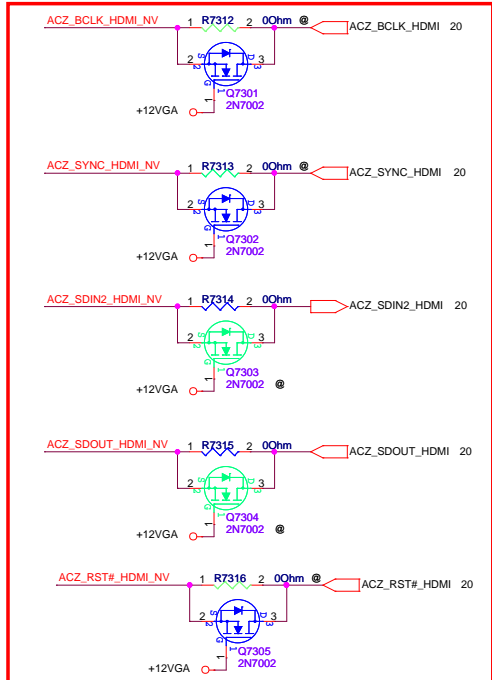


P/R V2.0 2008/6/30 R7302 change P/N

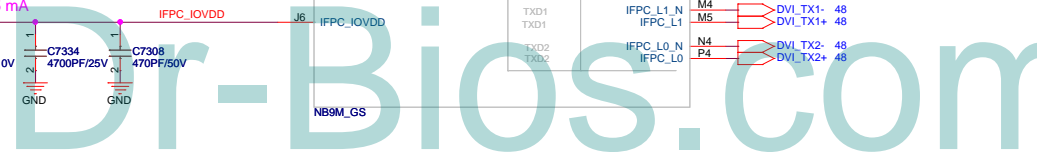
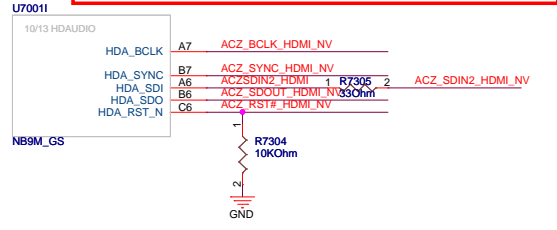
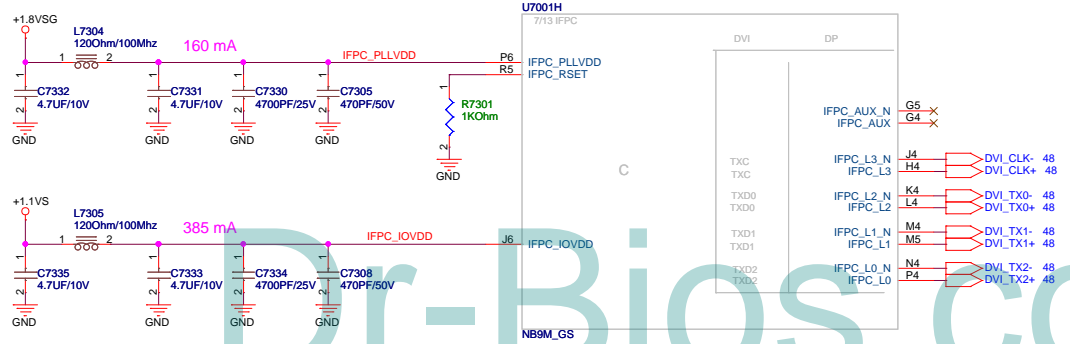
LVDS



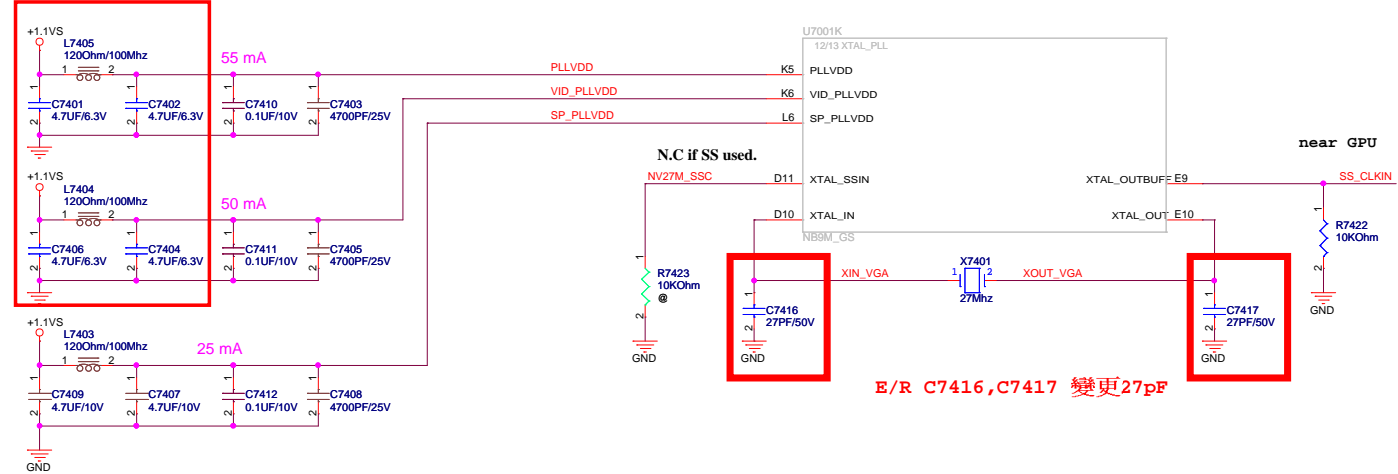
P/R V2.0 R7303 change to P/N:10G212909014010 (909 OHM 0402 1%)



HDMI

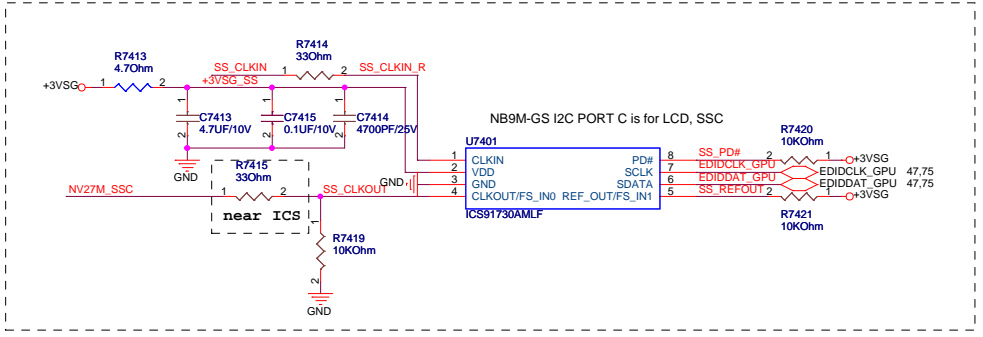


ASUS		Title : NB9MGS_DISPLAY	
ASUSTek COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
Custom	N10		1.0
Date: Monday, July 07, 2008		Sheet	73 of 97



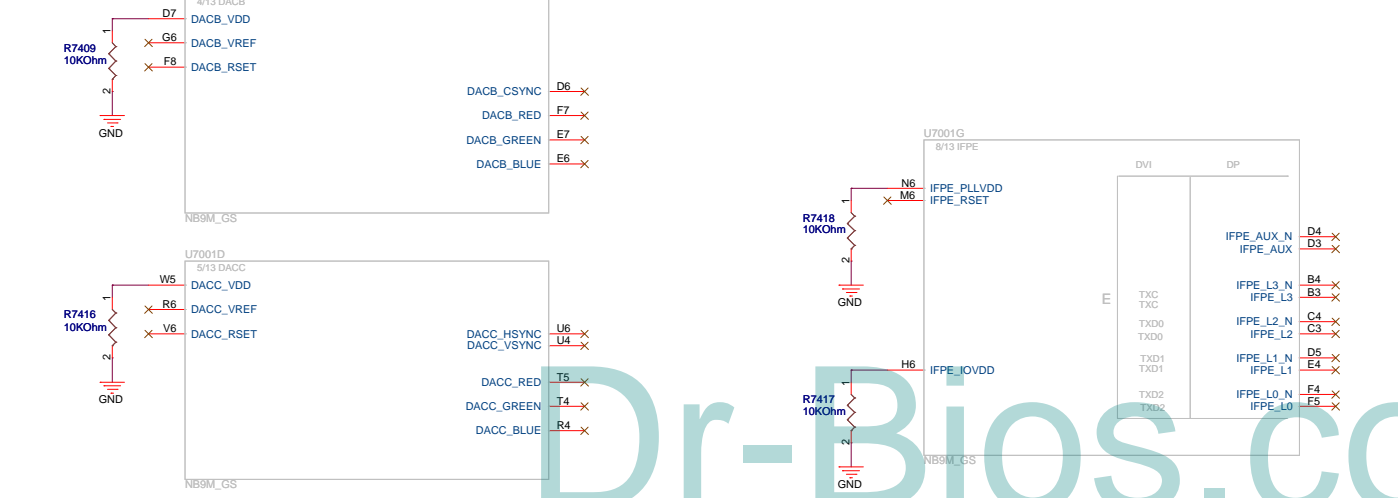
E/R C7416,C7417 變更27pF

EXTERNAL SPREAD SPECTRUM



U7001J		13/13 GND_NC	
AC11	GND_01	AA6	X
AC14	GND_02	NC_01	X
AC17	GND_03	AC19	X
AC2	GND_04	NC_02	X
AC20	GND_05	NC_03	X
AC23	GND_06	E15	X
AC26	GND_07	NC_04	X
AC3	GND_08		
ACB	GND_09		
AF11	GND_10		
AF14	GND_11		
AF17	GND_12		
AF2	GND_13		
AF20	GND_14		
AF23	GND_15		
AF26	GND_16		
AF5	GND_17		
AF8	GND_18		
B11	GND_19		
B14	GND_20		
B17	GND_21		
B2	GND_22		
B20	GND_23		
B23	GND_24		
B26	GND_25		
B5	GND_26		
B8	GND_27		
E11	GND_28		
E14	GND_29		
E17	GND_30		
E2	GND_31		
E20	GND_32		
E23	GND_33		
E26	GND_34		
E5	GND_35		
E8	GND_36		
H2	GND_37		
H5	GND_38		
J11	GND_39		
J14	GND_40		
J17	GND_41		
K19	GND_42		
K9	GND_43		
L11	GND_44		
L12	GND_45		
L13	GND_46		
L14	GND_47		
L15	GND_48		
L16	GND_49		
L17	GND_50		
L2	GND_51		
L5	GND_52		
M12	GND_53		
M13	GND_54		
M14	GND_55		
M15	GND_56		
M16	GND_57		
P19	GND_58		
P2	GND_59		
P23	GND_60		
P26	GND_61		
P5	GND_62		
P9	GND_63		
T12	GND_64		
T13	GND_65		
T14	GND_66		
T15	GND_67		
T16	GND_68		
U11	GND_69		
U12	GND_70		
U13	GND_71		
U14	GND_72		
U15	GND_73		
U16	GND_74		
U17	GND_75		
U2	GND_76		
U23	GND_77		
U26	GND_78		
U5	GND_79		
Y19	GND_80		
V9	GND_81		
W11	GND_82		
W14	GND_83		
W17	GND_84		
Y2	GND_85		
Y23	GND_86		
Y26	GND_87		
Y5	GND_88		

Other



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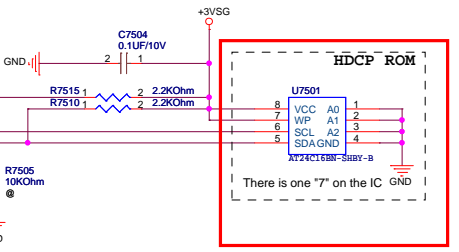
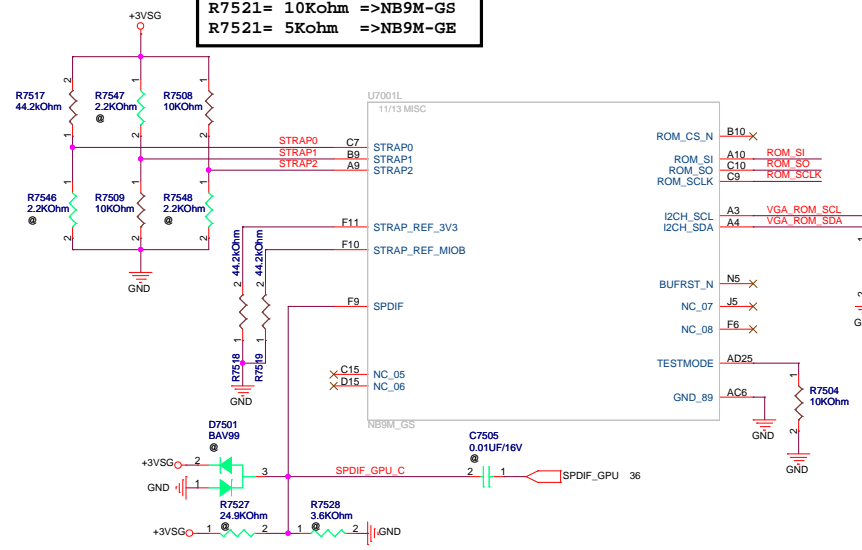
ASUS Title: NB9MGS_XTAL

ASUSTeK COMPUTER INC Engineer: ENGINEER

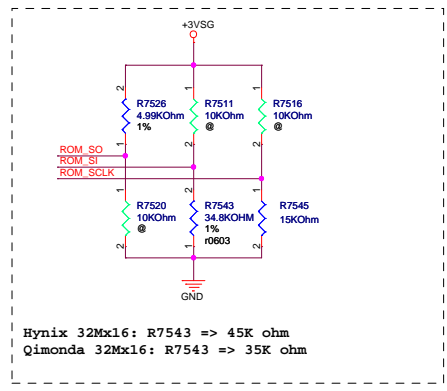
Size	Project Name	Rev
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Date: Wednesday, July 02, 2008	Sheet 74 of 97	

ROM

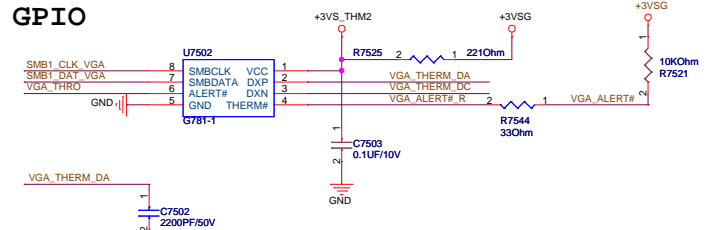
R7521= 10Kohm =>NB9M-GS
 R7521= 5Kohm =>NB9M-GE



E/R V1.1 2008/5/28 U7501 change P/N: 05G021402019

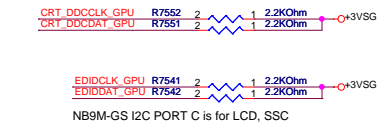
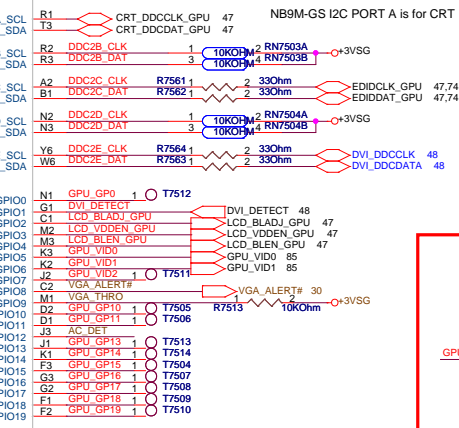
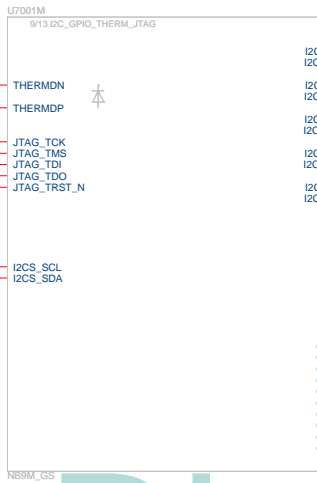


External thermal sensor

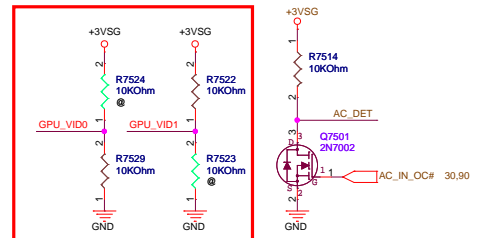


GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID 0
6	OUT	N/A	NVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	PBVPREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL




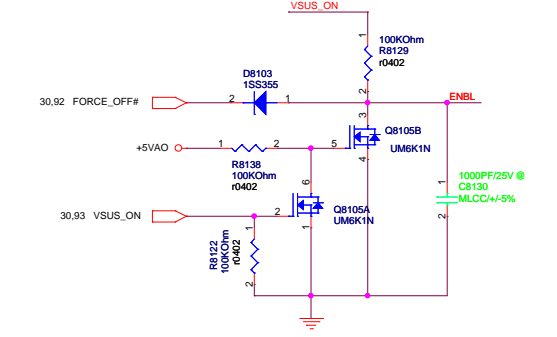
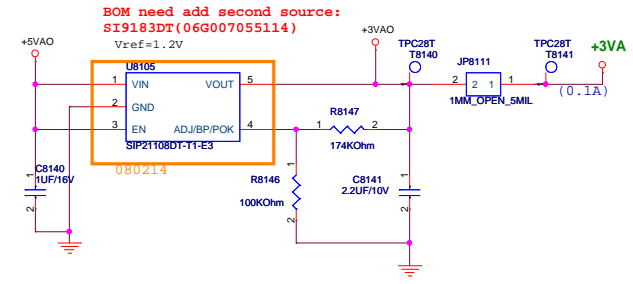
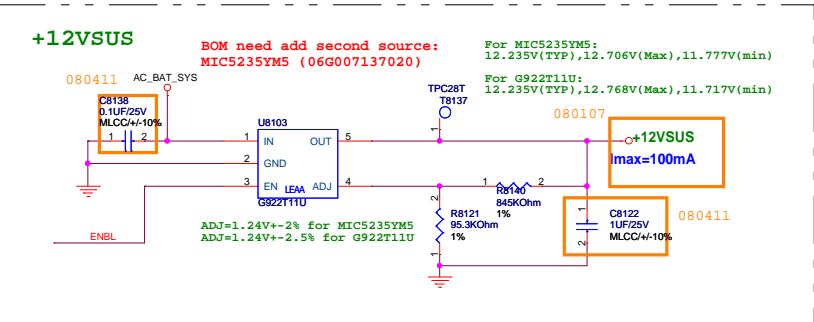
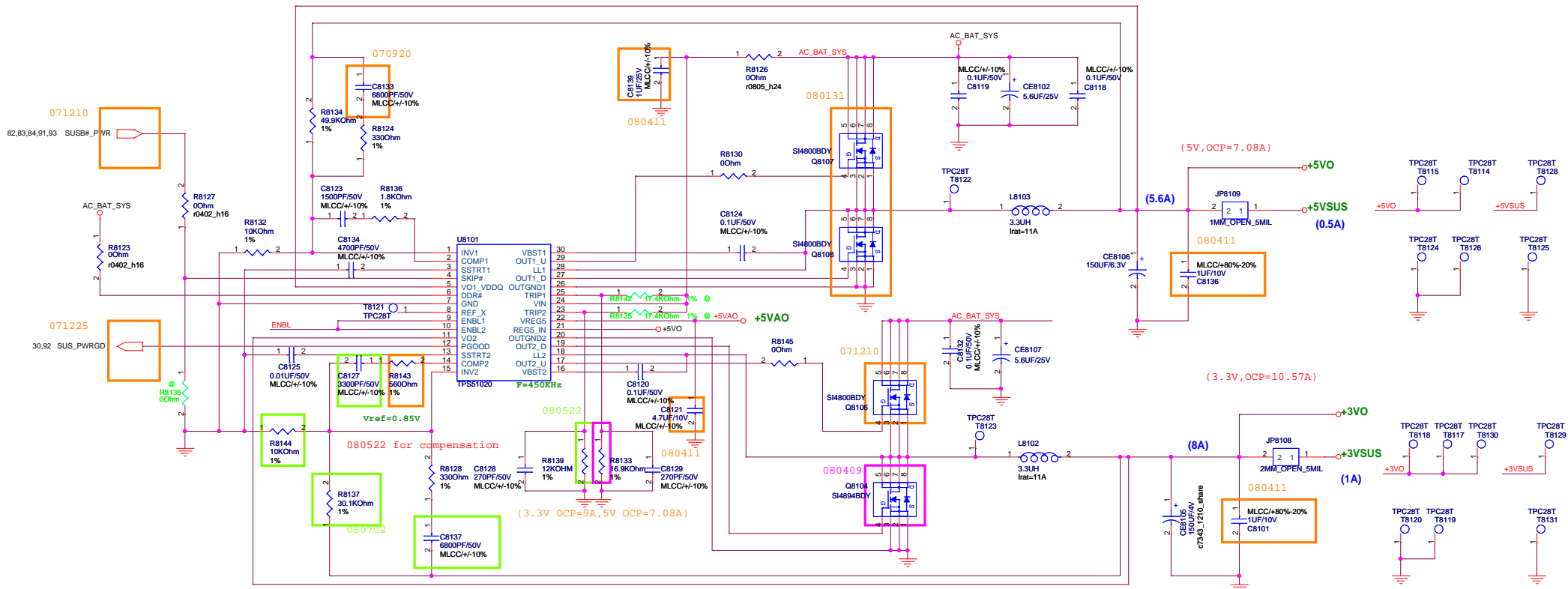
NB9M-GS I2C PORT E is for HDMI





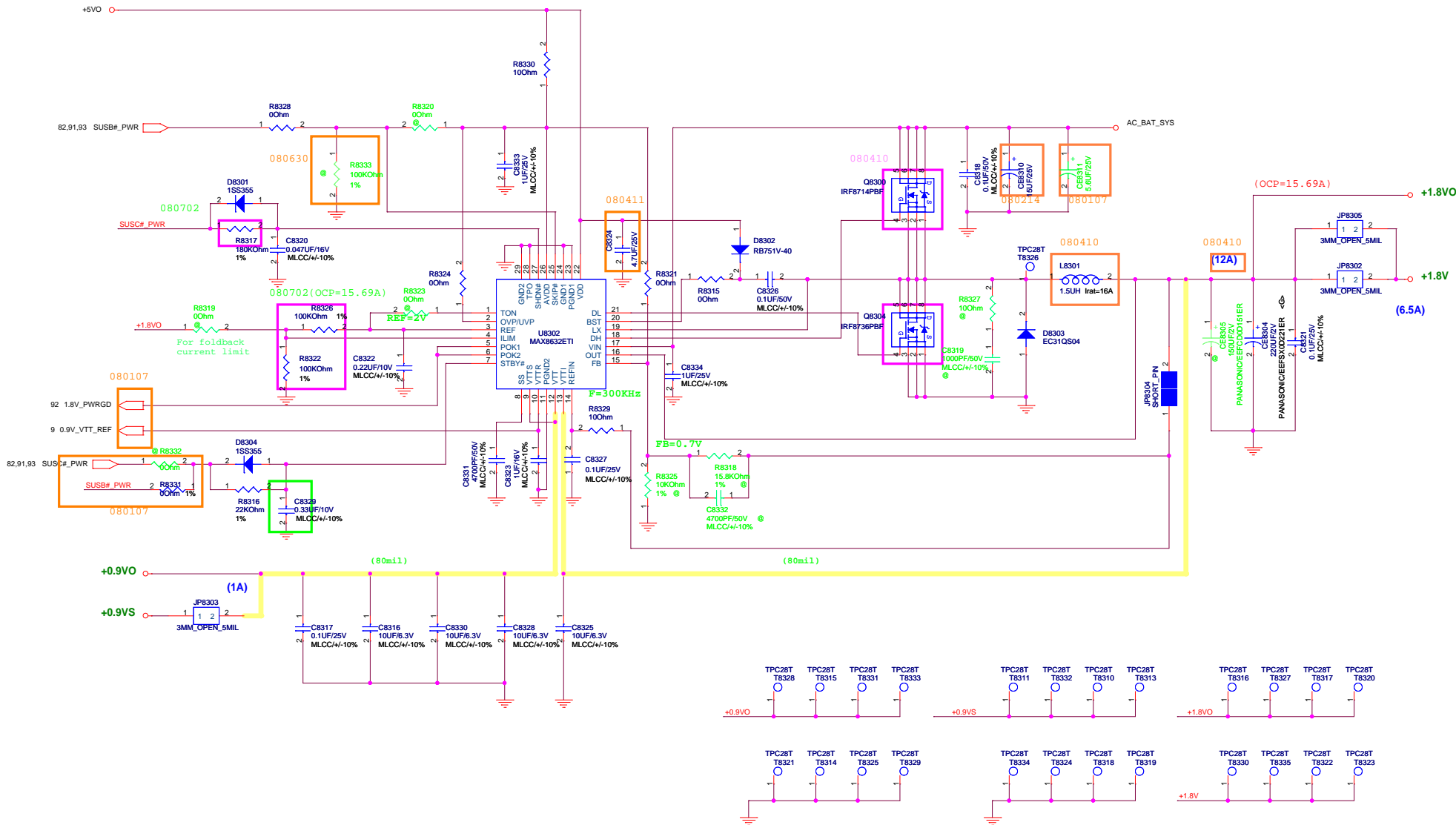
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		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
A	N10		1.0
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			1



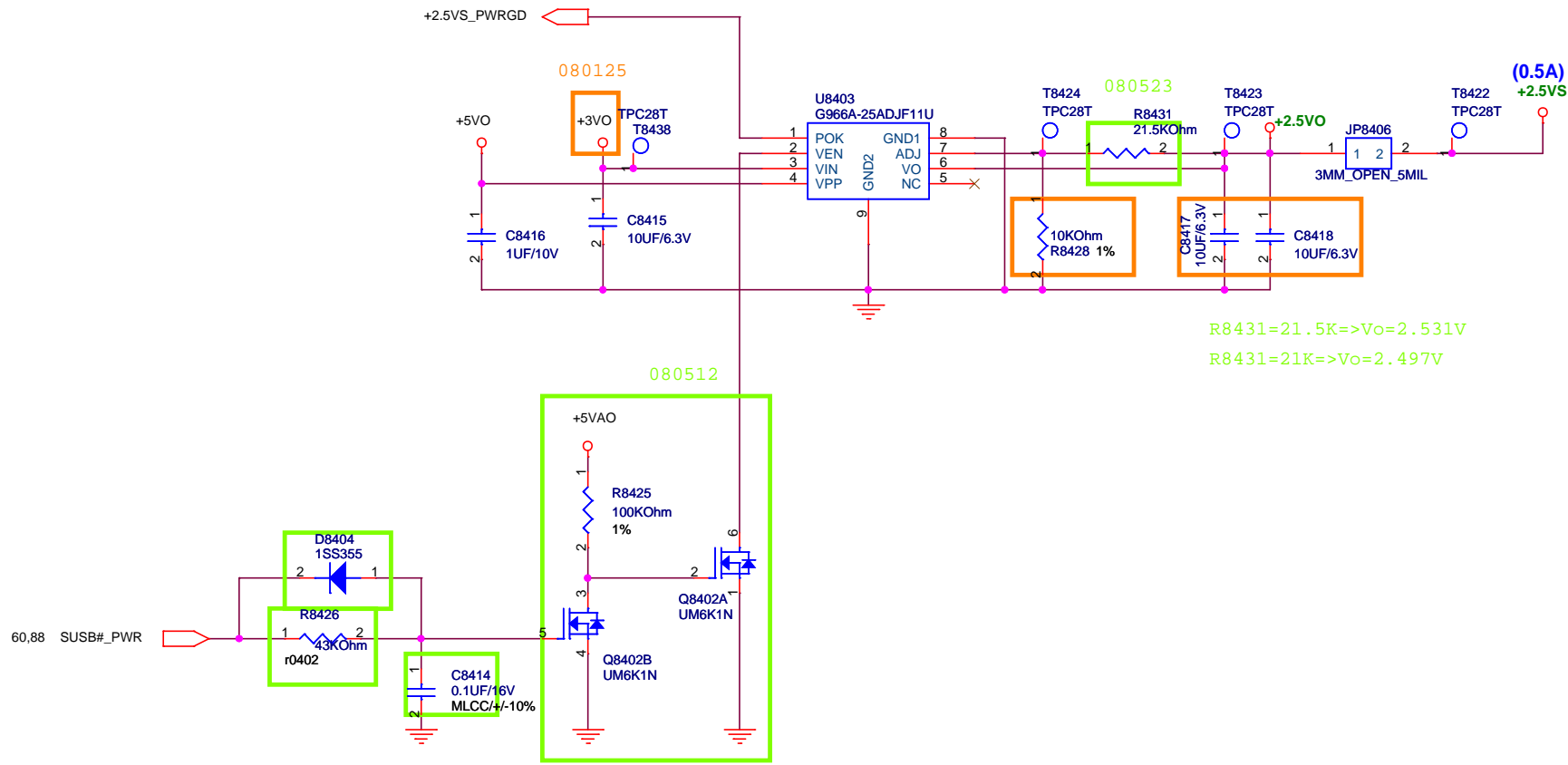
ASUS		Title : POWER_SYSTEM	
ASUSTek COMPUTER INC. NB6		Engineer: Benson	
Size	Project Name		Rev
Custom	N10		1.0
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+2.5VS

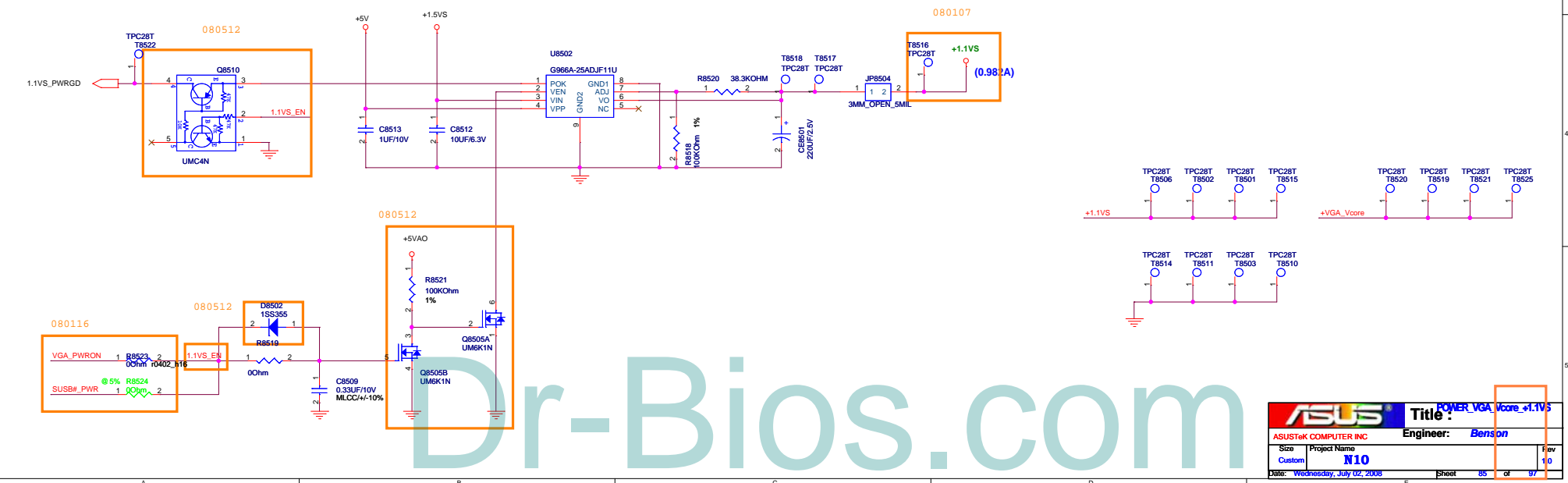
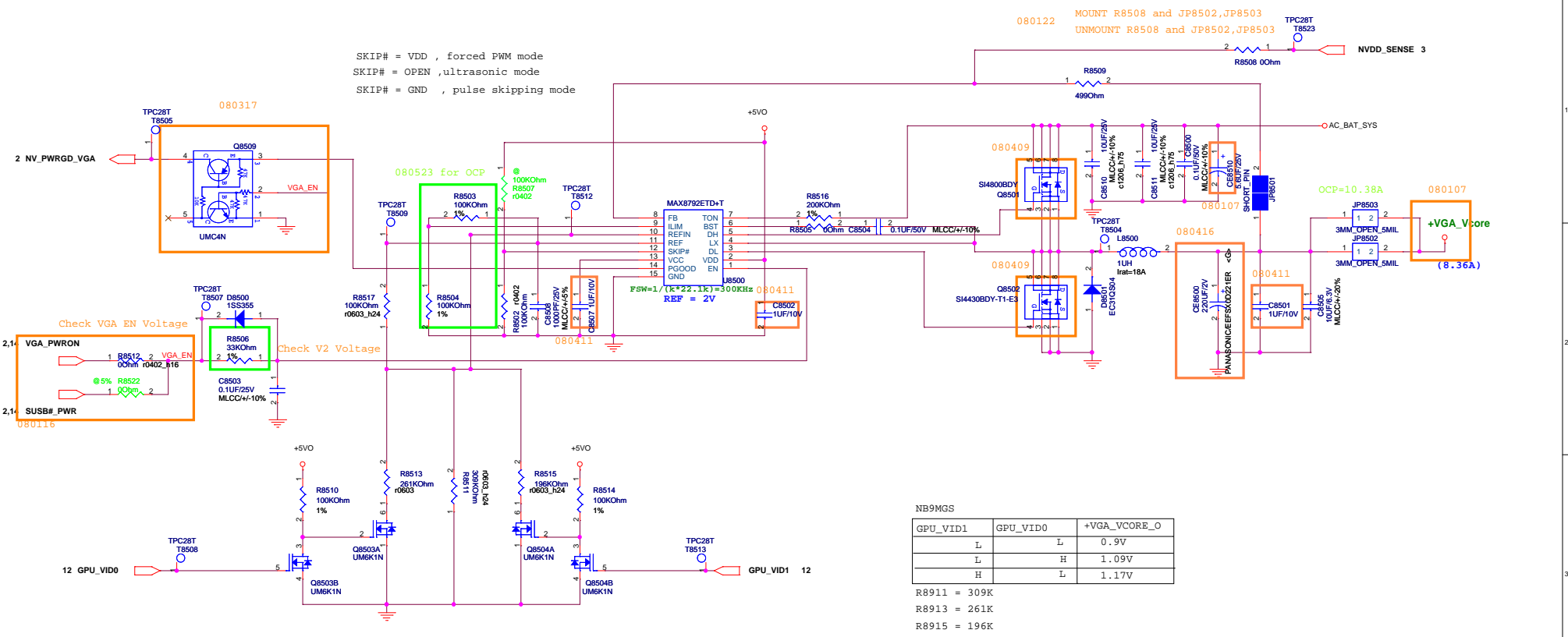


R8431=21.5K=>Vo=2.531V
R8431=21K=>Vo=2.497V

		Title : POWER_2.5VS&3VA	
ASUSTeK COMPUTER INC		Engineer: Benson	
Size Custom	Project Name N10	Rev 1.0	
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SKIP# = VDD , forced PWM mode
 SKIP# = OPEN , ultrasonic mode
 SKIP# = GND , pulse skipping mode



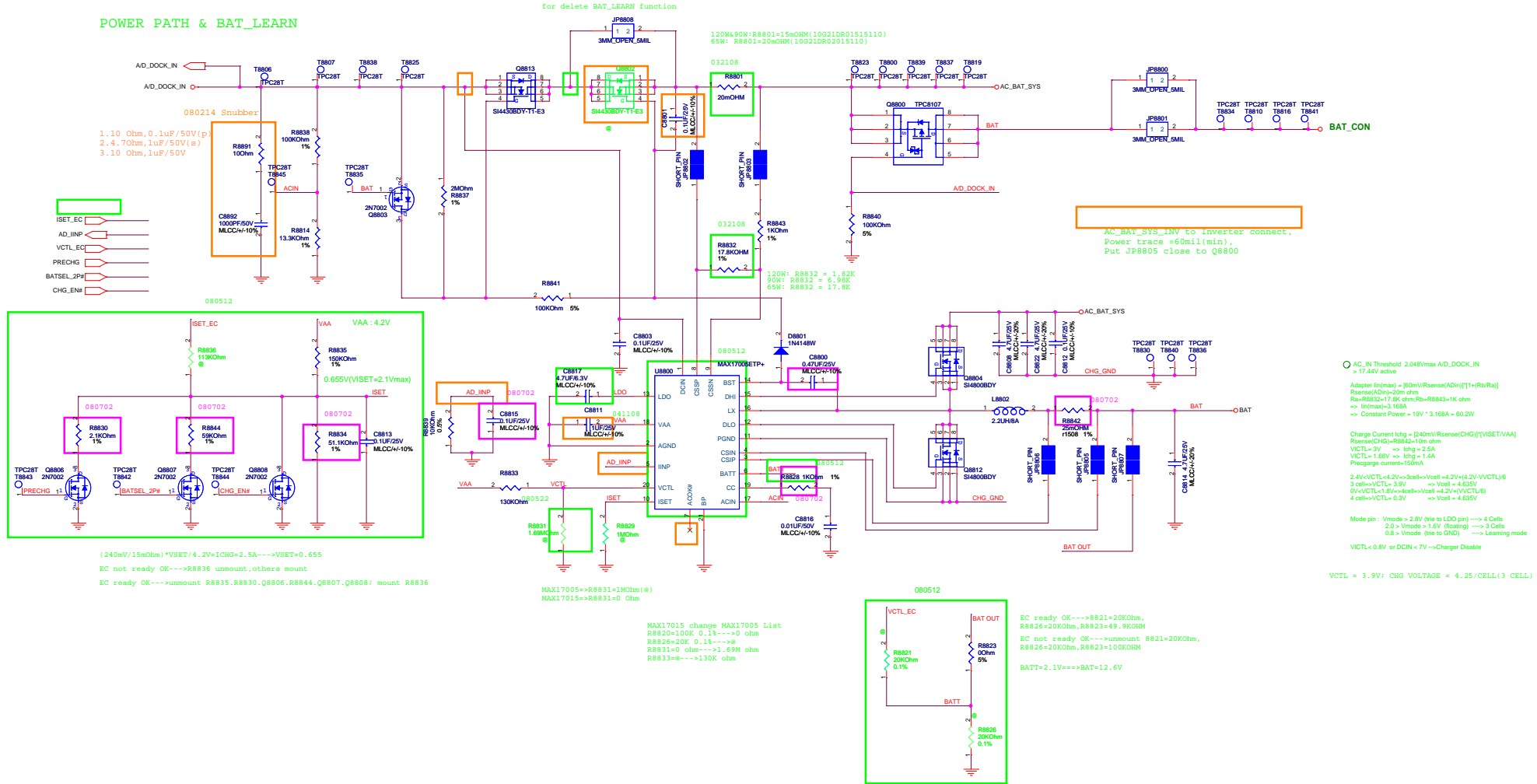
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		Title : POWER_SHUTDOWN#
ASUSTeK COMPUTER INC		Engineer: Benson
Size	Project Name	Rev
A	N10	1.0
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POWER PATH & BAT_LEARN



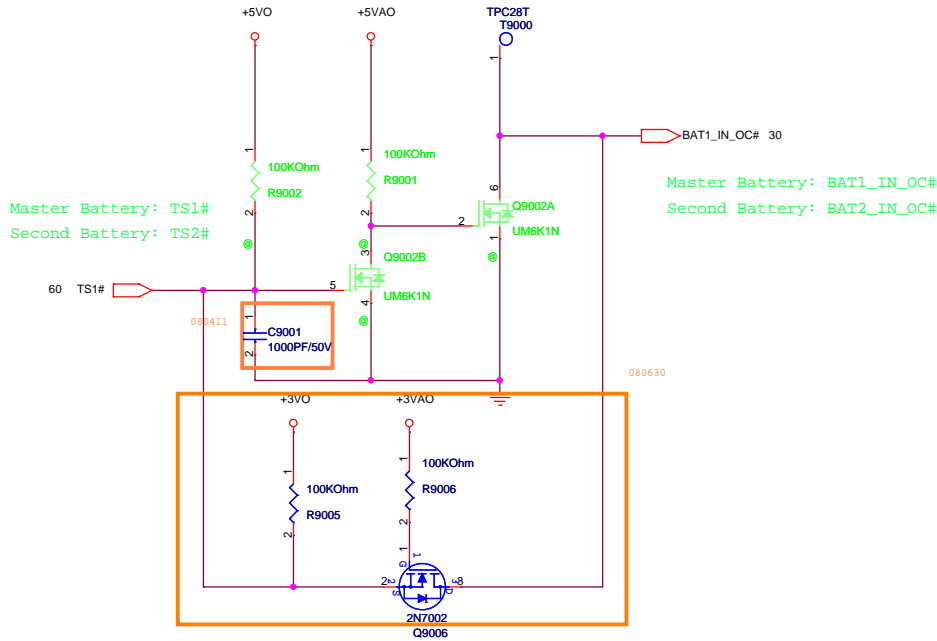
ASUS		Title : POWER_CHARGER	
Engineer: Benson			
Project Name			
Size	N10		
Rev	1.0		
Date: Wednesday, July 02, 2008	Sheet	58	of



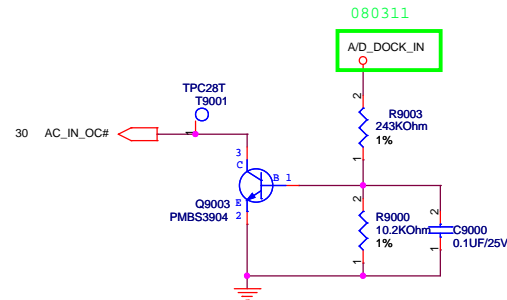
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		Title : NA	
ASUSTeK COMPUTER INC		Engineer: Benson	
Size	Project Name		Rev
A	N10		1.0
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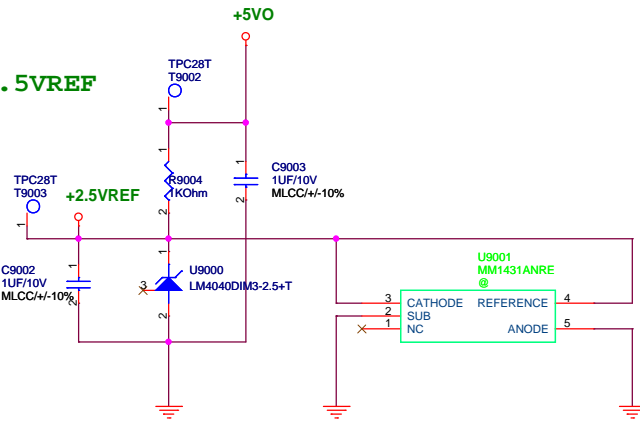
BATTERY IN DETECT



ADAPTER IN DETECT

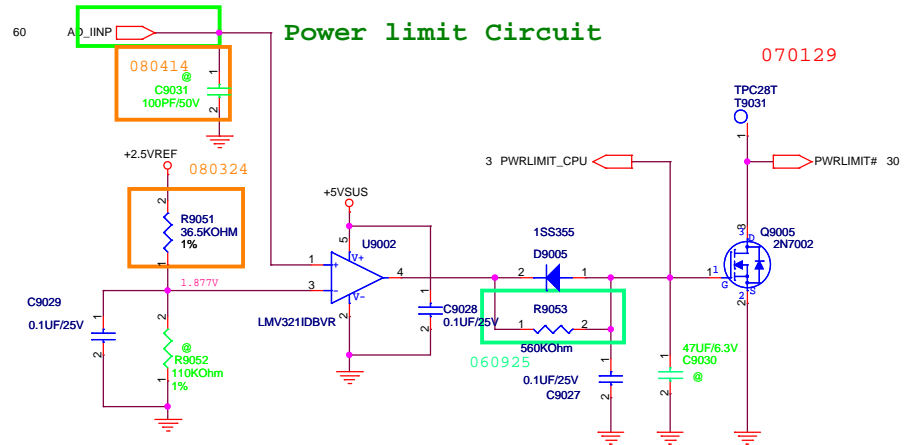


+ 2.5VREF



U8600 Main source change to 06G006002414(tolerance:1%).
Add second source 06G006002610 (tolerance:1%),
06G006002412 (tolerance:0.2%) and
06G006002020(tolerance:0.2%)

Power limit Circuit



$$V_{inp} = I_{input} * R_S * G_{linp} * R_{8807}$$

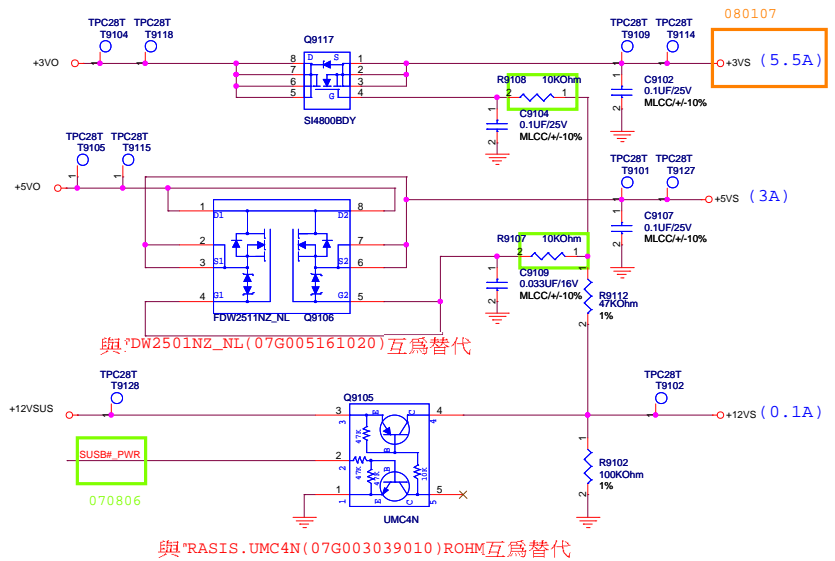
$$V_{inp} = 1.877V, R_S = 20mohm,$$

$$G_{linp} = 2.8uA/mV, I_{input} = 63.65W$$

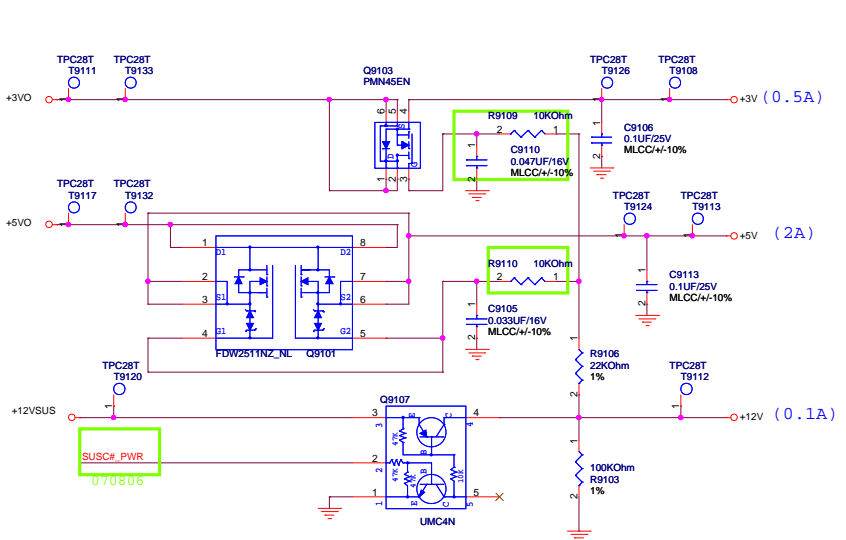
$$R_{8839} = 10K \text{ ----> } I_{input} = 3.35A$$



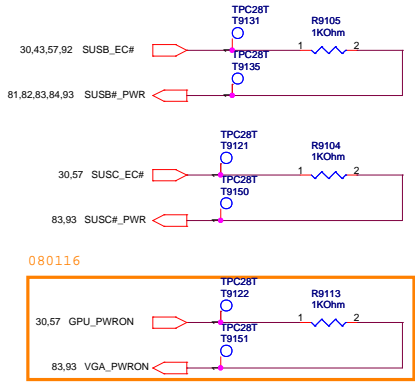
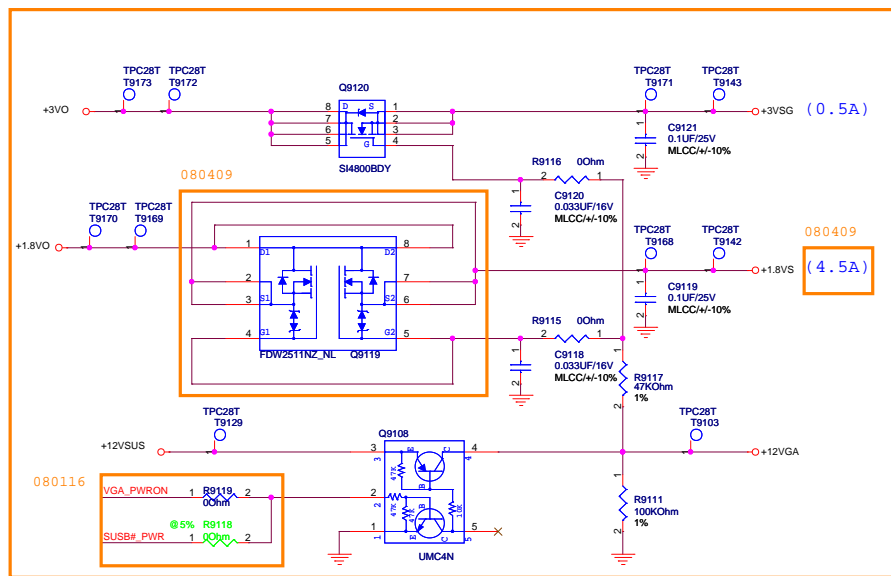
SUSB#_PWR POWER



SUSC#_PWR POWER

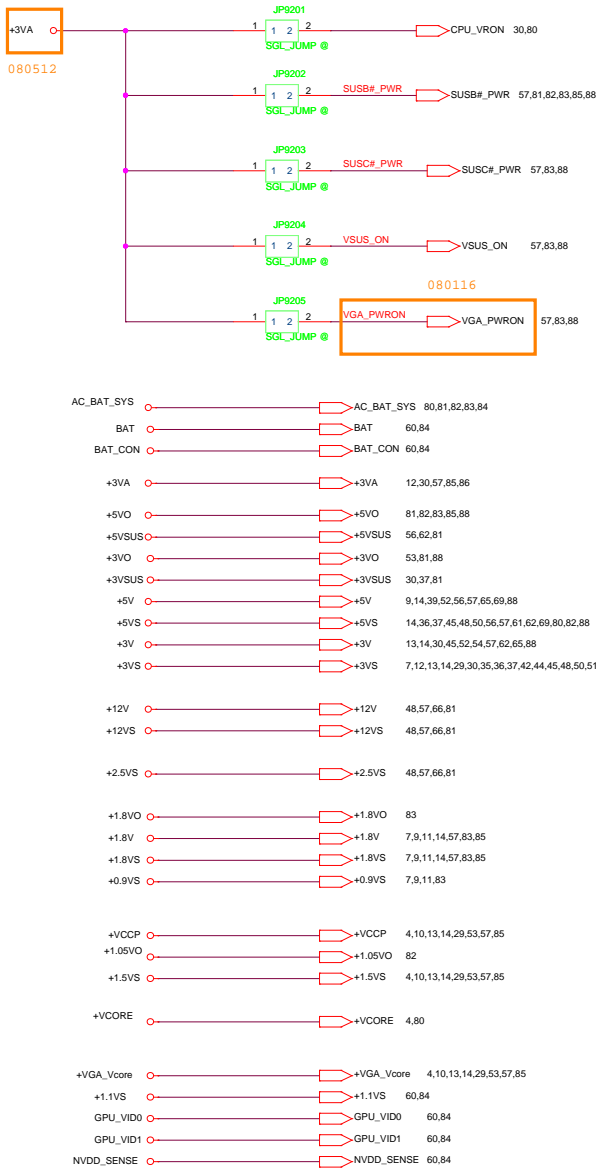


VGA_PWRON POWER

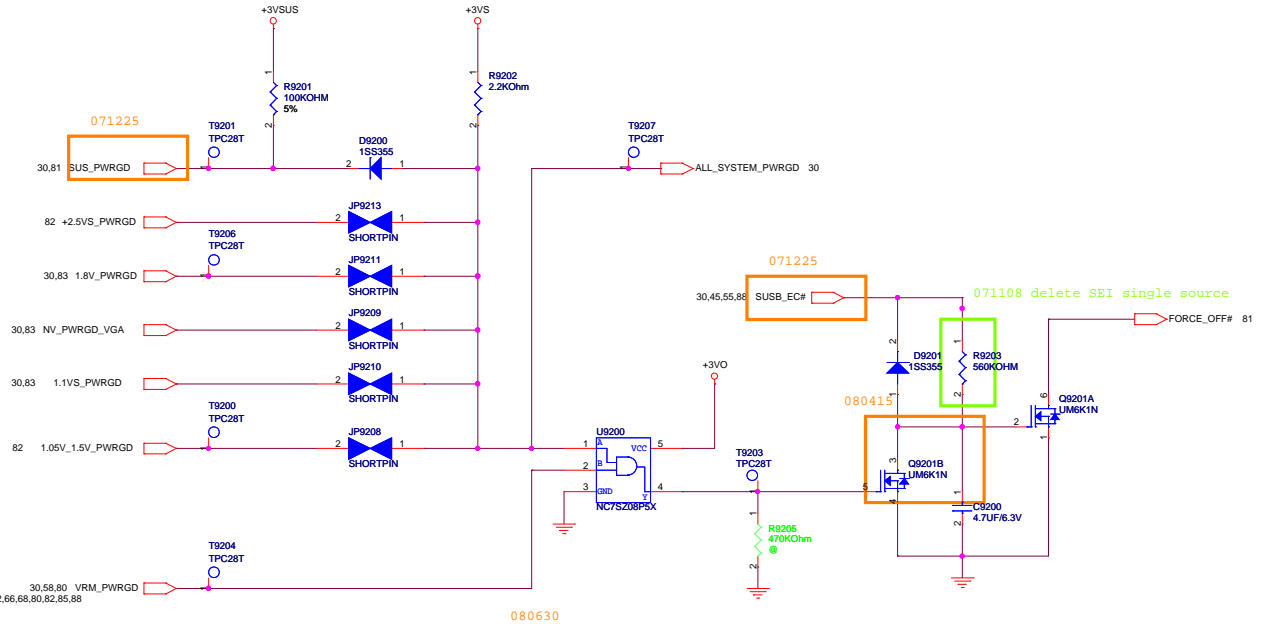


ASUS		Title: POWER_LOAD_SWITCH	
ASUSTeK COMPUTER INC		Engineer: Benson	
Size	Project Name		Rev
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FOR POWER TEST



POWER GOOD DETECTOR

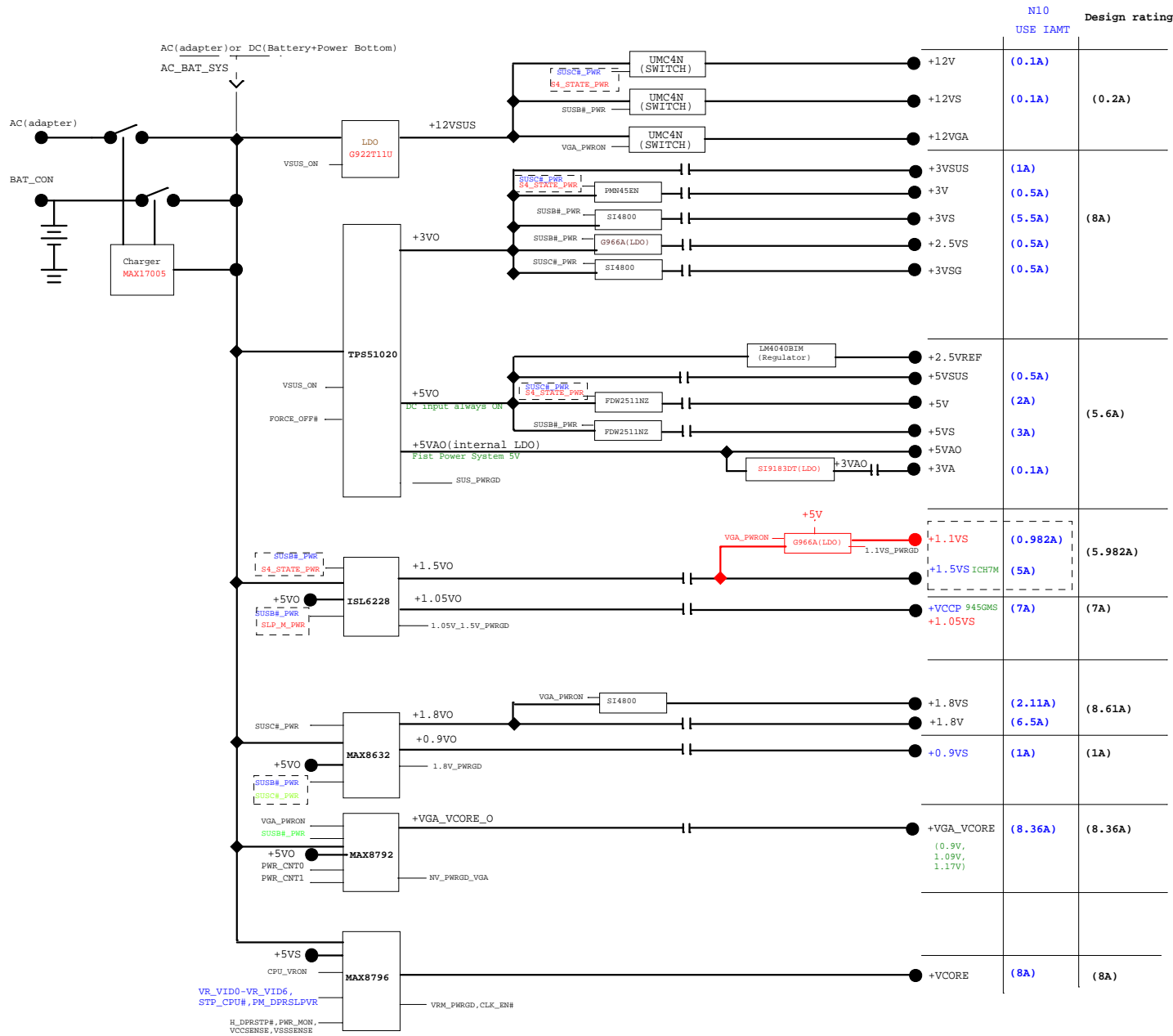


R2.0 080331 Add Q9201, R9204 and un-mount U9200 for cost down with R9209 change from 100kohm to 10 kohm

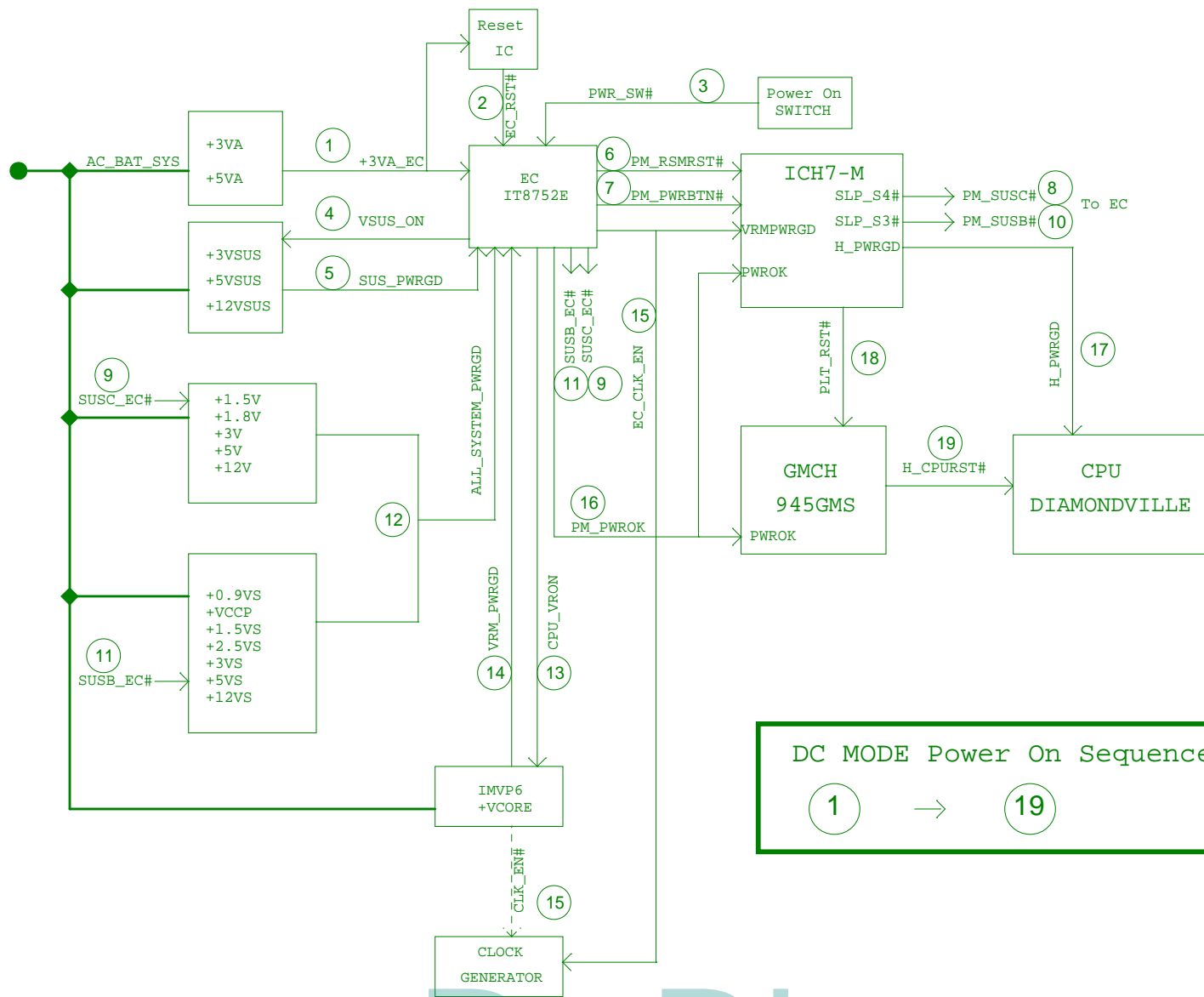
080401 Change Q9201 from 2N7002 to BSS138.

080402 Un-Mount Q9201 and R9204, mount U9200. Recover R9209 from 10Kohm to 100Kohm

ASUS		Title : Power_PROTECT_SIGMA	
ASUSTeK COMPUTER INC		Engineer: Benson	
Size	Project Name	Rev	
Custom	N10	1.0	
Date: Wednesday, July 02, 2008		Sheet	92 of 97



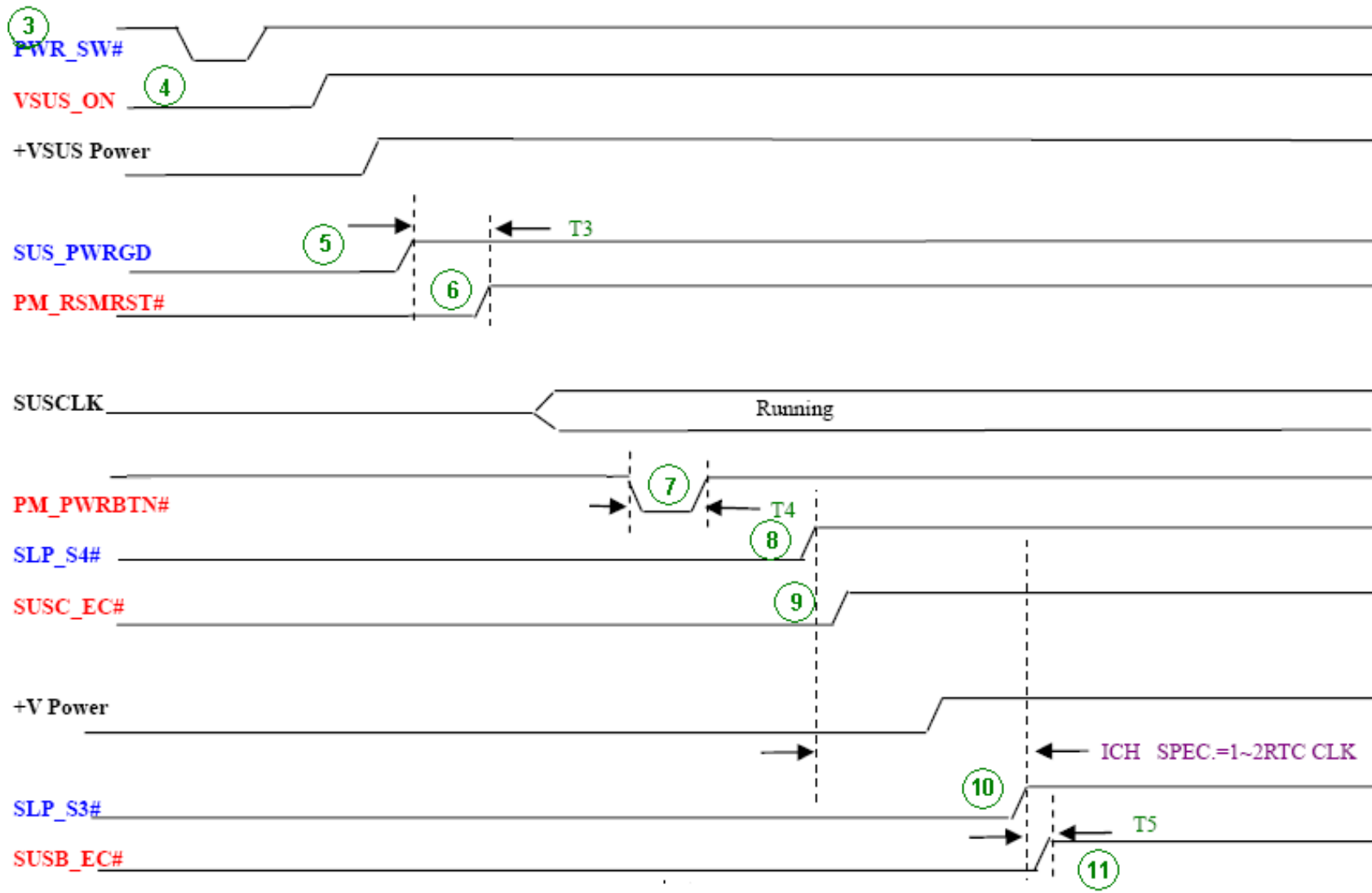
N10 POWER-ON SEQUENCE UNDER BATTERY MODE



1. Battery is plugged in only and +3VA_EC is on
2. EC_RST# is de-asserted
3. Power button is pressed
4. EC asserts VSUS_ON to turn SUS power on
5. SUS_PWRGD is asserted to indicate SUS power is OK
6. EC de-asserts PM_RSMRST# to reset RTC well of ICH7M
7. EC asserts PM_PWRBTN# to ICH7M from G2 to G0
8. ICH7M de-asserts PM_SUSC# to EC
9. EC de-asserts SUSC_EC# to turn +V power on
10. ICH7M de-asserts PM_SUSB# to EC
11. EC de-asserts SUSB_EC# to turn +VS power on
12. EC waits for ALL_SYSTEM_PWRGD
13. EC asserts CPU_VRON to turn CPU power on
14. EC waits for VRM_PWRGD
15. EC asserts EC_CLK_EN to enable clock generator
16. EC asserts PM_PWROK to 945GMS and ICH7M
17. ICH7M asserts H_PWRGD to CPU
18. ICH7M asserts PLT_RST# to reset 945GMS
19. 945GMS asserts H_CPURST# to reset CPU

DC MODE Power On Sequence
 1 → 19

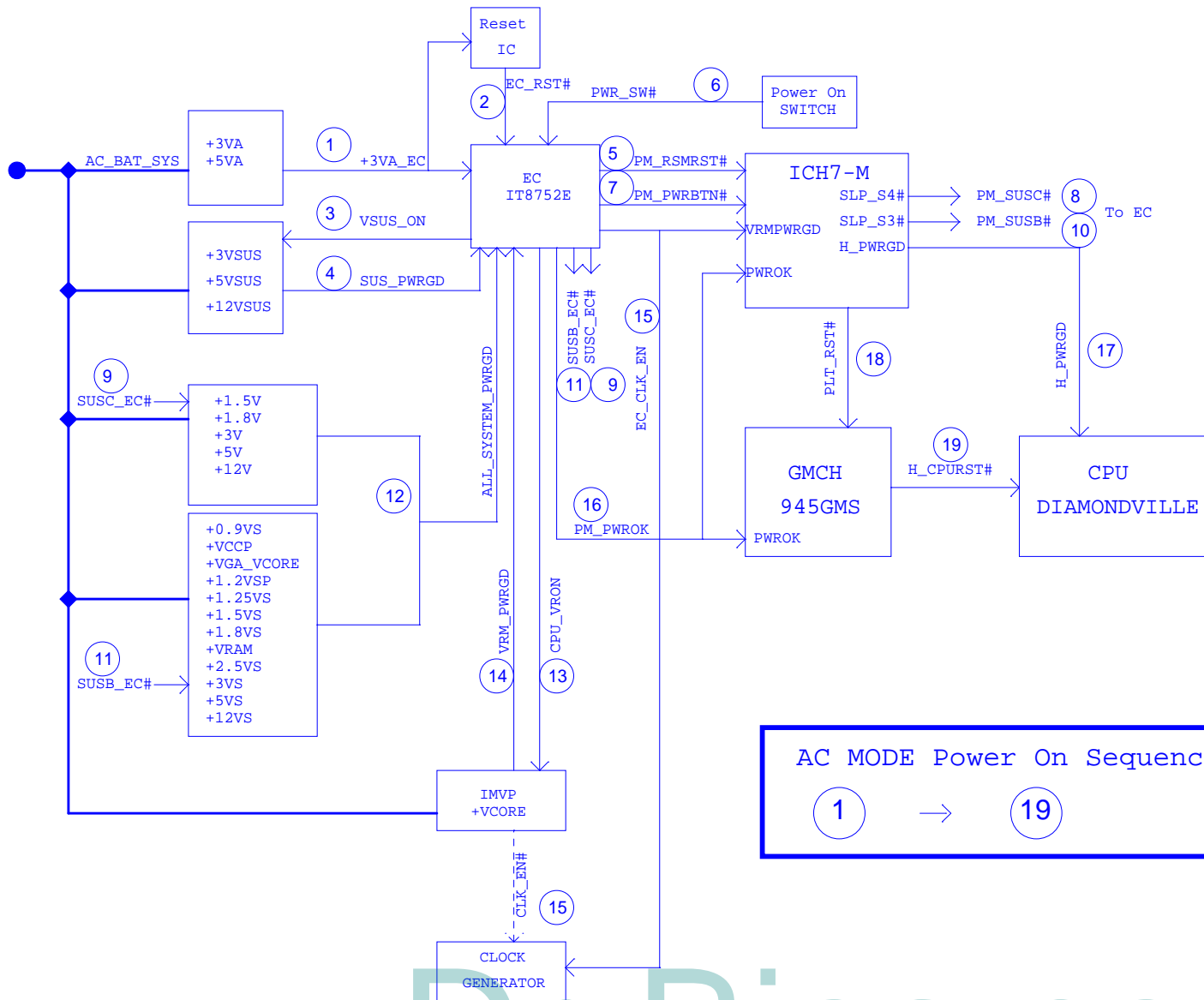
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ASUS		Title : POWER ON SEQUENCE(1)	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
A	N10		0.1
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N10 POWER-ON SEQUENCE UNDER BATTERY MODE

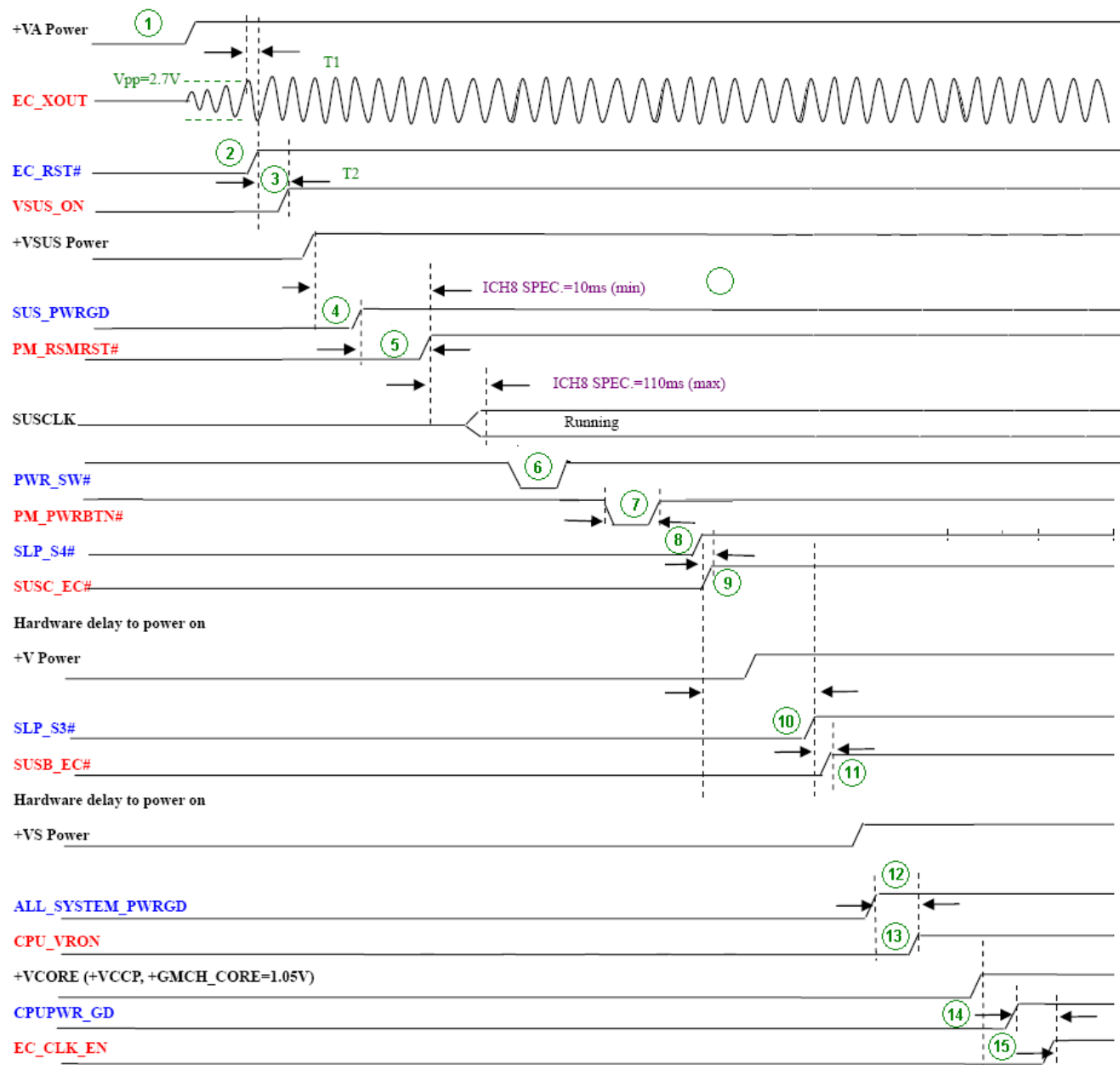


1. Battery is plugged in only and +3VA_EC is on
2. EC_RST# is de-asserted
3. Power button is pressed
4. EC asserts VSUS_ON to turn SUS power on
5. SUS_PWRGD is asserted to indicate SUS power is OK
6. EC de-asserts PM_RSMRST# to reset RTC well of ICH7M
7. EC asserts PM_PWRBTN# to ICH7M from G2 to G0
8. ICH7M de-asserts PM_SUSC# to EC
9. EC de-asserts SUSC_EC# to turn +V power on
10. ICH7M de-asserts PM_SUSB# to EC
11. EC de-asserts SUSB_EC# to turn +VS power on
12. EC waits for ALL_SYSTEM_PWRGD
13. EC asserts CPU_VRON to turn CPU power on
14. EC waits for VRM_PWRGD
15. EC asserts EC_CLK_EN to enable clock generator
16. EC asserts PM_PWROK to 945GMS and ICH7M
17. ICH7M asserts H_PWRGD to CPU
18. ICH7M asserts PLT_RST# to reset 945GMS
19. 945GMS asserts H_CPURST# to reset CPU

AC MODE Power On Sequence



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ASUS		Title : POWER ON SEQUENCE(1)	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
B	N10	0.1	
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