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PBL80 Project

LA-7441P REV 0.3 Schematic

Intel Sandy Bridge/Cougar Point

N12P-GS/Co lay GV - Optimus Only

2011-04-07 Rev. 0.3

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

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Title: Cover Page

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 1 of 59

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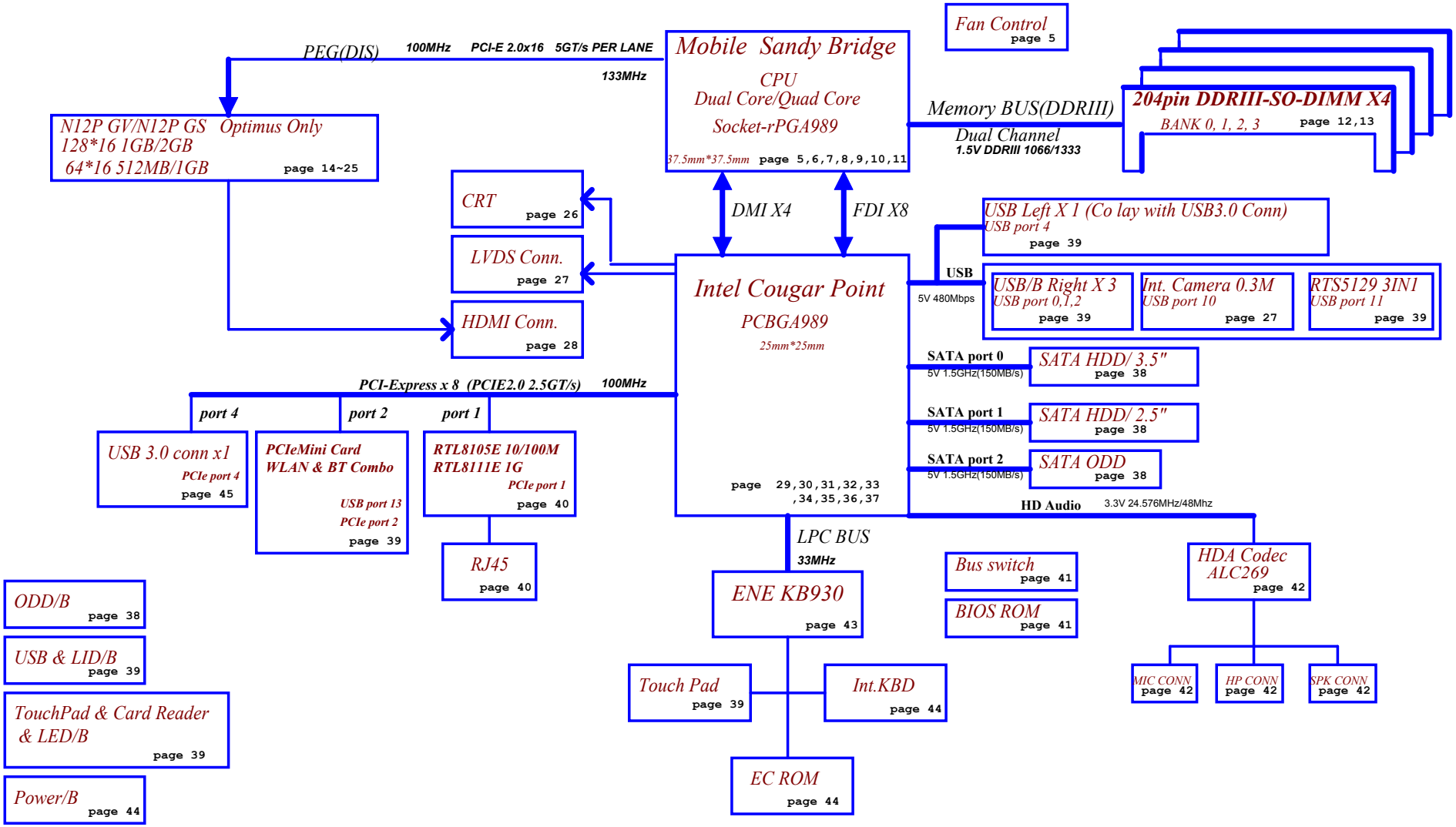
Model Name : PBL80 File

Name : LA-7441P



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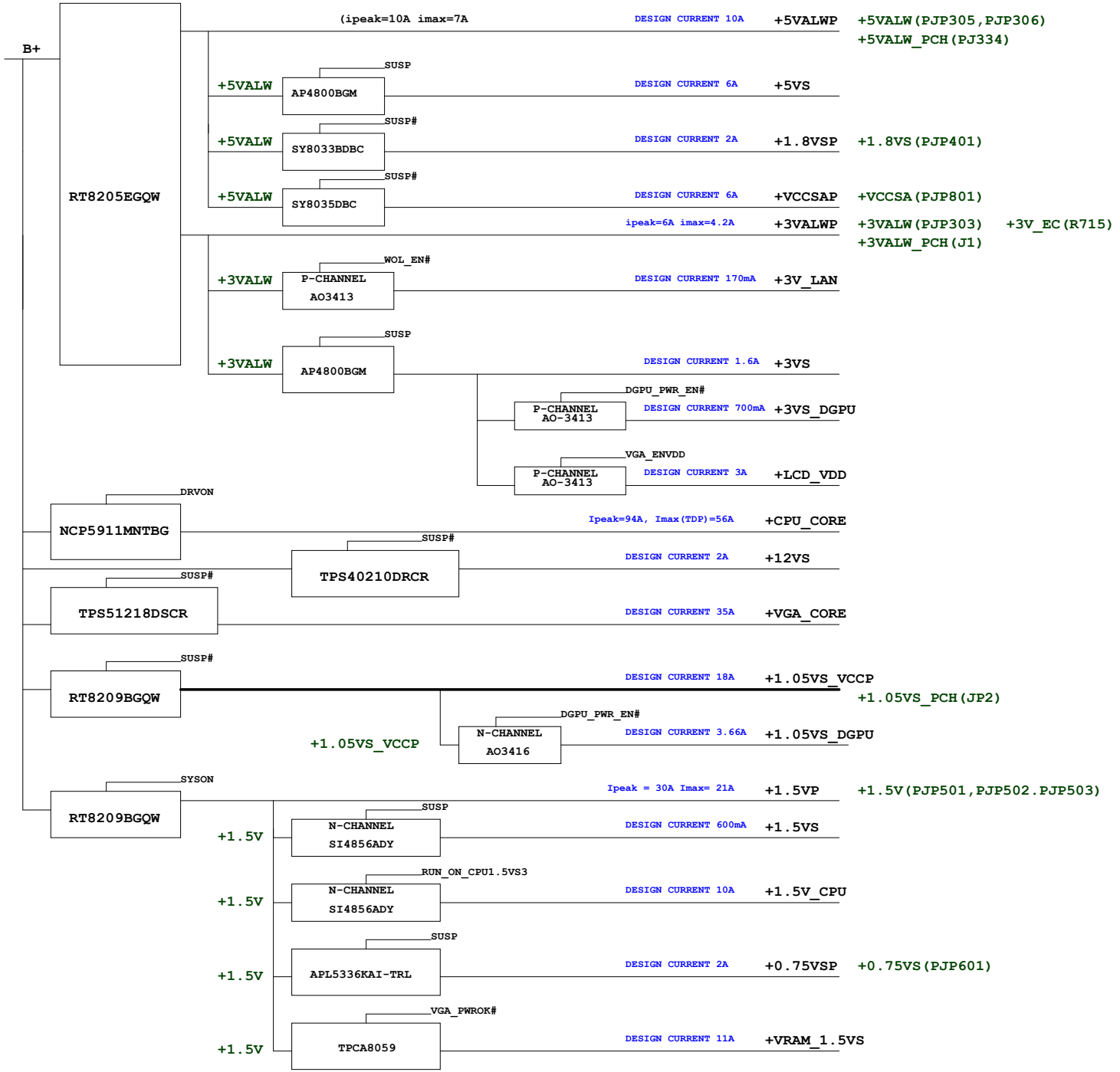
Title: Block Diagrams

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 2 of 59



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Title: Power Map

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 3 of 59

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +5VALW_PCH +3VALW_PCH +3V_LAN +3V_EC +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS_VCCP +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VCCSA +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +12VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

Function	VRAM					GPU		Board ID
description	VRAM	Samsung 64bits	Hynix 64bits	Samsung 128bits	Hynix 128bits	N12P-GS	N12P-GV	Adaptor
explain	VRAM	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Adaptor
BTO	8PCS@	PD 20K	PD 15K	PD 45.3K	PD 34.8K	N12PGS@	N12PGV@	90W@, 120W@

Function	Crisis recovery	HDMI	WLAN+BT		LAN	
description	BUS SWITCH	HDMI	WLAN+BT(BT pin 51)	WLAN+BT(BT pin 5)	Giga LAN	10/100M LAN
explain	BUS SWITCH	HDMI	WLAN+BT(BT pin 51)	WLAN+BT(BT pin 5)	Strap pin	Strap pin
BTO	Debug@	HDMI@	BT@	COMBO@	8111E@	8105E@

Function	USB3.0/2.0 Colay		SATA3.0 Repeater Chip		SATA Preemphasis		SATA Equalization	
description	USB3.0	USB2.0	MAXIM	TI	Preemphasis		Equalization	
explain	USB3.0	USB2.0	MAX4951	SN75LVCP601	Enable	Disable	Maximum	Normal
BTO	USB3@	USB2@	MAXIM@	TI@	DEN@	NDEN@	EQ@	NEQ@

Function	SATA path	
description	PCH	Repeater
explain	PCH	Repeater
BTO	SATA@	SATARP@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMMA1	A0 H	1010 0000 b
+3VS	DDR SO-DIMMA2	A0 H	1010 0010 b
+3VS	DDR SO-DIMMB1	A4 H	1010 0100 b
+3VS	DDR SO-DIMMB2	A0 H	1010 0110 b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	VGA Thermal Sensor (Internal)	9E H	1001 1010 b

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Title: Notes List

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 4 of 59

Support Dual Core/ Quad Core

C1 2 1 H_PWRGOOD
0.1U_0402_16V4Z
C2 2 1 H_PROCHOT#
0.1U_0402_16V4Z
C55 2 1 PM_SYS_PWRGD_BUF
0.1U_0402_16V4Z

JCPUB

<33> H_SNB_IVB# → C26 SNB_IVB#
T1 PAD @ TP_SKTOCC# → AN34 SKTOCC#
MISC

T2 PAD @ H_CATERR# → AL33 CATERR#
<34,43> H_PECI → AN33 PECI
<43> H_PROCHOT# → R6 56_0402_5% → AL32 PROCHOT#
<34> H_THERMTRIP# → R10 0_0402_5% → AN32 THERMTRIP#
THERMAL

<31> H_PM_SYNC → AM34 PM_SYNC
<34> H_PWRGOOD → AP33 UNCOREPWRGOOD
PM_SYS_PWRGD_BUF → R22 130_0402_5% → V8 SM_DRAMPWROK
BUF_CPU_RST# → AR33 RESET#
PWR MANAGEMENT

CLOCKS
BCLK A28 / BCLK# A27 → CLK_CPU_DMI <30> / CLK_CPU_DMI# <30>
DPLL_REF_SSCLK A16 / DPLL_REF_SSCLK# A15 → R3 / R4 1K_0402_5% / 1K_0402_5% → +1.05VS_VCCP
eDP

If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor

DDR3 MISC
SM_DRAMRST# R8 H_DRAMRST# → H_DRAMRST# <7>
SM_RCOMP[0] AK1 SM_RCOMP_0 R7 140_0402_1%
SM_RCOMP[1] A5 SM_RCOMP_1 R8 25.5_0402_1%
SM_RCOMP[2] A4 SM_RCOMP_2 R9 200_0402_1%
DDR3 Compensation Signals Layout Note:Please these resistors near Processor
from DDR

JTAG & BPM
PRDY# AP29 XDP_PRDY#_R R11 0_0402_5% XDP_PRDY#
PREQ# AP27 XDP_PREQ#_R R12 0_0402_5% XDP_PREQ#
TCK AR26 XDP_TCK_R R13 0_0402_5% XDP_TCK
TMS AR27 XDP_TMS_R R14 0_0402_5% XDP_TMS
TRST# AP30 XDP_TRST#_R R15 0_0402_5% XDP_TRST#
Routed as a single daisy chain
TDI AR28 XDP_TDI_R R16 0_0402_5% XDP_TDI
TDO AR26 XDP_TDO_R R18 0_0402_5% XDP_TDO
DBR# AL35 XDP_DBRESET#_R R21 0_0402_5% XDP_DBRESET#
R20 1K_0402_5% +3VS → XDP_DBRESET# <29,31>
BPM[0] AT28 XDP_BPM#0_R R24 0_0402_5% XDP_BPM#0
BPM[1] AR29 XDP_BPM#1_R R25 0_0402_5% XDP_BPM#1
BPM[2] AR30 XDP_BPM#2_R R26 0_0402_5% XDP_BPM#2
BPM[3] AT30 XDP_BPM#3_R R27 0_0402_5% XDP_BPM#3
BPM[4] AP32 XDP_BPM#4_R R28 0_0402_5%
BPM[5] AR31 XDP_BPM#5_R R30 0_0402_5%
BPM[6] AT31 XDP_BPM#6_R R32 0_0402_5%
BPM[7] AR32 XDP_BPM#7_R R34 0_0402_5%
CFG12 <10>
CFG13 <10>
CFG14 <10>
CFG15 <10>
Close to CPU side

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+1.05VS_VCCP
Processor Pullups
R17 2 1 62_0402_5% H_PROCHOT#
R23 2 1 10K_0402_5% H_PWRGOOD

Follow DG 0.71

+3VALW
FIT 1.5V POWER PLANE OF CPU
C3 0.1U_0402_16V4Z
U1 74AHC1G09GW_TSSOP5
+1.5V_CPU
R36 200_0402_5%
<31> PWROK → R37 0_0402_5%
<31> DRAMPWROK
PM_SYS_PWRGD_BUF
@ R38 39_0402_5%
<46,53> SUSP → SUSP
@ Q1 2N7002_SOT23
CHANGE U5 TO OPEN DRAIN MOS,OUTPUT=1.5V

PU/PD for JTAG signals
+1.05VS_VCCP
XDP_TMS_R R39 51_0402_5%
XDP_TDI_R R40 51_0402_5%
XDP_TDO_R R41 51_0402_5%
XDP_TCK_R R42 51_0402_5%
XDP_TRST#_R R43 51_0402_5%

Buffered reset to CPU

C56 PLT_RST# 0.1U_0402_16V4Z
C57 PLT_RST# 0.1U_0402_16V4Z
For ESD request
+3VS
C6 0.1U_0402_16V4Z
+1.05VS_VCCP
R50 75_0402_5%
R52 43_0402_1%
U3 SN74LVC1G07DCKR_SC70-5
<33,39> PLT_RST# → R55 0_0402_5%
BUFO_CPU_RST# → BUF_CPU_RST#
@ R53 0_0402_5%

XDP Connector

JXDP1 @
XDP_PREQ#
XDP_PRDY#
XDP_BPM#0
XDP_BPM#1
XDP_BPM#2
XDP_BPM#3
<29,31,43> PBTN_OUT# → H_PWRGOOD R44 1K_0402_5%
<10> CFG0 → PBTN_OUT# R45 0_0402_5%
<31,43,55> VGATE → CFG0 R46 1K_0402_5%
<10,30> CLK_RES_ITP → VGATE R47 0_0402_5%
<10,30> CLK_RES_ITP# → +1.05VS_VCCP
PLT_RST# R48 1K_0402_5%
XDP_CPU_HOOK0
XDP_CPU_HOOK1
XDP_CPU_HOOK2
XDP_CPU_HOOK3
XDP_CPU_HOOK6
XDP_DBRESET#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_TCK
C8 0.1U_0402_10V6K
C27 1U_0603_10V6K
ACES_87152-26051
For ESD request.

FAN Control Circuit

+5VS
1A
C4 10U_0805_10V4Z
U2 G996P11U SOP 8P
EN VIN VOUT VSET GND GND GND GND
+FAN_VCC
<43> EN_DFAN1 → R49 330_0402_5%
C7 0.047U_0402_16V7K
C5 @ 1000P_0402_50V7K
20mil
JFAN CVILU_CI4403M1HRT-NH @
GND GND
R51 10K_0402_5% +3VS
FAN_SPEED1 <43>
C9 @ 0.01U_0402_25V7K

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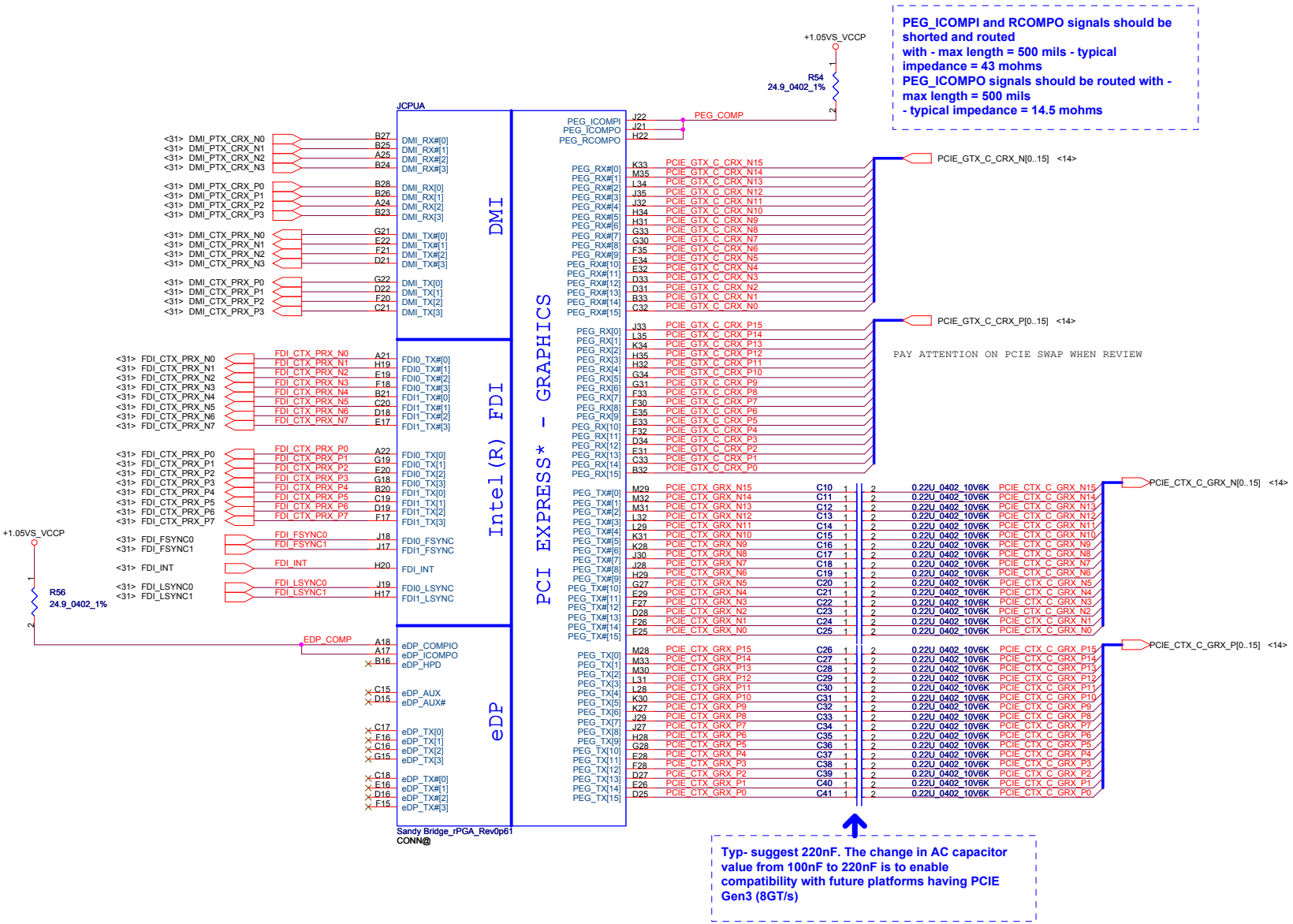
Title: Sandy Bridge(1/6)-CLK/MISC/JTAG/XDP/FAN
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3
Date: Monday, April 11, 2011 | Sheet 5 of 59



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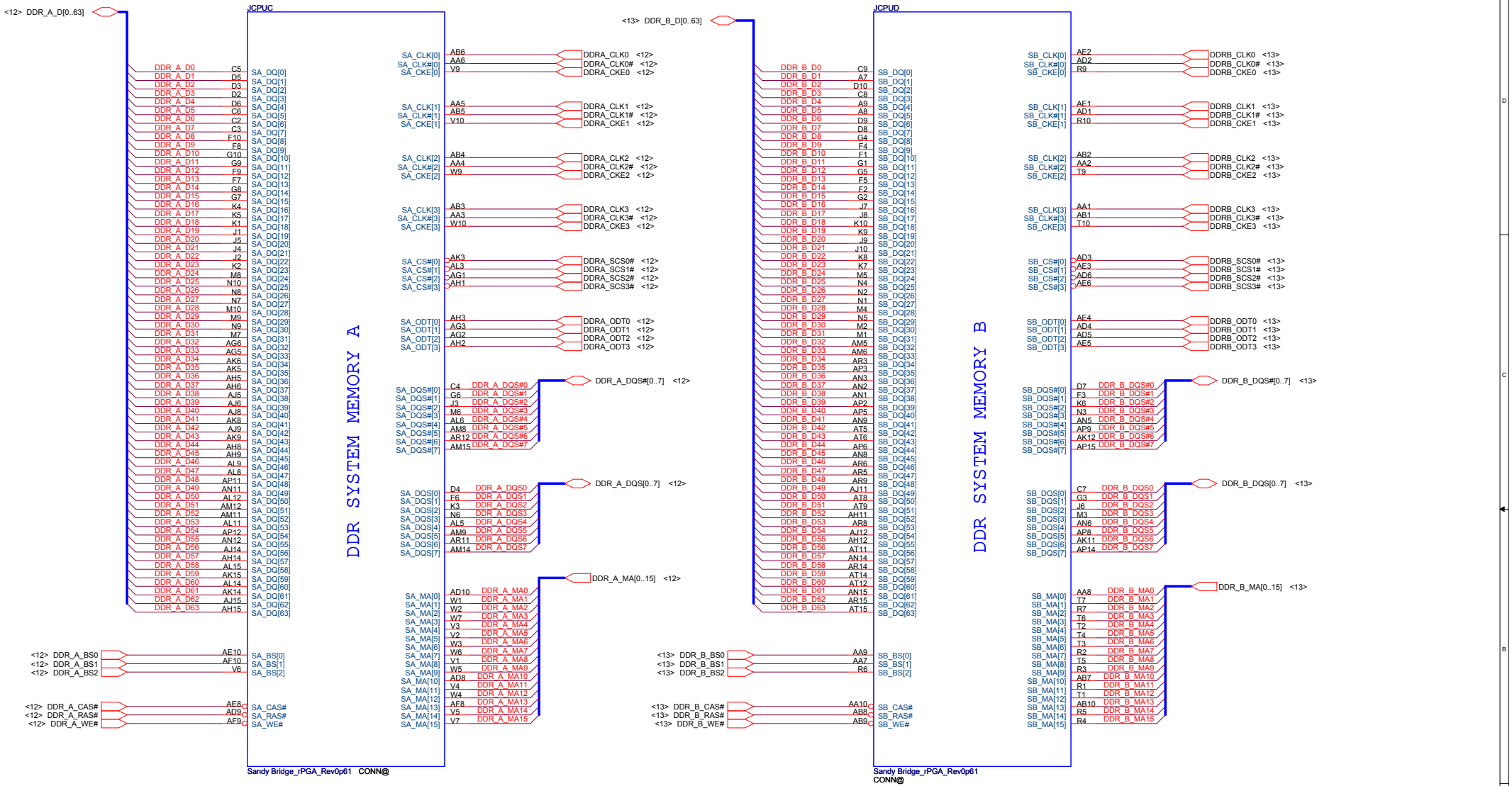
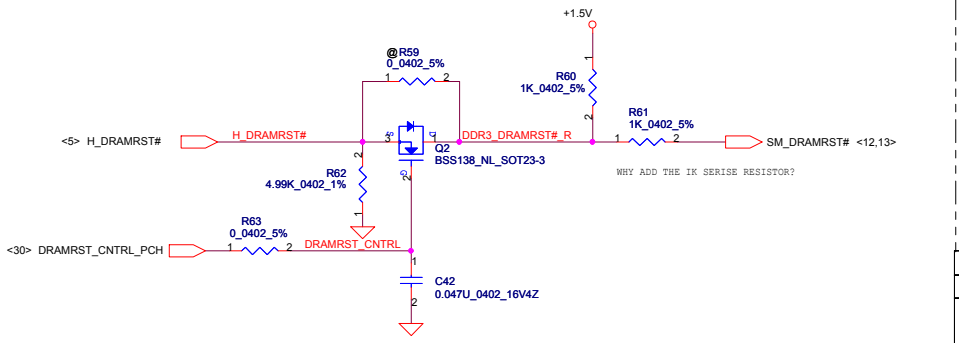
Compal Electronics, Inc.

Title: Sandy Bridge(2/6)-DMI/FDI/PEG/eDP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 6 of 59





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Title: Sandy Bridge(3/6)-DDR III

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 7 of 59

Group1

POWER

+CPU_CORE

JCPUF

94A

18A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

AG35	VCC1	VCCIO1	AH13
AG34	VCC2	VCCIO2	AH10
AG33	VCC3	VCCIO3	AG10
AG32	VCC4	VCCIO4	AC10
AG31	VCC5	VCCIO5	Y10
AG30	VCC6	VCCIO6	U10
AG29	VCC7	VCCIO7	P10
AG28	VCC8	VCCIO8	L10
AG27	VCC9	VCCIO9	J14
AG26	VCC10	VCCIO10	J13
AF35	VCC11	VCCIO11	J12
AF34	VCC12	VCCIO12	J11
AF33	VCC13	VCCIO13	H14
AF32	VCC14	VCCIO14	H12
AF31	VCC15	VCCIO15	H11
AF30	VCC16	VCCIO16	G14
AF29	VCC17	VCCIO17	G13
AF28	VCC18	VCCIO18	G12
AF27	VCC19	VCCIO19	F14
AF26	VCC20	VCCIO20	F13
AD35	VCC21	VCCIO21	F12
AD34	VCC22	VCCIO22	F11
AD33	VCC23	VCCIO23	E14
AD32	VCC24	VCCIO24	E12
AD31	VCC25	VCCIO25	E11
AD30	VCC26	VCCIO26	D14
AD29	VCC27	VCCIO27	D13
AD28	VCC28	VCCIO28	D12
AD27	VCC29	VCCIO29	D11
AD26	VCC30	VCCIO30	C14
AC35	VCC31	VCCIO31	C13
AC34	VCC32	VCCIO32	C12
AC33	VCC33	VCCIO33	C11
AC32	VCC34	VCCIO34	B14
AC31	VCC35	VCCIO35	B12
AC30	VCC36	VCCIO36	A14
AC29	VCC37	VCCIO37	A13
AC28	VCC38	VCCIO38	A12
AC27	VCC39	VCCIO39	A11
AC26	VCC40	VCCIO40	J23
AA35	VCC41		
AA34	VCC42		
AA33	VCC43		
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
V28	VCC68		
V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

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Material Note (+1.05VS_VCCP)

2 x 330 µF
(3x 330 µF for 2012 capable designs)
Top Socket Cavity 22U 0805 *7
Bottom Socket Cavity 22U 0805 *5

+1.05VS_VCCP

C43 22U_0805_6.3V6M
C44 22U_0805_6.3V6M
C45 22U_0805_6.3V6M
C46 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C48 22U_0805_6.3V6M
C49 22U_0805_6.3V6M
C50 22U_0805_6.3V6M
C51 22U_0805_6.3V6M
C52 22U_0805_6.3V6M
C53 22U_0805_6.3V6M
C54 22U_0805_6.3V6M
C62 330U_D2_2V_Y
C63 330U_D2_2V_Y
@C64 330U_D2_2V_Y

Cap quantity follow 439028_HR_PDDG_R1_51

+1.05VS_VCCP

C83 @ 330U_2.5V_M_R17
C73 @ 330U_2.5V_M_R17

reserve for test
please co-layout with C62,C63

+1.05VS_VCCP +1.05VS_VCCP

R65 130_0402_5%
R66 75_0402_5%
R67 43_0402_1%

AJ29	H_CPU_SVIDALRT#			VR_SVID_ALRT# <55>
AJ30	H_CPU_SVIDCLK	R68	0_0402_5%	VR_SVID_CLK <55>
AJ28	H_CPU_SVIDDAT	R69	0_0402_5%	VR_SVID_DAT <55>

VIDALERT#
VIDSCLK
VIDSOUT

Resistors close to CPU

Close to CPU

+CPU_CORE

VCCSENSE R70 100_0402_1%
VSSSENSE R71 100_0402_1%

AJ35	VCCSENSE_R	R72	VCCSENSE	VCCSENSE <55>
AJ34	VSSSENSE_R	R73	VSSSENSE	VSSSENSE <55>

0_0402_5%

VCC_SENSE
VSS_SENSE

B10 VCCIO_SENSE <52> R74 10_0402_5%

A10

VCCIO_SENSE
VSSIO_SENSE

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Title: Sandy Bridge(4/6)-PWR

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 8 of 59

POWER Group2

Material Note (GFXCORE)
2 x 330 µF on Bottom socket edge
Bottom Socket Cavity 22U 0805 *2
Bottom Socket Edge 22U 0805 *4
Top Socket Cavity 22U 0805 *2
Top Socket Edge 22U 0805 *4

+GFX_CORE
C217 330U_D2_2V_Y
C225 330U_D2_2V_Y
22U_0805_6.3V6M: C284 C285 C286 C414 C415 C416
22U_0805_6.3V6M: C364 C365 C410 C412 C411 C413

JCPUG
26A
AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES
VAXG_SENSE AK35
VSSAXG_SENSE AK34
R131 100_0402_1% +GFX_CORE
VCC_AXG_SENSE <55>
VSS_AXG_SENSE <55>
R129 100_0402_1%

VREF
SM_VREF AL1
+V_SM_VREF_CNT
R76 0_0402_5%
+1.5V_CPU
R75 1K_0402_1%
R77 1K_0402_1%
+V_SM_VREF
@ Q3 AP2302GN-HF_SOT23-3
RUN_ON_CPU1.5VS3
C65 0.1U_0402_16V4Z

Follow DG V1.5 P.109
+V_SM_VREF should have 20 mil trace width

DDR3 -1.5V RAILS
5A
VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AE1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1
+1.5V_CPU
@ JP1 JUMPER_43X118
+1.5V
10U_0603_6.3V6M: C66 C67 C68 C69 C70 C71
330U_D2_2V_Y C72

Material Note (VDDQ)
Bottom Socket Edge
1 x 330 µF
10U 0805 *6

SA RAIL
6A
VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25
+VCCSA
10U_0805_6.3V6M: C74 C75 C76
R78 0_0402_5%
VCCSA_SENSE
330U_D2_2V_Y C78

Material Note (VCCSA)
1 x 330 µF
Bottom Socket Cavity 10U 0805 *2
Bottom Socket Edge 10U 0805 *1

MISC
VCCSA_SENSE H23
VCCSA_SENSE <54>
FC_C22 C22
VCCSA_VID1 C24
H_FC_C22
VCCSA_SEL <54>
R79 10K_0402_5%
@R80 0_0402_5%

1.8V RAIL
+1.8VS
R124 0_0805_5%
C79 330U_D2_2V_Y @
C80 10U_0603_6.3V6M
C81 1U_0402_6.3V6K
C82 1U_0402_6.3V6K
+1.8VS_VCCPLL
VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

Material Note (+1.8VS_VCCPLL)
1 x 330 µF
Bottom Socket Edge
1U 0402 *1
10U 0805 *1

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CONN@

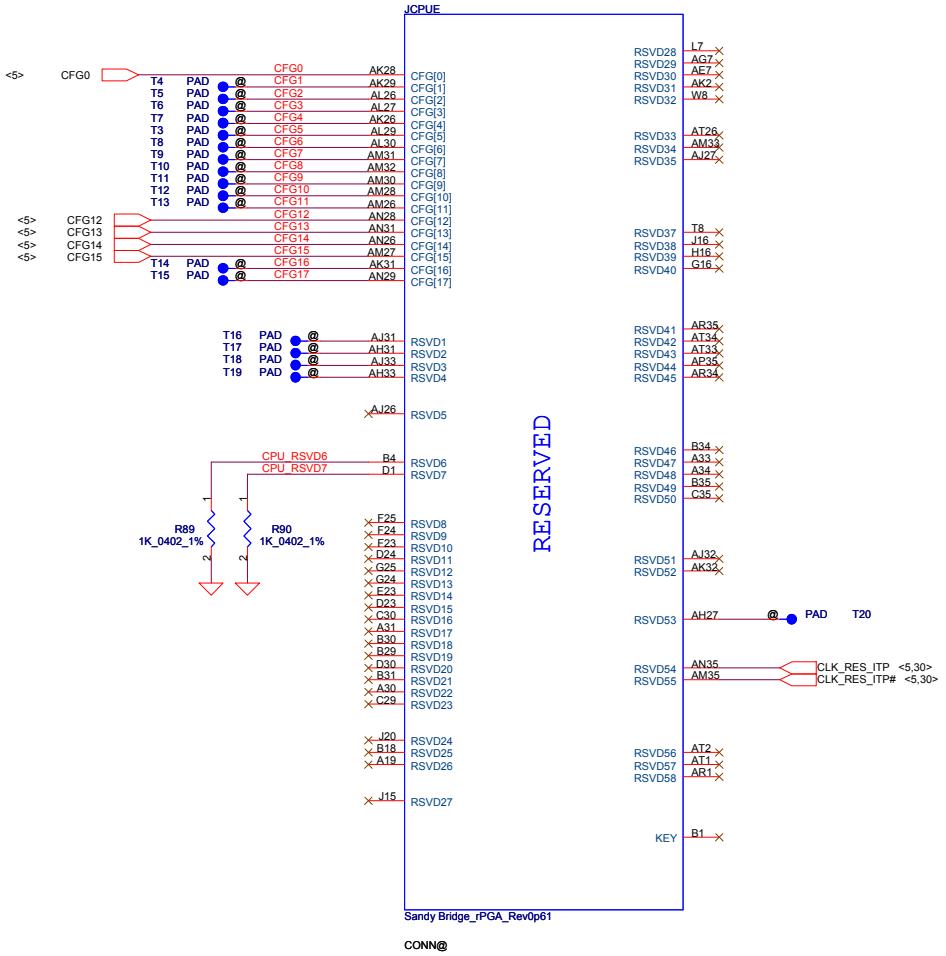
+1.5V_CPU Source

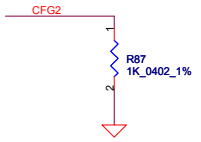
+1.5V Q4 SI4634DY-T1-GE3_SO8 +1.5V_CPU
+VSB
+3VALW
R81 100K_0402_5%
R82 470_0603_5%
R83 100K_0402_5%
RUN_ON_CPU1.5VS3
RUN_ON_CPU1.5VS3#
R84 0_0402_5%
<43> CPU1.5V_S3_GATE
@R86 0_0402_5%
<43,46,50,52,54,57,58> SUSP#
Q35A 2N7002DW-T/R7_SOT363-6
Q35B 2N7002DW-T/R7_SOT363-6
R85 330K_0402_5%
C86 0.1U_0402_16V4Z
Q6 2N7002H 1N SOT23-3

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

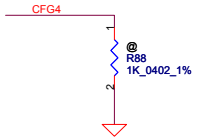
Compal Electronics, Inc.
Title: Sandy Bridge(4/6)-PWR
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3
Date: Monday, April 11, 2011 | Sheet 9 of 59

CFG Straps for Processor

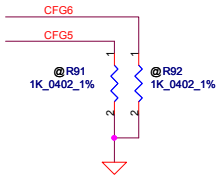




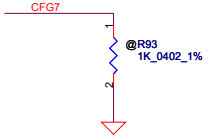
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

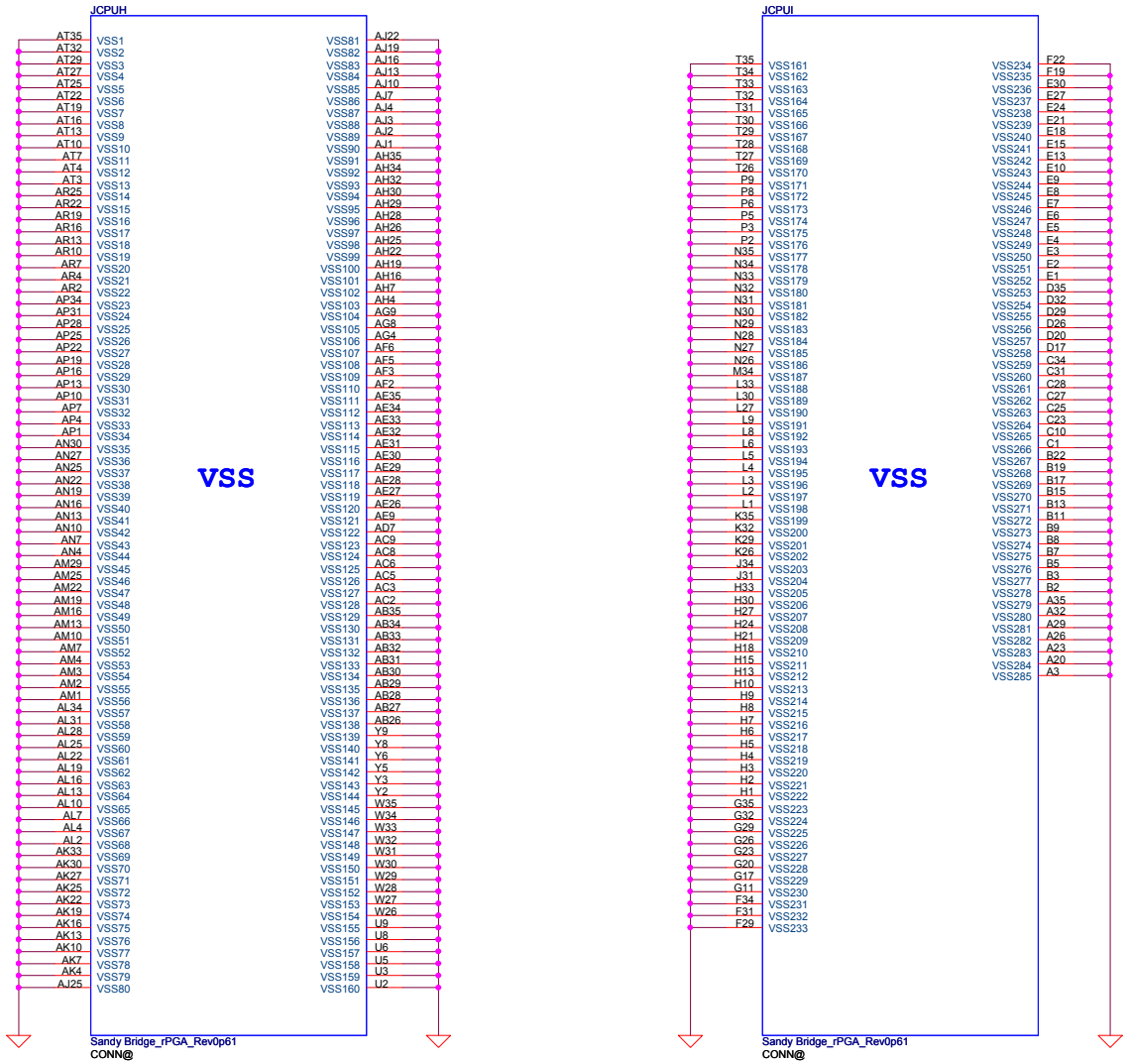
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(5/6) Reserve

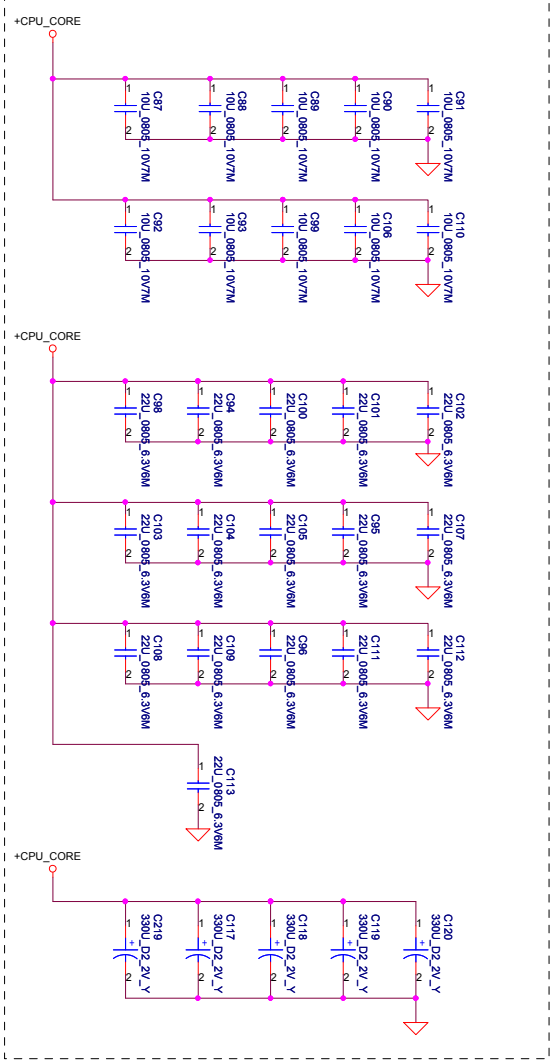
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 10 of 59



Material Note (+CPU_CORE)

4 x 330 µF
Top Socket Cavity 22U 0805 *8
Top Socket Edge 22U 0805 *8
Bottom Socket Cavity 10U 0805 *10



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(6/6)-GND

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 11 of 59

Support SO DIMM X 4
Support 1066/1333MHz

3A@1.5V

JDDR1

TYCO_2-2013289-1

@

Standard:5.2mm
<Address: SA1:SA0=00>
BOT

JDDR2

TYCO_2-2013287-1

@

Reverse:4mm
<Address: SA1:SA0=01>
TOP

Layout Note:
Place near JDIMMA1.203,204

Layout Note:
Place near JDIMMA2.203,204

Layout Note:
Place near JDIMM

Layout Note: Place these 4 Caps near Command and Control signals of JDIMMA

For EMI

0.65A@.75V

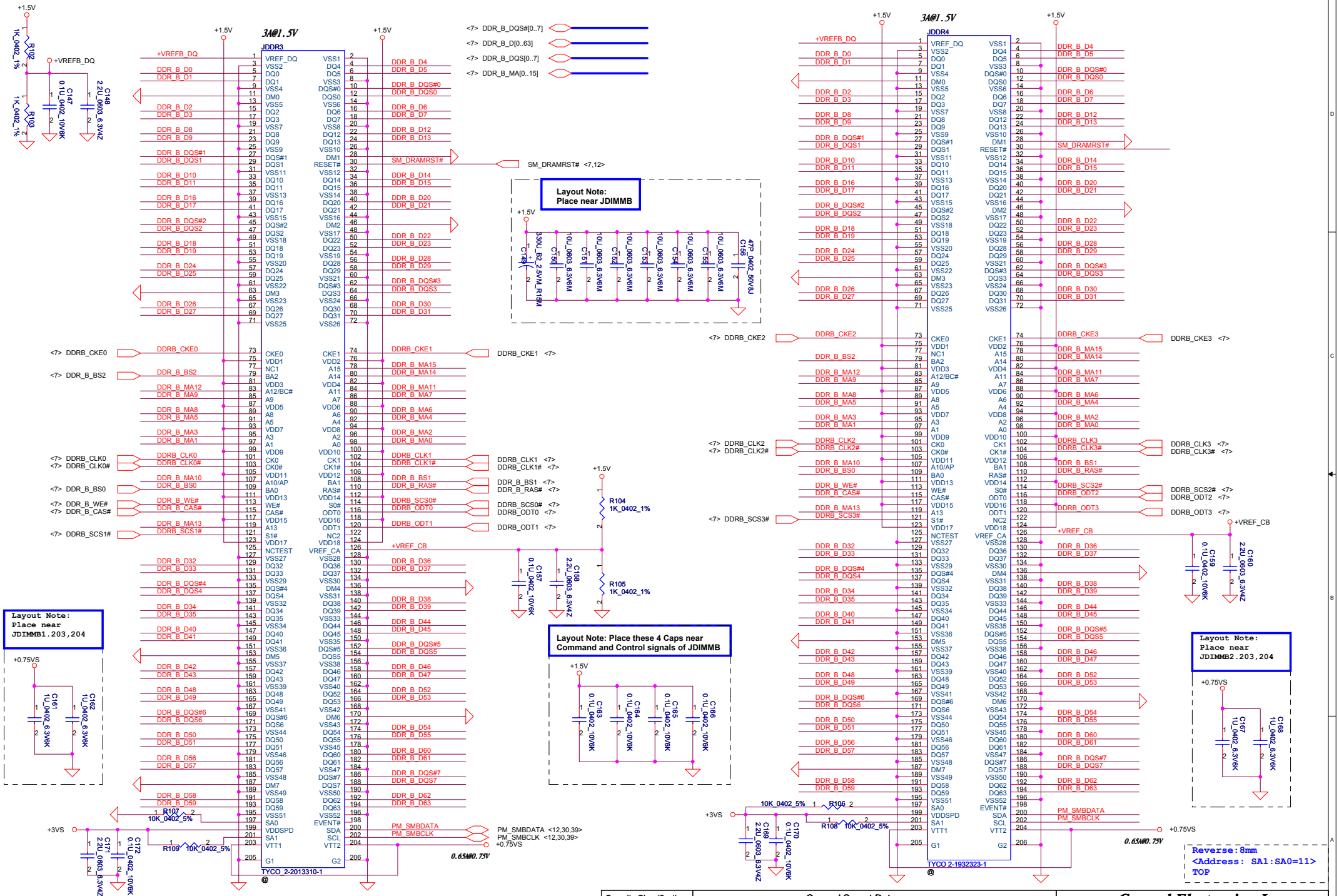
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: DDRIII-DIMMA

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 12 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: DDRIII-DIMMB

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 13 of 59

N12PGS@
UV1
N12P-GS-A1_BGA_973P

UV1A
Part 1 of 7

PCIE_CTX_C_GRX_P0 AP17 PEX_RX0
PCIE_CTX_C_GRX_N0 AN17 PEX_RX0_N
PCIE_CTX_C_GRX_P1 AN19 PEX_RX1
PCIE_CTX_C_GRX_N1 AP19 PEX_RX1_N
PCIE_CTX_C_GRX_P2 AR19 PEX_RX2
PCIE_CTX_C_GRX_N2 AR20 PEX_RX2_N
PCIE_CTX_C_GRX_P3 AP20 PEX_RX3
PCIE_CTX_C_GRX_N3 AN20 PEX_RX3_N
PCIE_CTX_C_GRX_P4 AN22 PEX_RX4
PCIE_CTX_C_GRX_N4 AP22 PEX_RX4_N
PCIE_CTX_C_GRX_P5 AR22 PEX_RX5
PCIE_CTX_C_GRX_N5 AR23 PEX_RX5_N
PCIE_CTX_C_GRX_P6 AP23 PEX_RX6
PCIE_CTX_C_GRX_N6 AN23 PEX_RX6_N
PCIE_CTX_C_GRX_P7 AN25 PEX_RX7
PCIE_CTX_C_GRX_N7 AP25 PEX_RX7_N
PCIE_CTX_C_GRX_P8 AR25 PEX_RX8
PCIE_CTX_C_GRX_N8 AR26 PEX_RX8_N
PCIE_CTX_C_GRX_P9 AP26 PEX_RX9
PCIE_CTX_C_GRX_N9 AN26 PEX_RX9_N
PCIE_CTX_C_GRX_P10 AN28 PEX_RX10
PCIE_CTX_C_GRX_N10 AP28 PEX_RX10_N
PCIE_CTX_C_GRX_P11 AR28 PEX_RX11
PCIE_CTX_C_GRX_N11 AR29 PEX_RX11_N
PCIE_CTX_C_GRX_P12 AP29 PEX_RX12
PCIE_CTX_C_GRX_N12 AN29 PEX_RX12_N
PCIE_CTX_C_GRX_P13 AN31 PEX_RX13
PCIE_CTX_C_GRX_N13 AP31 PEX_RX13_N
PCIE_CTX_C_GRX_P14 AR31 PEX_RX14
PCIE_CTX_C_GRX_N14 AR32 PEX_RX14_N
PCIE_CTX_C_GRX_P15 AR34 PEX_RX15
PCIE_CTX_C_GRX_N15 AP34 PEX_RX15_N

PCI EXPRESS

PEX_TX0 AL17 PCIE_GTX_C_CRX_P0
PEX_TX0_N AM17 PCIE_GTX_C_CRX_N0
PEX_TX1 AM18 PCIE_GTX_C_CRX_P1
PEX_TX1_N AM19 PCIE_GTX_C_CRX_N1
PEX_TX2 AL19 PCIE_GTX_C_CRX_P2
PEX_TX2_N AK19 PCIE_GTX_C_CRX_N2
PEX_TX3 AL20 PCIE_GTX_C_CRX_P3
PEX_TX3_N AM20 PCIE_GTX_C_CRX_N3
PEX_TX4 AM21 PCIE_GTX_C_CRX_P4
PEX_TX4_N AM22 PCIE_GTX_C_CRX_N4
PEX_TX5 AL22 PCIE_GTX_C_CRX_P5
PEX_TX5_N AK22 PCIE_GTX_C_CRX_N5
PEX_TX6 AL23 PCIE_GTX_C_CRX_P6
PEX_TX6_N AM23 PCIE_GTX_C_CRX_N6
PEX_TX7 AM24 PCIE_GTX_C_CRX_P7
PEX_TX7_N AM25 PCIE_GTX_C_CRX_N7
PEX_TX8 AL25 PCIE_GTX_C_CRX_P8
PEX_TX8_N AK25 PCIE_GTX_C_CRX_N8
PEX_TX9 AL26 PCIE_GTX_C_CRX_P9
PEX_TX9_N AM26 PCIE_GTX_C_CRX_N9
PEX_TX10 AM27 PCIE_GTX_C_CRX_P10
PEX_TX10_N AM28 PCIE_GTX_C_CRX_N10
PEX_TX11 AL28 PCIE_GTX_C_CRX_P11
PEX_TX11_N AK28 PCIE_GTX_C_CRX_N11
PEX_TX12 AK29 PCIE_GTX_C_CRX_P12
PEX_TX12_N AL29 PCIE_GTX_C_CRX_N12
PEX_TX13 AM29 PCIE_GTX_C_CRX_P13
PEX_TX13_N AM30 PCIE_GTX_C_CRX_N13
PEX_TX14 AM31 PCIE_GTX_C_CRX_P14
PEX_TX14_N AM32 PCIE_GTX_C_CRX_N14
PEX_TX15 AN32 PCIE_GTX_C_CRX_P15
PEX_TX15_N AP32 PCIE_GTX_C_CRX_N15

PEX_REFCLK AR16 CLK_PCIE_VGA
PEX_REFCLK_N AR17 CLK_PCIE_VGA#
PEX_CLKREQ_N AR13 CLK_REQ_GPU#
PEX_TSTCLK_OUT AJ17 PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N AJ18 PEX_TSTCLK_OUT#
PEX_RST_N AM16 PLTRST_VGA_R#
PEX_TERMP AG21

GPIO

GPIO0 K1 VGA_GPIO1
GPIO1 K2
GPIO2 K3
GPIO3 H3
GPIO4 H2
GPIO5 H1 GPU_VID0
GPIO6 H4 GPU_VID1
GPIO7 H5
GPIO8 H6 GPIO8
GPIO9 J7 THERM#_VGA
GPIO10 K4
GPIO11 K5
GPIO12 H7 GPIO12
GPIO13 J4
GPIO14 J6
GPIO15 L1 VGA_HDMI_HPD
GPIO16 L2
GPIO17 L4
GPIO18 M4
GPIO19 L7
GPIO20 L5
GPIO21 K6
GPIO22 L6
GPIO23 M6
GPIO24 M7

DVO

MIOA_D0_NC N1
MIOA_D1_NC P4
MIOA_D2_NC P1
MIOA_D3_NC P2
MIOA_D4_NC P3
MIOA_D5_NC T3
MIOA_D6_NC T2
MIOA_D7_NC T1
MIOA_D8_NC U4
MIOA_D9_NC U1
MIOA_D10_NC U2
MIOA_D11_NC U3
MIOA_D12_NC R6
MIOA_D13_NC T6
MIOA_D14_NC N6

MIOB_D0_NC Y1
MIOB_D1_NC Y2
MIOB_D2_NC Y3
MIOB_D3_NC AB2
MIOB_D4_NC AB1
MIOB_D5_NC AC4
MIOB_D6_NC AC1
MIOB_D7_NC AC2
MIOB_D8_NC AC3
MIOB_D9_NC AE3
MIOBD_10_NC AE2
MIOB_D11_NC U6
MIOB_D12_NC W6
MIOB_D13_NC Y6
MIOB_D14_NC

MIOA_HSYNC_NC N3
MIOA_VSYNC_NC L3
MIOB_HSYNC_NC W1
MIOB_VSYNC_NC W2
MIOA_DE_NC N2
MIOA_CTL3_NC P5
MIOA_VREF_NC N5
MIOB_DE_NC Y5
MIOB_CTL3_NC W3
MIOB_VREF_NC AF1
MIOA_CLKIN_NC N4
MIOA_CLKOUT_NC R4
MIOB_CLKIN_NC AE1
MIOB_CLKOUT_NC V4
MIOA_CLKOUT_NC_N T4
MIOB_CLKOUT_NC_N W4
MIOACAL_PD_VDDQ_NC U5
MIOACAL_PU_GND_NC T5
MIOBCAL_PD_VDDQ_NC AA7
MIOBCAL_PU_GND_NC AA6

CLK

PLLVDD AE9
SP_PLLVDD AF9
VID_PLLVDD AD9
XTAL_IN B1 XTALIN
XTAL_OUT B2 XTAL_OUT
XTAL_OUTBUFF D1 XTALOUT
XTAL_SSIN D2 XTALSSIN

I2C DACs

DACA_RED AM15
DACA_GREEN AM14
DACA_BLUE AL14
DACA_HSYNC AM13
DACA_VSYNC AL13
DACA_VDD AJ12
DACA_VREF AK12
DACA_RSET AK13
DACB_RED AK4
DACB_GREEN AL4
DACB_BLUE AJ4
DACB_HSYNC AM1
DACB_VSYNC AM2
DACB_VDD AG7
DACB_VREF AK6
DACB_RSET AH7

I2CS_SCL E2 SMB_CLK_GPU
I2CS_SDA E1 SMB_DATA_GPU
I2CC_SCL E3 VGA_EDID_CLK
I2CC_SDA E4 VGA_EDID_DATA
I2CB_SCL G3 I2CB_SCL
I2CB_SDA G2 I2CB_SDA
I2CA_SCL G1 I2CA_SCL
I2CA_SDA G4 I2CA_SDA
I2CH_SCL F6 HDCP_SCL
I2CH_SDA G6 HDCP_SDA

N12P-GV-A1_BGA_973P
N12PGV@

<6> PCIE_GTX_C_CRX_P[0..15] PCIE_GTX_C_CRX_P[0..15]
<6> PCIE_GTX_C_CRX_N[0..15] PCIE_GTX_C_CRX_N[0..15]
<6> PCIE_CTX_C_GRX_P[0..15] PCIE_CTX_C_GRX_P[0..15]
<6> PCIE_CTX_C_GRX_N[0..15] PCIE_CTX_C_GRX_N[0..15]

GPU_VID0 <57>
GPU_VID1 <57>
THERM#_VGA <15>
TV1 @

Under GPU(below 150mils) Near GPU
150mA
BLM18PG330SN1D_0603
+1.05VS_DGPU 1 LV1 2 0.1U_0402_16V4Z 0.1U_0402_16V4Z 10U_0603_6.3V6M +PLLVDD
CV1 CV2 CV3 CV4 CV5
0.1U_0402_16V4Z 0.1U_0402_16V4Z

PCIE_GTX_C_CRX_P0 CV6 0.22U_0402_10V6K PCIE_GTX_CRX_P0
PCIE_GTX_C_CRX_N0 CV7 0.22U_0402_10V6K PCIE_GTX_CRX_N0
PCIE_GTX_C_CRX_P1 CV8 0.22U_0402_10V6K PCIE_GTX_CRX_P1
PCIE_GTX_C_CRX_N1 CV9 0.22U_0402_10V6K PCIE_GTX_CRX_N1
PCIE_GTX_C_CRX_P2 CV10 0.22U_0402_10V6K PCIE_GTX_CRX_P2
PCIE_GTX_C_CRX_N2 CV11 0.22U_0402_10V6K PCIE_GTX_CRX_N2
PCIE_GTX_C_CRX_P3 CV12 0.22U_0402_10V6K PCIE_GTX_CRX_P3
PCIE_GTX_C_CRX_N3 CV13 0.22U_0402_10V6K PCIE_GTX_CRX_N3
PCIE_GTX_C_CRX_P4 CV14 0.22U_0402_10V6K PCIE_GTX_CRX_P4
PCIE_GTX_C_CRX_N4 CV15 0.22U_0402_10V6K PCIE_GTX_CRX_N4
PCIE_GTX_C_CRX_P5 CV16 0.22U_0402_10V6K PCIE_GTX_CRX_P5
PCIE_GTX_C_CRX_N5 CV17 0.22U_0402_10V6K PCIE_GTX_CRX_N5
PCIE_GTX_C_CRX_P6 CV18 0.22U_0402_10V6K PCIE_GTX_CRX_P6
PCIE_GTX_C_CRX_N6 CV19 0.22U_0402_10V6K PCIE_GTX_CRX_N6
PCIE_GTX_C_CRX_P7 CV20 0.22U_0402_10V6K PCIE_GTX_CRX_P7
PCIE_GTX_C_CRX_N7 CV21 0.22U_0402_10V6K PCIE_GTX_CRX_N7
PCIE_GTX_C_CRX_P8 CV22 0.22U_0402_10V6K PCIE_GTX_CRX_P8
PCIE_GTX_C_CRX_N8 CV23 0.22U_0402_10V6K PCIE_GTX_CRX_N8
PCIE_GTX_C_CRX_P9 CV24 0.22U_0402_10V6K PCIE_GTX_CRX_P9
PCIE_GTX_C_CRX_N9 CV25 0.22U_0402_10V6K PCIE_GTX_CRX_N9
PCIE_GTX_C_CRX_P10 CV26 0.22U_0402_10V6K PCIE_GTX_CRX_P10
PCIE_GTX_C_CRX_N10 CV27 0.22U_0402_10V6K PCIE_GTX_CRX_N10
PCIE_GTX_C_CRX_P11 CV28 0.22U_0402_10V6K PCIE_GTX_CRX_P11
PCIE_GTX_C_CRX_N11 CV29 0.22U_0402_10V6K PCIE_GTX_CRX_N11
PCIE_GTX_C_CRX_P12 CV30 0.22U_0402_10V6K PCIE_GTX_CRX_P12
PCIE_GTX_C_CRX_N12 CV31 0.22U_0402_10V6K PCIE_GTX_CRX_N12
PCIE_GTX_C_CRX_P13 CV32 0.22U_0402_10V6K PCIE_GTX_CRX_P13
PCIE_GTX_C_CRX_N13 CV33 0.22U_0402_10V6K PCIE_GTX_CRX_N13
PCIE_GTX_C_CRX_P14 CV34 0.22U_0402_10V6K PCIE_GTX_CRX_P14
PCIE_GTX_C_CRX_N14 CV35 0.22U_0402_10V6K PCIE_GTX_CRX_N14
PCIE_GTX_C_CRX_P15 CV36 0.22U_0402_10V6K PCIE_GTX_CRX_P15
PCIE_GTX_C_CRX_N15 CV37 0.22U_0402_10V6K PCIE_GTX_CRX_N15

<30> CLK_PCIE_VGA
<30> CLK_PCIE_VGA#
RV19 stuff per NV request.
12/17
RV19 200_0402_1%

<33> PLTRST_VGA#
RV22 0_0402_5%
RV23 2.49K_0402_1%

+PLLVDD 60mA 45mA 45mA

RV24 10M_0402_5%
YV1
XTALIN XTAL_OUT
27MHZ_16PF_X5H027000FG1H
CV46 18P_0402_50V8J
CV47 18P_0402_50V8J

RV27 10K_0402_5%
RV26 10K_0402_5%

Internal Thermal Sensor
<15> SMB_CLK_GPU
<15> SMB_DATA_GPU

<17,33,57> DGPU_PWR_EN
RV124 10K_0402_5%
QV2 2N7002_SOT23-3
<30> CLK_REQ_VGA#
CLK_REQ_GPU#
RV115 0_0402_5%
2N7002_SOT23-3 QV4
+3VS_DGPU
RV118 10K_0402_5%
RV123 10K_0402_5%
RV128 10K_0402_5%

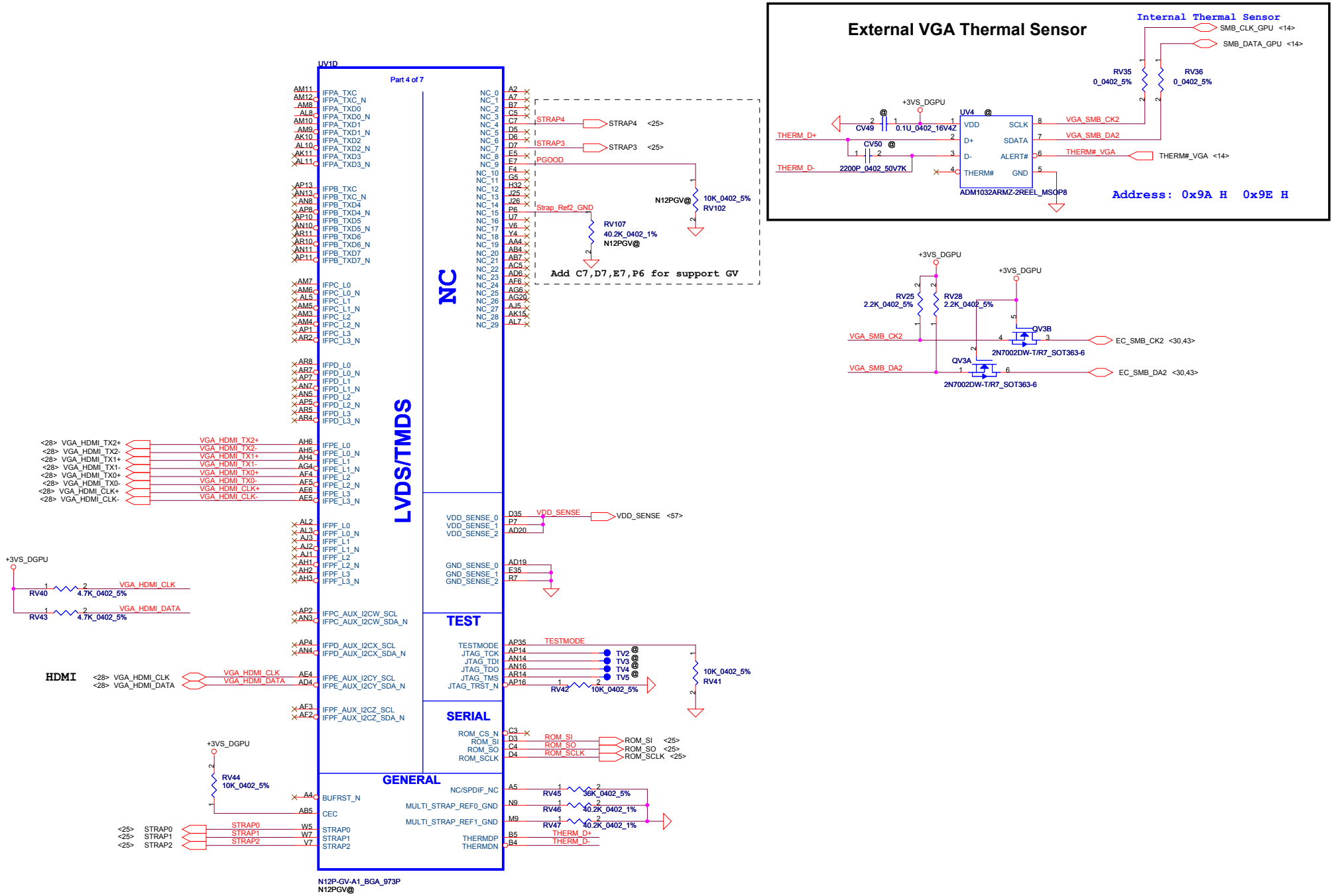
+3VS_DGPU
C880 0.1U_0402_16V4Z
RV32 10K_0402_5%
+DACB_VDD

<33,34,46,57> VGA_PWROK
<28> HDMI_HPD
R1430 0_0402_5%
U55 SN74AHC1G08DCKR_SC70-5
VGA_HDMI_HPD
C879 0.1U_0402_16V4Z
0_0402_5% @ R1431

+3VS_DGPU
GPIO8 RV1 10K_0402_5%
GPIO12 RV2 10K_0402_5%
VGA_EDID_CLK RV3 2.2K_0402_5%
VGA_EDID_DATA RV4 2.2K_0402_5%
SMB_CLK_GPU RV5 2.2K_0402_5%
SMB_DATA_GPU RV6 2.2K_0402_5%
THERM#_VGA RV7 100K_0402_5%
HDCP_SCL RV8 2.2K_0402_5%
HDCP_SDA RV9 2.2K_0402_5%
I2CA_SDA RV10 2.2K_0402_5%
I2CA_SCL RV11 2.2K_0402_5%
I2CB_SCL RV12 2.2K_0402_5%
I2CB_SDA RV13 2.2K_0402_5%
VGA_GPIO1 RV17 100K_0402_5%
VGA_HDMI_HPD RV20 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.
Title: VGA(1/12)-PCIE/DAC/GPIO
Size: Document Number: PBL80 LA-7441P M/B
Rev: 0.3
Date: Monday, April 11, 2011 Sheet 14 of 59

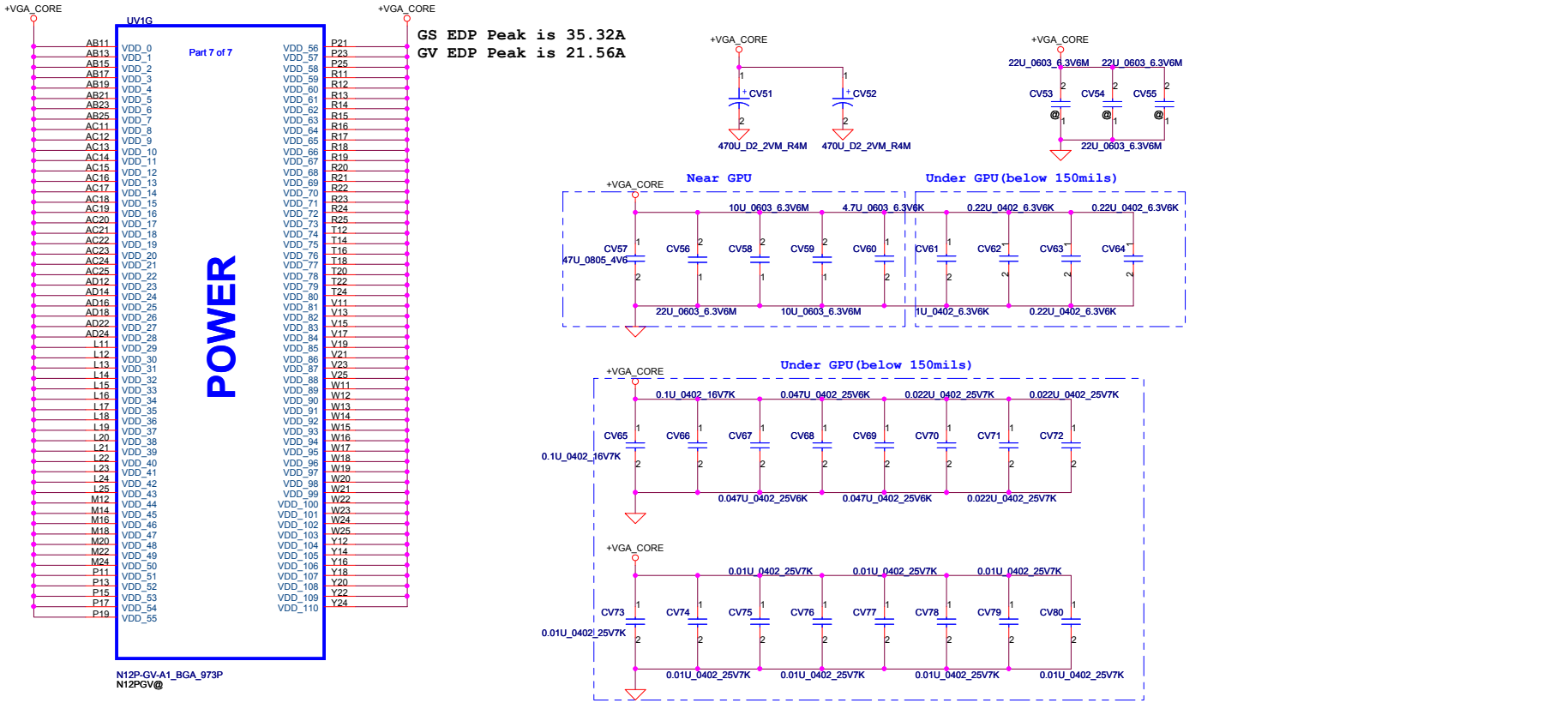


Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title	VGA(2/12)-LVDS/HDMI/DP/THM
Size	Document Number: PBL80 LA-7441P M/B
Rev	0.3
Date:	Monday, April 11, 2011
Sheet	15 of 59

Pstate	GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
P8-P12	0	0	0.825V	0.85V
P0(Hot)	1	0	0.975V	1V
	0	1		
P0(cold)	1	1	1V	1.025V



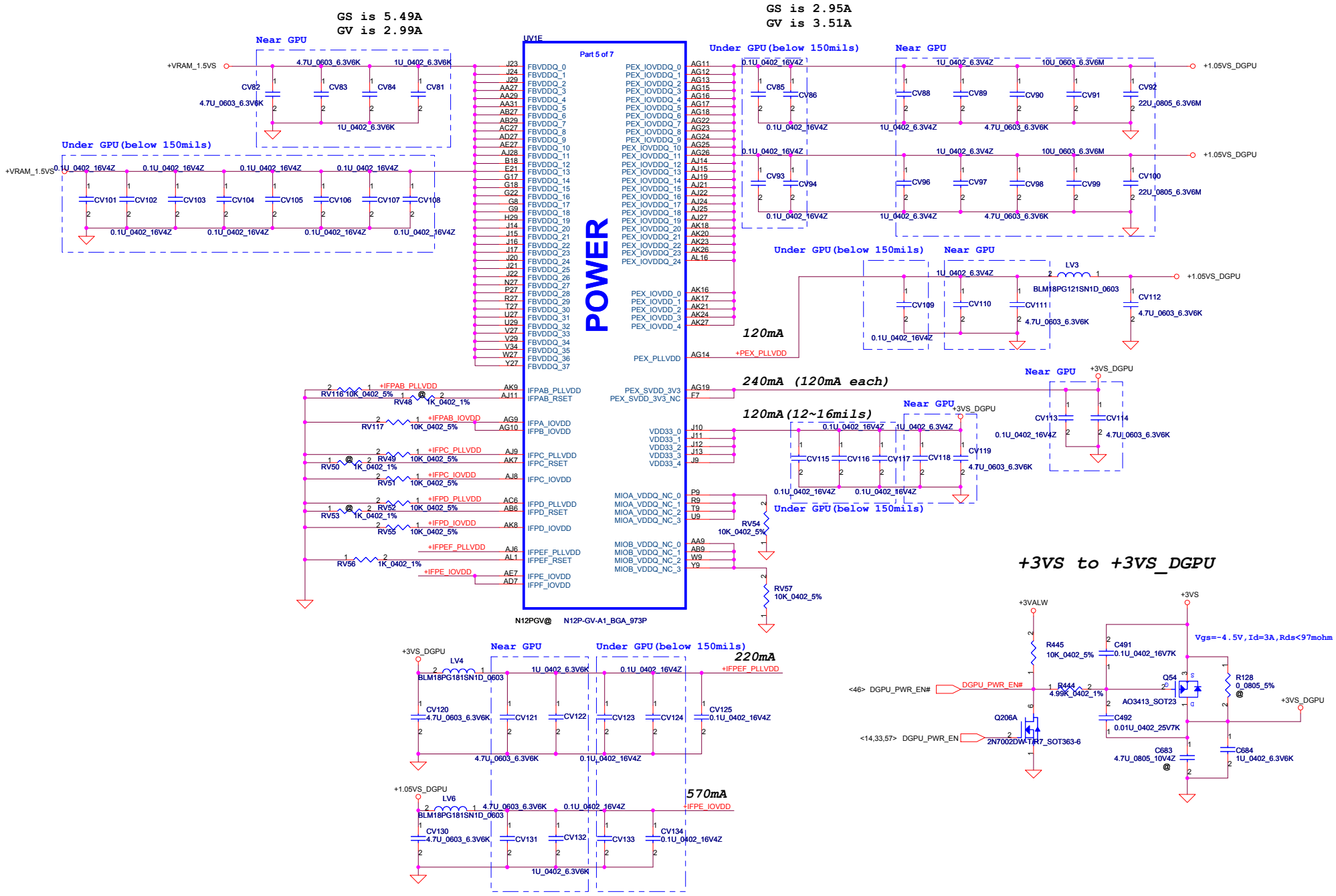
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

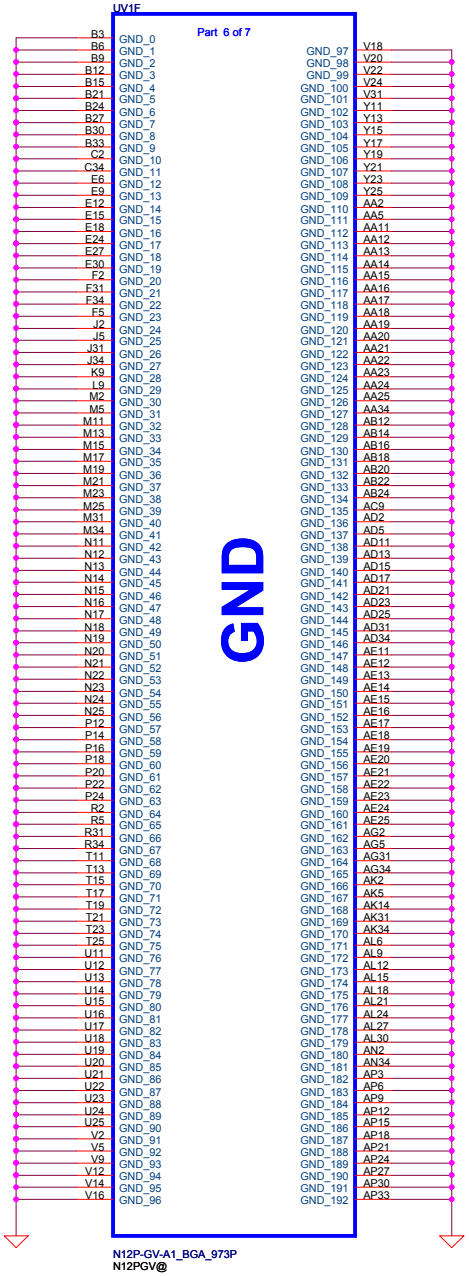
Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 16 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.	
Title	VGA(4/12)-POWER
Size	Document Number: PBL80 LA-7441P M/B
Rev	0.3
Date:	Monday, April 11, 2011
Sheet	17 of 59



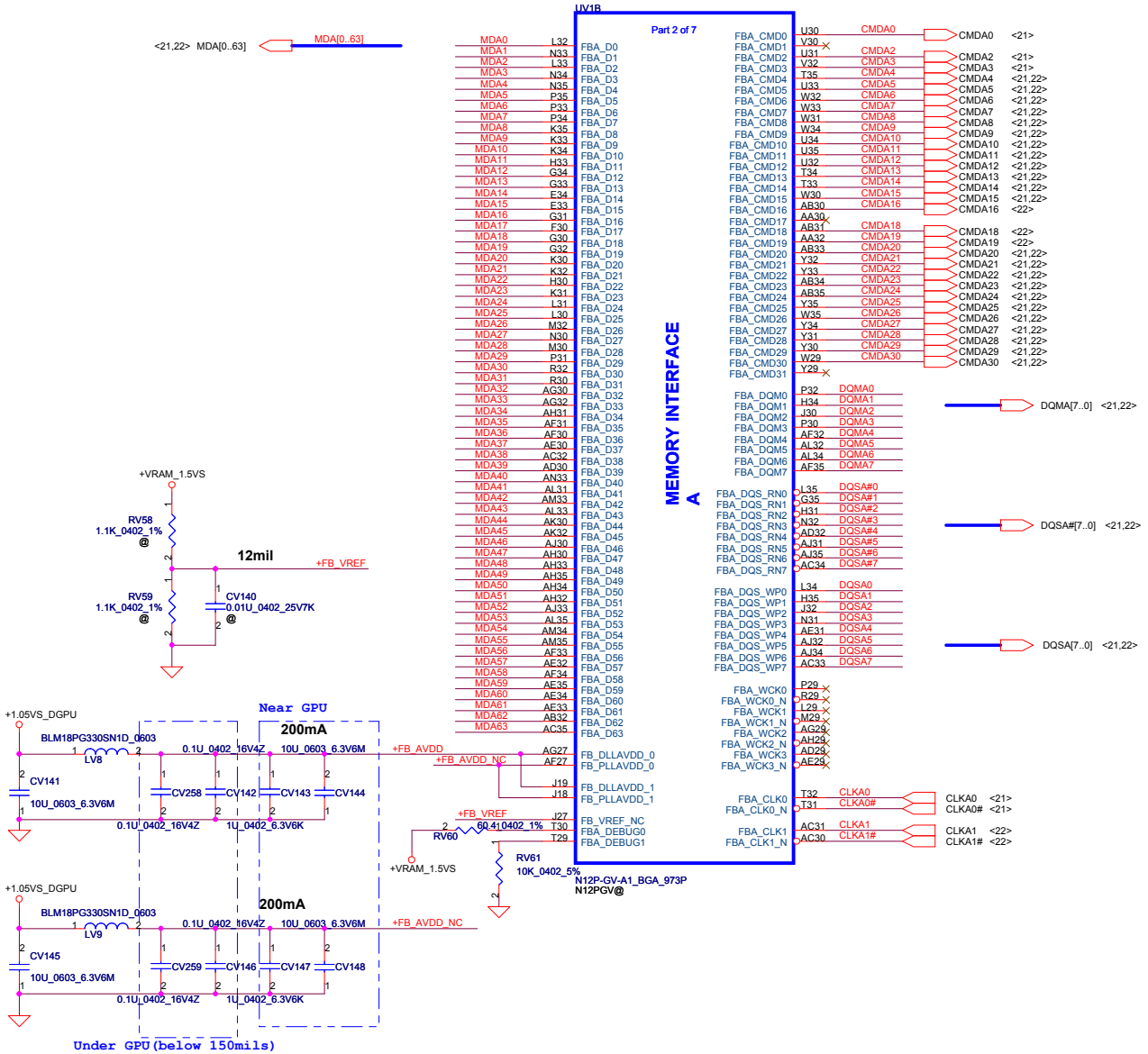
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 18 of 59



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

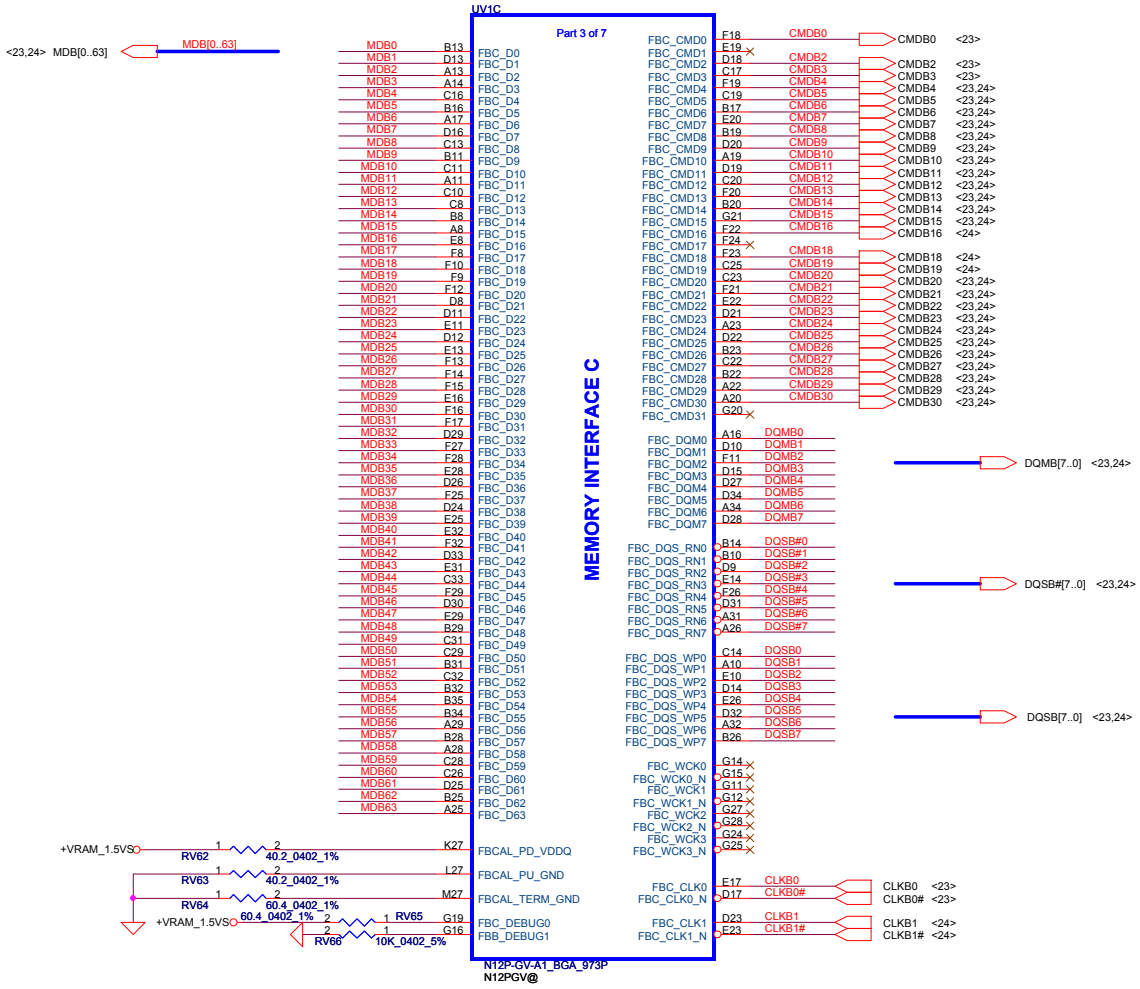
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 19 of 59



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

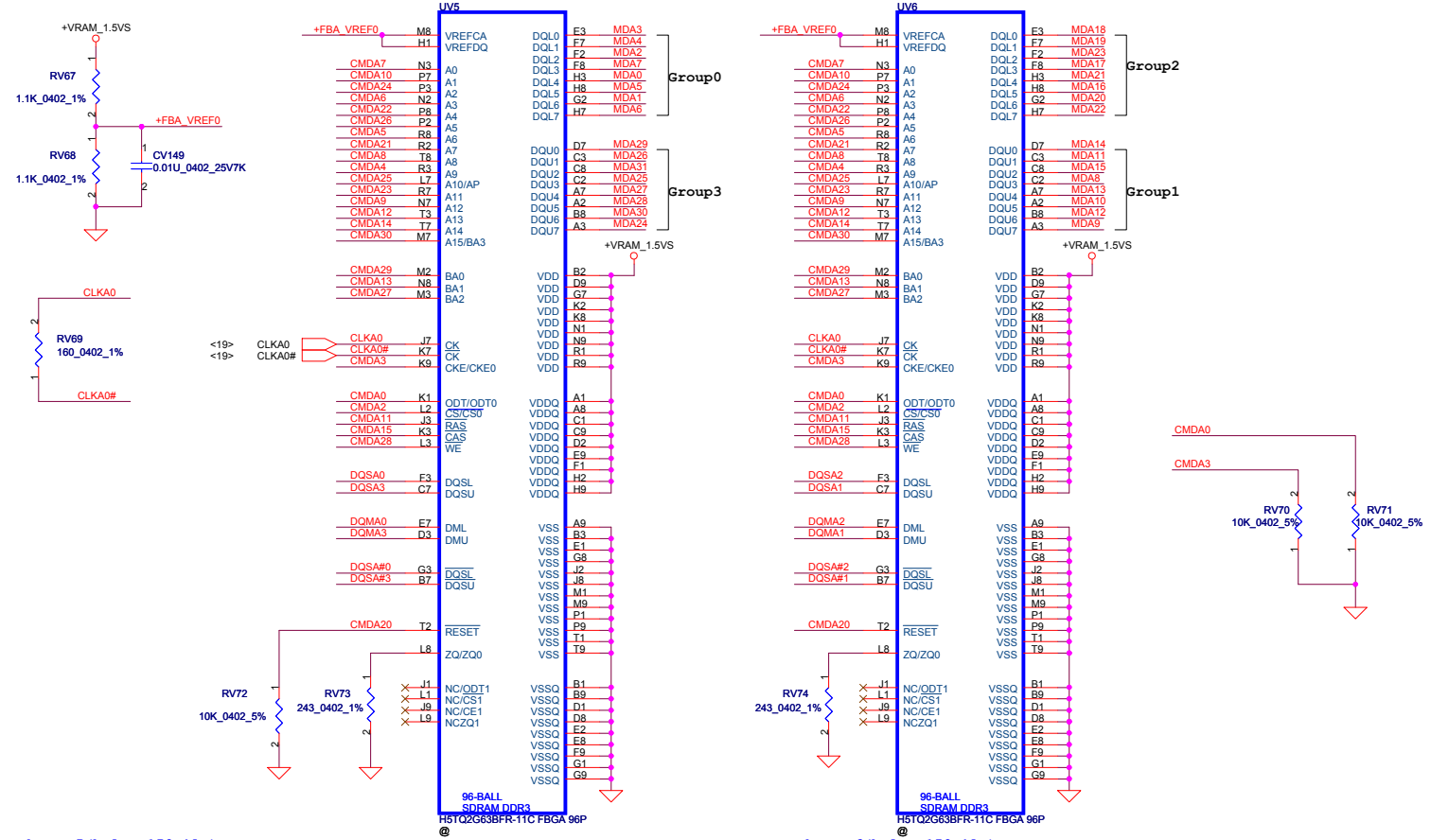
Title: VGA(7/12)-MEM Interface C

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 20 of 59

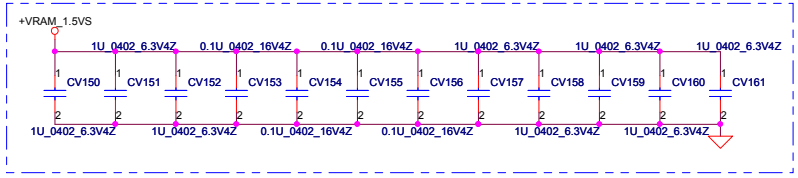
Memory Partition A - Lower 32 bits

Support N12P-GV/GS
Support Max VRAM 2G

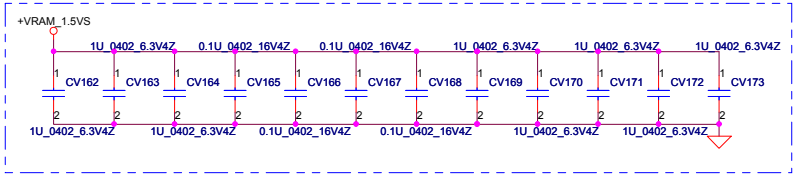


MDA[0..63] <19,22>
CMDA[30..0] <19,22>
DQMA[7..0] <19,22>
DQSA[7..0] <19,22>
DQSA#[7..0] <19,22>

Under UV5 (below 150mils)



Under UV6 (below 150mils)



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

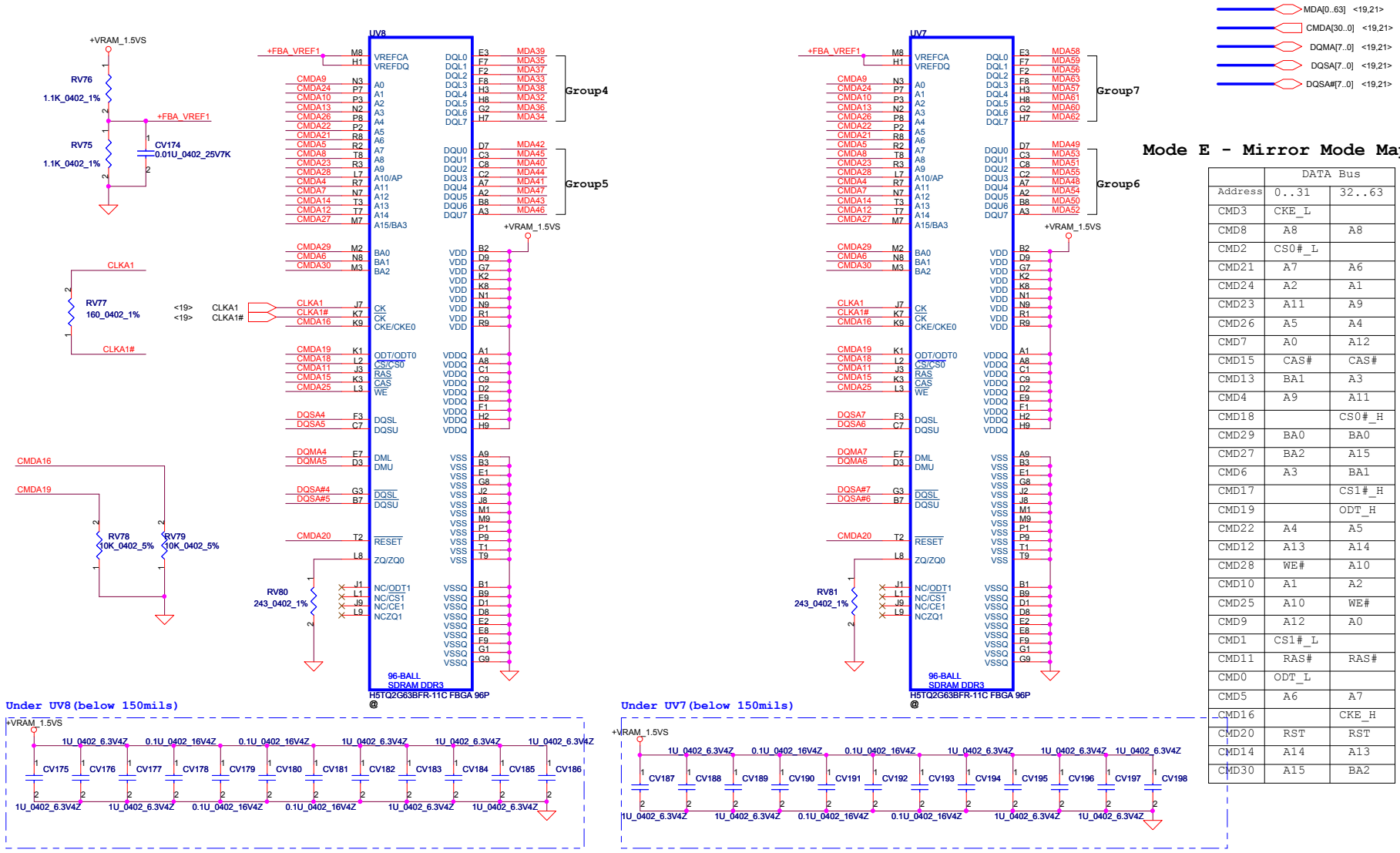
Compal Electronics, Inc.

Title: VGA(8/12)-VRAM A Lower

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 21 of 59

Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

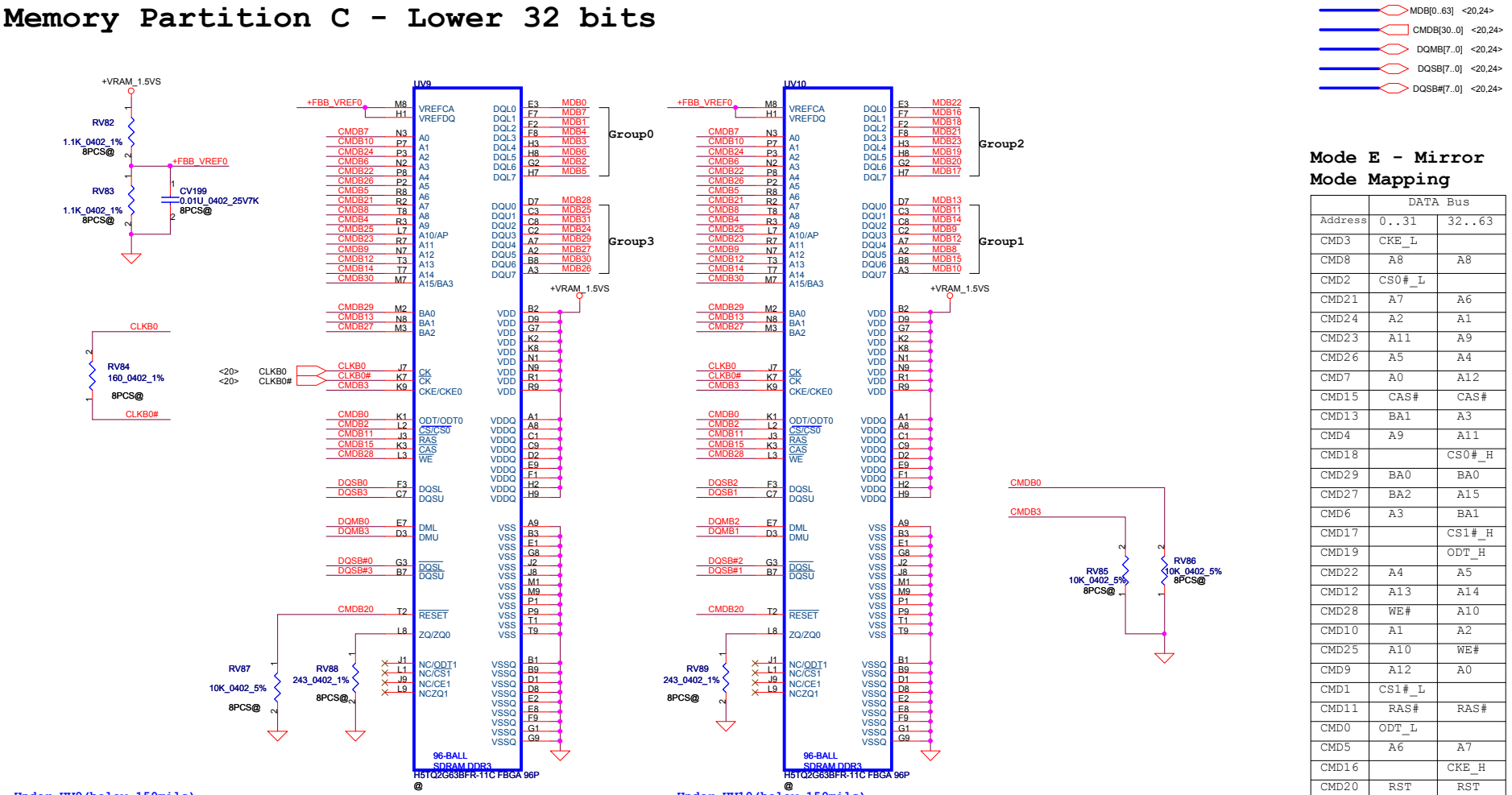
Compal Electronics, Inc.

Title: VGA(9/12)-VRAM A Upper

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 22 of 59

Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

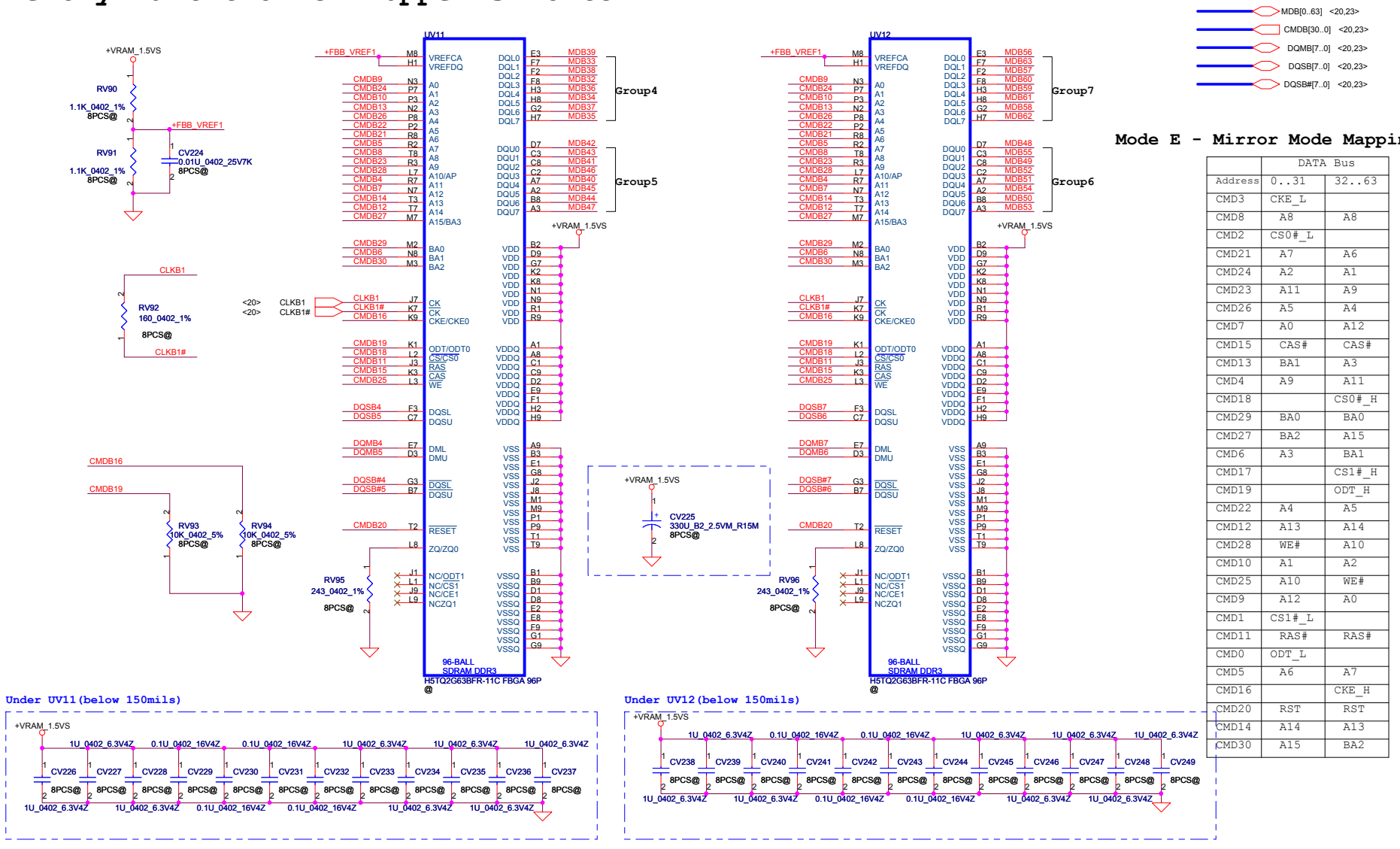
Compal Electronics, Inc.

Title: VGA(10/12)-VRAM C Lower

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 23 of 59

Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

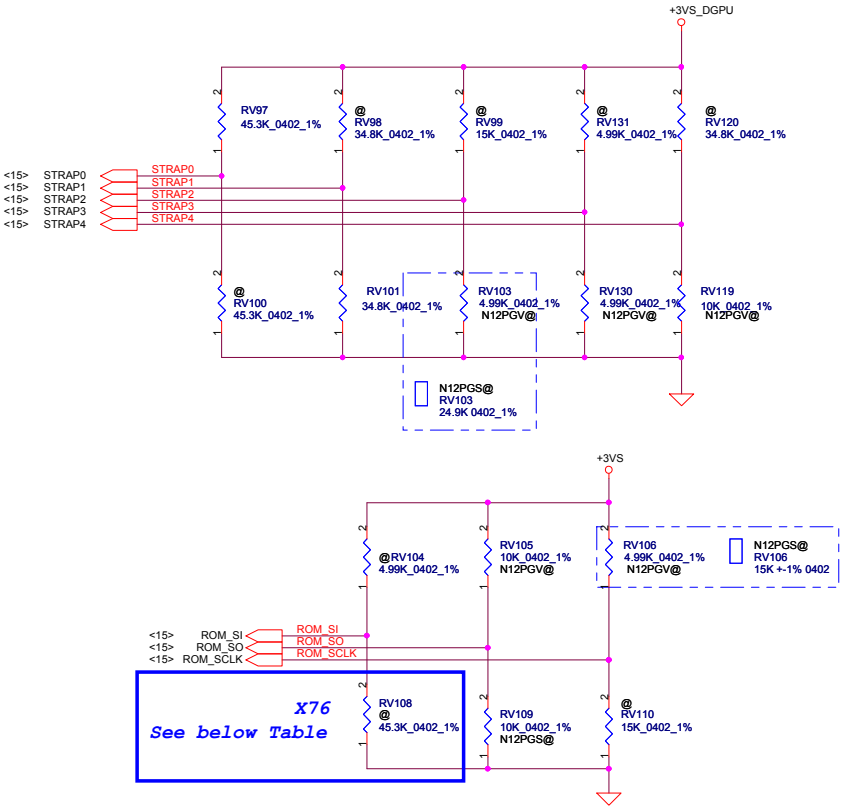
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(11/12)-VRAM C Upper

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 24 of 59



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SI	ROM_SCLK	ROM_SO	STRAP0
N12P-GS	0x0DF4	Below Table	Pull up 15K	Pull down 10K	Pull up 45K
N12P-GV	0x1050	Below Table	Pull up 5K	Pull up 10K	Pull up 45K

GPU	DeviceID	STRAP1	STRAP2	STRAP3	STRAP4
N12P-GS	0x0DF4	Pull down 35K	Pull down 25K		
N12P-GV	0x1050	Pull down 35K	Pull down 5K	Pull down 5K	Pull down 10K

GPU	DDR3 Type	VRAM		RAMCFG[3..0]		RV108
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C SA000041S20	512MB 1GB	0010	PD 15K	SD034154280 SD034154280
		Samsung K4W1G1646E-HC11 SA000041T00	512MB 1GB	0011	PD 20K	SD034200280 SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C SA00003YO00	1GB 2GB	0110	PD 34.8K	SD034348280 SD034348280
		Samsung K4W2G1646C-HC11 SA000047Q00	1GB 2GB	0111	PD 45.3K	SD034453280 SD034453280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C SA0000324C0	512MB	0010	PD 15K	SD034154280
		Samsung K4W1G1646G-BC12 SA00004HS00	512MB	0011	PD 20K	SD034200280
	128M16 800MHz	Hynix H5TQ2G63BFR-12C SA00003VS00	1GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC12 SA00003MQ40	1GB	0111	PD 45.3K	SD034453280

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

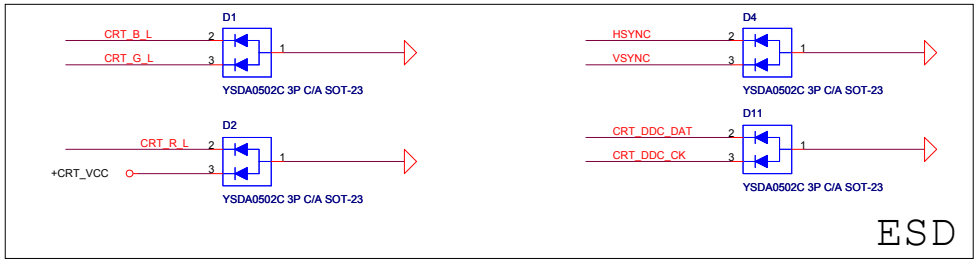
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

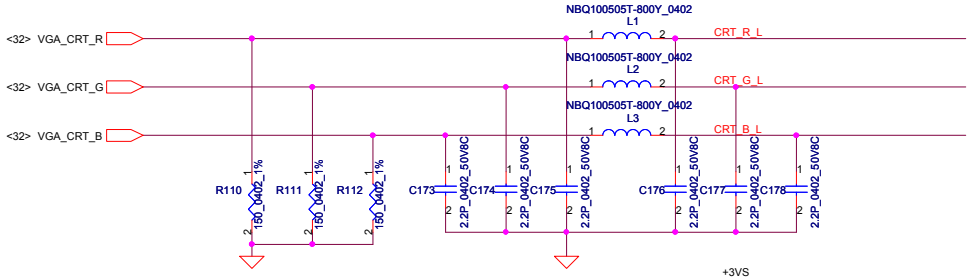
Compal Electronics, Inc.

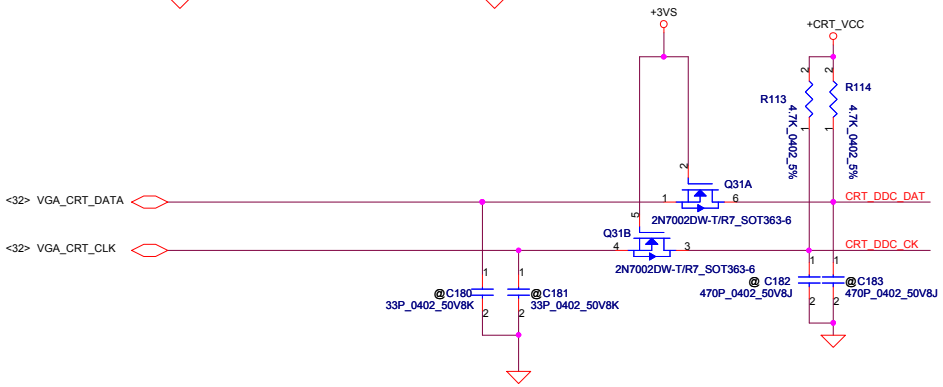
Title: VGA(12/12)-MISC

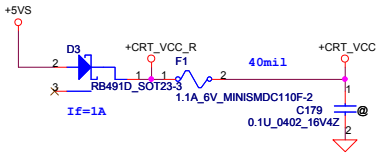
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 25 of 59

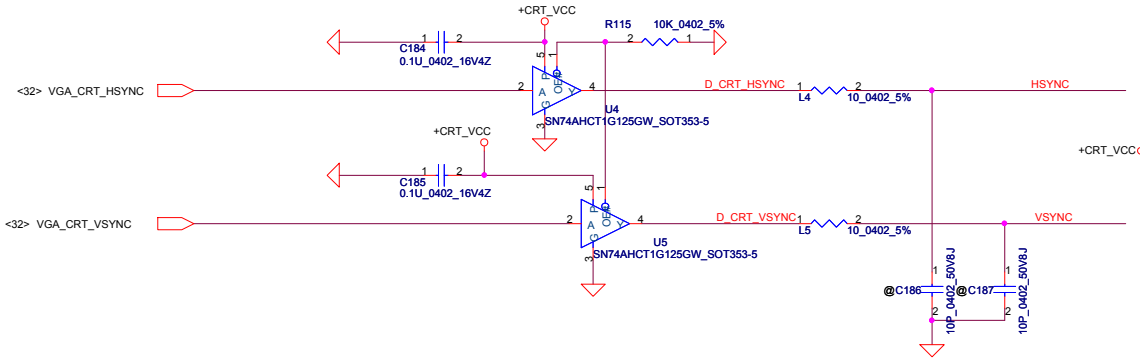


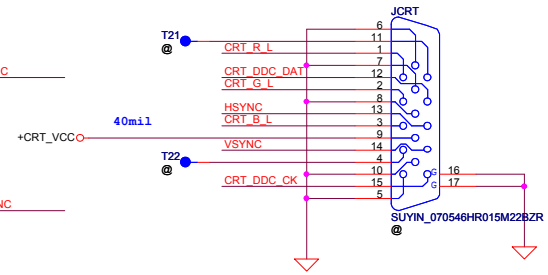






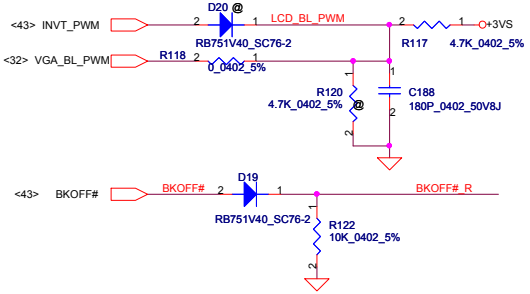
CRT CONNECTOR

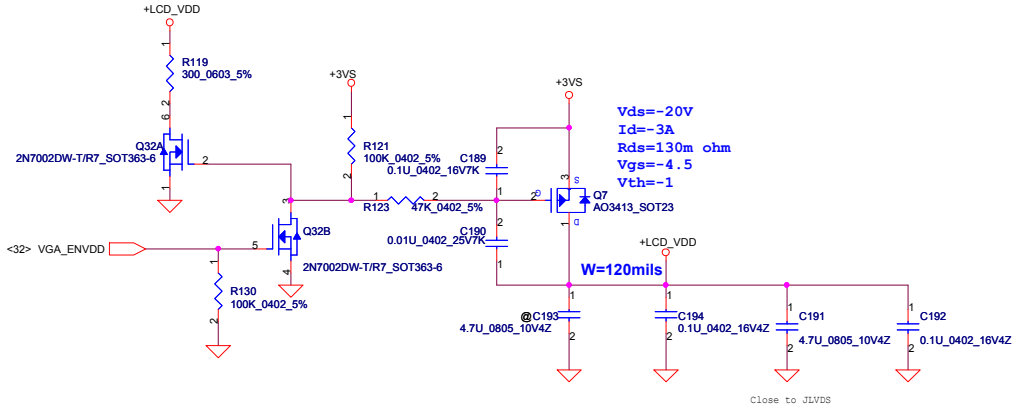




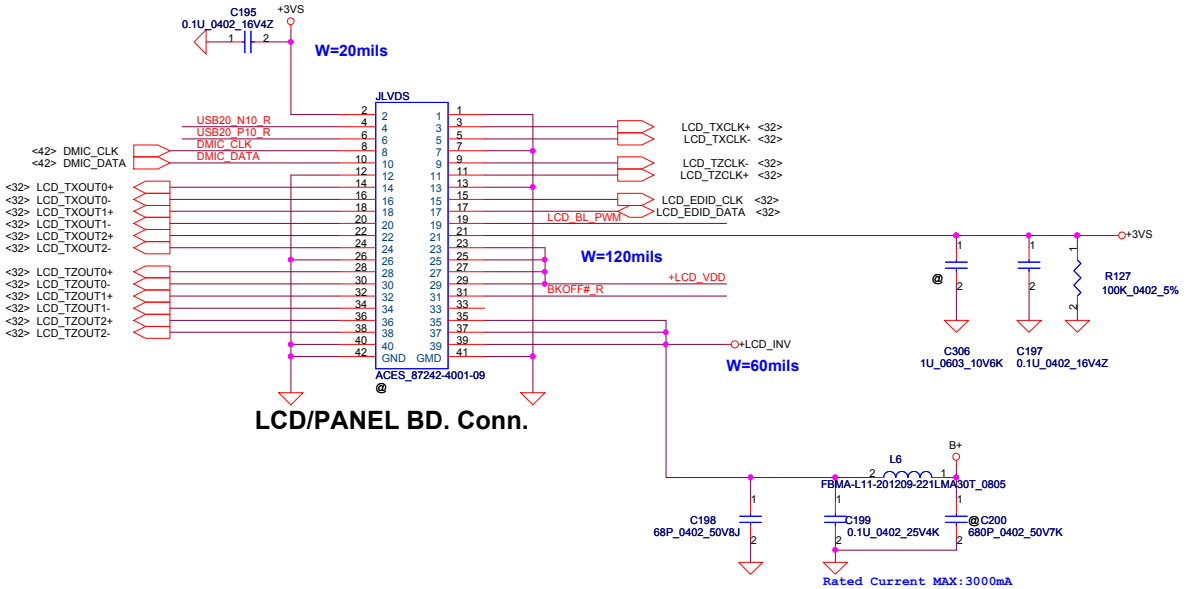
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.	
Title	CRT
Size	Document Number: PBL80 LA-7441P M/B
Rev	0.3
Date:	Monday, April 11, 2011
Sheet	26 of 59

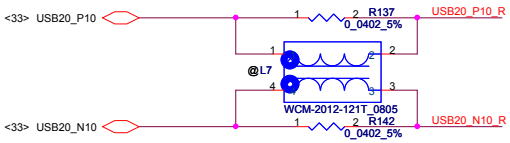


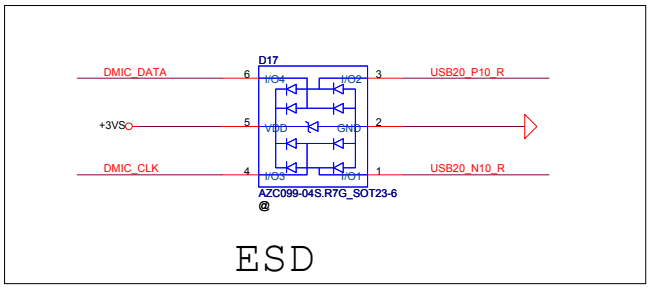


Dual Channel LVDS
Support 18.4" HD/FHD 16:9



LCD/PANEL BD. Conn.

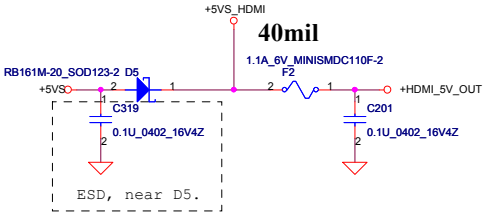


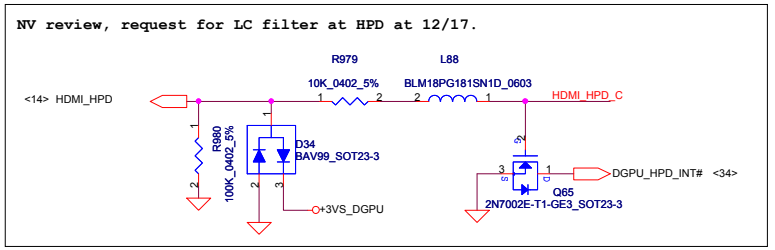


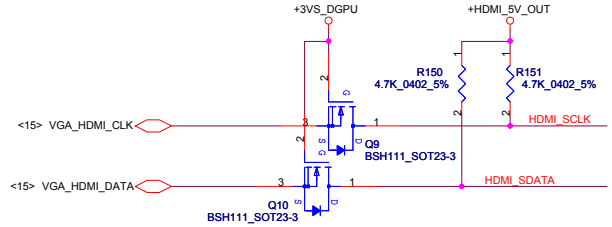
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

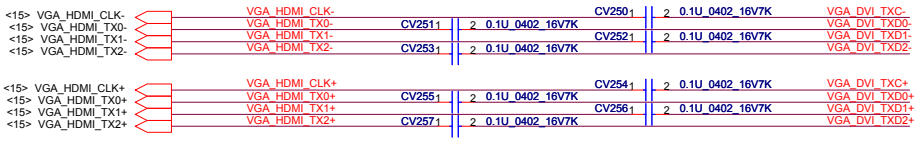
Compal Electronics, Inc.			
Title	LVDS		
Size	Document Number	PBL80 LA-7441P M/B	Rev 0.3
Date: Monday, April 11, 2011	Sheet 27 of 59		

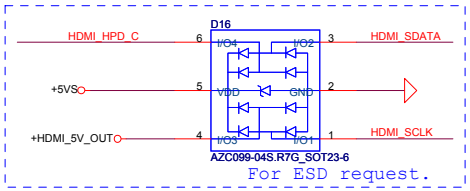
HDMI Connector

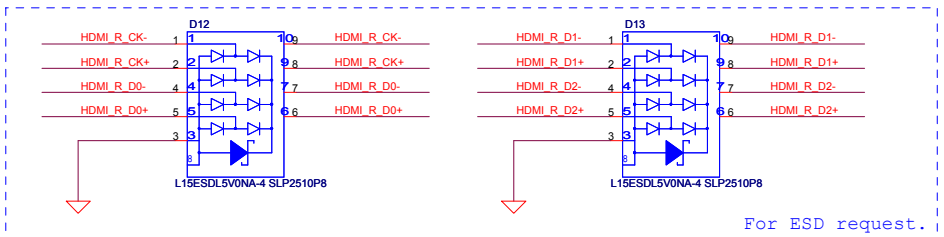


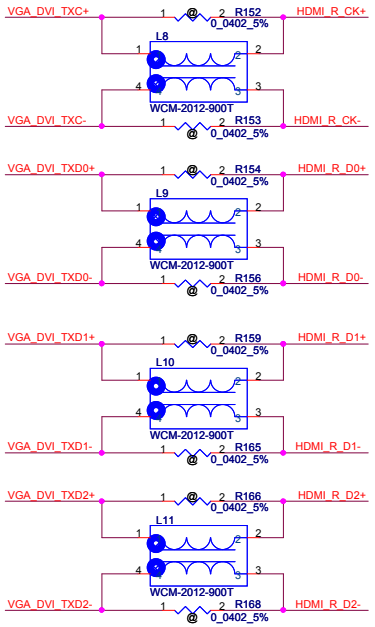


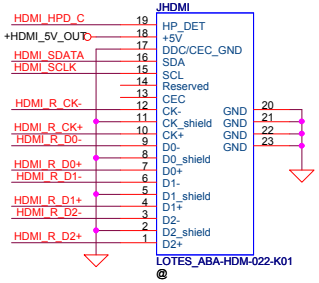


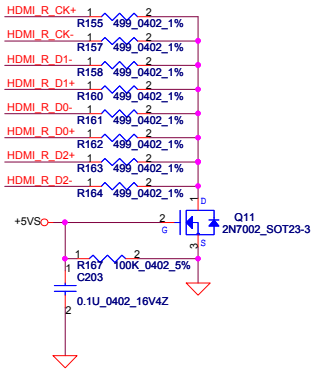












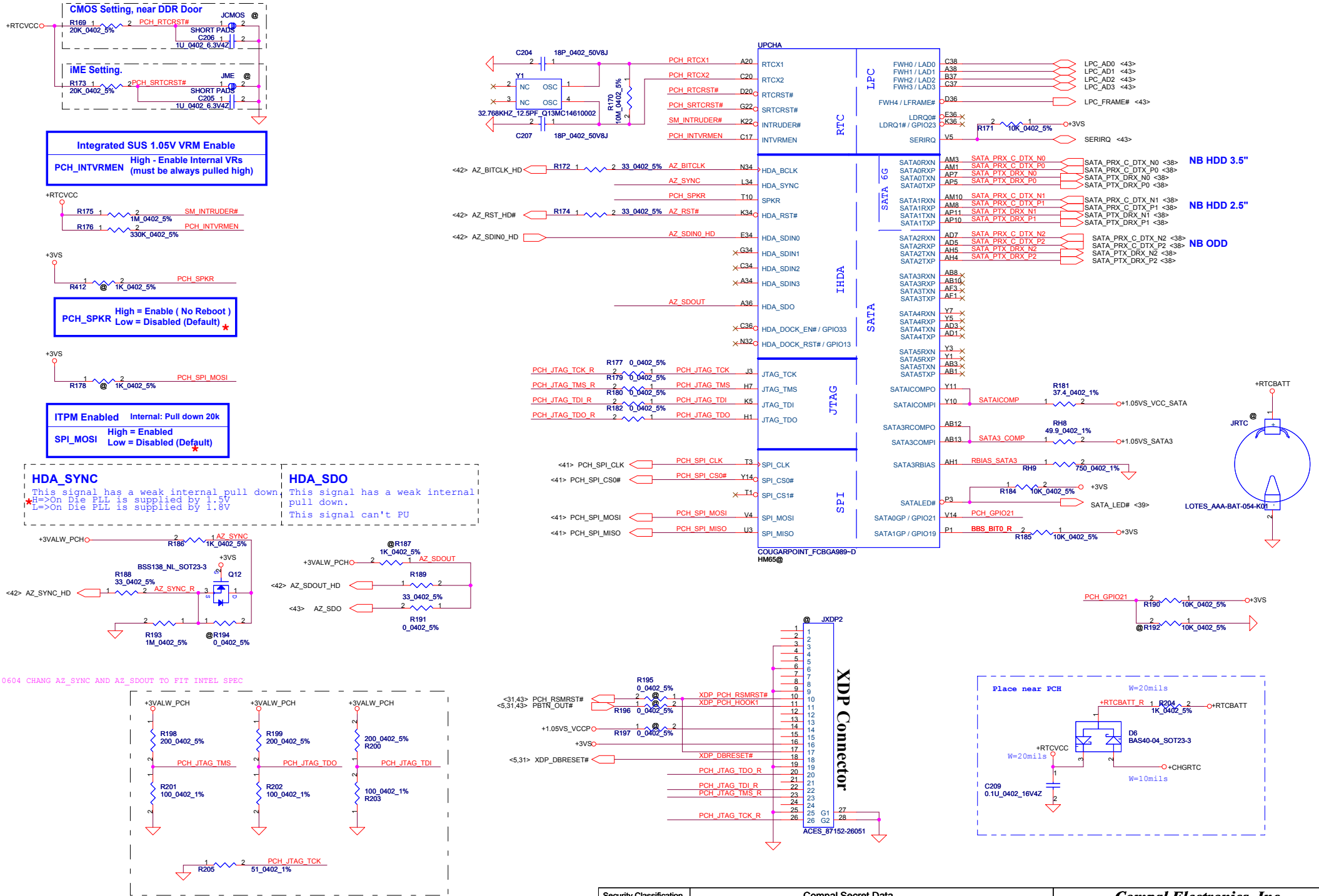
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 28 of 59



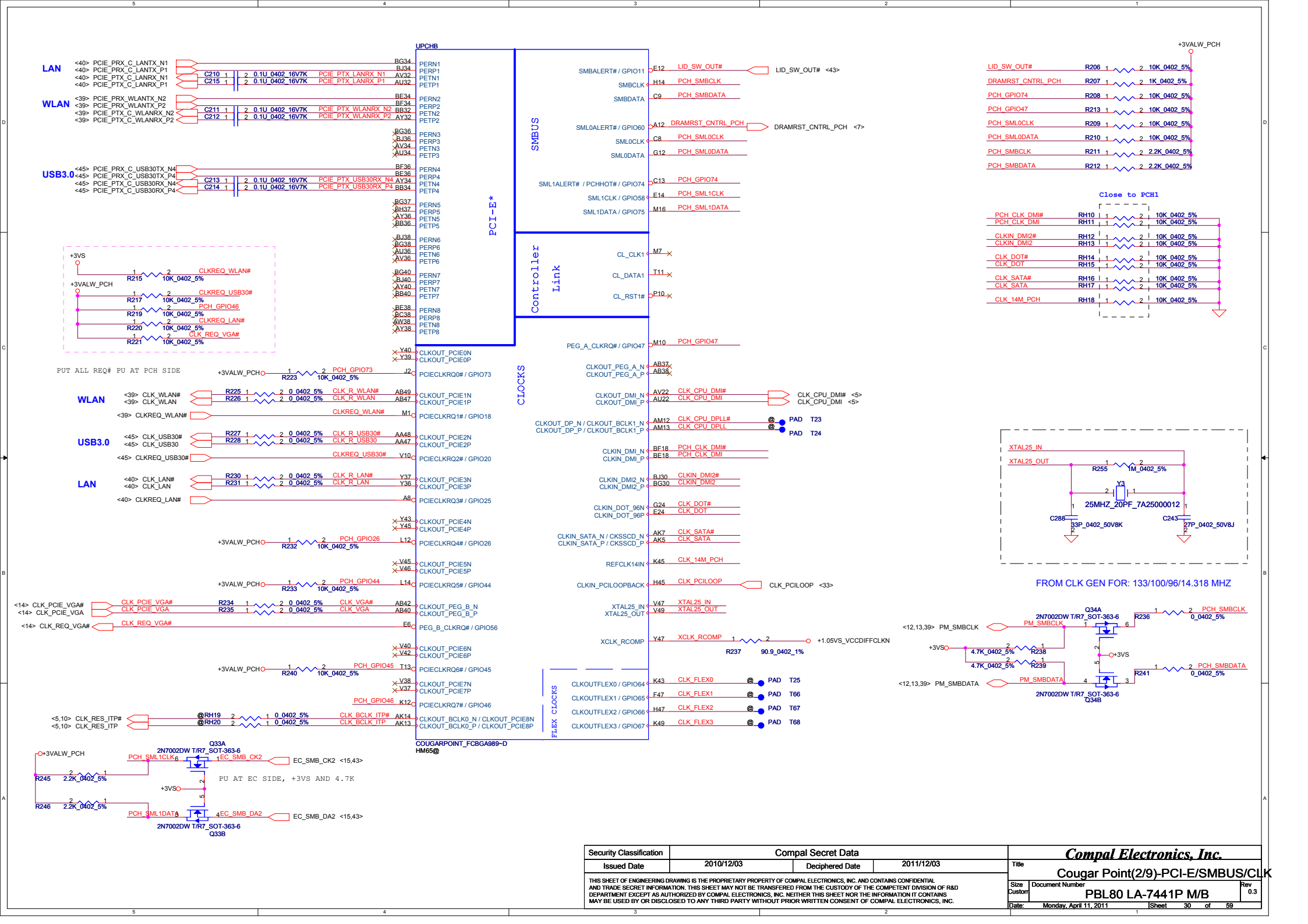
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(1/9)-HDA/SATA/XDP/RTC/SPI

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 29 of 59



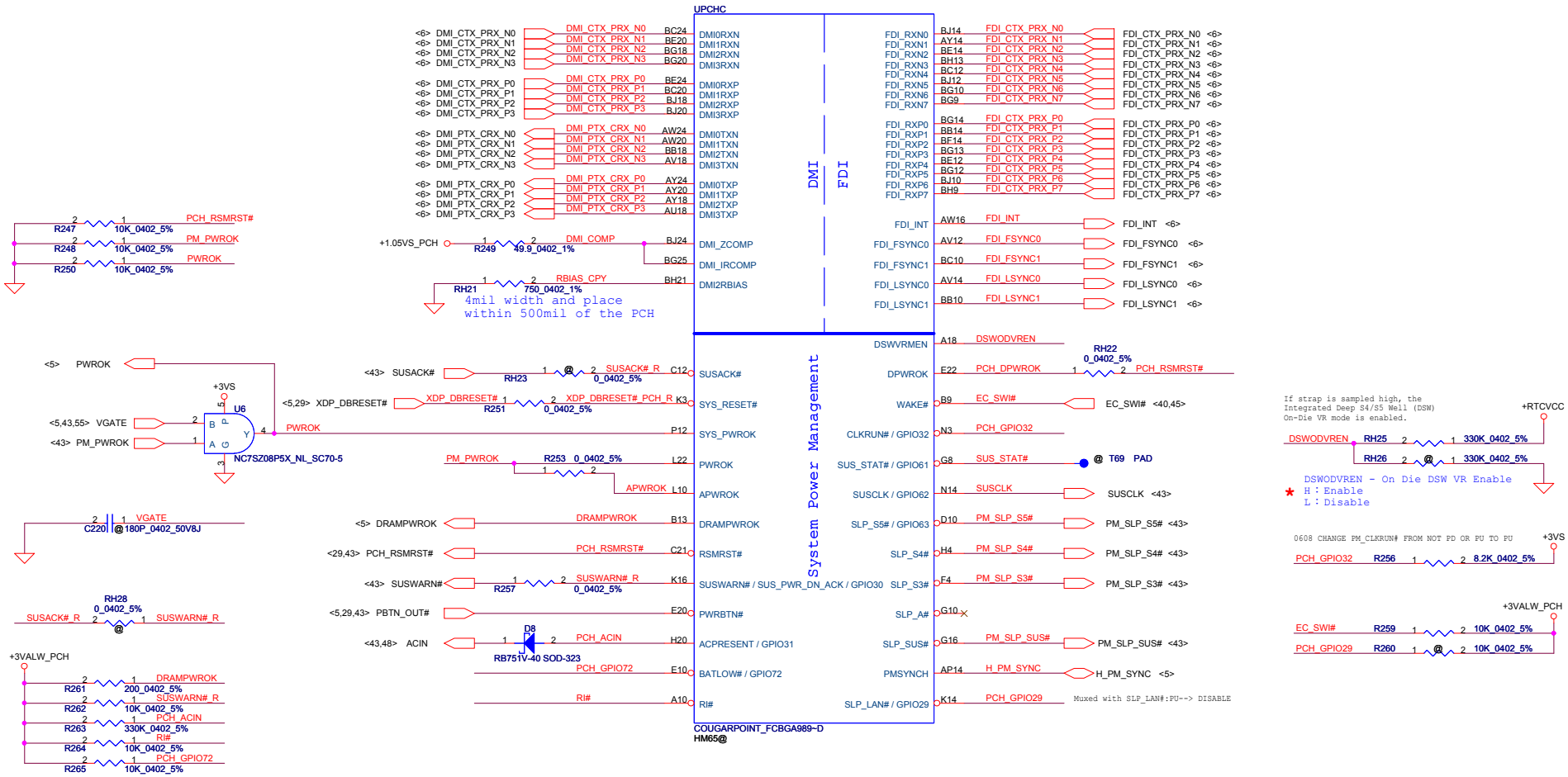
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(2/9)-PCI-E/SMBUS/CLK

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 30 of 59



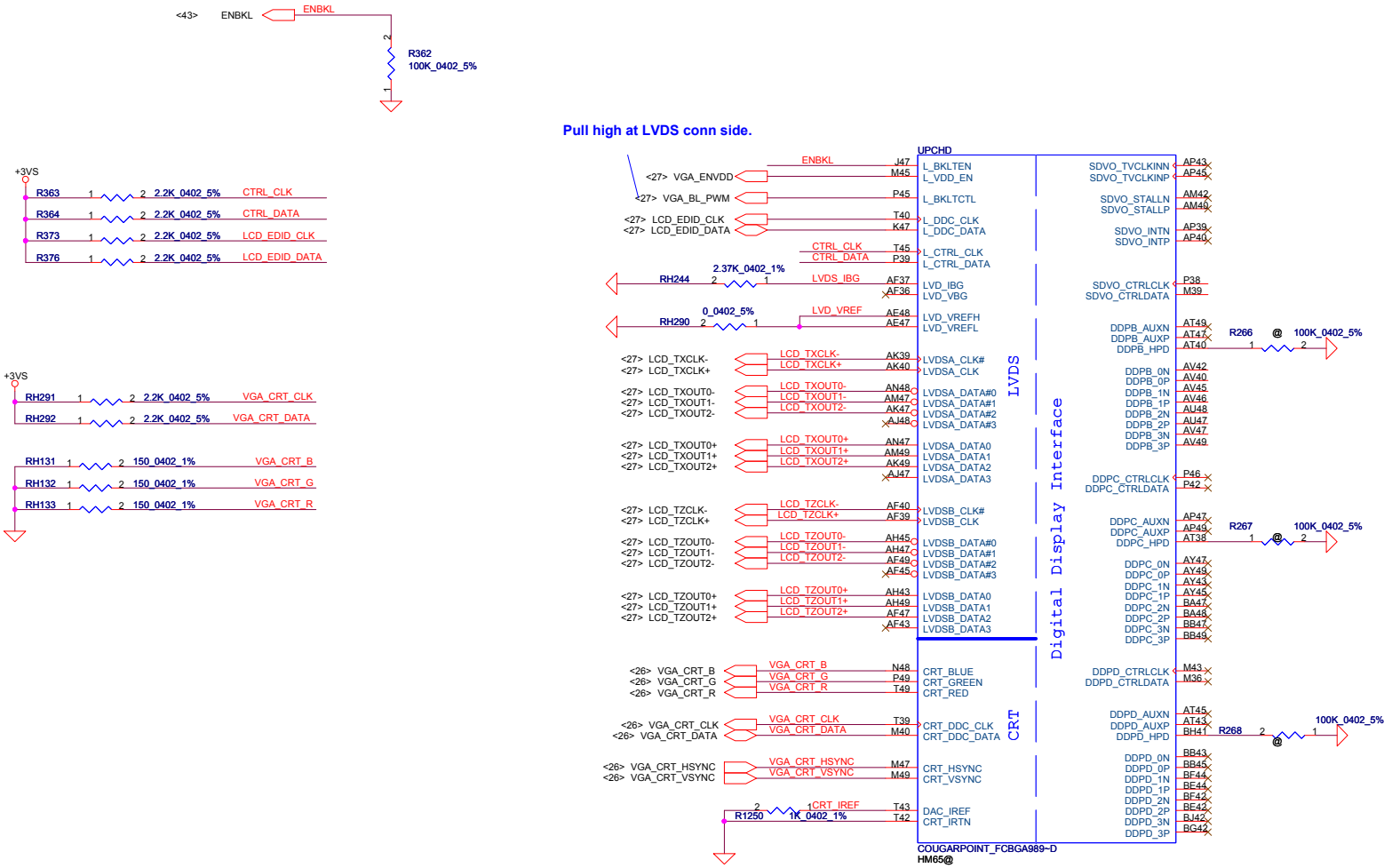
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(3/9)-DMI/FDI/PWM

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 31 of 59



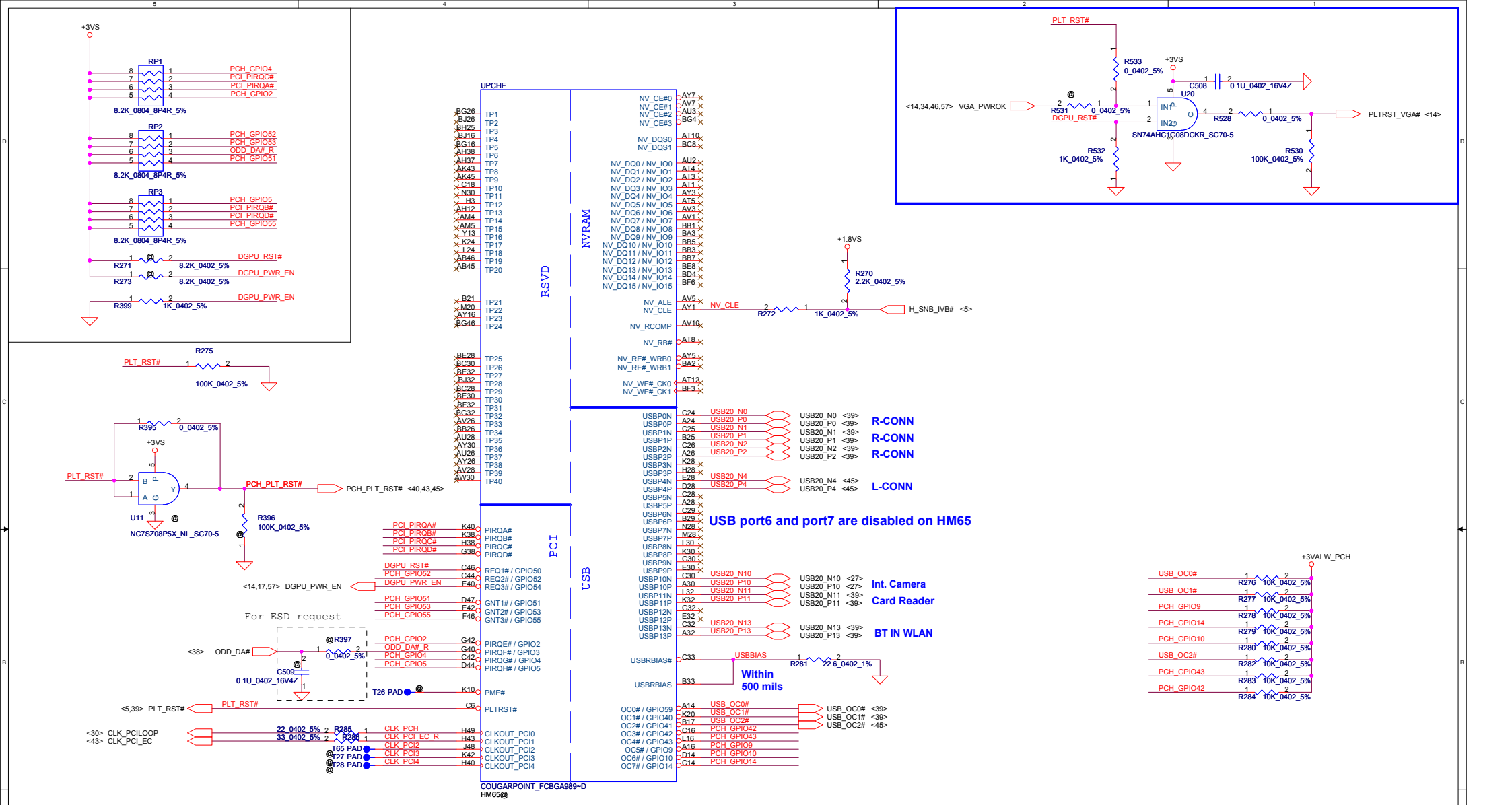
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(4/9)-CRT/LVDS/HDMI/DP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 32 of 59



Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

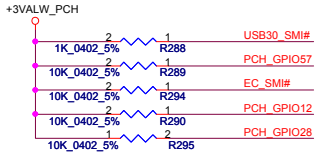
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

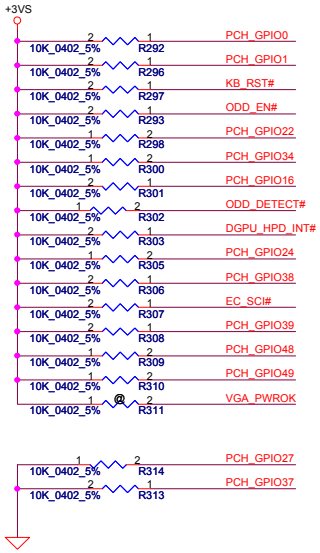
Compal Electronics, Inc.

Title: Cougar Point(5/9)-USB/PCI/NAND/STRAP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 33 of 59





GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

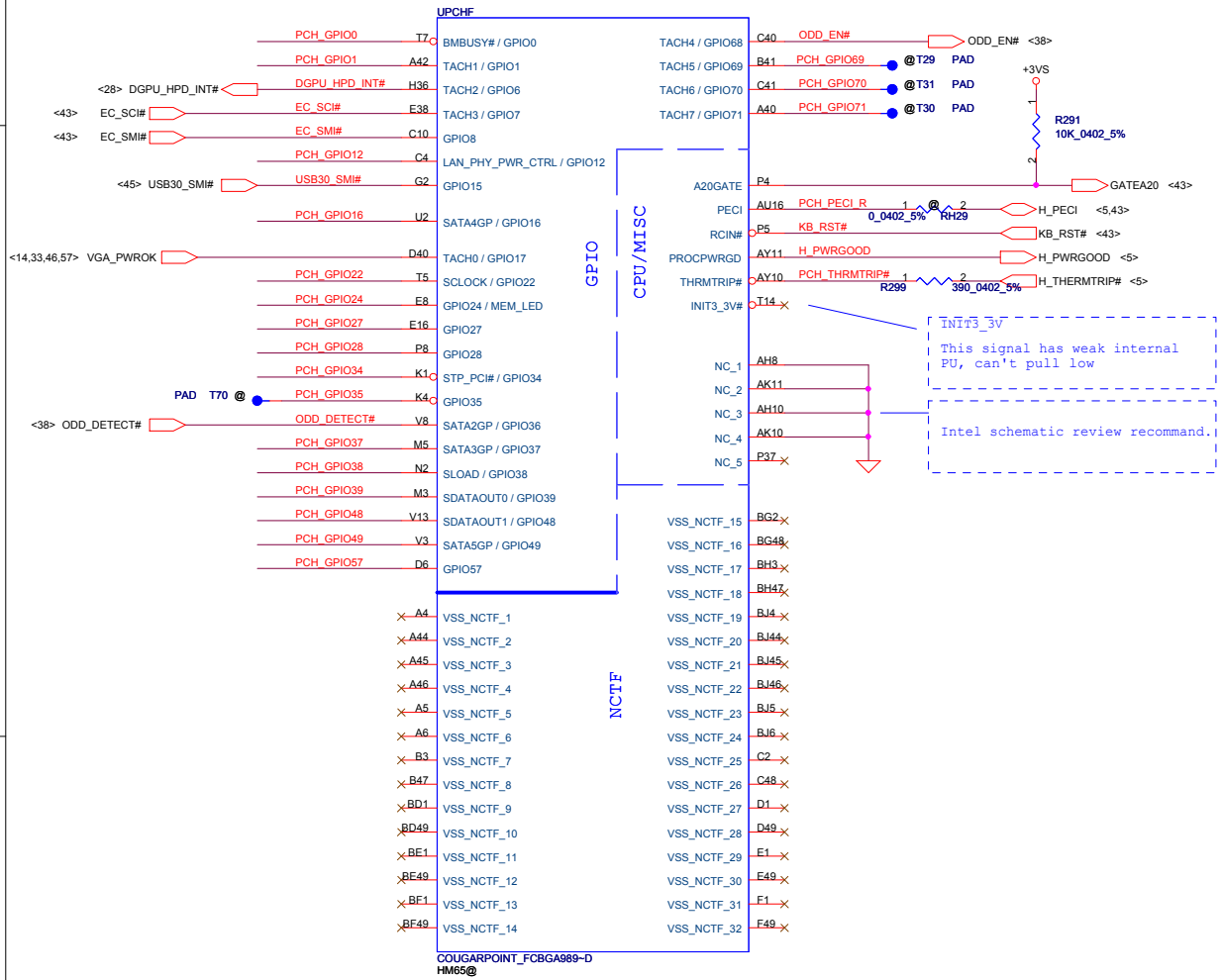
R315 1 @ 2 1K_0402_5% PCH_GPIO28

GPIO8
Integrated Clock Chip Enable

H ; Disable
* L ; Enable

R316 1 @ 2 1K_0402_5% EC_SMI#

Reserve for ICC enable.



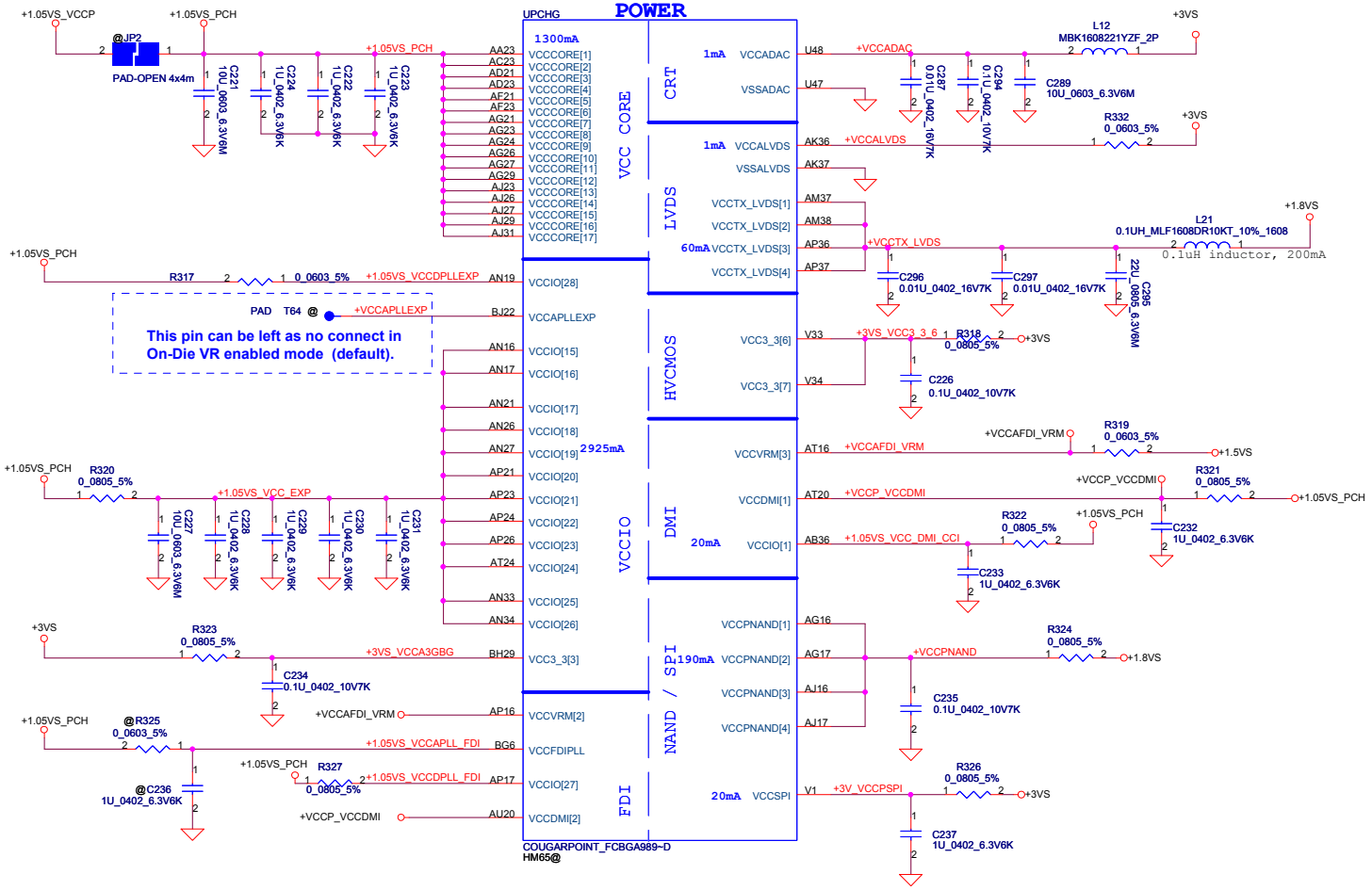
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(6/9)-CPU/GPIO/MISC

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 34 of 59



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: Cougar Point(7/9)-PWR1

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 35 of 59

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

Have internal VRM

POWER

UPCHJ

COUGARPOINT_FCBGA989~D
HM65@

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA

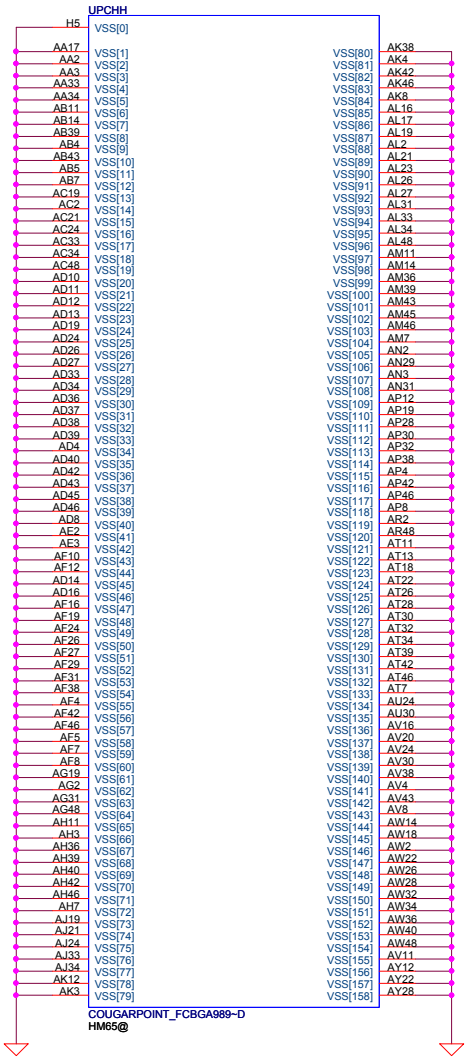
Security Classification: Compal Secret Data
Issued Date: 2010/12/03
Deciphered Date: 2011/12/03

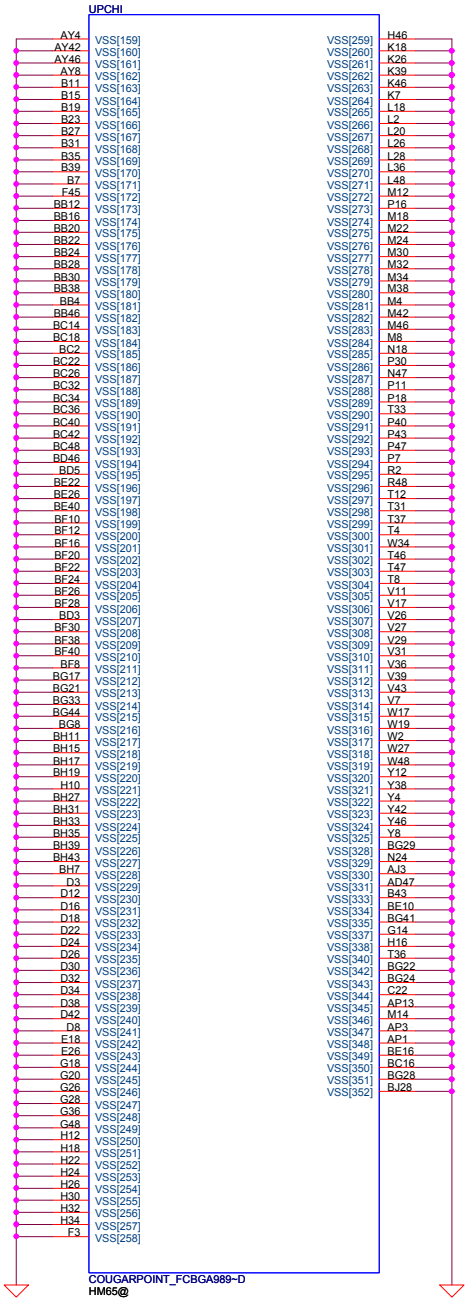
Compal Electronics, Inc.

Title: Cougar Point(8/9)-PWR2

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 36 of 59





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

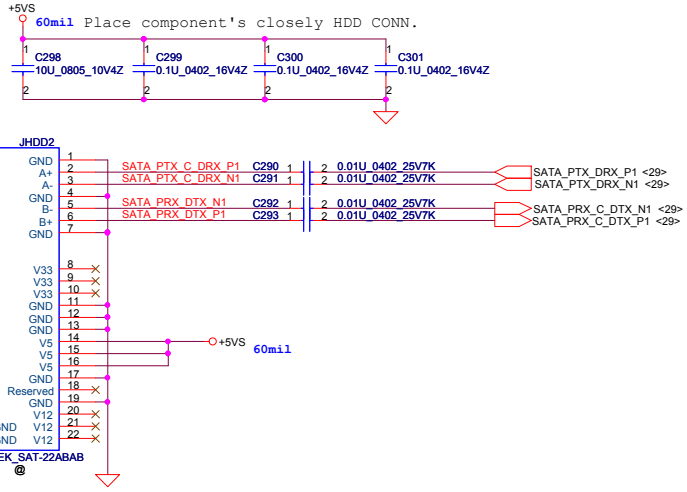
Compal Electronics, Inc.

Title: Cougar Point(9/9)-GND

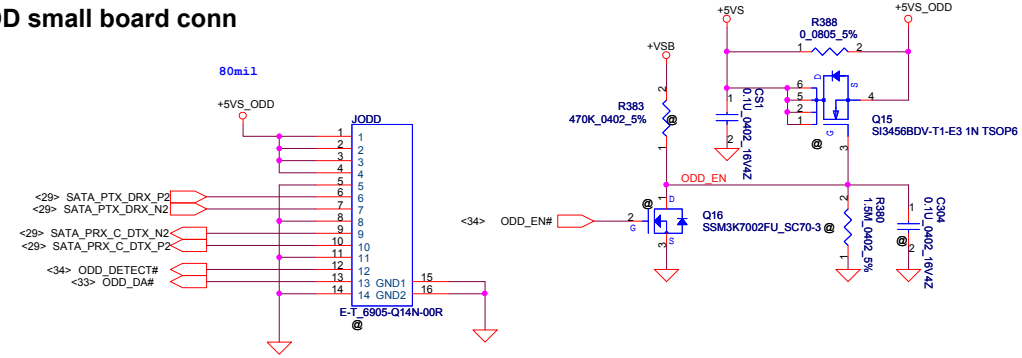
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 37 of 59

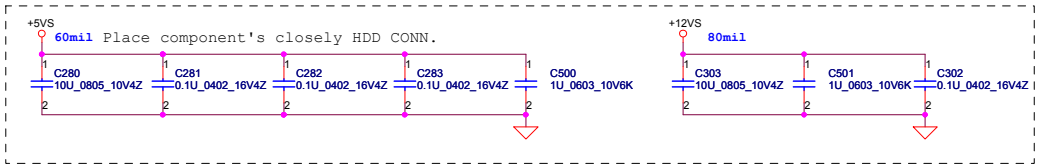
SATA HDD 2.5" Conn.



ODD small board conn

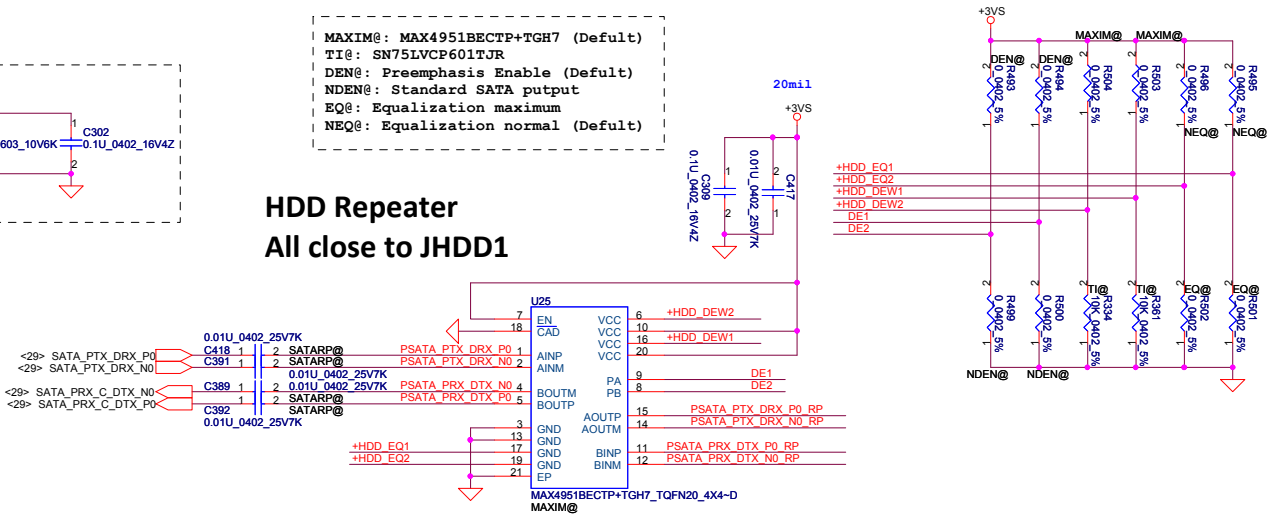


SATA HDD 3.5" Conn.

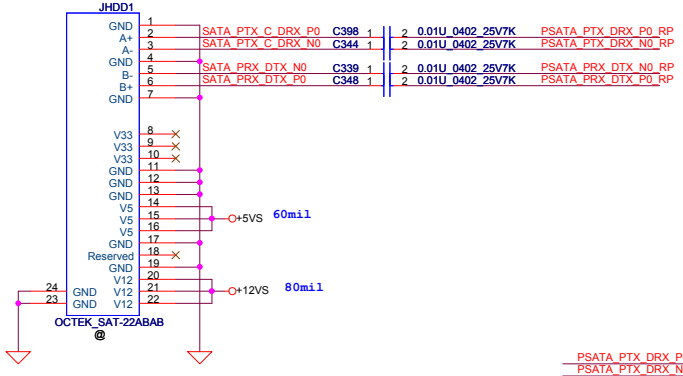


MAXIM@: MAX4951BECTP+TGH7 (Defult)
TI@: SN75LVCP601TJR
DEN@: Preemphasis Enable (Defult)
NDEN@: Standard SATA putput
EQ@: Equalization maximum
NEQ@: Equalization normal (Defult)

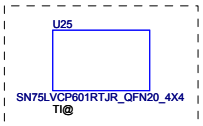
HDD Repeater
All close to JHDD1

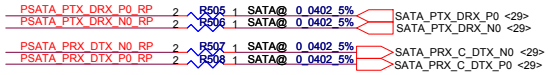


HDD



Note: +HDD_DEW1, +HDD_DEW2, +HDD_EQ1, +HDD_EQ2 need to route 10 mils





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

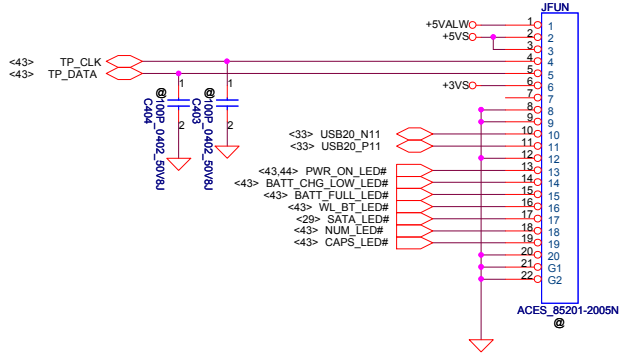
Compal Electronics, Inc.

Title: SATA-HDD&ODD/B

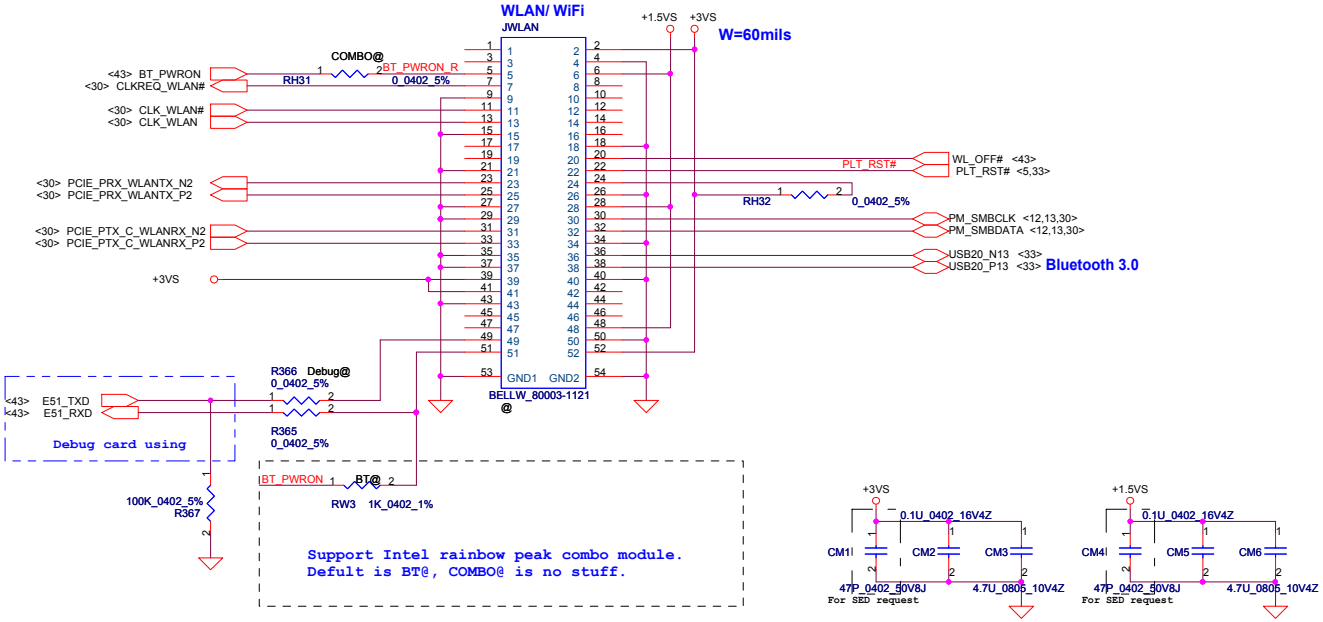
Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 38 of 59

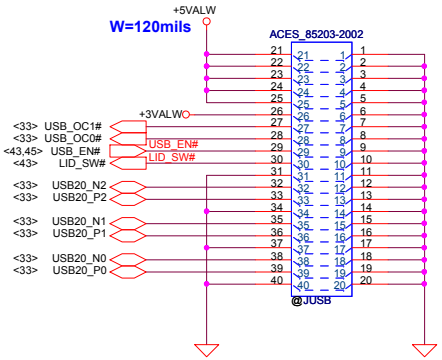
Touch pad & LID &
Card Reader & LED small board Connector



Slot 1 Half PCIe Mini Card-WLAN & BT3.0



USB & LID/B
Right USB X 3



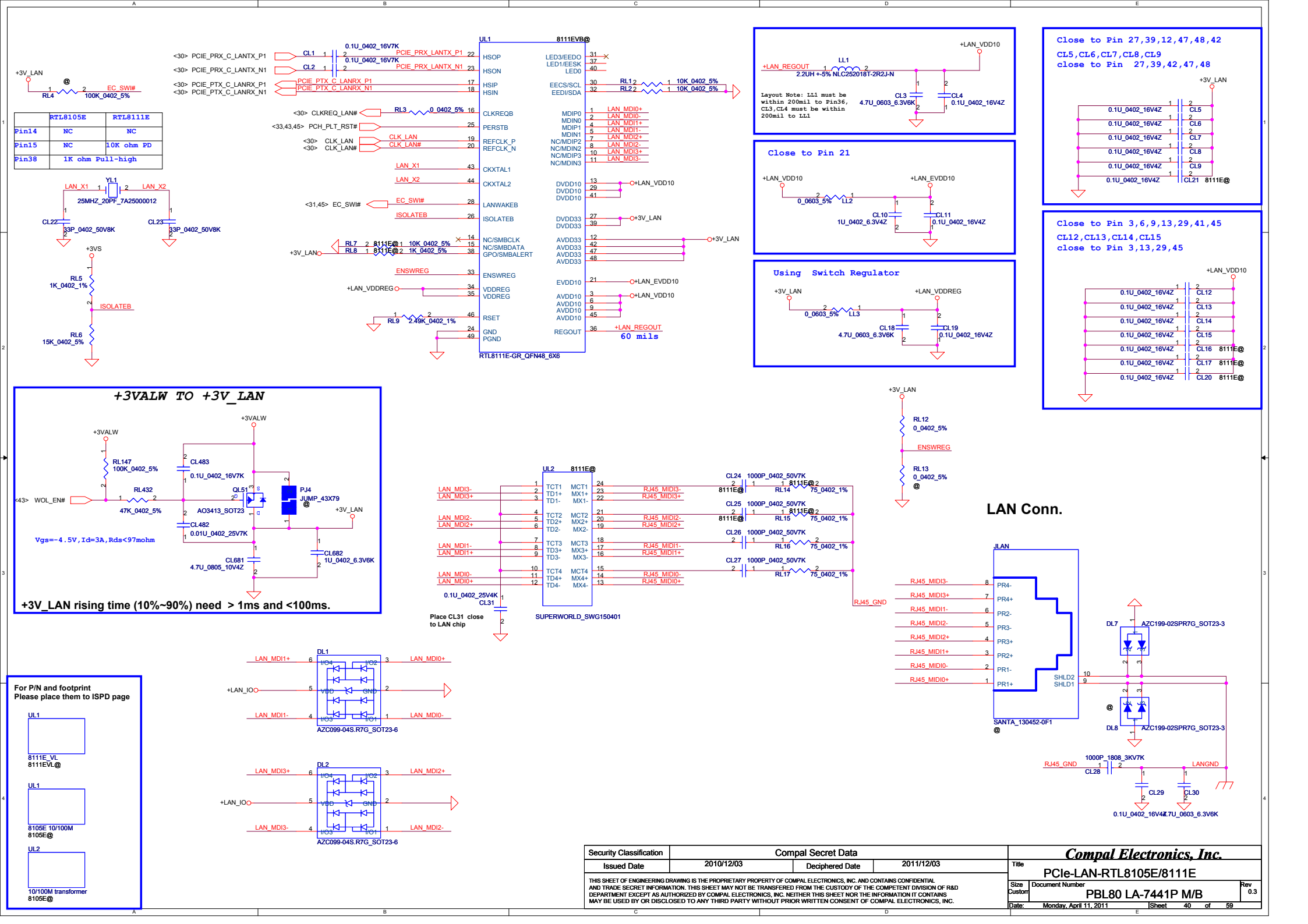
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: USB/LID/B&TP/LED/CR/B&PCIe-WLAN

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 39 of 59



Security Classification	Compal Secret Data
Issued Date	2010/12/03
Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E/8111E

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 40 of 59

BIOS Bus switch

SPI ROM For Basic ME ROM size 4MByte

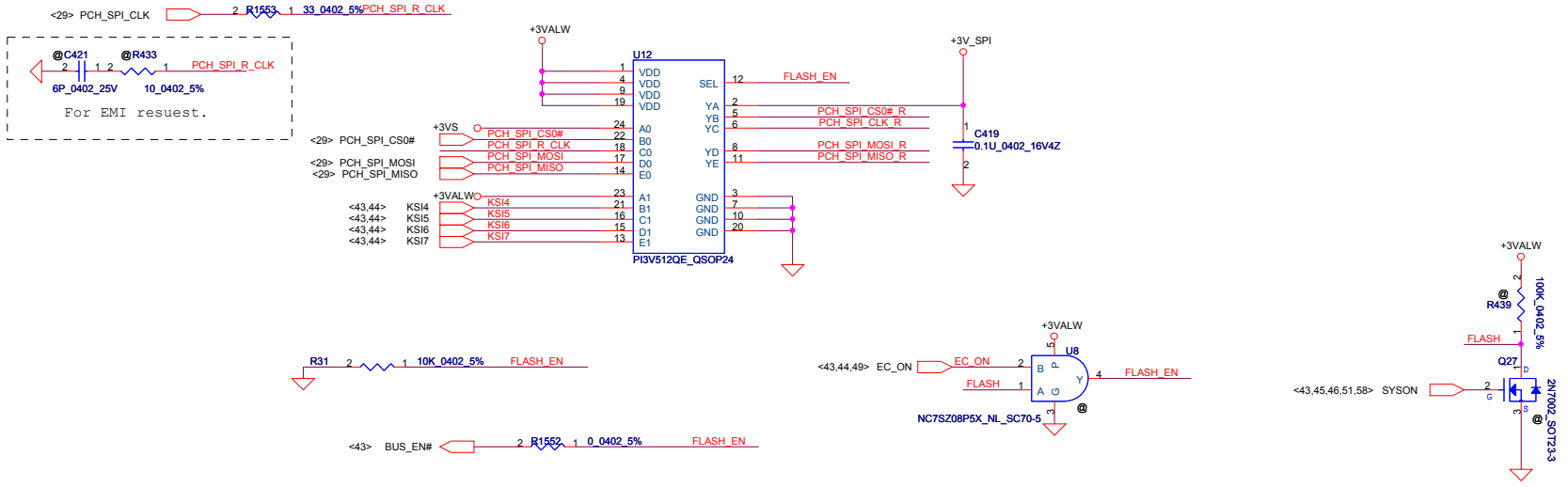
1. When Flash EC ROM.
   KSO2 to Low (Test mode)
   KSO3 to Low (ISP mode)---------FDA mode
   EC_ON->Low, BUS_EN#->Low
   U11 : Y->A0, PCH to BIOS ROM.
   KSI4,5,6,7 direct to EC_SPI

2. When Flash BIOS ROM.
   KSO2 to High
   KSO3 to Low (ISP mode)
   EC_ON->High, BUS_EN#->High.
   U11 : Y->A1, KSI4,5,6,7 to BIOS ROM.
   +3V_SPI from +3VALW
   Set EC pin KSI4,5,6,7 to HiZ.

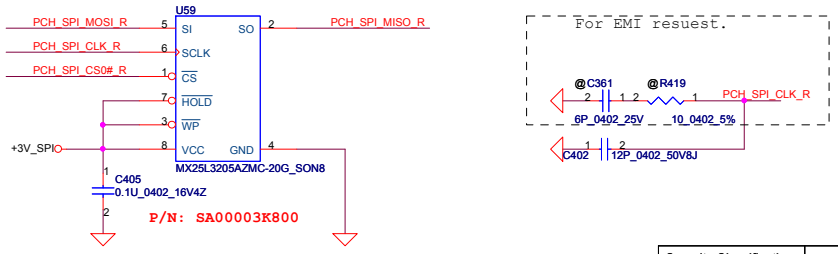
3.When normal operation.
   EC_ON->High , BUS_EN#->Low.
   U11 : Y->A0, PCH direct to BIOS ROM.
   +3V_SPI from +3VS.

4. When enter S3,4
   EC_ON->High, BUS_EN#->Low.
   U11 : Y->A1, PCH direct to BIOS ROM.
   But +3V_SPI from +3VS is no power.

** BUS_EN# only high when test mode.
   And must make sure it's low when FDA mode.
   Or HW use 10K pull down to GND.



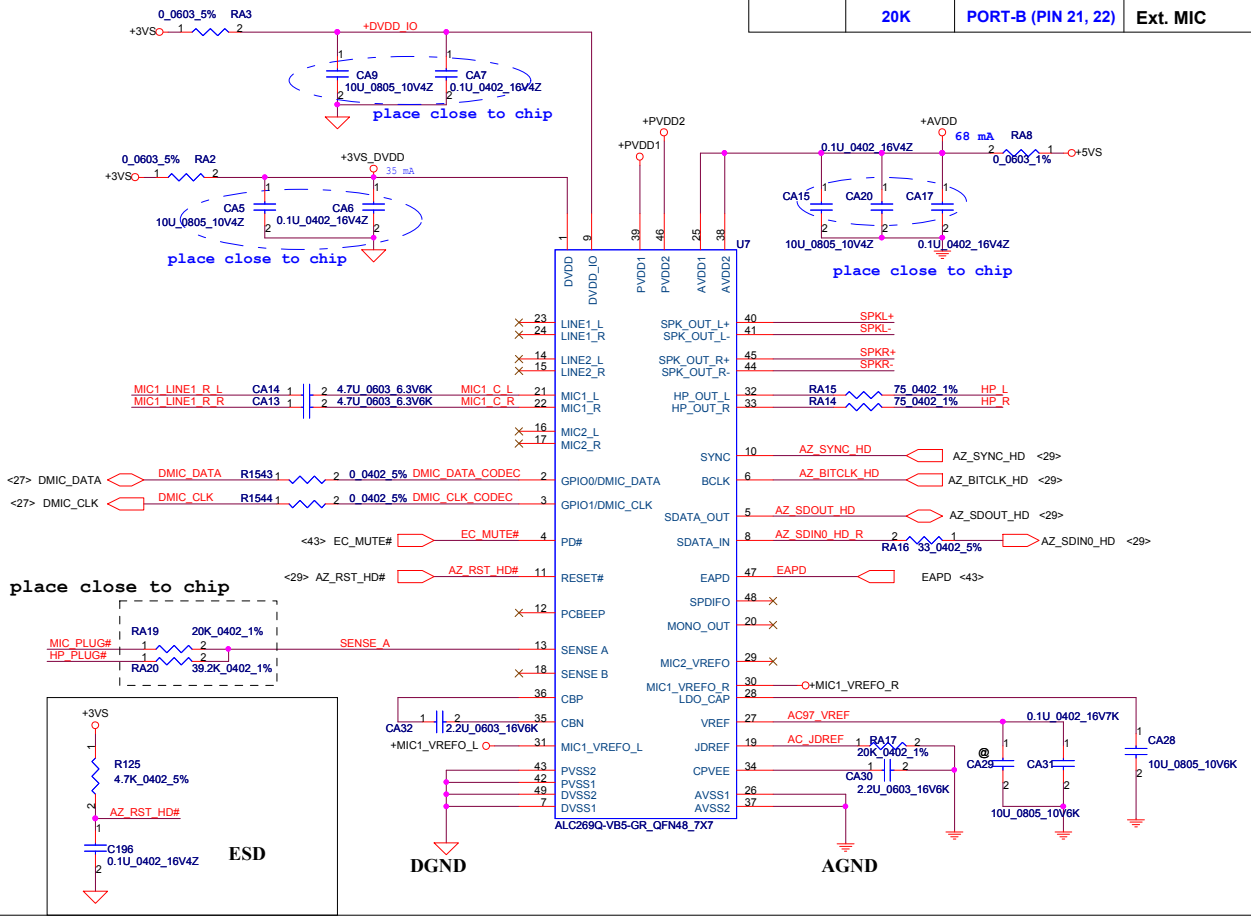
BIOS SPI Flash (4MByte*1)

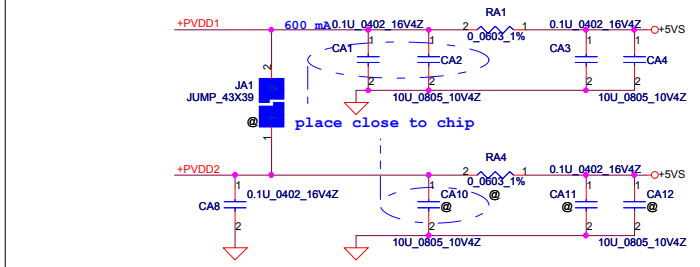


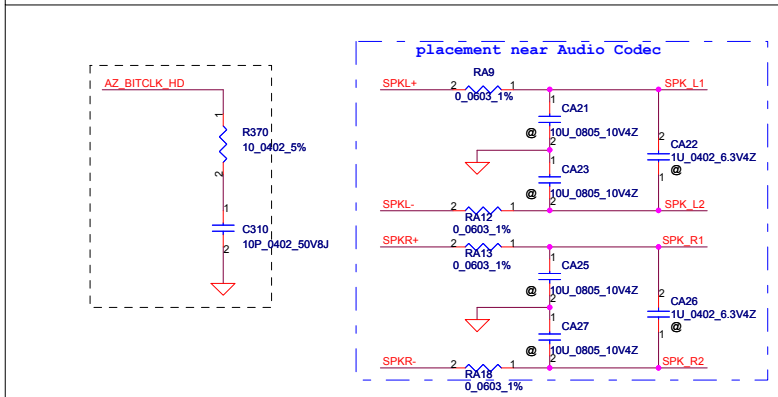
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

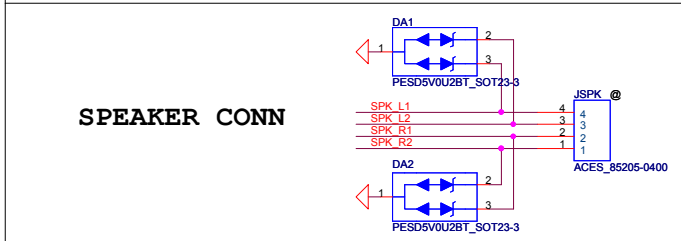
Compal Electronics, Inc.		
Title	Bus switch&BIOSROM	
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.3
Date: Monday, April 11, 2011	Sheet 41 of 59	

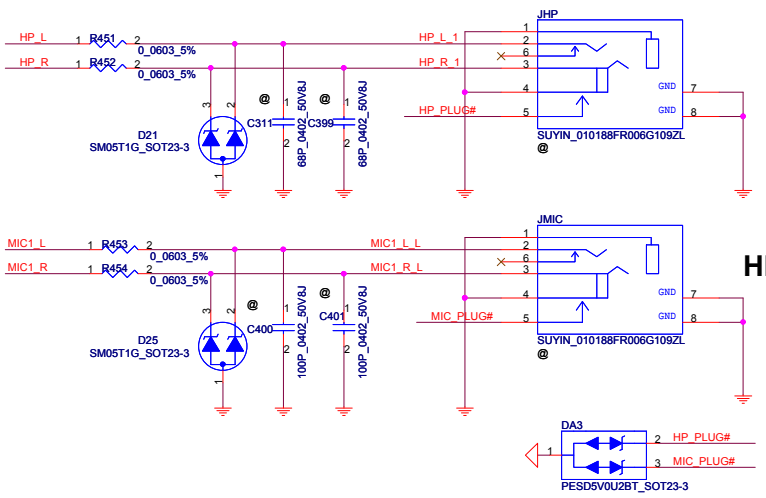
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC

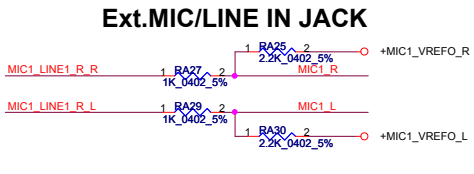












Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

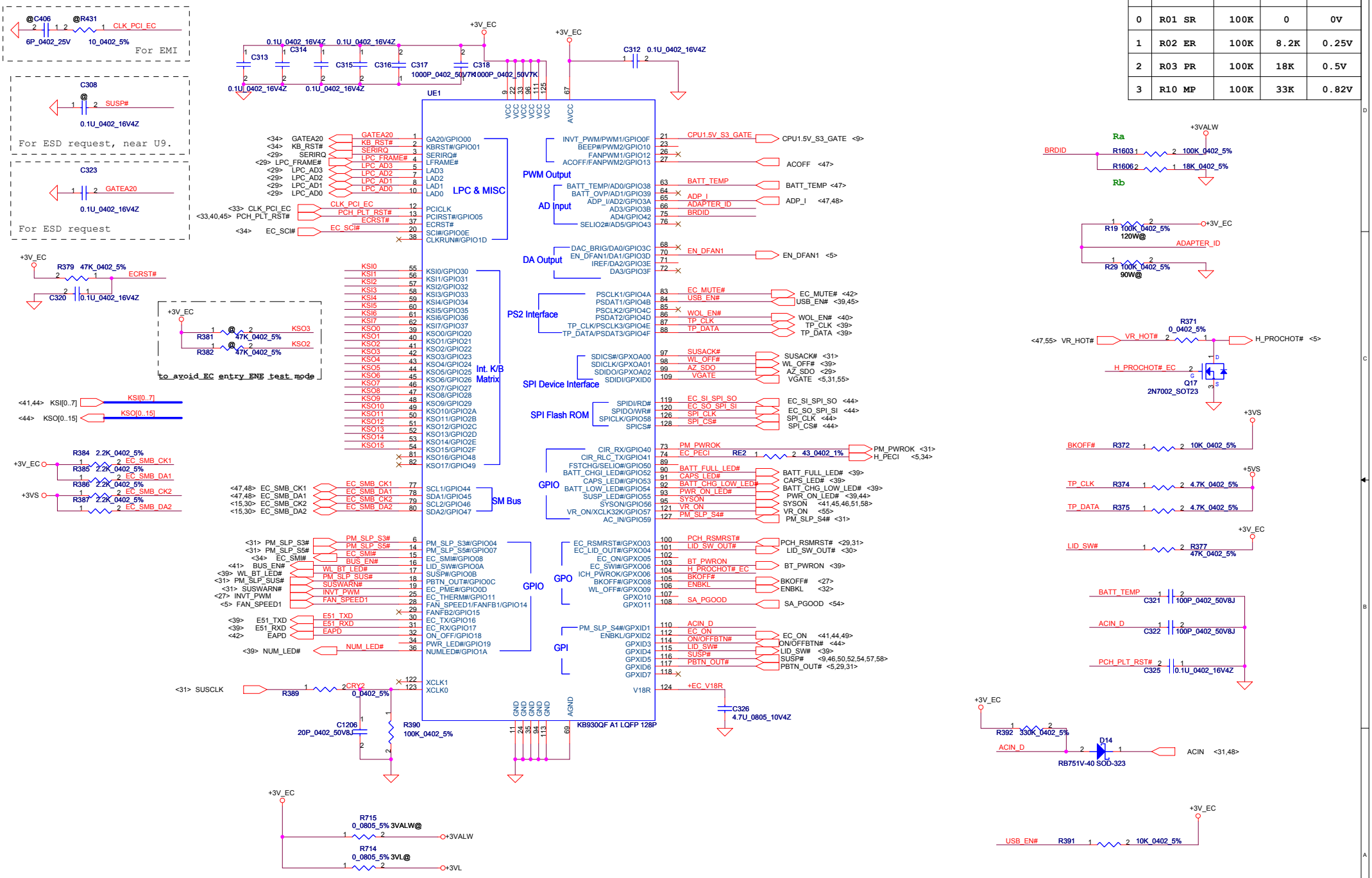
Compal Electronics, Inc.

Title: HD CODEC ALC269

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 42 of 59

ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

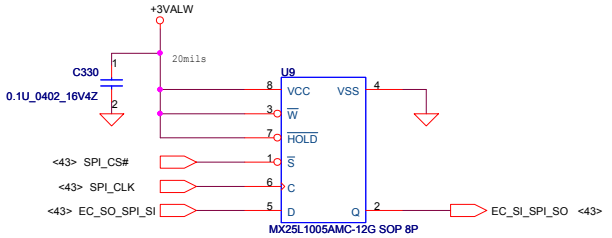
Compal Electronics, Inc.

Title: ENE-KB930

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

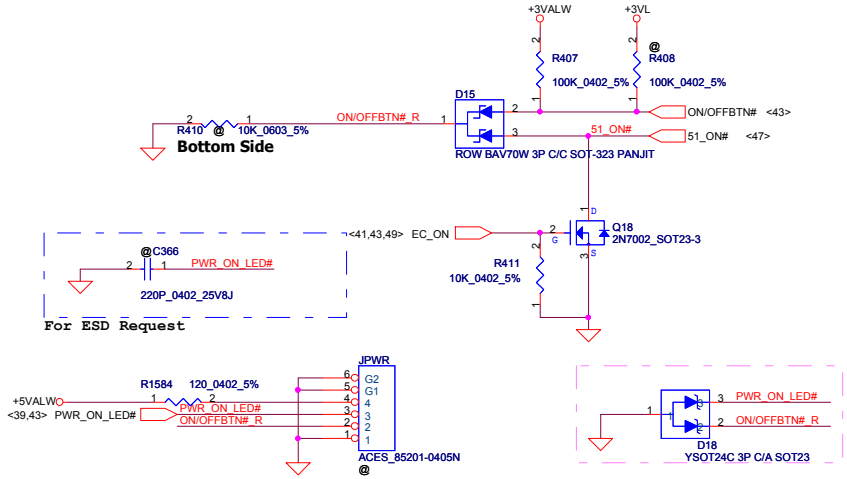
Date: Monday, April 11, 2011 | Sheet 43 of 59

SPI Flash (1MByte*1)

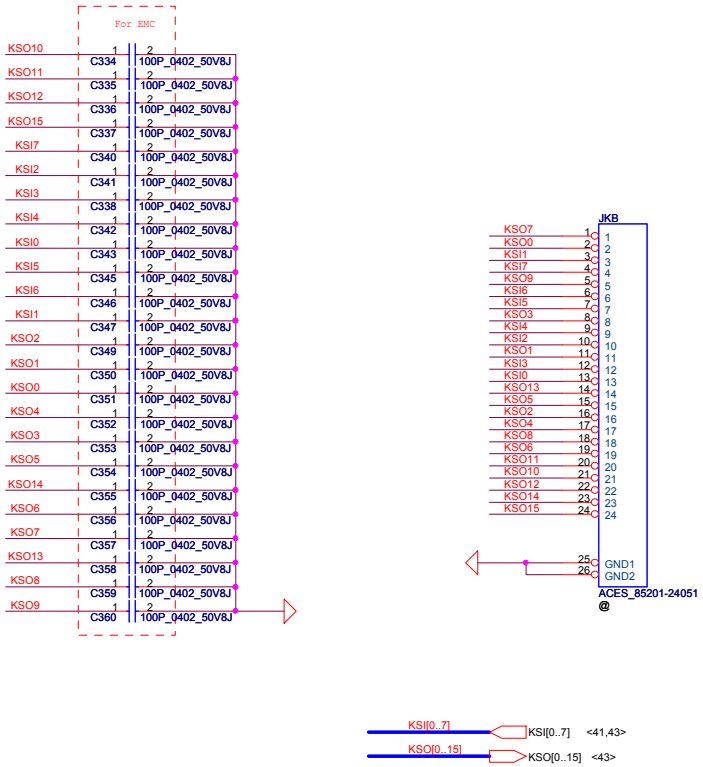


P/N :SA00002C100

Power Button/ PWR/B



KEYBOARD CONN.



KSI[0..7] KSI[0..7] <41,43>

KSO[0..15] KSO[0..15] <43>

Screw Hole

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H15 H21 H22

H_3P0 H_3P0 H_3P0 H_3P0 H_3P0 H_3P0 H_3P0 H_3P0 H_3P0 H_3P0 H_3P0N H_3P0X3P5N H_3P0X3P5N

@

CPU

H12 H11 H13 H14

H_4P7 H_4P2 H_4P2X4P7 H_4P2X4P7

VGA

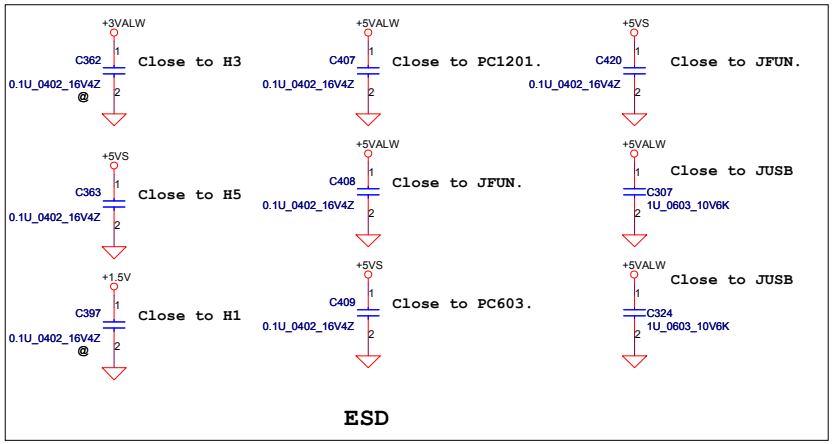
H20 H19 H18

H_2P9 H_2P9X3P9 H_2P9X3P9

WLAN

H17 H16

H_3P3 H_3P3



PCB Fedical Mark PAD

FD1 FD2 FD3 FD4

ISPD

PCB ZZZ

PCB LA-7441P REV01

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: ECROM/KB/PWR/B/SCREW

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 44 of 59

+1.5V to +1.05V Transfer

Vout=0.8*(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

+3V & +1.05V has power sequence timing:
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms

Close to U102.D7

Close to U102.P13

Follow Vendor recommend.

+3V:200mA
+1.05V:800mA

CSEL=0 : 24MHz XTAL
CSEL=1 : 48MHz Clock

Place as close as possibile to
UU2.N14 and UU2.M14

must to close to JUSB30

W=80mils

2.5A

35mA

Close to UU4.6

UPD720200A:
SMIB Low active

For UPD720200:
SMI high active

2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

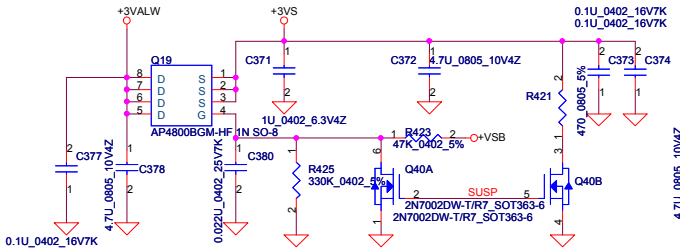
Title: PCIe-USB3.0

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 45 of 59

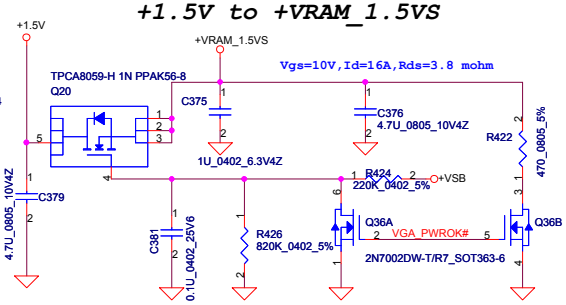
+3VALW TO +3VS

Vgs=-0V,Id=9A,Rds=18.5mohm

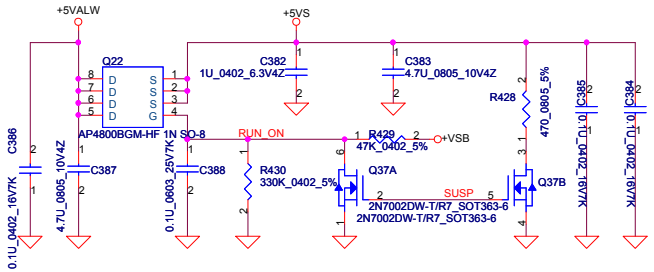


+1.5V to +VRAM_1.5VS

Vgs=10V,Id=16A,Rds=3.8 mohm

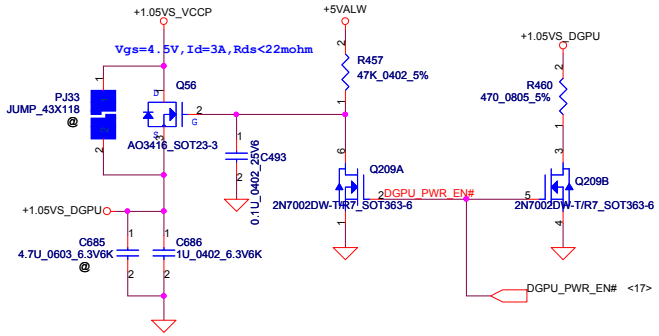


+5VALW TO +5VS



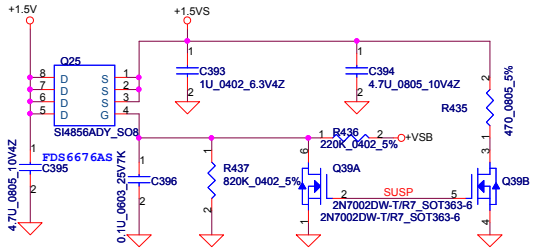
+1.05VS_VCCP to +1.05VS_DGPU

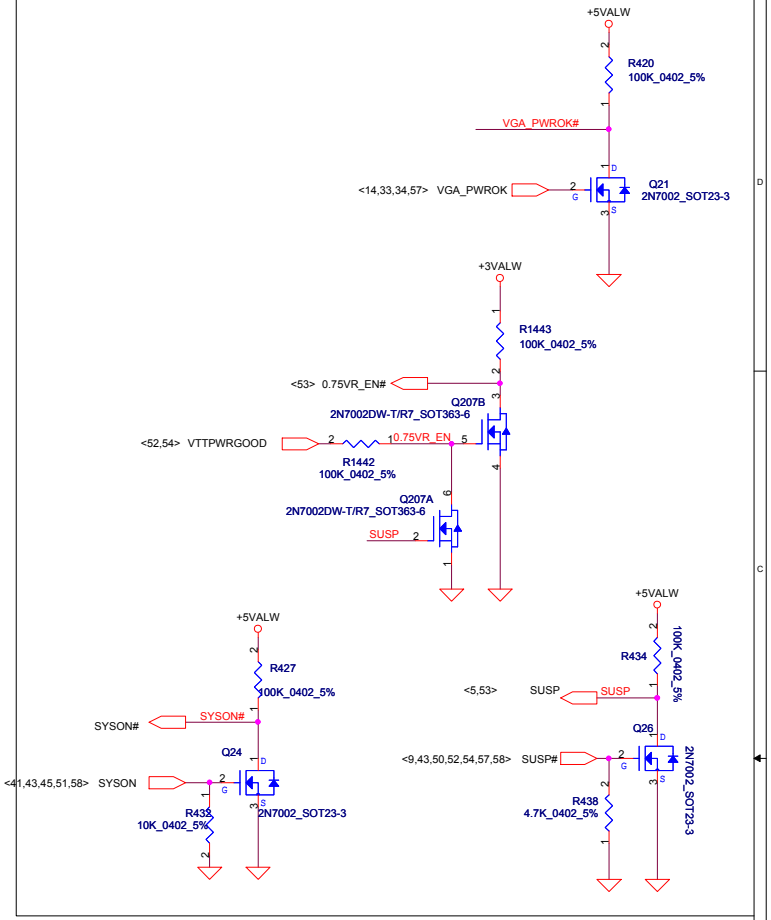
Vgs=4.5V,Id=3A,Rds<22mohm



+1.5V to +1.5VS

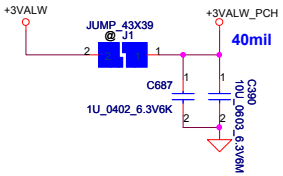
Vgs=10V,Id=14.5A,Rds=6mohm

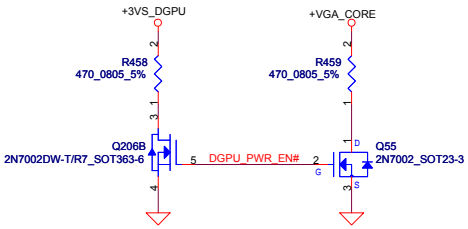


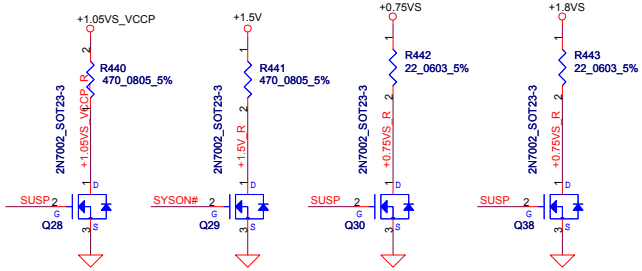


+3VALW TO +3VALW(PCH AUX Power)

Short J1 for PCH VCCSUS3.3







Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.3

Date: Monday, April 11, 2011 Sheet 46 of 59

DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

need confirm: ME give us battery connector P/N is DC040000800

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

If EC use 3VL and can not detect VGATE, must connect EN0

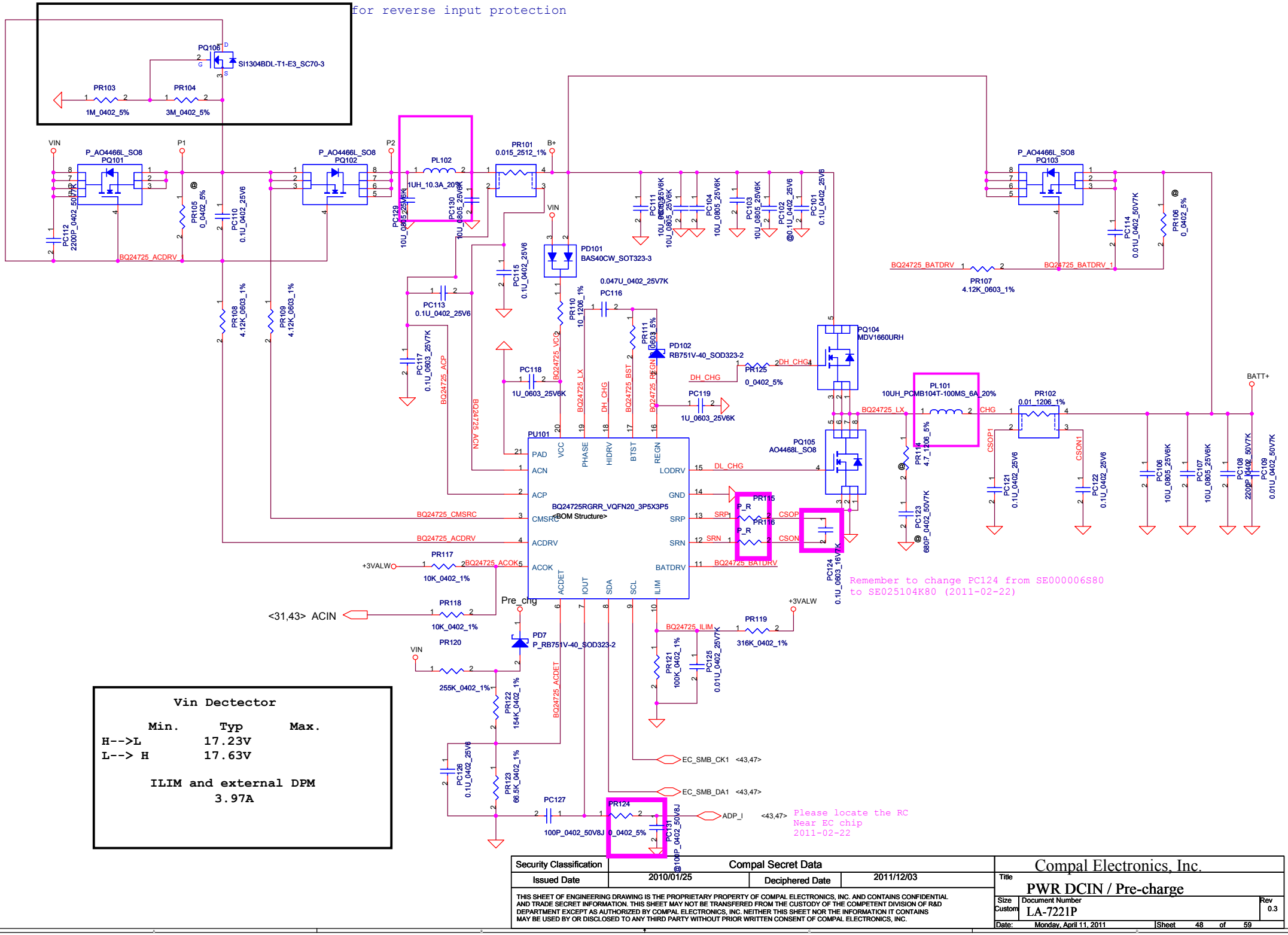
Reserve when EC use +3VL.
Install when EC use +3VALW.

(120mA,40mils ,Via NO.= 1)

@ Pre-charge

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/03

Compal Electronics, Inc.	
Title	DCIN / BATT CONN / OTP
Size	Document Number: NCL61 LA-6321P M/B
Rev	0.3
Date: Monday, April 11, 2011	Sheet 47 of 59


for reverse input protection
PQ106
SI1304BDL-T1-E3_SC70-3
PR103
1M_0402_5%
PR104
3M_0402_5%
VIN
P1
P2
P_AO4466L_SO8
PQ101
PQ102
PQ103
PL102
1UH_10.3A_20%
PR101
0.015_2512_1%
B+
PD101
BAS40CW_SOT323-3
PC112
2200P_0402_50V7K
PR105
0_0402_5%
PC110
0.1U_0402_25V6
PC129
10U_0805_25V6K
PC130
PC111
PC104
PC103
PC102
PC101
PR106
PC114
0.01U_0402_50V7K
BQ24725_ACDRV
PR108
4.12K_0603_1%
PR109
PC113
0.1U_0402_25V6
PC115
PC116
0.047U_0402_25V7K
PR110
10_1206_1%
PR111
PC117
0.1U_0603_25V7K
PC118
1U_0603_25V6K
PC119
PD102
RB751V-40_SOD323-2
PR125
0_0402_5%
DH_CHG
PQ104
MDV1660URH
PR107
4.12K_0603_1%
BQ24725_BATDRV
PL101
10UH_PCMB104T-100MS_6A_20%
PR102
0.01_1206_1%
BATT+
BQ24725_LX
PR114
4.7_1206_5%
PC123
680P_0402_50V7K
PC121
PC122
PC106
PC107
PC108
2200P_0402_50V7K
PC109
0.01U_0402_50V7K
PQ105
AO4468L_SO8
PU101
BQ24725RGRR_VQFN20_3P5X3P5
<BOM Structure>
PAD
ACN
ACP
CMSRC
ACDRV
ACOK
VCC
PHASE
HIDRV
BTST
REGN
LODRV
GND
SRP
SRN
BATDRV
ACDET
IOUT
SDA
SCL
ILIM
BQ24725_VCC
BQ24725_ACP
BQ24725_ACN
BQ24725_CMSRC
BQ24725_ACDET
BQ24725_ACOK
BQ24725_ILIM
DL_CHG
CSOP
CSON
PR115
PR116
PC124
0.1U_0603_16V7K
Remember to change PC124 from SE000006S80
to SE025104K80 (2011-02-22)
+3VALW
PR117
10K_0402_1%
PR118
10K_0402_1%
<31,43> ACIN
Pre_chg
PR119
316K_0402_1%
PR120
255K_0402_1%
PD7
P_RB751V-40_SOD323-2
PR121
100K_0402_1%
PC125
0.01U_0402_25V7K
PR122
154K_0402_1%
PC126
0.1U_0402_25V6
PR123
66.5K_0402_1%
PC127
100P_0402_50V8J
PR124
0_0402_5%
PC131
100P_0402_50V8J
EC_SMB_CK1 <43,47>
EC_SMB_DA1 <43,47>
ADP_I <43,47>
Please locate the RC
Near EC chip
2011-02-22
Vin Dectector
Min. Typ Max.
H-->L 17.23V
L--> H 17.63V
ILIM and external DPM
3.97A
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2011/12/03
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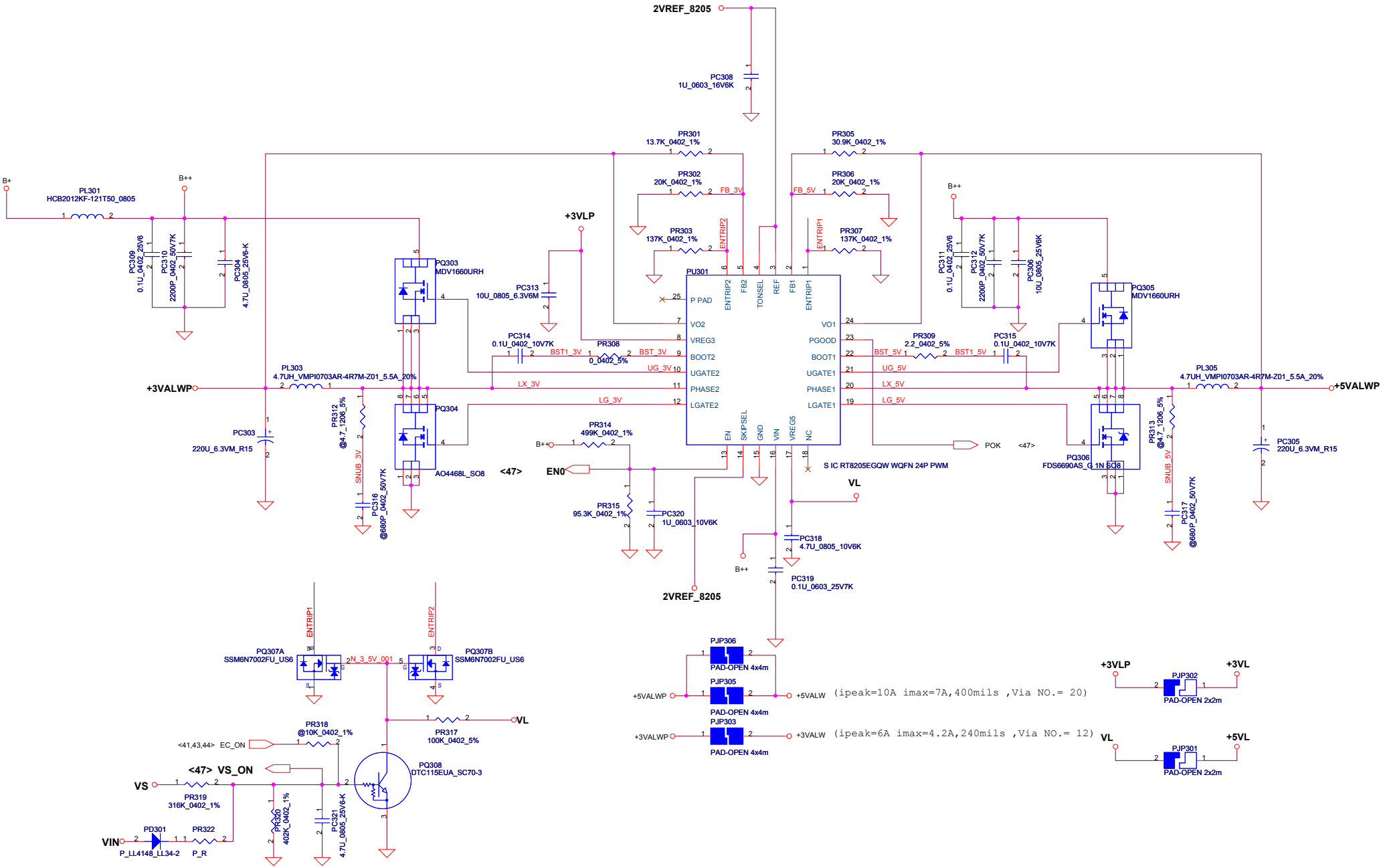
Compal Electronics, Inc.
Title
PWR DCIN / Pre-charge
Size
Custom
Document Number
LA-7221P
Rev
0.3
Date:
Monday, April 11, 2011
Sheet
48
of
59



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

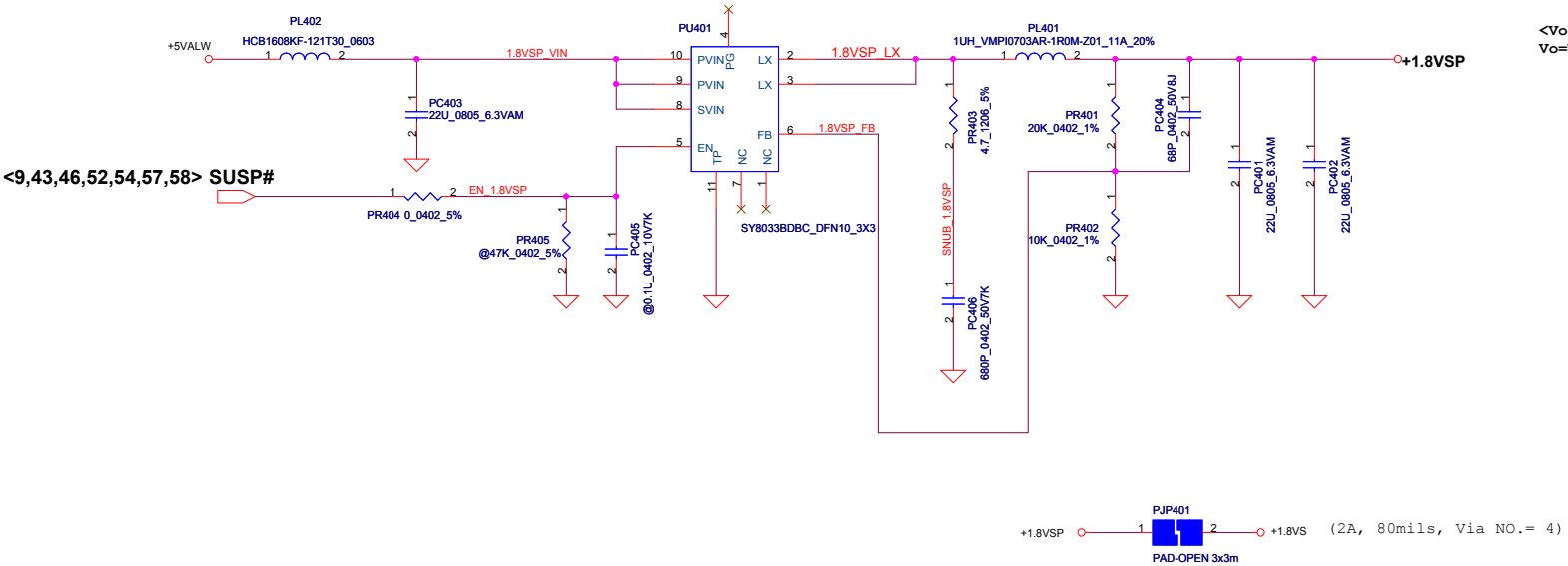
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
Custom	PBL21 LA6771P M/B	0.3

Date: Monday, April 11, 2011 | Sheet 49 of 59



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2A, 80mils, Via NO.= 4)

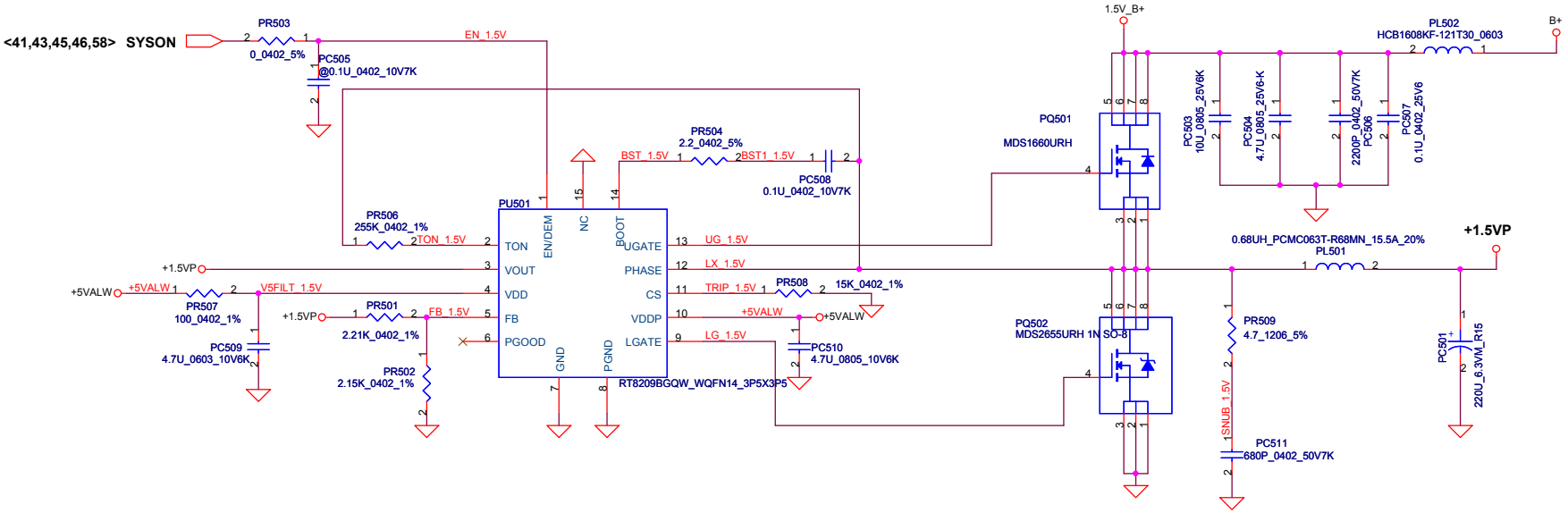
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.3

Date: Monday, April 11, 2011 | Sheet 50 of 59



(Ipeak = 30A Imax= 21A , 1200mils ,Via NO.= 6

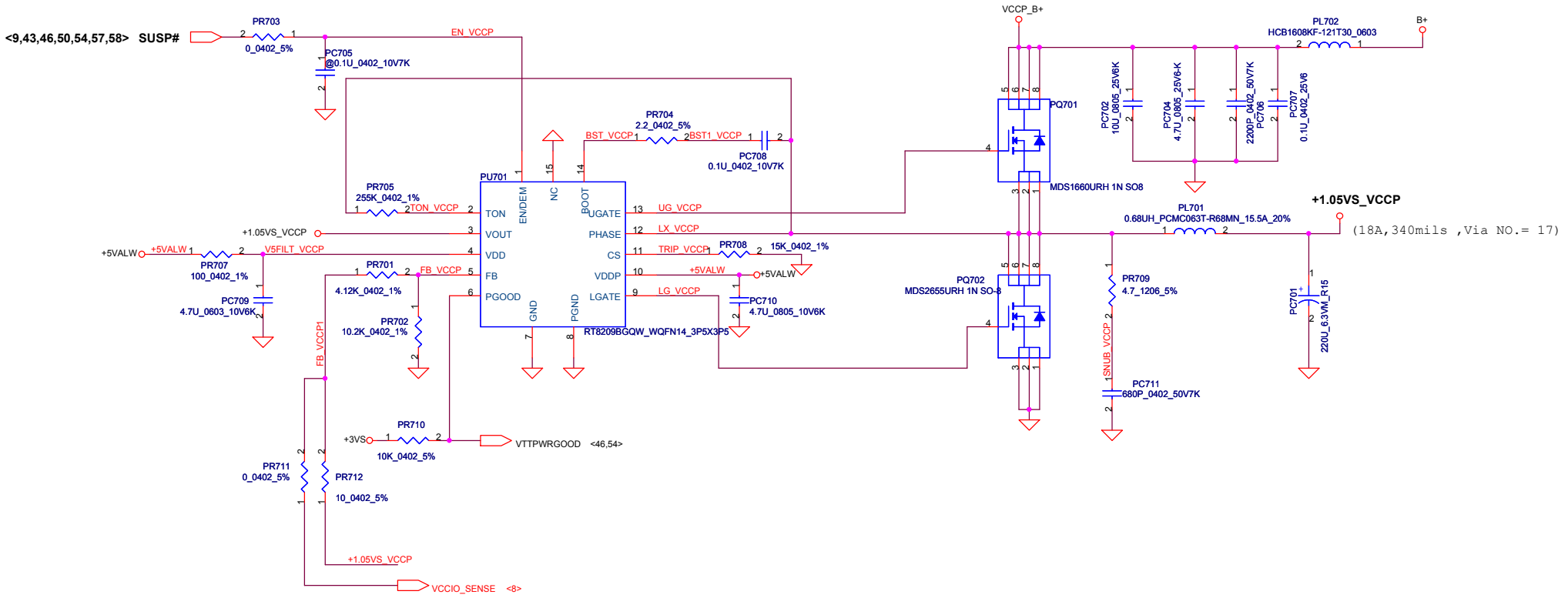
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	PBL21 LA6771P M/B	0.3

Date: Monday, April 11, 2011 | Sheet 51 of 59



VSSIO_SENSE connect to GND directly.

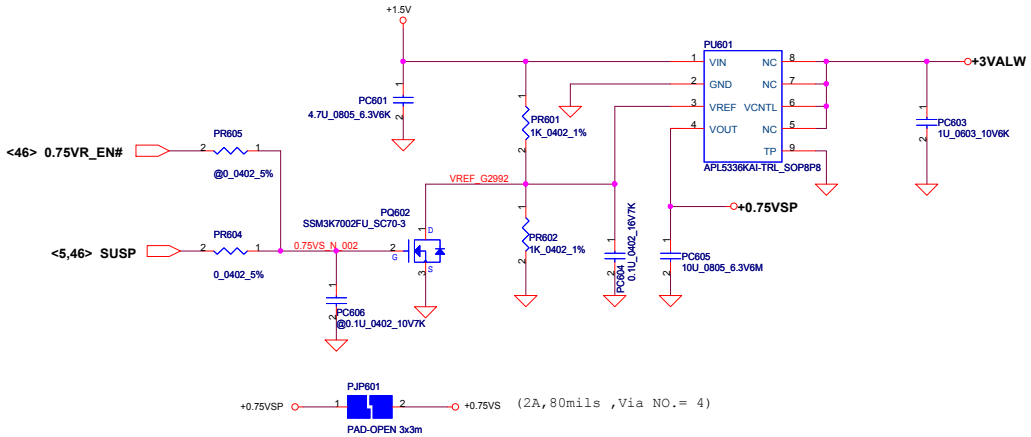
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: PWR+1.05VSP/+VCCPP

Size: Custom | Document Number: PBL21 LA6771P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 52 of 59



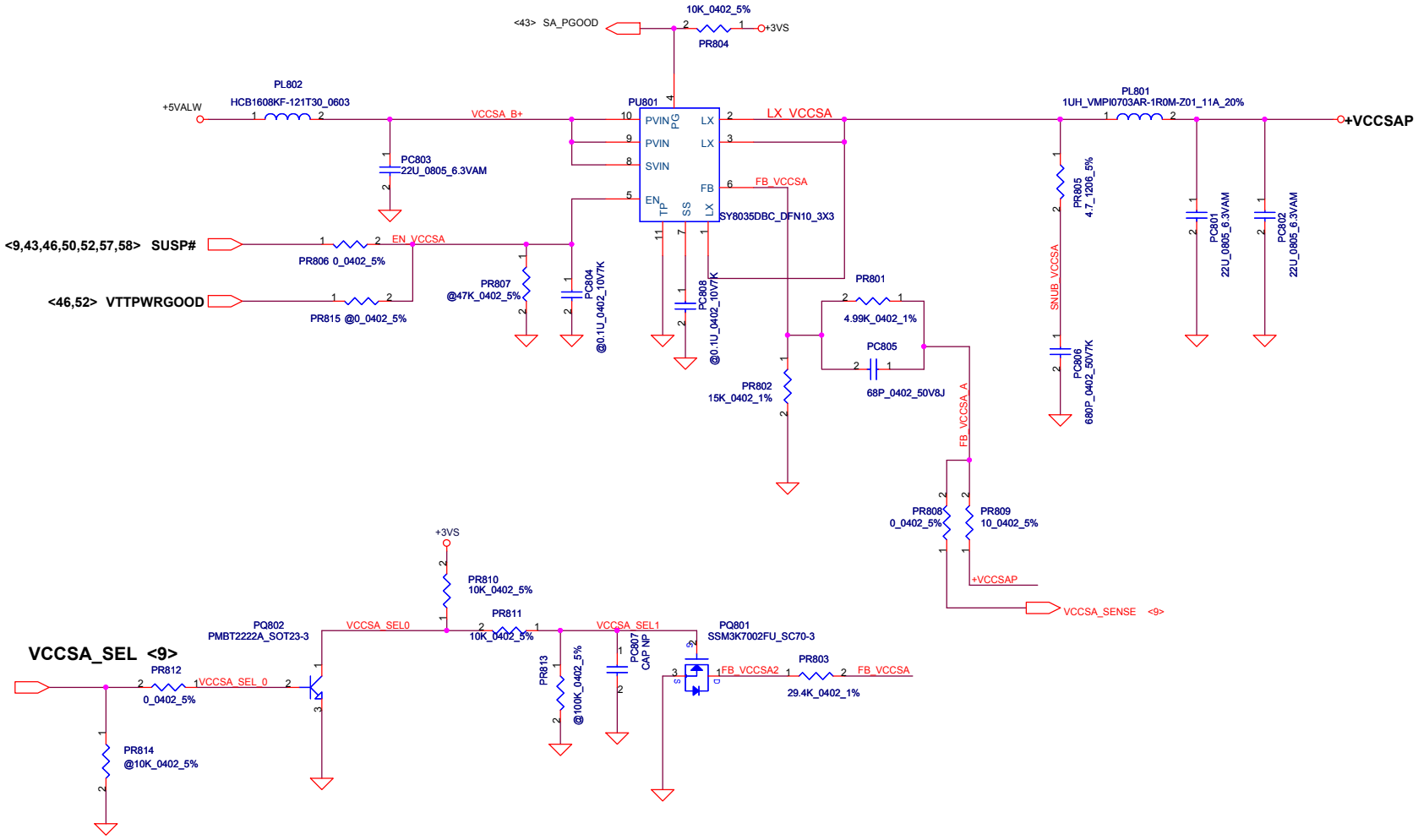
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2011/12/03

Compal Electronics, Inc.

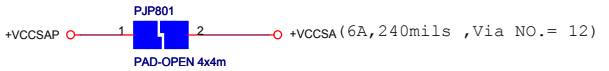
Title: 0.75VSP/1.2VSP

Size | Document Number: PBL21 LA6771P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 53 of 59



VCCSA_SEL	VCCSA Vout
0	0.9V
1	0.8V



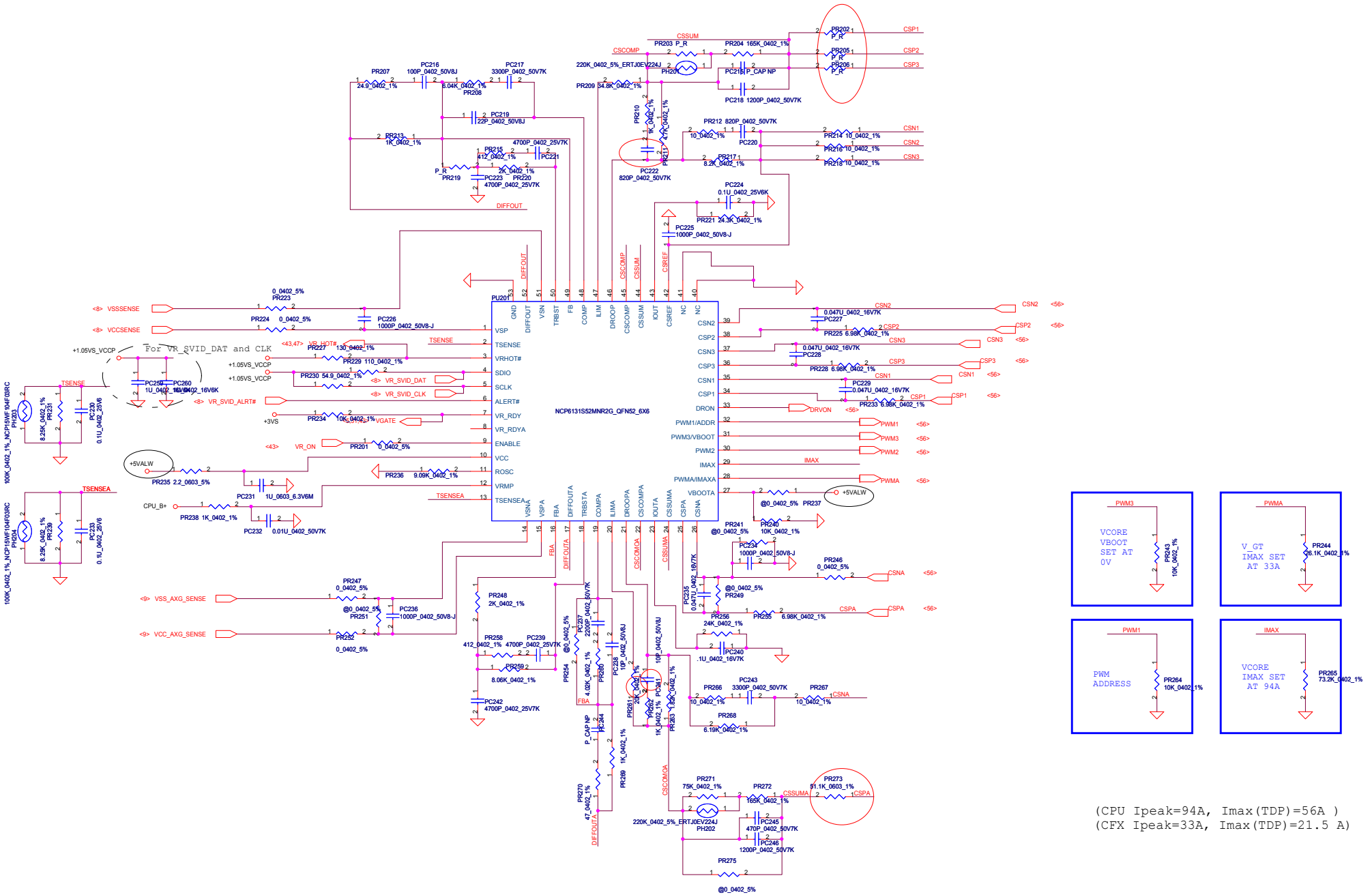
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: PWR+VCCSAP

Size: Custom | Document Number: PBL21 LA6771P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 54 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2011/12/03

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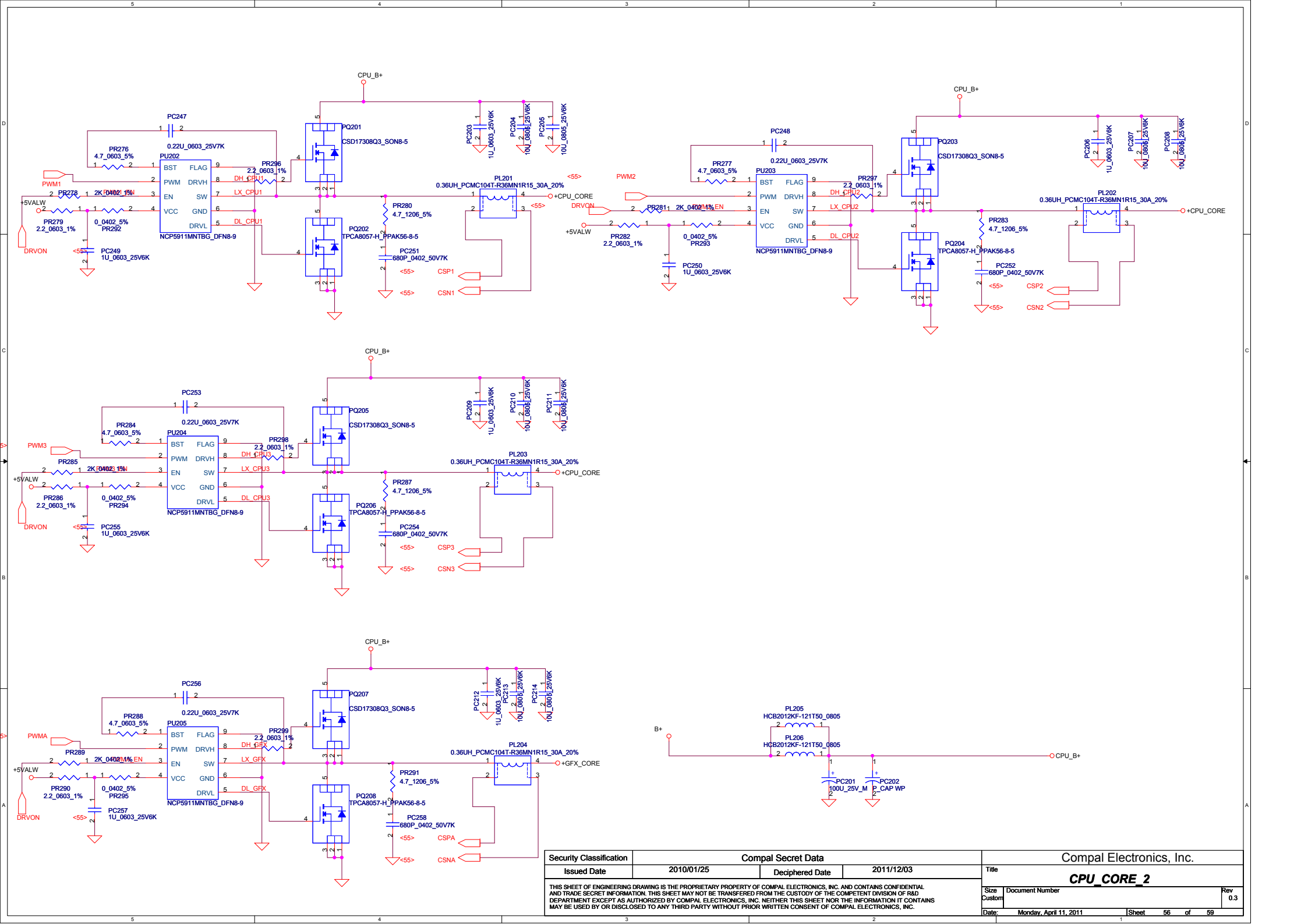
Title	CPU_CORE_1		
Size	Document Number		Rev
C	PCA60/70 LA-7001P M/B		0.3
Date:	Monday, April 11, 2011	Sheet	55 of 59



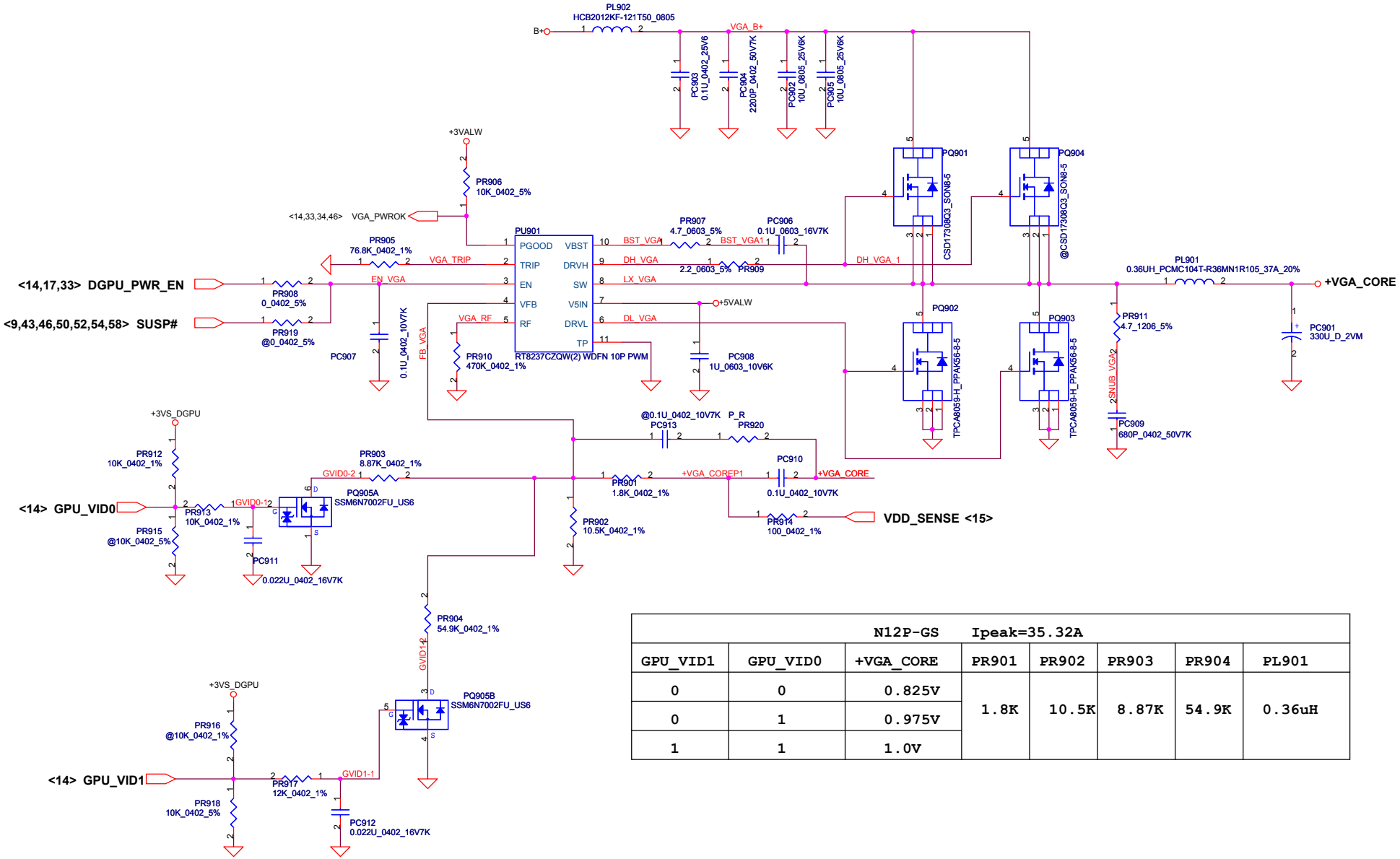
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: **CPU_CORE_2**

Size	Document Number	Rev
Custom		0.3

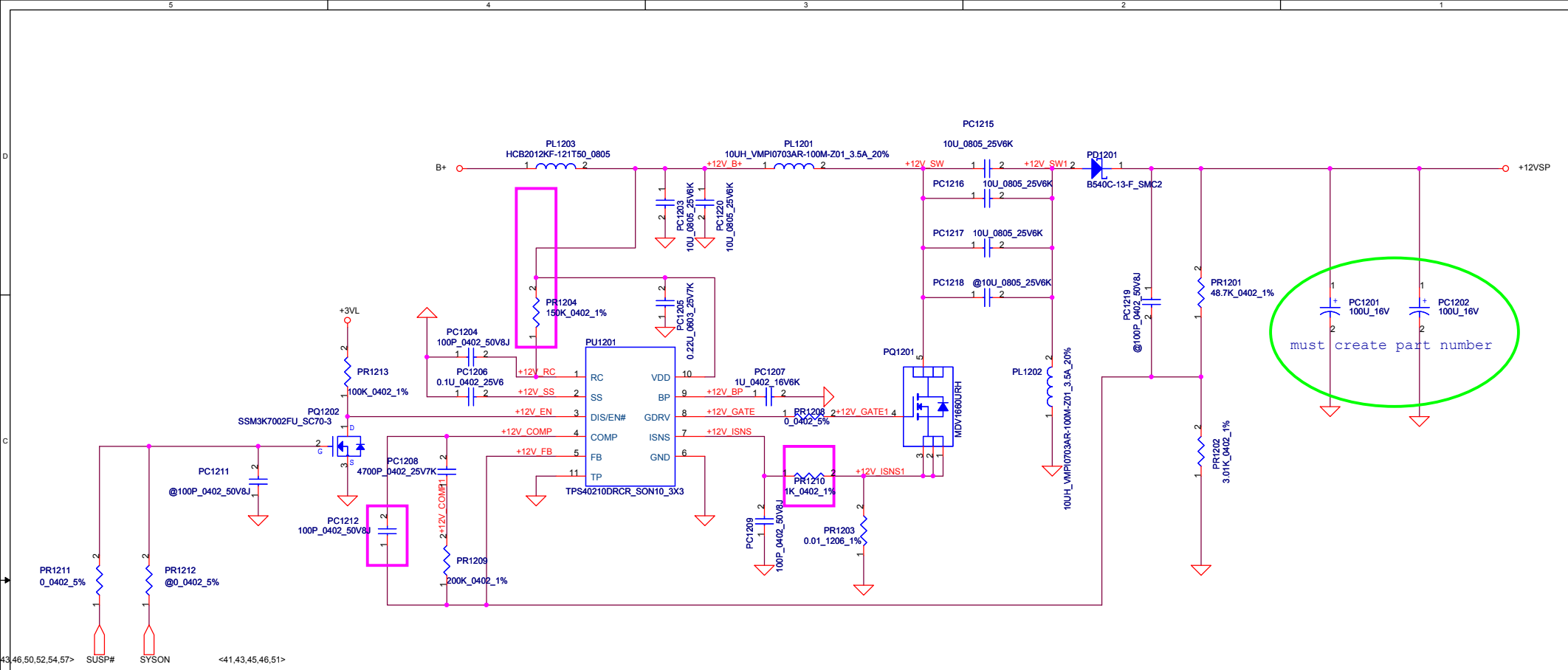
Date: Monday, April 11, 2011 | Sheet 56 of 59



N12P-GS Ipeak=35.32A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.825V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	0.975V					
1	1	1.0V					

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2011/12/03

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size	Document Number	PBL21 LA6771P M/B	Rev 0.3
Date: Monday, April 11, 2011	Sheet 57 of 59		



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/03

Compal Electronics, Inc.		
Title: PWR+12V_SEPIC		
Size: Custom	Document Number: PBL21 LA6771P M/B	Rev: 0.3
Date: Monday, April 11, 2011	Sheet 58 of 59	

PIR (Product Improve Record)

PBL80 LA-7441P SCHEMATIC CHANGE LIST
REVISION CHANGE:

Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	02/18	43	Change R392 to 330K	For Compal common design
2	02/18	39	Delete U10,R400,R401,C331,C332	Change LID SW to USB small board.
3	02/24	45	Change D23 to D23 and D7	
4	02/25	12	Add C202,C208,C216,C218	Add 0.1U X4 for EMI request.
5	02/25	43	Add R431,C406	Add RC for EMI request.
6	03/02	39	Add L22,L23,L23,R183,R214,R216,R218,R222,R224	For EMI request.
7	03/02	43	Add R391	For EC request.
8	03/02	28	Add C319	For ESD request.
9	03/02	28	Add C500,C501	For ESD request.
10	03/02	41	Add R433,C421	For EMI request.
11	03/02	41	Add R1553,C402	For HW test.
12	03/02	43	Add C308	For ESD request.
13	03/02	43	Delete R409	For HW no need.
14	03/02	44	Add C407,C408,C409,C420	For ESD request.
15	03/02	44	Delete C333,R406	For ESD request.

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	03/21	5	Add C55	For ESD request.
2	03/21	43	Add C323	For ESD request.
3	03/31	44	Add C307,C324	For ESD request.
4	04/06	5	Add C56,C57	For ESD request.
5	04/06	5	Add C327	For ESD request.

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: HW-PIR

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.3

Date: Monday, April 11, 2011 | Sheet 59 of 59