Compal Confidential

PBL60 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

2010-02-15

REV:1.0

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title	P01-Cover Page	
Size B	Document Number LA-7322P	Rev 1.0
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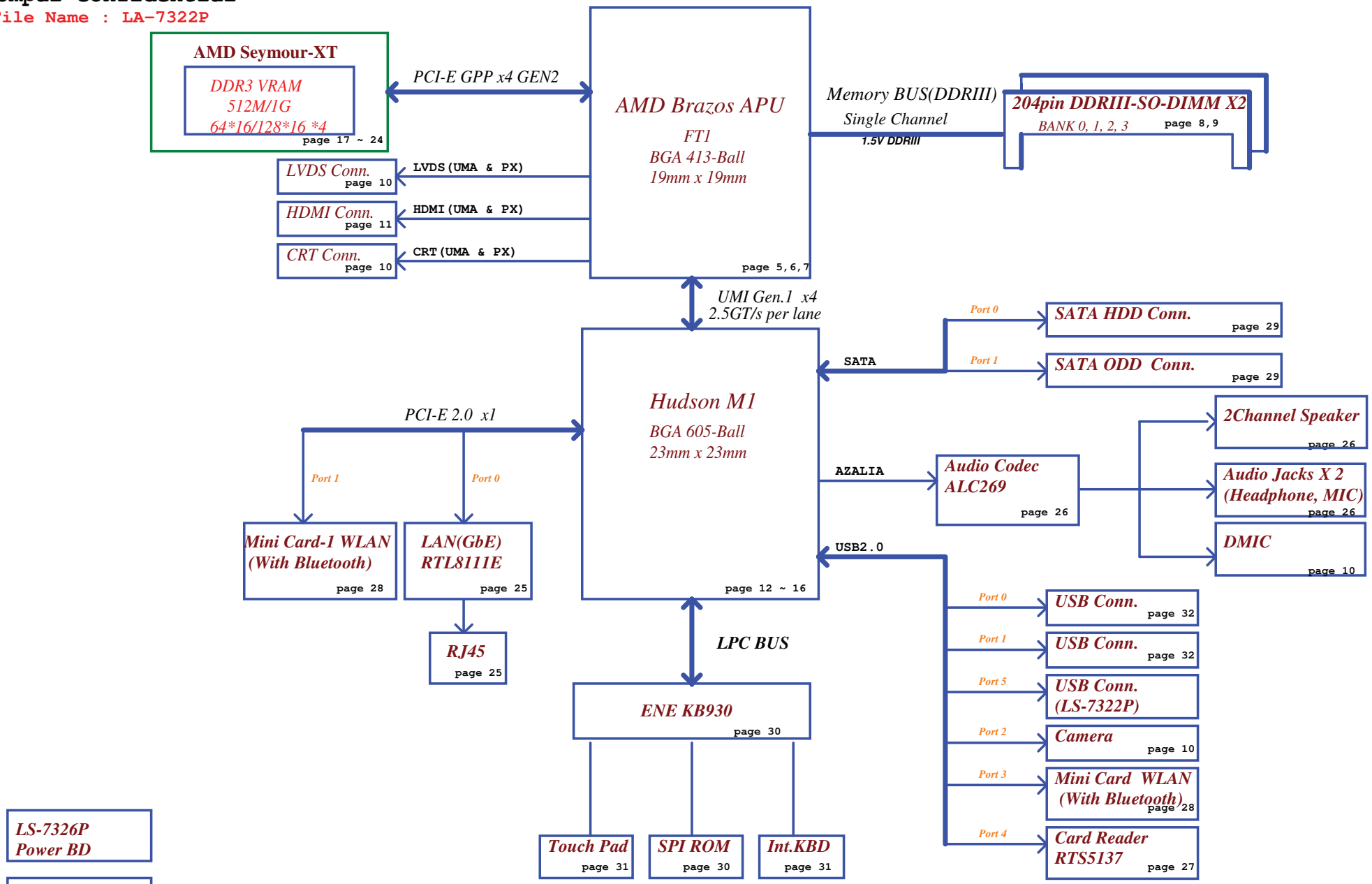

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Compal Electronics, Inc.			
Title	P02-Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH (+3VS)	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	FCH (+3VALW)	X	X	V	X	X	X

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI(WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

BOM Structure

15G@: 1.5G CPU (E240)
16G@: 1.6G CPU (E350)
1G@ : 1G CPU (C50)
UMA@ : APU output.
VGA@ : GPU used.
LS@ : Level shift used.
X76@L01 :VRAM 1G.
X76@L03 :VRAM 512M.

Symbol Note :

: means Digital Ground

: means Analog Ground

L01 : 16G@/VGA@/LS@/X76@L03
L02 : 16G@/UMA@/LS@
L03 : 15G@/VGA@/LS@/X76@L03
L04 : 15G@/UMA@/LS@
L05 : 16G@/VGA@/LS@/X76@L01
L06 : 15G@/VGA@/LS@/X76@L01
L07 : 1G@/VGA@/LS@/X76@L03
L08 : 1G@/UMA@/LS@
L09 : 1G@/VGA@/LS@/X76@L01

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Title: P03-Notes List

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Power-Up/Down Sequence

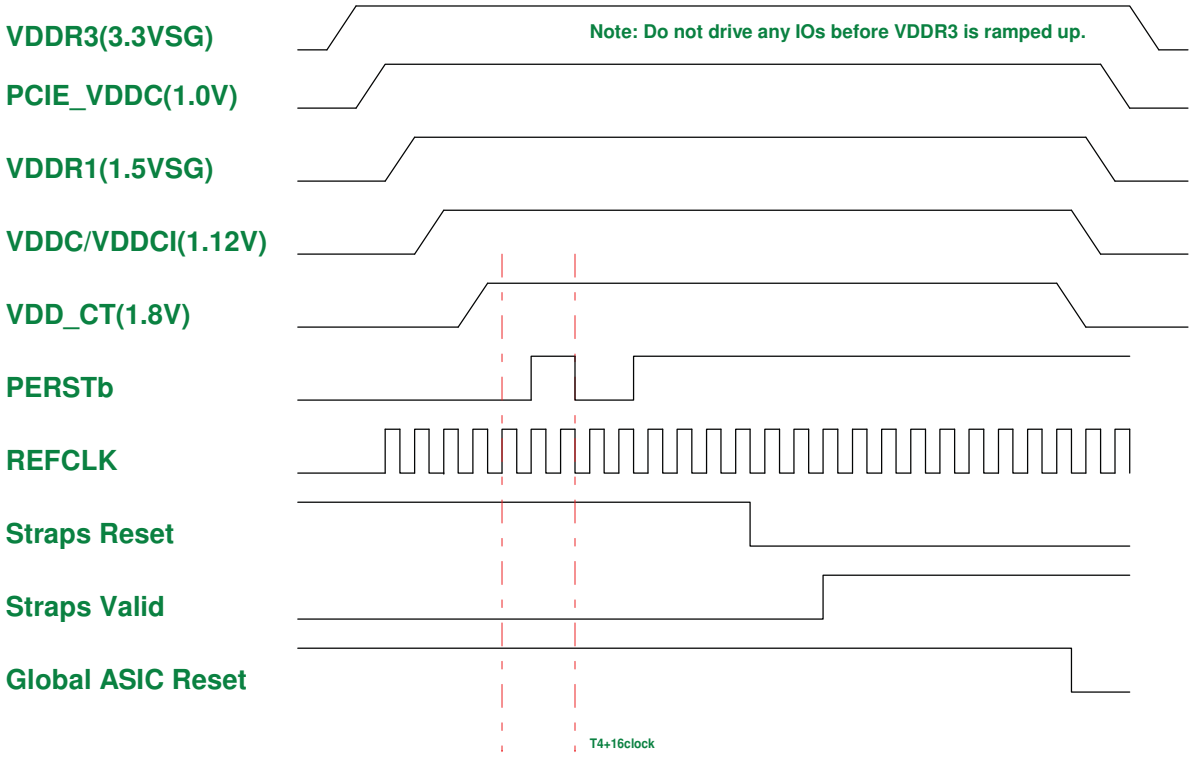
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



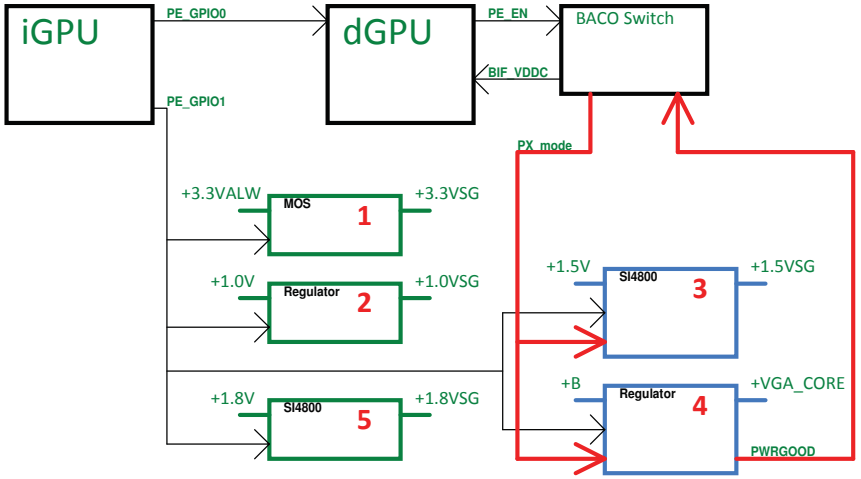
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: P04-dGPU Block Diagram

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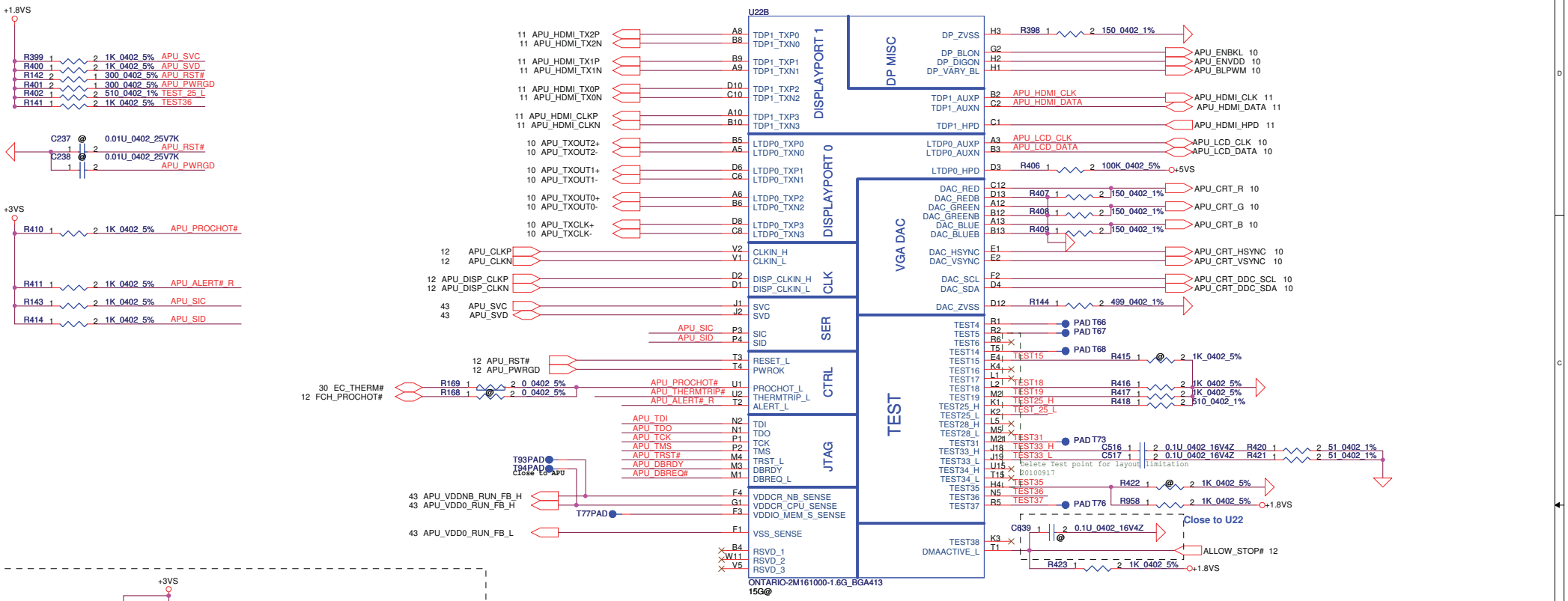
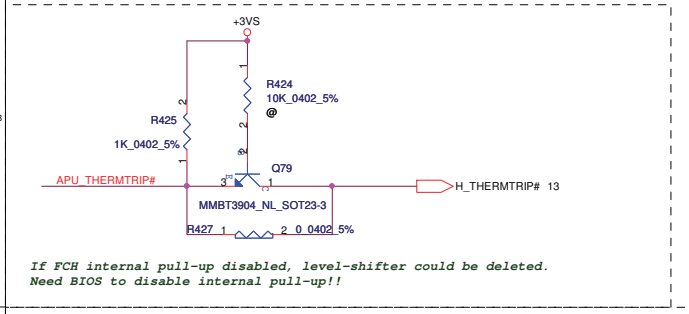
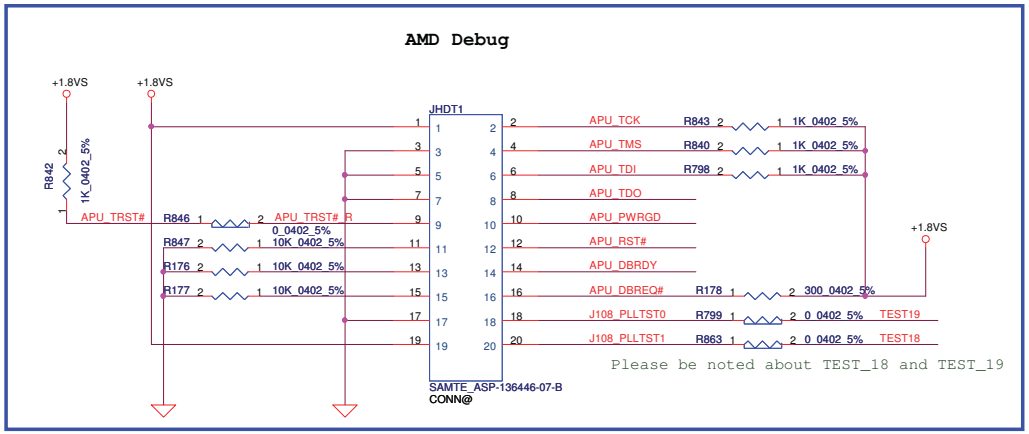
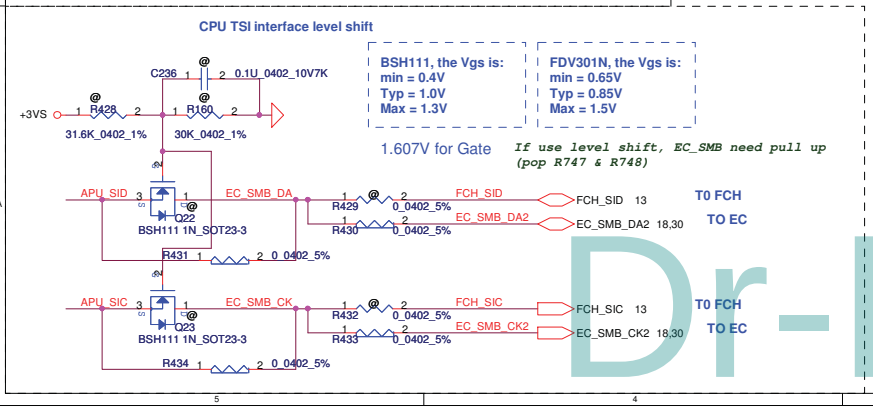




U22 16G@
ZACATE ZM161032B2238 1.6G BGA 413P

U22 1G@
ONTARIO CMC50AFPB22GT 1G





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Compal Electronics, Inc.			
Title	P05-FT1 CTRL/DP/CRT		
Size: Custom	Document Number: LA-7322P		Rev: 1.0
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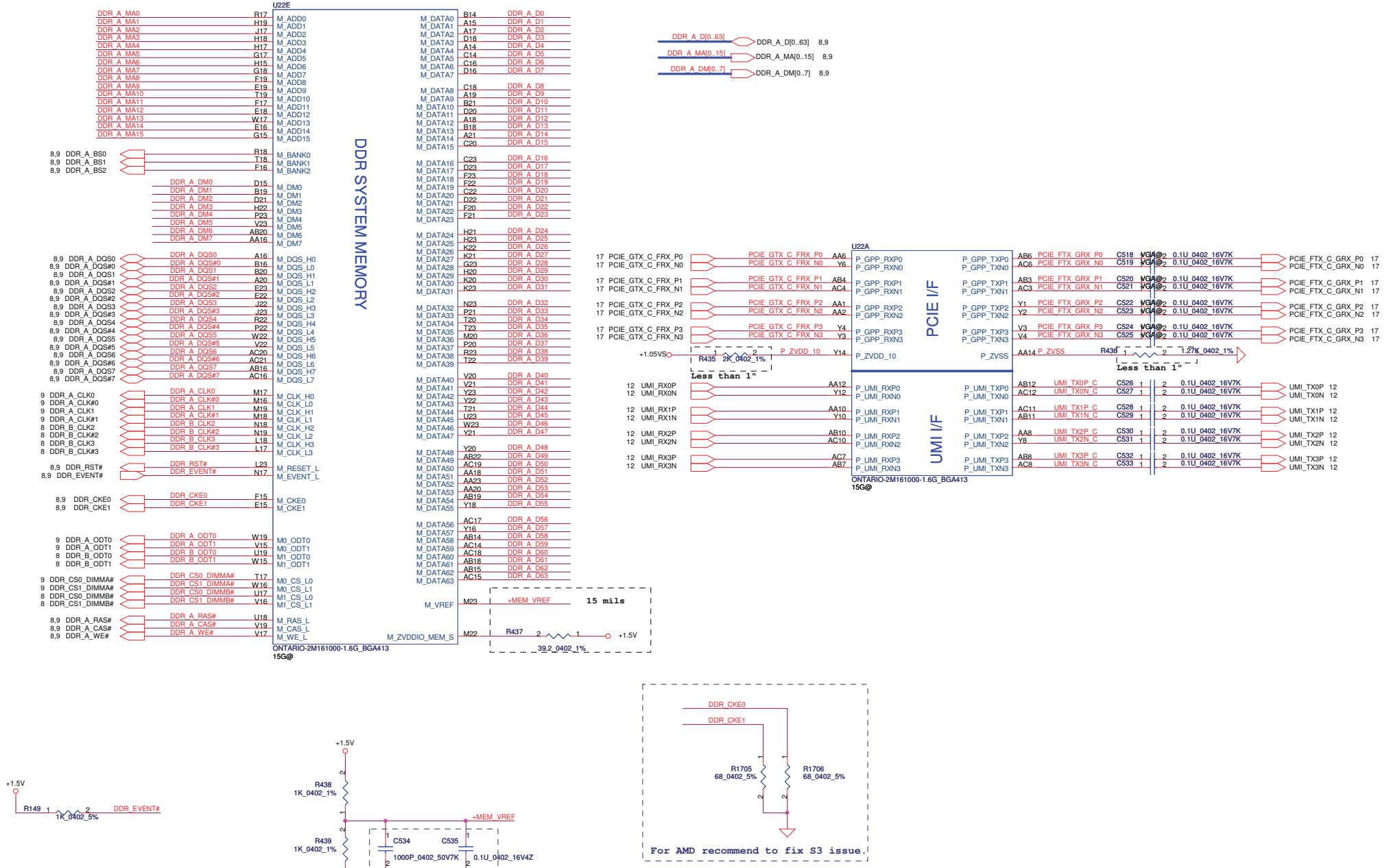

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Compal Electronics, Inc.

Title: P06-FT1 DDRIII/UMI/PCIE

Size	Document Number	Rev
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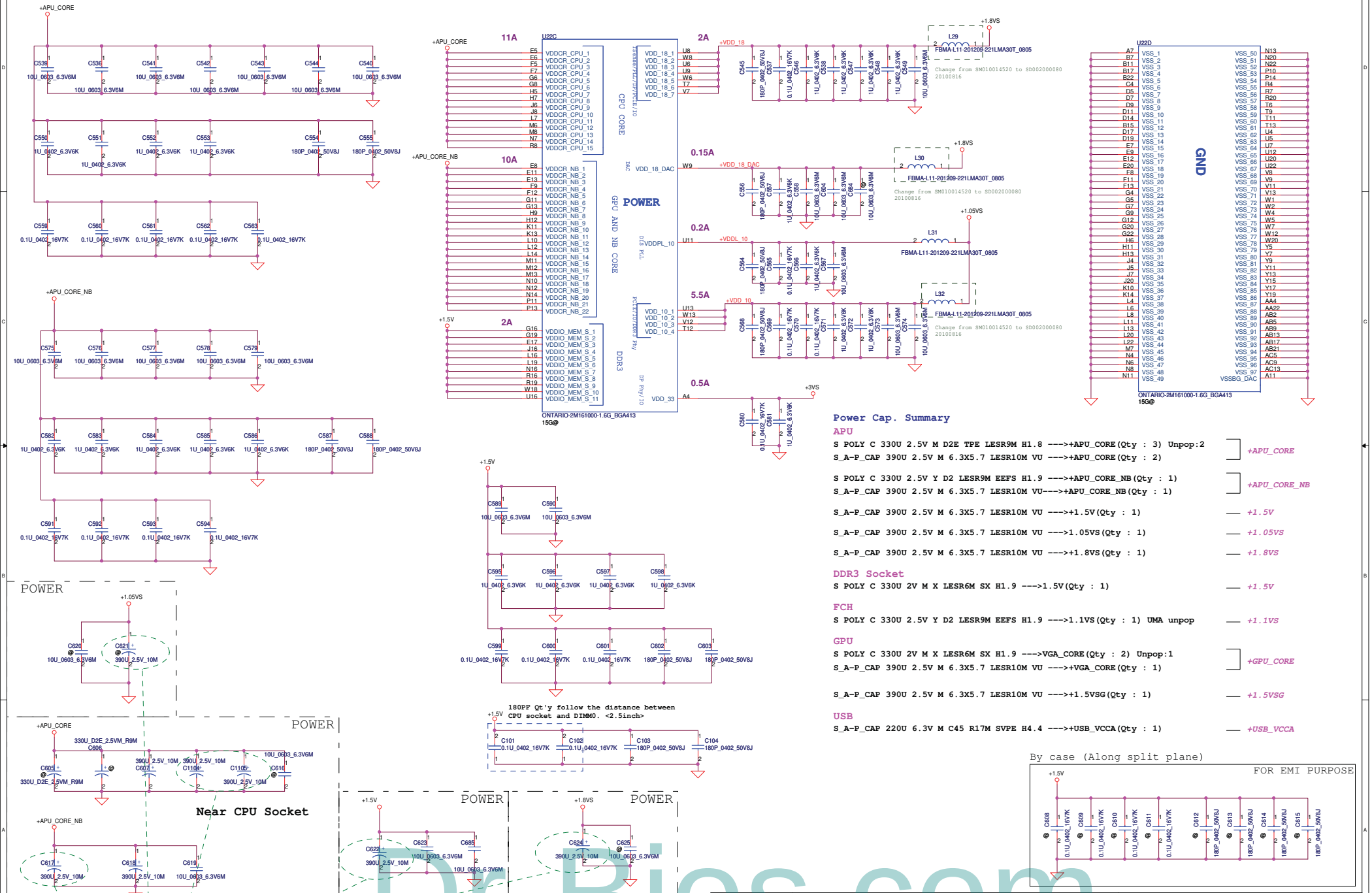

Power Cap. Summary

APU

```
S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 --->+APU_CORE(Qty : 3) Unpop:2
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+APU_CORE(Qty : 2)
```
+APU_CORE

```
S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->+APU_CORE_NB(Qty : 1)
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU--->+APU_CORE_NB(Qty : 1)
```
+APU_CORE_NB

```
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.5V(Qty : 1)
```
+1.5V

```
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->1.05VS(Qty : 1)
```
+1.05VS

```
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.8VS(Qty : 1)
```
+1.8VS

DDR3 Socket

```
S POLY C 330U 2V M X LESR6M SX H1.9 --->1.5V(Qty : 1)
```
+1.5V

FCH

```
S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->1.1VS(Qty : 1) UMA unpop
```
+1.1VS

GPU

```
S POLY C 330U 2V M X LESR6M SX H1.9 --->VGA_CORE(Qty : 2) Unpop:1
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+VGA_CORE(Qty : 1)
```
+GPU_CORE

```
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.5VSG(Qty : 1)
```
+1.5VSG

USB

```
S_A-P_CAP 220U 6.3V M C45 R17M SVPE H4.4 --->+USB_VCCA(Qty : 1)
```
+USB_VCCA

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Compal Electronics, Inc.			
Title	P07-FT1 PWR/VSS		
Size: C	Document Number: LA-7322P		Rev: 1.0
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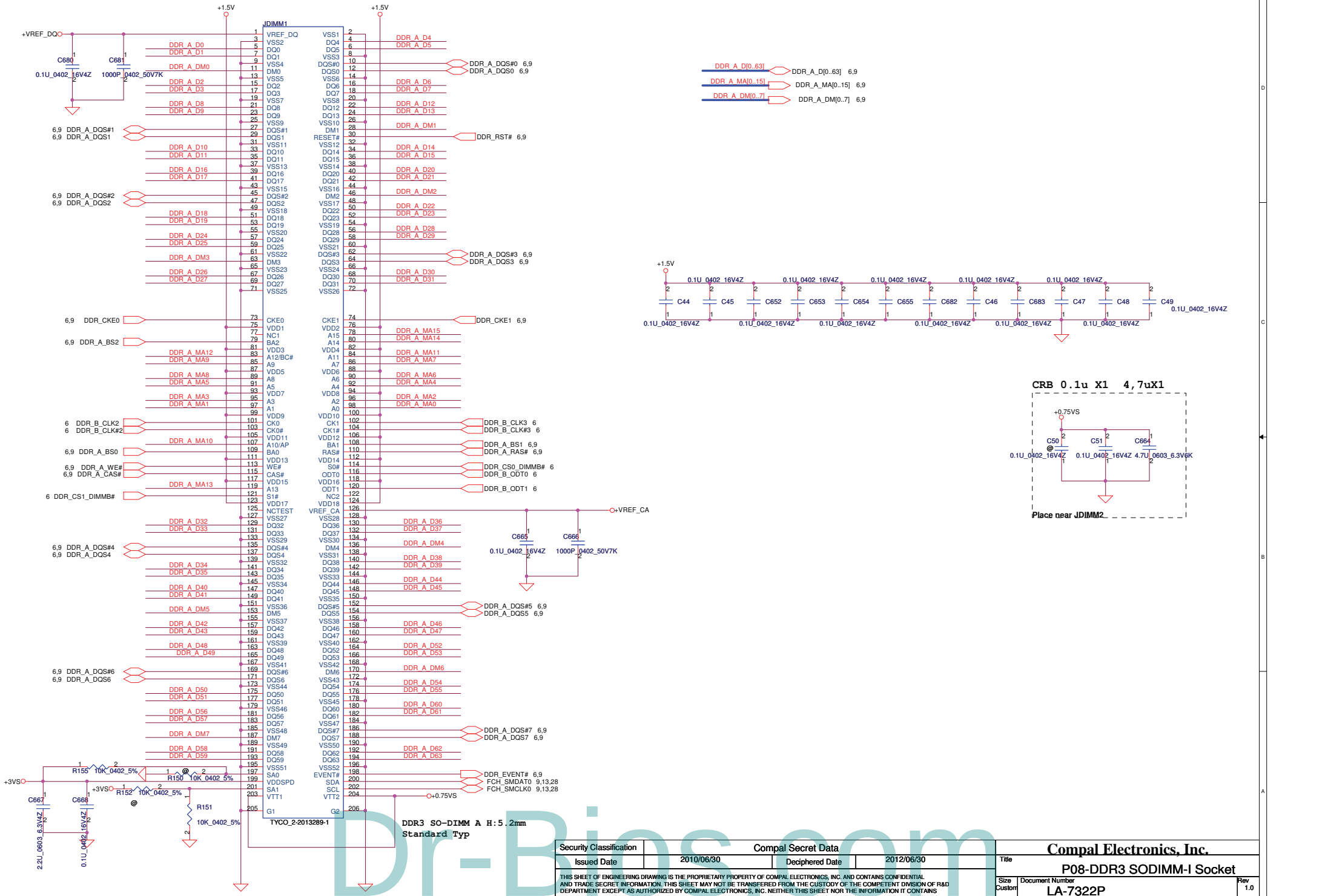

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Title	P08-DDR3 SODIMM-I Socket	
Size: Custom	Document Number: LA-7322P	Rev: 1.0
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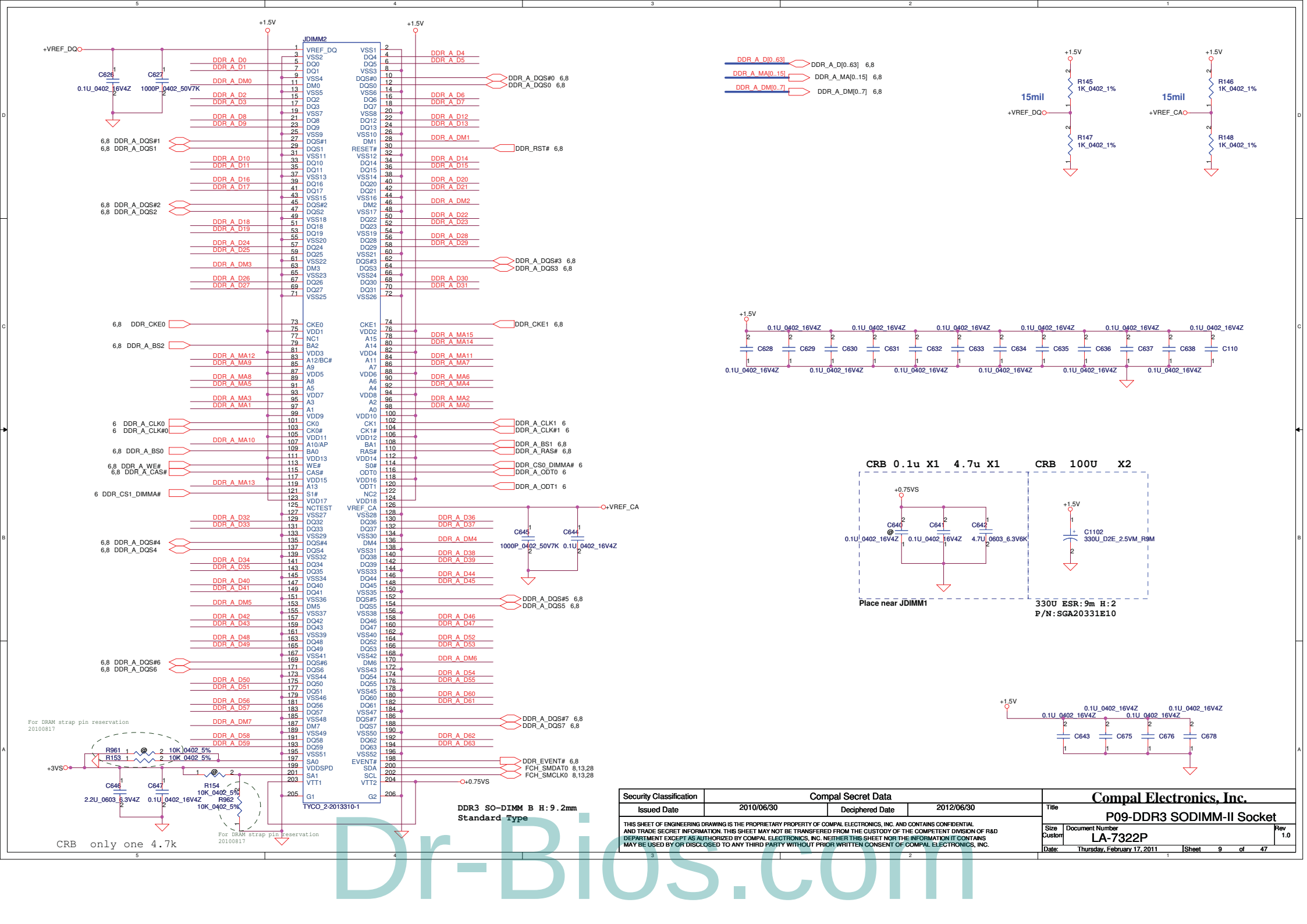

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: P09-DDR3 SODIMM-II Socket

Size	Document Number	Rev
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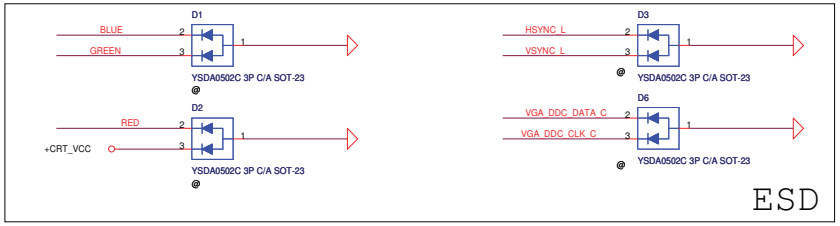
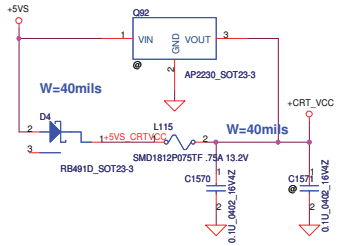
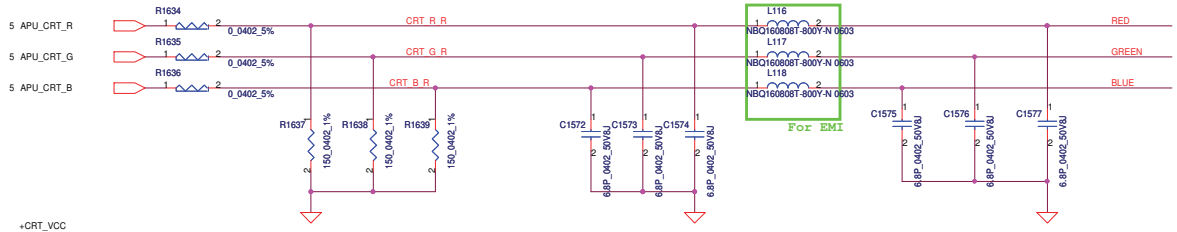
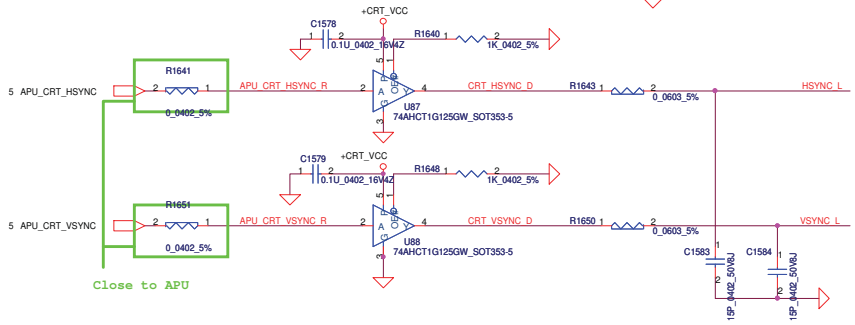
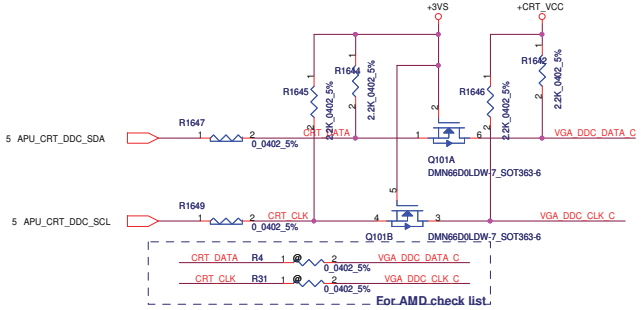
CRT

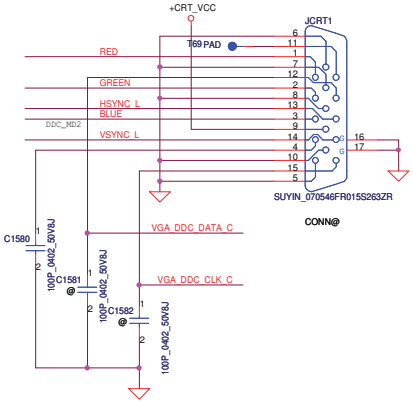




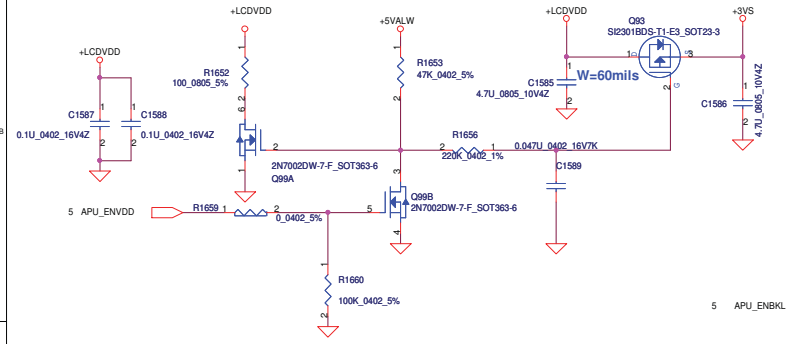


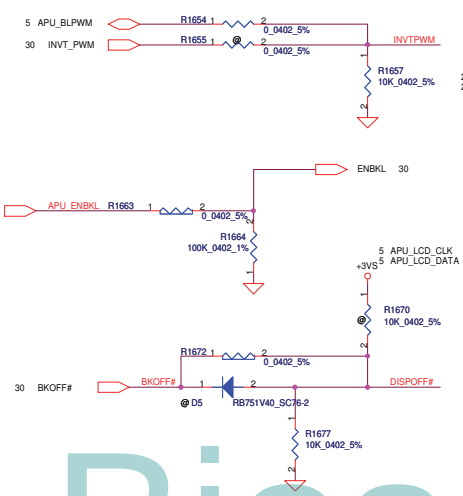


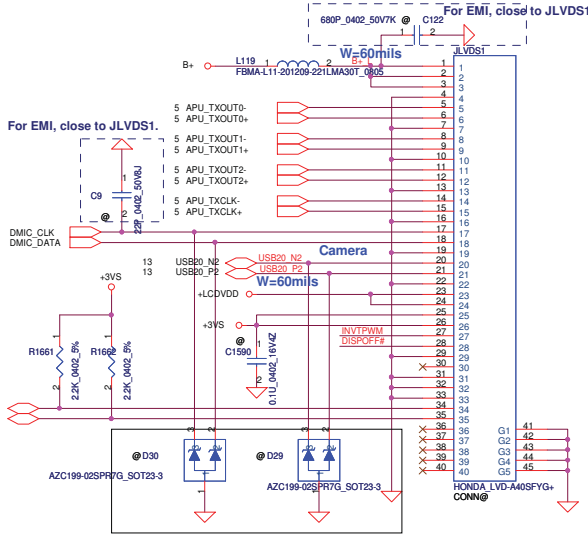




LCD POWER CIRCUIT







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Compal Electronics, Inc.			
Title	P10-LVDS/CRT CONN		
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close to U10VCC (+3VS) pins (one Pin one Capacitor)

+3VS
C1593 0.1U_0402_16V4Z @
C1594 0.1U_0402_16V4Z @
C1595 0.1U_0402_16V4Z @
C1596 0.1U_0402_16V4Z @
C1597 10U_0805_10V4Z-D LS@
C1598 0.1U_0402_16V4Z LS@
C1599 0.1U_0402_16V4Z LS@
C1600 0.1U_0402_16V4Z LS@

+3VS
R202 2.2K_0402_5%
R205 2.2K_0402_5%
APU_HDMI_CLK
APU_HDMI_DATA

+HDMI_5V_OUT
R200 2.2K_0402_5%
R201 2.2K_0402_5%
SCLK
SDATA
R200, R201 place near JHDMI connect

Q94 AP2230_SOT23-3
+5VS → VIN, GND, VOUT → +HDMI_5V_OUT

+5VS
C1591 1U_0603_10V6K
Q95 SI3456BDV-T1-E3 1N TSOP6
+HDMI_5V
W=40mils
F2 0.5A_15V_SMD1812P050TF
+HDMI_5V_OUT
C1592 1U_0603_10V6Z

+VSB
R1678 470K_0402_5%
EN_HDMI
Q96 SSM3K7002FU_SC70-3
R1679 1.5M_0402_5%
C1601 0.1U_0402_16V7K

5 APU_HDMI_CLKP
5 APU_HDMI_CLKN
C1602 0.1U_0402_16V7K HDMI_CLK
C1603 0.1U_0402_16V7K HDMI_CLK#

5 APU_HDMI_TX0P
5 APU_HDMI_TX0N
C1604 0.1U_0402_16V7K HDMI_TX0
C1605 0.1U_0402_16V7K HDMI_TX0#

5 APU_HDMI_TX1P
5 APU_HDMI_TX1N
C1606 0.1U_0402_16V7K HDMI_TX1
C1607 0.1U_0402_16V7K HDMI_TX1#

5 APU_HDMI_TX2P
5 APU_HDMI_TX2N
C1608 0.1U_0402_16V7K HDMI_TX2
C1609 0.1U_0402_16V7K HDMI_TX2#

+3VS
R1701 10K_0402_5%
HDMI_HPD_R#
HDMI_HPD_R
Q84 SSM3K7002FU_SC70-3
34,41 SUSP

5V PULL UP IN CONNECTER SIDE

HDMI_CLK#_L R208 0_0402_5% HDMI_R_CLK#
HDMI_CLK_L R210 0_0402_5% HDMI_R_CLK

Swap signal for layout route.

HDMI_TX0_L R211 0_0402_5% HDMI_R_TX0
HDMI_TX0#_L R213 0_0402_5% HDMI_R_TX0#

HDMI_TX1_L R214 0_0402_5% HDMI_R_TX1
HDMI_TX1#_L R220 0_0402_5% HDMI_R_TX1#

HDMI_TX2_L R223 0_0402_5% HDMI_R_TX2
HDMI_TX2#_L R226 0_0402_5% HDMI_R_TX2#

U89 ASM1442 QFN 48P

+3VS → VCC3V ×9
R1736 4.7K_0402_5%
R1685 4.7K_0402_5%
R1737 4.7K_0402_5%
R1687 4.7K_0402_5%
R1689 3.6K_0402_1%
FUNCTION1
FUCNTION2
ANALOG1(REXT)
5 APU_HDMI_HPD → APU_HDMI_HPD → HPD_SOURCE
5 APU_HDMI_DATA → APU_HDMI_DATA → SDA_SOURCE
5 APU_HDMI_CLK → APU_HDMI_CLK → SCL_SOURCE
R1692 4.7K_0402_5%
R1694 4.7K_0402_5%
ANALOG2

HDMI_R_CLK / HDMI_R_CLK# → OUT_D4+ / OUT_D4-
HDMI_R_TX2 / HDMI_R_TX2# → OUT_D3+ / OUT_D3-
HDMI_R_TX1 / HDMI_R_TX1# → OUT_D2+ / OUT_D2-
HDMI_R_TX0 / HDMI_R_TX0# → OUT_D1+ / OUT_D1-

Trace AS Short PASS

GND ×10

OE* ← HDMI_HPD_R#
SCL_SINK ← SCLK
SDA_SINK ← SDATA
HPD_SINK → HDMI_HPD_R
DDC_EN
R1684 4.7K_0402_5% +3VS
R1703 4.7K_0402_5% +3VS
FUNCTION3
FUNCTION4
R1686 4.7K_0402_5%
R1688 4.7K_0402_5%
R1707 4.7K_0402_5% +3VS

IN_D4+ / IN_D4- ← HDMI_CLK / HDMI_CLK#
R204 2.2K_0402_5%
IN_D3+ / IN_D3- ← HDMI_TX2 / HDMI_TX2#
IN_D2+ / IN_D2- ← HDMI_TX1 / HDMI_TX1#
IN_D1+ / IN_D1- ← HDMI_TX0 / HDMI_TX0#
THERMAL_GND

+HDMI_5V_OUT
HDMI_HPD_R
R1704 100K_0402_5%
JHDMI1 SUYIN_100042MR019S153ZL
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK- / CK_shield / CK+ / D0- / D0_shield / D0+ / D1- / D1_shield / D1+ / D2- / D2_shield / D2+
GND ×4

D11 L15ESDL5V0NA-4 SLP2510P8
HDMI_R_TX1 / HDMI_R_TX1#
HDMI_R_TX0 / HDMI_R_TX0#

D13 L15ESDL5V0NA-4 SLP2510P8
HDMI_R_TX2 / HDMI_R_TX2#
HDMI_R_CLK / HDMI_R_CLK#

For ESD request.

D16 AZC099-04S.R7G_SOT23-6
HDMI_HPD_R → SDATA
+5VS
+HDMI_5V_OUT → SCLK

For ESD request.

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P11-HDMI CONN

Size: Custom | Document Number: LA-7322P | Rev: 1.0

Date: Thursday, February 17, 2011 | Sheet 11 of 47

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

U31E

PCI EXPRESS I/F

PCIE_RST# P1 / A_RST# L1 → PCIE_RST_L / A_RST_L

30 A_RST#

UMI_RX0P AD26 / UMI_RX0N AD27 / UMI_RX1P AC28 / UMI_RX1N AC29 / UMI_RX2P AB29 / UMI_RX2N AB28 / UMI_RX3P AB26 / UMI_RX3N AB27
C53 0.1U_0402_16V7K UMI_RX0P_C
C54 0.1U_0402_16V7K UMI_RX0N_C
C55 0.1U_0402_16V7K UMI_RX1P_C
C56 0.1U_0402_16V7K UMI_RX1N_C
C57 0.1U_0402_16V7K UMI_RX2P_C
C58 0.1U_0402_16V7K UMI_RX2N_C
C59 0.1U_0402_16V7K UMI_RX3P_C
C60 0.1U_0402_16V7K UMI_RX3N_C

UMI_TX0P AE24 / UMI_TX0N AE23 / UMI_TX1P AD25 / UMI_TX1N AD24 / UMI_TX2P AC24 / UMI_TX2N AC25 / UMI_TX3P AB25 / UMI_TX3N AB24

+PCIE_VDDAN
R560 590_0402_1%
R561 2K_0402_1%
PCIE_CALRP AD29 / PCIE_CALRN AD28

LAN / WLAN

25 PCIE_FTX_C_DRX_P0 C61 0.1U_0402_16V7K PCIE_FTX_DRX_P0 AA28
25 PCIE_FTX_C_DRX_N0 C62 0.1U_0402_16V7K PCIE_FTX_DRX_N0 AA29
28 PCIE_FTX_C_DRX_P1 C717 0.1U_0402_16V7K PCIE_FTX_DRX_P1 Y29
28 PCIE_FTX_C_DRX_N1 C63 0.1U_0402_16V7K PCIE_FTX_DRX_N1 Y28

GPP_TX0P Y26 / GPP_TX0N Y27 / GPP_TX1P W28 / GPP_TX1N W29 / GPP_TX2P AA22 / GPP_TX2N Y21 / GPP_TX3P AA25 / GPP_TX3N AA24

25 PCIE_FRX_DTX_P0 / 25 PCIE_FRX_DTX_N0 / 28 PCIE_FRX_DTX_P1 / 28 PCIE_FRX_DTX_N1

GPP_RX0P W23 / GPP_RX0N V24 / GPP_RX1P W24 / GPP_RX1N W25 / GPP_RX2P AB22 / GPP_RX2N AB21 / GPP_RX3P AA20 / GPP_RX3N AA19

CLOCK GENERATOR

close to FCH within 1"

PCIE_RCLKP/NB_LNK_CLKP M23 / PCIE_RCLKN/NB_LNK_CLKN P23

5 APU_DISP_CLKP R564 0_0402_5% APU_DISP_CLKP_R U29 → NB_DISP_CLKP
5 APU_DISP_CLKN R565 0_0402_5% APU_DISP_CLKN_R U28 → NB_DISP_CLKN

NB_HT_CLKP T26 / NB_HT_CLKN T27

5 APU_CLKP R162 0_0402_5% APU_CLKP_R V21 → CPU_HT_CLKP
5 APU_CLKN R163 0_0402_5% APU_CLKN_R T21 → CPU_HT_CLKN

17 CLK_PCIE_VGA R569 0_0402_5% CLK_PCIE_VGA_R V23 → SLT_GFX_CLKP
17 CLK_PCIE_VGA# R570 0_0402_5% CLK_PCIE_VGA#_R T23 → SLT_GFX_CLKN

LAN / WLAN

25 CLK_PCIE_LAN R571 0_0402_5% CLK_PCIE_LAN_R L29 → GPP_CLK0P
25 CLK_PCIE_LAN# R572 0_0402_5% CLK_PCIE_LAN#_R L28 → GPP_CLK0N

28 CLK_PCIE_MINI1 R573 0_0402_5% CLK_PCIE_MINI1_R N29 → GPP_CLK1P
28 CLK_PCIE_MINI1# R574 0_0402_5% CLK_PCIE_MINI1#_R N28 → GPP_CLK1N

GPP_CLK2P M29 / GPP_CLK2N M28
GPP_CLK3P T25 / GPP_CLK3N V25
GPP_CLK4P L24 / GPP_CLK4N L23
GPP_CLK5P P25 / GPP_CLK5N M25
GPP_CLK6P P29 / GPP_CLK6N P28
GPP_CLK7P N26 / GPP_CLK7N N27
GPP_CLK8P T29 / GPP_CLK8N T28

C66 27_CLK_SD_48M — R655 22_0402_5% — 14M_25M_48M_OSC L25
10P_0402_50V8J
Y3 1M_0603_5% R576
25M_CLK_X1 L26 → 25M_X1
C67 12P_0402_50V8J
25MHZ_12PF_X5H025000FC1H-H
25M_CLK_X2 L27 → 25M_X2

21807-A11-HUDSON-M1_FCBGA605

PCI CLKS

PCICLK0 W2 → PAD T96
PCICLK1/GPO36 W1 → PCI_CLK1 16
PCICLK2/GPO37 W3 → PCI_CLK2 16
PCICLK3/GPO38 W4 → PCI_CLK3 16
PCICLK4/14M_OSC/GPO39 Y1 → PCI_CLK4 16
PCIRST_L V2 → PAD T92

PCI I/F

AD0/GPIO0 AA1 / AD1/GPIO1 AA4 / AD2/GPIO2 AA3 / AD3/GPIO3 AB1 / AD4/GPIO4 AA5 / AD5/GPIO5 AB2 / AD6/GPIO6 AB6 / AD7/GPIO7 AB5 / AD8/GPIO8 AA6 / AD9/GPIO9 AC2 / AD10/GPIO10 AC3 / AD11/GPIO11 AC4 / AD12/GPIO12 AC1 / AD13/GPIO13 AD1 / AD14/GPIO14 AD2 / AD15/GPIO15 AC6 / AD16/GPIO16 AE2 / AD17/GPIO17 AE1 / AD18/GPIO18 AF8 / AD19/GPIO19 AE3 / AD20/GPIO20 AF1

AD21/GPIO21 AG1 — R585 0_0402_5% — PE_GPIO0 17
AD22/GPIO22 AF2
AD23/GPIO23 AE9 → PCI_AD23 16
AD24/GPIO24 AD9 → PCI_AD24 16
AD25/GPIO25 AC11 → PCI_AD25 16
AD26/GPIO26 AF6 → PCI_AD26 16
AD27/GPIO27 AF4 → PCI_AD27 16
AD28/GPIO28 AF3 → VGA_PWRGD_R
AD29/GPIO29 AH2 / AD30/GPIO30 AG2 / AD31/GPIO31 AH3

CBE0_L AA8 / CBE1_L AD5 / CBE2_L AD8 / CBE3_L AA10 / FRAME_L AE8 / DEVSEL_L AB9 / IRDY_L AJ3 / TRDY_L AE7 / PAR AC5 / STOP_L AF5 / PERR_L AE6 / SERR_L AE4 / REQ0_L AE1 / REQ1_L/GPIO40 AH5 / REQ2_L/CLK_REQ8_L/GPIO41 AH4 / REQ3_L/CLK_REQ5_L/GPIO42 AC12

GNT0_L AD12 → PAD T95
GNT1_L/GPO44 AJ5 — R595 0_0402_5% PE_GPIO0
GNT2_L/GPO45 AH6 → PE_GPIO1 23,30
GNT3_L/CLK_REQ7_L/GPIO46 AB12 → PAD T97
CLKRUN_L AB11 — R99 10K_0402_5%
LOCK_L AD7

INTE_L/GPIO32 AJ6 / INTF_L/GPIO33 AG6 / INTG_L/GPIO34 AG4 / INTH_L/GPIO35 AJ4

LPC

LPCCLK0 H24 → R854 2_0_0402_5% → LPC_CLK1 16
LPCCLK1 H25 → R853 2_0_0402_5% → LPC_CLK0 16
R575 2_22_0402_5% → LPC_CLK0_EC 30
R577 2_22_0402_5% → CLK_PCI_DB 28

LAD0 J27 → LPC_AD0 28,30
LAD1 J26 → LPC_AD1 28,30
LAD2 H29 → LPC_AD2 28,30
LAD3 H28 → LPC_AD3 28,30
LFRAME_L G28 → LPC_FRAME# 28,30
LDRQ0_L J25
LDRQ1_L/CLK_REQ6_L/GPIO49 AA18
SERIRQ/GPIO48 AB19 → SERIRQ 30

CPU

ALLOW_LDTSTP/DMA_ACTIVE_L G21 → ALLOW_STOP# 5
PROCHOT_L H21 → FCH_PROCHOT# 5
LDT_PG K19 → APU_PWRGD 5
LDT_STP_L G22
LDT_RST_L J24 → APU_RST# 5

RTC

32K_X1 C1 → RTC_32KHI
32K_X2 C2 → RTC_32KHO
RTCCLK D2 → RTC_CLK → RTC_CLK 16,30
INTRUDER_ALERT_L B2
VDDBT_RTC_G B1 — R864 510_0402_5% W=20mils

C1272 0.1U_0402_16V4Z / C1271 1U_0402_6.3V4Z
for Clear CMOS
CLRP1 SHORT PADS
C1270 0.1U_0402_16V4Z
+RTCVCC
D23 DAN202UT106_SC70-3
R179 1K_0402_5%
+RTCBATT
+CHGRTC

Close to FCH

C64 10P_0402_50V8J
R563 20M_0603_5%
C65 10P_0402_50V8J
Y4 32.768KHZ_7PF_Q13MC1461000100
RTC_32KHI / RTC_32KHO

FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)
FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

+3VALW
C1234 0.1U_0402_16V4Z
A_RST# — R175 33_0402_5% — PLT_RST# 17,25,28
C1233 150P_0402_50V8J
R174 8.2K_0402_5%
U28 NC7SZ08P5X_NL_SC70-5
PCIE_RST# — R582 0_0402_5%

Need to check material?

+1.8VS / +3VS
R164 10K_0402_5%
APU_PWRGD — Q90 FDV301N_NL_SOT23-3 — H_PWRGD_L 43

+3VALW
C1199 0.1U_0402_16V4Z
U33 NC7SZ08P5X_NL_SC70-5
23,41,42,44 VGA_PWRGD → VGA_PWRGD
R830 0_0402_5% → VGA_PWRGD_R
R838 100K_0402_5%
R839 0_0402_5%
PE_GPIO1 — R109 10K_0402_5% For GPIO45 leakage

RTC BATT Conn.
+RTCBATT
JRTC1 SUYIN_060003HA002G202ZL

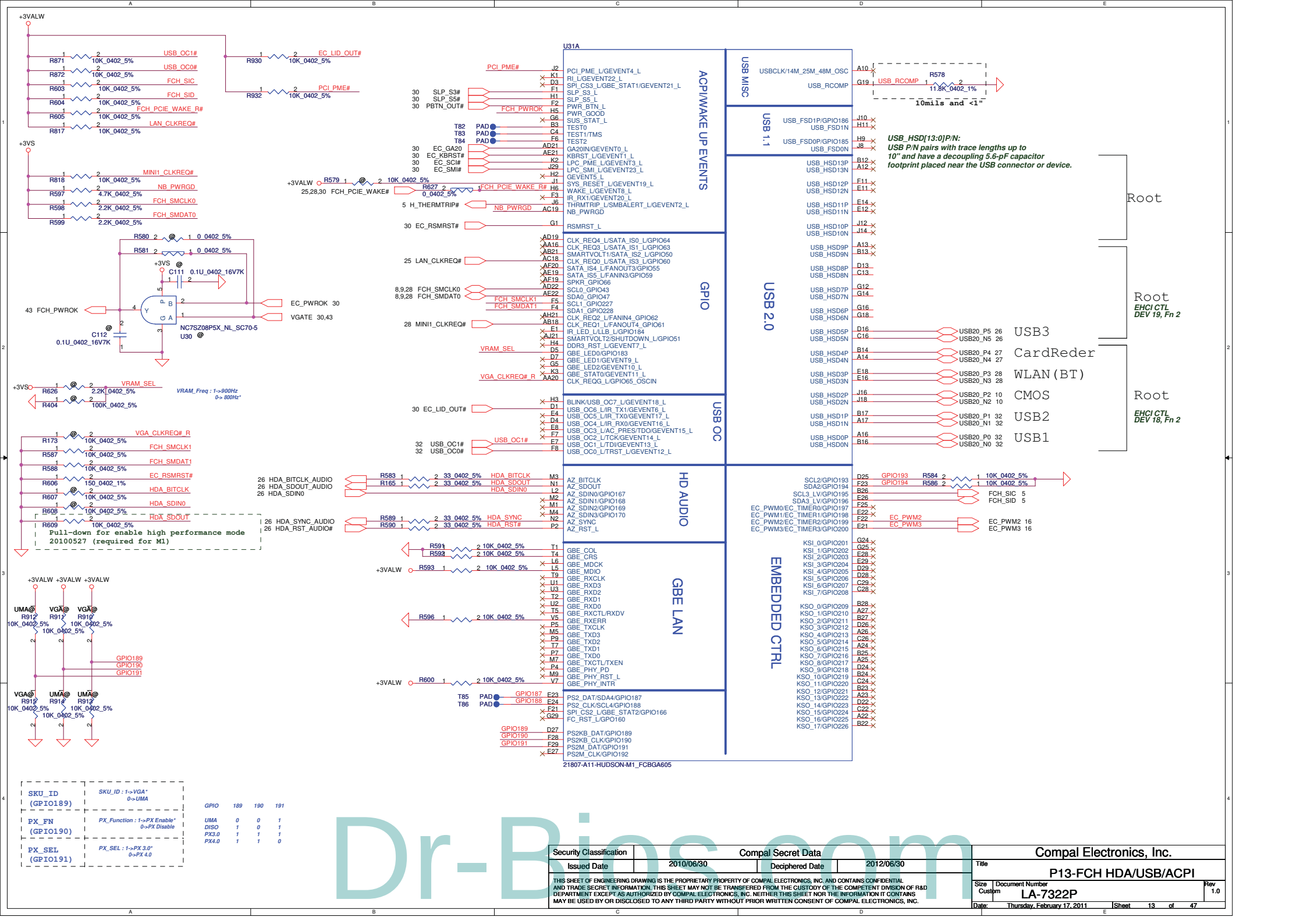
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P12-FCH PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	LA-7322P	1.0

Date: Thursday, February 17, 2011 Sheet 12 of 47



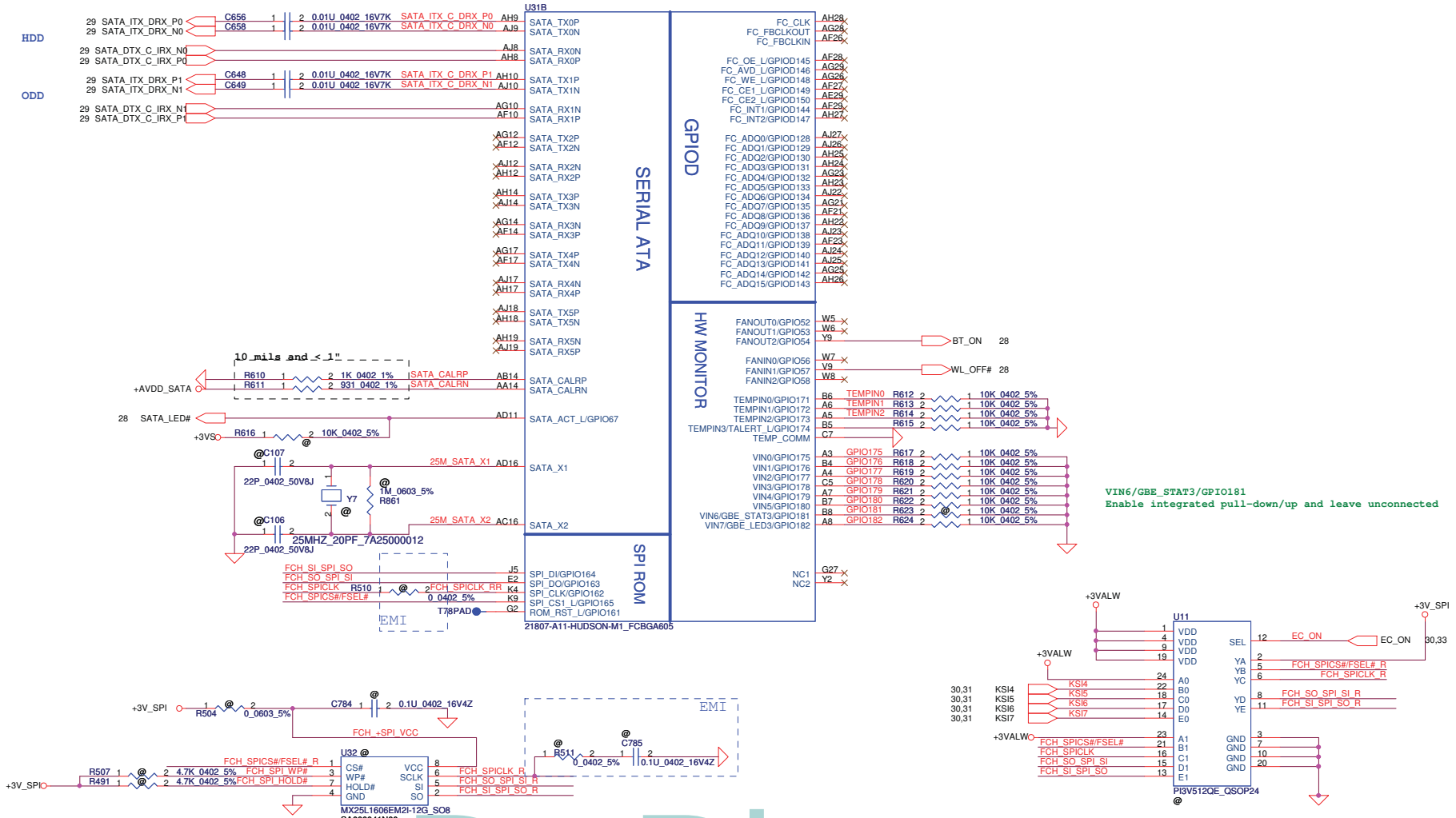
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P13-FCH HDA/USB/ACPI

Size	Document Number	Rev
Custom	LA-7322P	1.0

Date: Thursday, February 17, 2011 | Sheet 13 of 47



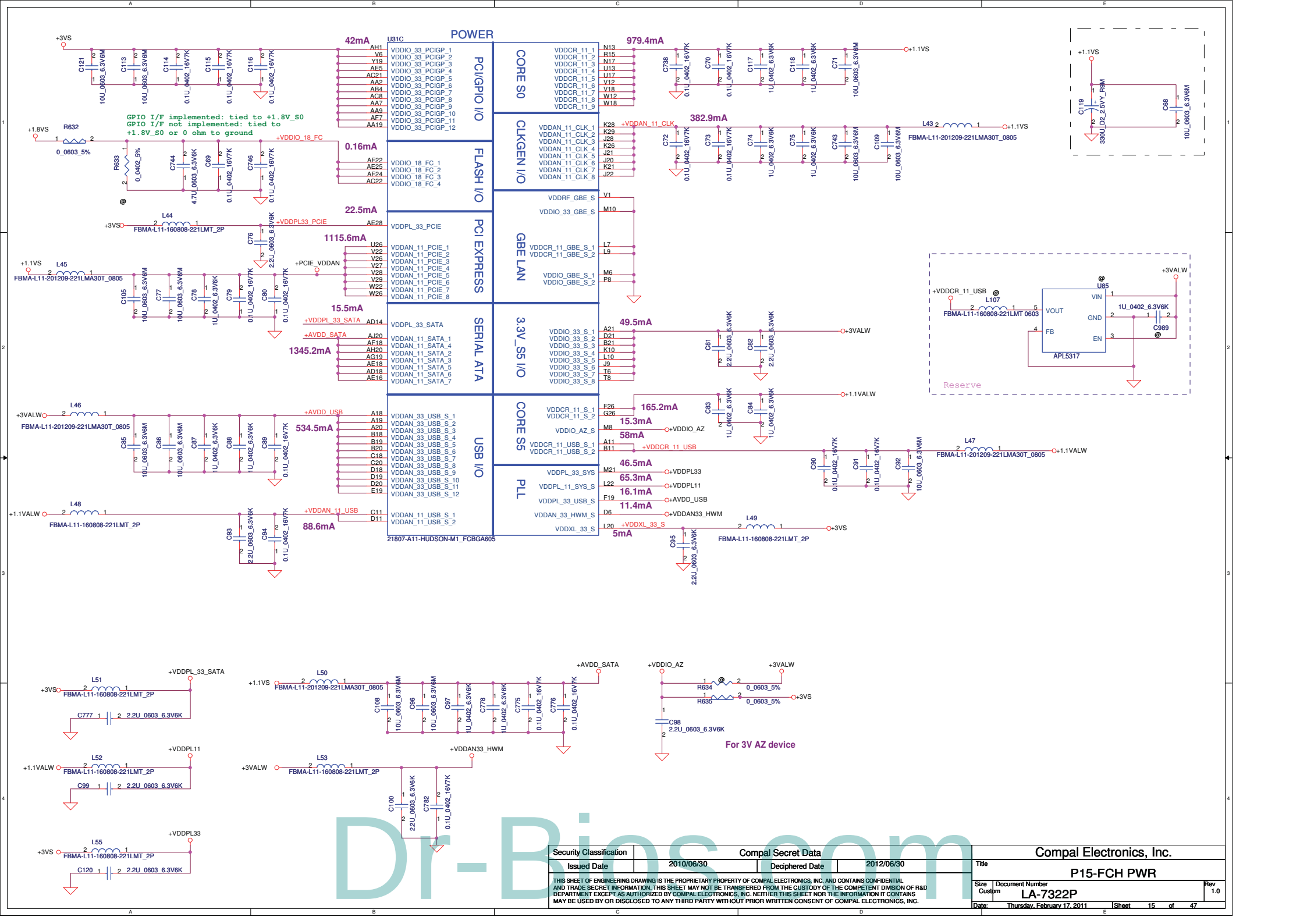
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P14-FCH-SATA/SPI

Size	Document Number	Rev
Custom	LA-7322P	1.0

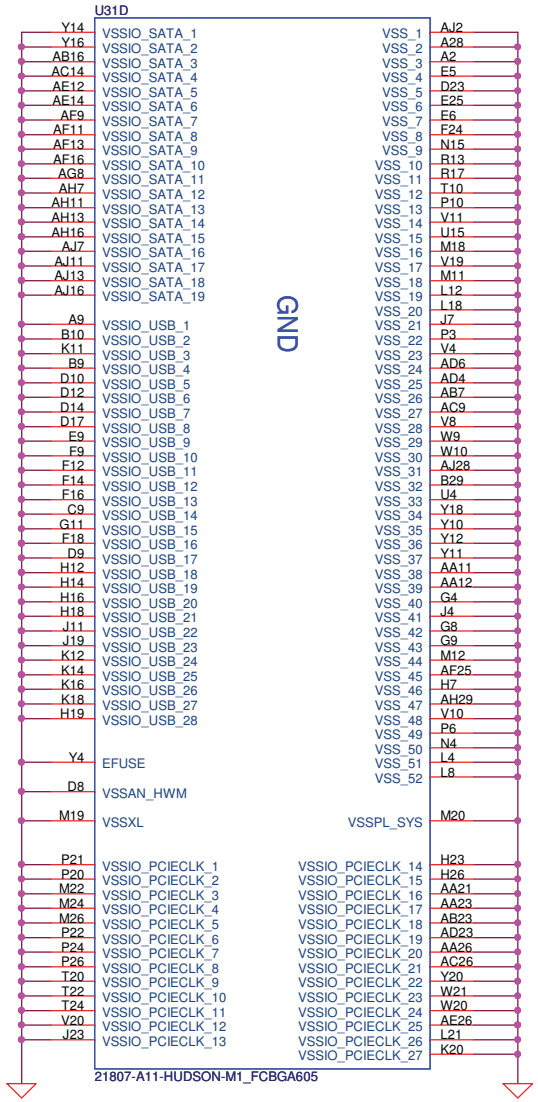
Date: Thursday, February 17, 2011 | Sheet 14 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

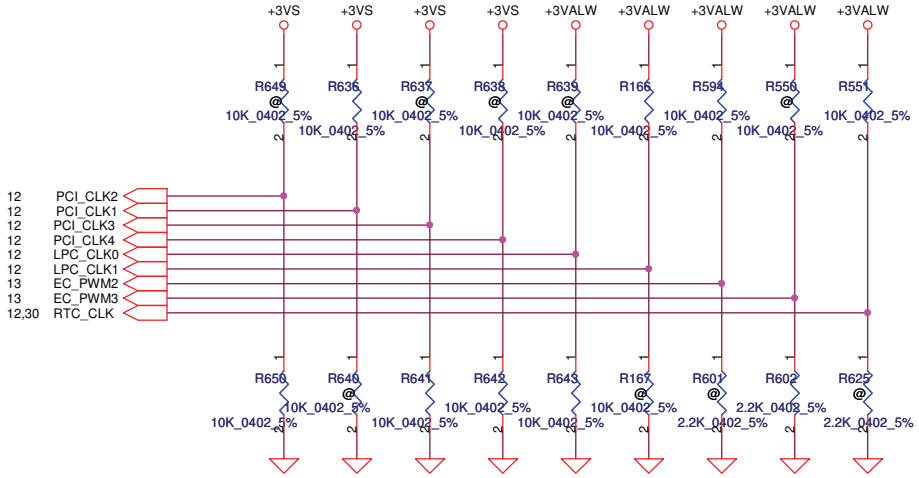
Title	P15-FCH PWR	
Size: Custom	Document Number: LA-7322P	Rev: 1.0
Date: Thursday, February 17, 2011	Sheet 15 of 47	



REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H.L)
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)

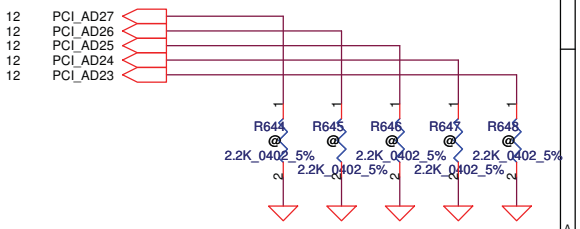


DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

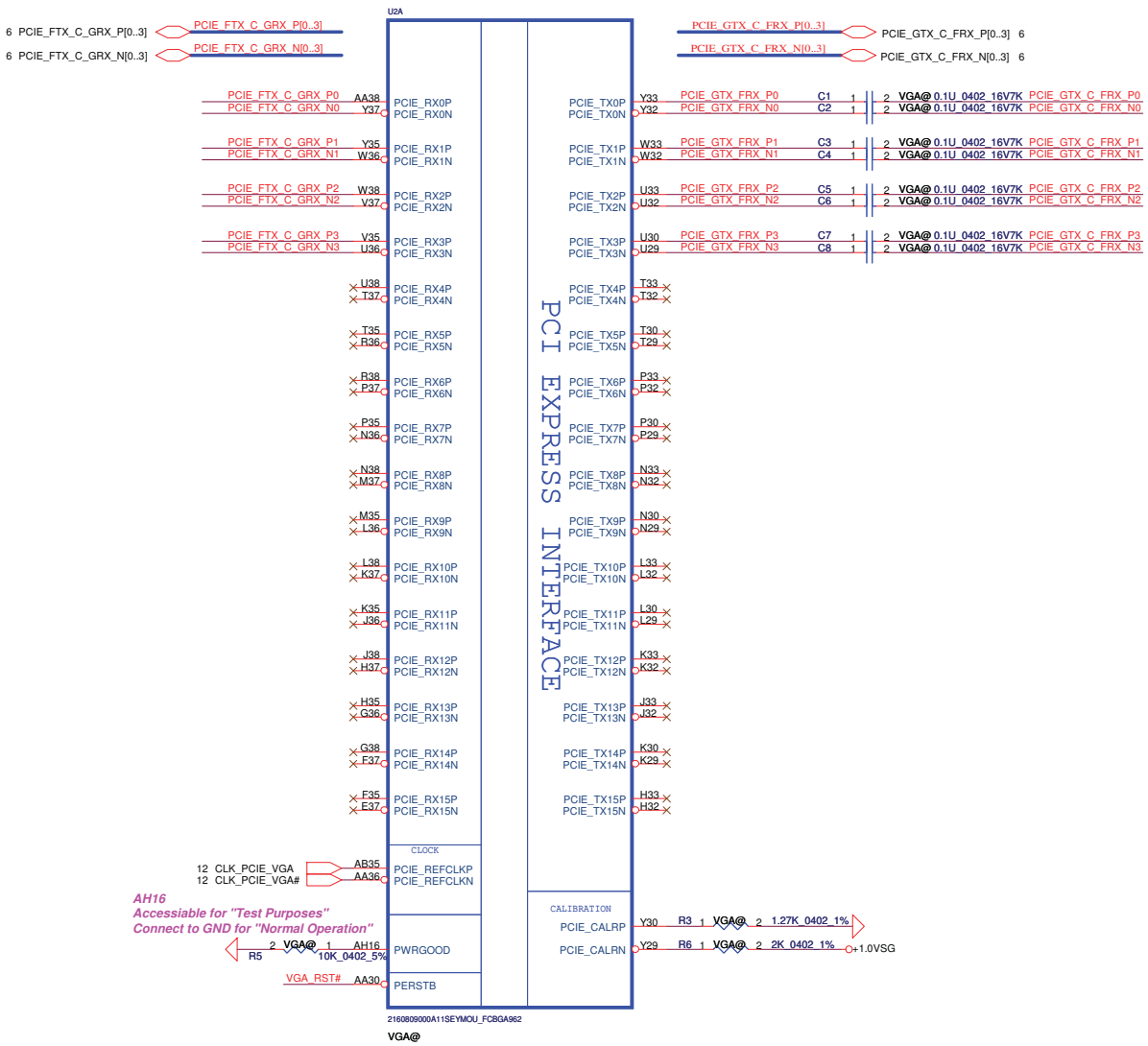
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

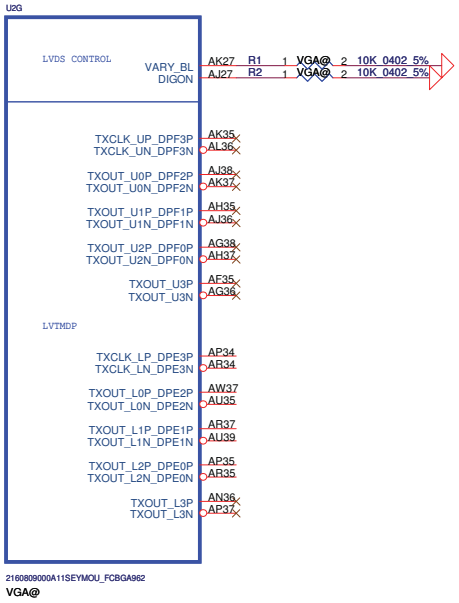
Check AD29,AD28 strap function check default

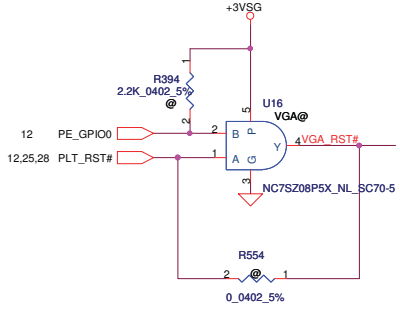


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/06/30	Deciphered Date 2012/06/30	Title: P16-FCH-VSS/Strap
			Size: B; Document Number: LA-7322P; Rev: 1.0
			Date: Thursday, February 17, 2011; Sheet 16 of 47

GFX PCIE LANE REVERSAL







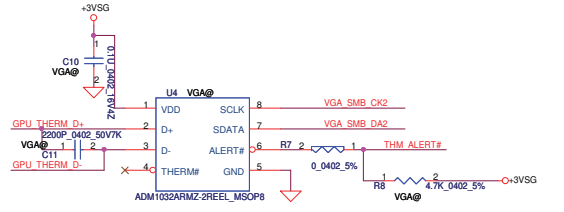
Seymour XT P/N: SA000047H10 (S IC 216-0809000 A11 SEYMOUR XT M2)

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

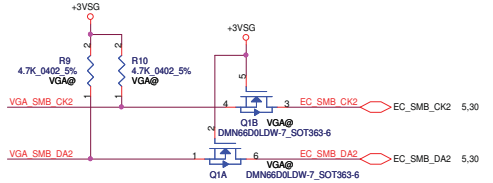
Compal Electronics, Inc.			
Title	P17-Vancouver_ PCIE / LVDS		
Size	Document Number		Rev
Custom	LA-7322P		1.0
Date:	Thursday, February 17, 2011	Sheet	17 of 47

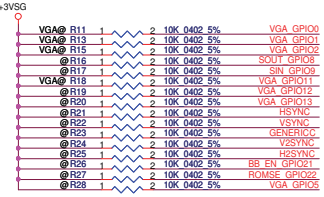
Strap Name		Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disable for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type, CONFIG[3:0] b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 128 MB 000 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

External VGA Thermal Sensor



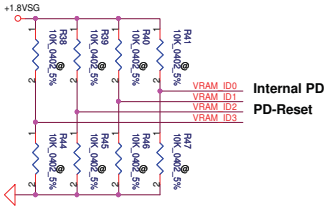
Address 1001 101X b





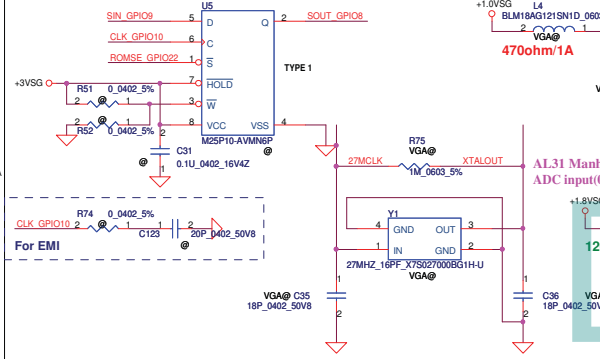
Robson (XT)/Seymour(XT)

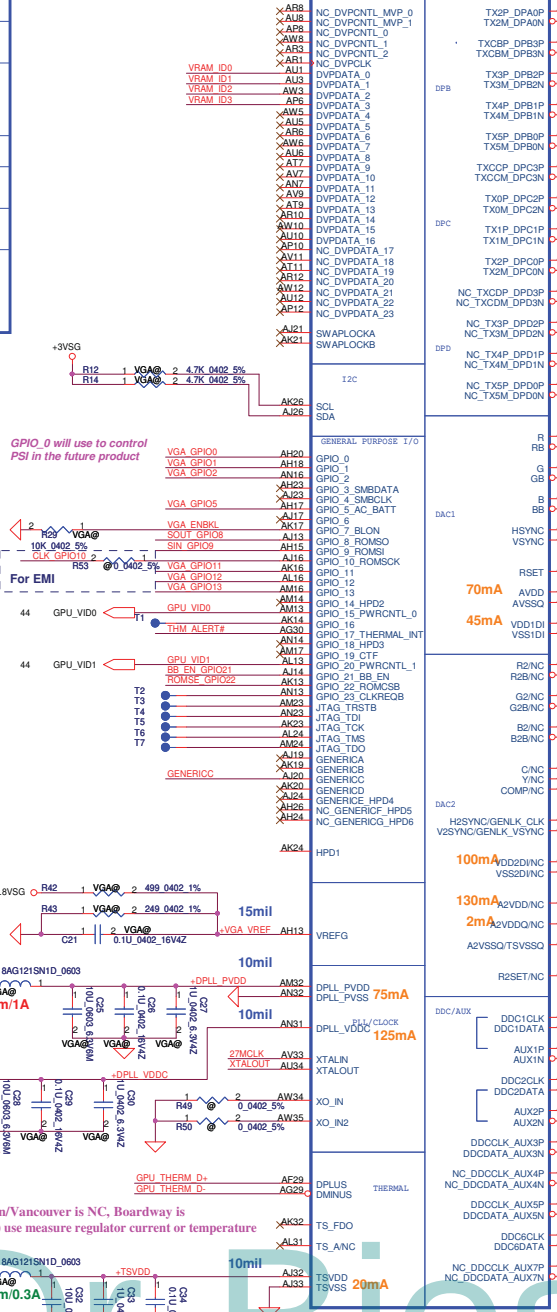
VRAM \ Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004GS30 64M16 K4W1G1646G-BC11	0	0	0	0
Samsung SA000047QA0 128M16 K4W2G1646C-HC11	0	0	0	1
Hynix SA00041S60 64M16 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16 H5TQ2G63BFR-11C	0	1	0	1



Internal PD
PD-Reset

FLASH ROM





Not share via for other GND

GPIO_0 will use to control PSI in the future product

For EMI

70mA
45mA
100mA
130mA
2mA
75mA
125mA
20mA

NC on Whistler and Seymour

In Whistler and Seymour, change to GENLK_CLK, GENLK_VSYNC for Global Swap Lock on multiple GPUs

Except A2VSSQ change to TSVSSQ, others are NC on Whistler and Seymour

NC on Park, Robson and Seymour

NC on Park, Robson and Seymour

AL31 Manhattan/Vancouver is NC, Boardway is ADC input(0-1V) use measure regulator current or temperature

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P18-Vancouver_Strap/DP/HDMI//CRT

Size	Document Number	Rev
Custom	LA-7322P	1.0

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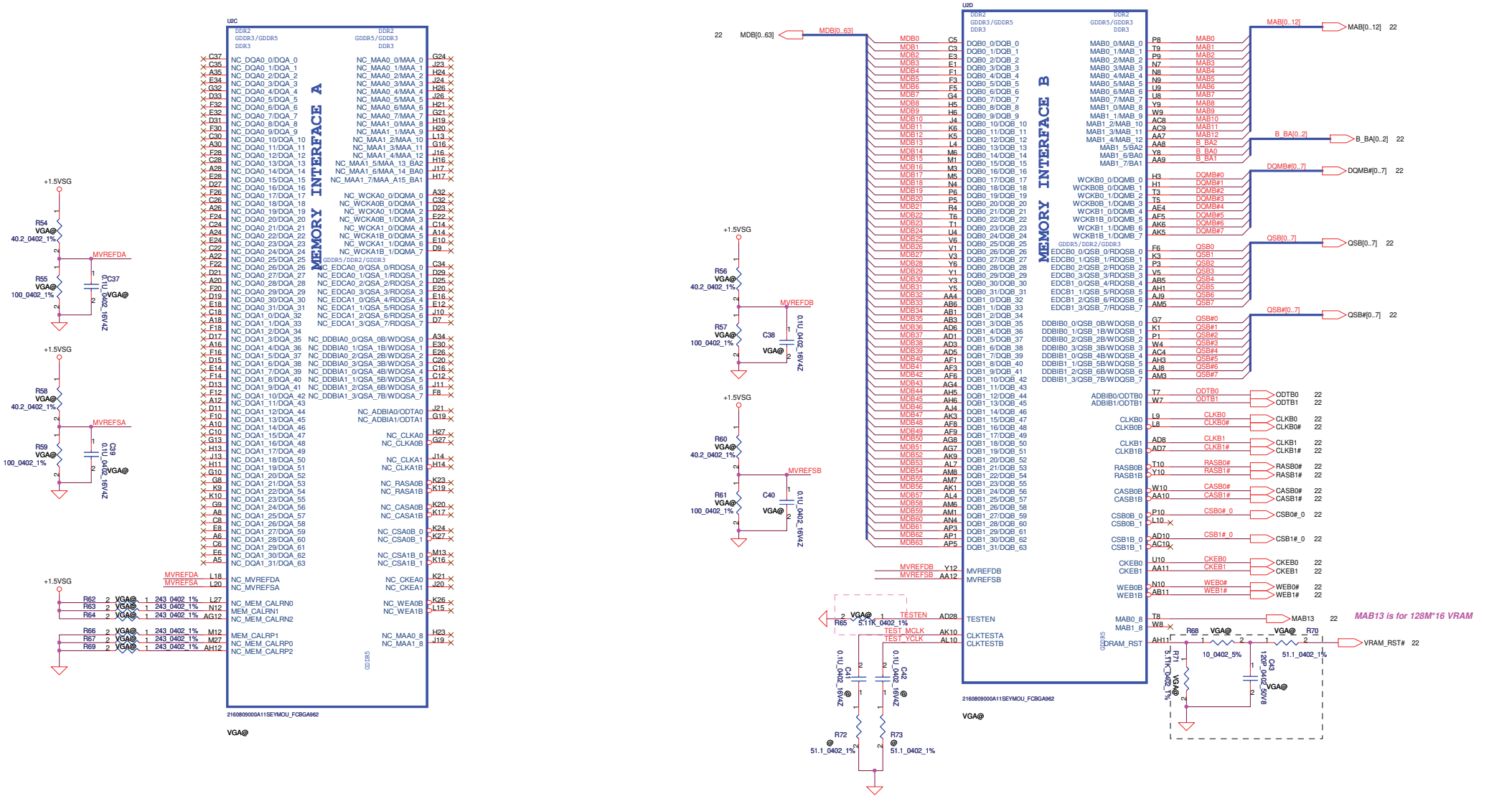
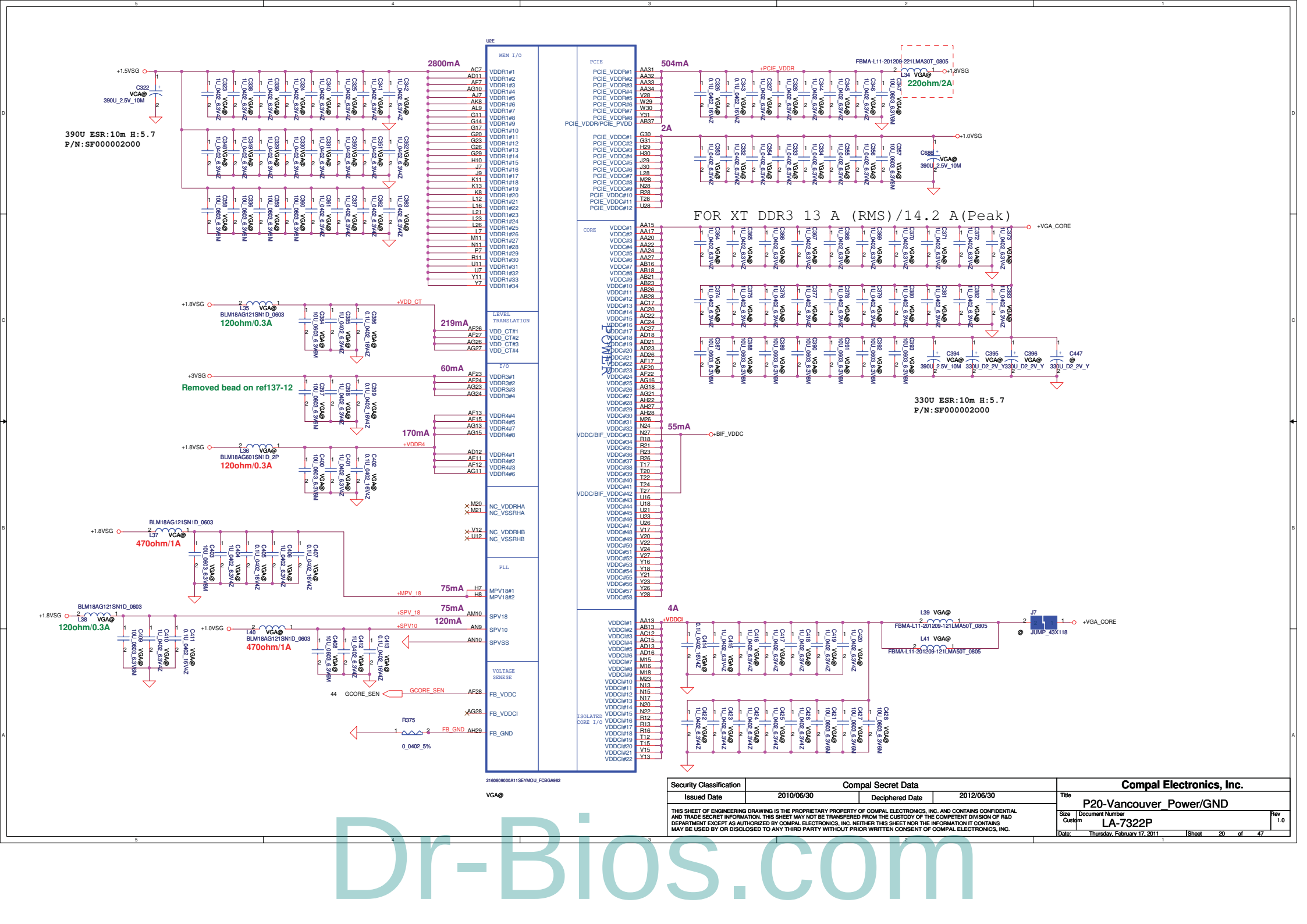
Robson,Seymour only support single channel memory (channel B only)



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title	P19-Vancouver_Memory	
Size: Custom	Document Number: LA-7322P	Rev: 1.0
Date: Thursday, February 17, 2011	Sheet 19 of 47	



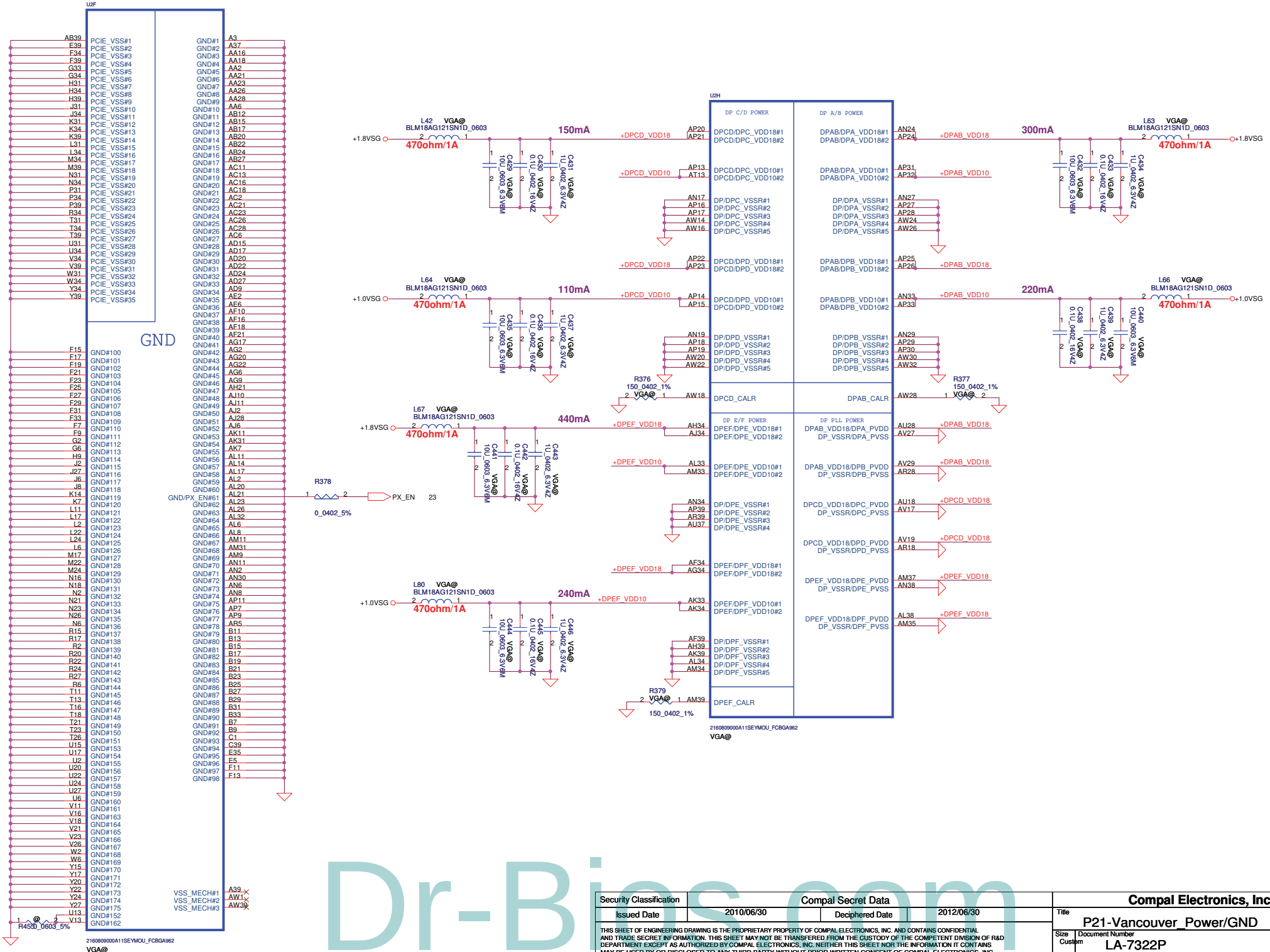
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P20-Vancouver_Power/GND

Size	Document Number	Rev
Custom	LA-7322P	1.0

Date: Thursday, February 17, 2011 | Sheet 20 of 47



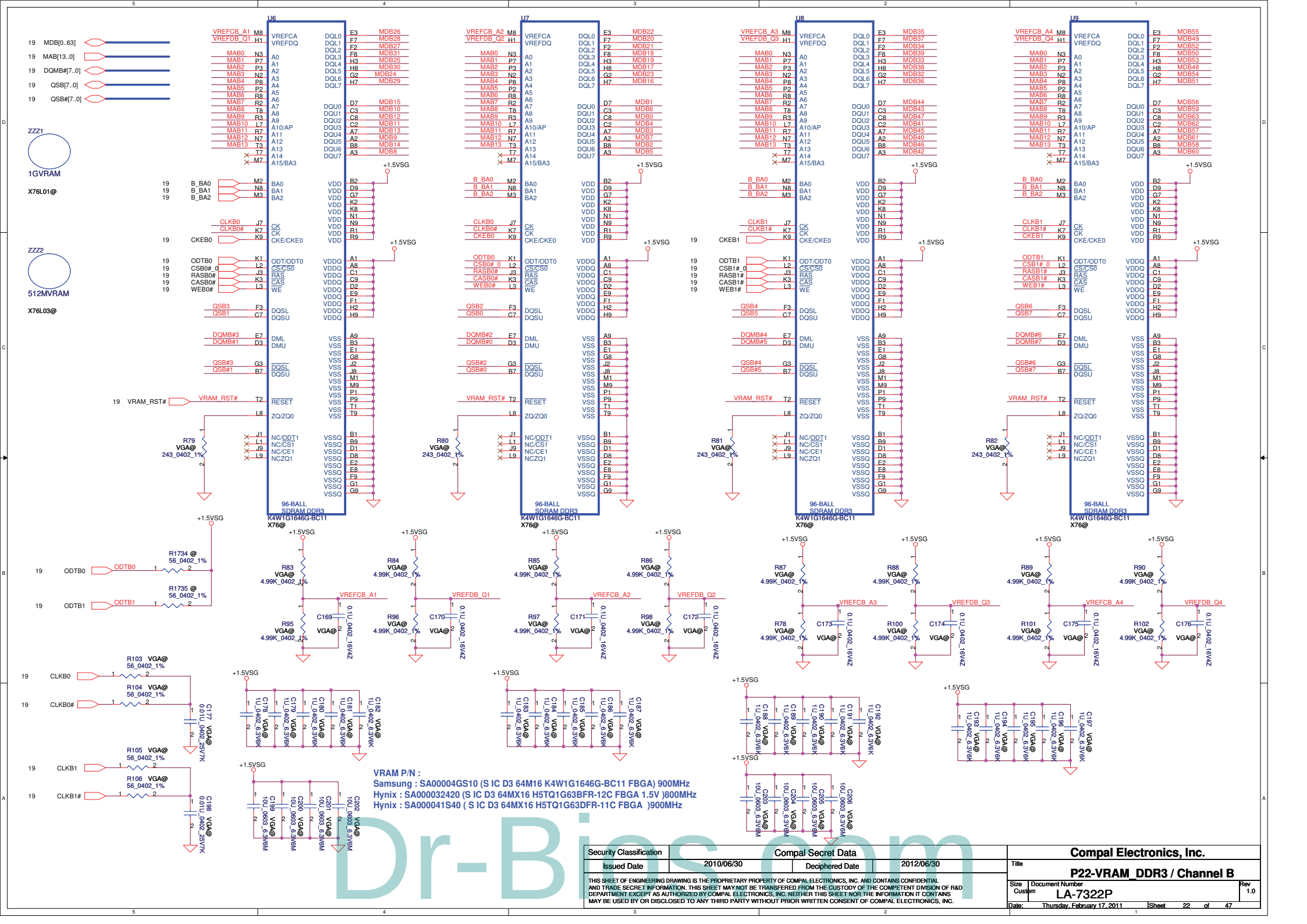
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P21-Vancouver_Power/GND

Size: Custom | Document Number: LA-7322P | Rev: 1.0

Date: Thursday, February 17, 2011 | Sheet 21 of 47



VRAM P/N :
Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA) 900MHz
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)800MHz
Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA)900MHz

Security Classification	Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date 2012/06/30

Compal Electronics, Inc.

Title: **P22-VRAM_DDR3 / Channel B**

Size	Document Number	Rev
Custom	LA-7322P	1.0

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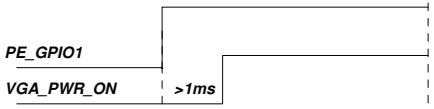
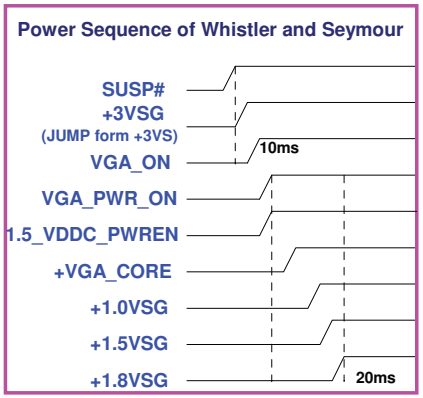
For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON

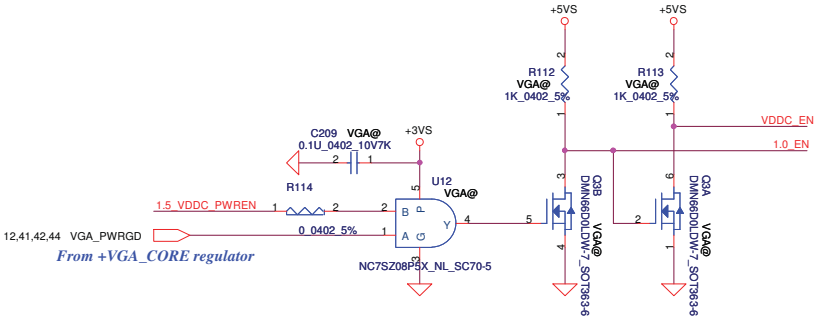


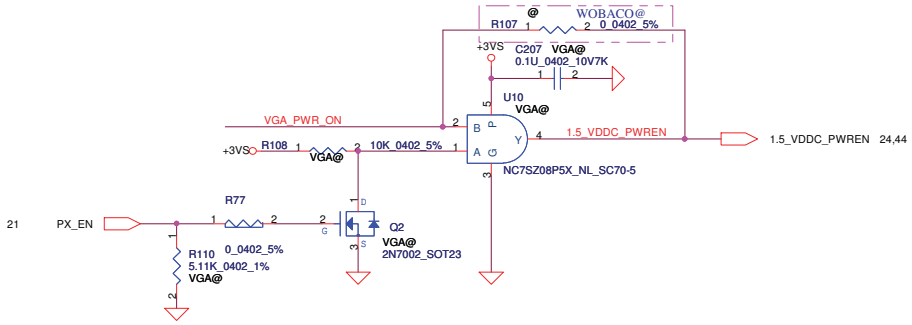
Power Sequence of Whistler and Seymour

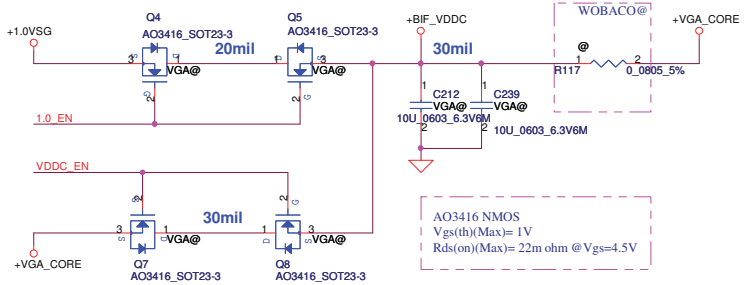


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Seymour
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON#
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN#







Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

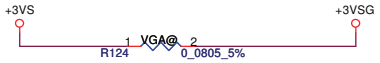
Compal Electronics, Inc.

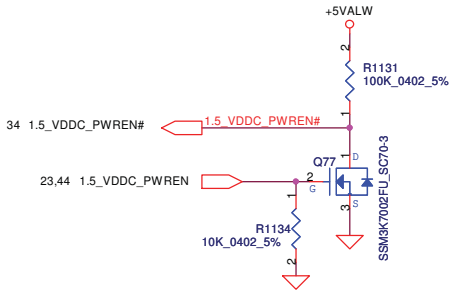
Title: P23-VGA power sequence and BACO

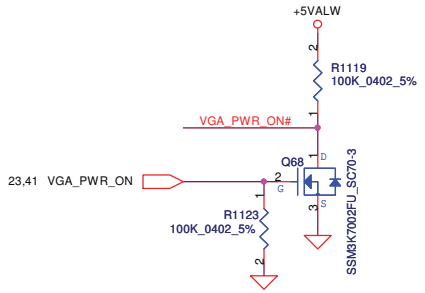
Size	Document Number	Rev
Custom	LA-7322P	1.0

Date: Thursday, February 17, 2011 Sheet 23 of 47

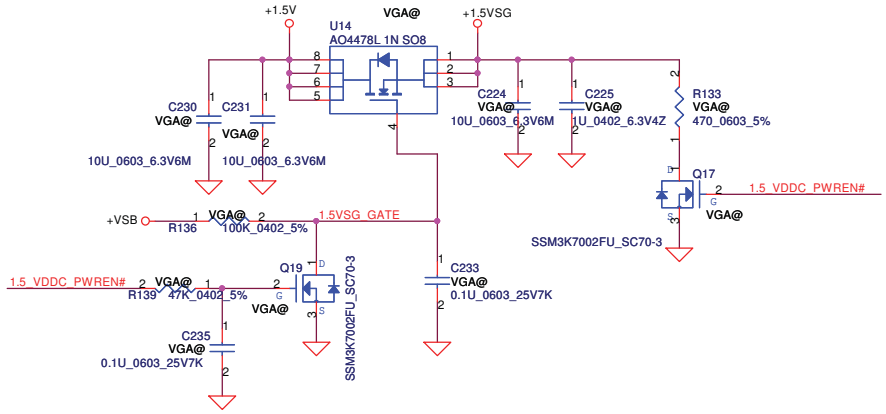
+3.3VS TO +3.3VSG





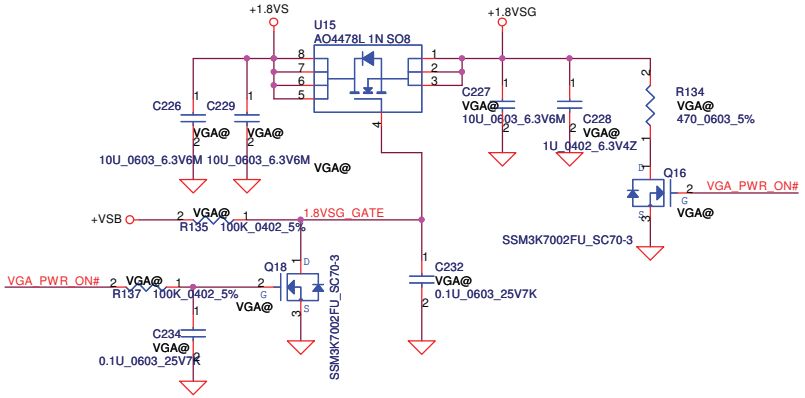


+1.5V TO +1.5VSG



+1.8VS TO +1.8VSG

Change P/N SB00000GV00



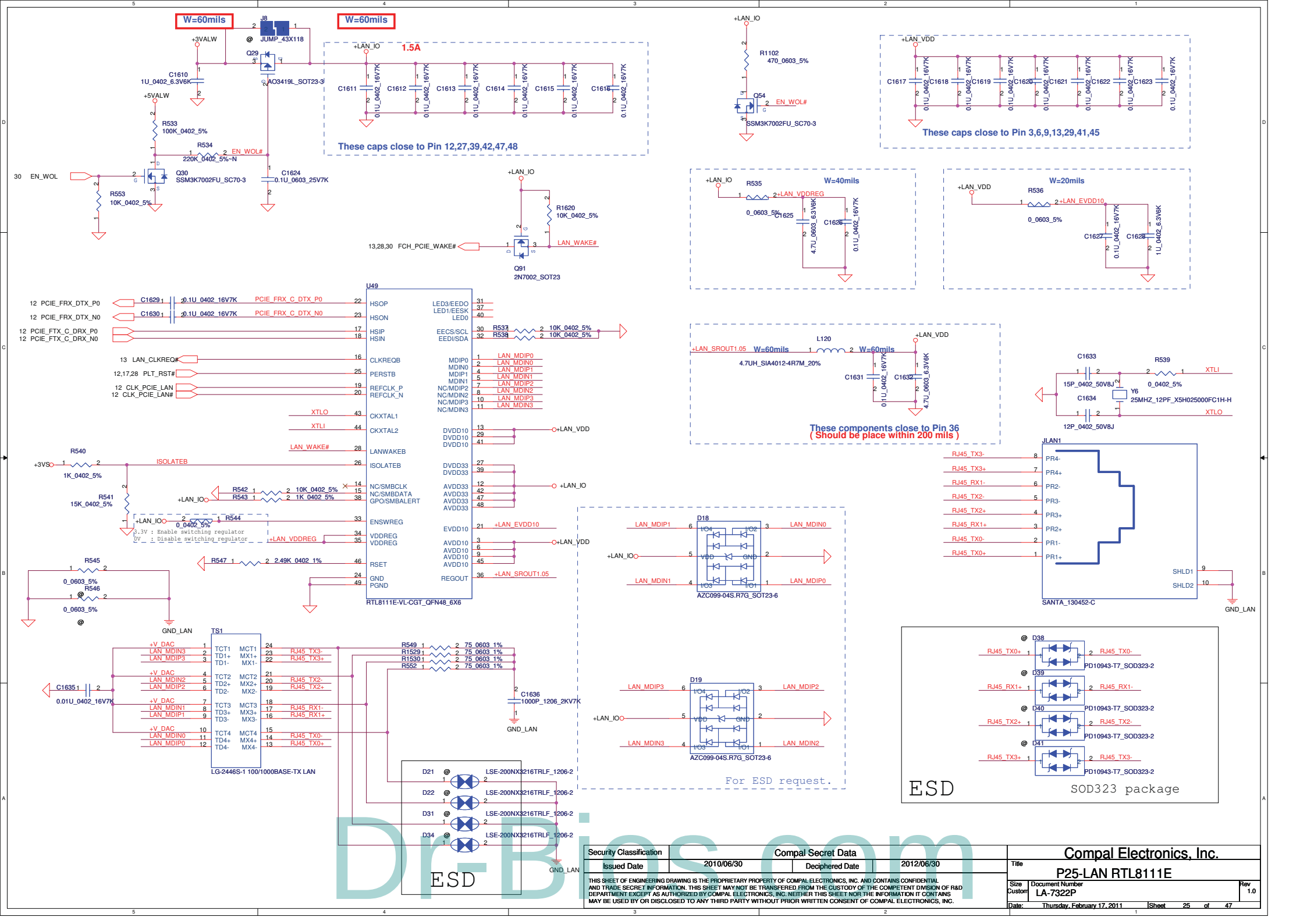
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P24-VGA DC Interface

Size	Document Number	Rev
Custom	LA-7322P	1.0

Date: Thursday, February 17, 2011 | Sheet 24 of 47



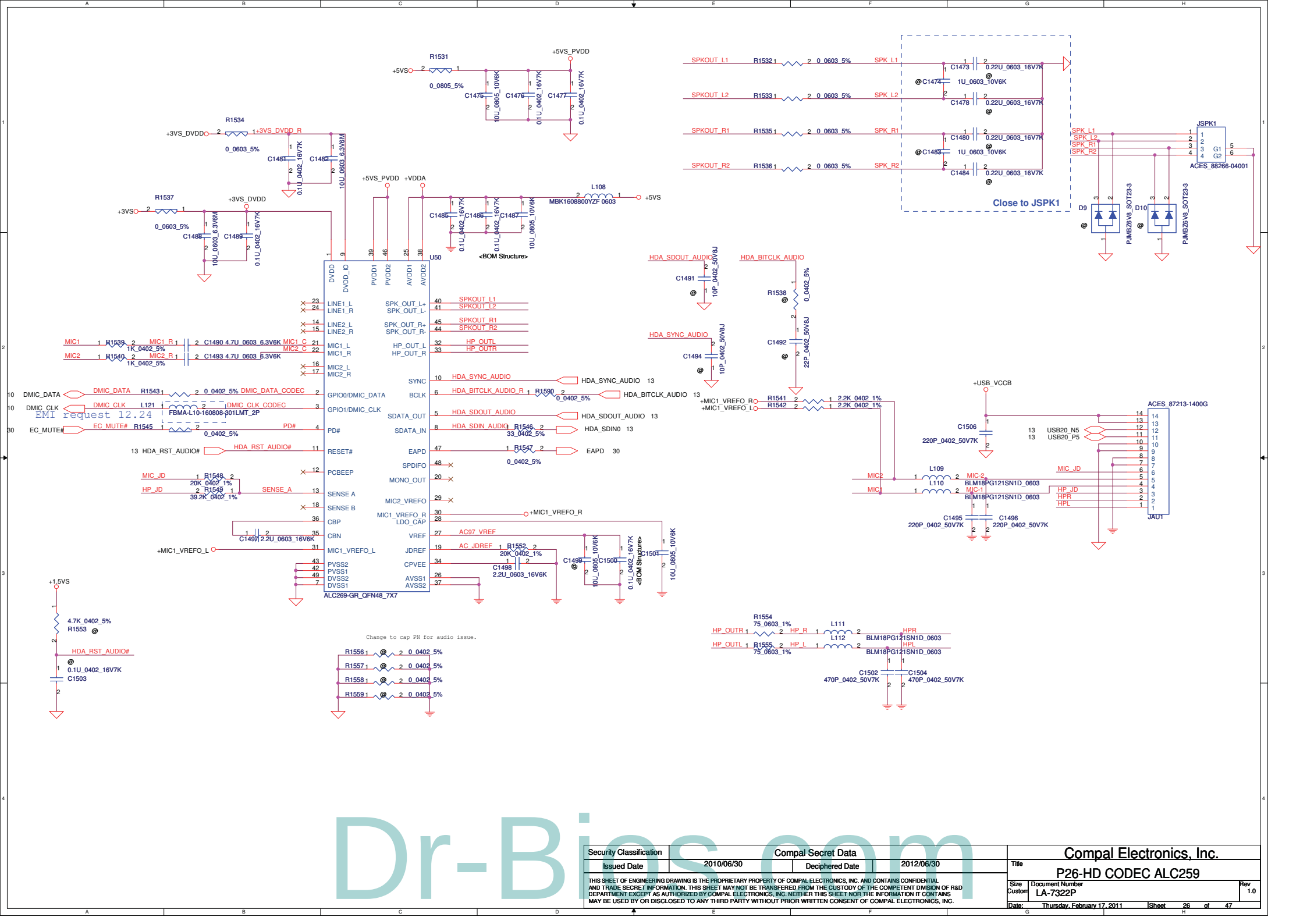
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P25-LAN RTL8111E

Size: Custom | Document Number: LA-7322P | Rev: 1.0

Date: Thursday, February 17, 2011 | Sheet 25 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P26-HD CODEC ALC259

Size	Document Number	Rev
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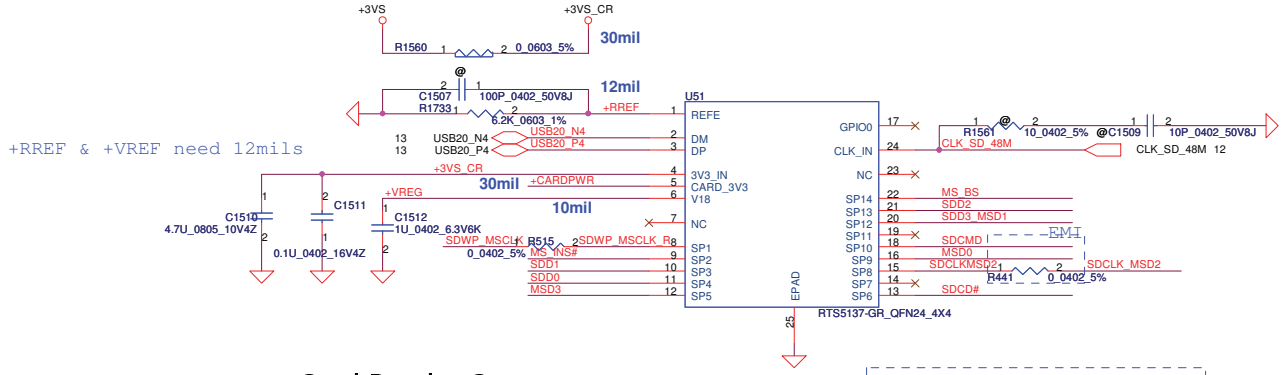
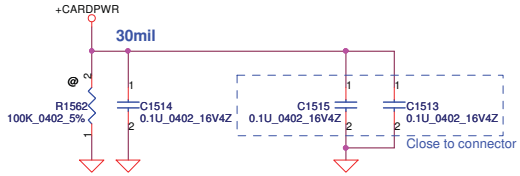
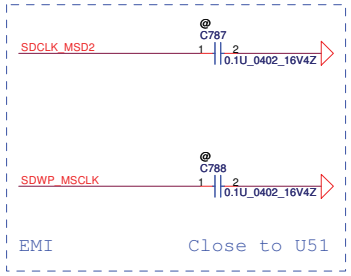
Card Reader RTS5137
(only SD/MMC/MS function)

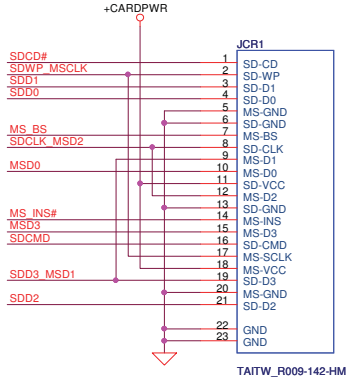


+RREF & +VREF need 12mils

Card Reader Connector





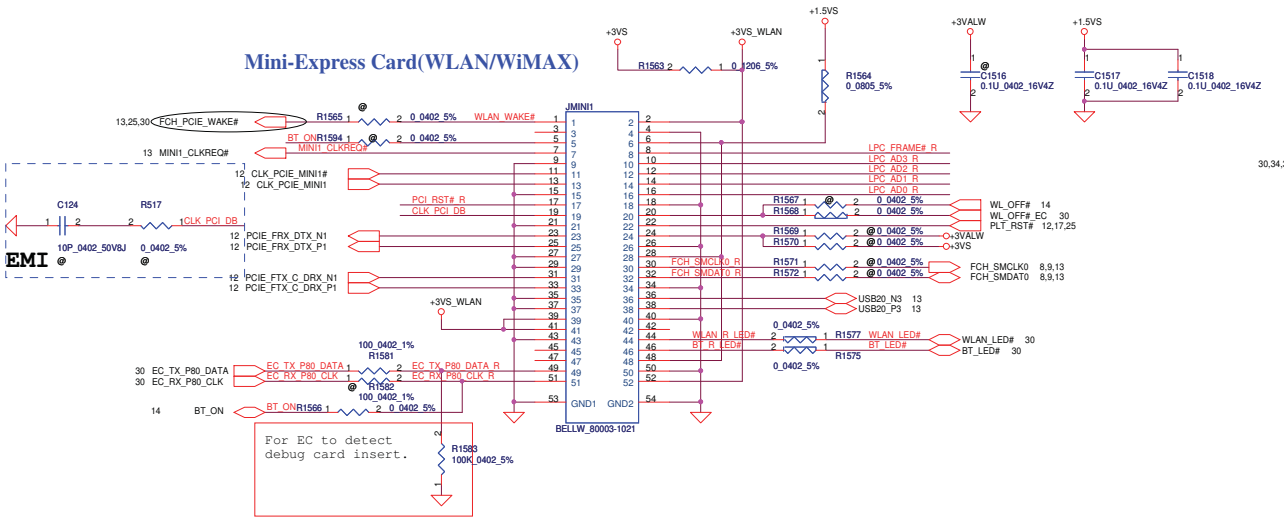


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

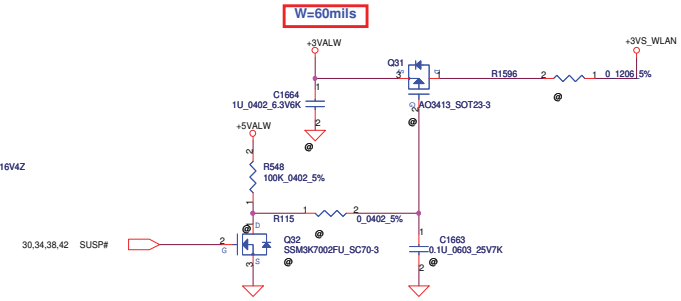
Compal Electronics, Inc.			
Title	P27-RTS5137 Media Card Controller		
Size: Custom	Document Number: LA-7322P		Rev: 1.0
Date: Thursday, February 17, 2011	Sheet 27 of 47		

Mini-Express Card for WLAN/WiMAX(Half)

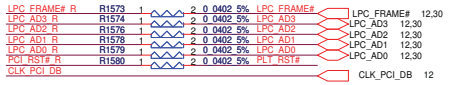
Mini-Express Card(WLAN/WiMAX)



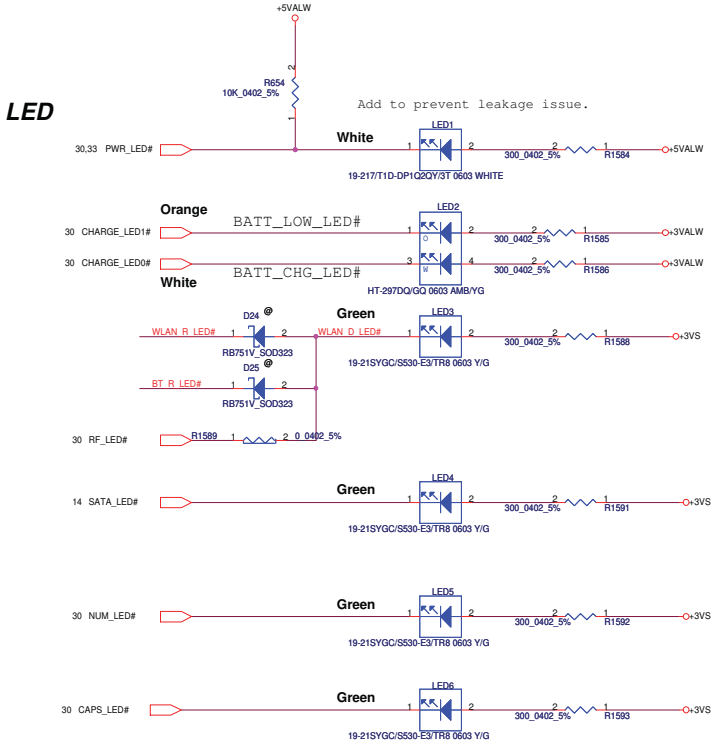
W=60mils

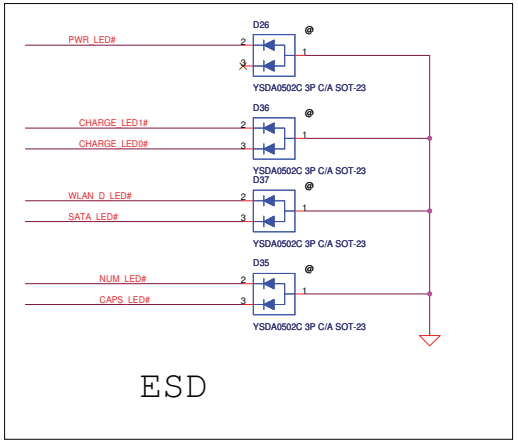


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



LED





Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.			
Title	P28-Mini PCIE/LED		
Size	Document Number		Rev
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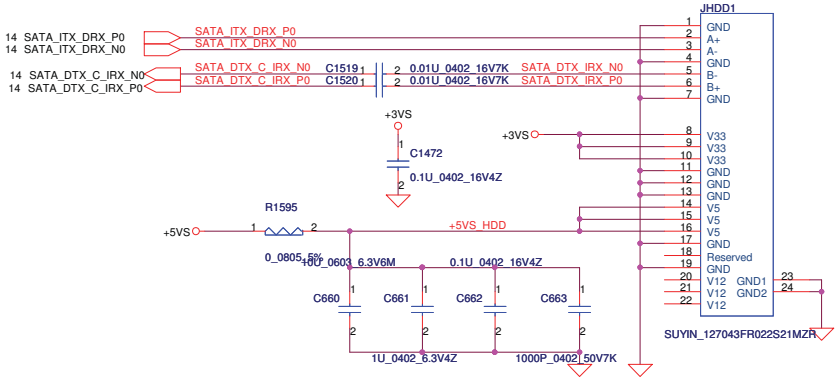
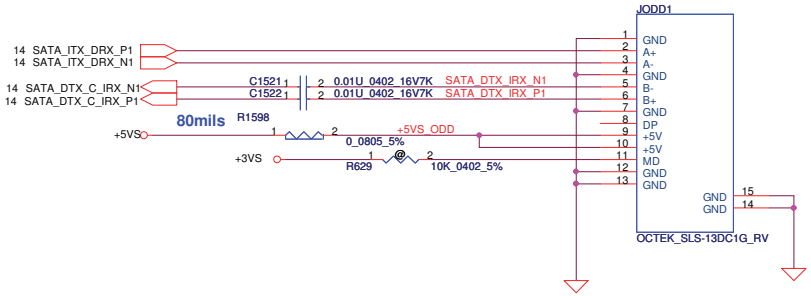
Date: Thursday, February 17, 2011	Sheet 28 of 47		

SATA HDD Conn.



SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.		
Title	P29-HDD & ODD CONN	
Size B	Document Number LA-7322P	Rev 1.0
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R10 PR	100K	46.4K	1.045V

FOR EC 128KB SPI ROM (150mil PACKAGE) SA00002C100

Reserve for EC Close to U47

If Q8 or R429, R432 implemented, R747 & R748 need to be mounted

EMI request 12.24

EMI request 12.24

20mils

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P30-BIOS & EC KB930

Size: Custom | Document Number: LA-7322P | Rev: 1.0

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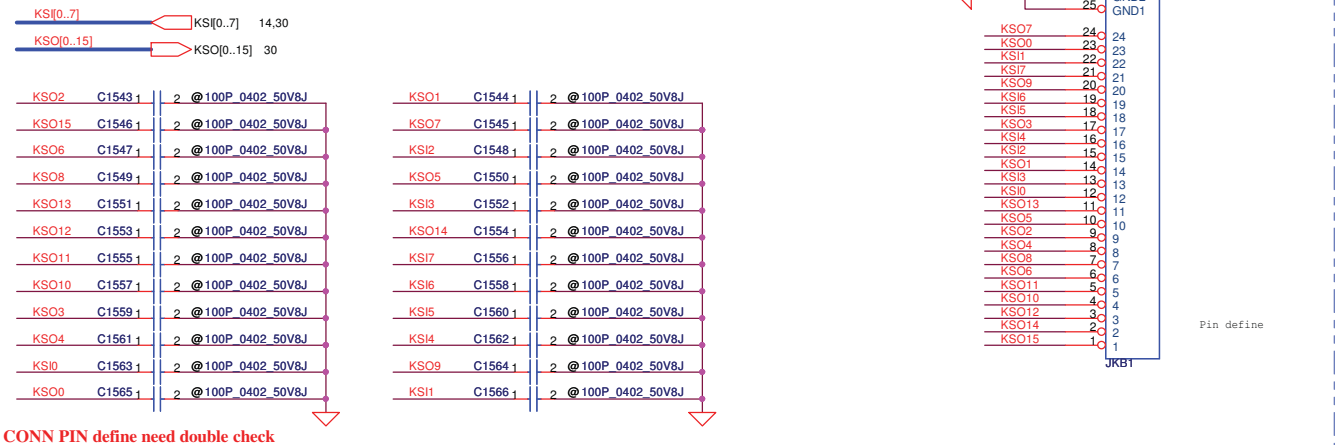
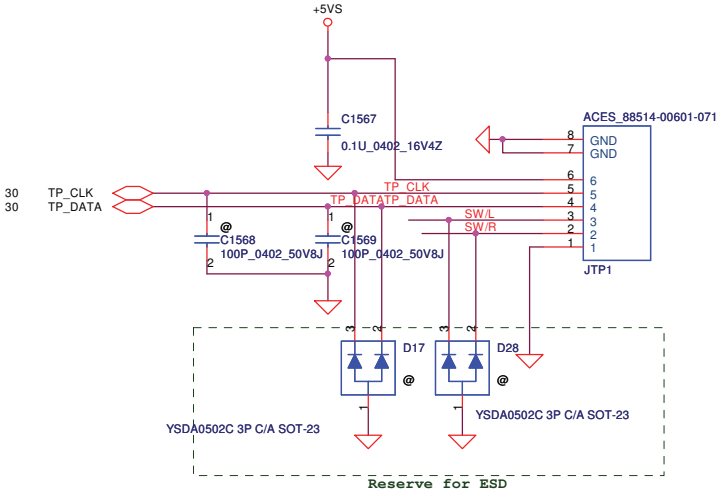
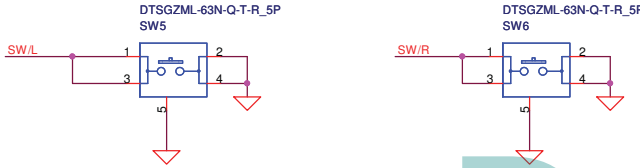
INT_KBD Conn.



CONN PIN define need double check

To TP/B Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size	Document Number	Rev
B	LA-7322P	1.0

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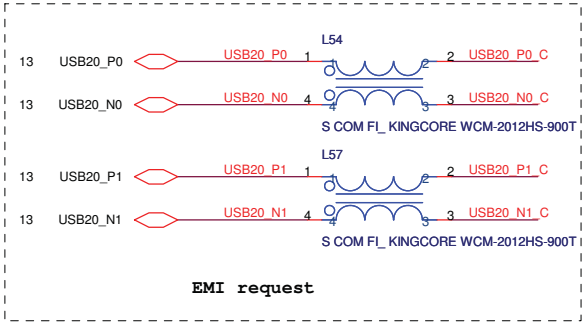
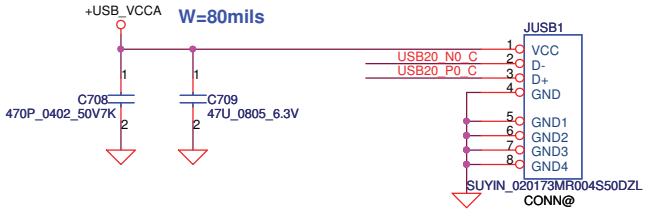
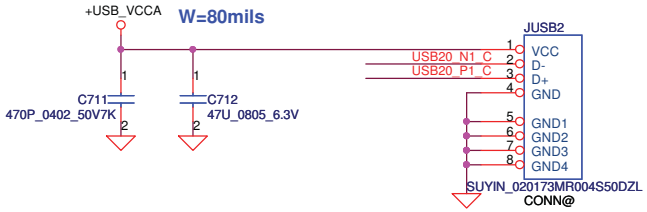
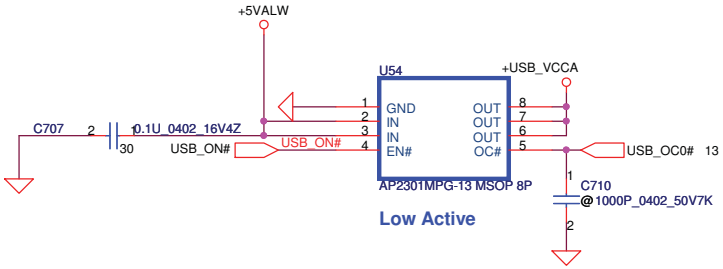


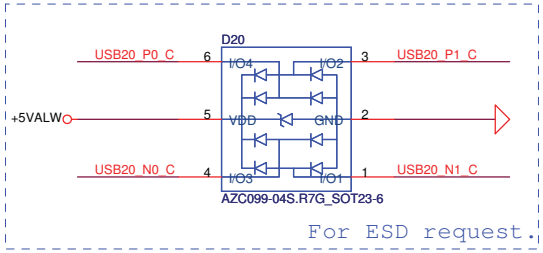
Left USB Conn.

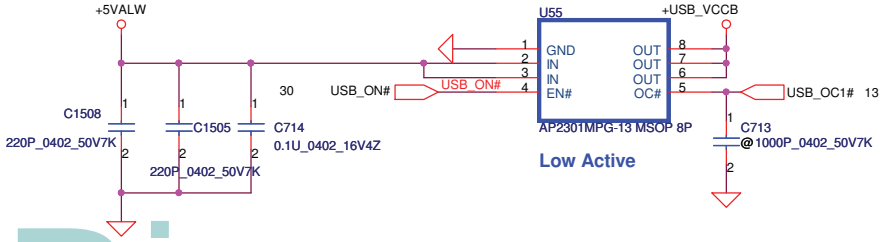


Left USB Conn.









Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.			
Title	P32-USB/BT/USBsub		
Size: Custom	Document Number: LA-7322P		Rev: 1.0
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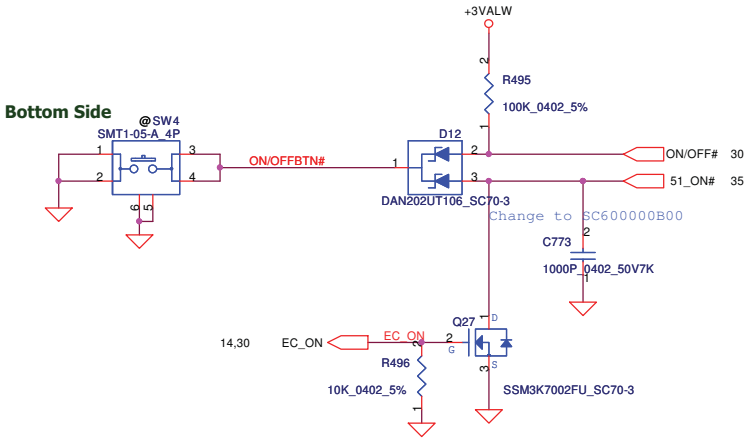
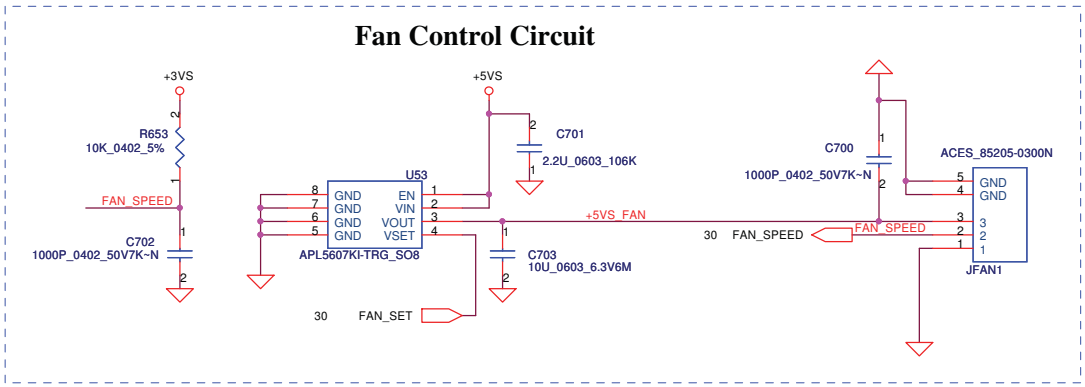
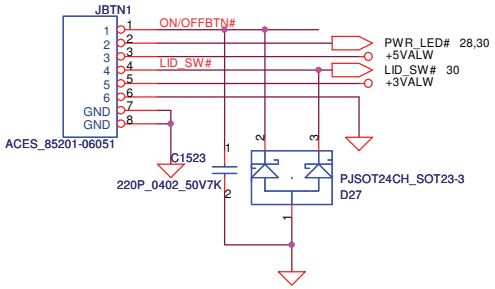
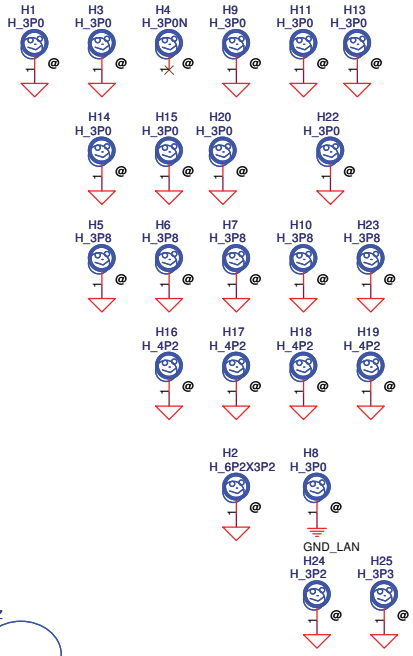
ON/OFF switch **Power Button**









Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P33-Other IO/USB (right)

Size	Document Number	Rev
Custom	LA-7322P	1.0

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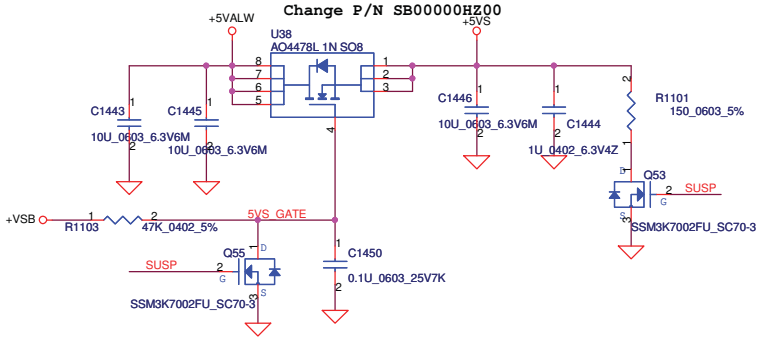
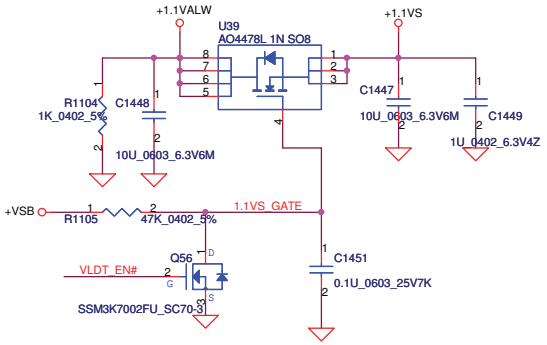
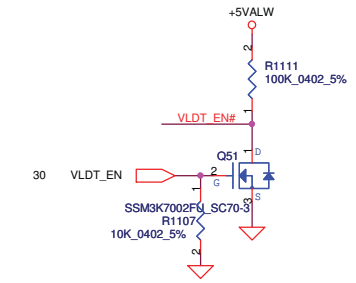
+5VALW TO +5VS

Change P/N SB00000HZ00



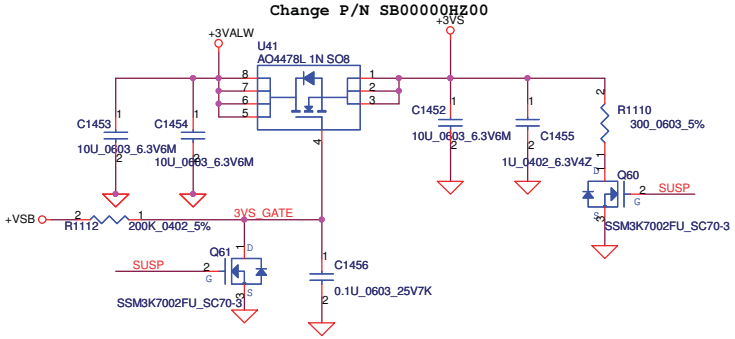
+1.1VALW TO +1.1VS

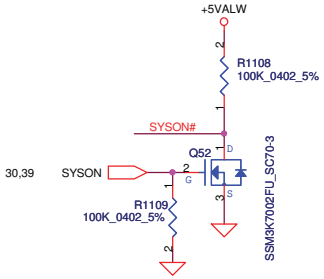


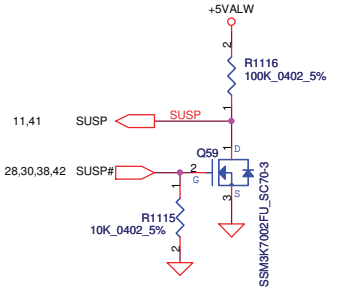


+3VALW TO +3VS

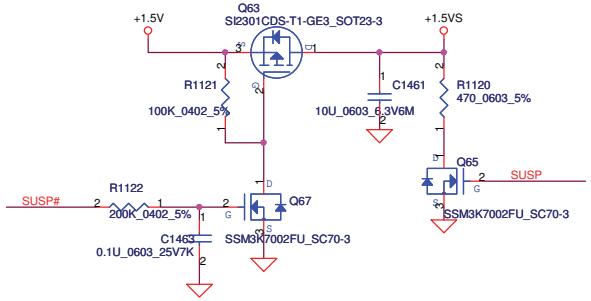
Change P/N SB00000HZ00

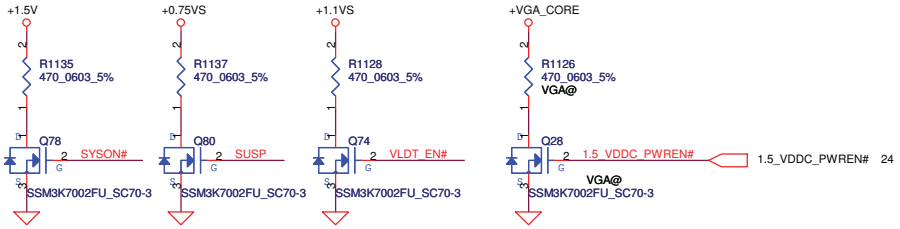






+1.5VS





Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P34-DC Interface

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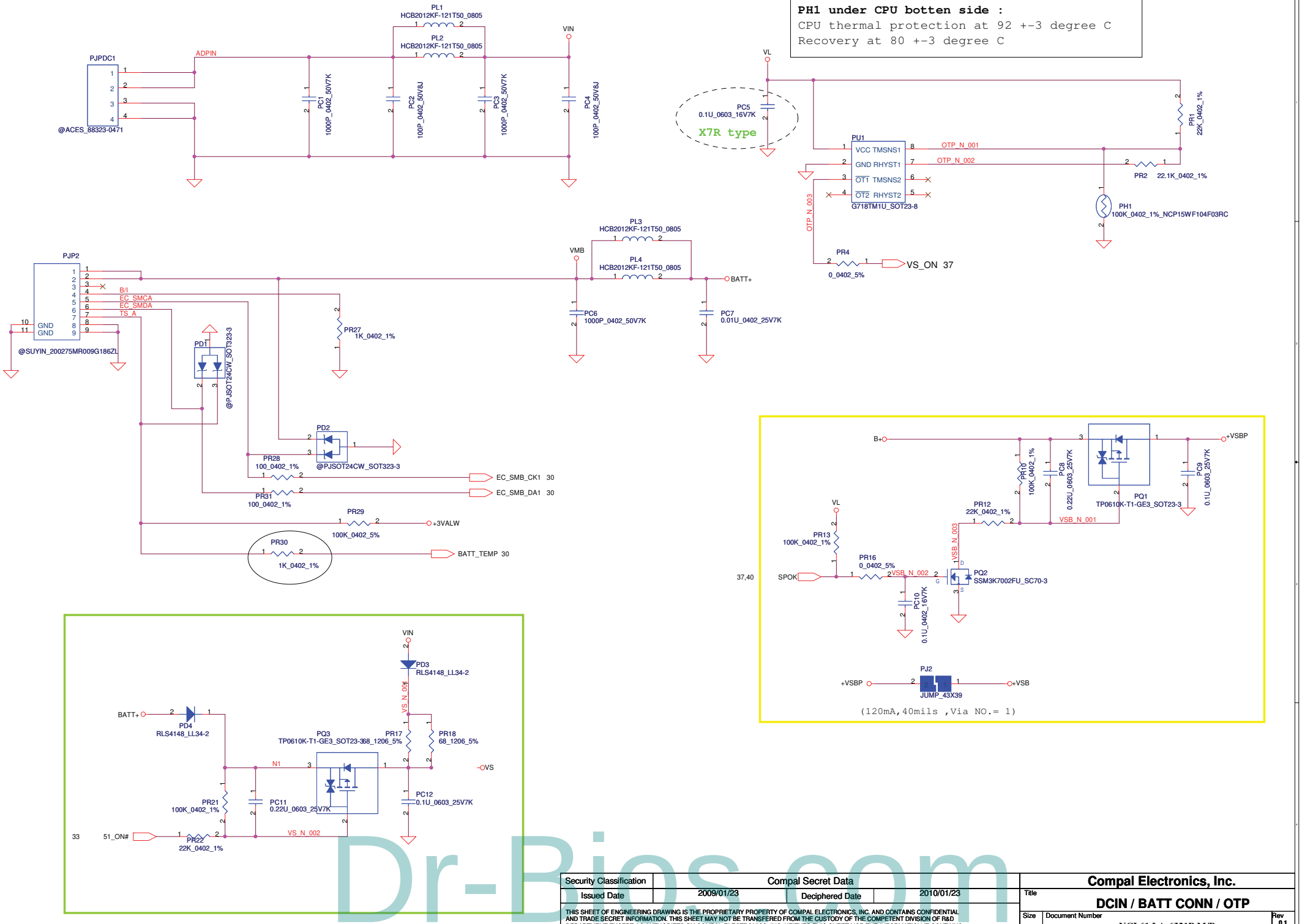
PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

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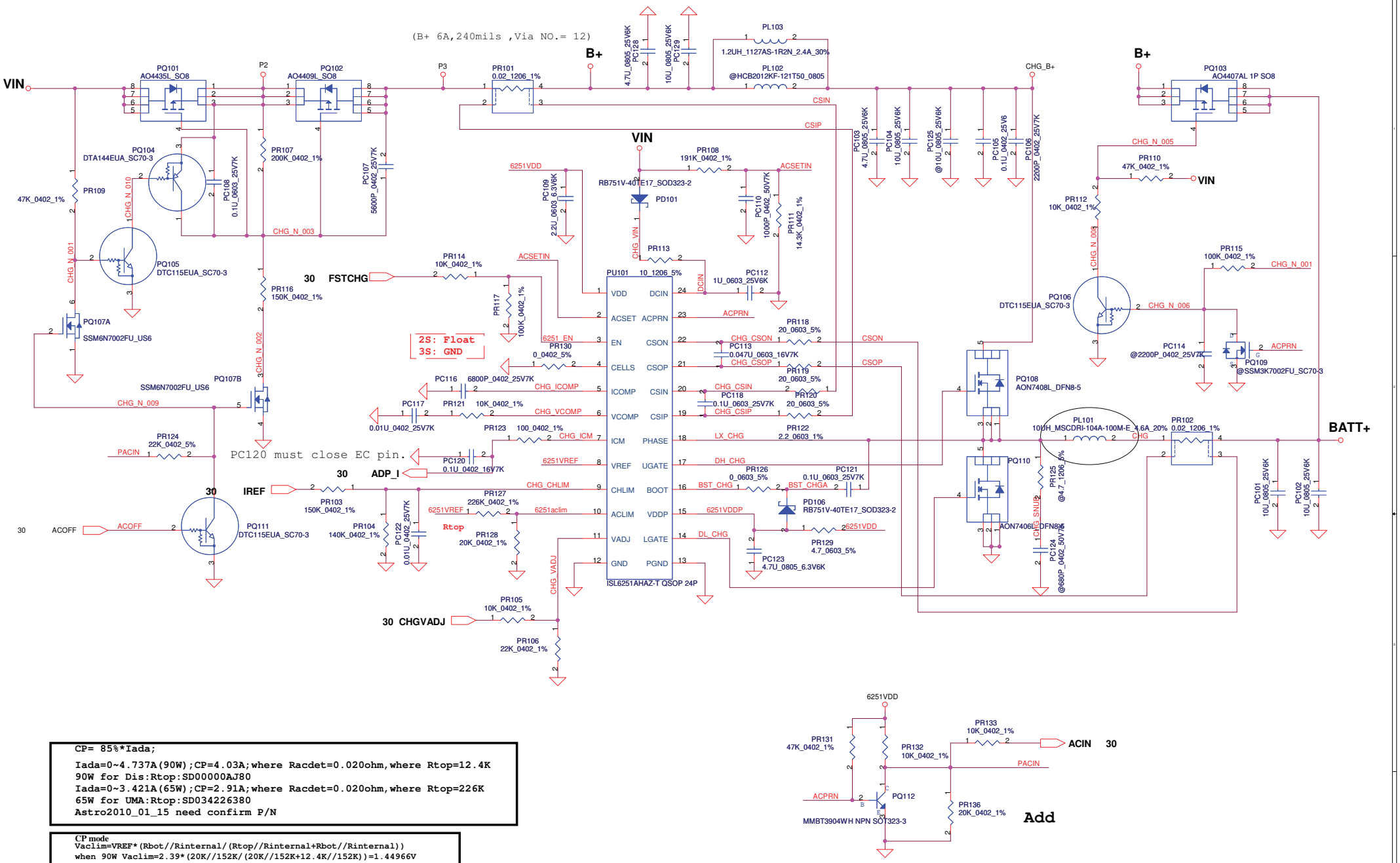

CP= 85%*Iada;

Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: CHARGER

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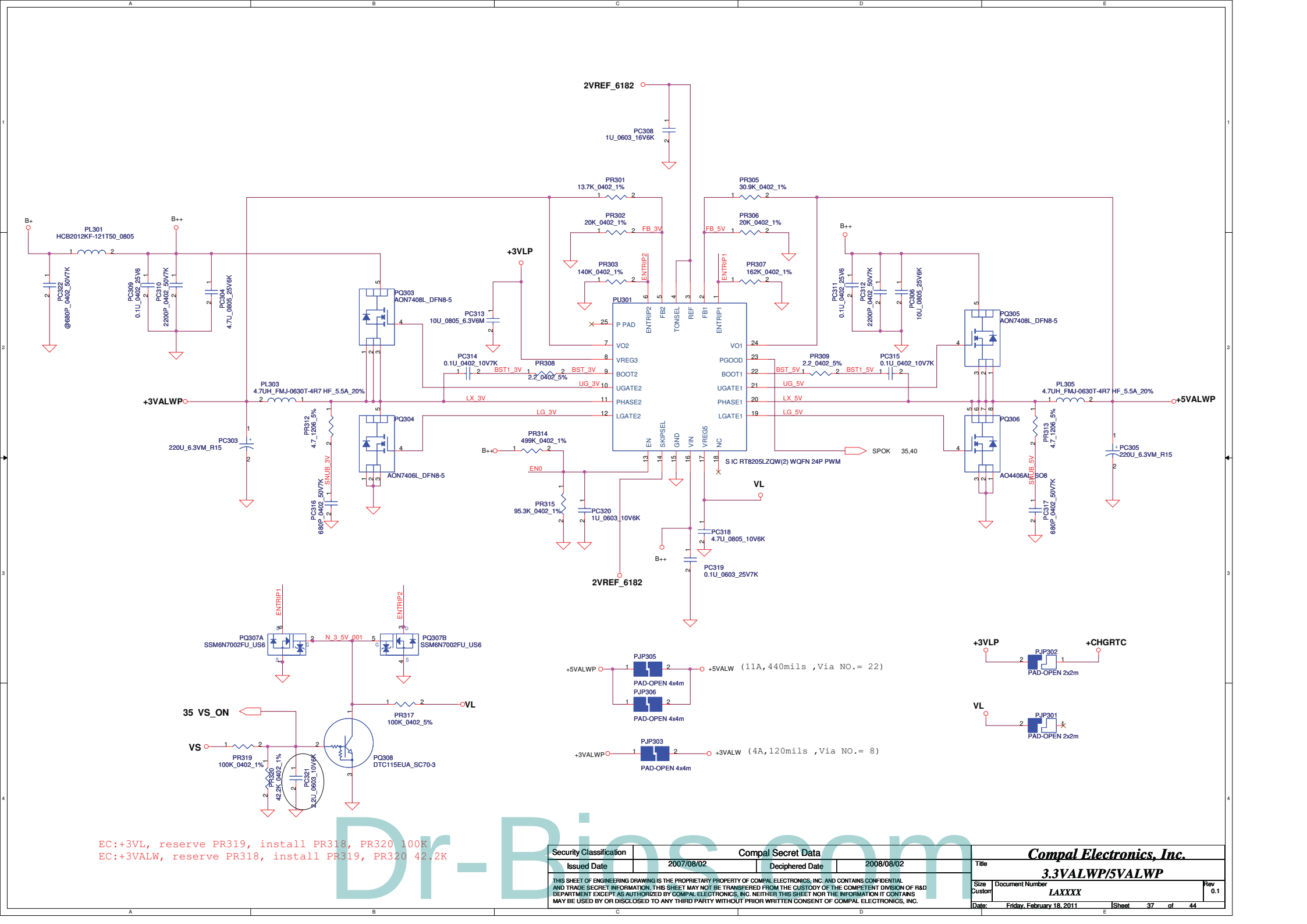
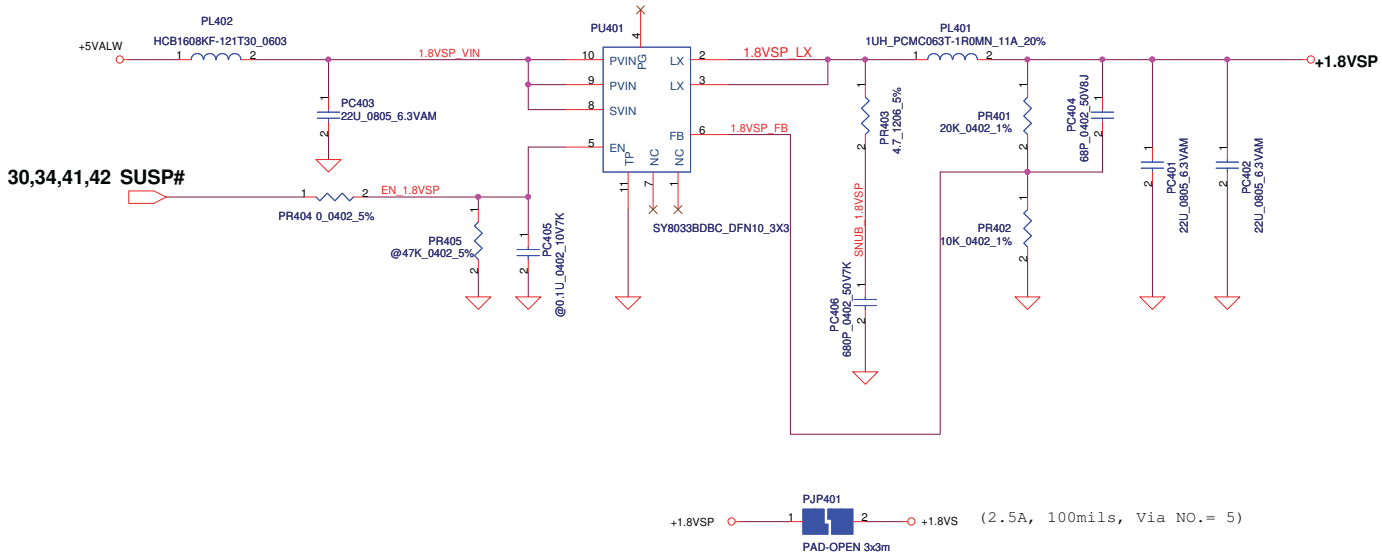


EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: LAXXXX		Rev: 0.1
Date: Friday, February 18, 2011	Sheet 37 of 44		

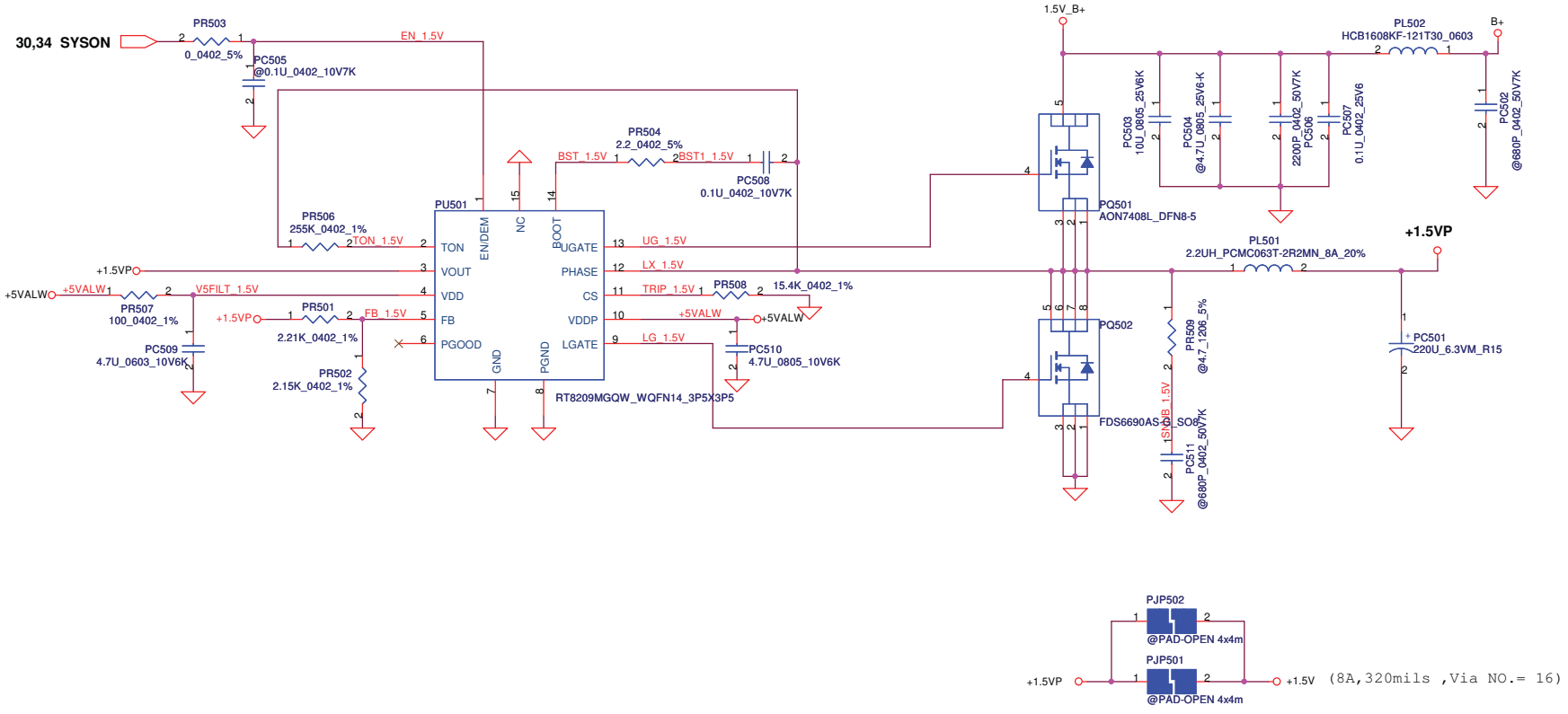


<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2.5A, 100mils, Via NO.= 5)

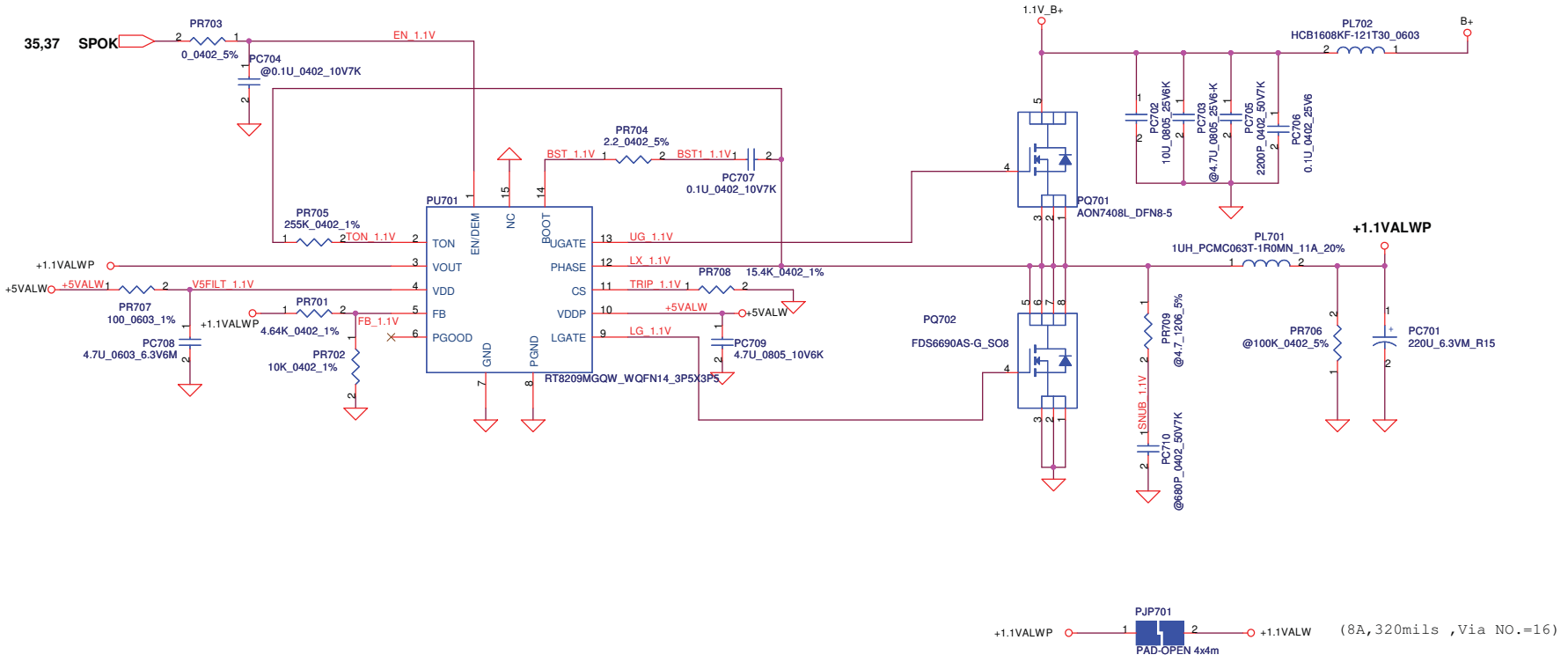
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	+1.8VSP
Size	Document Number: NCL61 LA-6321P M/B
Rev	0.1
Date: Friday, February 18, 2011	Sheet 38 of 44



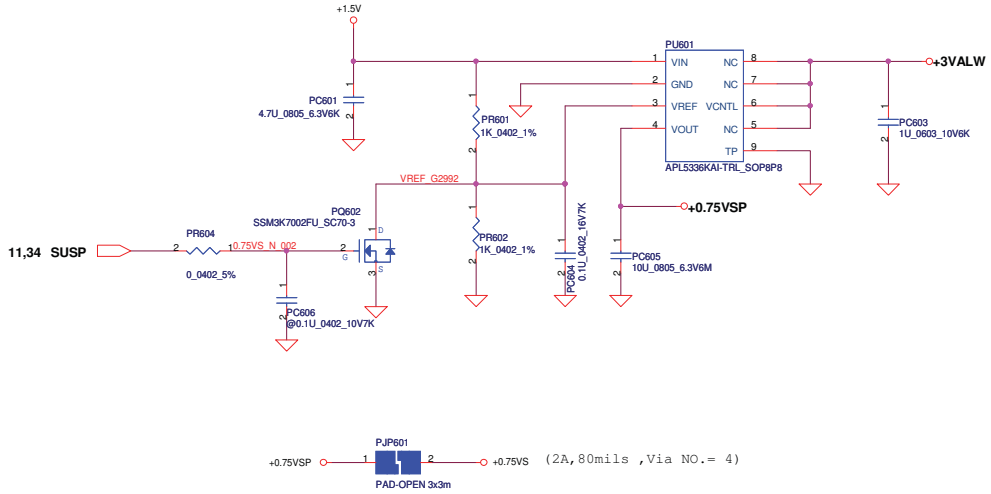
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title	+1.5VP		
Size	Document Number		Rev
	LAXXXX		0.1
Date:	Friday, February 18, 2011	Sheet	39 of 44

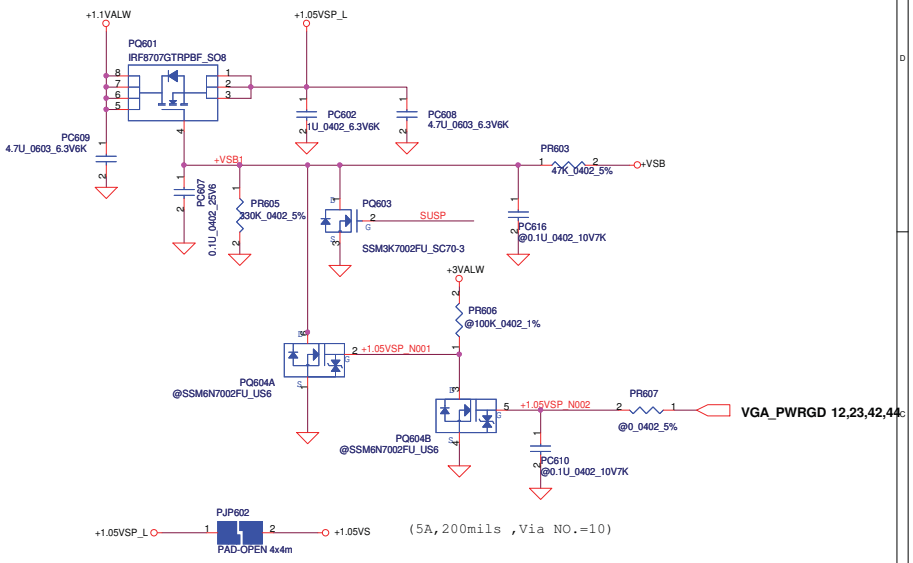


Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

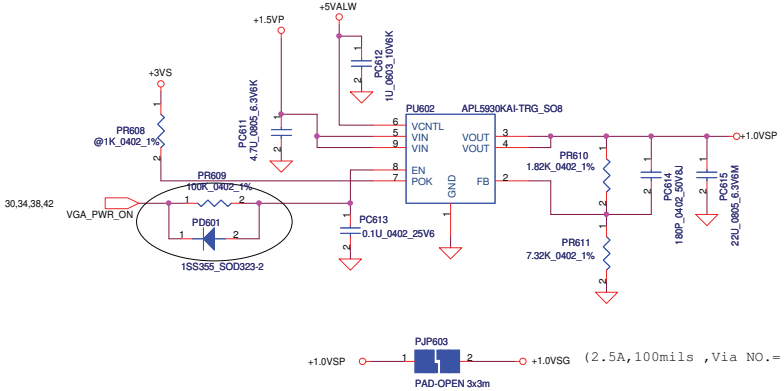
Compal Electronics, Inc.			
Title: PWR+1.1VALWP			
Size: Custom	Document Number: LAXXXX		Rev: 0.1
Date: Friday, February 18, 2011	Sheet 40 of 44		



+1.1VALW TO +1.05VSP



Need to confirm with HW power sequence.



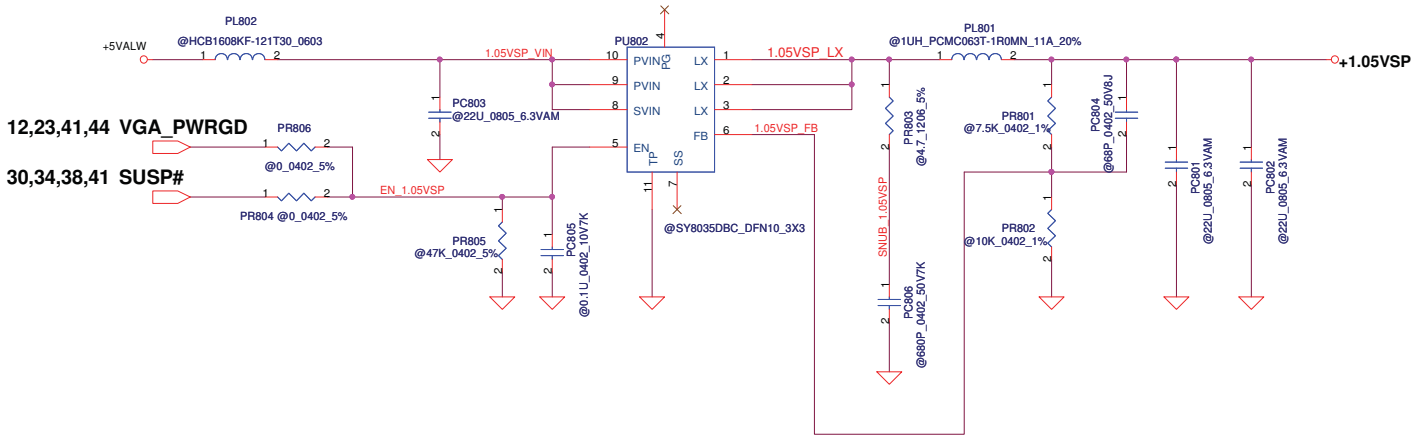
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: PWR 0.75VSP +1.05VSP

Size | Document Number: LAXXXX | Rev: 0.1

Date: Friday, February 18, 2011 | Sheet 41 of 44



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.05VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

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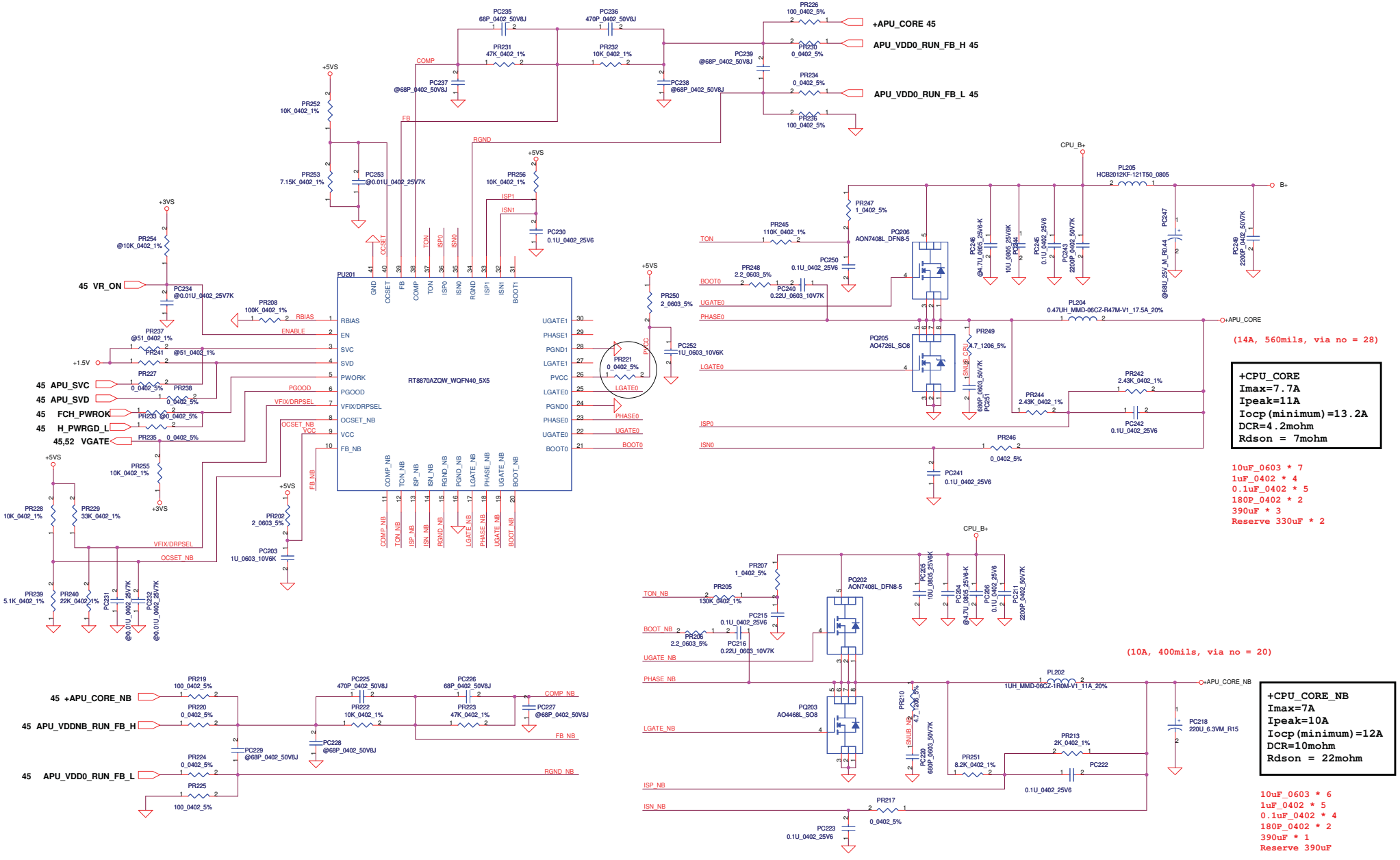
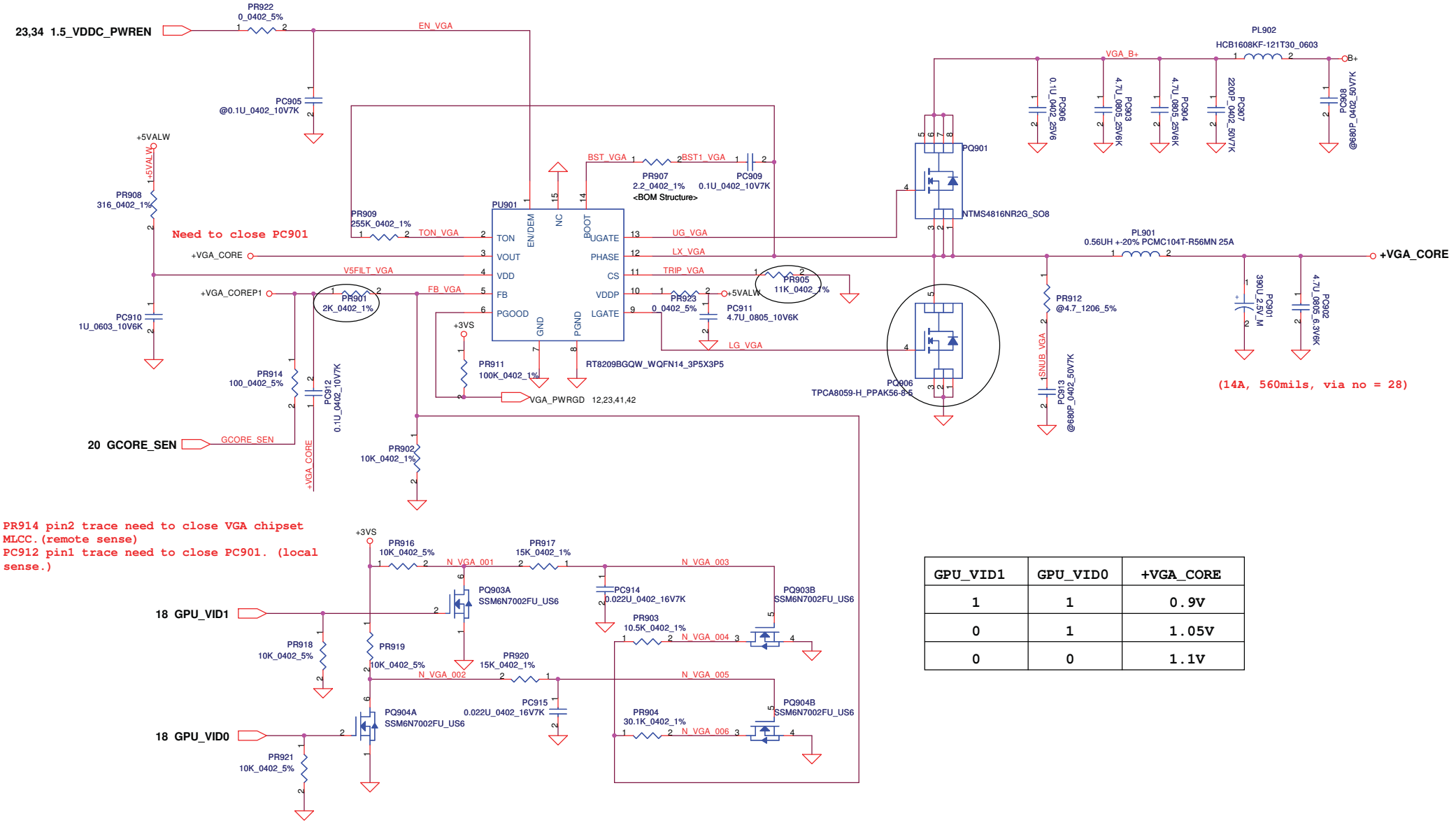


Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR-CPU_CORE			
Size: C	Document Number: LAXXXX		Rev: 0.1
Date: Friday, February 18, 2011	Sheet 43 of 44		

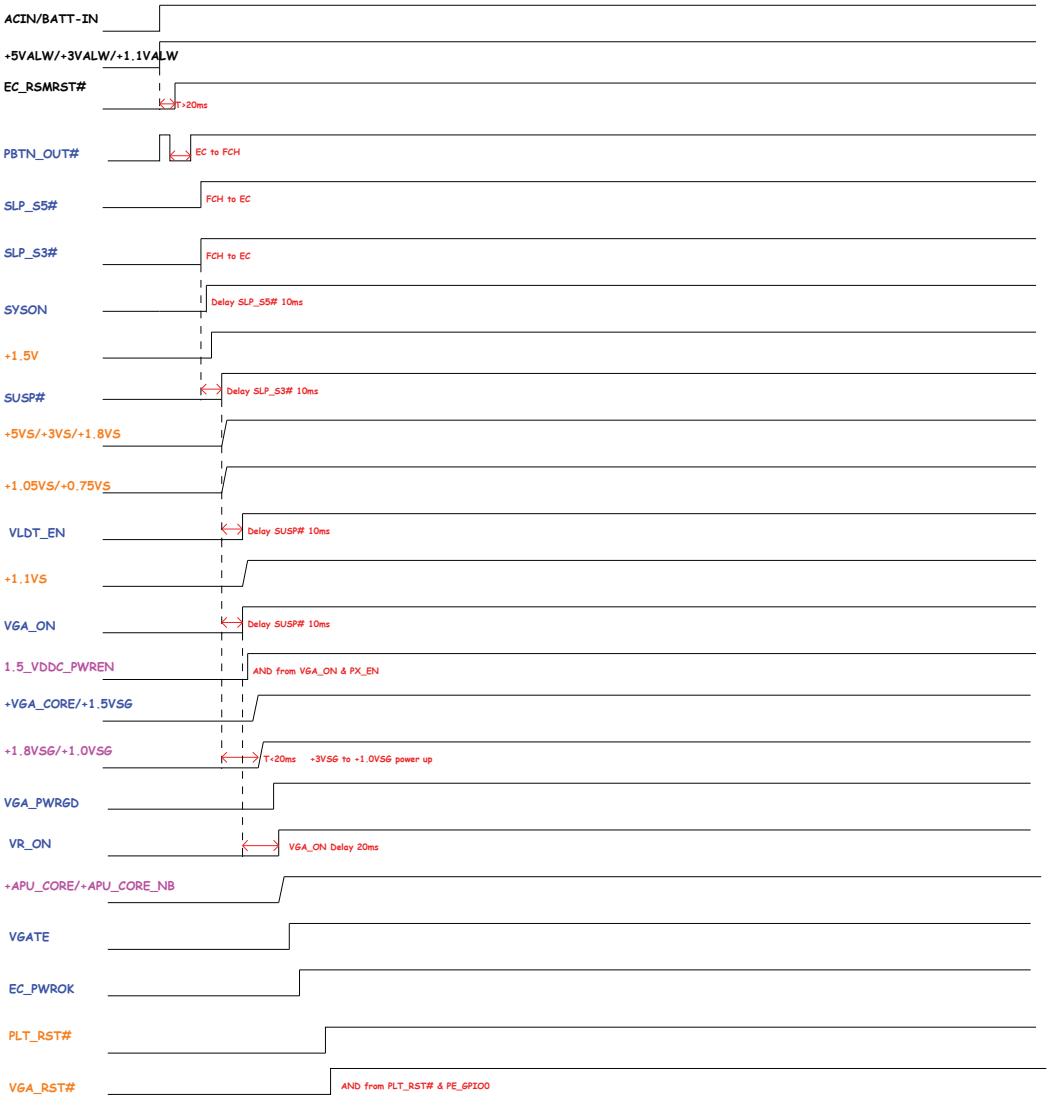


GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: VGA_CORE			
Size	Document Number: LAXXXX		Rev: 0.1
Date: Friday, February 18, 2011		Sheet 44 of 44	

POWER SEQUENCE



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2010/06/30

Title	Power Sequence	
Size	Document Number	Rev
	LA-7323P	1.0
Date: Thursday, February 10, 2011	Sheet 31 of 47	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		TP FFC error	0.11	PG#31	Swap JTP1 pin define	12/15	ER
2		SW5 SW6 footprint error	0.11	PG#31	Update SW5 SW6 footpint	12/15	ER
3		FAN module connecter pin define error	0.11	PG#33	Swap JFAN1 pin define	12/15	ER
4		DFB request to update footprint	0.11	PG#26 PG#33	Update JBTN1& JSPK1 footprint	12/15	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/15	ER
6		LID issue	0.11	PG#30	LID_SW# added a pull up 10Kohm. (R35)	12/15	ER
7		Update Broad ID	0.11	PG#30	Change R1606 from 26.1Kohm to 34.8Kohm	12/15	ER
8		Double component	0.11	PG#34	Del Q54 & R1102	12/15	ER
9		Update PW schematic	0.11			12/16	ER
10		APU_THERMTRIP# of FCH SPEC	0.11	PG#05	R424 & Q79 change to unpop, R427 change to pop	12/17	ER
11		EC release note	0.11	PG#30	Add C125 & R138	12/17	ER
12		Crasis circuit	0.12	PG#14	Add UH6,R512,R513,R514	12/20	ER
13		DDR3 SPD	0.12	PG#08	Reserve R155 R152	12/21	ER
14		Update PW schematic	0.13			12/23	ER
15		Clear CMOS	0.13	PG#12	R865 change to CLRP1	12/23	ER
16		Procurement recommend	0.13		D4,Q97,Q29 change PN & footprint	12/23	ER
17		WLAN PW spec	0.13	PG#28	Reserve Q31 ,Q32 circuit	12/24	ER
18		EMI request	0.13	PG#26	R1544 change to L121	12/24	ER
19		EMI request	0.13	PG#30	R1631 change to FBMA-10-100505-101T	12/24	ER
20		EMI request	0.13	PG#30	R516 change to 33ohm, C1535 change to 22P	12/24	ER
21		LAN power	0.13	PG#25	Add R553 & J8	12/27	ER
22		EMI request	0.13	PG#25	R549,R552,R1529,R1530 change to 0603	12/27	ER
23		Update PW schematic	0.13			12/27	ER
24		Crystal EA	0.2	PG#18	C35,C36 change to 18P from 20P	12/29	ER
25		Crystal EA	0.2	PG#25	C1634 change to 10P from 27P C1633 change to 12P from 27P	12/29	ER
26		Crystal EA	0.2	PG#12	C66 change to 8.2P from 22P C67 change to 10P from 22P	12/29	ER
27		PE_GPIO1 pull down	0.2	PG#12	Add R109 for PE_GPIO1	12/29	ER

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.		
Title: HW-PIR		
Size: Custom	Document Number: LA-7322P	Rev: 1.0
Date: Thursday, February 17, 2011	Sheet 46 of 47	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
28		Discharge time fail.	0.21	PG#34	Change R1110, R1101 from 470 ohm to 300 ,150 ohm.	01/11	ER
29		For frequency matching.	0.21	PG#12	Change Y4 from 12.5pF to 7 pF Change C64,C65 from 22p to 10pF.	01/11	ER
30		For CRT EA.	0.21	PG#10	Change C1572,C1573,C1574,C1575,C1576,C1577 from 10p to 6.8p. Change bead value.	01/11	ER
31		Change the strap for RAM.	0.21	PG#08 PG#09	Pop R153 and R155, un-pop R961,R150.	01/11	ER
32		Correct HDMI audio strap pin.	0.21	PG#18	Un-pop R21,R22 for DIS skew.	01/11	ER
33		Reserve for S3 can't be resume issue of some APU.	0.21	PG#06	Add R1705,R1706.	01/21	PR
34		For PR phase ME assemble.	0.21	PG#33	Del SW3 ,Unpop Sw4.	02/09	PR
35		For PR phase board ID.	0.22	PG#30	Change BID R1603 from 34.8k to 46.4k.	02/14	PR
36		For S3 resume fail issue.	1.0	PG#18	Add R75 1M ohm.	02/15	PR
37		For frequency matching.	1.0	PG#12	Change C66,C67 from 8.2pF 10pF p to 10pF 12pF.	02/16	PR
38		For frequency matching.	1.0	PG#25	C1634 change from 10P to 12P C1633 change from 12P to 15P	02/16	PR
39		For EMI test.	1.0	PG#32	Add C1508, C1505 220p.	02/17	PR
40		For EMI test.	1.0	PG#33	Add C1523 220p.	02/17	PR
41		For EMI test.	1.0	PG#26	Add C1506 220p.	02/17	PR
42		For only footprint.	1.0	PG#11	Del L11, L12, L13, L14	02/17	PR
43		For CRT EA.	1.0	PG#10	Change L116,L117,L118	02/17	PR
44			1.0	PG#10	Change R606 from 2.2k to 150 ohm.	02/17	PR
45		For LAN EMI test.	1.0	PG#25	Change TS1 from XXXXXX to SP050005L00	02/17	PR
46		For EMI request.	1.0	PG#30	Add C126 10 pF,change R516 to 39 ohm, C1535 to 33 pF.	02/17	PR
47							

Compal Electronics, Inc.
Title: HW-PIR
Size: Custom | Document Number: LA-7322P | Rev: 1.0
Date: Thursday, February 17, 2011 | Sheet 47 of 47