Compal Confidential

QBL60 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-21

LA-7552P REV: 0.1

Security Classification	Compal Secret Data		
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Title: Cover Page

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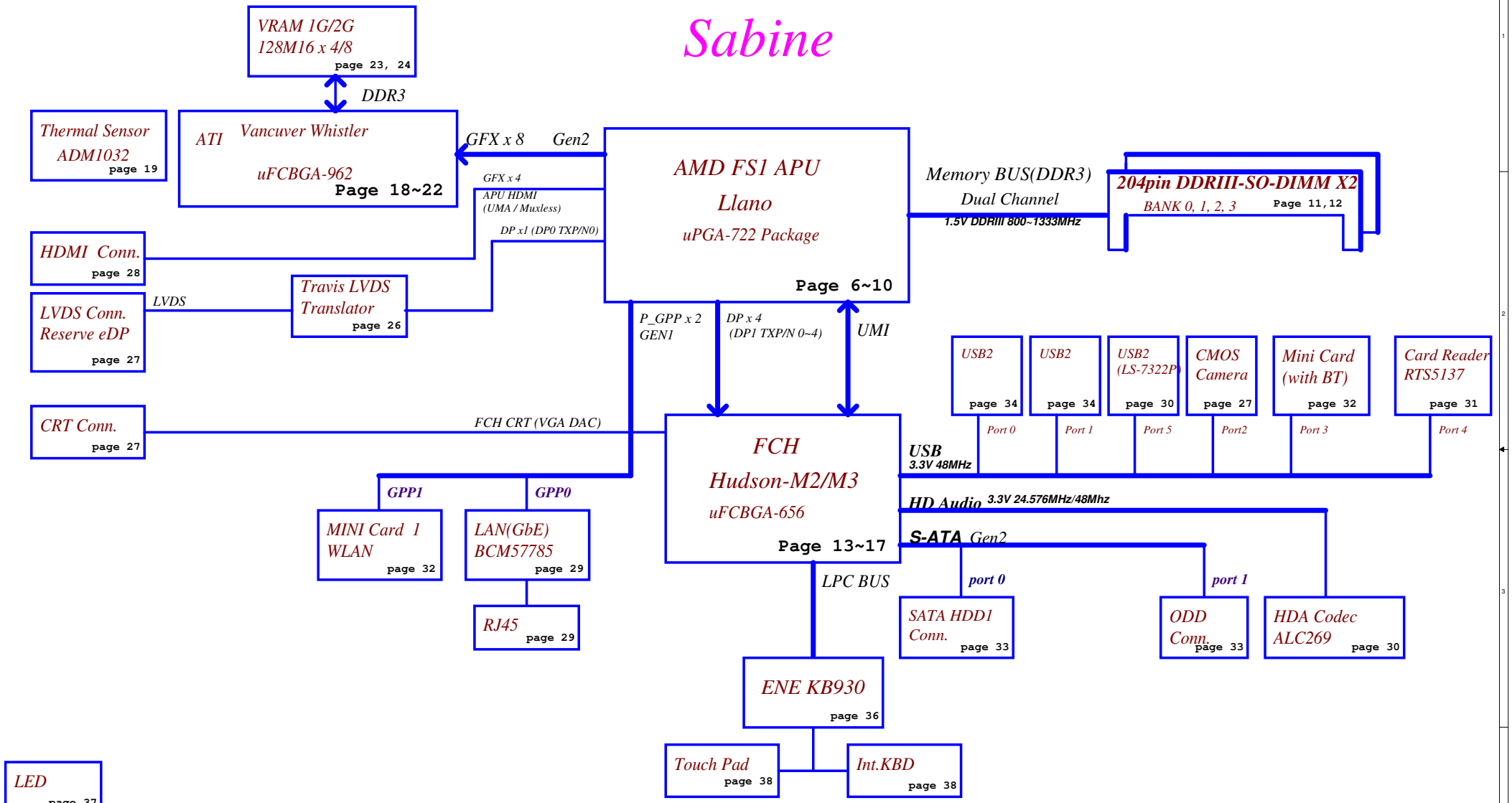
Compal Confidential

Model Name : QBL60



Security Classification	Compal Secret Data		
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Title: Block Diagrams

Size	Document Number	Rev
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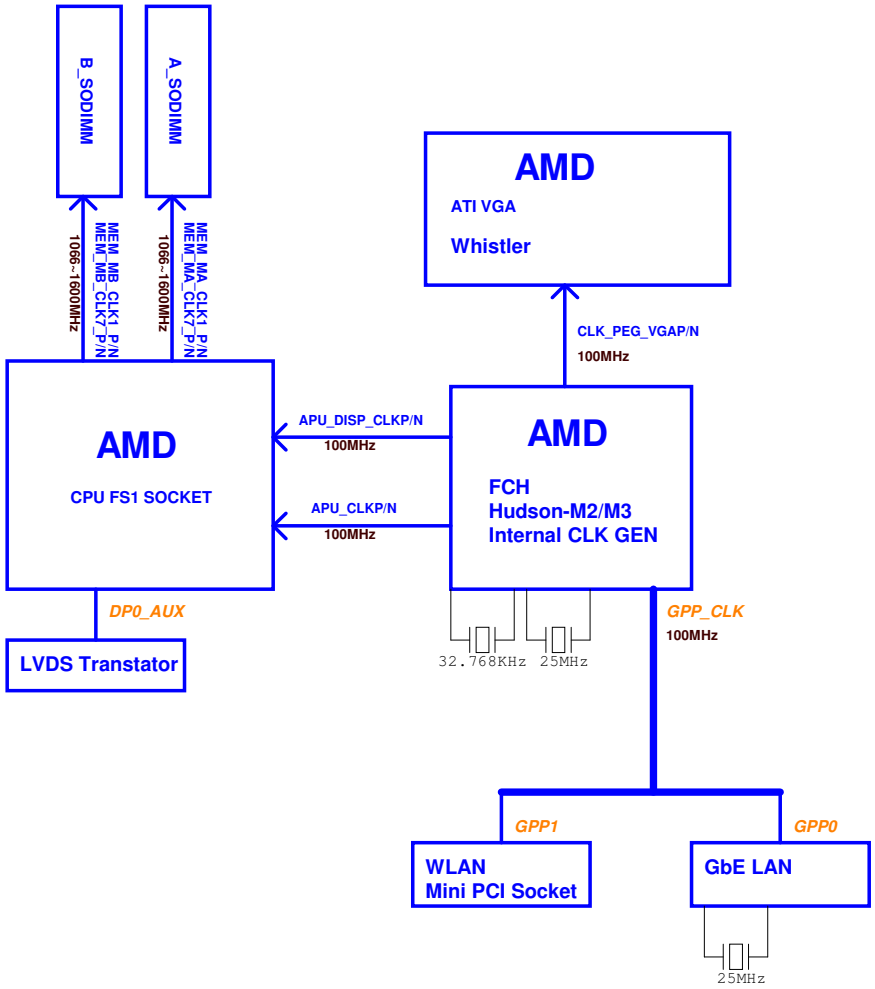
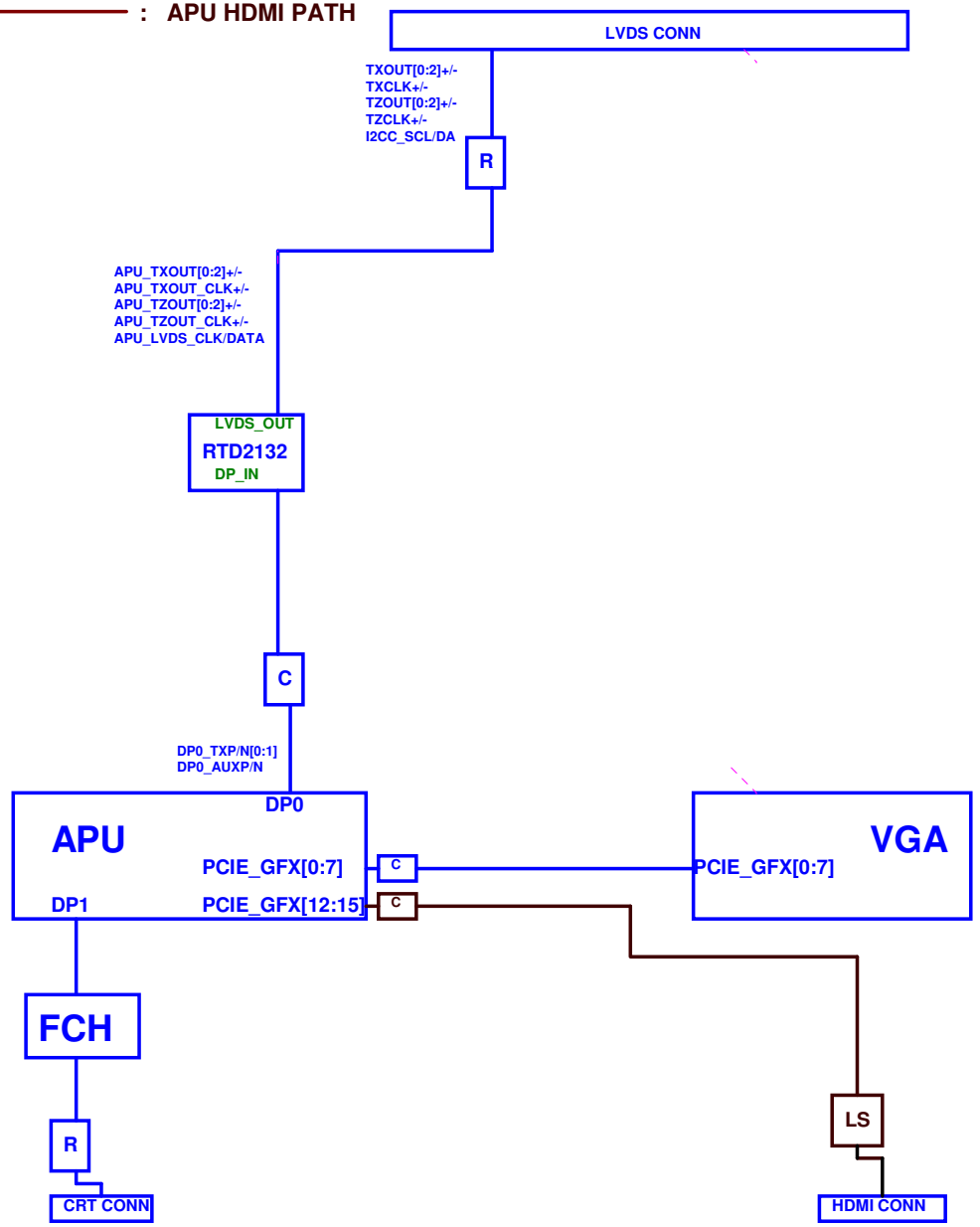
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title	CLOCK / DISPLAY DISTRIBUTION		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.1
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043I90

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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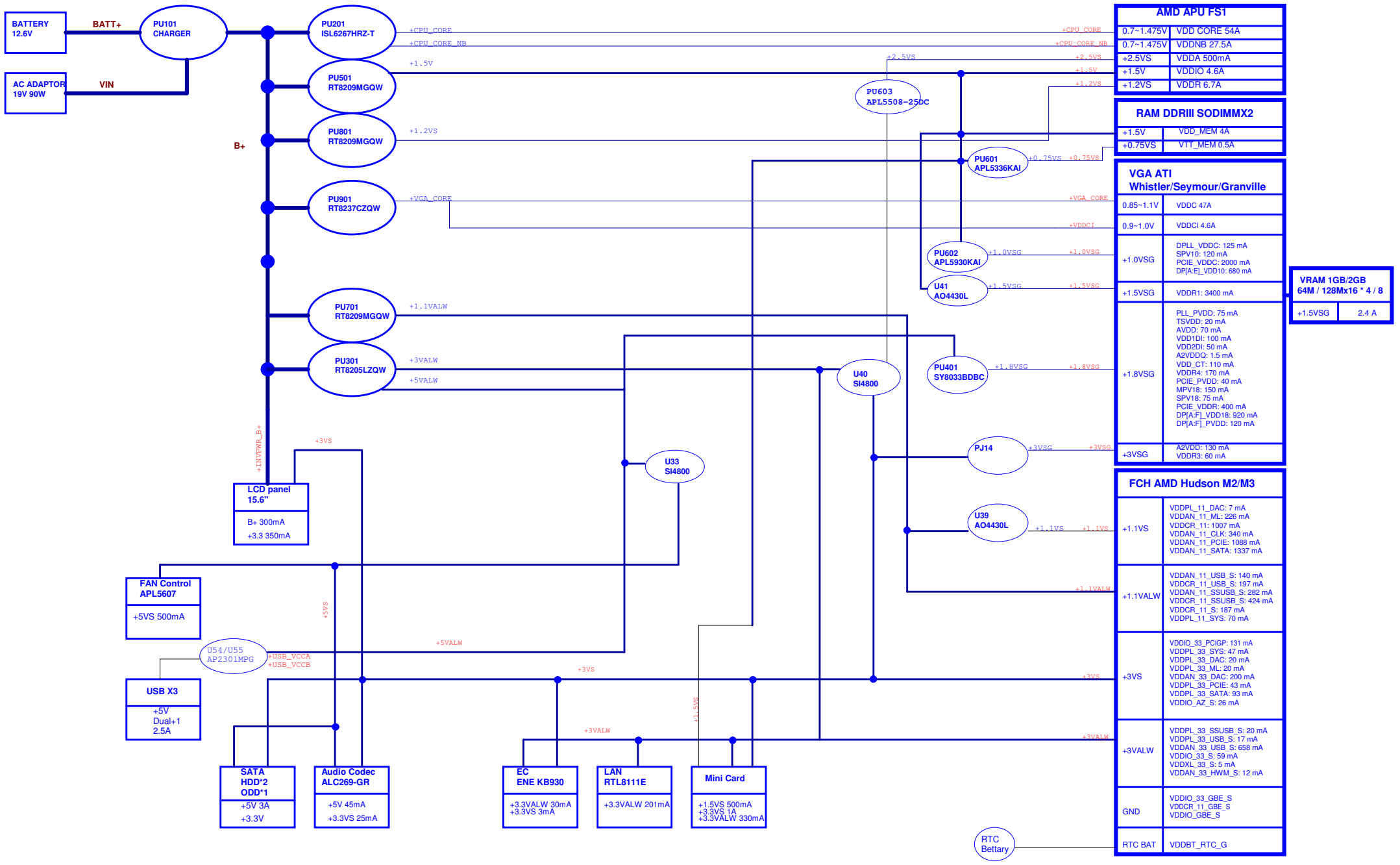

Security Classification	Compal Secret Data		
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Title: POWER DELIVERY CHART

Size	Document Number	Rev
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18 PCIE_GTX_C_FRX_P[0..7]
18 PCIE_GTX_C_FRX_N[0..7]

PCIE_FTX_C_GRX_P[0..7] 18
PCIE_FTX_C_GRX_N[0..7] 18

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

JCPU1A — CONN@

PCI EXPRESS — GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C917	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C918	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C919	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C920	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C921	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C922	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3	W8	P_GFX_RXP3	P_GFX_TXP3	W2	PCIE_FTX_GRX_P3	C923	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C924	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4	V7	P_GFX_RXP4	P_GFX_TXP4	V2	PCIE_FTX_GRX_P4	C925	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C926	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C927	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5	U6	P_GFX_RXN5	P_GFX_TXN5	V5	PCIE_FTX_GRX_N5	C928	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6	U8	P_GFX_RXP6	P_GFX_TXP6	U2	PCIE_FTX_GRX_P6	C929	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6	U9	P_GFX_RXN6	P_GFX_TXN6	U3	PCIE_FTX_GRX_N6	C930	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7	T7	P_GFX_RXP7	P_GFX_TXP7	T2	PCIE_FTX_GRX_P7	C931	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C932	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N7
	R5	P_GFX_RXP8	P_GFX_TXP8	T4					
	R6	P_GFX_RXN8	P_GFX_TXN8	T5					
	R8	P_GFX_RXP9	P_GFX_TXP9	R2					
	R9	P_GFX_RXN9	P_GFX_TXN9	R3					
	P7	P_GFX_RXP10	P_GFX_TXP10	P2					
	P8	P_GFX_RXN10	P_GFX_TXN10	P1					
	N5	P_GFX_RXP11	P_GFX_TXP11	P4					
	N6	P_GFX_RXN11	P_GFX_TXN11	P5					
	N8	P_GFX_RXP12	P_GFX_TXP12	N2	PCIE_FTX_GRX_P12				
	N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12				
	M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13				
	M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13				
	L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14				
	L6	P_GFX_RXN14	P_GFX_TXN14	M5	PCIE_FTX_GRX_N14				
	L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15				
	L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15				

For UMA Mux.

2
1
To HDMI
0
CK

GFP

29 PCIE_DTX_C_FRX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_DRX_P0	C950		0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29
29 PCIE_DTX_C_FRX_N0	AC6	P_GPP_RXN0	P_GPP_TXN0	AD5	PCIE_FTX_DRX_N0	C951		0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29
32 PCIE_DTX_C_FRX_P1	AC8	P_GPP_RXP1	P_GPP_TXP1	AC2	PCIE_FTX_DRX_P1	C952		0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32
32 PCIE_DTX_C_FRX_N1	AC9	P_GPP_RXN1	P_GPP_TXN1	AC3	PCIE_FTX_DRX_N1	C953		0.1U_0402_16V7K	PCIE_FTX_C_DRX_N1 32
	AB7	P_GPP_RXP2	P_GPP_TXP2	AB2					
	AB8	P_GPP_RXN2	P_GPP_TXN2	AB1					
	AA5	P_GPP_RXP3	P_GPP_TXP3	AB4					
	AA6	P_GPP_RXN3	P_GPP_TXN3	AB5					

GLAN

WLAN

UMI-LINK

13 UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C956		0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13
13 UMI_MTX_C_FRX_N0	AF7	P_UMI_RXN0	P_UMI_TXN0	AF2	UMI_FTX_MRX_N0	C957		0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 13
13 UMI_MTX_C_FRX_P1	AE6	P_UMI_RXP1	P_UMI_TXP1	AF5	UMI_FTX_MRX_P1	C958		0.1U_0402_16V7K	UMI_FTX_C_MRX_P1 13
13 UMI_MTX_C_FRX_N1	AE5	P_UMI_RXN1	P_UMI_TXN1	AF4	UMI_FTX_MRX_N1	C959		0.1U_0402_16V7K	UMI_FTX_C_MRX_N1 13
13 UMI_MTX_C_FRX_P2	AE9	P_UMI_RXP2	P_UMI_TXP2	AE3	UMI_FTX_MRX_P2	C960		0.1U_0402_16V7K	UMI_FTX_C_MRX_P2 13
13 UMI_MTX_C_FRX_N2	AE8	P_UMI_RXN2	P_UMI_TXN2	AE2	UMI_FTX_MRX_N2	C961		0.1U_0402_16V7K	UMI_FTX_C_MRX_N2 13
13 UMI_MTX_C_FRX_P3	AD8	P_UMI_RXP3	P_UMI_TXP3	AD1	UMI_FTX_MRX_P3	C962		0.1U_0402_16V7K	UMI_FTX_C_MRX_P3 13
13 UMI_MTX_C_FRX_N3	AD7	P_UMI_RXN3	P_UMI_TXN3	AD2	UMI_FTX_MRX_N3	C963		0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13

+1.2VS — R539 1 2 196_0402_1%

P_ZVDDP	K5	P_ZVDDP	P_ZVSS
		K4	P_ZVSS

P_ZVSS — R540 1 2 196_0402_1%

AMD_TOPEDO_FS-1

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

C935 1 2 0.1U_0402_16V4Z

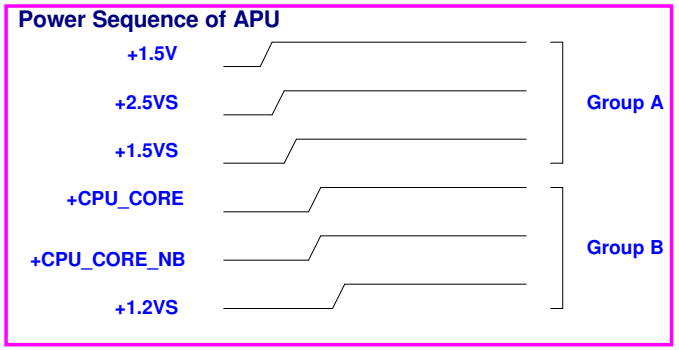
+3VS — R535 1 2 31.6K_0402_1% — R536 1 2 30K_0402_1%

8,14 APU_SID — APU_SID — Q9 BSH111 1N_SOT23-3 — EC_SMB_DA — R537 0_0402_5% — EC_SMB_DA2 19,26,36

8,14 APU_SIC — APU_SIC — Q10 BSH111 1N_SOT23-3 — EC_SMB_CK — R538 0_0402_5% — EC_SMB_CK2 19,26,36

To EC

Power Sequence of APU



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Compal Electronics, Inc.

Title: AMD FS1 PCIE / UMI / TSI

Size	Document Number	Rev
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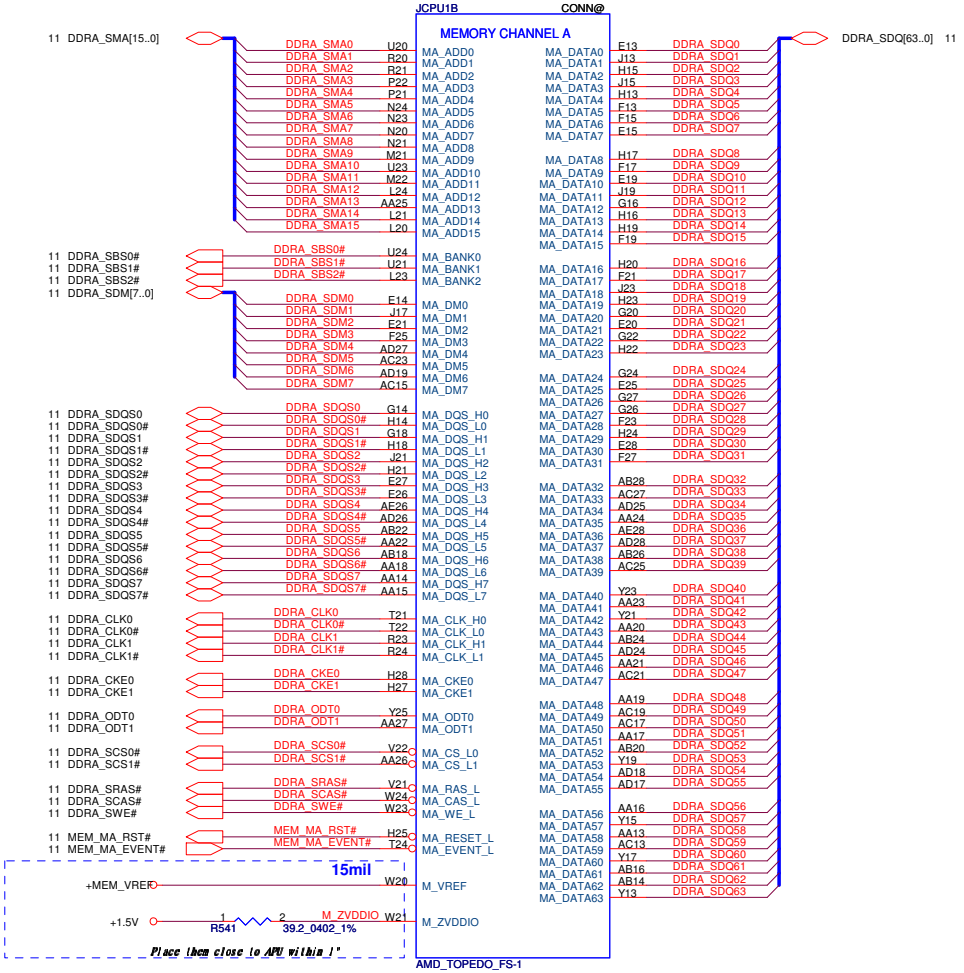

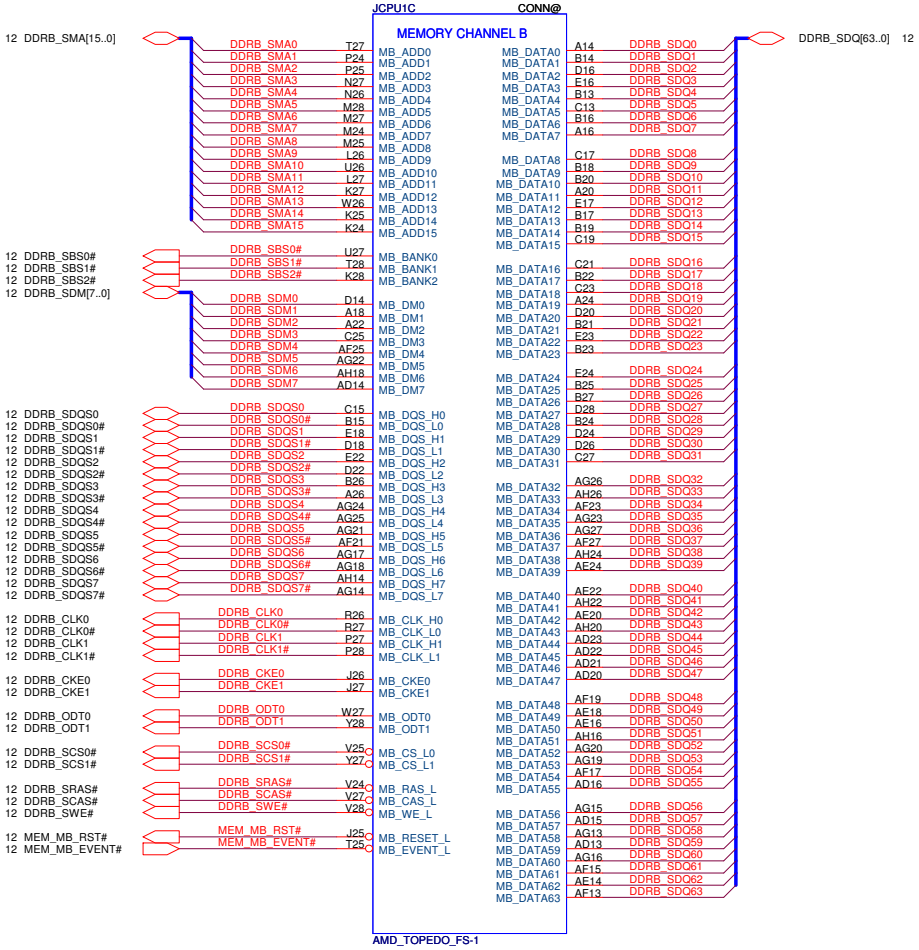

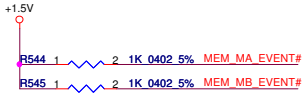

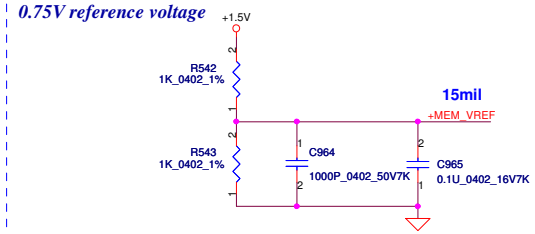

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: AMD FS1 DDRIII I/F

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

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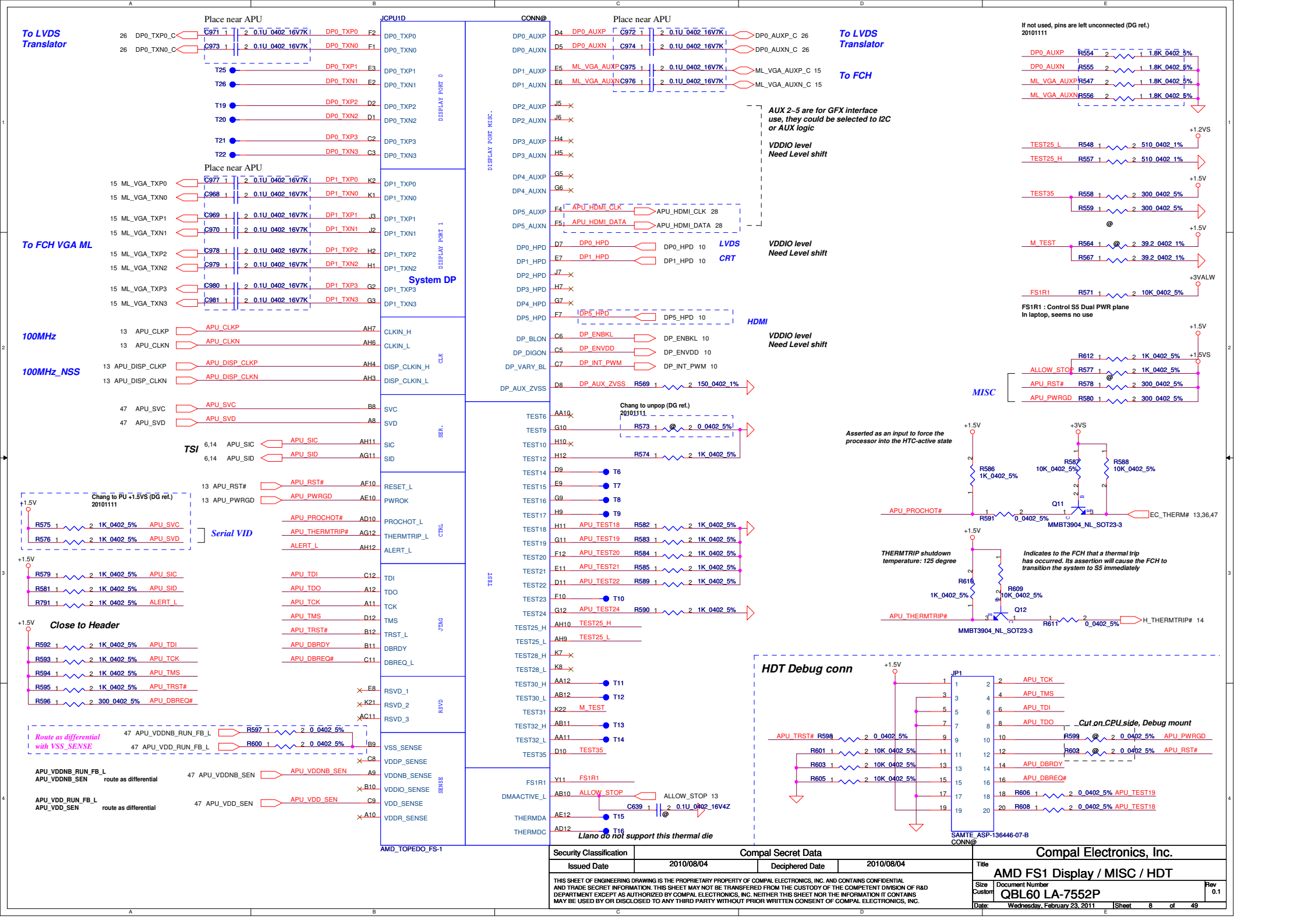

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: AMD FS1 Display / MISC / HDT

Size	Document Number	Rev
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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

CPU BOTTOM SIDE DECOUPLING

+CPU_CORE: C982 22U_0805_6.3V6M; C996 22U_0805_6.3V6M; C983 22U_0805_6.3V6M; C984 22U_0805_6.3V6M; C997 22U_0805_6.3V6M; C985 22U_0805_6.3V6M; C986 22U_0805_6.3V6M; C987 0.22U_0603_16V4Z; C988 0.22U_0603_16V4Z; C989 0.01U_0402_16V7K; C990 0.01U_0402_16V7K; C991 0.01U_0402_16V7K; C992 180P_0402_50V8J; C993 180P_0402_50V8J; C994 390U_2.5V_10M; C999 390U_2.5V_10M; C985 390U_2.5V_10M; 390U_2.5V_10M

+CPU_CORE_NB: C1000 22U_0805_6.3V6M; C1001 22U_0805_6.3V6M; C1002 22U_0805_6.3V6M; C1003 22U_0805_6.3V6M; C1004 0.22U_0603_16V4Z; C1005 0.22U_0603_16V4Z; C1006 180P_0402_50V8J; C1007 180P_0402_50V8J; C1008 180P_0402_50V8J; C1009 180P_0402_50V8J; C1010 390U_2.5V_10M; C1011 390U_2.5V_10M; 390U_2.5V_10M; <Bom Structure>

+CPU_CORE: C1014 390U_2.5V_10M; C1015 390U_2.5V_10M; 390U_2.5V_10M

+1.5V: C1012 22U_0805_6.3V6M; C1013 22U_0805_6.3V6M; C14 4.7U_0603_6.3V6K; C15 4.7U_0603_6.3V6K; C16 4.7U_0603_6.3V6K; C17 4.7U_0603_6.3V6K; C1018 0.22U_0603_16V4Z; C1019 0.22U_0603_16V4Z; C1020 0.22U_0603_16V4Z; C1021 0.22U_0603_16V4Z; C1022 0.22U_0603_16V4Z; C1023 0.22U_0603_16V4Z; C1024 180P_0402_50V8J; C1025 180P_0402_50V8J; C5 330U_D2.2V_Y

+1.5V: C1027 0.22U_0603_16V4Z; C1028 0.22U_0603_16V4Z; C1029 180P_0402_50V8J; C1030 180P_0402_50V8J

Decoupling between CPU and DIMMs across VDDIO and VSS split

JCPU1E CONN@ — AMD_TOPEDO_FS-1

2000mil	+CPU_CORE	C1 D3 D6 E1 F3 F6 F8 G1 H3 H6 H8 J1 K3 K6 L1 L11 L19 M3 M6 M10 M18 N1 N11 N19 P3 P6 P10 P18 R1 R11 R19 T3	VDD
2000mil	+CPU_CORE	T6 T10 T18 U1 U11 U19 V3 V6 V10 V18 W1 W11 W13 W15 W17 W19 Y3 Y6 Y10 Y12 Y14 Y16 Y18 Y20 AA1 AB3 AB6 AC1 AD3 AD6 AE1	VDD
900mil	+CPU_CORE_NB	J9 J10 J11 J12 J14 J16 K9 K10	VDDNB
900mil	+CPU_CORE_NB	K11 K12 K13 K14 K16 K17 K18 L18	VDDNB
160mil	+1.5V	G28 H26 J28 K20 K23 K26 L22 L25 L28 M20 M23 M26 N22 N25 N28 P20 P23 P26	VDDIO
160mil	+1.5V	R22 R25 R28 T20 T23 T26 U22 U25 U28 V20 V23 V26 W22 W25 W28 Y24 Y26 AA28	VDDIO
120mil	+1.2VS	AG2 AG3 AG4 AG5	VDDP_A_1 VDDP_A_2 VDDP_A_3 VDDP_A_4
120mil		A3 A4 B3 B4	VDDP_B_1 VDDP_B_2 VDDP_B_3 VDDP_B_4
160mil	+1.2VS	AG6 AG7 AG8 AG9	VDDR
160mil		A5 A6 B5 B6	VDDR
40mil	+VDDA_APU	AE11 AF11	VDDA
			VDDA

+2.5VS — L1 FBMA-L11-201209-221LMA30T_0805 — +VDDA_APU

C1040 3300P_0402_50V7K; C1041 0.22U_0603_16V4Z; C18 4.7U_0805_10V4Z; C1043 180P_0402_50V8J

Keep trace from resistor to APU within 0.6"

Keep trace from Caps to APU within 1.2"

C18 & C1043 follow AMD request 201012061900

VDDP decoupling

+1.2VS: C8 10U_0603_6.3V6M; C7 10U_0603_6.3V6M; C6 10U_0603_6.3V6M; C1034 180P_0402_50V8J; C1035 180P_0402_50V8J; C1036 180P_0402_50V8J; C1037 0.22U_0603_16V4Z; 0.22U_0603_16V4Z

+1.2VS: C1038 220U_6.3V_M

C1038 change to SF000002Y00 20101228

VDDR decoupling

+1.2VS: C1044 180P_0402_50V8J; C1045 180P_0402_50V8J; C1046 180P_0402_50V8J; C1047 180P_0402_50V8J; C1048 180P_0402_50V8J; C1049 1000P_0402_50V7K; C1050 1000P_0402_50V7K; C1051 1000P_0402_50V7K; 1000P_0402_50V7K

C1052 0.22U_0603_16V4Z; C1053 0.22U_0603_16V4Z; C1054 0.22U_0603_16V4Z; C1055 0.22U_0603_16V4Z; C10 4.7U_0603_6.3V6K; C11 4.7U_0603_6.3V6K; C12 4.7U_0603_6.3V6K; C13 4.7U_0603_6.3V6K

Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

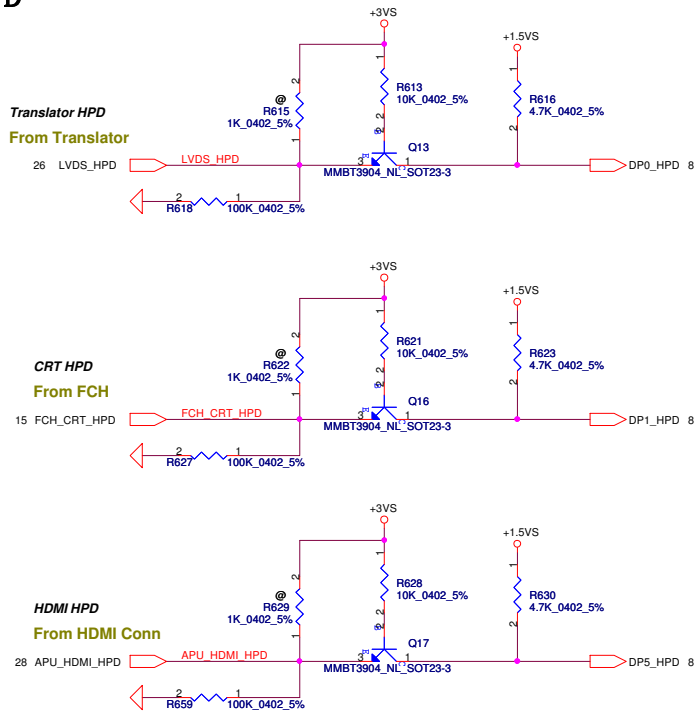
Compal Electronics, Inc.

Title: AMD FS1 PWR / GND

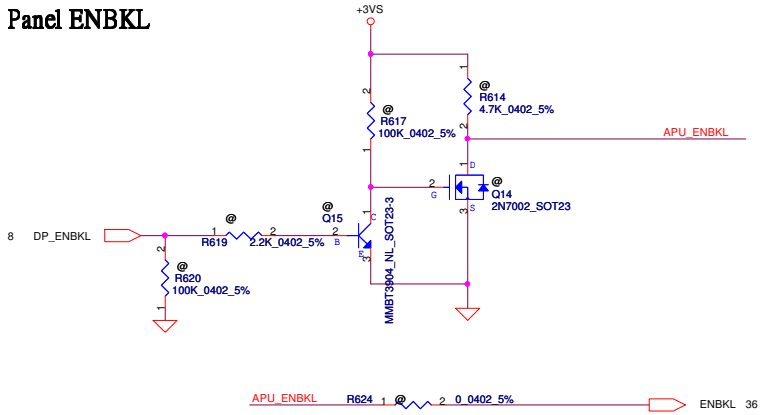
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 9 of 49

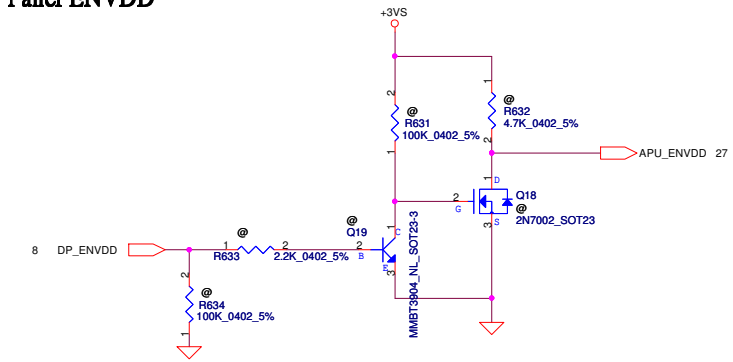
HPD



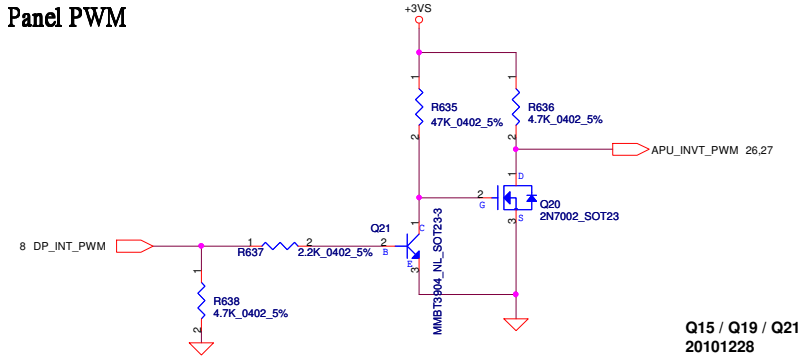
Panel ENBKL



Panel ENVDD



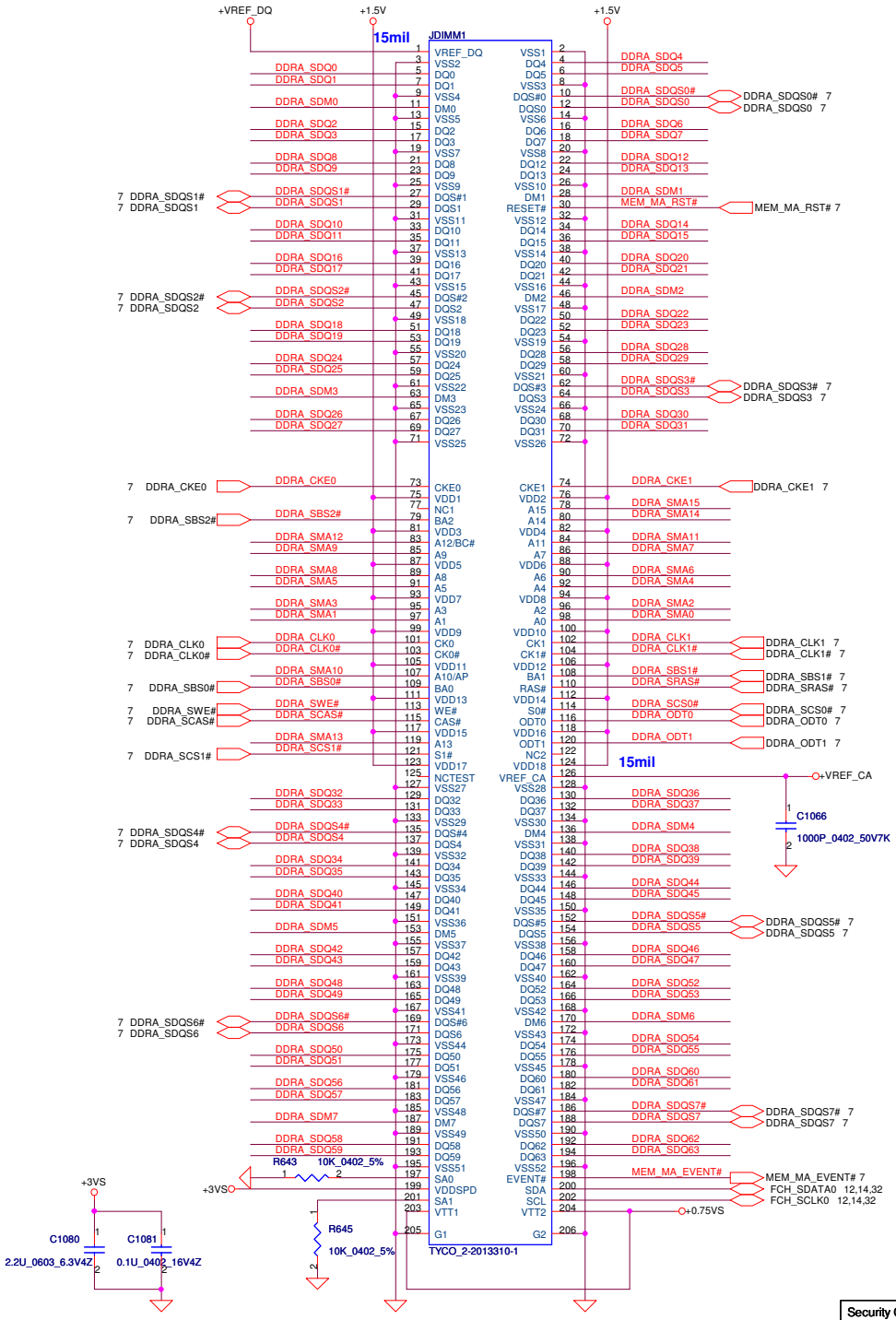
Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title	AMD FS1 Singal Level Shifter		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.1
Date: Wednesday, February 23, 2011	Sheet 10 of 49		

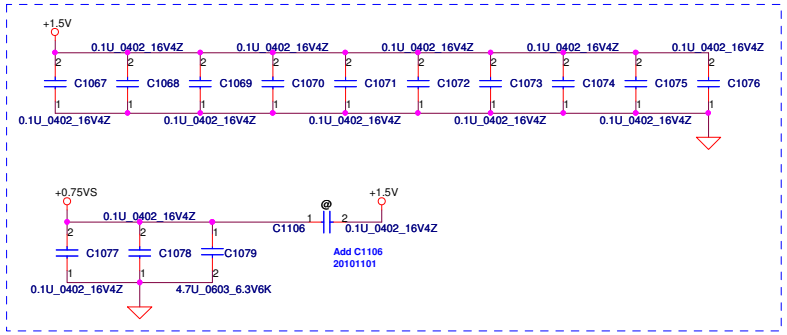


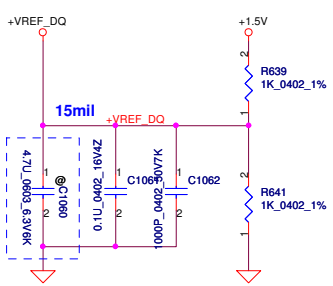
DIMM_A STD H:9.2mm

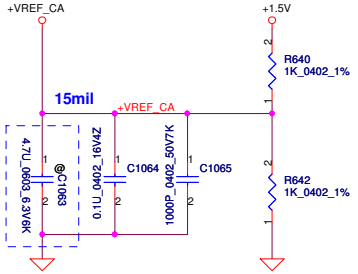
<Address: 00>

DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 7
DDRA_SDM[0..7] → DDRA_SDM[0..7] 7
DDRA_SMA[0..15] → DDRA_SMA[0..15] 7

Place near DIMM1







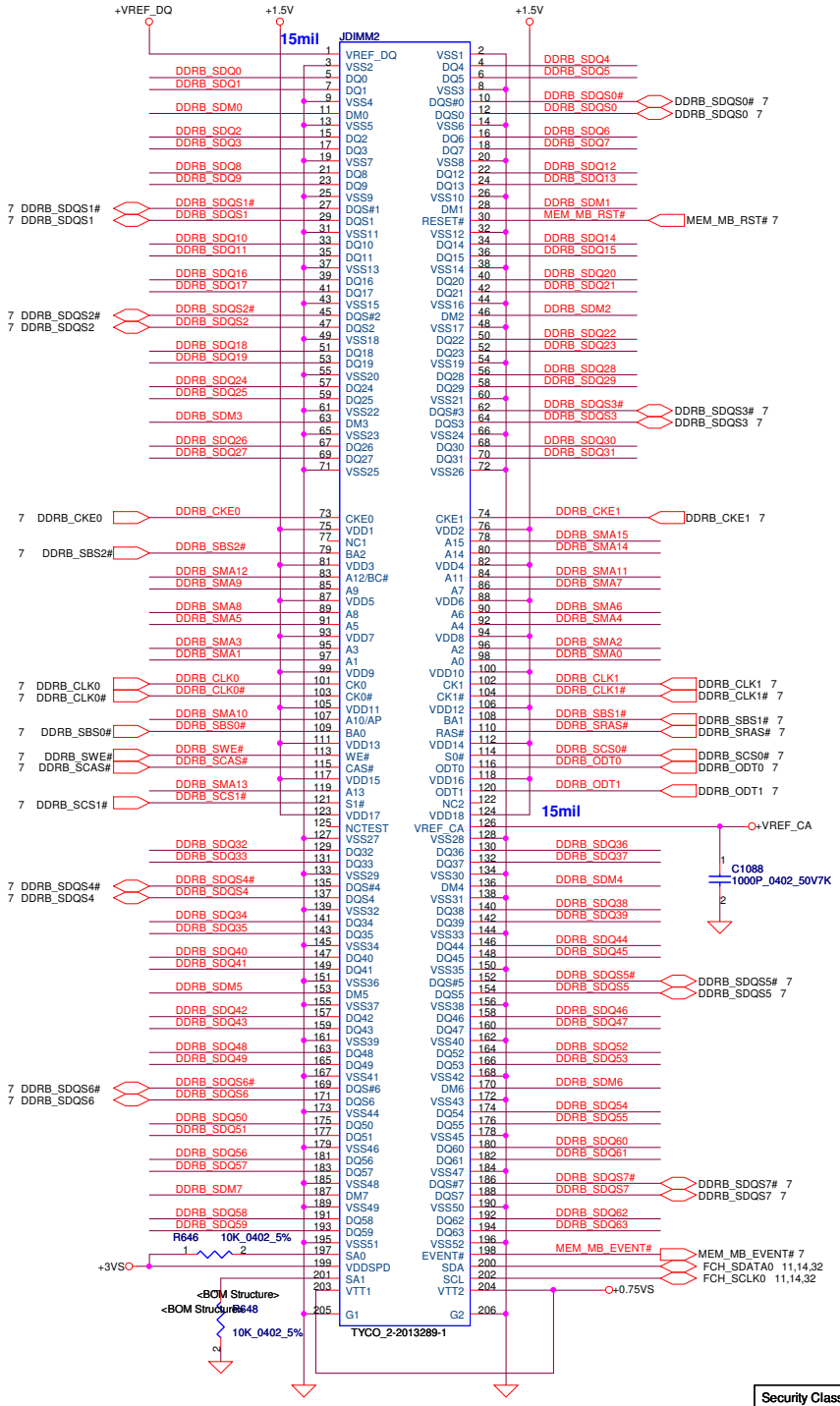
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 11 of 49



DIMM_B STD H:5.2mm

<Address: 01>

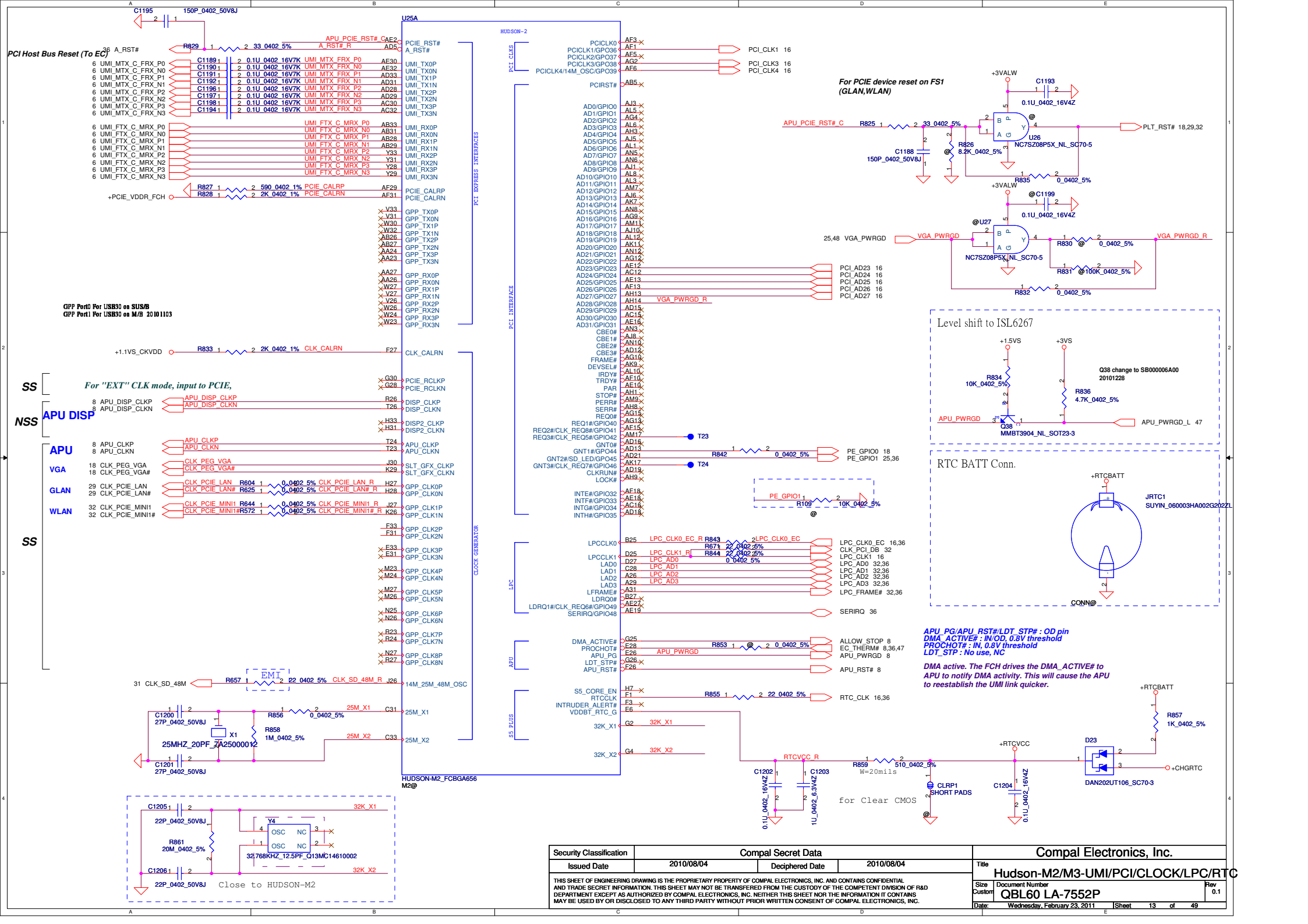
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 12 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 13 of 49

PCIE_RST2 : Reset PCIE device on Hudson2

U25D

HUDSON-2

THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain
VGA_PD: Support MLDAC power save if connect
0: MLDAC power on
1: MLDAC power off

Modify 2010212-AMD request

Modify 20101111

Project SKU ID

GPIO189 (use VGA)	L(NO)	H(YES)
	R44	R43
GPIO190 (use PX)	L(NO)	H(YES)
	R46	R45
GPIO191	L(15")	H(17")
	R48	R47

Add Project ID Table 201011301600

For FCH internal debug use

HUDSON-M2_FCBGA656
M2@

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
USB1
Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
CardReder
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2
WLAN(BT)
CMOS
USB3
USB2
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
On board USB Conn

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

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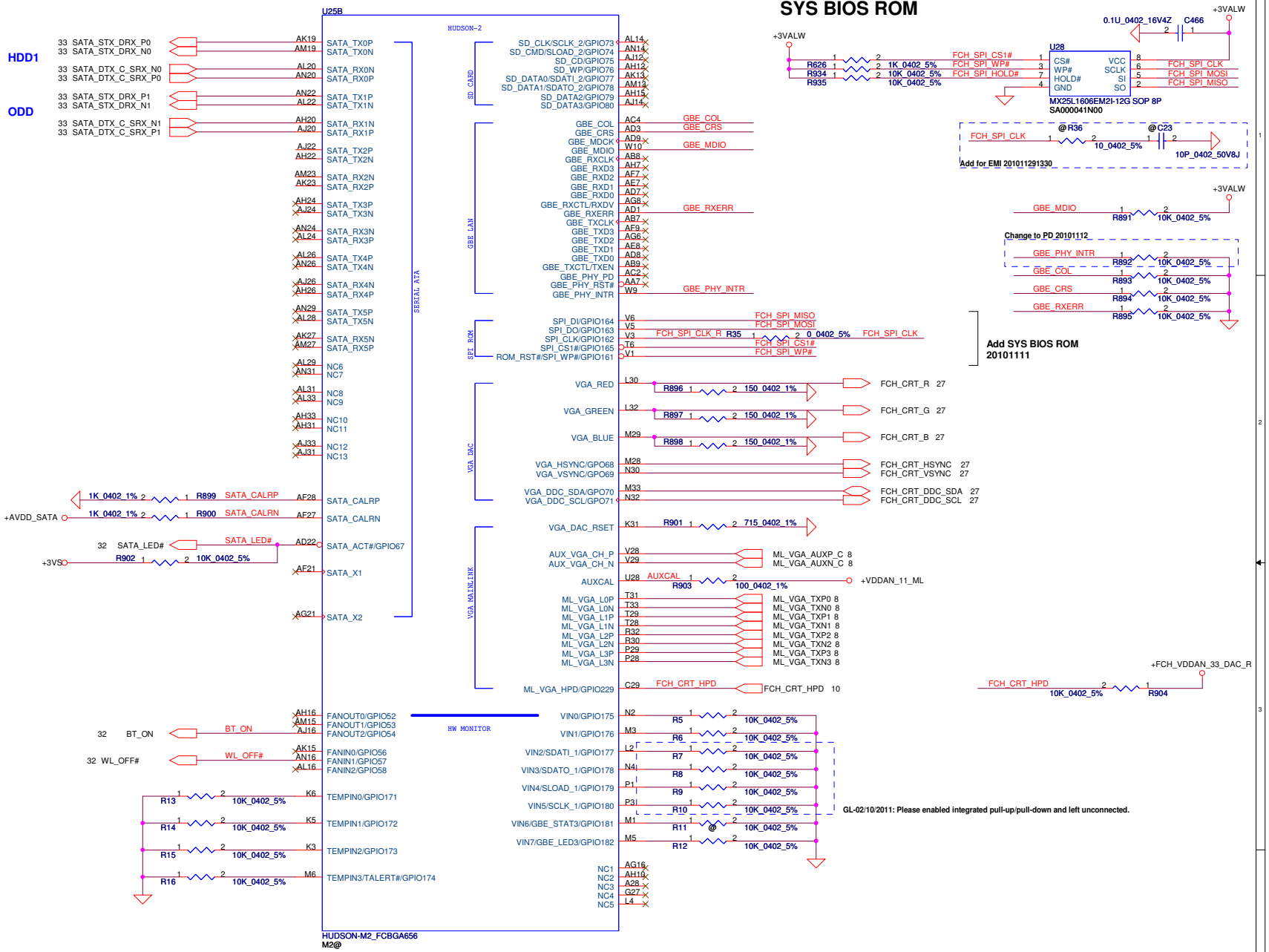
SYS BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

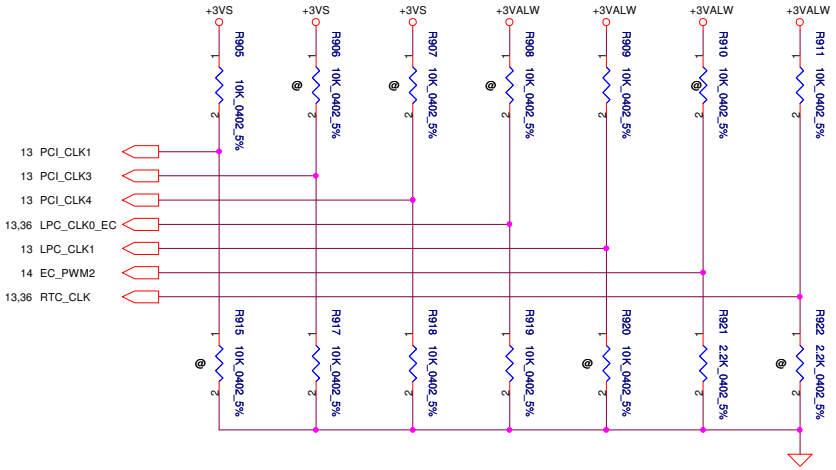
Title: Hudson-M2/M3-SATA/GBE/HWM

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 15 of 49

STRAP PINS

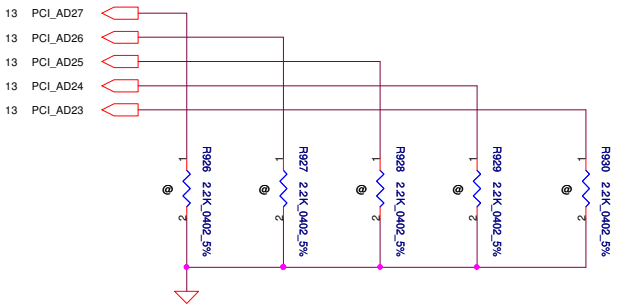
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

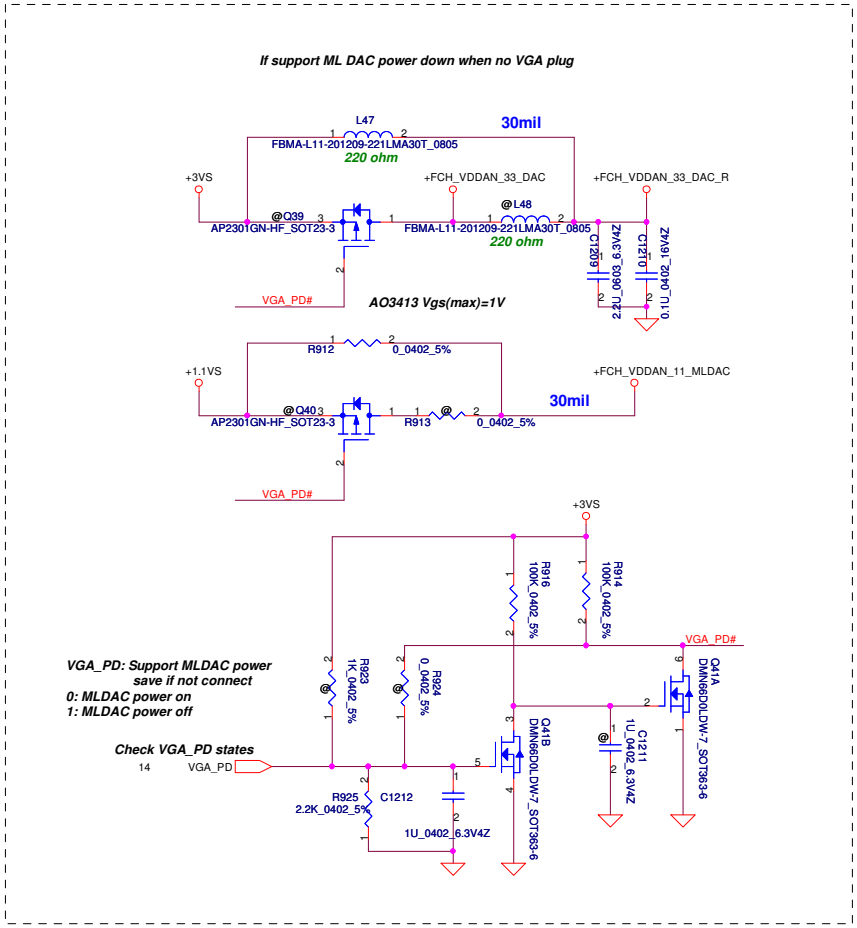


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 16 of 49

C1218 / C1219 / C1247 Change to SE00000I10
20101228

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB outputs

For A11: Cap = 1nF
For A12, Cap = DNI

change to 0ohm-AMD request 20110212

R1242 change to 2.2uf-AMD request 20110212

change to four 1uf-AMD request 20110212

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

Connected to VSS through a dedicated via.

For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S
Connected to VSS.

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

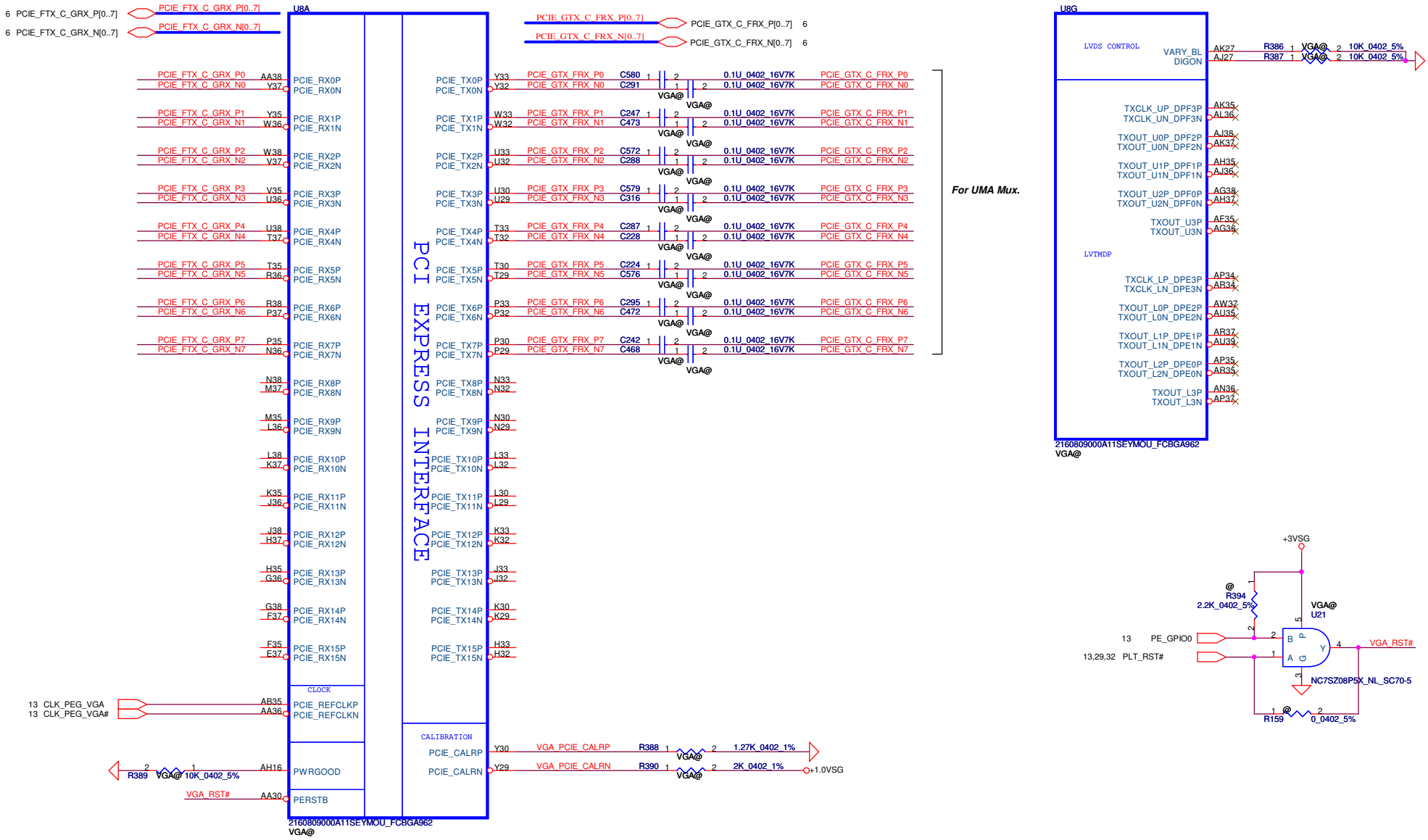
Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 17 of 49

GFX PCIE LANE REVERSAL



<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 Sheet 18 of 49

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 128 MB 000 / 256 MB 001 * / 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

External VGA Thermal Sensor

U9 VGA@ ADM1032ARMZ-2REEL_MSOP8

VRAM ID

VRAM \ Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004G330 64M16x8 K4W1G1646G-BC11	0	0	0	0
Samsung SA00004QA0 128M16x8 K4W2G1646C-HC11	0	0	0	1
Hynix SA00001560 64M16x8 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16x8 H5TQ2G63BFR-11C	0	1	0	1

GPIO5 fast-power reduction:
HW control will casue display disturb should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N,

GPIO7 Controls backlight on/off.
Active High ,need external PD
If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt
Critical temperature fault
Reserved
External BIOS device
ON(1)/OFF(0) inter PD
Internal Debug
no use can floating
ON(1)/OFF(0)
Stereo Sync
no use can NC
For ATI Cross fire
no use can NC

SM010030010
200ma 120ohm@100mhz DCR 0.2

AMD ref:470ohm/1A

AMD ref:120ohm/0.3A

SM010030010
200ma 120ohm@100mhz DCR 0.2

Back compatibility(Manhattan)

Whistler and Seymour
Except A2VSSQ change to TSVSSQ, others are NC

Future ASIC call MLPS.
OLD ASIC is Fan PWM

120ohm/0.3A

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

GPIO8 Serial-ROM output from ROM,
GPIO9 Serial-ROM input to ROM.
GPIO10 Serial-ROM clock to ROM.
GPIO22 erternal BIOS-ROM enable

GPIO8,GPIO9,GPIO10 no use can NC
GPIO22
Enable need 3K PH ,no use must NC

if GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD
if GPIO22 Low ,GPIO 11-13->CFG[0:2]
Config Primary memory-aperture size
CFG[3:0]
128MB 000
256MB 001 *
64MB 010

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

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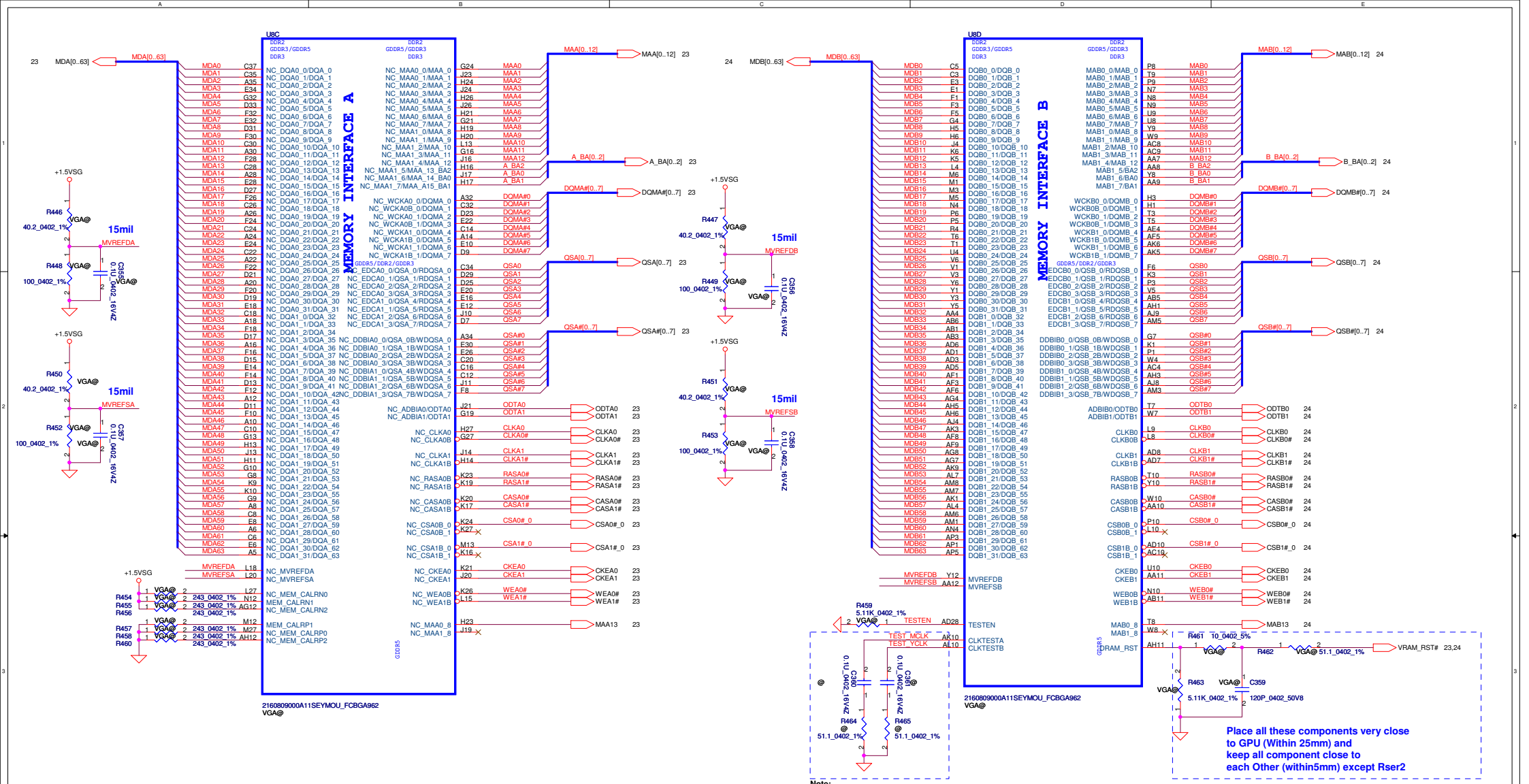


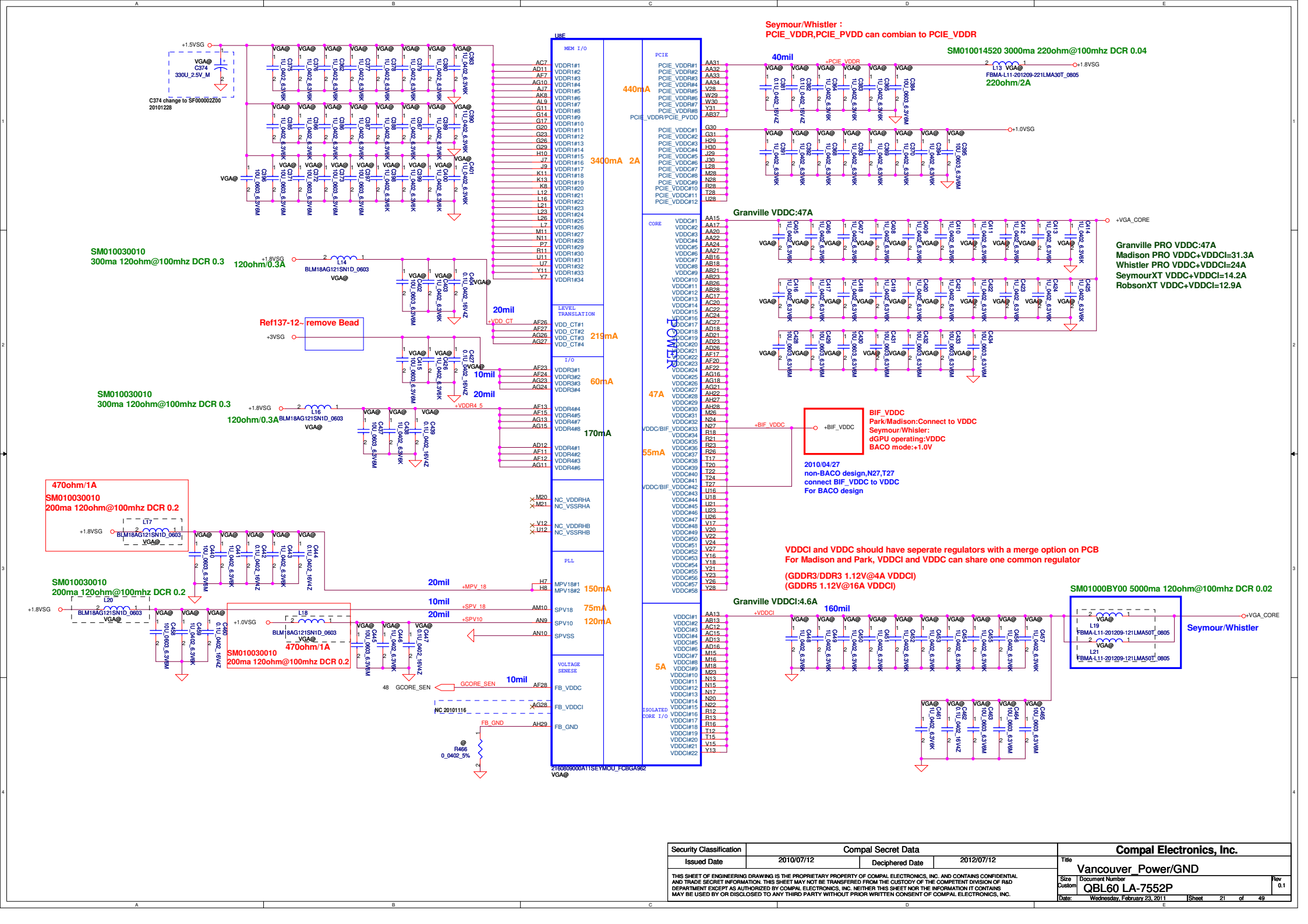
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Memory

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 20 of 49


Seymour/Whistler :
PCIE_VDDR,PCIE_PVDD can combian to PCIE_VDDR
SM010014520 3000ma 220ohm@100mhz DCR 0.04
40mil
220ohm/2A
Granville VDDC:47A
Granville PRO VDDC:47A
Madison PRO VDDC+VDDCI=31.3A
Whistler PRO VDDC+VDDCI=24A
SeymourXT VDDC+VDDCI=14.2A
RobsonXT VDDC+VDDCI=12.9A
SM010030010
300ma 120ohm@100mhz DCR 0.3
120ohm/0.3A
Ref137-remove Bead
BIF_VDDC
Park/Madison:Connect to VDDC
Seymour/Whisler:
dGPU operating:VDDC
BACO mode:+1.0V
2010/04/27
non-BACO design,N27,T27
connect BIF_VDDC to VDDC
For BACO design
470ohm/1A
SM010030010
200ma 120ohm@100mhz DCR 0.2
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)
Granville VDDCI:4.6A
160mil
SM01000BY00 5000ma 120ohm@100mhz DCR 0.02
Seymour/Whistler
Security Classification
Compal Secret Data
Issued Date
2010/07/12
Deciphered Date
2012/07/12
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Title
Vancouver_Power/GND
Size
Custom
Document Number
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Rev
0.1
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DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

PCIE_VSS#1 AB39
PCIE_VSS#2 E39
PCIE_VSS#3 F34
PCIE_VSS#4 F39
PCIE_VSS#5 G33
PCIE_VSS#6 G34
PCIE_VSS#7 H31
PCIE_VSS#8 H34
PCIE_VSS#9 H39
PCIE_VSS#10 J31
PCIE_VSS#11 J34
PCIE_VSS#12 K31
PCIE_VSS#13 K34
PCIE_VSS#14 K39
PCIE_VSS#15 L31
PCIE_VSS#16 L34
PCIE_VSS#17 M34
PCIE_VSS#18 M39
PCIE_VSS#19 N31
PCIE_VSS#20 N34
PCIE_VSS#21 P31
PCIE_VSS#22 P34
PCIE_VSS#23 P39
PCIE_VSS#24 R34
PCIE_VSS#25 T31
PCIE_VSS#26 T34
PCIE_VSS#27 T39
PCIE_VSS#28 U31
PCIE_VSS#29 U34
PCIE_VSS#30 V34
PCIE_VSS#31 V39
PCIE_VSS#32 W31
PCIE_VSS#33 W34
PCIE_VSS#34 Y34
PCIE_VSS#35 Y39

GND

GND#100 F15
GND#101 F17
GND#102 F19
GND#103 F21
GND#104 F23
GND#105 F25
GND#106 F27
GND#107 F29
GND#108 F31
GND#109 F33
GND#110 F7
GND#111 F9
GND#112 G2
GND#113 G6
GND#114 H9
GND#115 J2
GND#116 J27
GND#117 J6
GND#118 J8
GND#119 K14
GND#120 K7
GND#121 L11
GND#122 L17
GND#123 L2
GND#124 L22
GND#125 L24
GND#126 L6
GND#127 M17
GND#128 M22
GND#129 M24
GND#130 N16
GND#131 N18
GND#132 N2
GND#133 N21
GND#134 N23
GND#135 N26
GND#136 N6
GND#137 R15
GND#138 R17
GND#139 R2
GND#140 R20
GND#141 R22
GND#142 R24
GND#143 R27
GND#144 R6
GND#145 T11
GND#146 T13
GND#147 T16
GND#148 T18
GND#149 T21
GND#150 T23
GND#151 T26
GND#153 U15
GND#154 U17
GND#155 U2
GND#156 U20
GND#157 U22
GND#158 U24
GND#159 U27
GND#160 U6
GND#161 V11
GND#163 V16
GND#164 V18
GND#165 V21
GND#166 V23
GND#167 V26
GND#168 W2
GND#169 W6
GND#170 Y15
GND#171 Y17
GND#172 Y20
GND#173 Y22
GND#174 Y24
GND#175 Y27
GND#152 U13
GND#162 V13

GND#1 A3
GND#2 A37
GND#3 AA16
GND#4 AA18
GND#5 AA2
GND#6 AA21
GND#7 AA23
GND#8 AA26
GND#9 AA28
GND#10 AA6
GND#11 AB12
GND#12 AB15
GND#13 AB17
GND#14 AB20
GND#15 AB22
GND#16 AB24
GND#17 AB27
GND#18 AC11
GND#19 AC13
GND#20 AC16
GND#21 AC18
GND#22 AC2
GND#23 AC21
GND#24 AC23
GND#25 AC26
GND#26 AC28
GND#27 AC6
GND#28 AD15
GND#29 AD17
GND#30 AD20
GND#31 AD22
GND#32 AD24
GND#33 AD27
GND#34 AD9
GND#35 AE2
GND#36 AE6
GND#37 AF10
GND#38 AF16
GND#39 AF18
GND#40 AF21
GND#41 AG17
GND#42 AG2
GND#43 AG20
GND#44 AG22
GND#45 AG6
GND#46 AG9
GND#47 AH21
GND#48 AJ10
GND#49 AJ11
GND#50 AJ2
GND#51 AJ28
GND#52 AJ6
GND#53 AK11
GND#54 AK31
GND#55 AK7
GND#56 AL11
GND#57 AL14
GND#58 AL17
GND#59 AL2
GND#60 AL20
GND/PX_EN#61 AL21
GND#62 AL23
GND#63 AL26
GND#64 AL32
GND#65 AL6
GND#66 AL8
GND#67 AM11
GND#68 AM31
GND#69 AM9
GND#70 AN11
GND#71 AN2
GND#72 AN30
GND#73 AN6
GND#74 AN8
GND#75 AP11
GND#76 AP7
GND#77 AP9
GND#78 AR5
GND#79 B11
GND#80 B13
GND#81 B15
GND#82 B17
GND#83 B19
GND#84 B21
GND#85 B23
GND#86 B25
GND#87 B27
GND#88 B29
GND#89 B31
GND#90 B33
GND#91 B7
GND#92 B9
GND#93 C1
GND#94 C39
GND#95 E35
GND#96 E5
GND#97 F11
GND#98 F13

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW39

2160809000A11SEYMOU_FCBGA962
VGA@

REF137-13 update

PX_EN
PX_EN 25

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

U8H

Manhatann:300mA
Seymour:150mA

20mil +DPABCD_VDD18 AP20 AP21
DPCD/DPC_VDD18#1 DPCD/DPC_VDD18#2
DPAB/DPA_VDD18#1 DPAB/DPA_VDD18#2
AN24 AP24 20mil +DPABCD_VDD18 300mA

20mil +DPABCD_VDD10 AP13 AT13
DPCD/DPC_VDD10#1 DPCD/DPC_VDD10#2
DPAB/DPA_VDD10#1 DPAB/DPA_VDD10#2
AP31 AP32 20mil +DPABCD_VDD10

DP/DPC_VSSR#1 AN17
DP/DPC_VSSR#2 AP16
DP/DPC_VSSR#3 AP17
DP/DPC_VSSR#4 AW14
DP/DPC_VSSR#5 AW16
DP/DPA_VSSR#1 AN27
DP/DPA_VSSR#2 AP27
DP/DPA_VSSR#3 AP28
DP/DPA_VSSR#4 AW24
DP/DPA_VSSR#5 AW26

20mil +DPABCD_VDD18 AP22 AP23
DPCD/DPD_VDD18#1 DPCD/DPD_VDD18#2
DPAB/DPB_VDD18#1 DPAB/DPB_VDD18#2
AP25 AP26 20mil +DPABCD_VDD18

Manhatann:220mA
Seymour:110mA

20mil +DPABCD_VDD10 AP14 AP15
DPCD/DPD_VDD10#1 DPCD/DPD_VDD10#2
DPAB/DPB_VDD10#1 DPAB/DPB_VDD10#2
AN33 AP33 20mil +DPABCD_VDD10 220mA

DP/DPD_VSSR#1 AN19
DP/DPD_VSSR#2 AP18
DP/DPD_VSSR#3 AP19
DP/DPD_VSSR#4 AW20
DP/DPD_VSSR#5 AW22
DP/DPB_VSSR#1 AN29
DP/DPB_VSSR#2 AP29
DP/DPB_VSSR#3 AP30
DP/DPB_VSSR#4 AW30
DP/DPB_VSSR#5 AW32

R467 150_0402_1% VGA@ AW18
DPCD_CALR
DPAB_CALR
R468 150_0402_1% VGA@ AW28

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23 MBK1608221YZF_2P VGA@ +1.8VSG
FootPrint
VGA@ C469 10U_0603_6.3V6M
VGA@ C470 0.1U_0402_16V4Z
VGA@ C471 1U_0402_6.3V6K

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L25 MBK1608221YZF_2P VGA@ +1.0VSG
FootPrint
VGA@ C475 0.1U_0402_16V4Z
VGA@ C476 1U_0402_6.3V6K
VGA@ C477 10U_0603_6.3V6M

DP mode:300mA
LVDS mode:440mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L26 MBK1608221YZF_2P VGA@ +1.8VSG
FootPrint
VGA@ C478 10U_0603_6.3V6M
VGA@ C479 1U_0402_6.3V6K
VGA@ C480 0.1U_0402_16V4Z

20mil +DPEF_VDD18 AH34 AJ34
DPEF/DPE_VDD18#1 DPEF/DPE_VDD18#2
DPAB_VDD18/DPA_PVDD DP_VSSR/DPA_PVSS
AU28 AV27 20mA +DPABCD_VDD18 10mil

20mil +DPEF_VDD10 AL33 AM33
DPEF/DPE_VDD10#1 DPEF/DPE_VDD10#2
DPAB_VDD18/DPB_PVDD DP_VSSR/DPB_PVSS
AV29 AR28 20mA +DPABCD_VDD18 10mil

DP/DPE_VSSR#1 AN34
DP/DPE_VSSR#2 AP39
DP/DPE_VSSR#3 AR39
DP/DPE_VSSR#4 AU37
DPCD_VDD18/DPC_PVDD DP_VSSR/DPC_PVSS
AU18 AV17 20mA +DPABCD_VDD18 10mil

DPCD_VDD18/DPD_PVDD DP_VSSR/DPD_PVSS
AV19 AR18 20mA +DPABCD_VDD18 10mil

DP mode:220mA
LVDS mode:240mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L27 MBK1608221YZF_2P VGA@ +1.0VSG
FootPrint
VGA@ C481 10U_0603_6.3V6M
VGA@ C482 1U_0402_6.3V6K
VGA@ C483 0.1U_0402_16V4Z

20mil +DPEF_VDD18 AF34 AG34
DPEF/DPF_VDD18#1 DPEF/DPF_VDD18#2
DPEF_VDD18/DPE_PVDD DP_VSSR/DPE_PVSS
AM37 AN38 20mA +DPEF_VDD18 10mil

20mil +DPEF_VDD10 AK33 AK34
DPEF/DPF_VDD10#1 DPEF/DPF_VDD10#2
DPEF_VDD18/DPF_PVDD DP_VSSR/DPF_PVSS
AL38 AM35 20mA +DPEF_VDD18 10mil

DP/DPF_VSSR#1 AF39
DP/DPF_VSSR#2 AH39
DP/DPF_VSSR#3 AK39
DP/DPF_VSSR#4 AL34
DP/DPF_VSSR#5 AM34

R470 VGA@ 150_0402_1% AM39
DPEF_CALR

2160809000A11SEYMOU_FCBGA962
VGA@

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

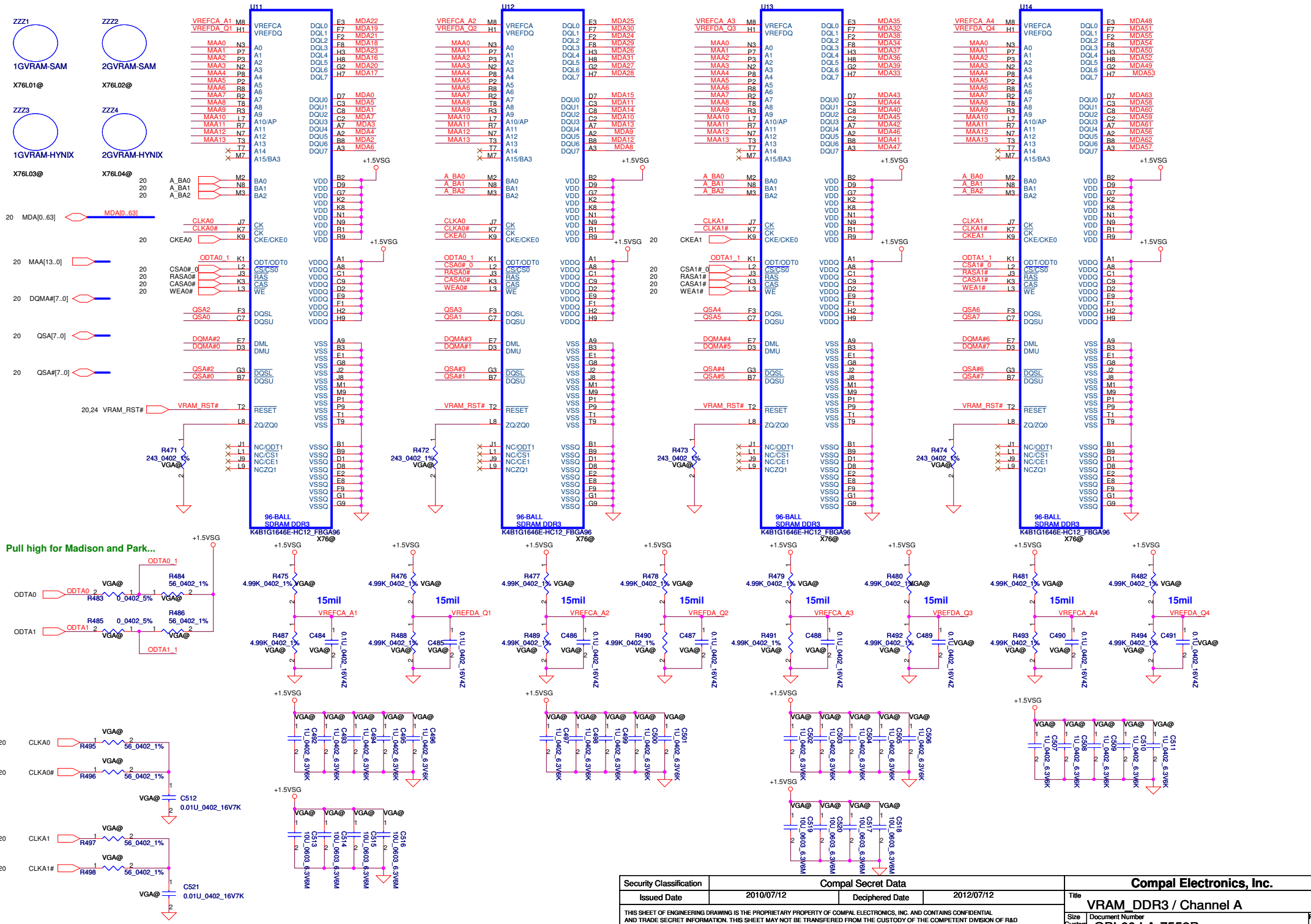
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 22 of 49



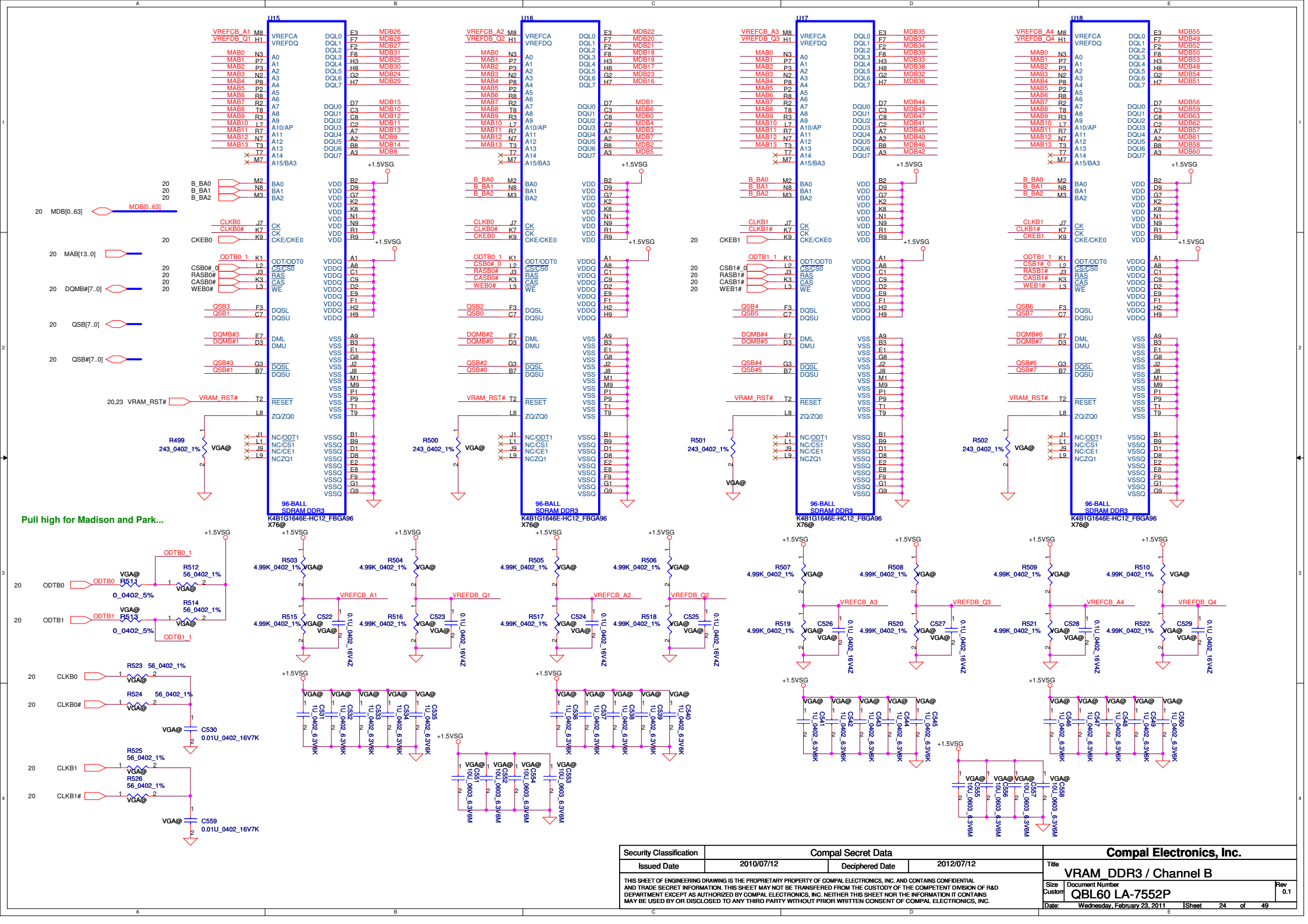
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 23 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

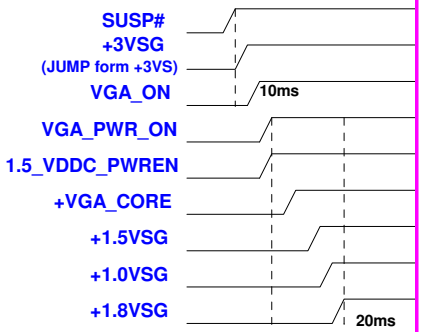
Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

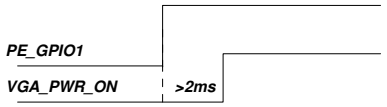
Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 24 of 49

Power Sequence of Whistler and Seymour

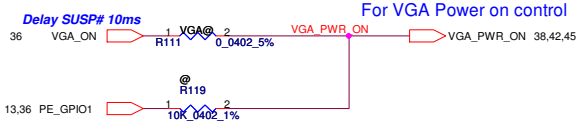


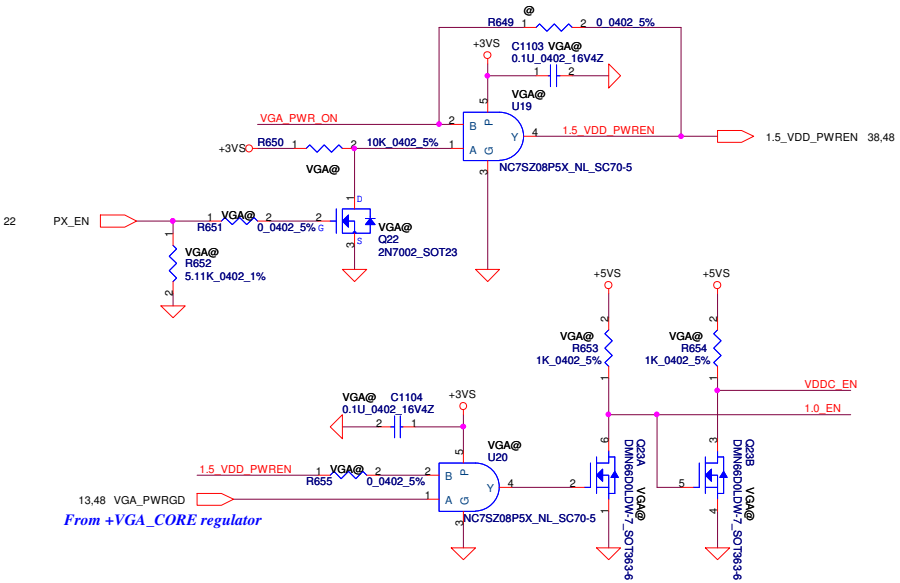
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

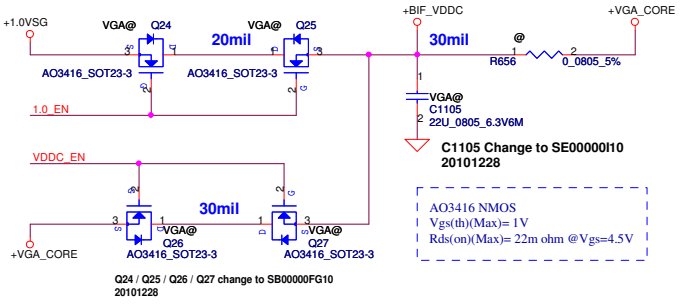


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN







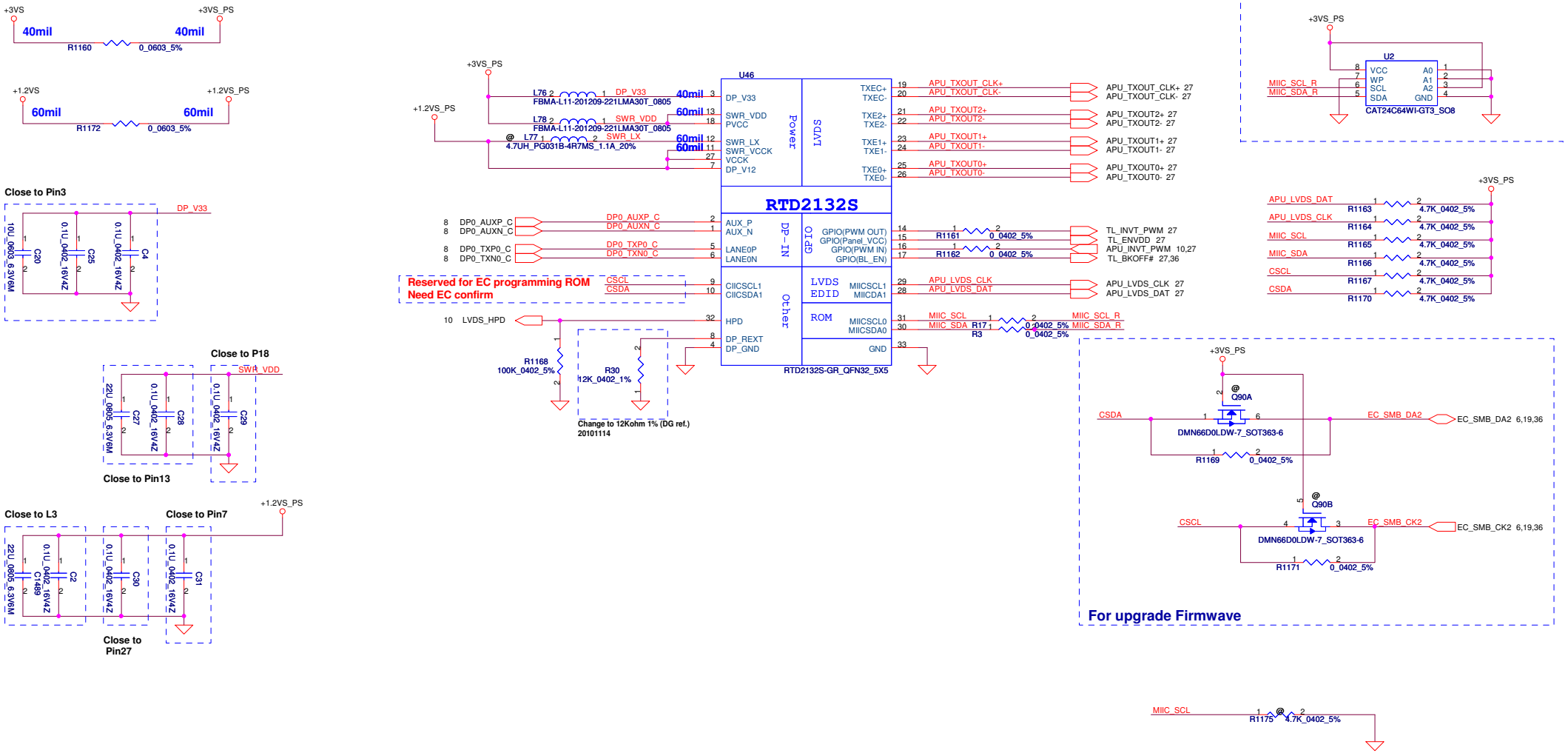
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: VGA power sequence and BACO

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

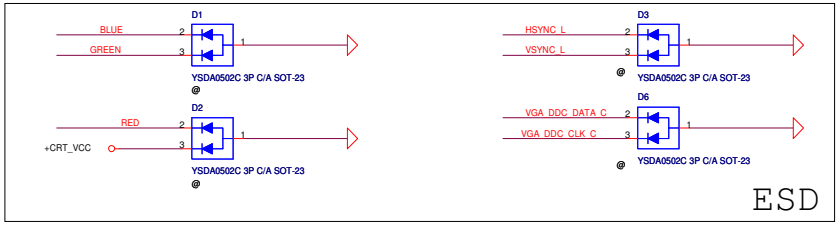
Date: Wednesday, February 23, 2011 Sheet 25 of 49

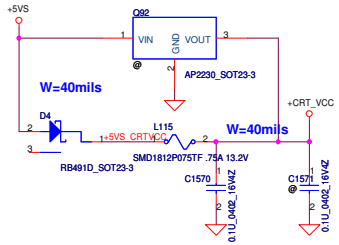


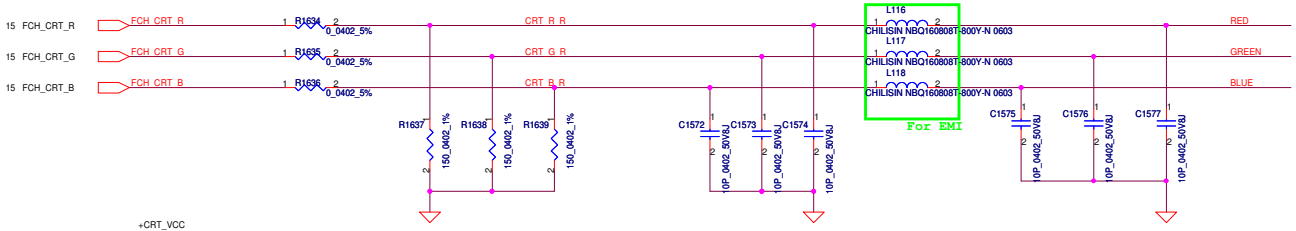
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

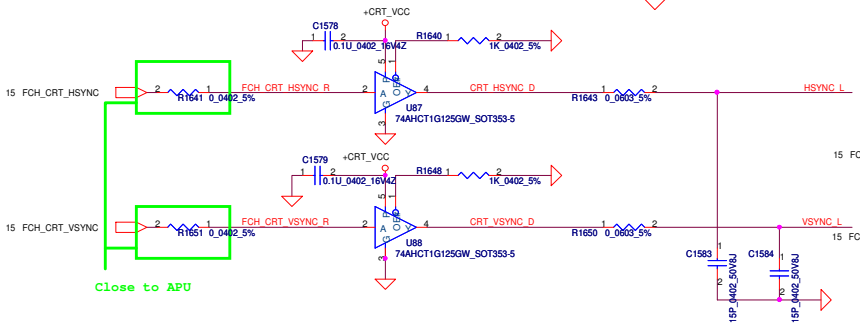
Title	LVDS Translator - RTD2132S		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.1
Date: Wednesday, February 23, 2011	Sheet 26 of 49		

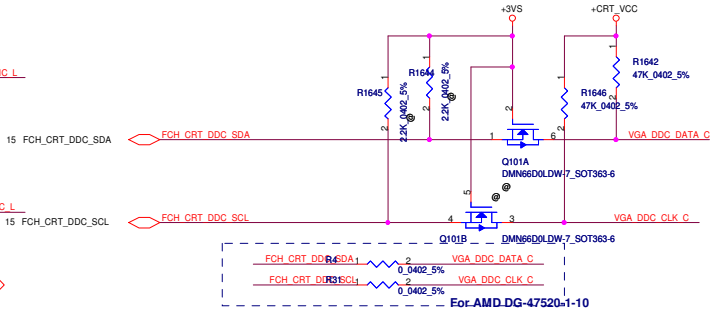
CRT

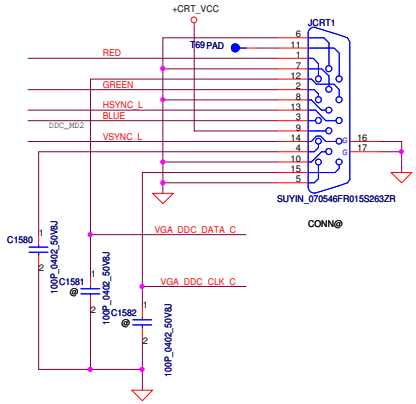




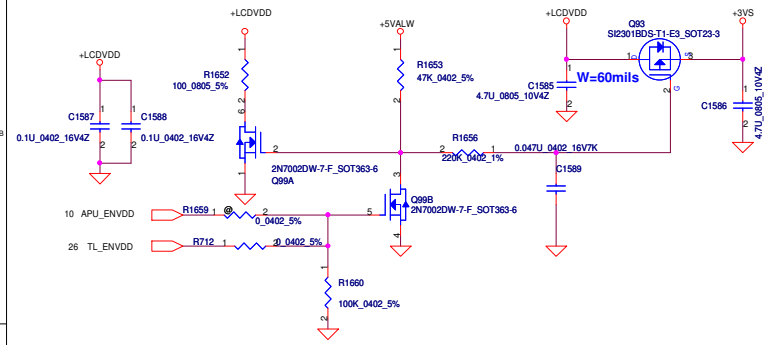


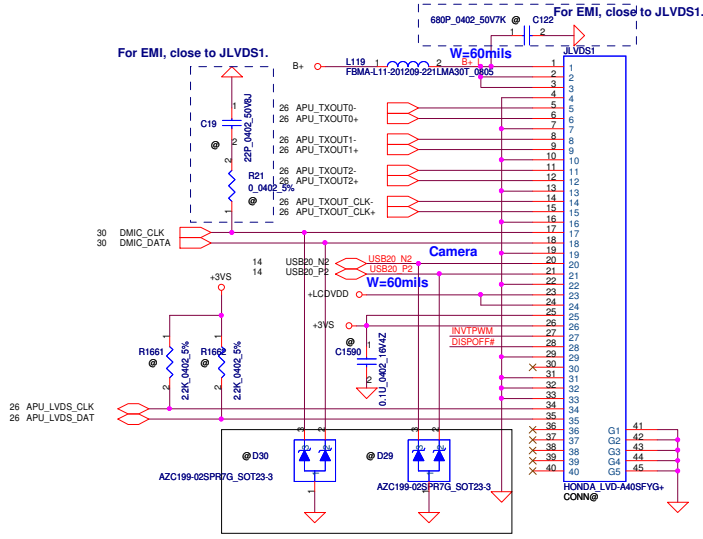




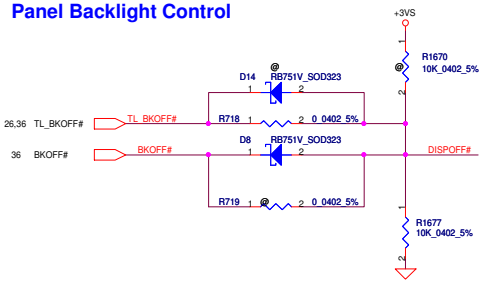


Panel LCDVDD Control

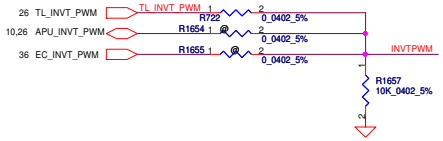




Panel Backlight Control

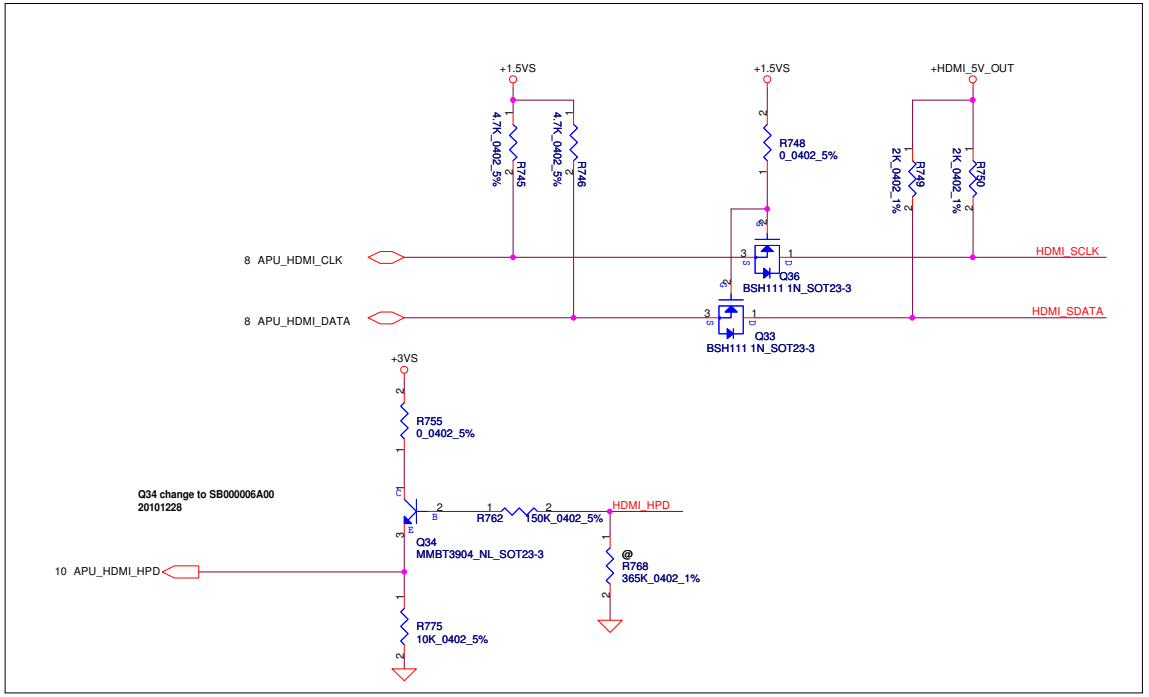


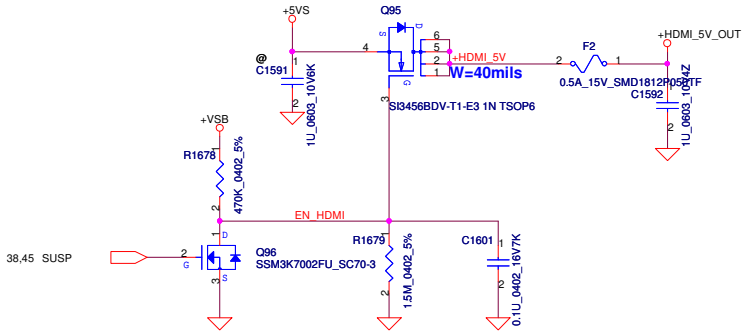
Panel PWM Control

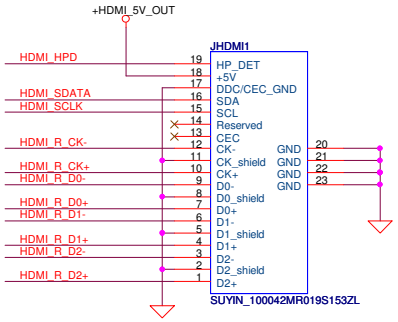


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.	
Title	P10-LVDS/CRT CONN
Size: C	Document Number: QBL60 LA-7552P
Rev: 0.1	
Date: Wednesday, February 23, 2011	Sheet 27 of 49



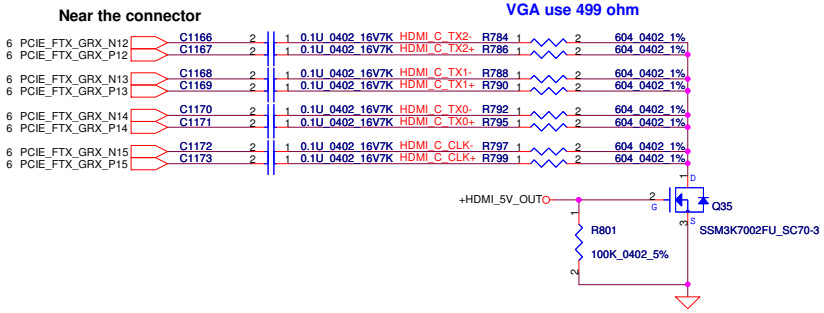


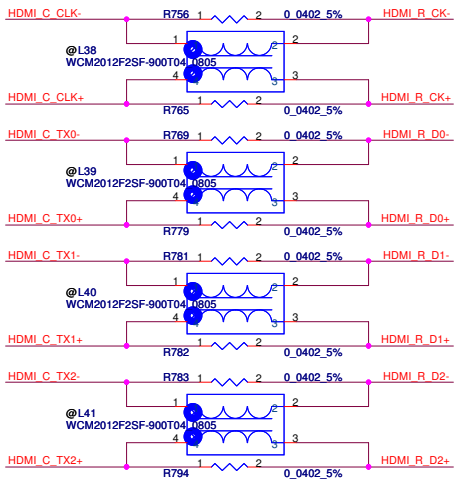


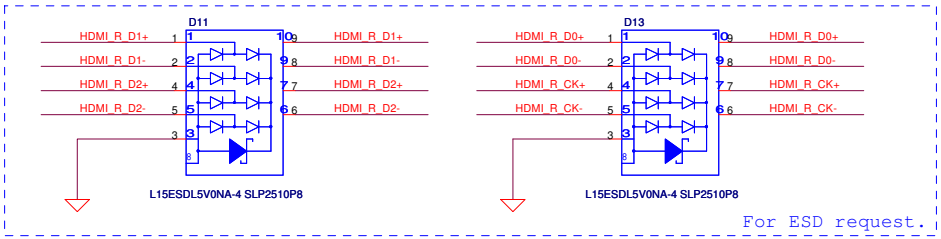
From APU

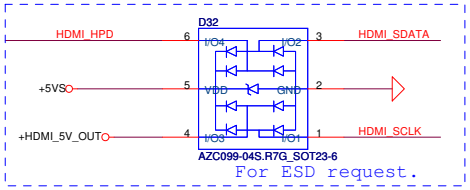
Near the connector

UMA use 604 ohm
VGA use 499 ohm









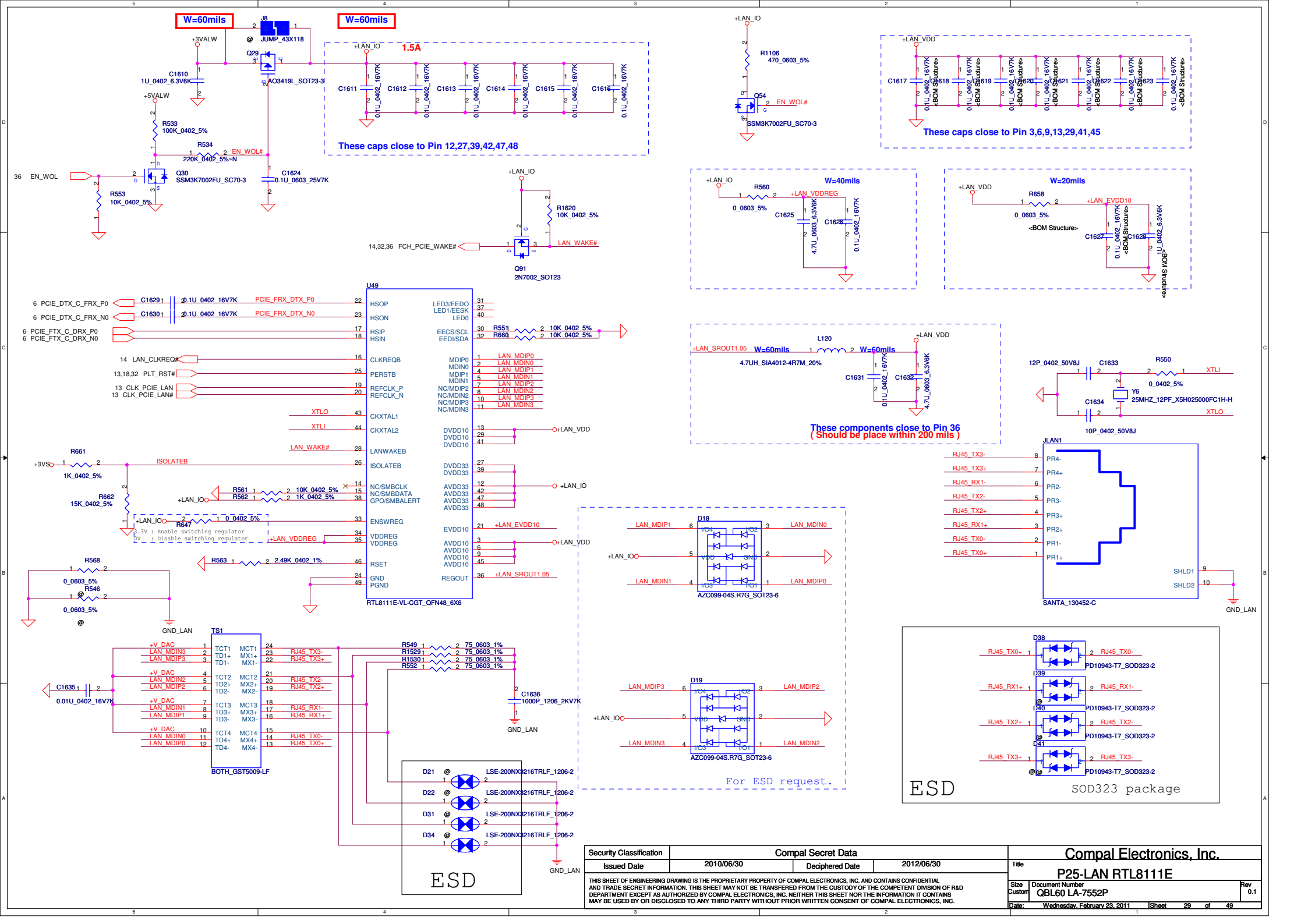
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 28 of 49



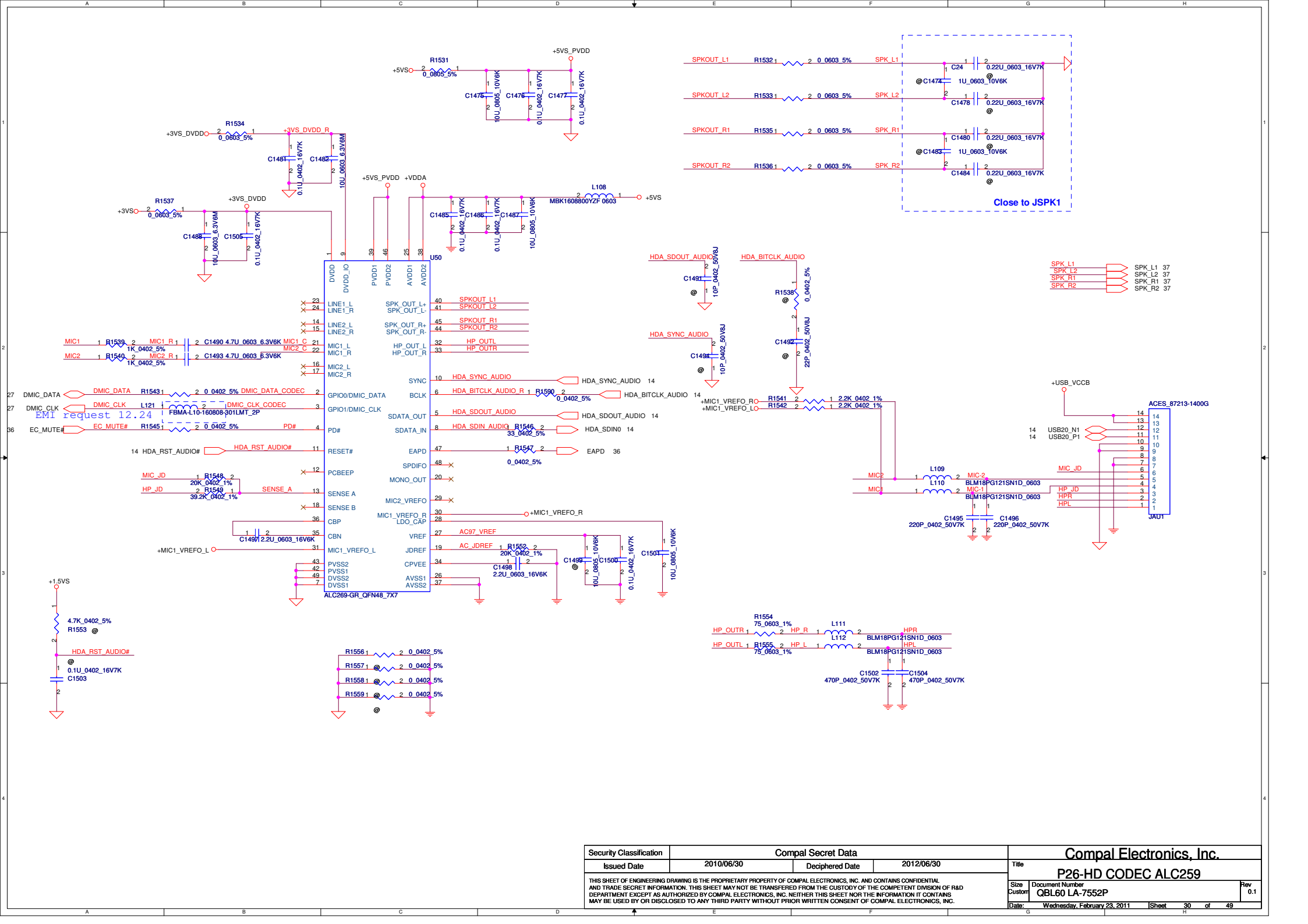
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P25-LAN RTL8111E

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 29 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

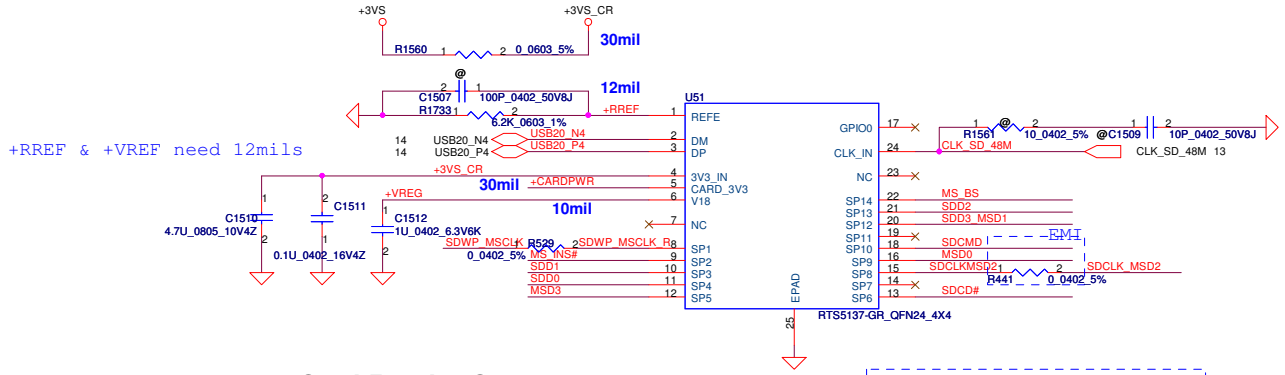
Compal Electronics, Inc.

Title: P26-HD CODEC ALC259

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

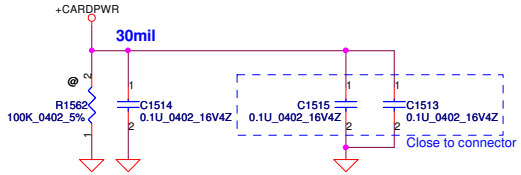
Date: Wednesday, February 23, 2011 Sheet 30 of 49

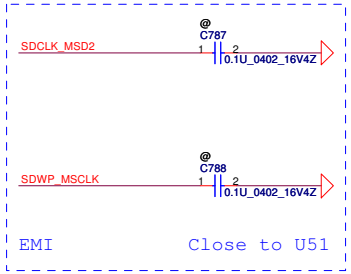
Card Reader RTS5137
(only SD/MMC/MS function)

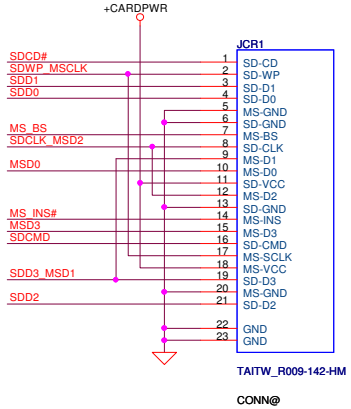


+RREF & +VREF need 12mils

Card Reader Connector







Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P27-RTS5137 Media Card Controller

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.1

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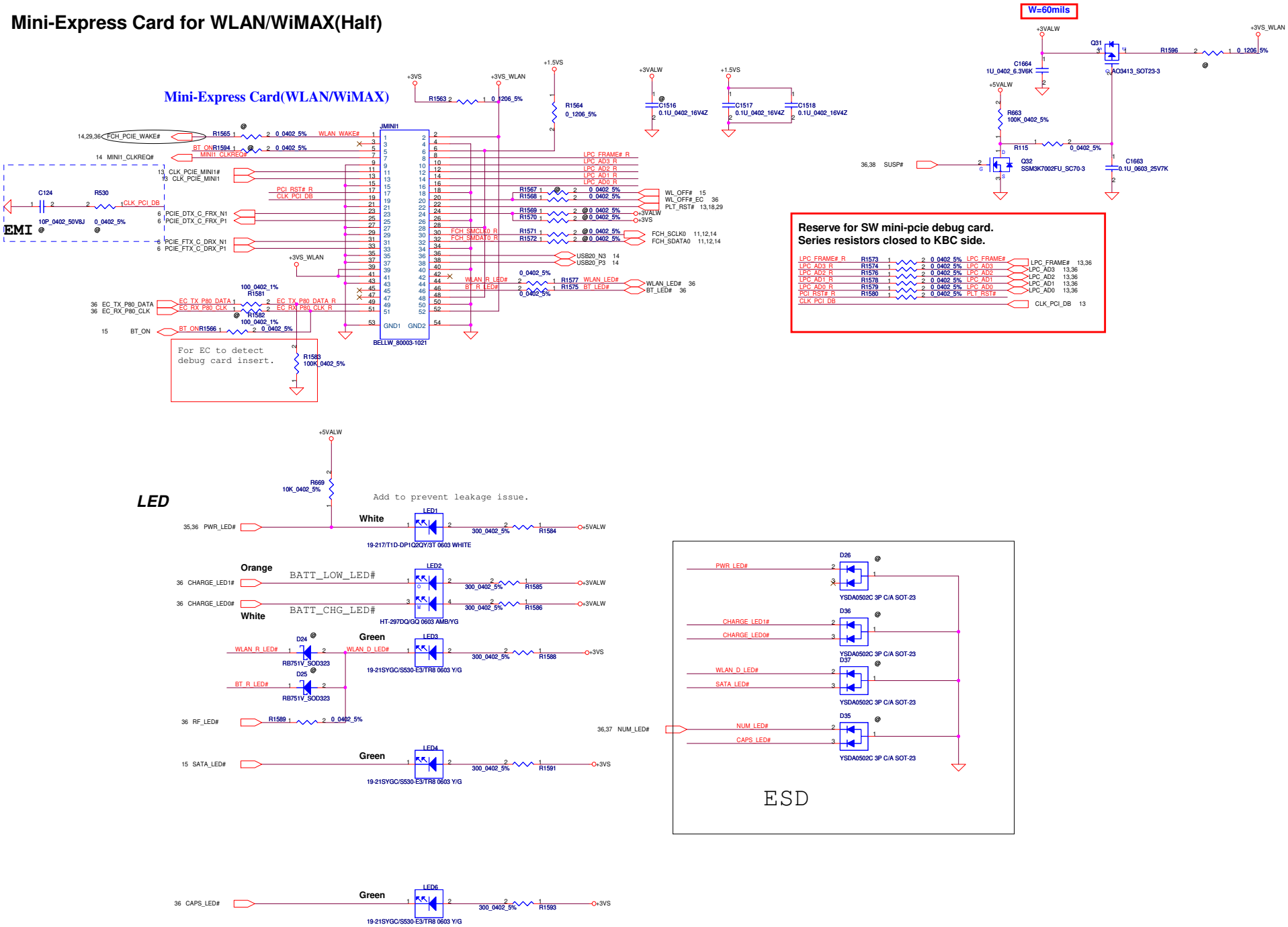
Mini-Express Card for WLAN/WiMAX(Half)

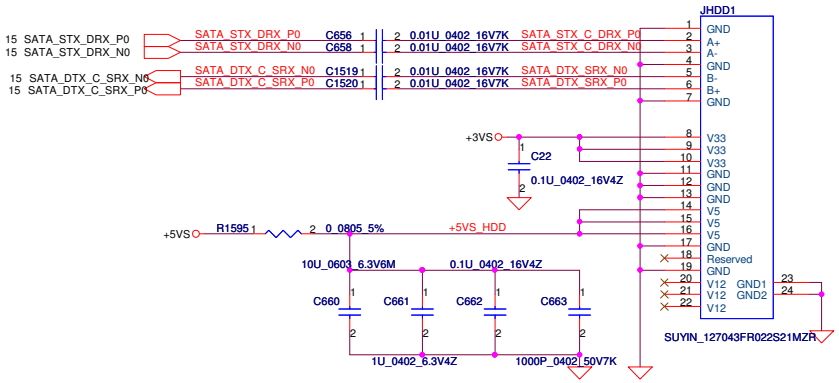


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

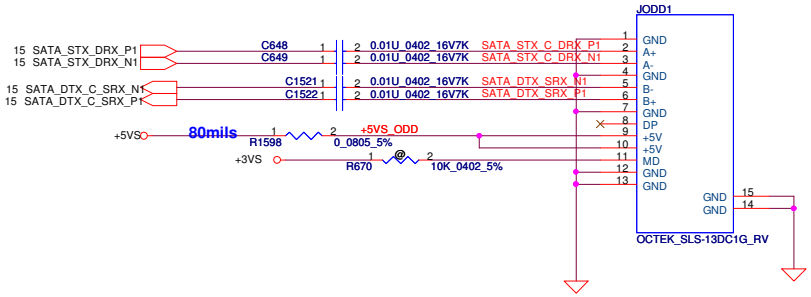
Compal Electronics, Inc.

Title	P28-Mini PCIE/LED	
Size	Document Number	Rev 0.1
	QBL60 LA-7552P	
Date: Wednesday, February 23, 2011	Sheet 32 of 49	

SATA HDD Conn.



SATA ODD FFC Conn.



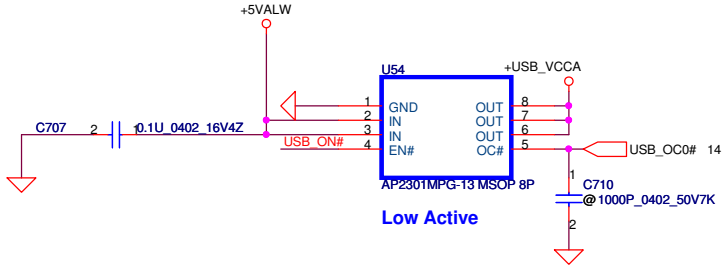
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

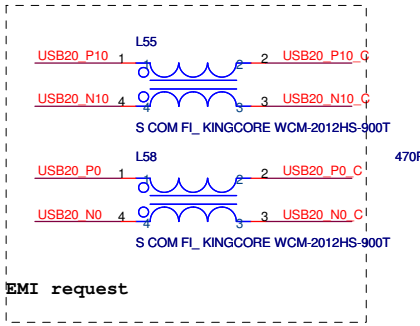
Compal Electronics, Inc.

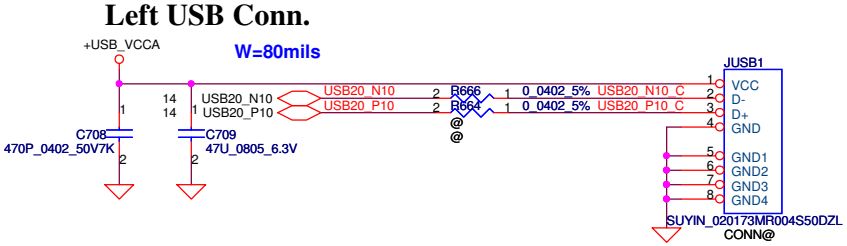
Title: P29-HDD & ODD CONN

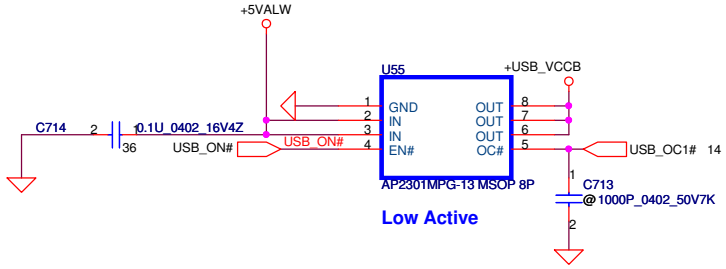
Size: B | Document Number: QBL60 LA-7552P | Rev: 0.1

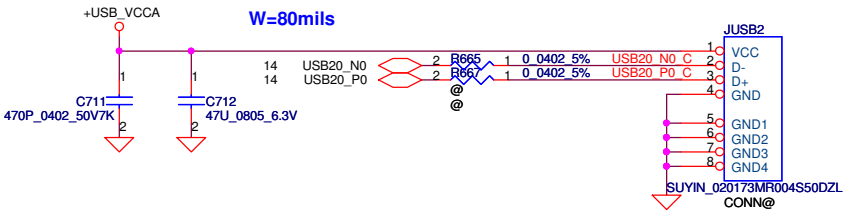
Date: Wednesday, February 23, 2011 | Sheet 33 of 49

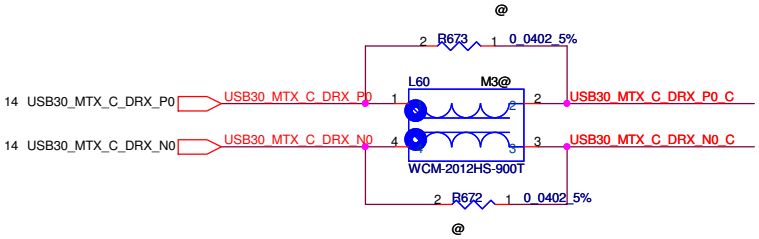


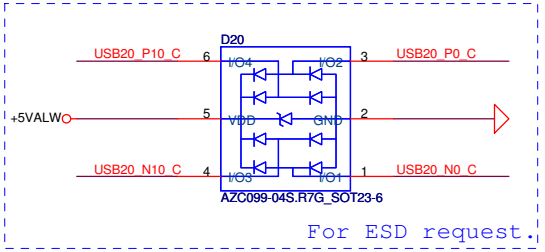


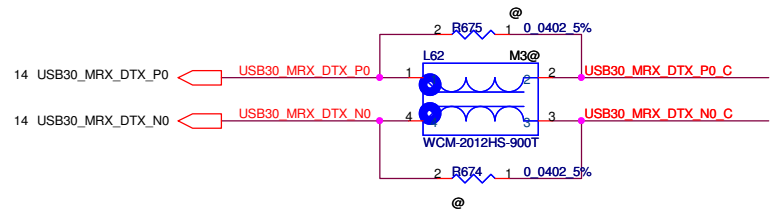


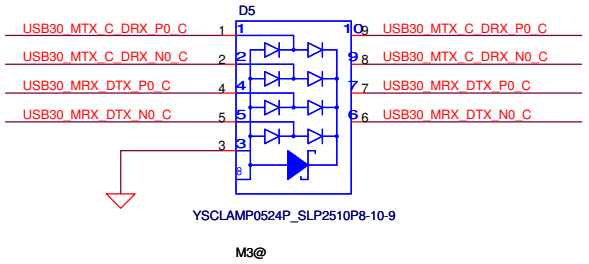












Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P32-USB/BT/USBsub

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

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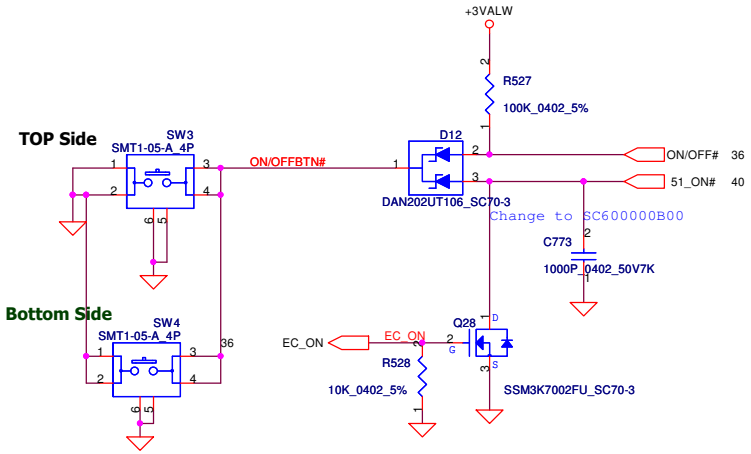
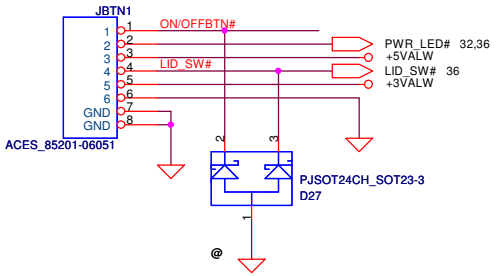
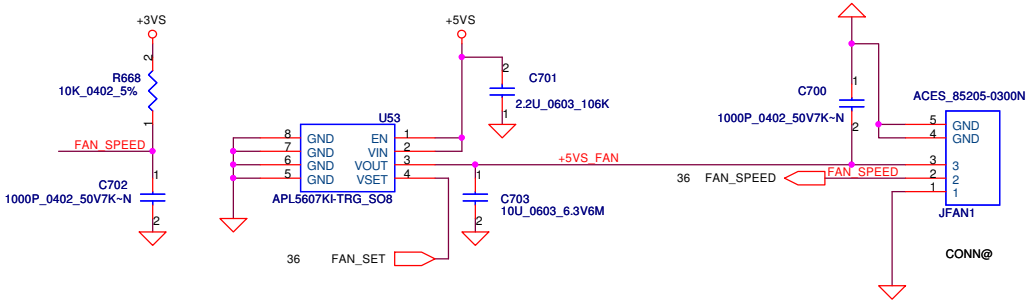
ON/OFF switch **Power Button**

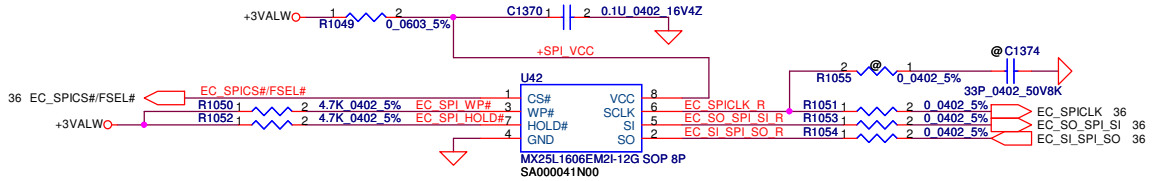




Fan Control Circuit



EC BIOS ROM



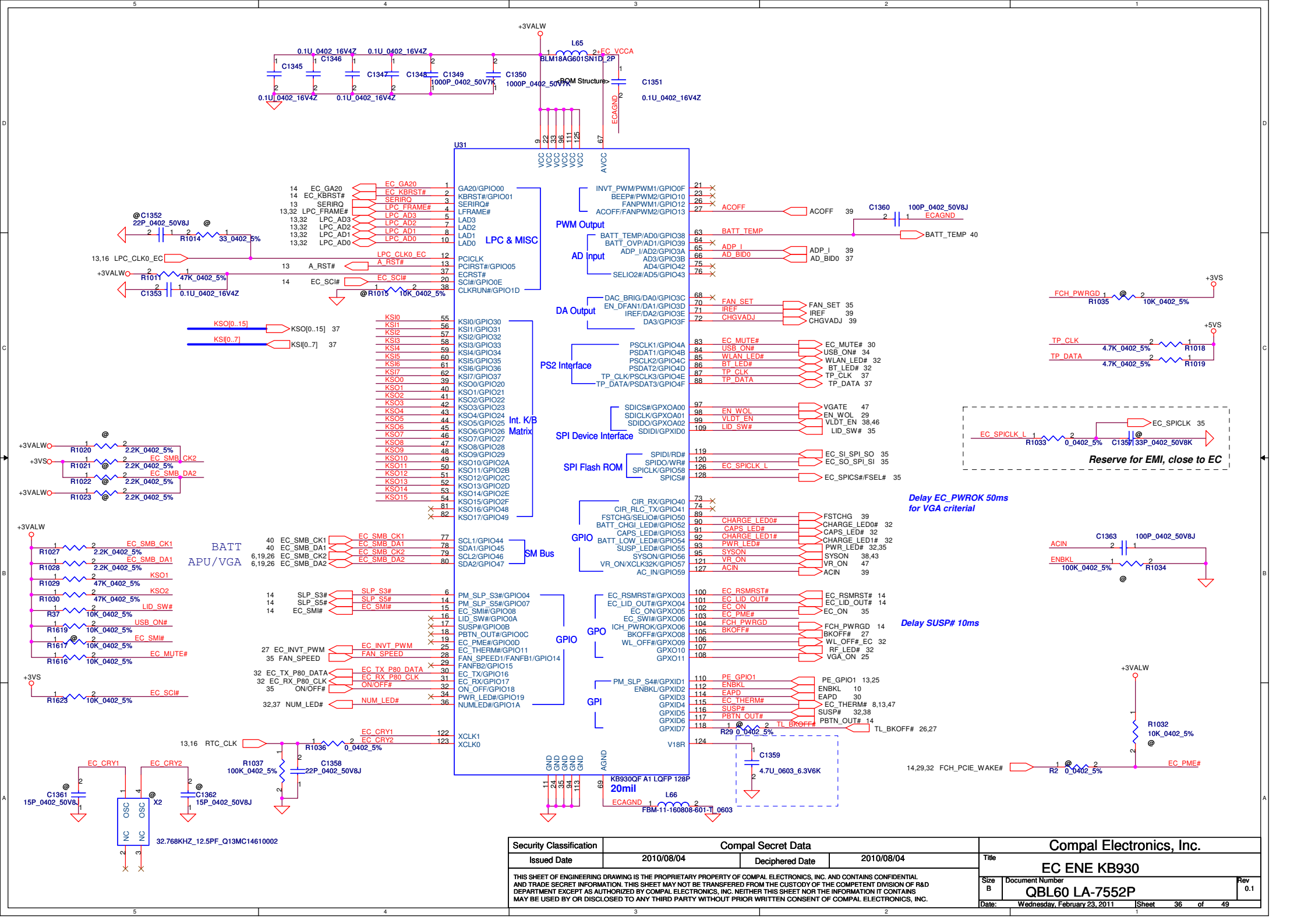
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size: B | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 35 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: EC ENE KB930

Size	Document Number	Rev
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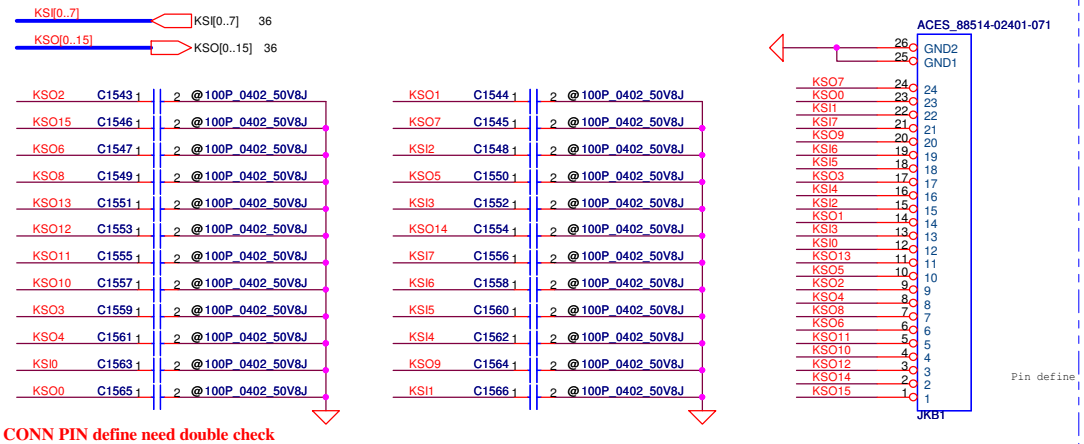
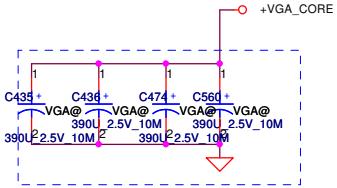
INT_KBD Conn.

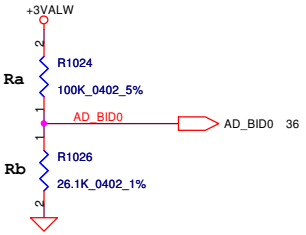


CONN PIN define need double check

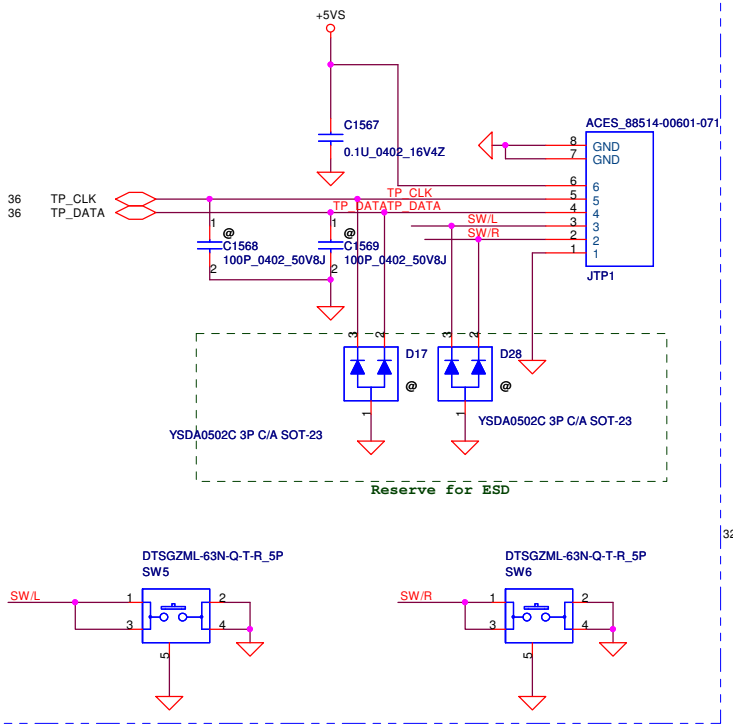


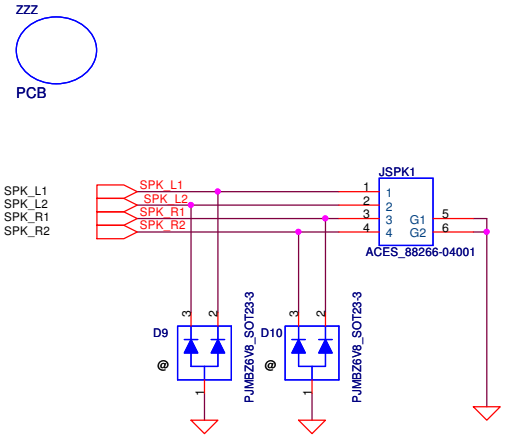
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R03 PR	100K	46.4K	1.045V
3	R10 MP	100K	56.2K	1.187V

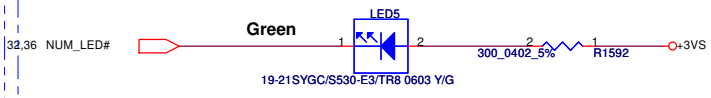
Analog Board ID definition

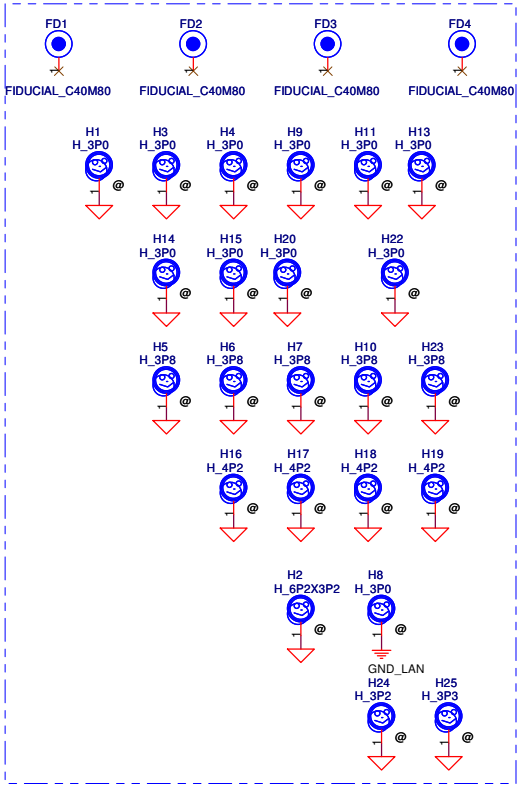


To TP/B Conn.





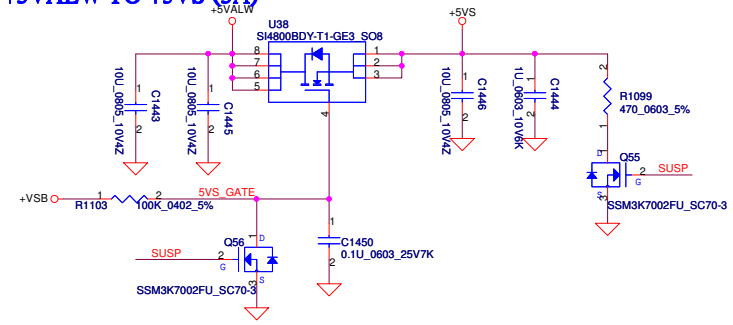




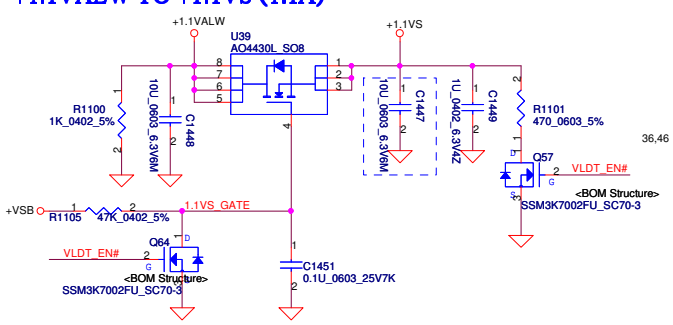
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

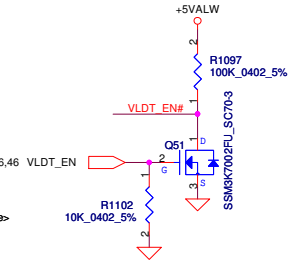
Compal Electronics, Inc.
Title: P33-Other IO/USB (right)
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1
Date: Wednesday, February 23, 2011 | Sheet 37 of 49

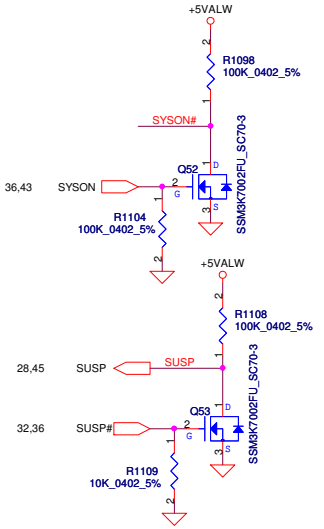
+5VALW TO +5VS (5A)



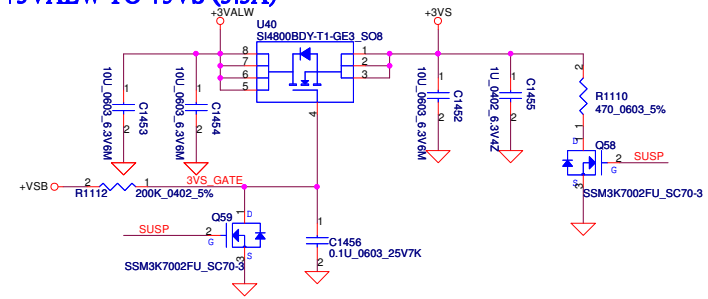
+1.1VALW TO +1.1VS (1.1A)



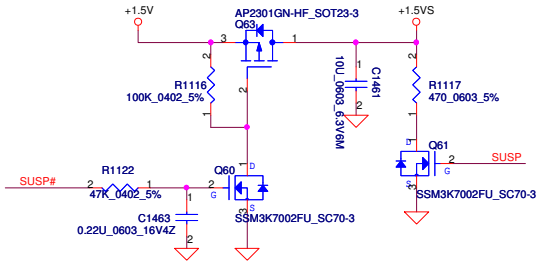




+3VALW TO +3VS (3.3A)

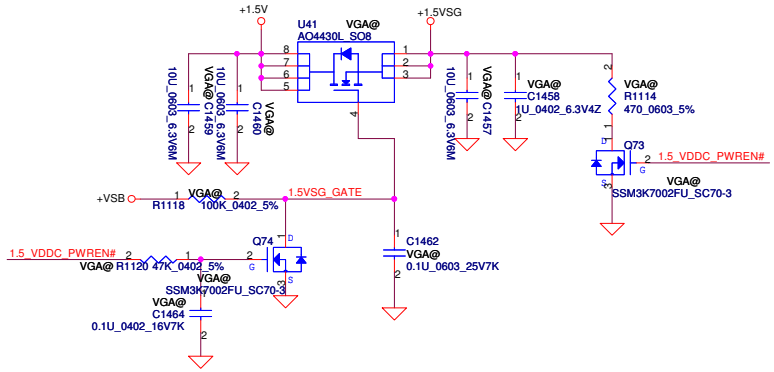


+1.5V TO +1.5VS (1.5A)

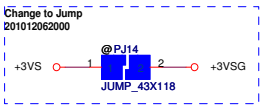


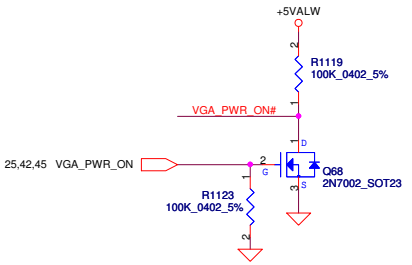
VGA Power

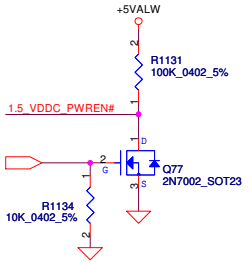
+1.5V to +1.5VSG (1.5A)

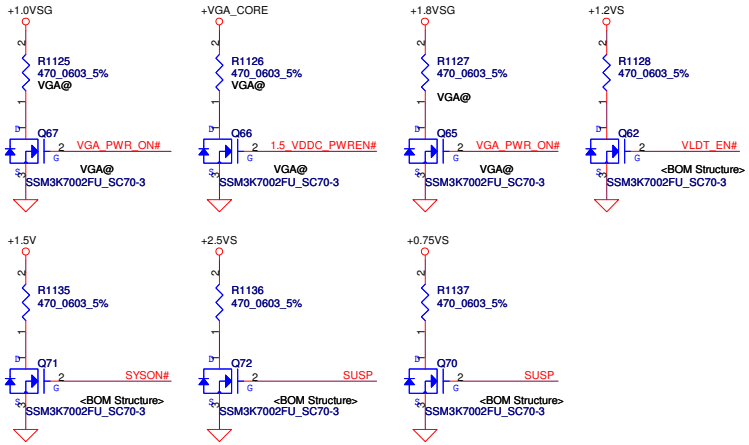


+3VS to +3VSG (3.3A)









Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	QBL60 LA-7552P	0.1

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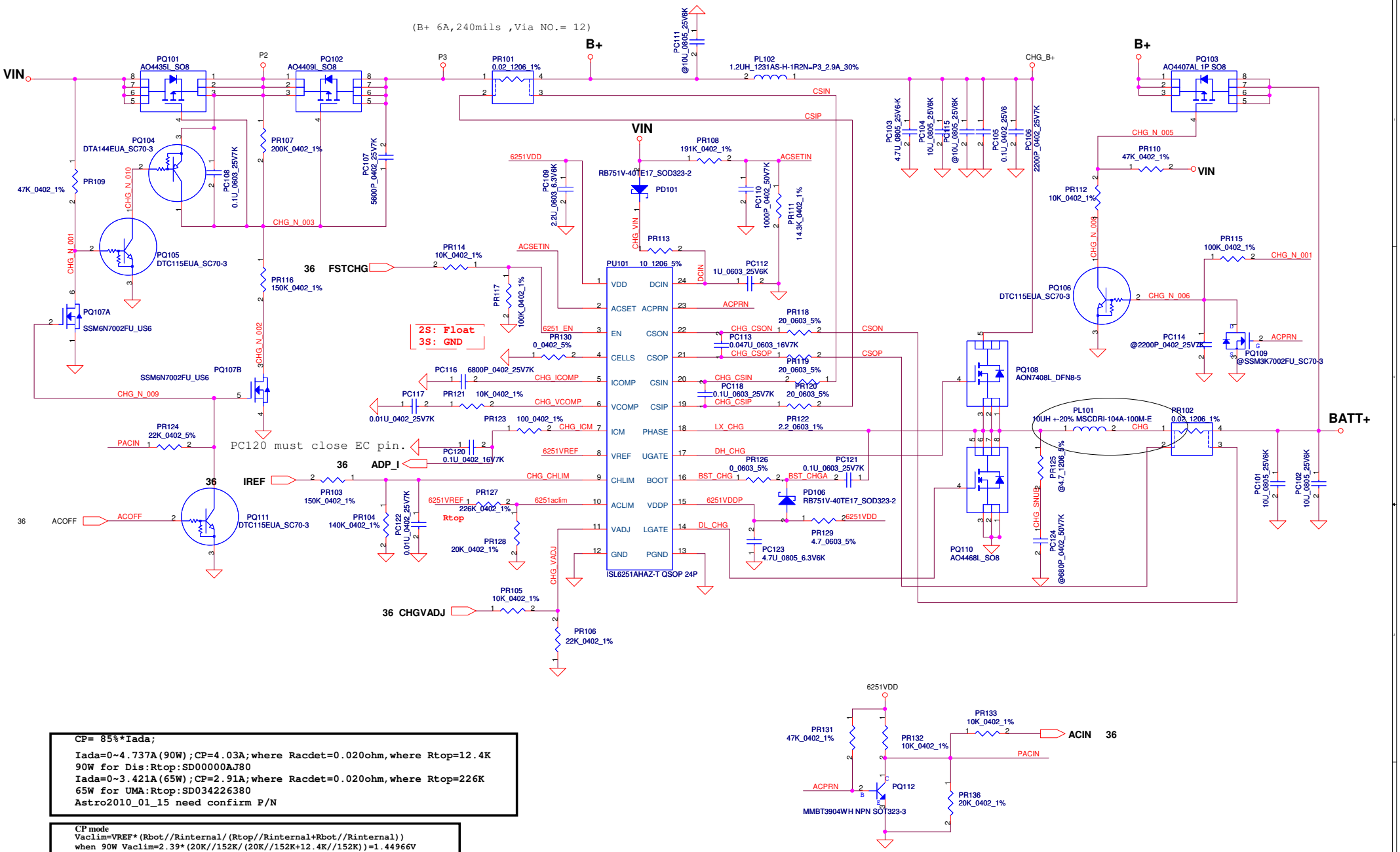


```
CP= 85%*Iada;
Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N
```

```
CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

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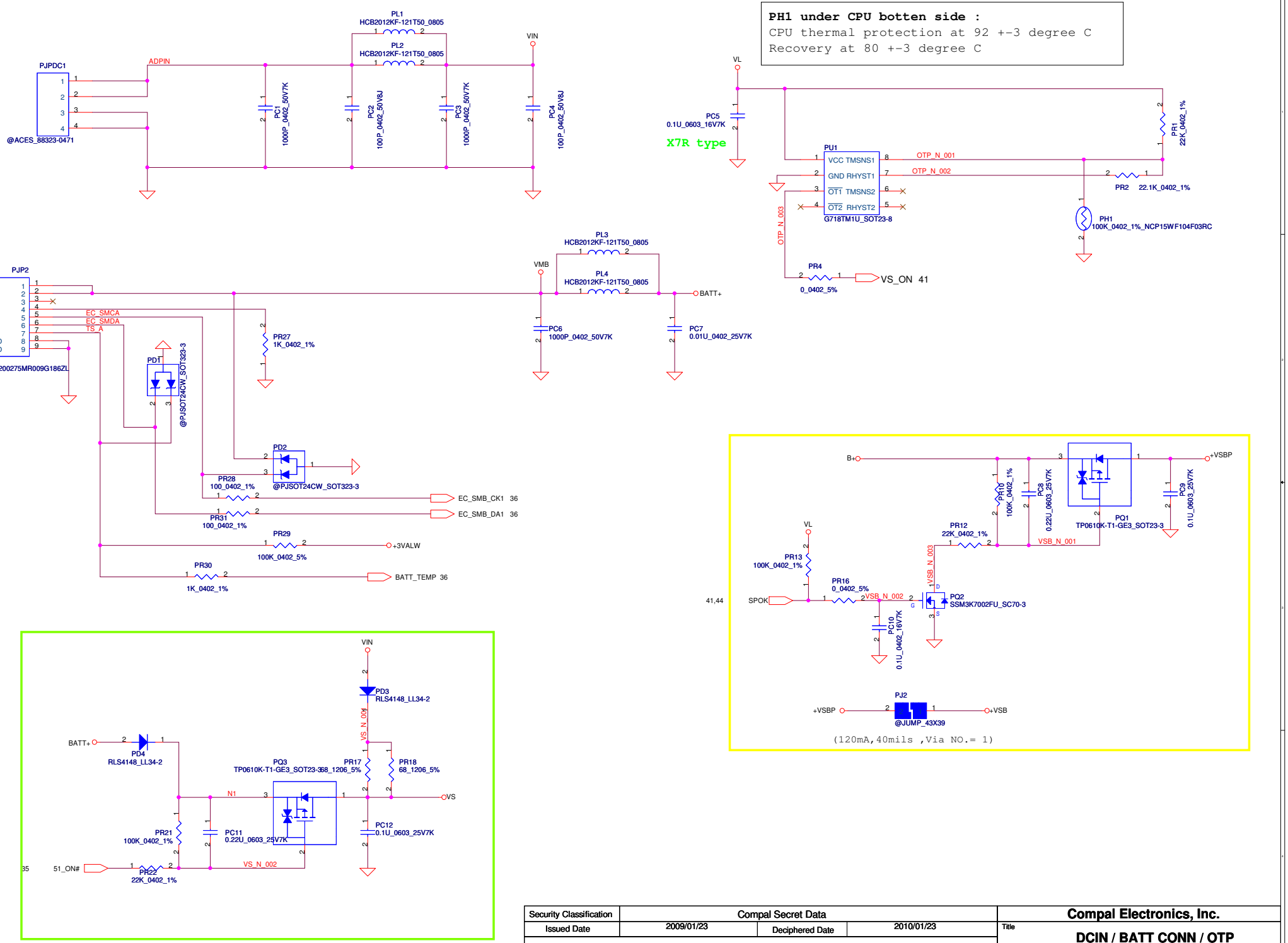
PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



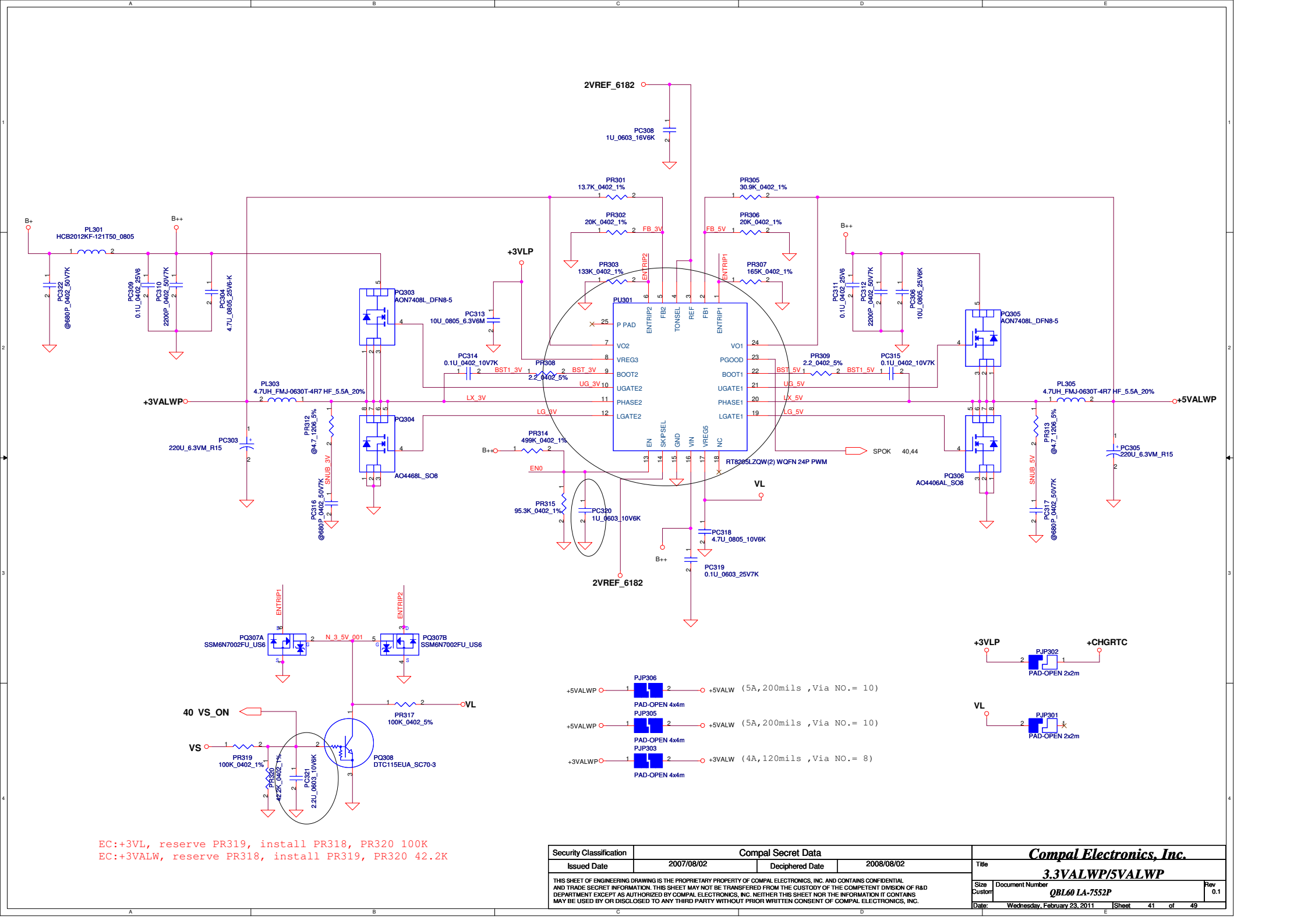
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

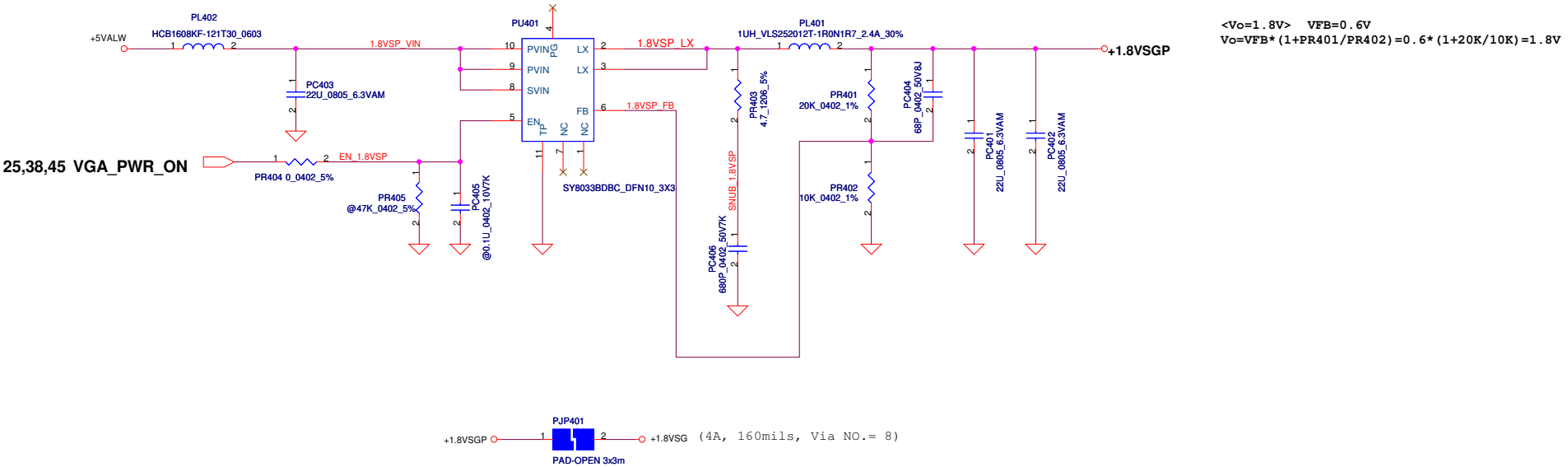
Date: Wednesday, February 23, 2011 | Sheet 40 of 49



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.1
Date: Wednesday, February 23, 2011	Sheet 41 of 49		

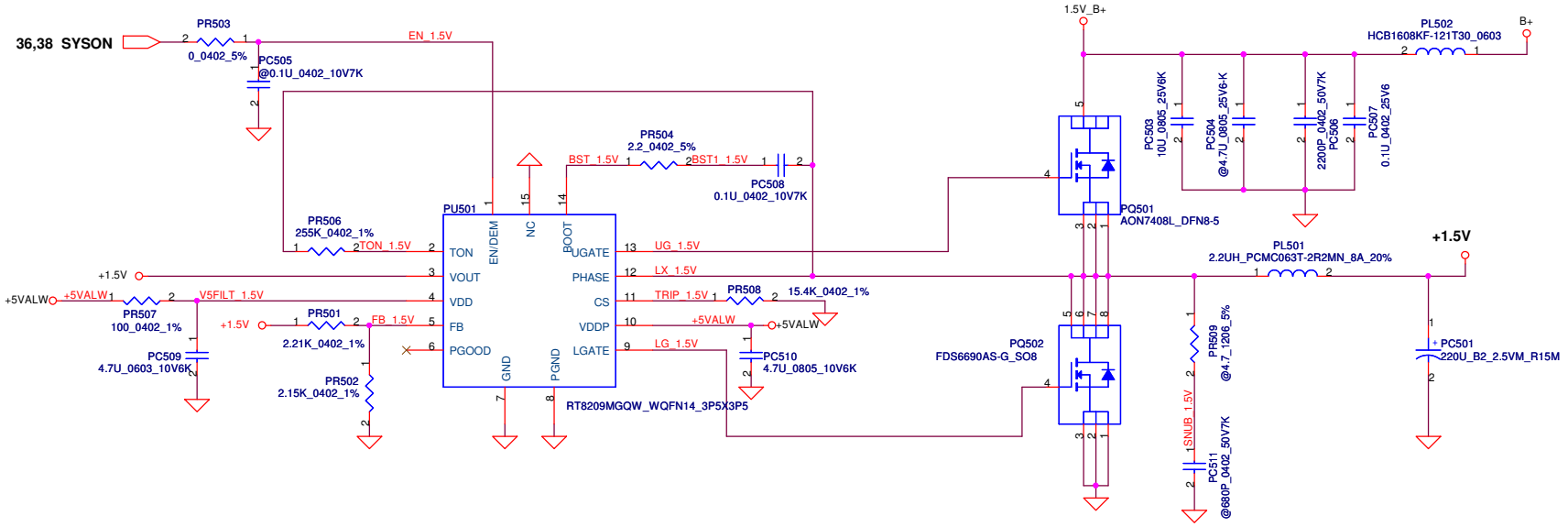


Compal Electronics, Inc.

Title: **+1.8VSGP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Wednesday, February 23, 2011 | Sheet 42 of 49



(8A,320mils ,Via NO.= 16)

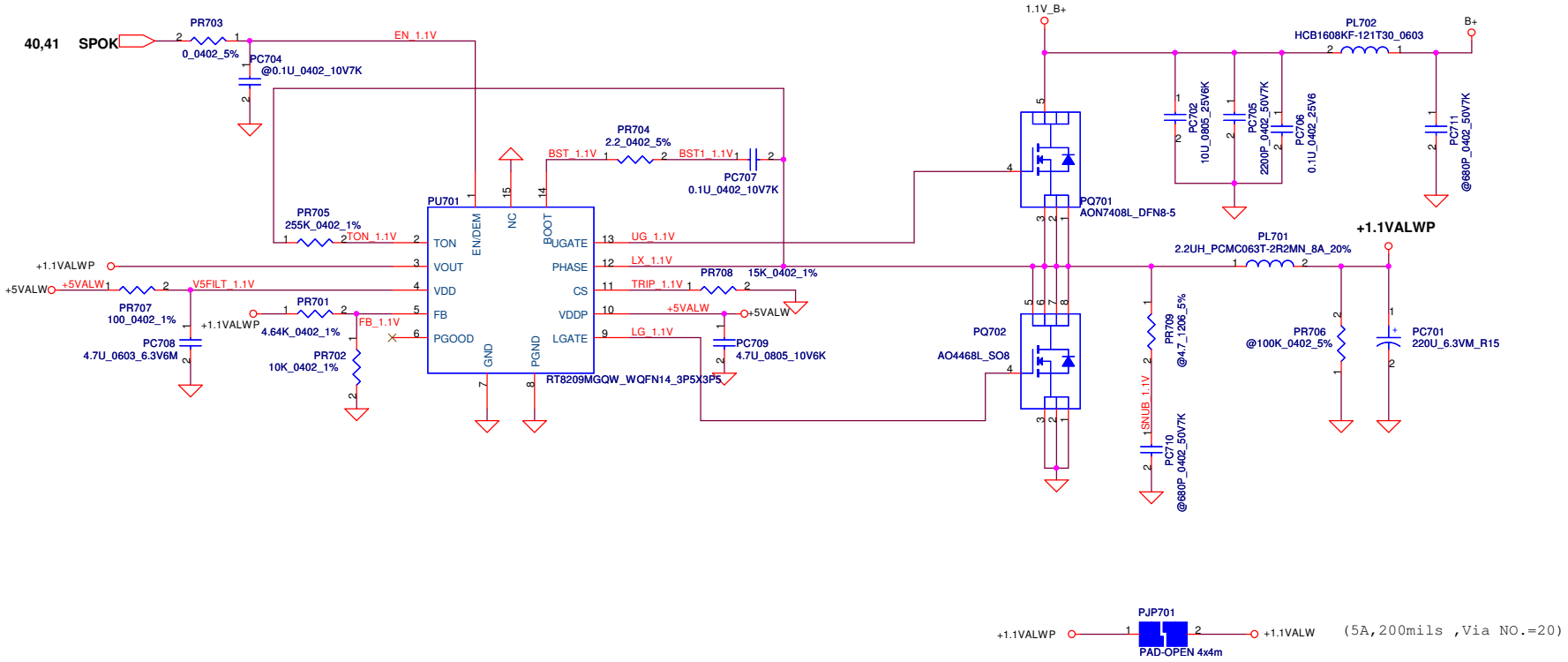
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 43 of 49



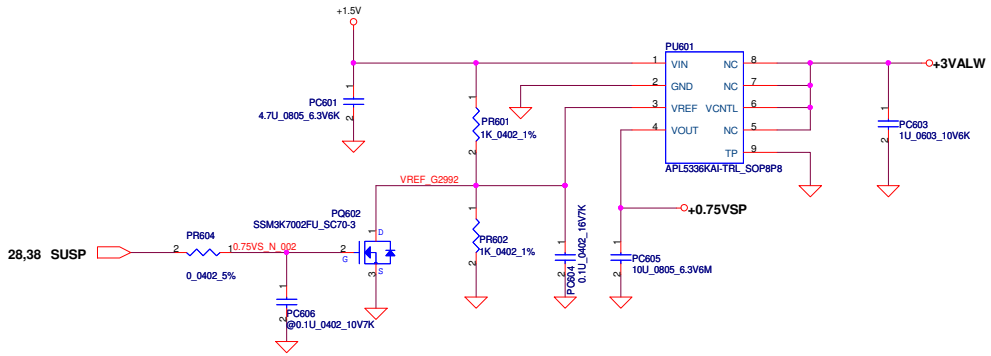
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

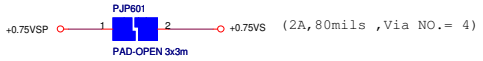
Compal Electronics, Inc.

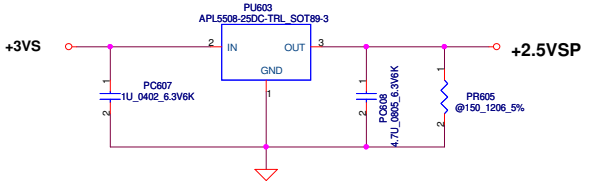
Title: PWR+1.1VALWP

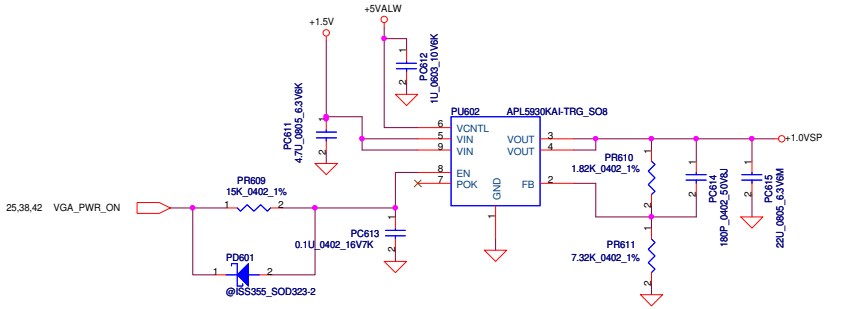
Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.1

Date: Wednesday, February 23, 2011 | Sheet 44 of 49









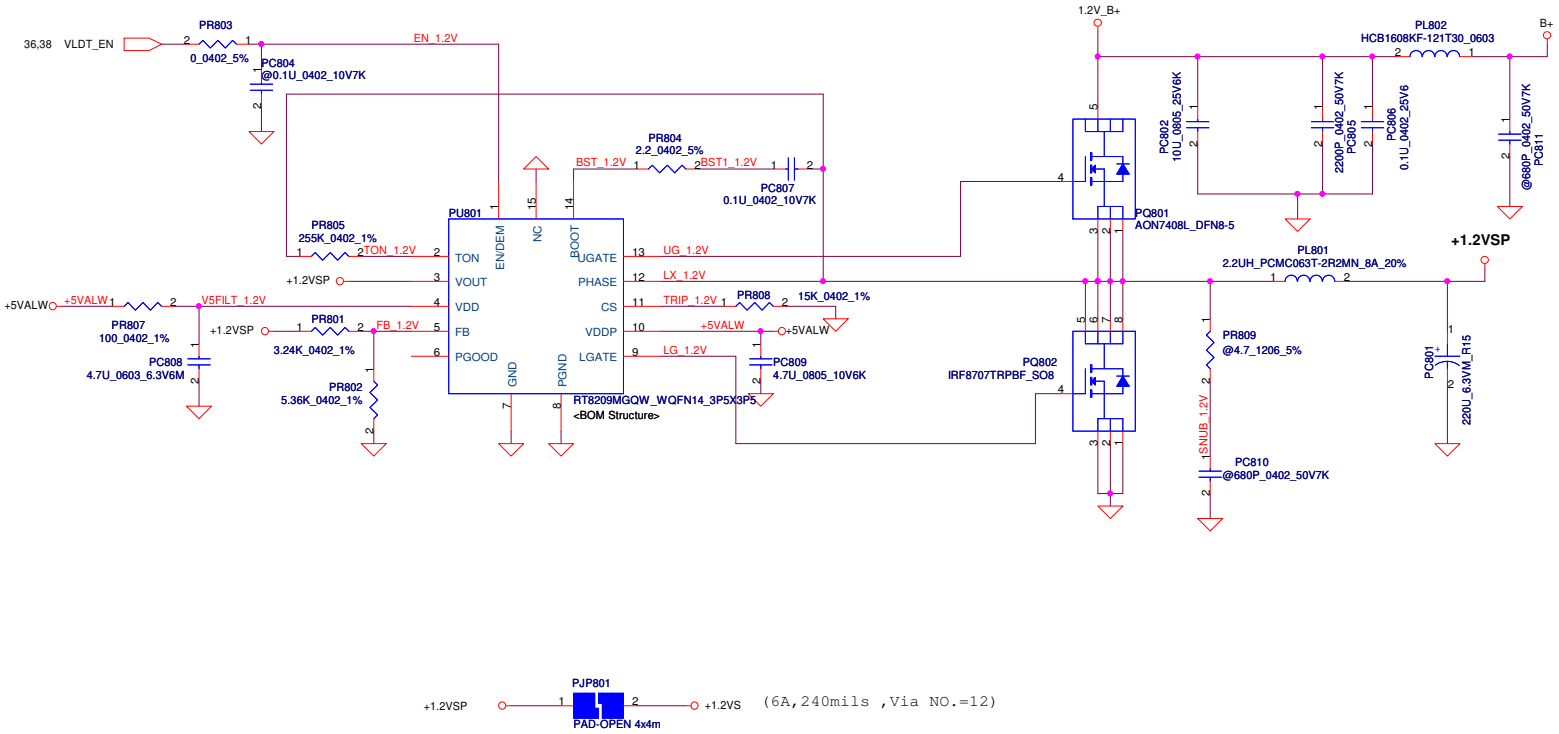
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **PWR 0.75VSP/1.0VSP/2.5VSP**

Size	Document Number	Rev
	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 45 of 49



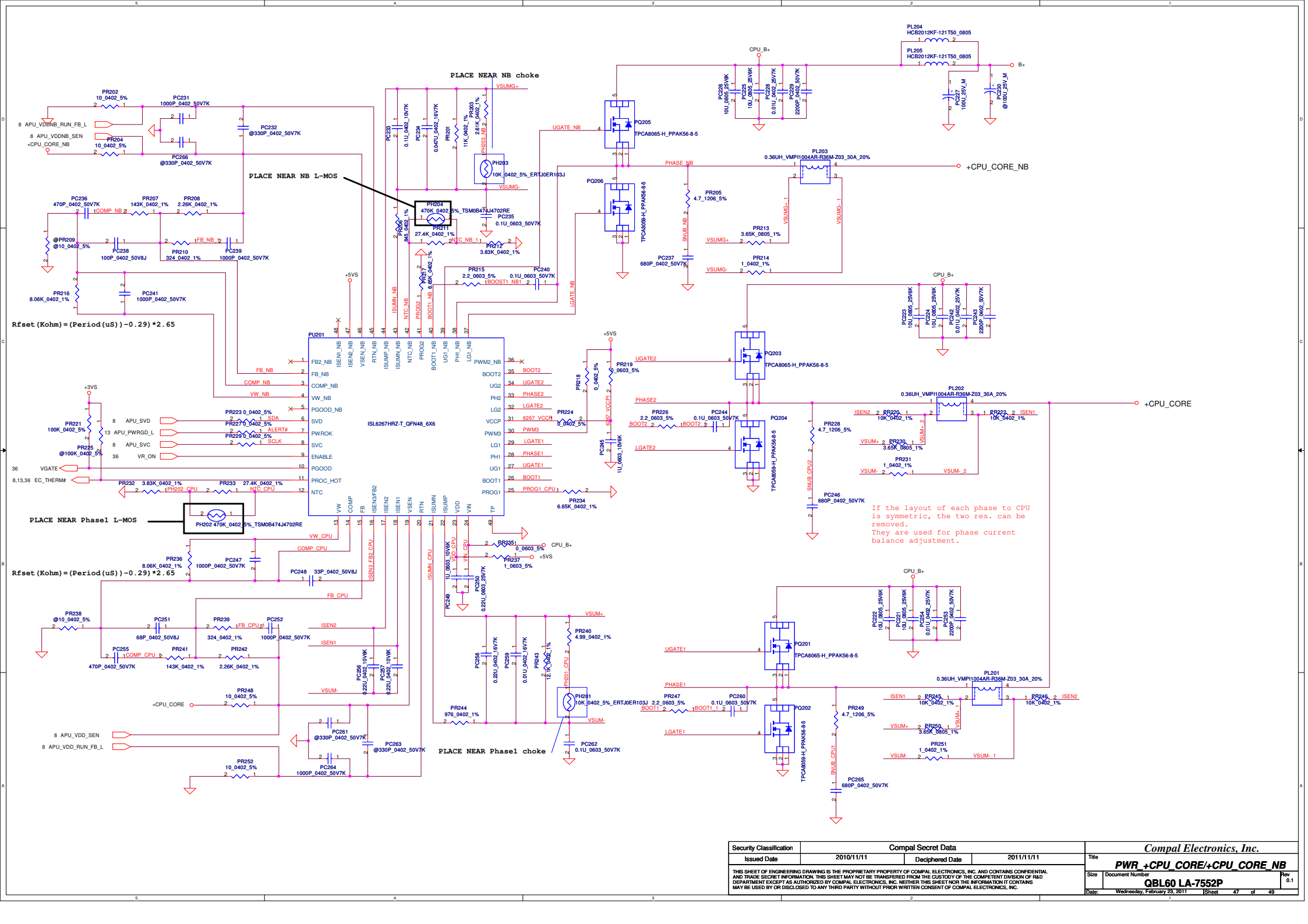
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.2VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

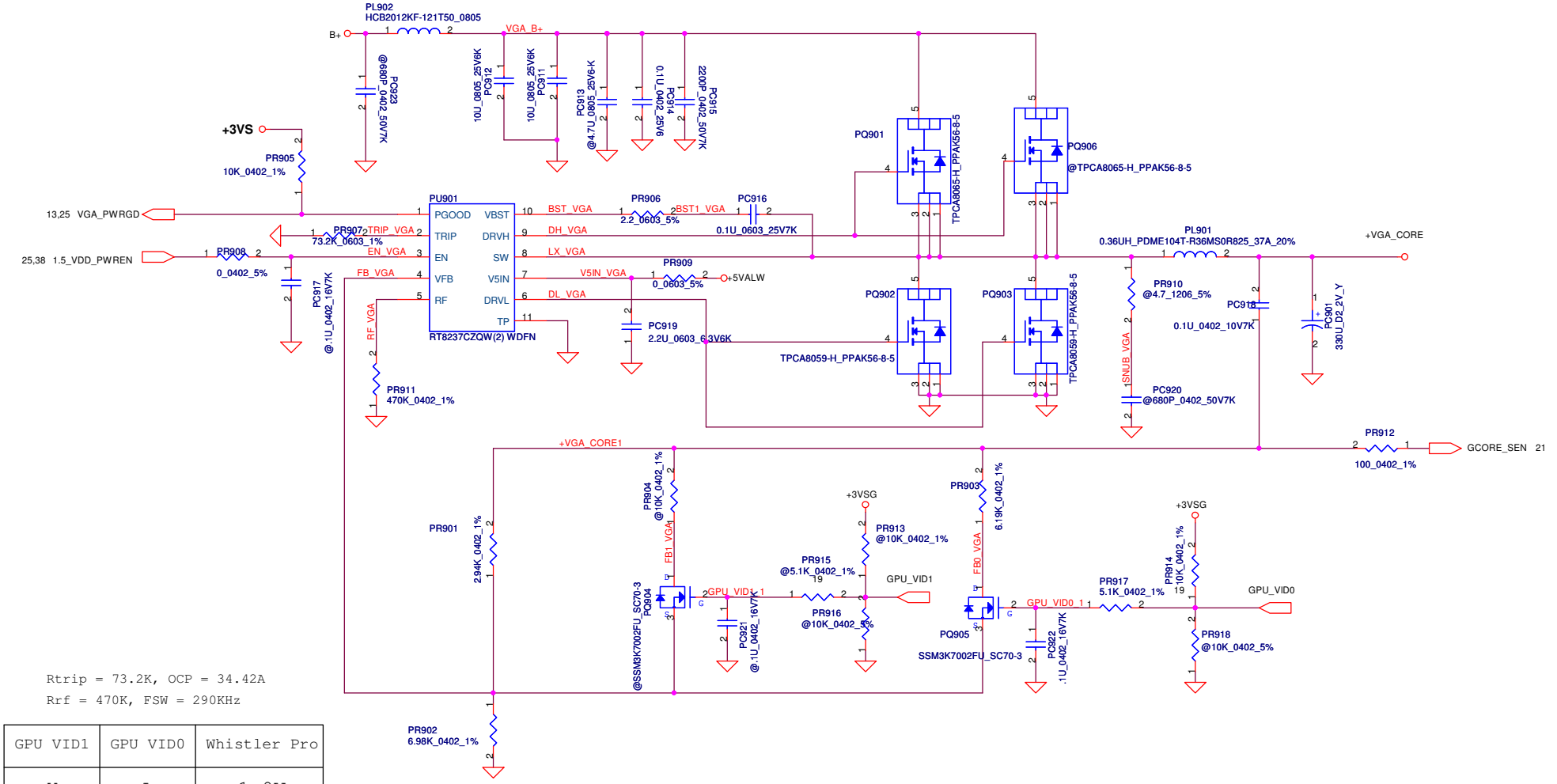
Date: Wednesday, February 23, 2011 | Sheet 46 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/11/11

Compal Electronics, Inc.

Title	PWR_+CPU_CORE/+CPU_CORE_NB		
Size	Document Number		Rev
	QBL60 LA-7552P		0.1
Date:	Wednesday, February 23, 2011	Sheet	47 of 49



Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **VGA_CORE**

Size	Document Number	Rev
	QBL60 LA-7552P	0.1

Date: Wednesday, February 23, 2011 | Sheet 48 of 49

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Compal Electronics, Inc.
Title: Changed-List History
Size: Document Number: QBL60 LA-7552P Rev: 0.1
Date: Wednesday, February 23, 2011 Sheet 49 of 49