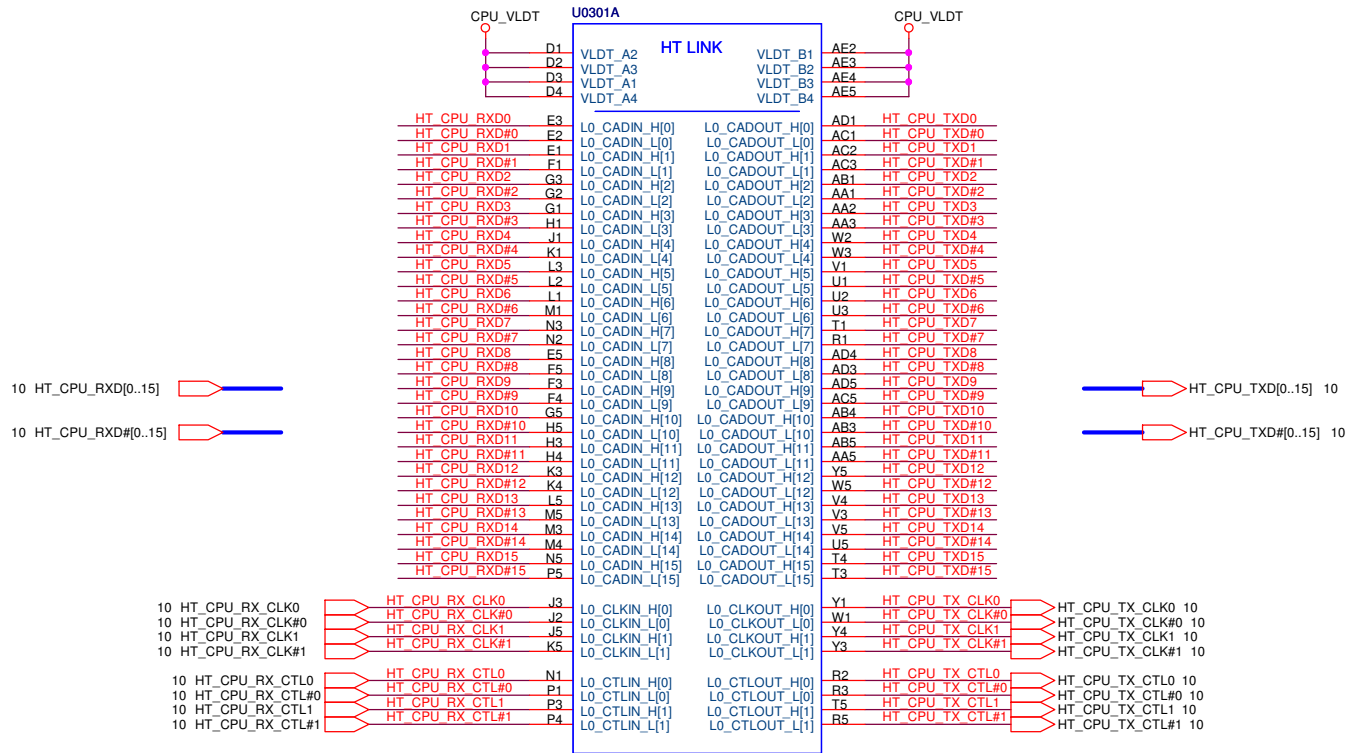
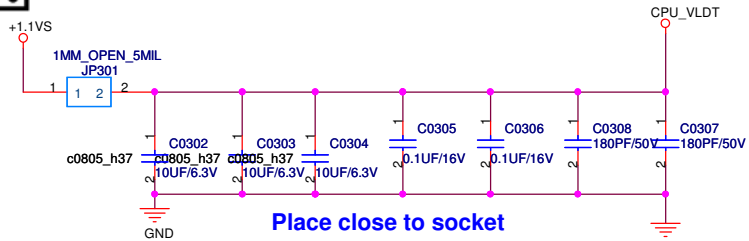


1.5A

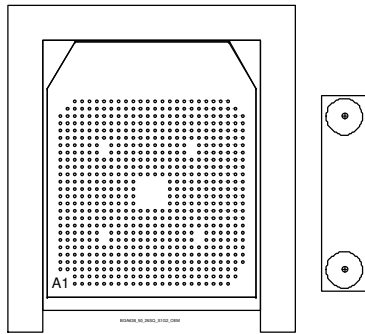


SOCKET638
Change P/N to 12G011306380
071113

Do not cross plane.

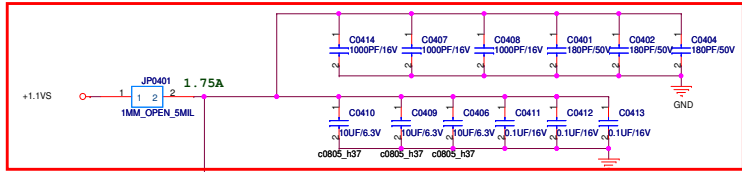


* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

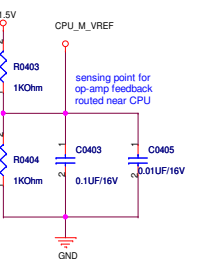
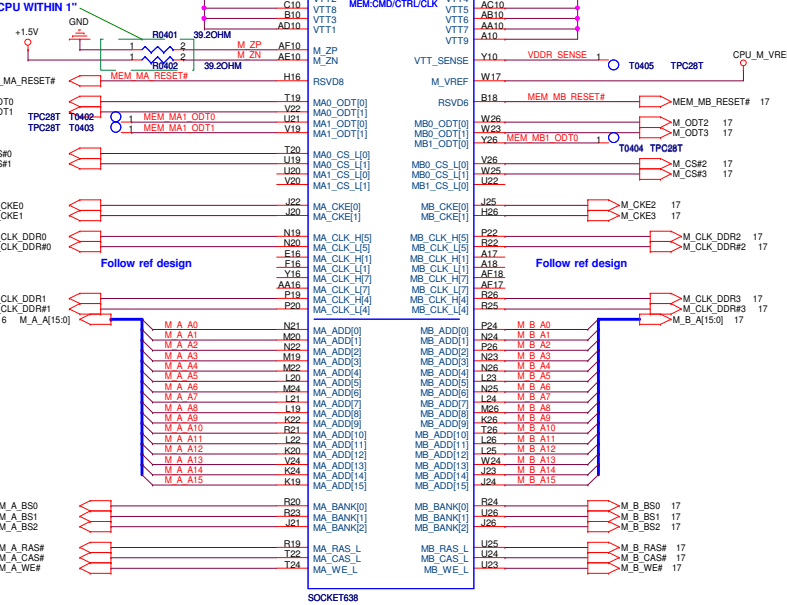


ASUS		Title : Griffin HT I/F	
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent_Chiang	
Size	Project Name	Rev	
B	K52N	1.0	
Date: Monday, February 08, 2010		Sheet	3 of 93

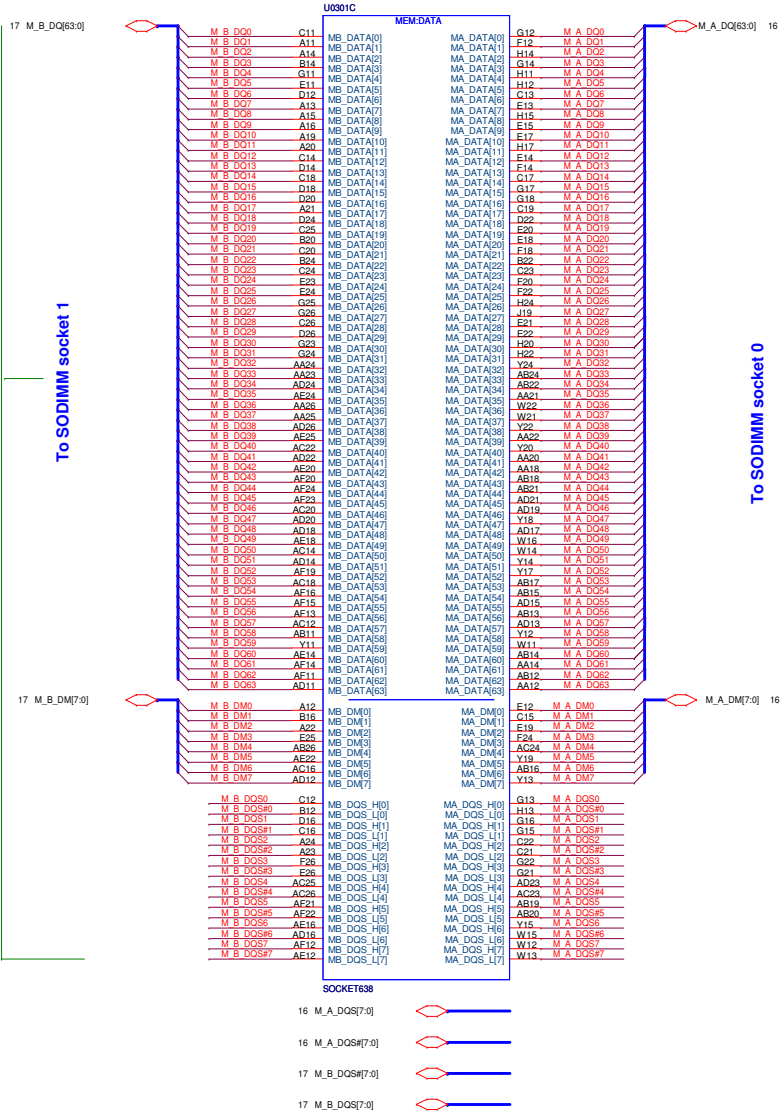
place close to socket



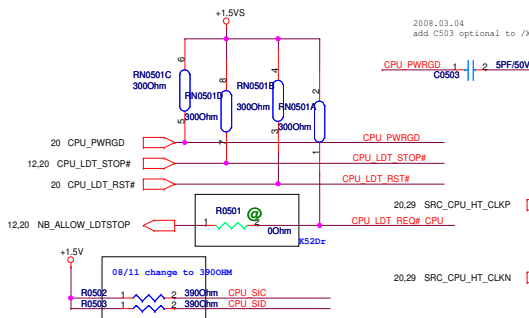
PLACE THEM CLOSE TO CPU WITHIN 1"



Processor Memory Interface

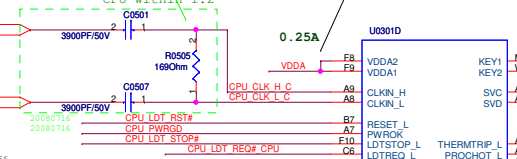
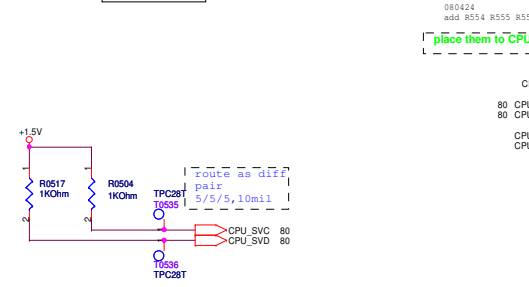


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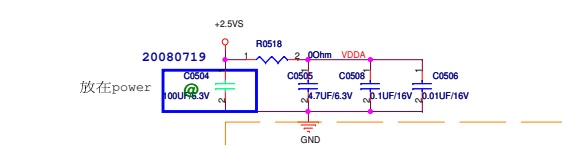
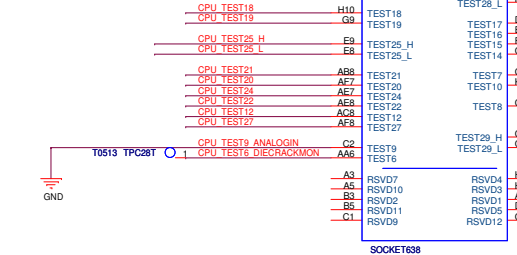
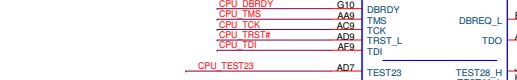
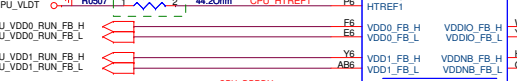


LAYOUT: ROUTE VDDA TRACE APPROX.
50 MILLS WIDE (USE 2x25 MIL TRACES TO
EXIT BALL FIELD) AND 500 MILS LONG.

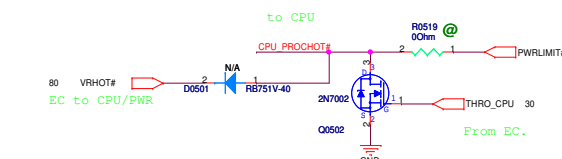
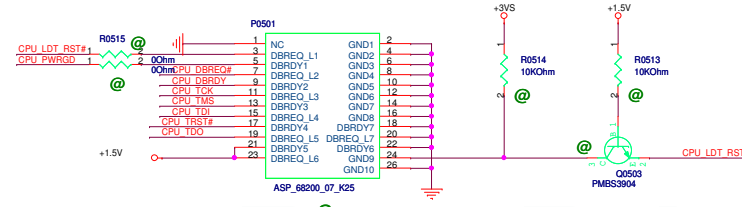
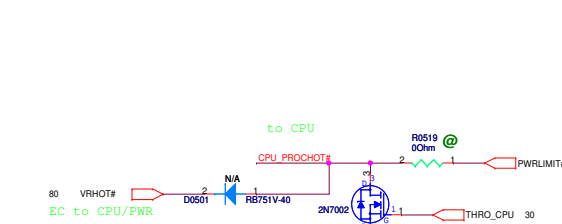
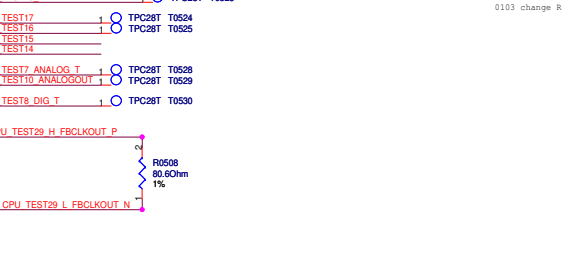
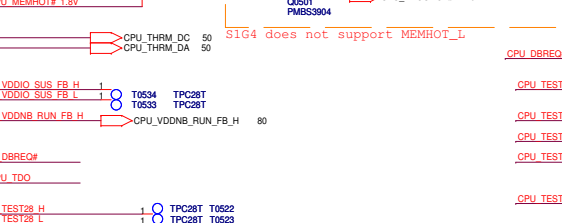
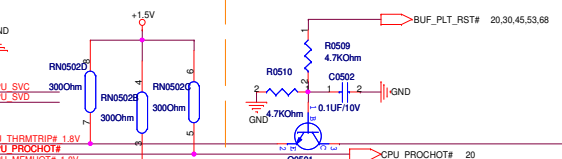
keep trace from resistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"

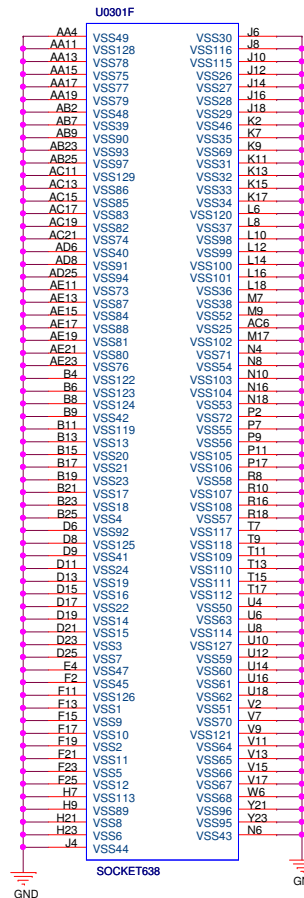
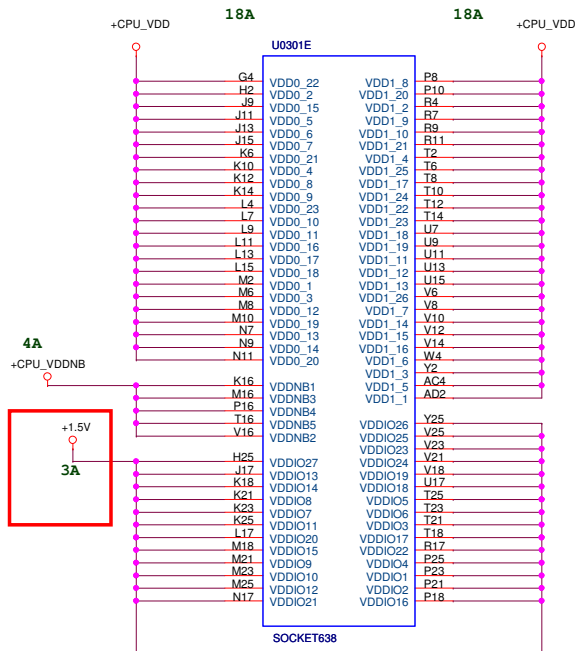


place them to CPU within 1.5"

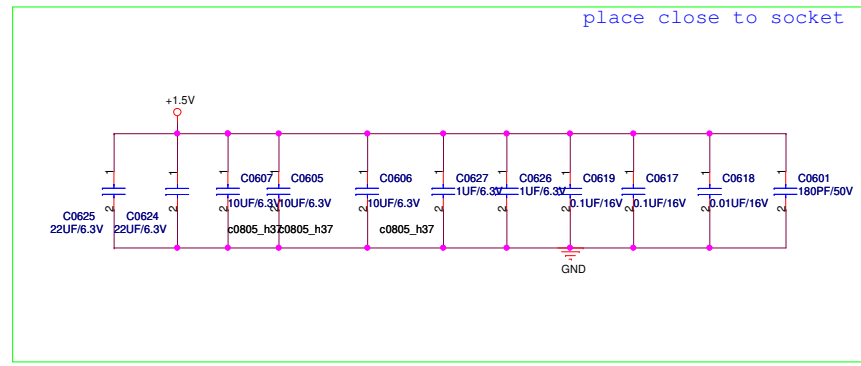
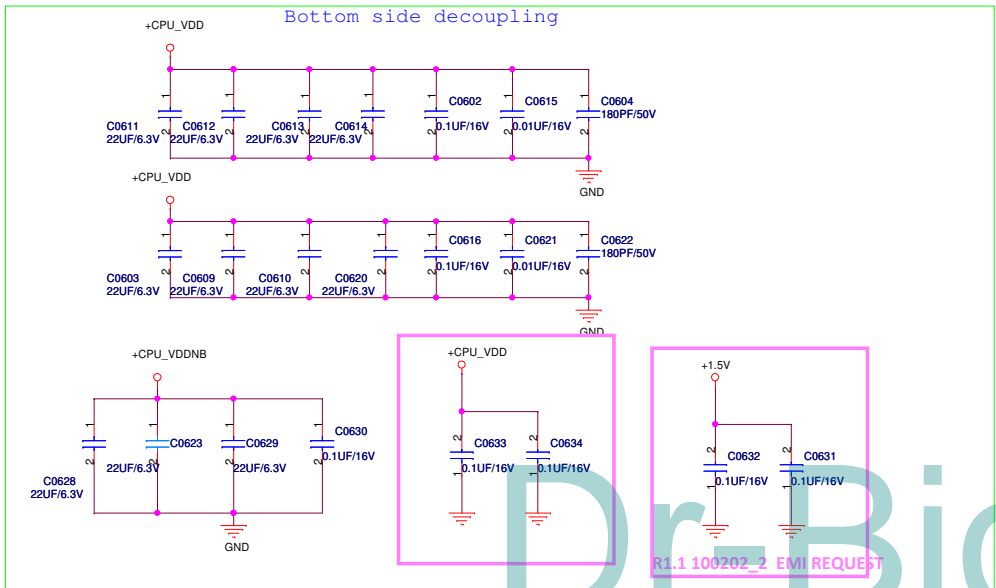


- T0514 TPC28T 1 CPU_CLK_H_C
- T0515 TPC28T 1 CPU_CLK_L_C
- T0516 TPC28T 1 CPU_LDT_STOP#
- T0517 TPC28T 1 CPU_PWRGD
- T0518 TPC28T 1 CPU_VDDIO_RUN_FB_H
- T0519 TPC28T 1 CPU_VDDIO_RUN_FB_L
- T0520 TPC28T 1 CPU_VDD1_RUN_FB_H
- T0521 TPC28T 1 CPU_VDD1_RUN_FB_L



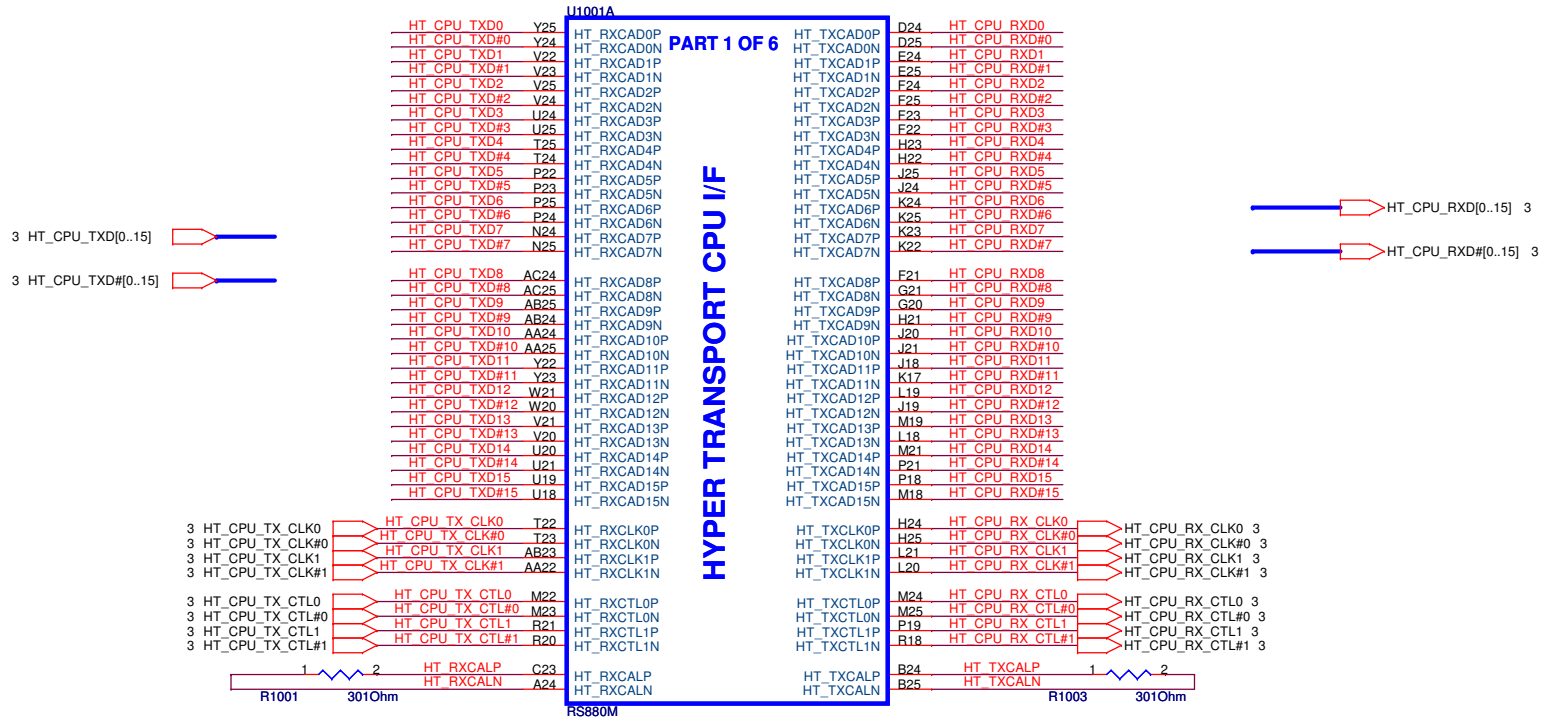


Decoupling between Processor and DIMMs, Place close to Porcessor as possible



place close to socket

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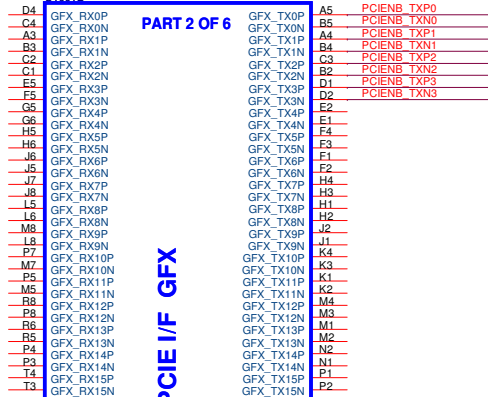
		Title : RS880M-HT LINK I/F
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent_Chiang
Size	Project Name	Rev
B	K52N	1.0
Date: Monday, February 08, 2010		Sheet 10 of 93

PCI-E:
0-3 HDMI@ RS780M
4-7 NC
8-15 VGA8x

HDMI

U1001B

PART 2 OF 6

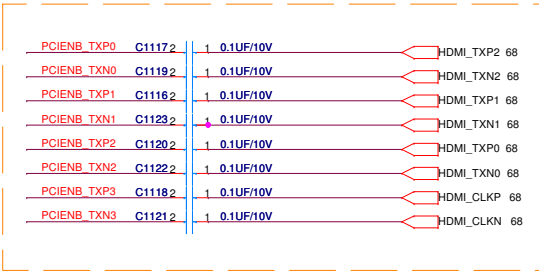


PCI-E I/F GFX

PCI-E I/F GPP

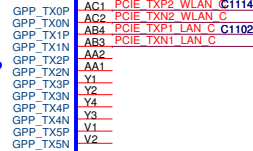
PCI-E I/F SB

RS880M



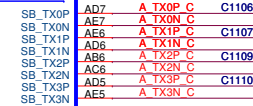
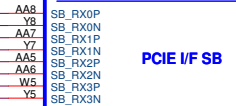
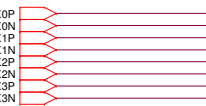
Wlan
Lan

53 PCIE_RXP2_WLAN
53 PCIE_RXN2_WLAN
68 PCIE_RXP1_LAN
68 PCIE_RXN1_LAN

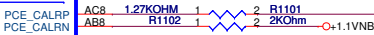


PCIE_TXP2_C 53
PCIE_TXN2_C 53
PCIE_TXP1_C 68
PCIE_TXN1_C 68

20 PCIE_SB_NB_RX0P
20 PCIE_SB_NB_RX0N
20 PCIE_SB_NB_RX1P
20 PCIE_SB_NB_RX1N
20 PCIE_SB_NB_RX2P
20 PCIE_SB_NB_RX2N
20 PCIE_SB_NB_RX3P
20 PCIE_SB_NB_RX3N



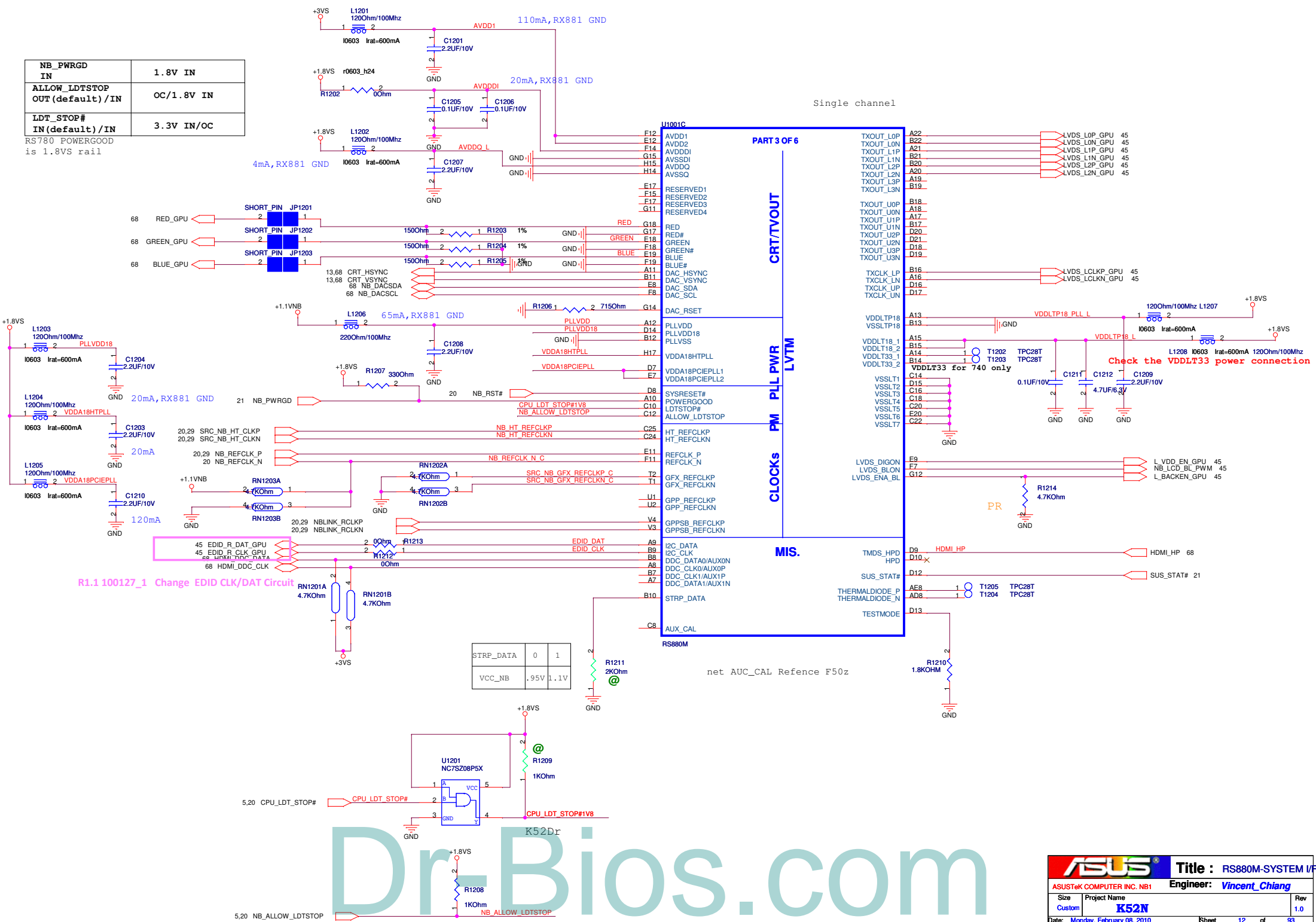
PCIE_NB_SB_TX0P 20
PCIE_NB_SB_TX0N 20
PCIE_NB_SB_TX1P 20
PCIE_NB_SB_TX1N 20
PCIE_NB_SB_TX2P 20
PCIE_NB_SB_TX2N 20
PCIE_NB_SB_TX3P 20
PCIE_NB_SB_TX3N 20



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NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT (default) / IN	OC/1.8V IN
LDT_STOP# IN (default) / IN	3.3V IN/OC

RS780 POWERGOOD
is 1.8VS rail

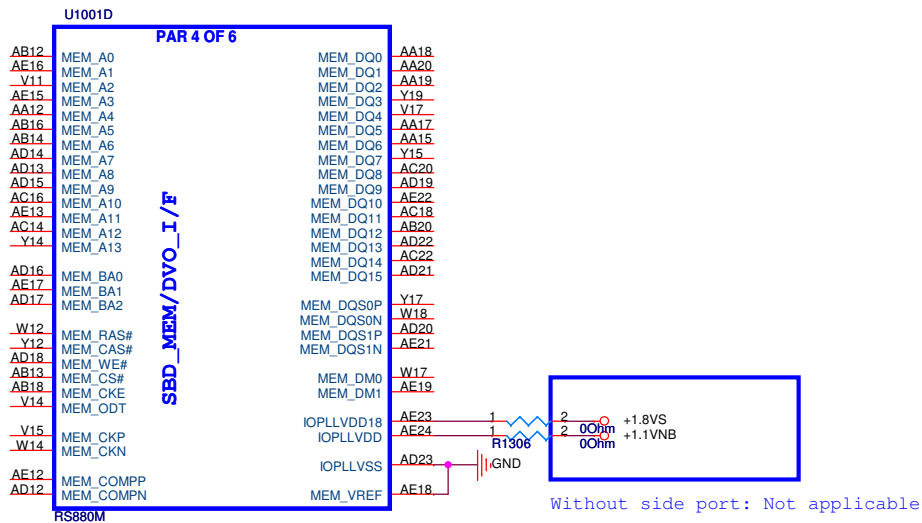


R1.1 100127_1 Change EDID CLK/DAT Circuit

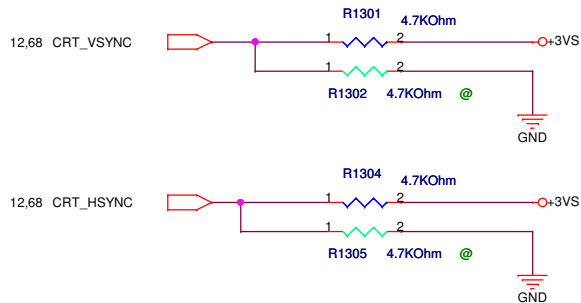
STRP_DATA	0	1
VCC_NB	.95V	1.1V

net AUC_CAL Reference F50z

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080118
 Disable Side Port Memory
 R1.1



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:

1 : Disable (Can still be enabled using nbocfg register access)
 0 : Enable

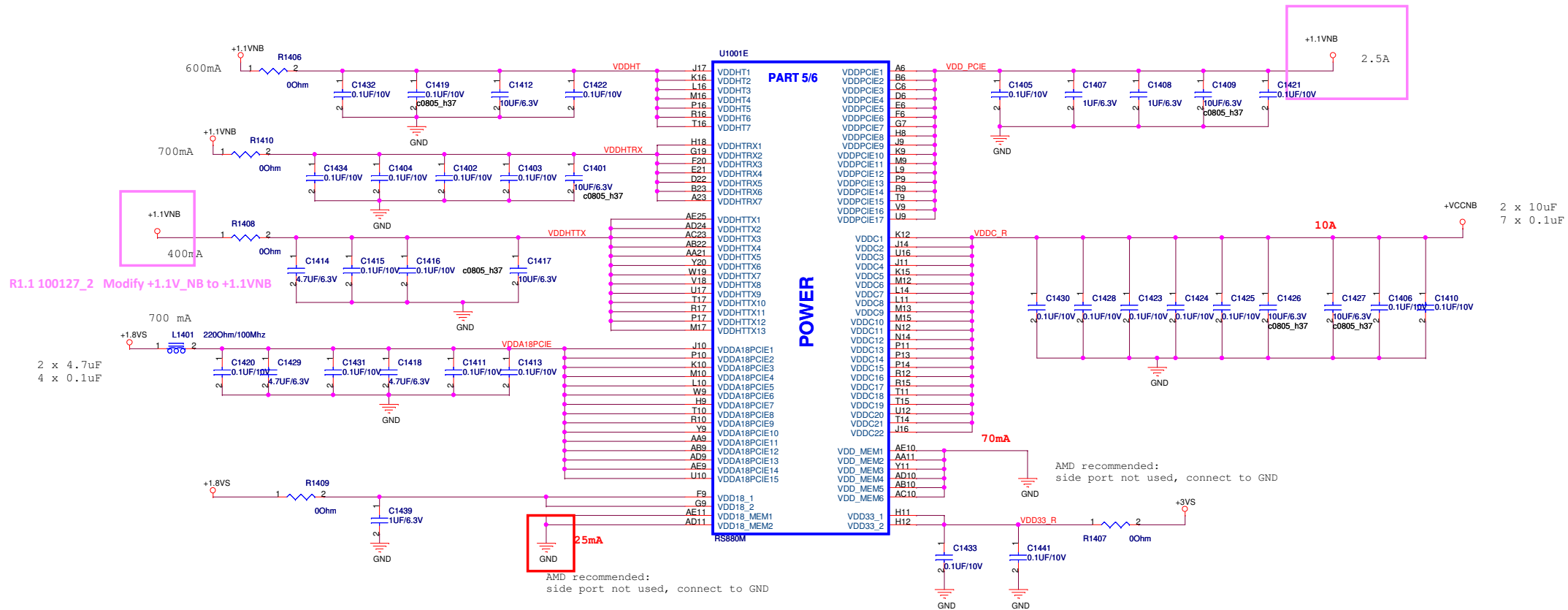
RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory

RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
 1 = Memory Side port Not available
 0 = Memory Side port available
 Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

ASUS		Title : RS880M-SPMEM/STRAPS	
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent_Chiang	
Size	Project Name	Rev	
B	K52N	1.0	
Date: Monday, February 08, 2010		Sheet	13 of 93

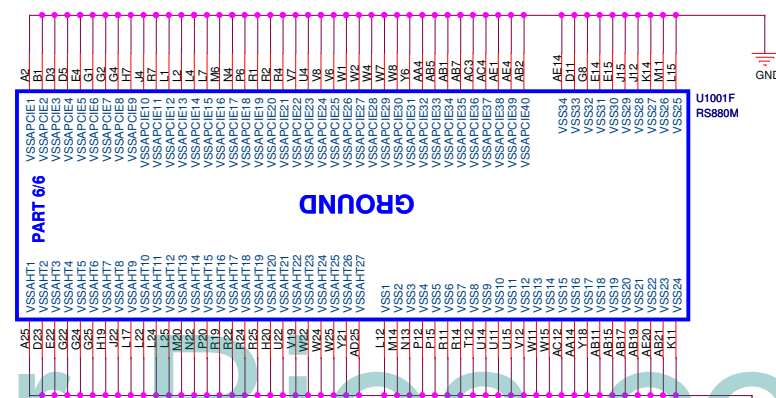


R1.1 100127_2 Modify +1.1V_NB to +1.1VNB

2 x 4.7uF
4 x 0.1uF

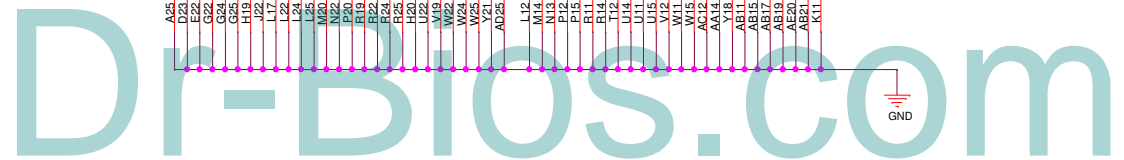
AMD recommended:
side port not used, connect to GND

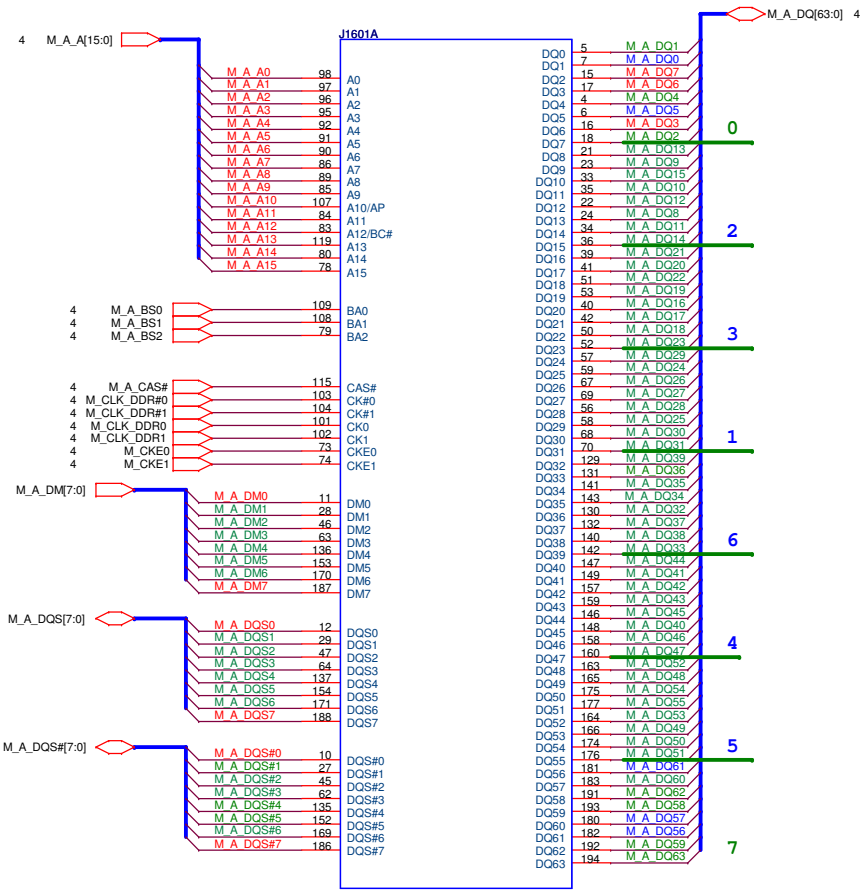
AMD recommended:
side port not used, connect to GND



RS880M POWER TABLE

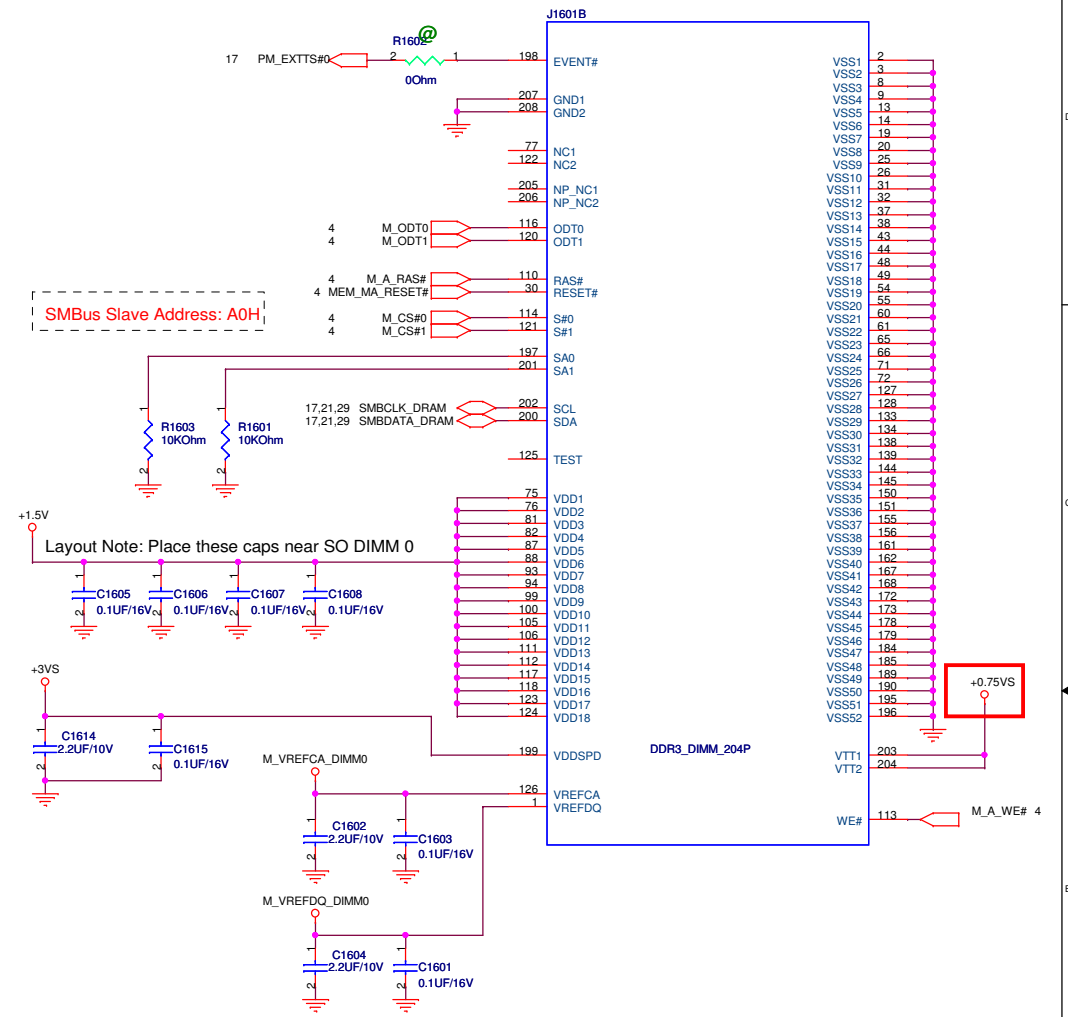
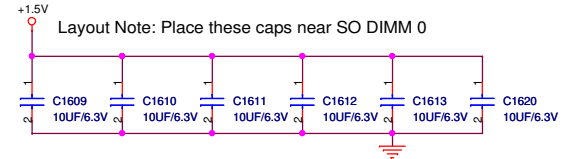
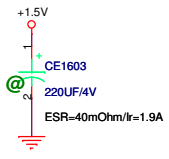
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL18	NC



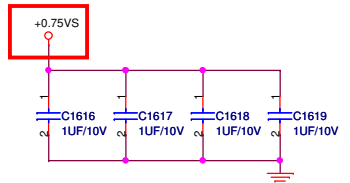


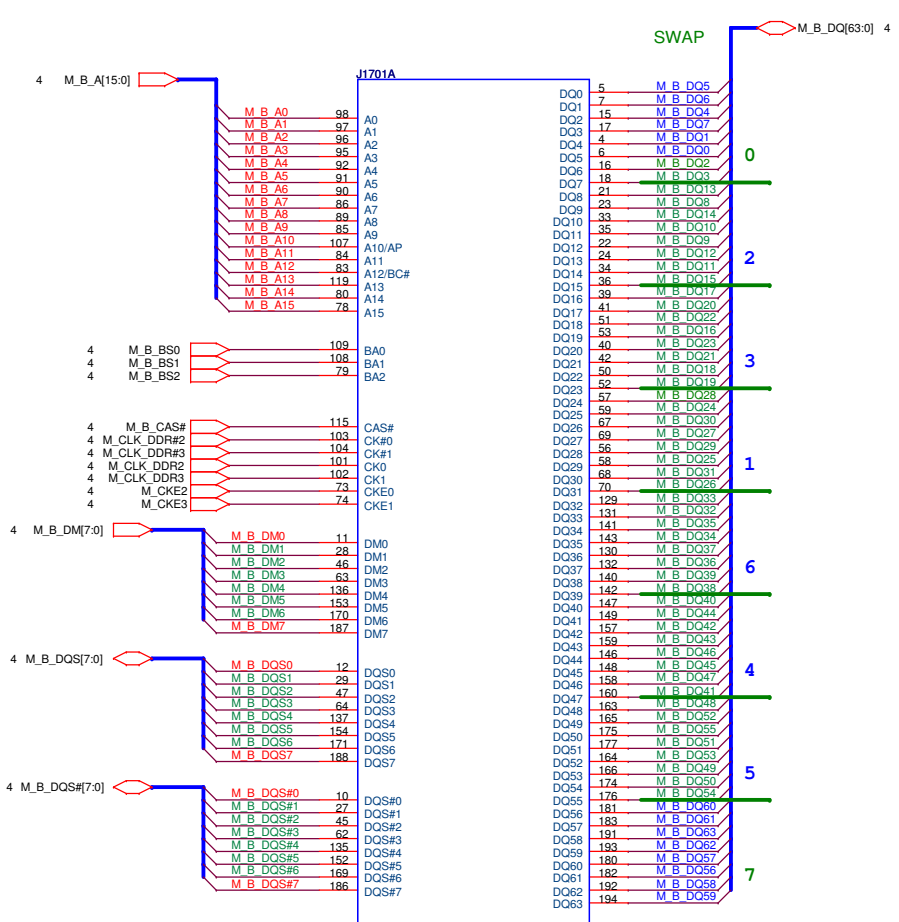
STD 5.2mm

DDR3_DIMM_204P



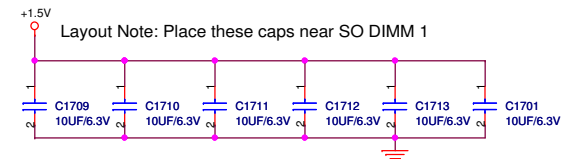
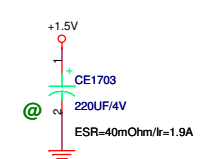
Layout Note: Place these caps near SO DIMM 0



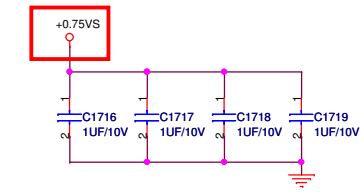
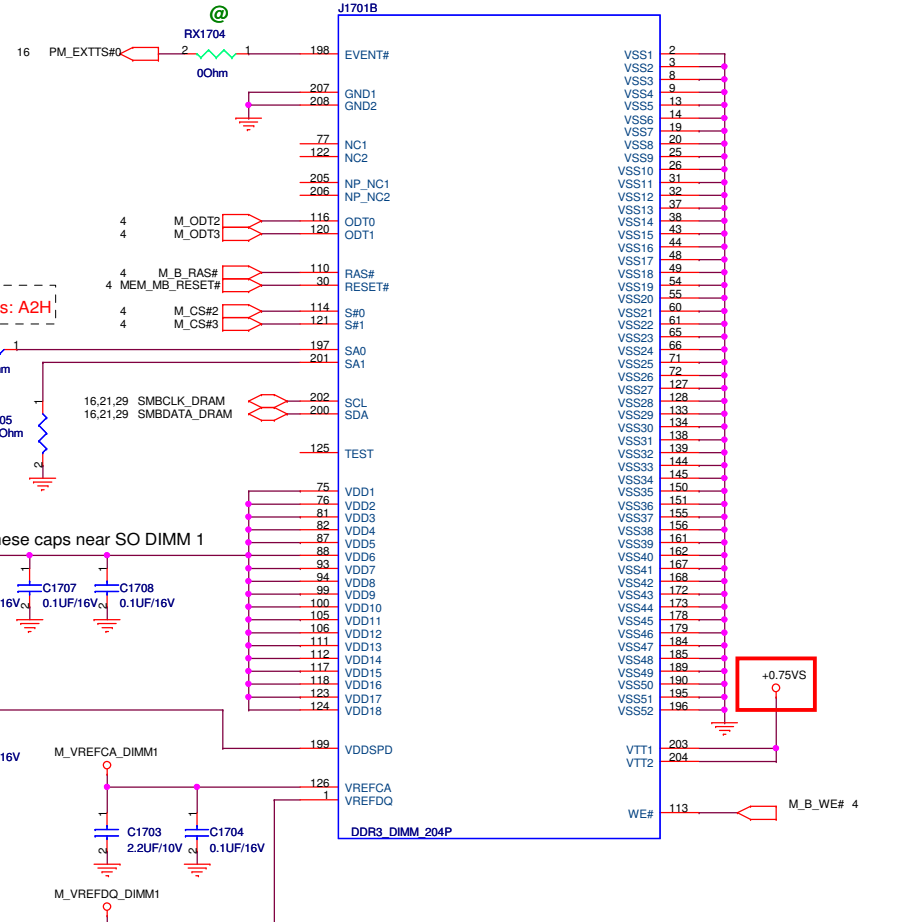
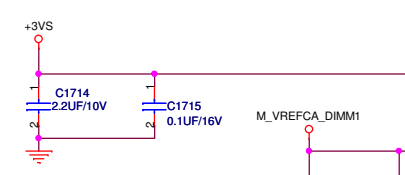
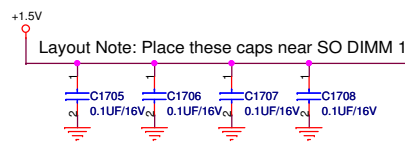
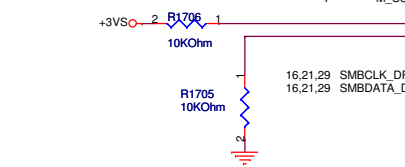


STD 9.2mm

DDR3_DIMM_204P

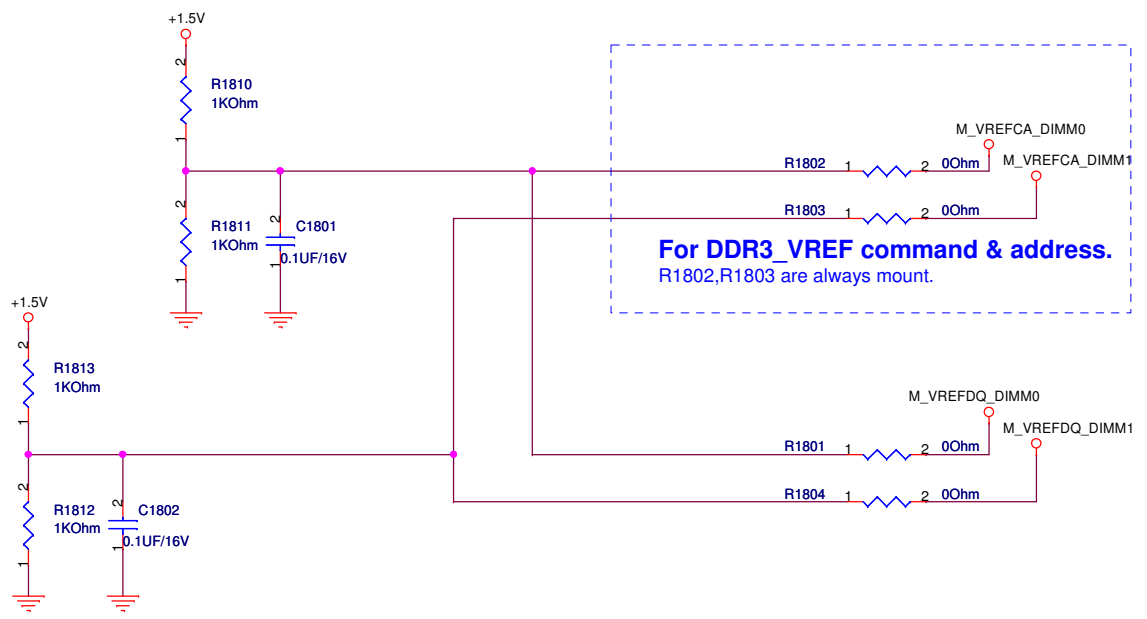


SMBus Slave Address: A2H



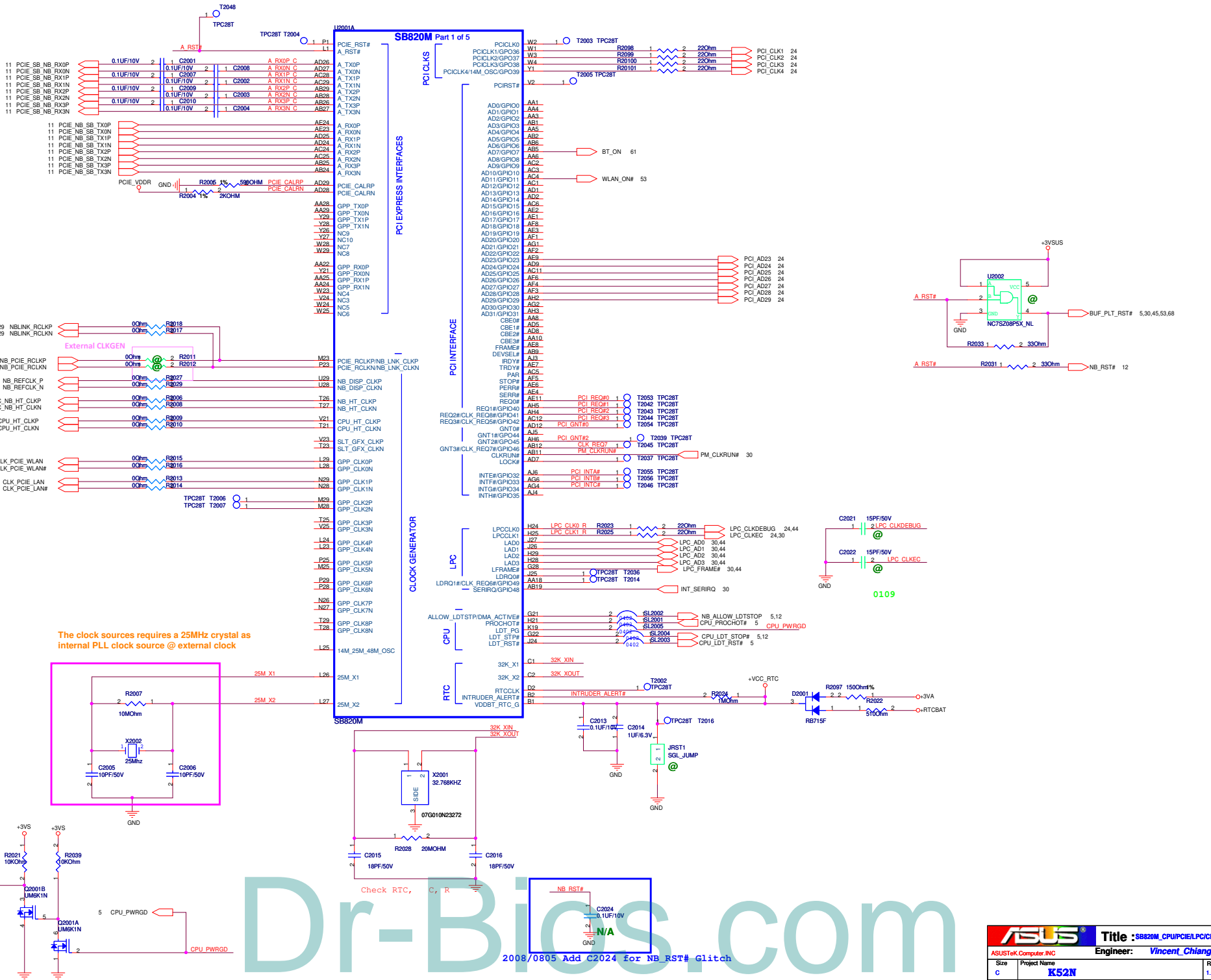
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DDR3 Vref

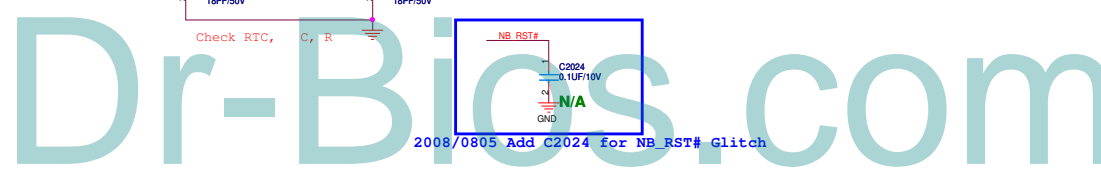


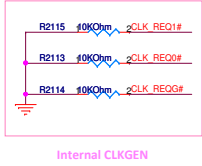
Dr-Bios

		Title DDR3 CA_DQ VOLTAGE	
ASUSTeK COMPUTER INC. NB6		Engineer: Vincent_Chiang	
Size	Project Name	Rev	
Custom	K52N	2.0	
Date: Monday, February 08, 2010		Sheet	18 of 99

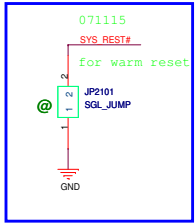


The clock source requires a 25MHz crystal as
internal PLL clock source @ external clock



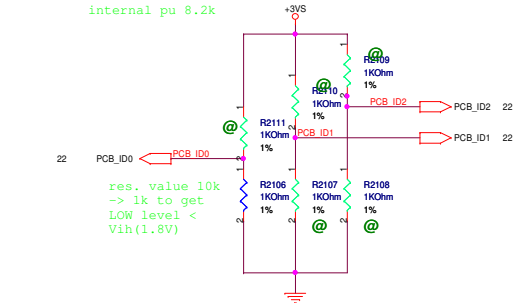


Internal CLKGEN

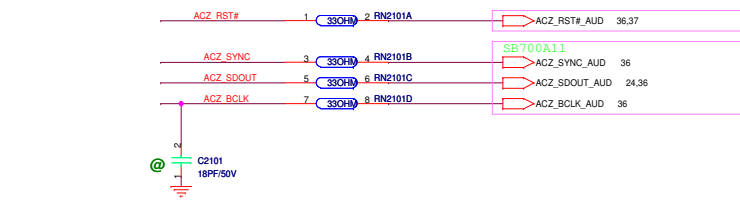


071115
SYS_RST#
for warm reset

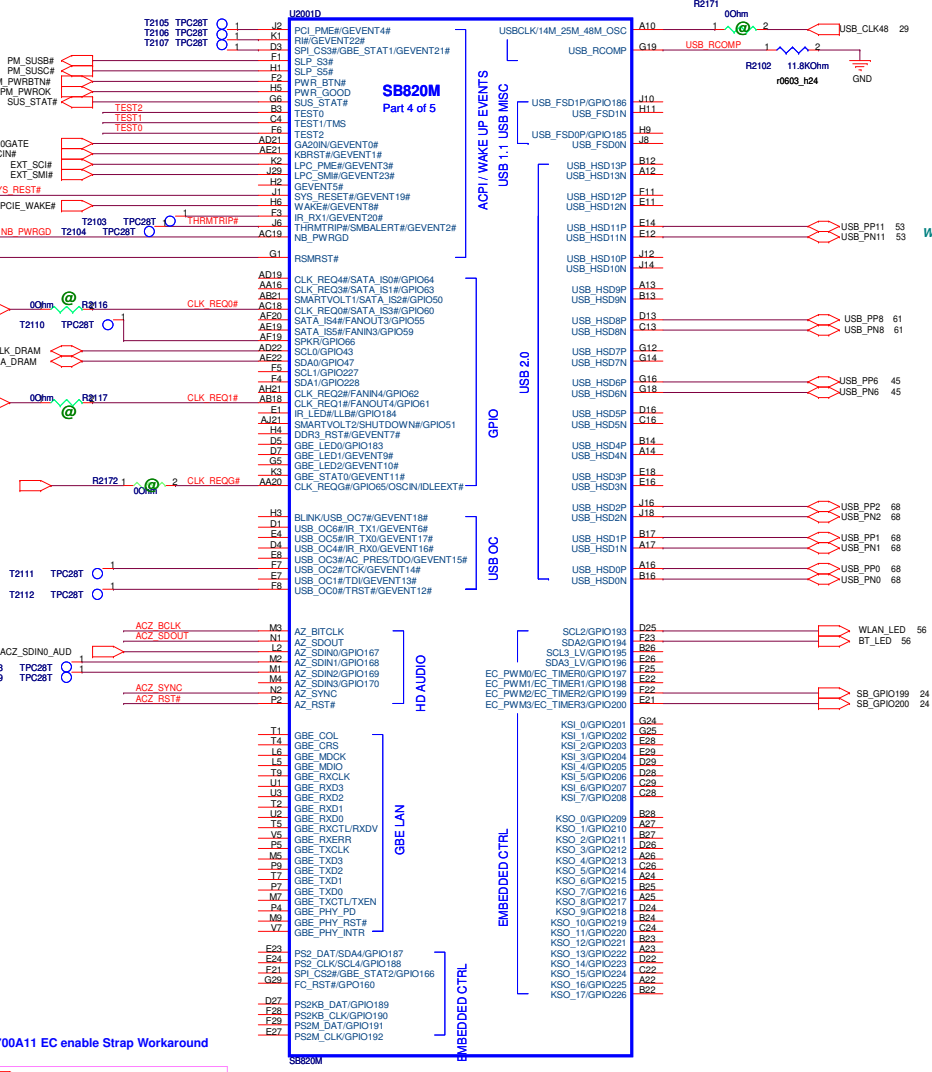
internal pu 8.2k



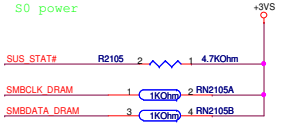
PUP AT SB700 SIDE



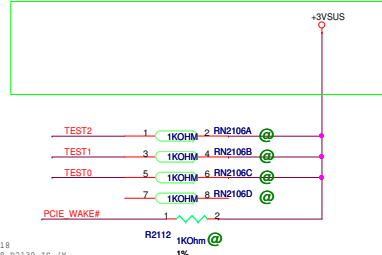
SB700A11 EC enable Strap Workaround



USB 0	External USB
USB 1	External USB
USB 2	External USB
USB 3	
USB 4	
USB 5	
USB 6	CAMERA
USB 7	
USB 8	BT
USB 9	
USB 10	
USB 11	WLAN (MiniCard)
USB 12	
USB 13	



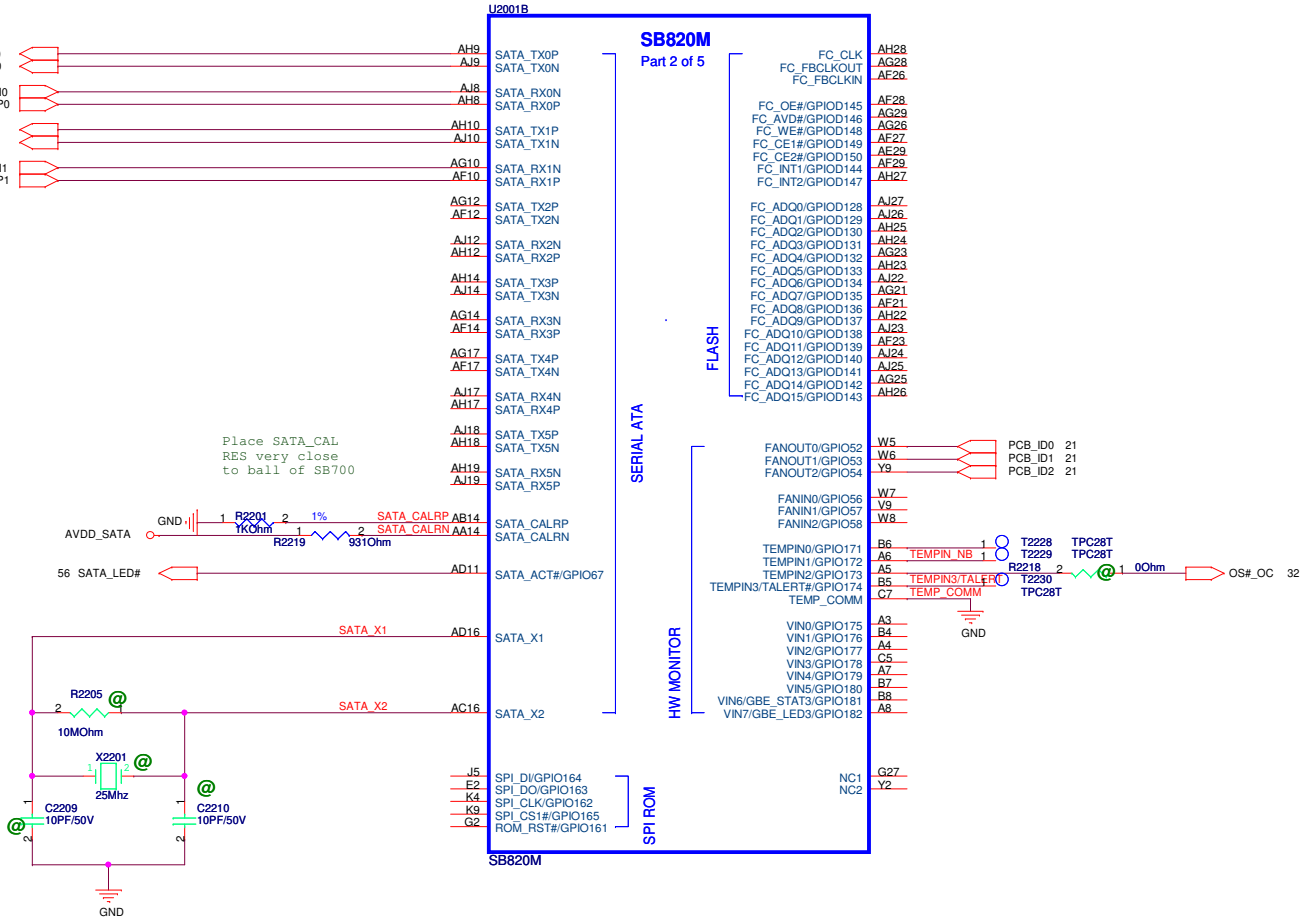
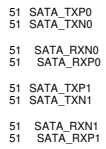
S0 power



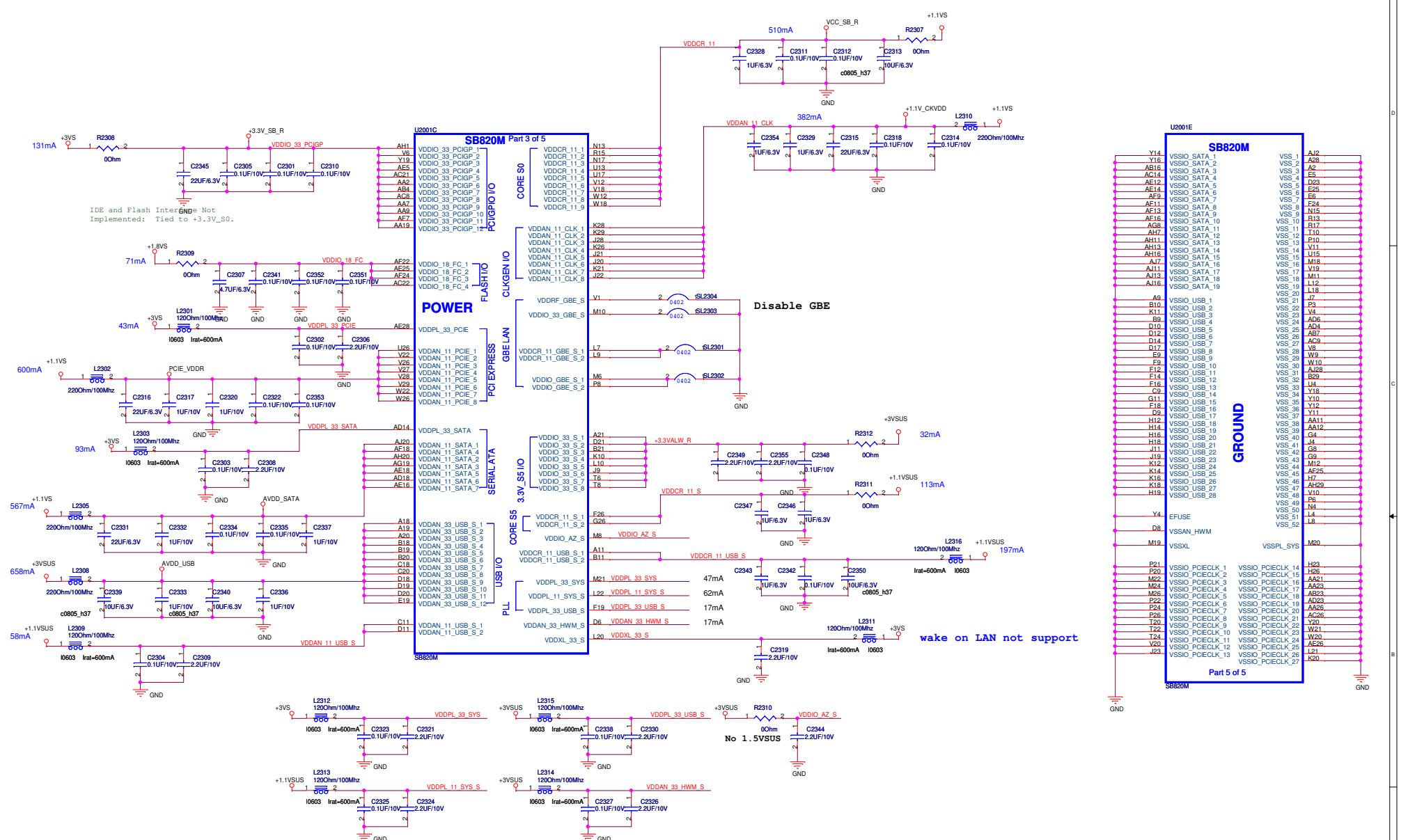
2008 04 18
ADD R2138 R2139 IS / X

for SATA HDD

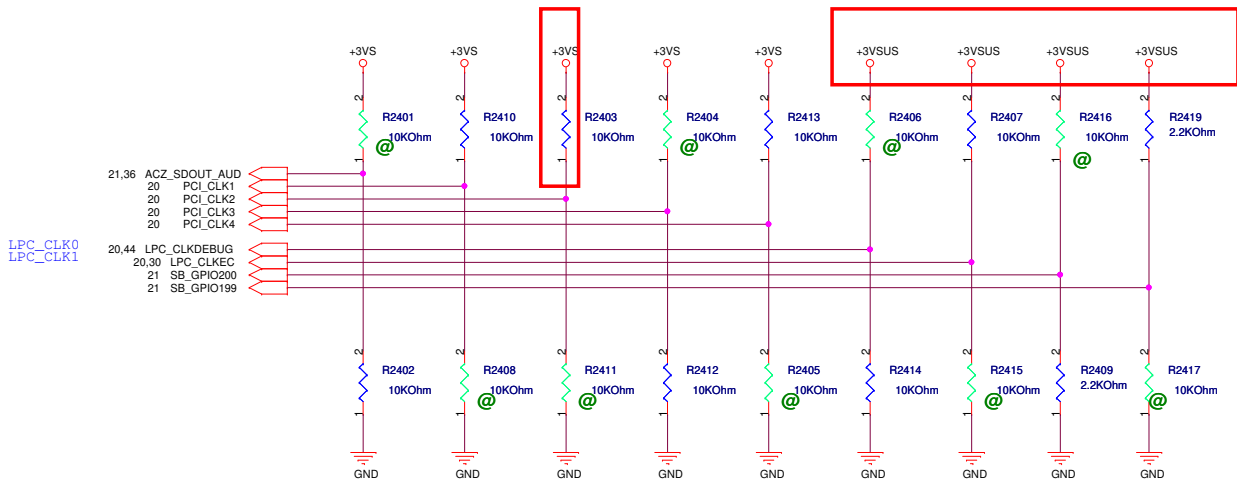
for SATA ODD



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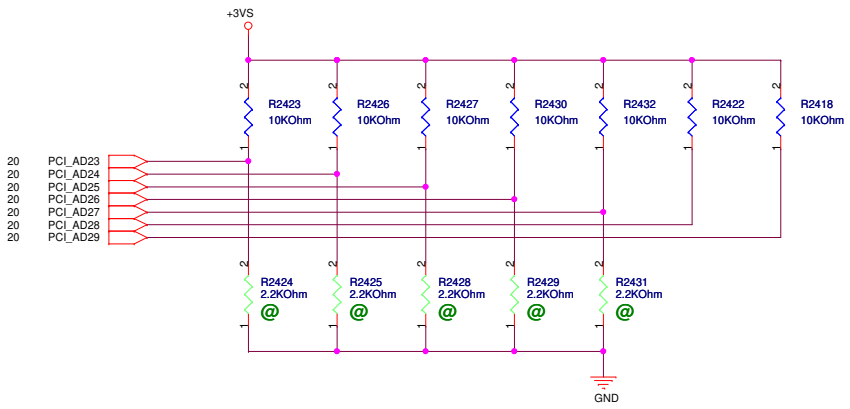


Dr-Bios.com



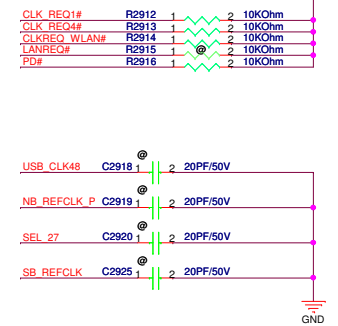
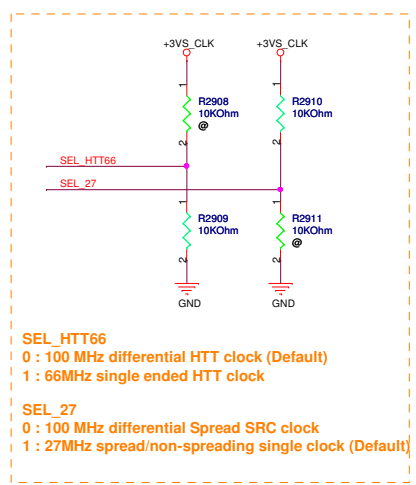
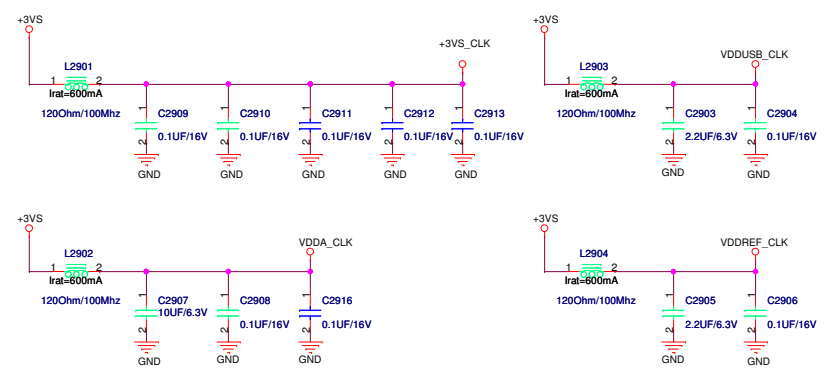
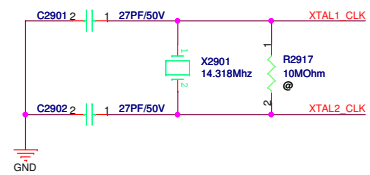
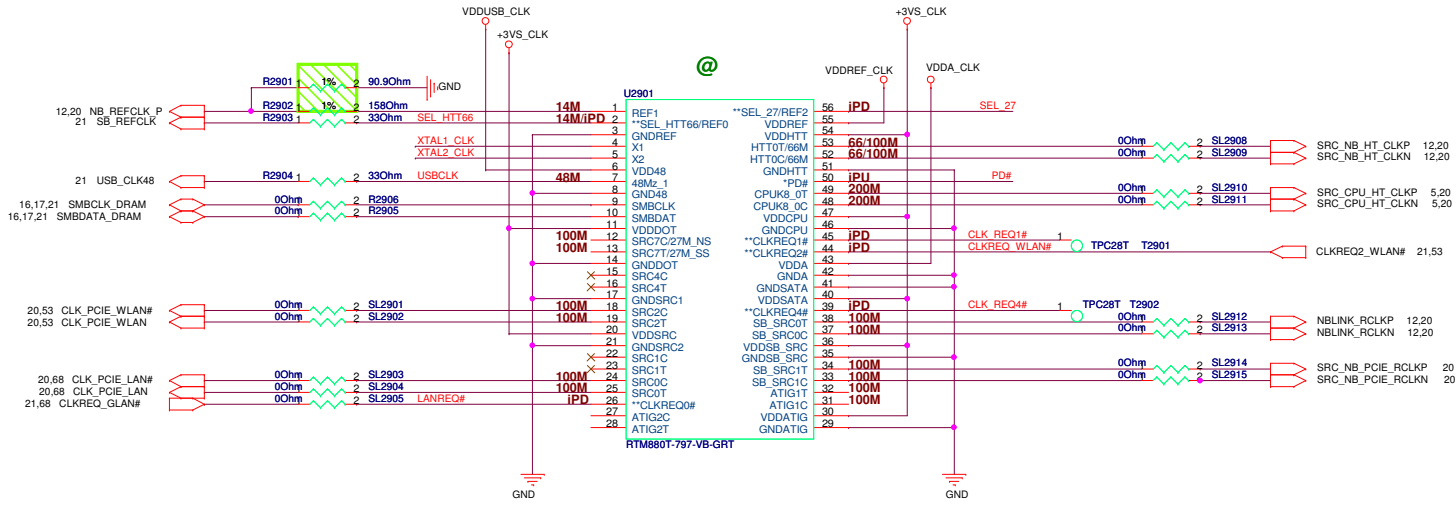
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled Modify	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

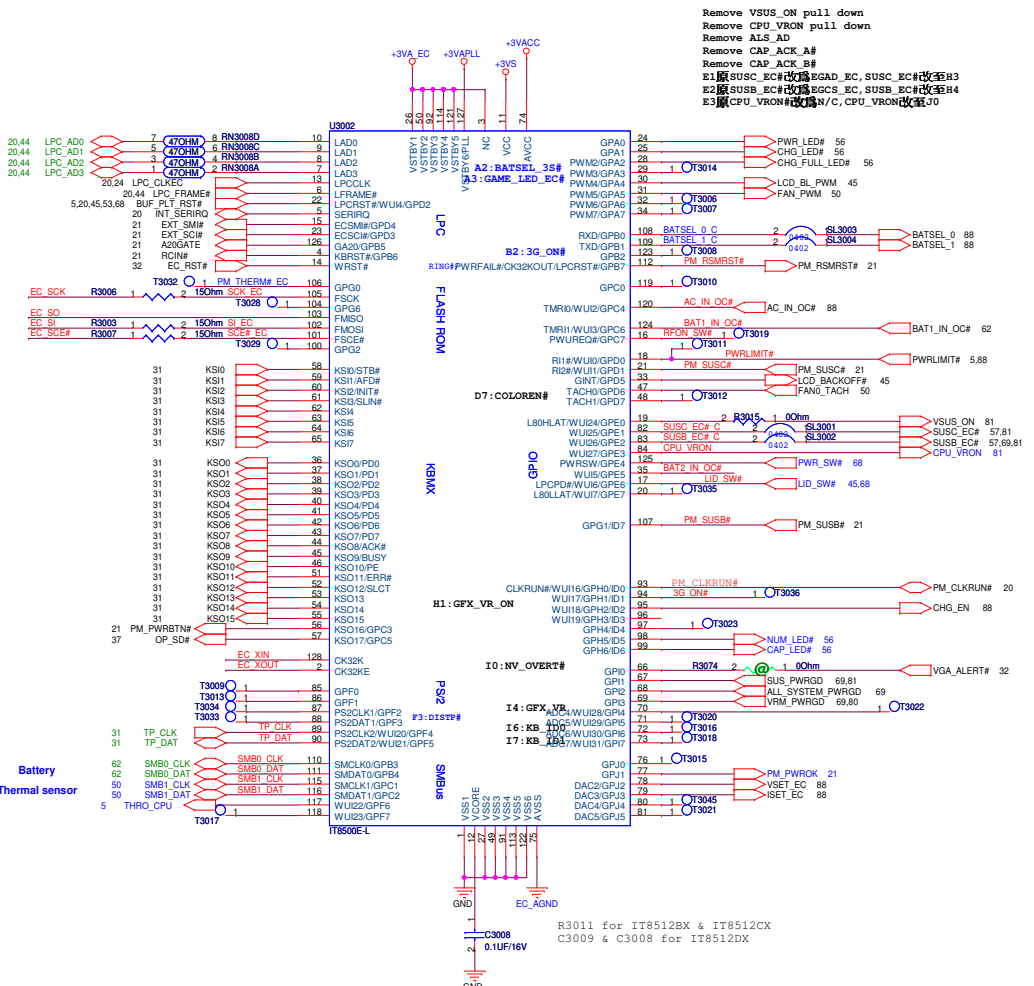
Dr-Bios.com



SEL_HTT66
 0 : 100 MHz differential HTT clock (Default)
 1 : 66MHz single ended HTT clock

SEL_27
 0 : 100 MHz differential Spread SRC clock
 1 : 27MHz spread/non-spreading single clock (Default)

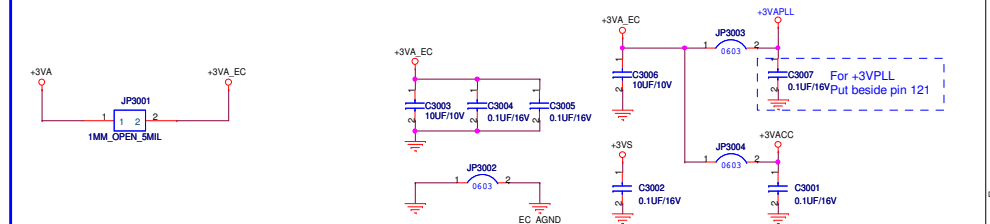
Dr-Bios.com



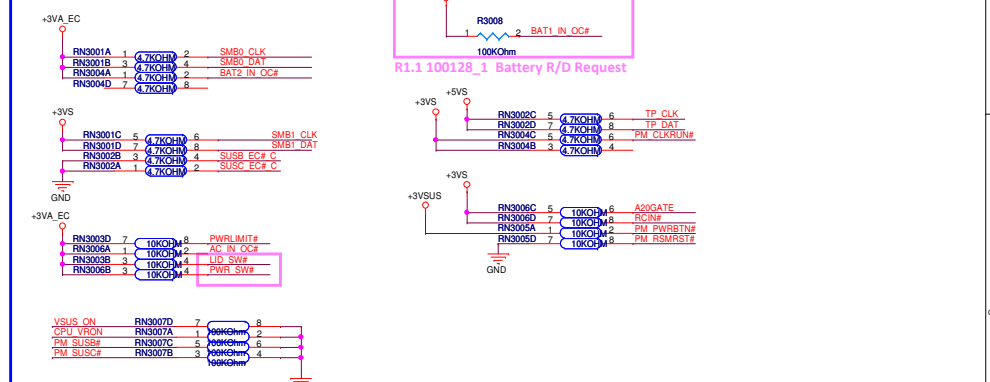
Remove VSUS_ON pull down
 Remove CPU_VRON pull down
 Remove ALS_AD
 Remove CAP_ACK_A#
 Remove CAP_ACK_B#
 E1原SUSC_EC改為EGAD_EC, SUSC_EC改為H3
 E2原SUSB_EC改為EGCS_EC, SUSB_EC改為H4
 E3原CPU_VRON改為N/C, CPU_VRON改為J0



R3011 for IT8512BX & IT8512CX
 C3009 & C3008 for IT8512DX



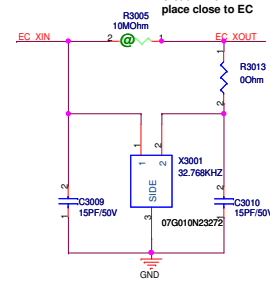
For PU / PD



iAMT EC strapping need to check

Note:
 EXT_SMI#, EXT_SC#, PU power plane
 depend on ICH9 GPIO.

For X'tal



For EC Hardware Strap

Note:
 Cloud=12.5PF
 place close to EC

For iAMT pin name

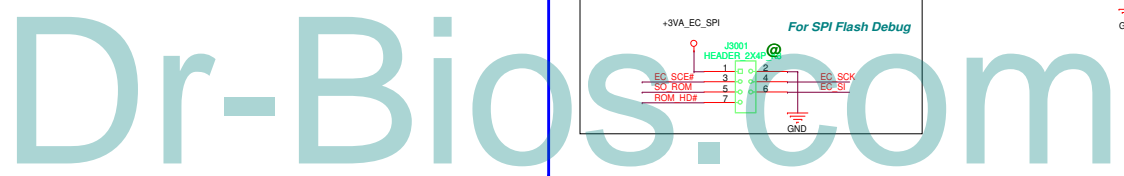
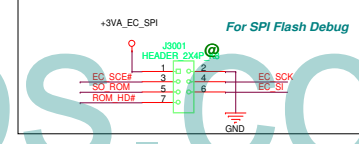
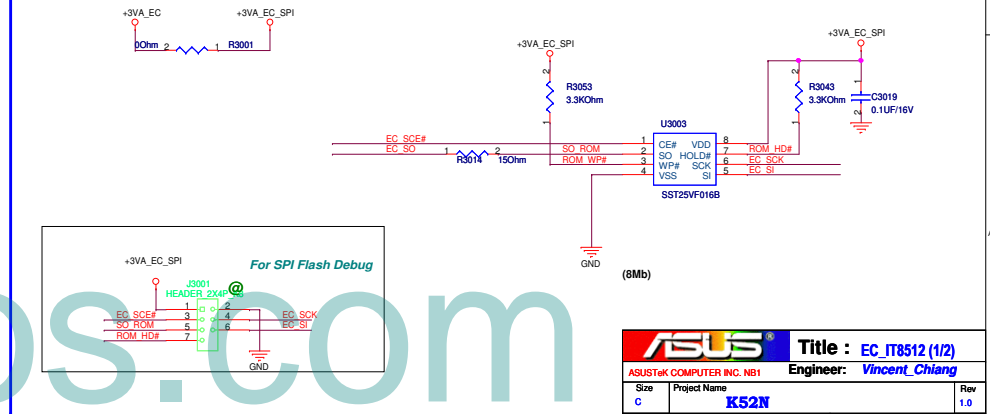
I/O Base Address
 Note: It can be programmable by EC firmware

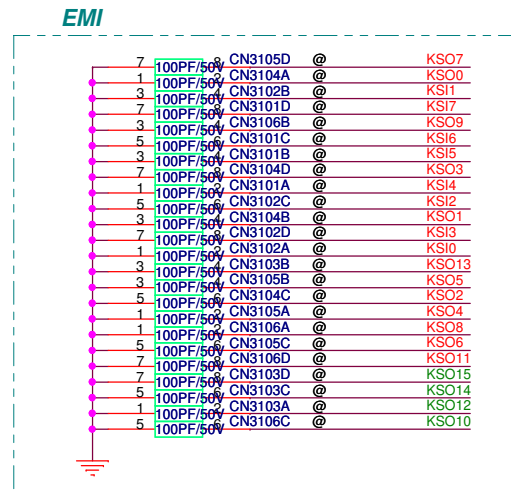
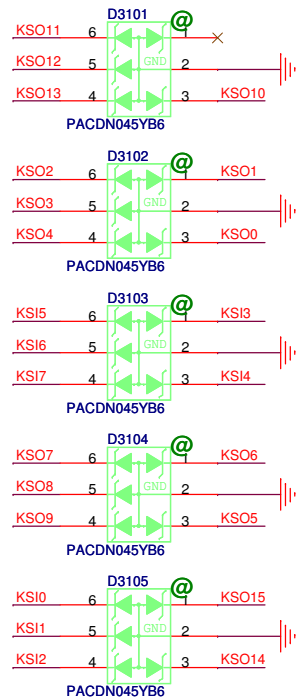
Share Memory
 Note: It can be programmable by EC firmware.

PP Enable
 Note: Default Int. Pull-Low

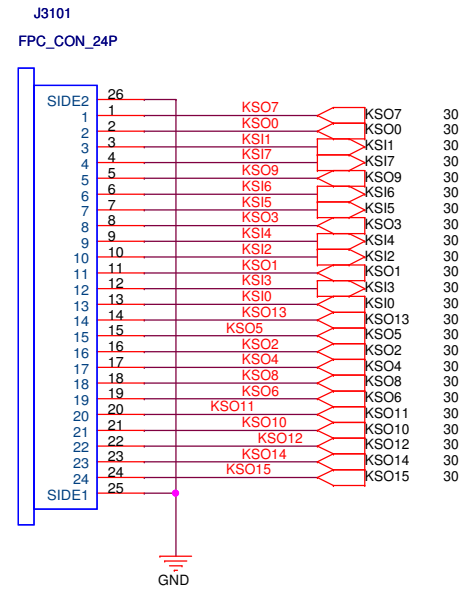
R3045: For Xtal measurement

AC_PRESENT
 PM_S4_STATE#
 S4_STATE_ON
 PM_SLP_M#
 SLP_M_ON
 EC_WLAN_PWR
 MP_PWRGD
 AC_PRESENT
 LAN_WOL_EN
 +3VM_PG
 +1.5VM_+3VMCLK_PG
 SUSPWR_ACK

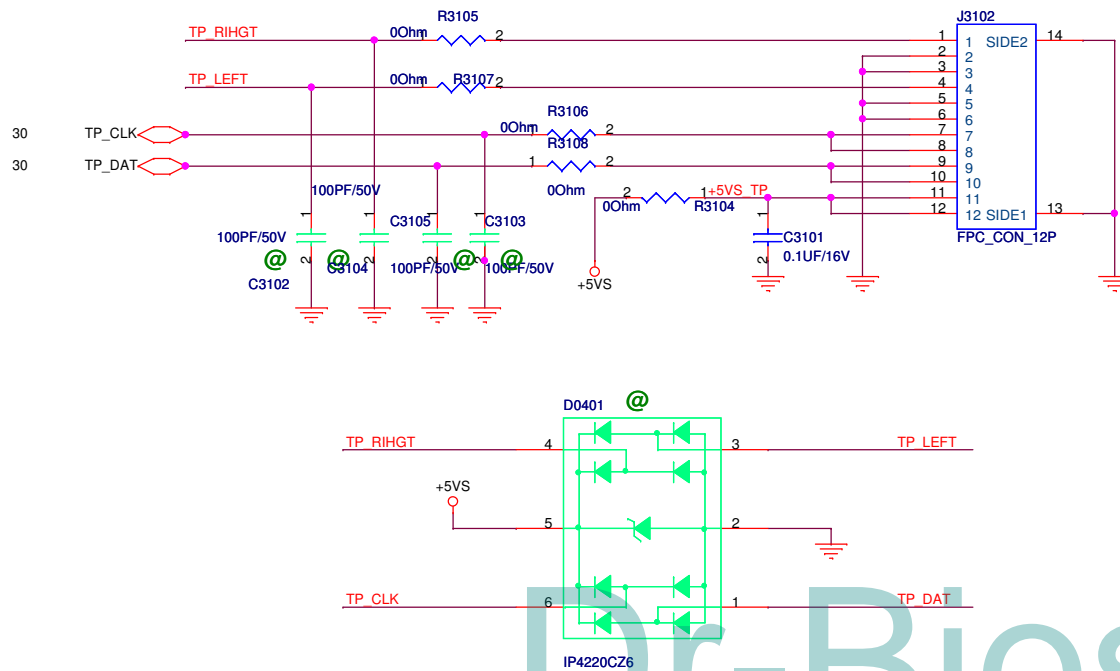




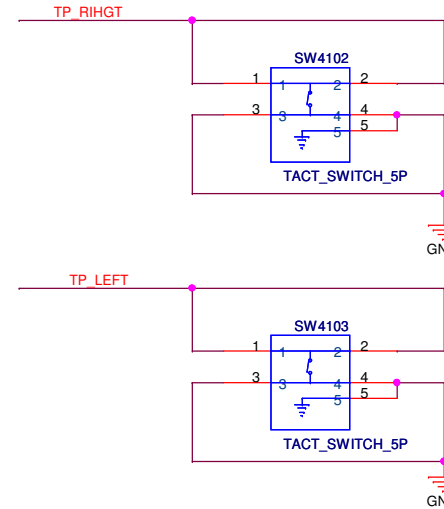
Keyboard



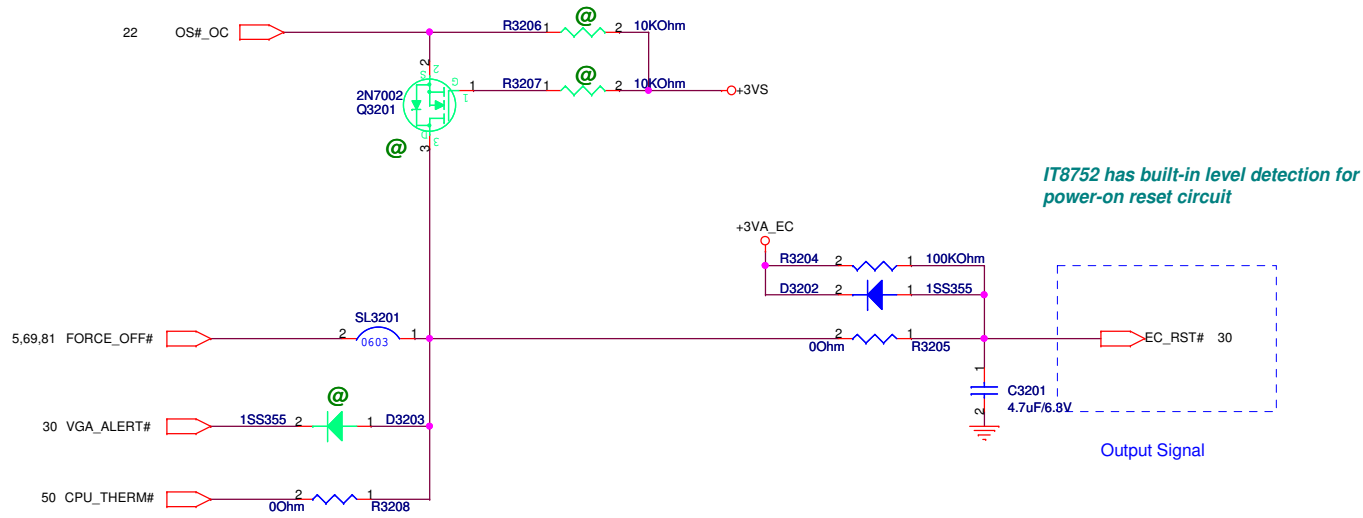
Touchpad



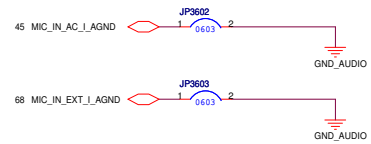
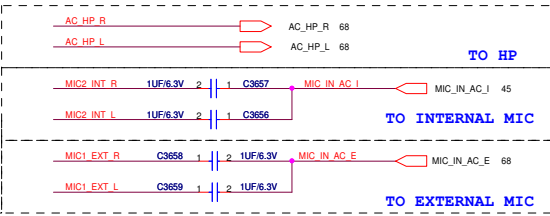
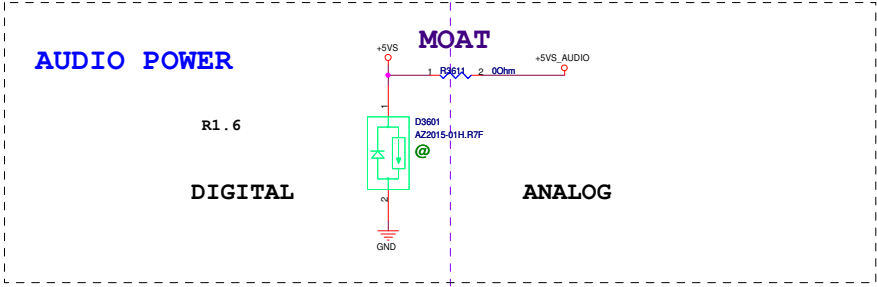
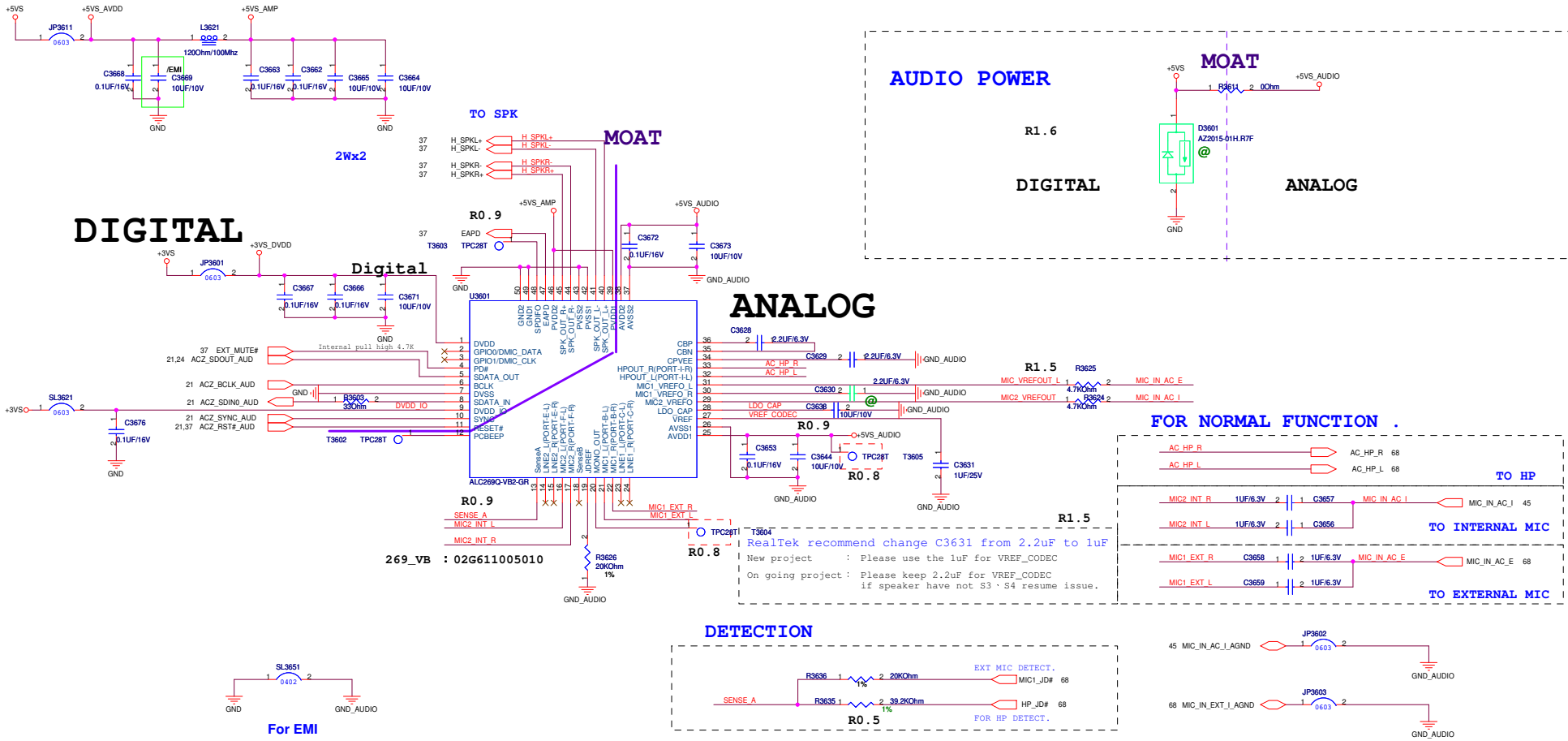
SW4102, SW4103 use PCB footprint of 12G091030050



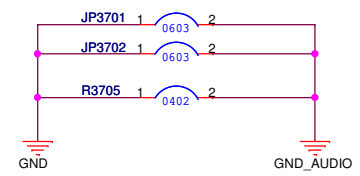
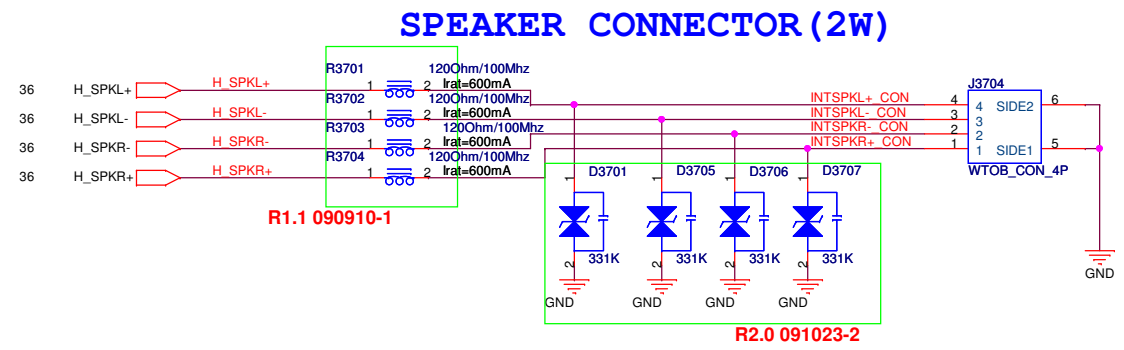
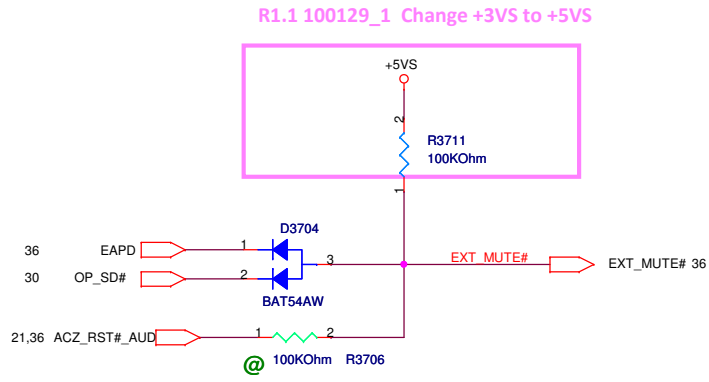
Dr-Bios.com



		Title : RST_Reset Circuit	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size B	Project Name K52N	Rev 1.0	
Date: Monday, February 08, 2010		Sheet	32 of 99



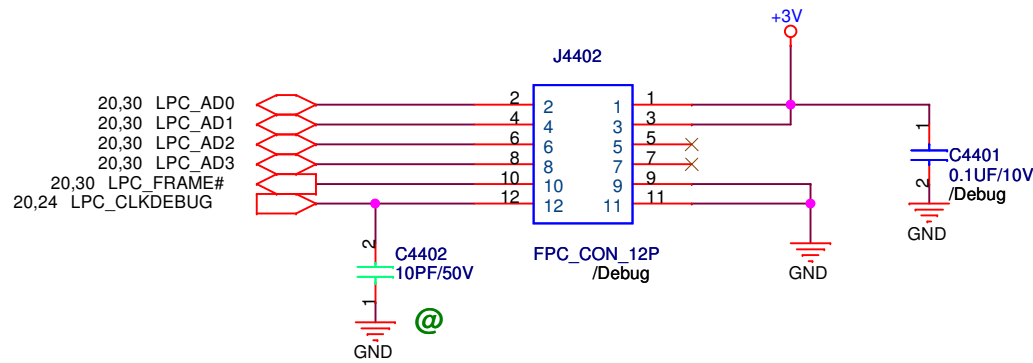
Dr-Bios.com



ASUS		Title : AUDIO AMP	
ASUSTeK COMPUTER INC. NB2		Engineer: Leon	
Size B	Project Name K52Jr	Rev 2.0	
Date: Monday, February 08, 2010		Sheet 37 of 99	

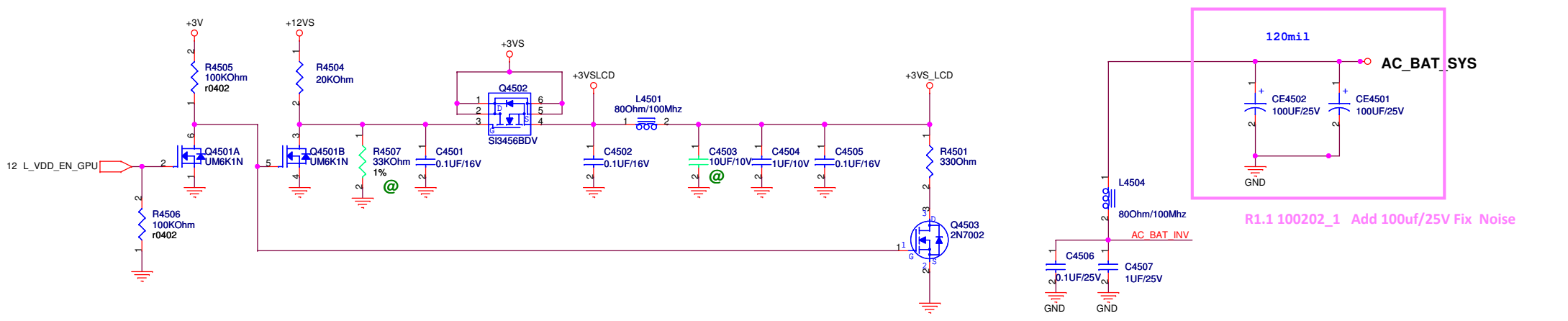
Dr-Bios.com

LPC Debug Port



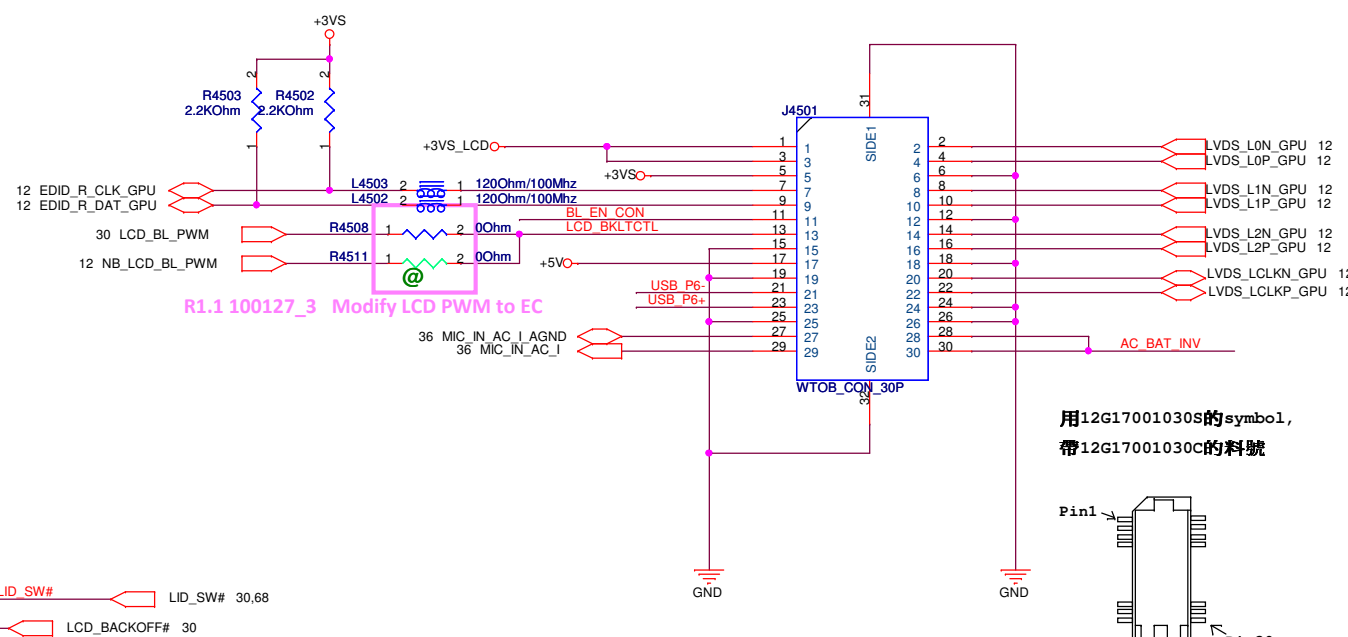
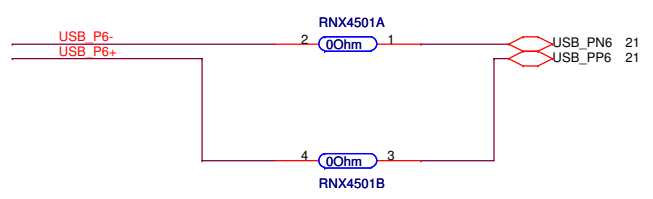
Dr-Bios.com

		Title : BUG_Debug	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size Custom	Project Name K52N		Rev 1.0
Date: Monday, February 08, 2010		Sheet 44 of 99	



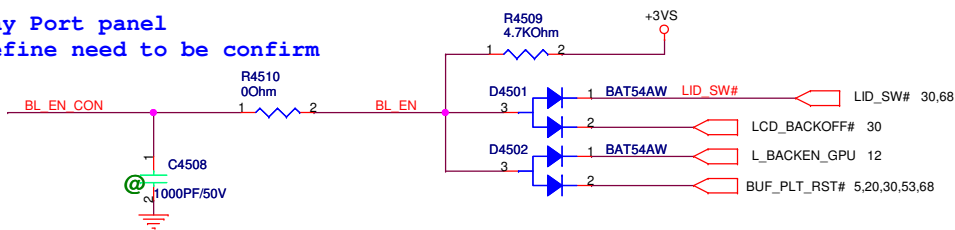
R1.1 100202_1 Add 100uf/25V Fix Noise

CAMERA & MIC

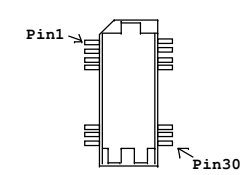


R1.1 100127_3 Modify LCD PWM to EC

Display Port panel pin define need to be confirm

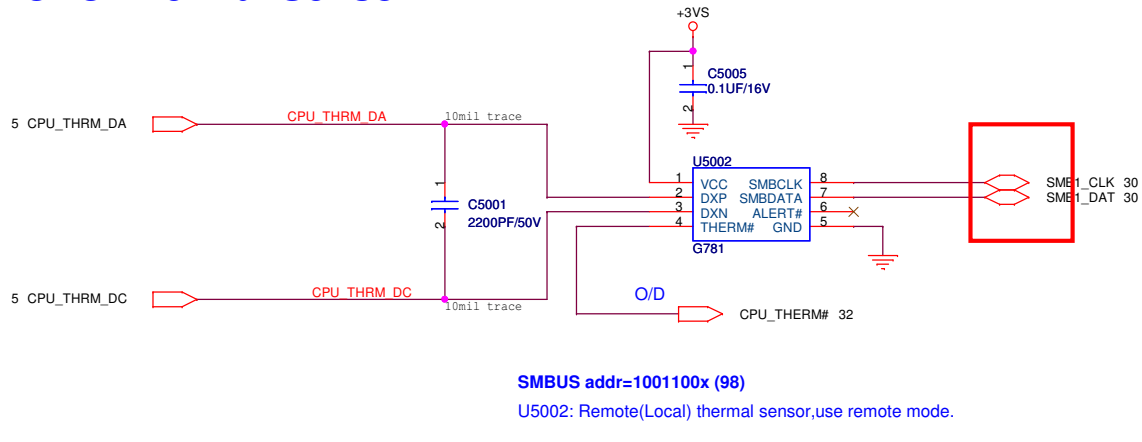


用12G17001030S的symbol, 帶12G17001030C的料號

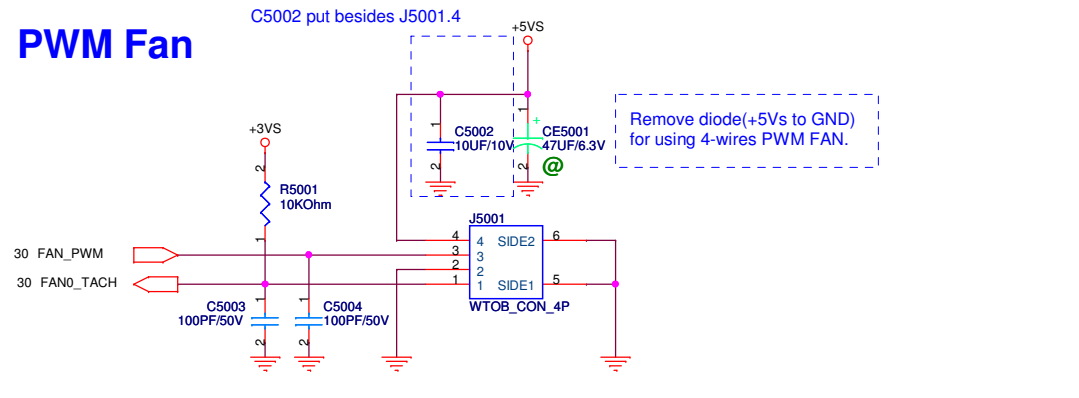


ASUS		Title : CRT_LCD Panel	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size	Project Name	Rev	
B	K52N	1.0	
Date: Monday, February 08, 2010	Sheet	45	of 99

CPU Thermal Sensor

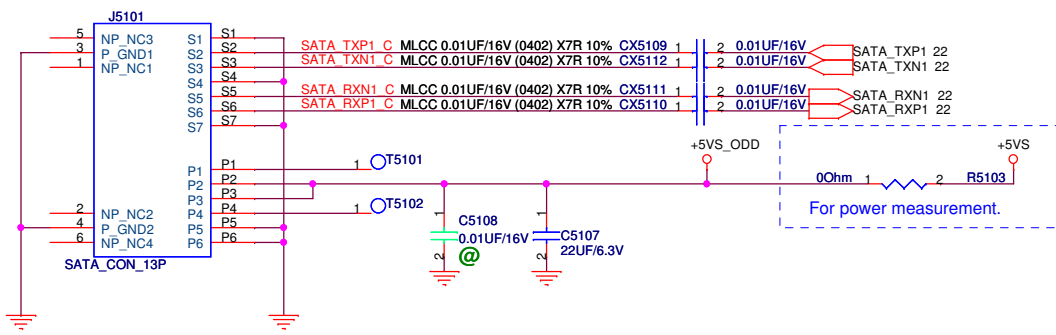


PWM Fan

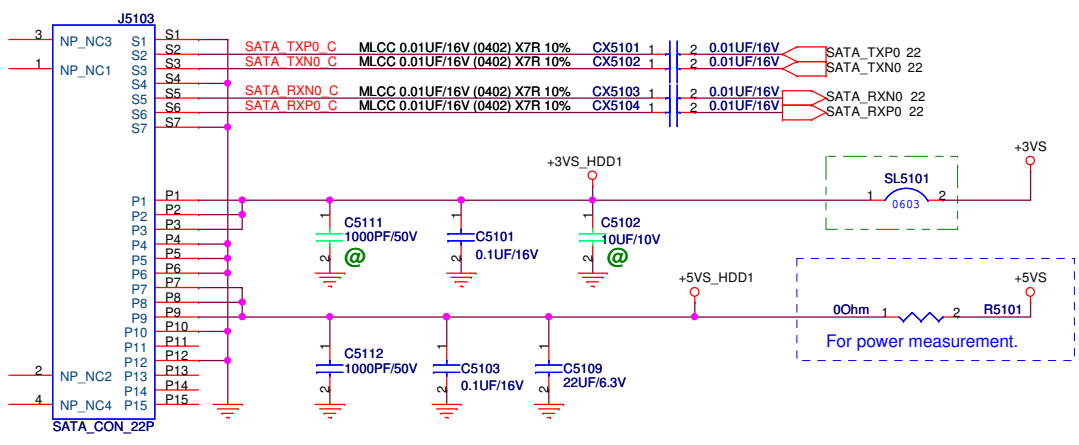


ASUS		Title : FAN_Fan & Sensor
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang
Size B	Project Name K52N	Rev 1.0
Date: Monday, February 08, 2010		Sheet 50 of 99

ODD

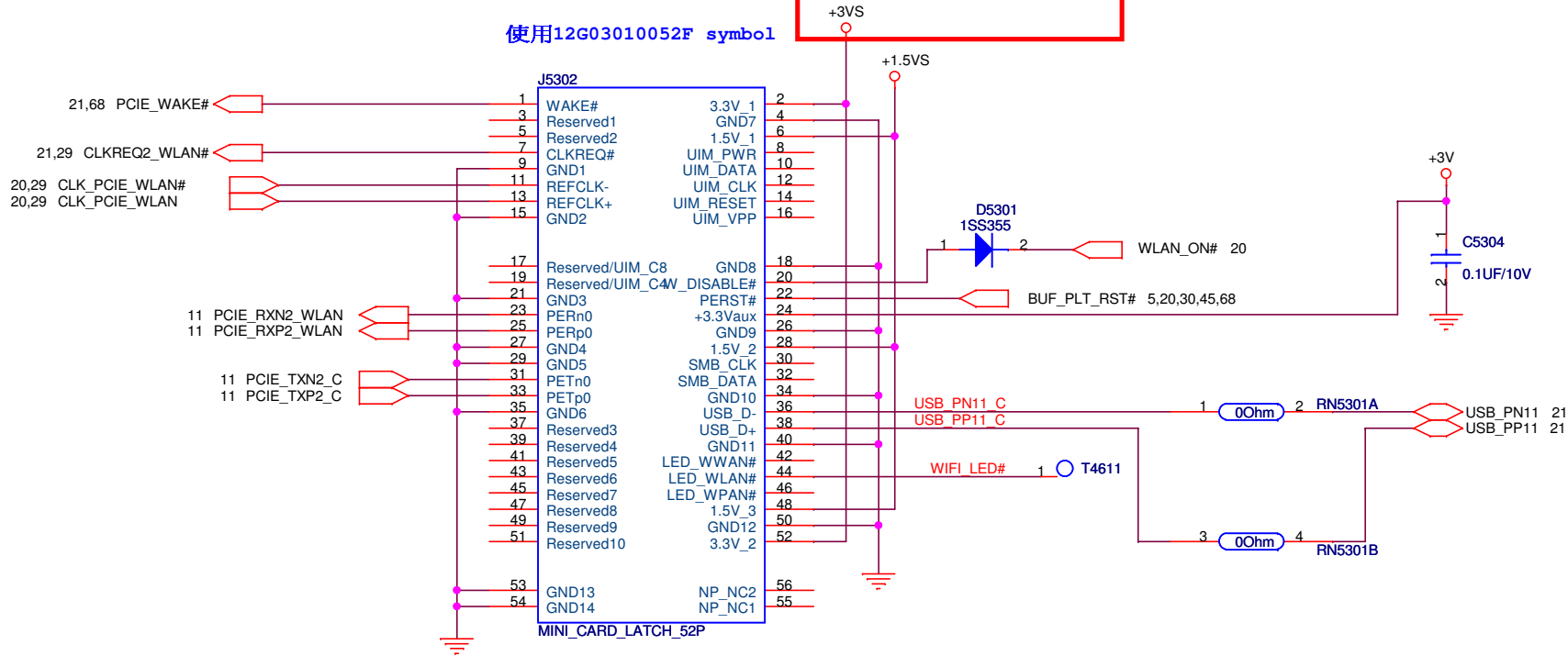


HDD (1st)



ASUS		Title : XDD_HDD & ODD	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size	Project Name	Rev	
B	K52N	1.0	
Date: Monday, February 08, 2010		Sheet 51 of 99	

Support wake from S3 only



WLAN

WLAN +3VAUX bypass capactor:
 Place 0.1uF near pin 2,24,52,39 41.
 Place 10uF near +3VAUX_WLAN source side.

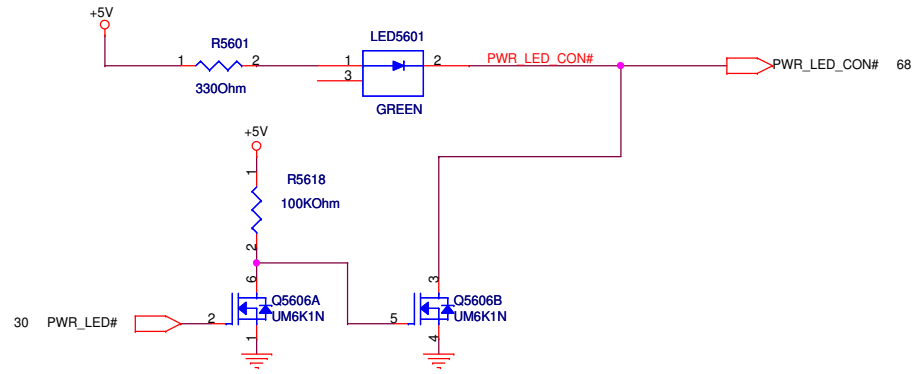
WLAN +1.5VS bypass capactor:
 Place 0.1uF near pin 6,28,48.
 Place 10uF near +1.5VS source side

WLAN nuts:
 Minicard spec R1.2:
 Full size card= 2pcs.
 Half size card= 2pcs.

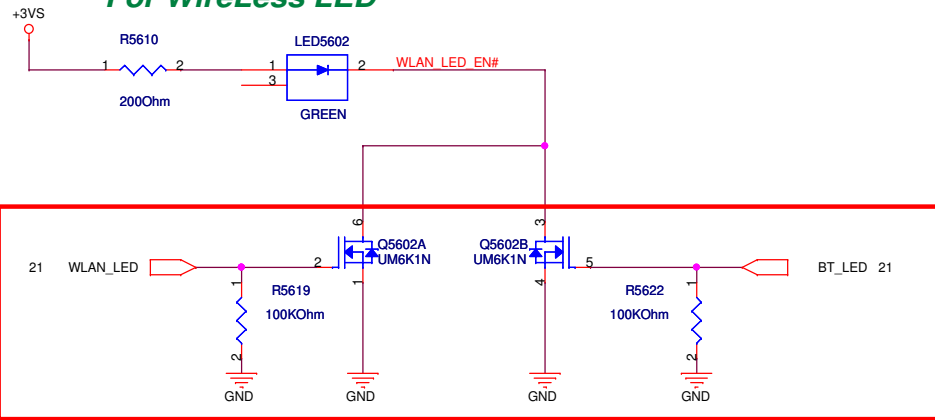
ASUS		Title :MINICARD(WLAN)	
ASUSTeK COMPUTER INC. NB6		Engineer: <u>Vincent_Chiang</u>	
Size Custom	Project Name K52N	Date: Monday, February 08, 2010	Rev 1.0
Date: Monday, February 08, 2010		Sheet 53	of 99

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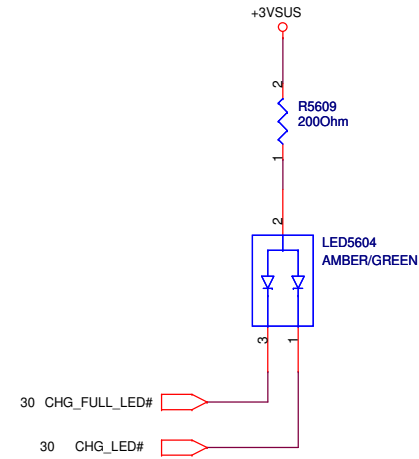
For POWER LED



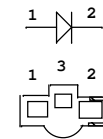
For WireLess LED



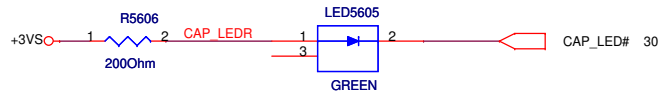
Charge LED



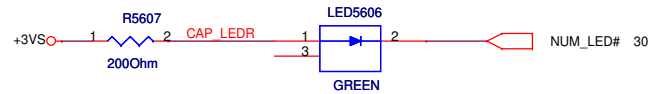
Side Light LED symbol



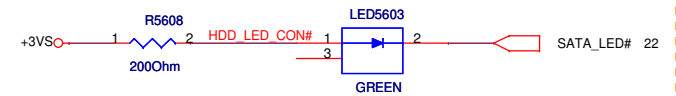
Cap. Lock LED



for Num Lock



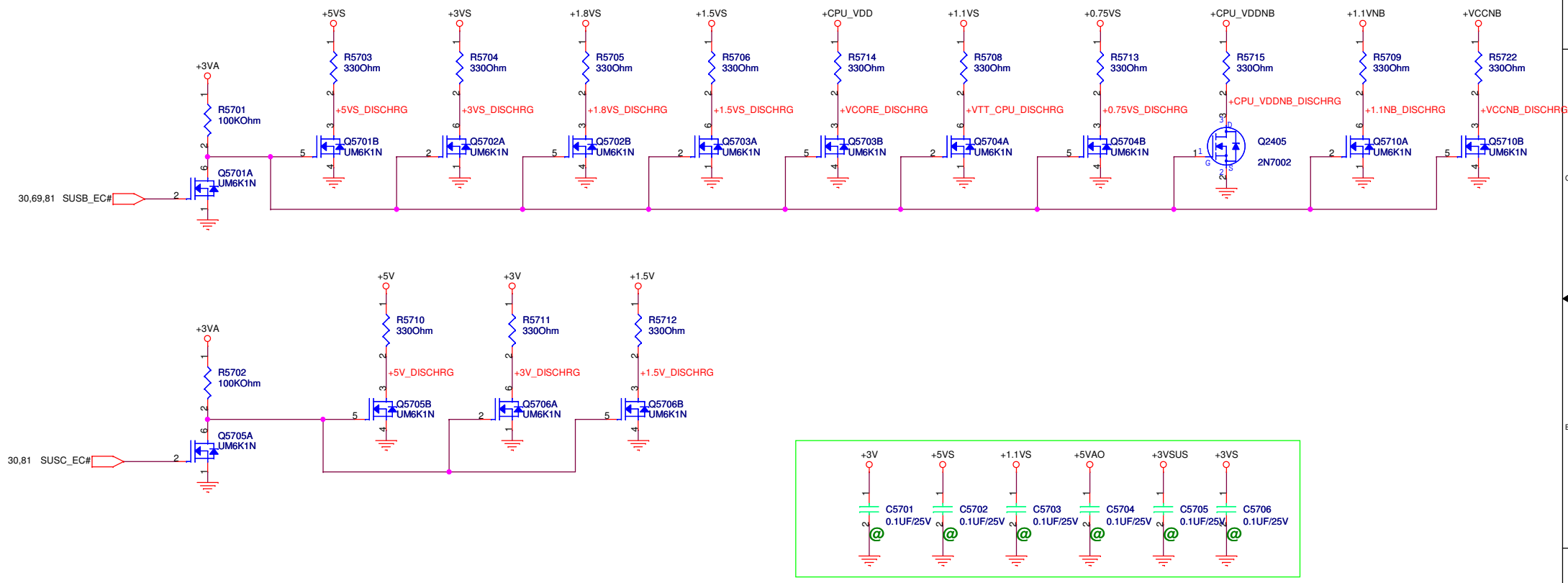
HDD LED



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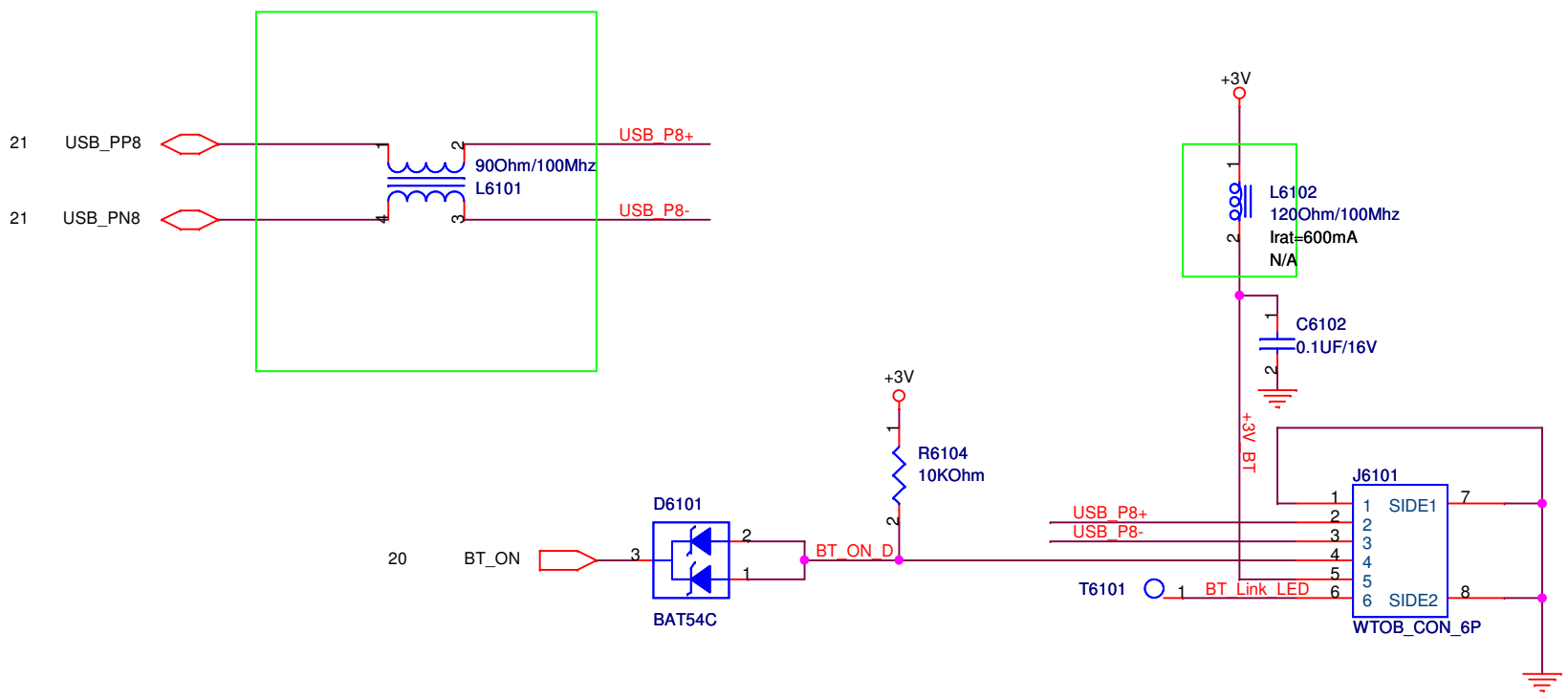
Main Board

Remove +2.5Vs is for ATI GFX



ASUS		Title : DSG_Discharge	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size B	Project Name K52N		Rev 1.0
Date: Monday, February 08, 2010		Sheet 57 of 99	

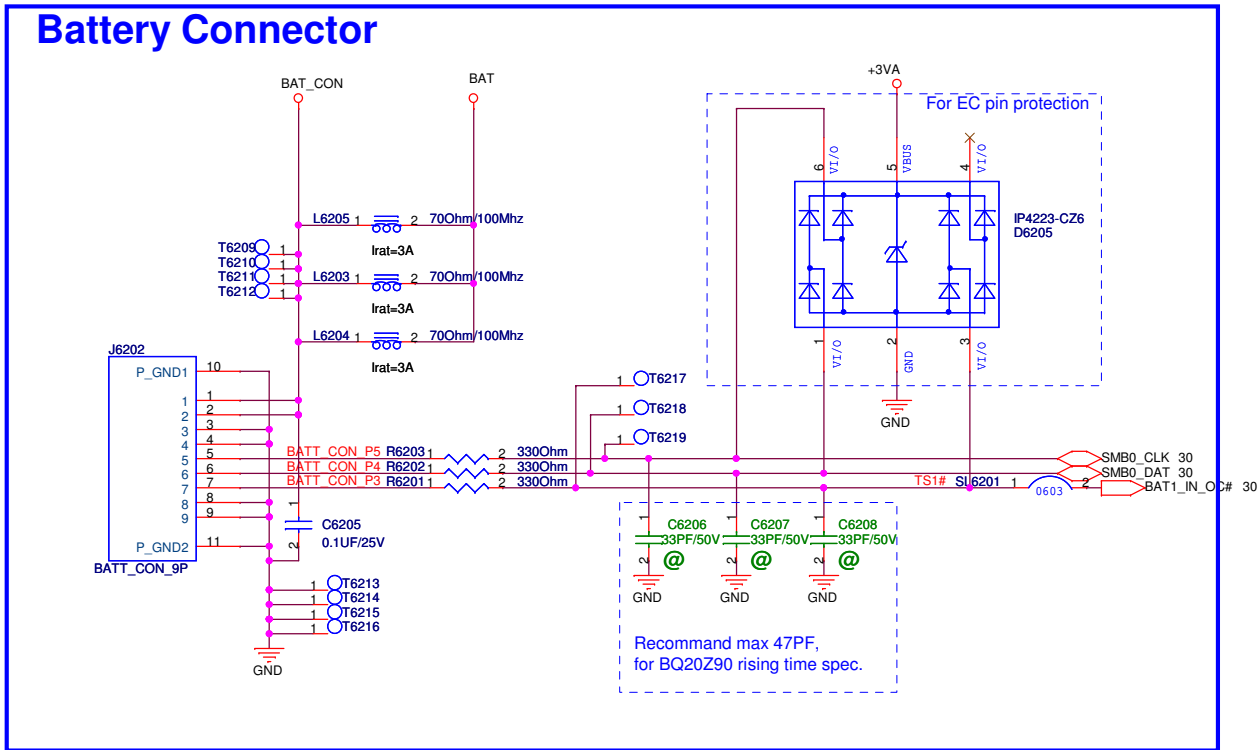
BLUETOOTH



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		Title : BT_Bluetooth	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size Custom	Project Name K52N	Rev 1.0	
Date: Monday, February 08, 2010		Sheet 61 of 99	

Battery Connector

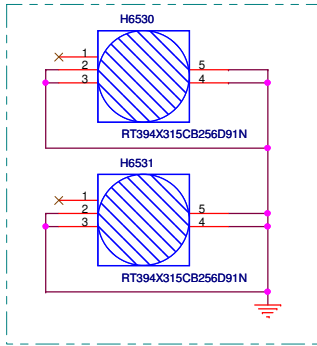


Total count: 11 pcs

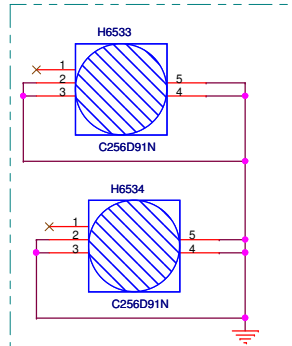
ASUS		Title : DC_DC & BAT Conn.	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size B	Project Name K52N	Rev 1.0	
Date: Monday, February 08, 2010		Sheet 62 of 99	

Main Board

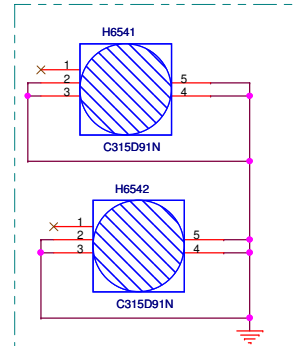
Screw Hole A



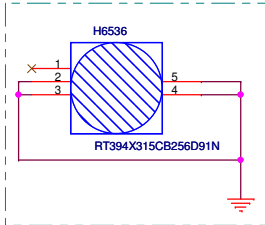
Screw Hole B



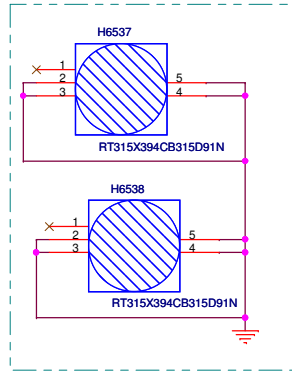
Screw Hole I



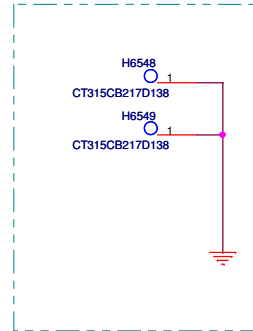
Screw Hole C



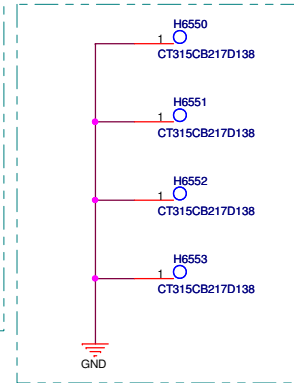
Screw Hole F



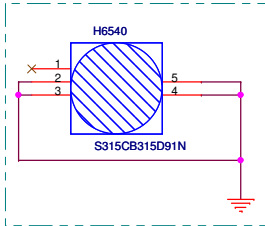
Screw Hole E



Screw from k52JR



Screw Hole H



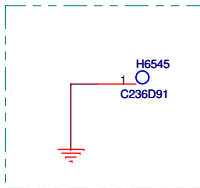
Tooling Hole K



Tooling Hole L

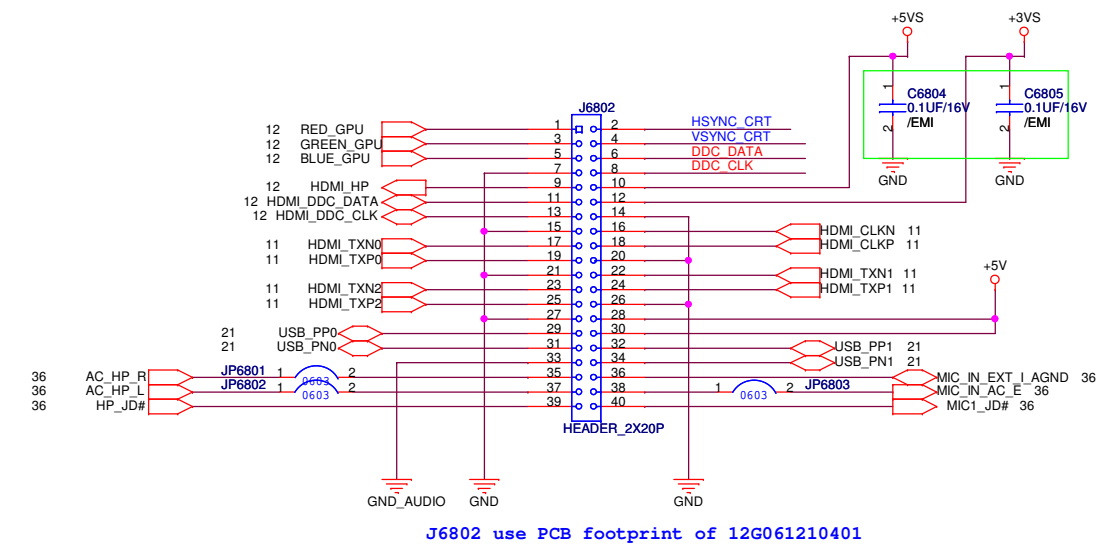
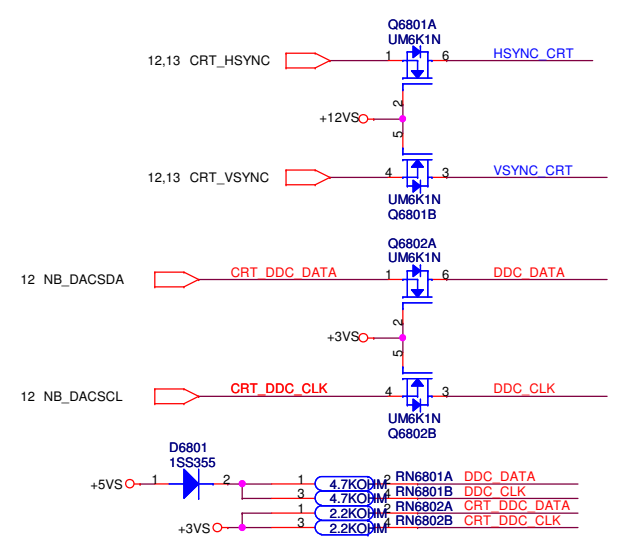
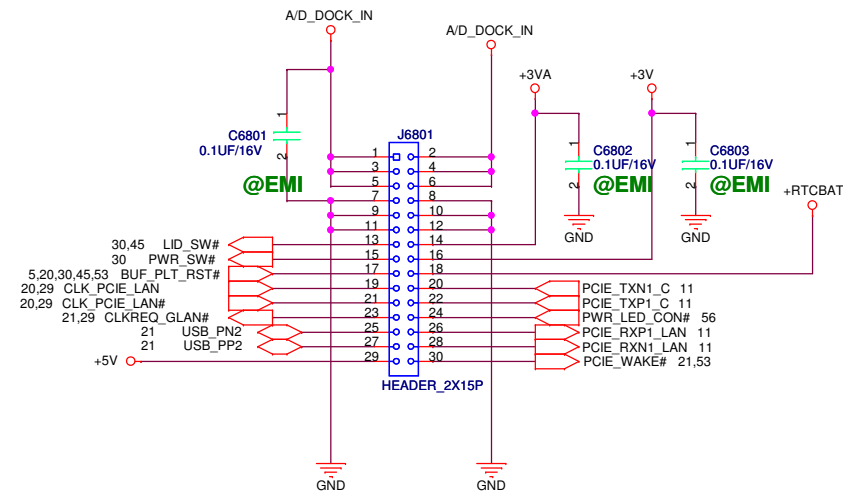


Screw Hole O



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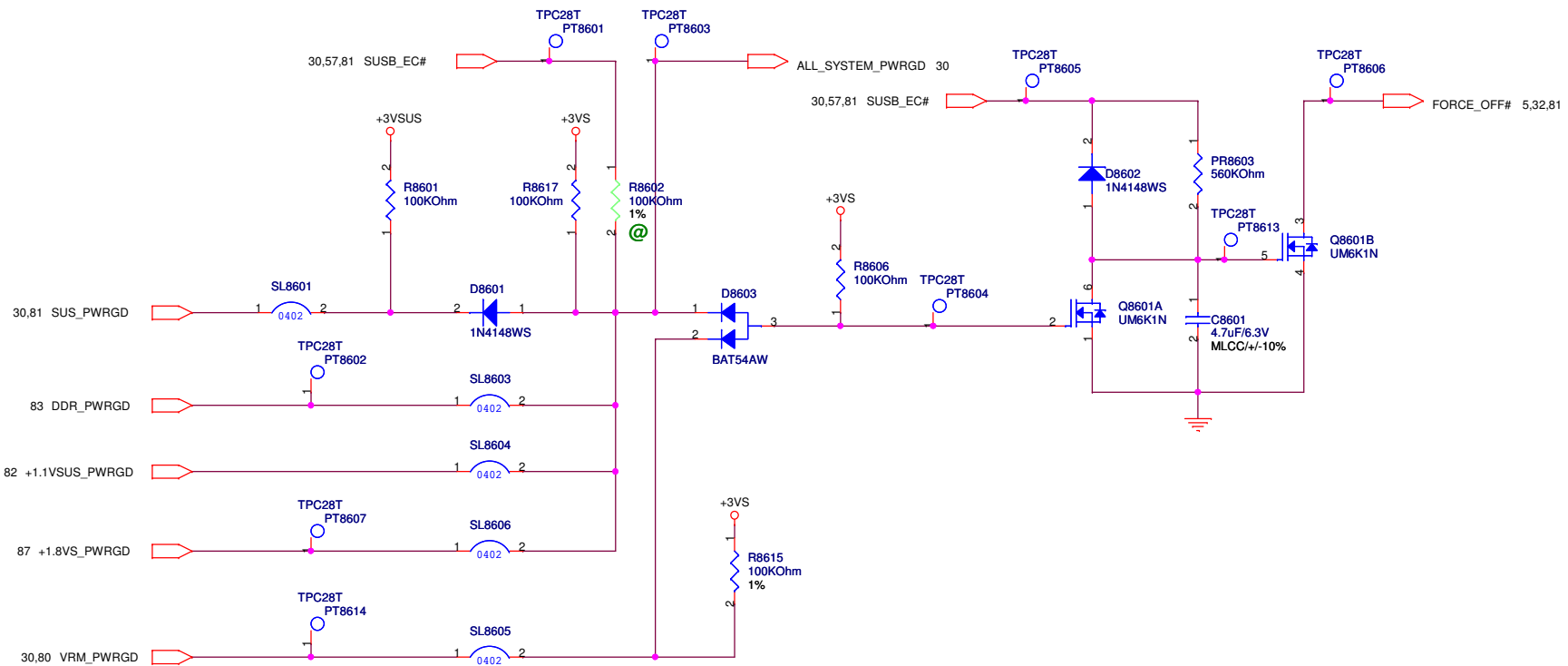
ASUS		Title : ME_Conn & Skew Hole	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size	Project Name		Rev
Custom	K52N		1.0
Date: Monday, February 08, 2010	Sheet	65	of 99



ASUS		Title :IO Connector	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>Vincent_Chiang</i>	
Size	Project Name	Rev	
B	K52N	1.0	
Date: Monday, February 08, 2010		Sheet	68 of 99

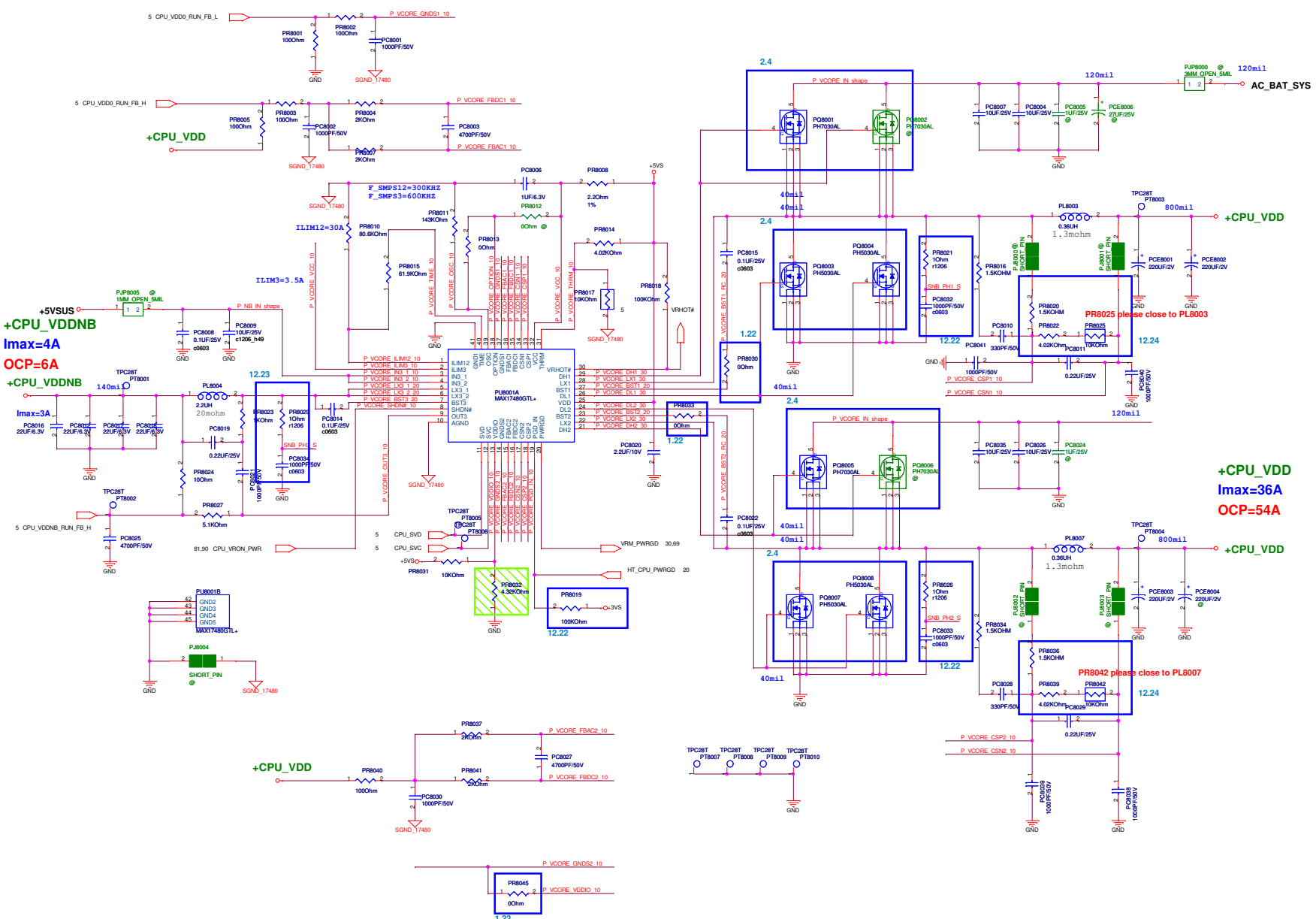
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POWER GOOD DETECTER



<Variant Name>

ASUS		Title : GOOD_DETECTER	
ASUSTeK COMPUTER INC		Engineer: <i>Vincent_Chiang</i>	
Size B	Project Name		Rev 1.0
Date: Monday, February 08, 2010		Sheet 69	of 95



+CPU_VDDNB
Imax=4A
OCP=6A

+CPU_VDD
Imax=36A
OCP=54A

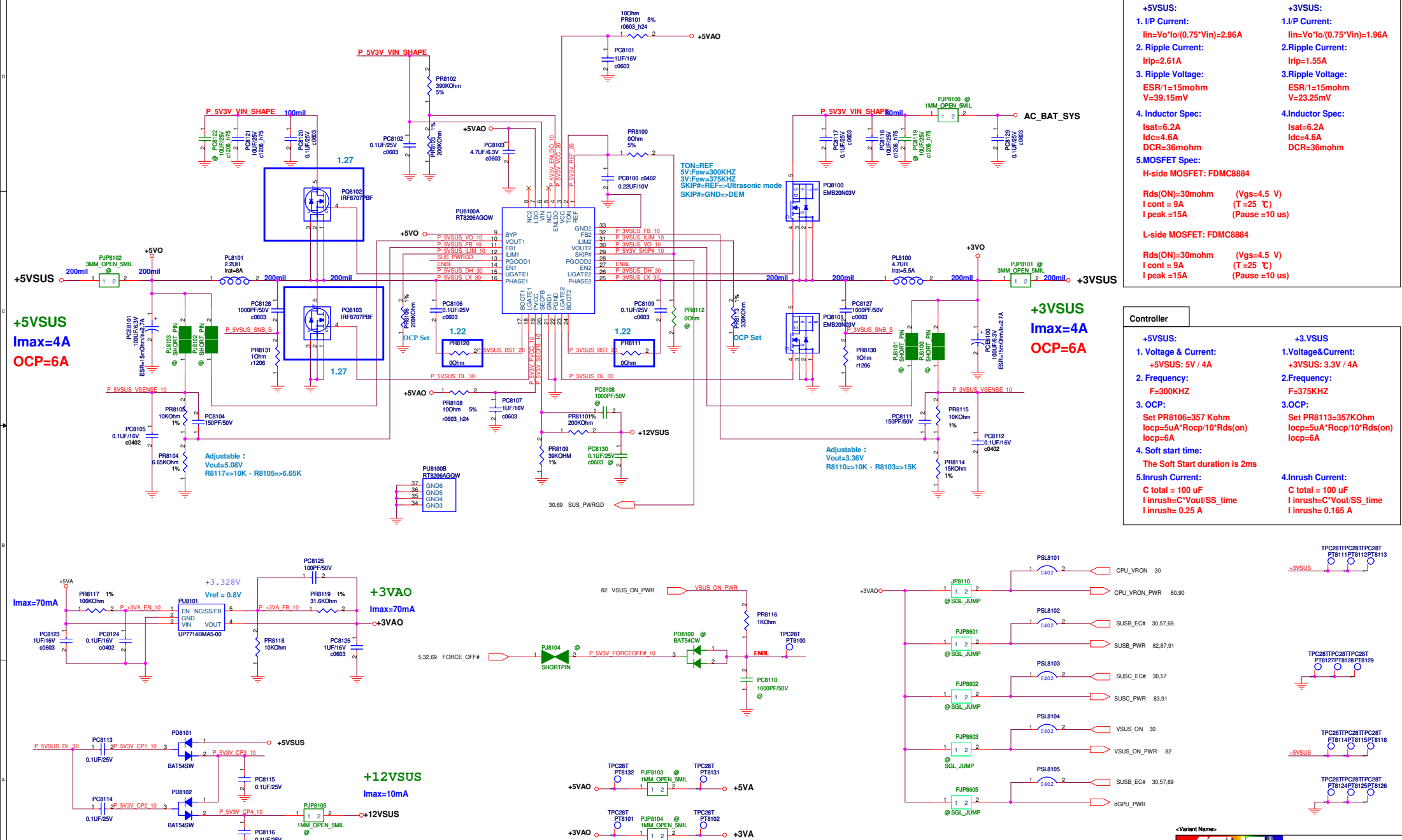
+CPU_VDD

+CPU_VDD

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ASUS		Title: +VCORE
ASUSTeK COMPUTER INC		Engineer: Siny
SGS	Project Name	Rev 1.0
Custom	K51AB	Date: Monday, February 08, 2010
Sheet 80 of 80		

+5VSUS / +3VSUS POWER SUPPLY

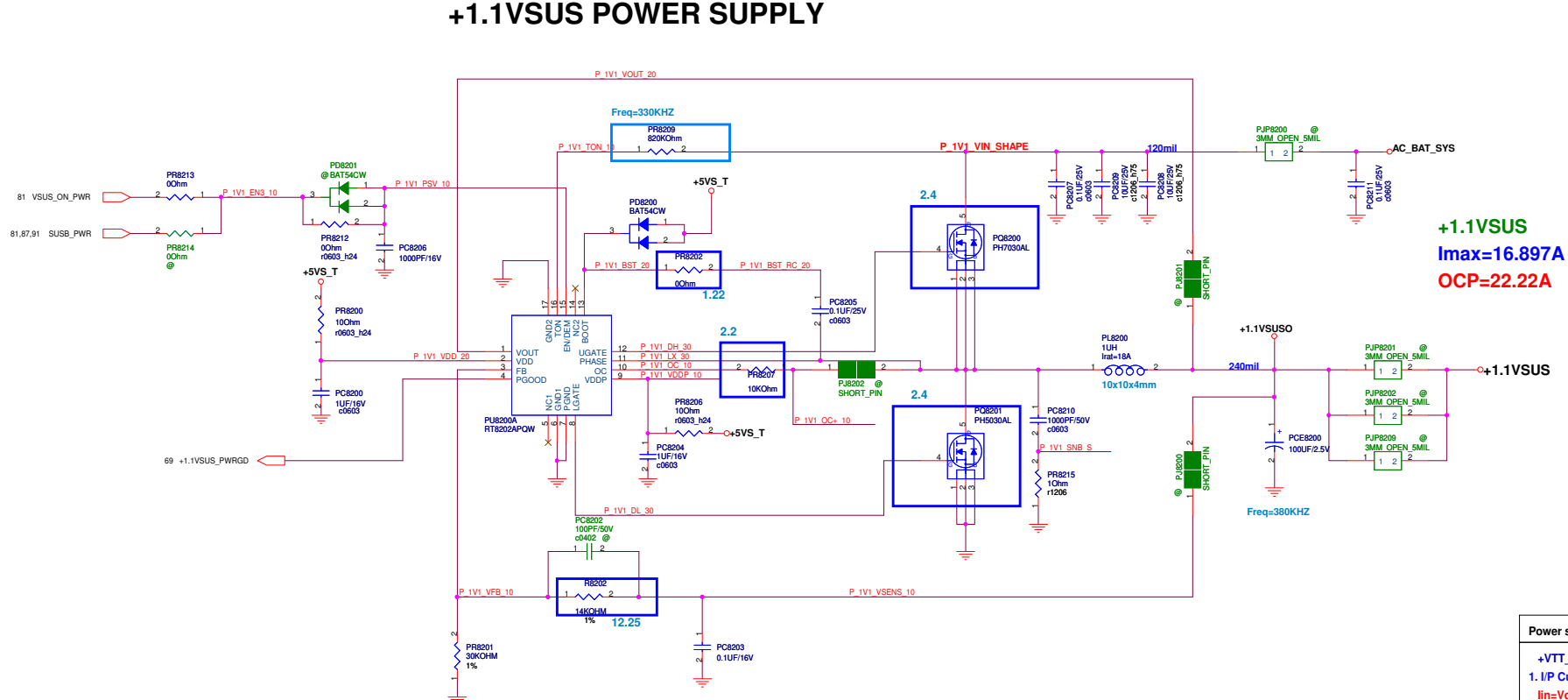


Power stage	
+5VSUS:	+3VSUS:
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.96A$	1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.96A$
2. Ripple Current: $I_{rip} = 2.61A$	2. Ripple Current: $I_{rip} = 1.55A$
3. Ripple Voltage: $ESR/1 = 15m\Omega$ $V = 39.15mV$	3. Ripple Voltage: $ESR/1 = 15m\Omega$ $V = 23.25mV$
4. Inductor Spec: $I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36m\Omega$	4. Inductor Spec: $I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36m\Omega$
5. MOSFET Spec: H-side MOSFET: FDMC8884	
$R_{ds(on)} = 30m\Omega$ ($V_{gs} = 4.5V$)	$V_{gs} = 4.5V$
$I_{cont} = 9A$	$T = 25^\circ C$
$I_{peak} = 15A$	(Pause = 10 us)
L-side MOSFET: FDMC8884	
$R_{ds(on)} = 30m\Omega$ ($V_{gs} = 4.5V$)	$V_{gs} = 4.5V$
$I_{cont} = 9A$	$T = 25^\circ C$
$I_{peak} = 15A$	(Pause = 10 us)

Controller	
+5VSUS:	+3VSUS:
1. Voltage & Current: +5VSUS: 5V / 4A	1. Voltage & Current: +3VSUS: 3.3V / 4A
2. Frequency: F = 300KHZ	2. Frequency: F = 375KHZ
3. OCP: Set PR8106 = 357 Kohm $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$ $I_{ocp} = 6A$	3. OCP: Set PR8113 = 357 Kohm $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$ $I_{ocp} = 6A$
4. Soft start time: The Soft Start duration is 2ms	4. Inrush Current: $C_{total} = 100 uF$ $I_{inrush} = C \cdot V_{out} / SS_time$ $I_{inrush} = 0.25 A$
5. Inrush Current: $C_{total} = 100 uF$ $I_{inrush} = C \cdot V_{out} / SS_time$ $I_{inrush} = 0.165 A$	

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+1.1VSUS POWER SUPPLY



PT8200	TPC28T
+1.1VSUS0	1
PT8201	TPC28T
+1.1VSUS0	1
PT8202	TPC28T
+1.1VSUS	1
PT8203	TPC28T
+1.1VSUS	1
PT8204	TPC28T
GND	1
PT8205	TPC28T
GND	1

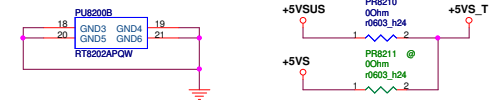
+1.1VSUS

I_{max}=16.897A

OCP=22.22A

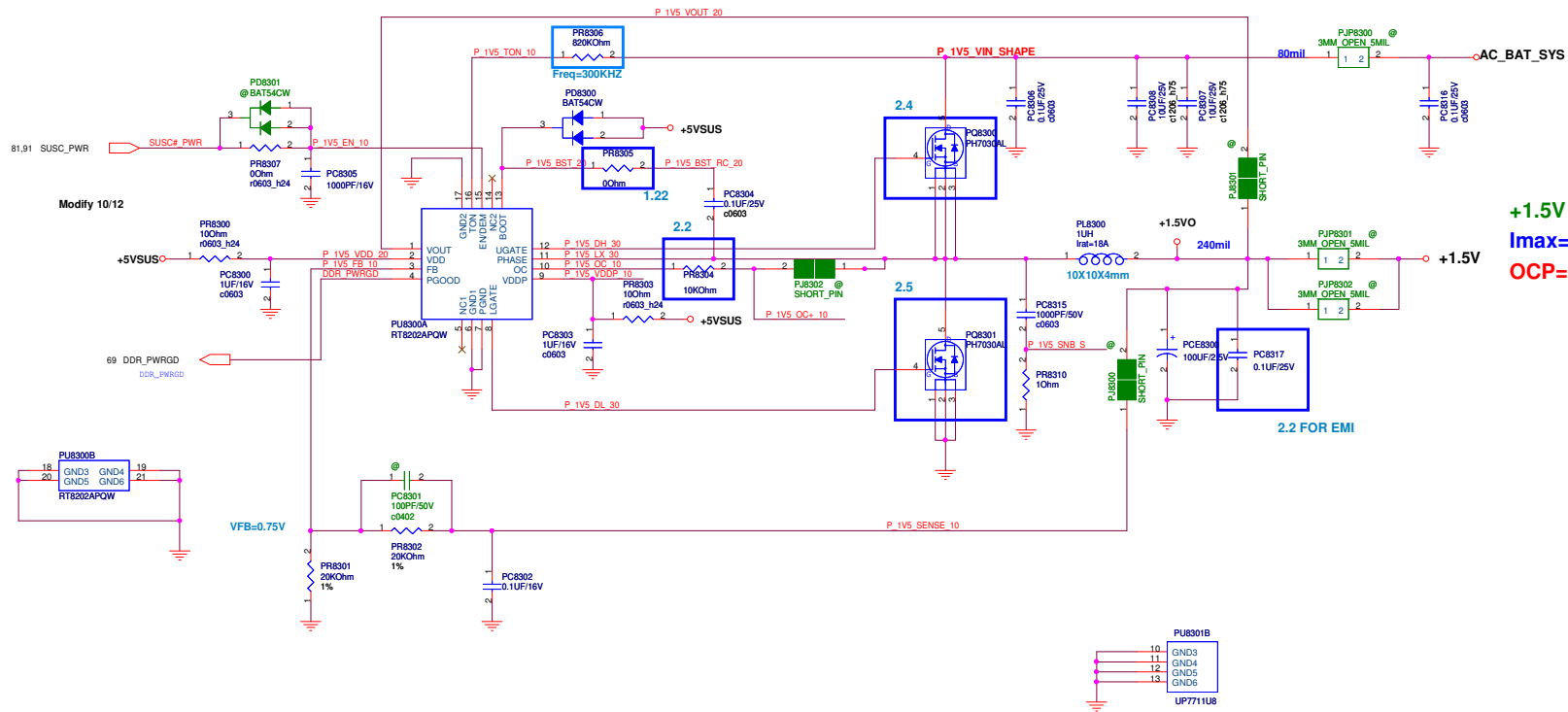
Controller	
+VTT_CPU:	
1. Voltage & Current:	
+VTT_CPU: 1.05V / 15A	
2. Frequency:	
F=330KHZ	
3. OCP:	
Set PR8207=4.99 Kohm	
I _{ocp} =R _{ocp} *20uA/R _{ds(on)}	
I _{ocp} =26A	
4. Soft start time:	
The SS duration is 1.35ms	
5. Inrush Current:	
C total = 440 uF	
I _{inrush} =C*V _{out} /SS_time	
I _{inrush} = 0.342 A	

Power stage	
+VTT_CPU:	
1. I/P Current:	
I _{in} =V _o *I _o /(0.75*V _{in})=2.33A	
2. Ripple Current:	
I _{rip} =5.36A	
3. Ripple Voltage:	
ESR/2=7.5mohm	
V _{ripple} =40.26mV	
4. Inductor Spec:	
I _{sat} =40A	
I _{dc} =25A	
DCR=1.6mohm	
5. MOSFET Spec:	
H-side MOSFET: RJK0355DPA	
R _{ds(ON)} =16.5mohm	(V _{gs} =4.5 V)
I _{cont} = 30A	(T=25 °C)
I _{peak} = 120 A	(Pause =10 us)
L-side MOSFET: RJK0353DPA	
R _{ds(ON)} =7.6mohm	(V _{gs} =4.5 V)
I _{cont} = 35A	(T=25 °C)
I _{peak} = 140 A	(Pause =10 us)



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+1.5V & +0.75VS POWER SUPPLY



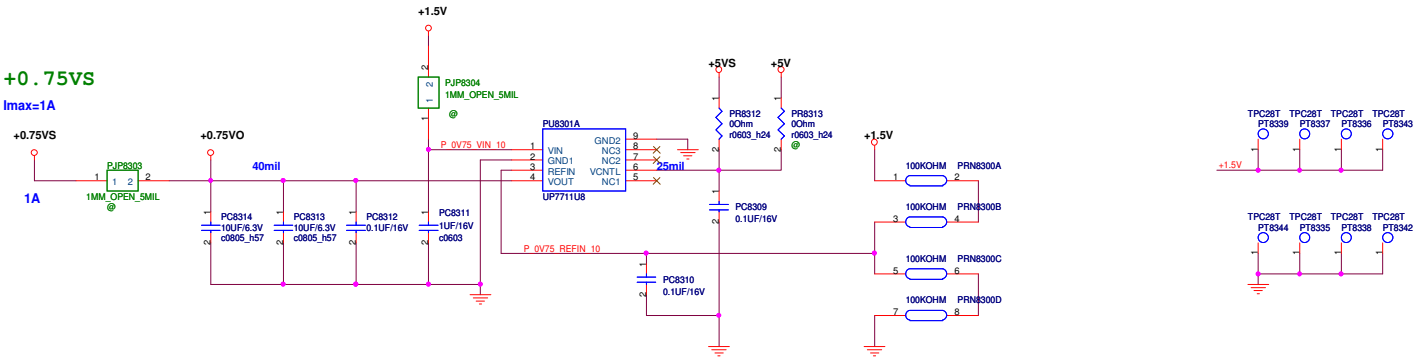
Power stage

- DDR III:
- I/P Current:
 $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 2.22A$
 - Ripple Current:
 $I_{rip} = 4.62A$
 - Ripple Voltage:
 $ESR / I = 15m\Omega$
 $V = 69.3mV$
 - Inductor Spec:
 $I_{sat} = 12.7A$
 $I_{dc} = 9.5A$
 $DCR = 8.5m\Omega$
 - MOSFET Spec:
H-side MOSFET: RJK0355DPA
 $R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)
L-side MOSFET: RJK0355DPA
 $R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

+1.5V
I_{max} = 10.5A
OCP = 15.38A

Controller

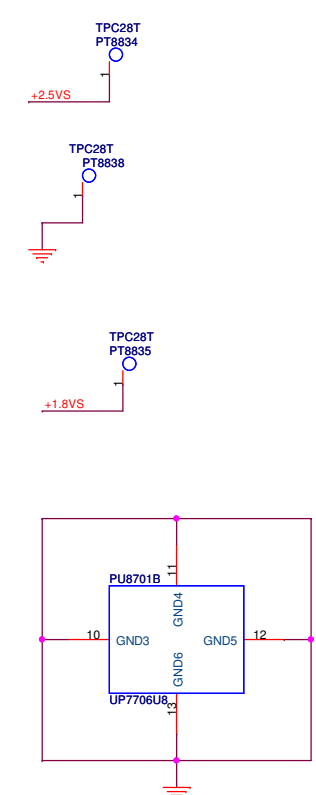
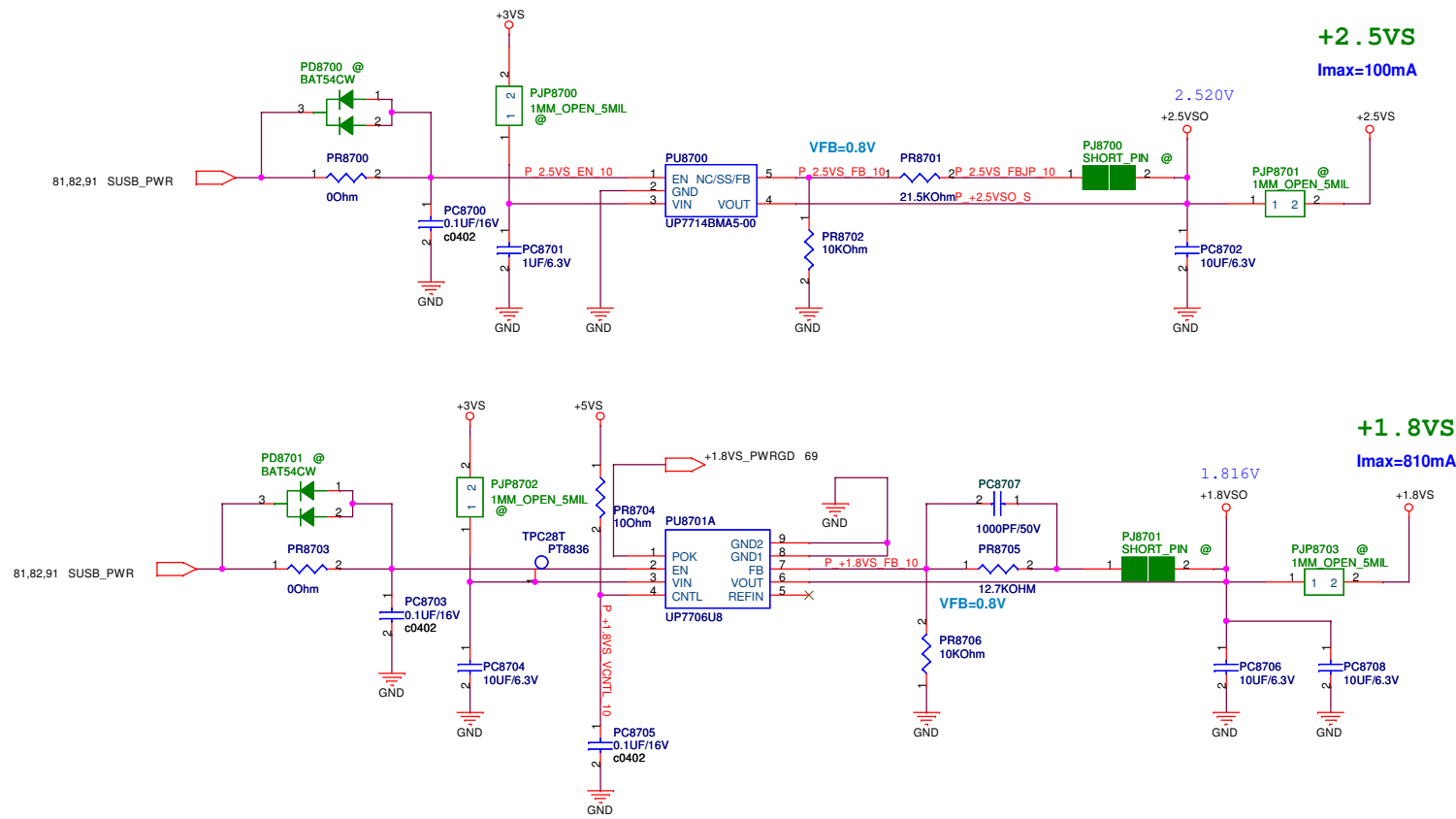
- DDR III:
- Voltage & Current:
+1.5V: 1.5V / 10A
 - Frequency:
F = 300KHZ
 - OCP:
Set R8302 = 12 Kohm
 $I_{ocp} = R_{ocp} \cdot 20\mu A / R_{ds(on)}$
 $I_{ocp} = 14.3A$
 - Soft start time:
The Soft Start duration is 1.35ms
 - Inrush Current:
 $C_{total} = 220\mu F$
 $I_{inrush} = C \cdot V_{out} / SS_{time}$
 $I_{inrush} = 0.244A$
1. Voltage & Current:
+0.75V: 0.75V / 1A



<Variant Names>

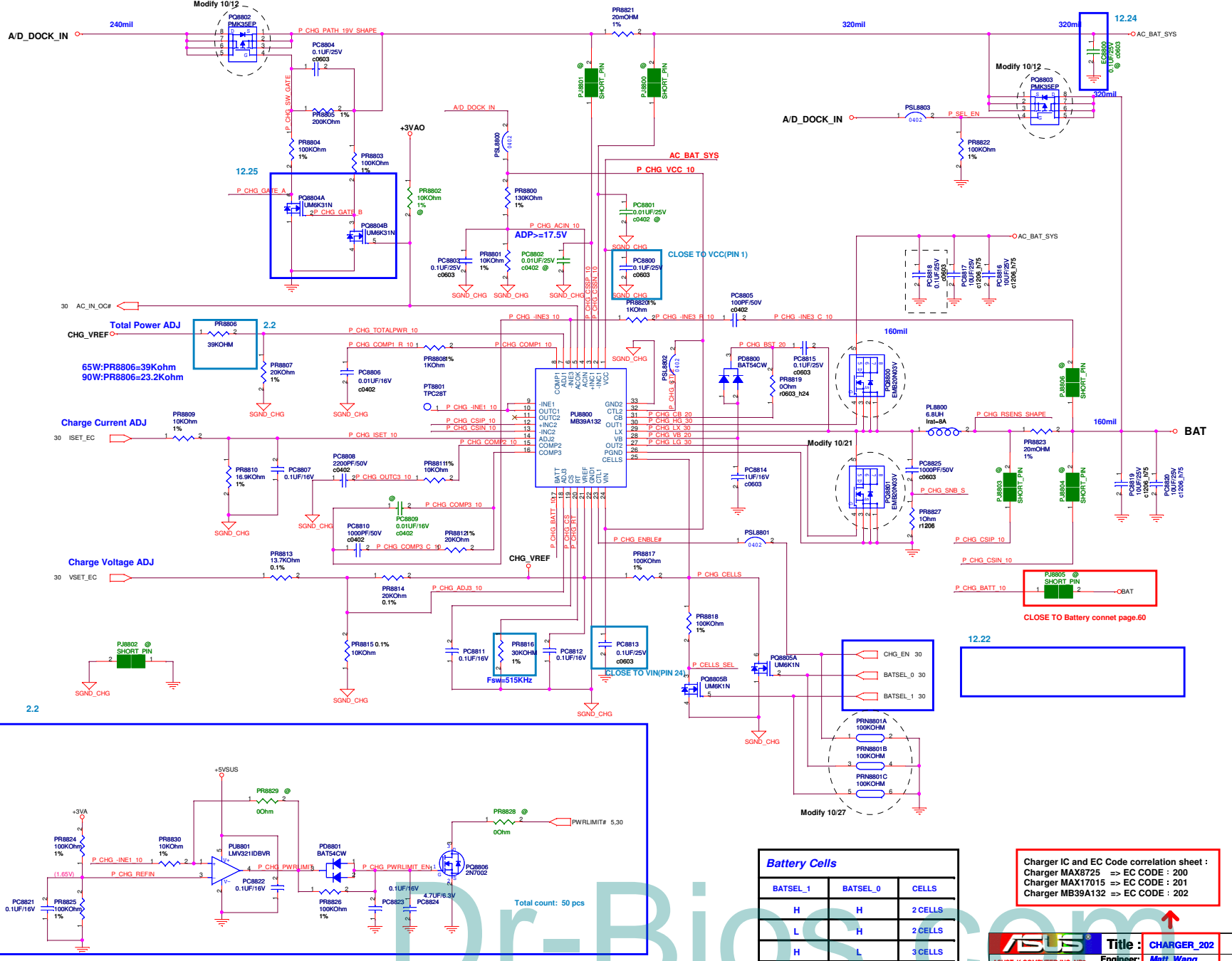
ASUS		Title : POWER_I/O_DDR	
ASUSTeK COMPUTER INC. NB		Engineer: Matt_Wang	
Size	Project Name	Rev	
Custom	Design IP	1.0	
Date: Monday, February 08, 2010	Sheet	63	of 95

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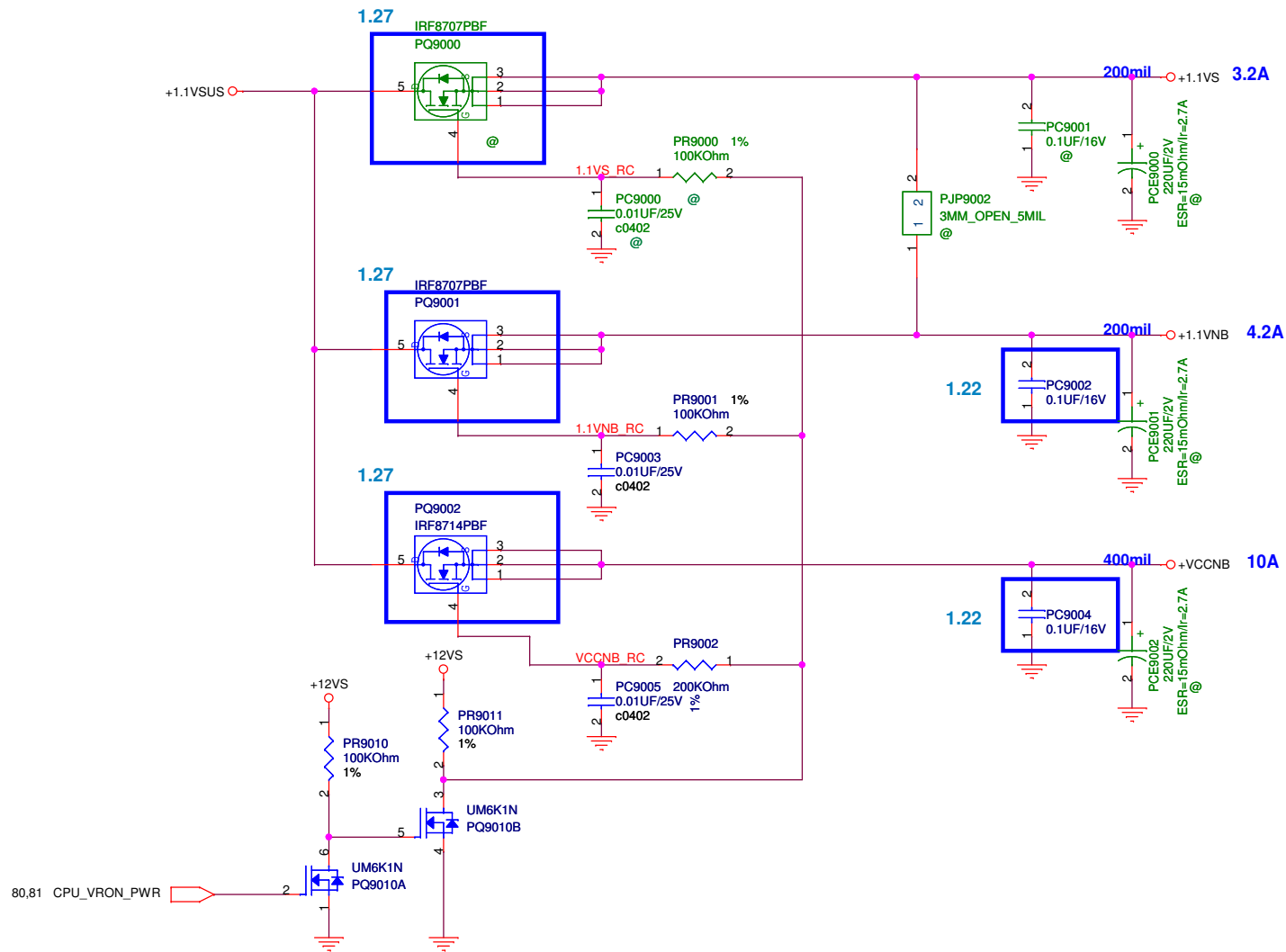
PT8805 TPC28T AC_BAT_SYS 1	PT8811 TPC28T A/D_DOCK_IN 1	PT8817 TPC28T BAT 1	PT8820 TPC28T BATSEL_0 1	PT8823 TPC28T AC_IN_OCF 1	PT8826 TPC28T PWRLIMIT# 1	PT8828 TPC28T GND 1
PT8806 TPC28T AC_BAT_SYS 1	PT8812 TPC28T A/D_DOCK_IN 1	PT8818 TPC28T BAT 1	PT8821 TPC28T BATSEL_1 1	PT8824 TPC28T ISET_EC 1	PT8827 TPC28T GND 1	PT8829 TPC28T GND 1
PT8804 TPC28T AC_BAT_SYS 1	PT8807 TPC28T A/D_DOCK_IN 1	PT8810 TPC28T A/D_DOCK_IN 1	PT8813 TPC28T A/D_DOCK_IN 1	PT8816 TPC28T BAT 1	PT8819 TPC28T BAT 1	PT8822 TPC28T CHG_EN 1
						PT8825 TPC28T VSET_EC 1
						PT8831 TPC28T GND 1
						PT8830 TPC28T GND 1



Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

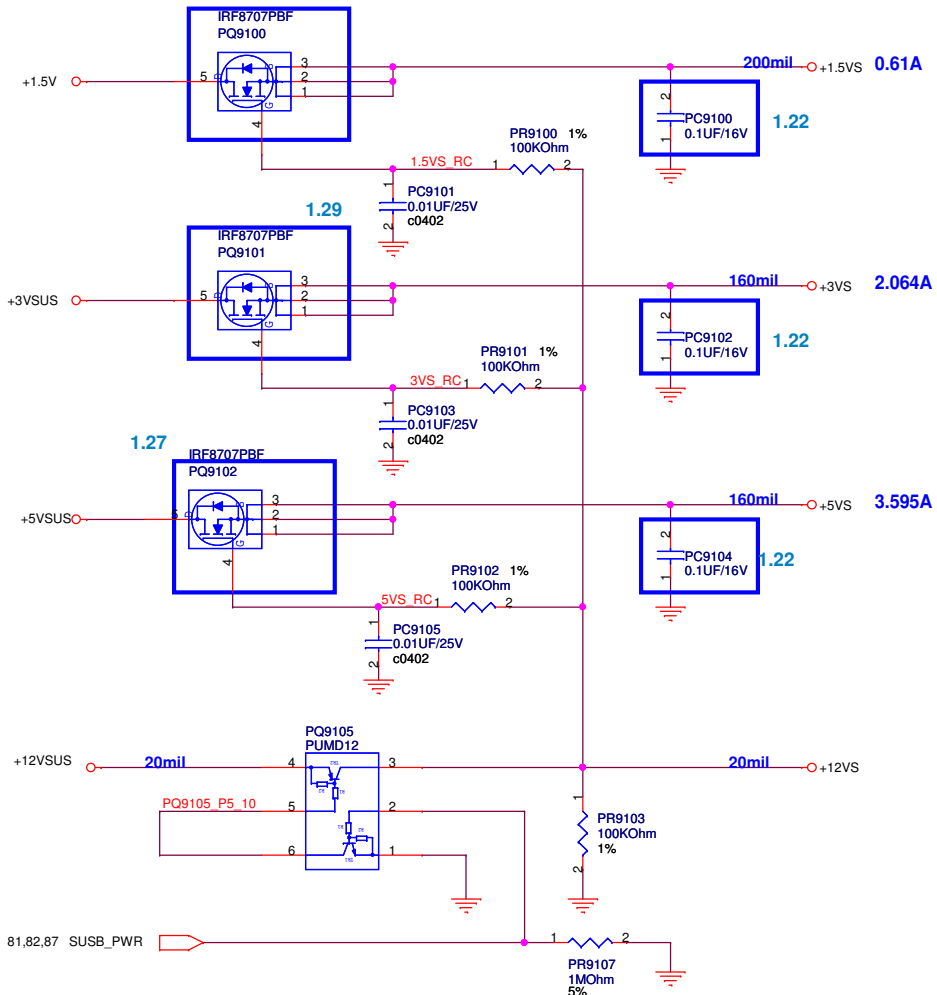
Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202



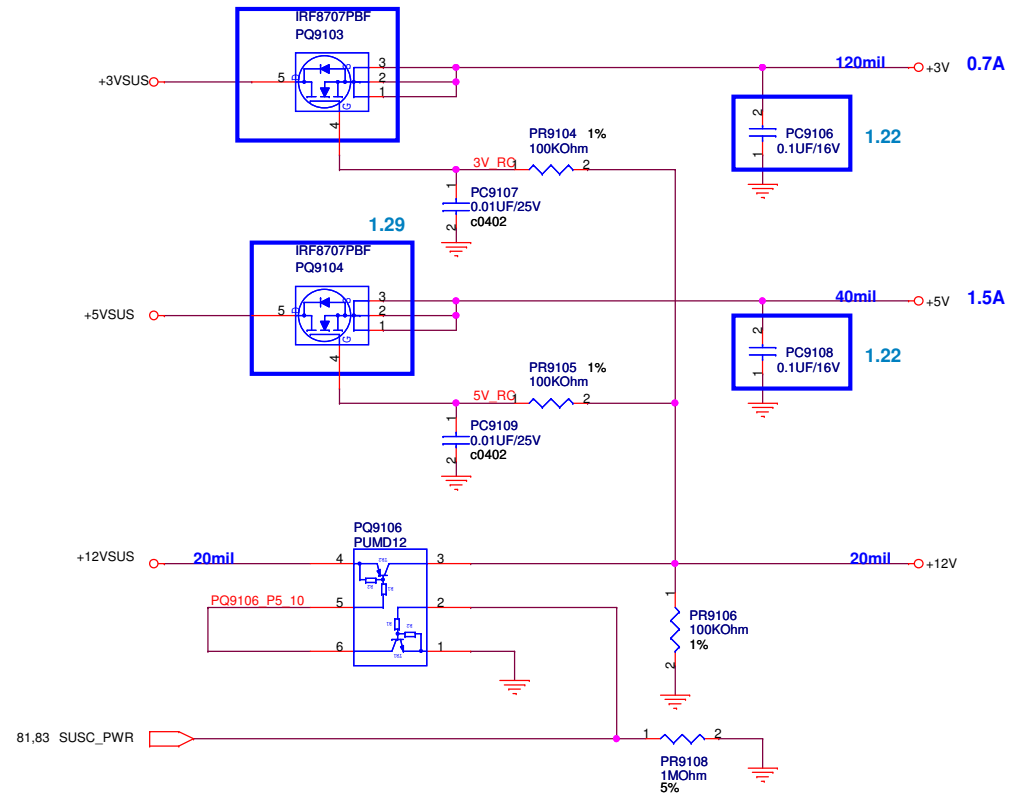
<Variant Name>

		Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Matt_Wang	
Size Custom	Project Name Design_IP	Rev 1.0	
Date: Monday, February 08, 2010		Sheet	90 of 95

SUSB_PWR POWER 1.29



SUSC_PWR POWER 1.29



ASUS		Title : POWER_LOAD_SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Matt_Wang	
Size	Project Name	Rev	
B	Design_IP	1.0	
Date: Monday, February 08, 2010		Sheet	91 of 95