K52N SCHEMATIC R10

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5	CPU-PENRYN(2)
6	CPU CAP
7	DDR2 SO-DIMM_0
8	DDR2 SO-DIMM_1
9	DDR2 ADDRESS TERMINATION
10	NB_-CANTIGA--CPU (1)
11	NB_-CANTIGA--DDR2/PEG (2)
12	NB_-CANTIGA--DDR2 bus (3)
13	NB_-CANTIGA--POWER (4)
14	NB_CANTIGA--POWER (5)
15	NB_-CANTIGA--GND/Strapping (6)
20	SB_-ICH9M--(1)-SATA,AUDIO,ACZ
21	SB_-ICH9M--(2)-PCI,PCI-E,USB
22	SB_-ICH9M--(3)-GPIO
23	SB_-ICH9M--(4)-PWR/GND
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35	MDC
36	CODEC-ALC663
37	AUDIO_AMP-1431&HP
38	Microphone&Line-in
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41	CARDBUS R5C833(1394 & SD)
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43	EXPRESS CARD
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48	HDMI
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53	WLAN(MINI CARD)
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57	DISCHARGE

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66	E-SATA
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82	82_POWER_I/O_1.5VS & 1.05VS
83	83_POWER_I/O_DDR & VTT
85	85_POWER_VGA_CORE & +1.1VO
87	87_POWER_SHUTDOWN#
88	88_POWER_CHARGER
90	90_POWER_PROTECT
91	91_POWER_LOAD SWITCH
92	92_POWER_PROTECT
93	93_POWER_SIGNAL
94	94_POWER_FLOWCHART

ASUSTeK COMPUTER INC. NB1

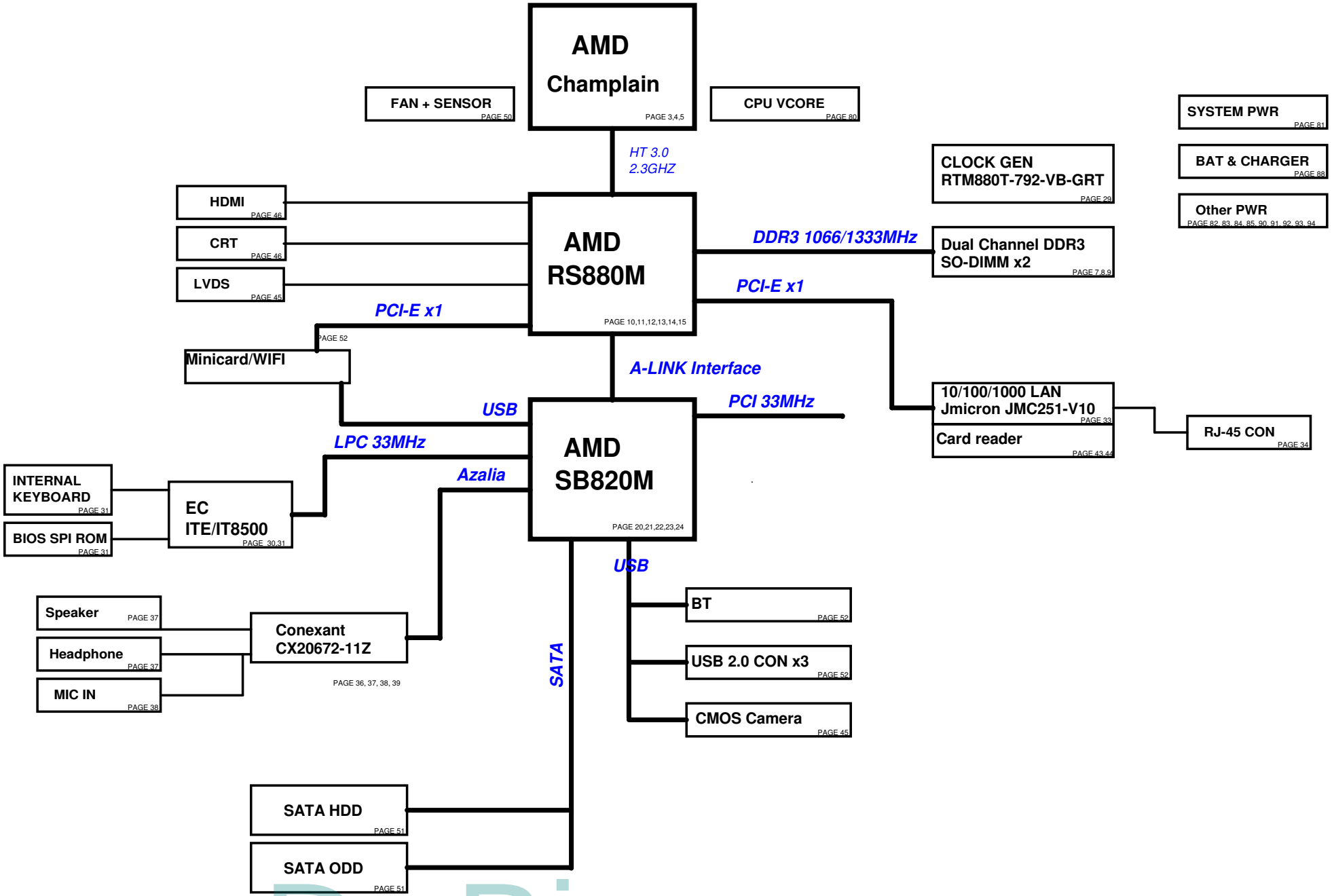
Title : Page Reference

Engineer: Vincent_Chiang

Size	Project Name	Rev
Custom	K52N	1.0

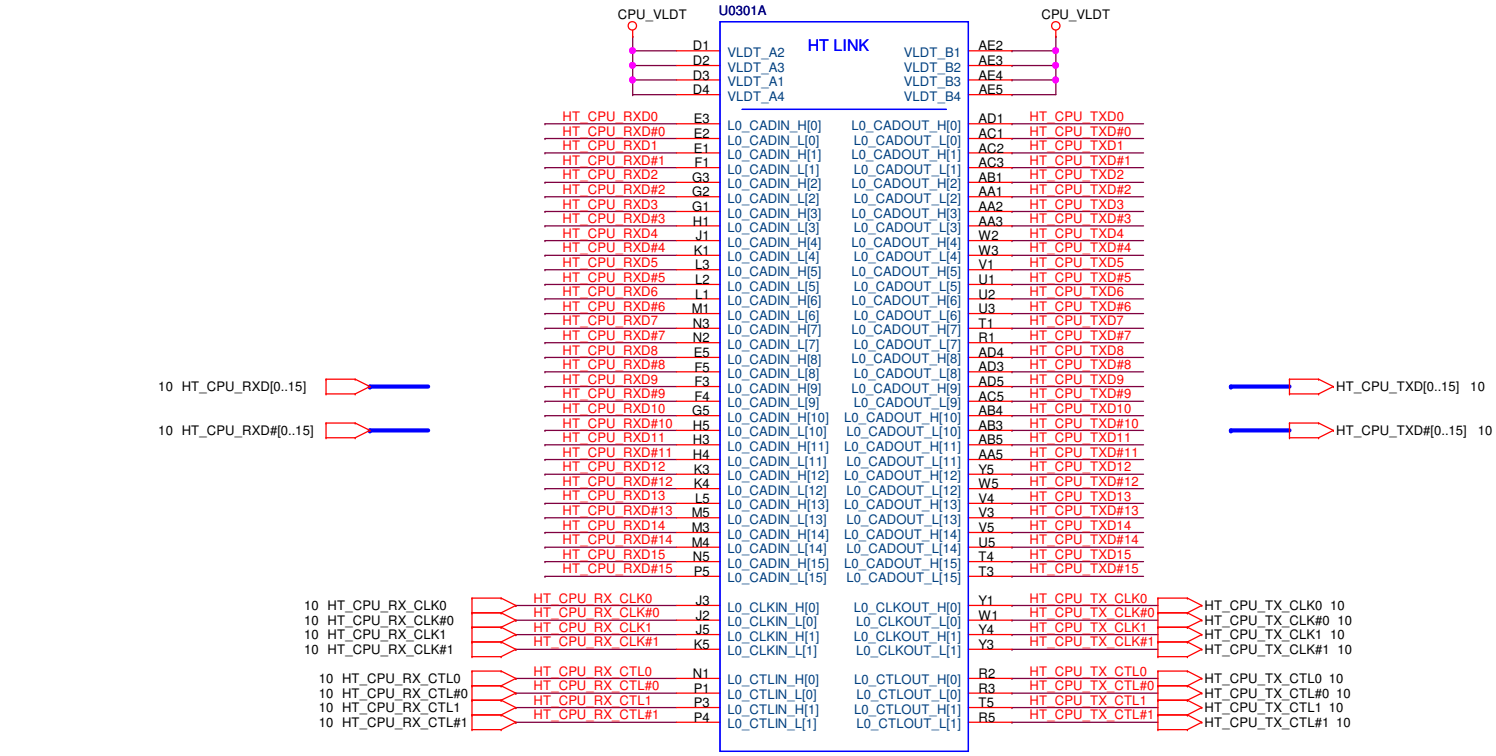
Date: Monday, February 08, 2010 Sheet 1 of 93

K52N Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 2 of 93	

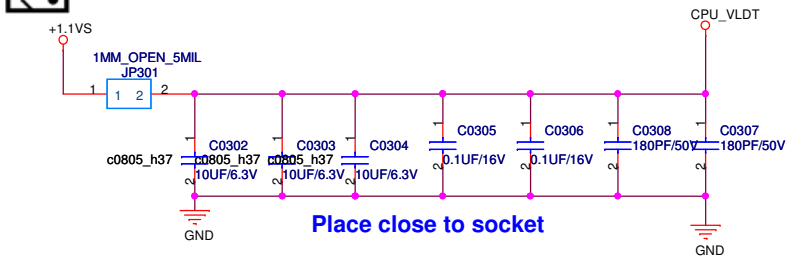
1.5A



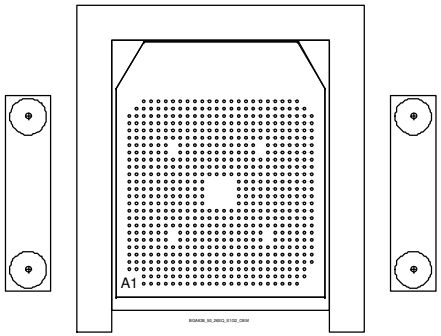
Change P/N to 12G011306380

071113

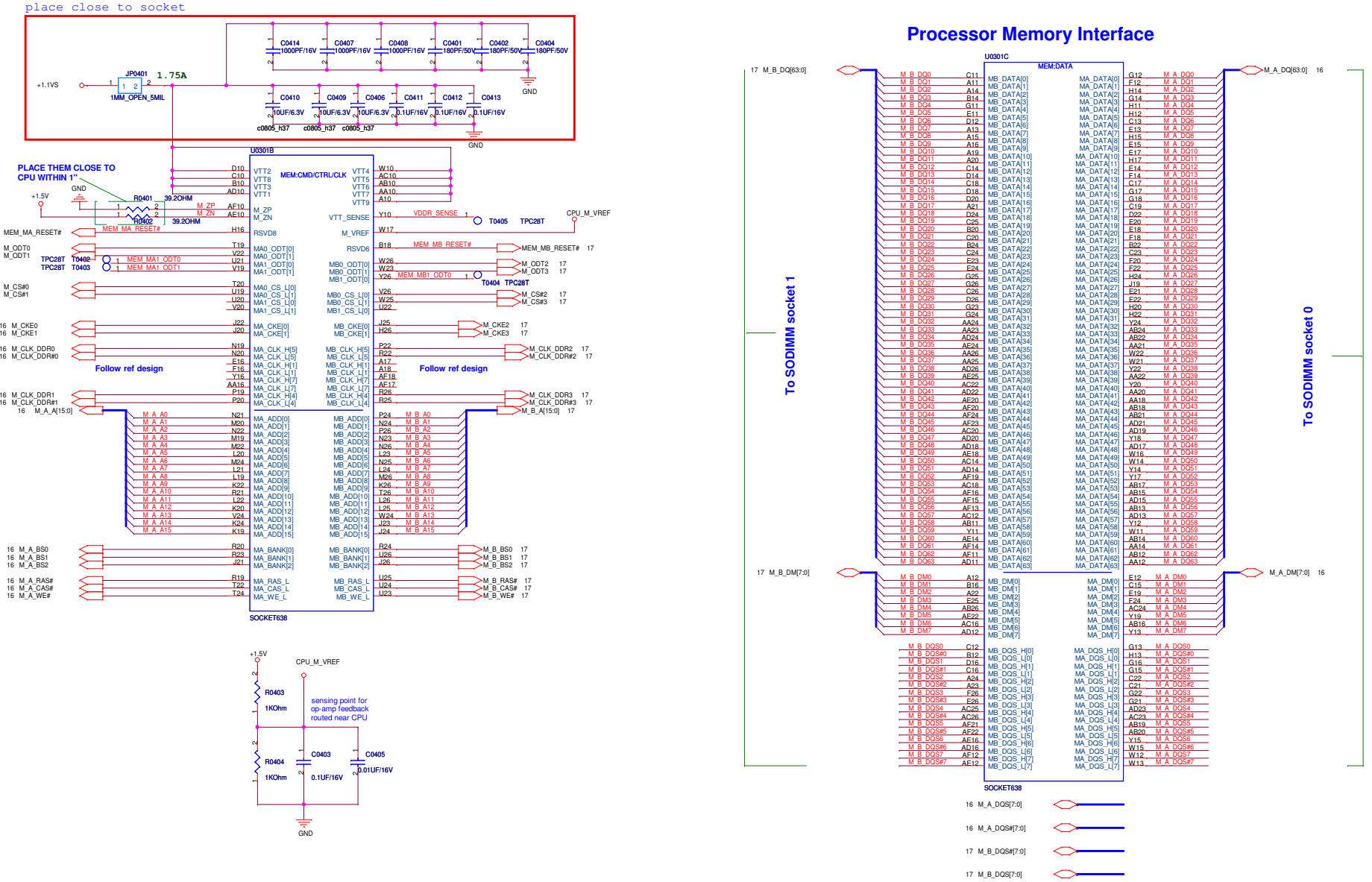
Do not cross plane.



* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

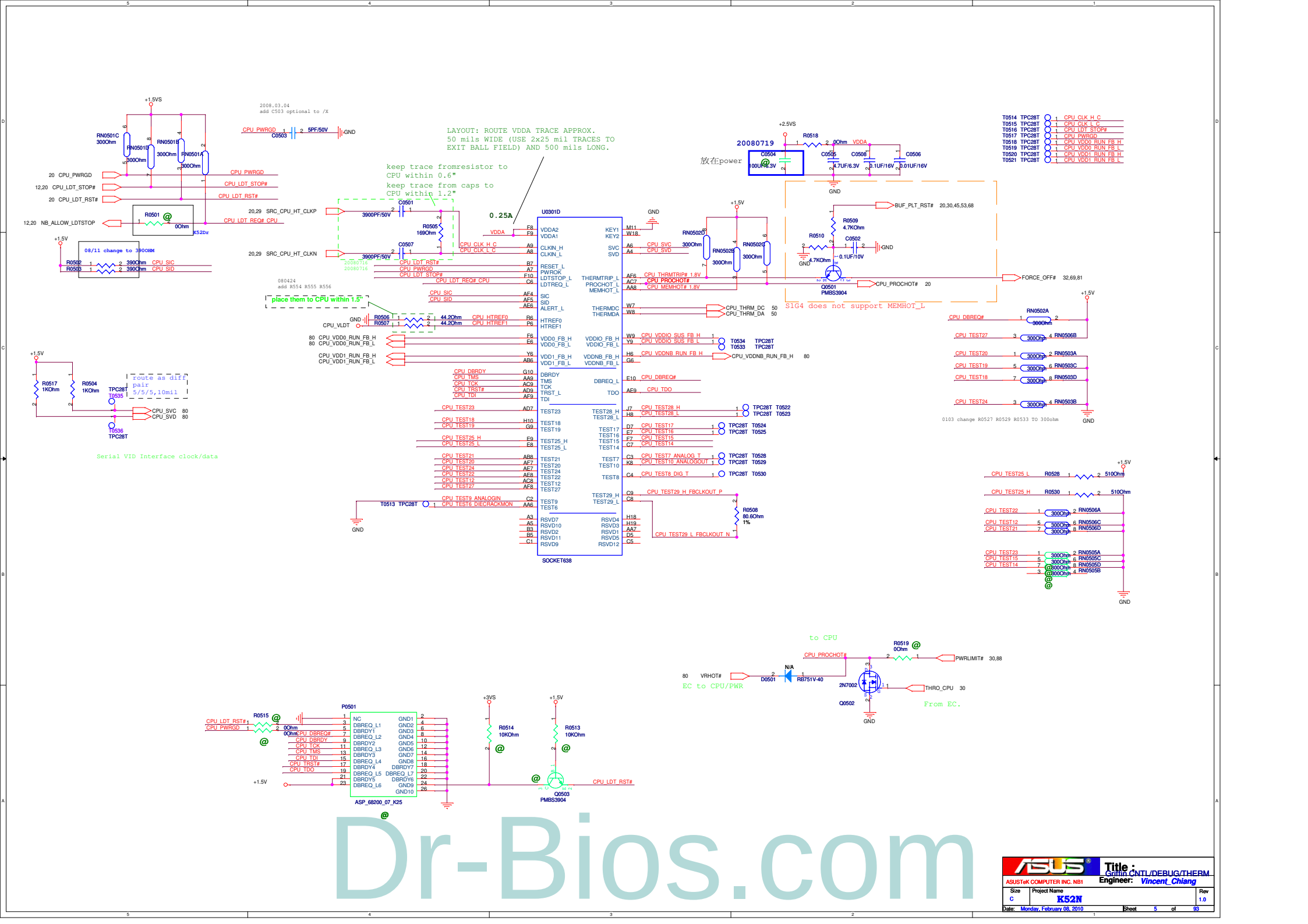


ASUSTeK COMPUTER INC. NB1	Title : Griffin HT I/F	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 3 of 93	

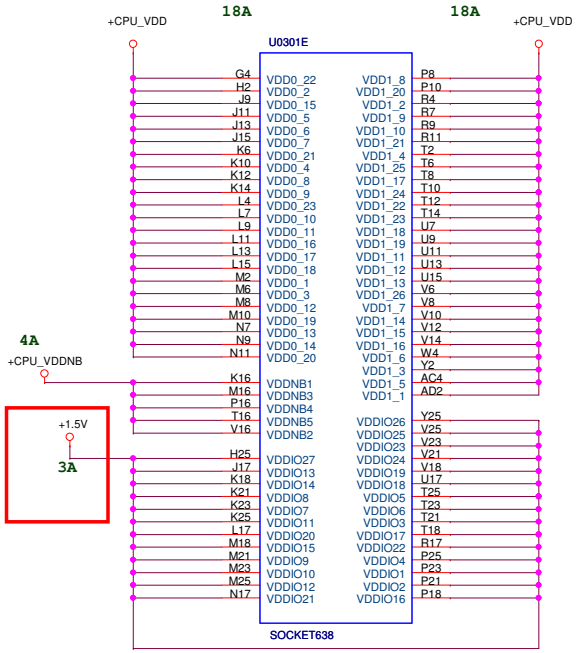


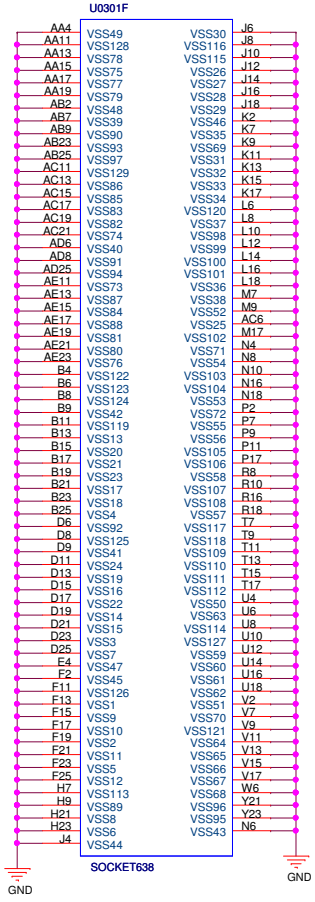
Processor Memory Interface

ASUSTeK COMPUTER INC. NB1	Title: Penryn DDR2 MEMORY I/F	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 4 of 93	

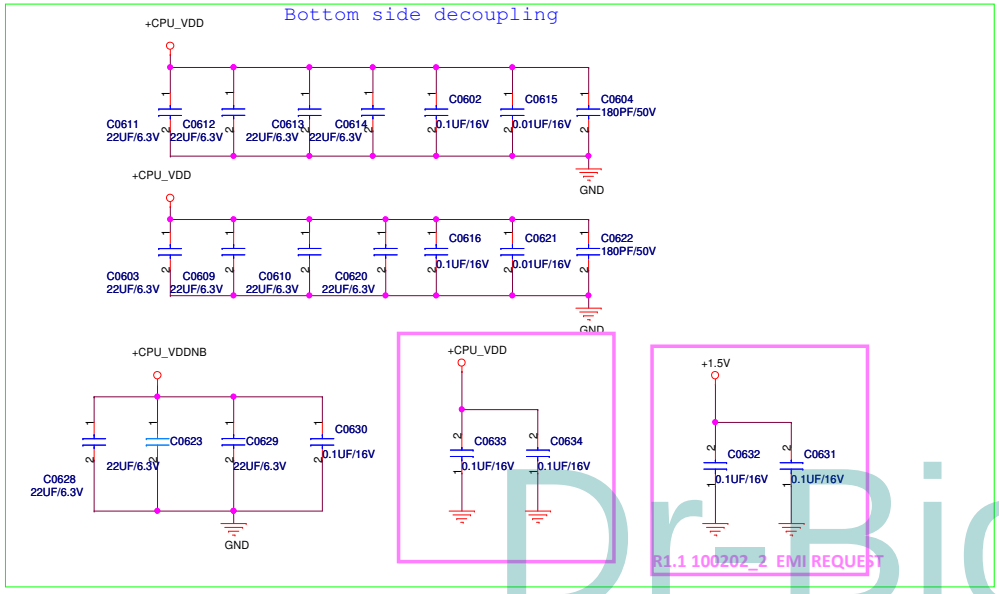


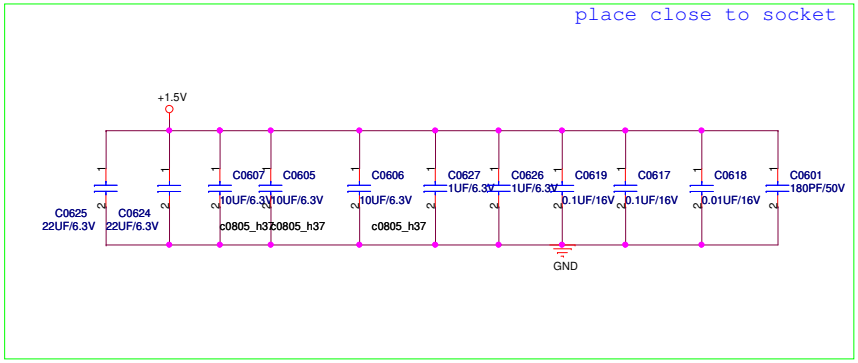
ASUSTeK COMPUTER INC. NB1	Title : Griffin CNTL/DEBUG/THERM	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 5 of 93	





Decoupling between Processor and DIMMs, Place close to Porcessor as possible



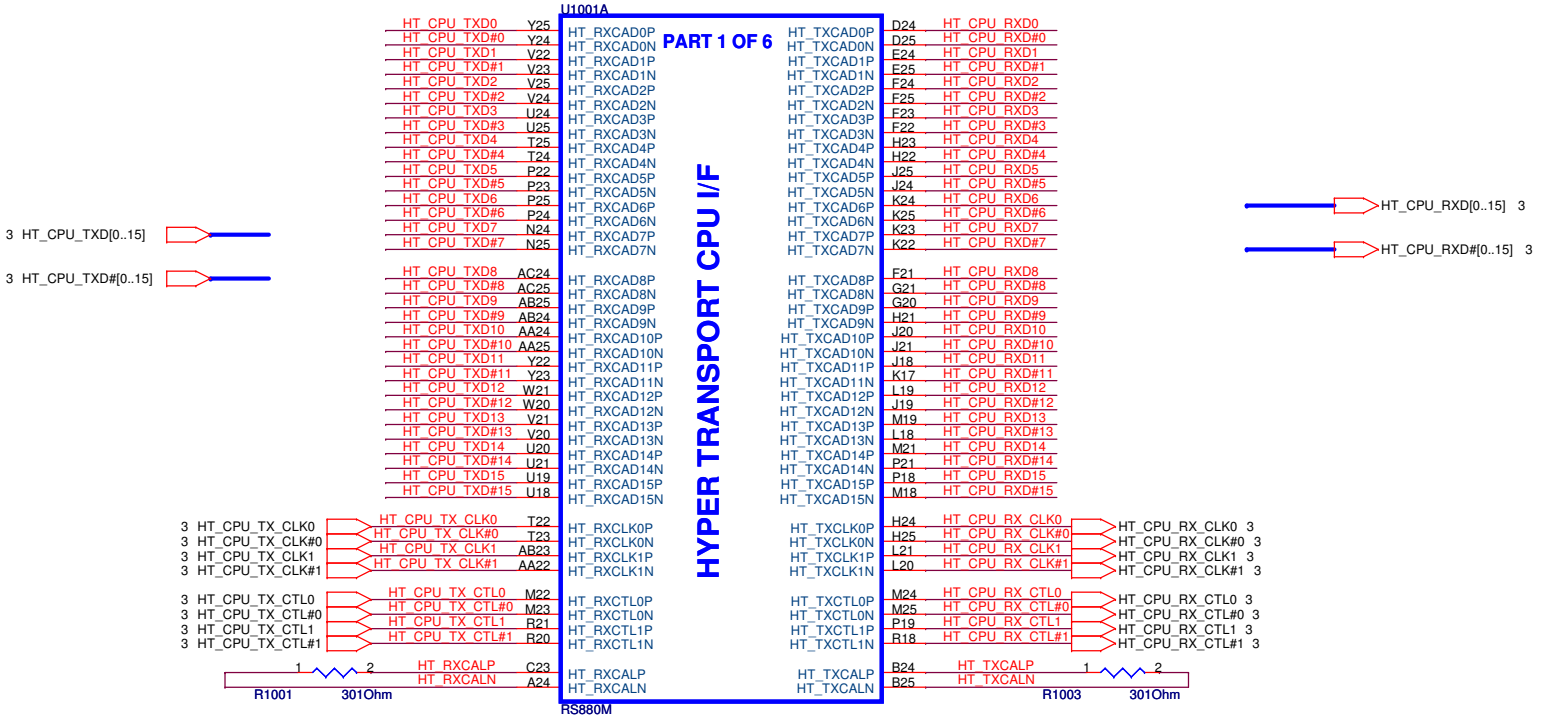


ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 6 of 93	

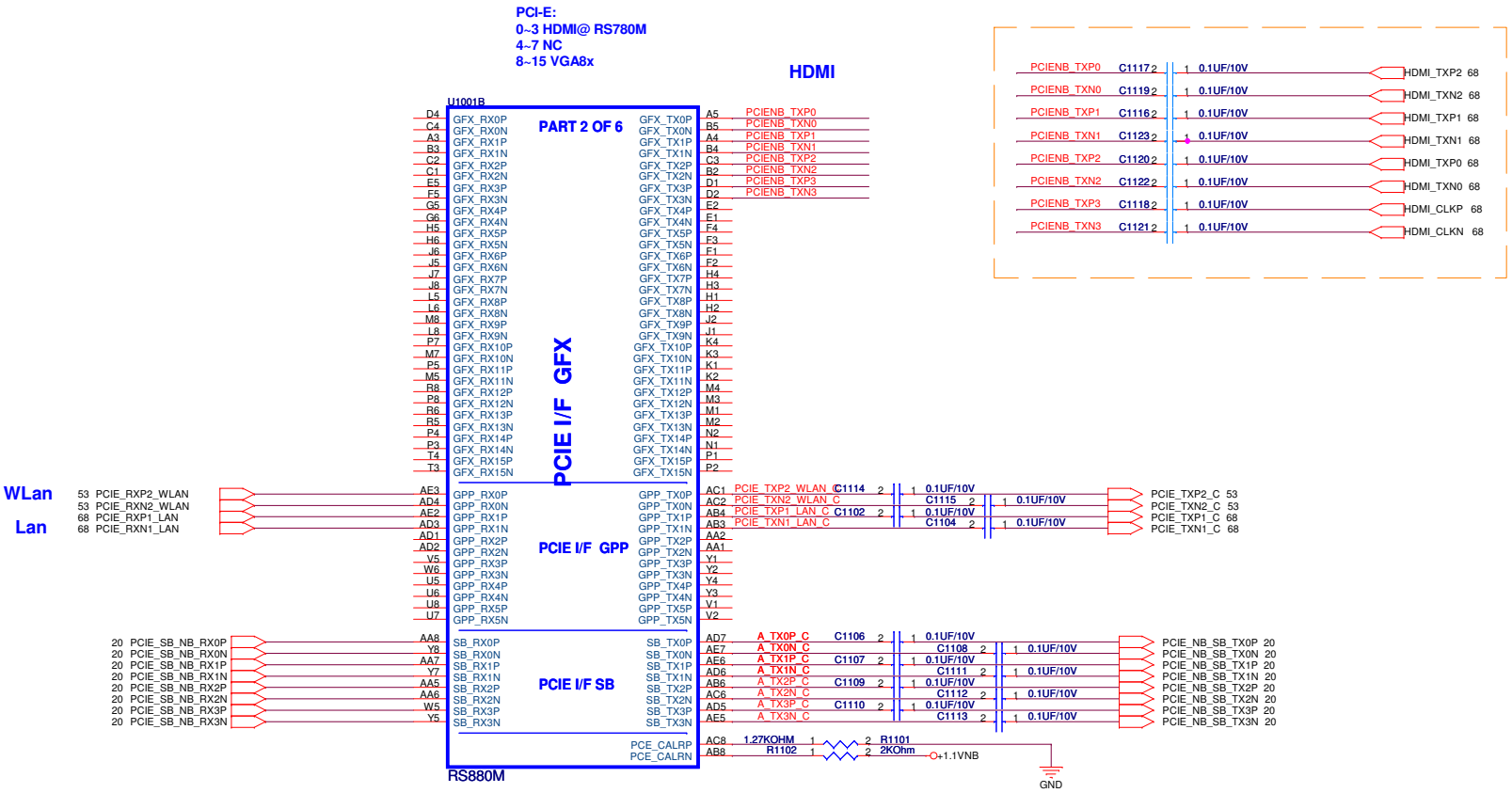
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 7 of 93	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 8 of 93	

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: Vincent_Chiang
Size: B	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 9 of 93



ASUSTeK COMPUTER INC. NB1	Title : RS880M-HT LINK I/F	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 10 of 93	



ASUSTeK COMPUTER INC. NB1	Title : RS880M-PCIE LINK I/F	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 11 of 93	

NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

RS780 POWERGOOD is 1.8VS rail

Single channel

110mA,RX881 GND

20mA,RX881 GND

4mA,RX881 GND

65mA,RX881 GND

20mA,RX881 GND

20mA

120mA

PR

R1.1 100127_1 Change EDID CLK/DAT Circuit

net AUC_CAL Refence F50z

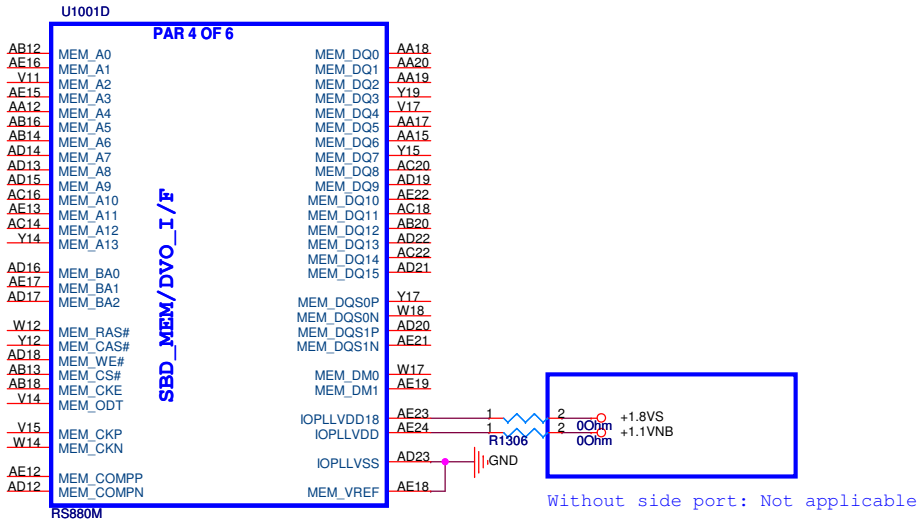
Check the VDDLT33 power connection

VDDLT33 for 740 only

STRP_DATA	0	1
VCC_NB	.95V	1.1V

K52Dr

ASUSTeK COMPUTER INC. NB1	Title : RS880M-SYSTEM I/F	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 12 of 93	



Without side port: Not applicable

080118

Disable Side Port Memory

R1.1

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

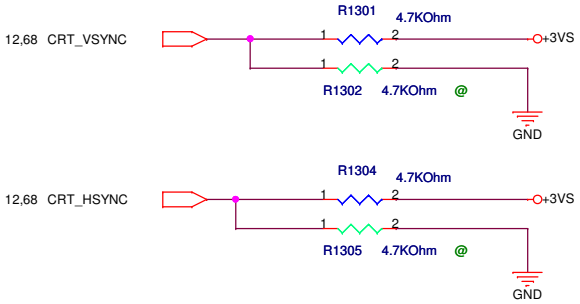
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

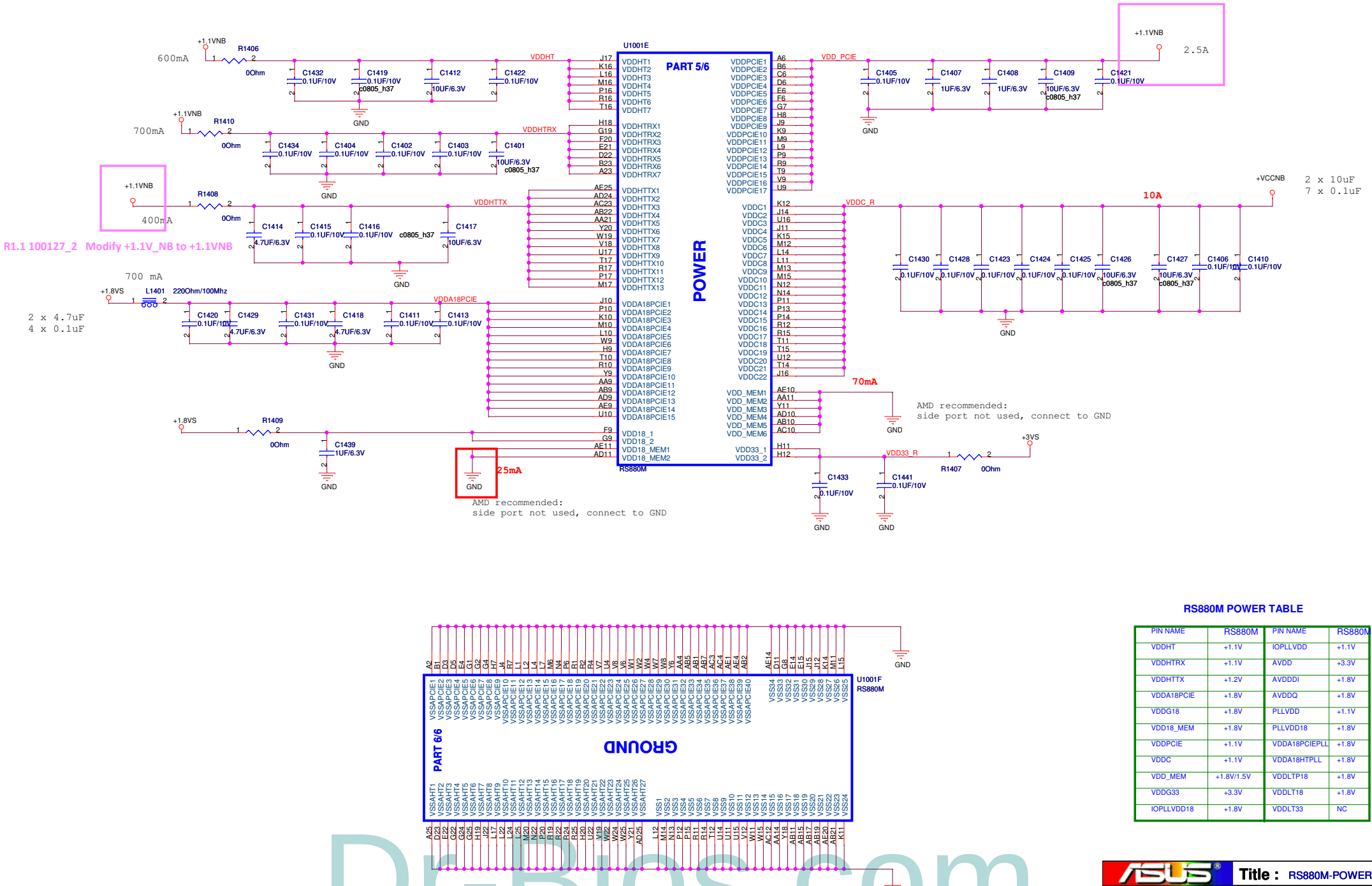
RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



ASUSTeK COMPUTER INC. NB1	Title : RS880M-SPMEM/STRAPS	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 13 of 93	



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

ASUSTeK COMPUTER INC. NB1

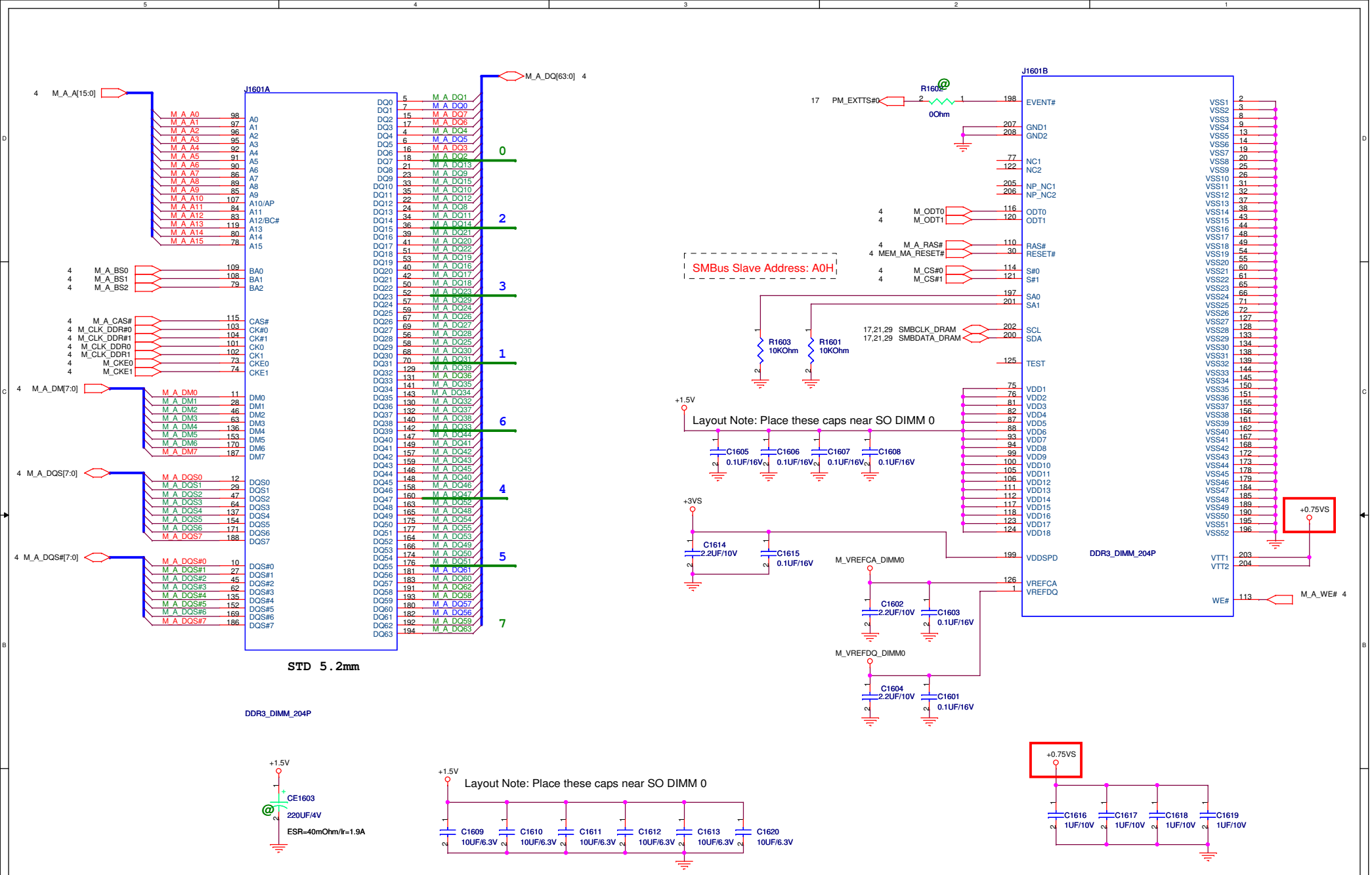
Title : RS880M-POWER

Engineer: Vincent_Chiang

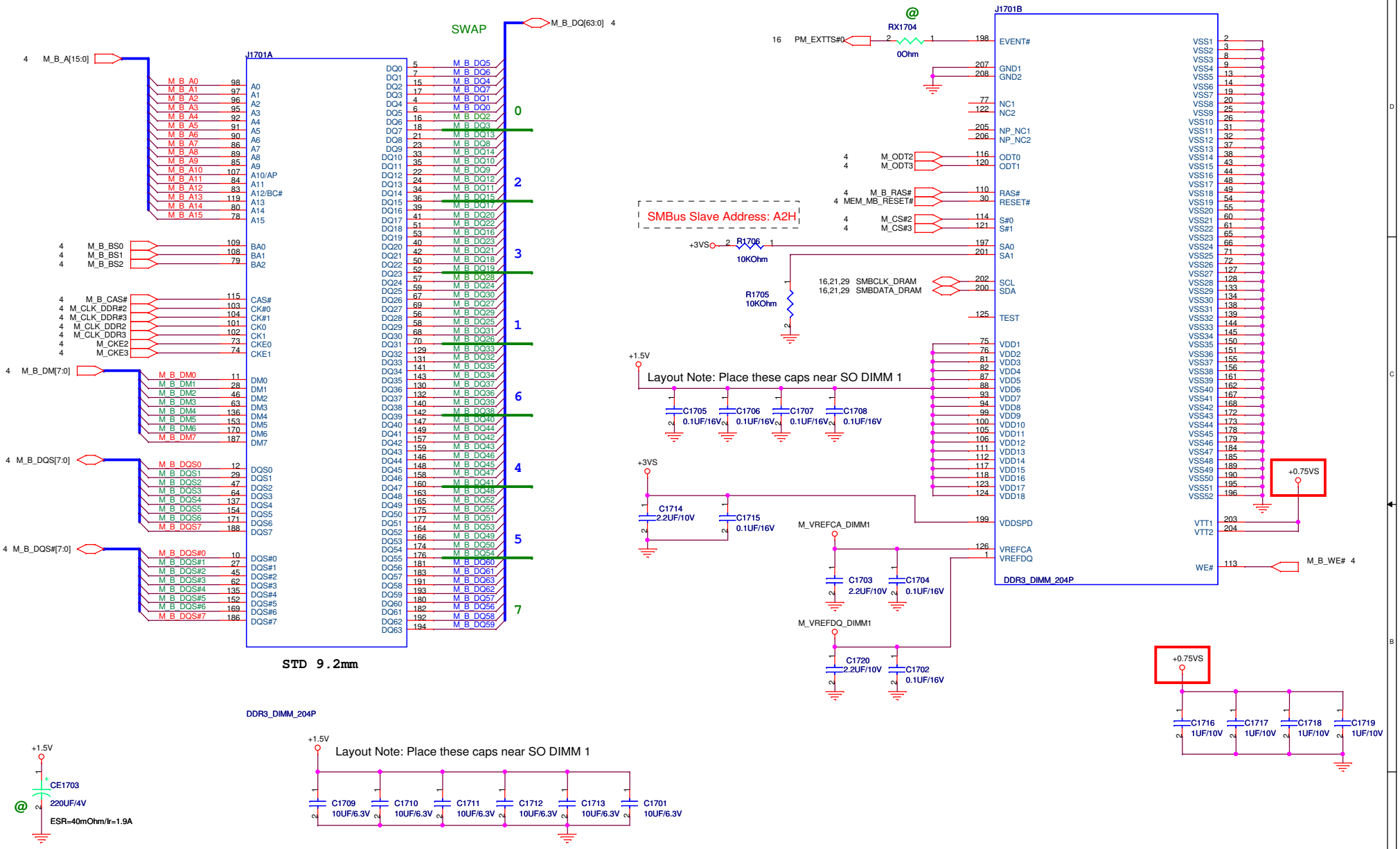
Size	Project Name	Rev
Custom	K52N	1.0

Date: Monday, February 08, 2010 Sheet 14 of 93

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: Vincent_Chiang
Size: A	Project Name: K52N
Rev: 2.0	
Date: Monday, February 08, 2010	Sheet 15 of 93

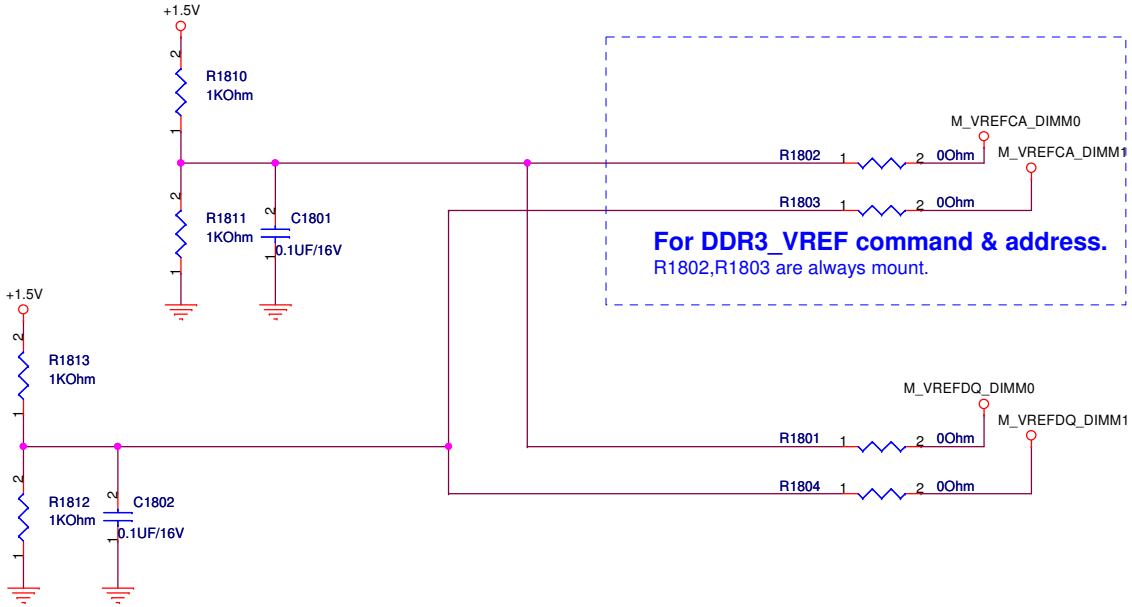


ASUSTeK COMPUTER INC. NB6	Title: DDR3 SO-DIMM_0		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 2.0
Date: Monday, February 08, 2010	Sheet 16 of 99		



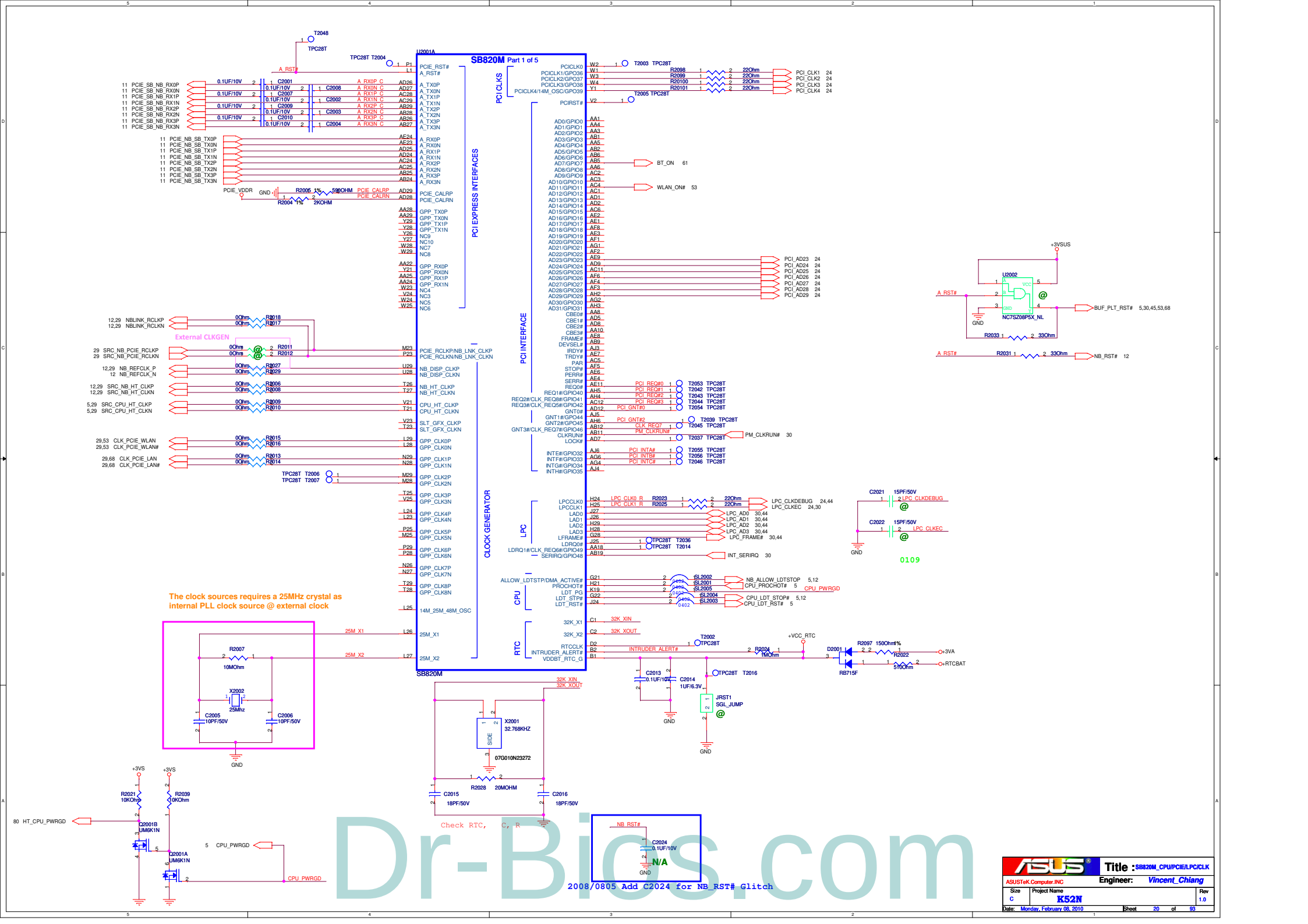
ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 17 of 99	

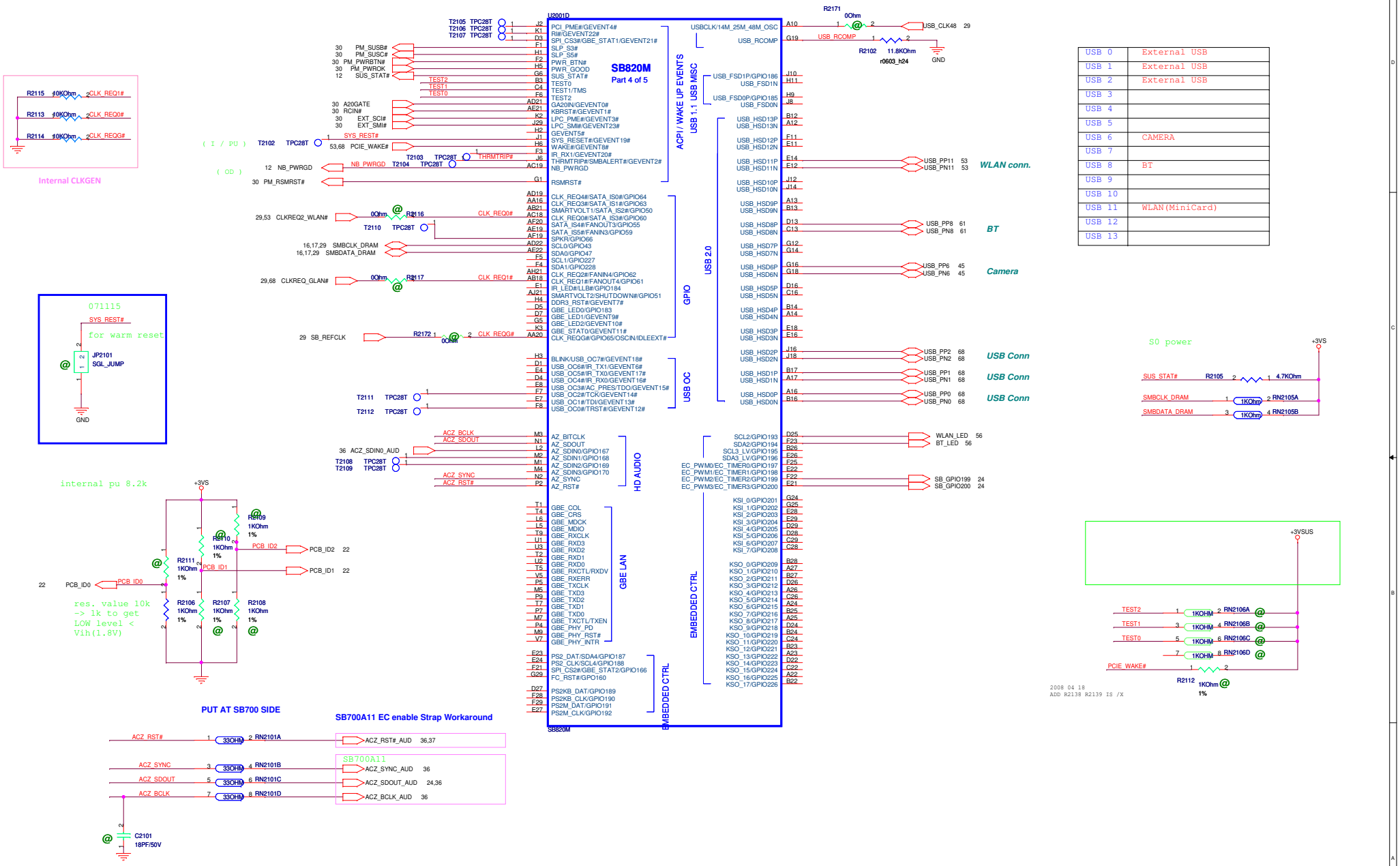
DDR3 Vref



ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 18 of 99	

Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: K52N
Rev: 2.0	
Date: Monday, February 08, 2010	Sheet 19 of 93


SB820M Part 1 of 5
U2001A
SB820M
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
PCI CLKS
LPC
CPU
RTC
External CLKGEN
The clock sources requires a 25MHz crystal as internal PLL clock source @ external clock
2008/0805 Add C2024 for NB_RST# Glitch
Check RTC, C, R
Dr-Bios.com
Title : SB820M_CPU/PCIE/LPC/CLK
ASUSTeK.Computer.INC
Engineer: Vincent_Chiang
Project Name K52N
Rev 1.0
Date: Monday, February 08, 2010
Sheet 20 of 93



USB 0	External USB
USB 1	External USB
USB 2	External USB
USB 3	
USB 4	
USB 5	
USB 6	CAMERA
USB 7	
USB 8	BT
USB 9	
USB 10	
USB 11	WLAN(MiniCard)
USB 12	
USB 13	

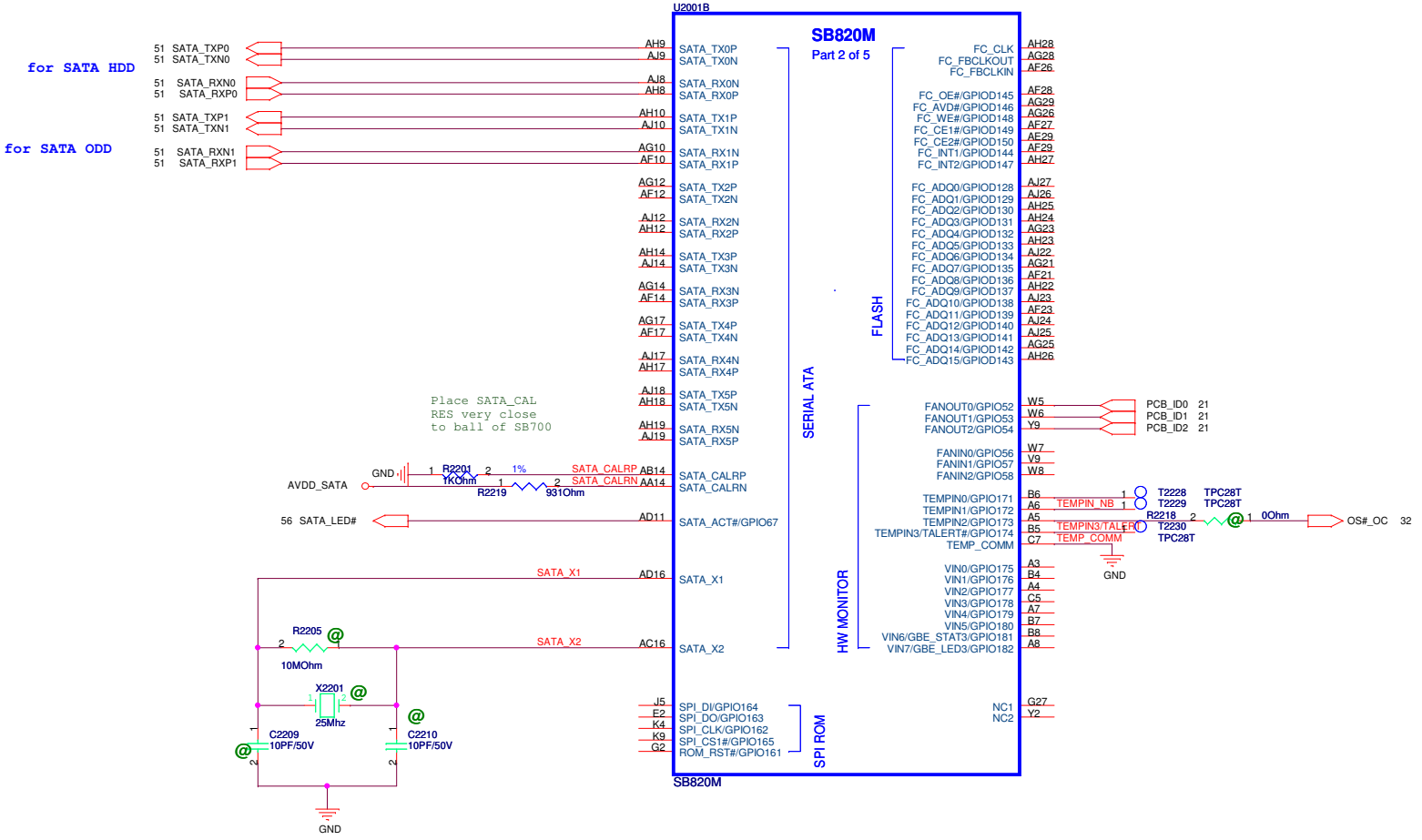
ASUSTeK.Computer.INC

Title : SB700_GPIO/USB/HD/ACPI

Engineer: Vincent_Chiang

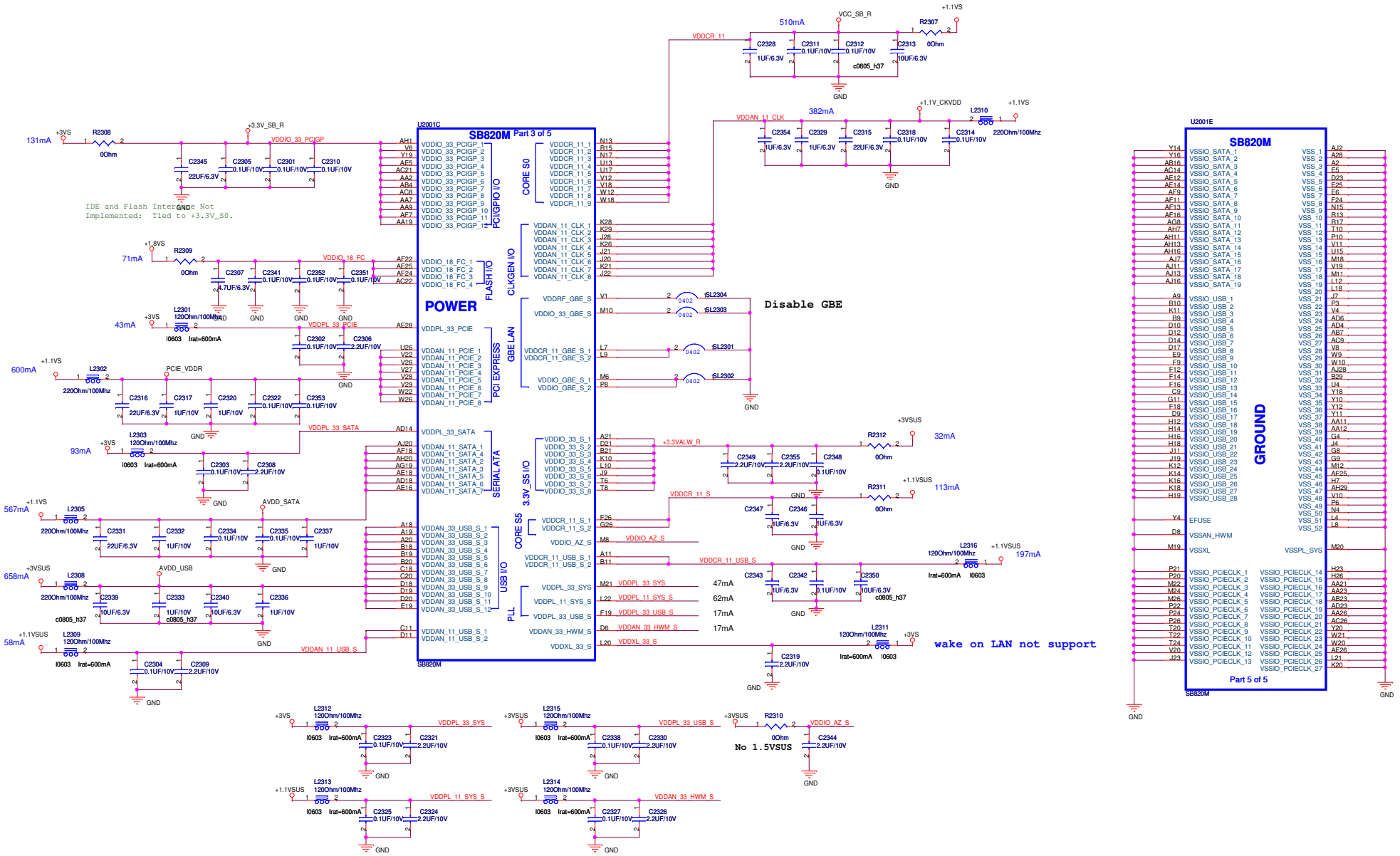
Size	Project Name	Rev
C	K52N	1.0

Date: Monday, February 08, 2010 Sheet 21 of 93

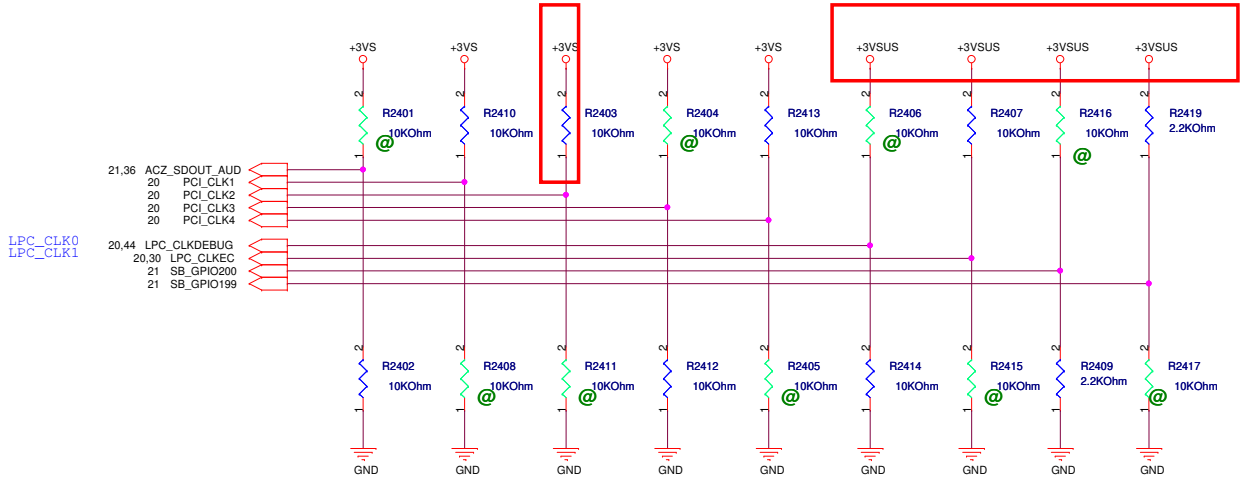


ASUSTeK.Computer.INC	Title : SB820M_PATA/SATA	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 22 of 93	

Check power Level and state

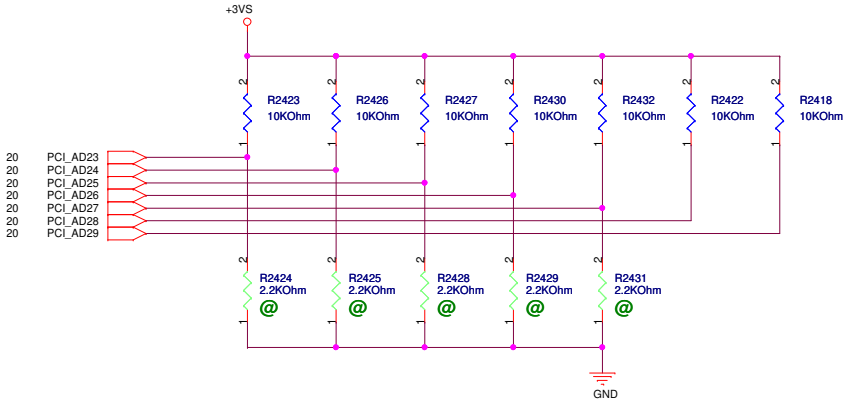


ASUSTeK.Computer.INC	Title : SB820M_POWER		
	Engineer: Vincent_Chiang		
Size: C	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 23 of 93		



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled Modify	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

ASUSTeK.Computer.INC

Title : SB820M_STRAP

Engineer: Vincent_Chiang

Size	Project Name	Rev
Custom	K52N	1.0

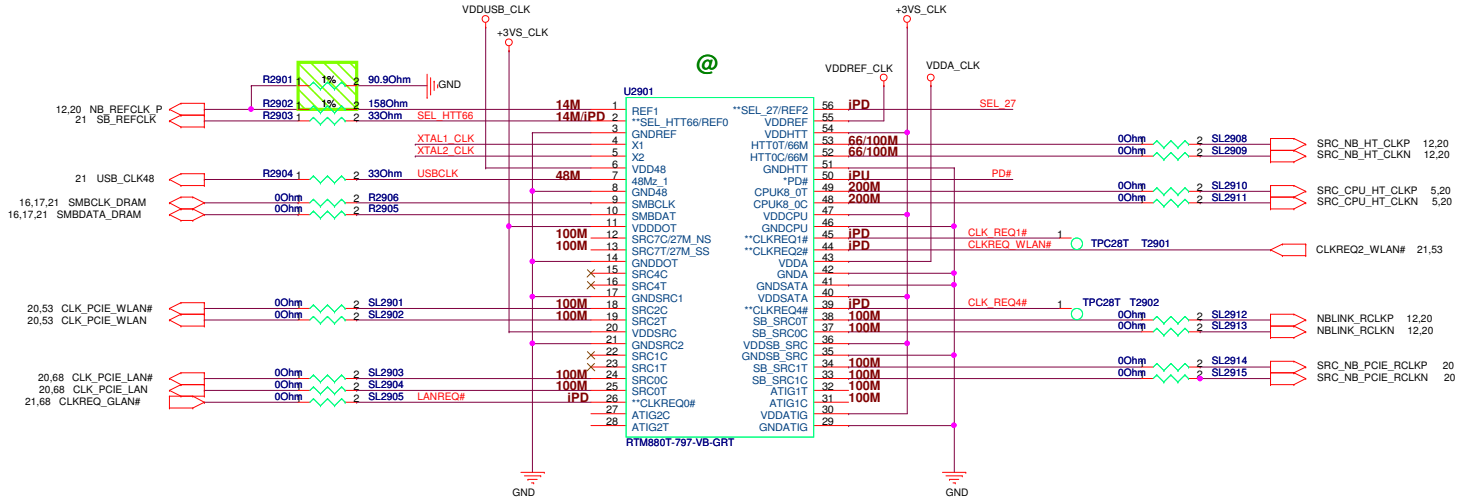
Date: Monday, February 08, 2010 Sheet 24 of 93

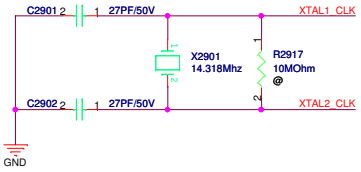
ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 25 of 93	

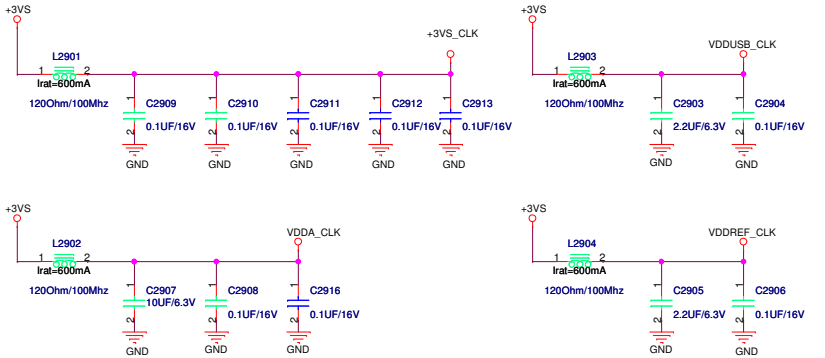
ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 26 of 93	

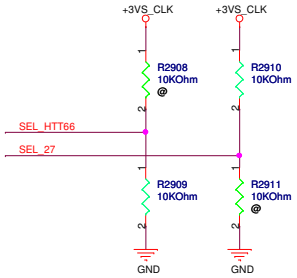
ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size A	Project Name K52N	Rev 1.0
Date: Monday, February 08, 2010	Sheet 27 of 93	

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 28 of 93		



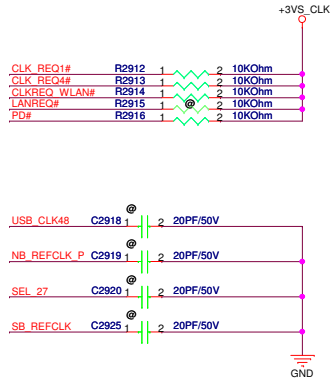






SEL_HTT66
0 : 100 MHz differential HTT clock (Default)
1 : 66MHz single ended HTT clock

SEL_27
0 : 100 MHz differential Spread SRC clock
1 : 27MHz spread/non-spreading single clock (Default)



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICS9LPRS489AGLFT

Engineer:

Size	Project Name	Rev
Custom	K51AB	2.0

Date: Monday, February 08, 2010 Sheet 29 of 93

Remove VSUS_ON pull down
Remove CPU_VRON pull down
Remove ALS_AD
Remove CAP_ACK_A#
Remove CAP_ACK_B#
E1:原SUSC_EC#改隔EGAD_EC,SUSC_EC#改至H3
E2:原SUSB_EC#改隔EGCS_EC,SUSB_EC#改至H4
E3:原CPU_VRON#改隔N/C,CPU_VRON改至J0

U3002

LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus

A2:BATSEL_3S#
A3:GAME_LED_EC#
B2:3G_ON#
H1:GFX_VR_ON
I0:NV_OVERT#
I4:GFX_VR
I6:KB_TDO
I7:KB_TDI
D7:COLOREN#
F3:DISTP#

IT8500E-L

R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX

Battery
Thermal sensor

For PU / PD

R3008 100KOhm BAT1_IN_OC#
R1.1 100128_1 Battery R/D Request

iAMT EC strapping need to check

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For X'tal

Note:
Cload=12.5PF place close to EC

X3001 32.768KHZ
07G010N23272

For EC Hardware Strap

I/O Base Address
Note: It can be programmable by EC fireware

Share Memory
Note: It can be programmable by EC fireware.

PP Enable
Note: Default Int. Pull-Low

R3045: For Xtal measurement

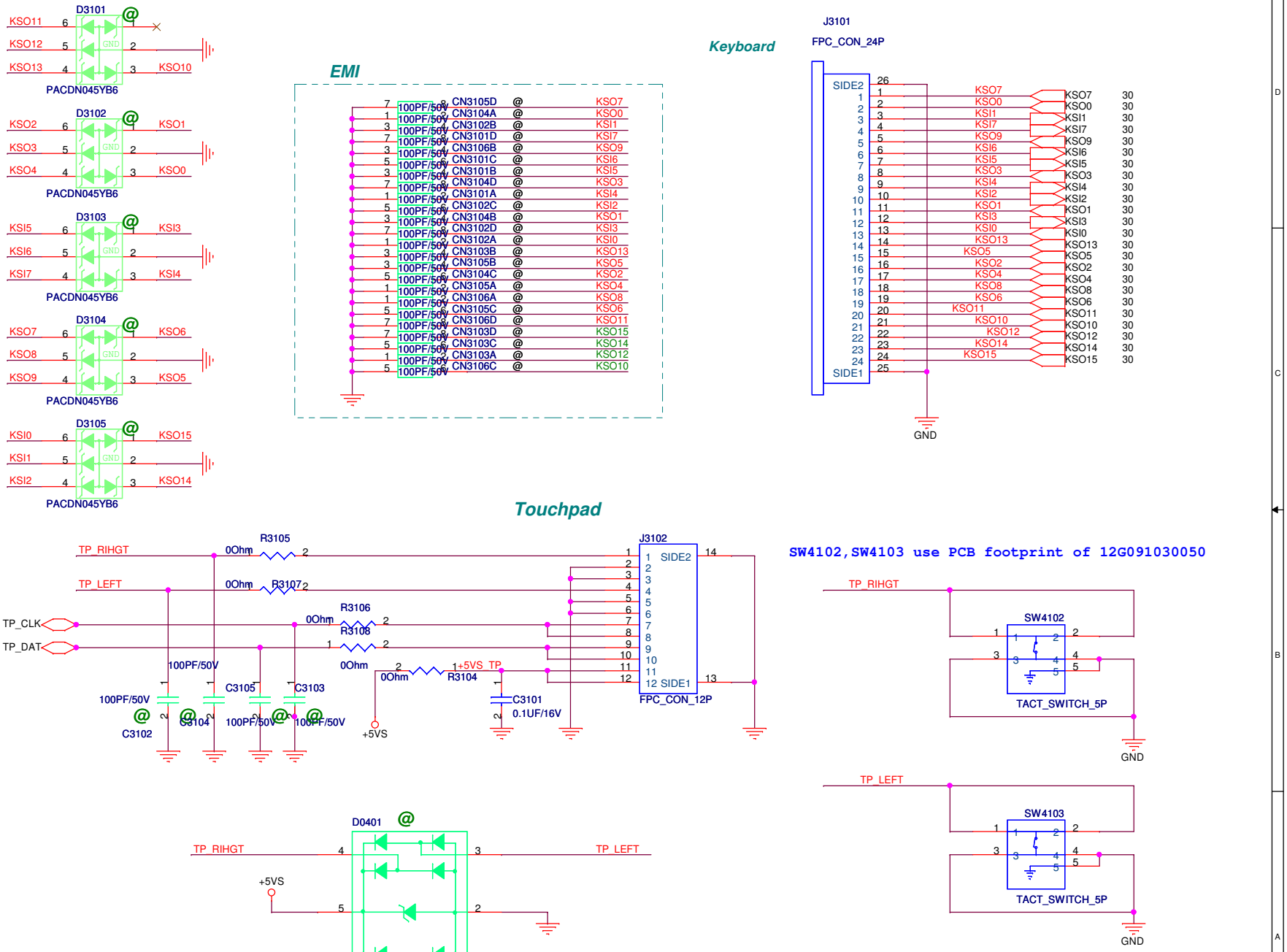
For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

U3003 SST25VF016B (8Mb)

For SPI Flash Debug

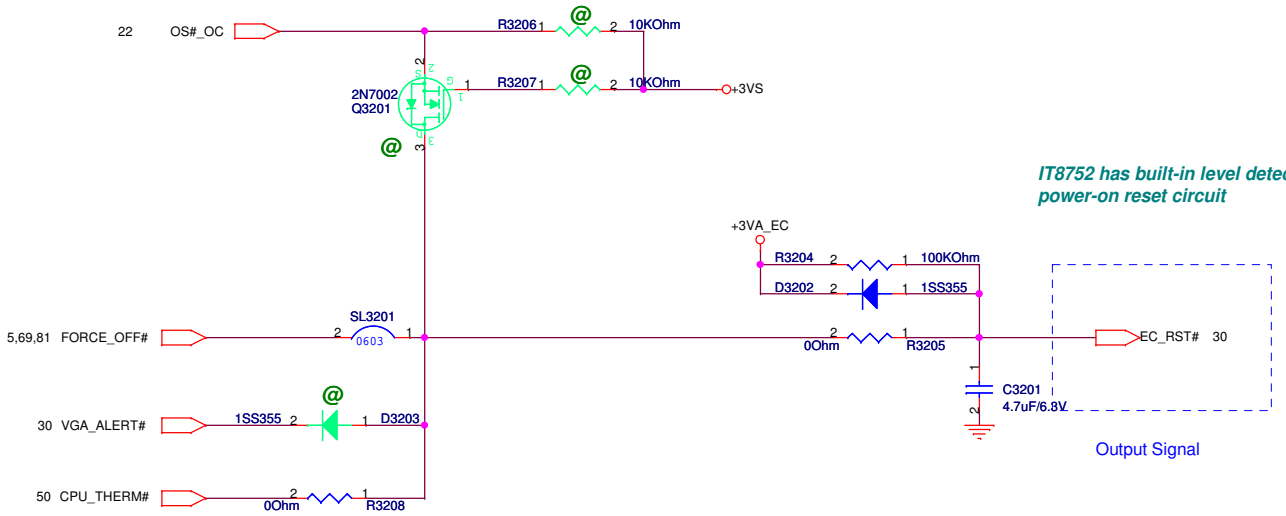
Title :	EC_IT8512 (1/2)
ASUSTeK COMPUTER INC. NB1	Engineer: Vincent_Chiang
Size: C	Project Name: K52N
Rev: 1.0	
Date: Tuesday, February 09, 2010	Sheet 30 of 93



ASUSTeK COMPUTER INC. NB4	Title : EC_IT8541(2/2)KB, TP	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 31 of 99	

Thermal Policy

Main Board



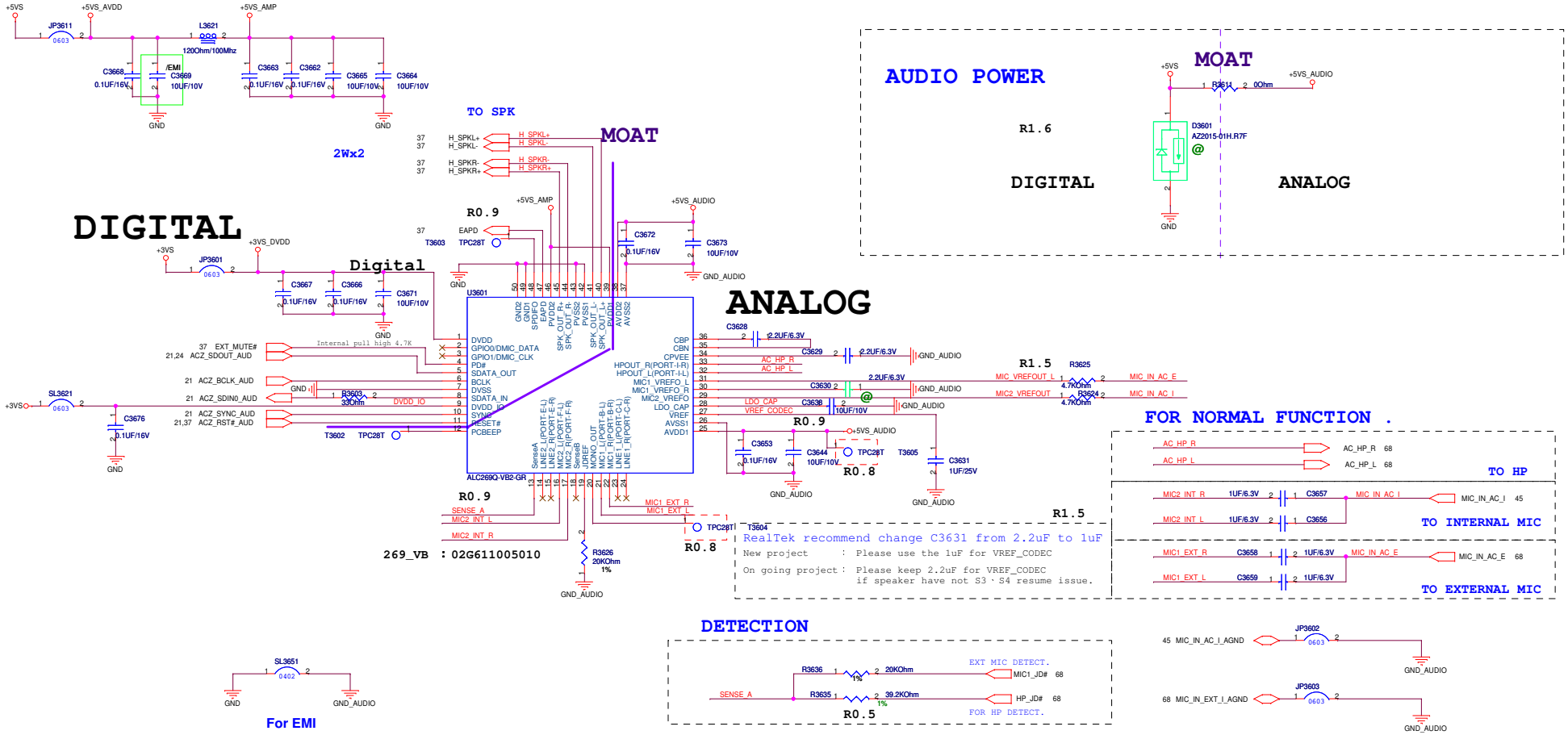
ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 32 of 99	

ASUSTeK COMPUTER INC. NB4	Title : LAN-AR8131	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 33 of 99	

ASUSTeK COMPUTER INC. NB4	Title : LAN_RJ45	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 34 of 99	

PE_GPIO2 for LVDS_SEL

ASUSTeK COMPUTER INC. NB1	Title : Hybrid Switch		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 35 of 93		



<Variant Name>

ASUSTeK COMPUTER INC. NB2

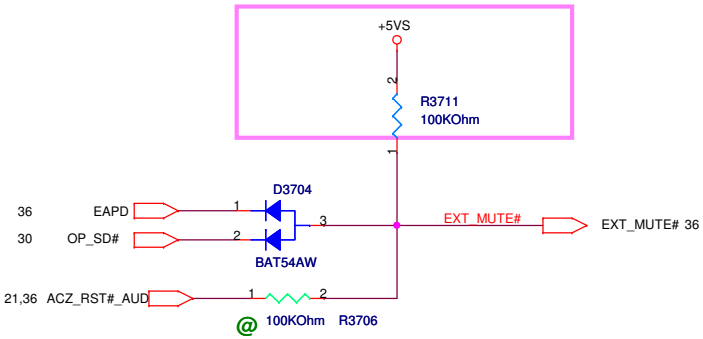
Title : CODEC ALC 269

Engineer: Leon

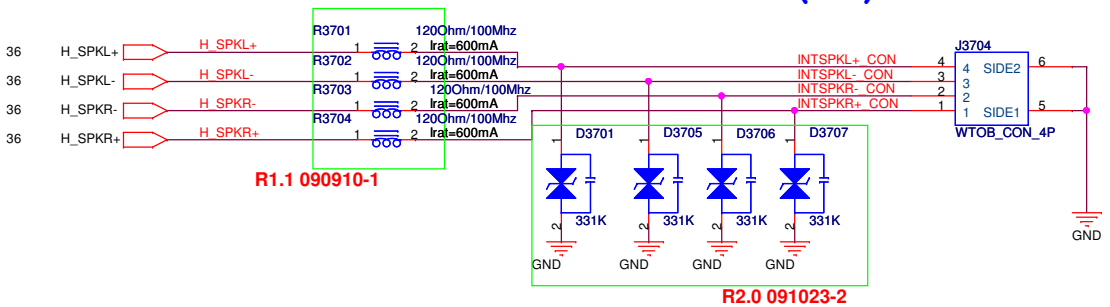
Size	Project Name	Rev
C	K52Jr	2.0

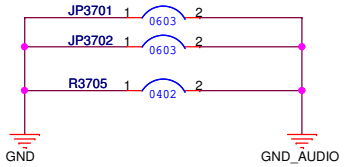
Date: Monday, February 08, 2010 Sheet 36 of 99

R1.1 100129_1 Change +3VS to +5VS



SPEAKER CONNECTOR (2W)





ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP	
	Engineer: Leon	
Size: B	Project Name: K52Jr	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 37 of 99	

R1.2,item L3

<Variant Name>

Title : AUD_****

ASUSTeK COMPUTER INC. NB2

Engineer: Vincent_Chiang

Size	Project Name	Rev
Custom	K52N	1.0

Date: Monday, February 08, 2010 Sheet 38 of 99

Main Board

ASUSTeK COMPUTER INC. NB4	Title : AUD_****	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 39 of 99	

ASUSTeK COMPUTER INC. NB1	Title : AU6433	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 40 of 99	

R1.2,item L1

ASUSTeK COMPUTER INC. NB4	Title : CB_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 41 of 99	

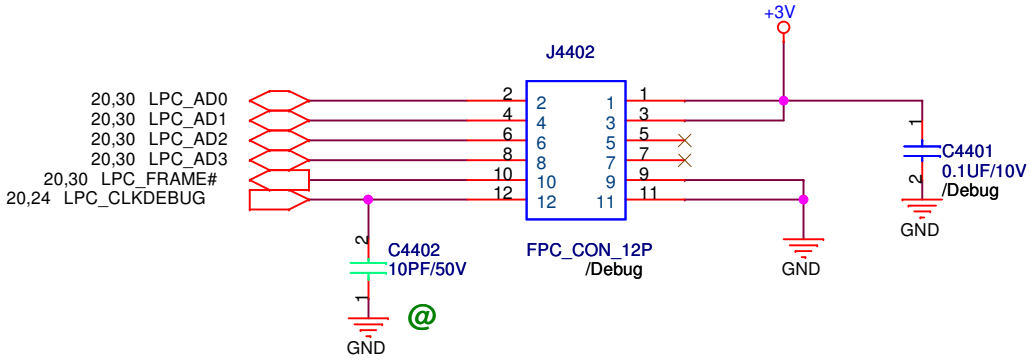
R1.2,item L1

ASUSTeK COMPUTER INC. NB4	Title : CB_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 42 of 99	

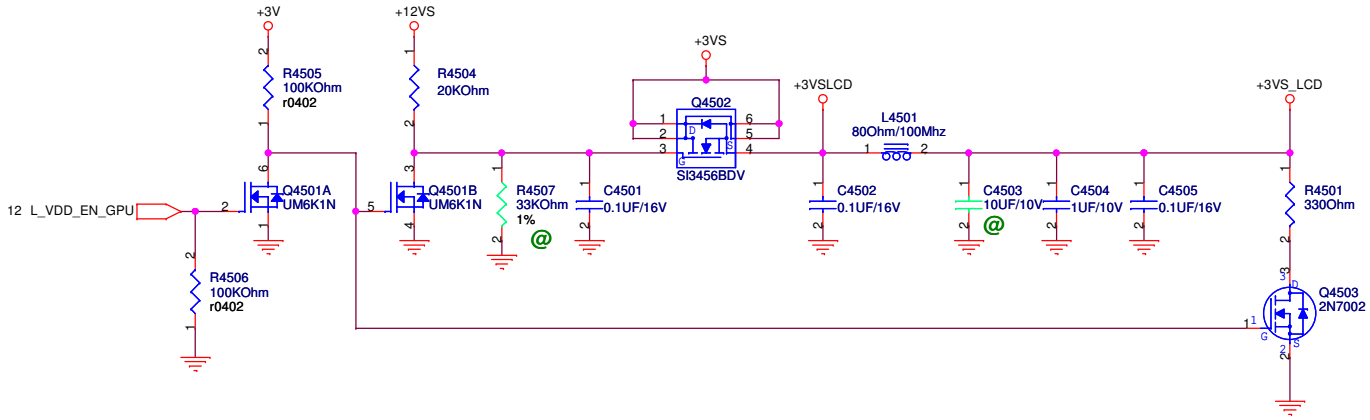
Main Board

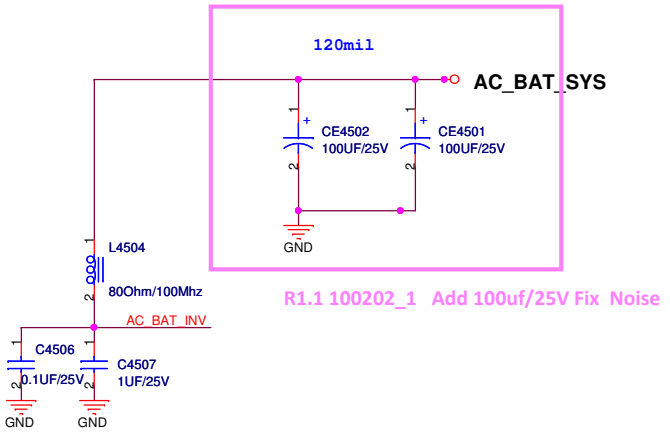
ASUSTeK COMPUTER INC. NB4	Title : CB_NewCard		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 43 of 99		

LPC Debug Port



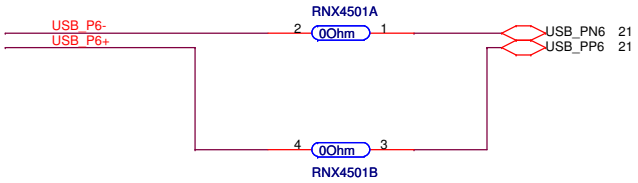
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 44 of 99	

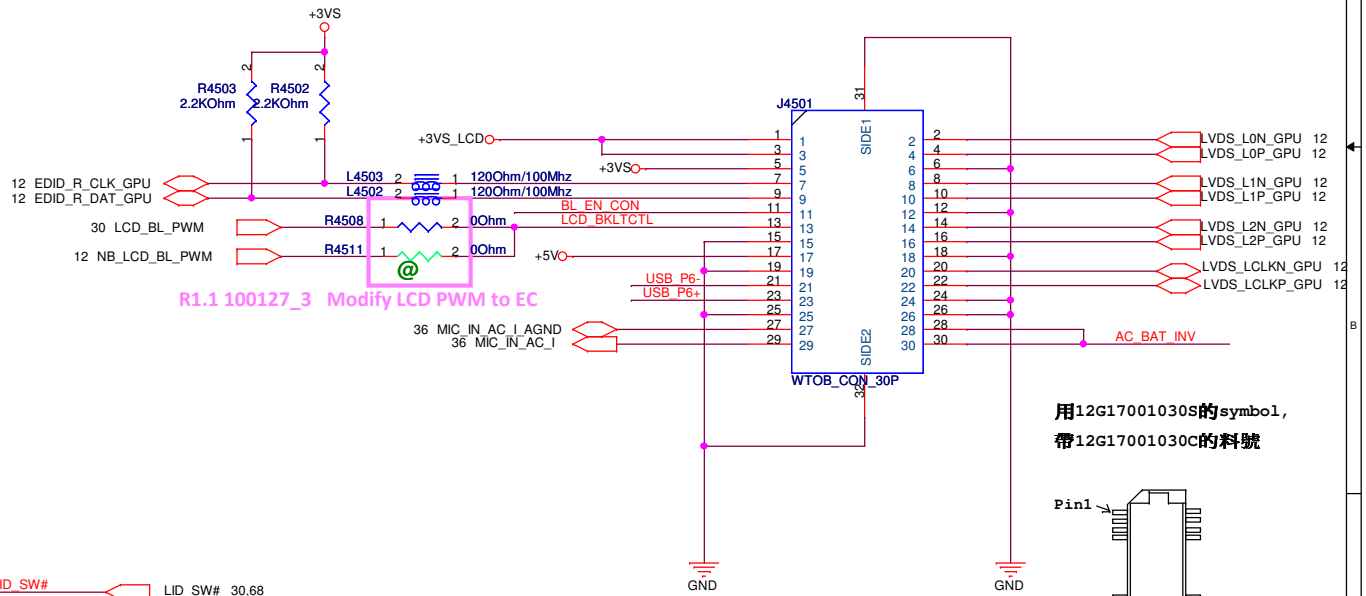




R1.1 100202_1 Add 100uf/25V Fix Noise

CAMERA & MIC

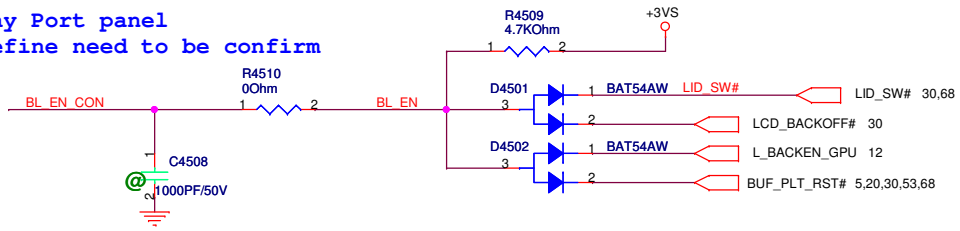




R1.1 100127_3 Modify LCD PWM to EC

用12G17001030S的symbol,
帶12G17001030C的料號

Display Port panel pin define need to be confirm



ASUSTeK COMPUTER INC. NB4	Title : CRT_LCD Panel	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 45 of 99	

ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 46 of 99		

Main Board

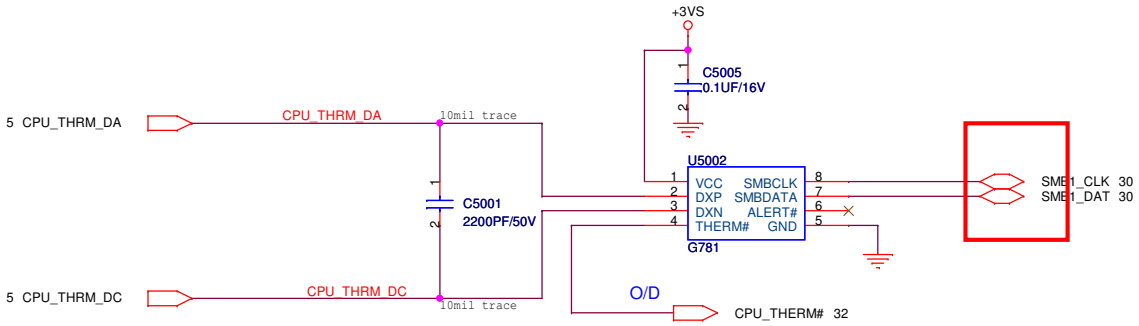
ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 47 of 99	

Title :	TV_HDMI
ASUSTeK COMPUTER INC. NB4	Engineer: Vincent_Chiang
Size: Custom	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 48 of 99

Main Board

ASUSTeK COMPUTER INC. NB4	Title : TV_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 49 of 99	

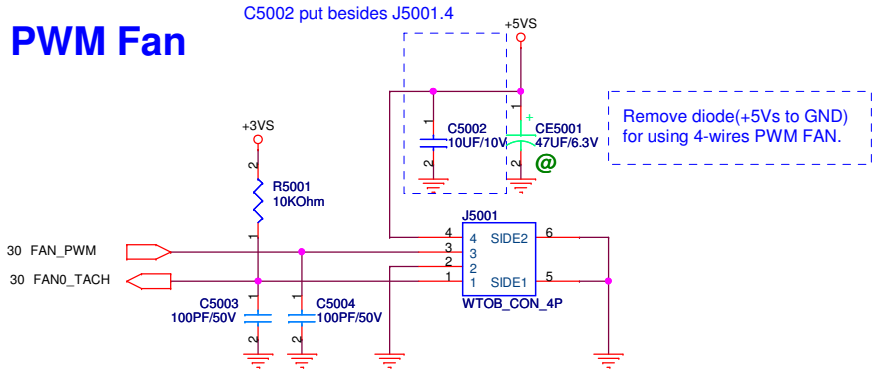
CPU Thermal Sensor



SMBUS addr=1001100x (98)

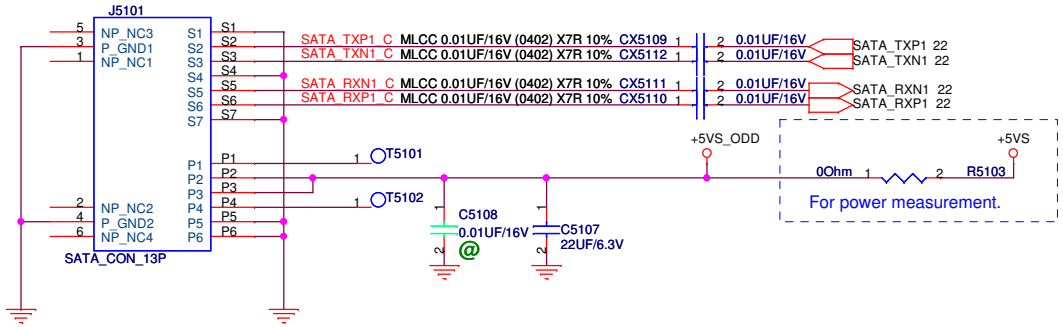
U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

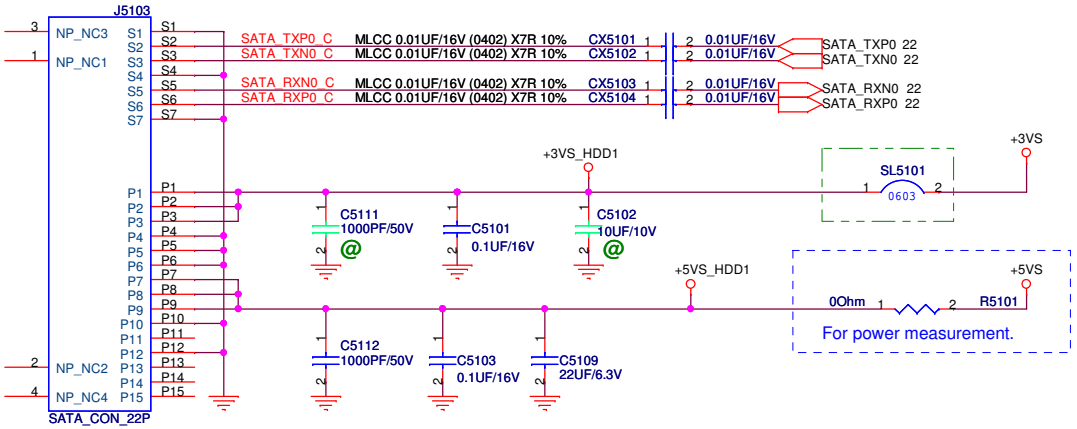


Title : FAN_Fan & Sensor		
ASUSTeK COMPUTER INC. NB4	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 50 of 99	

ODD



HDD (1st)



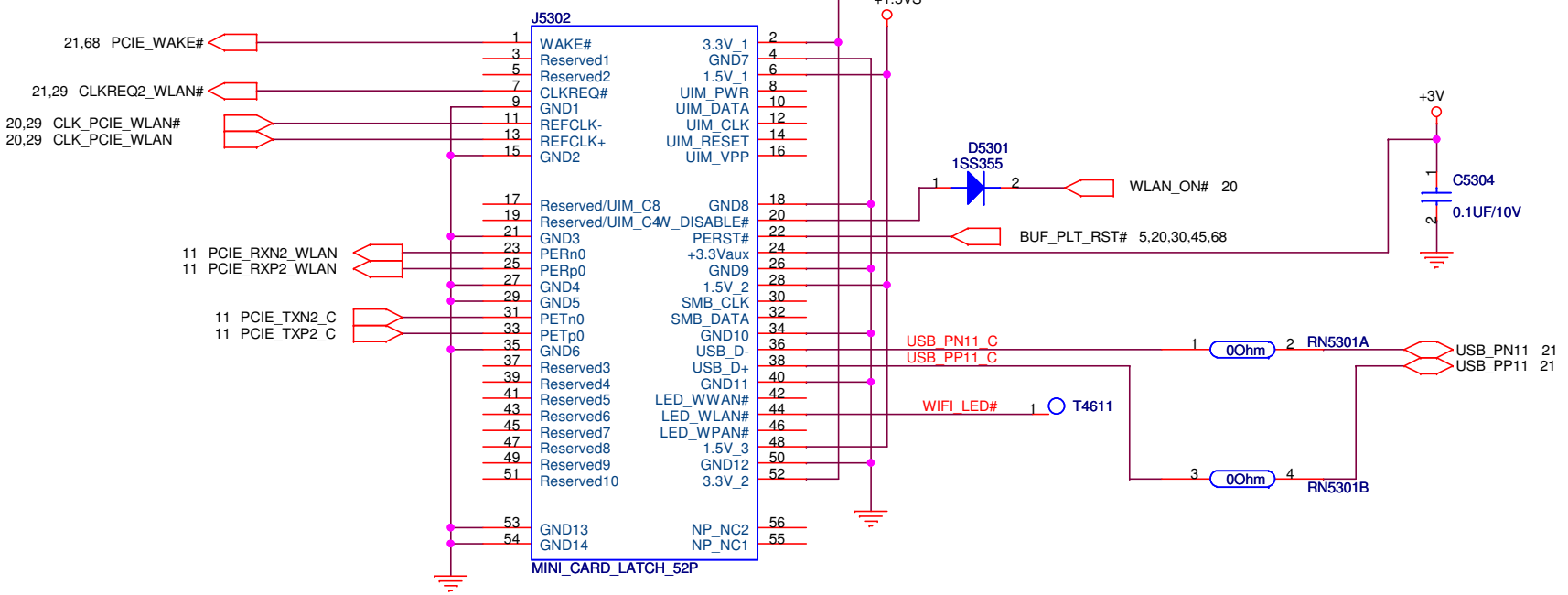
ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 51 of 99	

USB ports

ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *2	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 52 of 99	

Suppport wake from S3 only

使用12G03010052F symbol

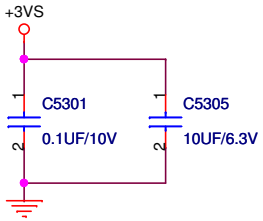


WLAN

WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

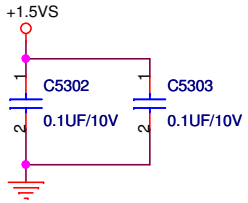
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

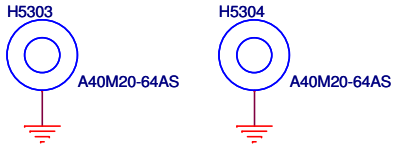


WLAN nuts:

Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.



ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 53 of 99	

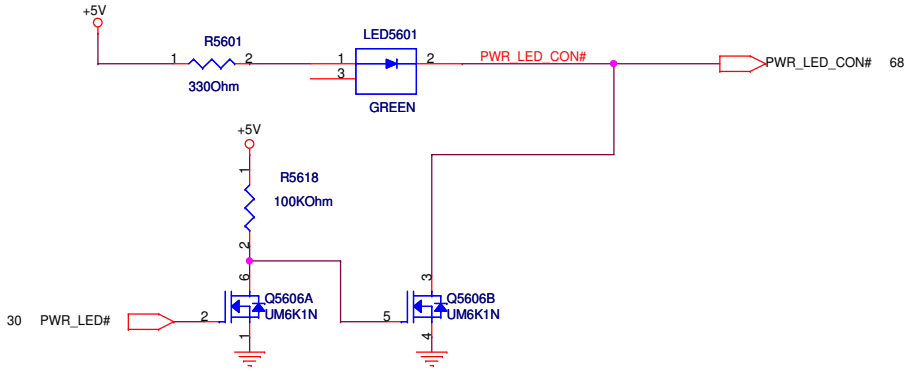
Main Board

ASUSTeK COMPUTER INC. NB4	Title : BAR_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 54 of 99	

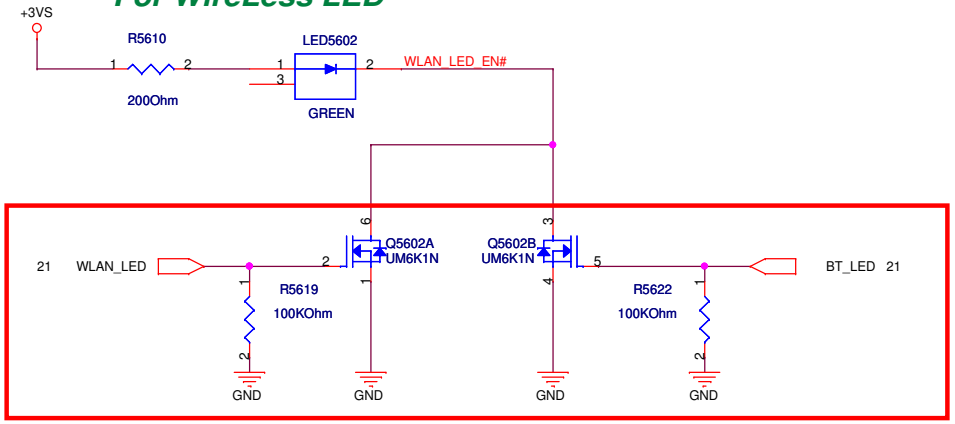
Main Board

ASUSTeK COMPUTER INC. NB4	Title : SIO_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 55 of 99	

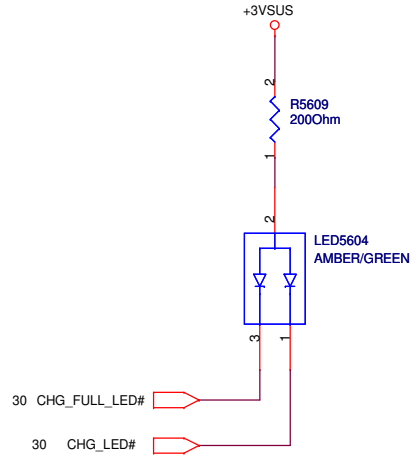
For POWER LED



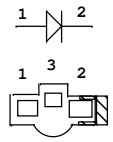
For WireLess LED



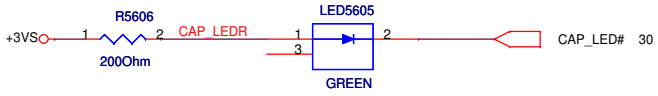
Charge LED



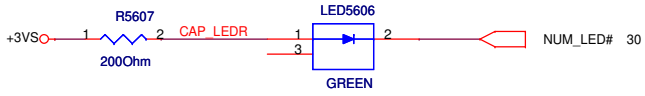
Side Light LED symbol



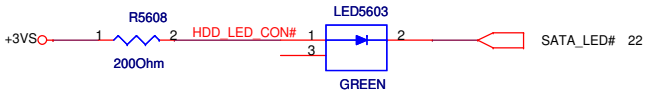
Cap. Lock LED



for Num Lock



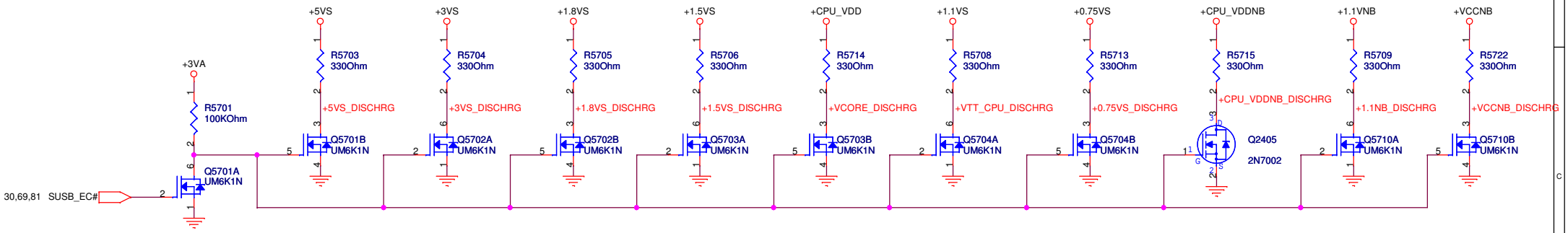
HDD LED

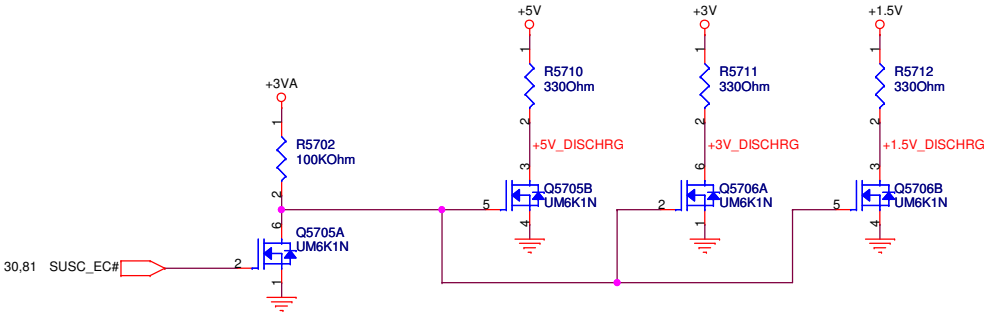


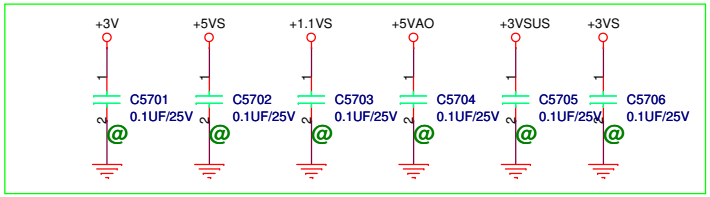
ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 56 of 99	

Remove +2.5Vs is for ATI GFX

Main Board







ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 57 of 99	

ASUSTeK COMPUTER INC. NB4	Title : PCI_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 58 of 99	

Main Board

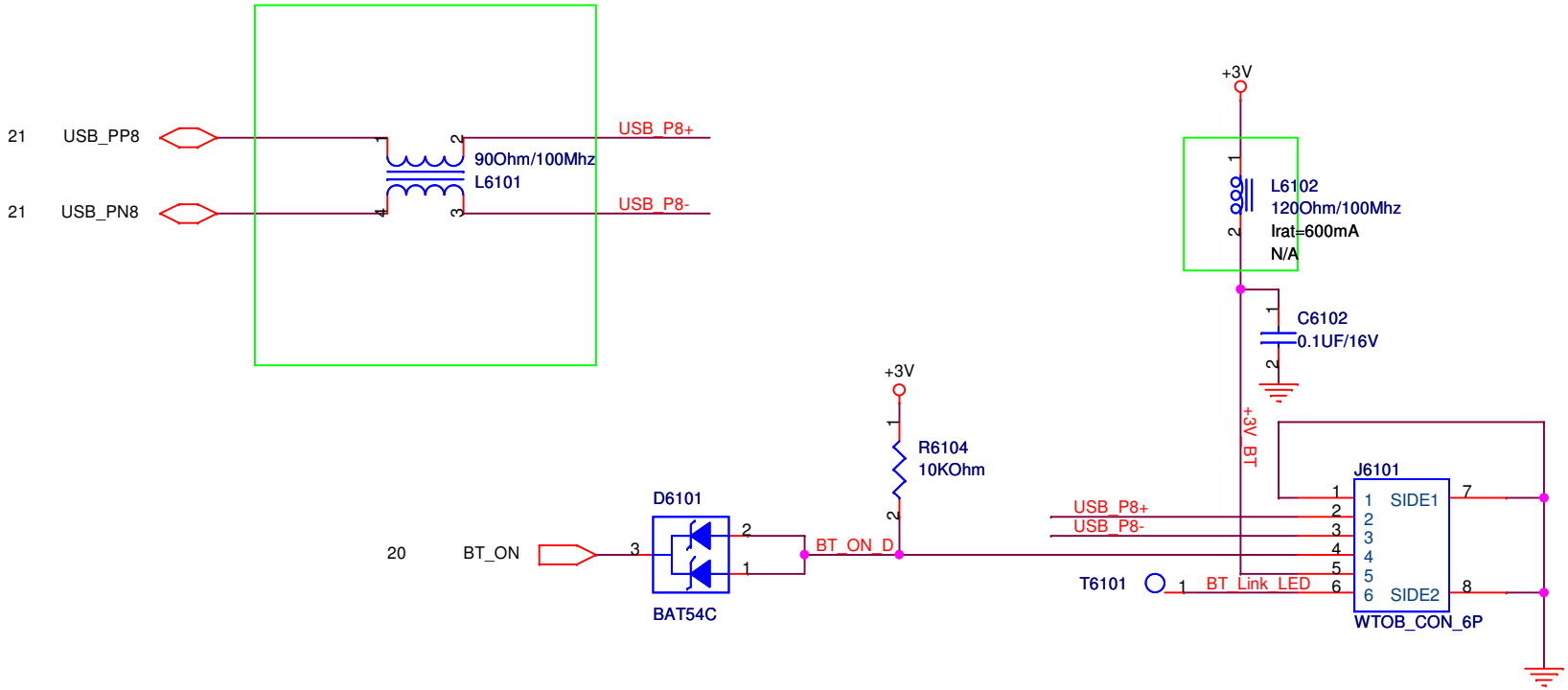
ASUSTeK COMPUTER INC. NB4	Title : DJ_****	
	Engineer: Vincent_Chiang	
Size: C	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 59 of 99	

POWER GOOD DETECTER

<Variant Name>

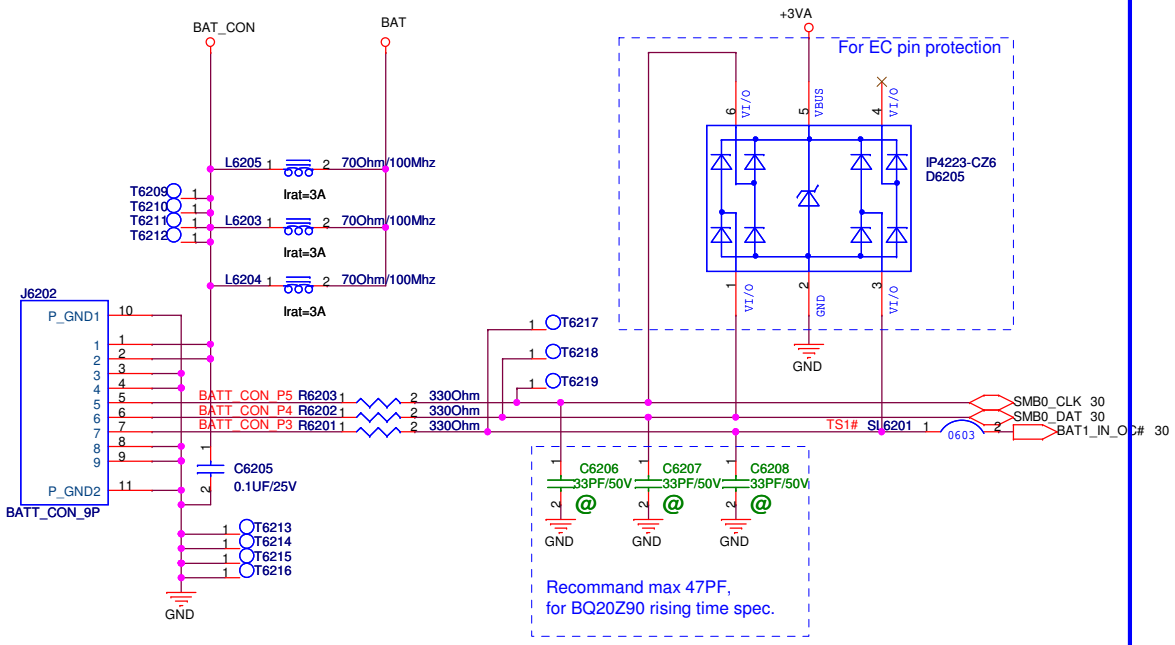
ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 60 of 99	

BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 61 of 99	

Battery Connector



Total count: 11 pcs

ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 62 of 99	

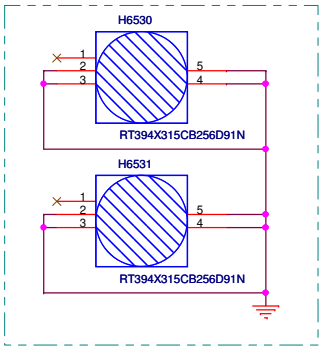
Main Board

ASUSTeK COMPUTER INC. NB4	Title : FP_FP Conn	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 63 of 99	

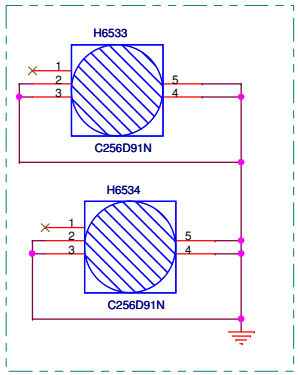
Title :	TUN_TV Tuner
ASUSTeK COMPUTER INC. NB4	Engineer: Vincent_Chiang
Size: Custom	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 64 of 99

Main Board

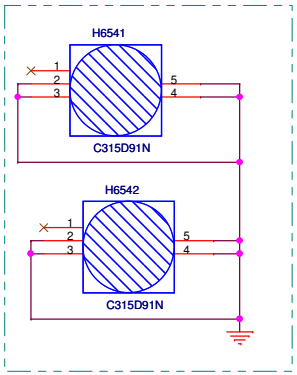
Screw Hole A



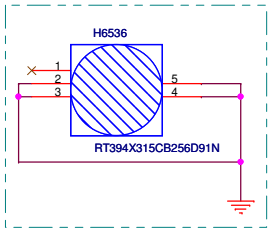
Screw Hole B



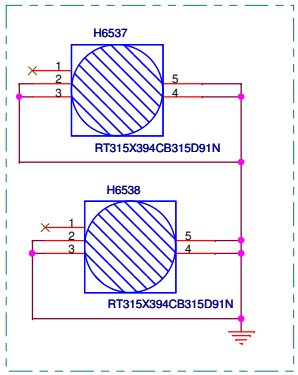
Screw Hole I



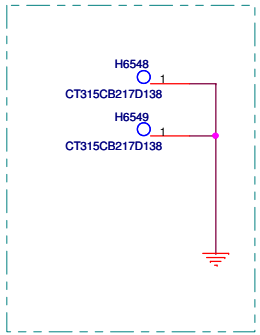
Screw Hole C



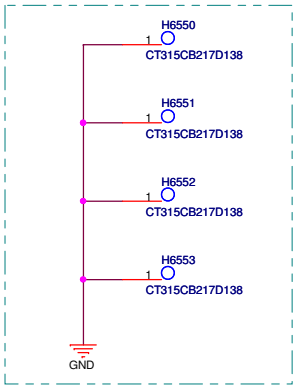
Screw Hole F



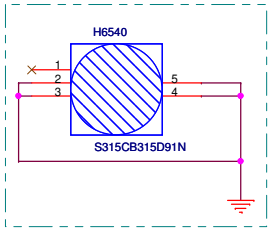
Screw Hole E



Screw from k52JR

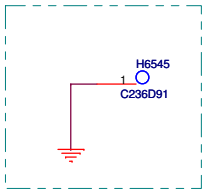


Screw Hole H



Tooling Hole K

Screw Hole O



Tooling Hole L

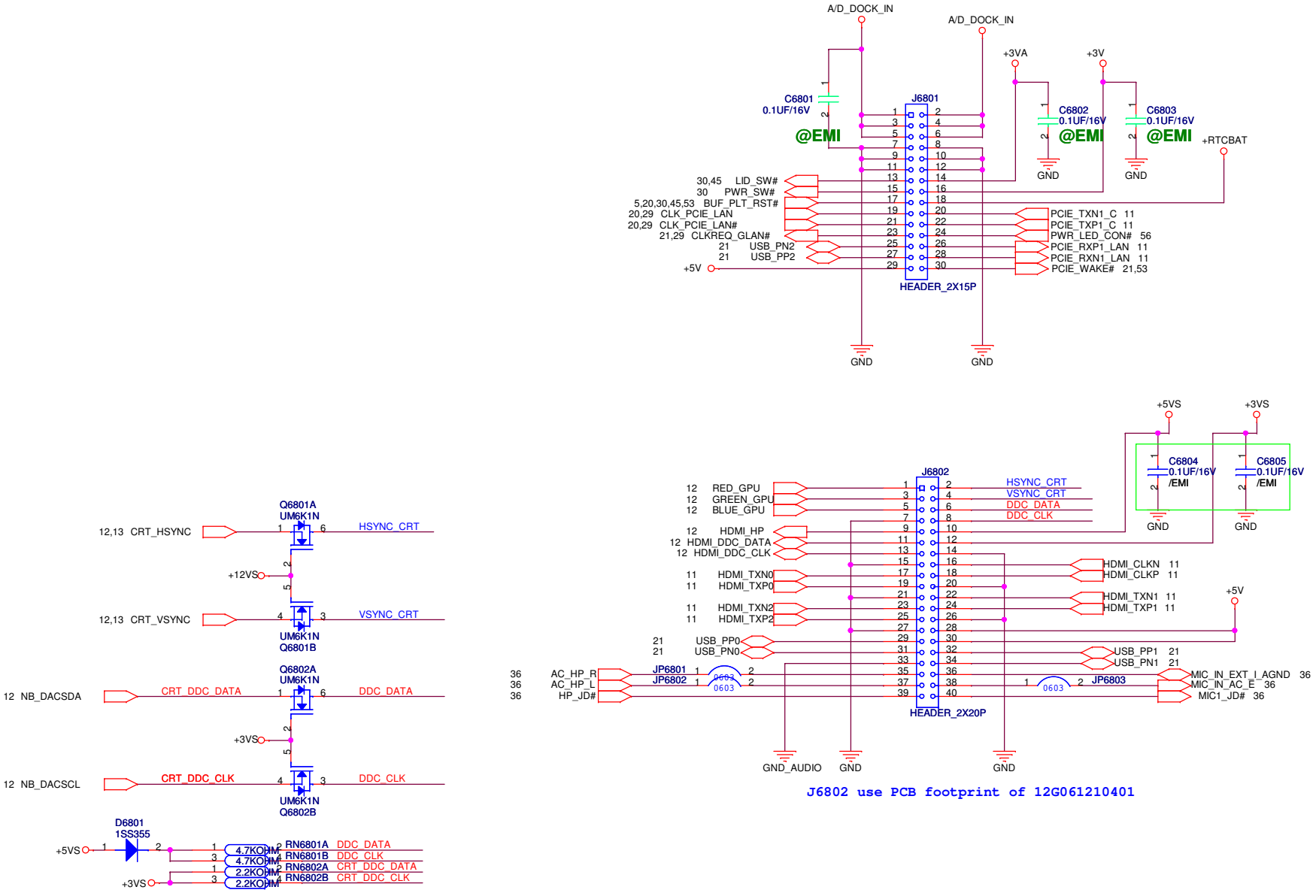
ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 65 of 99	

Title :	ESA_ESATA
ASUSTeK COMPUTER INC. NB4	Engineer: Vincent_Chiang
Size: Custom	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 66 of 99

PCH XDP

BRAIDWOOD (ONFI)

ASUSTeK COMPUTER INC. NB4	Title : PCH_XDP, ONFI	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 67 of 99	



J6802 use PCB footprint of 12G061210401

ASUSTeK COMPUTER INC. NB4

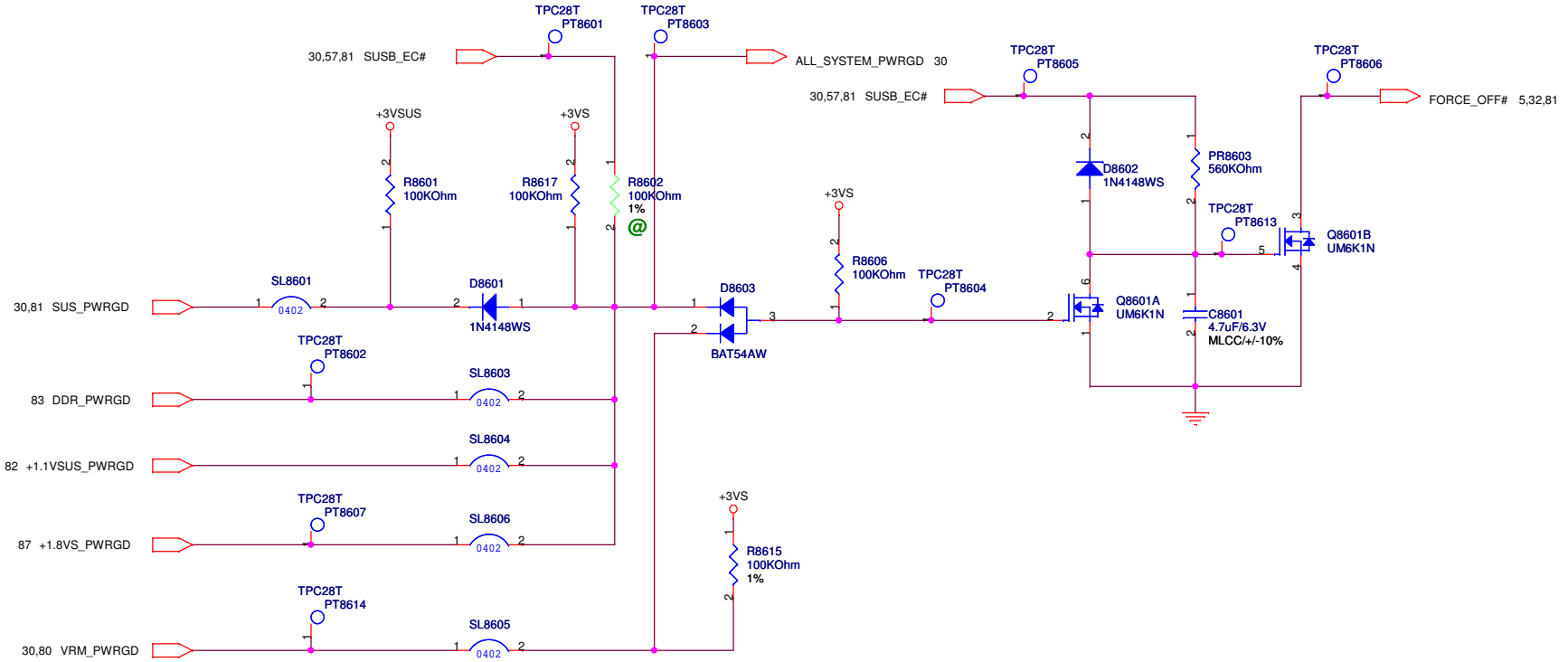
Title : IO Connector

Engineer: Vincent_Chiang

Size	Project Name	Rev
B	K52N	1.0

Date: Monday, February 08, 2010 Sheet 68 of 99

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC

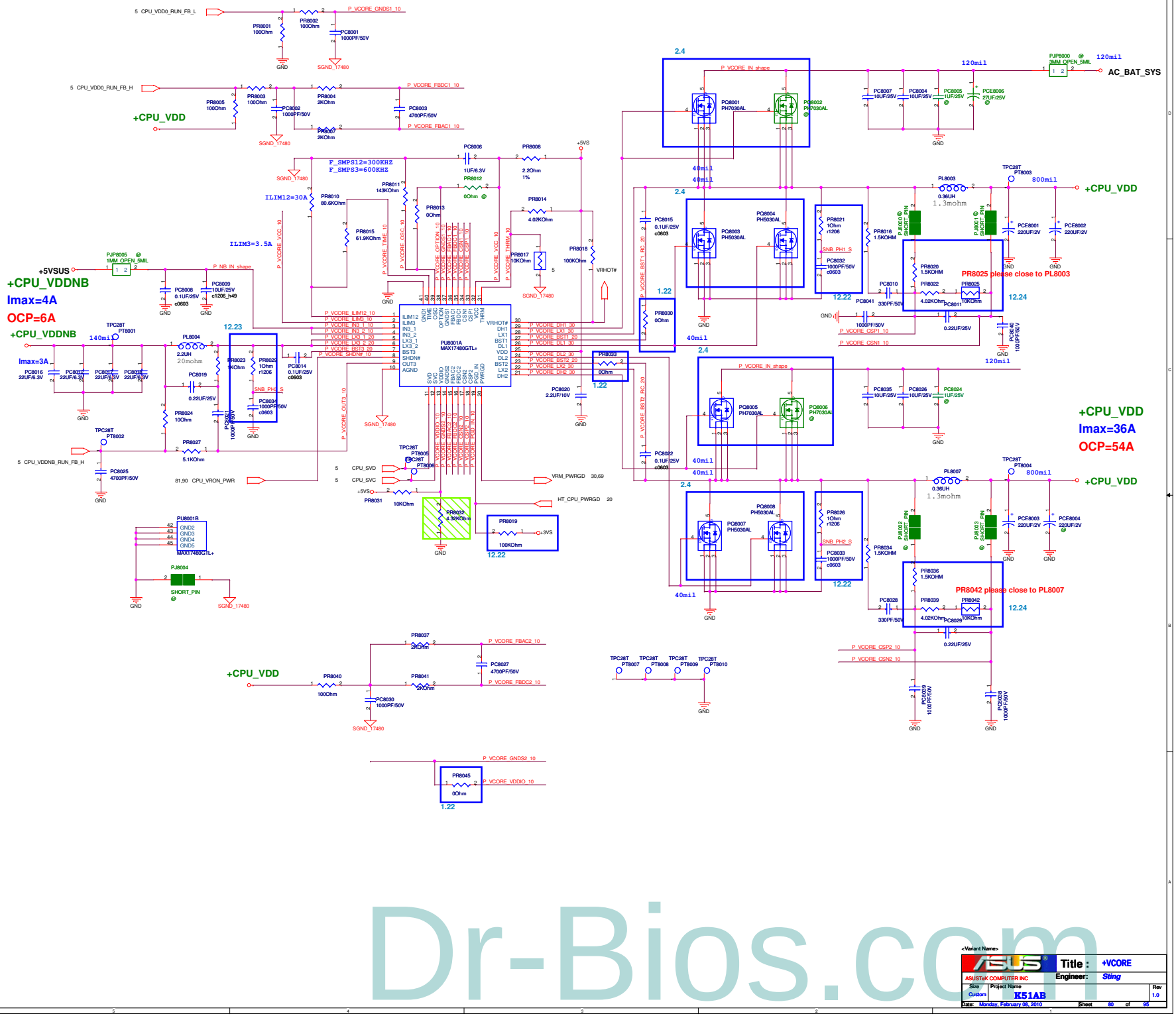
Title : GOOD_DETECTER

Engineer: Vincent_Chiang

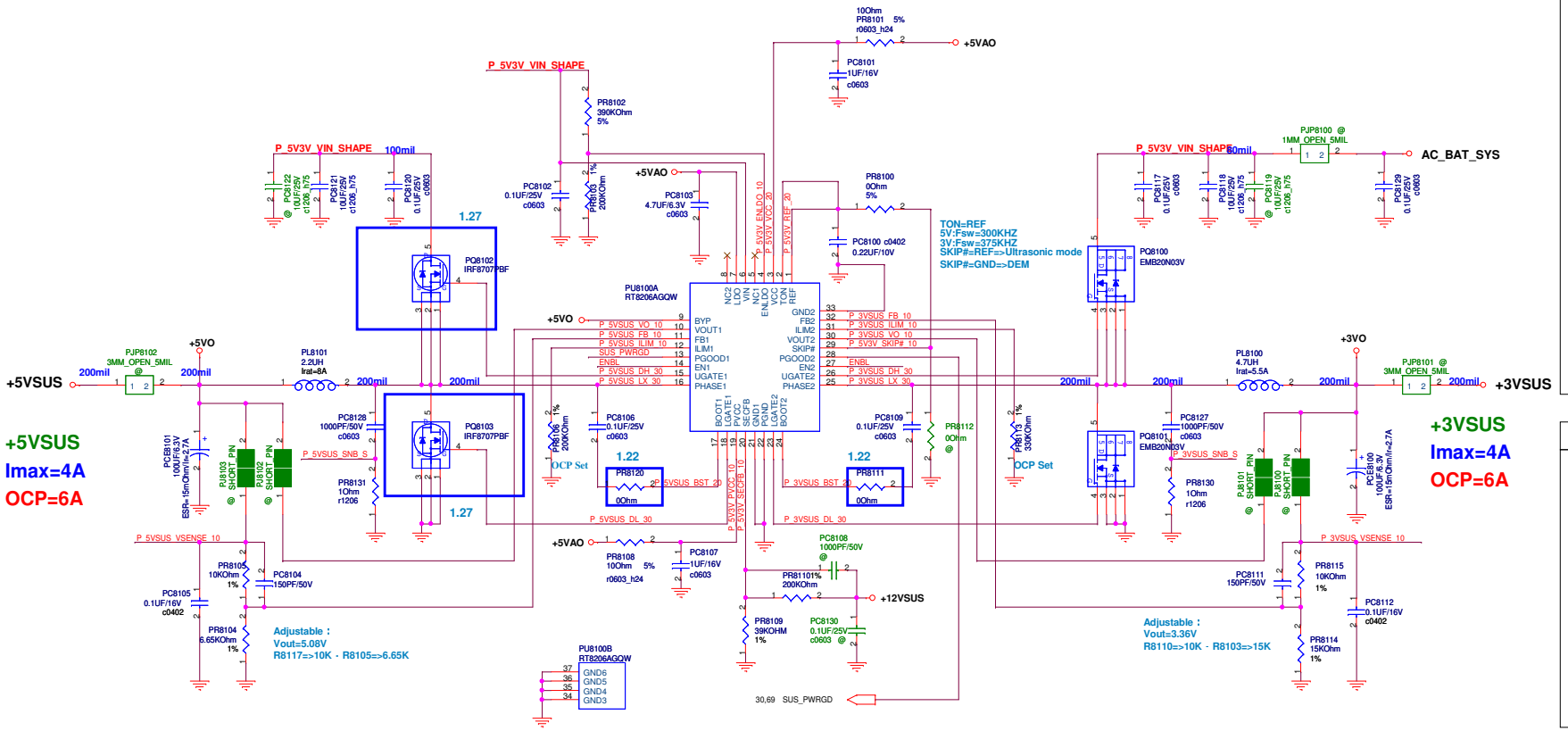
Size	Project Name	Rev
B		1.0

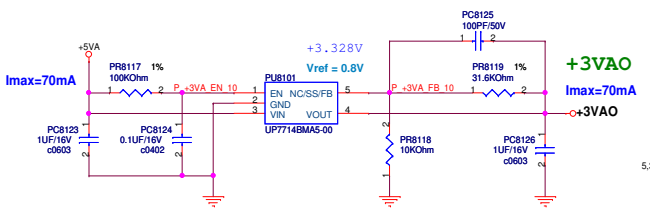
Date: Monday, February 08, 2010 Sheet 69 of 95

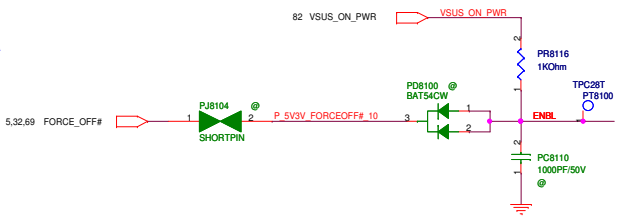
ASUSTeK COMPUTER INC. NB4	Title : VGA_MXM(2.1a)	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 70 of 99	

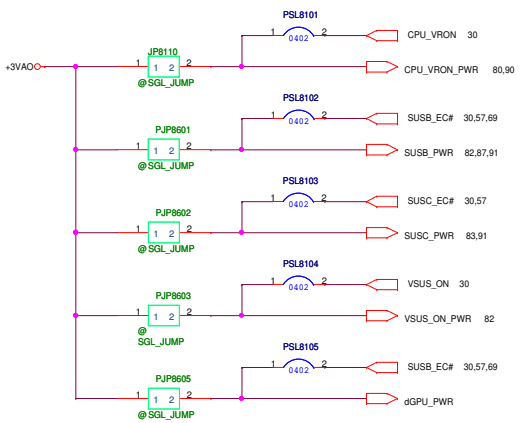

+CPU_VDDNB
Imax=4A
OCP=6A
+CPU_VDD
Imax=36A
OCP=54A
AC_BAT_SYS
+5VSUS
+CPU_VDD
PR8025 please close to PL8003
PR8042 please close to PL8007
F_SMPS12=300KHZ
F_SMPS3=600KHZ
ILIM12=30A
ILIM3=3.5A
PU8001A MAX17480GTL+
PU8001B MAX17480GTL+
PJ8004 SHORT_PIN
Title : +VCORE
ASUSTeK COMPUTER INC
Engineer: Sting
Project Name K51AB
Rev 1.0
Monday, February 08, 2010
Sheet 80 of 85

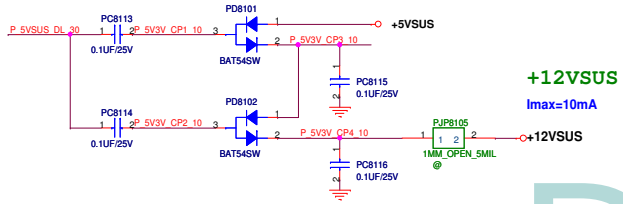
+5VSUS / +3VSUS POWER SUPPLY

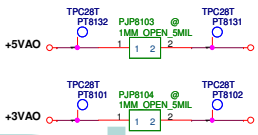












Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.96A
2. Ripple Current:
   Irip=2.61A
3. Ripple Voltage:
   ESR/1=15mohm
   V=39.15mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm
5. MOSFET Spec:
   H-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)
   L-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.96A
2. Ripple Current:
   Irip=1.55A
3. Ripple Voltage:
   ESR/1=15mohm
   V=23.25mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm

Controller

+5VSUS:

1. Voltage & Current:
   +5VSUS: 5V / 4A
2. Frequency:
   F=300KHZ
3. OCP:
   Set PR8106=357 Kohm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Soft start time:
   The Soft Start duration is 2ms
5. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.25 A

+3.VSUS

1. Voltage&Current:
   +3VSUS: 3.3V / 4A
2. Frequency:
   F=375KHZ
3. OCP:
   Set PR8113=357KOhm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.165 A

<Variant Name>

Title : POWER_SYSTEM

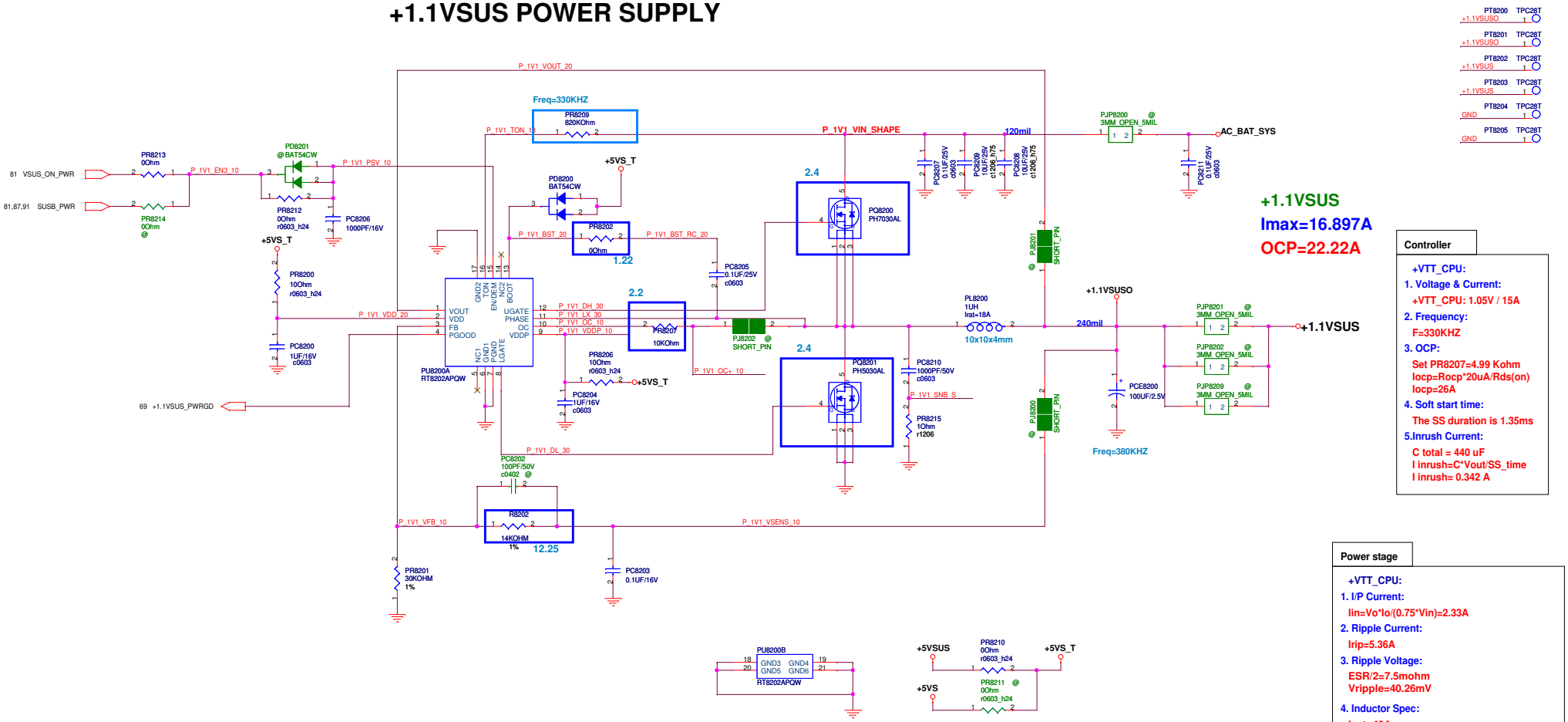
ASUSTeK COMPUTER INC. NB

Engineer: Matt_Wang

Size: Custom | Project Name: Design_IP | Rev: 1.0

Date: Monday, February 08, 2010 | Sheet 81 of 95

+1.1VSUS POWER SUPPLY



Controller

+VTT_CPU:

1. Voltage & Current:
   +VTT_CPU: 1.05V / 15A
2. Frequency:
   F=330KHZ
3. OCP:
   Set PR8207=4.99 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26A
4. Soft start time:
   The SS duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.342 A

Power stage

+VTT_CPU:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.33A
2. Ripple Current:
   Irip=5.36A
3. Ripple Voltage:
   ESR/2=7.5mohm
   Vripple=40.26mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.6mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

<Variant Name>

ASUSTeK COMPUTER INC. NB

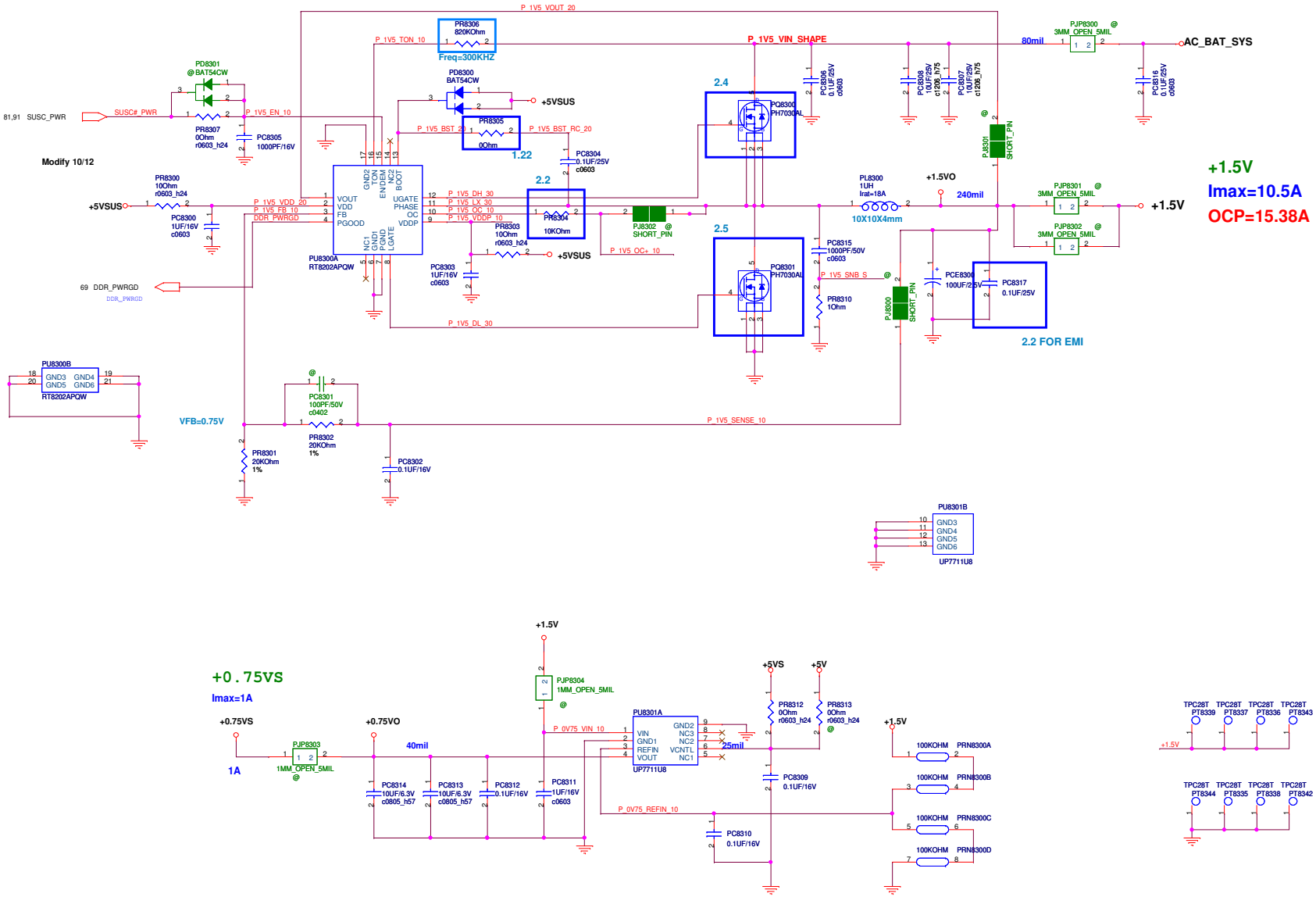
Title : POWER_I/O_+VCCP

Engineer: Matt_Wang

Size	Project Name	Rev
Custom	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 82 of 95

+1.5V & +0.75VS POWER SUPPLY



Power stage

DDR III:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.22A
2. Ripple Current:
   Irip=4.62A
3. Ripple Voltage:
   ESR/1=15mohm
   V=69.3mV
4. Inductor Spec:
   Isat=12.7A
   Idc=9.5A
   DCR=8.5mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

Controller

DDR III:

1. Voltage & Current:
   +1.5V: 1.5V / 10A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8302=12 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=14.3A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.244 A

1. Voltage & Current:
   +0.75V: 0.75V / 1A

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR

Engineer: Matt_Wang

Size	Project Name	Rev
Custom	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 83 of 95

ASUSTek Computer INC.	Title :	
	Engineer:	
Size: A3	Project Name: Oemga	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 84 of 95	

GPU NVDD POWER SUPPLY

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : POWER_I/O_NVDD	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 85 of 96	

<variant_name><Variant Name></variant_name>

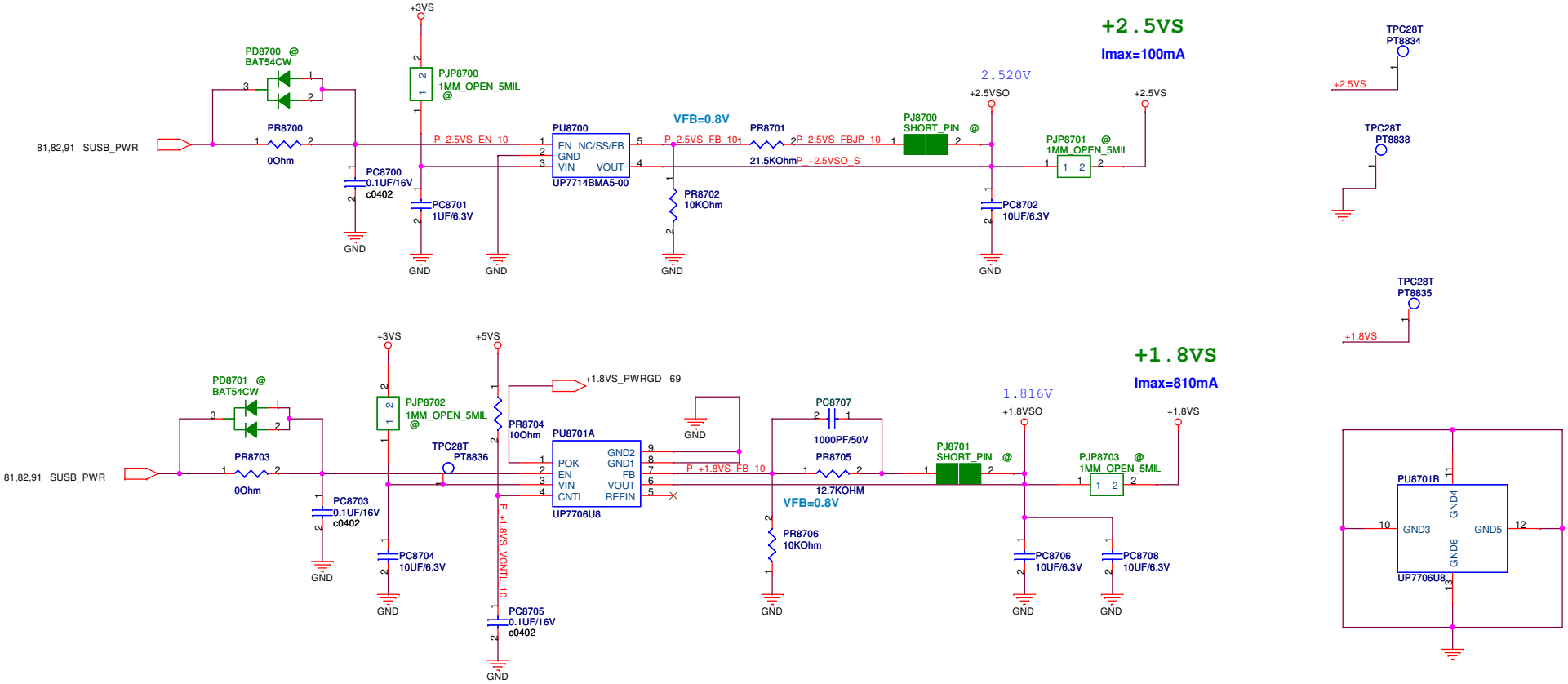
Title : Block Diagram

ASUSTeK COMPUTER INC. NB6

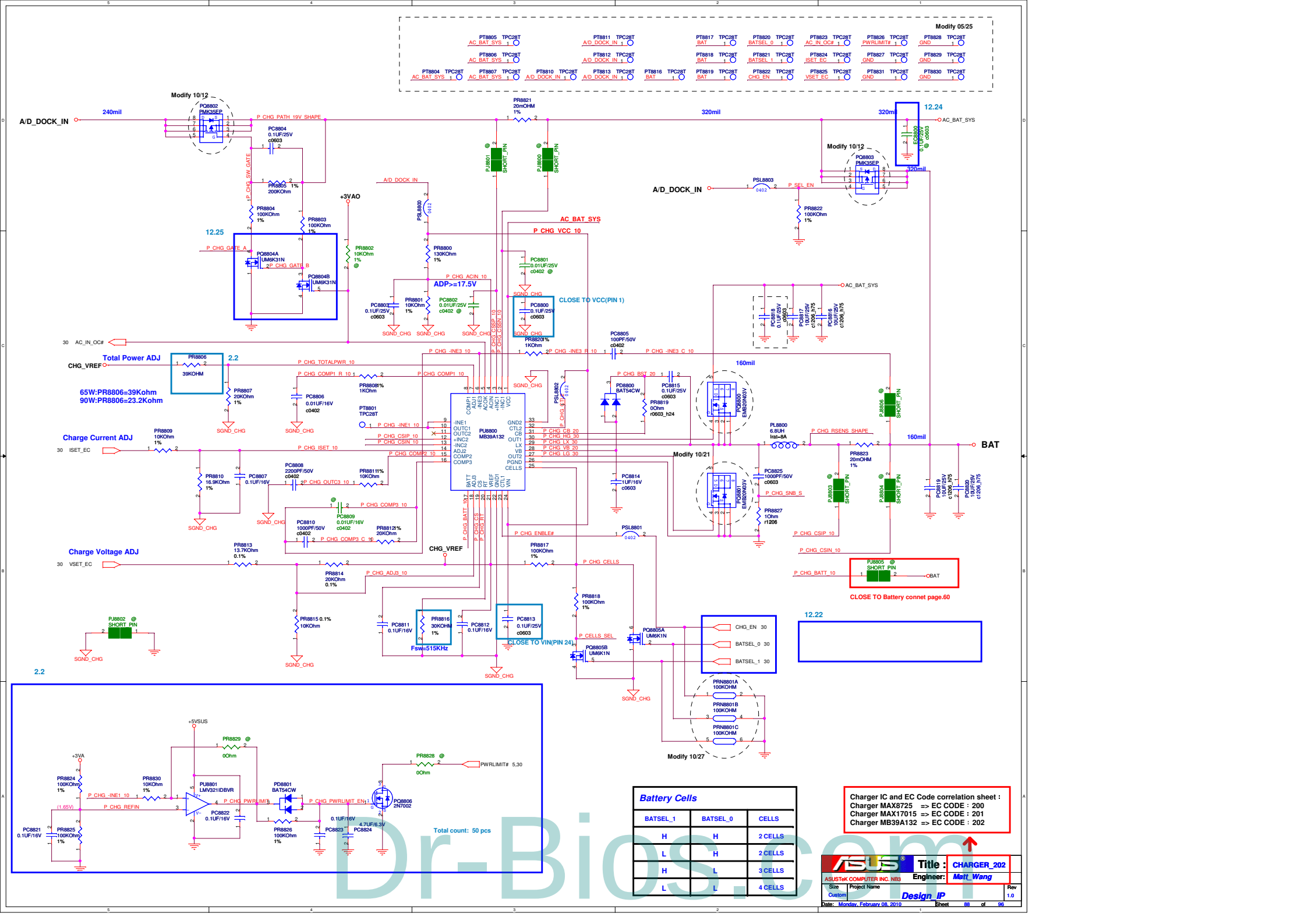
Engineer: Jeff Kao

Size	Project Name	Rev
A	K42Dr	R1.0

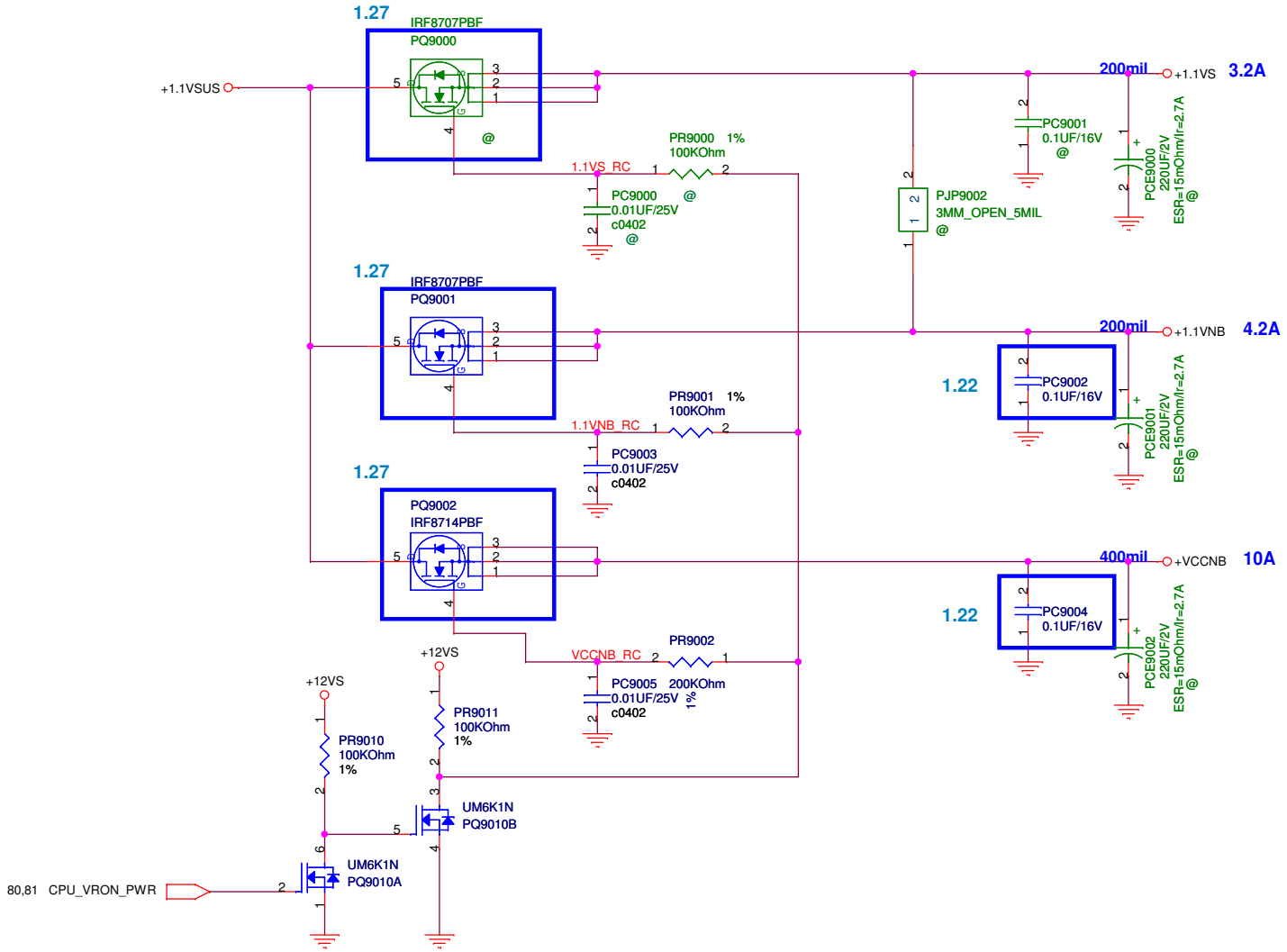
Date: Monday, February 08, 2010 Sheet 86 of 95



ASUSTek Computer INC.	Title :	
	Engineer:	
Size: A3	Project Name: Oemga	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 87 of 95	

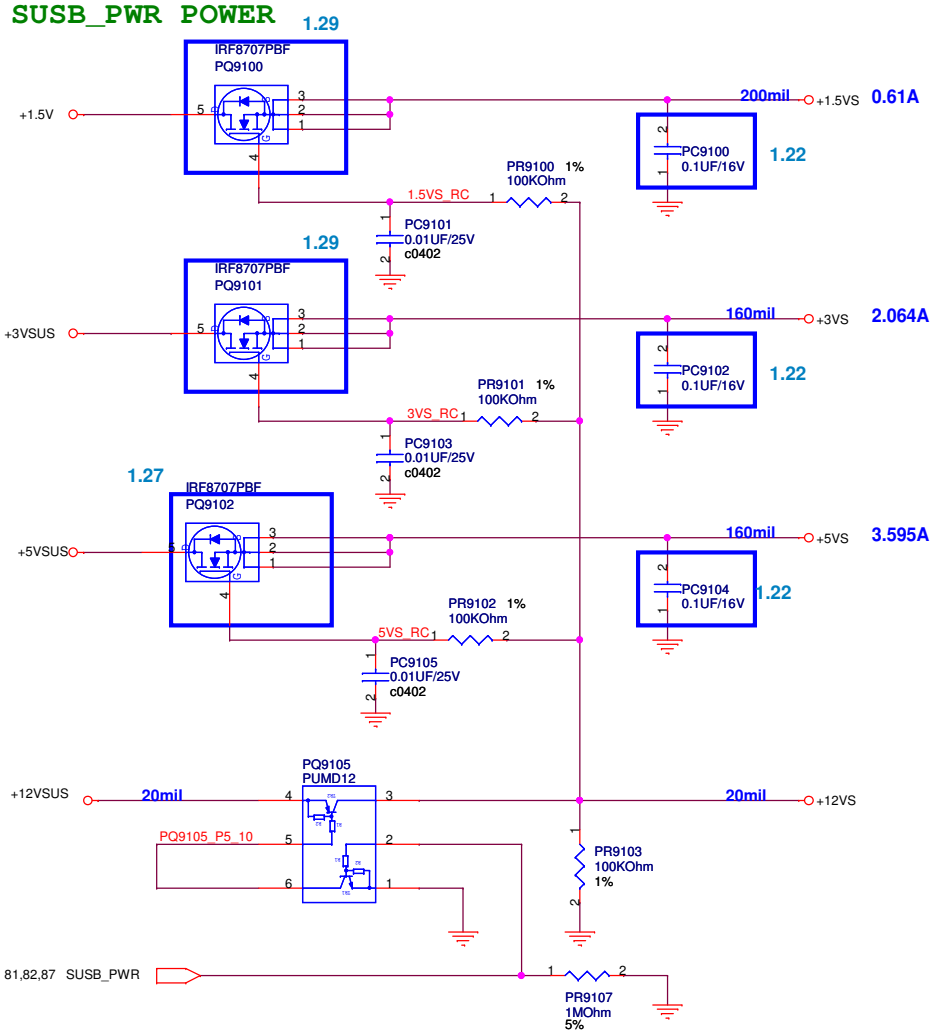

Modify 05/25
PT8805 TPC28T AC_BAT_SYS
PT8806 TPC28T AC_BAT_SYS
PT8804 TPC28T AC_BAT_SYS
PT8807 TPC28T AC_BAT_SYS
PT8811 TPC28T A/D_DOCK_IN
PT8812 TPC28T A/D_DOCK_IN
PT8810 TPC28T A/D_DOCK_IN
PT8813 TPC28T A/D_DOCK_IN
PT8816 TPC28T BAT
PT8817 TPC28T BAT
PT8818 TPC28T BAT
PT8819 TPC28T BAT
PT8820 TPC28T BATSEL_0
PT8821 TPC28T BATSEL_1
PT8822 TPC28T CHG_EN
PT8823 TPC28T AC_IN_OC#
PT8824 TPC28T ISET_EC
PT8825 TPC28T VSET_EC
PT8826 TPC28T PWRLIMIT#
PT8827 TPC28T GND
PT8831 TPC28T GND
PT8828 TPC28T GND
PT8829 TPC28T GND
PT8830 TPC28T GND
A/D_DOCK_IN
240mil
Modify 10/12
PQ8802 PMK35EP
P_CHG_PATH_19V_SHAPE
PC8804 0.1UF/25V c0603
P_CHG_SW_GATE
PR8805 200KOhm
PR8804 100KOhm 1%
PR8803 100KOhm 1%
+3VAO
12.25
P_CHG_GATE_A
PQ8804A UM6K31N
P_CHG_GATE_B
PQ8804B UM6K31N
PR8802 10KOhm 1% @
PSL8800 0402
PR8800 130KOhm 1%
P_CHG_ACIN_10
ADP>=17.5V
PC8803 0.1UF/25V c0603
PR8801 10KOhm 1%
PC8802 0.01UF/25V c0402 @
SGND_CHG
P_CHG_CSSP_10
P_CHG_CSSN_10
PR8821 20mOHM 1%
PJ8801 @ SHORT_PIN
PJ8800 @ SHORT_PIN
AC_BAT_SYS
P_CHG_VCC_10
PC8801 0.01UF/25V c0402 @
PC8800 0.1UF/25V c0603
CLOSE TO VCC(PIN 1)
PR8820 1% 1KOhm
320mil
12.24
EC8800 0.1UF/25V c0603
Modify 10/12
PQ8803 PMK35EP
PSL8803 0402
P_SEL_EN
PR8822 100KOhm 1%
PC8818 0.1UF/25V c0603
PC8817 10UF/25V c1206_h75
PC8816 10UF/25V c1206_h75
30 AC_IN_OC#
Total Power ADJ
CHG_VREF
PR8806 39KOHM
2.2
P_CHG_TOTALPWR_10
65W:PR8806=39Kohm
90W:PR8806=23.2Kohm
PR8807 20KOhm 1%
P_CHG_COMP1_R_10
PR8808 1% 1KOhm
P_CHG_COMP1_10
PC8806 0.01UF/16V c0402
PT8801 TPC28T
P_CHG_-INE3_10
P_CHG_-INE3_R_10
PC8805 100PF/50V c0402
P_CHG_-INE3_C_10
160mil
PD8800 BAT54CW
PC8815 0.1UF/25V c0603
PR8819 0Ohm c0603_h24
PQ8800 EMB20N03V
PJ8806 @ SHORT_PIN
Charge Current ADJ
30 ISET_EC
PR8809 10KOhm 1%
P_CHG_ISET_10
PR8810 16.9KOhm 1%
PC8807 0.1UF/16V
PC8808 2200PF/50V c0402
P_CHG_OUTC3_10
PR8811 1% 10KOhm
P_CHG_COMP2_10
PC8809 0.01UF/16V c0402 @
P_CHG_COMP3_10
PC8810 1000PF/50V c0402
P_CHG_COMP3_C_10
PR8812 1% 20KOhm
PU8800 MB39A132
P_CHG_-INE1_10
P_CHG_CSIP_10
P_CHG_CSIN_10
P_CHG_CB_20
P_CHG_HG_30
P_CHG_LX_30
P_CHG_VB_20
P_CHG_LG_30
P_CHG_BATT_10
P_CHG_CHG_S
P_CHG_RT
PC8814 1UF/16V c0603
Modify 10/21
PL8800 6.8UH Irat=8A
P_CHG_RSENS_SHAPE
160mil
BAT
PR8823 20mOHM 1%
PJ8803 @ SHORT_PIN
PJ8804 @ SHORT_PIN
PC8825 1000PF/50V c0603
PQ8801 EMB20N03V
P_CHG_SNB_S
PR8827 1Ohm r1206
P_CHG_CSIP_10
P_CHG_CSIN_10
P_CHG_BATT_10
PJ8805 @ SHORT_PIN
OBAT
CLOSE TO Battery connet page.60
PC8820 10UF/25V c1206_h75
Charge Voltage ADJ
30 VSET_EC
PR8813 13.7KOhm 0.1%
PR8814 20KOhm 0.1%
P_CHG_ADJ3_10
PR8815 0.1% 10KOhm
PJ8802 @ SHORT_PIN
SGND_CHG
PC8811 0.1UF/16V
PR8816 30KOHM 1%
Fsw=515KHz
PC8812 0.1UF/16V
PC8813 0.1UF/25V c0603
CLOSE TO VIN(PIN 24)
CHG_VREF
PR8817 100KOhm 1%
P_CHG_CELLS
PR8818 100KOhm 1%
P_CELLS_SEL
PQ8805A UM6K1N
PQ8805B UM6K1N
CHG_EN 30
BATSEL_0 30
BATSEL_1 30
12.22
PRN8801A 100KOHM
PRN8801B 100KOHM
PRN8801C 100KOHM
Modify 10/27
2.2
+5VSUS
PR8829 @ 0Ohm
+3VA
PR8824 100KOhm 1%
PR8830 10KOhm 1%
P_CHG_-INE1_10
(1.65V)
P_CHG_REFIN
PU8801 LMV321IDBVR
PC8822 0.1UF/16V
PR8825 100KOhm 1%
PC8821 0.1UF/16V
PD8801 BAT54CW
P_CHG_PWRLIMIT_5
P_CHG_PWRLIMIT_EN
PR8826 100KOhm 1%
PC8823 0.1UF/16V
PC8824 4.7UF/6.3V
PR8828 @ 0Ohm
PWRLIMIT# 5,30
PQ8806 2N7002
Total count: 50 pcs
Battery Cells
BATSEL_1 | BATSEL_0 | CELLS
H | H | 2 CELLS
L | H | 2 CELLS
H | L | 3 CELLS
L | L | 4 CELLS
Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202
ASUSTeK COMPUTER INC. NB3
Title : CHARGER_202
Engineer: Matt_Wang
Size: Custom
Project Name: Design_IP
Rev: 1.0
Date: Monday, February 08, 2010
Sheet 88 of 96
Dr-Bios.com

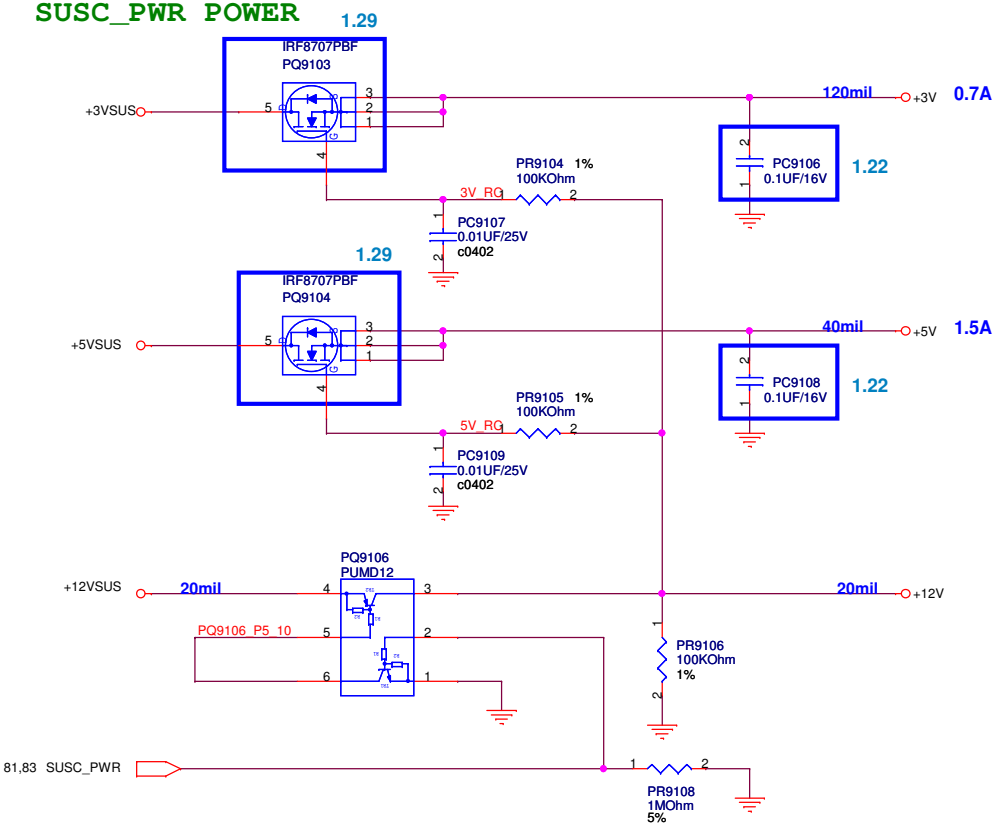
Title :	
ASUSTek Computer INC.	Engineer:
Size: Custom	Project Name: Oemga
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 89 of 95



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 90 of 95	





<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_LOAD SWITCH

Engineer: Matt_Wang

Size	Project Name	Rev
B	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 91 of 95

Title :	
ASUSTek Computer INC.	Engineer:
Size: Custom	Project Name: Oemga
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 92 of 95

AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,88
BAT	BAT	62,88

+3VAO	+3VAO	81,88
+5VA	+5VA	81
+3VA	+3VA	20,30,57,62,68,81,88
+5VAO	+5VAO	57,81
+5VO	+5VO	81
+5VSUS	+5VSUS	80,81,82,83,88,91
+5V	+5V	45,56,57,68,83,91
+5VS	+5VS	30,31,36,37,50,51,57,68,80,82,83,87,91
+3VO	+3VO	81
+3VSUS	+3VSUS	20,21,23,24,30,56,57,69,81,91
+3V	+3V	44,45,53,57,61,68,91
+3VS	+3VS	5,12,13,14,16,17,20,21,23,24,29,30,32,36,45,50,51,53,56,57,68,69,80,87,91
+12VSUS	+12VSUS	81,91
+12V	+12V	91
+12VS	+12VS	45,68,90,91
+1.8VO	+1.8VO	
+1.8VS	+1.8VS	12,13,14,23,57,87

+0.75VS	+0.75VS	16,17,57,83
+0.75VO	+0.75VO	83

+1.5V	+1.5V	4,5,6,16,17,18,57,83,91
+1.5VO	+1.5VO	83
+1.5VS	+1.5VS	5,53,57,91

+CPU_VDD	+CPU_VDD	6,57,80
+CPU_VDDNB	+CPU_VDDNB	6,57,80
+1.1VS	+1.1VS	3,4,23,57,90
+1.1VNB	+1.1VNB	11,12,13,14,57,90
+VCCNB	+VCCNB	14,57,90

A/D_DOCK_IN	A/D_DOCK_IN	68,88

<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Morris / Eric

Size	Project Name	Rev
C	K52Jr	2.0

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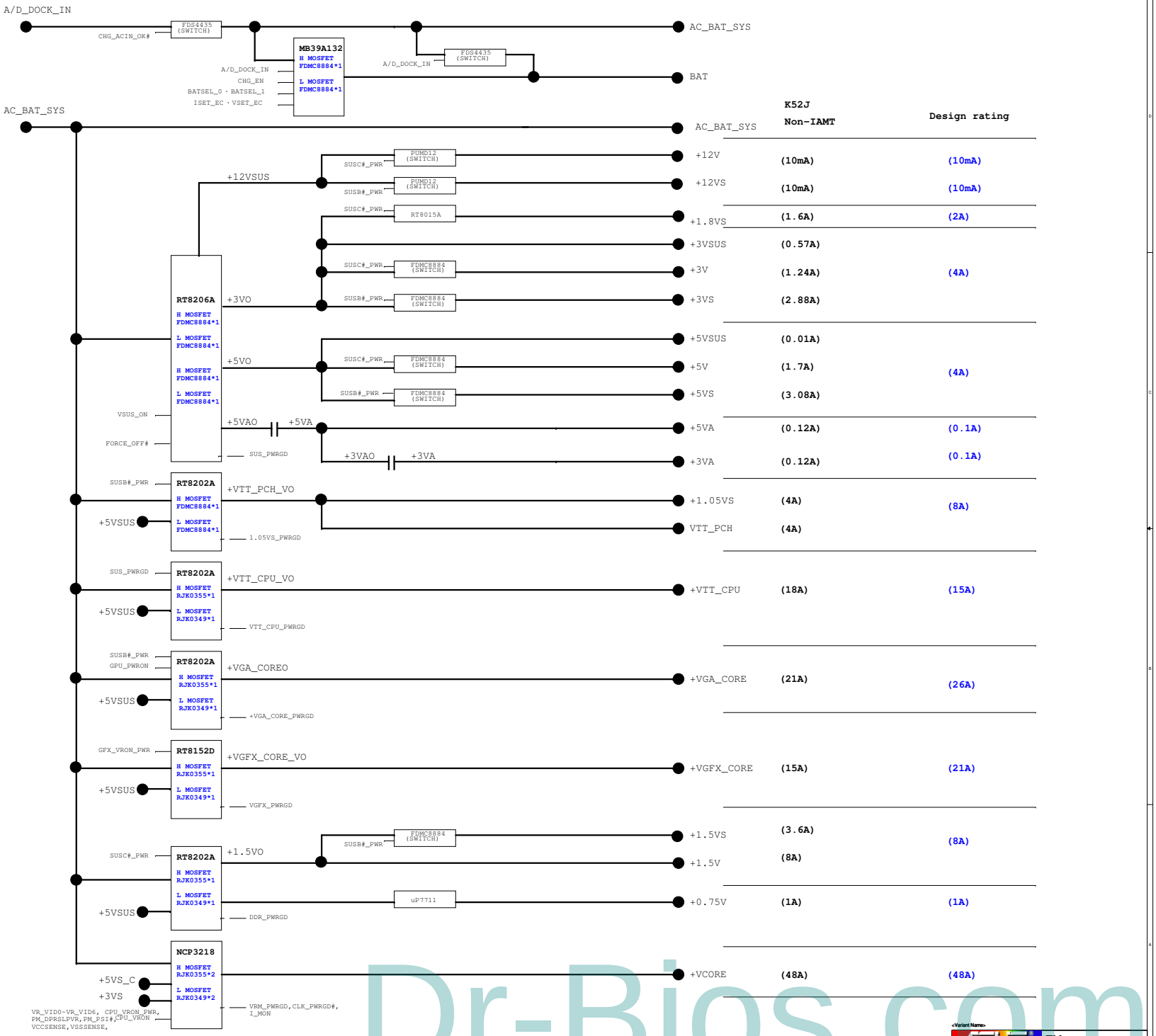

	K52J Non-IAMT	Design rating
AC_BAT_SYS		
+12V	(10mA)	(10mA)
+12VS	(10mA)	(10mA)
+1.8VS	(1.6A)	(2A)
+3VSUS	(0.57A)	
+3V	(1.24A)	(4A)
+3VS	(2.88A)	
+5VSUS	(0.01A)	
+5V	(1.7A)	(4A)
+5VS	(3.08A)	
+5VA	(0.12A)	(0.1A)
+3VA	(0.12A)	(0.1A)
+1.05VS	(4A)	(8A)
VTT_PCH	(4A)	
+VTT_CPU	(18A)	(15A)
+VGA_CORE	(21A)	(26A)
+VGFX_CORE	(15A)	(21A)
+1.5VS	(3.6A)	(8A)
+1.5V	(8A)	
+0.75V	(1A)	(1A)
+VCORE	(48A)	(48A)

R1.1 100128 Modify Page36/Page37 For Realtek Audio Chip
R1.1 100127_1 Change EDID CLK/DAT Circuit
R1.1 100127_2 Modify +1.1V_NB to +1.1VNB
R1.1 100127_3 Modify LCD PWM to EC
R1.1 100128_1 Support Battery (Battery Request)
R1.1 100129_1 Change +3VS to +5VS For Audio
R1.1 100202_1 Add 100uf/25V Fix Noise
R1.1 100202_2 EMI REQUEST
R1.1 100202_3 Add CLKGEN IN Circuit For SB800 (Change CLK for Page 29)

ASUSTeK COMPUTER INC. NB	Title : System History	
	Engineer:	
Size: C	Project Name: K52Jr	Rev
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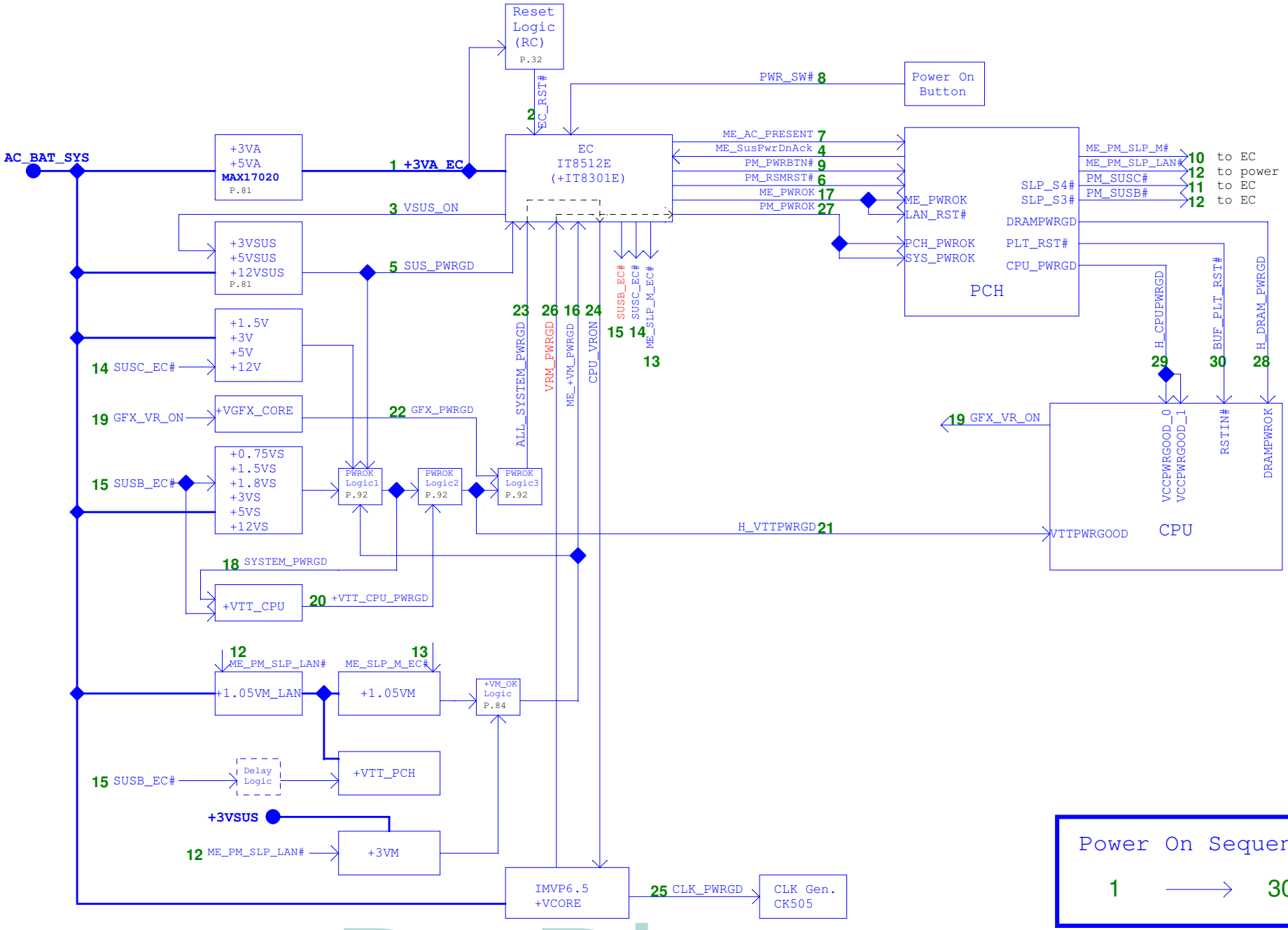
ASUSTeK COMPUTER INC. NB	Title : System History	
	Engineer:	
Size: C	Project Name: K52Jr	Rev
Date: Monday, February 08, 2010	Sheet 96 of 99	

AC-IN Mode

M52J Power On Sequence Diagram Rev. 0.31



Power On Sequence

1 → 30

ASUSTeK COMPUTER INC

Title : POWER SEQUENCE

Engineer: Leon

Size	Project Name	Rev
C	K52Jr	2.0

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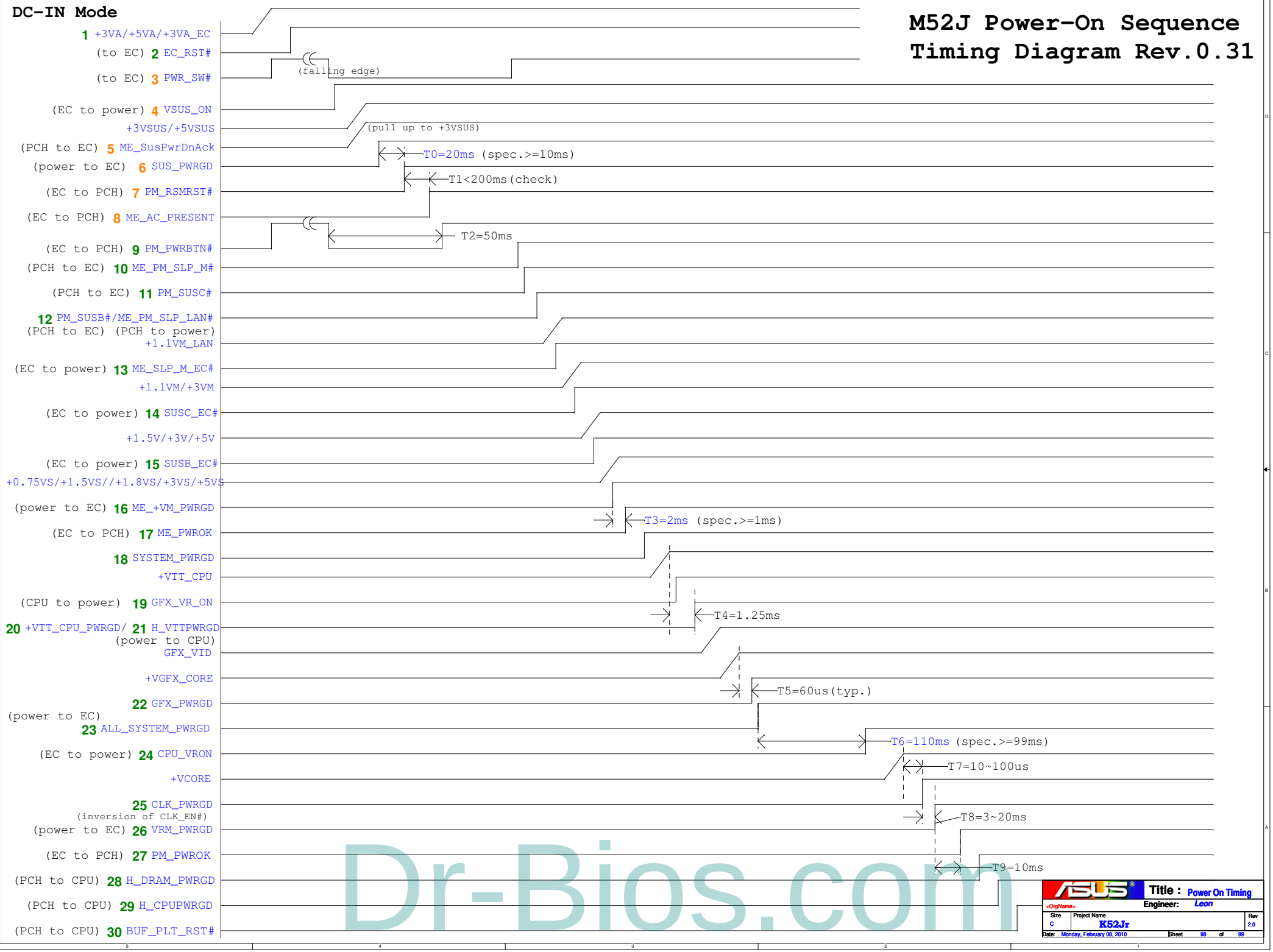
M52J Power-On Sequence Timing Diagram Rev.0.31

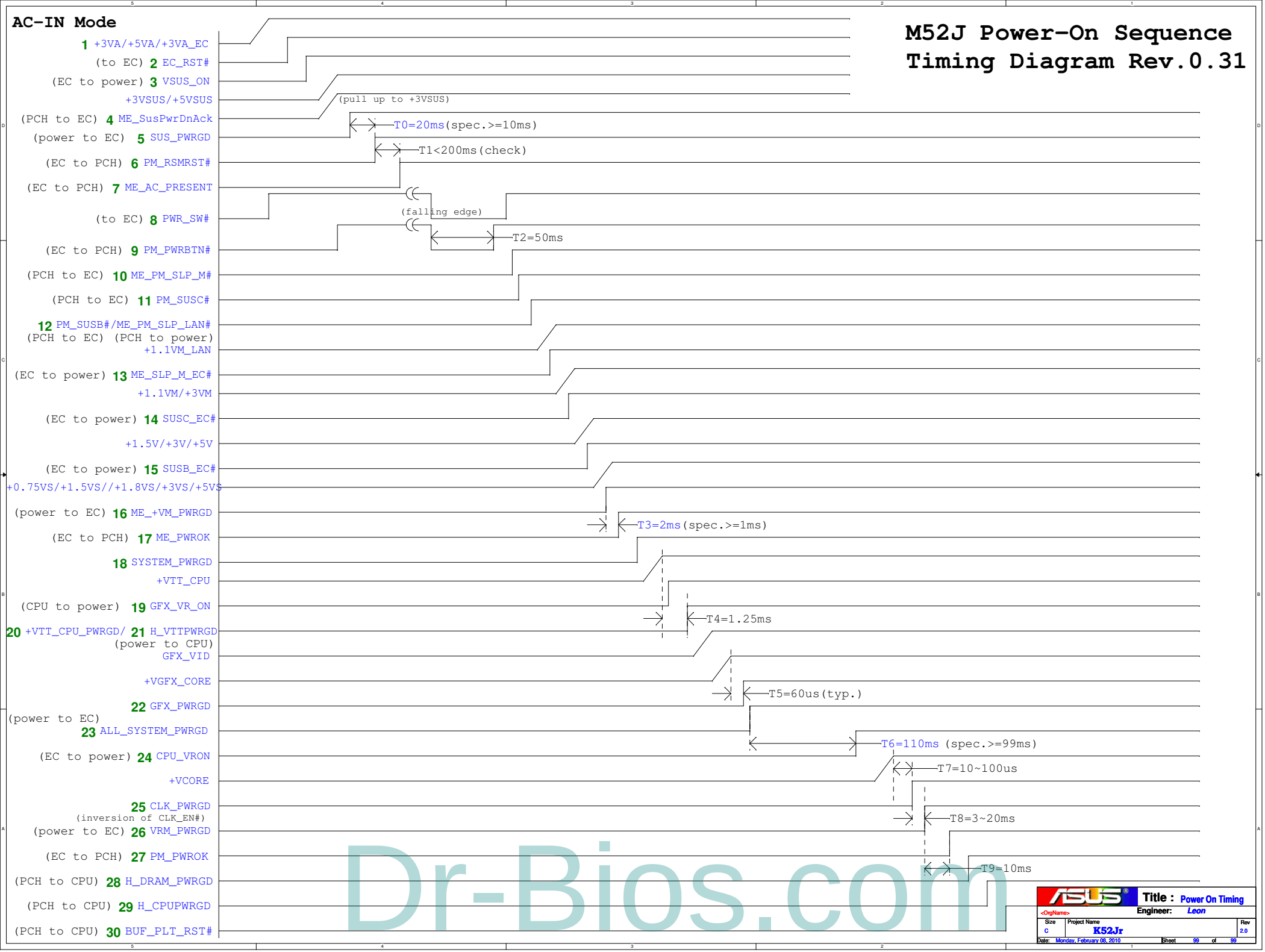
DC-IN Mode



ASUS	Title : Power On Timing	
<OrgName>	Engineer: Leon	
Size: C	Project Name: K52Jr	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 98 of 99	

M52J Power-On Sequence Timing Diagram Rev.0.31

AC-IN Mode



ASUS

Title : Power On Timing

<OrgName> Engineer: Leon

Size	Project Name	Rev
C	K52Jr	2.0

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