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VAL40 MB Schematic Document

LA-8226P

Rev: 1.0

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VAL40

ZZZ1
PCB-MB
PCB P/N for Lead BOM
DA80000V100

NV
N13M-GE1
Gb1B-64
23x23mm
Page 20 ~ 28

PEG 16X

Intel
Ivy Bridge ULV
Processor
BGA 1023
Page 4 ~ 9
+VCC_CORE, +VCCP,
+VCC_GFXCORE_AVG, +1.5V_CPU_VDDQ,
+1.8VS, _VCCSA

DDR3 1333/1600MHz 1.5V
Dual Channel

DDR3-SO-DIMM X 2
BANK 0, 1, 2, 3
+1.5V, +0.75VS
Page 10, 11

FDI x8
(UMA)
100MHz
2.7GT/s

DMI x4
100MHz
5GB/s

LCD conn
Page 30
LVDS, EDID, DISPOFF#, PWM

CRT Conn
Page 30
RGB, HV Sync, DDC

HDMI
Page 35
HDMI, DDC

Intel
PANTHER-POINT
PCH

HM76

FCBGA 989 Balls

Page 12 ~ 19

+1.05VS, +1.8VS, +3VS,
+3V_PCH, +5V_PCH, +RTCVCC,
+VCCAFDI_VRM

USB2.0

port 2
USB conn x1
USB Board Page 33

port 11
Camera
Page 30

port 3
Card Reader
RTS5137 Page 34

Memory Card Slot
SD/MMC
Page 34

port 10
MiniCard-1
Page 40

USB3.0

port 0,1
port 1,2
USB3.0 conn x2
Page 36

Azalia

Realtek
ALC269 Page 33

Audio Jack (HP)
Page 33

Audio Jack (MIC)
Page 33

Speaker Connector
Page 33

SATA

port 0
2.5" SATA HDD Connector
Page 31

port 2
SATA ODD Connector
Page 31

PCI-e

port 1
LAN/CRT Board
10/100/1000 LAN
Realtek GbE
RTL8111F Page 32

port 2
Mini Card-1
WLAN
Bluetooth
Page 40

SPI

SPI ROM 8MB
Page 12

LPC BUS

Click Pad CONN.
Page 38

ENE KB9012QF
+3VLP/+3VALW page 39

Int. KBD
Page 38

External board

DC/DC Interface CKT.
Page 29,41

LS-8221P
USB/B Page 33

Fan Control
Page 37

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MIC/B Page 30

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Title: Block Diagram

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BTO Option Table

BOM Structure	BTO Item
DIS@	VGA componet
GE8@	N13M-GE1_GB1b-64
X76L07@	VRAM Hynix 2Gbx8 256Mx8
GCLK@	G-CLK
GCLKDIS@	G-CLK + SLG3NB300
GCLKUMA@	G-CLK + SLG3NB244
NONGCLK@	NONE G-CLK
AI@	AI Charger
NAI@	Non AI Charger
46@	HDMI royalty rule
I33110@	CPU BGA i3-3110M 2.4G/3M
I32370@	CPU BGA i3-2370M 2.4G/3M
I32350@	CPU BGA i3-2350M 2.3G/3M

CPU BOM Config

I33310@	i3-3110M	CR	2.4G	SA00005M830 (INT I3-3110M 2.4G/3M SR0N2 BGA)
I32370@	i3-2370M	HR	2.4G	SA000059I60 (INT I3-2370M 2.4G/3M SR0DQ BGA)
I32350@	i3-2350M	HR	2.3G	SA00004QXA0 (INT I3-2350M 2.3G/3M SR0DQ BGA)

BOM Config : DIS

K45B(i3-3110M) DIS@/GE8@/X7607@/GCLK@/GCLKDIS@/I33110@/NAI@

* K45B(i3-2370M) DIS@/GE8@/X7607@/GCLK@/GCLKDIS@/I32370@/NAI@

BOM Config : UMA

K45B(i3-3110M) GCLK@/GCLKUMA@/I33110@/NAI@

K45B(i3-2370M) GCLK@/GCLKUMA@/I32370@/NAI@

* K45B(i3-2350M) GCLK@/GCLKUMA@/I32350@/NAI@

VRAMX8X8

N13M-GE1 x8

CPU

SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

	USB3 PORT	DESTINATION
PCH	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

	USB2 PORT	DESTINATION
PCH	0	USB2.0+3.0
	1	USB2.0+3.0
	2	USB2
	3	Card Reader
	4	None
	5	None
	6	None
	7	None
	8	None
	9	None
	10	JMINI1 (WLAN) Bluetooth
	11	CAMERA
	12	None
	13	None

Voltage Rails

Power Plane	Description	S0	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 51ON power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes List

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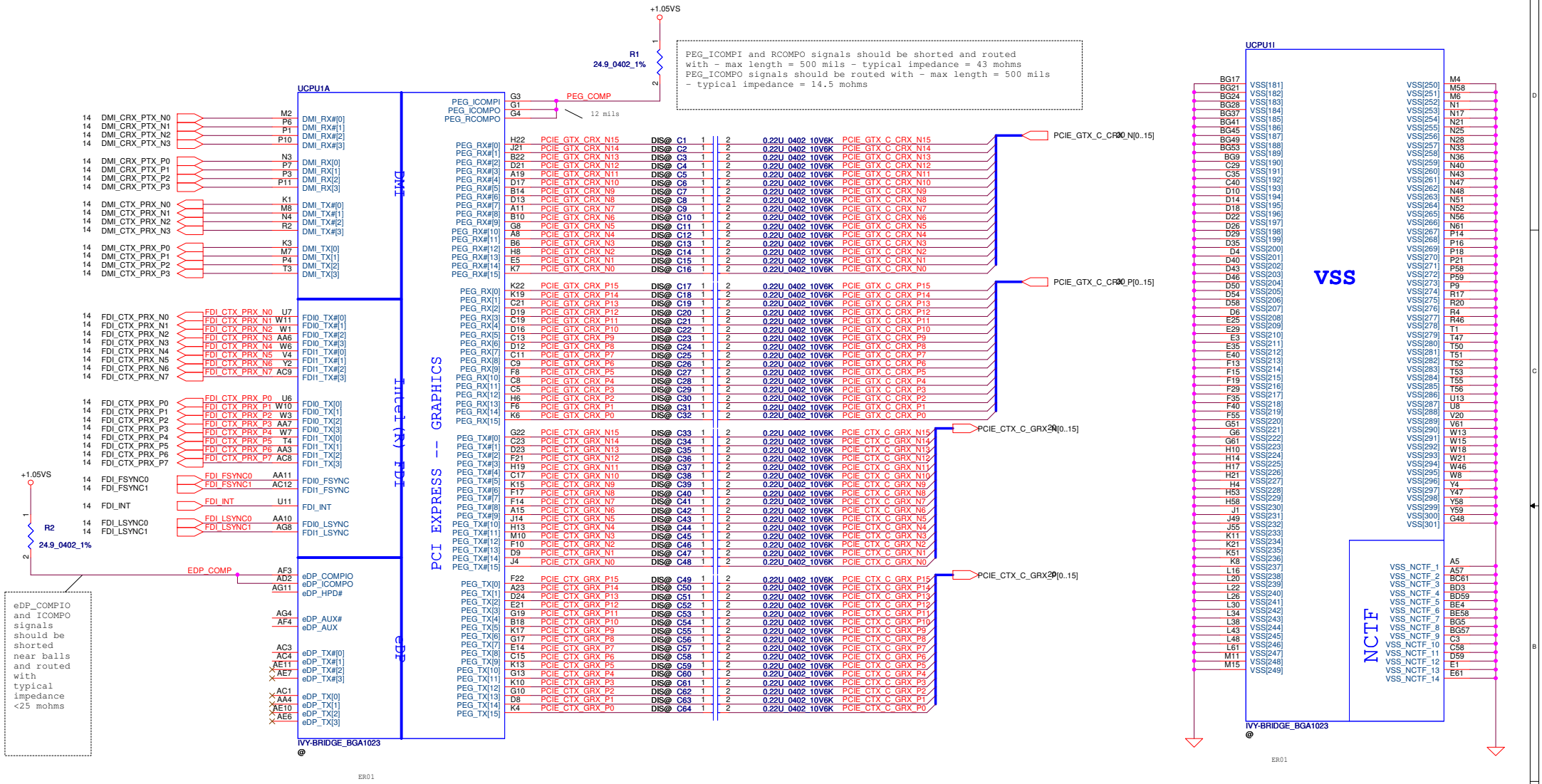

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Title: PROCESSOR(1/6) DMI,FDI,PEG

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Processor Pullups

+1.05VS — H_PROCHOT# — 62_0402_5% — R16

@ C68 100P_0402_50V8J H_PECI

Reserve for EMI please close to JCPU1

+3V_PCH — ER03 — R576 0_0402_5%

+3VS — R3 10K_0402_5%

+1.5V_CPU_VDDQ — R4 200_0402_1%

C65 0.1U_0402_16V4Z-D

14 SYSTEM_PWROK — R9 @ 0_0402_5% — S_PWG

14 PM_DRAM_PWRGD — R11 0_0402_5% — D_PWG

+3V_PCH — R14 200_0402_1%

U1 74AHC1G09GW TSSOP 5P — VDDPWRGOOD

UCPU1B

MISC

16 H_SNB_IVB# — F49 PROC_SELECT#

C57 — PROC_DETECT#

CLOCKS

BCLK J3 CLK_CPU_DMI_R — R18 0_0402_5% — CLK_CPU_DMI 13

BCLK# H2 CLK_CPU_DMI#_R — R19 0_0402_5% — CLK_CPU_DMI# 13

DPLL_REF_CLK AG3 CLK_CPU_DPLL_R

DPLL_REF_CLK# AG1 CLK_CPU_DPLL#_R

THERMAL

PAD T1 @ — H_CATERR# — C49 CATERR#

39 H_PECI — A48 PECI

39 H_PROCHOT# — R23 56_0402_5% — H_PROCHOT#_R — C45 PROCHOT#

16 H_THERMTRIP# — D45 THERMTRIP#

DDR3 MISC

SM_DRAMRST# AT30 H_DRAMRST# — H_DRAMRST# 6

SM_RCOMP[0] BF44 SM_RCOMP0

SM_RCOMP[1] BE43 SM_RCOMP1

SM_RCOMP[2] BG43 SM_RCOMP2

PWR MANAGEMENT

14 H_PM_SYNC — C48 PM_SYNC

16 H_CPUPWRGD — R684 33_0402_5% — H_CPUPWRGD_R — B46 UNCOREPWRGOOD

VDDPWRGOOD — R36 130_0402_1% — BE45 SM_DRAMPWROK

BUF_CPU_RST# — D44 RESET#

JTAG & BPM

PRDY# N53 XDP_PRDY#

PREQ# N55 XDP_PREQ#

TCK L56 XDP_TCK

TMS L55 XDP_TMS

TRST# J58 XDP_TRST#

TDI M60 XDP_TDI_R

TDO L59 XDP_TDO_R

DBR# K58 XDP_DBRESET#_R1 — R37 0_0402_5% — XDP_DBRESET#1R

BPM#[0] G58

BPM#[1] E55

BPM#[2] E59

BPM#[3] G55

BPM#[4] G59

BPM#[5] H60

BPM#[6] J59

BPM#[7] J61

IVY-BRIDGE_BGA1023

@ ER01

+3VS — C69 0.1U_0402_16V4Z

+1.05VS — R15 75_0402_5%

15,32,39,40 PLT_RST# — U2 SN74LVC1G07DCKR_SC70-5 — BUFO_CPU_RST# — R17 43_0402_1% — BUF_CPU_RST#

@ R20 0_0402_5%

+1.05VS — CLK_CPU_DPLL# R — R21 1K_0402_1%

CLK_CPU_DPLL_R — R22 1K_0402_1%

XDP_DBRESET#_R1 — 1K_0402_5% — R24 — +3VS

H_CPUPWRGD_R — 10K_0402_5% — R25

PU/PD for JTAG signals

+1.05VS

XDP_TMS — 51_0402_5% — R26

XDP_TDI_R — 51_0402_5% — R27

XDP_PREQ# — 51_0402_5% — @ R28

XDP_TDO_R — 51_0402_5% — R29

XDP_TCK — 51_0402_5% — R32

XDP_TRST# — 51_0402_5% — R33

DDR3 Compensation Signals

SM_RCOMP0 — 140_0402_1% — R34

SM_RCOMP1 — 25.5_0402_1% — R38

SM_RCOMP2 — 200_0402_1% — R39

@ C70 100P_0402_50V8J H_DRAMRST#

Reserve for EMI please close to JCPU1

@ C71 100P_0402_50V8J XDP_DBRESET#_R1

Reserve for EMI please close to JCPU1

@ C72 100P_0402_50V8J VDDPWRGOOD_R

Reserve for EMI please close to JCPU1

C421 100P_0402_50V8J H_CPUPWRGD_R

Reserve for EMI please close to JCPU1

@ C426 100P_0402_50V8J BUF_CPU_RST#

Reserve for EMI please close to JCPU1

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Title: PROCESSOR(2/6) PM,XDP,CLK

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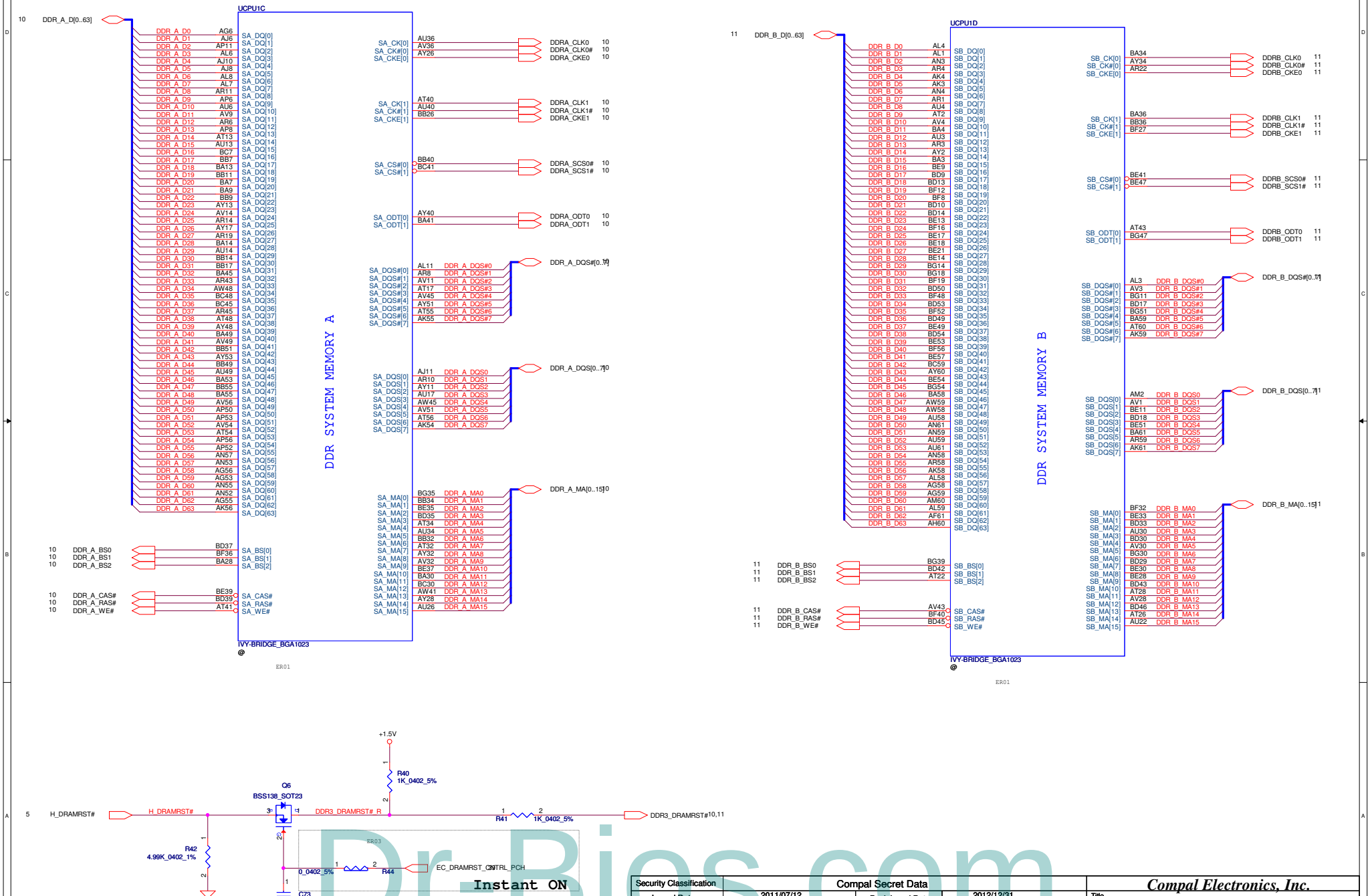

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Compal Electronics, Inc.

Title: PROCESSOR(3/6) DDRIII

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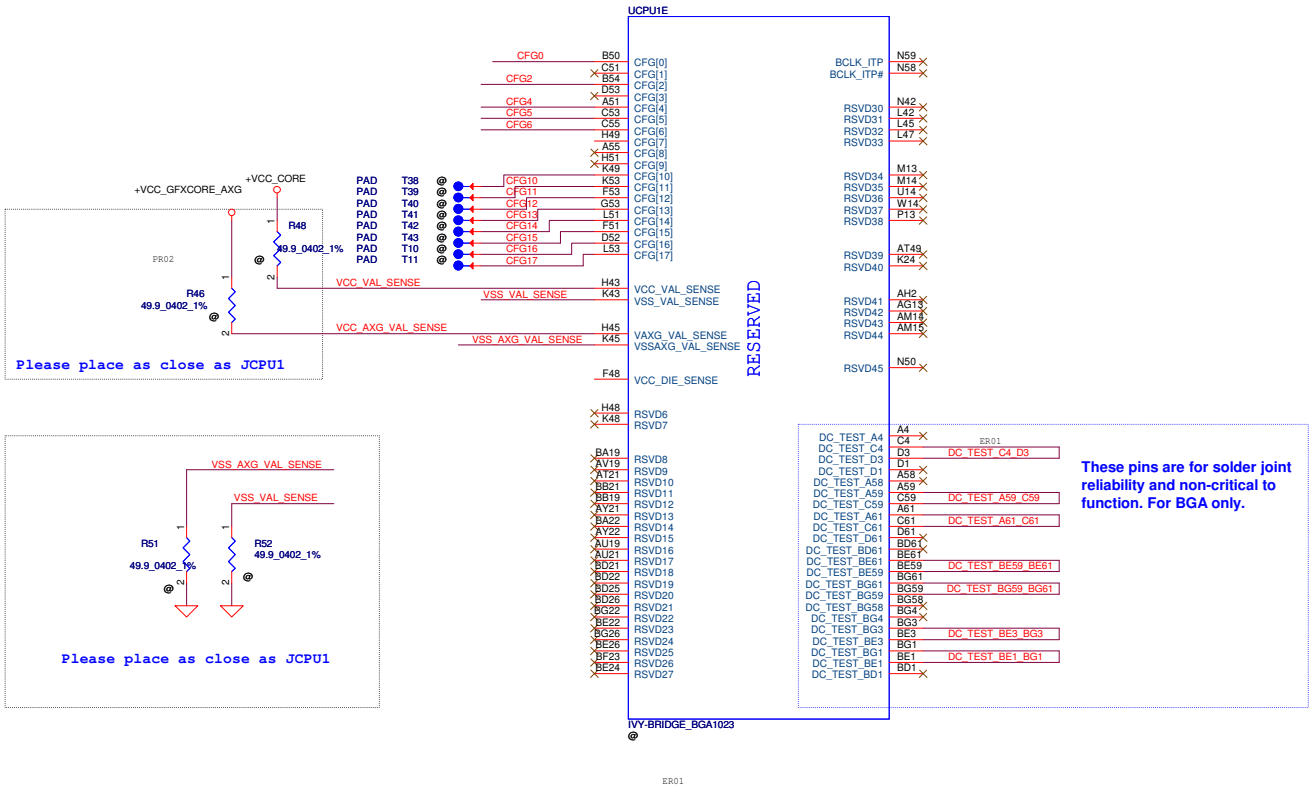
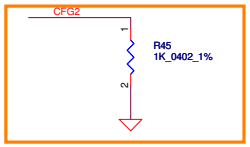
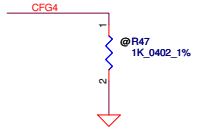


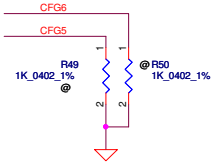
CFG Straps for Processor



PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

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Title	PROCESSOR(4/6) RSVD,CFG		
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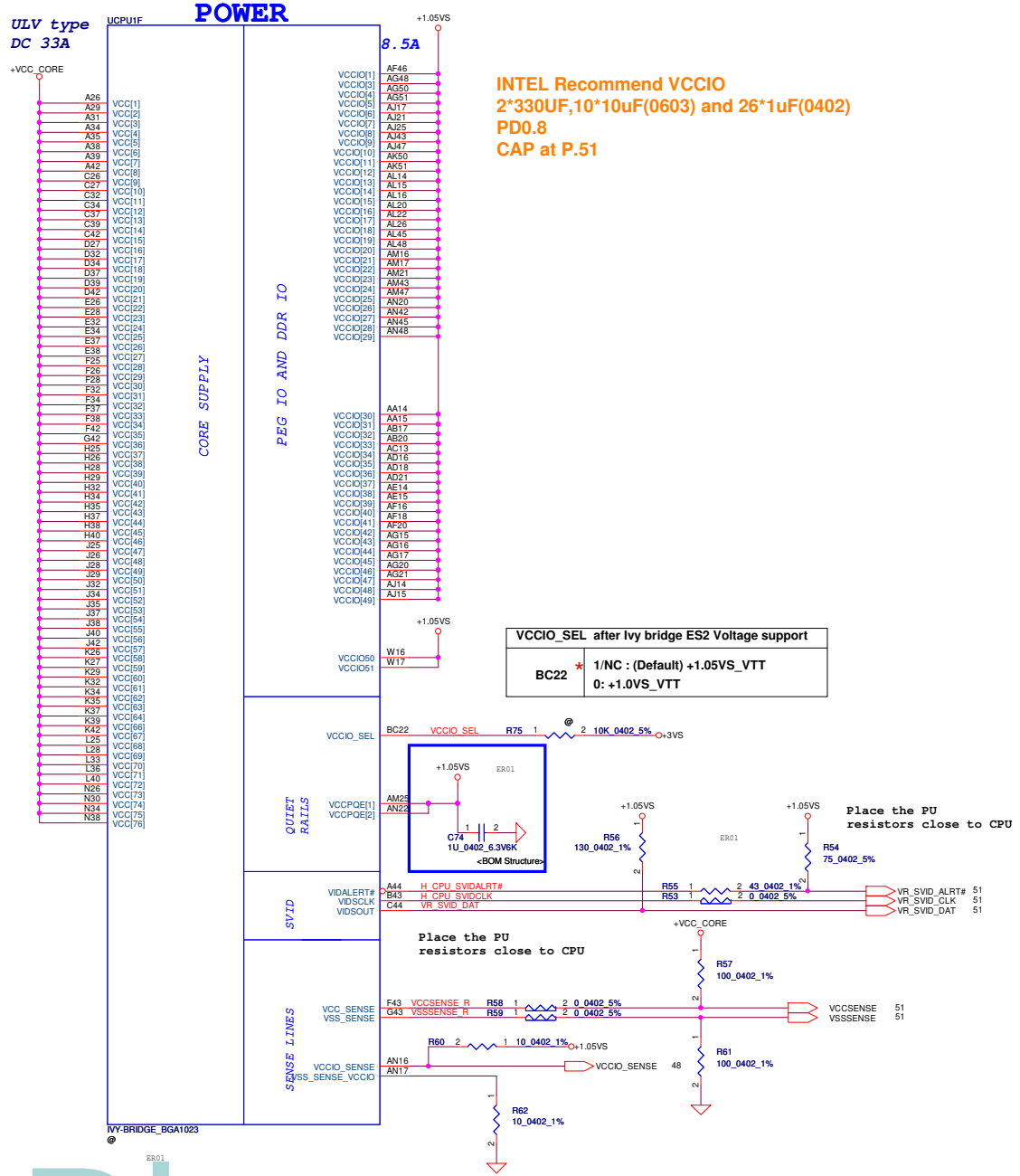
POWER

ULV type
DC 33A

8.5A

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51



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Title: PROCESSOR(5/6) PWR,BYPASS

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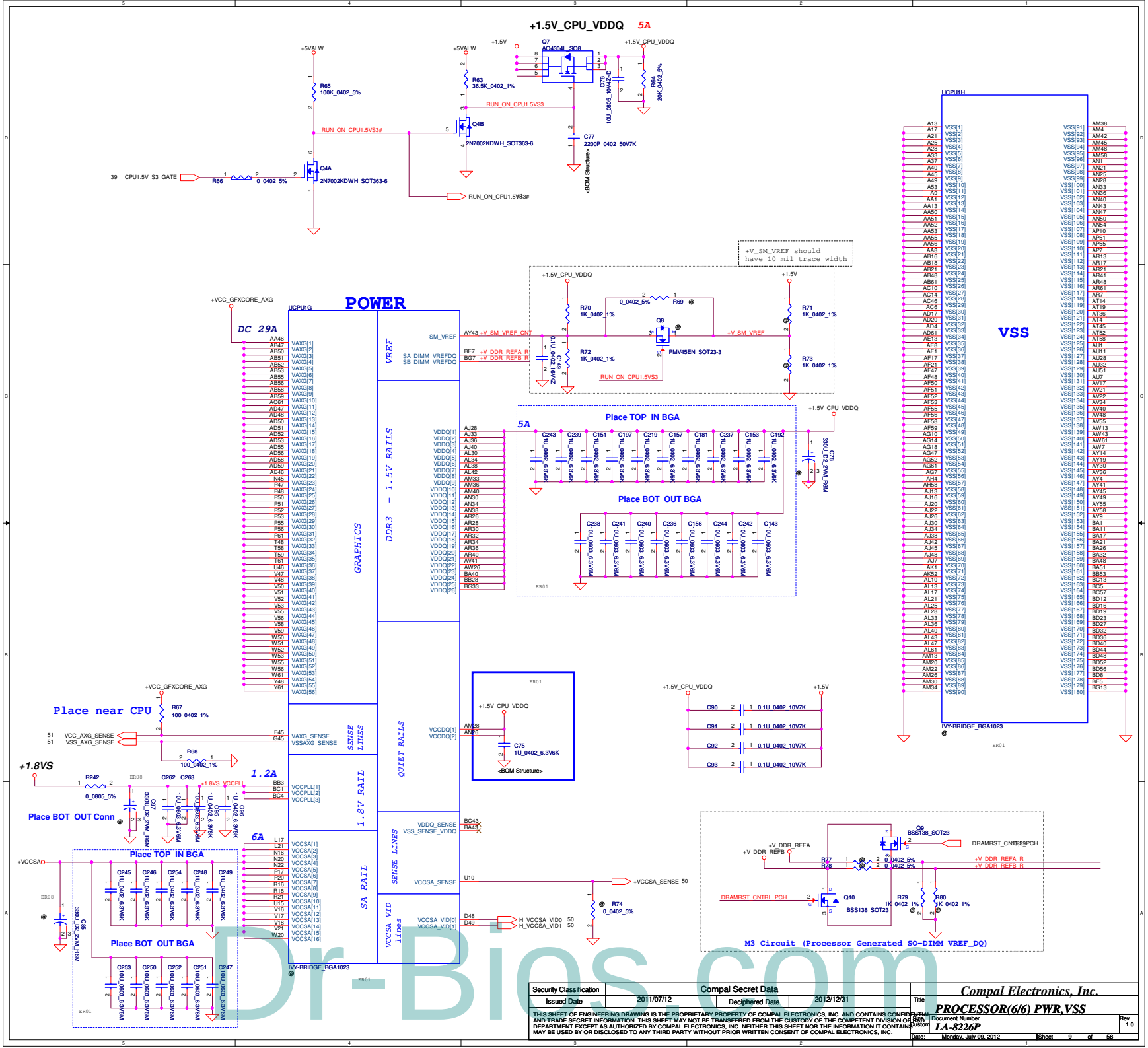

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3.56A

DDR3 SO-DIMM A

JDIMM1

+1.5V

R81 1K_0402_1%

R82 1K_0402_1%

+V_DDR_REFA

C98 0.1U_0402_10V6K

C99 2.2U_0402_6.3V6M

6 DDR_A_D[0..63]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#[0..7]
6 DDR_A_MA[0..15]

	1	VREF_DQ	VSS1	2			
	3	VSS2	DQ4	4	DDR_A_D4		
DDR_A_D0	5	DQ0	DQ5	6	DDR_A_D5		
DDR_A_D1	7	VSS3	DQ1	8			
	9	DQ1	VSS4	10	DDR_A_DQS#0		
	11	VSS4	DQS#0	12	DDR_A_DQS0		
DDR_A_D2	13	DM0	DQS0	14			
DDR_A_D3	15	VSS5	DQ6	16	DDR_A_D6		
	17	DQ2	DQ7	18	DDR_A_D7		
DDR_A_D8	19	DQ3	VSS8	20			
DDR_A_D9	21	VSS7	DQ12	22	DDR_A_D12		
	23	DQ8	DQ13	24	DDR_A_D13		
DDR_A_DQS#1	25	DQ9	VSS10	26			
DDR_A_DQS1	27	VSS9	DM1	28			
	29	DQS#1	RESET#	30	DDR3_DRAMRST#	DDR3_DRAMRST#	6
DDR_A_D10	31	DQS1	VSS12	32			
DDR_A_D11	33	VSS11	DQ14	34	DDR_A_D14		
	35	DQ10	DQ15	36	DDR_A_D15		
DDR_A_D16	37	DQ11	VSS14	38			
DDR_A_D17	39	VSS13	DQ20	40	DDR_A_D20		
	41	DQ16	DQ21	42	DDR_A_D21		
DDR_A_DQS#2	43	DQ17	VSS16	44			
DDR_A_DQS2	45	VSS15	DM2	46			
	47	DQS#2	VSS17	48			
DDR_A_D18	49	DQS2	DQ22	50	DDR_A_D22		
DDR_A_D19	51	VSS18	DQ23	52	DDR_A_D23		
	53	DQ18	VSS19	54			
DDR_A_D24	55	DQ19	DQ28	56	DDR_A_D28		
DDR_A_D25	57	VSS20	DQ29	58	DDR_A_D29		
	59	DQ24	VSS21	60			
	61	DQ25	DQS#3	62	DDR_A_DQS#3		
	63	VSS22	DQS3	64	DDR_A_DQS3		
DDR_A_D26	65	DM3	VSS24	66			
DDR_A_D27	67	VSS23	DQ30	68	DDR_A_D30		
	69	DQ26	DQ31	70	DDR_A_D31		
	71	DQ27	VSS26	72			
6 DDRA_CKE0	DDRA_CKE0	73	CKE0	CKE1	74	DDRA_CKE1	DDRA_CKE1 6
		75	VDD1	VDD2	76		
6 DDR_A_BS2	DDR_A_BS2	77	NC1	A15	78	DDR_A_MA15	
		79	BA2	A14	80	DDR_A_MA14	
	DDR_A_MA12	81	VDD3	VDD4	82		
	DDR_A_MA9	83	A12/BC#	A11	84	DDR_A_MA11	
		85	A9	A7	86	DDR_A_MA7	
	DDR_A_MA8	87	VDD5	VDD6	88		
	DDR_A_MA5	89	A8	A6	90	DDR_A_MA6	
		91	A5	A4	92	DDR_A_MA4	
	DDR_A_MA3	93	VDD7	VDD8	94		
	DDR_A_MA1	95	A3	A2	96	DDR_A_MA2	
		97	A1	A0	98	DDR_A_MA0	
6 DDRA_CLK0	DDRA_CLK0	99	VDD9	VDD10	100		
6 DDRA_CLK0#	DDRA_CLK0#	101	CK0	CK1	102	DDRA_CLK1	DDRA_CLK1 6
		103	CK0#	CK1#	104	DDRA_CLK1#	DDRA_CLK1# 6
	DDR_A_MA10	105	VDD11	VDD12	106		
6 DDR_A_BS0	DDR_A_BS0	107	A10/AP	BA1	108	DDR_A_BS1	DDR_A_BS1 6
		109	BA0	RAS#	110	DDR_A_RAS#	DDR_A_RAS# 6
6 DDR_A_WE#	DDR_A_WE#	111	VDD13	VDD14	112		
6 DDR_A_CAS#	DDR_A_CAS#	113	WE#	S0#	114	DDRA_SCS0#	DDRA_SCS0# 6
		115	CAS#	ODT0	116	DDRA_ODT0	DDRA_ODT0 6
	DDR_A_MA13	117	VDD15	VDD16	118		
6 DDRA_SCS1#	DDRA_SCS1#	119	A13	ODT1	120	DDRA_ODT1	DDRA_ODT1 6
		121	S1#	NC2	122		
		123	VDD17	VDD18	124		
		125	NCTEST	VREF_CA	126	+VREF_CA	
		127	VSS27	VSS28	128		
	DDR_A_D32	129	DQ32	DQ36	130	DDR_A_D36	
	DDR_A_D33	131	DQ33	DQ37	132	DDR_A_D37	
		133	VSS29	VSS30	134		
	DDR_A_DQS#4	135	DQS#4	DM4	136		
	DDR_A_DQS4	137	DQS4	VSS31	138		
	DDR_A_D34	139	VSS32	DQ38	140	DDR_A_D38	
	DDR_A_D35	141	DQ34	DQ39	142	DDR_A_D39	
		143	DQ35	VSS33	144		
	DDR_A_D40	145	VSS34	DQ44	146	DDR_A_D44	
	DDR_A_D41	147	DQ40	DQ45	148	DDR_A_D45	
		149	DQ41	VSS35	150		
		151	VSS36	DQS#5	152	DDR_A_DQS#5	
		153	DM5	DQS5	154	DDR_A_DQS5	
		155	VSS37	VSS38	156		
	DDR_A_D42	157	DQ42	DQ46	158	DDR_A_D46	
	DDR_A_D43	159	DQ43	DQ47	160	DDR_A_D47	
		161	VSS39	VSS40	162		
	DDR_A_D48	163	DQ48	DQ52	164	DDR_A_D52	
	DDR_A_D49	165	DQ49	DQ53	166	DDR_A_D53	
		167	VSS41	VSS42	168		
	DDR_A_DQS#6	169	DQS#6	DM6	170		
	DDR_A_DQS6	171	DQS6	VSS43	172		
		173	VSS44	DQ54	174	DDR_A_D54	
	DDR_A_D50	175	DQ50	DQ55	176	DDR_A_D55	
	DDR_A_D51	177	DQ51	VSS45	178		
		179	VSS46	DQ60	180	DDR_A_D60	
	DDR_A_D56	181	DQ56	DQ61	182	DDR_A_D61	
	DDR_A_D57	183	DQ57	VSS47	184		
		185	VSS48	DQS#7	186	DDR_A_DQS#7	
		187	DM7	DQS7	188	DDR_A_DQS7	
	DDR_A_D58	189	VSS49	VSS50	190		
	DDR_A_D59	191	DQ58	DQ62	192	DDR_A_D62	
		193	DQ59	DQ63	194	DDR_A_D63	
		195	VSS51	VSS52	196		
		197	SA0	EVENT#	198		
+3VS		199	VDDSPD	SDA	200	PCH_SMBDATA	PCH_SMBDATA 11,13,38,40
		201	SA1	SCL	204	PCH_SMBCLK	PCH_SMBCLK 11,13,38,40
		203	VTT1	VTT2	204	+0.75VS	
		205	G1	G2	206		

TYCO 2-1932323-1

C119 2.2U_0402_6.3V6M
C118 0.1U_0402_10V6K
R85 10K_0402_5%
R86 10K_0402_5%

+1.5V

R83 1K_0402_1%
R84 1K_0402_1%

C108 0.1U_0402_10V6K
C109 2.2U_0402_6.3V6M

Layout Note:
Place near JDDRL

C100 330U_B2_2.5VM_R15M
C101 10U_0603_6.3V6M
C102 10U_0603_6.3V6M
C103 10U_0603_6.3V6M
C104 10U_0603_6.3V6M
C105 10U_0603_6.3V6M
C106 10U_0603_6.3V6M
C107 @ 10U_0603_6.3V6M

Layout Note: Place these 4 Caps near Command and Control signals of JDDRL

C110 1U_0402_6.3V6K
C111 1U_0402_6.3V6K
C112 1U_0402_6.3V6K
C113 1U_0402_6.3V6K

Layout Note:
Place near JDDRL.203,204

+0.75VS

C114 1U_0402_6.3V6K
C115 1U_0402_6.3V6K
C116 1U_0402_6.3V6K
C117 1U_0402_6.3V6K

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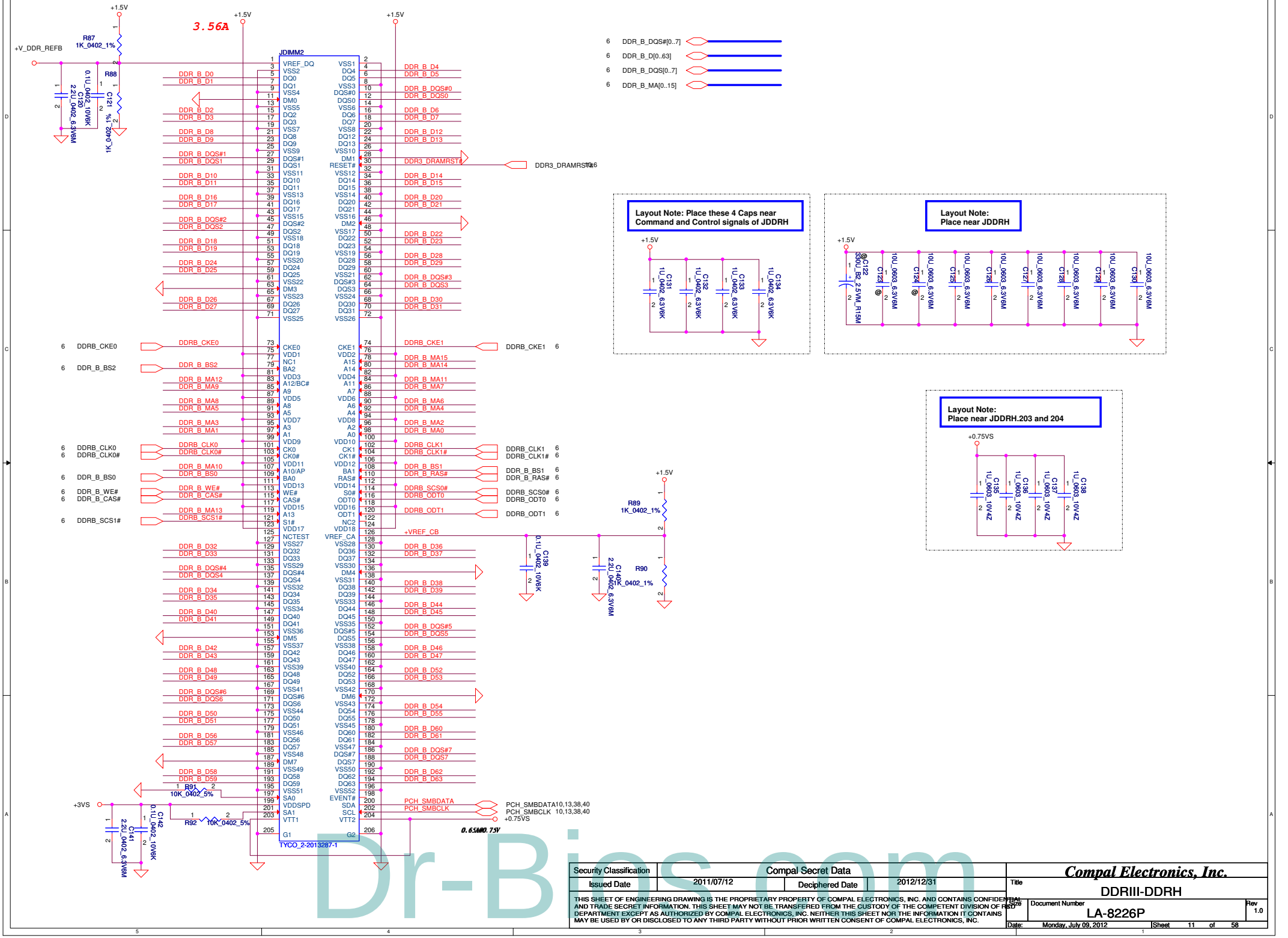
Compal Electronics, Inc.			
Title	DDRIII-DDRL		
Size	Document Number		Rev
Custom	LA-8226P		1.0
Date: Monday, July 09, 2012	Sheet 10 of 58		



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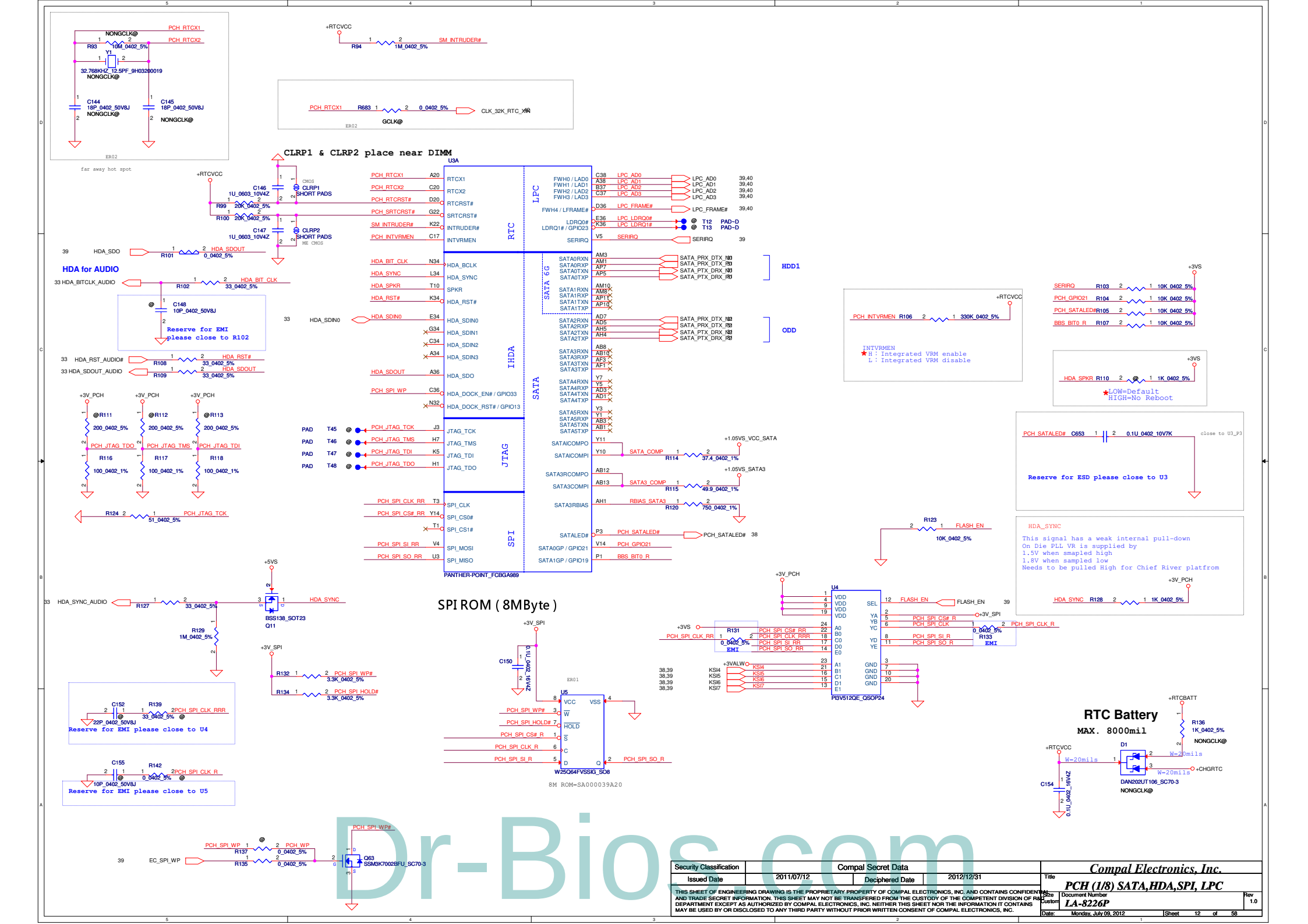
Title	DDRIII-DDRH		
Size	Document Number	LA-8226P	Rev 1.0
Date: Monday, July 09, 2012	Sheet 11 of 58		



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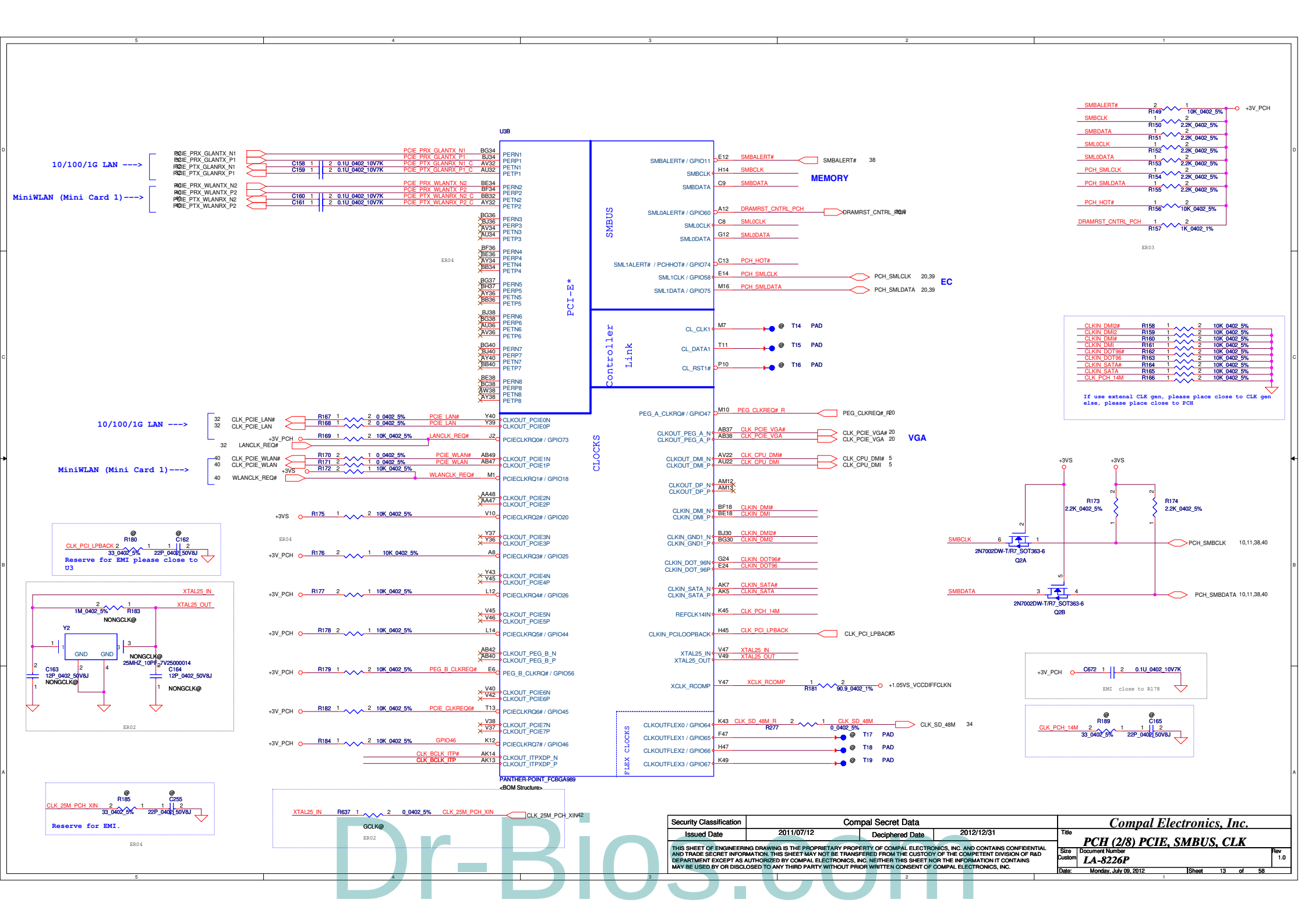
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size: Custom | Document Number: LA-8226P | Rev: 1.0

Date: Monday, July 09, 2012 | Sheet 12 of 58



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Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: LA-8226P | Rev: 1.0

Date: Monday, July 09, 2012 | Sheet 13 of 58

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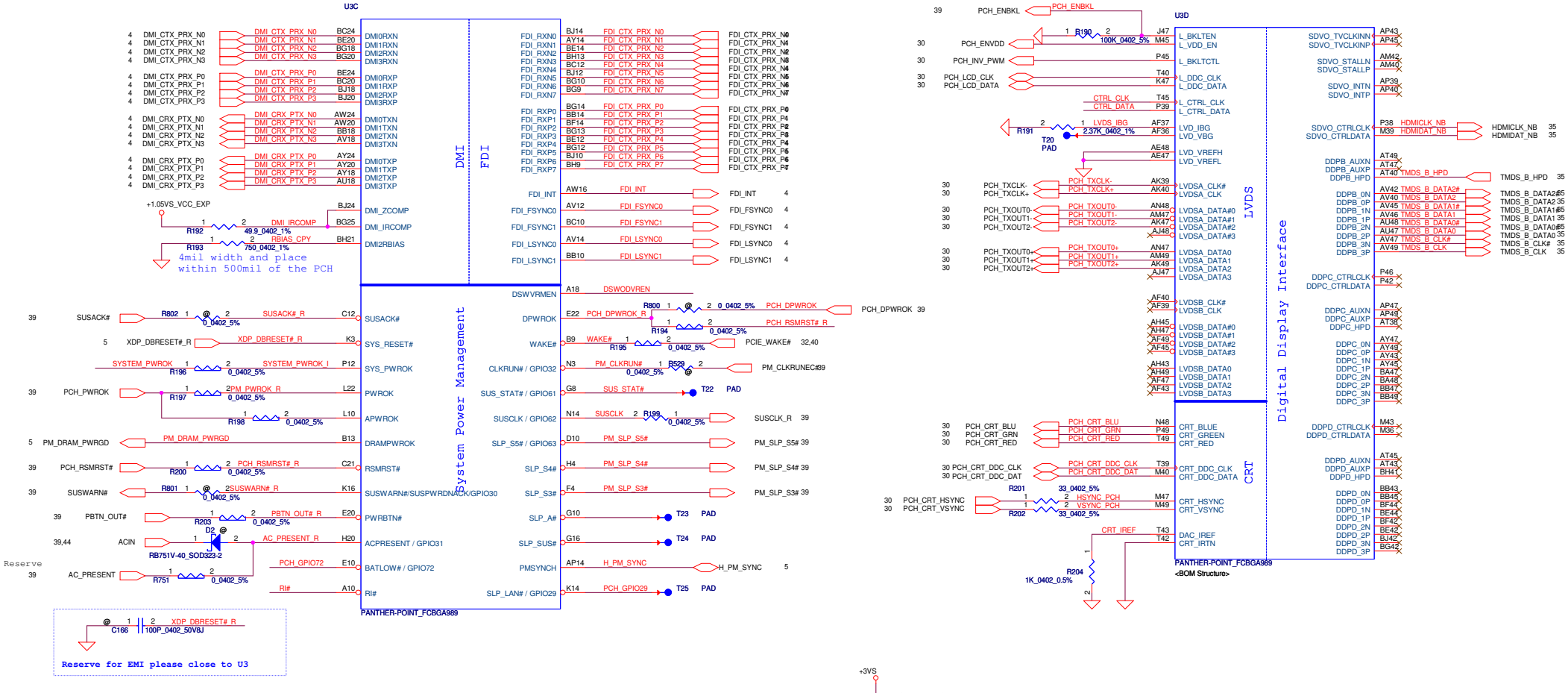

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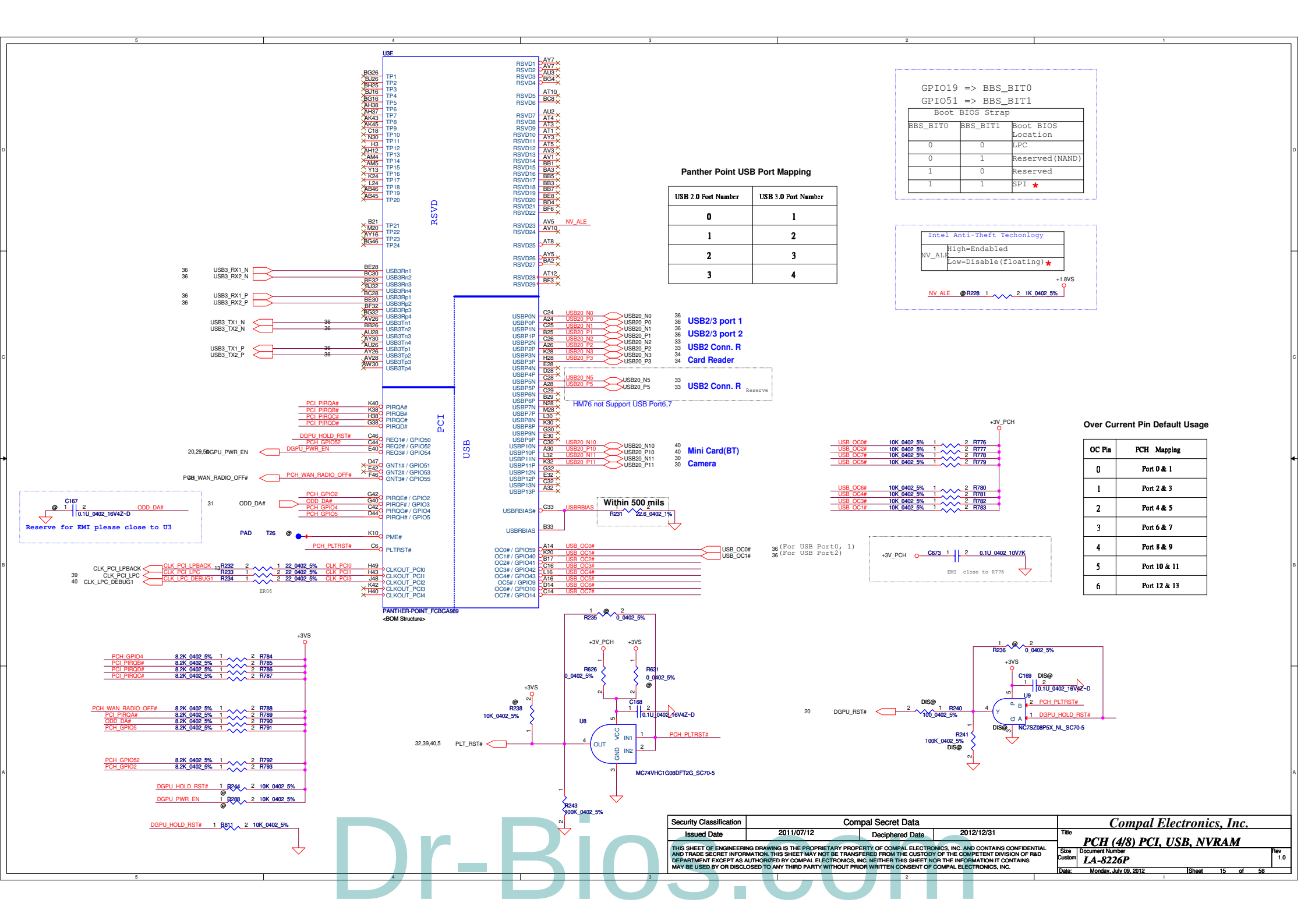
Compal Electronics, Inc.			
Title	PCH (3/8) DMI,FDI,PM,GFX,DP		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 14 of 58		



GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap

BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★

Intel Anti-Theft Techonlogy

NV_ALE	High=Endabled
	Low=Disable(floating)★

+1.8VS
NV_ALE @R228 1K_0402_5%

Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size: Custom | Document Number: LA-8226P | Rev: 1.0

Date: Monday, July 09, 2012 | Sheet 15 of 58

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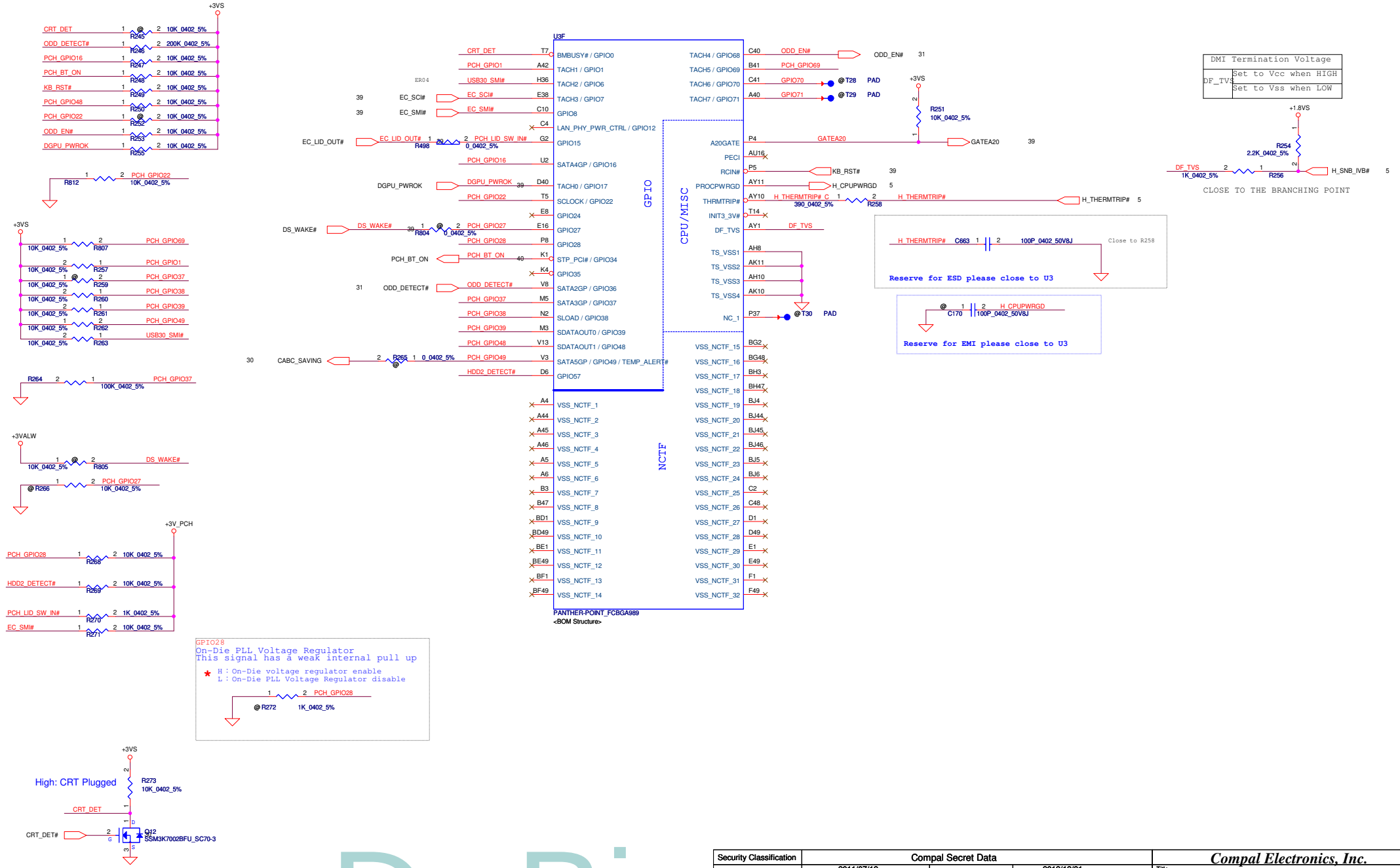

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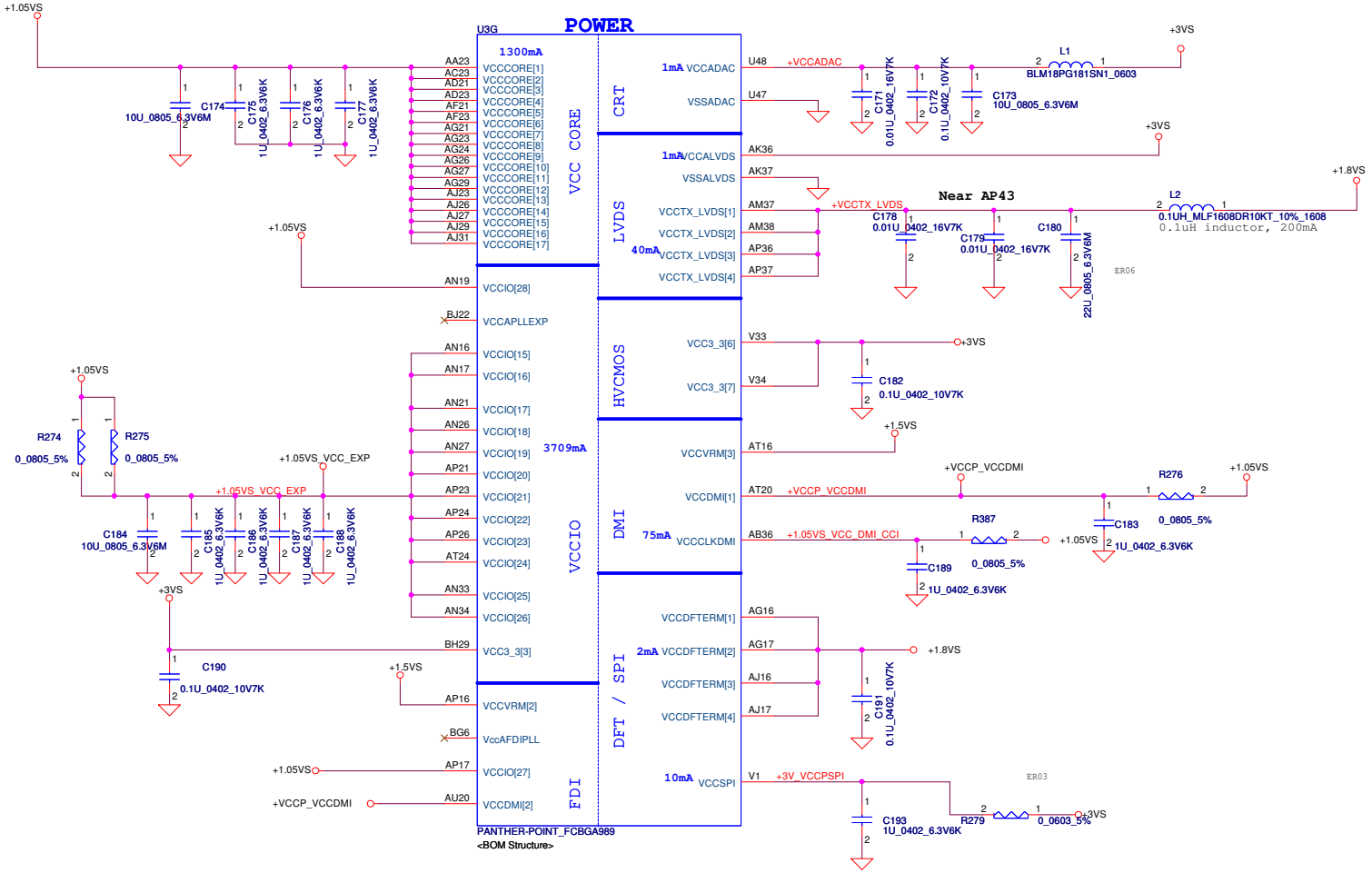
Compal Electronics, Inc.		
Title: PCH (5/8) GPIO, CPU, MISC		
Size: Custom	Document Number: LA-8226P	Rev: 1.0
Date: Monday, July 09, 2012	Sheet 16 of 58	



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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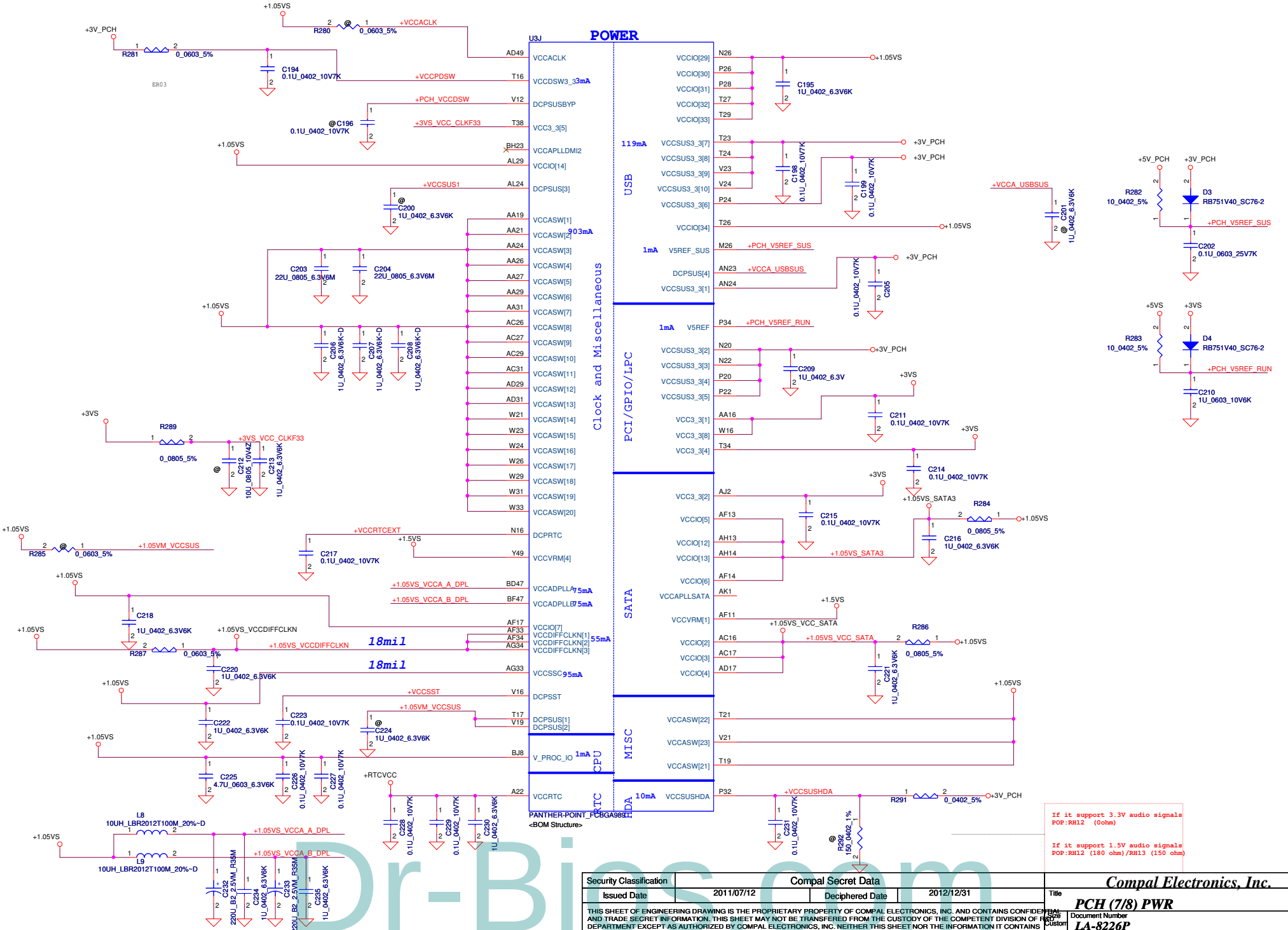
Compal Electronics, Inc.			
Title: PCH (6/8) PWR			
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 17 of 58		



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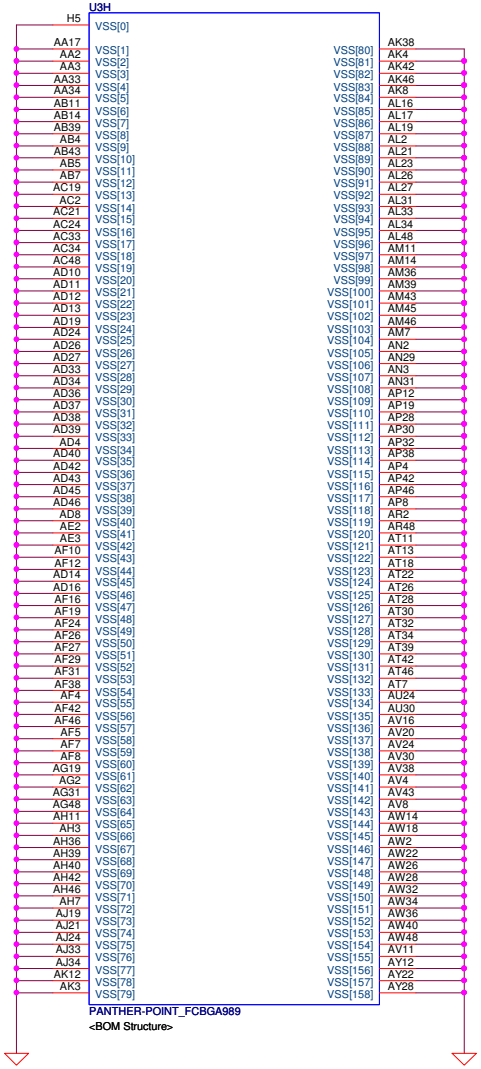
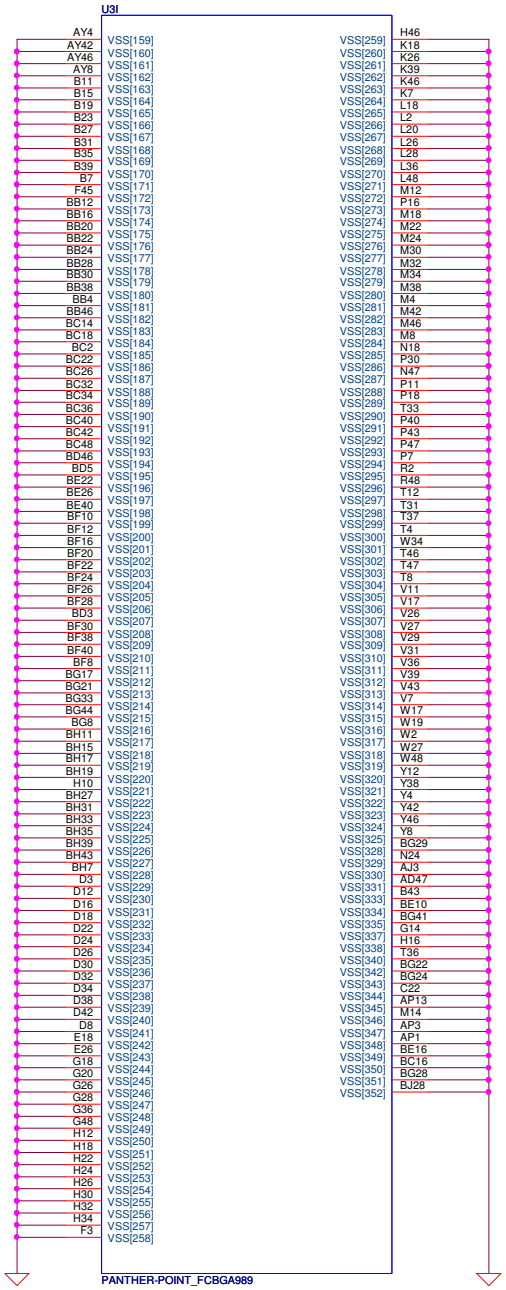
Compal Electronics, Inc.			
Title	PCH (7/8) PWR		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 18 of 58		





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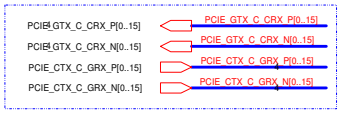
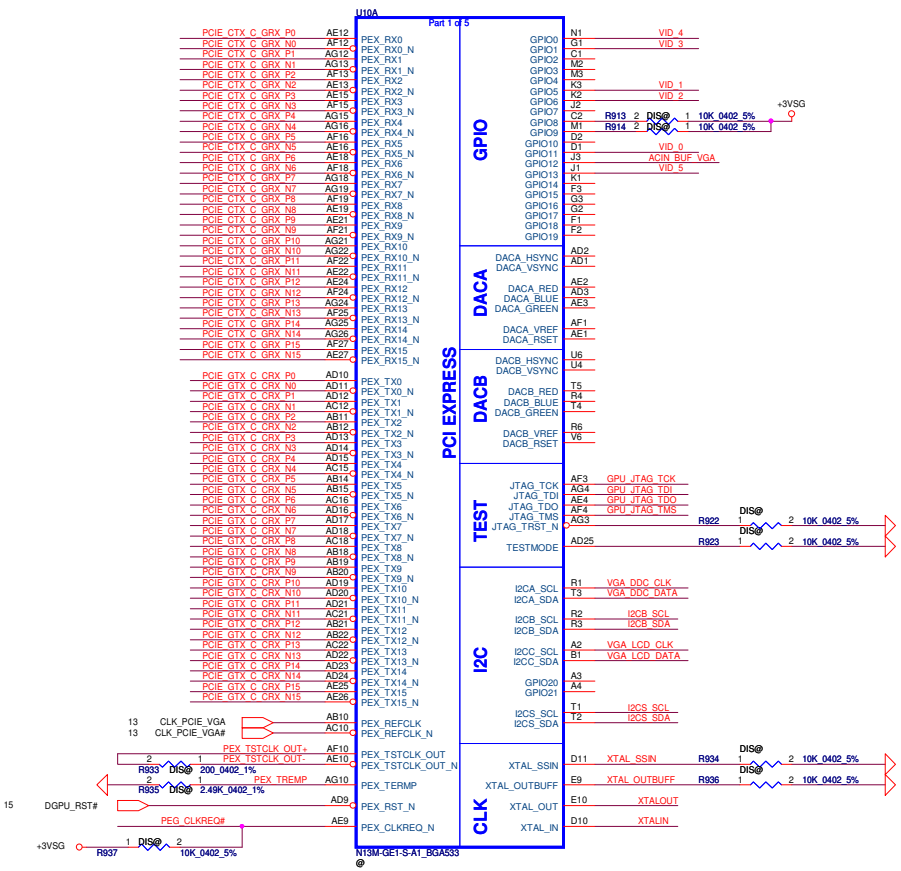
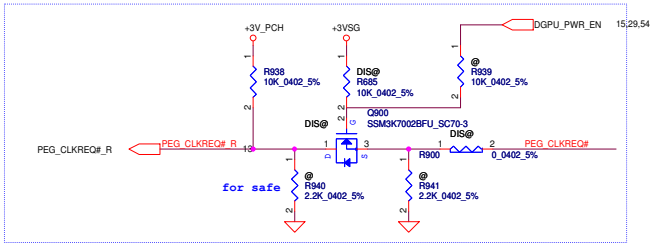
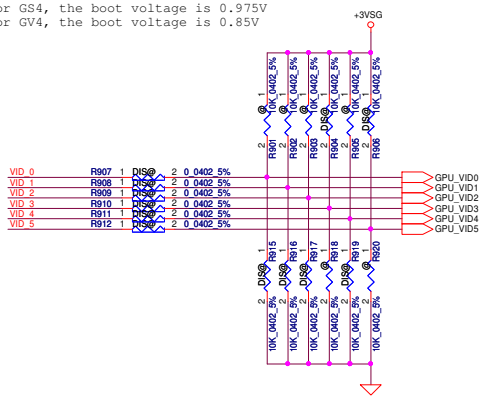
Compal Electronics, Inc.			
Title: PCH (8/8) VSS			
Size: B (5.25) Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 19 of 58		

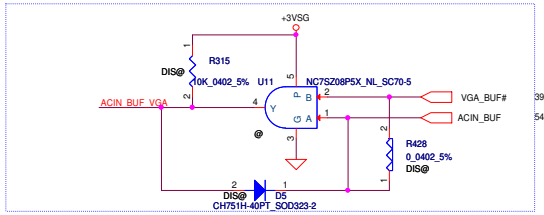


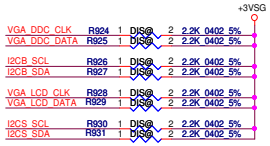


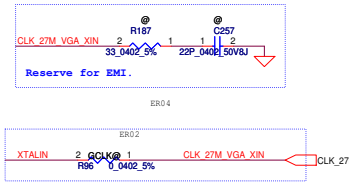


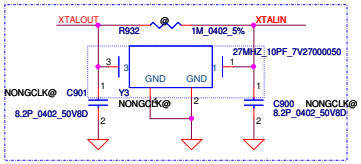
for GS4, the boot voltage is 0.975V
for GV4, the boot voltage is 0.85V

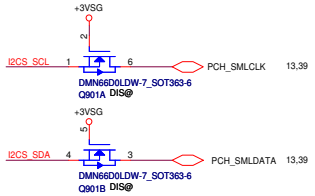












GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VDD
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT#
GPIO9	I/O	ALERT#
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU_VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU_VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

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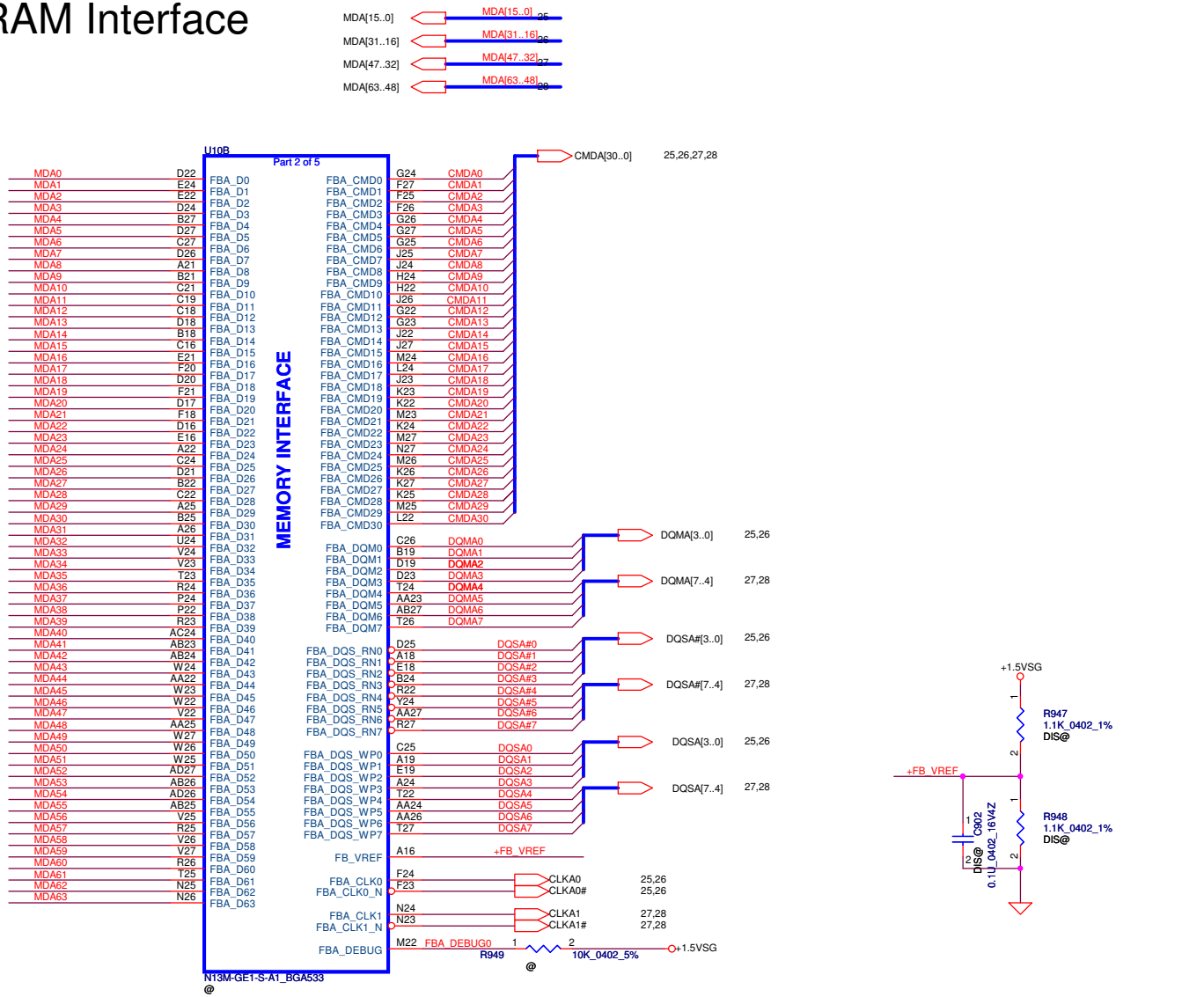
Date: Monday, July 09, 2012	Sheet 20 of 58		

VRAM Interface



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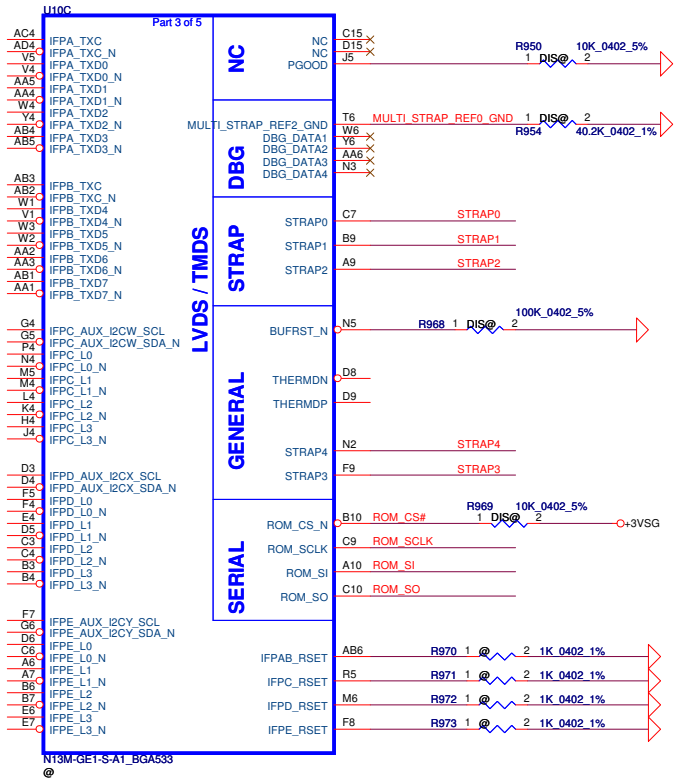
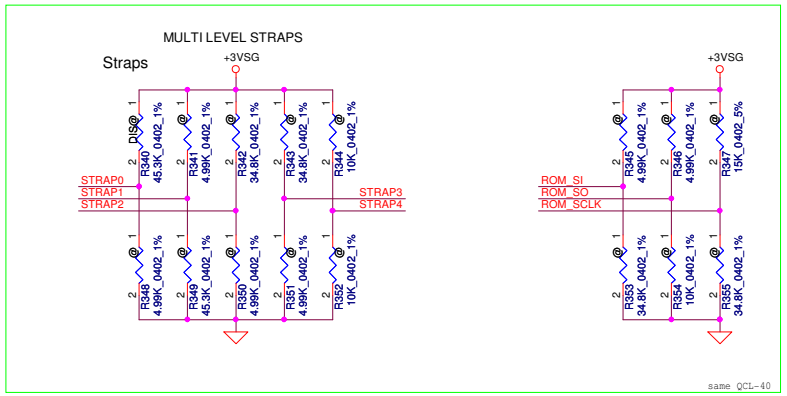
				Date: Monday, July 09, 2012	Sheet 21 of 58





Need check with NVIDIA

For N13M-GE1 GB1b-64_256Mx8 strap table

	GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
Cancel	N13M-GE1	800 MHz	256M* 8* 8 2GB	ELPIDA SA000056P00 EDJ2108BCSE-DJ-F	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 5K	R PU 10K	R PU 5K
X76 L07	N13M-GE1	800 MHz	256M* 8* 8 2GB	HYNIX SA000056O00 H5TQ2G83CFR-H9C	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 10K	R PU 10K	R PU 5K

SA000056A10
C.S N13M-GE1-S-A1 FCBGA533
NVIDIA GB1b-64 GF119-660-A1 (小包裝)
搭配VRAM 256*8*8

256M*8*8
1.SA000056O00
DDR3 1600 256*8 1.5V FBGA78
HYNIX/H5TQ2G83CFR-PBC
2.SA000056P00
DDR3 1600 256*8 1.5V FBGA78
ELPIDA/EDJ2108BDBG-GN-F

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Issued Date	2011/07/12	Deciphered Date	2012/12/31
Title	N13M LVDS 3/9		
Size Custom	Document Number LA-8226P		Rev 1.0
Date: Monday, July 09, 2012	Sheet 22 of 58		

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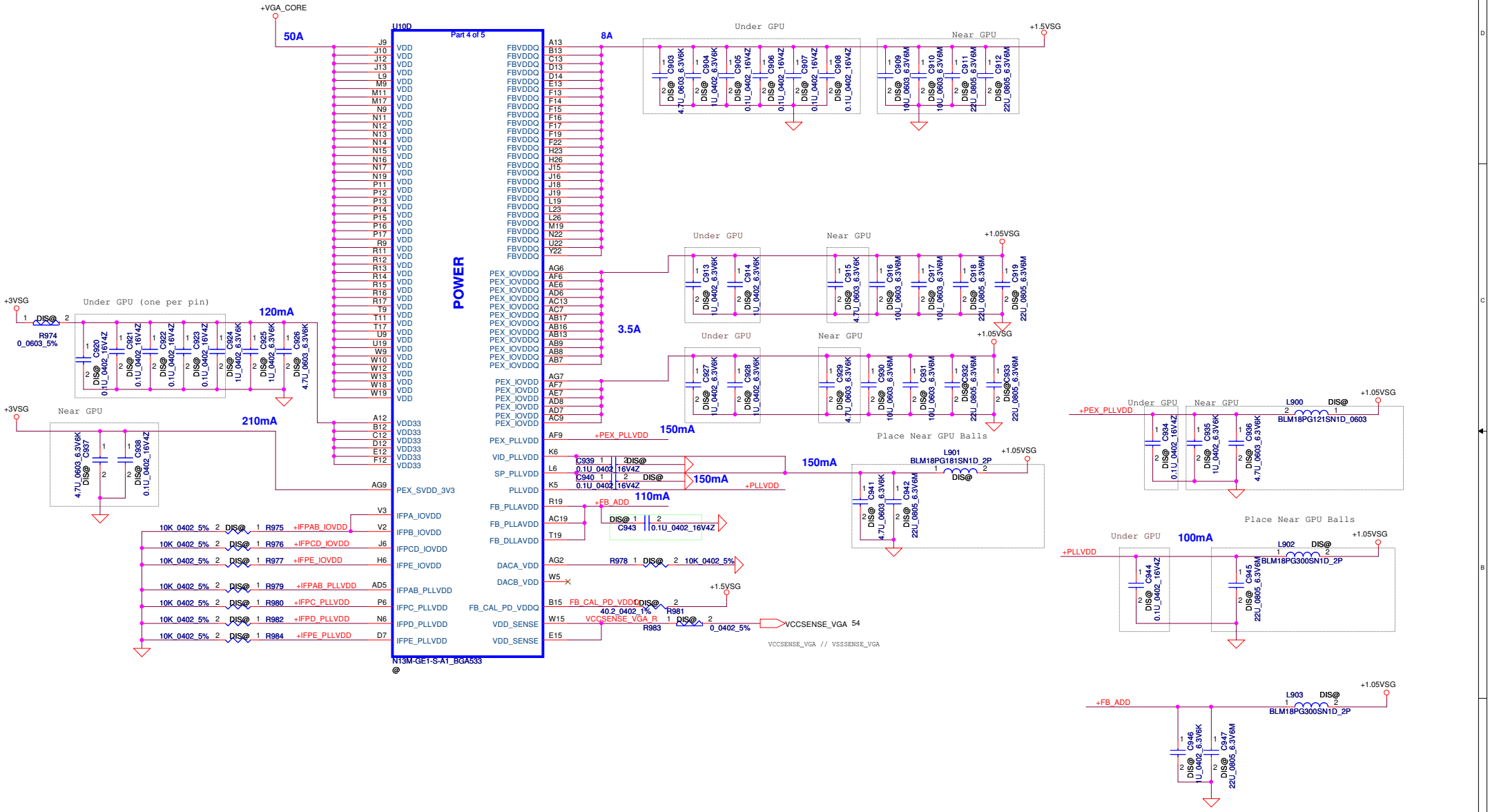

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Title	N13M POWER & GND 4/9		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 23 of 58		

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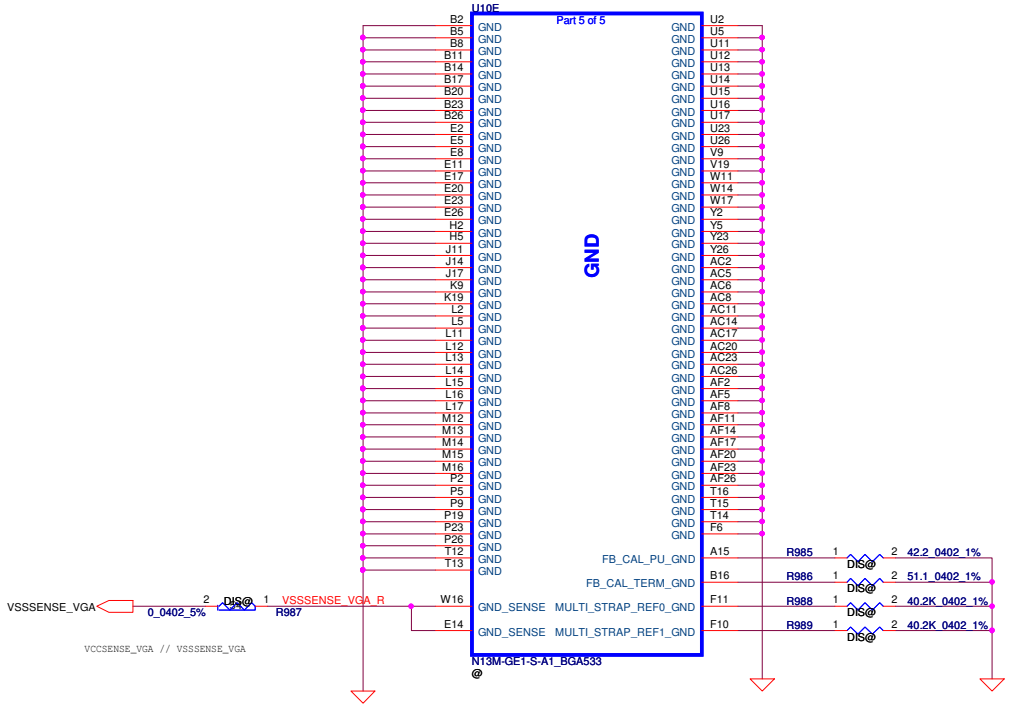

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Issued Date	2011/07/12	Deciphered Date	2012/12/31

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Title: N13M POWER & GND 5/9		
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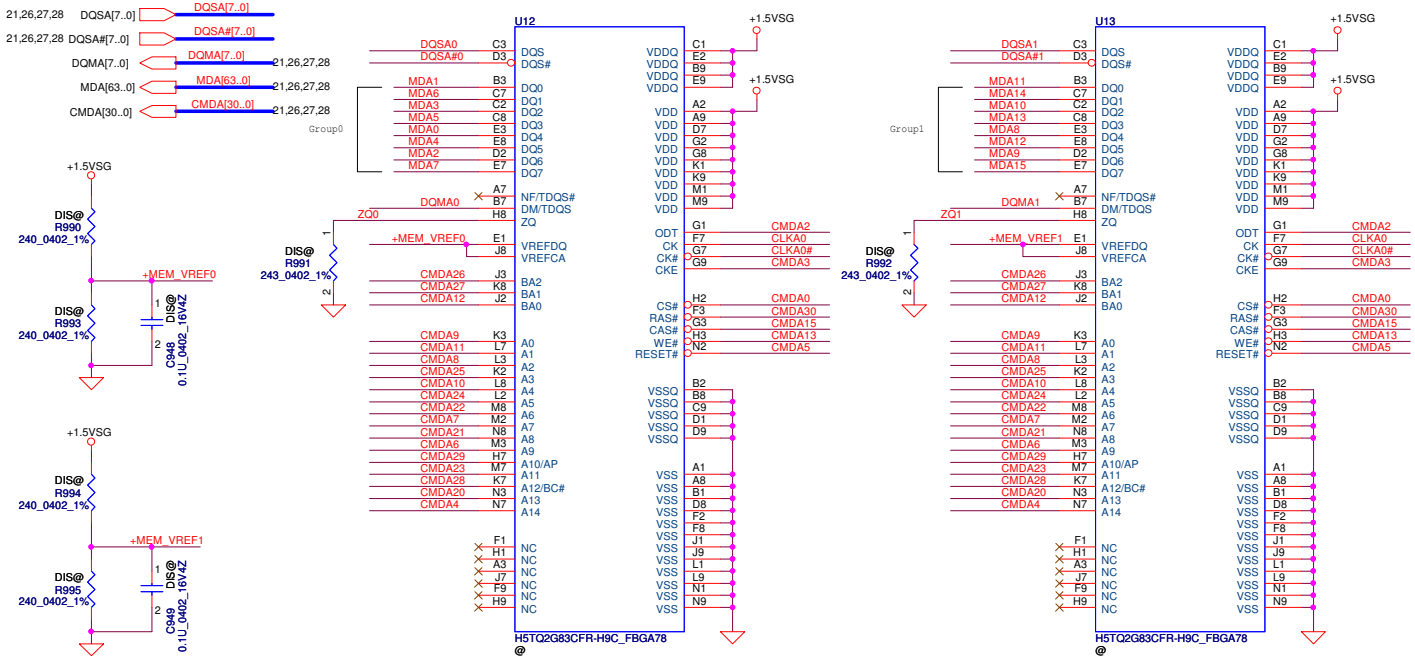
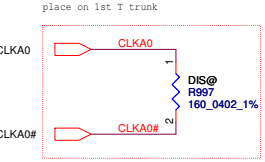
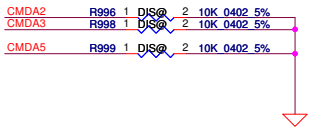
VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB

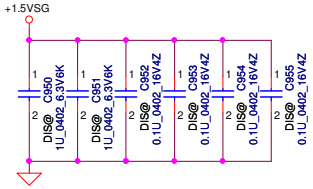


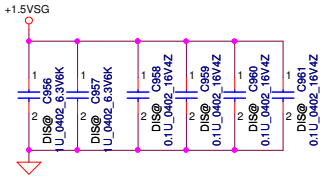
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH





	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)

Elpida : SAxxxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxx)

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Title	N13M DDR3 6/9
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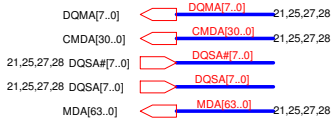
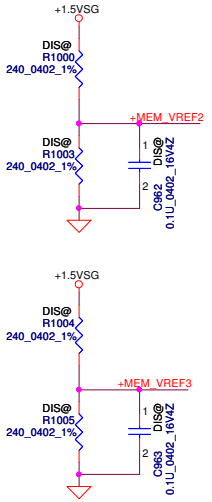
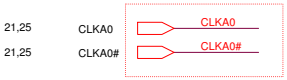
Date: Monday, July 09, 2012	Sheet 25 of 58

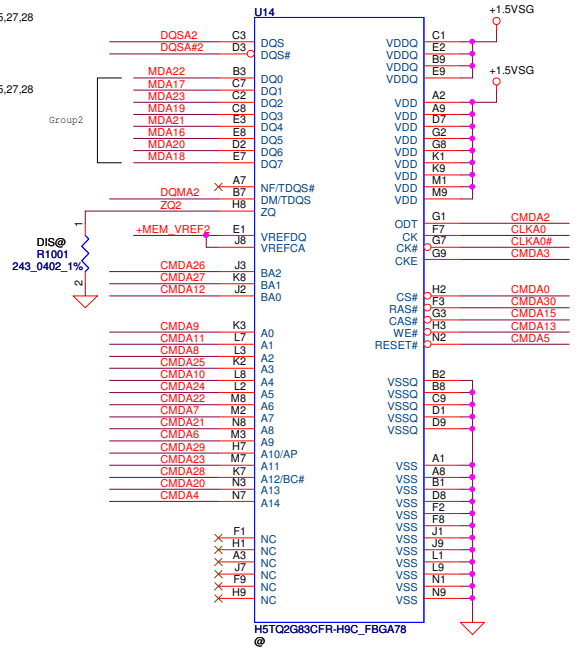
VRAM DDR3 chips

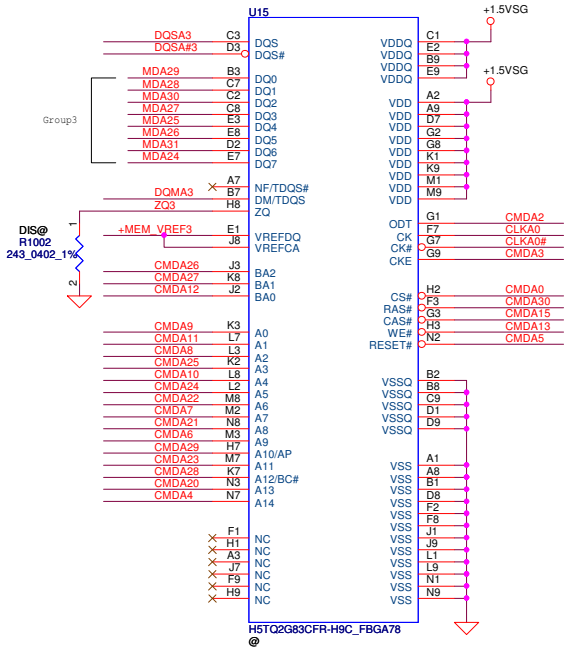
256Mx8 DDR3 *8==>2GB



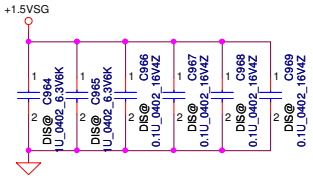


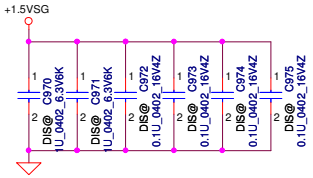






Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH





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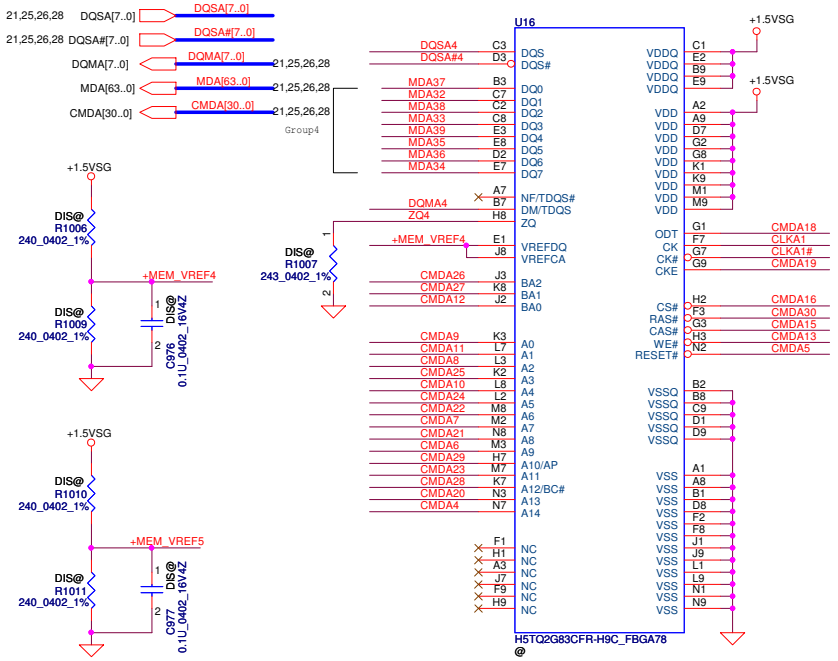
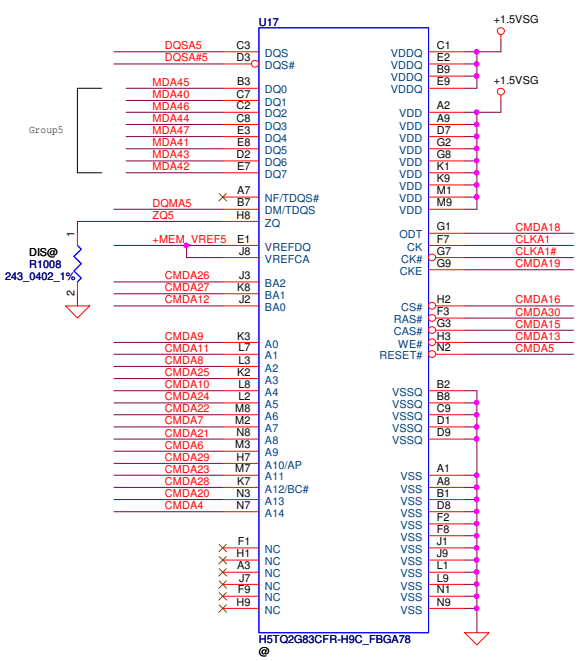
Title	N13M DDR3 7/9		
Size	Document Number		Rev
Custom	LA-8226P		1.0
Date:	Monday, July 09, 2012	Sheet	26 of 58

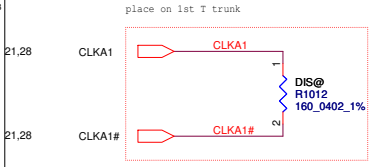
VRAM DDR3 chips

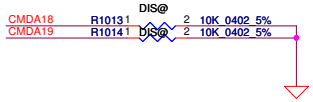
256Mx8 DDR3 *8==>2GB

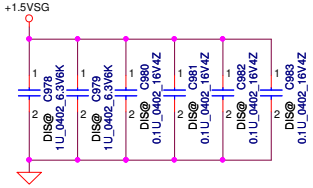
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

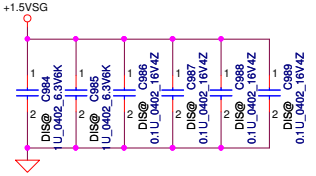












Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)

Elpida : SAxxxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxx)

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Custom	LA-8226P		1.0
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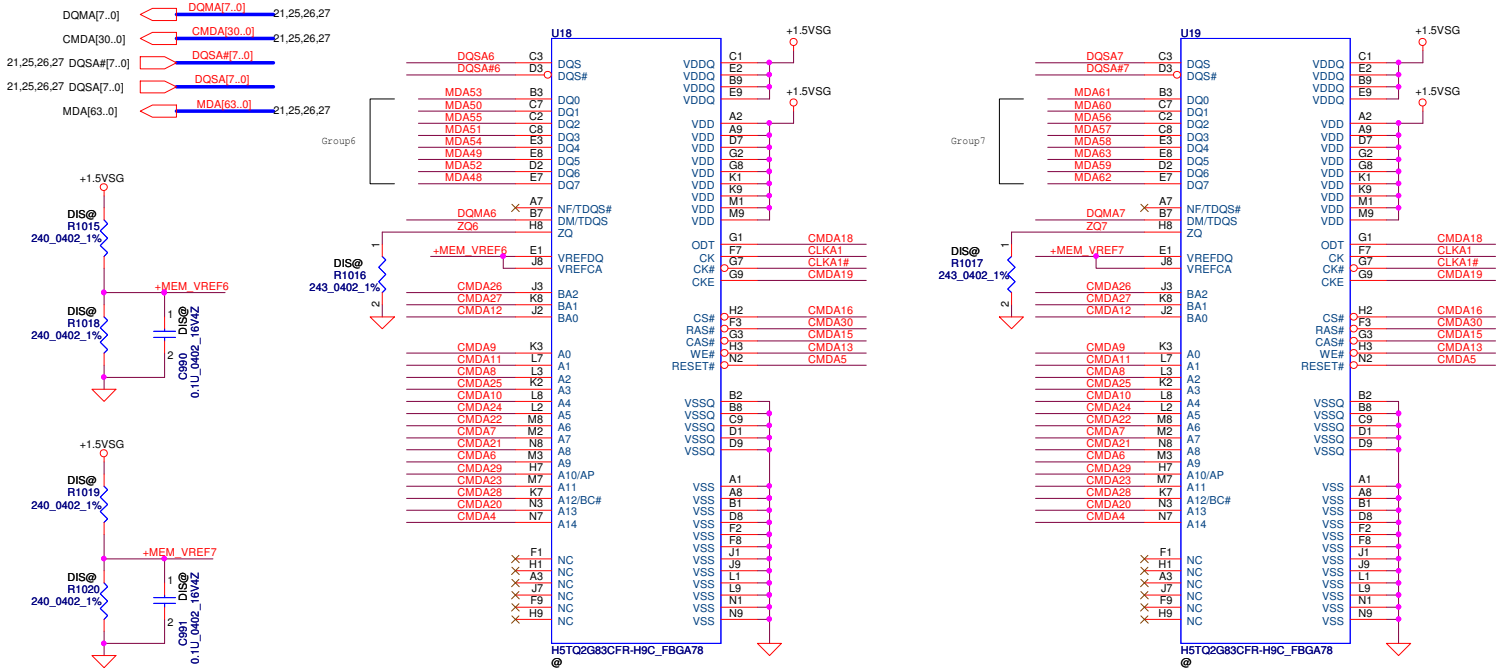
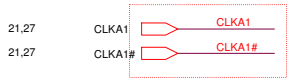
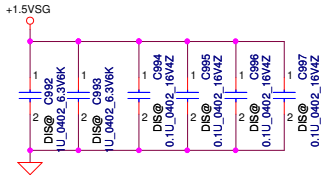
VRAM DDR3 chips

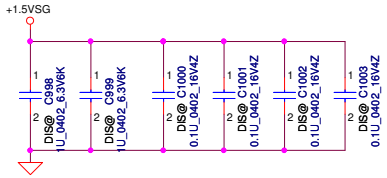
256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH







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Compal Electronics, Inc.	
Title	N13M DDR3 9/9
Size: Custom	Document Number: LA-8226P
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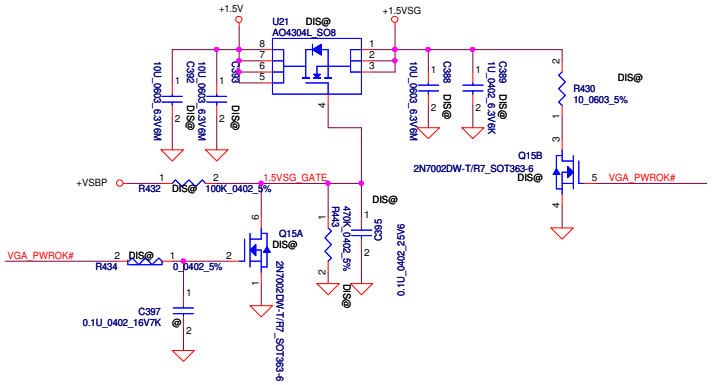
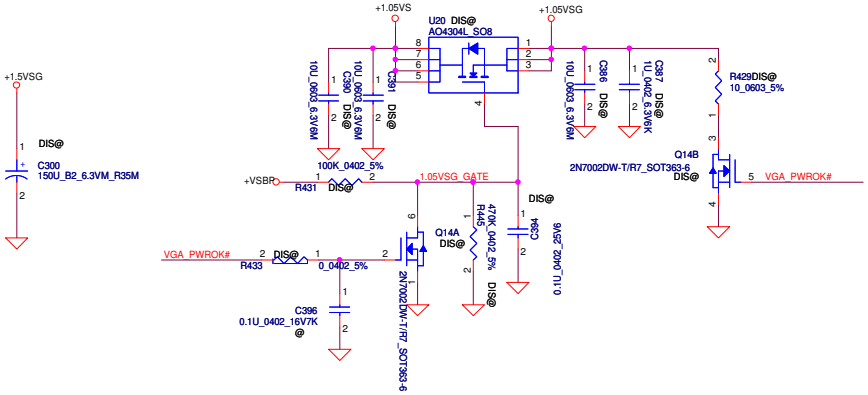
Date: Monday, July 09, 2012	Sheet 28 of 58

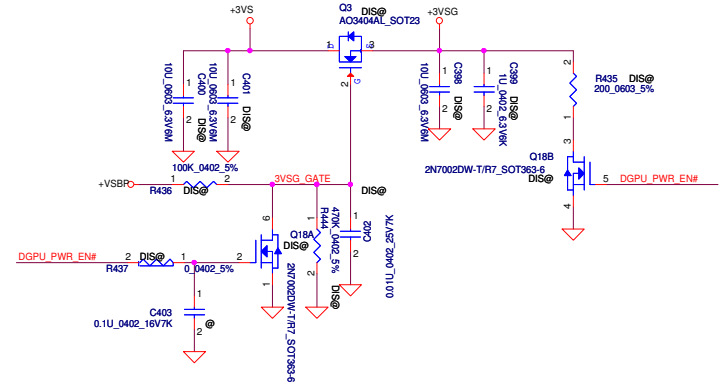
+1.5V to +1.5VSG

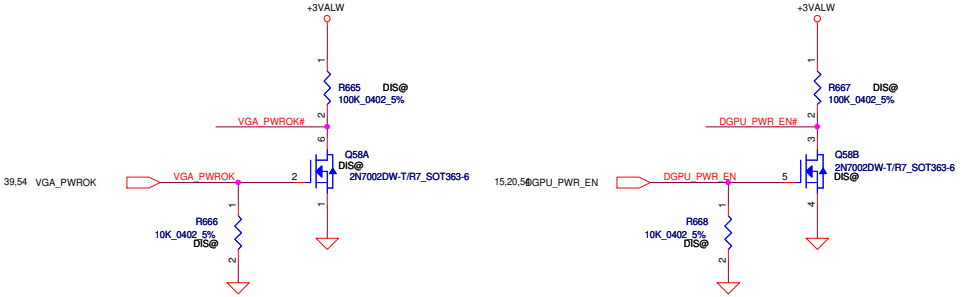


+VCCP to +1.05VSG



+3VS to +3VSG





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Compal Electronics, Inc.			
Title	PCH (2/8) PCIE, SMBUS, CLK		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
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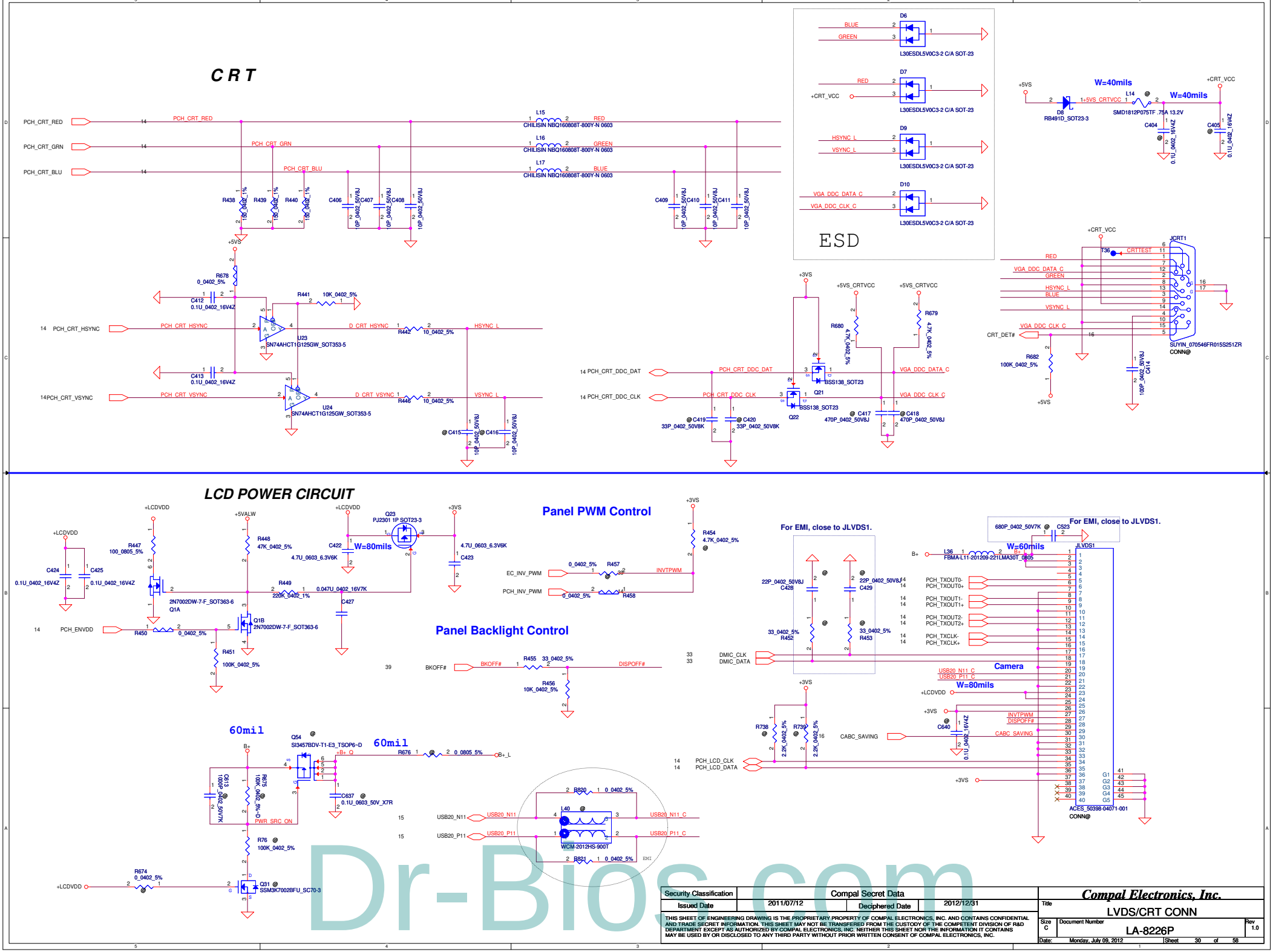
CRT
PCH_CRT_RED
PCH_CRT_GRN
PCH_CRT_BLU
PCH_CRT_HSYNC
PCH_CRT_VSYNC
L15 CHILISIN NBQ160808T-800Y-N 0603
L16 CHILISIN NBQ160808T-800Y-N 0603
L17 CHILISIN NBQ160808T-800Y-N 0603
R438 150_0402_1%
R439 150_0402_1%
R440 150_0402_1%
C406 10P_0402_50V8J
C407 10P_0402_50V8J
C408 10P_0402_50V8J
C409 10P_0402_50V8J
C410 10P_0402_50V8J
C411 10P_0402_50V8J
+5VS
R678 0_0402_5%
C412 0.1U_0402_16V4Z
R441 10K_0402_5%
U23 SN74AHCT1G125GW_SOT353-5
D_CRT_HSYNC
R442 10_0402_5%
HSYNC_L
C413 0.1U_0402_16V4Z
U24 SN74AHCT1G125GW_SOT353-5
D_CRT_VSYNC
R443 10_0402_5%
VSYNC_L
@C415 10P_0402_50V8J
@C416 10P_0402_50V8J
ESD
D6 L30ESDL5V0C3-2 C/A SOT-23
D7 L30ESDL5V0C3-2 C/A SOT-23
D9 L30ESDL5V0C3-2 C/A SOT-23
D10 L30ESDL5V0C3-2 C/A SOT-23
BLUE
GREEN
RED
+CRT_VCC
HSYNC_L
VSYNC_L
VGA_DDC_DATA_C
VGA_DDC_CLK_C
+5VS
W=40mils
D8 RB491D_SOT23-3
+5VS_CRTVCC
L14 SMD1812P075TF .75A 13.2V
C404 0.1U_0402_16V4Z
C405 0.1U_0402_16V4Z
+3VS
R680 4.7K_0402_5%
R679 4.7K_0402_5%
PCH_CRT_DDC_DAT
PCH_CRT_DDC_CLK
BSS138_SOT23
Q21
Q22
@C419 33P_0402_50V8K
@C420 33P_0402_50V8K
@C417 470P_0402_50V8J
@C418 470P_0402_50V8J
JCRT1
CRTTEST
CRT_DET#
R682 100K_0402_5%
C414 100P_0402_50V8J
SUYIN_070546FR015S251ZR
CONN@
LCD POWER CIRCUIT
+LCDVDD
+5VALW
R447 100_0805_5%
R448 47K_0402_5%
4.7U_0603_6.3V6K
C422
W=80mils
Q23 PJ2301 1P SOT23-3
C423
C424 0.1U_0402_16V4Z
C425 0.1U_0402_16V4Z
2N7002DW-7-F_SOT363-6
Q1A
R449 220K_0402_1%
0.047U_0402_16V7K
C427
PCH_ENVDD
R450 0_0402_5%
Q1B 2N7002DW-7-F_SOT363-6
R451 100K_0402_5%
Panel PWM Control
R454 4.7K_0402_5%
EC_INV_PWM
PCH_INV_PWM
R457
R458
INVTPWM
Panel Backlight Control
BKOFF#
R455 33_0402_5%
R456 10K_0402_5%
DISPOFF#
For EMI, close to JLVDS1.
22P_0402_50V8J C428
22P_0402_50V8J C429
33_0402_5% R452
33_0402_5% R453
DMIC_CLK
DMIC_DATA
680P_0402_50V7K @ C523
W=60mils
L36 FBMA-L11-201209-221LMA30T_0805
JLVDS1
PCH_TXOUT0-
PCH_TXOUT0+
PCH_TXOUT1-
PCH_TXOUT1+
PCH_TXOUT2-
PCH_TXOUT2+
PCH_TXCLK-
PCH_TXCLK+
Camera
USB20_N11_C
USB20_P11_C
W=80mils
R738 2.2K_0402_5%
R739 2.2K_0402_5%
CABC_SAVING
C640 0.1U_0402_16V4Z
PCH_LCD_CLK
PCH_LCD_DATA
ACES_50398-04071-001
CONN@
60mil
Q54 SI3457BDV-T1-E3_TSOP6-D
R676 0_0805_5%
B+_L
C613 1000P_0402_50V7K
R675 100K_0402_5%
C637 @ 0.1U_0603_50V_X7R
PWR_SRC_ON
R76 @ 100K_0402_5%
R674 0_0402_5%
Q31 @ SSM3K7002BFU_SC70-3
USB20_N11
USB20_P11
R820 0_0402_5%
R821 0_0402_5%
L40 @
WCM-2012HS-900T
EMI
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Security Classification
Compal Secret Data
Issued Date
2011/07/12
Deciphered Date
2012/12/31
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Compal Electronics, Inc.
Title
LVDS/CRT CONN
Size C
Document Number
LA-8226P
Rev 1.0
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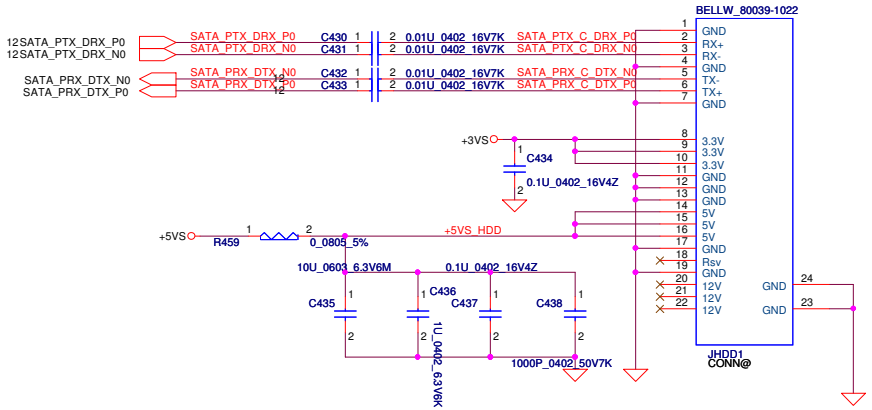
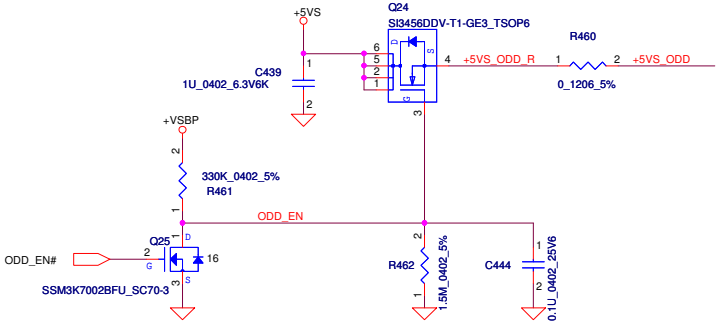
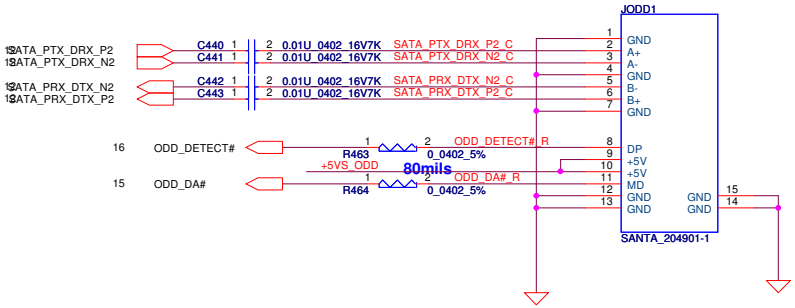
SATA HDD Conn.

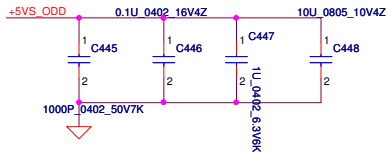




SATA ODD Conn.



Placea caps. near ODD CONN.



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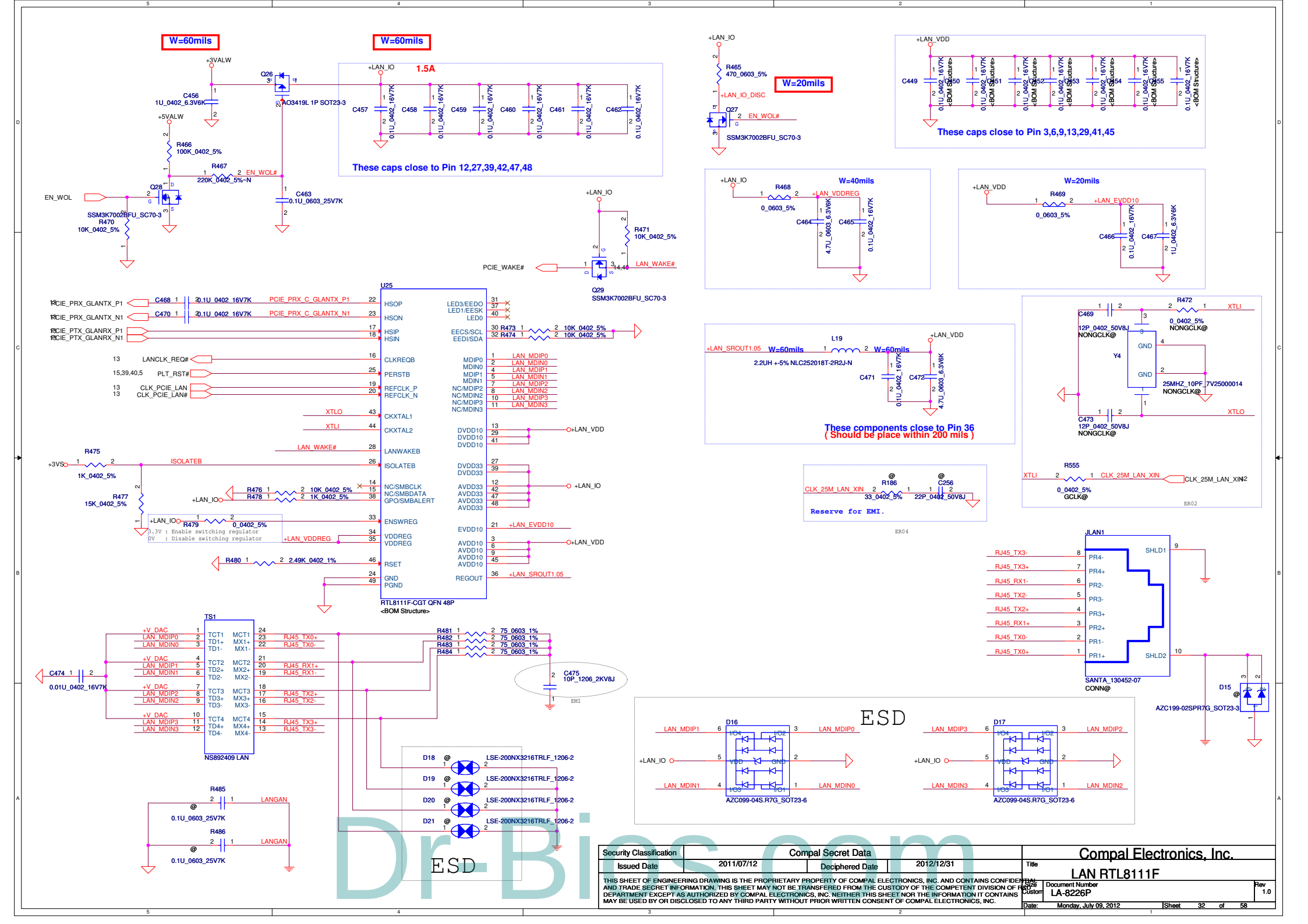
Compal Electronics, Inc.			
Title: HDD & ODD CONN			
Size: B	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 31 of 58		


W=60mils
W=60mils
1.5A
+3VALW
+5VALW
+LAN_IO
C456 1U_0402_6.3V6K
Q26 AO3419L 1P SOT23-3
C457 C458 C459 C460 C461 C462 0.1U_0402_16V7K
These caps close to Pin 12,27,39,42,47,48
R466 100K_0402_5%
R467 220K_0402_5%~N
EN_WOL#
Q28 SSM3K7002BFU_SC70-3
R470 10K_0402_5%
C463 0.1U_0603_25V7K
EN_WOL
R471 10K_0402_5%
Q29 SSM3K7002BFU_SC70-3
PCIE_WAKE#
LAN_WAKE#
R465 470_0603_5%
W=20mils
+LAN_IO_DISC
Q27 SSM3K7002BFU_SC70-3
EN_WOL#
+LAN_VDD
C449 C450 C451 C452 C453 C454 C455 0.1U_0402_16V7K
<BOM Structure>
These caps close to Pin 3,6,9,13,29,41,45
W=40mils
R468 0_0603_5%
+LAN_VDDREG
C464 4.7U_0603_6.3V6K
C465 0.1U_0402_16V7K
W=20mils
R469 0_0603_5%
+LAN_EVDD10
C466 0.1U_0402_16V7K
C467 1U_0402_6.3V6K
U25
RTL8111F-CGT QFN 48P
<BOM Structure>
PCIE_PRX_GLANTX_P1
PCIE_PRX_GLANTX_N1
PCIE_PTX_GLANRX_P1
PCIE_PTX_GLANRX_N1
C468 0.1U_0402_16V7K
C470 0.1U_0402_16V7K
PCIE_PRX_C_GLANTX_P1
PCIE_PRX_C_GLANTX_N1
HSOP
HSON
HSIP
HSIN
LANCLK_REQ#
PLT_RST#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLKREQB
PERSTB
REFCLK_P
REFCLK_N
XTLO
XTLI
CKXTAL1
CKXTAL2
LAN_WAKE#
LANWAKEB
ISOLATEB
NC/SMBCLK
NC/SMBDATA
GPO/SMBALERT
ENSWREG
VDDREG
RSET
GND
PGND
LED3/EEDO
LED1/EESK
LED0
EECS/SCL
EEDI/SDA
MDIP0
MDIN0
MDIP1
MDIN1
NC/MDIP2
NC/MDIN2
NC/MDIP3
NC/MDIN3
DVDD10
DVDD33
AVDD33
AVDD10
REGOUT
R473 10K_0402_5%
R474 10K_0402_5%
LAN_MDIP0
LAN_MDIN0
LAN_MDIP1
LAN_MDIN1
LAN_MDIP2
LAN_MDIN2
LAN_MDIP3
LAN_MDIN3
+LAN_VDD
+LAN_IO
+LAN_EVDD10
+LAN_VDDREG
+LAN_SROUT1.05
R475 1K_0402_5%
R476 10K_0402_5%
R477 15K_0402_5%
R478 1K_0402_5%
R479 0_0402_5%
3.3V : Enable switching regulator
0V : Disable switching regulator
R480 2.49K_0402_1%
+3VS
L19
+LAN_SROUT1.05
W=60mils
W=60mils
2.2UH +-5% NLC252018T-2R2J-N
C471 0.1U_0402_16V7K
C472 4.7U_0603_6.3V6K
These components close to Pin 36
(Should be place within 200 mils)
R472 0_0402_5%
NONGCLK@
C469 12P_0402_50V8J
C473 12P_0402_50V8J
Y4
25MHZ_10PF_7V25000014
XTLI
XTLO
R555 0_0402_5%
GCLK@
CLK_25M_LAN_XIN
CLK_25M_LAN_XIN2
ER02
R186
C256 22P_0402_50V8J
33_0402_5%
Reserve for EMI.
ER04
JLAN1
SANTA_130452-07
CONN@
RJ45_TX3-
RJ45_TX3+
RJ45_RX1-
RJ45_TX2-
RJ45_TX2+
RJ45_RX1+
RJ45_TX0-
RJ45_TX0+
PR4-
PR4+
PR2-
PR3-
PR3+
PR2+
PR1-
PR1+
SHLD1
SHLD2
D15 AZC199-02SPR7G_SOT23-3
TS1
NS892409 LAN
+V_DAC
TCT1 MCT1
TD1+ MX1+
TD1- MX1-
TCT2 MCT2
TD2+ MX2+
TD2- MX2-
TCT3 MCT3
TD3+ MX3+
TD3- MX3-
TCT4 MCT4
TD4+ MX4+
TD4- MX4-
RJ45_TX0+
RJ45_TX0-
RJ45_RX1+
RJ45_RX1-
RJ45_TX2+
RJ45_TX2-
RJ45_TX3+
RJ45_TX3-
C474 0.01U_0402_16V7K
R481 R482 R483 R484 75_0603_1%
C475 10P_1206_2KV8J
EMI
D18 D19 D20 D21 LSE-200NX3216TRLF_1206-2
R485 0.1U_0603_25V7K
R486 0.1U_0603_25V7K
LANGAN
ESD
D16 AZC099-04S.R7G_SOT23-6
D17 AZC099-04S.R7G_SOT23-6
ESD
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Issued Date
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Compal Electronics, Inc.
Title
LAN RTL8111F
Size
Custom
Document Number
LA-8226P
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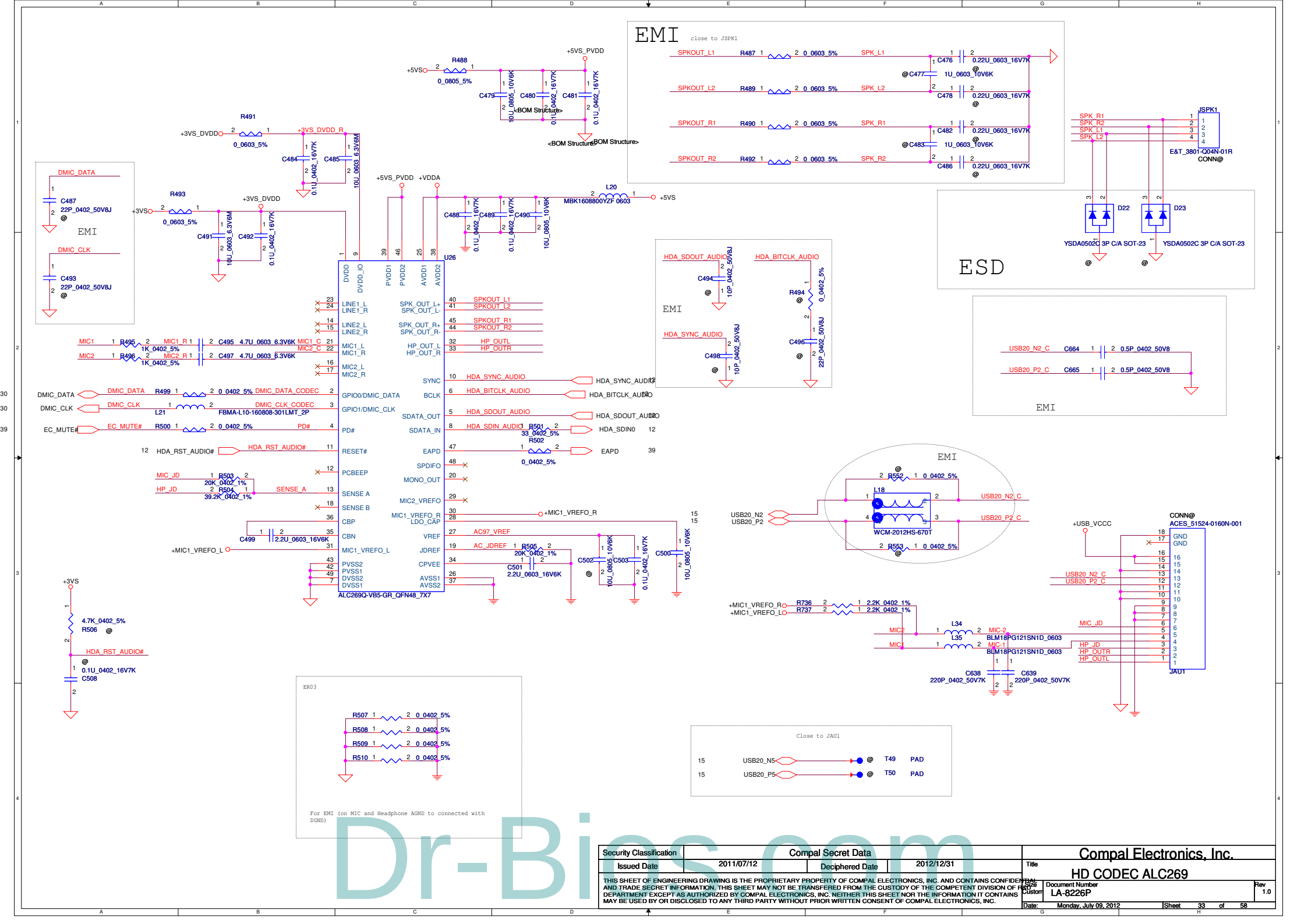

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Compal Electronics, Inc.			
Title	HD CODEC ALC269		
Size	Document Number	Rev	
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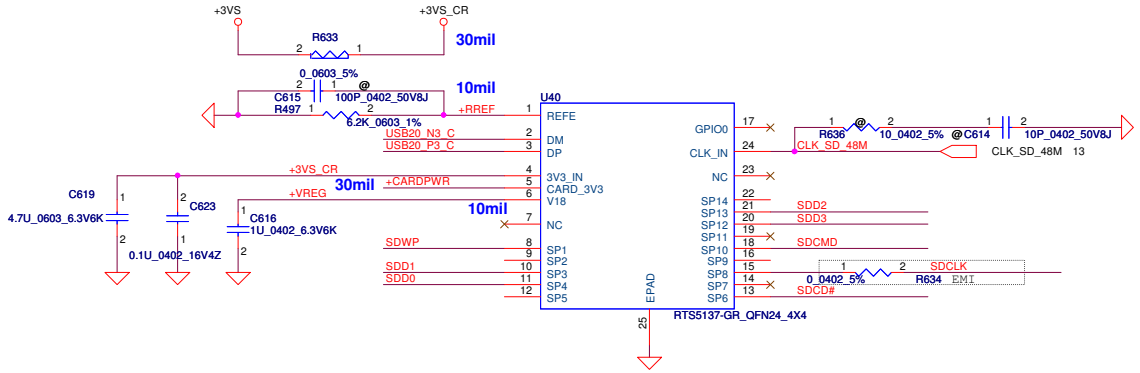
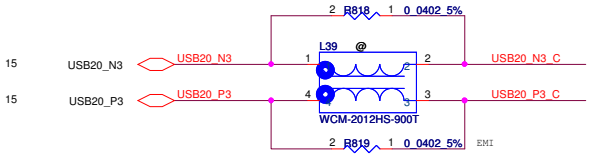
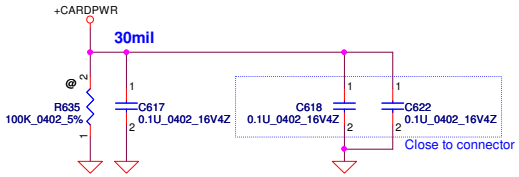
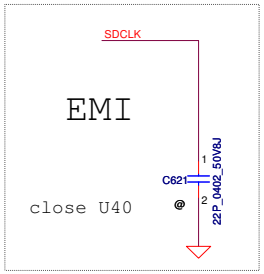
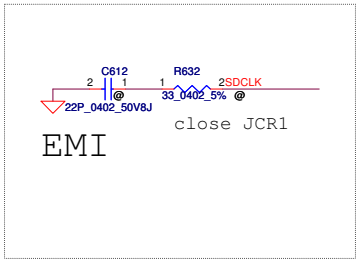
Card Reader Connector

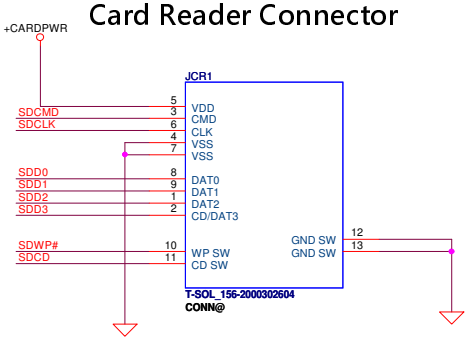


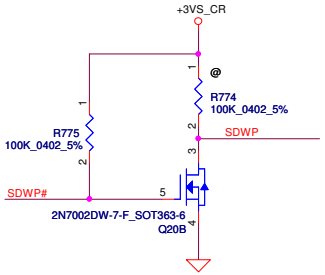


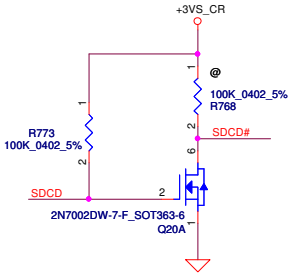












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Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

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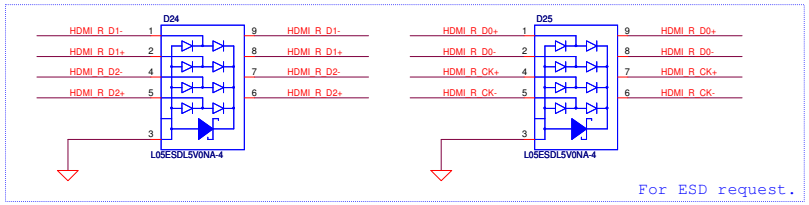
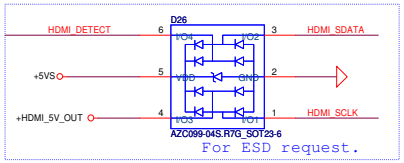
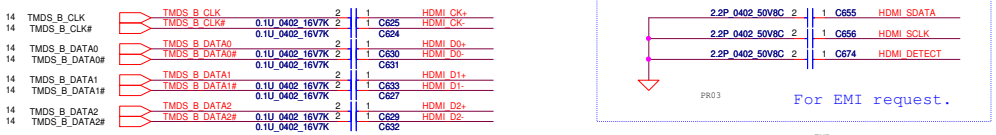
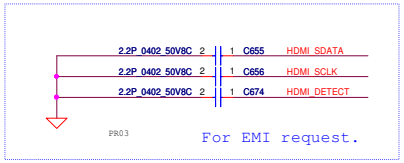
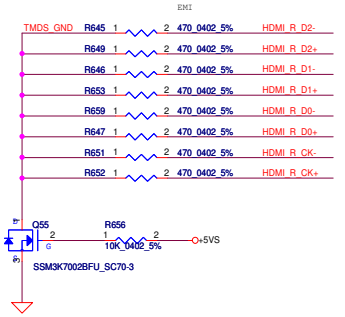
Compal Electronics, Inc.			
Title	RTS5137 Media Card Controller		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 34 of 58		

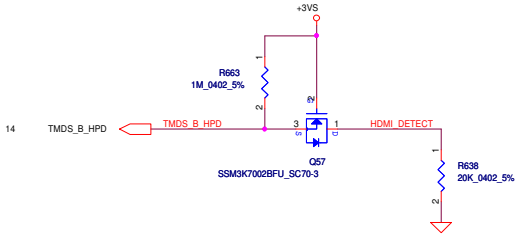


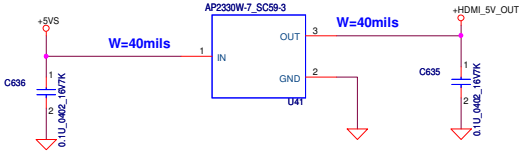


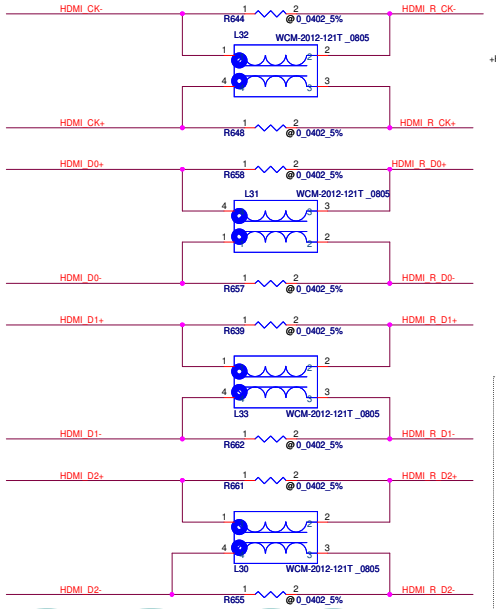


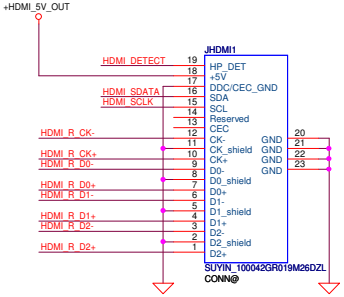


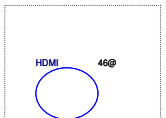


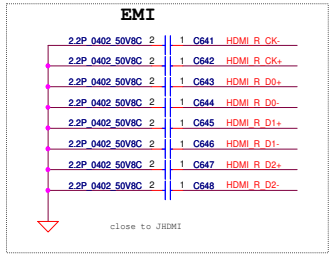


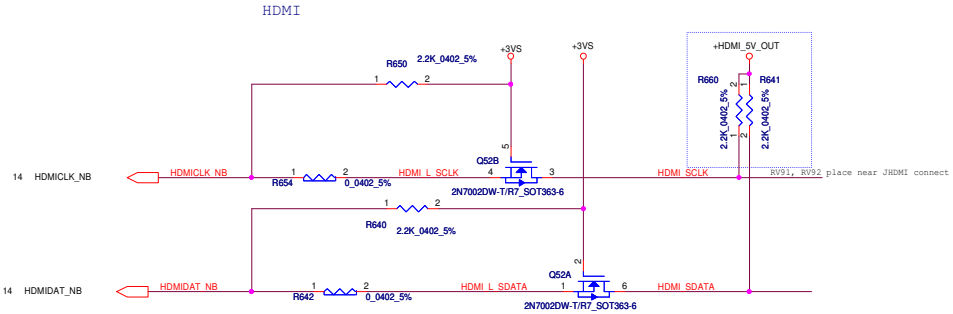












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Issued Date	2011/07/12	Deciphered Date	2012/12/31

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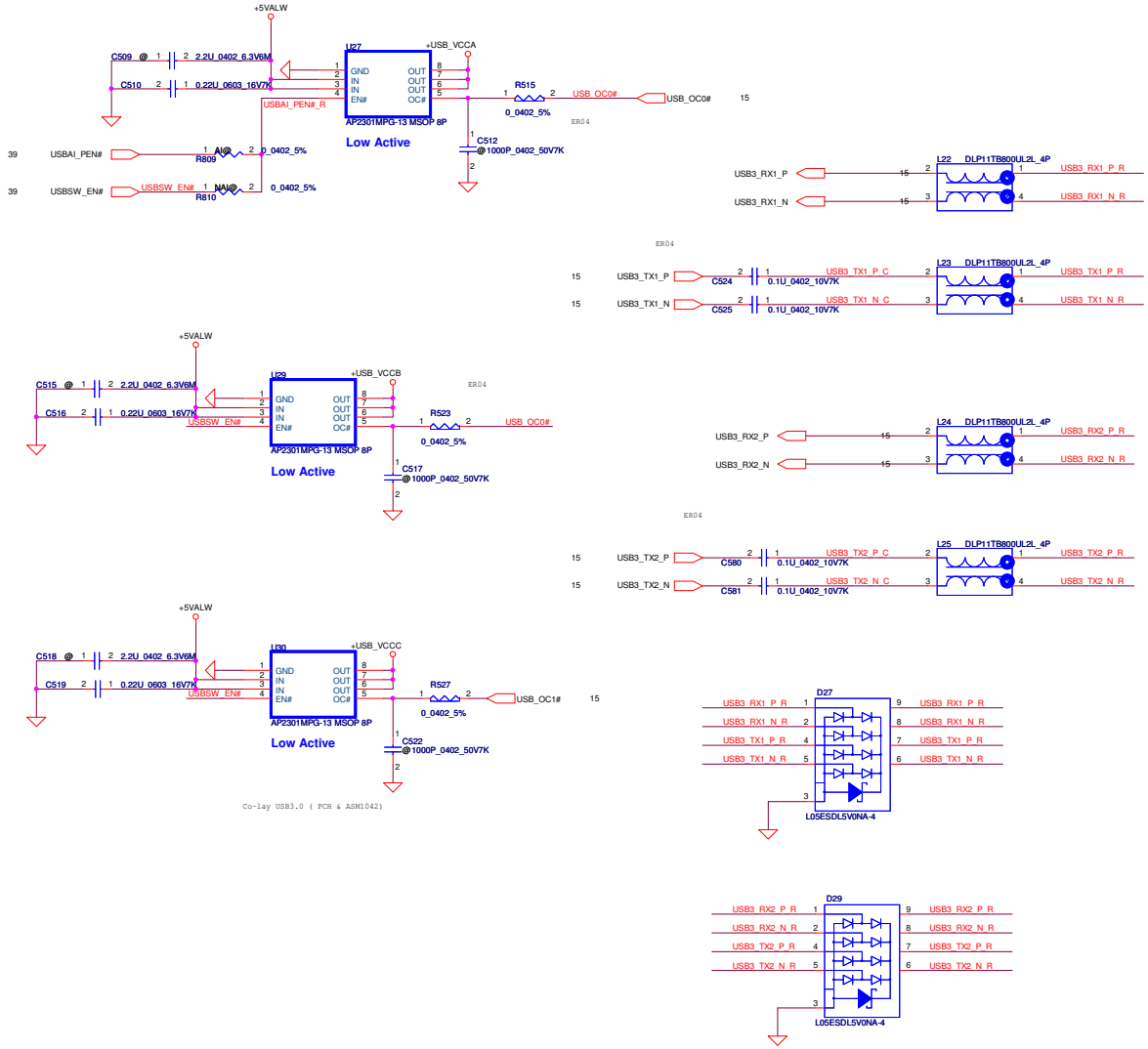
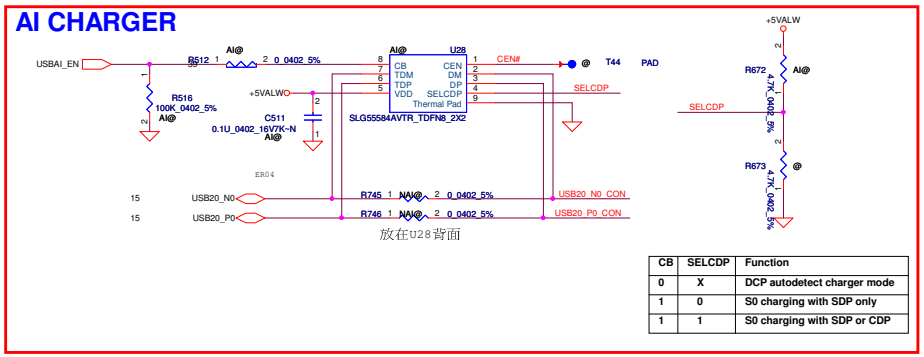
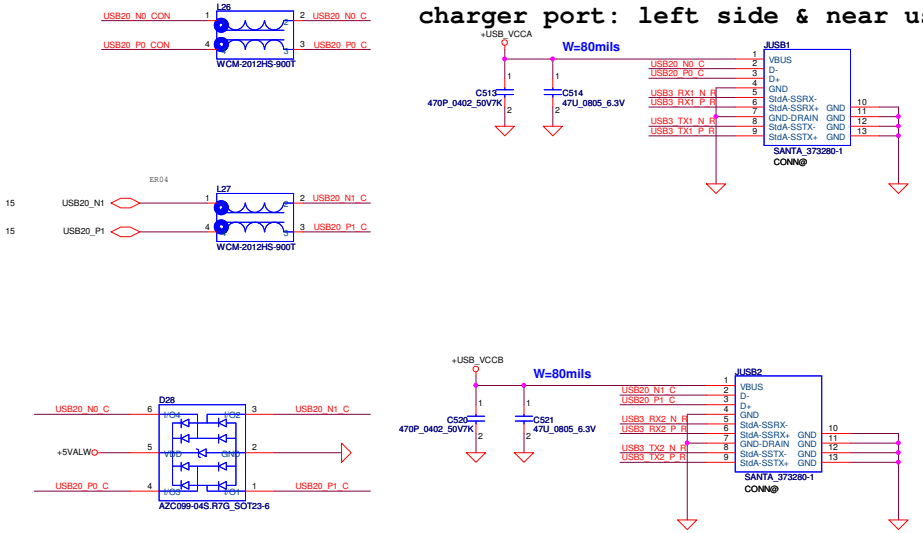
Compal Electronics, Inc.			
Title: HDMI Connector			
Size: C	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 35 of 58		



AI CHARGER



CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP



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Compal Electronics, Inc.

Title: USB2.0/USB3.0 CONN

Document Number: LA-8226P

Rev: 1.0

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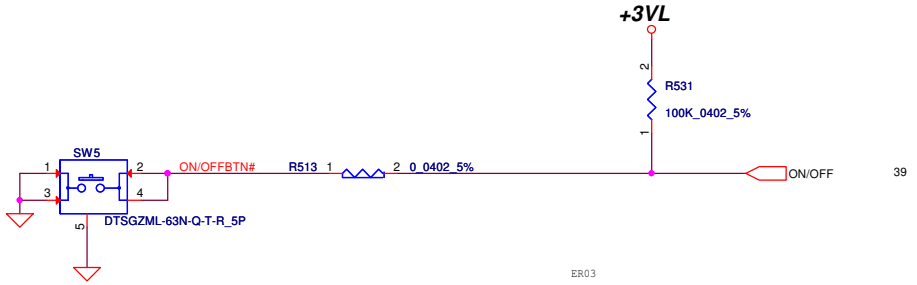
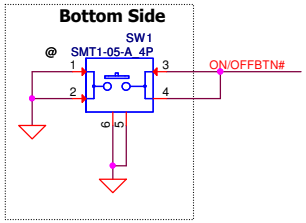
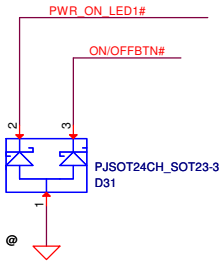
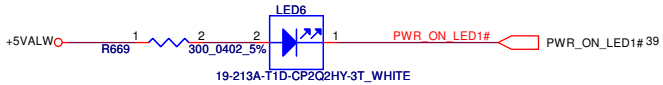
Power Button

ON/OFF switch

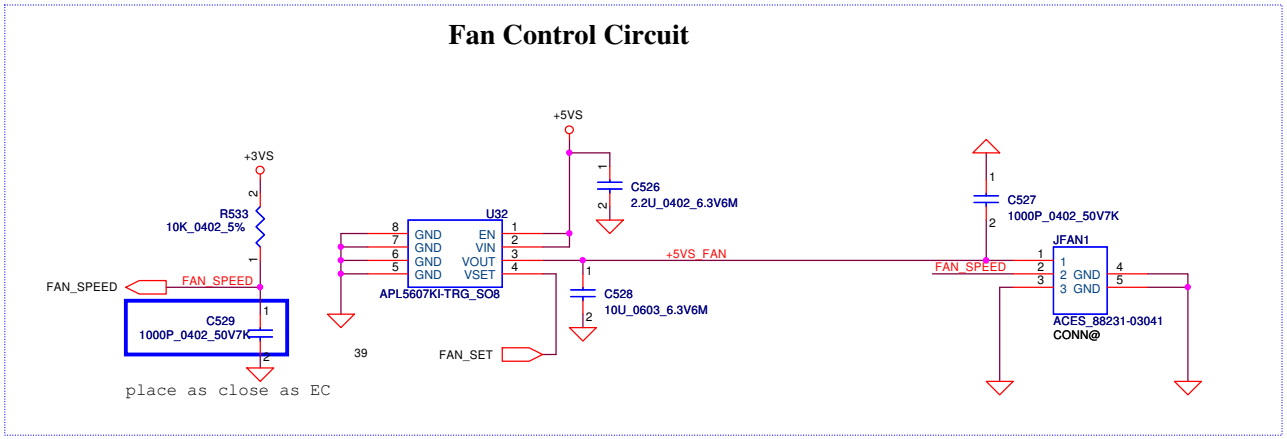




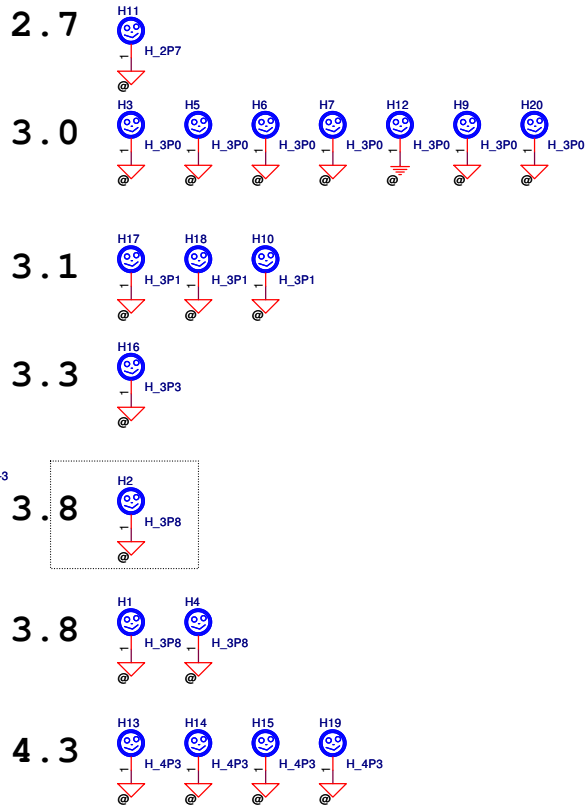




Fan Control Circuit



Screw Hole



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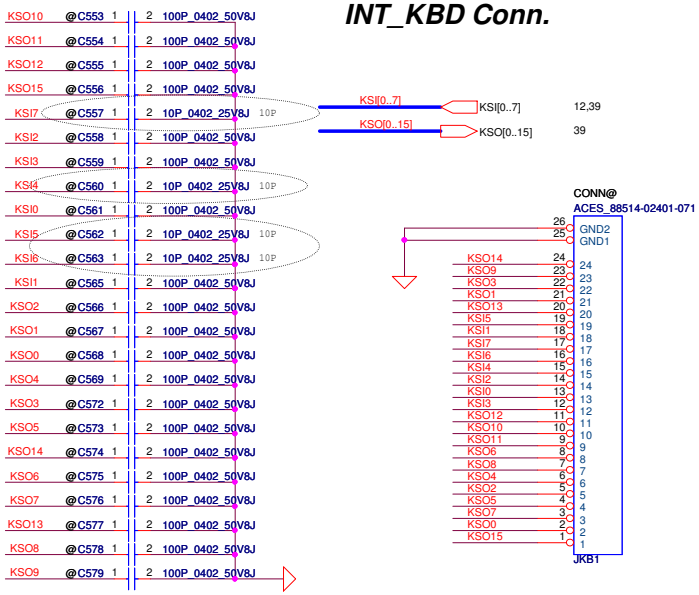
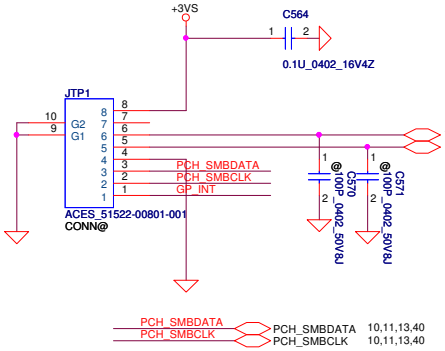
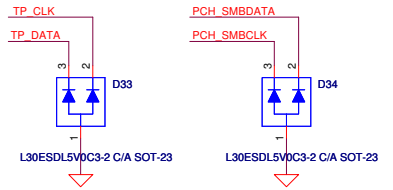
Compal Electronics, Inc.			
Title	PWRBTN/ FAN / Screws		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 37 of 58		

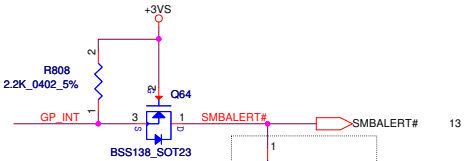
Touch/B Connector

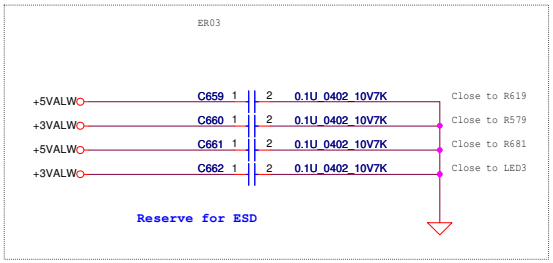
INT_KBD Conn.



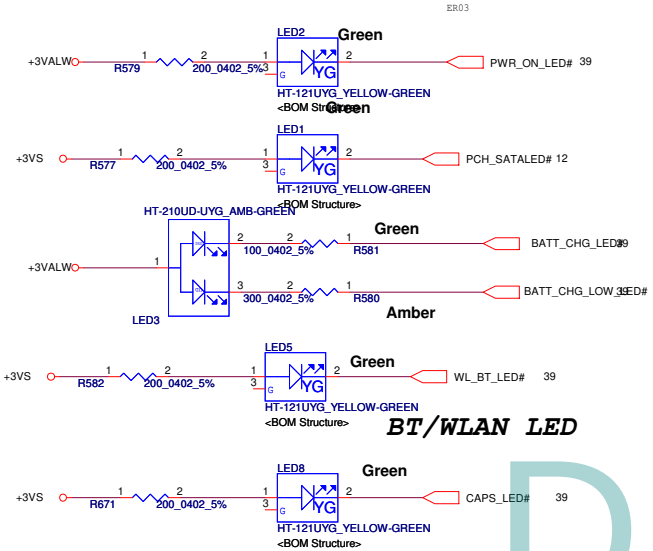




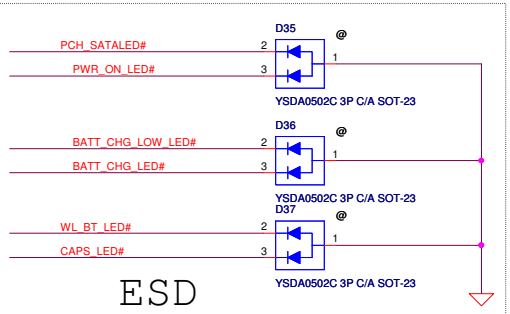


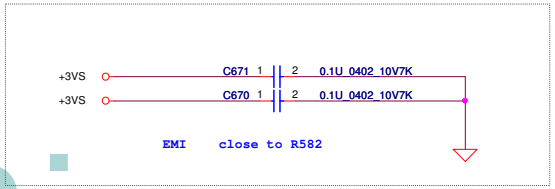


LED



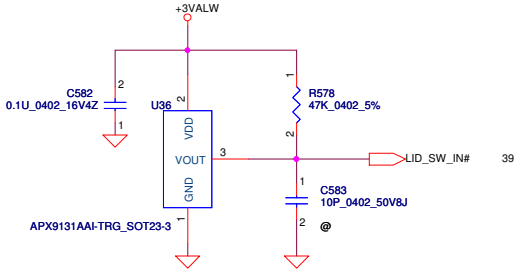
BT/WLAN LED





Lid Switch

(Hall Effect Switch)



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Issued Date	2011/07/12	Deciphered Date 2012/12/31	Title: KB/EC ROM/TP/FUN/LED
Size: B	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 38 of 58		

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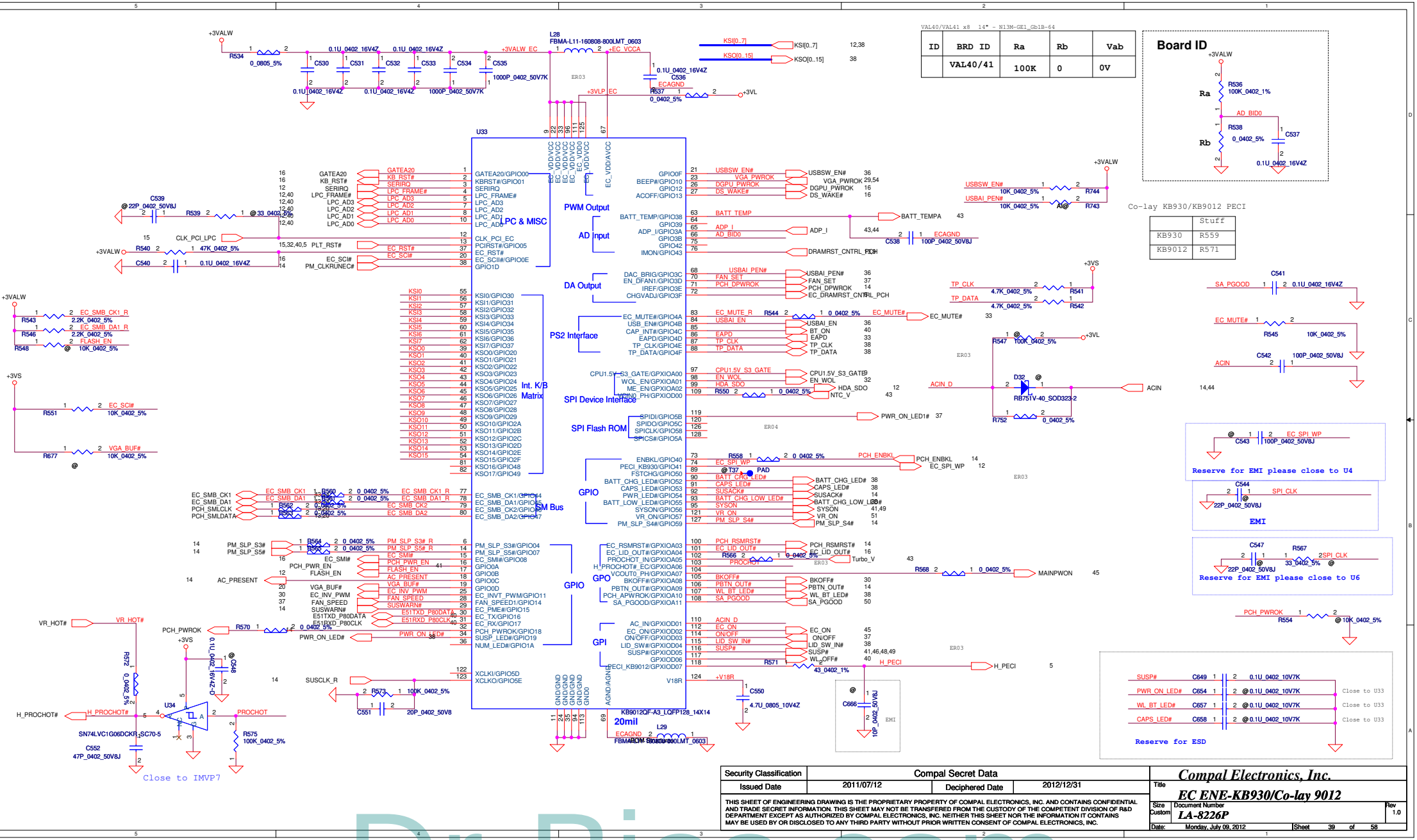

ID	BRD ID	Ra	Rb	Vab
	VAL40/41	100K	0	0V

	Stuff
KB930	R559
KB9012	R571

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: EC ENE-KB930/Co-lay 9012

Size: Custom | Document Number: LA-8226P | Rev: 1.0

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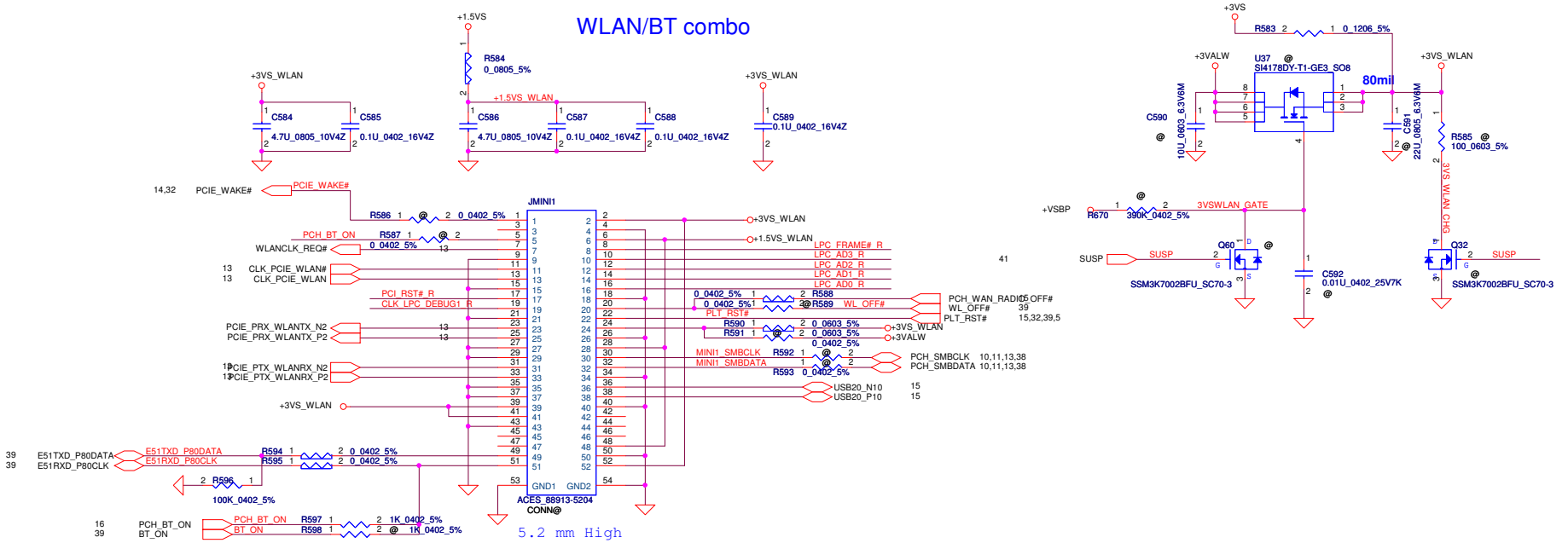
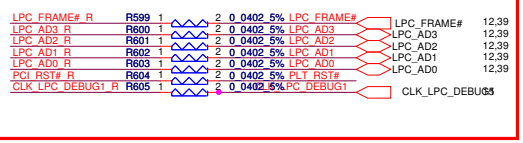
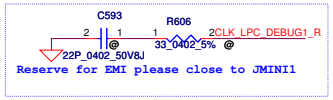
WLAN/BT combo



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





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Issued Date	2011/07/12	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: WLAN/ WWAN/ m-SATA

Size: Custom | Document Number: LA-8226P | Rev: 1.0

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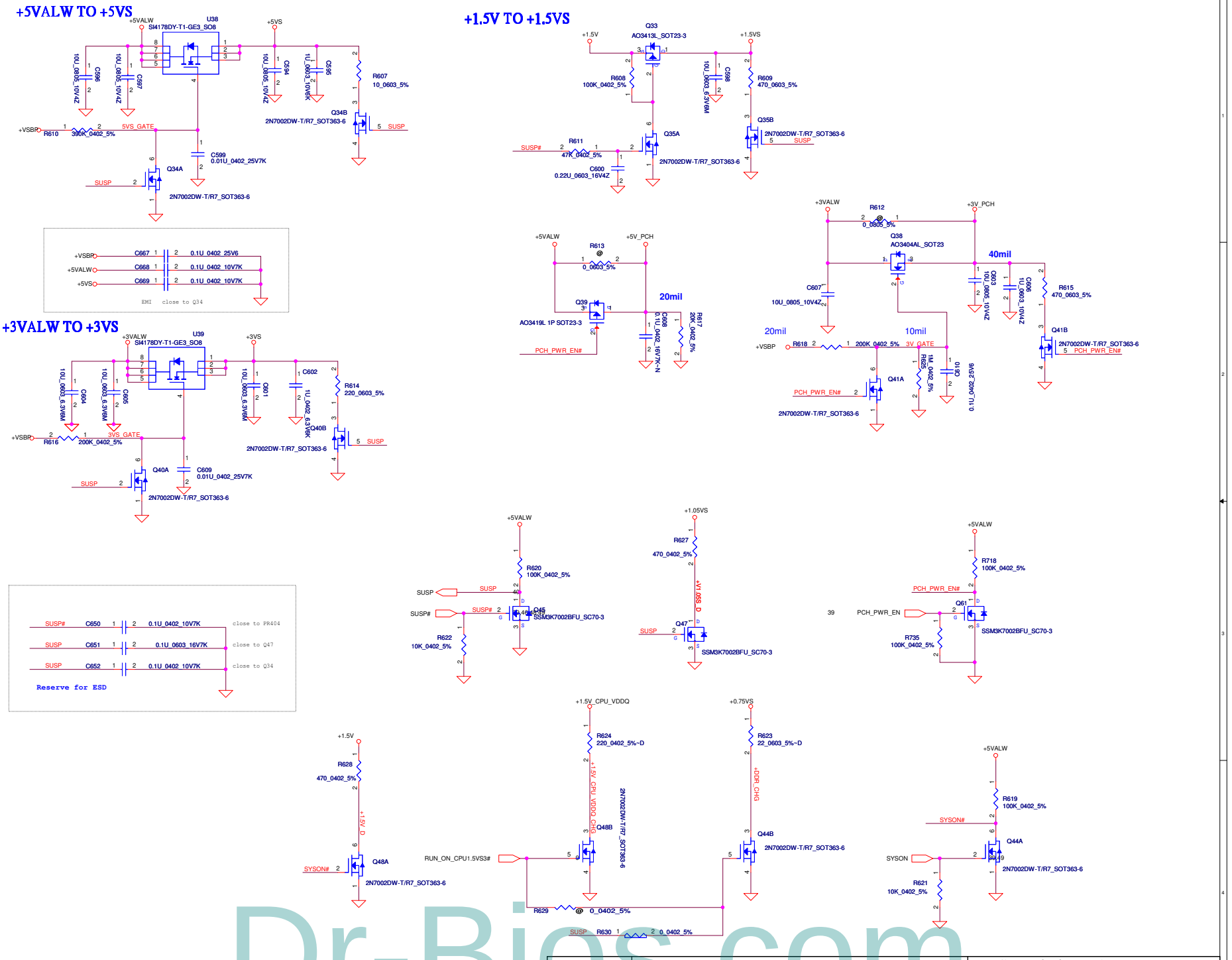

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Issued Date	2011/07/12	Deciphered Date	2012/12/31

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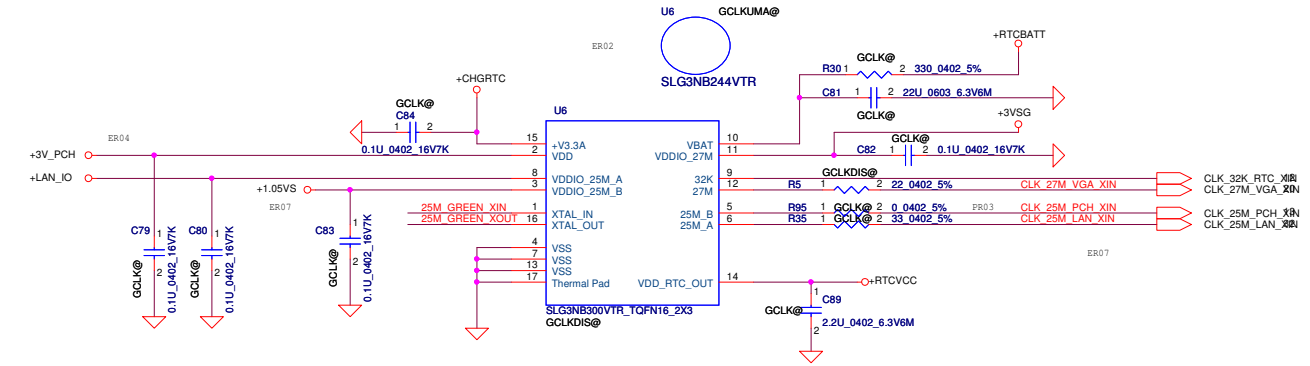
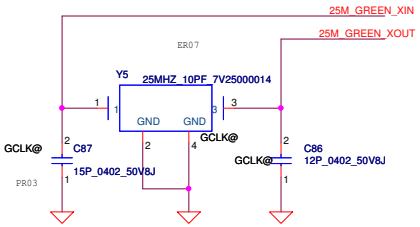
Compal Electronics, Inc.

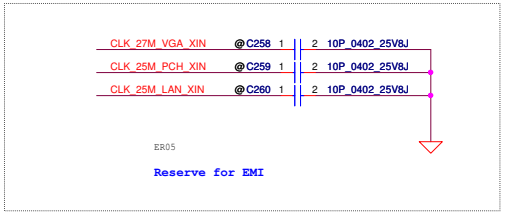
Title: DC/DC Interface

Size: Custom | Document Number: LA-8226P | Rev: 1.0

Date: Monday, July 09, 2012 | Sheet 41 of 58







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: Green CLK SLG3NB300VTR

Size: Custom | Document Number: LA-8226P | Rev: 1.0

Date: Friday, July 13, 2012 | Sheet 42 of 58

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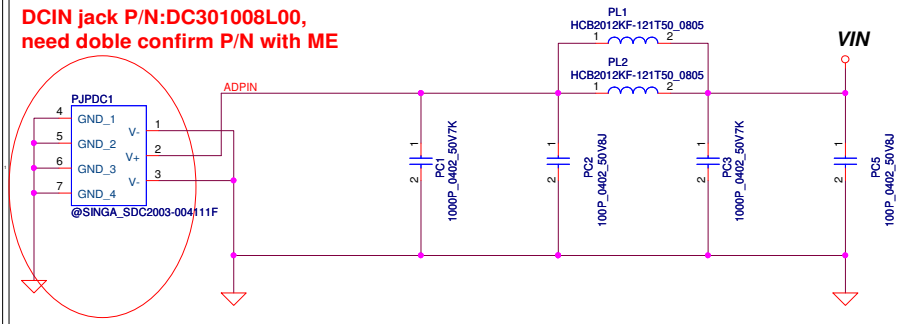
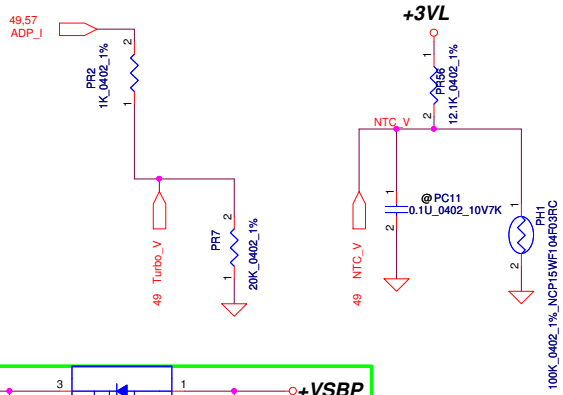
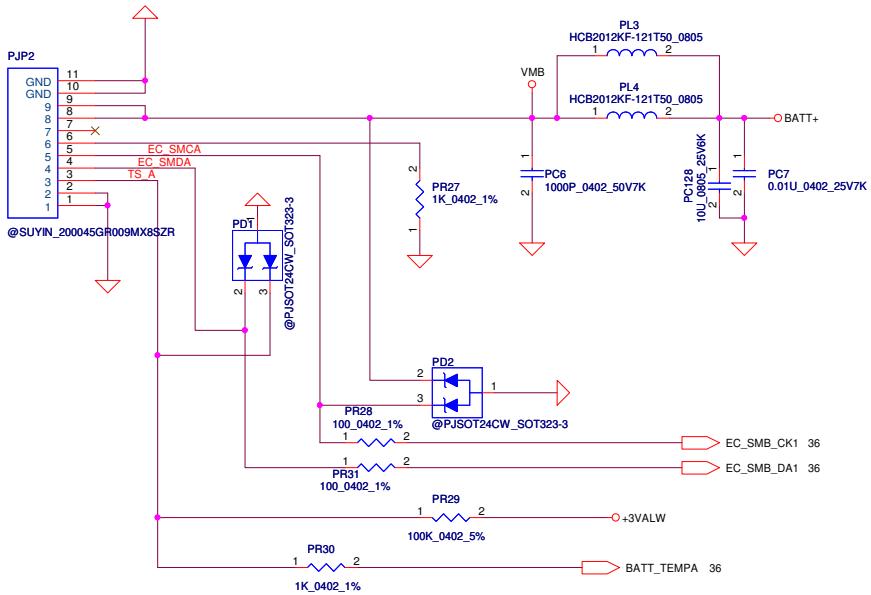
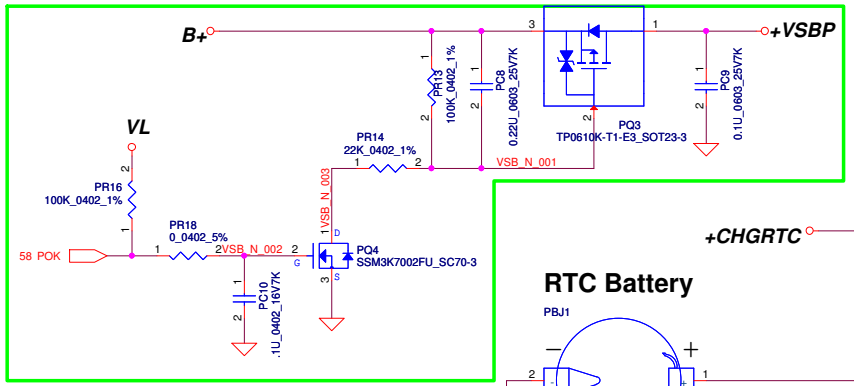
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

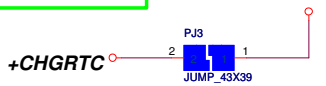


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

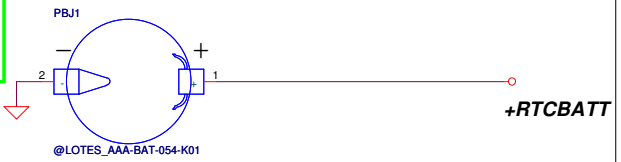








RTC Battery



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/01/23	Deciphered Date 2010/01/23	Title PWR-DCIN / BATT CONN / OTP
Size	Document Number LA-8226P		Rev 1.0
Date: Friday, July 13, 2012		Sheet 43 of 56	

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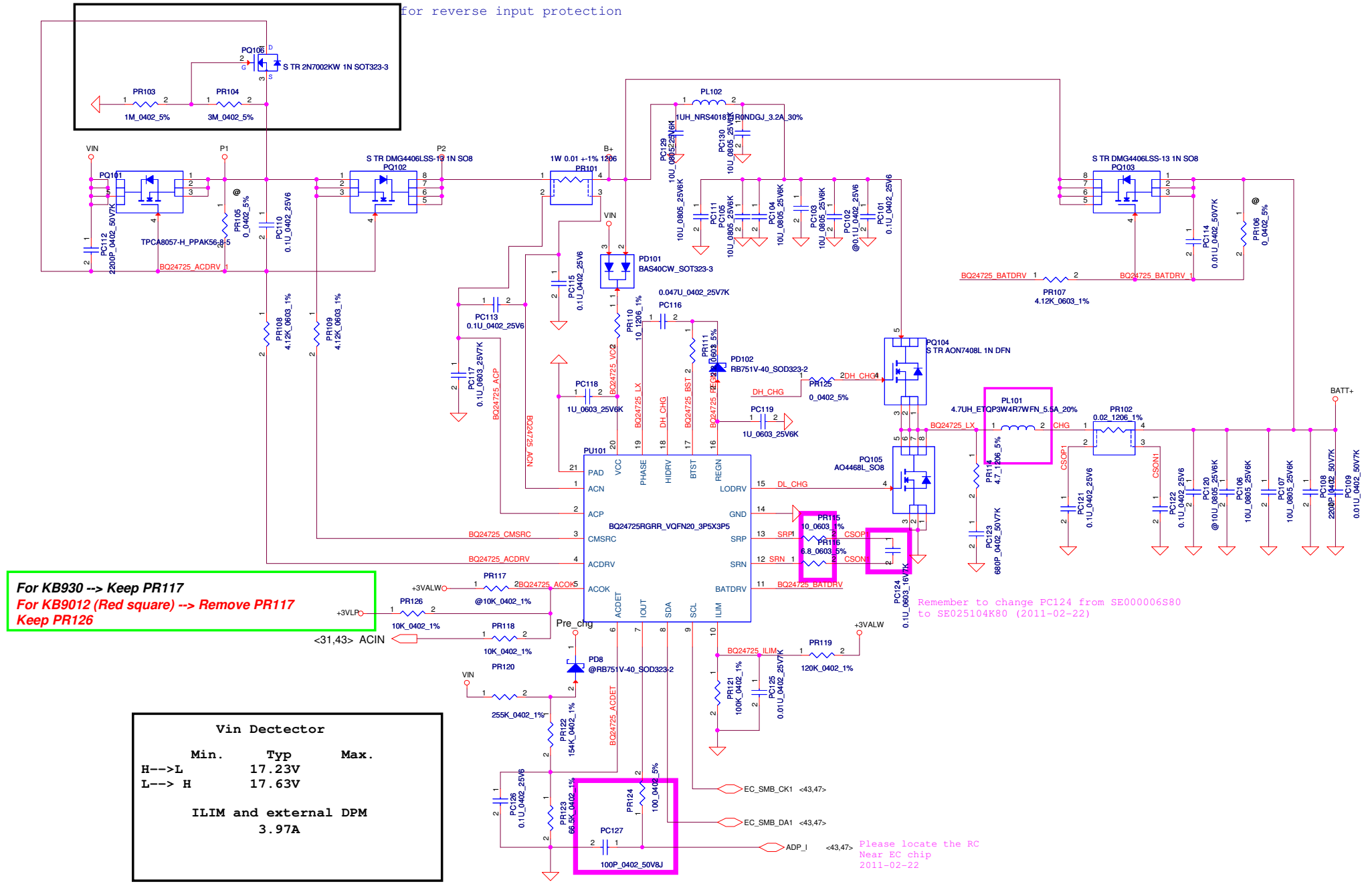

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Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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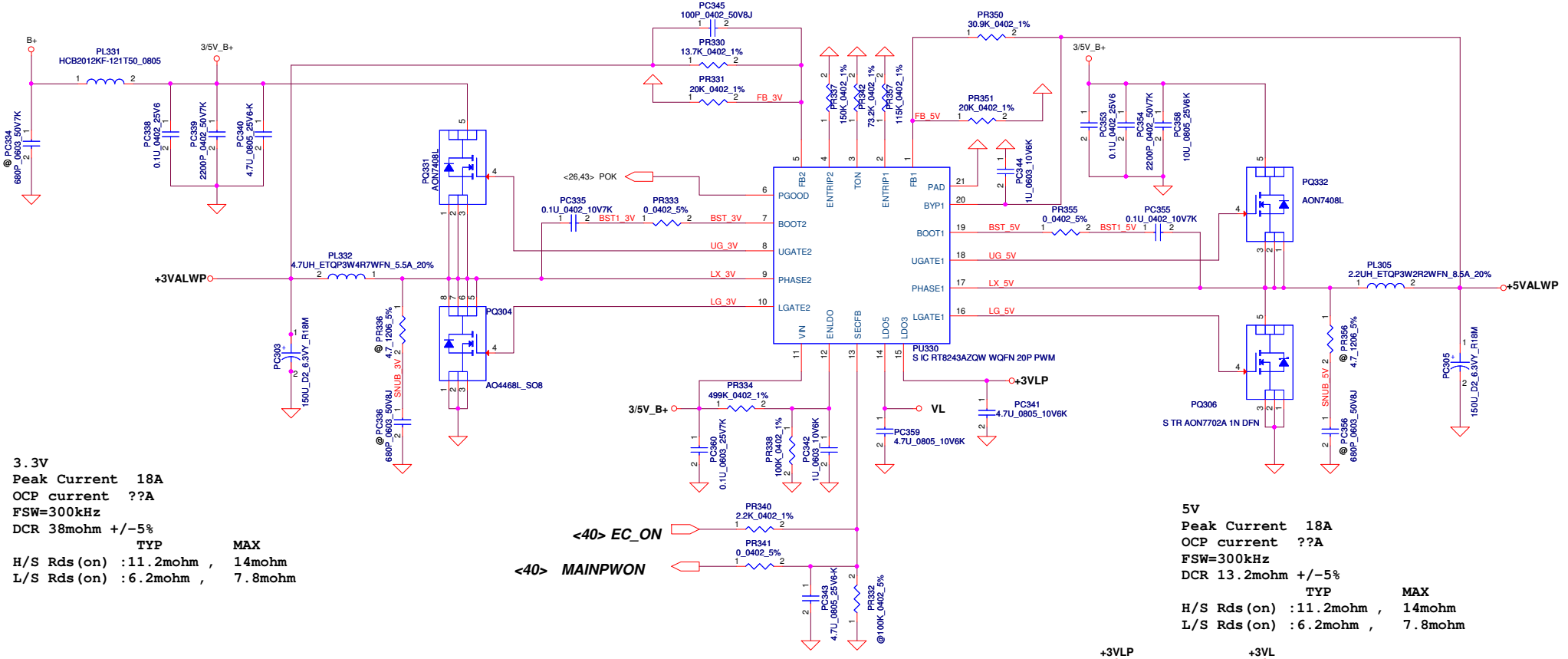
Compal Electronics, Inc.			
Title	PWR-CHARGER		
Size	Document Number		Rev
	LA-8226P		1.0
Date:	Friday, July 13, 2012	Sheet	44 of 56



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Security Classification	Compal Secret Data		
Issued Date	2012/03/13	Deciphered Date	2012/12/31

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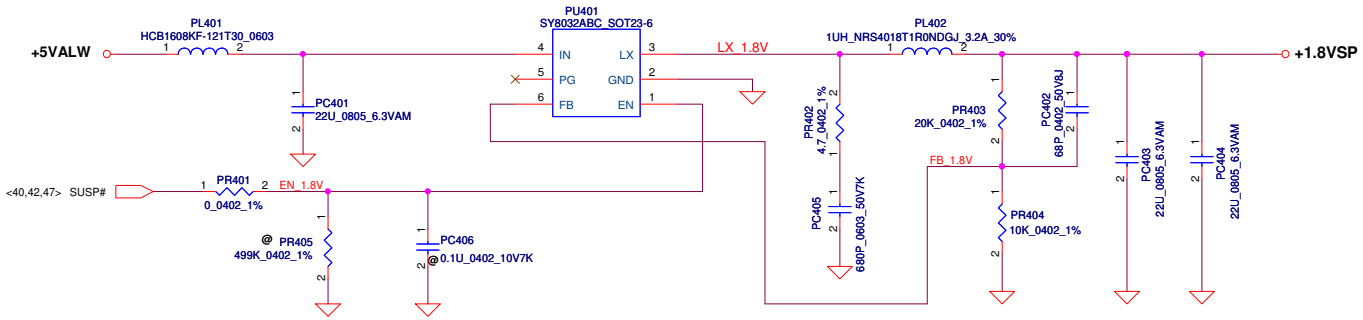
Compal Electronics, Inc.			
Title: PWR-3.3VALWP/5VALWP			
Size: A3 Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 45 of 53		



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Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: **PWR-1.8VSP**

Size	Document Number	Rev
	LA-8226P	1.0

Date: Friday, July 13, 2012 | Sheet 46 of 56

(8.5A,360mils ,Via NO.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

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Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

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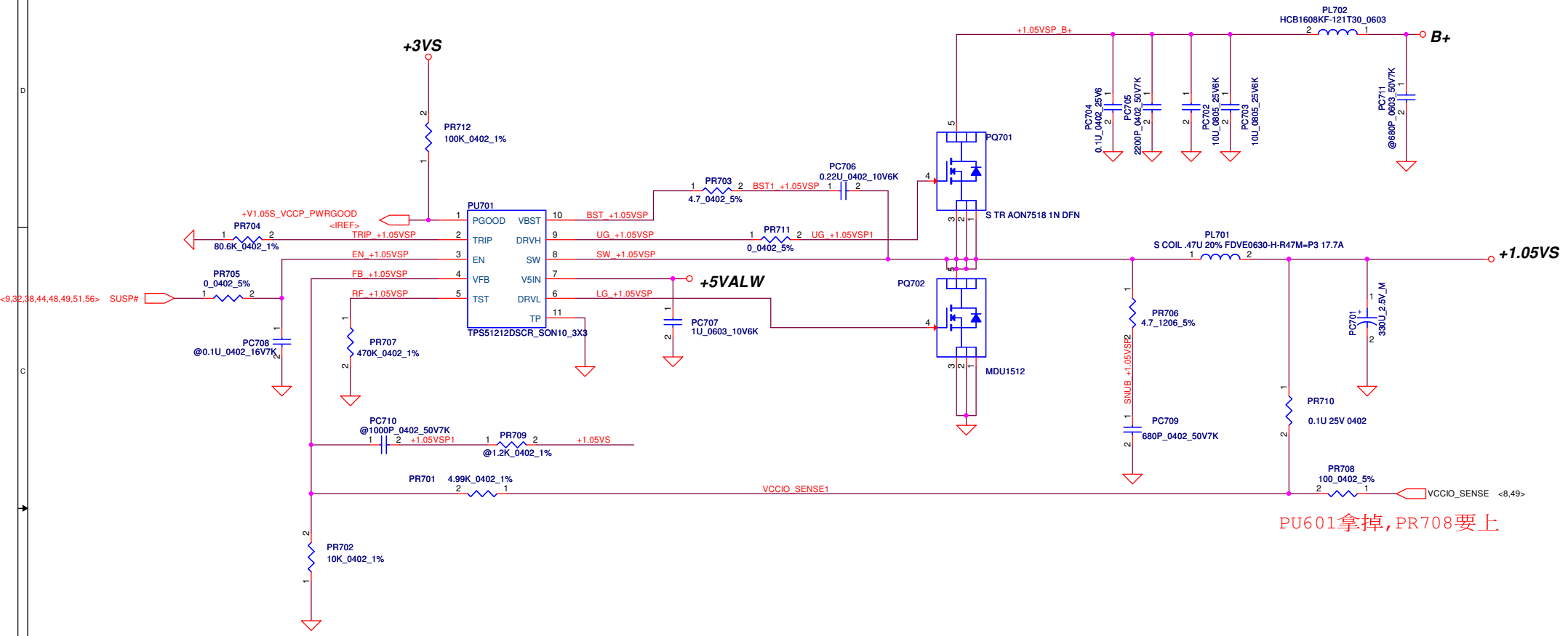
Compal Electronics, Inc.

Title: PWR-V1.05S_VCCP

Size	Document Number	Rev
Custom	LA-8226P	1.0

Date: Friday, July 13, 2012 | Sheet 47 of 56



PU601拿掉,PR708要上

(12A,480mils ,Via NO.= 24)

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Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

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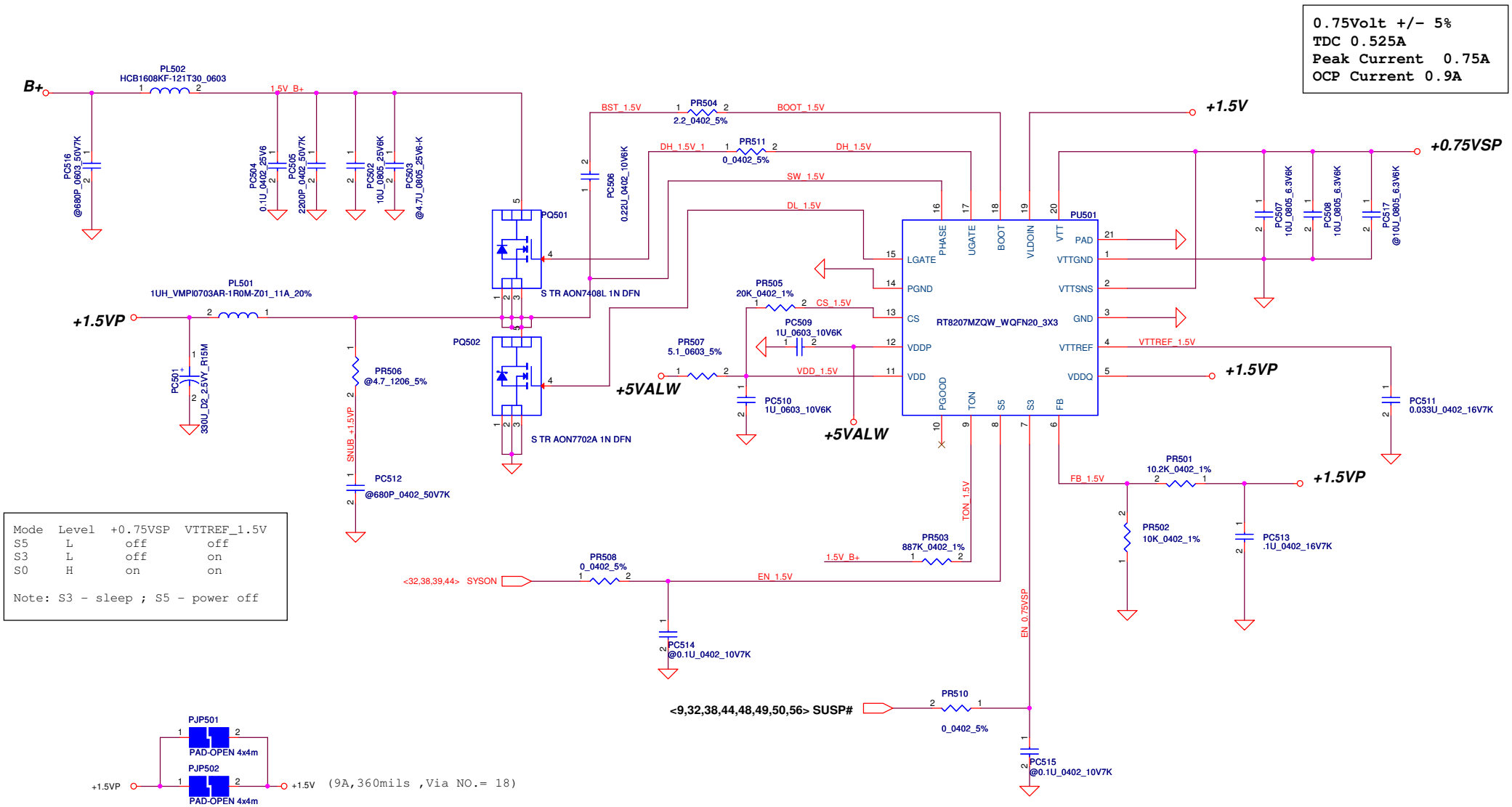
Compal Electronics, Inc.

Title: PWR-V1.05SP

Size: Custom | Document Number: LA-8226P | Rev: 1.0

Date: Friday, July 13, 2012 | Sheet 48 of 56



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Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

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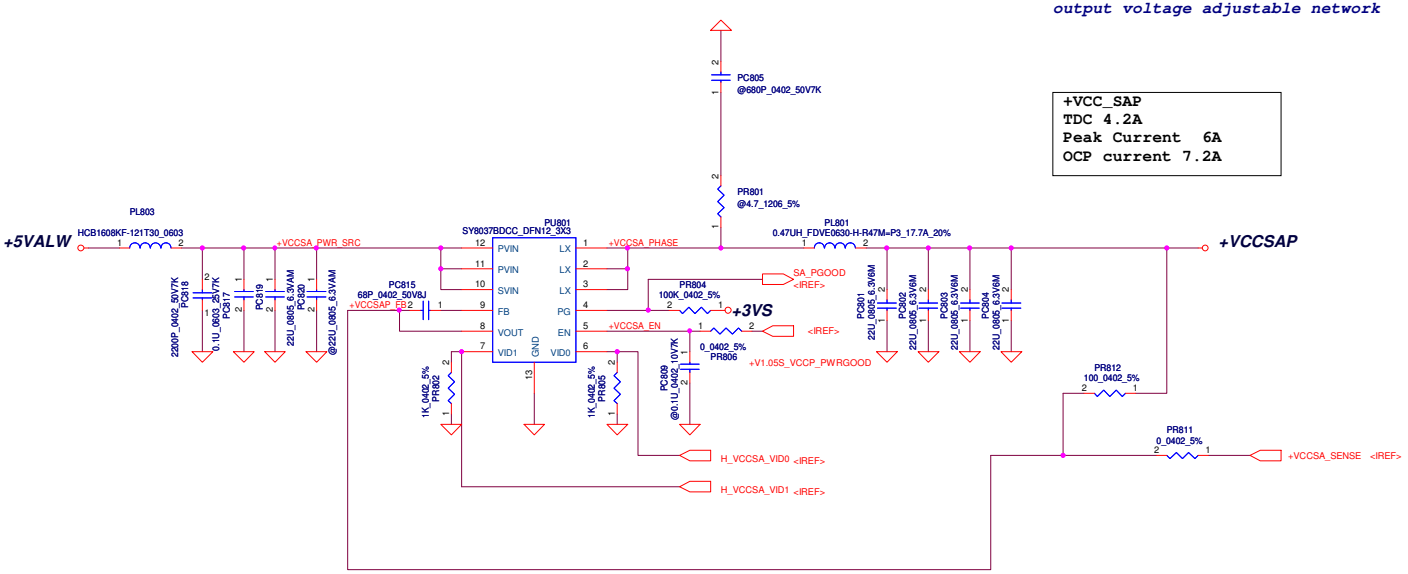
Compal Electronics, Inc.			
Title	PWR-1.5VP / +0.75VSP		
Size Custom	Document Number LA-8226P		Rev 1.0
Date: Friday, July 13, 2012	Sheet 49 of 56		

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



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Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

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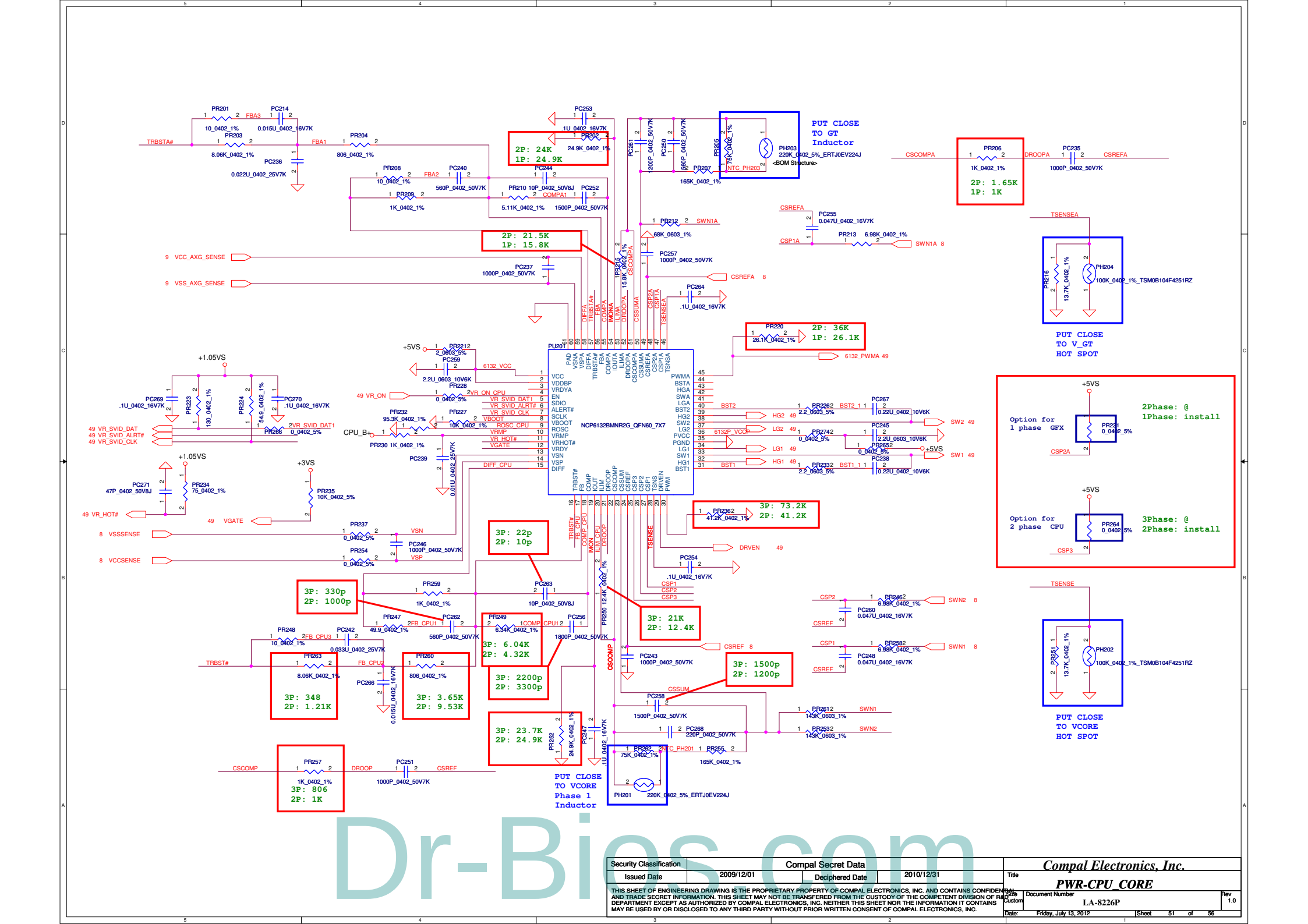
Compal Electronics, Inc.			
Title: PWR-VCC_SAP			
Size: C	Document Number: LA-8226P		Rev: 1.0
Date: Friday, July 13, 2012		Sheet 50 of 56	



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/12/01	Deciphered Date	2010/12/31
Title	PWR-CPU_CORE		
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Friday, July 13, 2012	Sheet 51 of 56		

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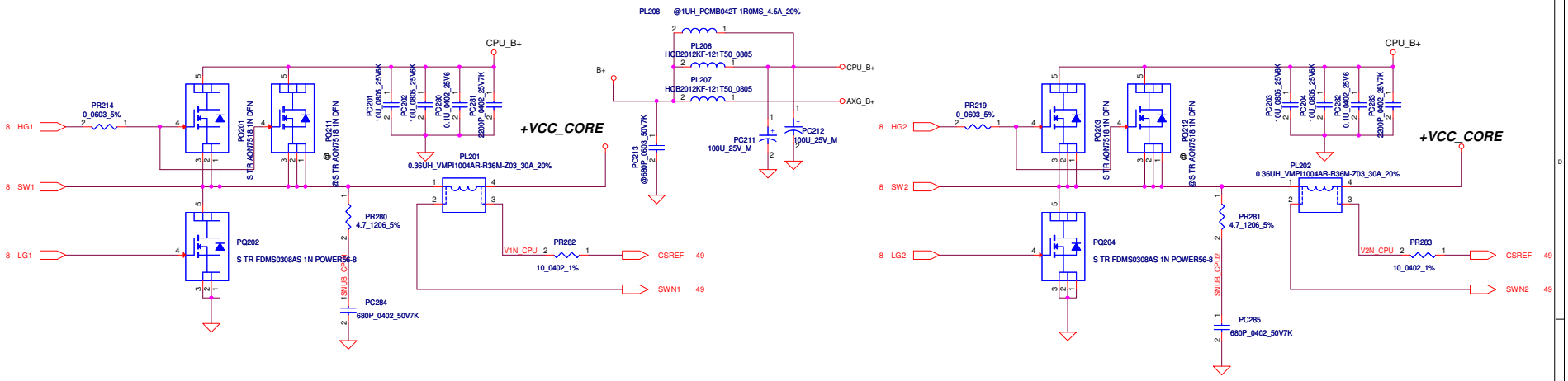
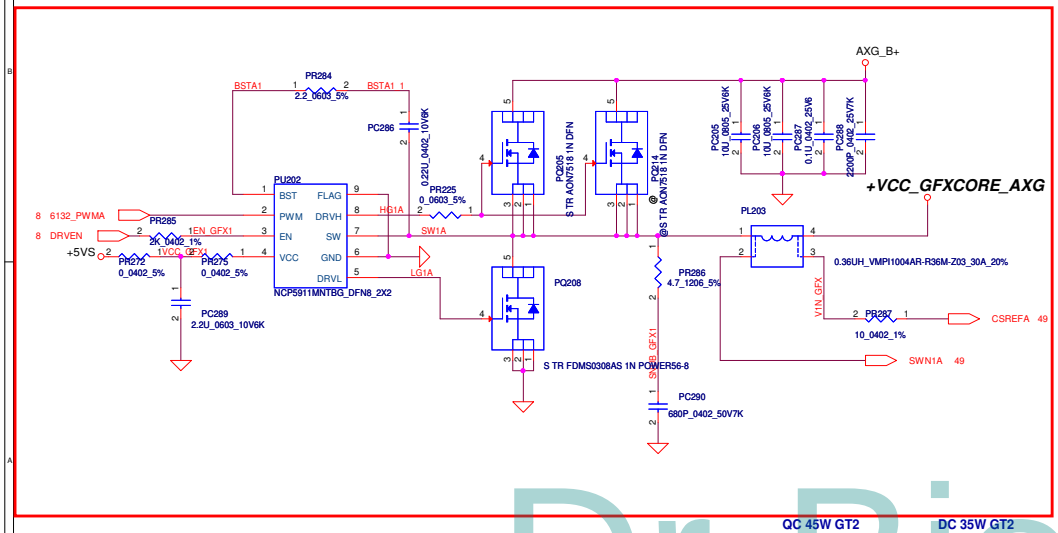


QC 45W CPU
solution: 3+2
MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
Gfx_core --> 上1(CSD17308) 下1(TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
Gfx_core --> 上1(CSD17308) 下1(TPCA8057)

QC 45W CPU	DC 35W CPU
VID1=0.9V	VID1=1.05V
IccMax=94A	IccMax=53A
Icc_Dyn=66A	Icc_Dyn=43A
Icc_TDC=56A	Icc_TDC=33A
R_LL=1.9m ohm	R_LL=1.9m ohm
OCP~110A	OCP~65A



QC 45W GT2	DC 35W GT2
VID1=1.23V	VID1=1.23V
IccMax=46A	IccMax=33A
Icc_Dyn=37A	Icc_Dyn=20.2A
Icc_TDC=38A	Icc_TDC=21.5A
R_LL=3.9m ohm	R_LL=3.9m ohm
OCP~55A	OCP~40A

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Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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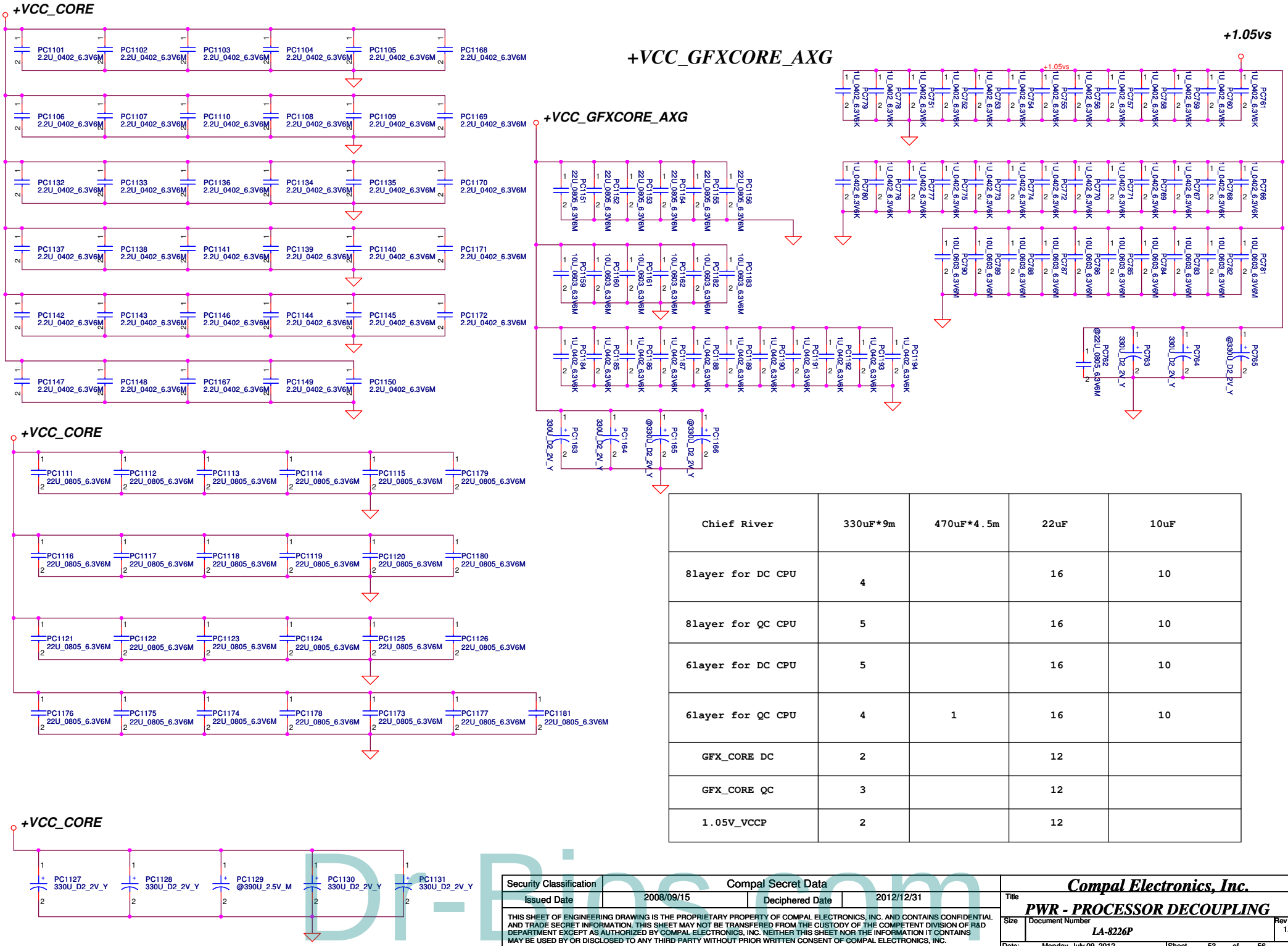
Compal Electronics, Inc.			
Title	PWR-CPU_CORE		
Size C	Document Number LA-8226P		Rev 1.0
Date: Friday, July 13, 2012	Sheet 52 of 56		



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

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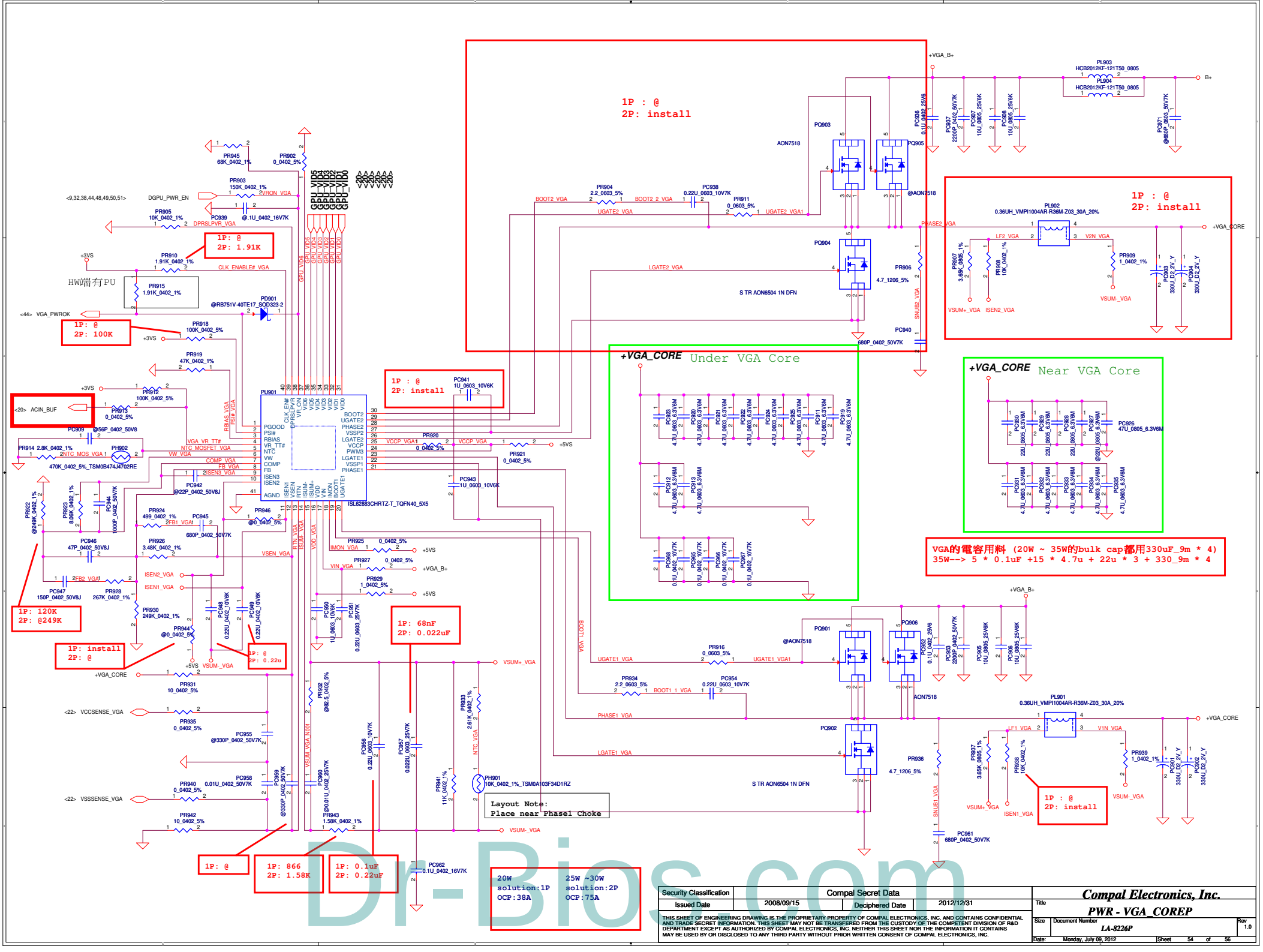
Compal Electronics, Inc.	
Title	PWR - PROCESSOR DECOUPLING
Size	Document Number: LA-8226P
Rev	1.0
Date:	Monday, July 09, 2012
Sheet	53 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

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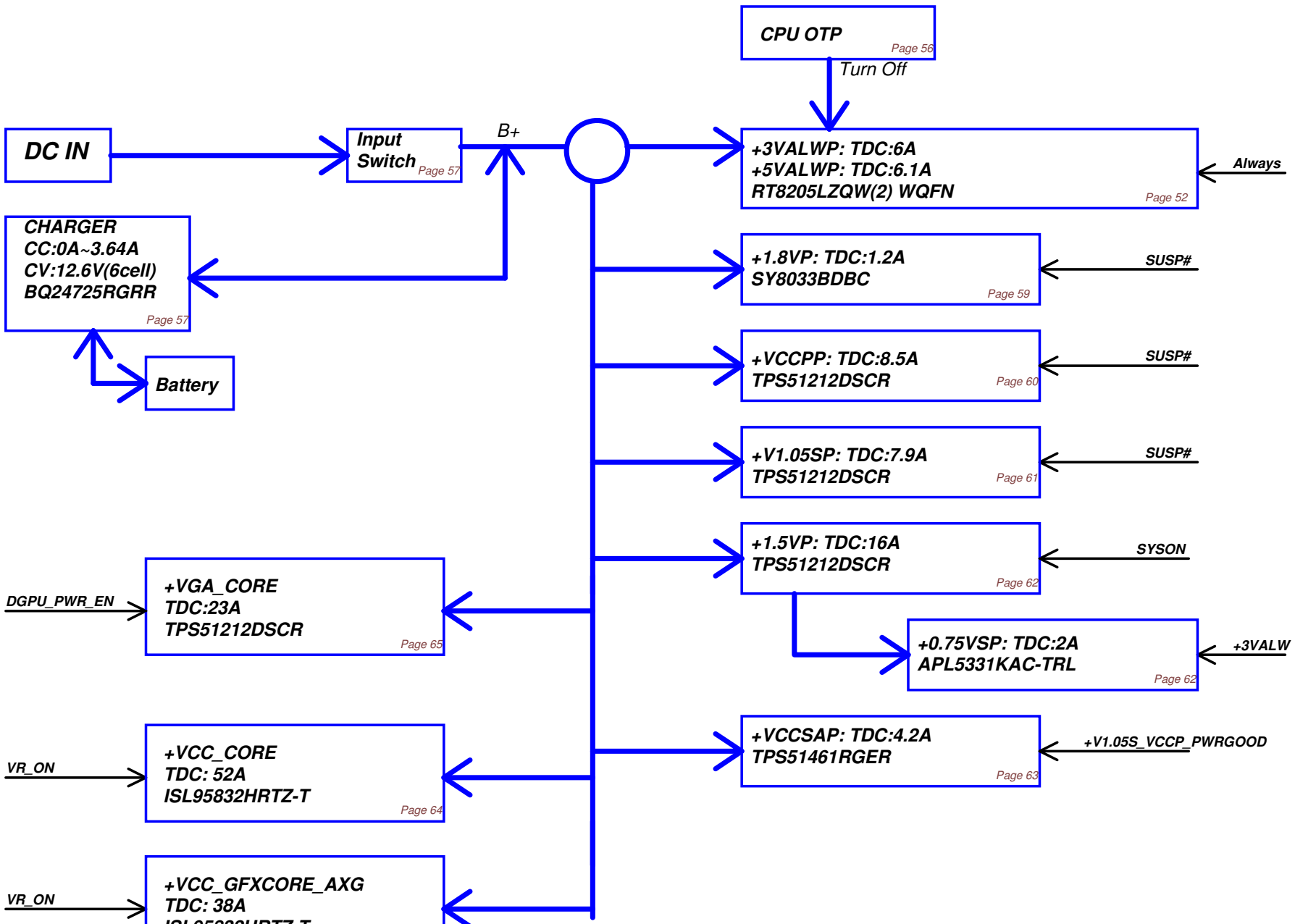
Compal Electronics, Inc.			
Title	PWR - VGA_COREP		
Size	Document Number	LA-8226P	Rev 1.0
Date: Monday, July 09, 2012	Sheet 54 of 56		

Power block



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Security Classification	Compal Secret Data		
Issued Date	2010/08/03	Deciphered Date	2012/12/31

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Compal Electronics, Inc.			
Title: POWER BLOCK DIAGRAM			
Size: Custom	Document Number: LA-8226P		Rev: 1.0
Date: Monday, July 09, 2012	Sheet 55 of 56		

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	51.52	modify CPU soultion to 2+1	20120522	daniel_kao	only support BGA1023 35W		
2	43	Delete 51_ON circuit	20120522	daniel_kao	EC : 9012		
3	46	change 1.8v to SY8032A	20120522	daniel_kao			
4	45	change 3v/5v to RT8243A.	20120522	daniel_kao			
5	43	delete G718 circuit.	20120522	daniel_kao	follow EC 9012		
6	44	change EMI ISN Choke (PL102) to SH00000MW00.	20120522	daniel_kao			
7	53	Follow BGA1023 request, modify output MLCC count.	20120522	daniel_kao			
8	44	change pr101 from 2512 to 1206	20120523	daniel_kao			
9	45	Change pq304 from AON7406L to AON4468L change pq332 form AON7518 to AON7408L change pq306 from AON7212L to FDMC7692S change pl305 to 2.2UH +-20% ETQP3W2R2WFN 8.5A	20120523	daniel_kao			

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/09/15	Deciphered Date	2012/12/31
Title	PWR - PIR		
Size	Document Number		Rev
A3	LA-8226P		1.0
Date:	Monday, July 09, 2012	Sheet	56 of 56

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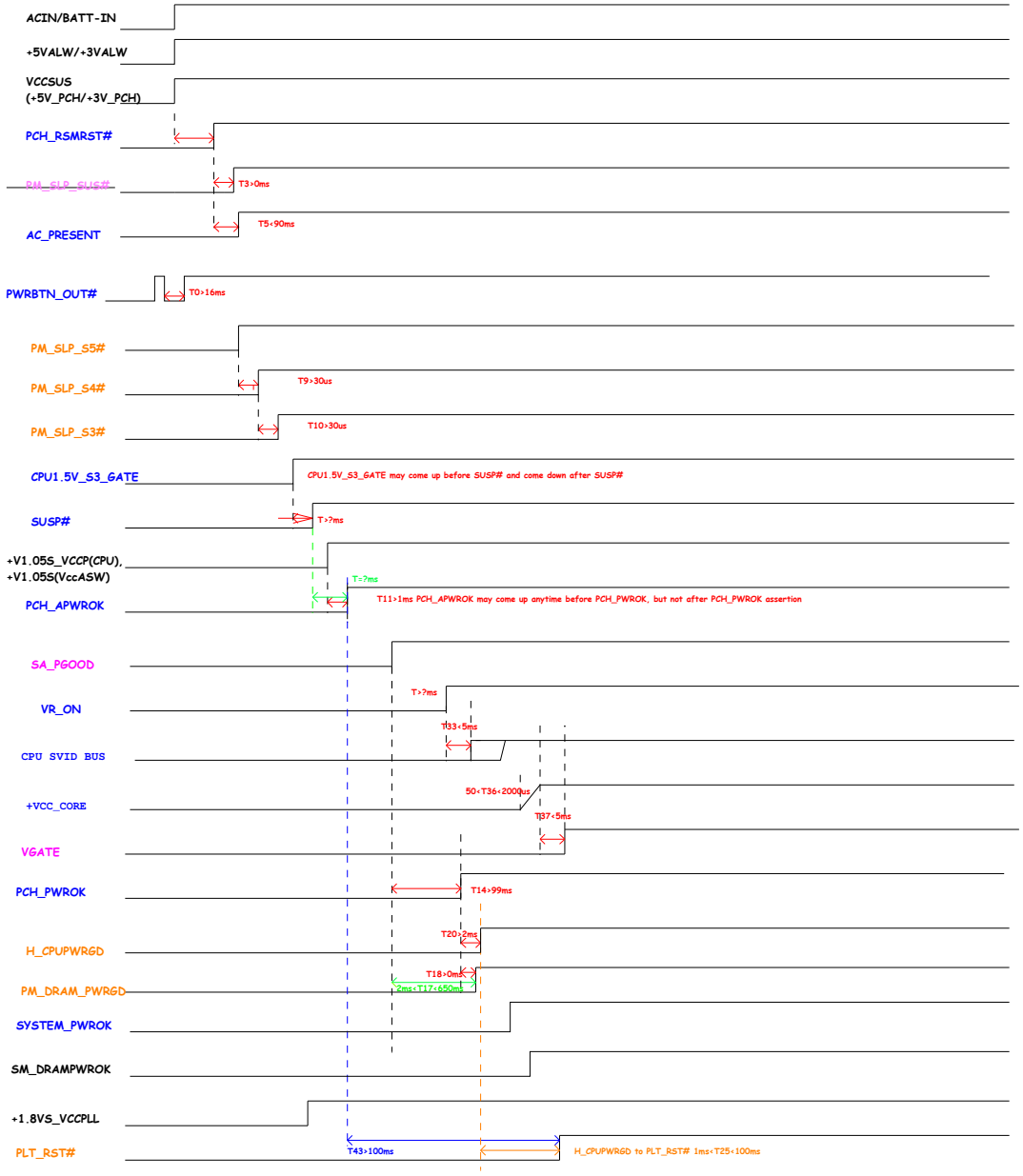
Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

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Security Classification:	Compal Secret Data		
Issued Date: 2009/12/01	Deciphered Date: 2011/12/31	Title: Power Sequence	
Size:	Document Number: LA-8236P		Rev: 1.0
Date: Monday, July 23, 2012	Sheet: 57 of 58		

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FM: LA-8224PR10_0416.DSN

Version Change List (P. I. R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		CPU change from socket to BGA 1023	0.1	4~9	CPU change to UCPU1(BGA1023) from JCPU1(socket).	5/28	
		Modify CPU Cap.	0.1	8,9	Change C74,C75 to 1uf/0402 Del C79,C80,C81,C82,C83,C84. Add C243,C239,C151,C177,C219,C157,C181,C237, C153,C192 to 1uf/0402 Add C238,C241,C240,C236,C156,C244,C242,C143 to 10uf/0603 Del C86,C87,C88,C89,C94. Add C245,C246,C254,C248,C249, to 1uF/0402. Add C253,C250,C252,C251,C247 to 10uf/0603.	5/28	
ER02		For Green CLK	0.1	12 13 32 20 43	Add R683 0 ohm. (PCH_32K) Add R637 0 ohm. (PCH_25M) Add R555 0 ohm. (LAN_25M) Add R96 0 ohm. (VGA_27M) Add C89 2.2uF. Add C86,C87 12pF. Add C81 22uF. Add C79,C83,C84,C82,C80 0.1uF. Add Y5 25M. Add U6 SLG3NB300VTR. Add R31 1M. Add R5 22ohm. Add R95,R35 33ohm. Add R30 330ohm. Add R97 0ohm.	5/28	
ER03		Remove reserve components	0.1	33 39 35 38 5,6,13, 17,18	Del C504,C505,C507. Del C655,C656,R681. Del C626,C628,C634,F1,Q53,Q56,R643,R664. Del D30,Q30,R532,R530. Del R267,R43,R750,R278,R290.	5/29	

ER04		Remove ASM1042 (Del page 36)
		Green CLK VDD change
		EMI solution
			0.1	13,36,37
				43
				13,32,20
					Del ASM1042 .
					U6 VDD change to +3V_PCH from +LAN_IO.
					Add R185,R186,R187.(reserve)
					Add C255,C256,C257.(reserve)
						5/30	

ER05		EMI solution	0.1	42	Add C258,C259,C260.(reserve)	5/31	
ER06		BOM modify	0.1	17 15	C180 change to 22uf (SE000000I10). stuff R234 0 ohm	6/4	
ER07		Green CLK modify EMI solution	0.1	42 38	Del R31,R97. Change U6 pin3 voltage to +1.05VS. Add C261.(reserve)	6/4	
ER08		Modify Cap.	0.1	09	Add C262,C263 to 10uf . un-stuff C97,C85,C78 .	6/6	
PR01		Change JDIMM1. footprint	1.0	10	Change JDIMM1 footprint.(TYCO_2-2013298-1_204P)	7/4	
PR02		Swap Resistor	1.0	07	Swap R48 & R46.	7/5	
PR03		EMI solution / GCLK	1.0	35,42	Add C655,C656,C674 to 2.2pf . C87 change to 15pf. R95 change to 0 ohm.		

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