ZZZ

PCB

Part Number = DA60000M700

Compal Confidential

PBL50 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + DGPU Seymour XT-M2

2011-02-15

REV:0.22

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title	P01-Cover Page	
Size B	Document Number LA7321P PBL50	Rev 0.22
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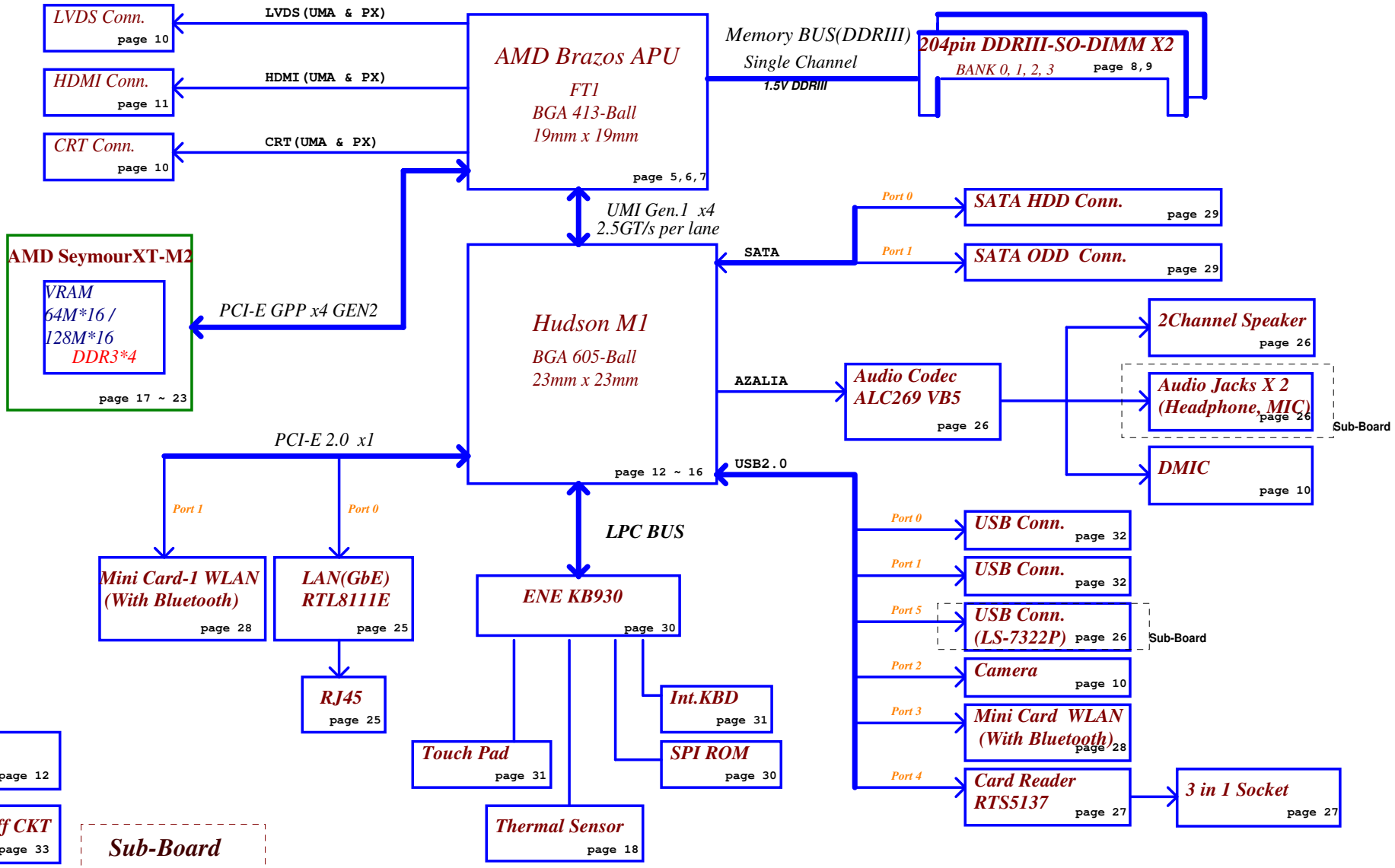
Compal confidential
File Name : LA-7321P



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	P02-Block Diagrams		
Size B	Document Number LA7321P PBL50		Rev 0.22
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE / PU Rail	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930 +3VALW	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V +3VS	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH +3VS	V	X	X	V	V	X
FCH_SIC FCH_SID	FCH +3VALW	X	X	V Reserve	X	X	X

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

Symbol Note :

: means Digital Ground

: means Analog Ground

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI(WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

10G@ : 1.0G CPU (C50)
15G@ : 1.5G CPU (E240)
16G@ : 1.6G CPU (E350)
UMA@ : APU output.
VGA@ : GPU used.
LS@ : Level shift used.
X76@ : VRAM.

X76@L01: Samsung 1G
X76@L02: Hynix 1G
X76@L03: Samsung 512M
X76@L04: Hynix 512M

DIS M/B BOM Config
L01: 16G@/VGA@/LS@ --X76@L04
L02: 16G@/UMA@/LS@
L03: 15G@/VGA@/LS@ --X76@L03
L04: 15G@/UMA@/LS@
L05: 16G@/VGA@/LS@ --X76@L01
L06: 15G@/VGA@/LS@ --X76@L02
L07: 10G@/UMA@/LS@

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Title: P03-Notes List

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Power-Up/Down Sequence

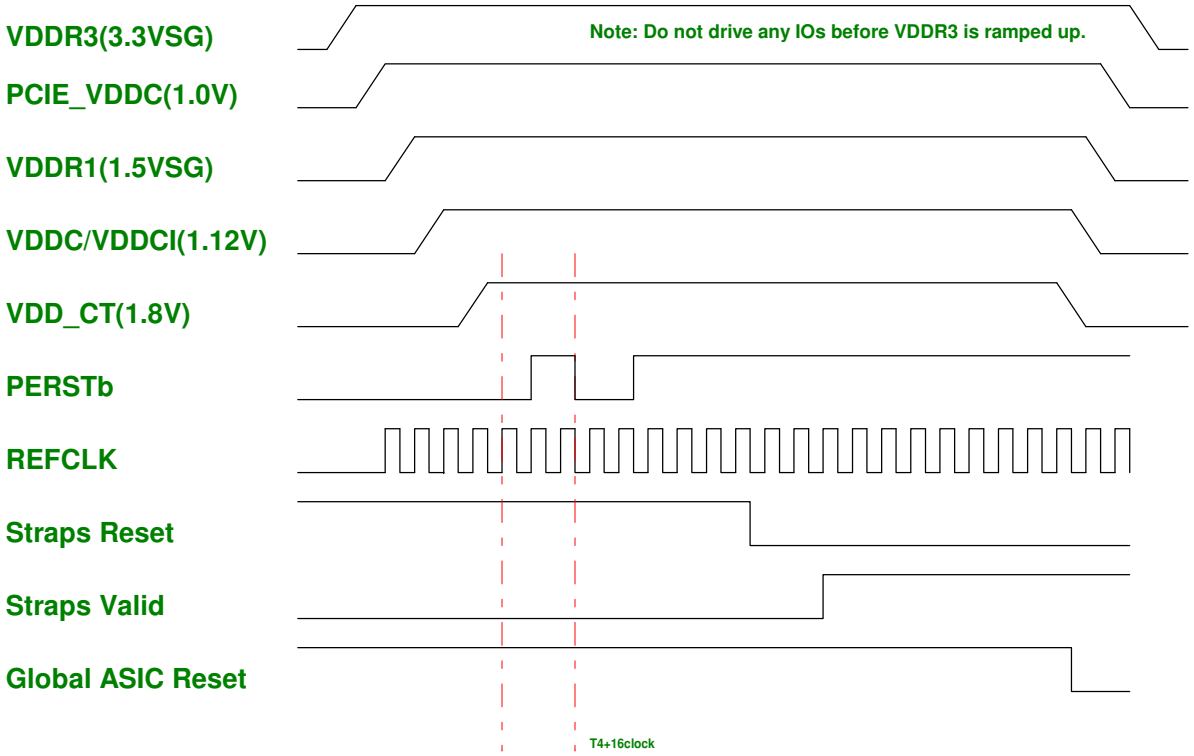
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



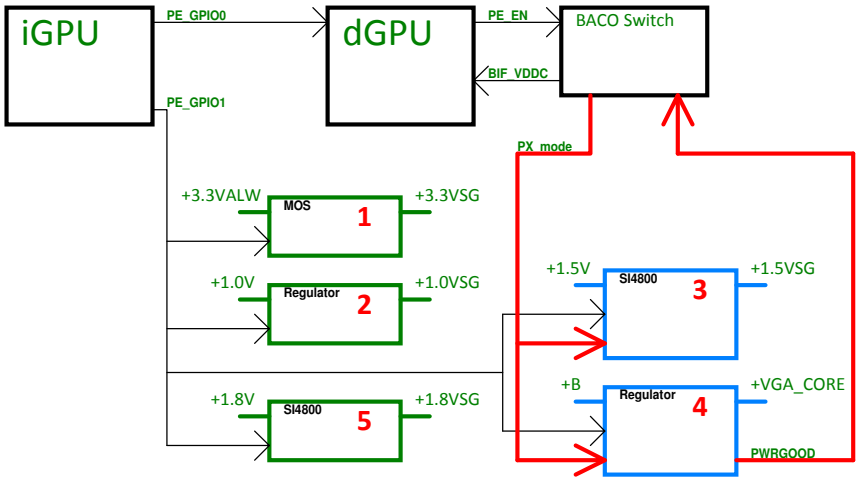
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: P04-dGPU Block Diagram

Size	Document Number	Rev
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APU 10G@: SA00004KD70 (S IC ONTARIO CMC50AFPB22GT 1.0G BGA 413P) - C50
APU 15G@: SA00004KF50 (S IC ZACATE EME240GBB12GT 1.5G BGA 413P) - E240
APU 16G@: SA00004KG70 (S IC ZACATE EME350GBB22GT 1.6G BGA 413P) - E350

U22 16G@
ZACATE EME350GBB22GT 1.6G BGA 413P
U22 10G@
ONTARIO CMC50AFPB22GT 1.0G BGA 413P

+1.8VS
R399 1 2 1K 0402 5% APU_SVC
R400 1 2 1K 0402 5% APU_SVD
R142 2 1 300 0402 5% APU_RST#
R401 2 1 300 0402 5% APU_PWRGD
R402 1 2 510 0402 1% TEST_25_L
R141 1 2 1K 0402 5% TEST36

C237 1 @ 2 0.01U 0402 25V7K APU_RST#
C238 1 @ 2 0.01U 0402 25V7K APU_PWRGD

+3VS
R410 1 2 1K 0402 5% APU_PROCHOT#
R411 1 2 1K 0402 5% APU_ALERT# R
R143 1 2 1K 0402 5% APU_SIC
R414 1 2 1K 0402 5% APU_SID

U22B

DISPLAYPORT 1
11 APU_HDMI_TX2P → A8 TDP1_TXP0
11 APU_HDMI_TX2N → B8 TDP1_TXN0
11 APU_HDMI_TX1P → B9 TDP1_TXP1
11 APU_HDMI_TX1N → A9 TDP1_TXN1
11 APU_HDMI_TX0P → D10 TDP1_TXP2
11 APU_HDMI_TX0N → C10 TDP1_TXN2
11 APU_HDMI_CLKP → A10 TDP1_TXP3
11 APU_HDMI_CLKN → B10 TDP1_TXN3

DISPLAYPORT 0
10 APU_TXOUT2+ → B5 LTDP0_TXP0
10 APU_TXOUT2- → A5 LTDP0_TXN0
10 APU_TXOUT1+ → D6 LTDP0_TXP1
10 APU_TXOUT1- → C6 LTDP0_TXN1
10 APU_TXOUT0+ → A6 LTDP0_TXP2
10 APU_TXOUT0- → B6 LTDP0_TXN2
10 APU_TXCLK+ → D8 LTDP0_TXP3
10 APU_TXCLK- → C8 LTDP0_TXN3

CLK
12 APU_CLKP → V2 CLKIN_H
12 APU_CLKN → V1 CLKIN_L
12 APU_DISP_CLKP → D2 DISP_CLKIN_H
12 APU_DISP_CLKN → D1 DISP_CLKIN_L

SER
43 APU_SVC → J1 SVC
43 APU_SVD → J2 SVD
APU_SIC → P3 SIC
APU_SID → P4 SID

CTRL
12 APU_RST# → T3 RESET_L
12 APU_PWRGD → T4 PWROK
30 EC_THERM# → R169 1 2 0 0402 5%
12 FCH_PROCHOT# → R168 1 @ 2 0 0402 5%
APU_PROCHOT# → U1 PROCHOT_L
APU_THERMTRIP# → U2 THERMTRIP_L
APU_ALERT# R → T2 ALERT_L

JTAG
APU_TDI → N2 TDI
APU_TDO → N1 TDO
APU_TCK → P1 TCK
APU_TMS → P2 TMS
APU_TRST# → M4 TRST_L
APU_DBRDY → M3 DBRDY
APU_DBREQ# → M1 DBREQ_L
T93PAD
T94PAD Close @ APU
T77PAD

VDDCR_NB_SENSE → F4
43 APU_VDDNB_RUN_FB_H
VDDCR_CPU_SENSE → G1
43 APU_VDD0_RUN_FB_H
VDDIO_MEM_S_SENSE → F3
43 APU_VDD0_RUN_FB_L → F1
VSS_SENSE

RSVD_1 → B4
RSVD_2 → W11
RSVD_3 → V5

ZACATE EME240GBB12GT 1.5G BGA 413P
15G@

DP MISC
DP_ZVSS → H3 R398 1 2 150 0402 1%
DP_BLON → G2 APU_ENBKL 10
DP_DIGON → H2 APU_ENVDD 10
DP_VARY_BL → H1 APU_BLPWM 10

TDP1_AUXP → B2 APU_HDMI_CLK 11
TDP1_AUXN → C2 APU_HDMI_DATA 11
TDP1_HPD → C1 APU_HDMI_HPD 11

LTDP0_AUXP → A3 APU_LCD_CLK 10
LTDP0_AUXN → B3 APU_LCD_DATA 10
LTDP0_HPD → D3 R406 1 2 100K 0402 5% +5VS

VGA DAC
DAC_RED → C12
DAC_REDB → D13 R407 1 2 150 0402 1% APU_CRT_R 10
DAC_GREEN → A12
DAC_GREENB → B12 R408 1 2 150 0402 1% APU_CRT_G 10
DAC_BLUE → A13
DAC_BLUEB → B13 R409 1 2 150 0402 1% APU_CRT_B 10
DAC_HSYNC → E1 APU_CRT_HSYNC 10
DAC_VSYNC → E2 APU_CRT_VSYNC 10
DAC_SCL → F2 APU_CRT_DDC_SCL 10
DAC_SDA → D4 APU_CRT_DDC_SDA 10
DAC_ZVSS → D12 R144 1 2 499 0402 1%

TEST
TEST4 → R1 PAD T66
TEST5 → R2 PAD T67
TEST6 → R6 @ PAD T68
TEST14 → T5
TEST15 → E4 TEST15 R415 1 @ 2 1K 0402 5%
TEST16 → K4 @
TEST17 → L1
TEST18 → L2 TEST18 R416 1 2 1K 0402 5%
TEST19 → M2 TEST19 R417 1 2 1K 0402 5%
TEST25_H → K1 TEST25_H R418 1 2 510 0402 1%
TEST25_L → K2 TEST_25_L
TEST28_H → L5
TEST28_L → M5
TEST31 → M2 TEST31 PAD T73
TEST33_H → J18 TEST33_H C516 2 0.1U 0402 16V4Z R420 1 2 51 0402 1%
TEST33_L → J19 TEST33_L C517 2 0.1U 0402 16V4Z R421 1 2 51 0402 1%
TEST34_H → U15 delete Test point for layout limitation
TEST34_L → T15 Z0100917
TEST35 → H4 TEST35 R422 1 @ 2 1K 0402 5%
TEST36 → N5 TEST36 R958 1 2 1K 0402 5% +1.8VS
TEST37 → R5 TEST37 PAD T76

TEST38 → K3
DMAACTIVE_L → T1 ALLOW_STOP# 12
R423 1 2 1K 0402 5% +1.8VS
C639 1 2 0.1U 0402 16V4Z

+3VS
R424 10K 0402 5%
R425 1K 0402 5%
Q79 MMBT3904_NL_SOT23-3
APU_THERMTRIP# → H_THERMTRIP# 13
R427 0 0402 5%

If FCH internal pull-up disabled, level-shifter could be deleted.
Need BIOS to disable internal pull-up!!

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Typ = 1.0V
Max = 1.3V

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

1.607V for Gate

If use level shift, EC_SMB need pull up (pop R747 & R748)

+3VS
C236 1 @ 2 0.1U 0402 10V7K
R428 1 @ 2 31.6K 0402 1%
R160 1 @ 2 30K 0402 1%

APU_SID → Q22 BSH111 1N_SOT23-3 → EC_SMB_DA
R429 1 @ 2 0 0402 5% FCH_SID → FCH_SID 13
R430 1 2 0 0402 5% EC_SMB_DA2 → EC_SMB_DA2 18,30
R431 1 2 0 0402 5%
T0 FCH
TO EC

APU_SIC → Q23 BSH111 1N_SOT23-3 → EC_SMB_CK
R432 1 @ 2 0 0402 5% FCH_SIC → FCH_SIC 13
R433 1 2 0 0402 5% EC_SMB_CK2 → EC_SMB_CK2 18,30
R434 1 2 0 0402 5%
T0 FCH
TO EC

AMD Debug

+1.8VS
R842 1 2 1K 0402 5%
APU_TRST# → R846 1 2 0 0402 5% APU_TRST# R
R847 2 1 10K 0402 5%
R176 2 1 10K 0402 5%
R177 2 1 10K 0402 5%

JHDT1
SAMTE_ASP-136446-07-B
CONN@

APU_TCK → R843 2 1 1K 0402 5%
APU_TMS → R840 2 1 1K 0402 5%
APU_TDI → R798 2 1 1K 0402 5%
APU_TDO
APU_PWRGD
APU_RST#
APU_DBRDY
APU_DBREQ# → R178 1 2 300 0402 5%
J108_PLLTST0 → R799 1 2 0 0402 5% TEST19
J108_PLLTST1 → R863 1 2 0 0402 5% TEST18
+1.8VS

Please be noted about TEST_18 and TEST_19

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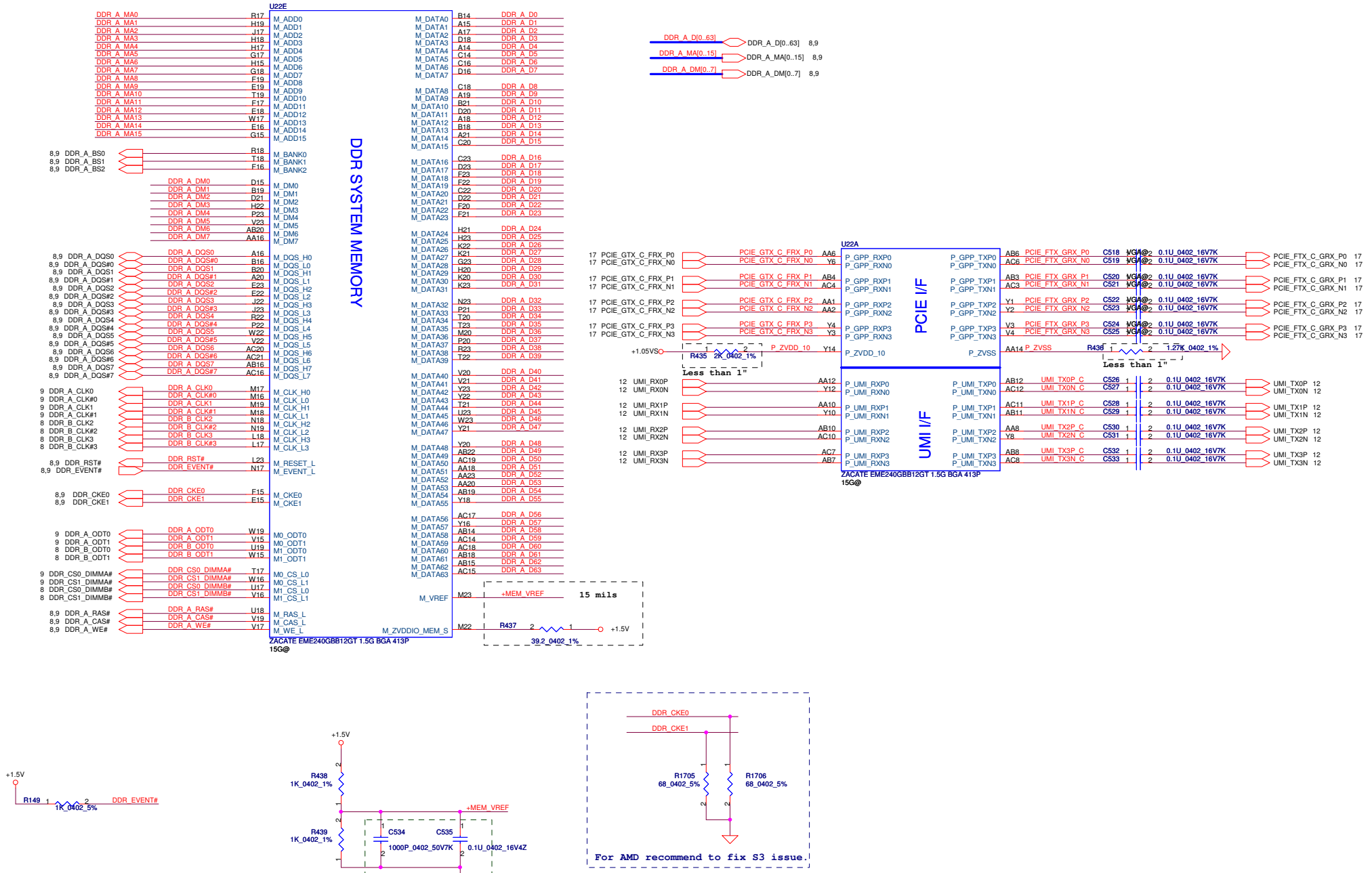
Title: P05-FT1 CTRL/DP/CRT

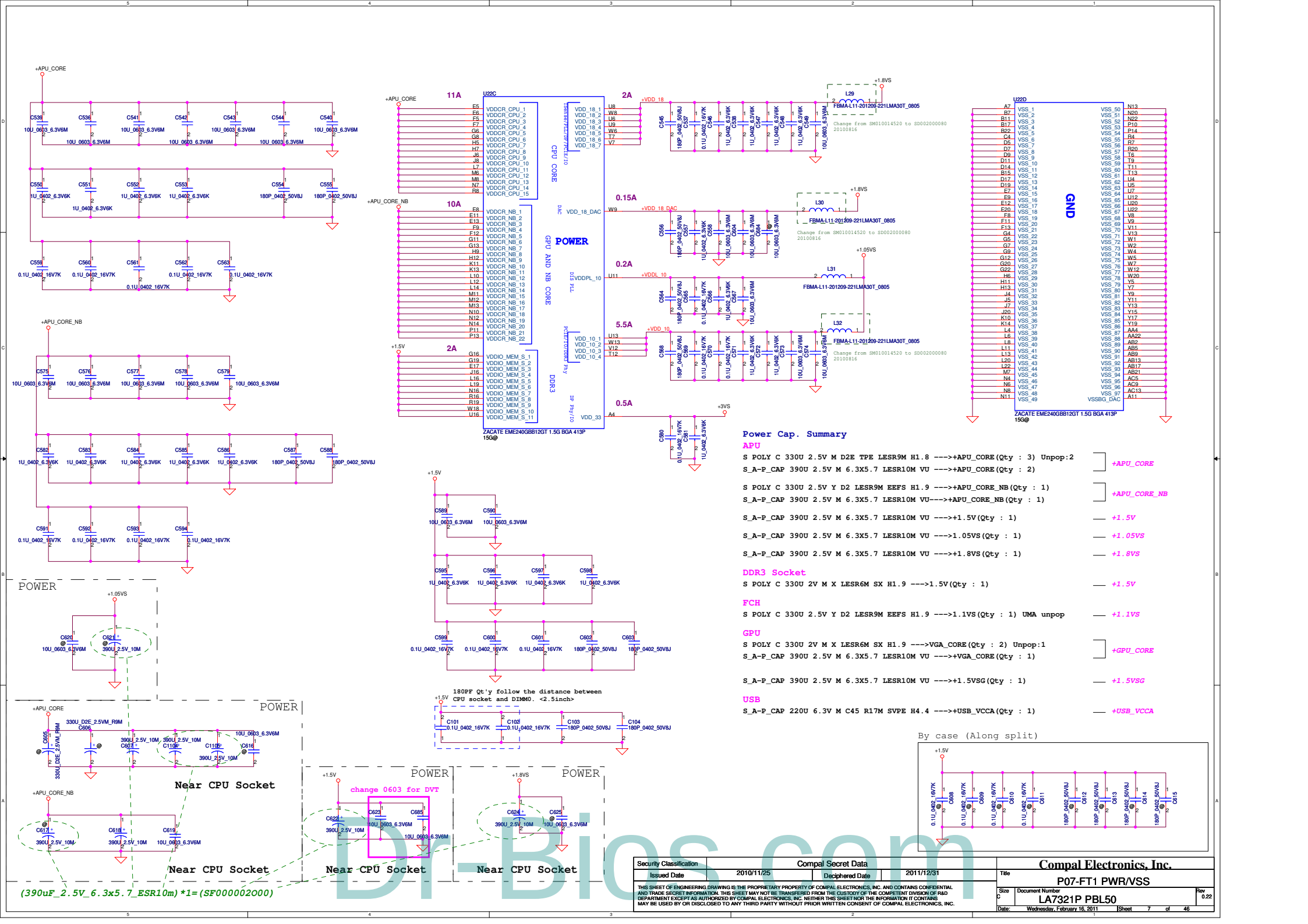
Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

Date: Thursday, February 17, 2011 | Sheet 5 of 46



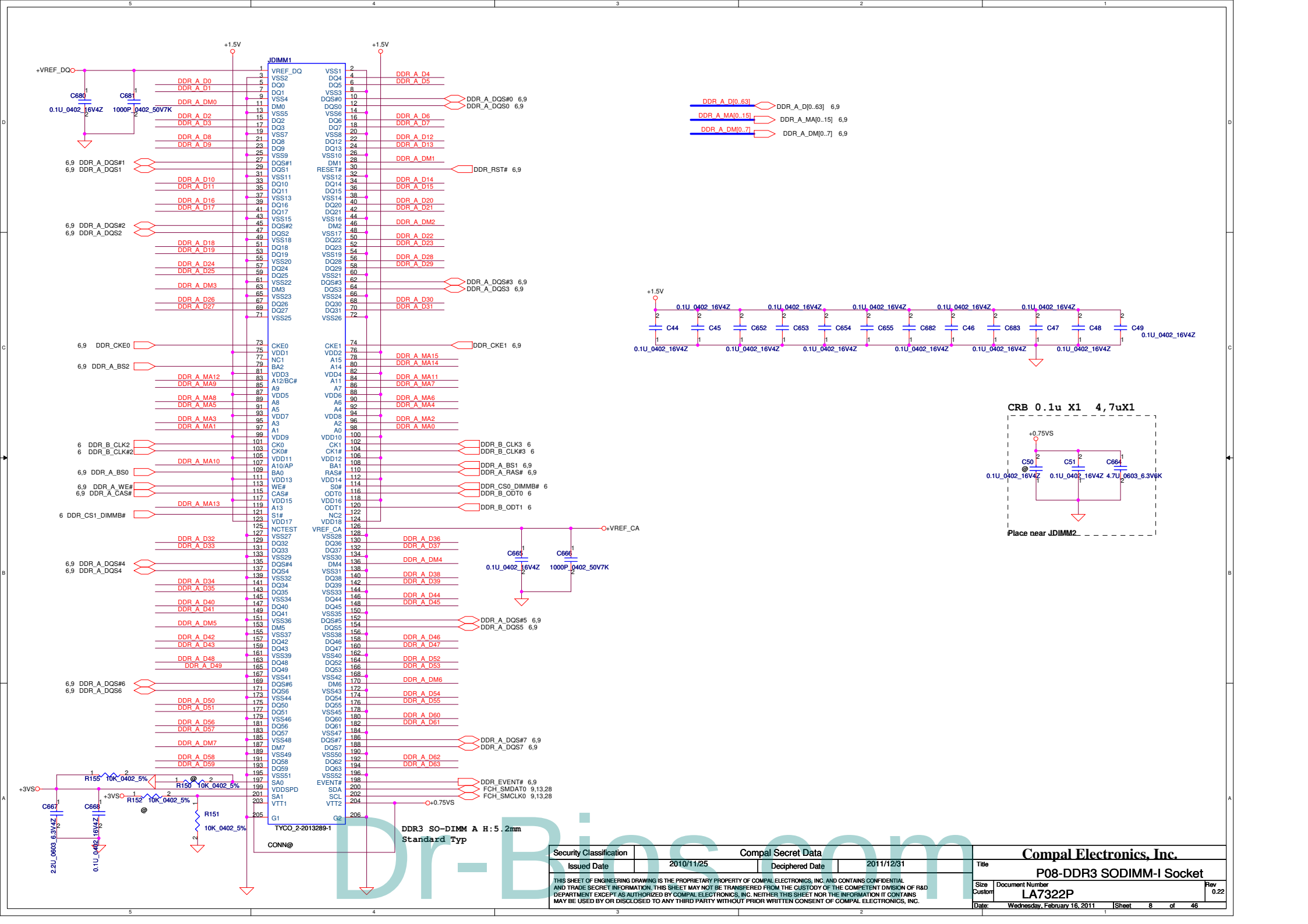
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	P06-FT1 DDRIII/UMI/PCIE		
Size: Custom	Document Number: LA7321P PBL50		Rev: 0.22
Date: Wednesday, February 16, 2011	Sheet 6 of 46		



Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	P07-FT1 PWR/VSS		
Size C	Document Number LA7321P PBL50		Rev 0.22
Date: Wednesday, February 16, 2011	Sheet 7 of 46		



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Issued Date	2010/11/25	Deciphered Date	2011/12/31

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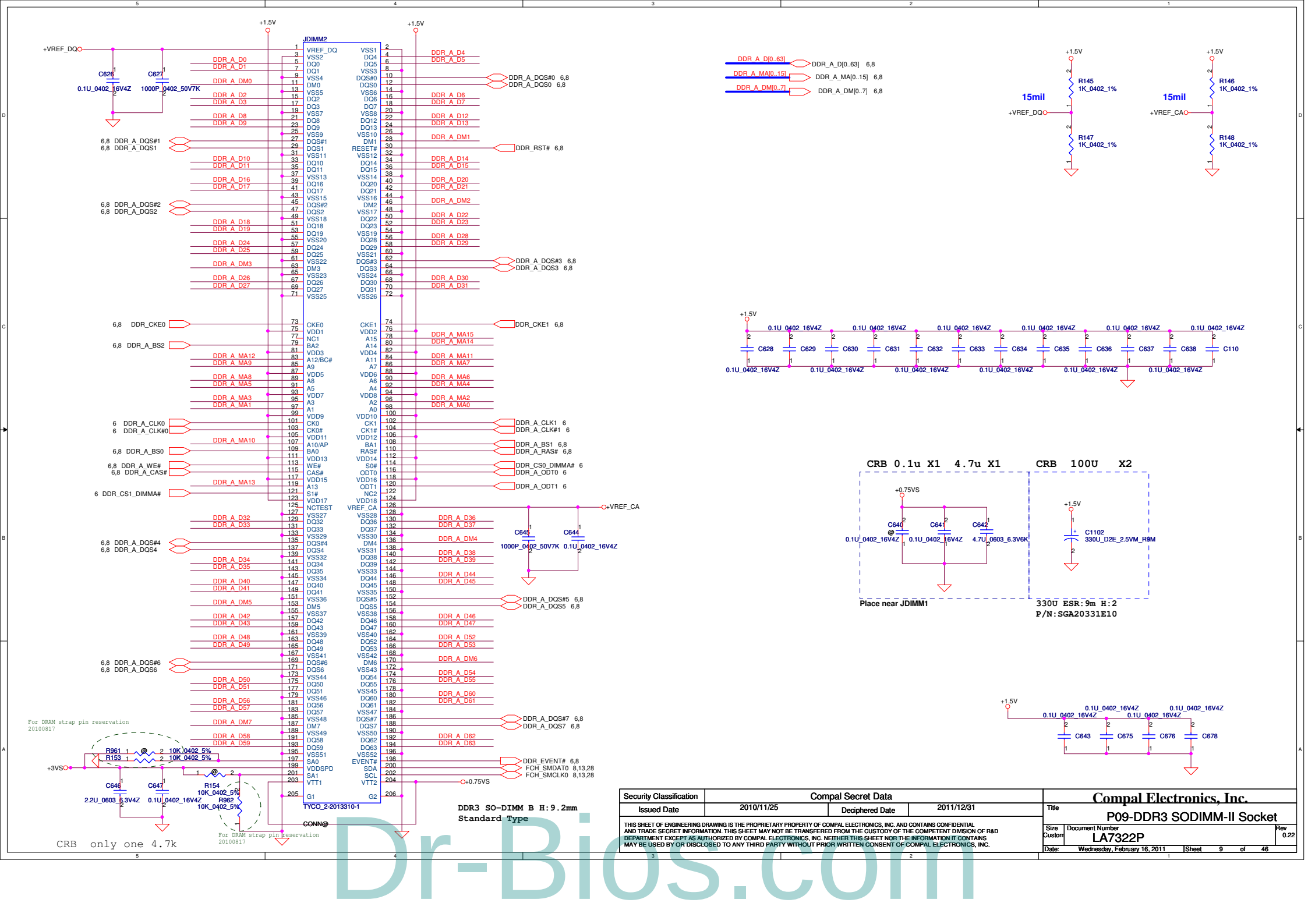
Title: P08-DDR3 SODIMM-I Socket

Size	Document Number	Rev
Custom	LA7322P	0.22

Date: Wednesday, February 16, 2011 | Sheet 8 of 46



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Compal Electronics, Inc.

Title: P09-DDR3 SODIMM-II Socket

Size	Document Number	Rev
Custom	LA7322P	0.22

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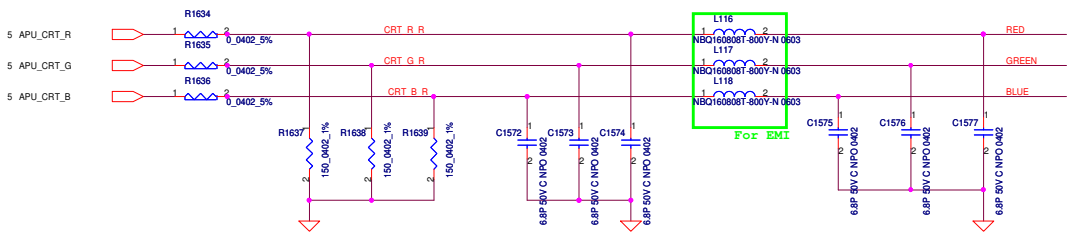
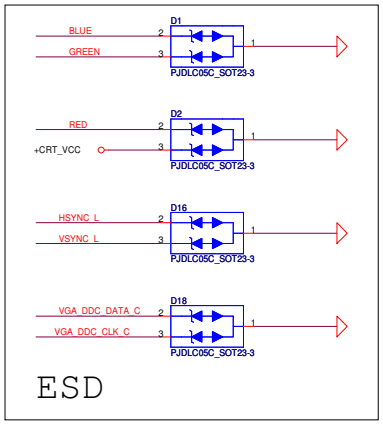
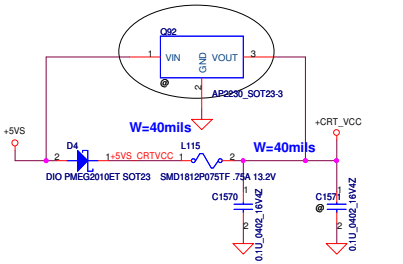
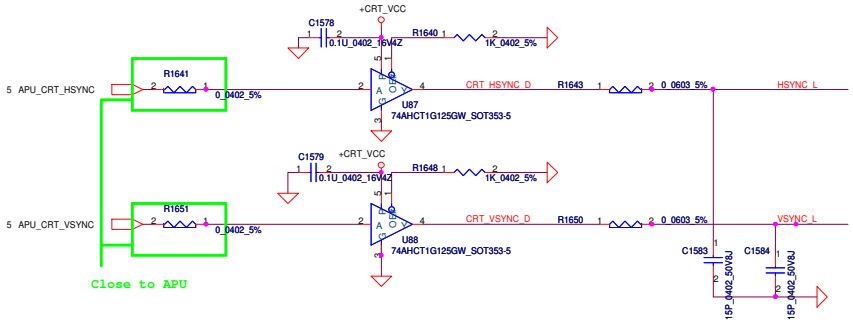
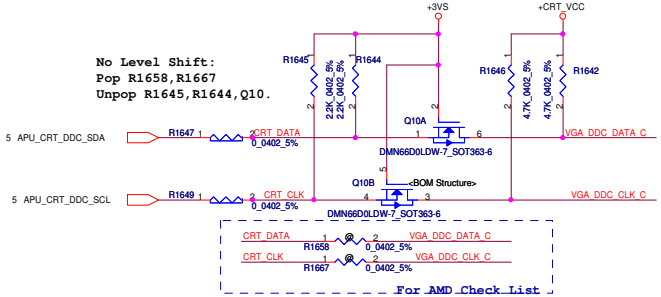
CRT

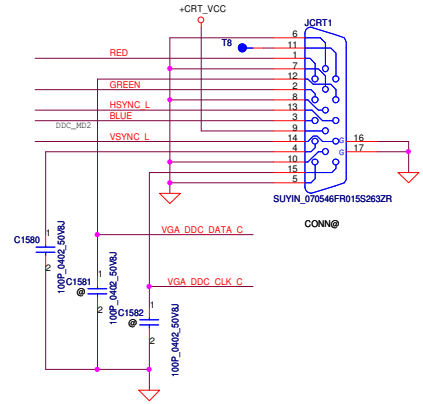




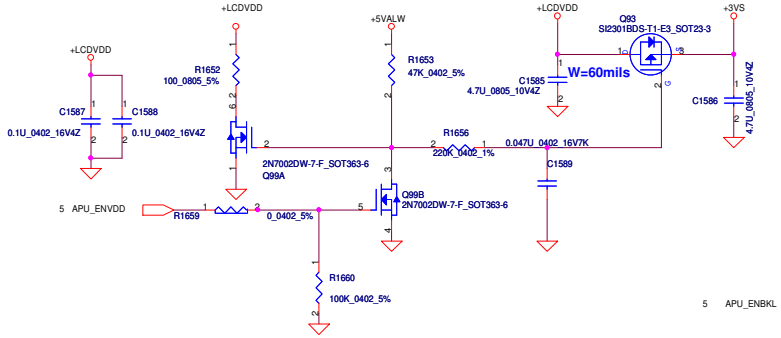


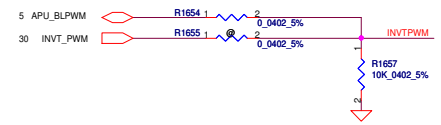


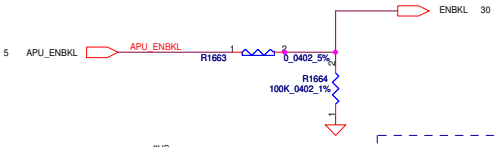


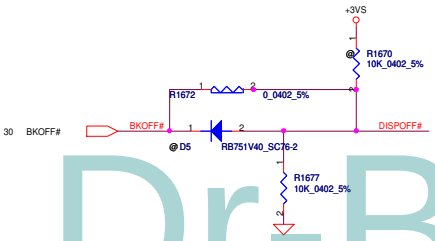


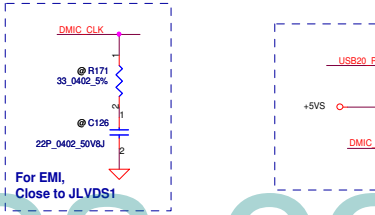
LCD POWER CIRCUIT

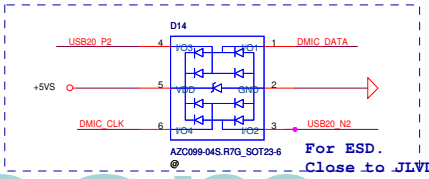


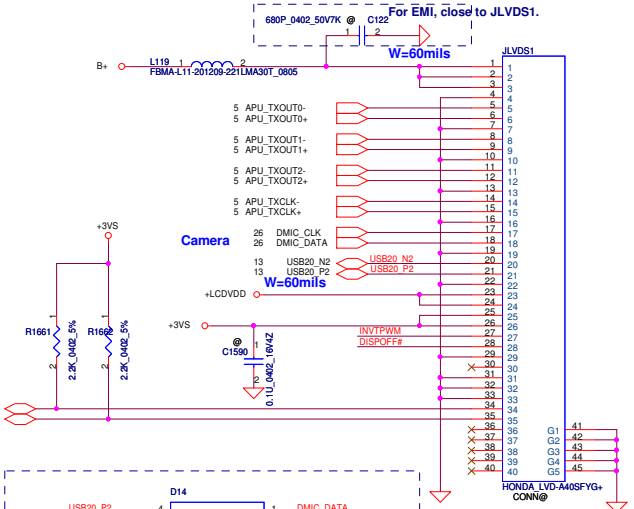












Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	P10-LVDS/CRT CONN		
Size C	Document Number LA7321P PBL50		Rev 0.22
Date: Thursday, February 17, 2011	Sheet 10 of 46		

close to U10VCC (+3VS) pins (one Pin one Capacitor)

Trace AS Short PASS

For ESD request.

Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P11-HDMI CONN

Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

Date: Wednesday, February 16, 2011 | Sheet 11 of 46

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

U31E

PCIE_RST# P1 / A_RST# L1

PCI EXPRESS I/F

LAN / WLAN

30	A_RST#			
6	UMI_RX0P	C53 0.1U_0402_16V7K UMI_RX0P_C	AD26	UMI_TX0P
6	UMI_RX0N	C54 0.1U_0402_16V7K UMI_RX0N_C	AD27	UMI_TX0N
6	UMI_RX1P	C55 0.1U_0402_16V7K UMI_RX1P_C	AC28	UMI_TX1P
6	UMI_RX1N	C56 0.1U_0402_16V7K UMI_RX1N_C	AC29	UMI_TX1N
6	UMI_RX2P	C57 0.1U_0402_16V7K UMI_RX2P_C	AB29	UMI_TX2P
6	UMI_RX2N	C58 0.1U_0402_16V7K UMI_RX2N_C	AB28	UMI_TX2N
6	UMI_RX3P	C59 0.1U_0402_16V7K UMI_RX3P_C	AB26	UMI_TX3P
6	UMI_RX3N	C60 0.1U_0402_16V7K UMI_RX3N_C	AB27	UMI_TX3N
6	UMI_TX0P		AE24	UMI_RX0P
6	UMI_TX0N		AE23	UMI_RX0N
6	UMI_TX1P		AD25	UMI_RX1P
6	UMI_TX1N		AD24	UMI_RX1N
6	UMI_TX2P		AC24	UMI_RX2P
6	UMI_TX2N		AC25	UMI_RX2N
6	UMI_TX3P		AB25	UMI_RX3P
6	UMI_TX3N		AB24	UMI_RX3N
+PCIE_VDDAN		R560 590_0402_1% / R561 2K_0402_1%	AD29	PCIE_CALRP
			AD28	PCIE_CALRN
25	PCIE_FTX_C_DRX_P0	C61 0.1U_0402_16V7K PCIE_FTX_DRX_P0	AA28	GPP_TX0P
25	PCIE_FTX_C_DRX_N0	C62 0.1U_0402_16V7K PCIE_FTX_DRX_N0	AA29	GPP_TX0N
28	PCIE_FTX_C_DRX_P1	C717 0.1U_0402_16V7K PCIE_FTX_DRX_P1	Y29	GPP_TX1P
28	PCIE_FTX_C_DRX_N1	C63 0.1U_0402_16V7K PCIE_FTX_DRX_N1	Y28	GPP_TX1N
			Y26	GPP_TX2P
			Y27	GPP_TX2N
			W28	GPP_TX3P
			W29	GPP_TX3N
25	PCIE_FRX_DTX_P0		AA22	GPP_RX0P
25	PCIE_FRX_DTX_N0		Y21	GPP_RX0N
28	PCIE_FRX_DTX_P1		AA25	GPP_RX1P
28	PCIE_FRX_DTX_N1		AA24	GPP_RX1N
			W23	GPP_RX2P
			V24	GPP_RX2N
			W24	GPP_RX3P
			W25	GPP_RX3N

CLOCK GENERATOR

close to FCH within 1"

LAN / WLAN

			M23	PCIE_RCLKP/NB_LNK_CLKP
			P23	PCIE_RCLKN/NB_LNK_CLKN
5	APU_DISP_CLKP	R564 0_0402_5% APU_DISP_CLKP_R	U29	NB_DISP_CLKP
5	APU_DISP_CLKN	R565 0_0402_5% APU_DISP_CLKN_R	U28	NB_DISP_CLKN
			T26	NB_HT_CLKP
			T27	NB_HT_CLKN
5	APU_CLKP	R162 0_0402_5% APU_CLKP_R	V21	CPU_HT_CLKP
5	APU_CLKN	R163 0_0402_5% APU_CLKN_R	T21	CPU_HT_CLKN
17	CLK_PCIE_VGA	R569 0_0402_5% CLK_PCIE_VGA_R	V23	SLT_GFX_CLKP
17	CLK_PCIE_VGA#	R570 0_0402_5% CLK_PCIE_VGA#_R	T23	SLT_GFX_CLKN
25	CLK_PCIE_LAN	R571 0_0402_5% CLK_PCIE_LAN_R	L29	GPP_CLK0P
25	CLK_PCIE_LAN#	R572 0_0402_5% CLK_PCIE_LAN#_R	L28	GPP_CLK0N
28	CLK_PCIE_MINI1	R573 0_0402_5% CLK_PCIE_MINI1_R	N29	GPP_CLK1P
28	CLK_PCIE_MINI1#	R574 0_0402_5% CLK_PCIE_MINI1#_R	N28	GPP_CLK1N
			M29	GPP_CLK2P
			M28	GPP_CLK2N
			T25	GPP_CLK3P
			V25	GPP_CLK3N
			L24	GPP_CLK4P
			L23	GPP_CLK4N
			P25	GPP_CLK5P
			M25	GPP_CLK5N
			P29	GPP_CLK6P
			P28	GPP_CLK6N
			N26	GPP_CLK7P
			N27	GPP_CLK7N
			T29	GPP_CLK8P
			T28	GPP_CLK8N
			L25	14M_25M_48M_OSC
			L26	25M_X1
			L27	25M_X2

For EMI

27 CLK_SD_48M — R585 0_0402_5% — CLK_SD_48M_R

C66 10P_0402_50V8J / C67 10P_0402_50V8J / Y3 / 1M_0603_5% R576

25MHZ 12PF X5H025000FC1H-H

21807-A11-HUDSON-M1_FCBGA605

Close to FCH

C64 10P_0402_50V8J / C65 10P_0402_50V8J / R563 20M_0603_5% / Y4 OSC NC OSC NC 32.768KHZ_7PF_Q13MC1461000100 / RTC_32KHI / RTC_32KHO

FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)

FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

PCI CLKS

PCICLK0	W2	PAD T96
PCICLK1/GPO36	W1	PCI_CLK1 16
PCICLK2/GPO37	W3	PCI_CLK2 16
PCICLK3/GPO38	W4	PCI_CLK3 16
PCICLK4/14M_OSC/GPO39	Y1	PCI_CLK4 16
PCIRST_L	V2	PAD T92

PCI I/F

AD0/GPIO0	AA1	
AD1/GPIO1	AA4	
AD2/GPIO2	AA3	
AD3/GPIO3	AB1	
AD4/GPIO4	AA5	
AD5/GPIO5	AB2	
AD6/GPIO6	AB6	
AD7/GPIO7	AB5	
AD8/GPIO8	AA6	
AD9/GPIO9	AC2	
AD10/GPIO10	AC3	
AD11/GPIO11	AC4	
AD12/GPIO12	AC1	
AD13/GPIO13	AD1	
AD14/GPIO14	AD2	
AD15/GPIO15	AE2	
AD16/GPIO16	AE1	
AD17/GPIO17	AF8	
AD18/GPIO18	AE3	
AD19/GPIO19	AF1	
AD20/GPIO20	AG1	
AD21/GPIO21	AF2	R595 0_0402_5% — PE_GPIO0 17
AD22/GPIO22	AE9	
AD23/GPIO23	AD9	PCI_AD23 16
AD24/GPIO24	AC11	PCI_AD24 16
AD25/GPIO25	AF6	PCI_AD25 16
AD26/GPIO26	AF4	PCI_AD26 16
AD27/GPIO27	AF3	VGA_PWRGD_R — PCI_AD27 16
AD28/GPIO28	AH2	
AD29/GPIO29	AG2	
AD30/GPIO30	AH3	
AD31/GPIO31	AA8	
CBE0_L	AD5	
CBE1_L	AD8	
CBE2_L	AA10	
CBE3_L	AE8	
FRAME_L	AB9	
DEVSEL_L	AJ3	
IRDY_L	AE7	
TRDY_L	AC5	
PAR	AF5	
STOP_L	AE6	
PERR_L	AE4	
SERR_L	AE11	
REQ0_L	AH5	
REQ1_L/GPIO40	AH4	
REQ2_L/CLK_REQ8_L/GPIO41	AC12	
REQ3_L/CLK_REQ5_L/GPIO42	AD12	
GNT0_L	AJ5	R627 0_0402_5% PE_GPIO0
GNT1_L/GPO44	AH6	R554 10K_0402_5% — PE_GPIO1 23,30
GNT2_L/GPO45	AB12	
GNT3_L/CLK_REQ7_L/GPIO46	AB11	R99 10K_0402_5%
CLKRUN_L	AD7	
LOCK_L		
	AJ6	
INTE_L/GPIO32	AG6	
INTF_L/GPIO33	AG4	
INTG_L/GPIO34	AJ4	
INTH_L/GPIO35		

LPC

LPCCLK0	H24	R854 0_0402_5% — LPC_CLK1 16
LPCCLK1	H25	R853 0_0402_5% — LPC_CLK0 16
LAD0	J27	R575 22_0402_5% — LPC_CLK0_EC 30
LAD1	J26	R577 22_0402_5% — CLK_PCI_DB 28
LAD2	H29	LPC_AD0 28,30
LAD3	H28	LPC_AD1 28,30
LFRAME_L	G28	LPC_AD2 28,30
LDRQ0_L	J25	LPC_AD3 28,30
LDRQ1_L/CLK_REQ6_L/GPIO49	AA18	LPC_FRAME# 28,30
SERIRQ/GPIO48	AB19	SERIRQ 30

CPU

ALLOW_LDTSTP/DMA_ACTIVE_L	G21	ALLOW_STOP# 5
PROCHOT_L	H21	FCH_PROCHOT# 5
LDT_PG	K19	APU_PWRGD 5
LDT_STP_L	G22	
LDT_RST_L	J24	APU_RST# 5

RTC

32K_X1	C1	RTC_32KHI
32K_X2	C2	RTC_32KHO
RTCCLK	D2	RTC_CLK_R — For EMI. R855 0_0402_5% — RTC_CLK 16,30
INTRUDER_ALERT_L	B2	
VDDBT_RTC_G	B1	R864 510_0402_5% W=20mils

C1272 0.1U_0402_16V4Z / C1271 1U_0402_6.3V4Z / C1270 0.1U_0402_16V4Z

for Clear CMOS Location near to DRAM Boer.

CLRP1 SHORT PADS

+3VALW — C1234 0.1U_0402_16V4Z

A_RST# — R175 33_0402_5% — U28 NC7SZ08P5X_NL_SC70-5 — PLT_RST# 17,25,28

C1233 150P_0402_50V8J / R174 8.2K_0402_5% / R582 0_0402_5% — PCIE_RST#

Need to check material?

+1.8VS / +3VS — R164 10K_0402_5% — APU_PWRGD — Q90 FDV301N_NL_SOT23-3 — H_PWRGD_L 43

+3VALW — C1199 0.1U_0402_16V4Z — @U33 NC7SZ08P5X_NL_SC70-5

23,41,42,44 VGA_PWRGD — VGA_PWRGD — R830 0_0402_5% — VGA_PWRGD_R

R838 100K_0402_5% / R839 0_0402_5%

RTC BATT Conn. — +RTCBATT — JRTC1 SUYIN_060003FA002G201NL

+RTCBATT — R179 1K_0402_5%

+RTCVCC — D23 DAN202UT106_SC70-3 — +CHGRTC

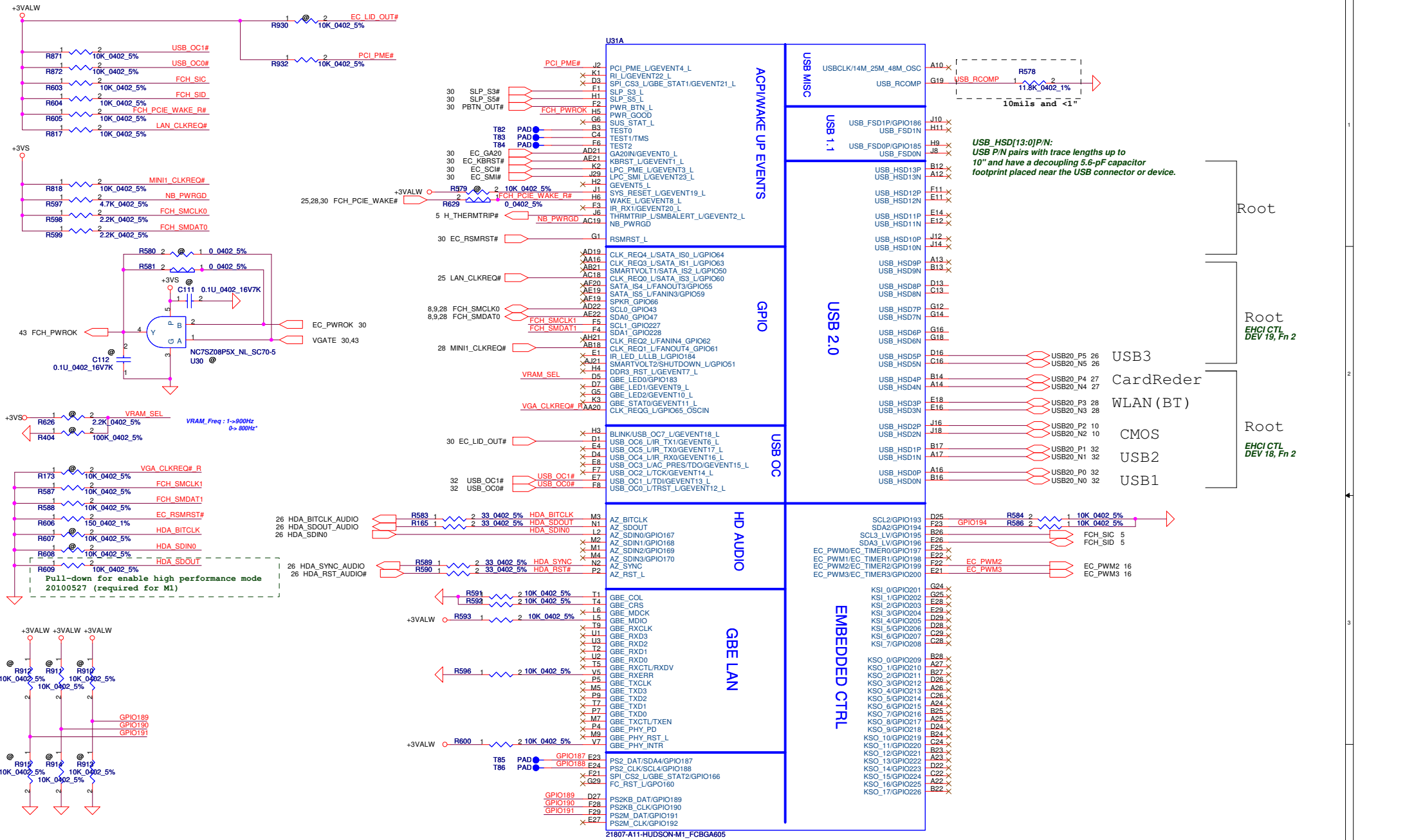
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P12-FCH PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

Date: Tuesday, February 22, 2011 — Sheet 12 of 46



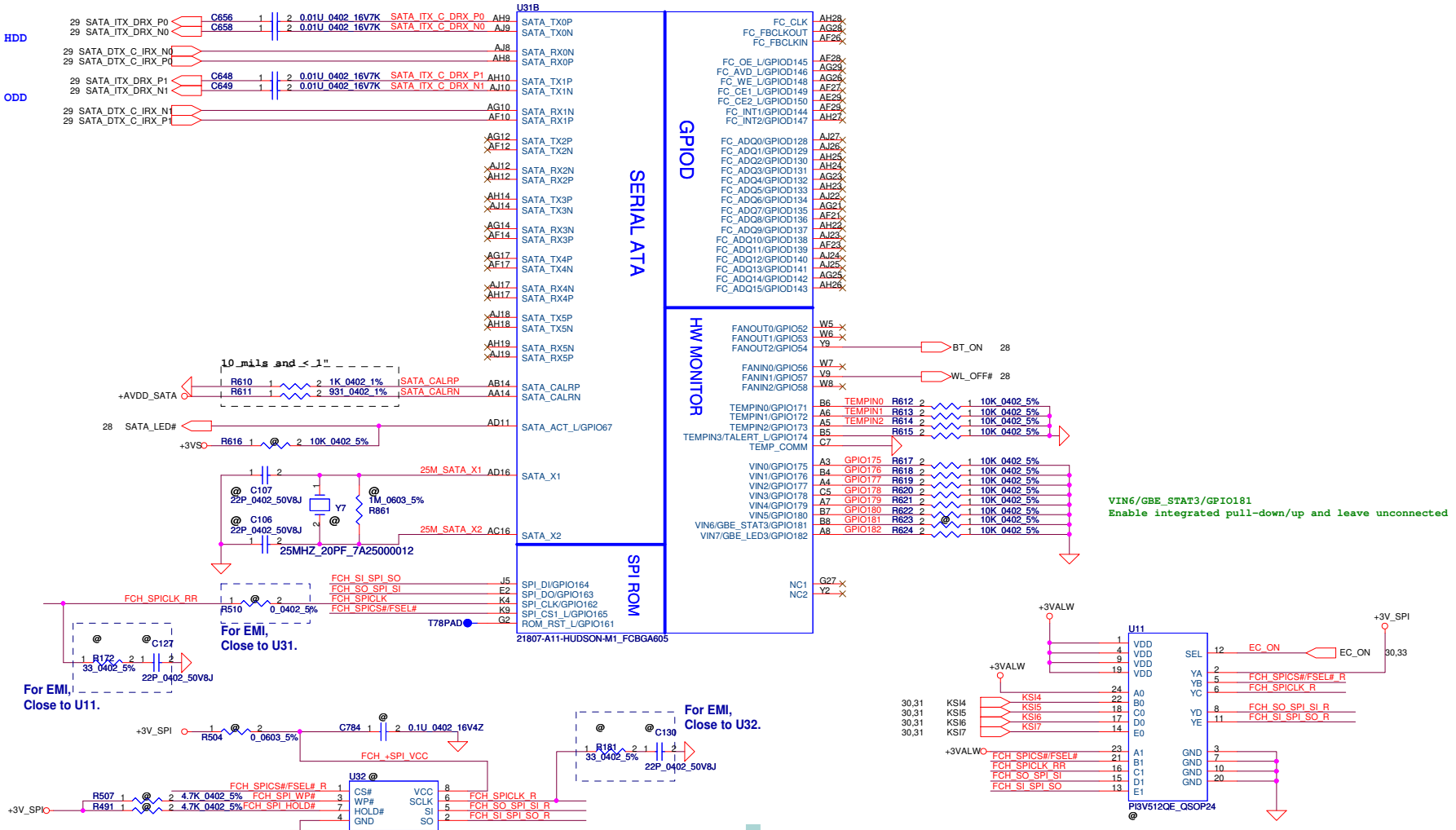
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P13-FCH HDA/USB/ACPI

Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

Date: Thursday, February 17, 2011 | Sheet 13 of 46



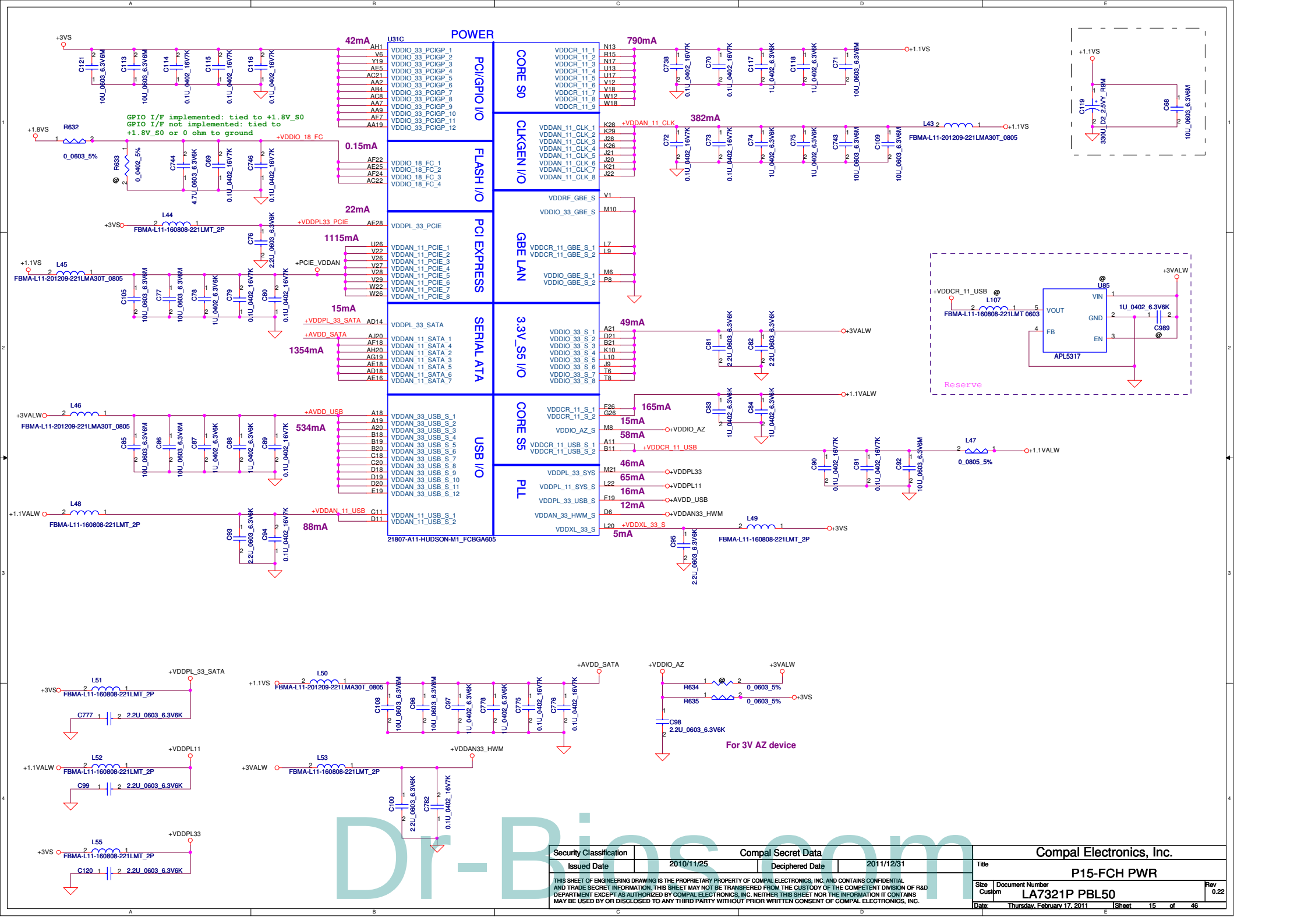
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P14-FCH-SATA/SPI

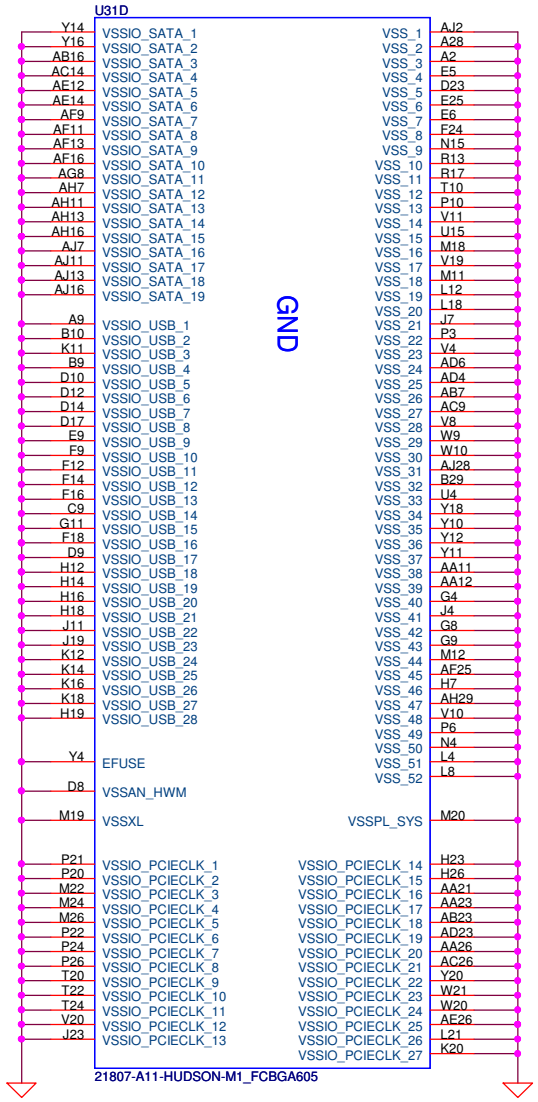
Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

Date: Wednesday, February 16, 2011 | Sheet 14 of 46



Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

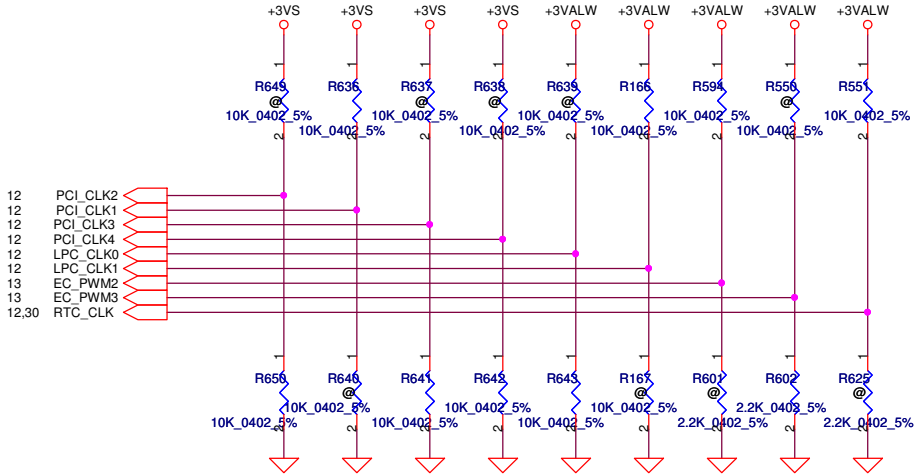
Compal Electronics, Inc.			
Title	P15-FCH PWR		
Size: Custom	Document Number: LA7321P PBL50		Rev: 0.22
Date: Thursday, February 17, 2011	Sheet 15 of 46		



REQUIRED STRAPS

Check Internal PU/PD

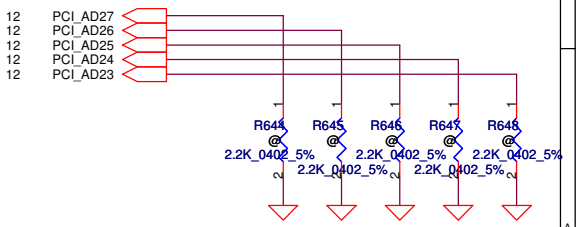
	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H.L) *
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)



DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved



Check AD29,AD28 strap function check default

Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

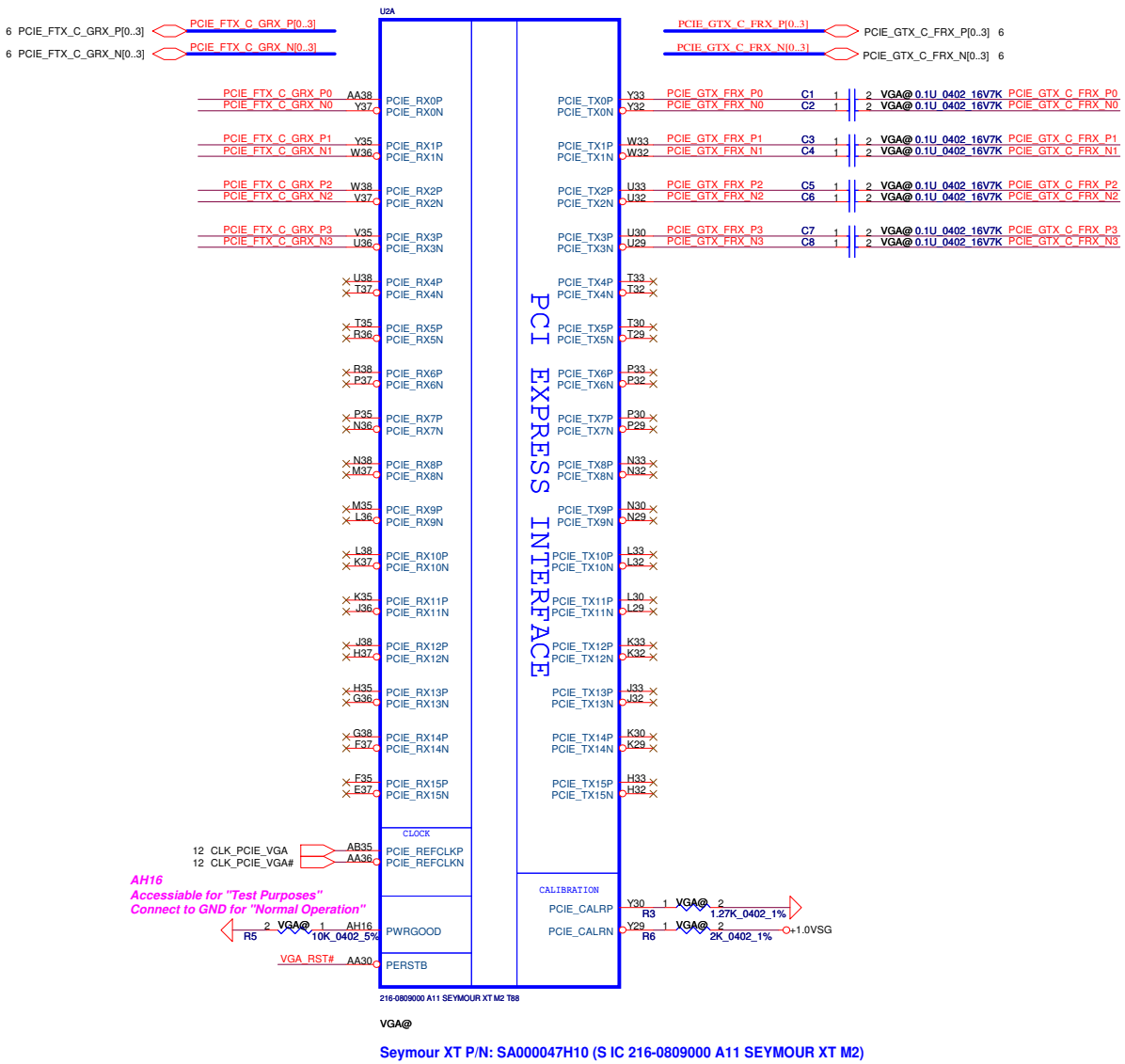
Compal Electronics, Inc.

Title: P16-FCH-VSS/Strap

Size: B | Document Number: LA7321P PBL50 | Rev: 0.22

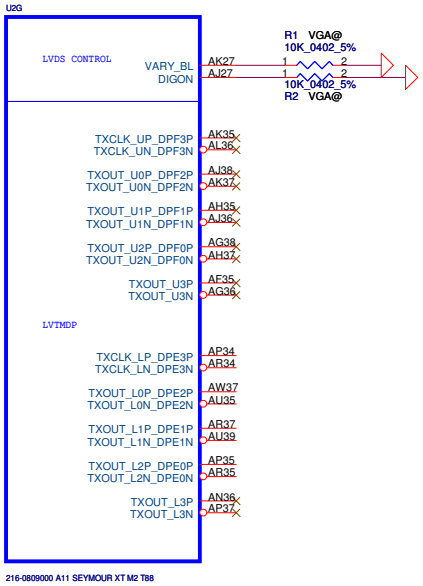
Date: Wednesday, February 16, 2011 | Sheet 16 of 46

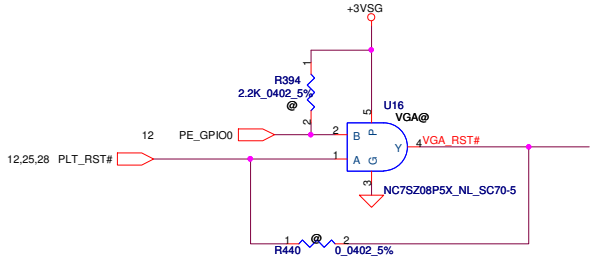
GFX PCIE LANE REVERSAL



Seymour XT P/N: SA000047H10 (S IC 216-0809000 A11 SEYMOUR XT M2)

add for VB support.





Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

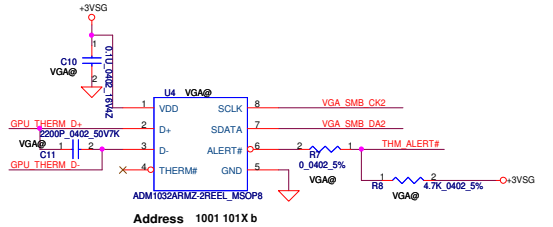
Title: P17-Vancouver_ PCIE / LVDS

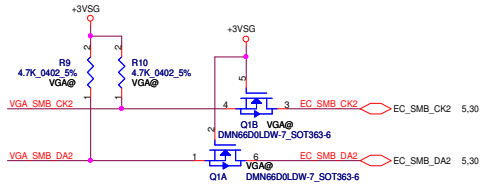
Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

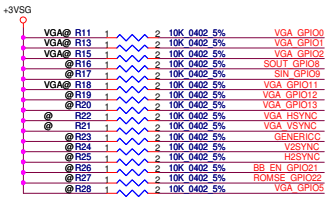
Date: Wednesday, February 16, 2011 | Sheet 17 of 46

Strap Name		Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

External VGA Thermal Sensor

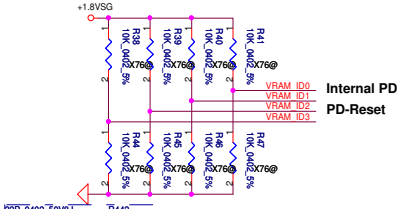


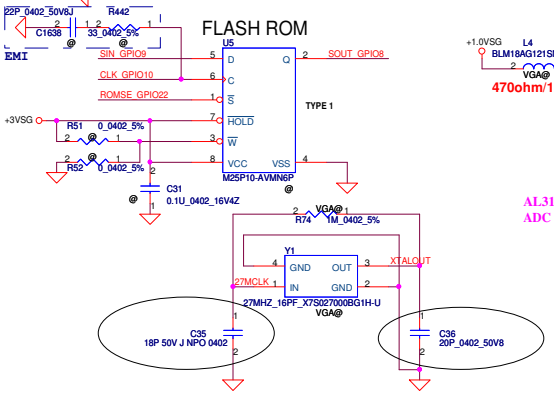


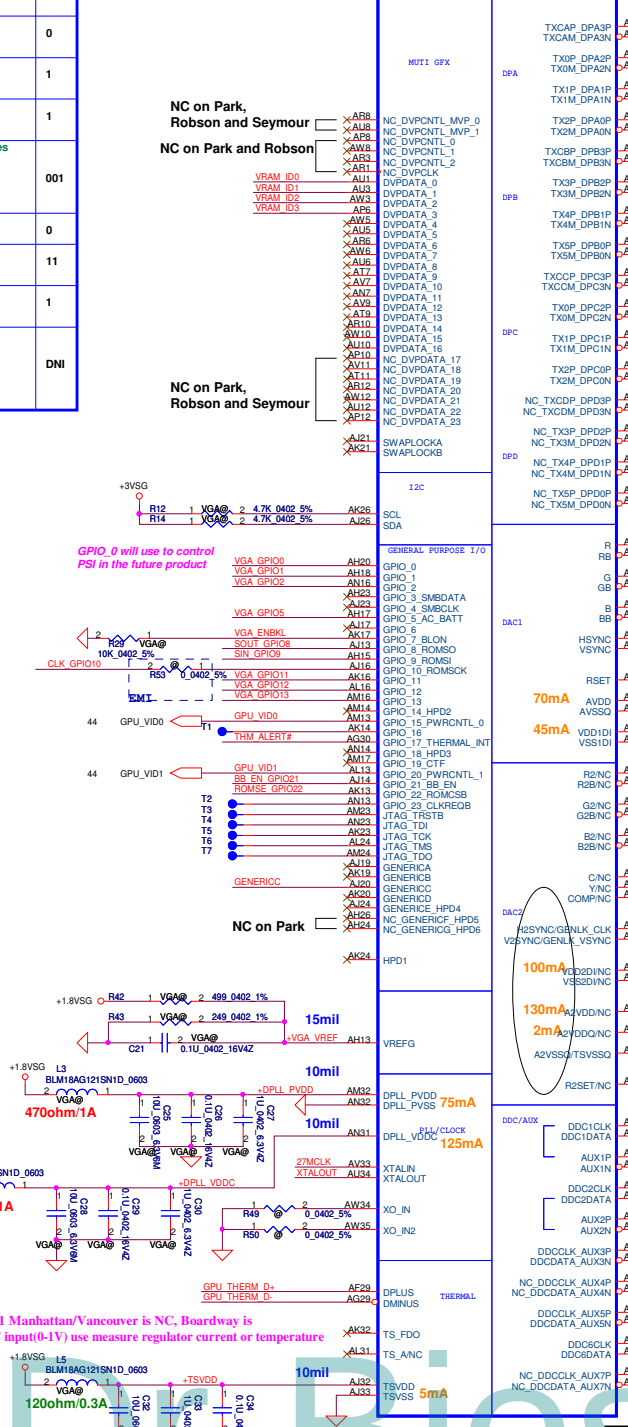


Seymour(XT)

VRAM \ Location	VRAM_ID3 <Revserve>	VRAM_ID2 <Vendor>	VRAM_ID1 <Revserve>	VRAM_ID0 <size>
Samsung 1G X76L01	0	0	0	1
Hynix 1G X76L02	0	1	0	1
Samsung 512M X76L03	0	0	0	0
Hynix 512M X76L04	0	1	0	0







Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

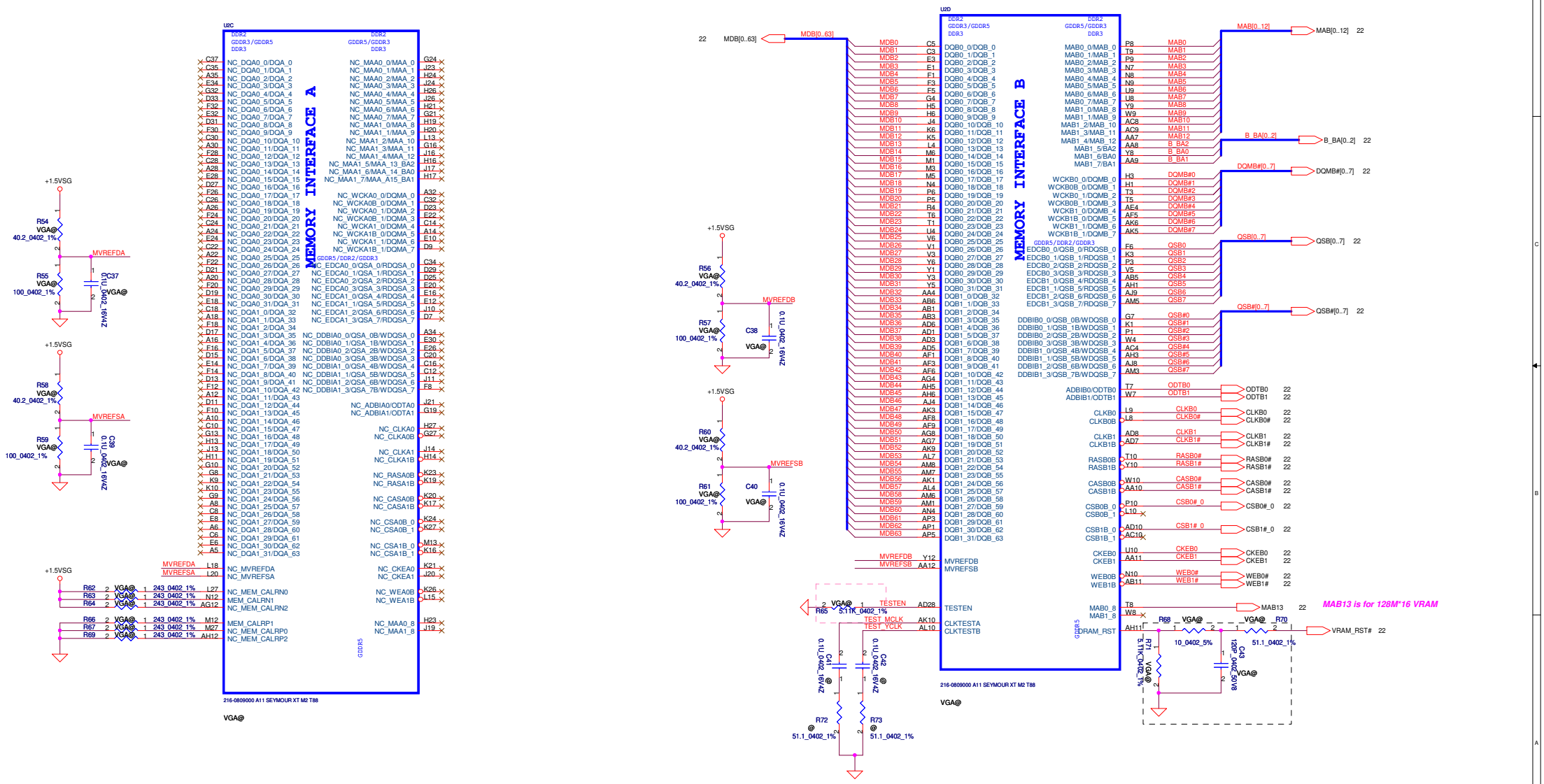
Compal Electronics, Inc.

Title: P18-Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

Date: Friday, February 18, 2011 Sheet 18 of 46

Robson,Seymour only support single channel memory (channel B only)



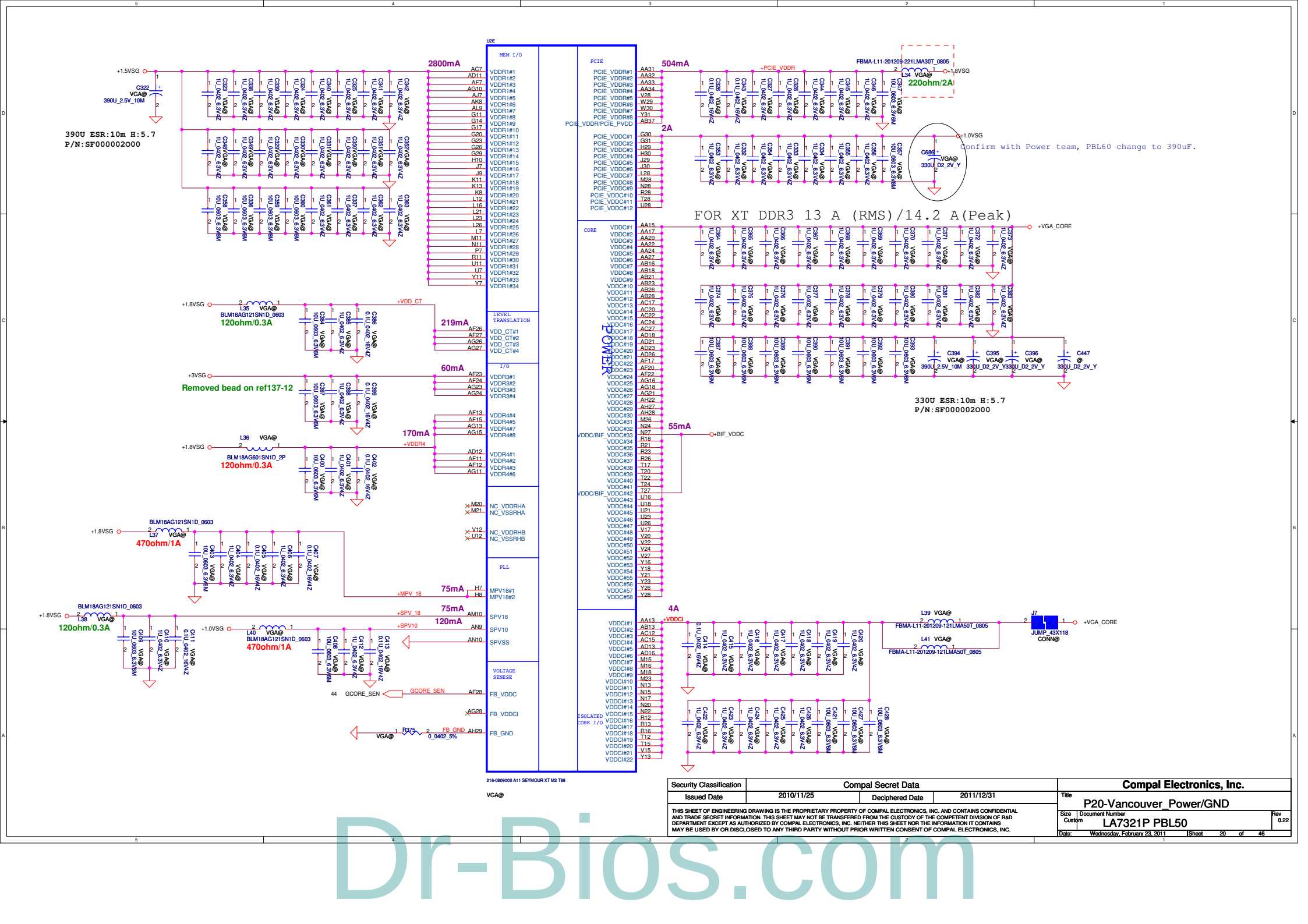
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P19-Vancouver_Memory

Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

Date: Tuesday, February 15, 2011 | Sheet 19 of 46



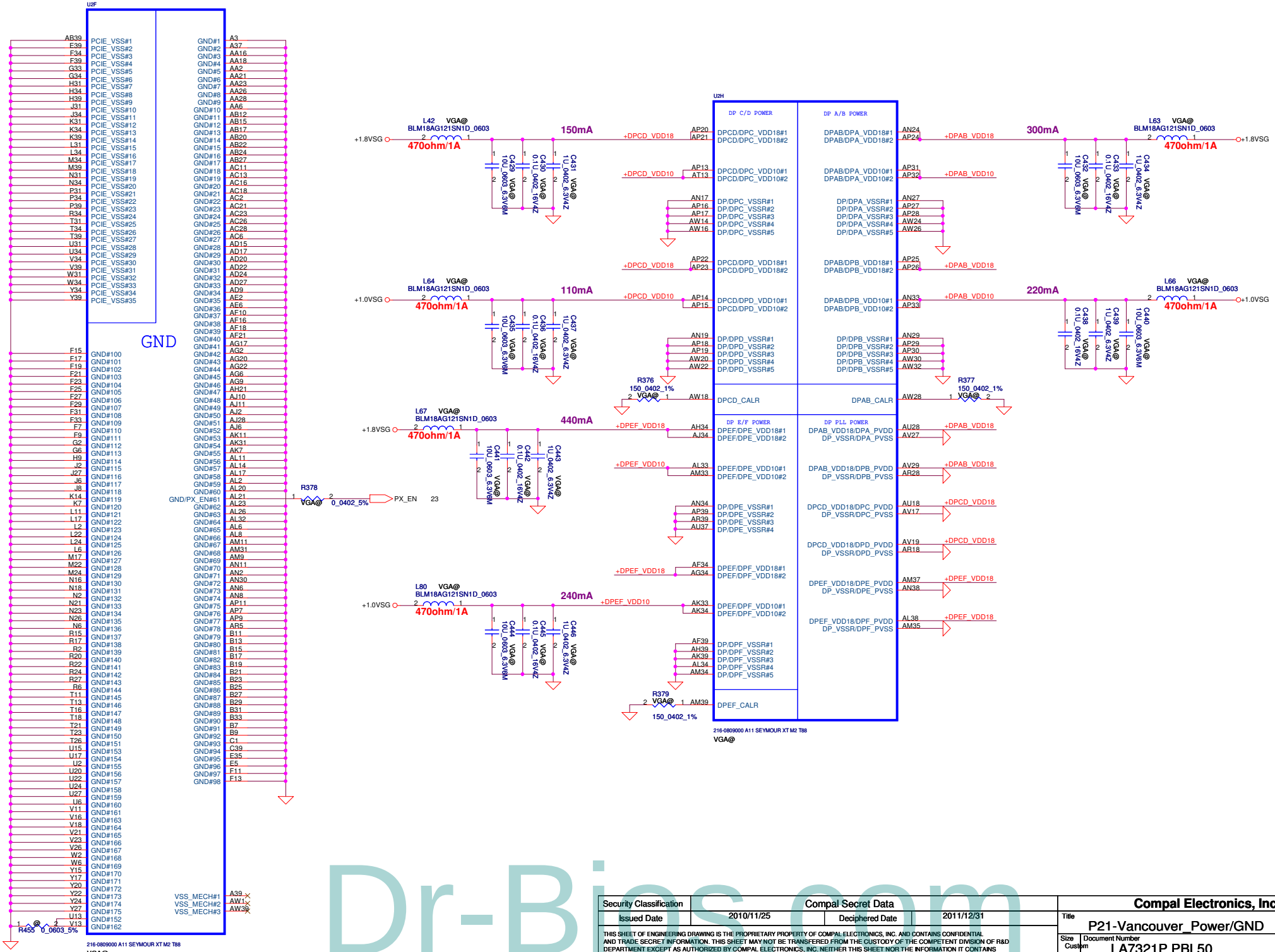
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P20-Vancouver_Power/GND

Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

Date: Wednesday, February 23, 2011 | Sheet 20 of 46



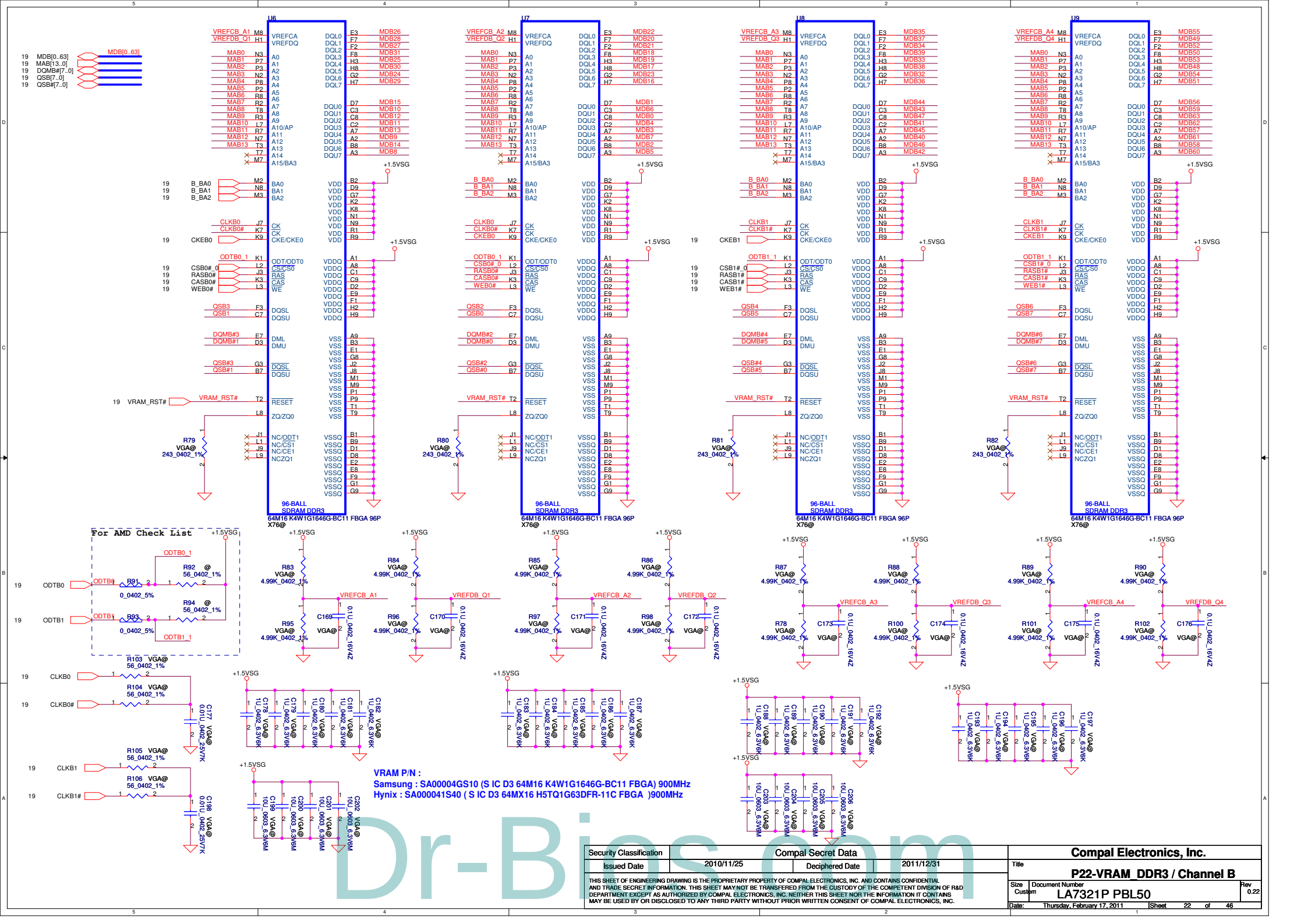
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P21-Vancouver_Power/GND

Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

Date: Tuesday, February 15, 2011 | Sheet 21 of 46


U6
U7
U8
U9
96-BALL SDRAM DDR3
64M16 K4W1G1646G-BC11 FBGA 96P
X76@
For AMD Check List
+1.5VSG
VRAM P/N :
Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA) 900MHz
Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA)900MHz
Dr-Bios.com
Security Classification
Compal Secret Data
Issued Date
2010/11/25
Deciphered Date
2011/12/31
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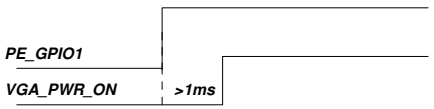
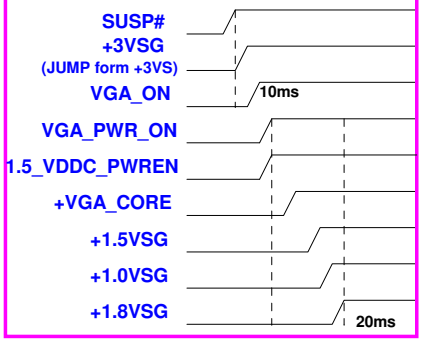
Compal Electronics, Inc.
Title
P22-VRAM_DDR3 / Channel B
Size
Custom
Document Number
LA7321P PBL50
Rev
0.22
Date:
Thursday, February 17, 2011
Sheet
22
of
46

For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON

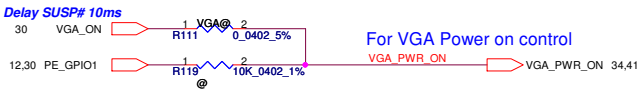


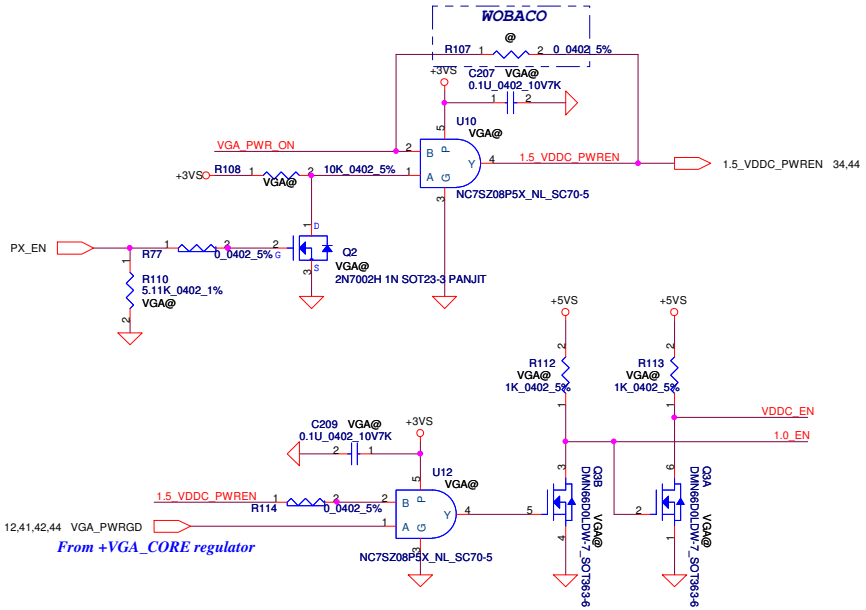
Power Sequence of Whistler and Seymour

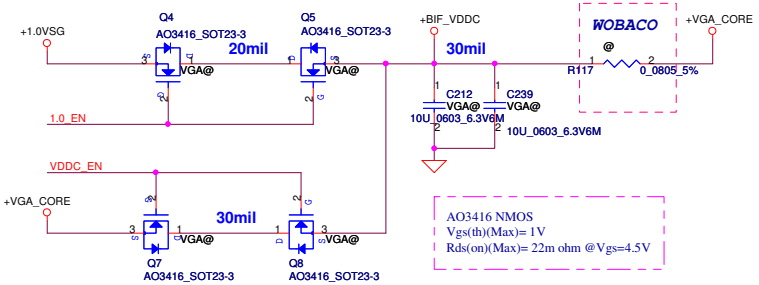


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN







Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P23-VGA power sequence and BACO

Size: Custom | Document Number: LA7321P PBL50 | Rev: 0.22

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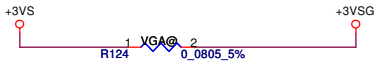
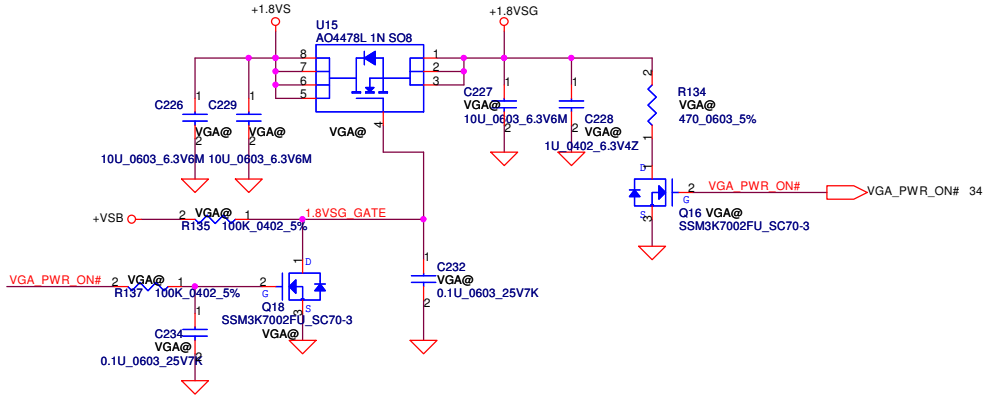
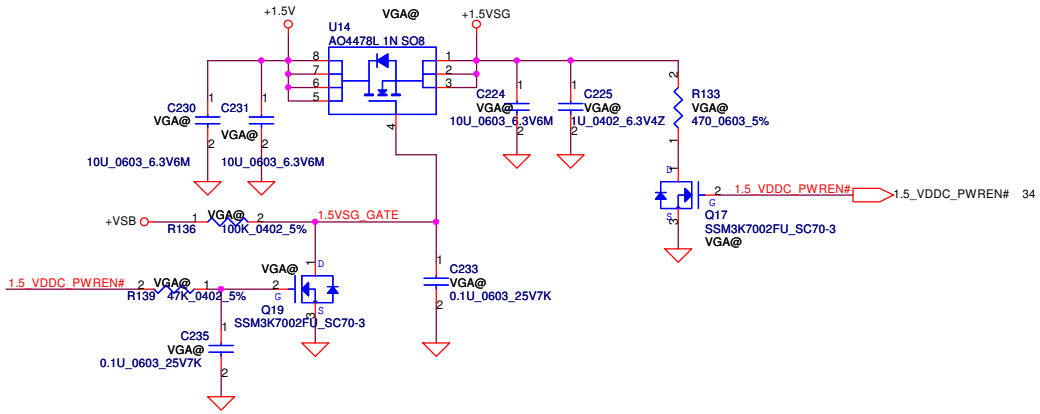
+3.3VS TO +3.3VSG



+1.8VS TO +1.8VSG

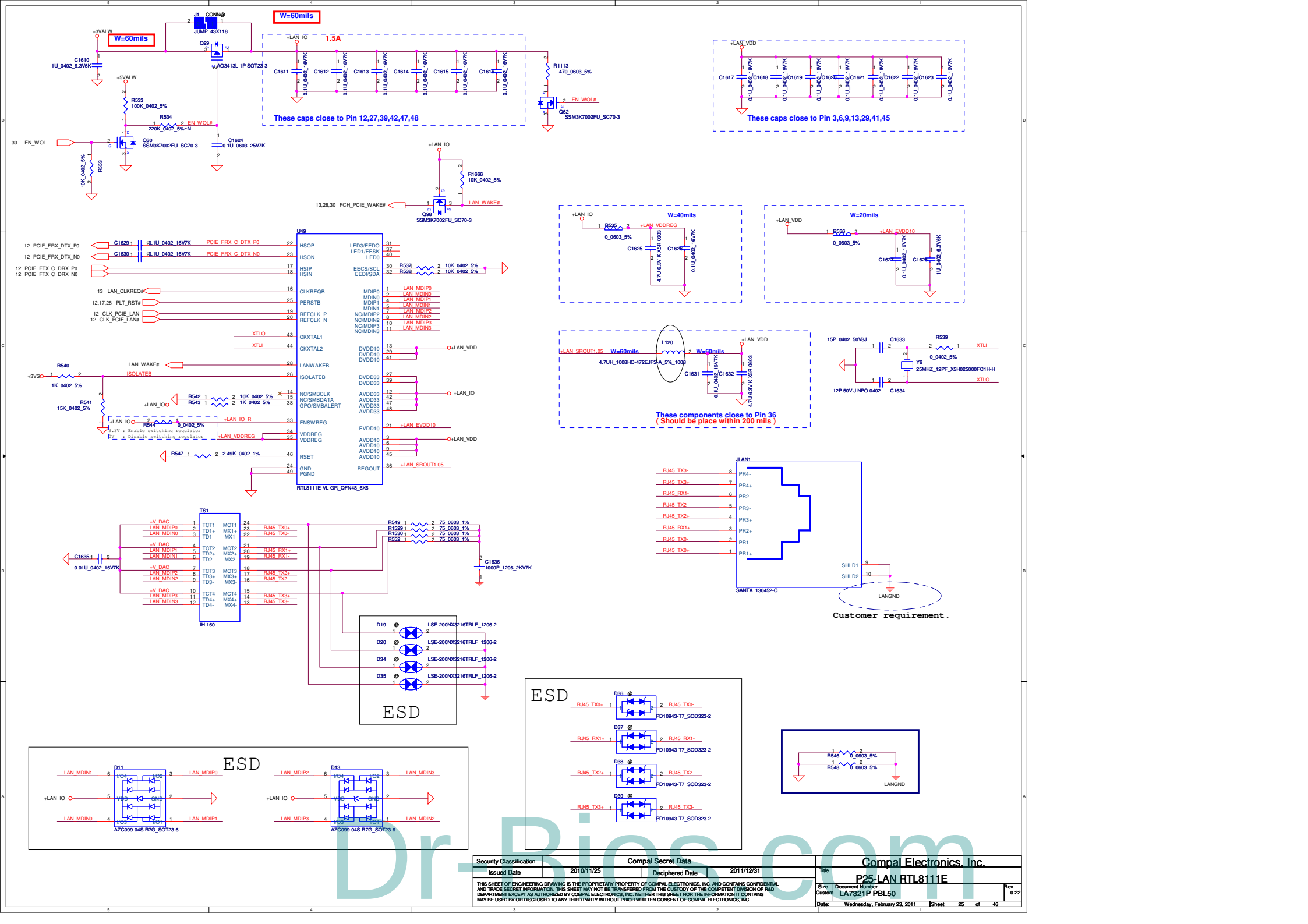


+1.5V TO +1.5VSG



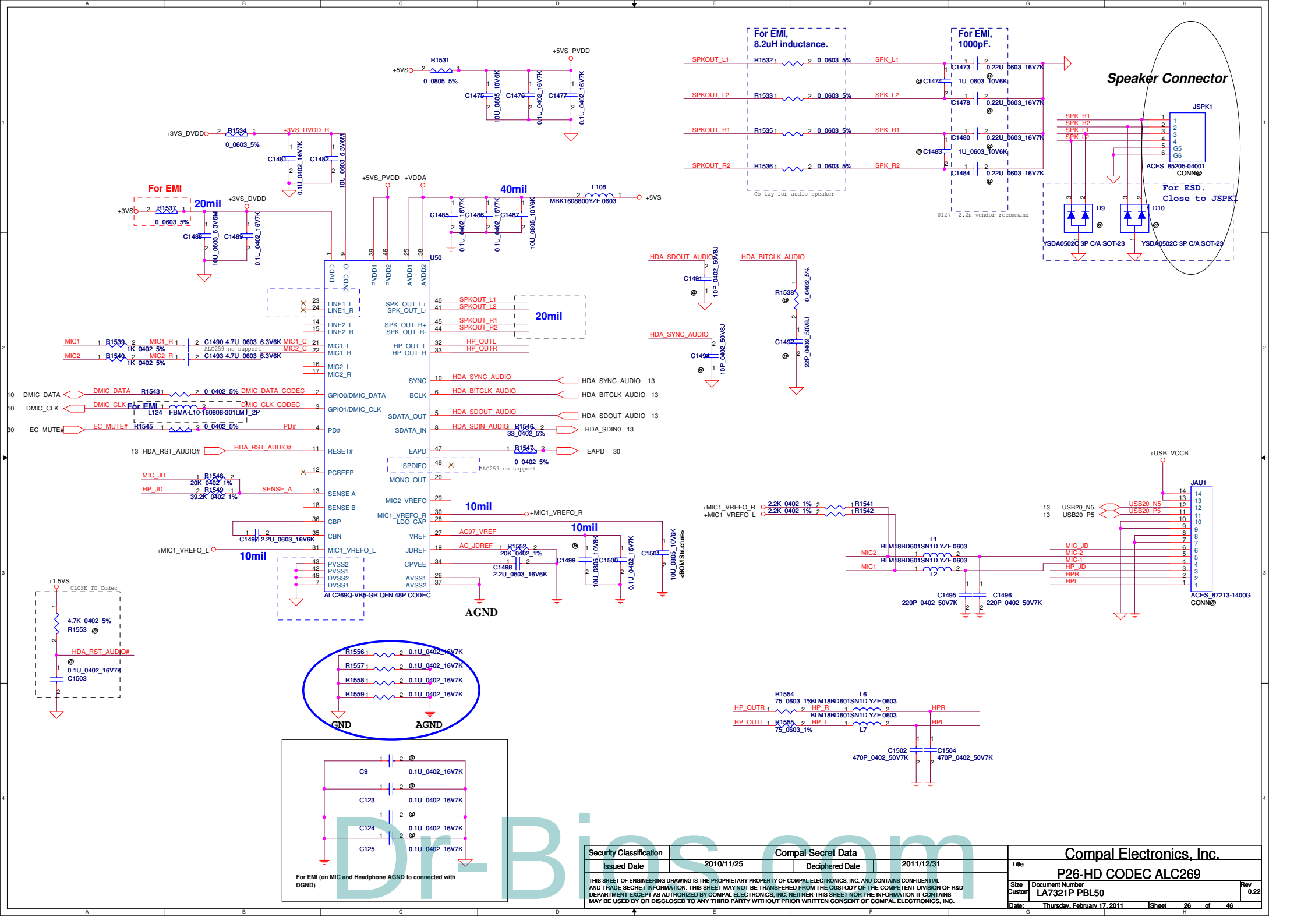
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.		
Title	P24-VGA DC Interface	
Size: Custom	Document Number: LA7321P PBL50	Rev: 0.22
Date: Tuesday, February 15, 2011	Sheet 24 of 46	



Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	P25-LAN RTL8111E		
Size	Document Number		Rev
Custom	LA7321P PBL50		0.22
Date:	Wednesday, February 23, 2011	Sheet	25 of 46



Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

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Compal Electronics, Inc.	
Title	P26-HD CODEC ALC269
Size: Custom	Document Number: LA7321P PBL50
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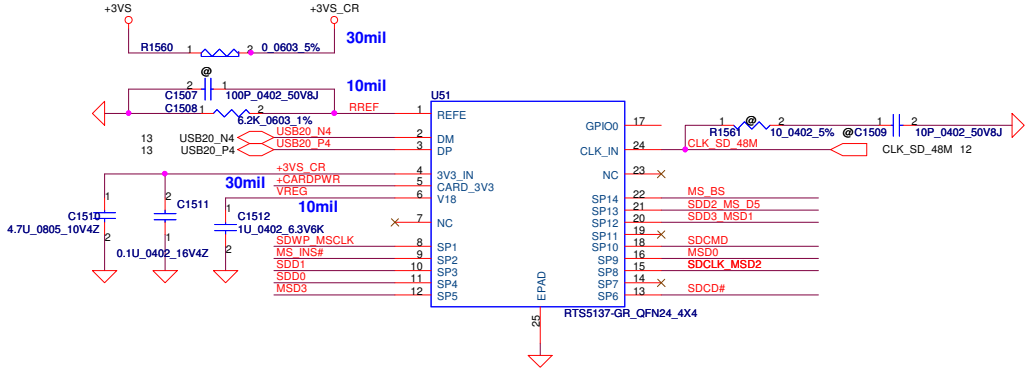
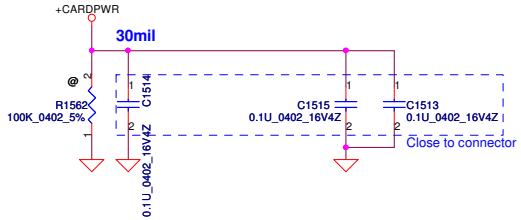
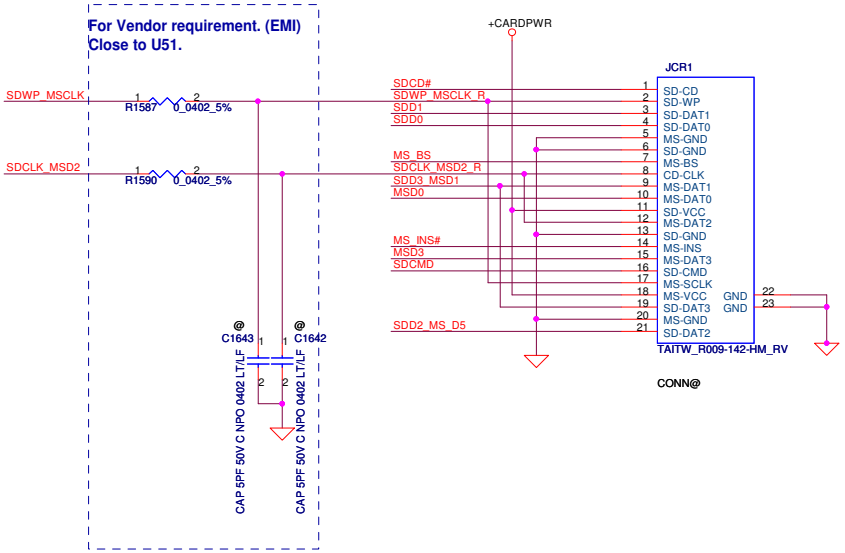
Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector

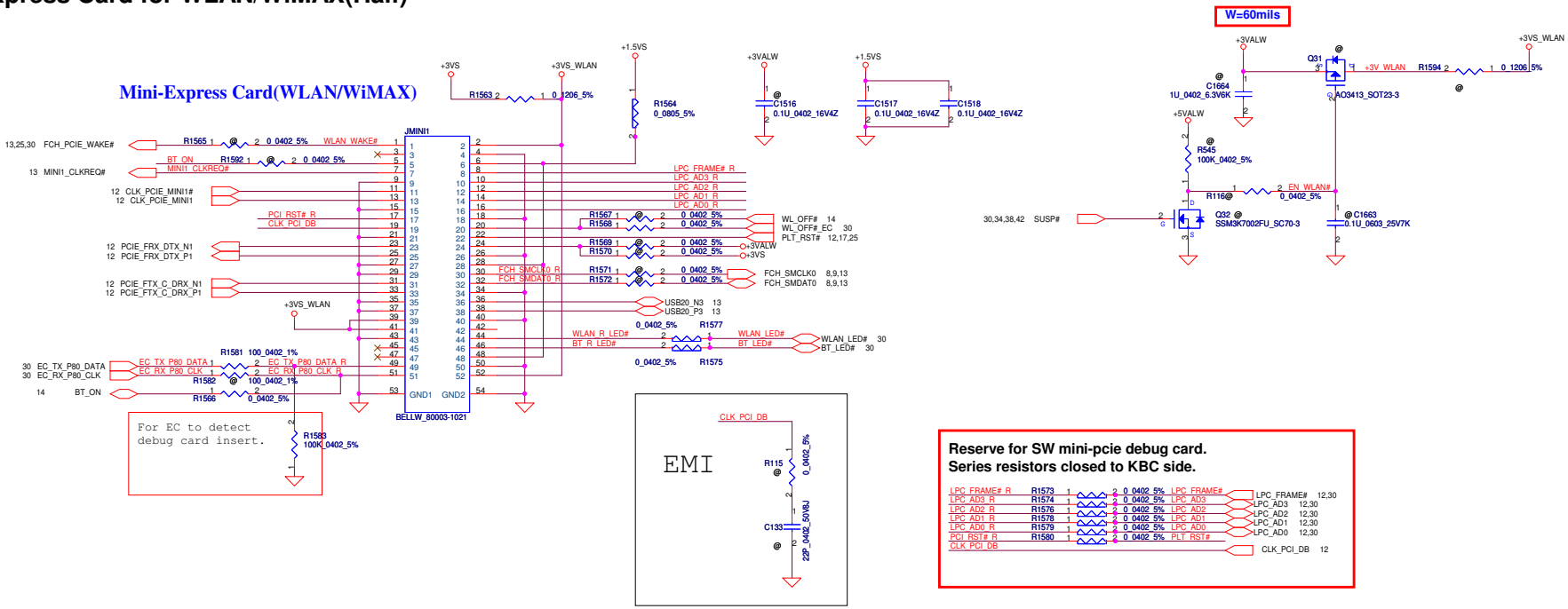




Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

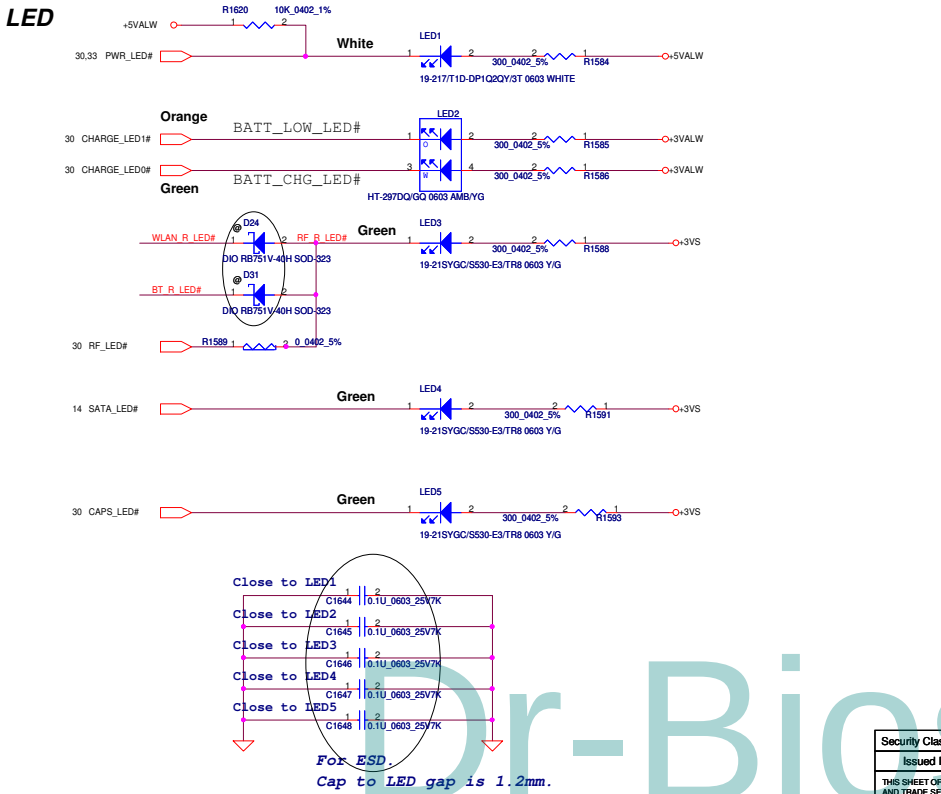
Compal Electronics, Inc.		
Title	P27-RTS5137 Media Card Controller	
Size: Custom	Document Number: LA7321P PBL50	Rev: 0.22
Date: Thursday, February 17, 2011	Sheet 27 of 46	

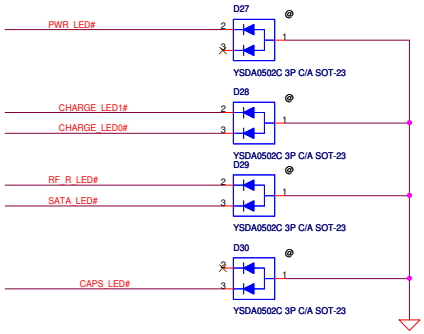
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LED

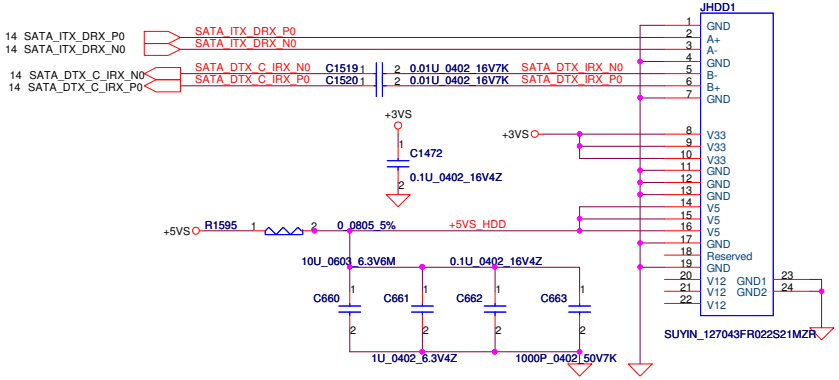




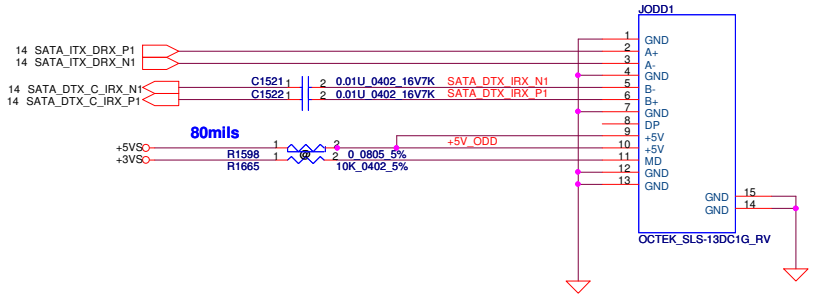
Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	P28-Mini PCIE/LED		
Size	Document Number		Rev
	LA7321P PBL50		0.22
Date:	Friday, February 18, 2011	Sheet	28 of 46

SATA HDD Conn.



SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.		
Title	P29-HDD & ODD CONN	
Size B	Document Number LA7321P PBL50	Rev 0.22
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 PR	100K	18K	0.5V
3		100K	33K	0.82V

changed 09.09.08

FOR EC 128KB SPI ROM (150mil PACKAGE) SA00002C100

EMI

Reserve, and close to U47.

If Q8 or R429, R432 implemented, R747 & R748 need to be mounted

20mils

Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P30-BIOS & EC KB930

Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

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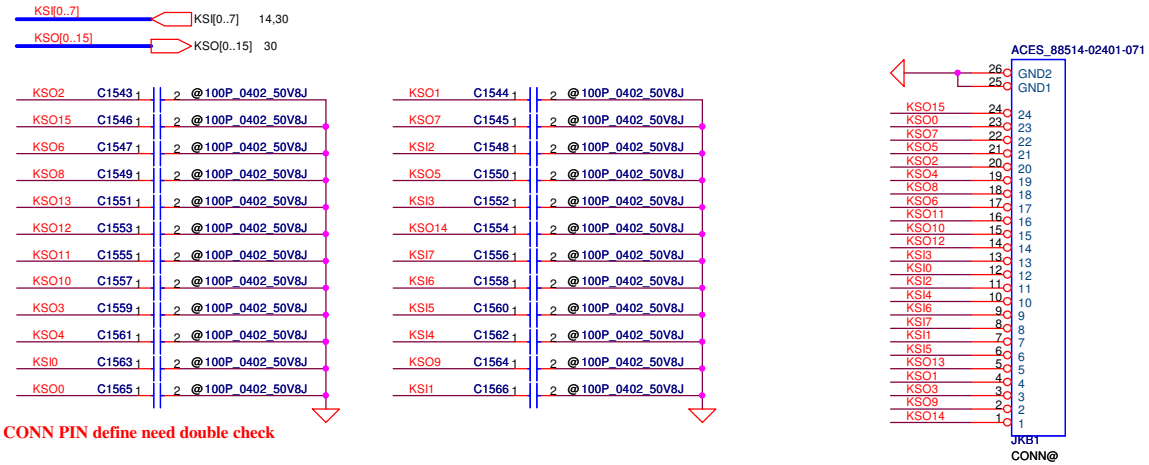
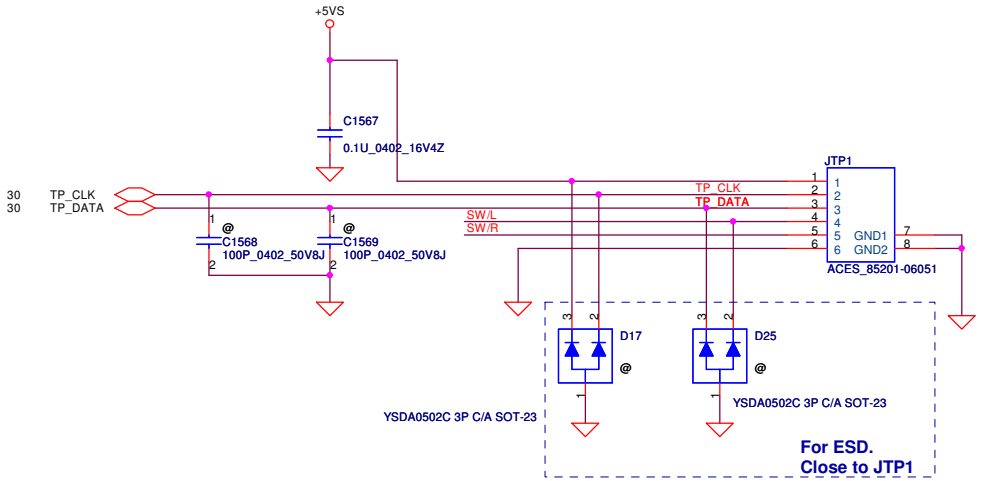
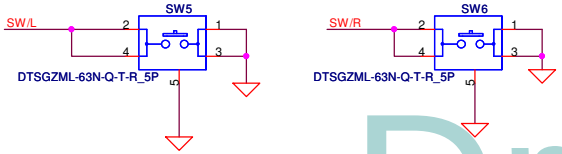
INT_KBD Conn.



CONN PIN define need double check

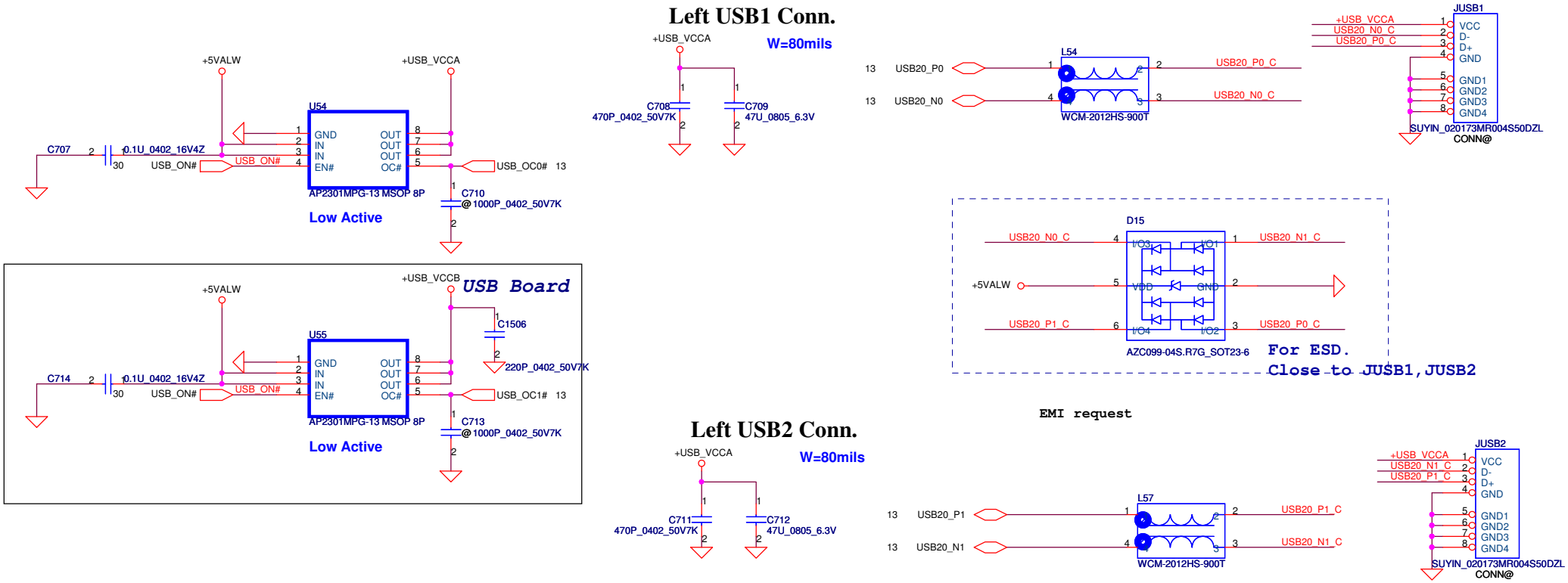
To TP/B Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	P31-KB /SW/TP/Lid		
Size B	Document Number LA7321P PBL50		Rev 0.22
Date: Tuesday, February 15, 2011	Sheet 31 of 46		



Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P32-USB/BT/USBsub

Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

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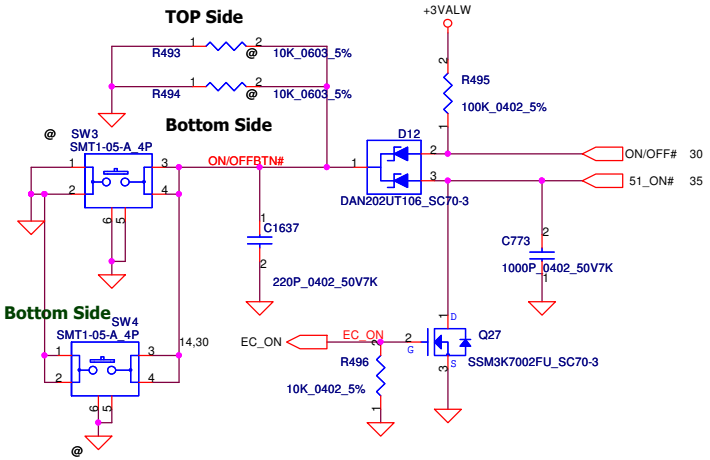
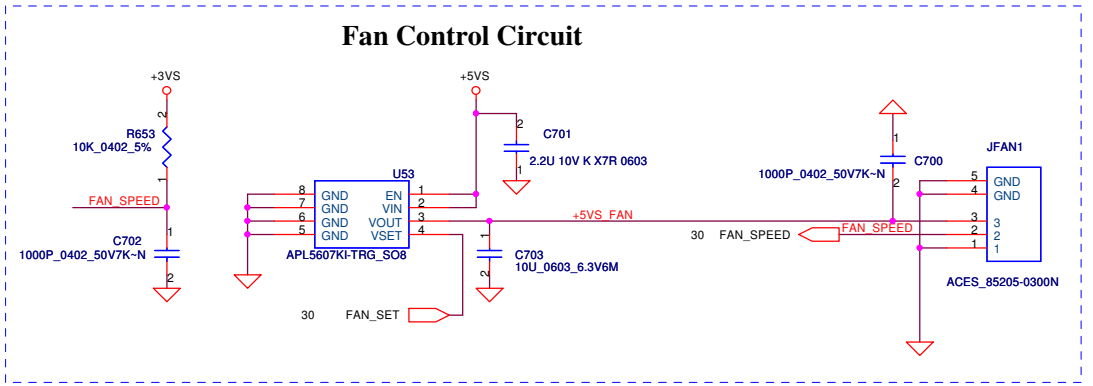
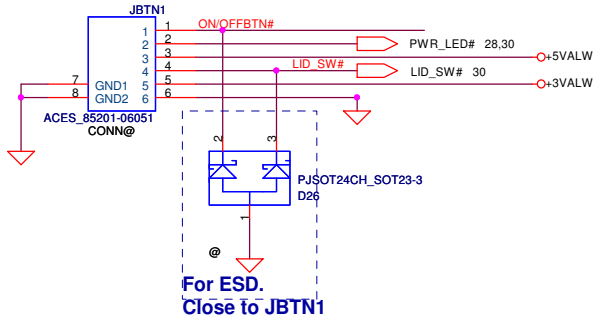
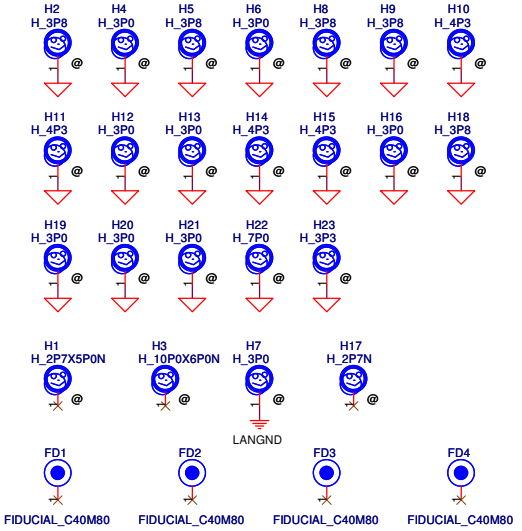
ON/OFF switch **Power Button**









Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/11/25	Deciphered Date 2011/12/31	Title: P33-Other IO/USB (right)

Size	Document Number	Rev
Custom	LA7321P PBL50	0.22

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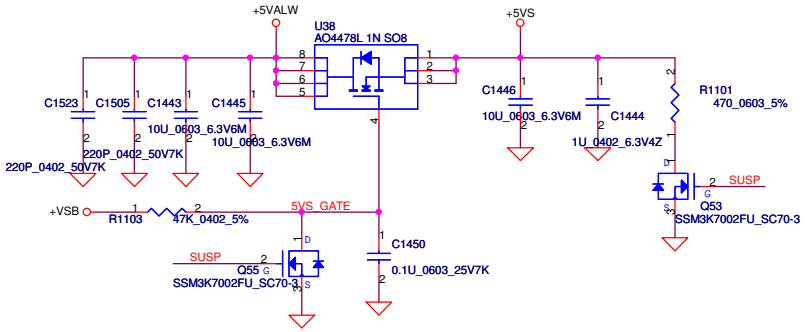
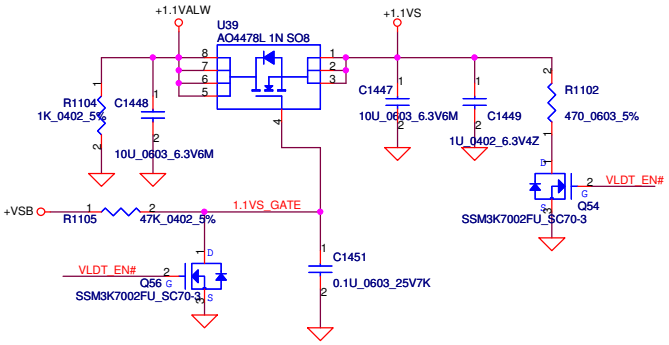
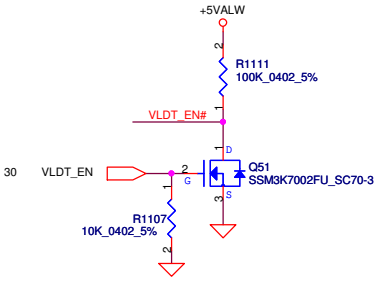
+5VALW TO +5VS

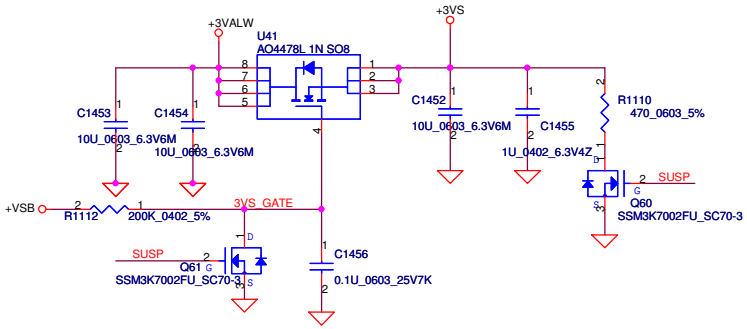


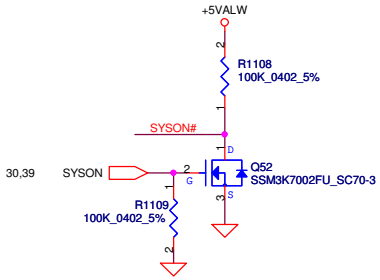
+1.1VALW TO +1.1VS

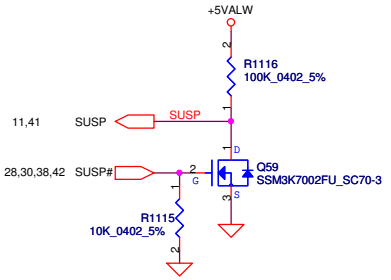




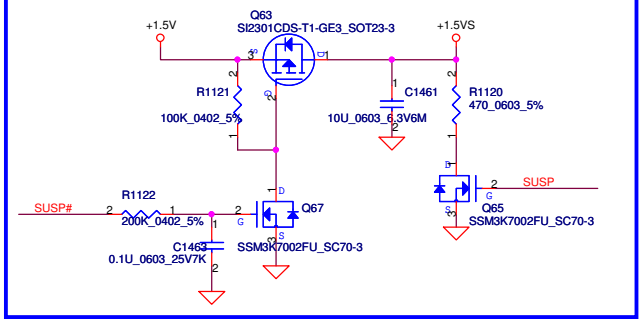
+3VALW TO +3VS

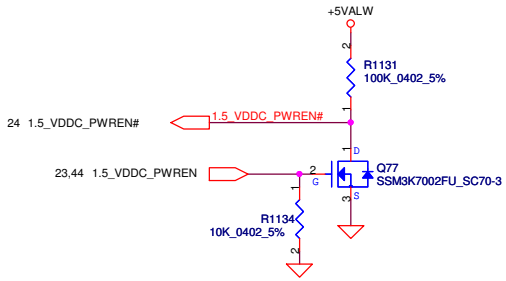


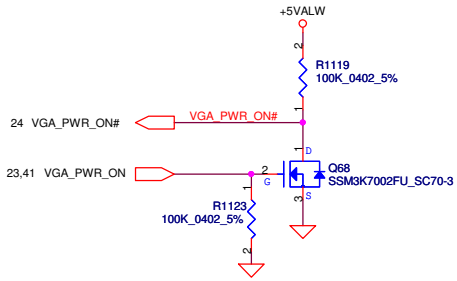


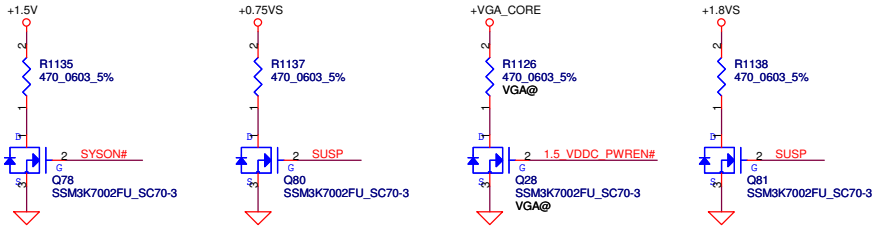


+1.5VS









Security Classification	Compal Secret Data		
Issued Date	2010/11/25	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P34-DC Interface

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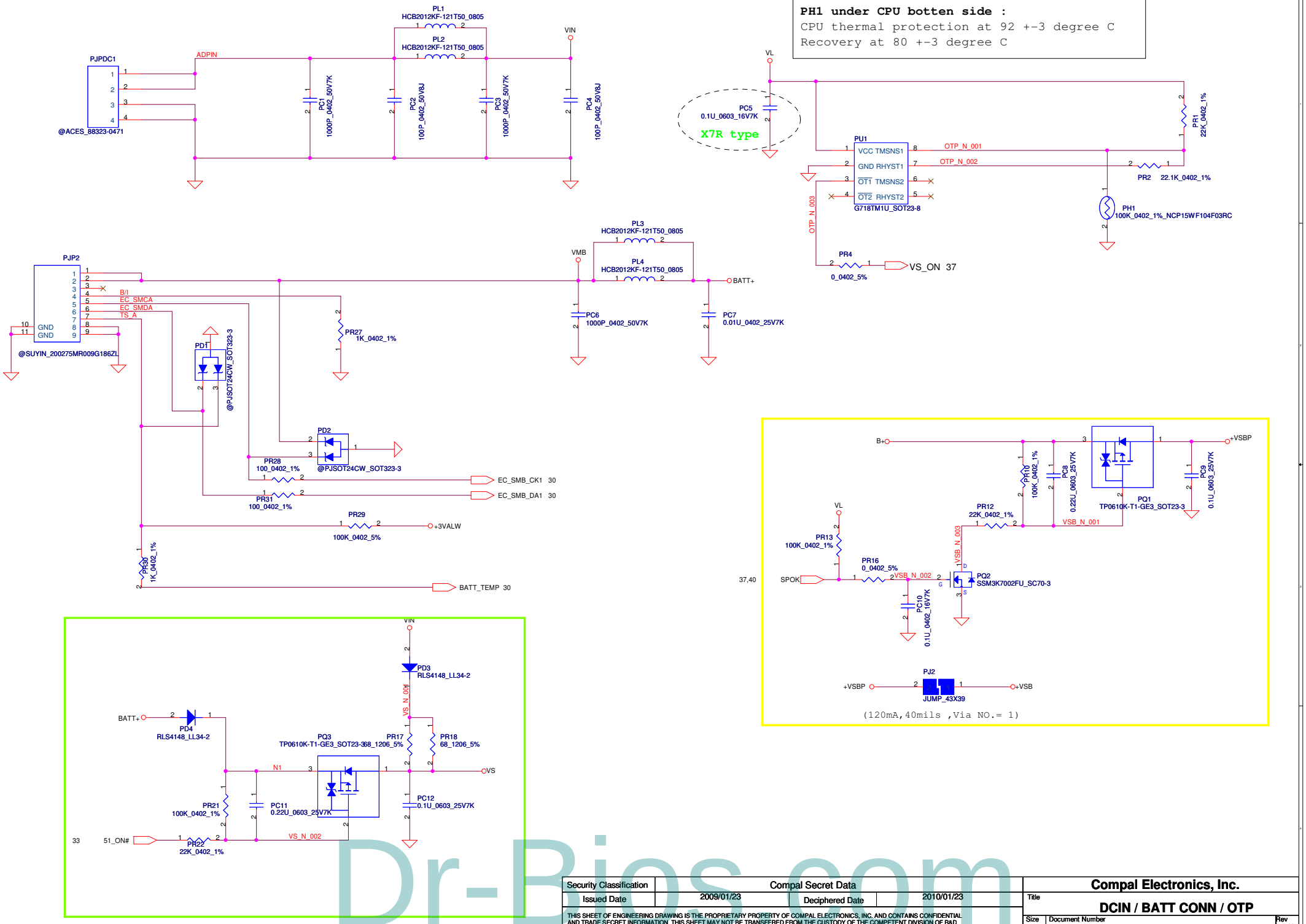

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	DCIN / BATT CONN / OTP		
Size	Document Number		Rev
	NCL61 LA-6321P M/B		0.22
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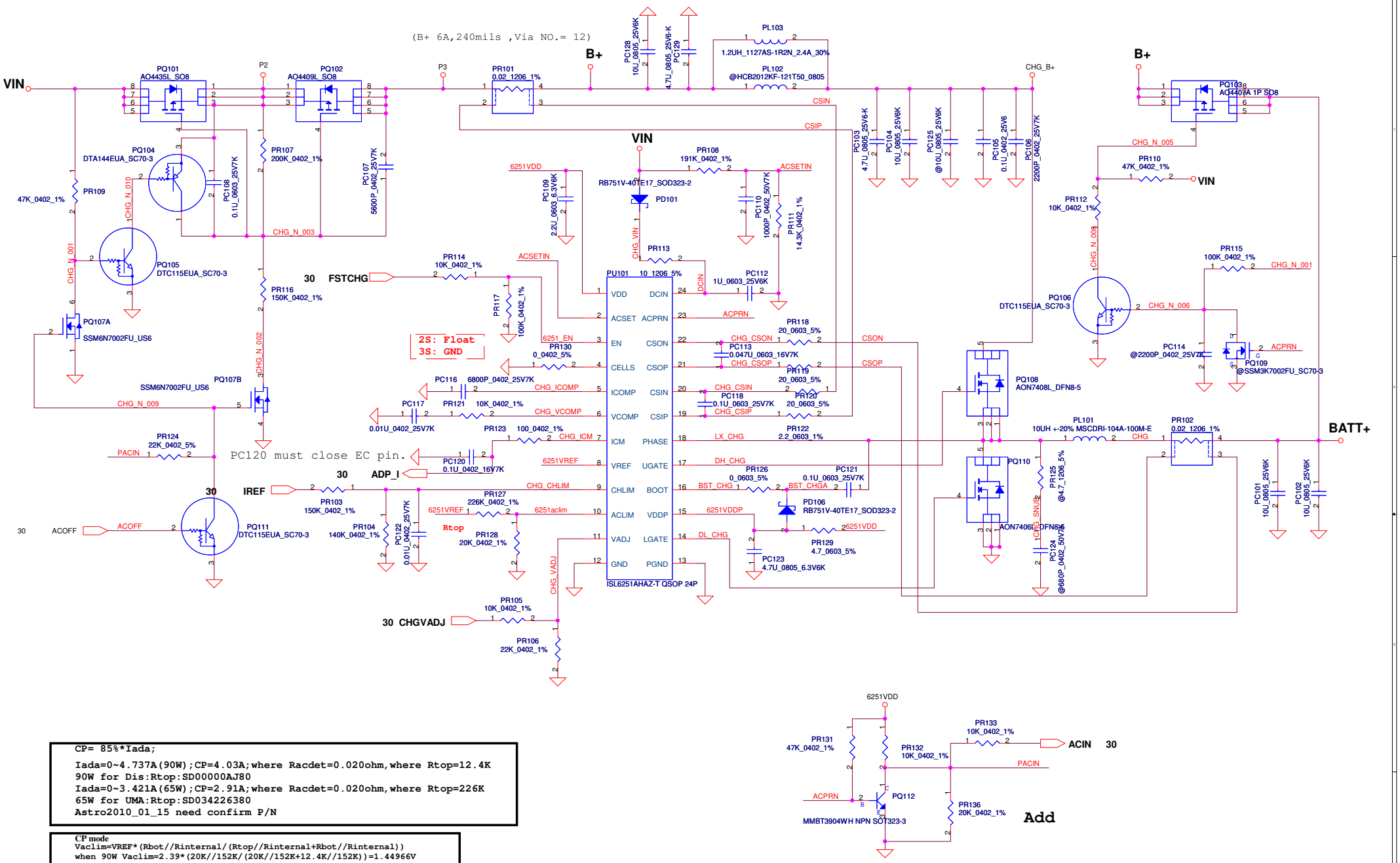


CP= 85%*Iada;

Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

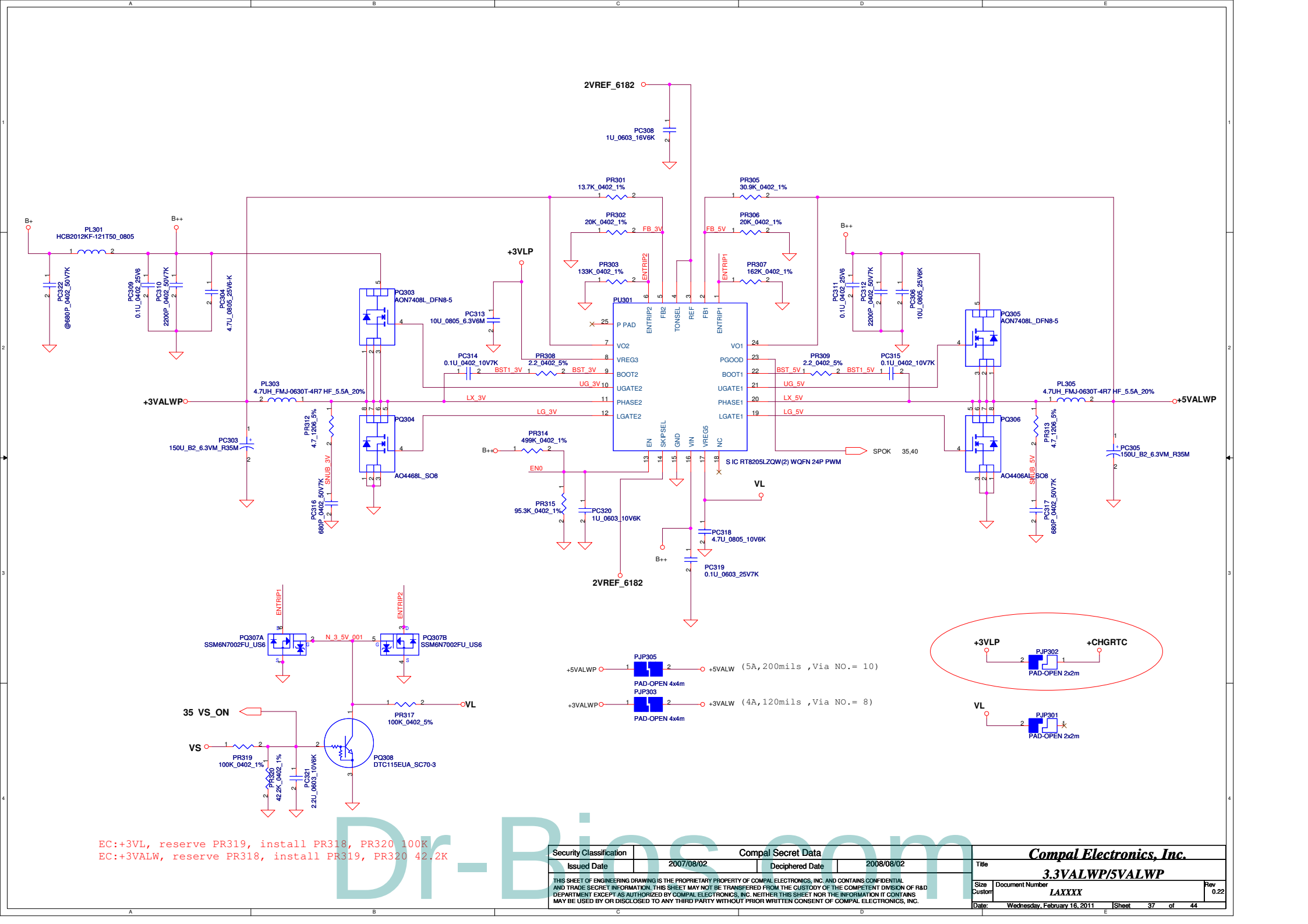
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.22

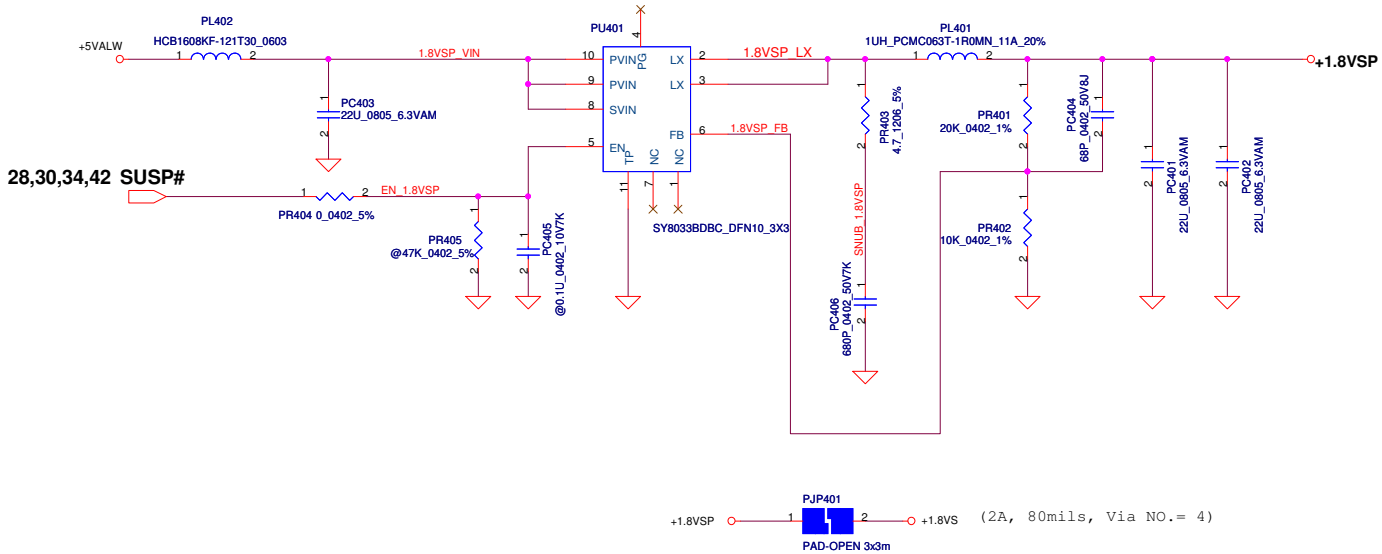
Date: Wednesday, February 16, 2011 | Sheet 36 of 44



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: LAXXXX		Rev: 0.22
Date: Wednesday, February 16, 2011	Sheet 37 of 44		

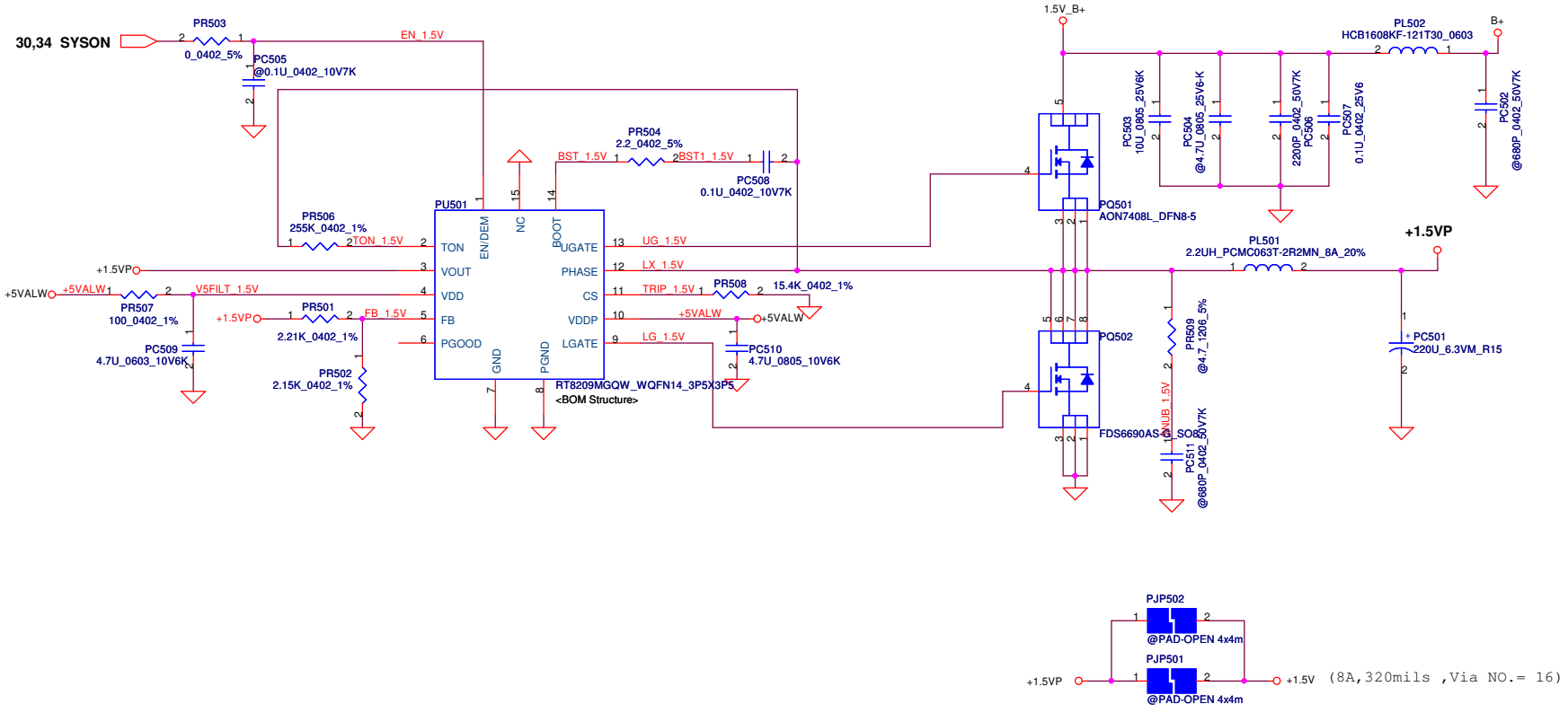


<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2A, 80mils, Via NO.= 4)

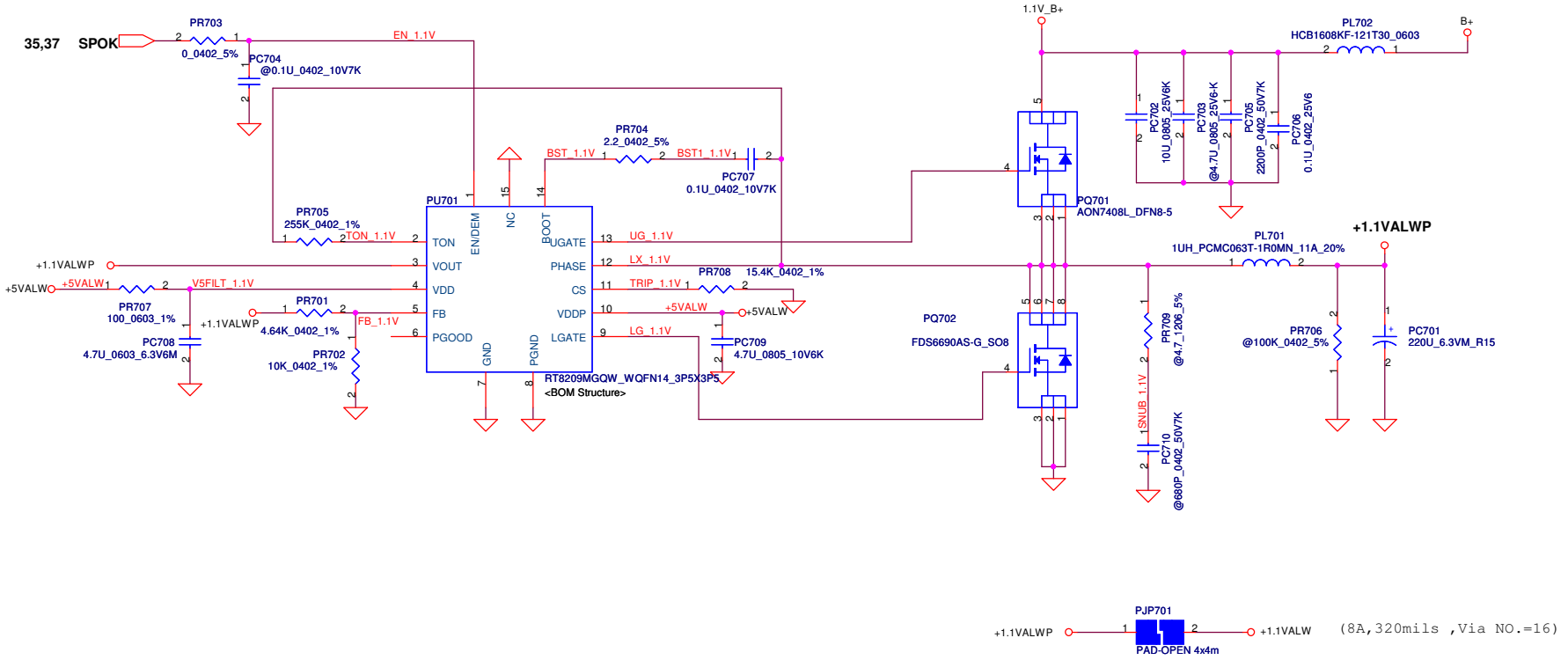
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	+1.8VSP
Size	Document Number: NCL61 LA-6321P M/B
Rev	0.22
Date: Tuesday, February 15, 2011	Sheet 38 of 44



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title	+1.5VP		
Size	Document Number	LAXXXX	Rev 0.22
Date:	Wednesday, February 16, 2011	Sheet 39 of 44	



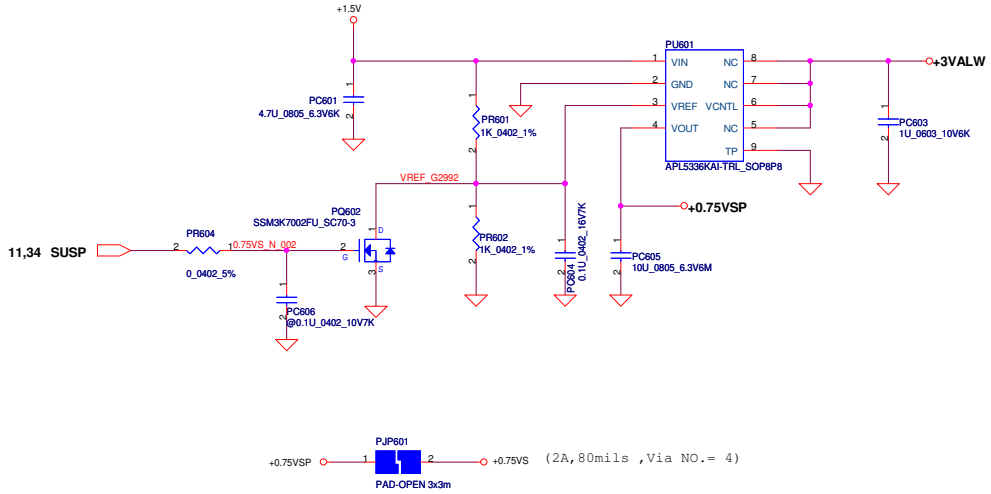
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

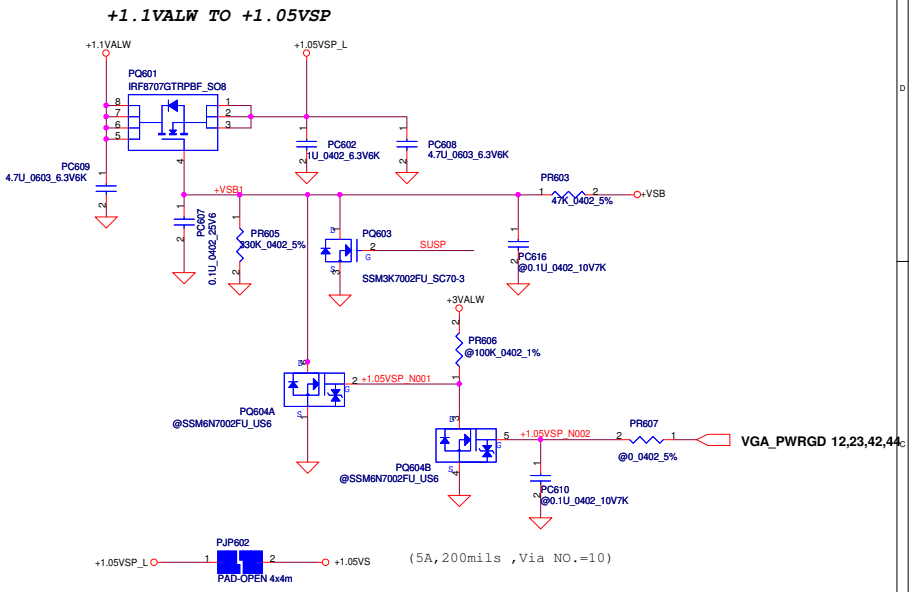
Compal Electronics, Inc.

Title: PWR+1.1VALWP

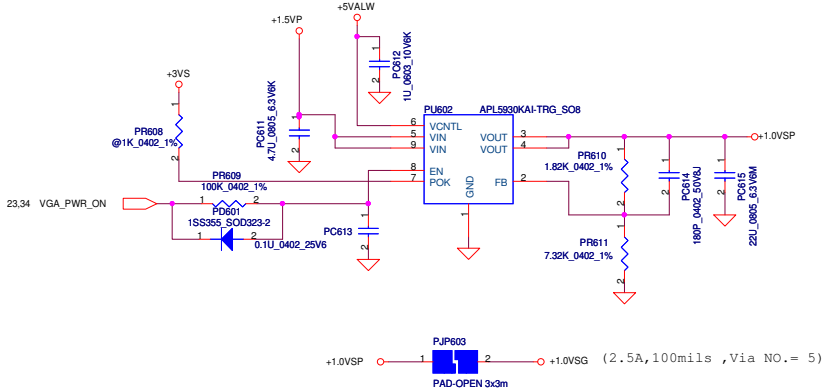
Size: Custom | Document Number: LAXXXX | Rev: 0.22

Date: Wednesday, February 16, 2011 | Sheet 40 of 44





Need to confirm with HW power sequence.



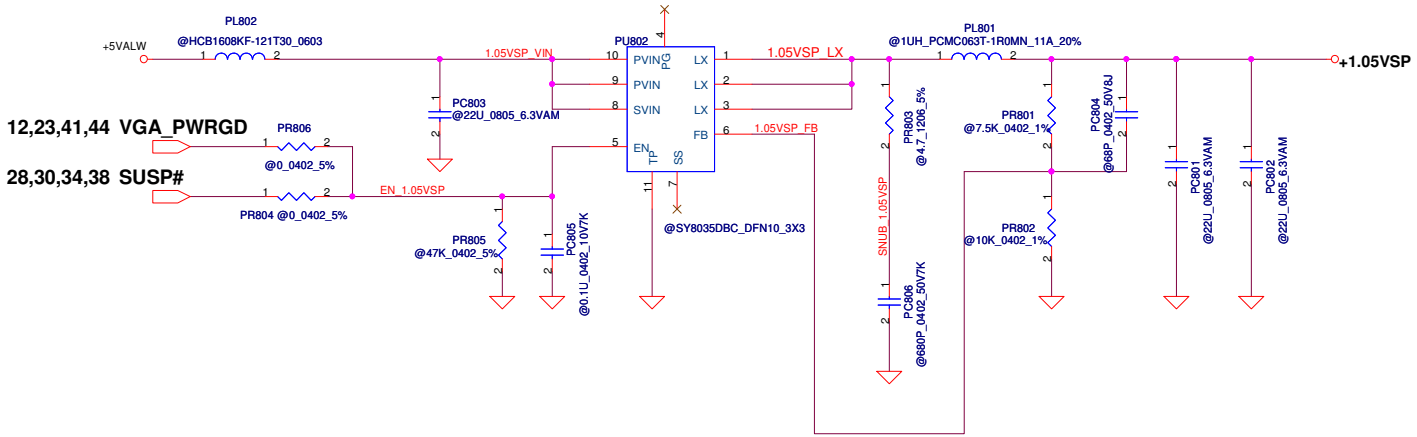
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: PWR 0.75VSP +1.05VSP

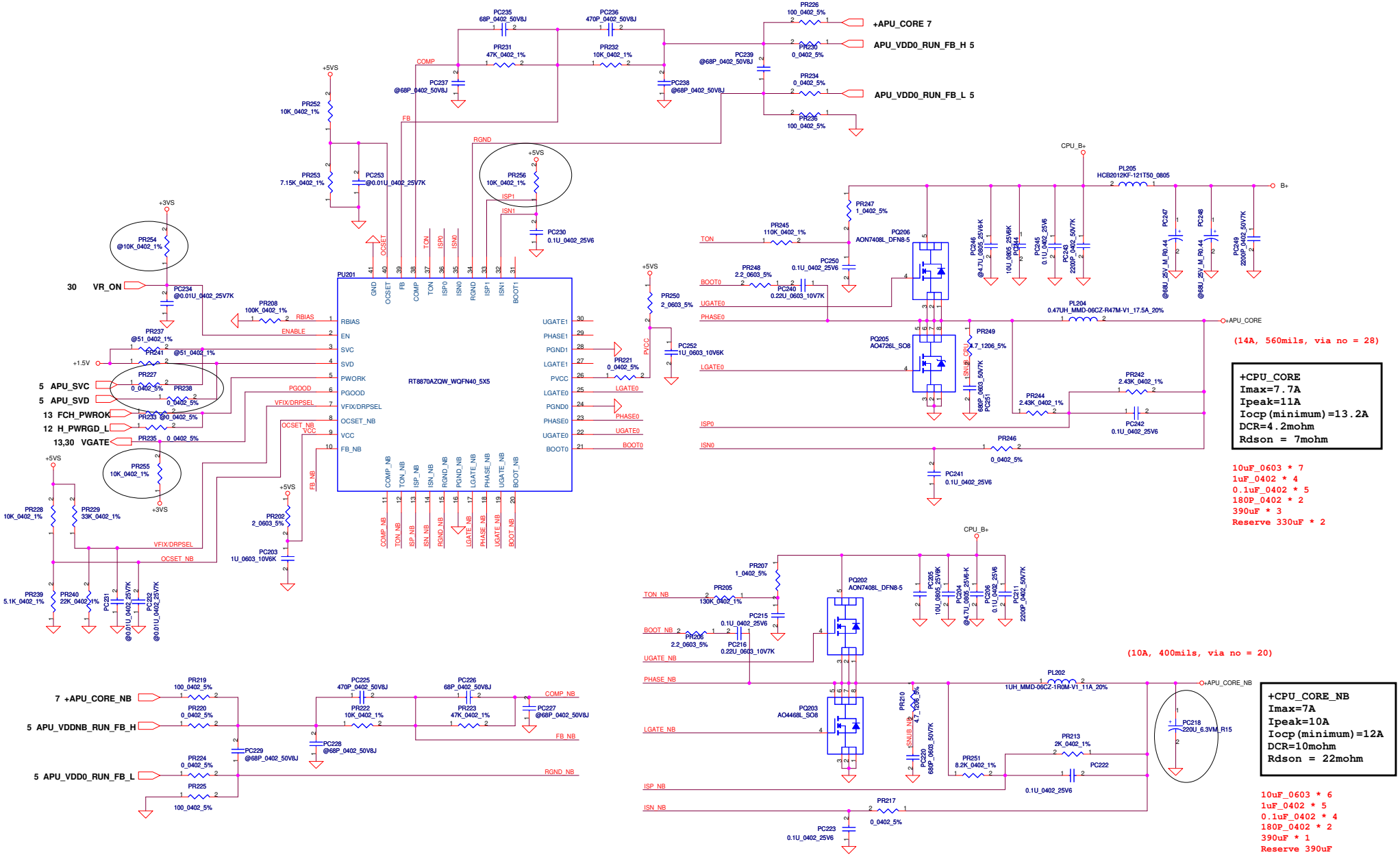
Size | Document Number: LAXXXX | Rev: 0.22

Date: Wednesday, February 16, 2011 | Sheet 41 of 44



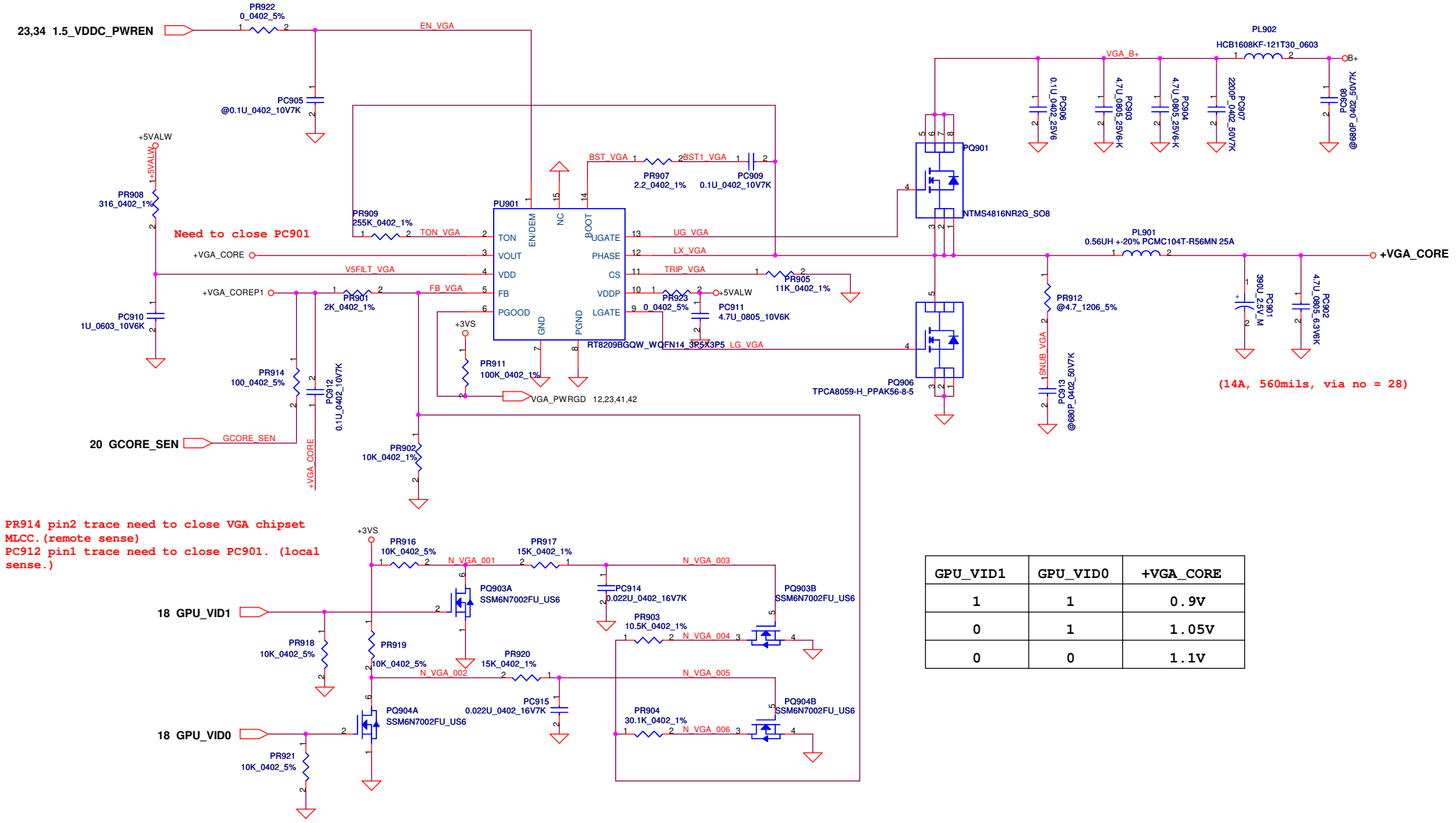
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	+1.8VSP		
Size	Document Number	NCL61 LA-6321P M/B	Rev 0.22
Date: Tuesday, February 15, 2011	Sheet 42 of 44		



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PWR-CPU_CORE		
Size C	Document Number LAXXXX		Rev 0.22
Date: Wednesday, February 16, 2011	Sheet 43 of 44		

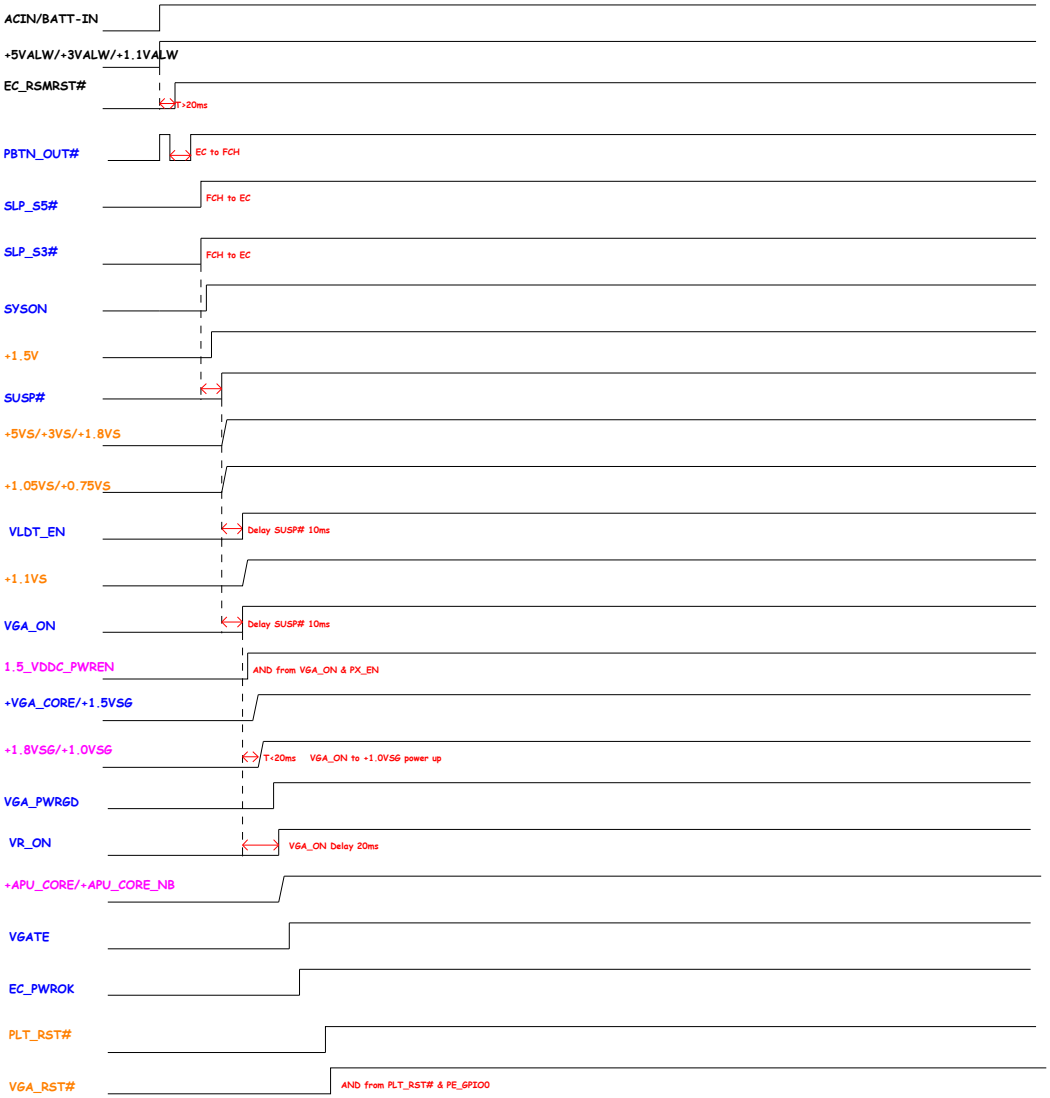


GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: VGA_CORE			
Size	Document Number: LAXXXX		Rev: 0.22
Date: Friday, February 18, 2011		Sheet 44 of 44	

POWER SEQUENCE



Security Classification	Compal Secret Data		
Issued Date	2010/11/05	Deciphered Date	2011/12/31

Title	Power Sequence		
Size	Document Number	LA-6691P	Rev 3.0A
Date	Tuesday, February 15, 2011	Sheet	45 of 48

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P30	KB930	2010/12/16	COMPAL	Power button no function.	Add R1621 pull up to +3VALW.	0.12
2	P31	TP button	2010/12/16	COMPAL	SW5,SW6 footprint error	Modify SW5,SW6 symbol.	0.12
3	P33	Fan Connector	2010/12/16	COMPAL	Fan no function.	Modify Fan connector pin define.	0.12
4	P35 ~ P44	Power schematic update	2010/12/16	COMPAL		Power schematic update	0.12
5	P30	KB930	2010/12/17	COMPAL	Modify board ID for ER phase.	Change R1606 from 0 ohm to 8.2K ohm.	0.12
6	P5	FCH THERMTRIP	2010/12/17	COMPAL	Modify BOM structure of thermtrip circuit. For FCH spec.	Change Q79 and R424 to unpop and change R427 to pop.	0.12
7							
8	P30	KB930	2010/12/17	COMPAL	Vendor's recommend for XCLK0 signal.	Add R1669 and C129.	0.12
9	P14	FCH SPI	2010/12/21	COMPAL	Add U11 circuit for flash BIOS crisis circuit.	Add U11 circuit.	0.12
10	P8	DDR3 SO-DIMM1	2010/12/21	COMPAL	Reserve R155,R152 for DDR3 DIMM1. (SA)		0.12
11	P33	Screw hole	2010/12/22	COMPAL	Thermal issue, modify H22.	Modify H22 to 7.0.	0.13
12	P35 ~ P44	Power schematic update	2010/12/22	COMPAL		Power schematic update	0.13
13	P12	FCH RTC	2010/12/23	COMPAL	Customer requirement for clear CMOS	Change R865 to Jump.	0.13
14	P28	WLAN & LED	2010/12/23	COMPAL	For ESD solution on LED.	Add C1644~C1648.	0.13
15	P26	Audio Codec	2010/12/24	COMPAL	For EMI solution on DMIC CLK.	Change R1544 to L124.	0.13
16	P30	KB930	2010/12/24	COMPAL	For EMI solution on SPI CLK.	Change R1631 to L125 and pop R180 and C1535.	0.13
17	P14	FCH SPI	2010/12/24	COMPAL		Modify Crisis circuit.	0.13
18	P10	CRT	2010/12/24	COMPAL	For ESD solution on CRT.	Pop D1,D2,D16,D18	0.13
19	P35 ~ P44	Power schematic update	2010/12/24	COMPAL		Power schematic update	0.13
20	P25	LAN	2010/12/24	COMPAL		Reserve J1 jump for LAN power.	0.13
21	P14	FCH SPI	2010/12/25	COMPAL	For EMI requirement.	Reserve R181,C130 close to U32.	0.13
22	P25	LAN	2010/12/27	COMPAL	For LAN power discharge.	Add R1113,Q62.	0.13
23	P25	LAN	2010/12/27	COMPAL	Prevent LAN wake up signal fo floating.	Add R553 pull down to GND.	0.13
24	P25	LAN	2010/12/27	COMPAL	For ESD requirement.	Change R549,R1529,R1530,R552 to 0603 size.	0.13
25	P34	DC to DC	2010/12/27	COMPAL	For Power sequence.	Change R1103 from 100K to 47K.	0.13
26	P11	HDMI	2010/12/28	COMPAL	For EMI requirement.	Modify L11~L14 circuit and remove un-LS circuit.	0.13
27	P12,18,25	Crystal	2010/12/29	COMPAL	For Vendor recommend.	Modify C35,C66,C67,C1633,C1634.	0.2
28	P26	Audio Codec	2010/12/30	COMPAL	For EMI Requirement.	Unpop R1556,R1557,R1558,R1559.	0.2
29	P30	KB930	2010/12/31	COMPAL	Change ROM footprint.	Change U48 footprint.	0.2
30	P16	FCH Strap	2010/12/31	COMPAL	Change FCH Strap for SPI-ROM	Pop R594,R602; Unpop R601,R550.	0.2
31	P18	Seymour Strap	2011/01/10	COMPAL	For AMD requirement.	Unpop R21,R22.	0.21
32	P34	DC to DC	2011/01/11	COMPAL	For +1.8VS discharge issue.	Add Q81,R1138.	0.21
33	P13	FCH HDA/USB/ACPI	2011/02/11	COMPAL	For RSMRST pluse issue	Change R606 from 2.2k ohm to 150 ohm	0.22
34	P30	EC	2011/02/11	COMPAL	For MB Board ID	Change R1606 to 18K	0.22
35	P10	CRT	2011/02/11	COMPAL	For CRT EA AND EMI	Change L116, L117, L118 TO 80 ohm	0.22
36	P25	LAN	2011/02/11	COMPAL	For EMI request	Change D36, D37, D38, D39 footprint	0.22
37	P18	VGA	2011/02/15	COMPAL	For S3 can't resume issue	ADD R74 (1M ohm) on Y1's cap	0.22
38	P25	LAN	2011/02/15	COMPAL	Follow vendor recommand to change Crystal's cap value	Change C1633 to 15P, C1634 to 12P	0.22
39	P30	EC	2011/02/16	COMPAL	For EMI requirement	Change R180 to 39 ohm, C1535 to 33P	0.23
40	P25	LAN	2011/02/16	COMPAL	For EMI requirement	Change TS1 to IH-160	0.23
41	P26	AUDIO	2011/02/17	COMPAL	For EMI requirement	Change R1556, R1557, R1558, R1559 to 0.1u caps	0.23
42	P34	DC-DC	2011/02/17	COMPAL	For EMI requirement	ADD C1505, C1523 on +5VALW	0.23
43	P32	USB	2011/02/17	COMPAL	For EMI requirement	ADD C1506 on +USB_VCCB	0.23
44	P33	PWRBTN	2011/02/17	COMPAL	For EMI requirement	ADD C1603 on ON/OFFBTN#	0.23
45	P25	LAN	2011/02/18	COMPAL	For EMI requirement	Stuff R546, R548	0.23
46							
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Compal Electronics, Inc.
Title: EE-PIR-1
Size: Custom | Document Number: LA-6211P | Rev: 0.22
Date: Wednesday, February 23, 2011 | Sheet 48 of 48