

Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2011-04-25

Rev: 1.0

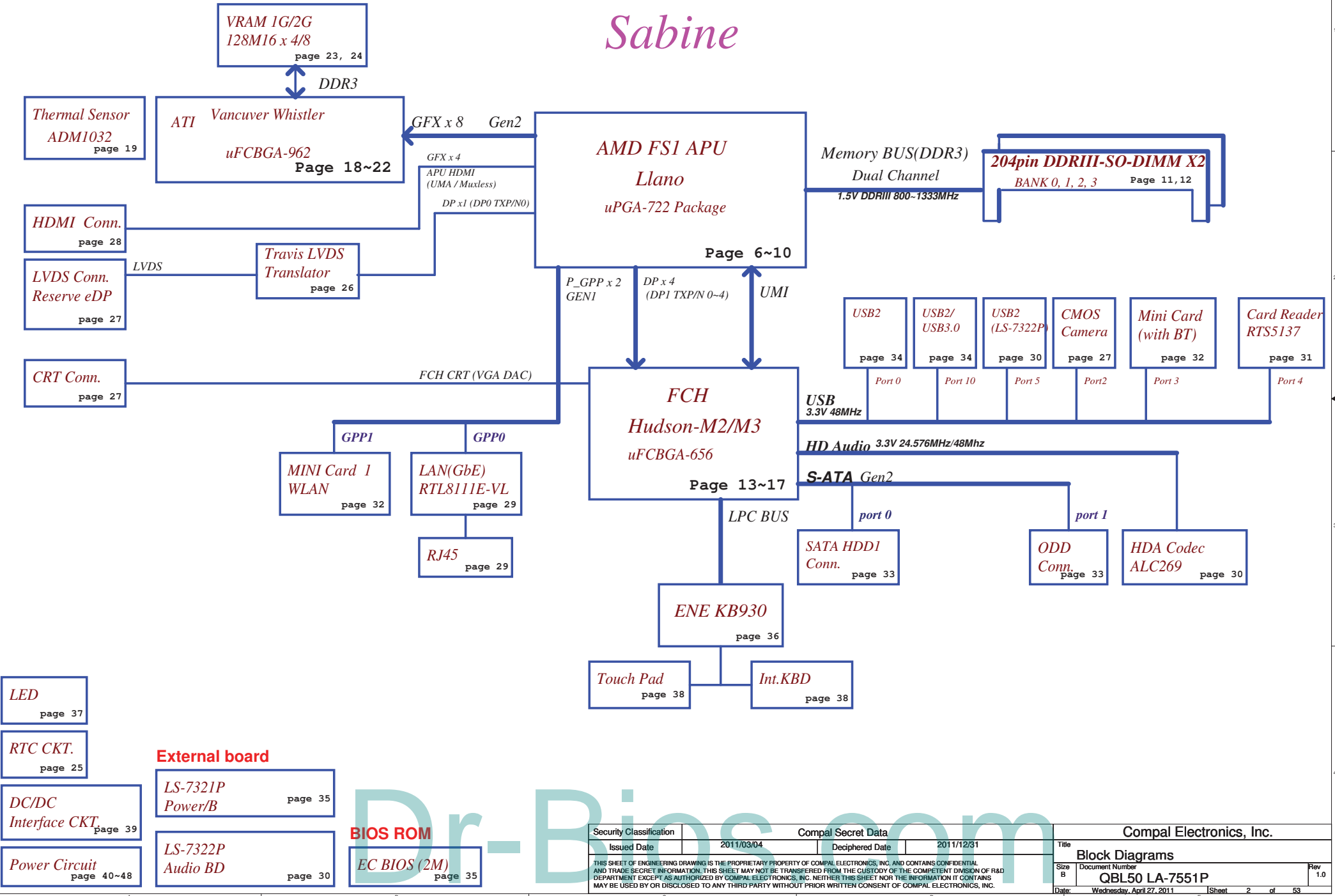
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Issued Date	2011/03/04	Compal Electronics, Inc.		
Deciphered Date	2011/12/31	Cover Page		
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Model Name : QBL50

Sabine



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RTC CKT.
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DC/DC
Interface CKT.
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Power Circuit
page 40~48

External board
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Power/B
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LS-7322P
Audio BD
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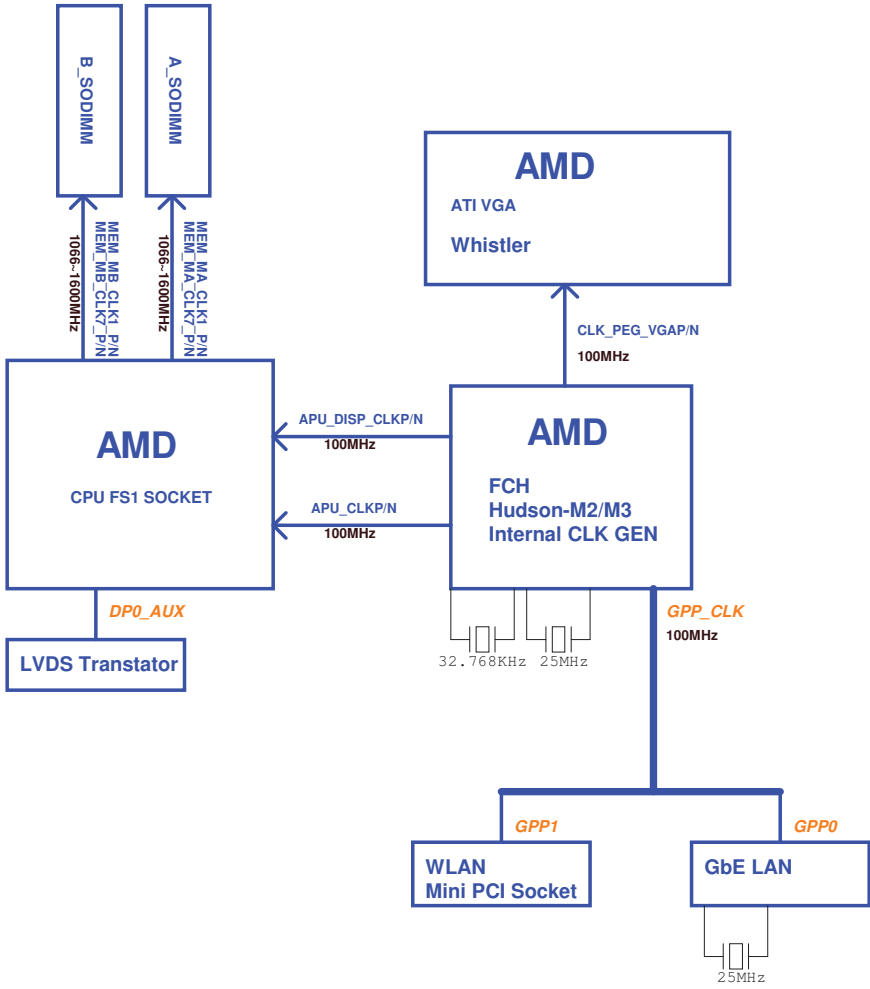
BIOS ROM
EC BIOS (2M)
page 35

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Issued Date		Deciphered Date	

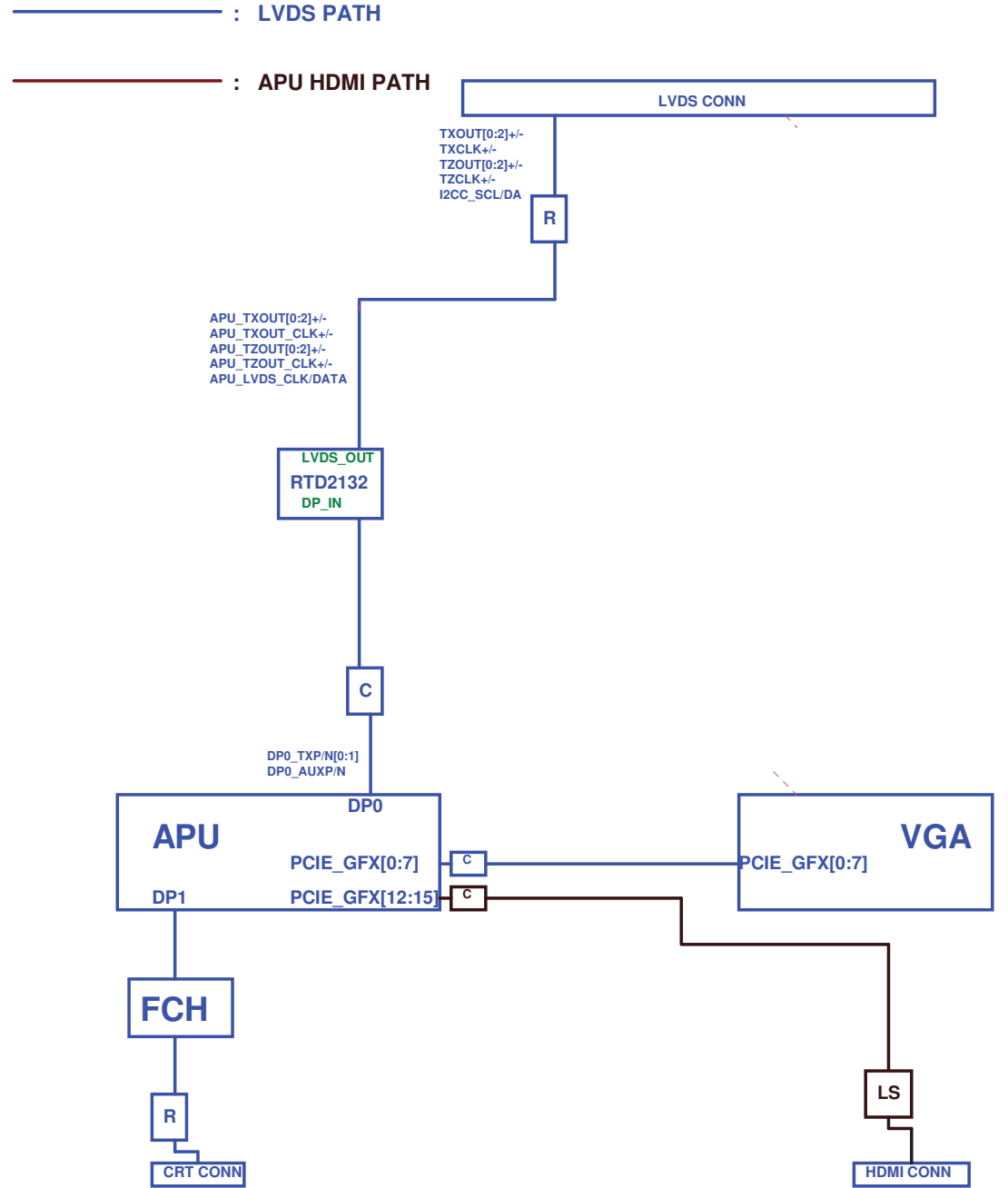
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Title Block Diagrams			
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CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B



BOM Config

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

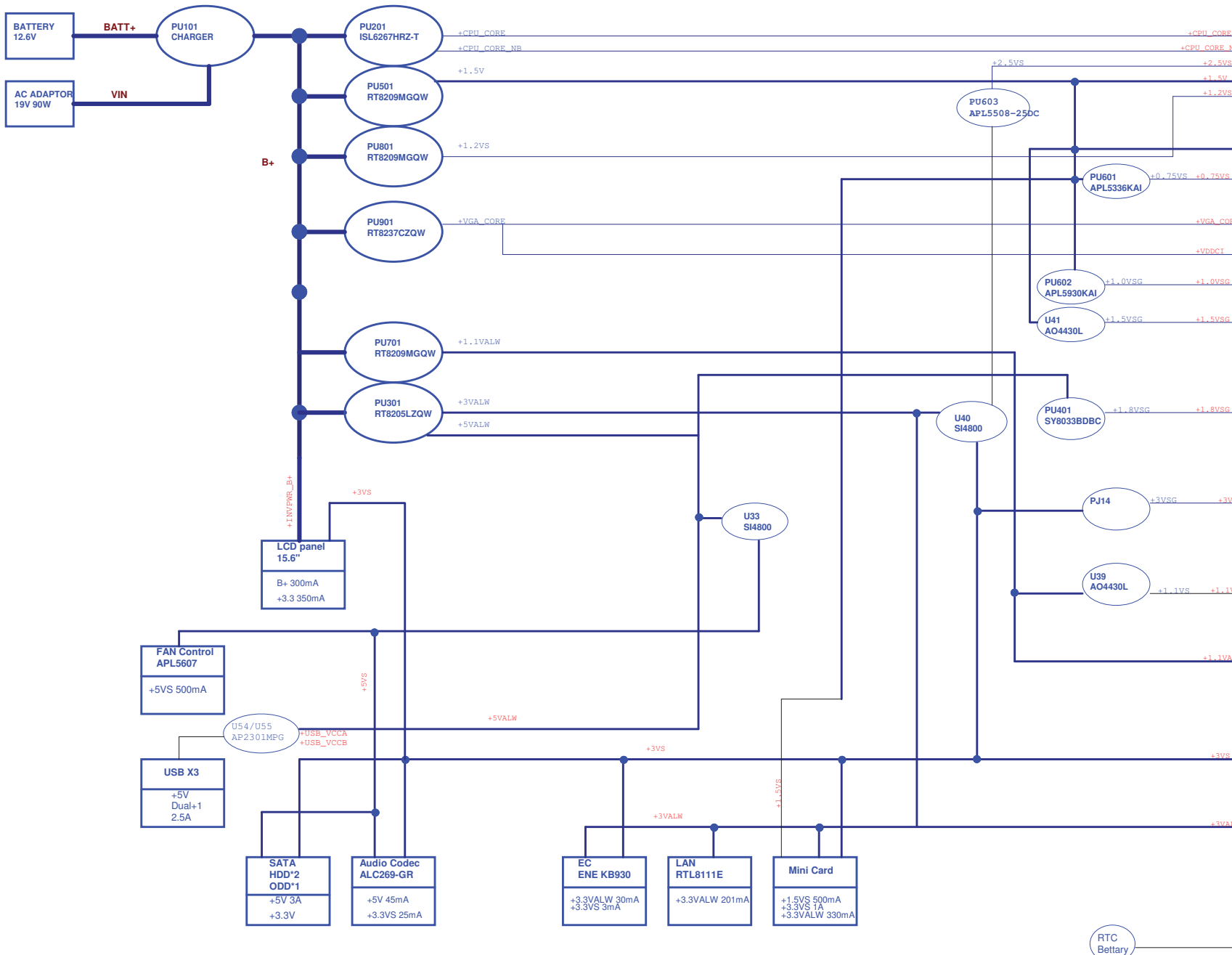
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA) (APU)	1001 101X b	9AH
			RTD2132S (TL)		

FCH SM Bus 0 address

FCH SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

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AMD APU FS1	
0.7~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A

RAM DDRIII SODIMM X2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A





VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCI_E_VDDC: 2000 mA DP[A]E_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1D1: 100 mA VDD2D1: 50 mA A2VDDC: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCI_E_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCI_E_VDDR: 400 mA DP[A]F_VDD18: 920 mA DP[A]F_PVDD: 120 mA
+3VSG	A2VDD: 130 mA VDDR3: 60 mA





VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIE: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDAN_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G



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18 PCIE_GTX_C_FRX_P0[0..7]  
 18 PCIE_GTX_C_FRX_N0[0..7]  

PCIE_FTX_C_GRX_P[0..7] 18  
 PCIE_FTX_C_GRX_N[0..7] 18  

APU To HDMI

 PCIE_FTX_GRX_P[12..15] 28
 PCIE_FTX_GRX_N[12..15] 28

JCPU1A		CONN@	
PCI EXPRESS			
PCIE_GTX_C_FRX_P0 AA8	P_GFX_RXP0	P_GFX_TXP0	AA2 PCIE_FTX_GRX_P0 C917VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0 AA9	P_GFX_RXN0	P_GFX_TXN0	AA3 PCIE_FTX_GRX_N0 C918VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1 Y7	P_GFX_RXP1	P_GFX_TXP1	Y2 PCIE_FTX_GRX_P1 C919VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1 Y8	P_GFX_RXN1	P_GFX_TXN1	Y1 PCIE_FTX_GRX_N1 C920VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2 W5	P_GFX_RXP2	P_GFX_TXP2	Y4 PCIE_FTX_GRX_P2 C921VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2 W6	P_GFX_RXN2	P_GFX_TXN2	Y5 PCIE_FTX_GRX_N2 C922VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3 W8	P_GFX_RXP3	P_GFX_TXP3	W2 PCIE_FTX_GRX_P3 C923VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3 W9	P_GFX_RXN3	P_GFX_TXN3	W3 PCIE_FTX_GRX_N3 C924VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4 V7	P_GFX_RXP4	P_GFX_TXP4	V2 PCIE_FTX_GRX_P4 C925VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4 V8	P_GFX_RXN4	P_GFX_TXN4	V1 PCIE_FTX_GRX_N4 C926VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5 U5	P_GFX_RXP5	P_GFX_TXP5	V4 PCIE_FTX_GRX_P5 C927VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5 U6	P_GFX_RXN5	P_GFX_TXN5	V5 PCIE_FTX_GRX_N5 C928VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6 U8	P_GFX_RXP6	P_GFX_TXP6	U2 PCIE_FTX_GRX_P6 C929VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P6
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PCIE_GTX_C_FRX_N7 T8	P_GFX_RXN7	P_GFX_TXN7	T1 PCIE_FTX_GRX_N7 C932VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N7
X B5	P_GFX_RXP8	P_GFX_TXP8	T4 X
X B6	P_GFX_RXN8	P_GFX_TXN8	T5 X
X B8	P_GFX_RXP9	P_GFX_TXP9	B2 X
X B9	P_GFX_RXN9	P_GFX_TXN9	R3 X
X P7	P_GFX_RXP10	P_GFX_TXP10	P2 X
X P8	P_GFX_RXN10	P_GFX_TXN10	P1 X
X N5	P_GFX_RXP11	P_GFX_TXP11	P4 X
X N6	P_GFX_RXN11	P_GFX_TXN11	P5 X
N8	P_GFX_RXP12	P_GFX_TXP12	N2 PCIE_FTX_GRX_P12
N9	P_GFX_RXN12	P_GFX_TXN12	N3 PCIE_FTX_GRX_N12
M7	P_GFX_RXP13	P_GFX_TXP13	M2 PCIE_FTX_GRX_P13
M8	P_GFX_RXN13	P_GFX_TXN13	M1 PCIE_FTX_GRX_N13
L5	P_GFX_RXP14	P_GFX_TXP14	M4 PCIE_FTX_GRX_P14
L6	P_GFX_RXN14	P_GFX_TXN14	M5 PCIE_FTX_GRX_N14
L8	P_GFX_RXP15	P_GFX_TXP15	L2 PCIE_FTX_GRX_P15
L9	P_GFX_RXN15	P_GFX_TXN15	L3 PCIE_FTX_GRX_N15

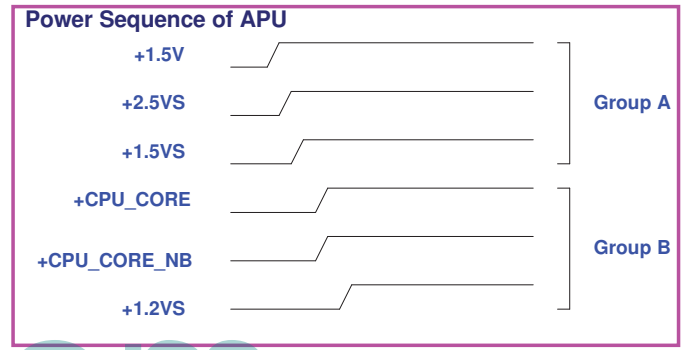
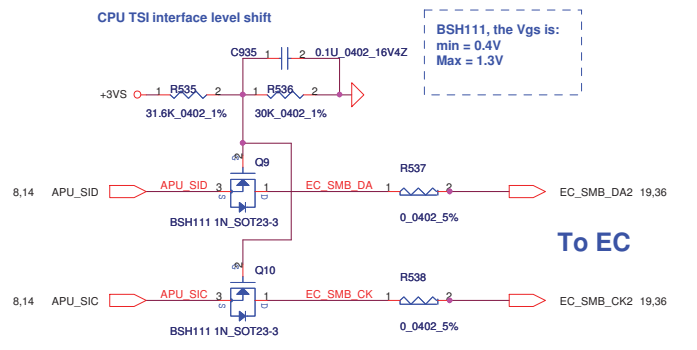
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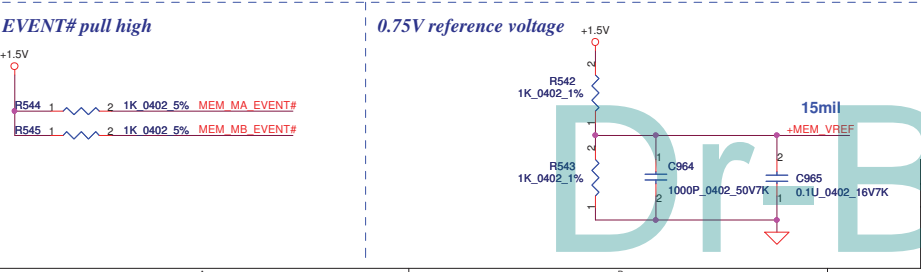
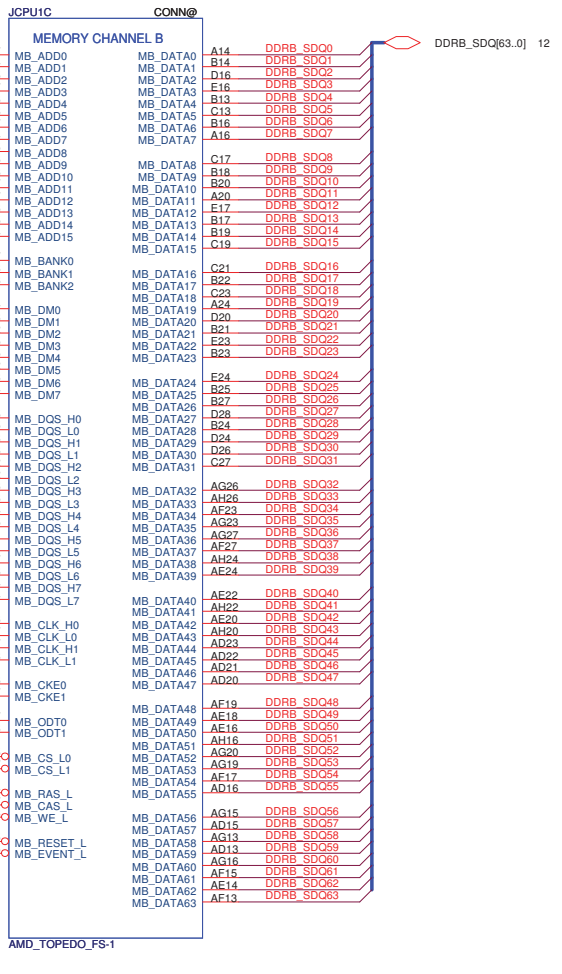
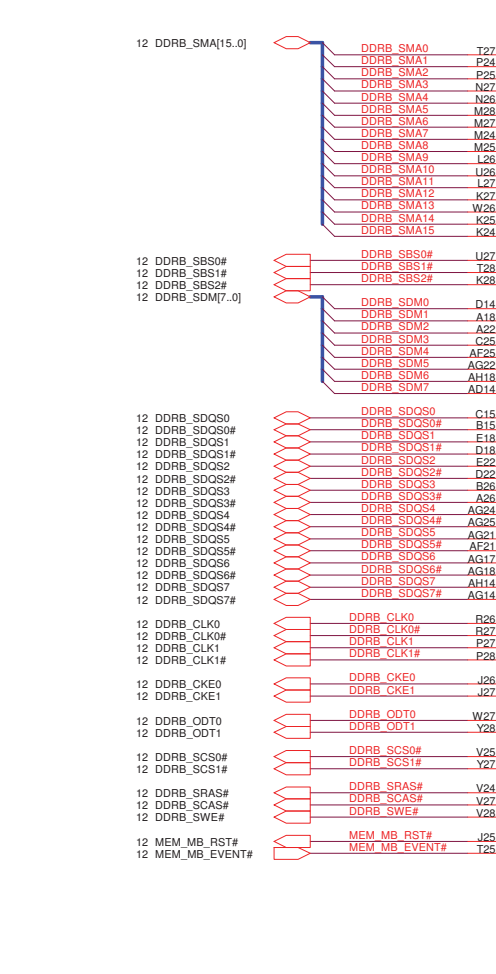
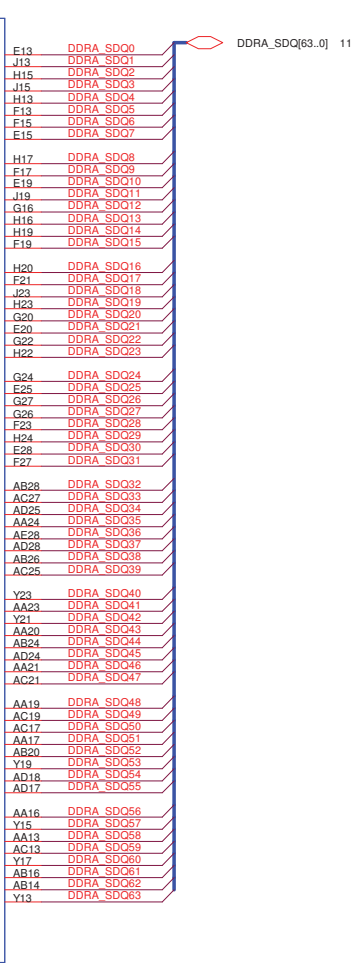
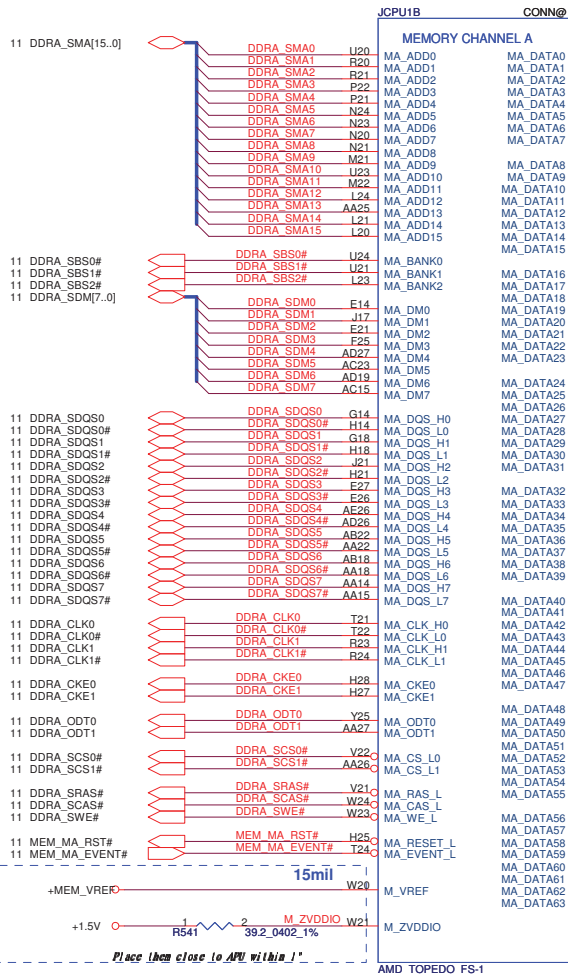
2
1
0
To HDMI
CK

GPP		GLAN		WLAN	
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29 PCIE_DTX_C_FRX_N0 AC6	P_GPP_RXN0	P_GPP_TXN0	AD5 PCIE_FTX_DRX_N0 C951 1 2 0.1U_0402_16V7K PCIE_FTX_C_DRX_N0 29		
32 PCIE_DTX_C_FRX_P1 AC8	P_GPP_RXP1	P_GPP_TXP1	AC2 PCIE_FTX_DRX_P1 C952 1 2 0.1U_0402_16V7K PCIE_FTX_C_DRX_P1 32		
32 PCIE_DTX_C_FRX_N1 AC9	P_GPP_RXN1	P_GPP_TXN1	AC3 PCIE_FTX_DRX_N1 C953 1 2 0.1U_0402_16V7K PCIE_FTX_C_DRX_N1 32		
X AB7	P_GPP_RXP2	P_GPP_TXP2	AB2 X		
X AB8	P_GPP_RXN2	P_GPP_TXN2	AB1 X		
X AA5	P_GPP_RXP3	P_GPP_TXP3	AB4 X		
X AA6	P_GPP_RXN3	P_GPP_TXN3	AB5 X		

UMI - I/UR		UMI	
13 UMI_MTX_C_FRX_P0 AF8	P_UMI_RXP0	P_UMI_TXP0	AF1 UMI_FTX_MRX_P0 C956 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_P0 13
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13 UMI_MTX_C_FRX_P1 AE6	P_UMI_RXP1	P_UMI_TXP1	AF5 UMI_FTX_MRX_P1 C958 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_P1 13
13 UMI_MTX_C_FRX_N1 AE5	P_UMI_RXN1	P_UMI_TXN1	AF4 UMI_FTX_MRX_N1 C959 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_N1 13
13 UMI_MTX_C_FRX_P2 AE9	P_UMI_RXP2	P_UMI_TXP2	AE3 UMI_FTX_MRX_P2 C960 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_P2 13
13 UMI_MTX_C_FRX_N2 AE8	P_UMI_RXN2	P_UMI_TXN2	AE2 UMI_FTX_MRX_N2 C961 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_N2 13
13 UMI_MTX_C_FRX_P3 AD8	P_UMI_RXP3	P_UMI_TXP3	AD1 UMI_FTX_MRX_P3 C962 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_P3 13
13 UMI_MTX_C_FRX_N3 AD7	P_UMI_RXN3	P_UMI_TXN3	AD2 UMI_FTX_MRX_N3 C963 1 2 0.1U_0402_16V7K UMI_FTX_C_MRX_N3 13

+1.2VS   P_ZVDDP K5
 196_0402_1%
 P_ZVSS
 K4 P_ZVSS   R540 196_0402_1%





Security Classification	Compal Secret Data		Title	AMD FS1 DDRIII I/F	
Issued Date	2010/08/04	Deciphered Date	2011/12/31	Size	Document Number
				QBL50 LA-7551P	Rev 1.0
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To LVDS Translator

To FCH VGA ML

100MHz

100MHz_NSS

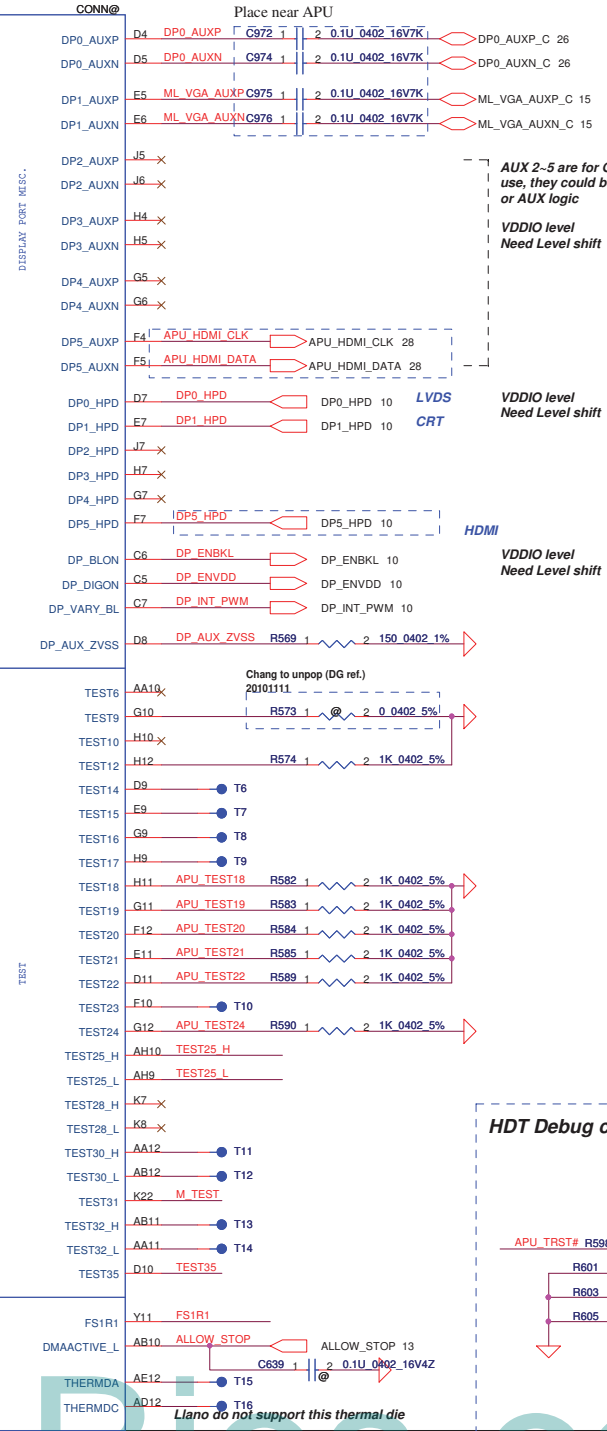
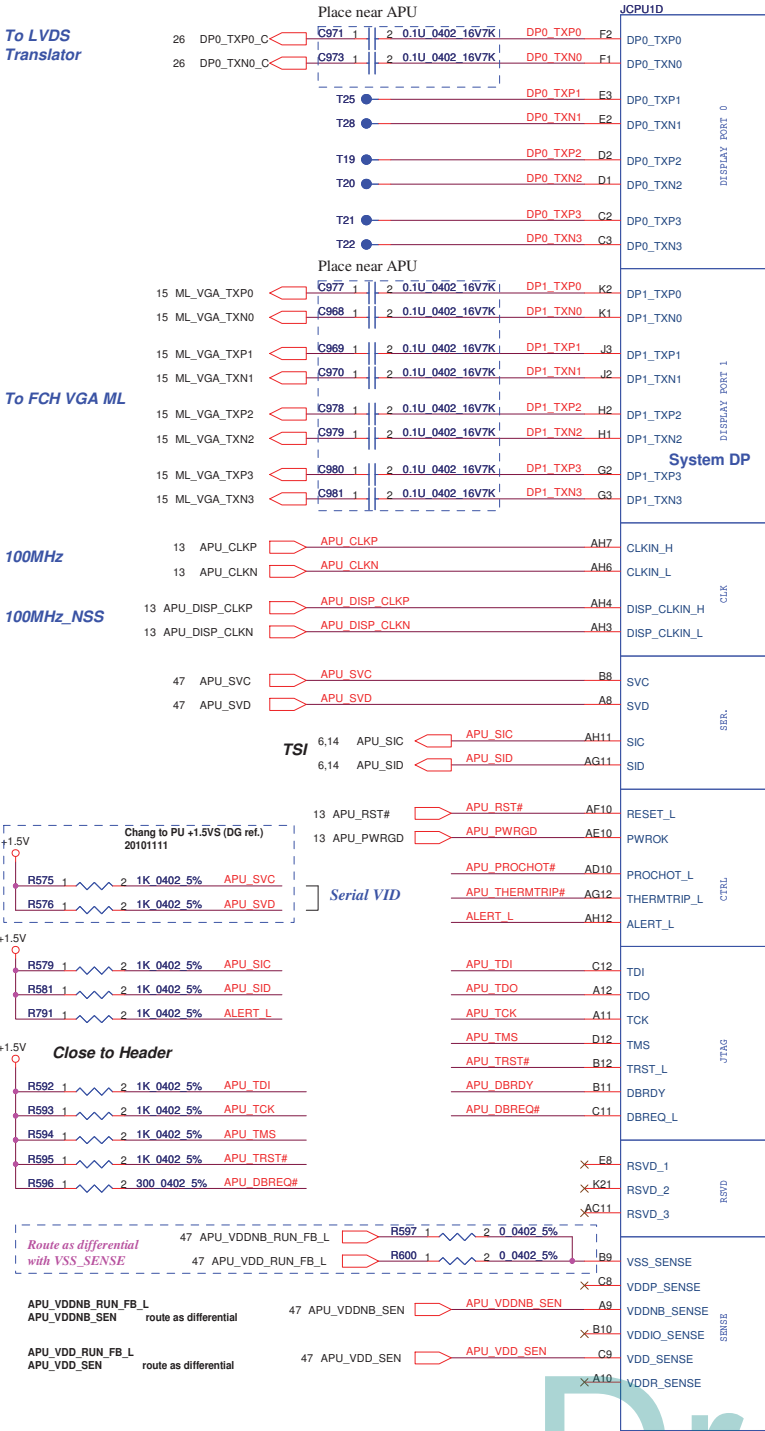
Serial VID

Close to Header

Route as differential with VSS_SENSE

APU_VDDNB_RUN_FB_L route as differential

APU_VDD_RUN_FB_L route as differential



To LVDS Translator

To FCH

AUX 2-5 are for GFX interface use, they could be selected to I2C or AUX logic

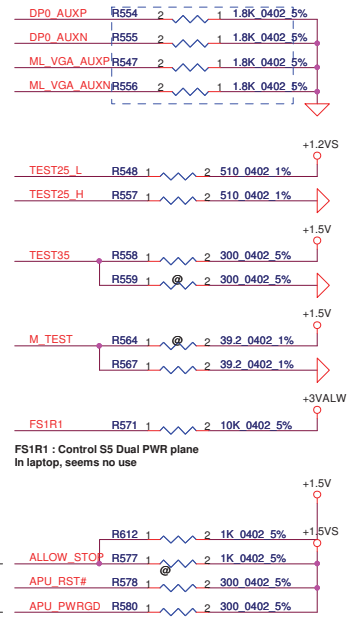
VDDIO level Need Level shift

VDDIO level Need Level shift

VDDIO level Need Level shift

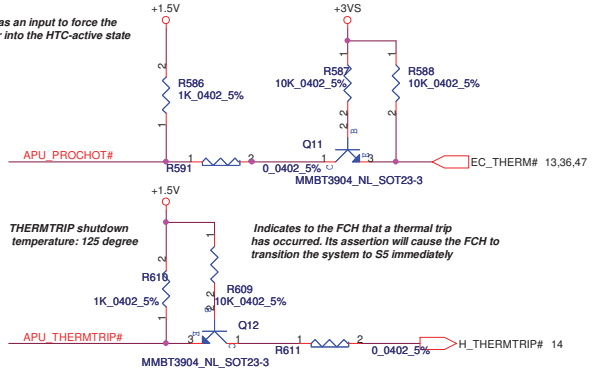
If not used, pins are left unconnected (DG ref.)

20101111

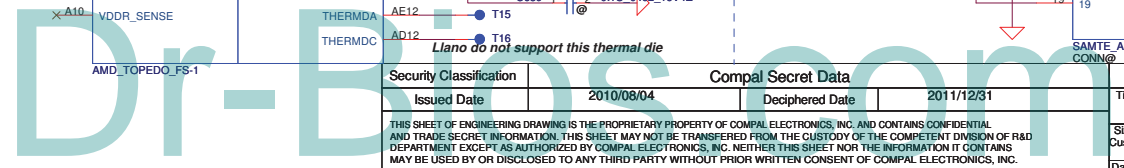
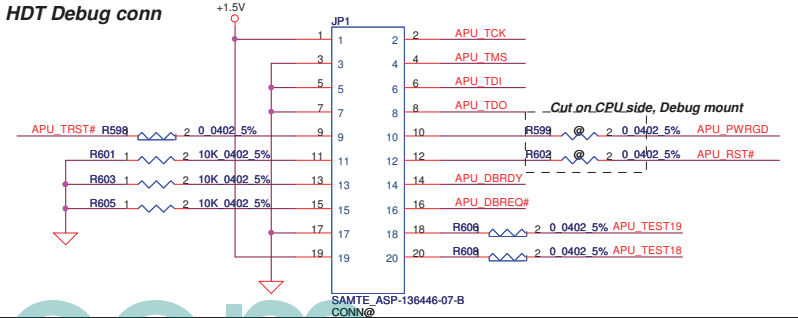


MISC

Asserted as an input to force the processor into the HTC-active state



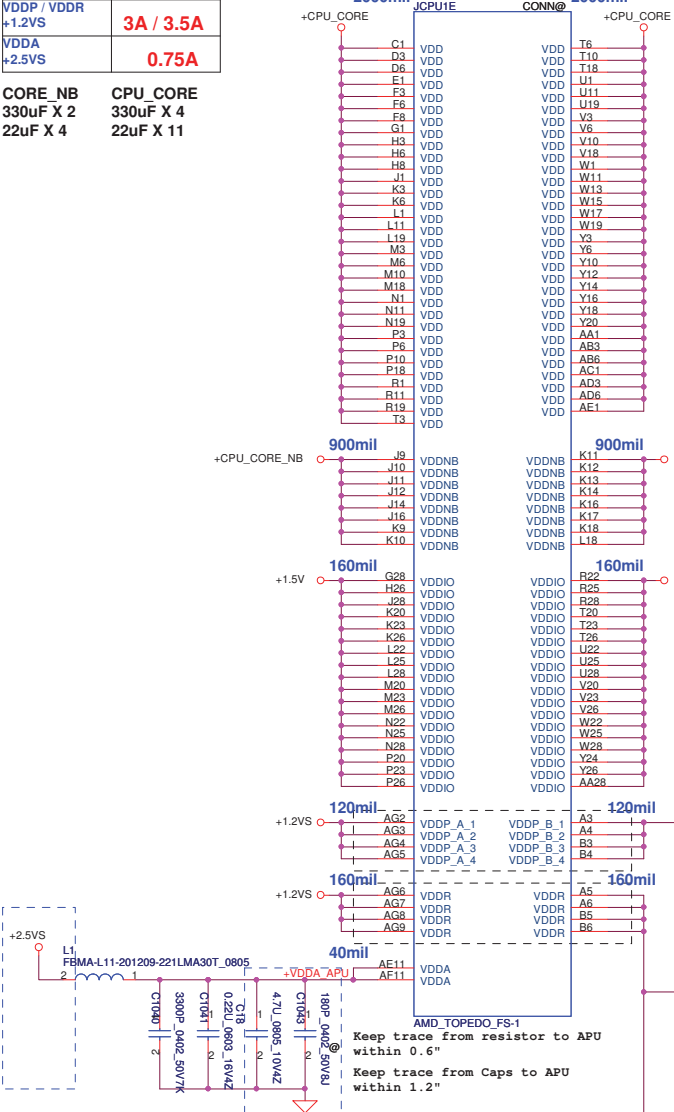
HDT Debug conn



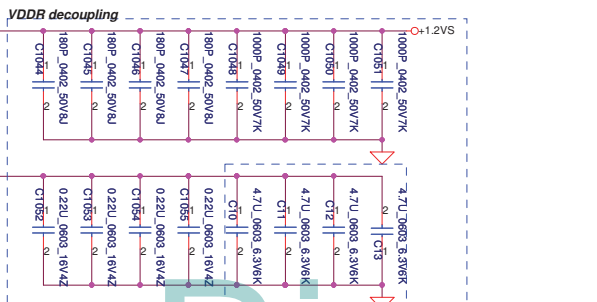
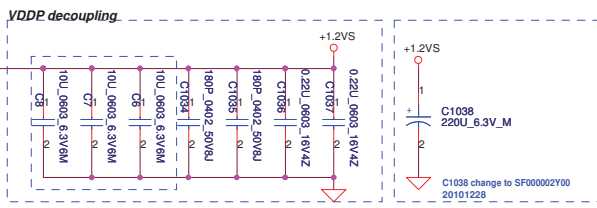
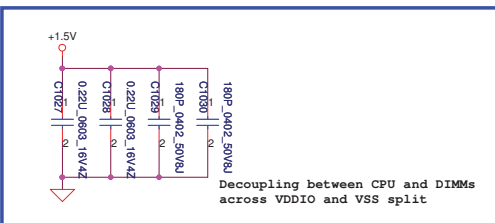
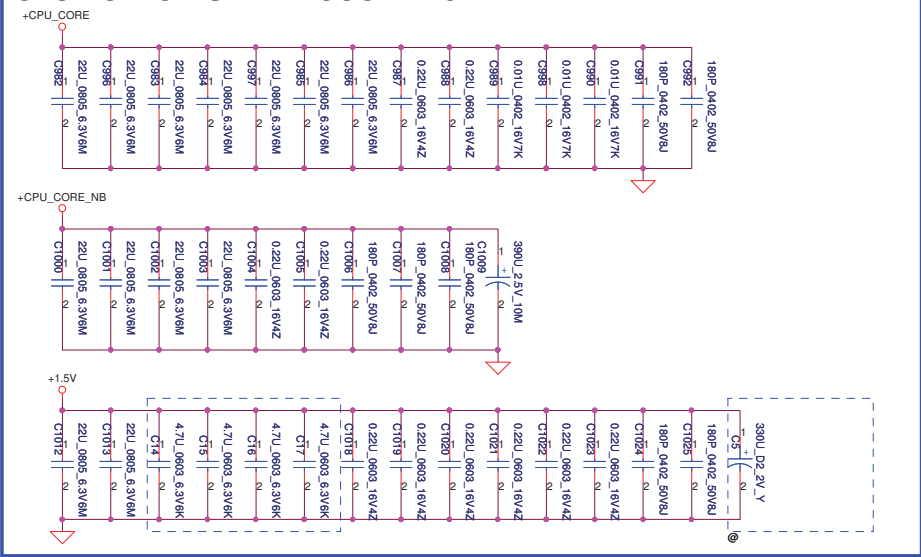
Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/04	Deciphered Date	2011/12/31	AMD FS1 Display / MISC / HDT	
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Size	Custom	Document Number	QBL50 LA-7551P		
Date	Wednesday, April 27, 2011	Sheet	8	of	53

Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB CPU_CORE
330uF X 2 330uF X 4
22uF X 4 22uF X 11



CPU BOTTOM SIDE DECOUPLING



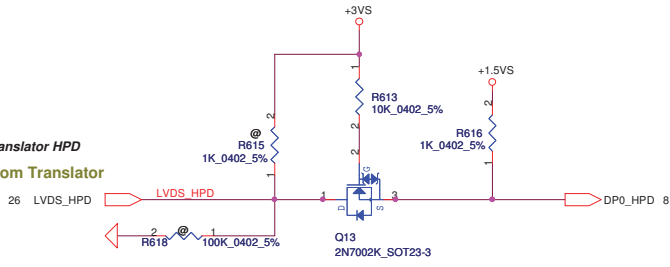
JCPU1F	CONN@
A7	T11
A13	T19
A15	L4
A17	L7
A19	L10
A21	L18
A23	V3
A25	V11
B7	V19
C4	W4
C10	W7
C14	W10
C16	W12
C18	W14
C20	W16
C22	W18
C24	Y9
C28	Y22
C28	Y22
D13	AA7
D15	AB9
D17	AB13
D19	AB15
D21	AB17
D23	AB19
D25	AB21
D27	AB23
E4	AB25
E10	AB27
E12	AC4
F5	AC7
F11	AC10
F14	AC12
F16	AC14
F18	AC16
F20	AC18
F22	AC20
F24	AC22
F26	AC24
F28	AC26
G4	AC28
G8	AD9
G12	AD11
G16	AD13
G17	AE7
G19	AE13
G21	AE15
G23	AE17
G25	AE19
J4	AE21
J8	AE23
J18	AE25
J20	AE27
J22	AF3
J24	AF6
K18	AF9
L4	AF12
L7	AF14
L10	AF16
M9	AF20
M11	AF22
M19	AF24
N4	AF24
N7	AF26
N10	AF28
N18	AG10
P9	AH5
P11	AH8
P19	AH13
R4	AH15
R7	AH17
R10	AH19
R16	AH21
T9	AH23
	AH25

AMD_TOPEDO_FS-1

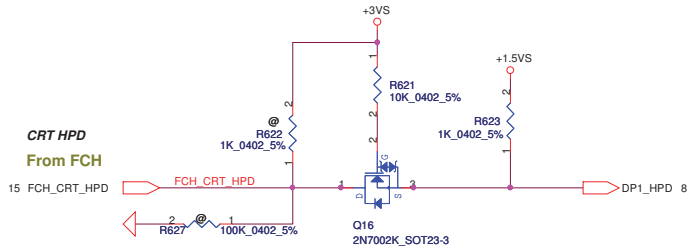
Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3				180pF x 4
10nF x 3		4.7uF x 4				
		0.22uF x 6				
		180pF x 4				

HPD

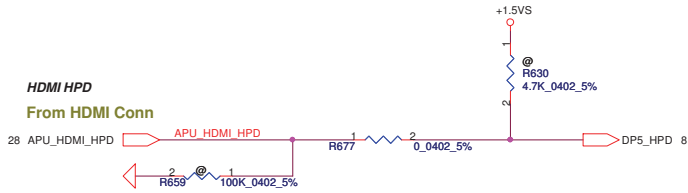
Translator HPD From Translator



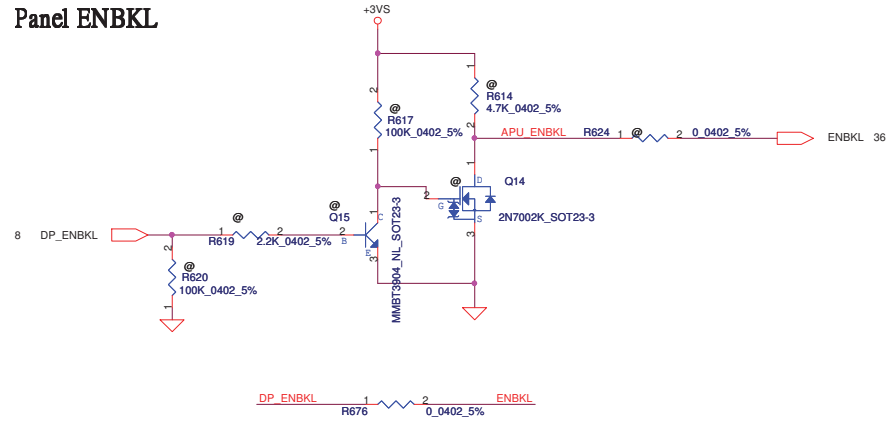
CRT HPD From FCH



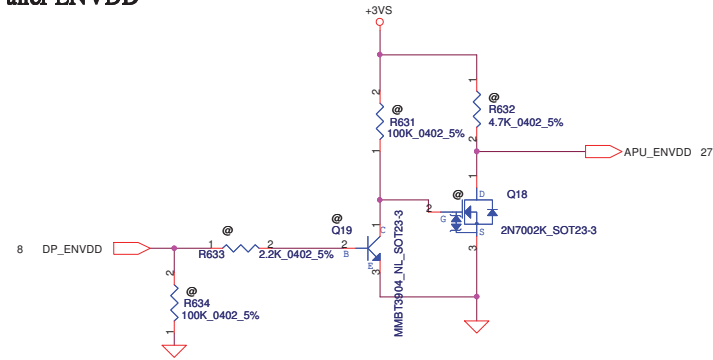
HDMI HPD From HDMI Conn



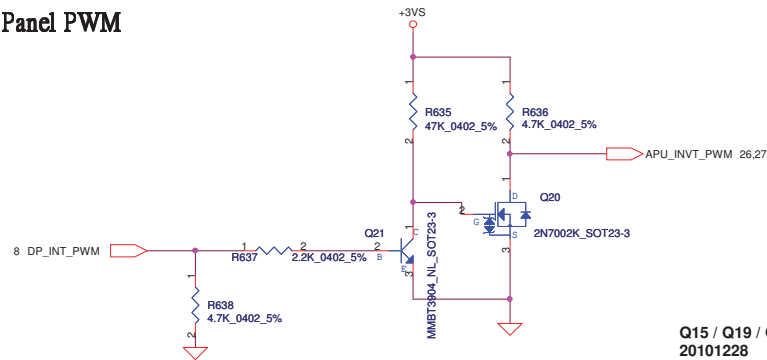
Panel ENBKL



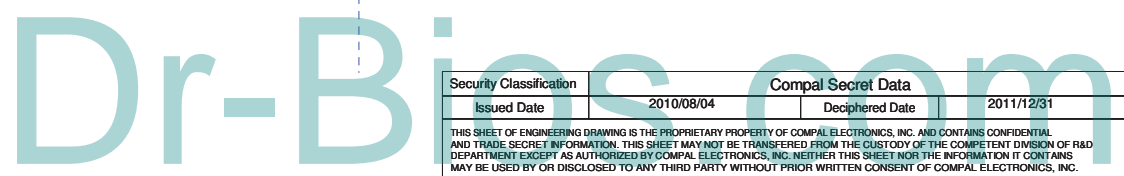
Panel ENVDD



Panel PWM

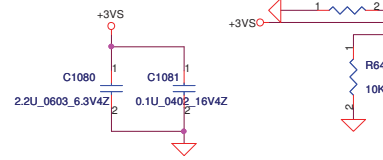
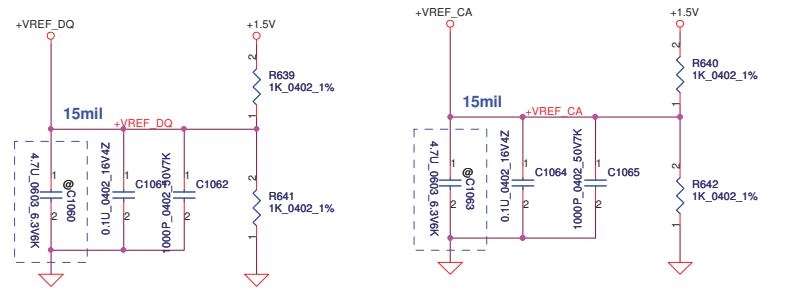
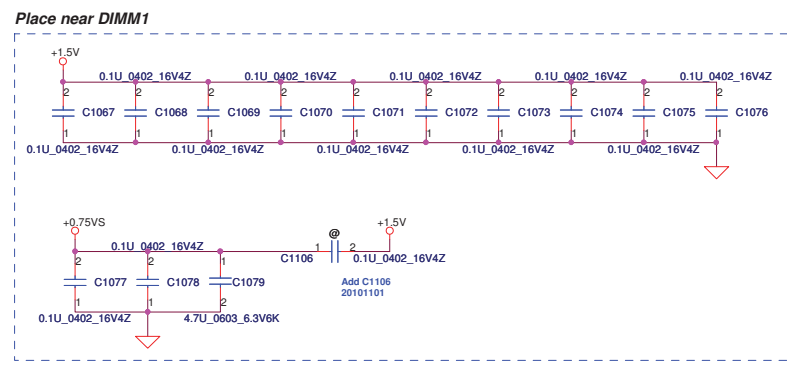
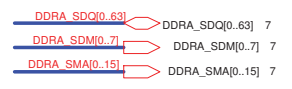
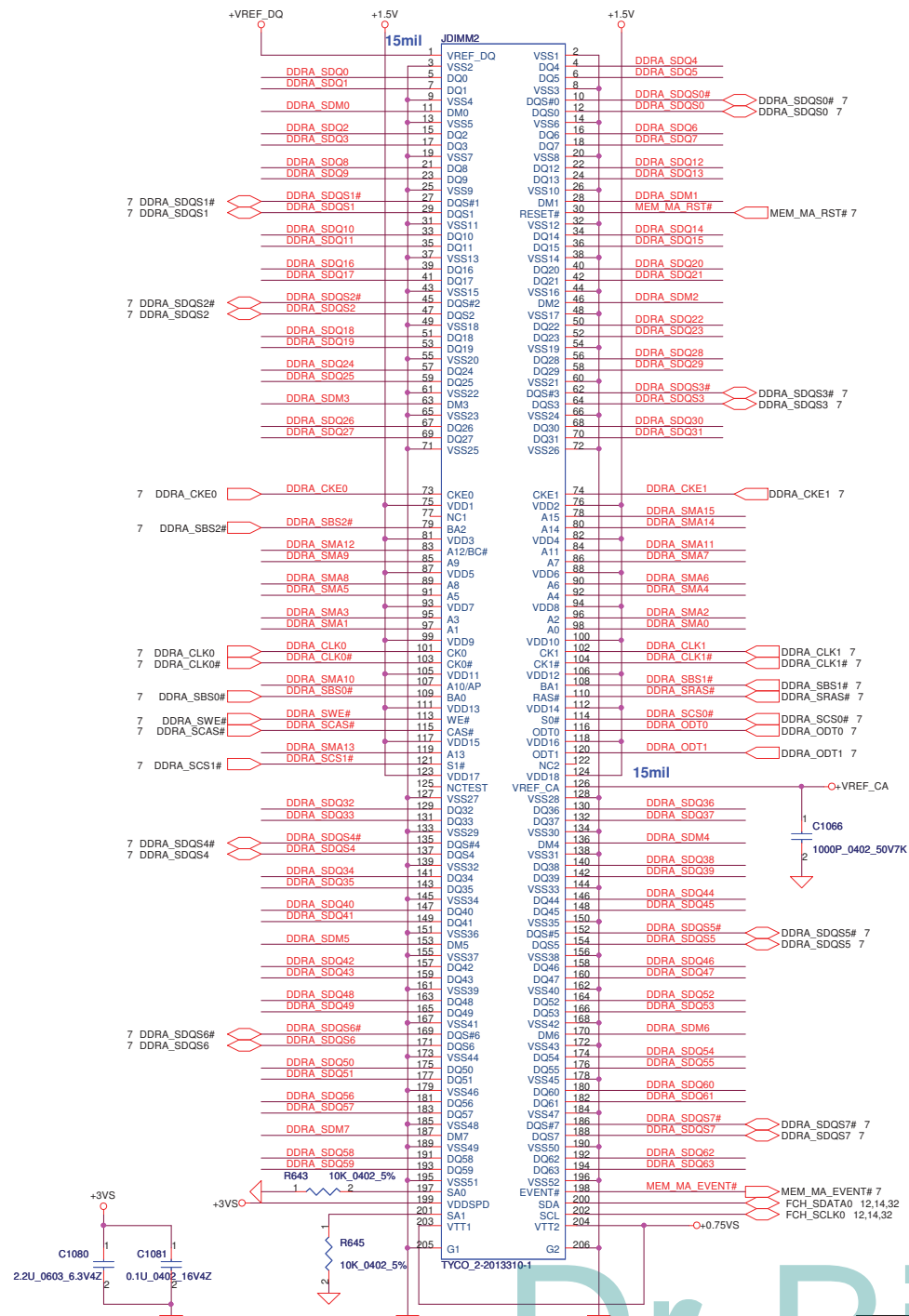


Q15 / Q19 / Q21 change to SB000006A00
20101228



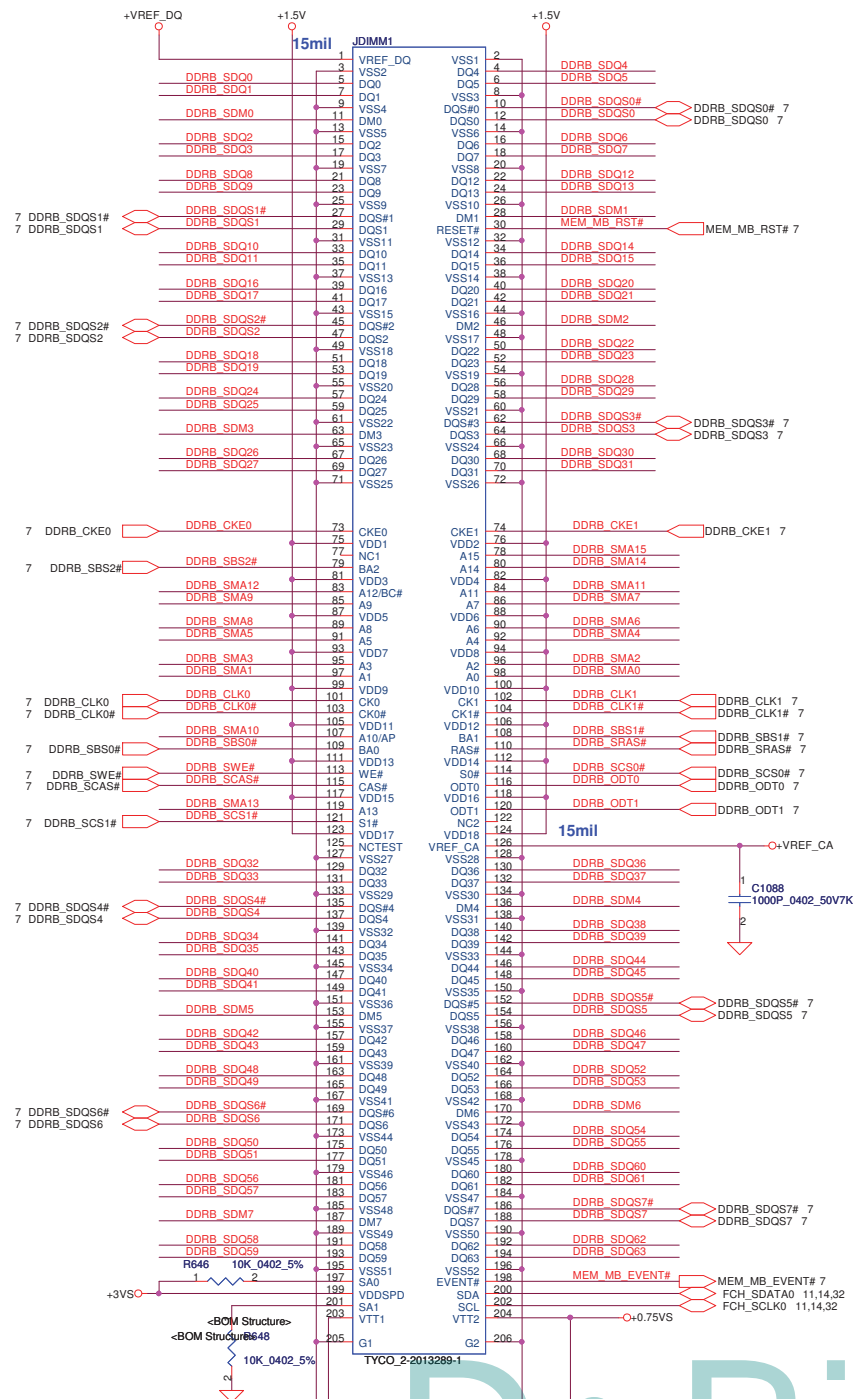
Security Classification	Compal Secret Data		Title	AMD FS1 Singal Level Shifter	
Issued Date	2010/08/04	Deciphered Date	2011/12/31	Size	Document Number
				Custom	QBL50 LA-7551P
				Date	Wednesday, April 27, 2011
				Sheet	10 of 53
				Rev	1.0

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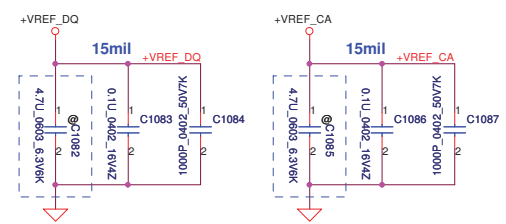
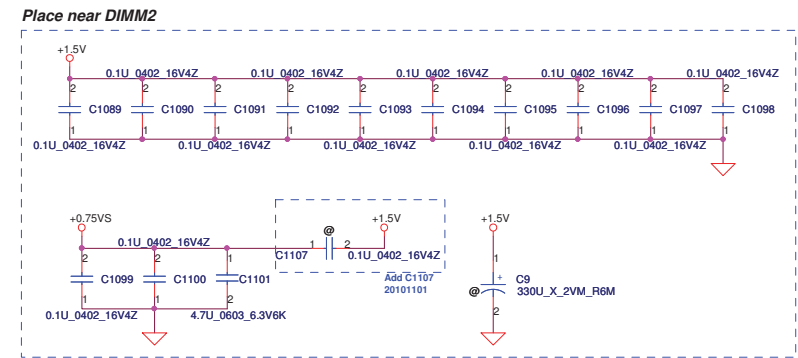


DIMM_A STD H:9.2mm
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/04	Deciphered Date	2011/12/31	Title	
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Size	Document Number	Date		Rev	1.0
Custom	QBL50 LA-7551P	Wednesday, April 27, 2011		Sheet	11 of 53



- DDRB_SDO[0..63] DDRB_SDO[0..63] 7
- DDRB_SDM[0..7] DDRB_SDM[0..7] 7
- DDRB_SMA[0..15] DDRB_SMA[0..15] 7

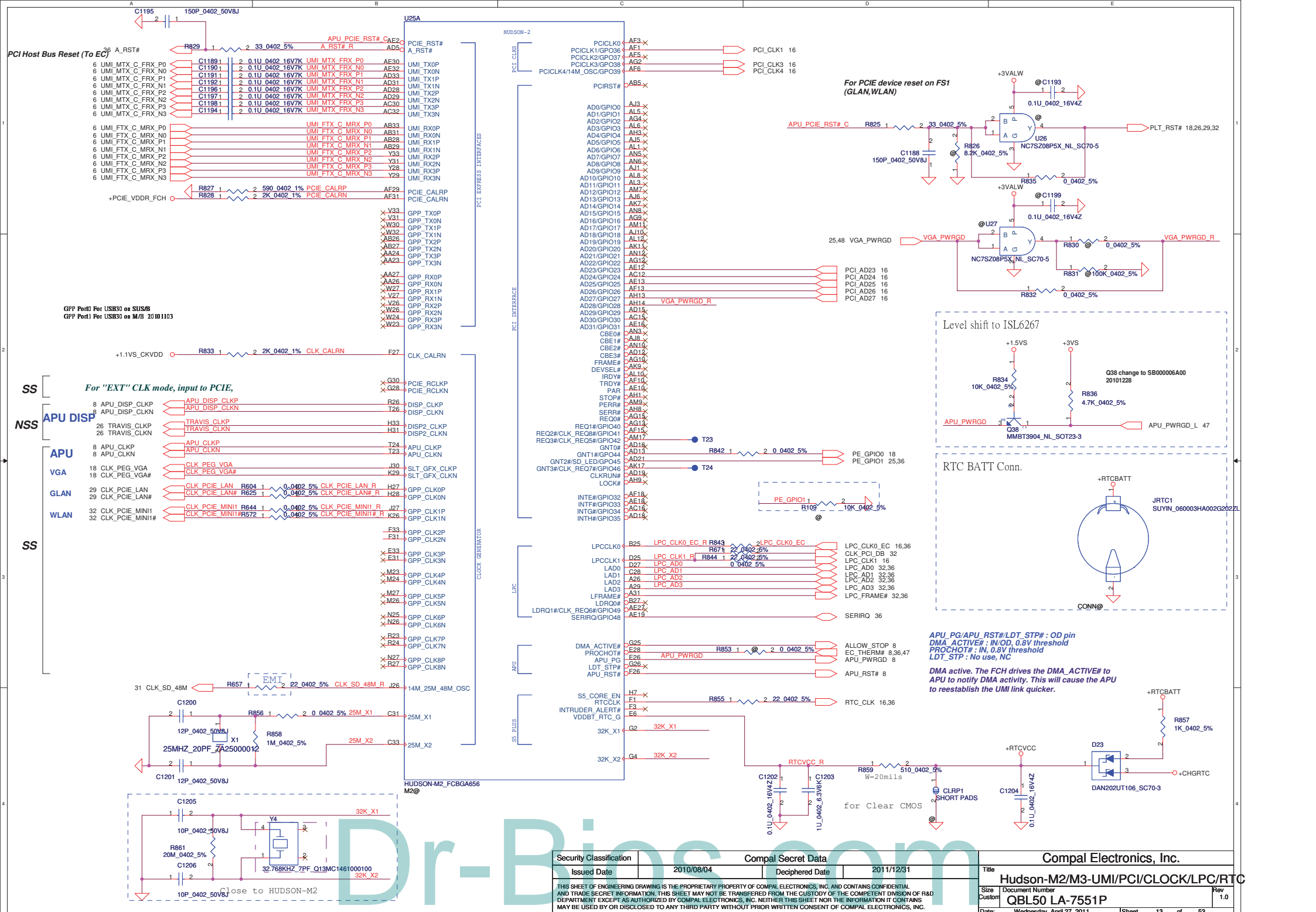


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Security Classification	Compal Secret Data	
Issued Date	2010/08/04	Deciphered Date
		2011/12/31

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Compal Electronics, Inc.		
Title		
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Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0
Date:	Wednesday, April 27, 2011	E Sheet 12 of 53

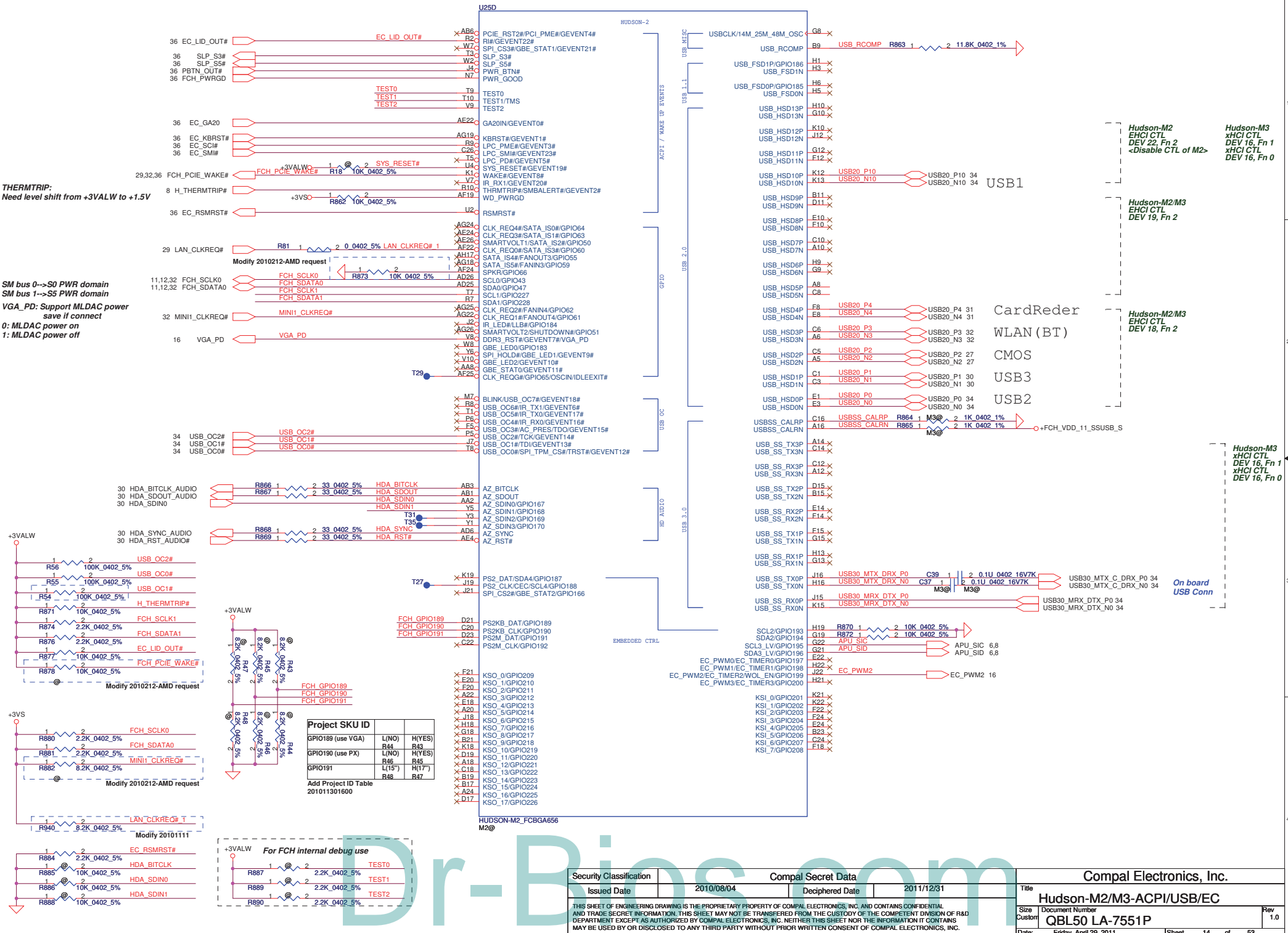


Security Classification	Compal Secret Data
Issued Date	2010/08/04
Deciphered Date	2011/12/31

Compal Electronics, Inc.	
Title	Hudson-M2/M3-UMI/PCI/Clock/LPC/RTC
Size	Document Number
Custom	QBL50 LA-7551P
Date	Wednesday, April 27, 2011
Sheet	13 of 53

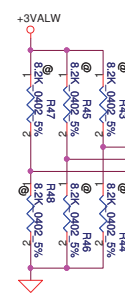
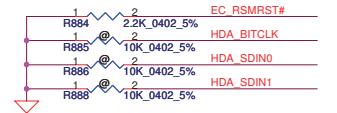
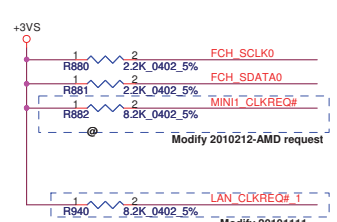
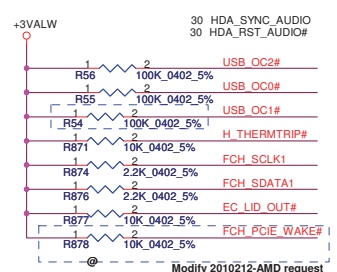
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PCIE_RST2 : Reset PCIE device on Hudson2



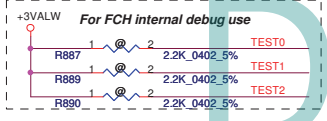
THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0->S0 PWR domain
SM bus 1->S5 PWR domain
VGA_PD: Support MLDAC power
save if connect
0: MLDAC power on
1: MLDAC power off



Project SKU ID	L(N)O	H(Y)ES
GPIO189 (use VGA)	R46	R45
GPIO190 (use PX)	R46	R45
GPIO191	R48	R47

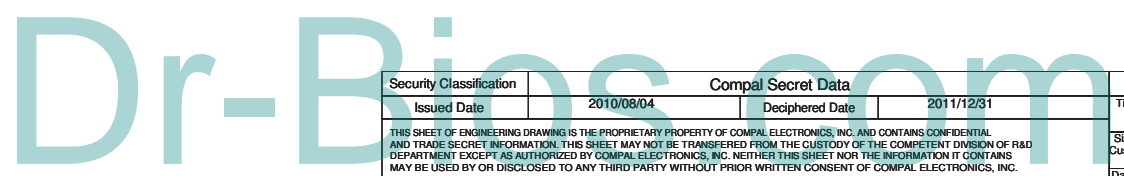
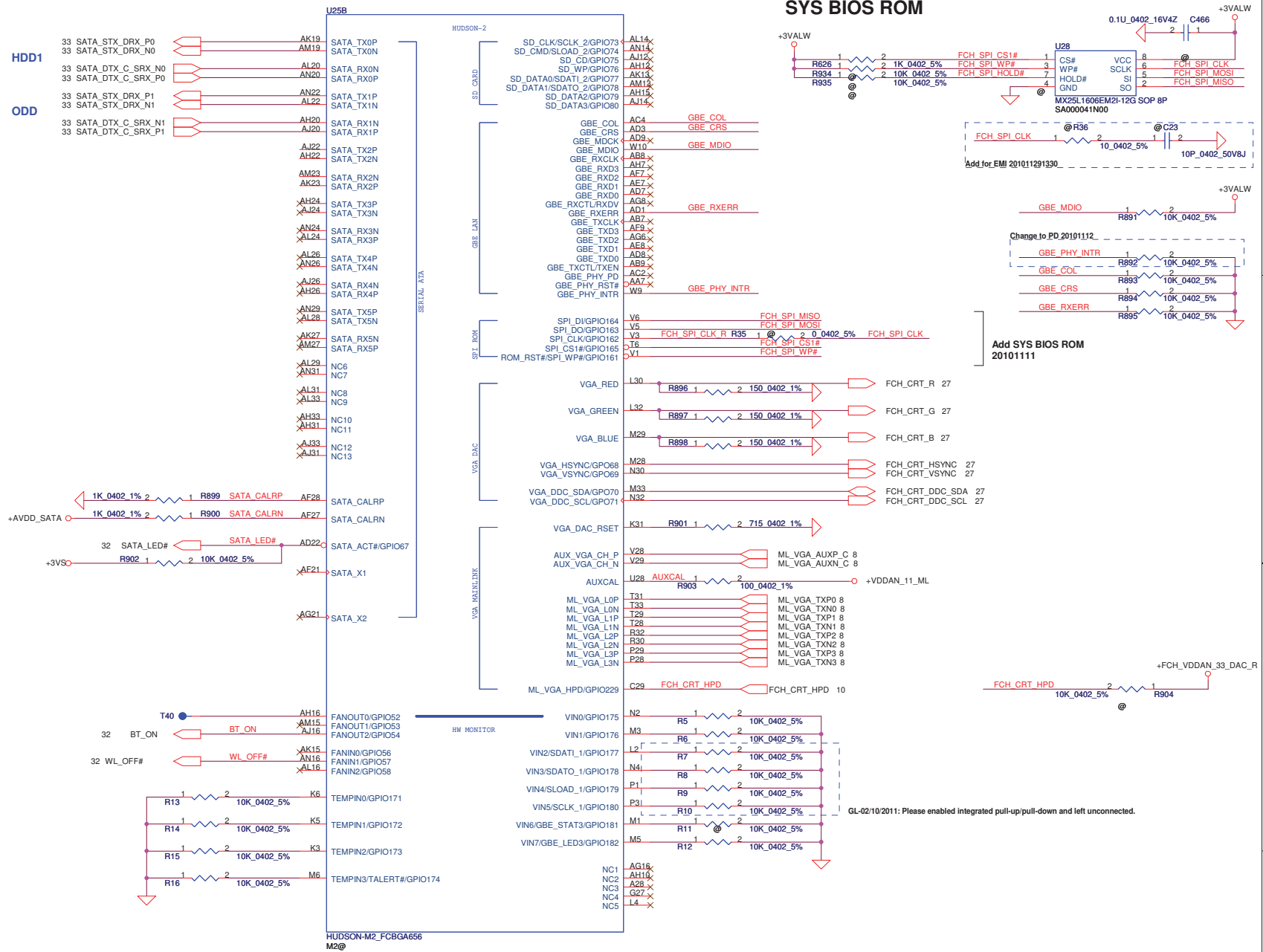
Add Project ID Table
201011301600



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		2011/12/31

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Compal Electronics, Inc.		Title
Size	Document Number	Hudson-M2/M3-ACPI/USB/EC
Custom	QBL50 LA-7551P	Rev 1.0
Date:	Friday, April 29, 2011	Sheet 14 of 53

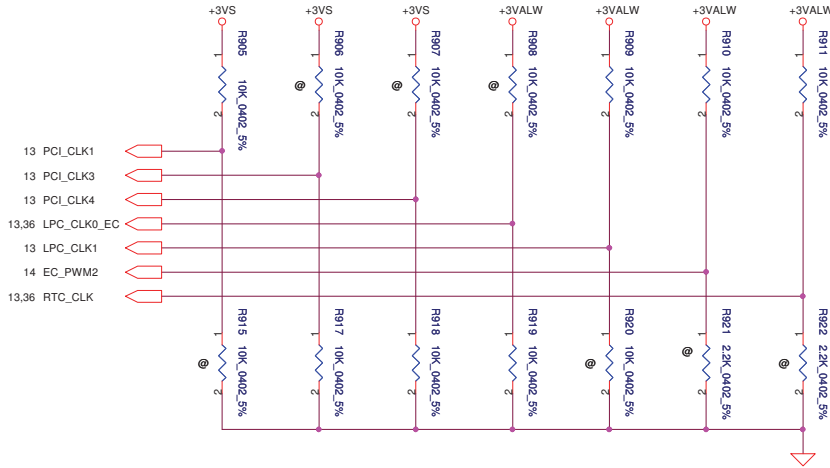


Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/04	Deciphered Date	2011/12/31	Hudson-M2/M3-SATA/GBE/HWM	
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				Custom	1.0
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Compal Electronics, Inc.
Hudson-M2/M3-SATA/GBE/HWM
Document Number
QBL50 LA-7551P
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STRAP PINS

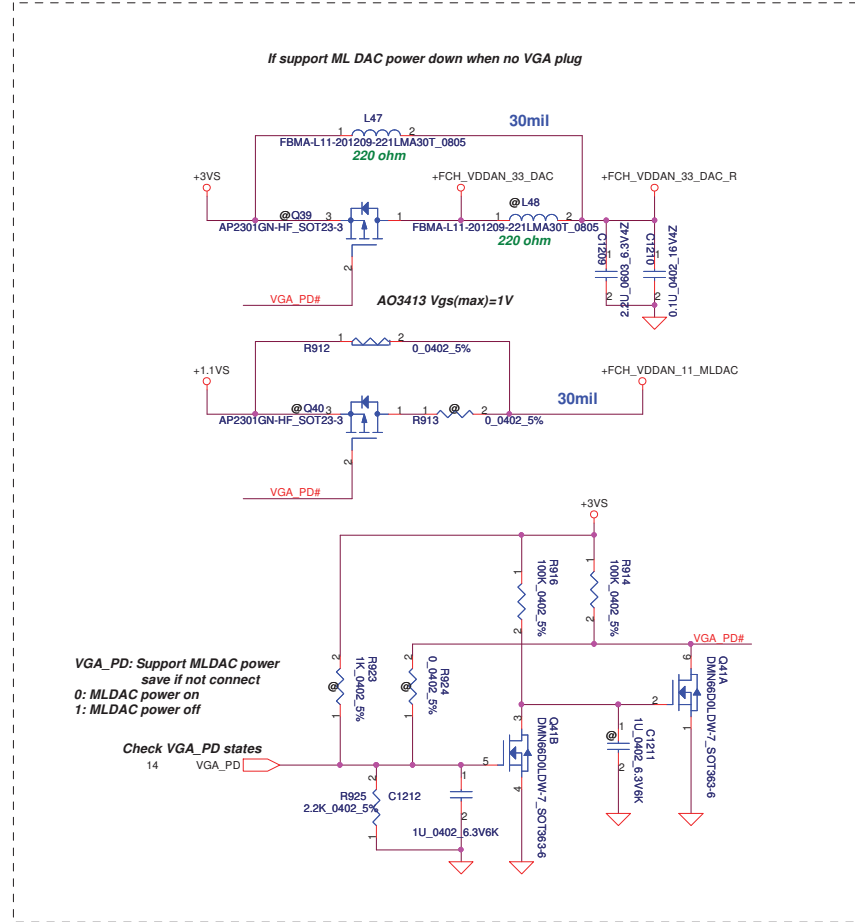
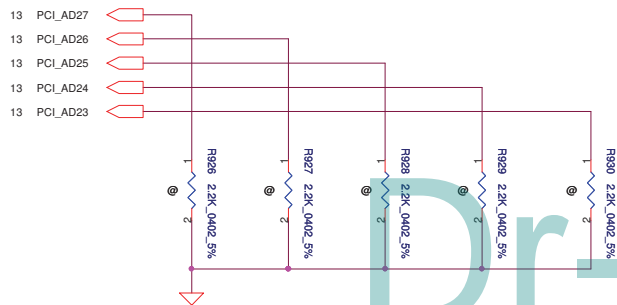
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



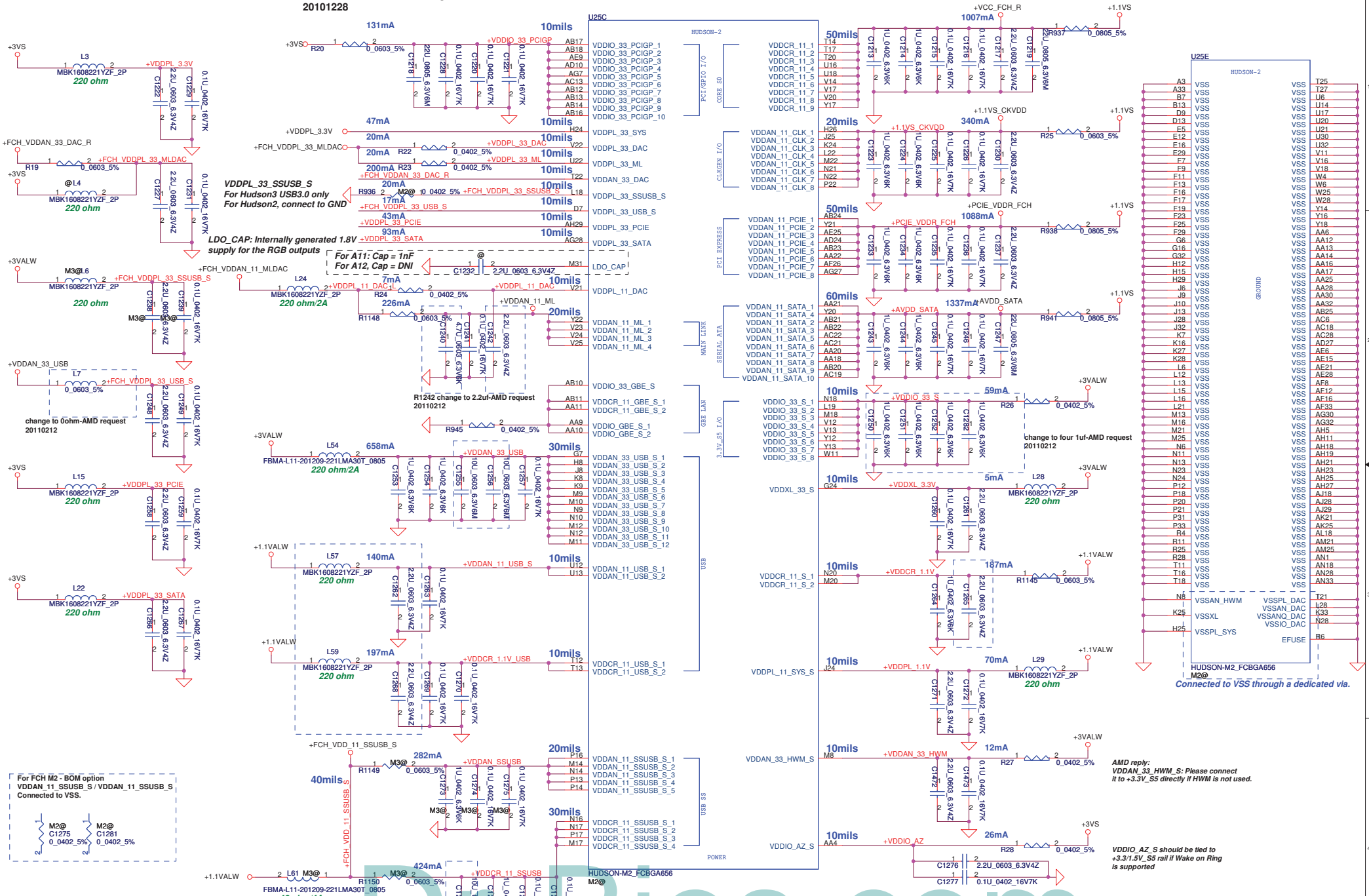
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS



C1218 / C1219 / C1247 Change to SE00000110
20101228



For FCH M2 - BOM option
VDDAN_11_S_SUSB_S / VDDAN_11_S_SUSB_S
Connected to VSS.

Connected to VSS through a dedicated via.

AMD reply:
VDDAN_33_HWM_S: Please connect
it to +3.3V_S5 directly if HWM is not used.

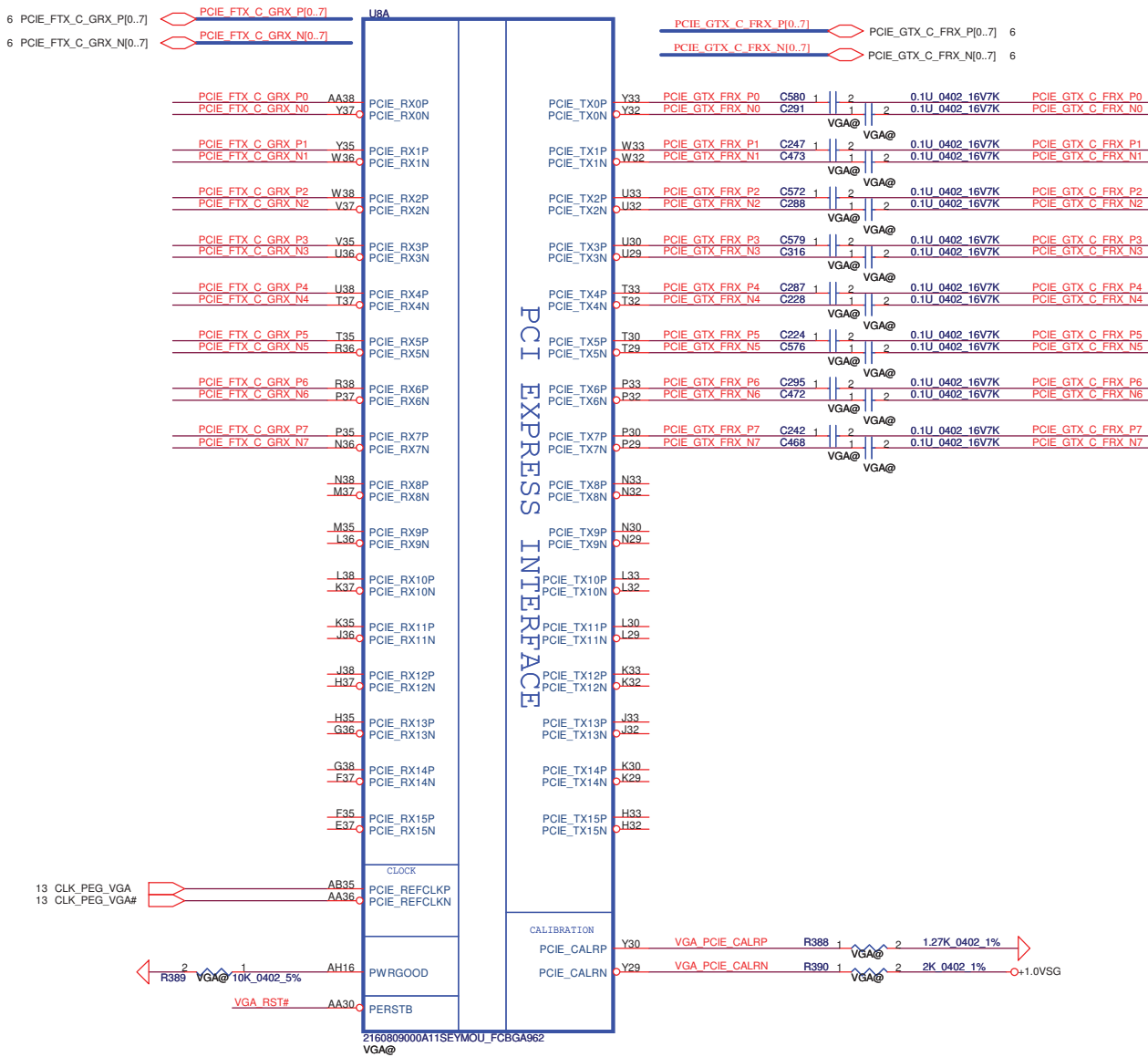
VDDIO_AZ_S should be tied to
+3.3V_S5 rail if Wake on Ring
is supported

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				Date:	Friday, April 29, 2011
				Sheet	17 of 53

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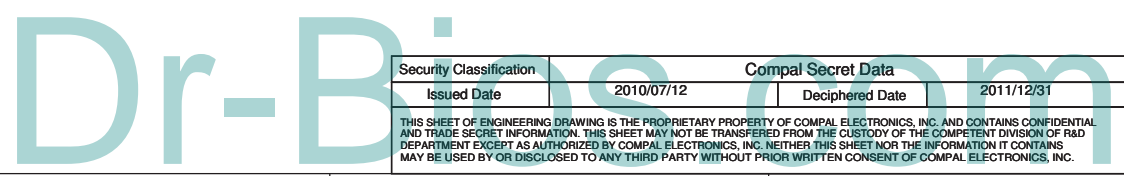
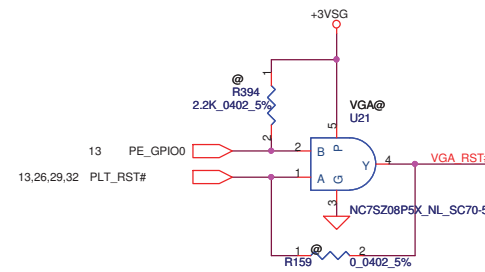
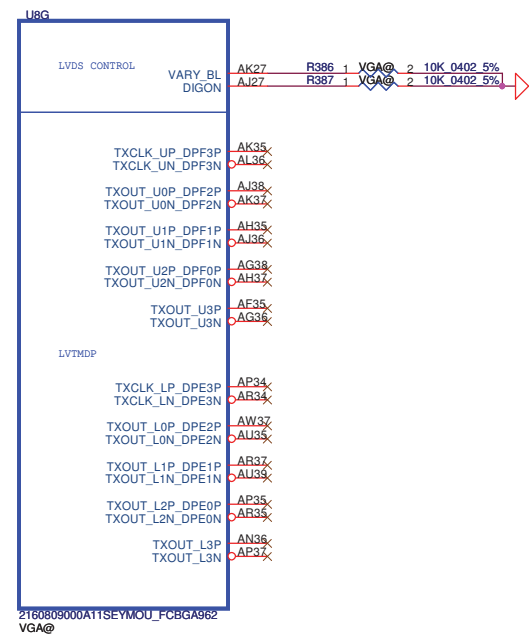
Hudson-M2/M3-POWER/GND

GFX PCIE LANE REVERSAL



<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need



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Size Custom	Document Number			Rev	
QBL50 LA-7551P				1.0	
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Strap Name	Pin Straps description <all Internal PD>	Setting
VIP_DEVICE_EN (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines memory apertures 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
CONFIG[1]		
CONFIG[0]		
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device (Internal PD) 0: Disable, 1: Enable	0
AUD[1]	HSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
AUD[0]	VSYNC	
BIF_GEN2_EN	GPIO2 Advertises the PCIe device as 5.0 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2VSYNC (GENLK_CLK) GPIO8 GPIO21 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

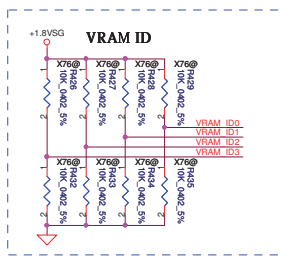
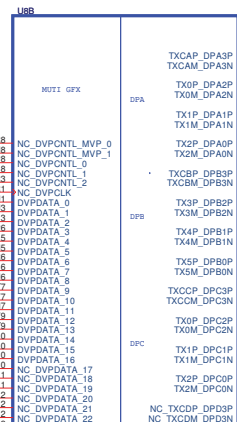
Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour



GPIO5 fast-power reduction: HW control will cause display disturb should use SW method control
GPIO6 voltage control signal, No use can NC!

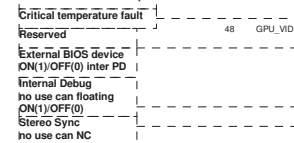
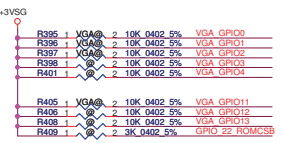
Move to DDCCLK_AUX3P,DDCCDATA_AUX3N,

GPIO7 Controls backlight on/off. Active High, need external PD
If GPIO22 High, GPIO 11-13 -> CFG[0:2] Config ROM type, GPU has internal PD

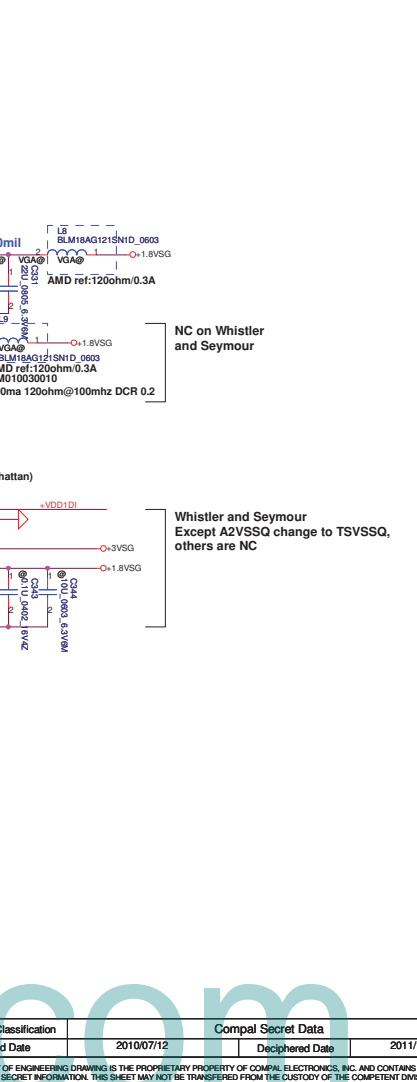
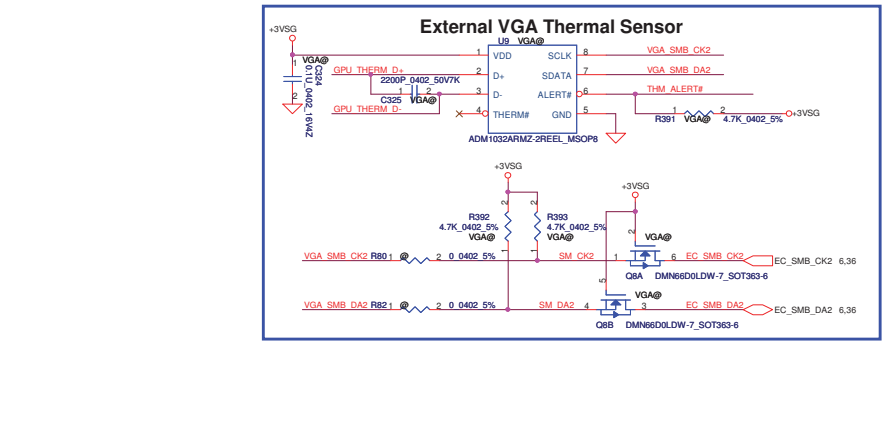
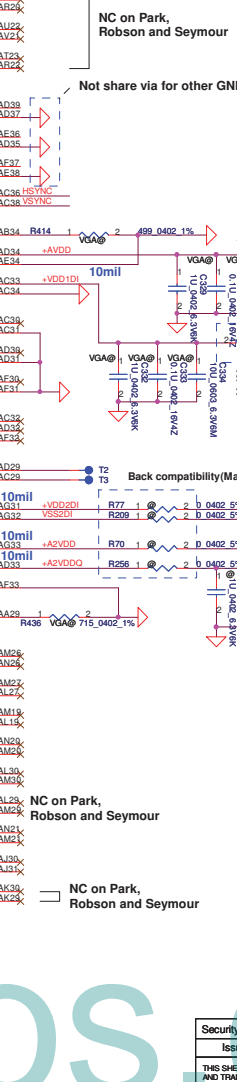
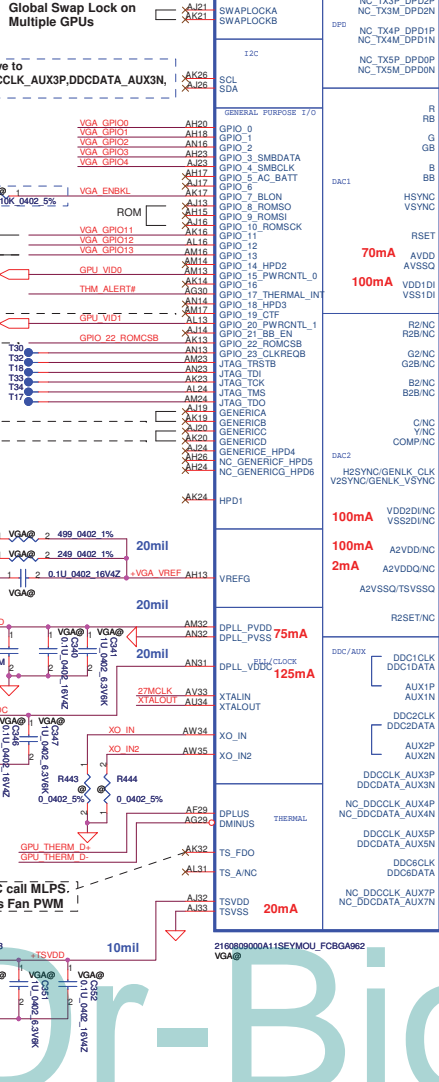
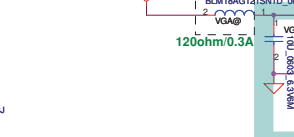
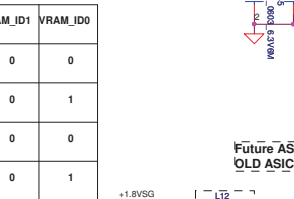
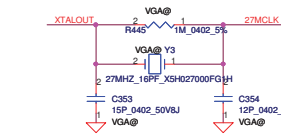
GPIO15,16,20 Voltage control signal
GPIO15 no use can NC
Thermal monitor interrupt
Critical temperature fault

Reserved

External BIOS device ON(1)/OFF(0) internal PD
Internal Debug no use can floating ON(1)/OFF(0)
Stereo Sync no use can NC
For ATI Cross fire no use can NC

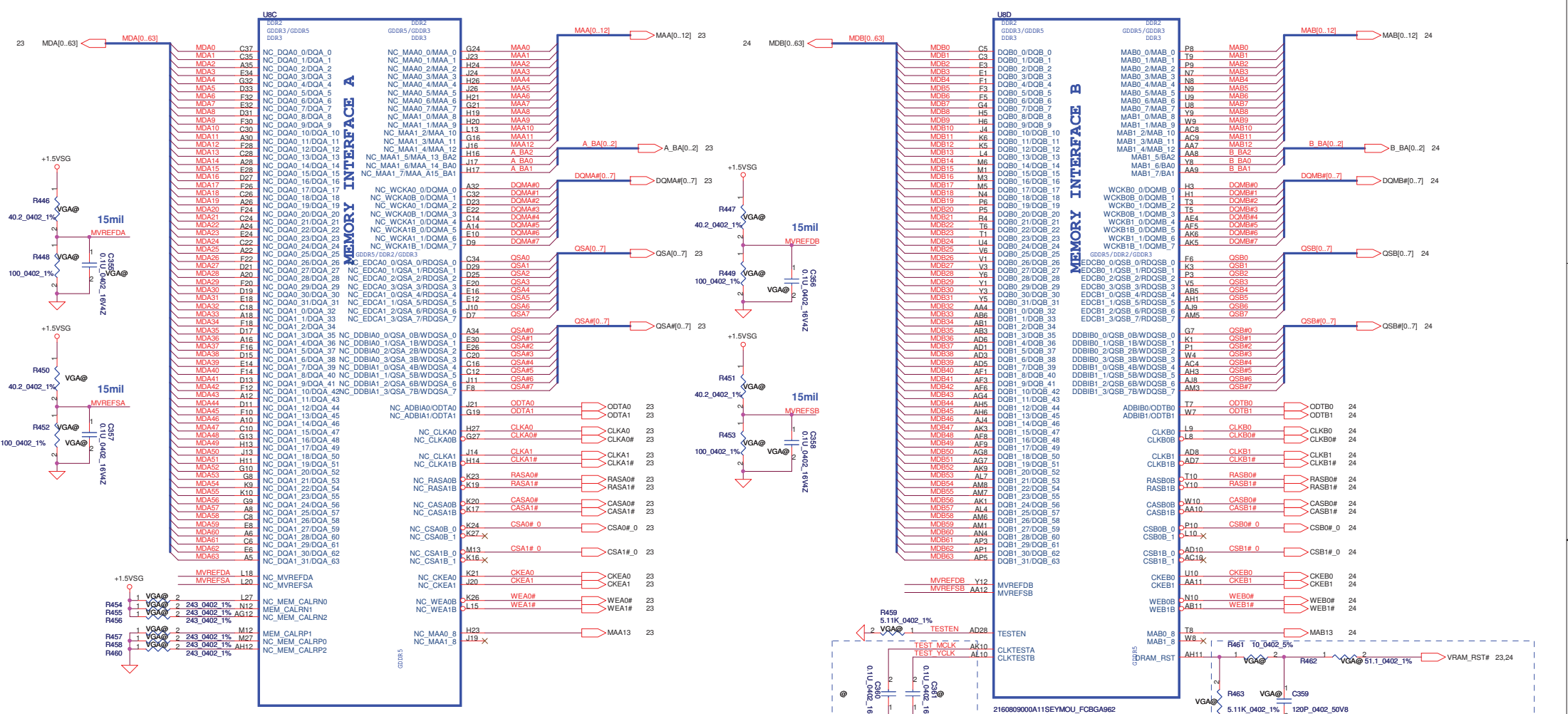


VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung BA100046E30	64M16x8	0	0	0	0
K4M1G1646G-BC11					
Samsung SA0000470A0	128M16x8	0	0	0	1
K4M2G1646G-BC11					
Hynix BA100041S60	64M16x8	0	1	0	0
H5TQ1G63DFR-11C					
Hynix SA00003Y030	128M16x8	0	1	0	1
H5TQ2G63BFR-11C					



GPIO8 Serial-ROM output from ROM, if GPIO22 High, GPIO 11-13 -> CFG[0:2] Config ROM type, GPU has internal PD
GPIO10 Serial-ROM input to ROM, if GPIO22 Low, GPIO 11-13 -> CFG[0:2] Config Primary memory-aperture size
GPIO22 Serial-ROM clock to ROM, Config ROM type, GPU has internal PD
GPIO22 external BIOS-ROM enable, Config Primary memory-aperture size
CFG[3:0], 128MB 000
256MB 001
64MB 010

GPIO8, GPIO9, GPIO10 no use can NC
GPIO22 Enable need 3K PH, no use must NC



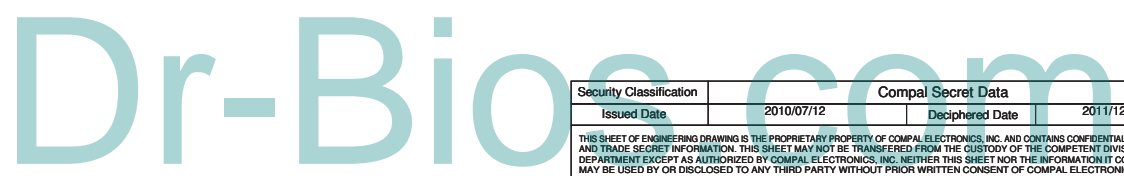
2160809000A11SEYMOU_FCBGA962
VGA@

2160809000A11SEYMOU_FCBGA962
VGA@

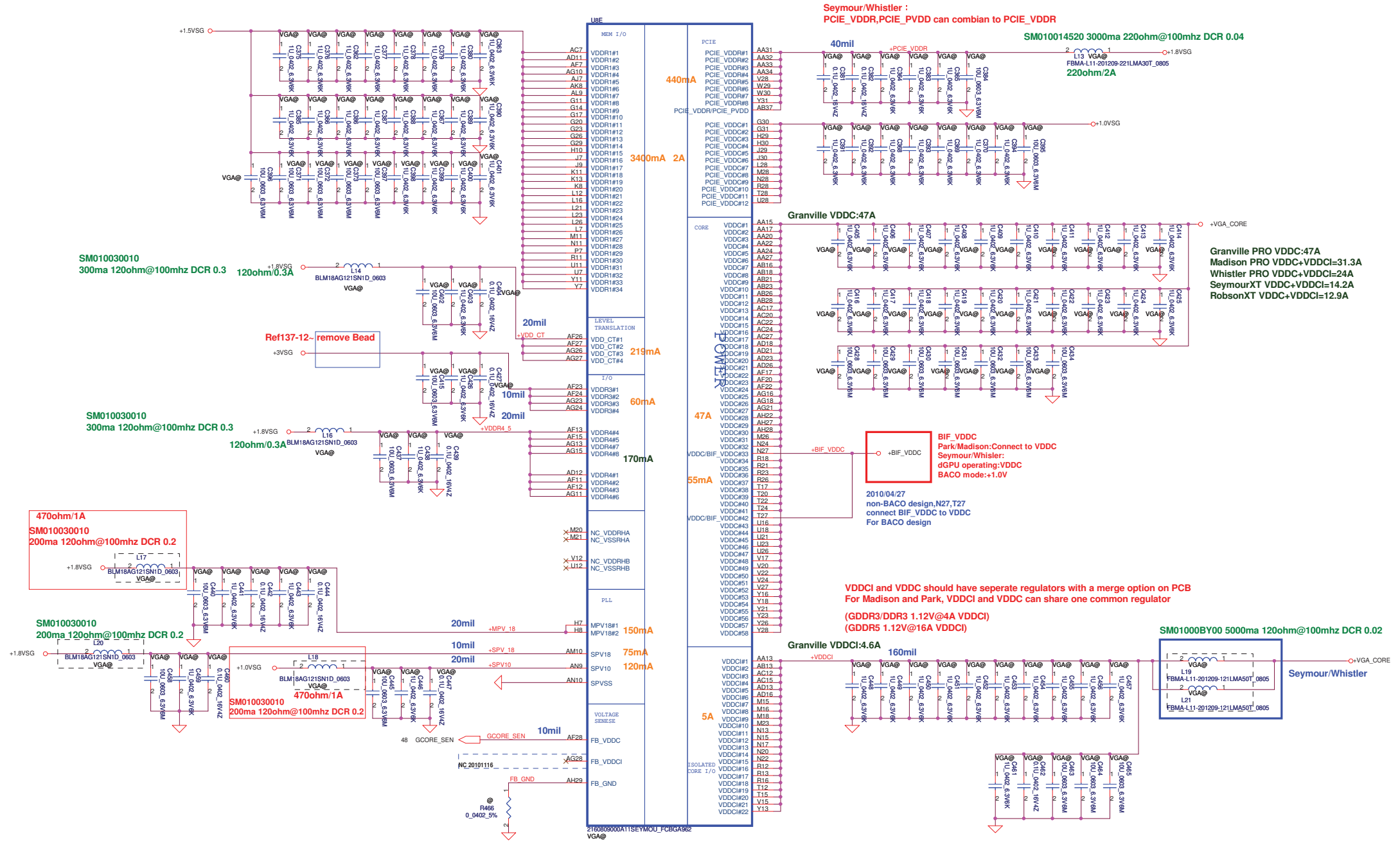
Note:
route 50ohms single-ended
and 100ohms diff
and keep short
REF137-03 suggest

Park&Seymour is single channel for memory (channel B only)

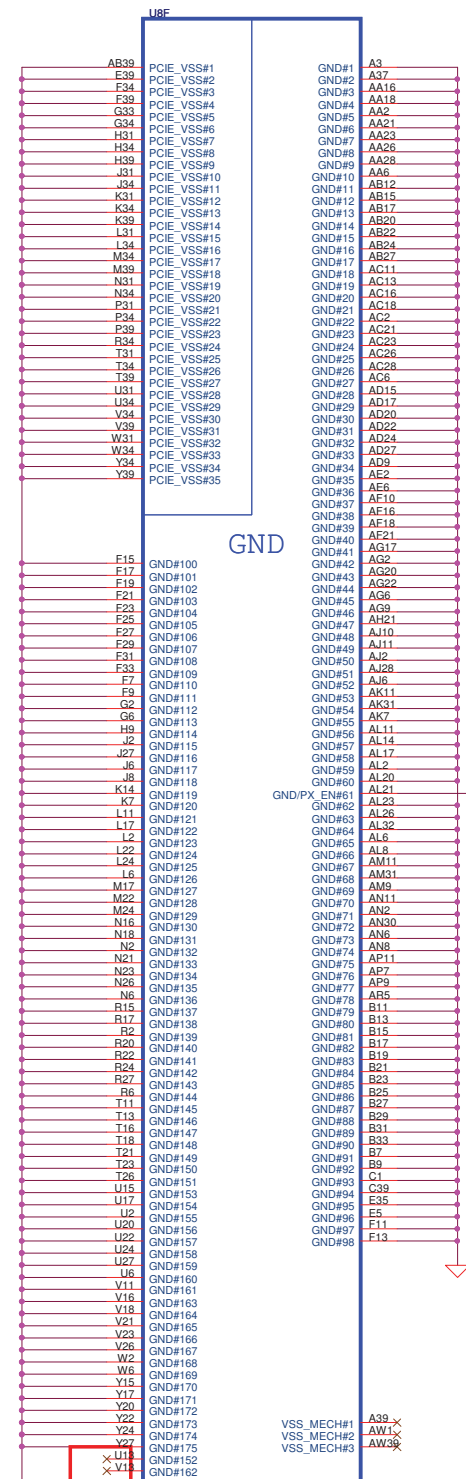
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within5mm) except Rser2



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Customer			Vancouver_Power/GND	
Document Number			QBL50 LA-7551P	
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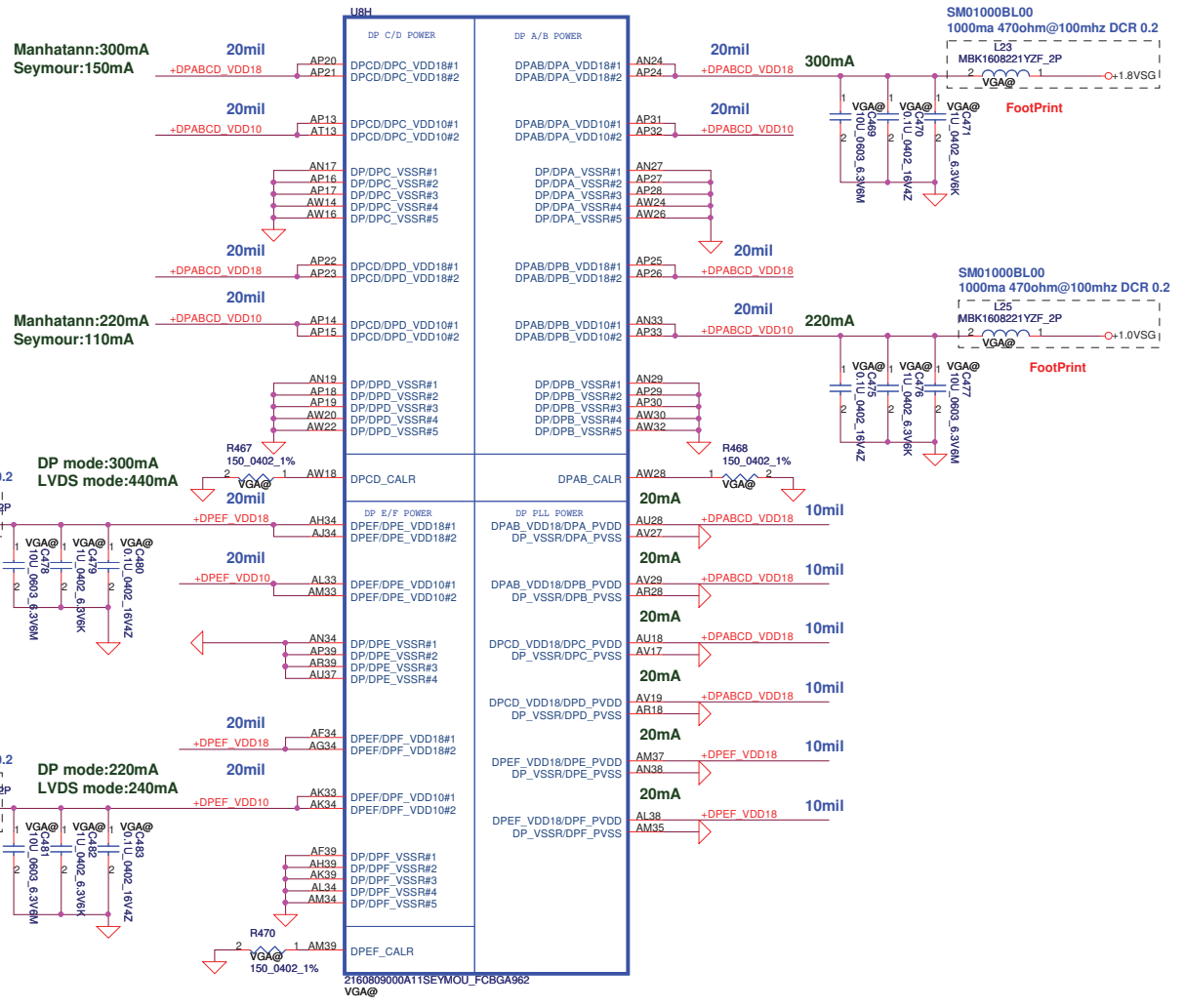


DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD can combian to DPAB_VDD18
 DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD can combian to DPCD_VDD18
 (DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
 DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD can combian to DPEF_VDD18

Seymour/Whistler :
 DPA_VDD10,DPB_VDD10 can combian to DPAB_VDD10
 DPC_VDD10,DPD_VDD10 can combian to DPCD_VDD10
 DPE_VDD10,DPD_VDD10 can combian to DPEF_VDD10

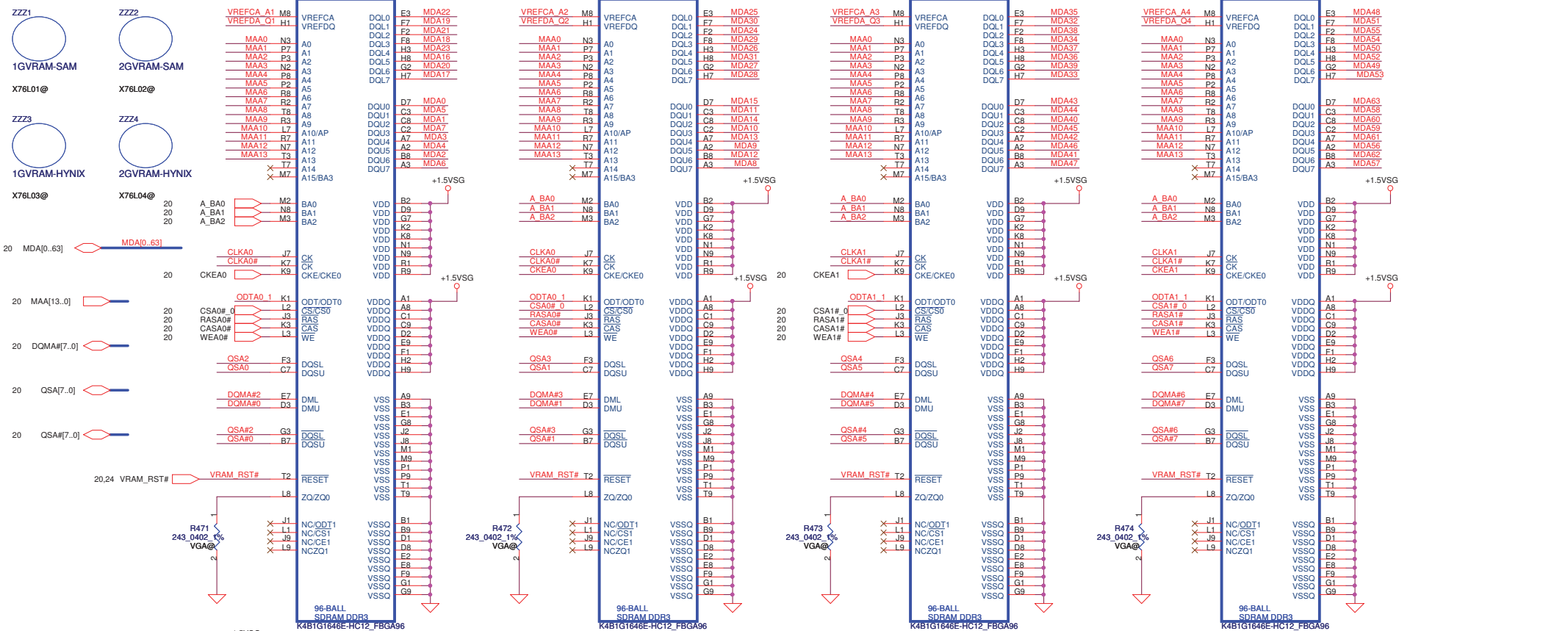
DPx-VSSR,DPx_PVSS can combian to DP_VSSR (Manhattan should have individual GND) where x is A,B,C,D,E,F

Park/Madison :AL21:left NC
 Seymour/Whistler:
 AL21:PX_EN
 use to control discreate GPU regulators for power express BACO mode
 Support BACO:
 output High3.3V:turn off regulators (BACO mode on)
 output Low0V:turn on regulators (BACO mode off)
 need PD resistor
 No support BACO:
 left NC

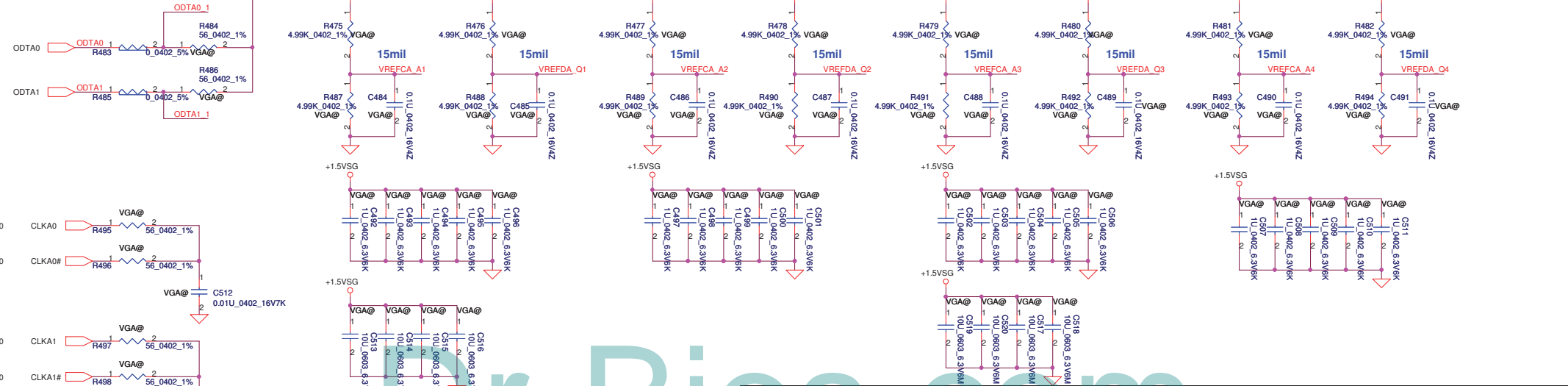


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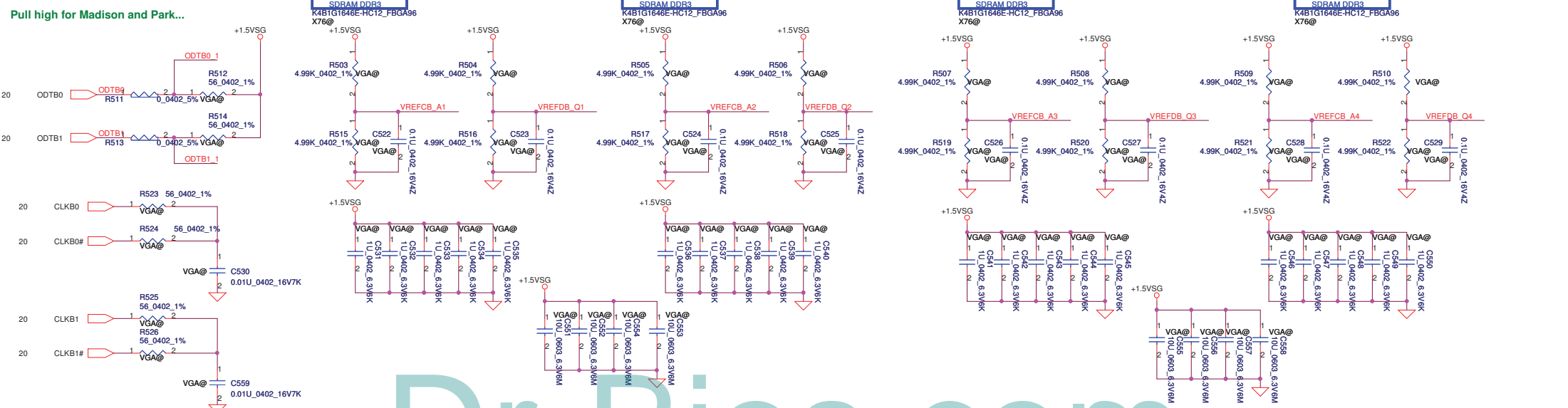
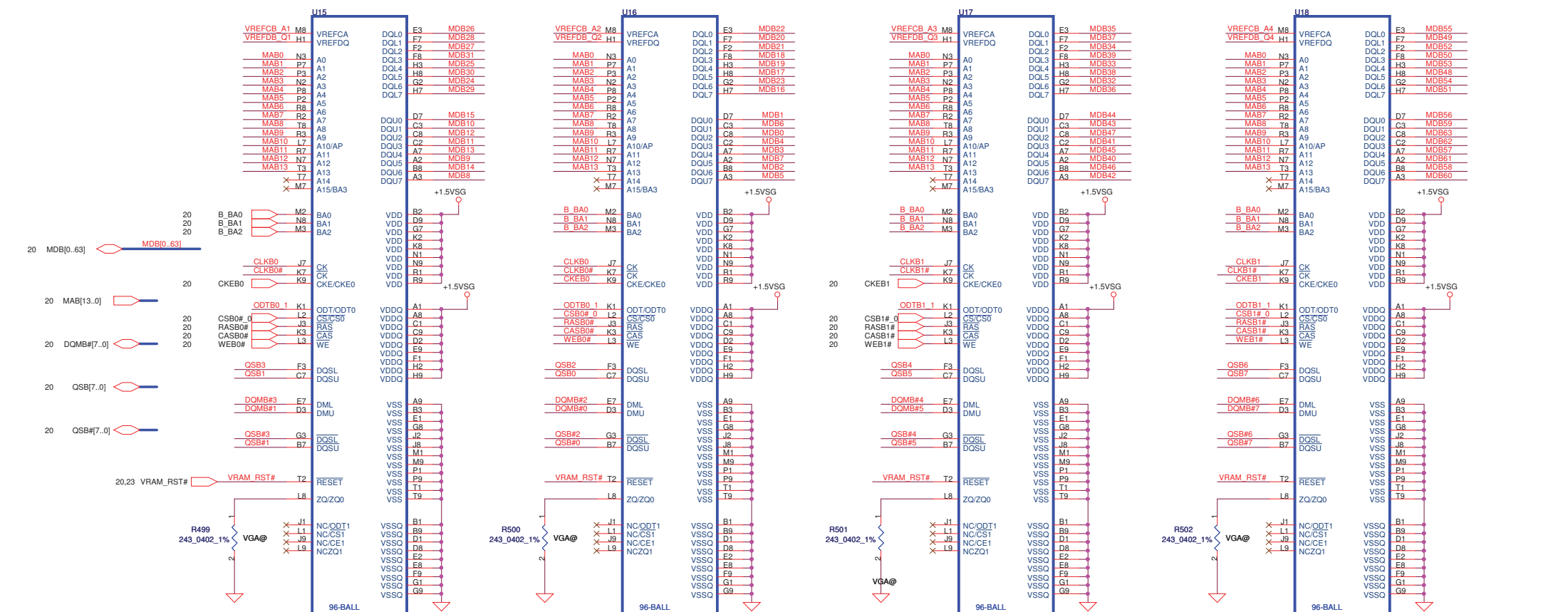
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Title	Vancouver Power/GND	
Size	Document Number	Rev
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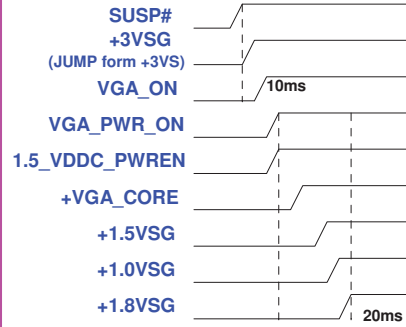
Pull high for Madison and Park...



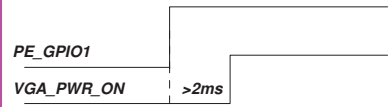
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2011/12/31	VRAM DDR3 / Channel A	
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Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

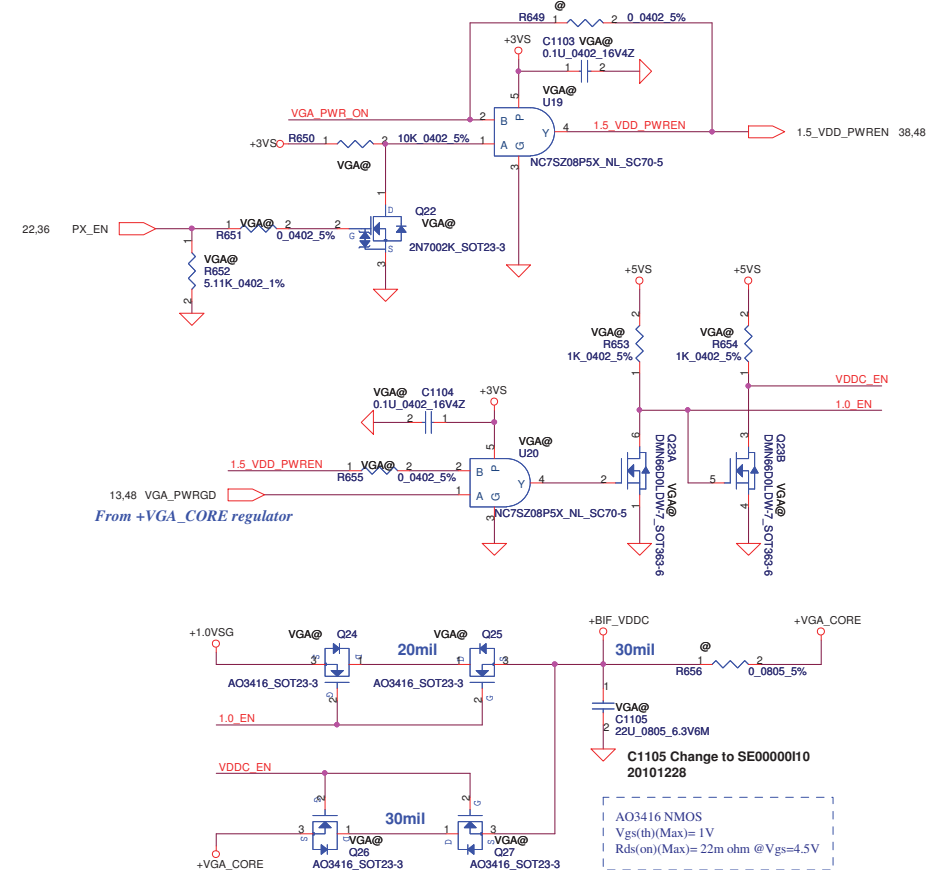
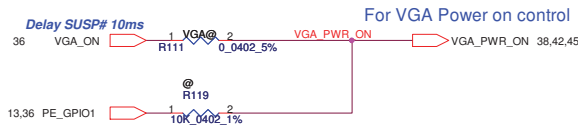


VGA Muxless with BACO Status Mapping table

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

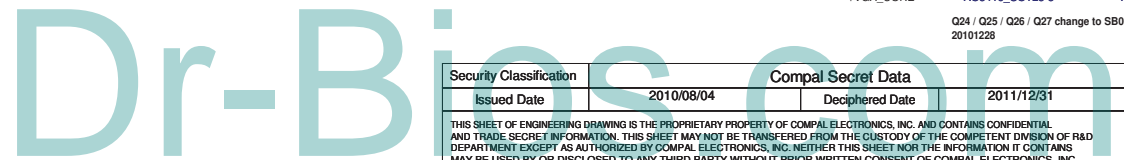
VGA_PWR_ON source signal	Whistler
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



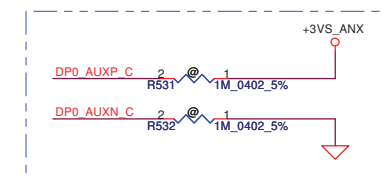
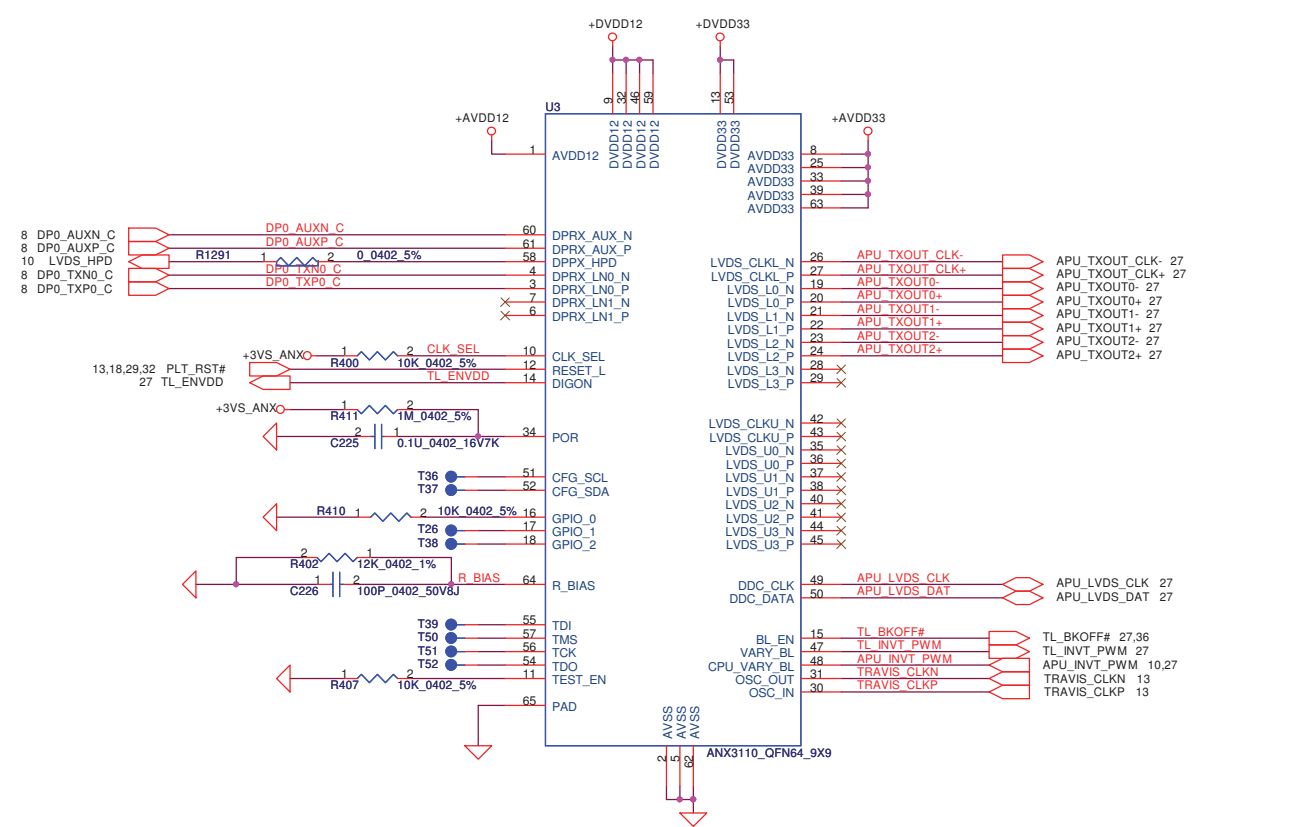
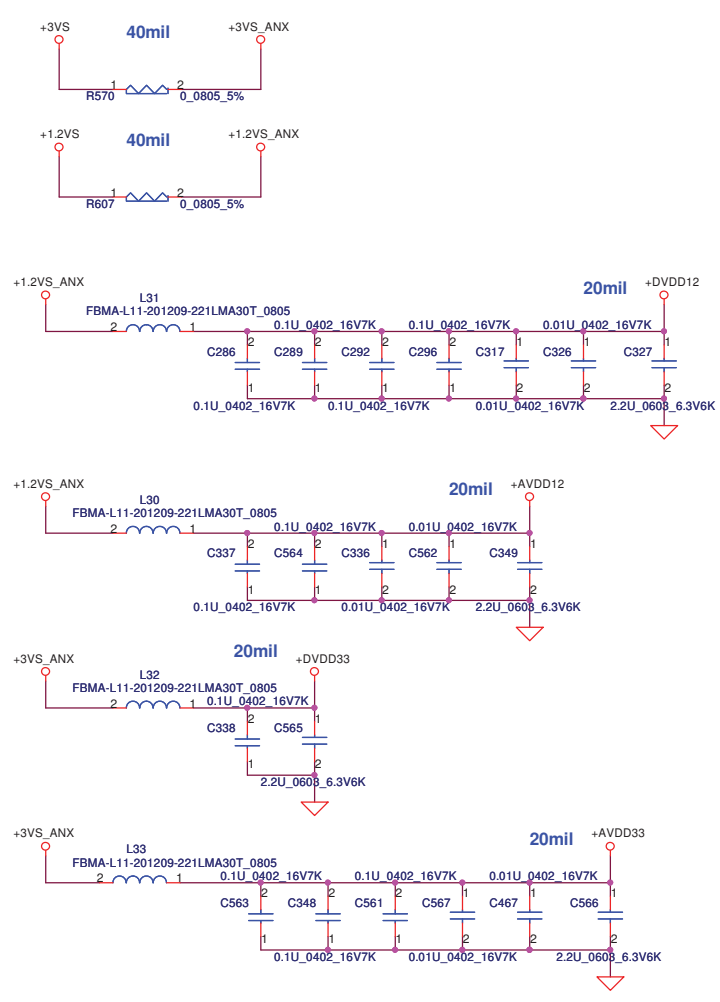
Q24 / Q25 / Q26 / Q27 change to SB00000FG10 20101228

C1105 Change to SE00000H10 20101228

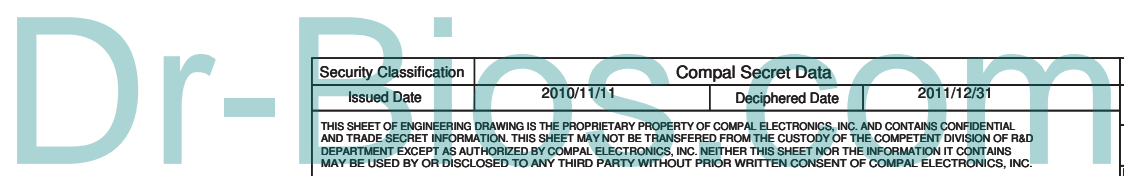
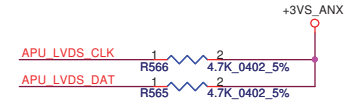
AO3416 NMOS
 $V_{gs(th)}(Max) = 1V$
 $R_{ds(on)}(Max) = 22m\ \Omega @ V_{gs} = 4.5V$



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Title	VGA power sequence and BACO		
Size	Document Number	Rev	
Customer	QBL50 LA-7551P		1.0
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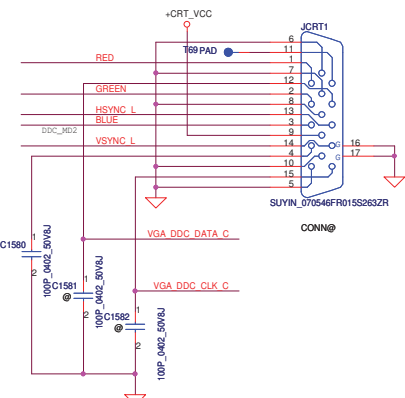
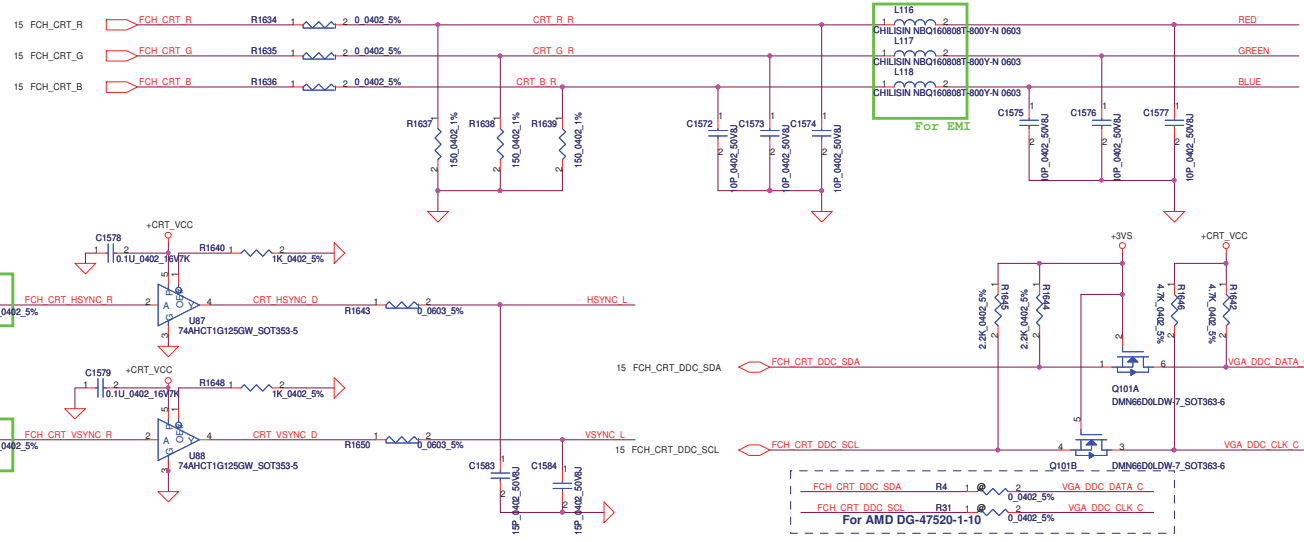
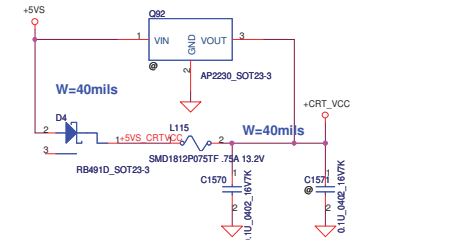
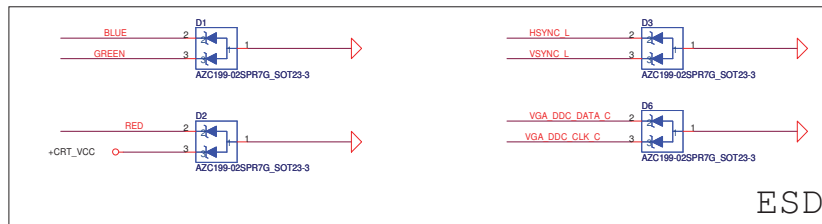


Place via on each trace bus and let resistor very close the via

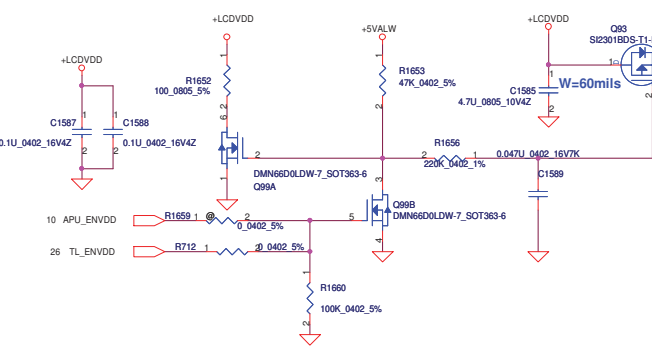


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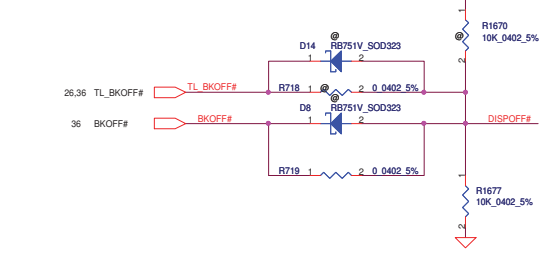
CRT



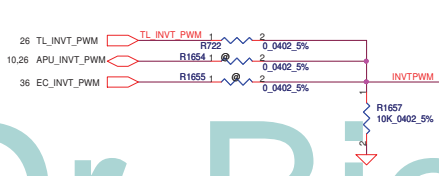
Panel LCDVDD Control



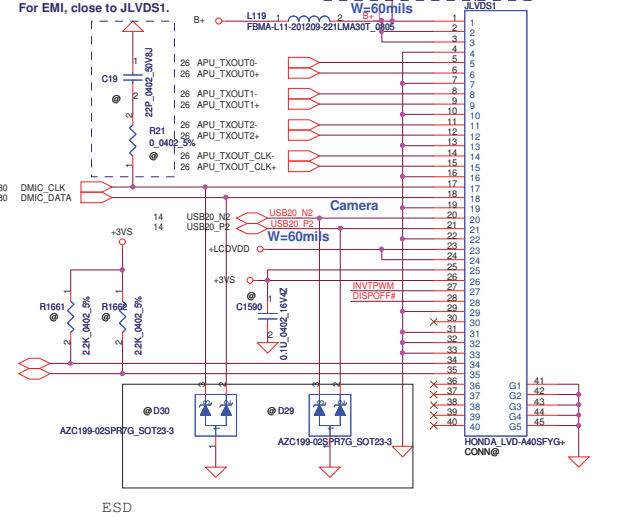
Panel Backlight Control



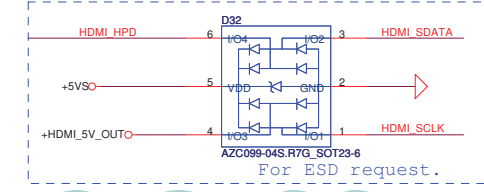
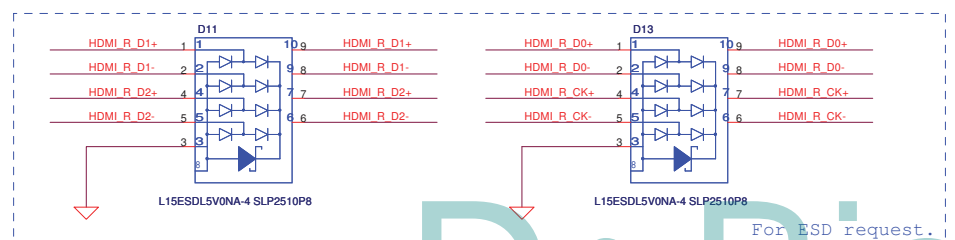
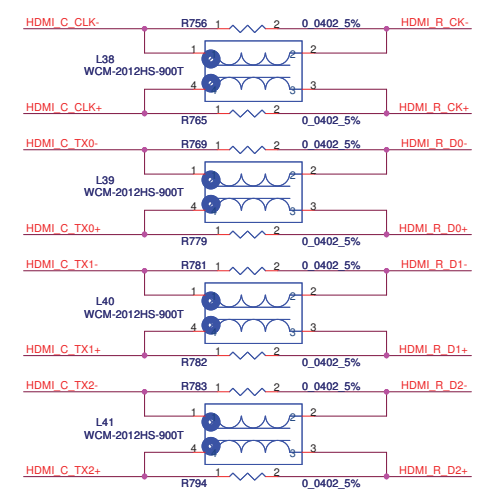
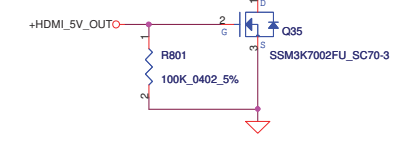
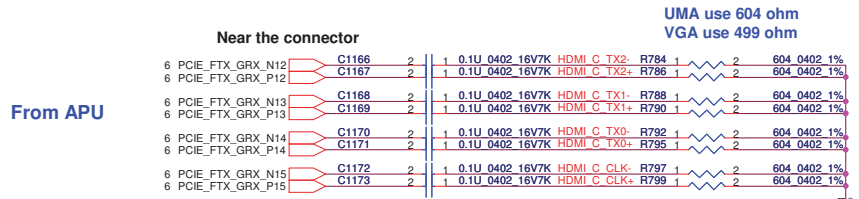
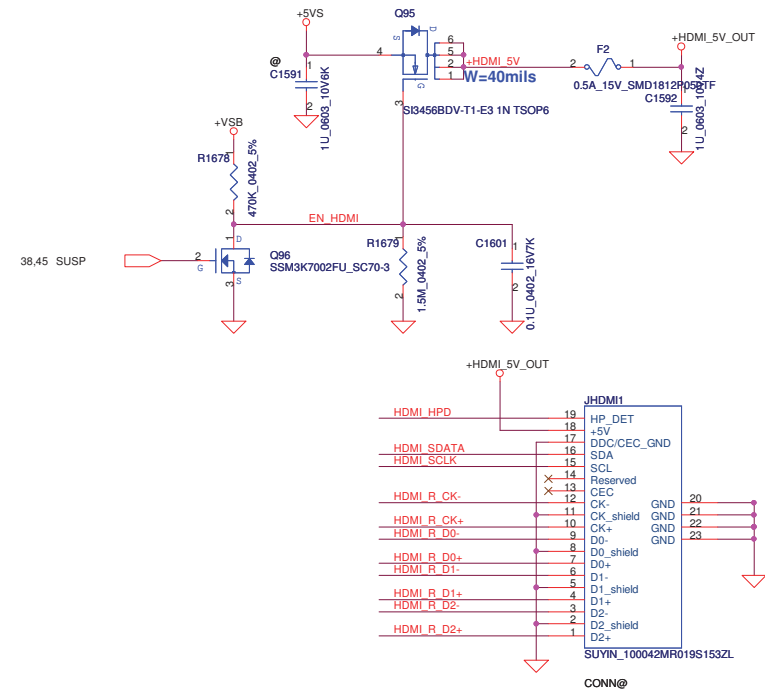
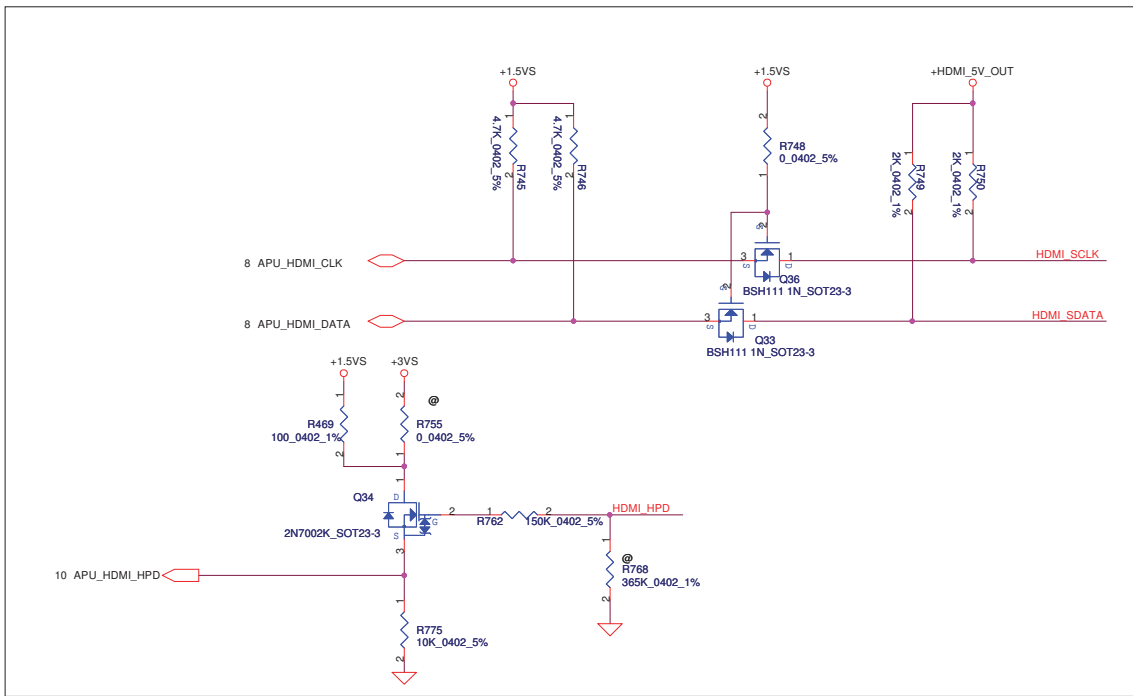
Panel PWM Control



For EMI, close to JLVDS1.



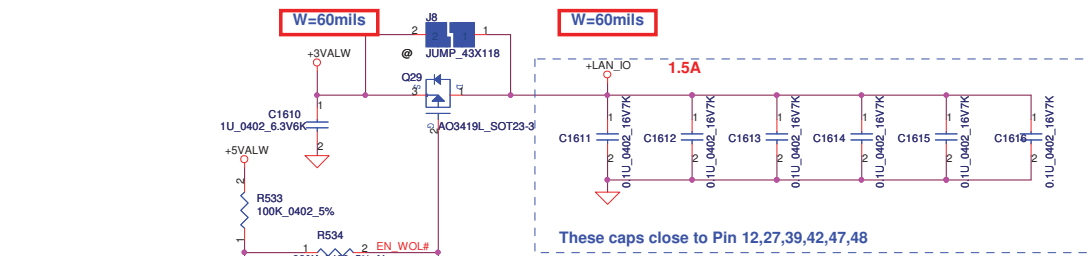
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Size	Document Number	Rev	1.0
C	QBL50 LA-7551P	Date:	Wednesday, April 27, 2011
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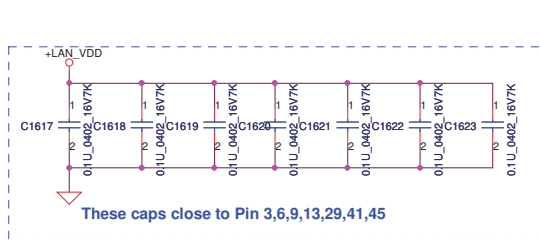
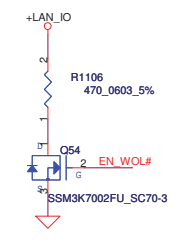
Dr-Bliss.com

For ESD request.

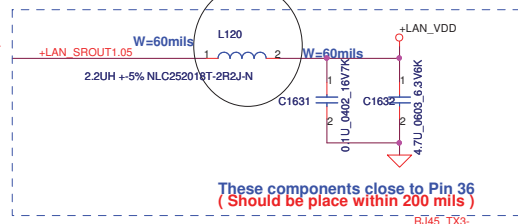
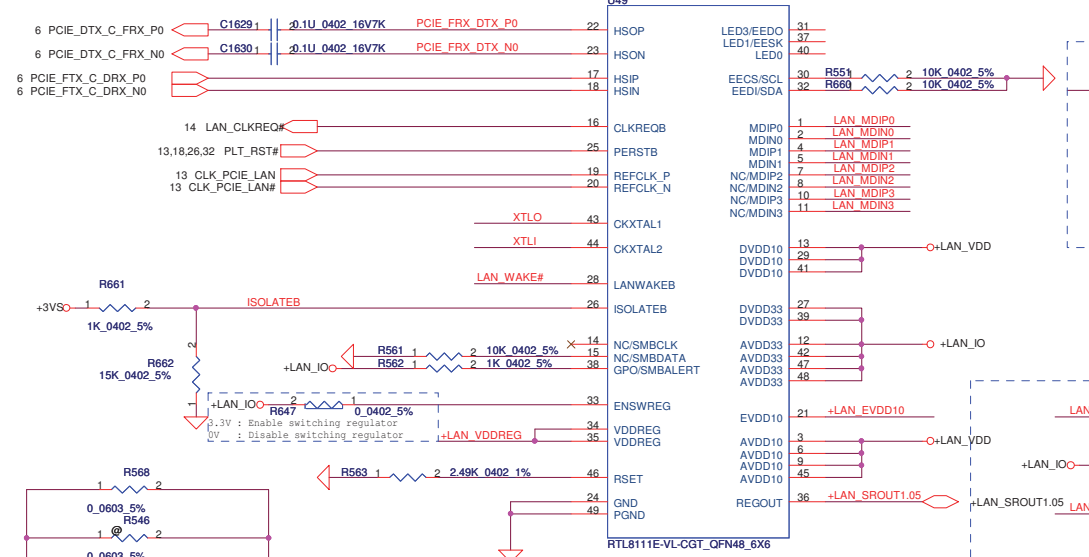
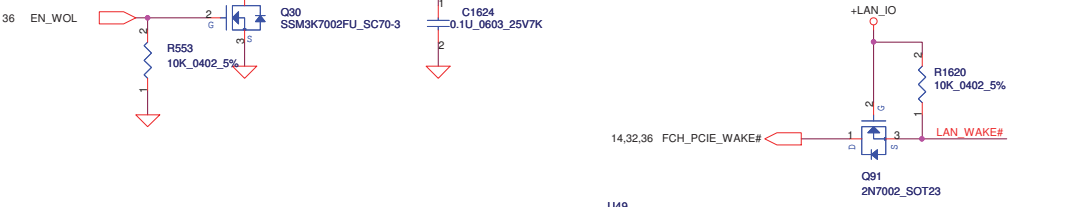
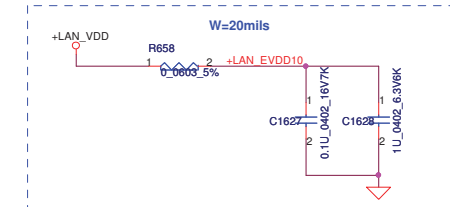
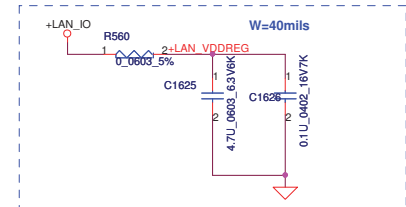
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		Date	Wednesday, April 27, 2011	1 Sheet 28 of 53



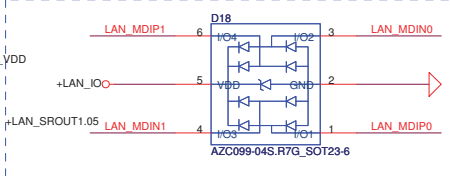
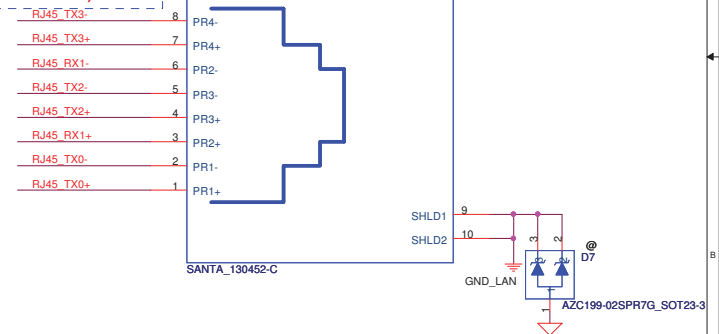
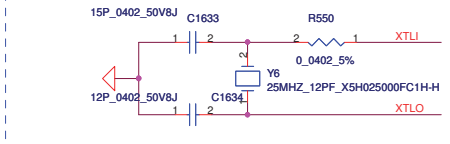
These caps close to Pin 12,27,39,42,47,48



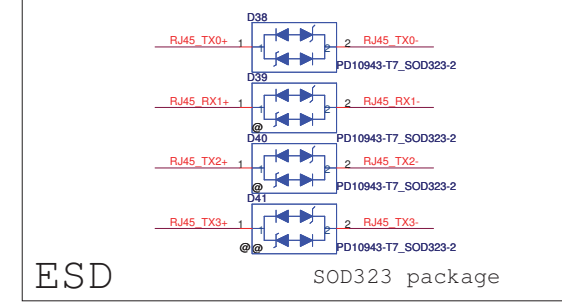
These caps close to Pin 3,6,9,13,29,41,45



These components close to Pin 36 (Should be place within 200 mils)

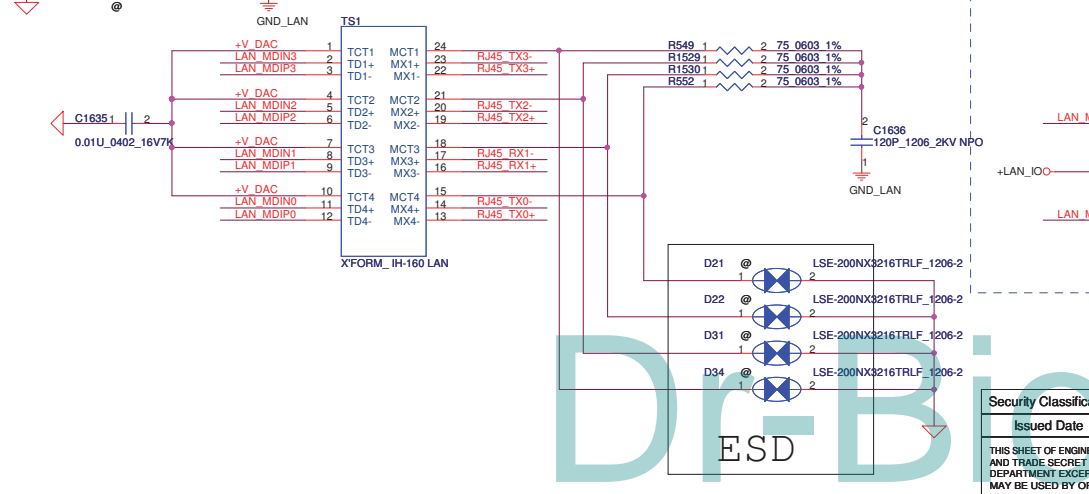


For ESD request.



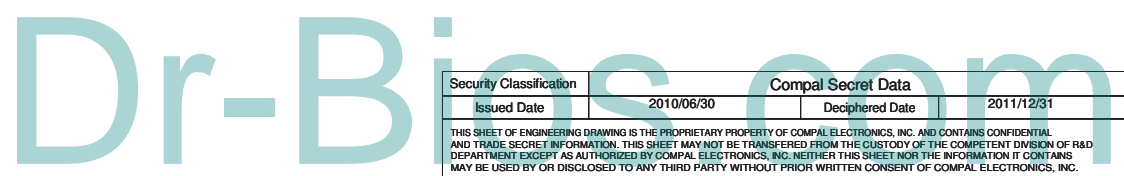
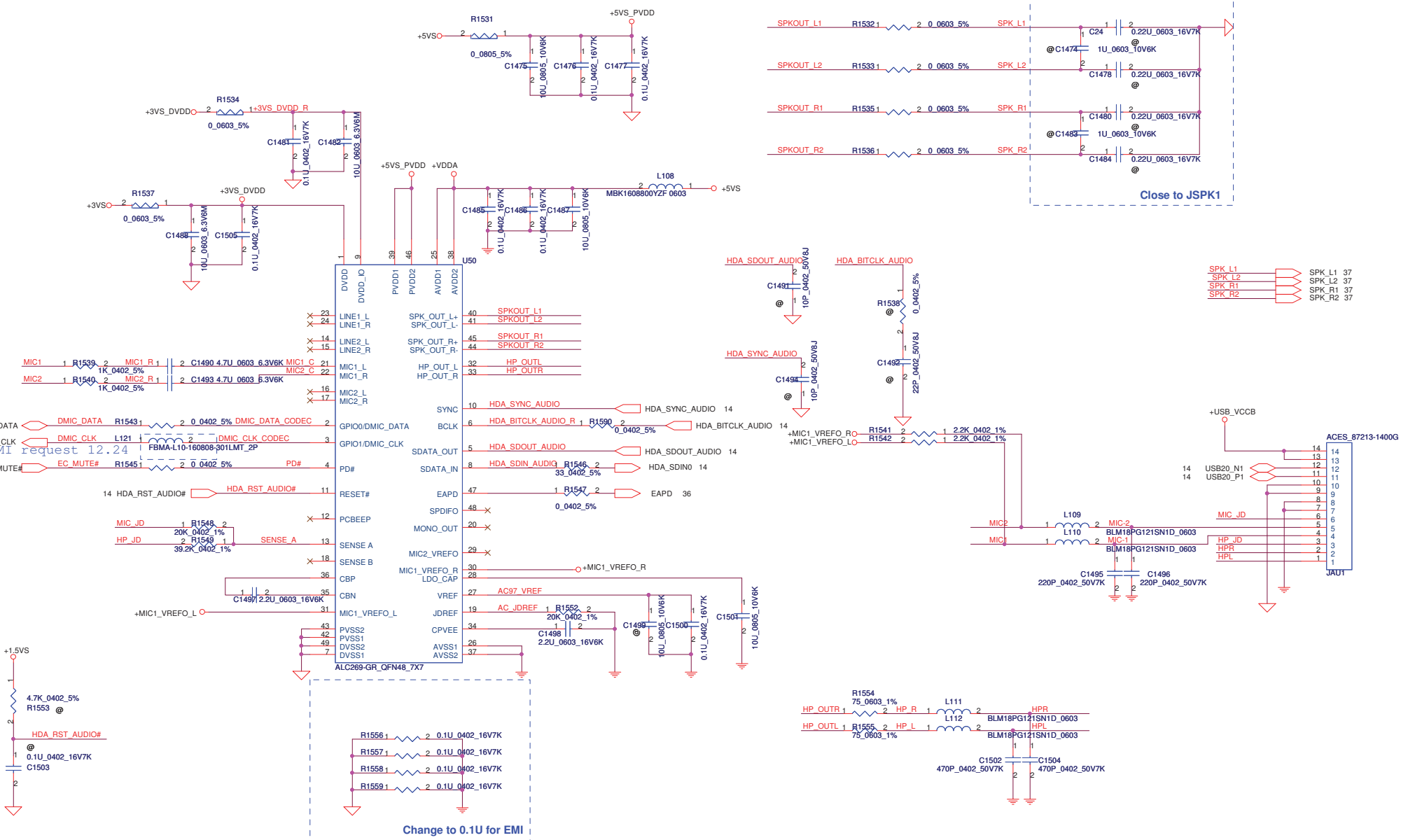
ESD

SOD323 package



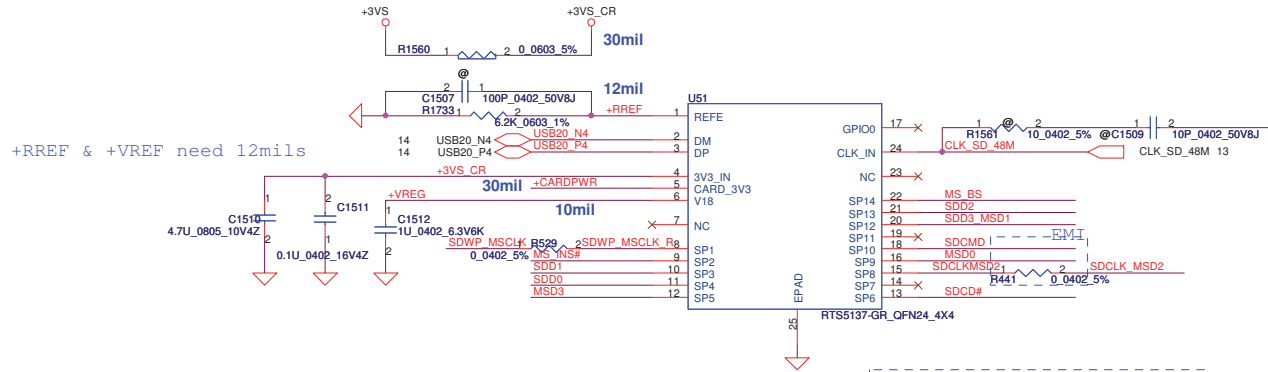
ESD

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Size	Document Number	Rev		
Customer	QBL50 LA-7551P			1.0
Date	Wednesday, April 27, 2011	Sheet	29	of 53

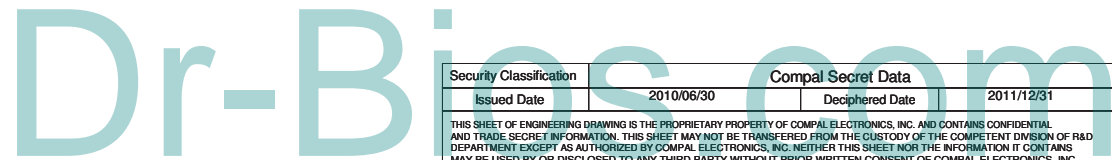
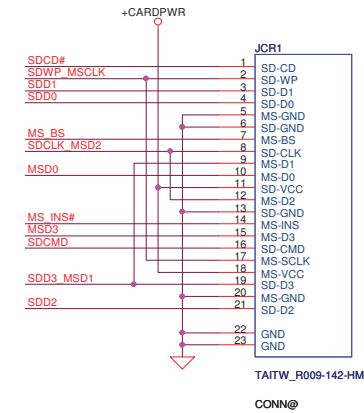
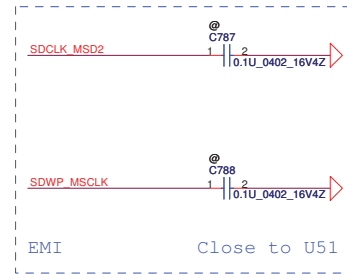
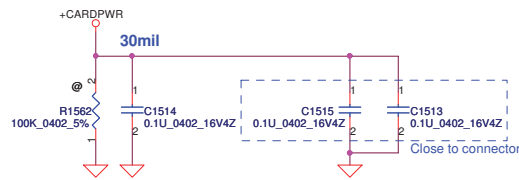


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Size	Document Number	Rev		Date	
Custom	QBL50 LA-7551P	1.0		Wednesday, April 27, 2011	
Date			Sheet 30 of 53		

Card Reader RTS5137 (only SD/MMC/MS function)



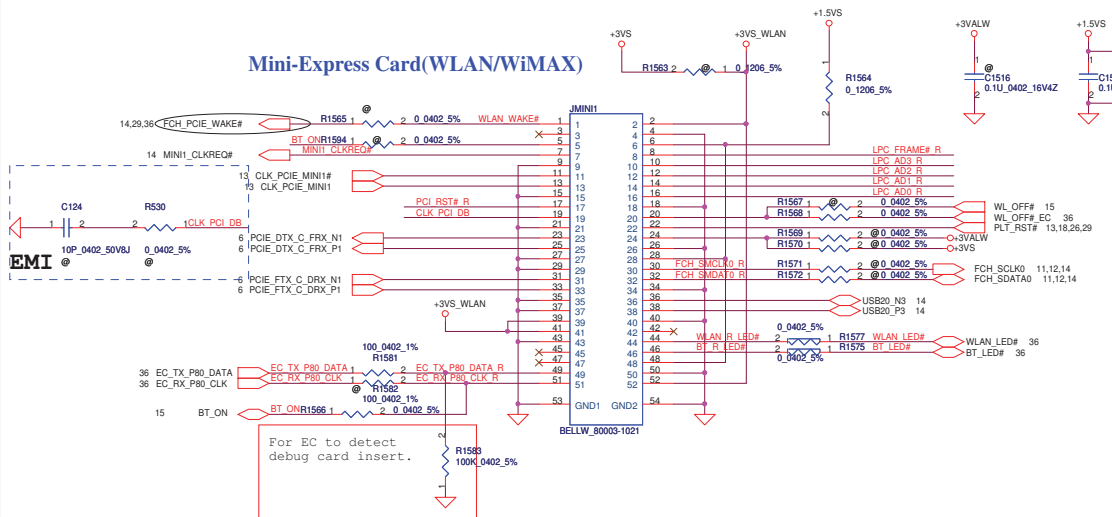
Card Reader Connector



Security Classification	2010/06/30	Compal Secret Data	Deciphered Date	2011/12/31	Title	Compal Electronics, Inc.	
Issued Date					P27-RTS5137 Media Card Controller		
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					Custom	QBL50 LA-7551P	1.0
					Date:	Wednesday, April 27, 2011	Sheet 31 of 53

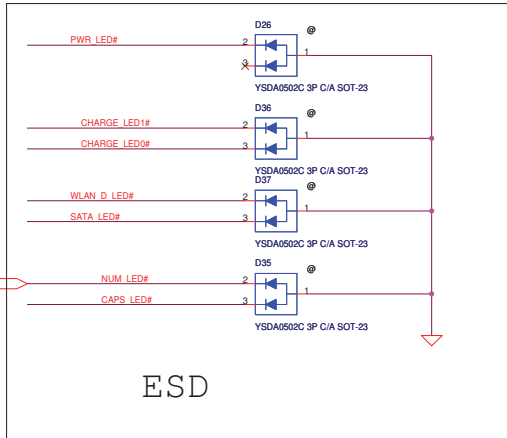
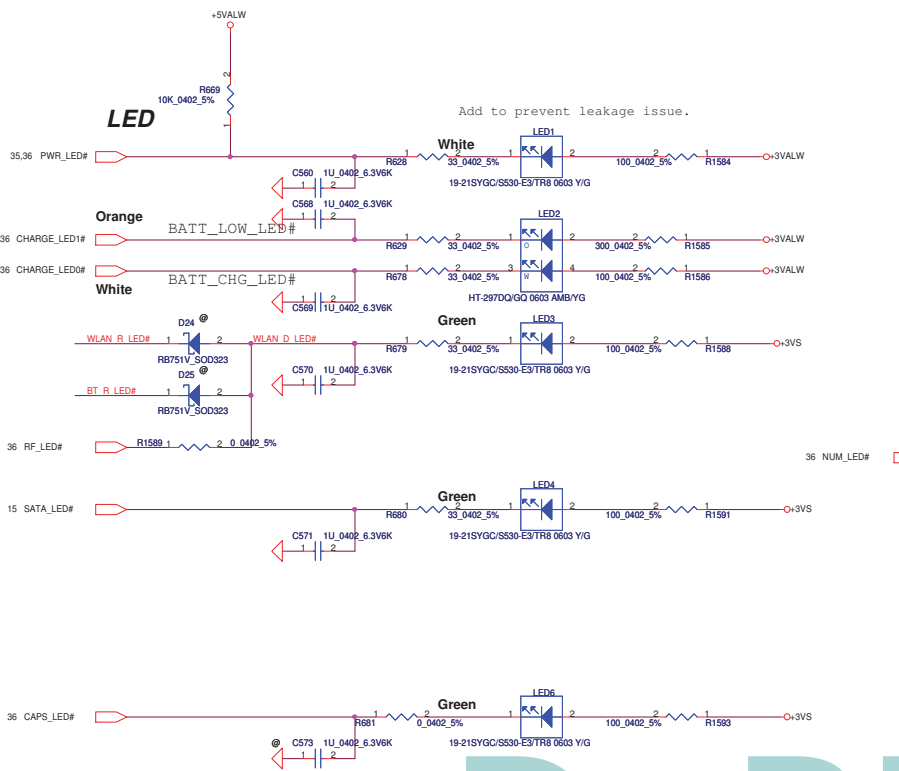
Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

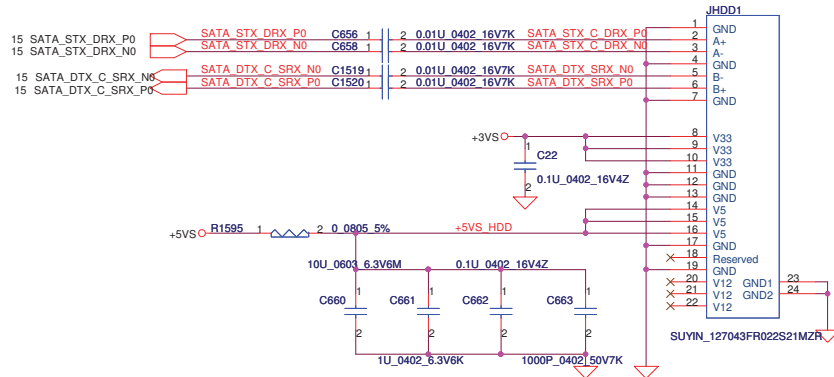
LPC_FRAME# R	R1573	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	13,36
LPC_AD3 R	R1574	1	2	0.0402 5%	LPC_AD3	LPC_AD3	13,36
LPC_AD2 R	R1576	1	2	0.0402 5%	LPC_AD2	LPC_AD2	13,36
LPC_AD1 R	R1578	1	2	0.0402 5%	LPC_AD1	LPC_AD1	13,36
LPC_AD0 R	R1579	1	2	0.0402 5%	LPC_AD0	LPC_AD0	13,36
PCI_RST# R	R1580	1	2	0.0402 5%	PLT_RST#	PLT_RST#	13
CLK_PCIE_DB					CLK_PCIE_DB	CLK_PCIE_DB	13



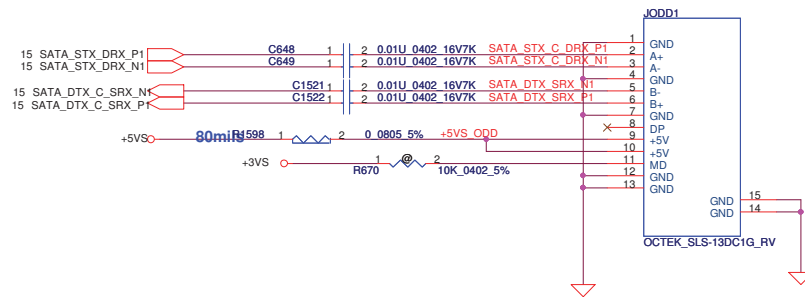
Dr-Bios.com

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SATA HDD Conn.

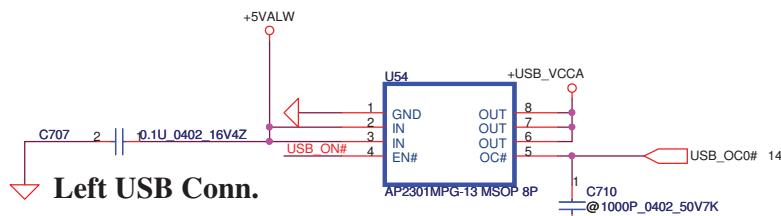


SATA ODD FFC Conn.



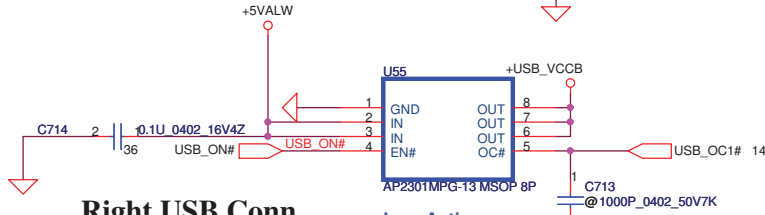
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Issued Date		Deciphered Date		P29-HDD & ODD CONN		Size	Document Number	
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						Date	Wednesday, April 27, 2011	Sheet 33 of 53



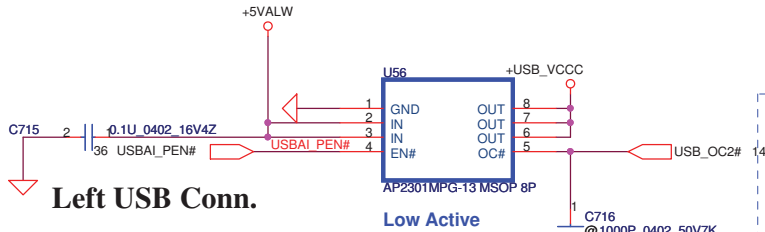
Left USB Conn.

Low Active



Right USB Conn.

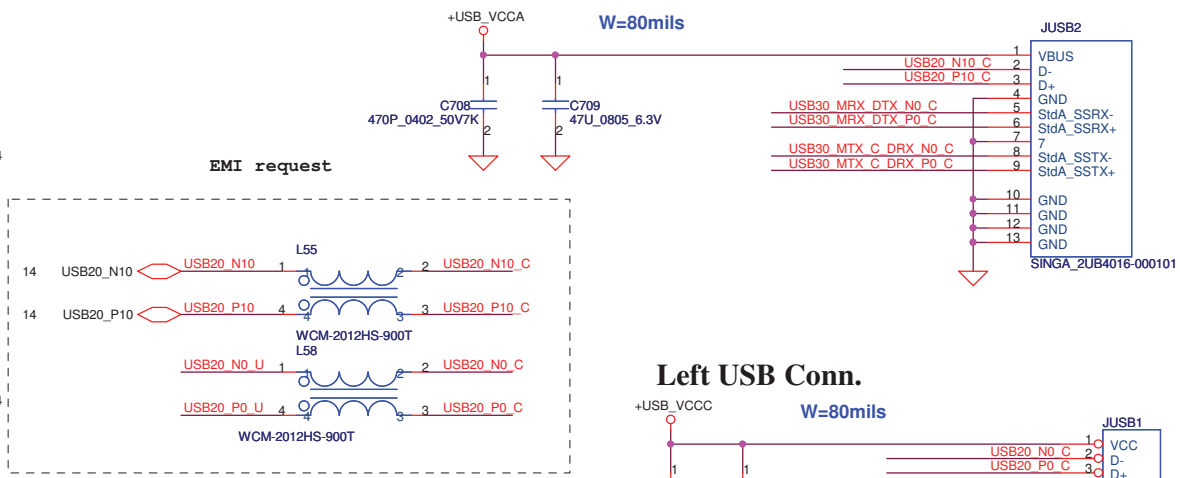
Low Active



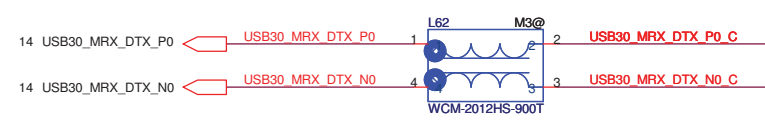
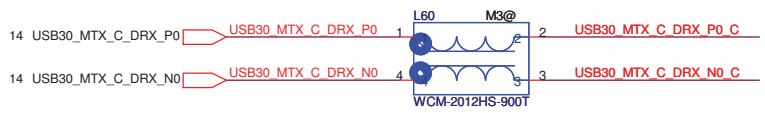
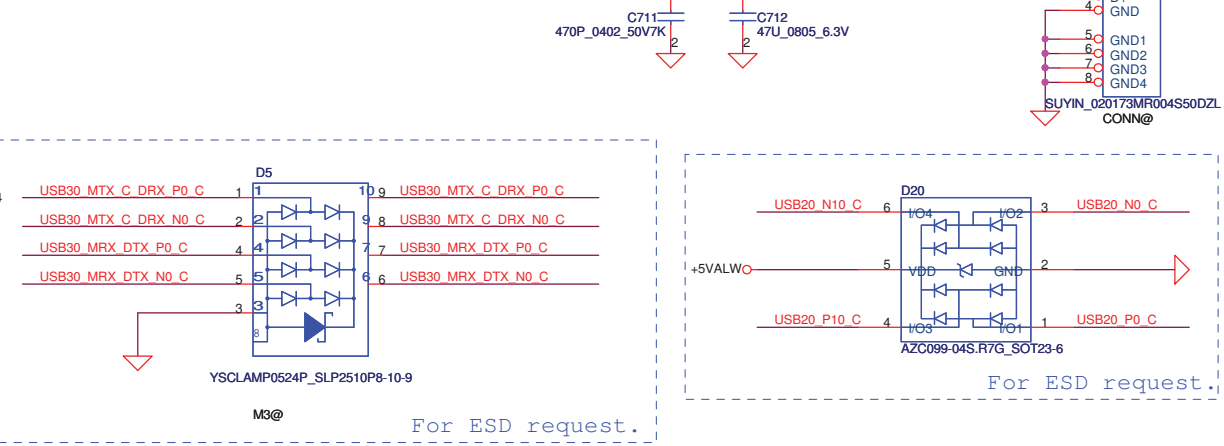
Left USB Conn.

Low Active

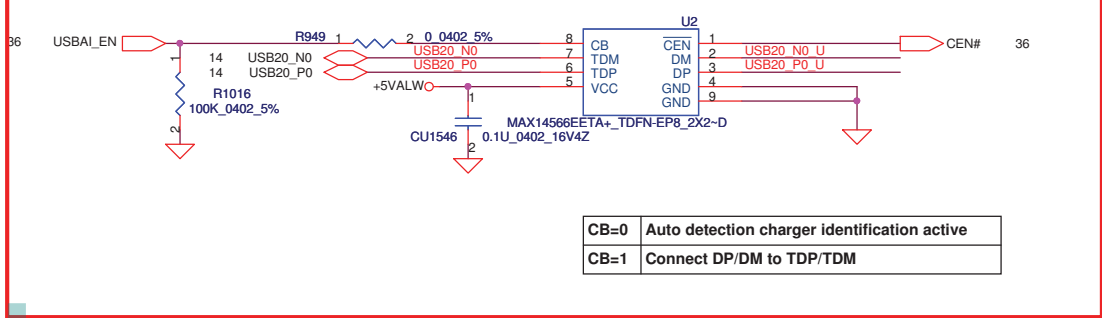
Left USB Conn. W=80mils



Left USB Conn. W=80mils

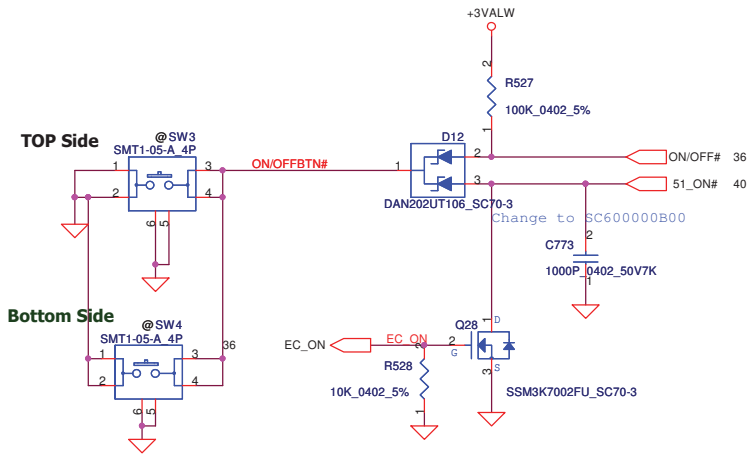


AI CHARGER

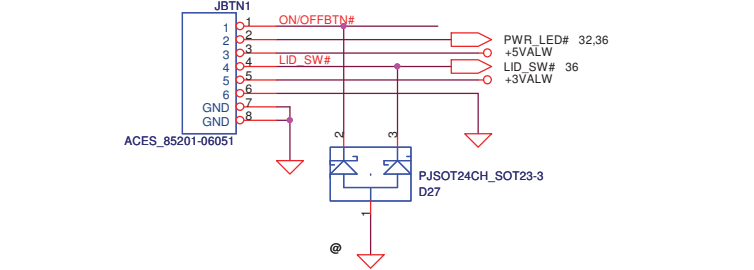
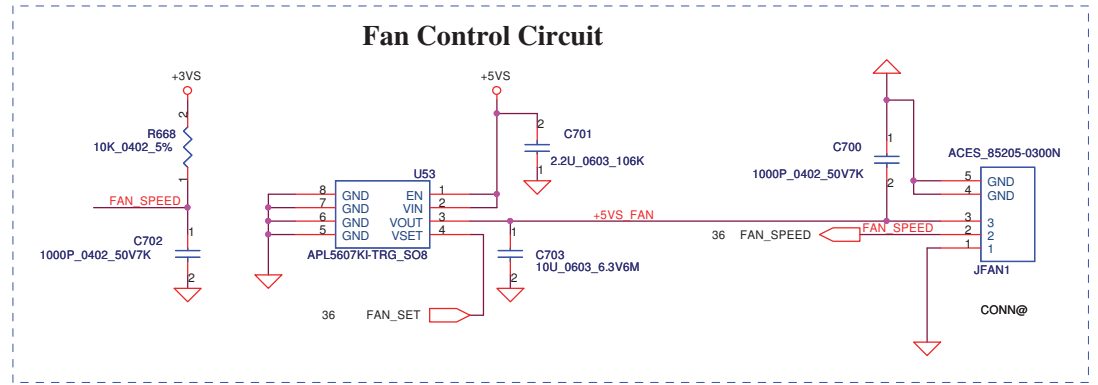


CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

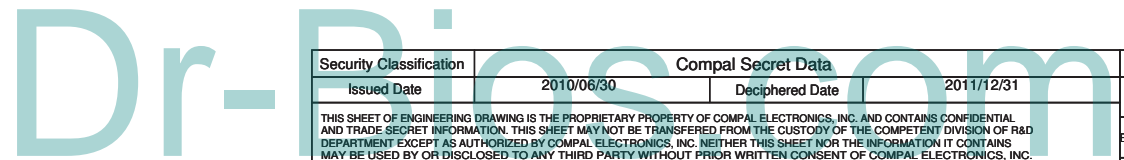
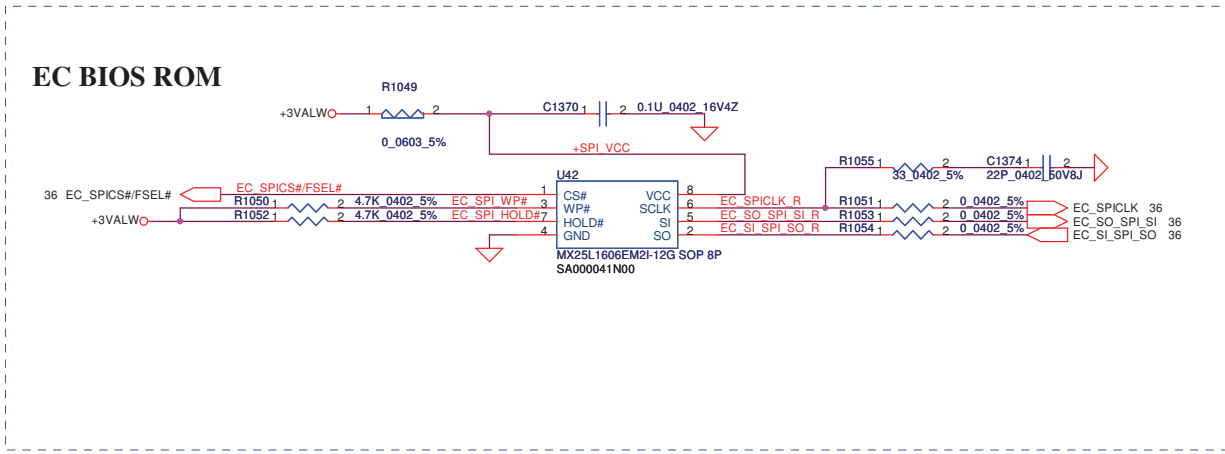
ON/OFF switch Power Button



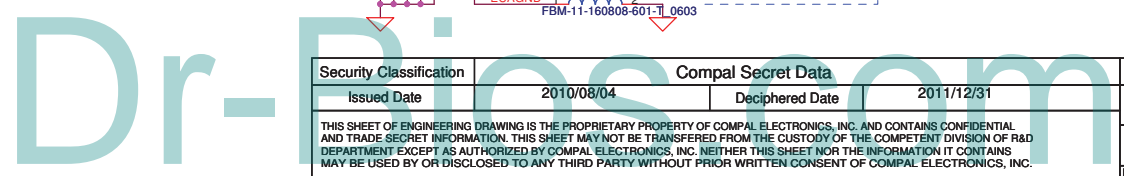
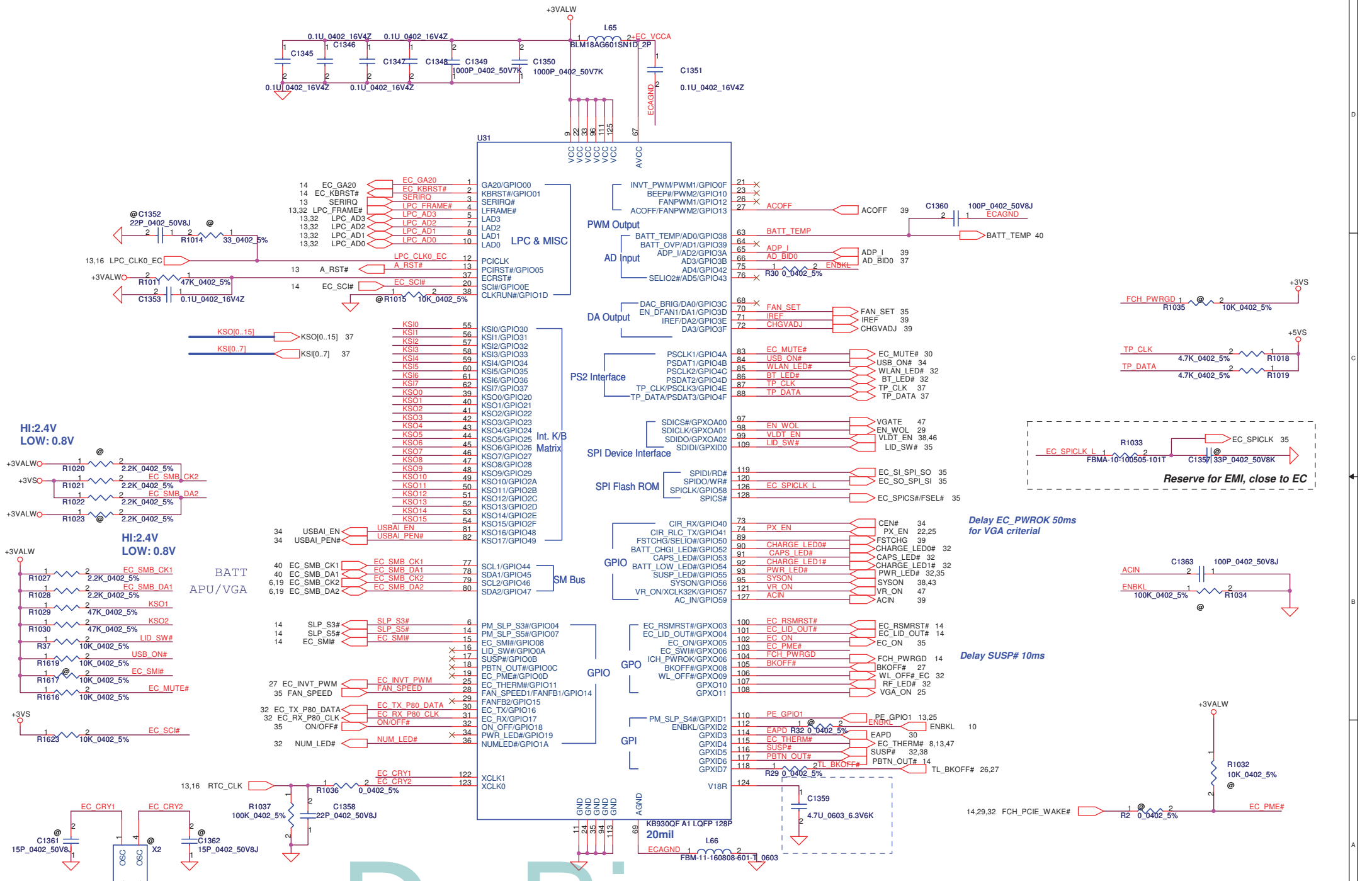
Fan Control Circuit



EC BIOS ROM



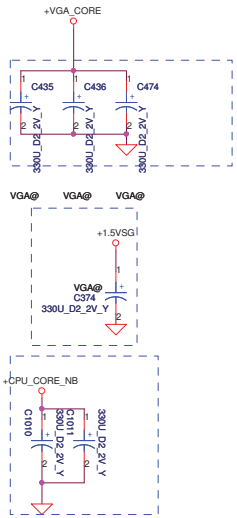
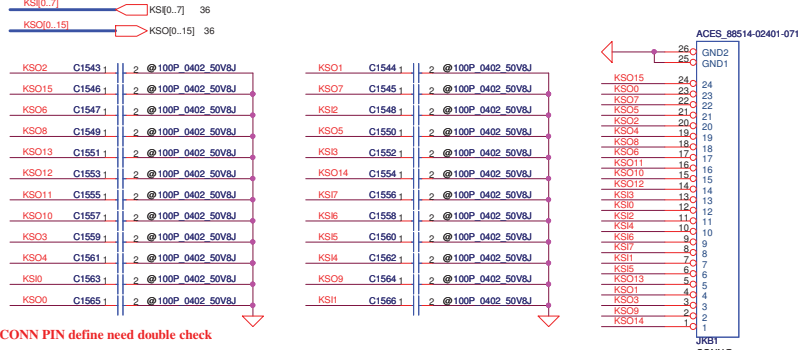
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Issued Date	2010/06/30	Deciphered Date	2011/12/31	Title	
				P31-KB /SW/TP/Lid	
Size	Document Number			Rev	
B	QBL50 LA-7551P			1.0	
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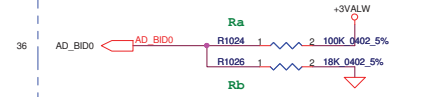
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Issued Date	2010/08/04	Deciphered Date	2011/12/31
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Compal Electronics, Inc.		
Title EC ENE KB930		
Size B	Document Number QBL50 LA-7551P	Rev 1.0
Date Friday, April 29, 2011	Sheet 36	of 53

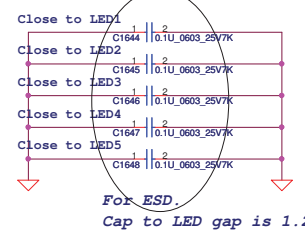
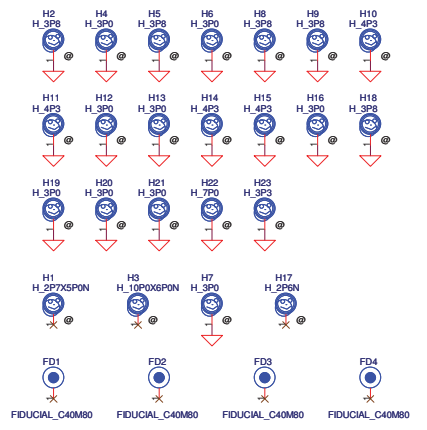
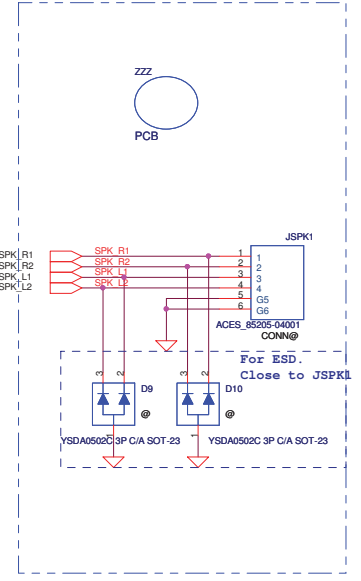
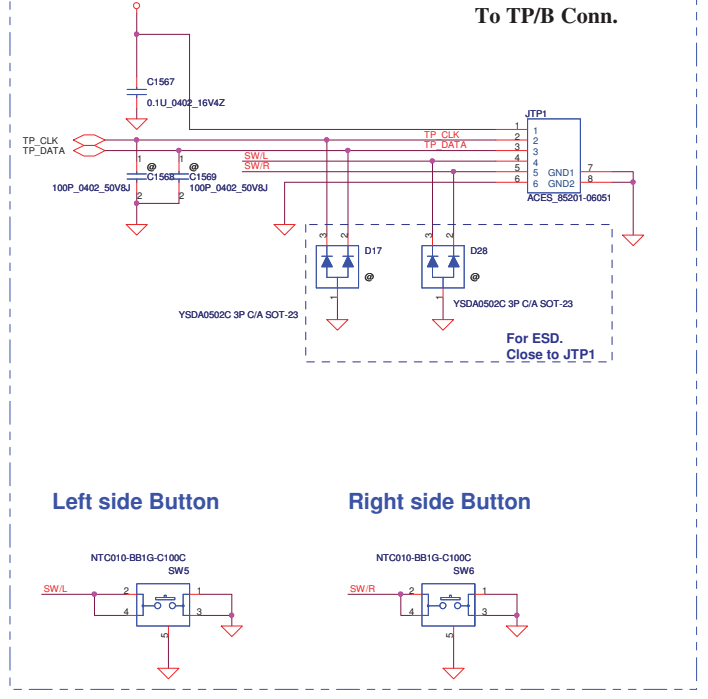
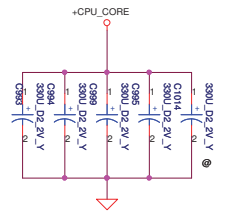
INT_KBD Conn.



ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 MP	100K	18K	0.5V
3	Reserve	100K	33K	0.82V

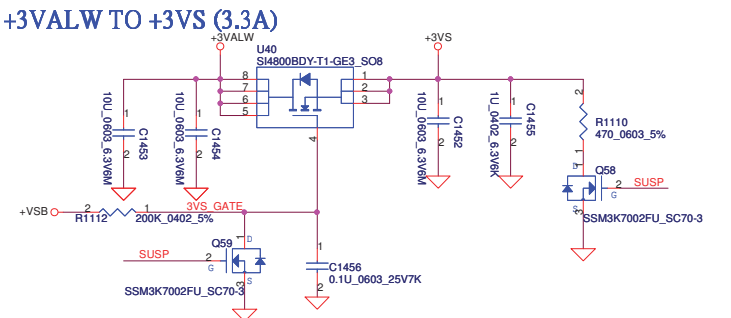
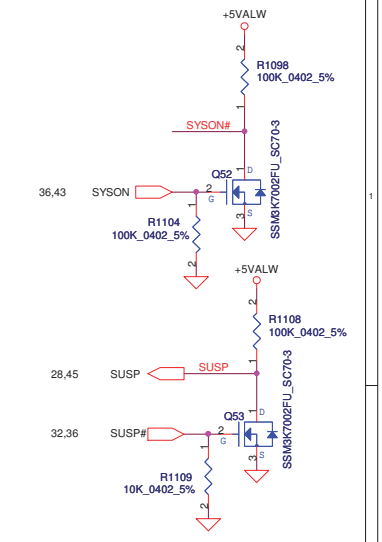
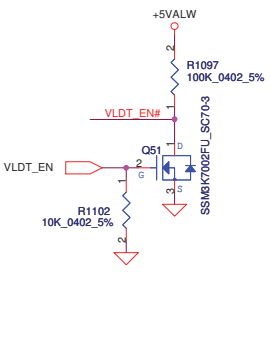
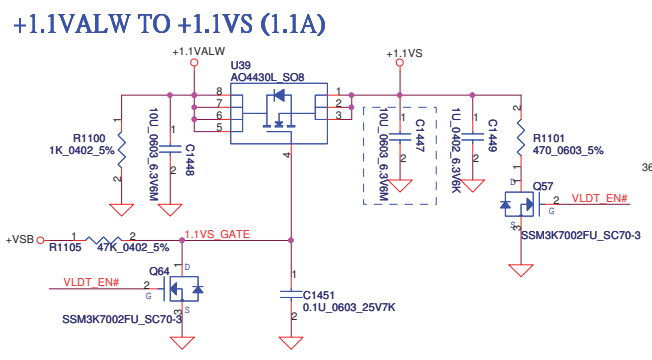
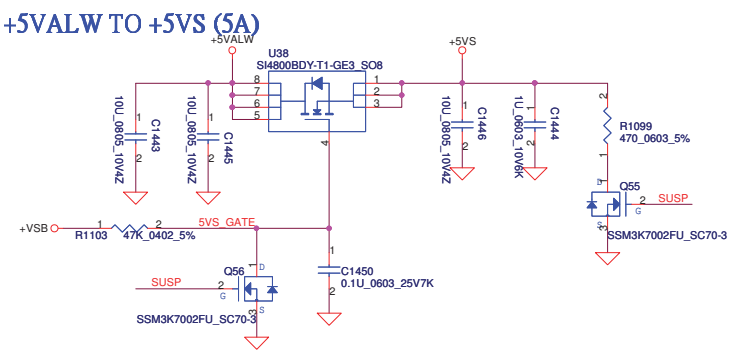


P9 FS1 PWR/GND



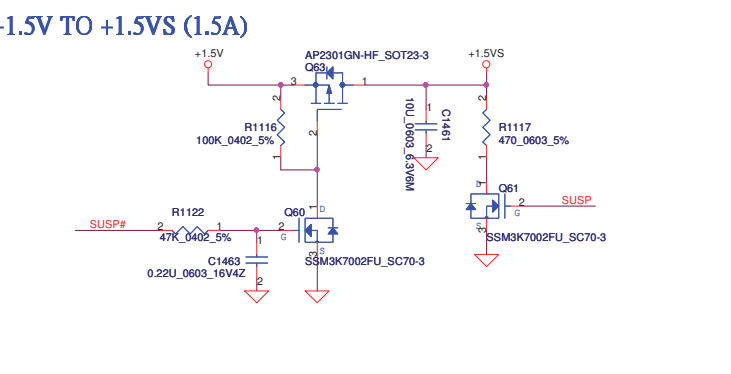
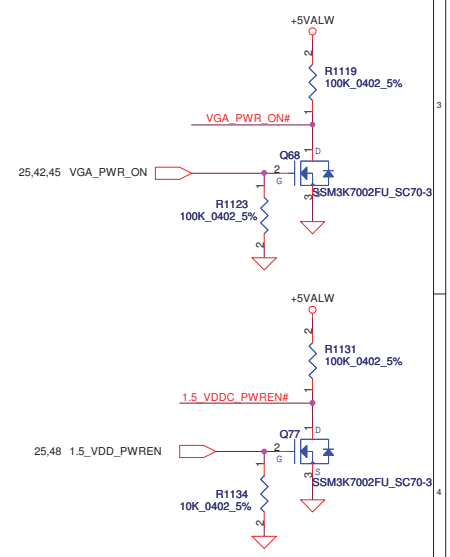
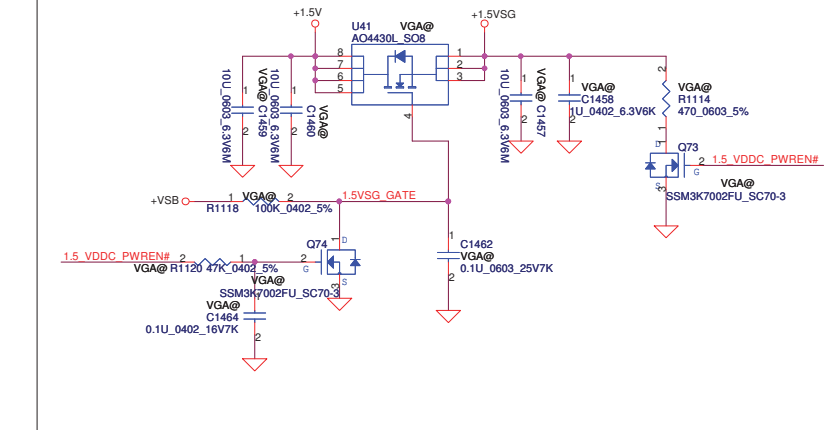
Note: Differential page:
P1,P2,P9,P29,P37
And Power schematic.

Security Classification	Compal Secret Data	Title	
Issued Date	2011/03/04	P33-Other IO/USB (right)	
Deciphered Date	2011/12/31	Size	Document Number
		Customer	QBL50 LA-7551P
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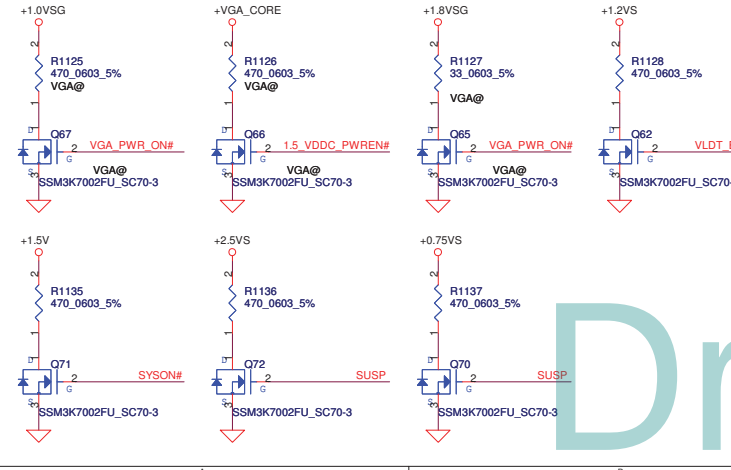
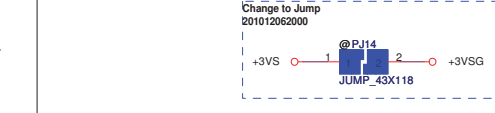


VGA Power

+1.5V to +1.5VSG (1.5A)

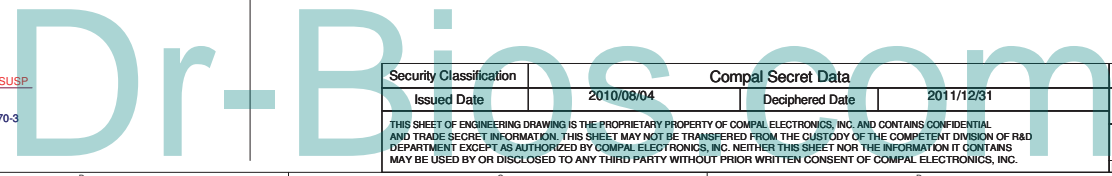


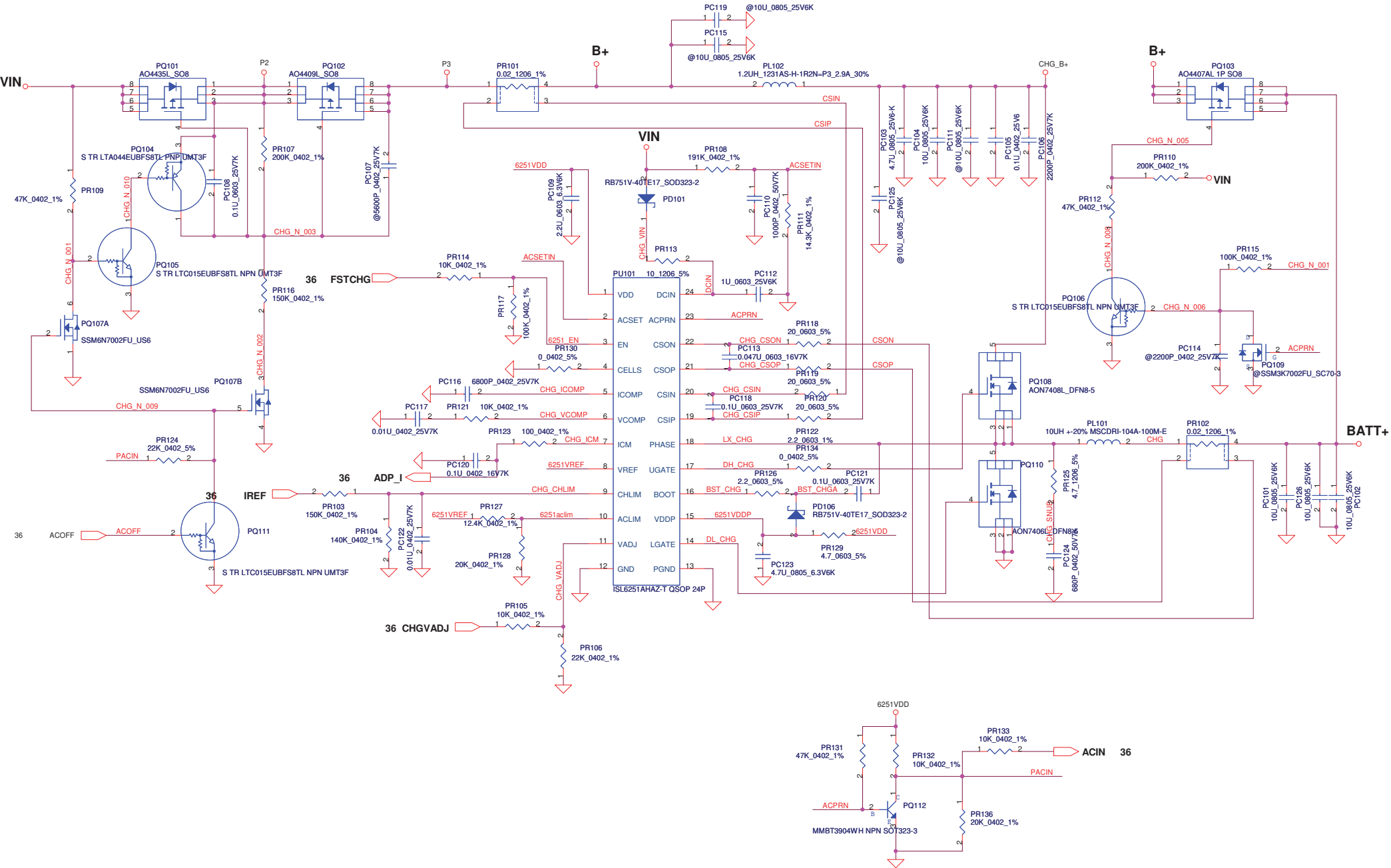
+3VS to +3VSG (3.3A)



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Compal Electronics, Inc.		
DC Interface		
Size B	Document Number	Rev 1.0
QBL50 LA-7551P		
Date:	Wednesday, April 27, 2011	Sheet 38 of 53

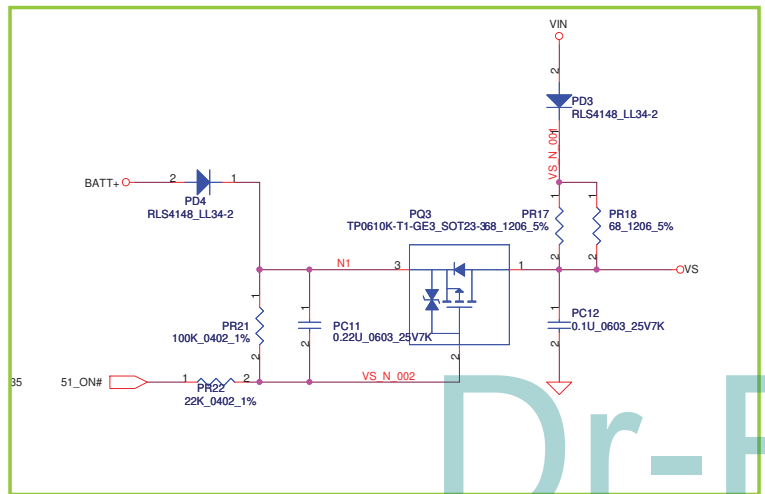
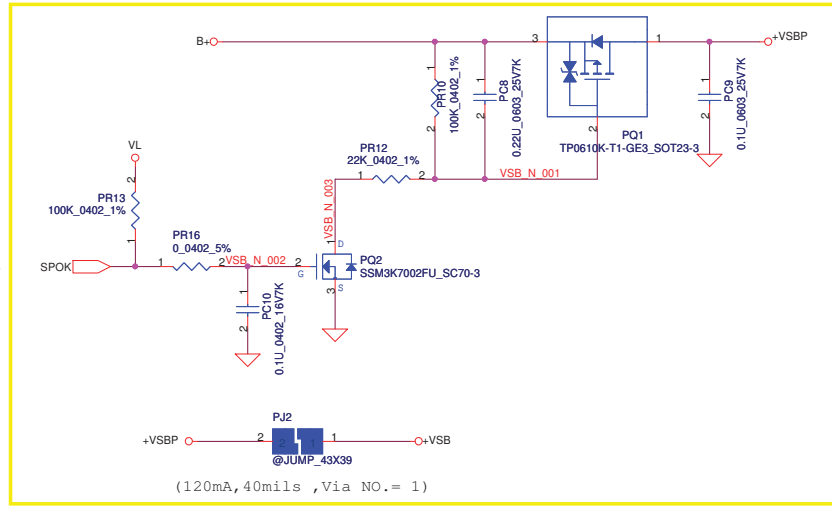
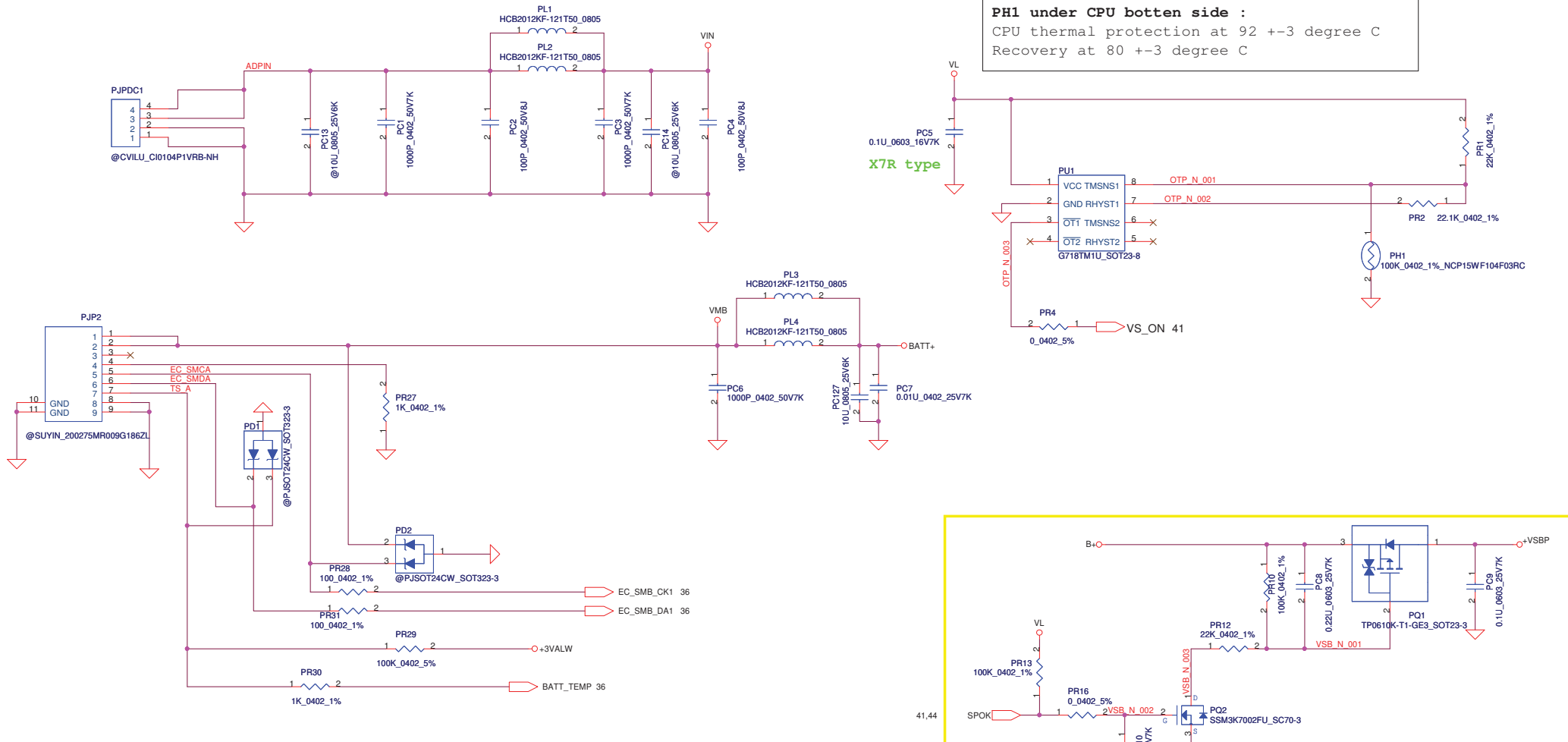




Dr-Bios.com

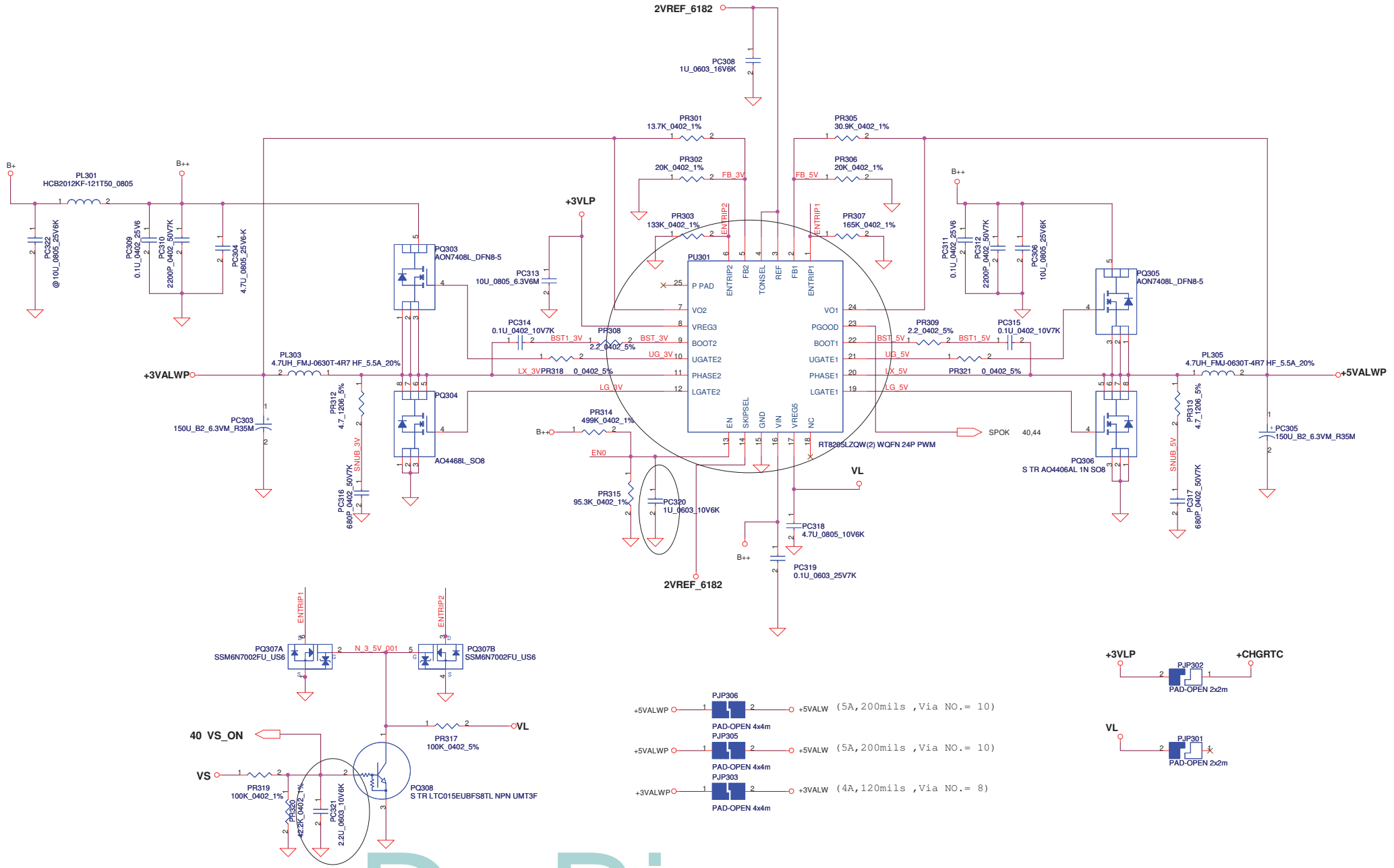
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2011/12/31	Title	
				CHARGER	
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				Date:	Wednesday, April 27, 2011
				Sheet	39 of 53

PH1 under CPU botten side :
 CPU thermal protection at 92 +-3 degree C
 Recovery at 80 +-3 degree C



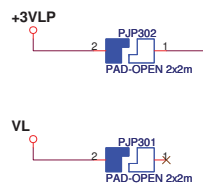
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Issued Date	2009/01/23	Deciphered Date	2011/12/31
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Compal Electronics, Inc.		
Title DCIN / BATT CONN / OTP		
Size	Document Number NCL61 LA-6321P M/B	Rev 1.0
Date:	Wednesday, April 27, 2011	Sheet 40 of 53

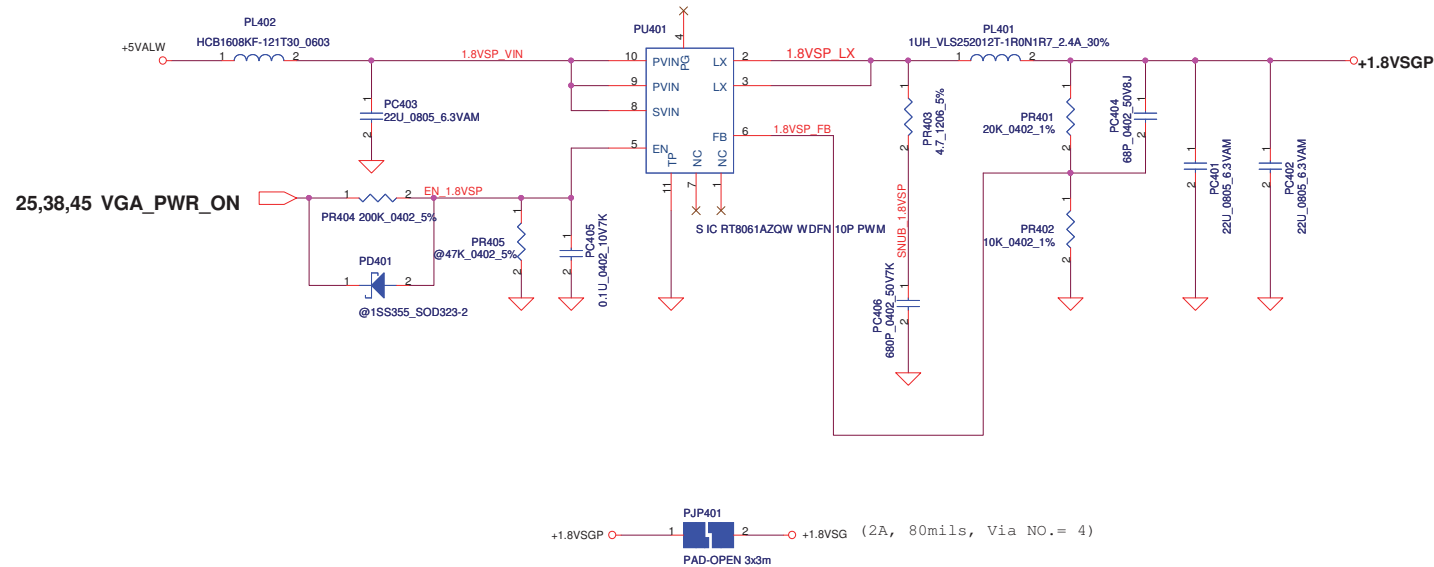


EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

- +5VALWP → PJP306 → +5VALW (5A, 200mils, Via NO. = 10)
- +5VALW → PJP305 → +5VALW (5A, 200mils, Via NO. = 10)
- +3VALWP → PJP303 → +3VALW (4A, 120mils, Via NO. = 8)



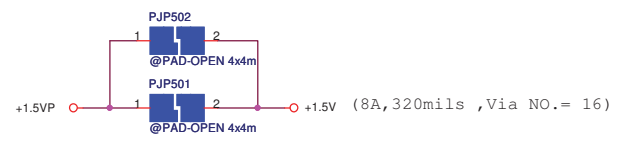
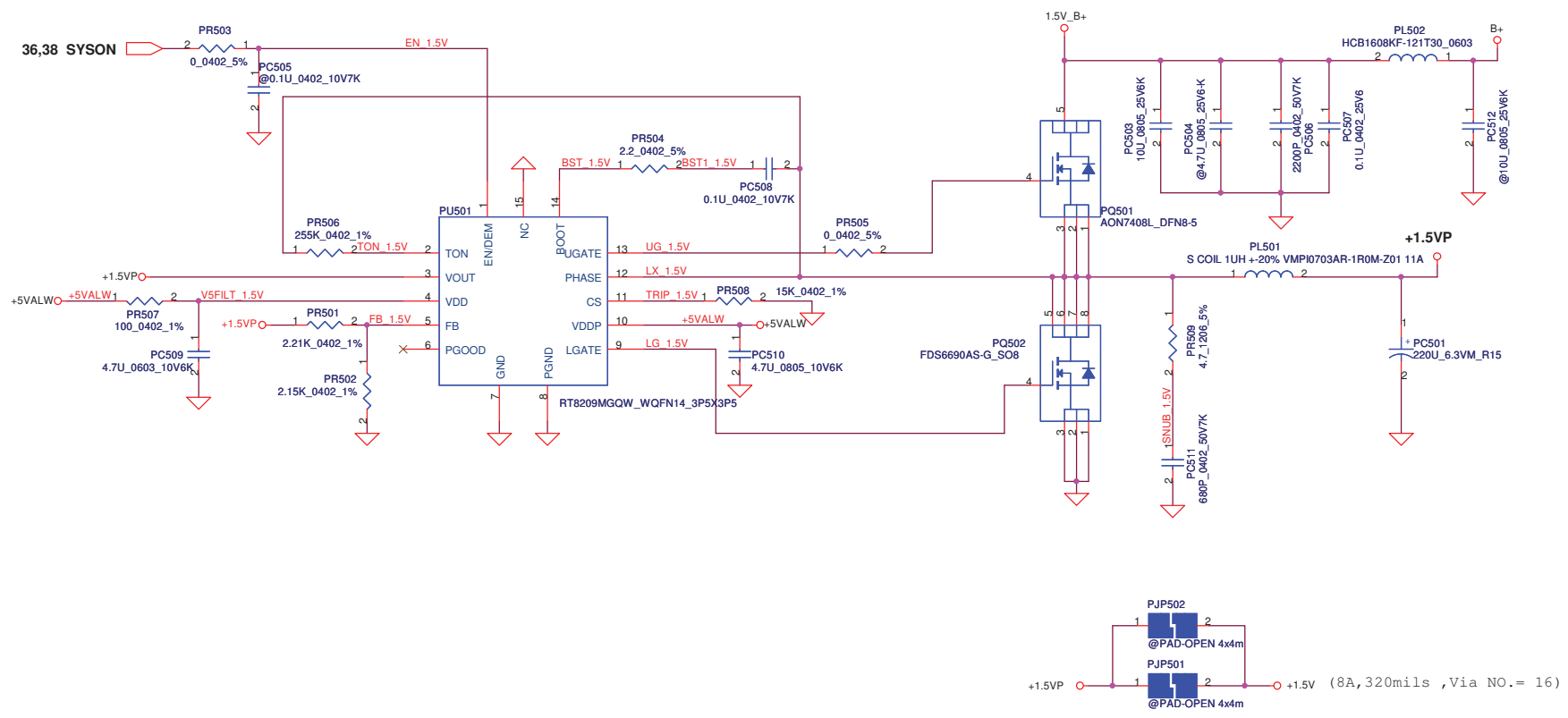
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2011/12/31	3.3VALWP/5VALWP	
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$V_o = 1.8V$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$

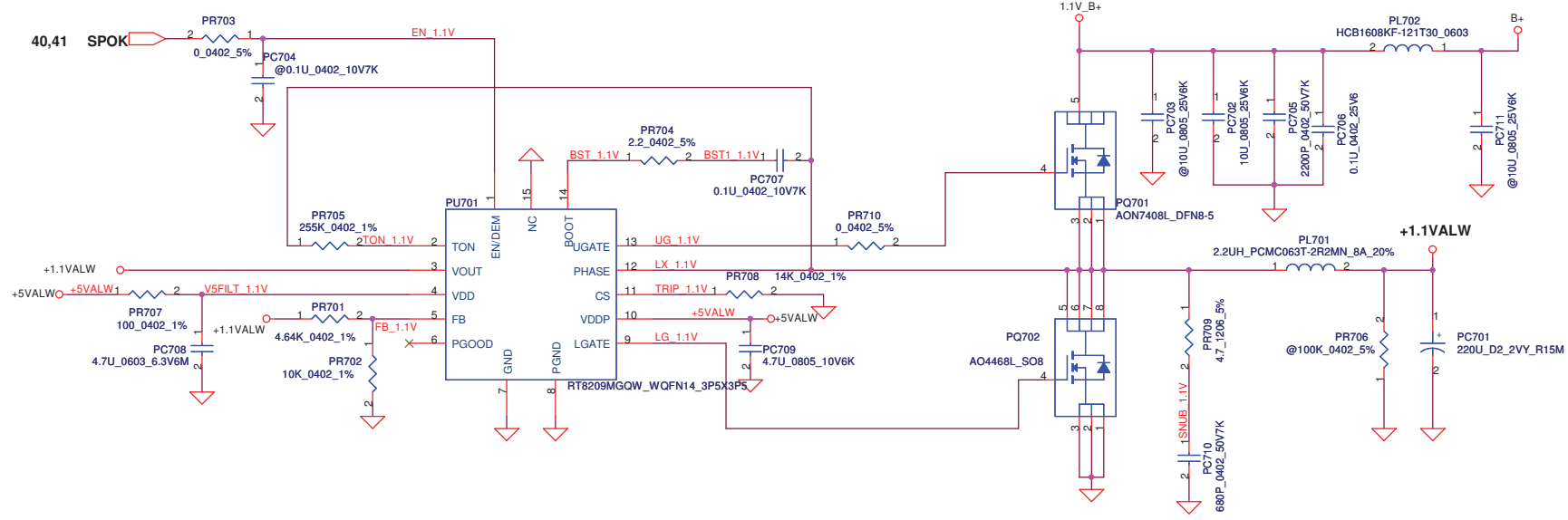
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Size	Document Number	NCL61 LA-6321P M/B		Rev	1.0
Date:	Wednesday, April 27, 2011	Sheet	42	of	53



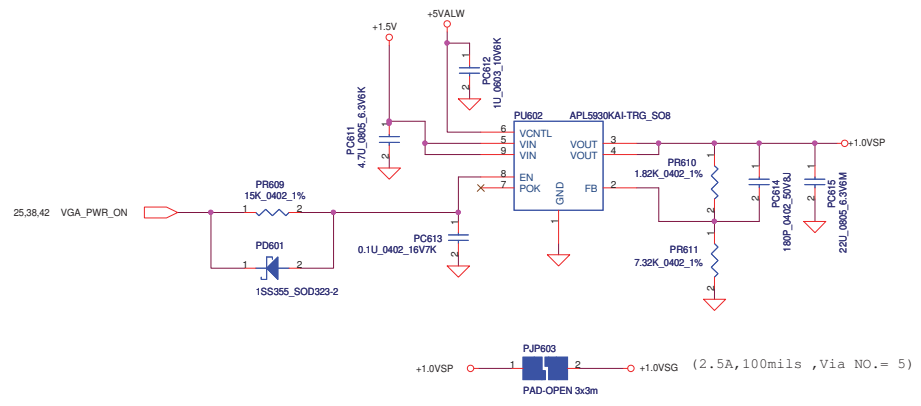
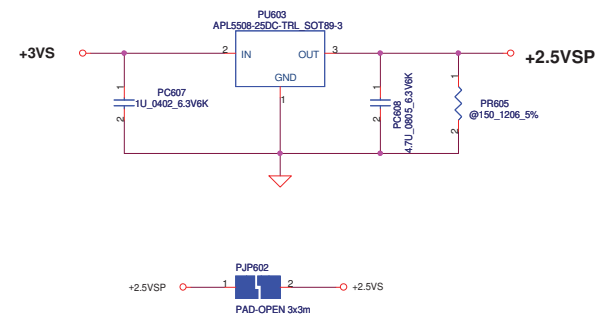
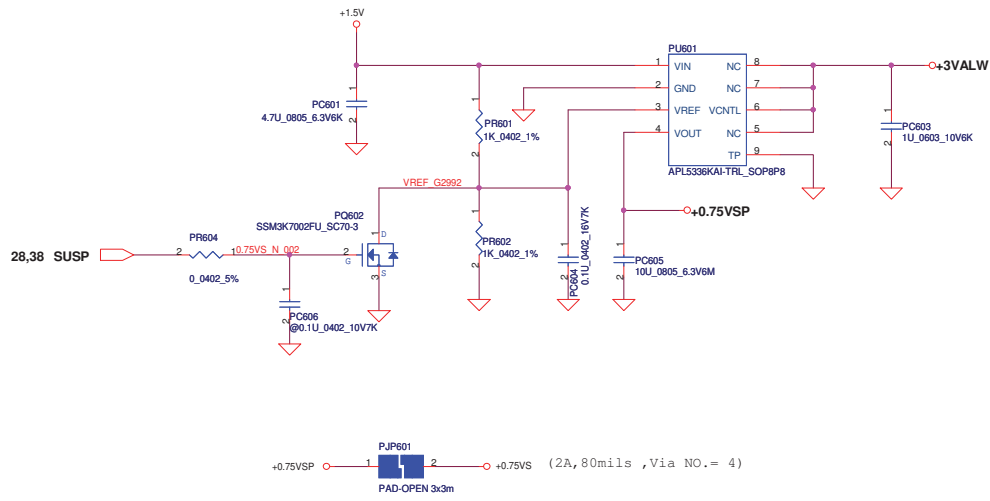
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Issued Date	2007/05/29	Deciphered Date	2011/12/31	Title	
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				Size	Document Number
				Date:	Wednesday, April 27, 2011
				Sheet	43 of 53
				Rev	1.0



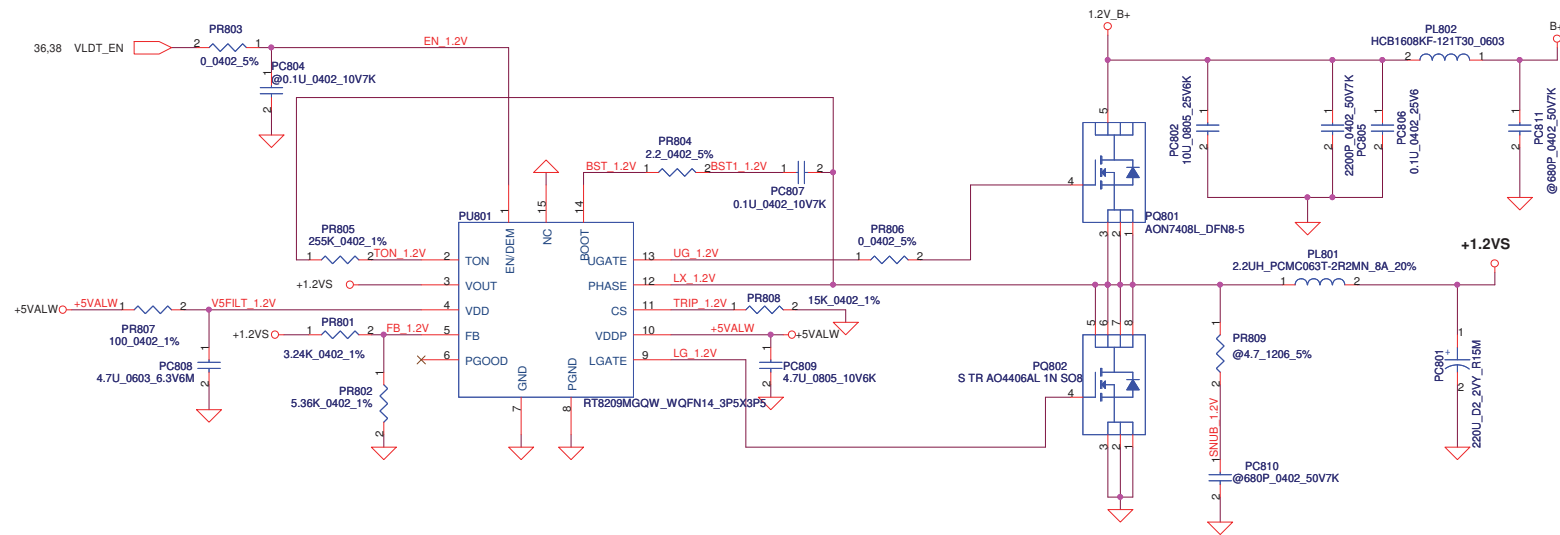
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Issued Date	2009/12/01	Deciphered Date	2011/12/31	Title	PWR+1.1VALWP
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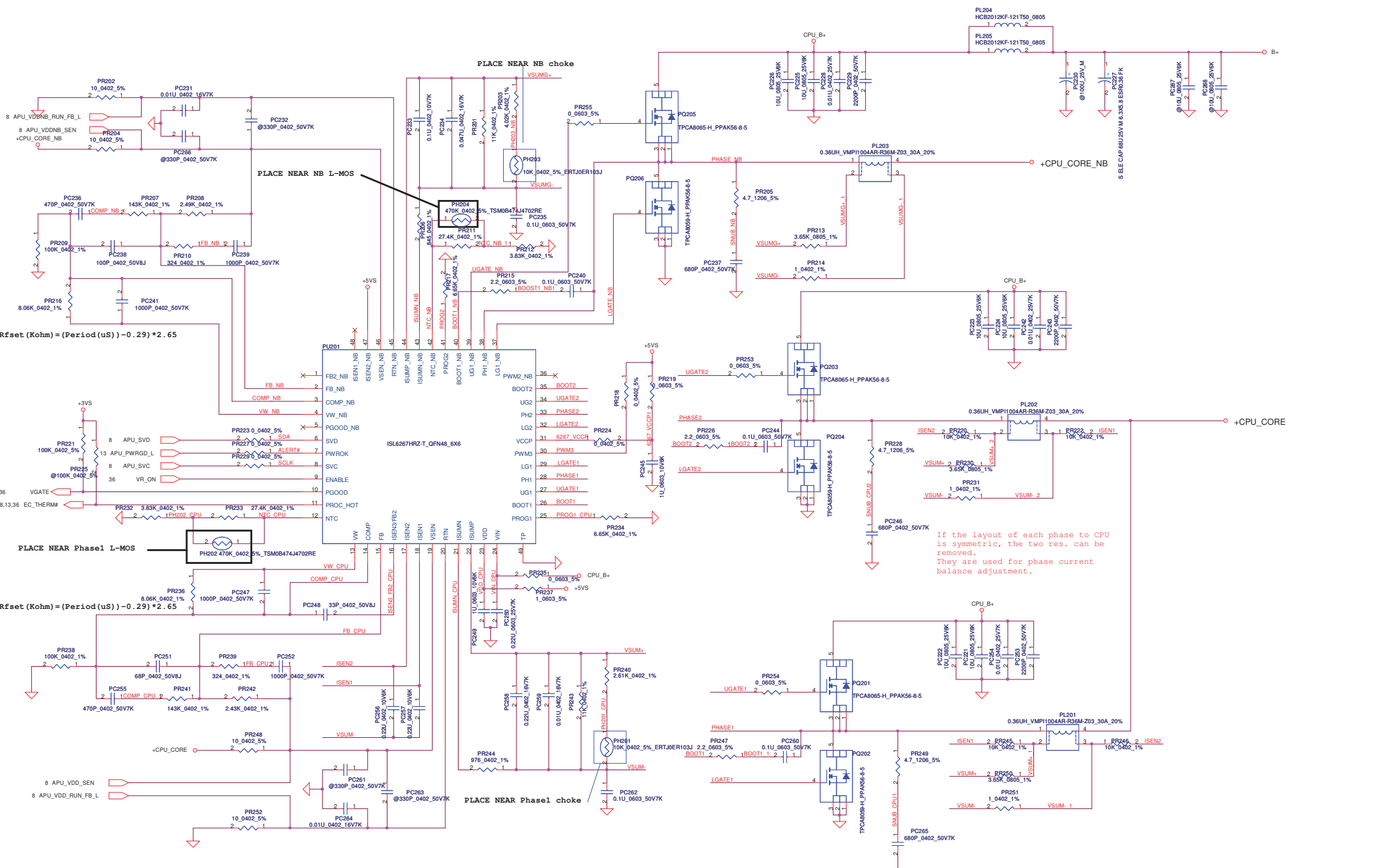
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Issued Date	2006/11/23	Deciphered Date	2011/12/31	Title
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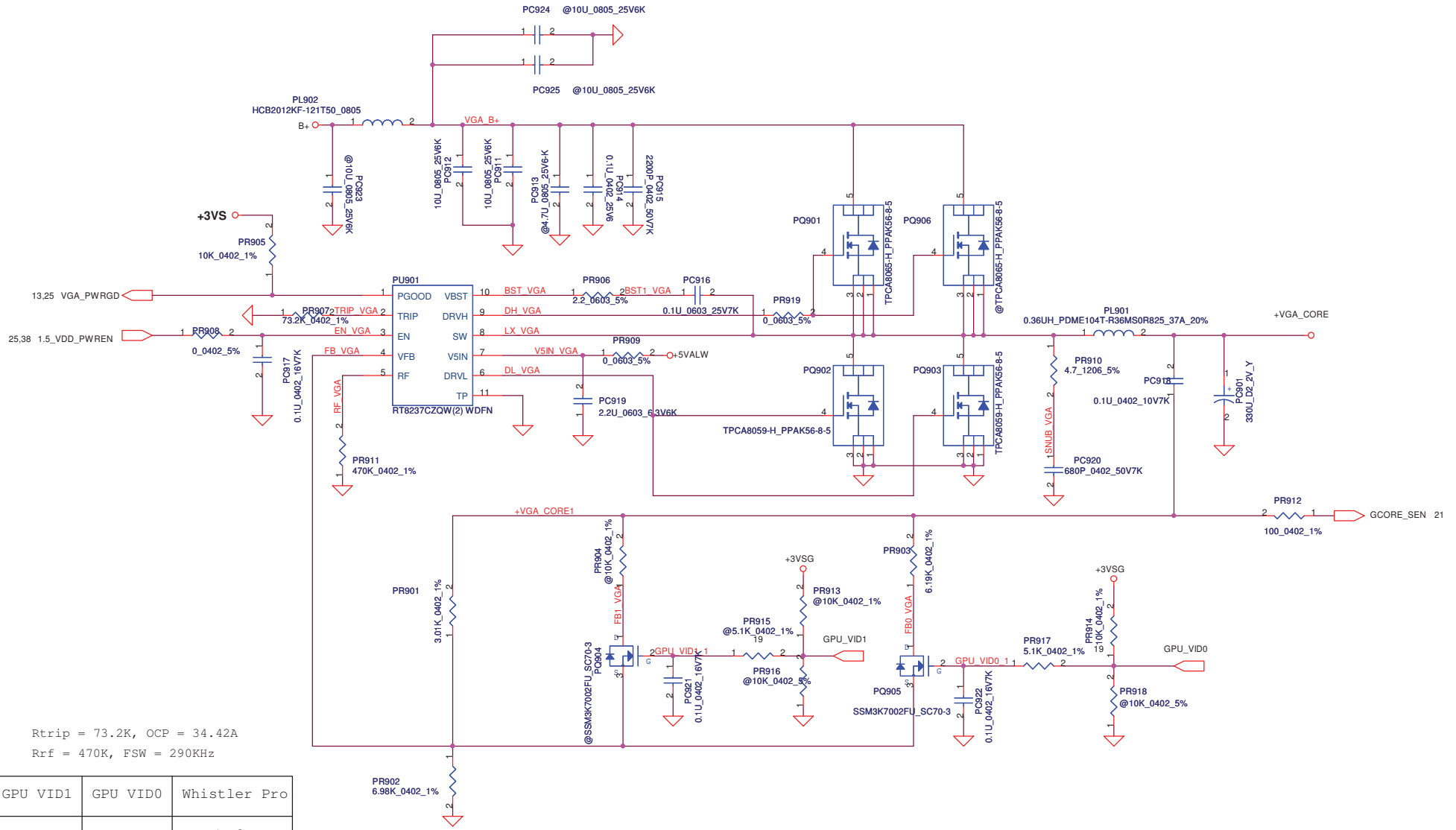
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Issued Date	2009/01/23	Deciphered Date	2011/12/31	Title	+1.2VSP	
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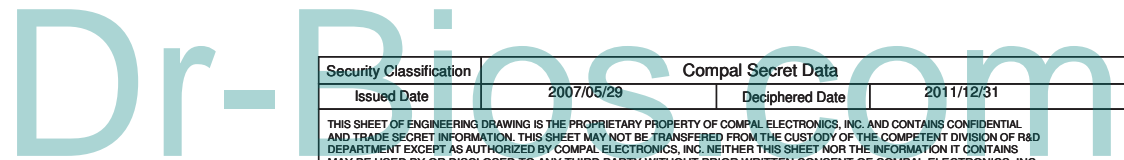
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Title		PWR +CPU_CORE+CPU_CORE_NB	
Size	Document Number	QBL50 LA-7551P	
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Rtrip = 73.2K, OCP = 34.42A
 Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

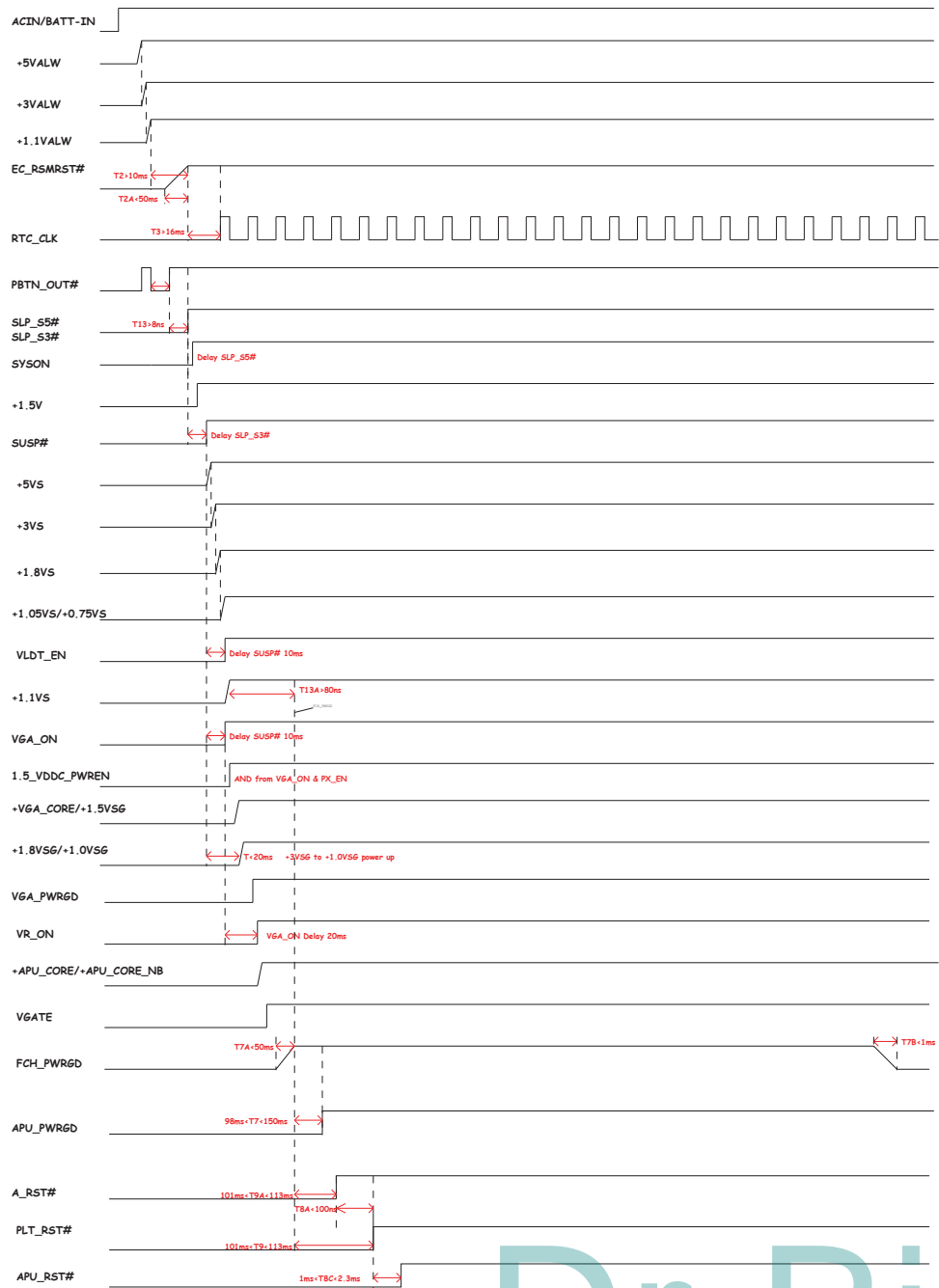


Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Security Classification	Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/09/15	Deciphered Date	2011/12/31	Title	
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				08150 LA-7551P	1.0
				Date	Wednesday, April 27, 2011
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POWER SEQUENCE



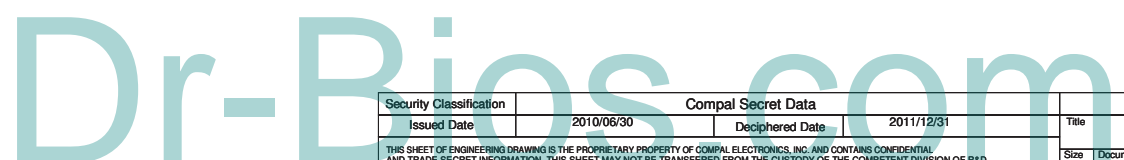
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Item	Value	Unit
Model Name	8150SG	
Revision	1.0	
Created Date	2011/03/11	
Updated Date	2011/03/11	
Author	Dr-Bios.com	
Power Sequence	QML09 LA-7501P	
Page	1 of 1	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD request	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

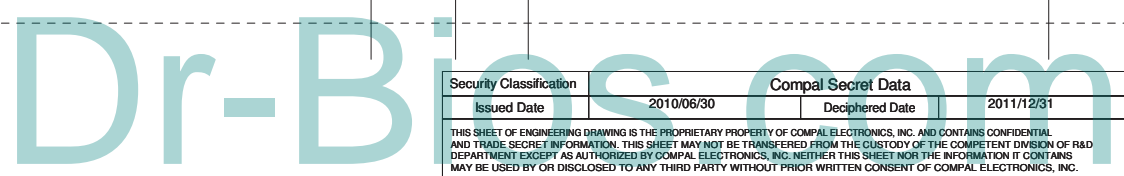
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Size	Document Number	Rev			
Custom	QBL50 LA-7551P	1.0			
Date:	Wednesday, April 27, 2011	Sheet	51	of	53

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI request	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uF	03/29	ER
2		For share ROM request	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI request	0.2	PG#34	D5 change to SC300001Y00 (YSCLAMP0524P)	03/29	ER
4		For Crystal vendor recommend	0.21	PG#13	Y4 change to SJ100007N00 (32.768K 7PF)	04/07	PR
5		For EMI recommend	0.21	PG#29	TS1 change to SP050006F00 (IH-160)	04/07	PR
6		For discharge EA	0.21	PG#38	R1127 change from 470 ohm to 33 ohm	04/07	PR
7		For leakage current	0.21	PG#27	R1644,R1645,Q101 change to install R4,R31 change to un-install	04/07	PR
8		For EMI recommend	0.21	PG#29	C1636 change from 1000P to 120P	04/08	PR
9		For thermal recommend	0.21	PG#19	Add R78, R79, R80, R82	04/18	PR
10		Reserve PX_EN signal	0.21	PG#36	Reserve signal PX_EN to EC pin 74	04/18	PR
11		Swap JDIMM1 & JDIMM2 location	0.21	PG#11 PG#12	Follow ME BOM	04/18	PR
12		Do not use for MP	0.21	PG#35	Del SW3 SW4	04/18	PR
13		Change Board ID to PR10	0.21	PG#37	Change R1036 to 18k	04/18	PR
14		For DFB request del co-lay schematic	0.21	PG#34	Del R672~R675, R664~R667	04/18	PR
15		For EMI request	0.22	PG#29	ADD D7	04/19	PR
16		For EMI request	1.0	PG#13	unstuff C1193	04/25	PR
17		For Customer change FCH P/N	1.0	PG#13 ~17	location U25, for M2 change to SA000042C80, M3 change to SA000043ID0	04/25	PR
18		For ESD request	1.0	PG#32	R628,R629,R678,R679,R680,R681 change from 0ohm to 33ohm & Add 1uF for C560,C568,C569,C570,C573,C571	04/27	PR
19							
20							
21							
22							
23							
24							
25							
26							
27							



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				Custom	HW-PIR
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase																																																																																																																																																																																																																																																																																																																		
1		For MP cost down	1.0		As picture	03/15	PR																																																																																																																																																																																																																																																																																																																		
2					<table border="1"> <thead> <tr> <th>Reference</th> <th>Value</th> <th>Source Part</th> <th>Source Library</th> <th>Page</th> <th>Schematic</th> </tr> </thead> <tbody> <tr><td>R22</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R23</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R24</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R26</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R27</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R28</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R81</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P14-HUD...</td><td>SCHEMA...</td></tr> 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<tr><td>R606</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P08-FS1 ...</td><td>SCHEMA...</td></tr> <tr><td>R608</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P08-FS1 ...</td><td>SCHEMA...</td></tr> <tr><td>R611</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P08-FS1 ...</td><td>SCHEMA...</td></tr> <tr><td>R647</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P29-LAN ...</td><td>SCHEMA...</td></tr> <tr><td>R912</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P16-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R945</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R1291</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P26-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R1575</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P32-Mini...</td><td>SCHEMA...</td></tr> <tr><td>R1577</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P32-Mini...</td><td>SCHEMA...</td></tr> <tr><td>R1634</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R1635</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R1636</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R1641</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R1651</td><td>0_0402_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R19</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R20</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R25</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R560</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P29-LAN ...</td><td>SCHEMA...</td></tr> <tr><td>R658</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P29-LAN ...</td><td>SCHEMA...</td></tr> <tr><td>R1049</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P35-FAN ...</td><td>SCHEMA...</td></tr> <tr><td>R1145</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R1148</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R1534</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P30-HD ...</td><td>SCHEMA...</td></tr> <tr><td>R1537</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P30-HD ...</td><td>SCHEMA...</td></tr> <tr><td>R1560</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P31-RTS...</td><td>SCHEMA...</td></tr> <tr><td>R1643</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R1650</td><td>0_0603_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P27-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R570</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P26-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R607</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P26-LVD...</td><td>SCHEMA...</td></tr> <tr><td>R937</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R938</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R941</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P17-HUD...</td><td>SCHEMA...</td></tr> <tr><td>R1531</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P30-HD ...</td><td>SCHEMA...</td></tr> <tr><td>R1595</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P33-HDD...</td><td>SCHEMA...</td></tr> <tr><td>R1598</td><td>0_0805_5%</td><td>R-SHORT</td><td>X\CIS_SYMB...</td><td>P33-HDD...</td><td>SCHEMA...</td></tr> </tbody> </table>	Reference	Value	Source Part	Source Library	Page	Schematic	R22	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R23	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R24	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R26	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R27	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R28	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R81	0_0402_5%	R-SHORT	X\CIS_SYMB...	P14-HUD...	SCHEMA...	R483	0_0402_5%	R-SHORT	X\CIS_SYMB...	P23-VRA...	SCHEMA...	R485	0_0402_5%	R-SHORT	X\CIS_SYMB...	P23-VRA...	SCHEMA...	R511	0_0402_5%	R-SHORT	X\CIS_SYMB...	P24-VRA...	SCHEMA...	R513	0_0402_5%	R-SHORT	X\CIS_SYMB...	P24-VRA...	SCHEMA...	R537	0_0402_5%	R-SHORT	X\CIS_SYMB...	P06-FS1 ...	SCHEMA...	R538	0_0402_5%	R-SHORT	X\CIS_SYMB...	P06-FS1 ...	SCHEMA...	R591	0_0402_5%	R-SHORT	X\CIS_SYMB...	P08-FS1 ...	SCHEMA...	R598	0_0402_5%	R-SHORT	X\CIS_SYMB...	P08-FS1 ...	SCHEMA...	R606	0_0402_5%	R-SHORT	X\CIS_SYMB...	P08-FS1 ...	SCHEMA...	R608	0_0402_5%	R-SHORT	X\CIS_SYMB...	P08-FS1 ...	SCHEMA...	R611	0_0402_5%	R-SHORT	X\CIS_SYMB...	P08-FS1 ...	SCHEMA...	R647	0_0402_5%	R-SHORT	X\CIS_SYMB...	P29-LAN ...	SCHEMA...	R912	0_0402_5%	R-SHORT	X\CIS_SYMB...	P16-HUD...	SCHEMA...	R945	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R1291	0_0402_5%	R-SHORT	X\CIS_SYMB...	P26-LVD...	SCHEMA...	R1575	0_0402_5%	R-SHORT	X\CIS_SYMB...	P32-Mini...	SCHEMA...	R1577	0_0402_5%	R-SHORT	X\CIS_SYMB...	P32-Mini...	SCHEMA...	R1634	0_0402_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R1635	0_0402_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R1636	0_0402_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R1641	0_0402_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R1651	0_0402_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R19	0_0603_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R20	0_0603_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R25	0_0603_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R560	0_0603_5%	R-SHORT	X\CIS_SYMB...	P29-LAN ...	SCHEMA...	R658	0_0603_5%	R-SHORT	X\CIS_SYMB...	P29-LAN ...	SCHEMA...	R1049	0_0603_5%	R-SHORT	X\CIS_SYMB...	P35-FAN ...	SCHEMA...	R1145	0_0603_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R1148	0_0603_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R1534	0_0603_5%	R-SHORT	X\CIS_SYMB...	P30-HD ...	SCHEMA...	R1537	0_0603_5%	R-SHORT	X\CIS_SYMB...	P30-HD ...	SCHEMA...	R1560	0_0603_5%	R-SHORT	X\CIS_SYMB...	P31-RTS...	SCHEMA...	R1643	0_0603_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R1650	0_0603_5%	R-SHORT	X\CIS_SYMB...	P27-LVD...	SCHEMA...	R570	0_0805_5%	R-SHORT	X\CIS_SYMB...	P26-LVD...	SCHEMA...	R607	0_0805_5%	R-SHORT	X\CIS_SYMB...	P26-LVD...	SCHEMA...	R937	0_0805_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R938	0_0805_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R941	0_0805_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...	R1531	0_0805_5%	R-SHORT	X\CIS_SYMB...	P30-HD ...	SCHEMA...	R1595	0_0805_5%	R-SHORT	X\CIS_SYMB...	P33-HDD...	SCHEMA...	R1598	0_0805_5%	R-SHORT	X\CIS_SYMB...	P33-HDD...	SCHEMA...		
Reference	Value	Source Part	Source Library	Page	Schematic																																																																																																																																																																																																																																																																																																																				
R22	0_0402_5%	R-SHORT	X\CIS_SYMB...	P17-HUD...	SCHEMA...																																																																																																																																																																																																																																																																																																																				
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