

Compal Confidential

QBL60 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-04-25

LA-7552P REV: 1.0

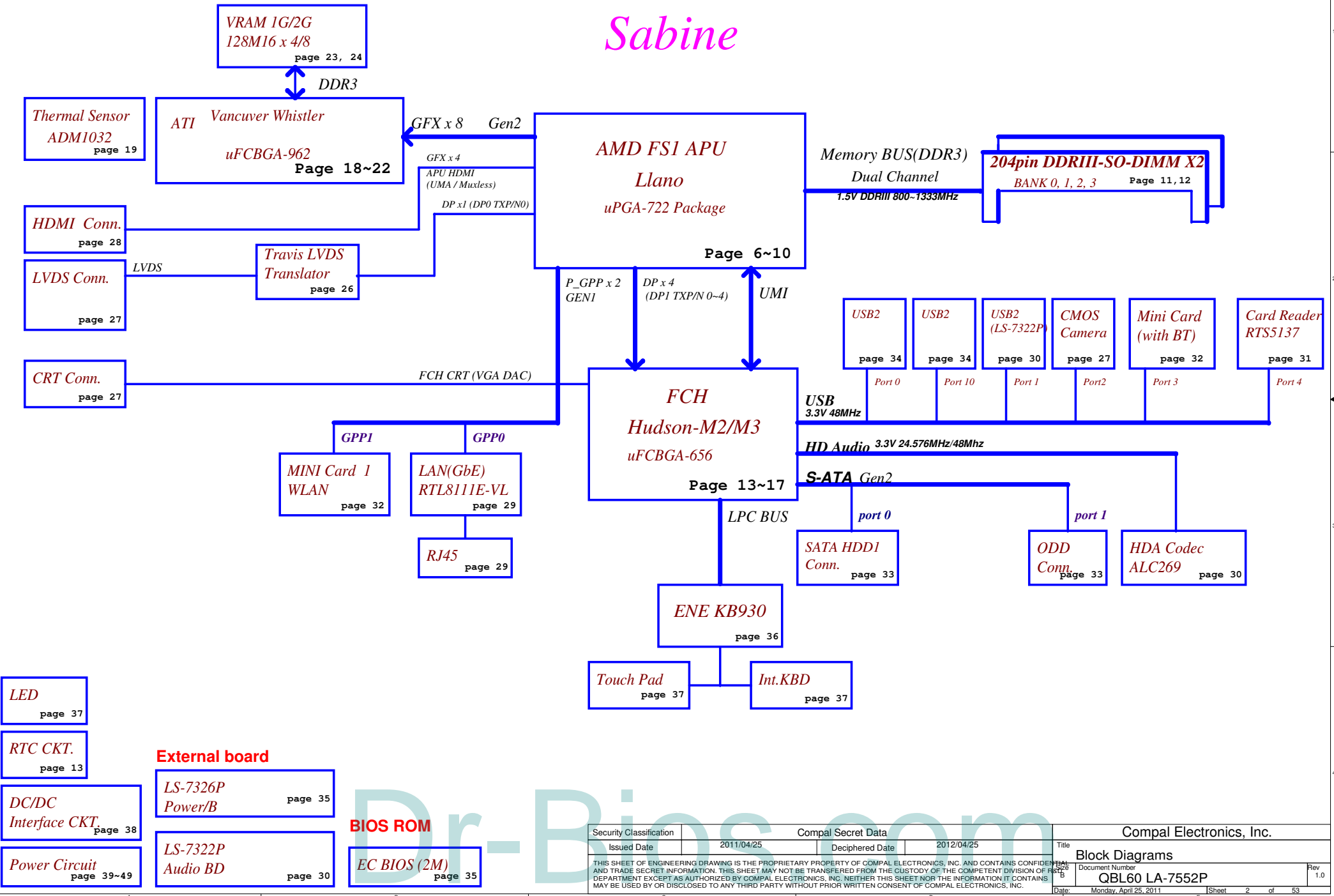
Dr-Bios.com

Security Classification	Compal Secret Data		Title		
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				QBL60 LA-7552P	1.0
				Date: Monday, April 25, 2011	Sheet 1 of 53

Compal Confidential

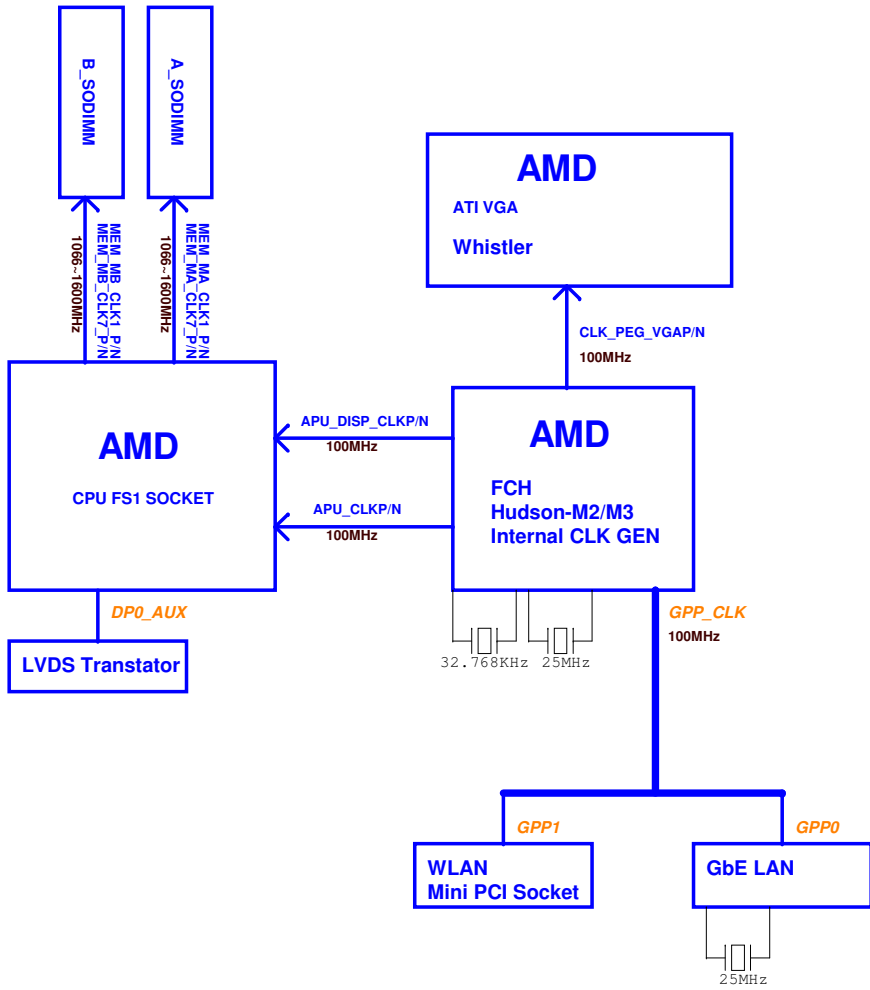
Model Name : QBL60

Sabine

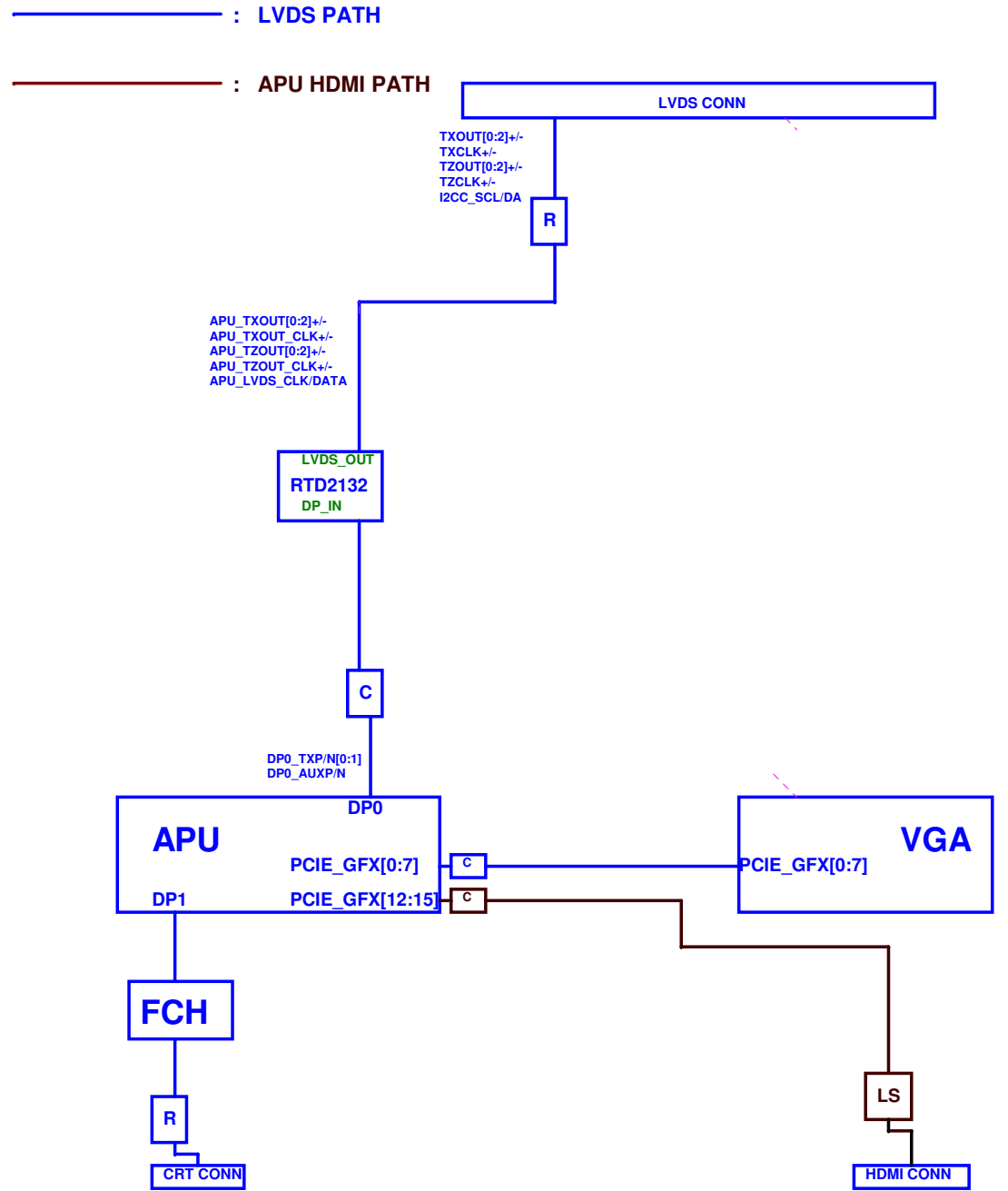


Security Classification	2011/04/25	Compal Secret Data	Deciphered Date	2012/04/25	Title	Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Document Number	Block Diagrams		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date	Monday, April 25, 2011	Sheet	2 of 53
					Rev	1.0	
					Model Name	QBL60 LA-7552P	

CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



Security Classification	Compal Secret Data		Title	CLOCK / DISPLAY DISTRIBUTION	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	1.0
Date:	Monday, April 25, 2011	Sheet	3	of	53

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			(APU)		
			RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

FCH SM Bus 1 address

Device	Address	HEX	Device	Address	HEX

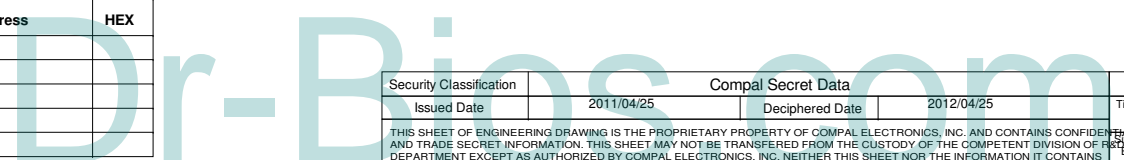
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

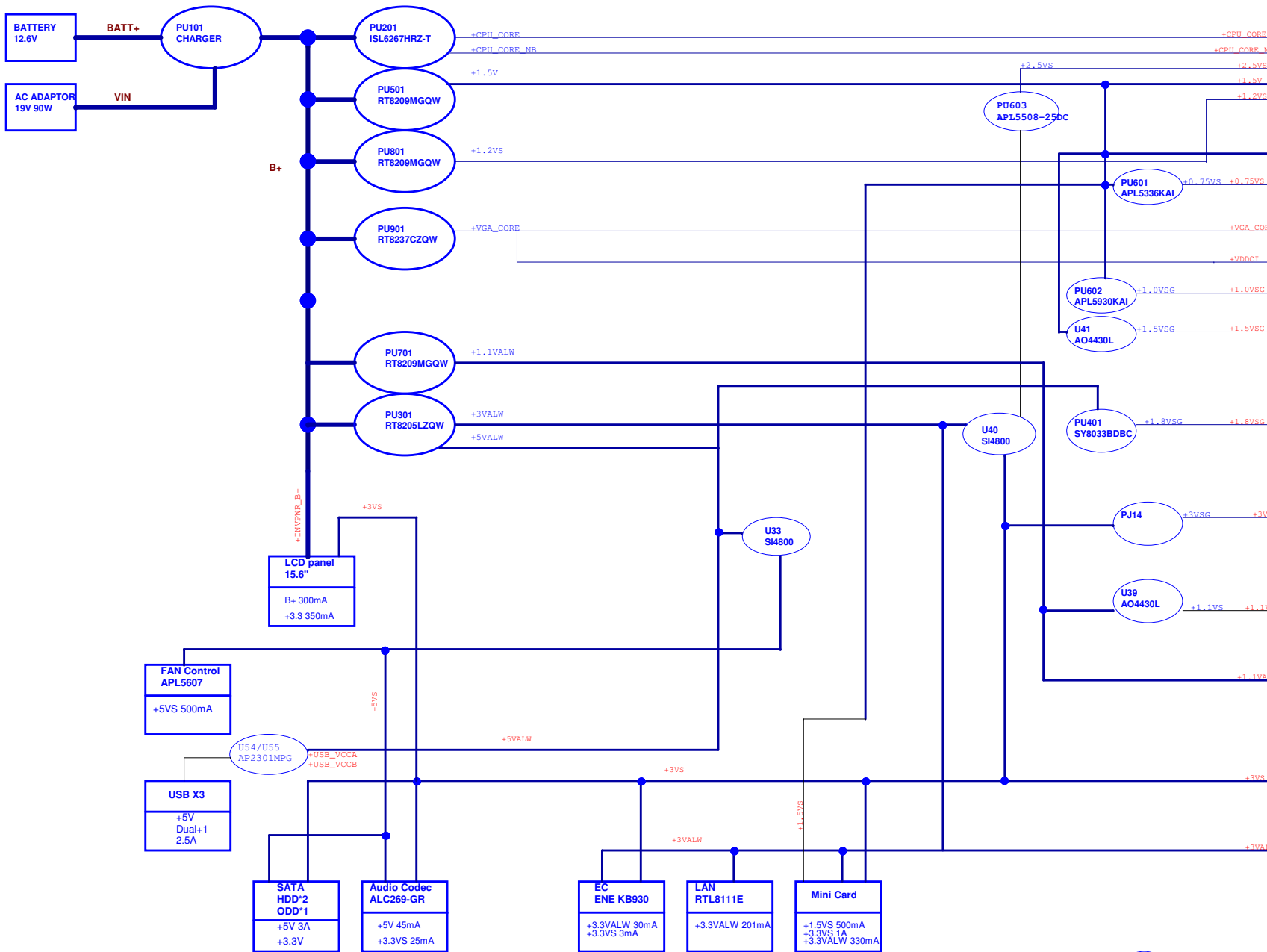
BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B



BOM Config



Security Classification	2011/04/25	Compal Secret Data	Deciphered Date	2012/04/25	Title	Compal Electronics, Inc.
Issued Date					Notes List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT TO ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Document Number
						QBL60 LA-7552P
						Rev 1.0
Date: Monday, April 25, 2011						Sheet 4 of 53



AMD APU FS1	
0.7~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A

RAM DDRIII SODIMMX2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCI_E_VDDC: 2000 mA DP[A,E]_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1D1: 100 mA VDD2D1: 50 mA AVDDC: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCI_E_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCI_E_VDDR: 400 mA DP[A,F]_VDD18: 920 mA DP[A,F]_PVDD: 120 mA
+3VSG	AVDD: 130 mA VDDR3: 60 mA

VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIE: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G



18 PCIE_GTX_C_FRX_P[0..7]

18 PCIE_GTX_C_FRX_N[0..7]

PCIE_FTX_C_GRX_P[0..7] 18

PCIE_FTX_C_GRX_N[0..7] 18

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28

PCIE_FTX_GRX_N[12..15] 28

JCPU1A		CONN@	
PCI EXPRESS			
PCIE_GTX_C_FRX_P0 AA8	P_GFX_RXP0	P_GFX_TXP0	AA2 PCIE_FTX_GRX_P0 C917VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0 AA9	P_GFX_RXN0	P_GFX_TXN0	AA3 PCIE_FTX_GRX_N0 C918VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1 Y7	P_GFX_RXP1	P_GFX_TXP1	Y2 PCIE_FTX_GRX_P1 C919VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1 Y8	P_GFX_RXN1	P_GFX_TXN1	Y1 PCIE_FTX_GRX_N1 C920VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2 W5	P_GFX_RXP2	P_GFX_TXP2	Y4 PCIE_FTX_GRX_P2 C921VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2 W6	P_GFX_RXN2	P_GFX_TXN2	Y5 PCIE_FTX_GRX_N2 C922VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3 W8	P_GFX_RXP3	P_GFX_TXP3	W2 PCIE_FTX_GRX_P3 C923VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3 W9	P_GFX_RXN3	P_GFX_TXN3	W3 PCIE_FTX_GRX_N3 C924VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4 V7	P_GFX_RXP4	P_GFX_TXP4	V2 PCIE_FTX_GRX_P4 C925VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4 V8	P_GFX_RXN4	P_GFX_TXN4	V1 PCIE_FTX_GRX_N4 C926VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5 U5	P_GFX_RXP5	P_GFX_TXP5	V4 PCIE_FTX_GRX_P5 C927VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5 U6	P_GFX_RXN5	P_GFX_TXN5	V5 PCIE_FTX_GRX_N5 C928VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6 U8	P_GFX_RXP6	P_GFX_TXP6	U2 PCIE_FTX_GRX_P6 C929VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6 U9	P_GFX_RXN6	P_GFX_TXN6	U3 PCIE_FTX_GRX_N6 C930VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7 T7	P_GFX_RXP7	P_GFX_TXP7	T2 PCIE_FTX_GRX_P7 C931VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7 T8	P_GFX_RXN7	P_GFX_TXN7	T1 PCIE_FTX_GRX_N7 C932VGA@ 1 2 0.1U_0402_16V7K PCIE_FTX_C_GRX_N7
X R5	P_GFX_RXP8	P_GFX_TXP8	T4 X
X R6	P_GFX_RXN8	P_GFX_TXN8	T5 X
X R8	P_GFX_RXP9	P_GFX_TXP9	R2 X
X R9	P_GFX_RXN9	P_GFX_TXN9	R3 X
X P7	P_GFX_RXP10	P_GFX_TXP10	P2 X
X P8	P_GFX_RXN10	P_GFX_TXN10	P1 X
X N5	P_GFX_RXP11	P_GFX_TXP11	P4 X
X N6	P_GFX_RXN11	P_GFX_TXN11	P5 X
N8	P_GFX_RXP12	P_GFX_TXP12	N2 PCIE_FTX_GRX_P12
N9	P_GFX_RXN12	P_GFX_TXN12	N3 PCIE_FTX_GRX_N12
M7	P_GFX_RXP13	P_GFX_TXP13	M2 PCIE_FTX_GRX_P13
M8	P_GFX_RXN13	P_GFX_TXN13	M1 PCIE_FTX_GRX_N13
L5	P_GFX_RXP14	P_GFX_TXP14	M4 PCIE_FTX_GRX_P14
L6	P_GFX_RXN14	P_GFX_TXN14	M5 PCIE_FTX_GRX_N14
L8	P_GFX_RXP15	P_GFX_TXP15	L2 PCIE_FTX_GRX_P15
L9	P_GFX_RXN15	P_GFX_TXN15	L3 PCIE_FTX_GRX_N15

For UMA Mux.

2
1
0
CK
To HDMI

29 PCIE_DTX_C_FRX_P0 AC5

29 PCIE_DTX_C_FRX_N0 AC6

32 PCIE_DTX_C_FRX_P1 AC8

32 PCIE_DTX_C_FRX_N1 AC9

GPP		GPP	
P_GPP_RXP0	P_GPP_TXP0	AD4 PCIE_FTX_DRX_P0 C950 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29
P_GPP_RXN0	P_GPP_TXN0	AD5 PCIE_FTX_DRX_N0 C951 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29
P_GPP_RXP1	P_GPP_TXP1	AC2 PCIE_FTX_DRX_P1 C952 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32
P_GPP_RXN1	P_GPP_TXN1	AC3 PCIE_FTX_DRX_N1 C953 1 2 0.1U_0402_16V7K	PCIE_FTX_C_DRX_N1 32
X AB7	P_GPP_RXP2	AB2 X	
X AB8	P_GPP_RXN2	AB1 X	
X AA5	P_GPP_RXP3	AB4 X	
X AA6	P_GPP_RXN3	AB5 X	

GLAN
WLAN

13 UMI_MTX_C_FRX_P0 AF8

13 UMI_MTX_C_FRX_N0 AF7

13 UMI_MTX_C_FRX_P1 AE6

13 UMI_MTX_C_FRX_N1 AE5

13 UMI_MTX_C_FRX_P2 AE9

13 UMI_MTX_C_FRX_N2 AE8

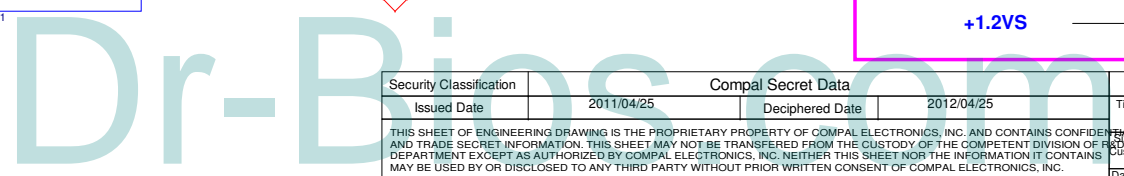
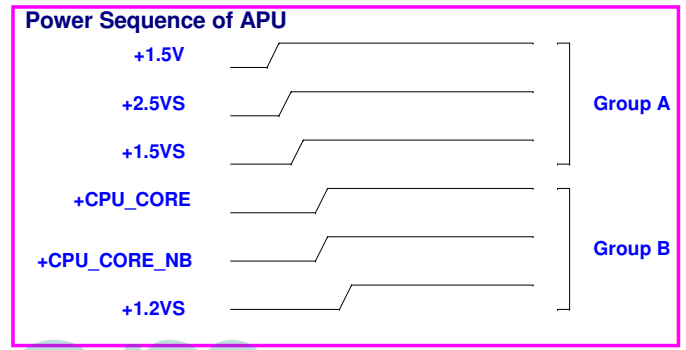
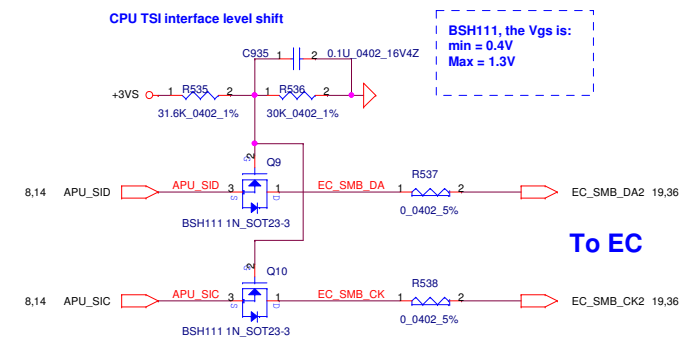
13 UMI_MTX_C_FRX_P3 AD8

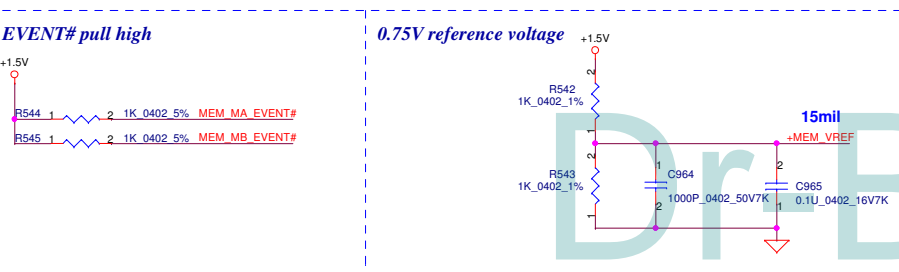
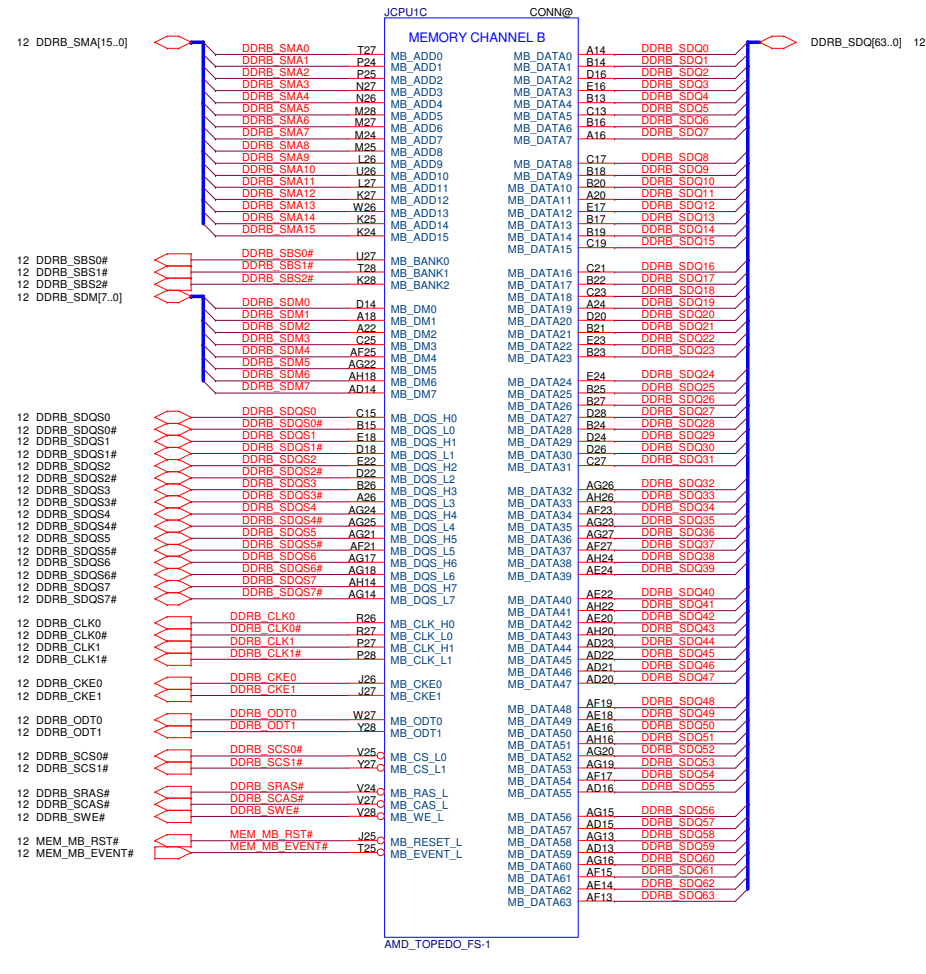
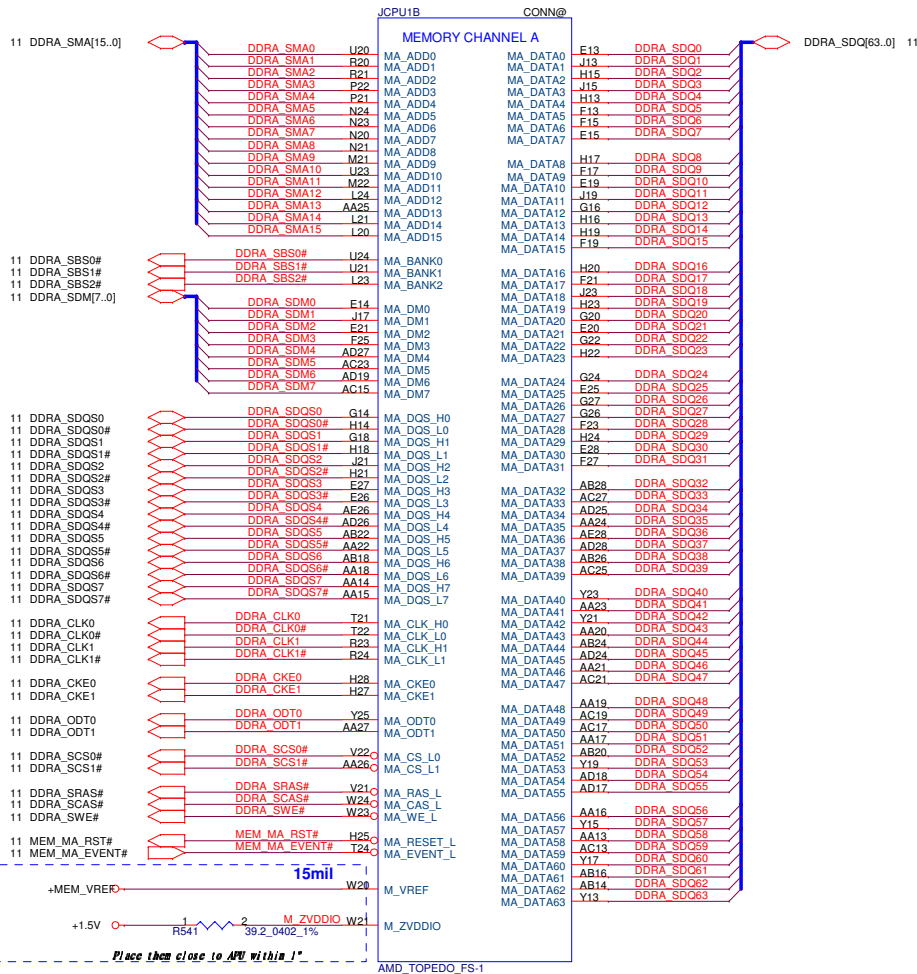
13 UMI_MTX_C_FRX_N3 AD7

UMI - CLK		UMI - CLK	
P_UMI_RXP0	P_UMI_TXP0	AF1 UMI_FTX_MRX_P0 C956 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13
P_UMI_RXN0	P_UMI_TXN0	AF2 UMI_FTX_MRX_N0 C957 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 13
P_UMI_RXP1	P_UMI_TXP1	AE5 UMI_FTX_MRX_P1 C958 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P1 13
P_UMI_RXN1	P_UMI_TXN1	AE4 UMI_FTX_MRX_N1 C959 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N1 13
P_UMI_RXP2	P_UMI_TXP2	AE3 UMI_FTX_MRX_P2 C960 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P2 13
P_UMI_RXN2	P_UMI_TXN2	AE2 UMI_FTX_MRX_N2 C961 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N2 13
P_UMI_RXP3	P_UMI_TXP3	AD1 UMI_FTX_MRX_P3 C962 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_P3 13
P_UMI_RXN3	P_UMI_TXN3	AD2 UMI_FTX_MRX_N3 C963 1 2 0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13

+1.2VS R539 196_0402_1% K5 P_ZVDDP

P_ZVSS R540 196_0402_1% K4 P_ZVSS





Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	AMD FS1 DDRIII /F
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Date:	Monday, April 25, 2011	Sheet	7	of 53

To LVDS Translator

To FCH VGA ML

100MHz

100MHz_NSS

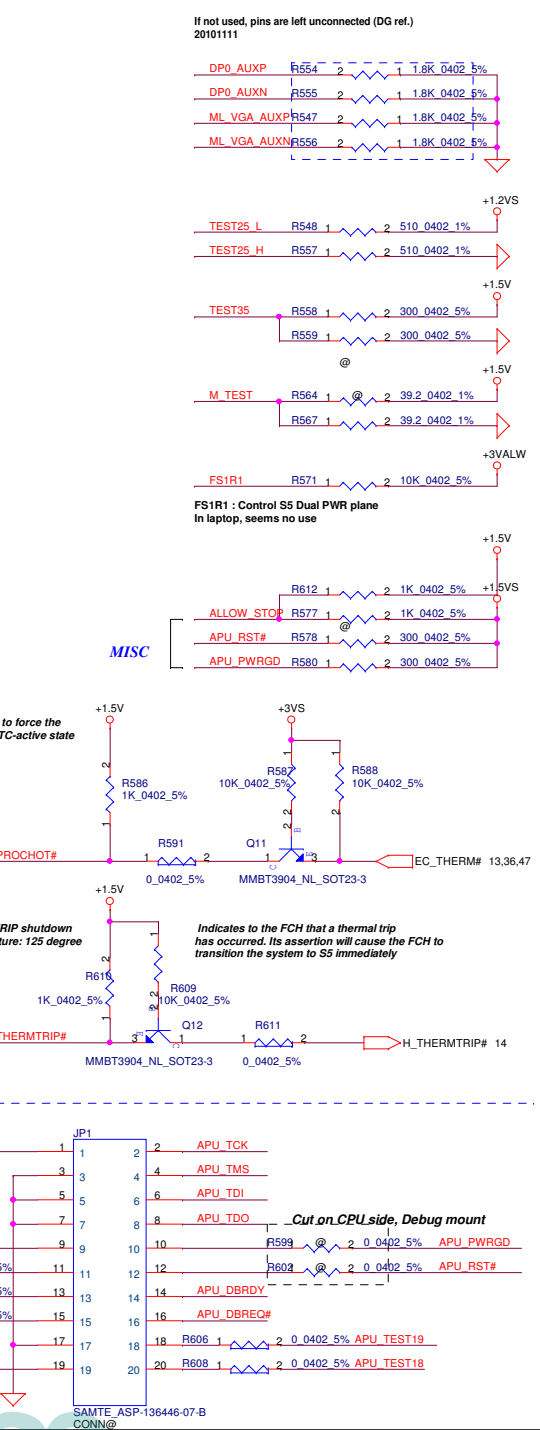
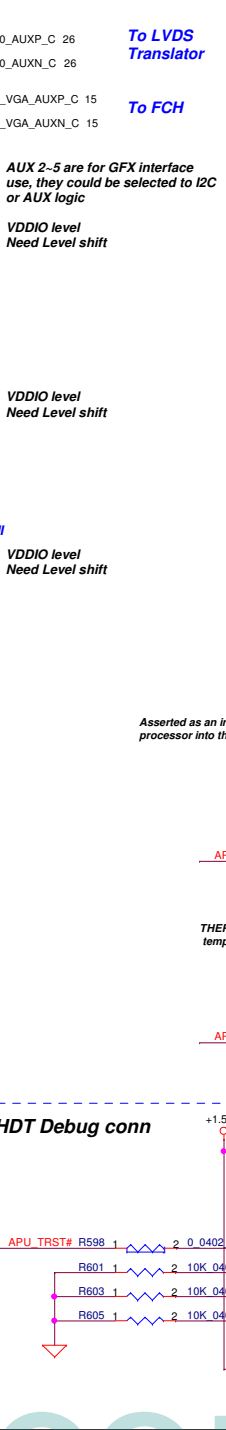
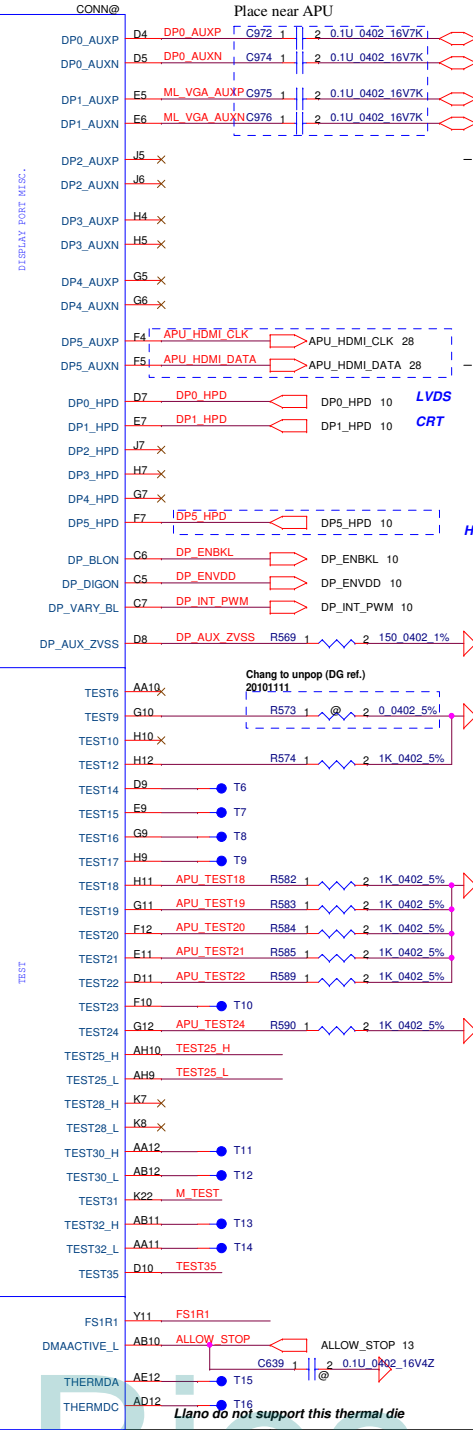
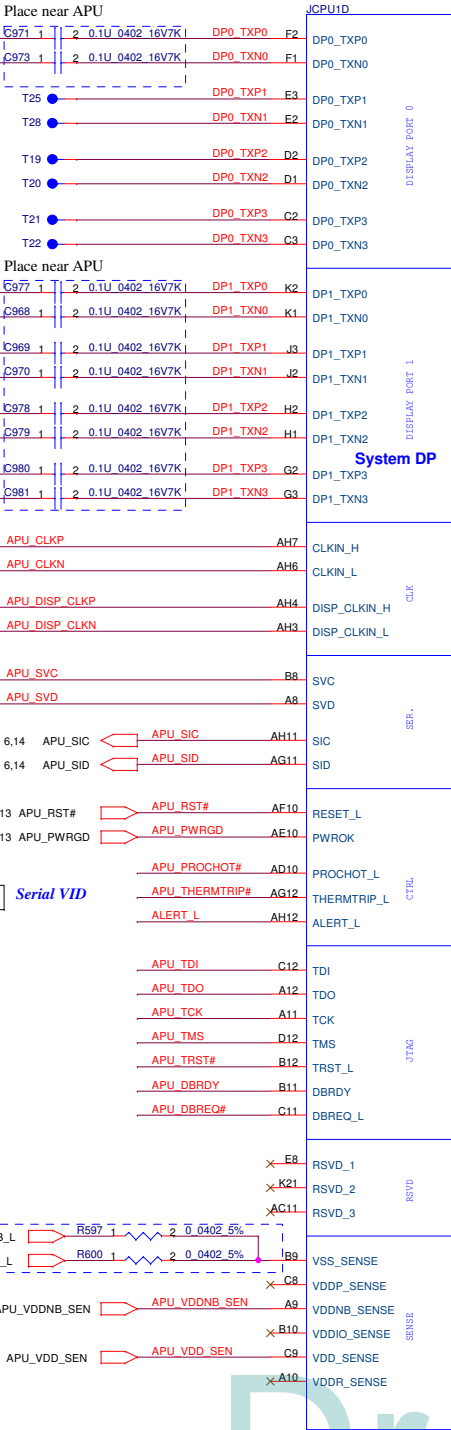
Chang to PU +1.5V (DG ref.) 20101111

Close to Header

Route as differential with VSS_SENSE

APU_VDDNB_RUN_FB_L route as differential

APU_VDD_RUN_FB_L route as differential



If not used, pins are left unconnected (DG ref.) 20101111

AUX 2-5 are for GFX interface use, they could be selected to I2C or AUX logic

VDDIO level Need Level shift

VDDIO level Need Level shift

VDDIO level Need Level shift

Asserted as an input to force the processor into the HTC-active state

THERMTRIP shutdown temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

Cut on CPU side, Debug mount

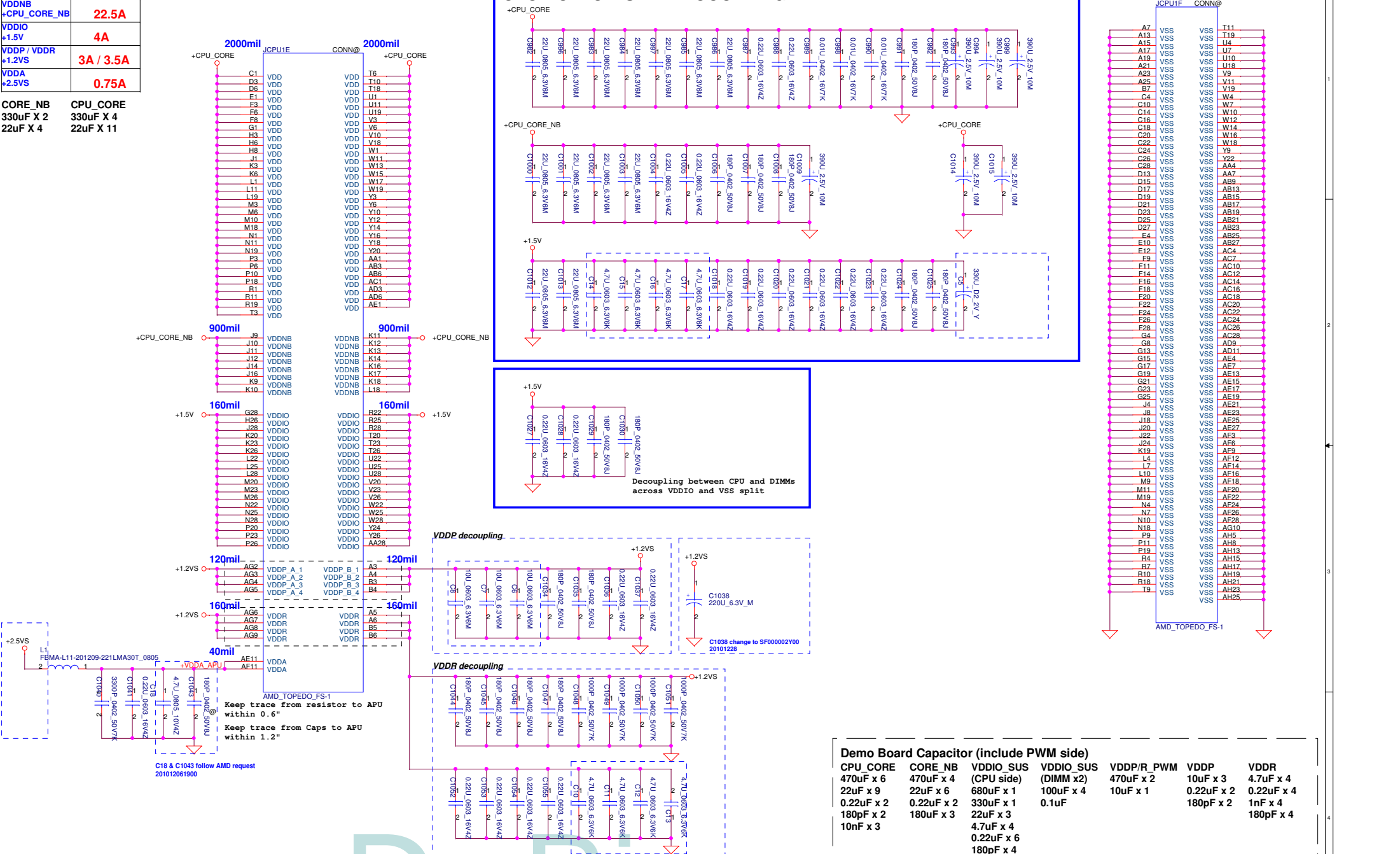
Llano do not support this thermal die

Security Classification	Compal Secret Data	Title	AMD FS1 Display / MISC / HDT
Issued Date	2011/04/25	Deciphered Date	2012/04/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number	QBL60 LA-7552P
Date	Monday, April 25, 2011	Sheet	8 of 53

Power Name	Consumption
VDD	
+CPU_CORE	50A
VDDNB	
+CPU_CORE_NB	22.5A
VDDIO	
+1.5V	4A
VDDP / VDDR	
+1.2VS	3A / 3.5A
VDDA	
+2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

CPU BOTTOM SIDE DECOUPLING

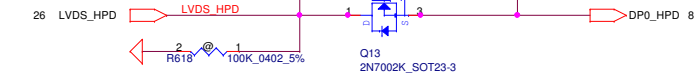


JCPU1F	CONN@
A7	T11
A13	T19
A15	T14
A17	L17
A19	L10
A21	L18
A23	V9
A25	V11
C4	V19
B7	W4
C10	W7
C14	W10
C16	W12
C18	W14
C20	W16
C22	W18
C24	Y9
C26	Y2
C28	AA4
D13	AA7
D15	AB9
D17	AB13
D19	AB15
D21	AB17
D23	AB19
D25	AB21
D27	AB23
E4	AB25
E10	AB27
E12	AC4
F3	AC7
F11	AC10
F14	AC12
F16	AC14
F18	AC16
F20	AC18
F22	AC20
F24	AC22
F26	AC24
F28	AC26
G4	AC28
G8	AD9
G12	AD11
G15	AE4
G17	AE7
G19	AE13
G21	AE15
G23	AE17
G25	AE19
J4	AE21
J8	AE23
J12	AE25
J20	AE27
J22	AF3
J24	AF6
K18	AF9
L4	AF12
L7	AF14
L10	AF16
M5	AF18
M11	AF20
M19	AF22
N4	AF24
N10	AF26
N12	AF28
N18	AG10
P9	AH5
P11	AH8
P19	AH13
R4	AH15
R7	AH17
R10	AH19
R18	AH21
T9	AH23
	AH25

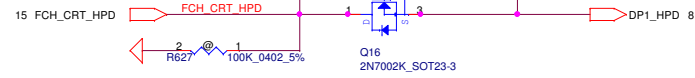
Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3				180pF x 4
10nF x 3		4.7uF x 4				
		0.22uF x 6				
		180pF x 4				

HPD

Translator HPD From Translator



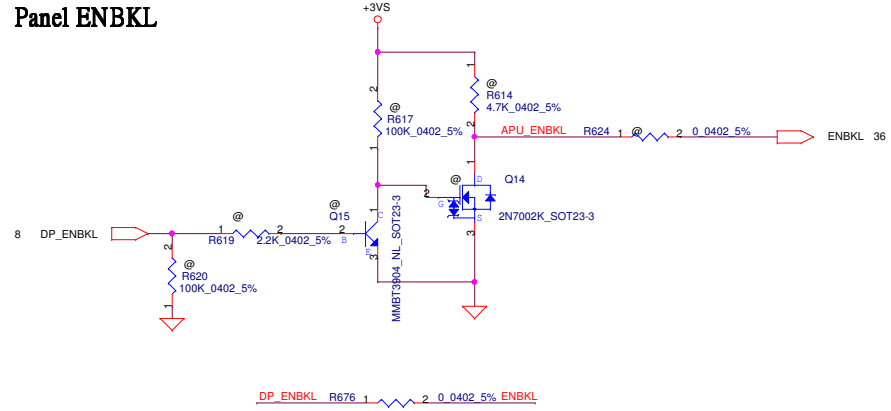
CRT HPD From FCH



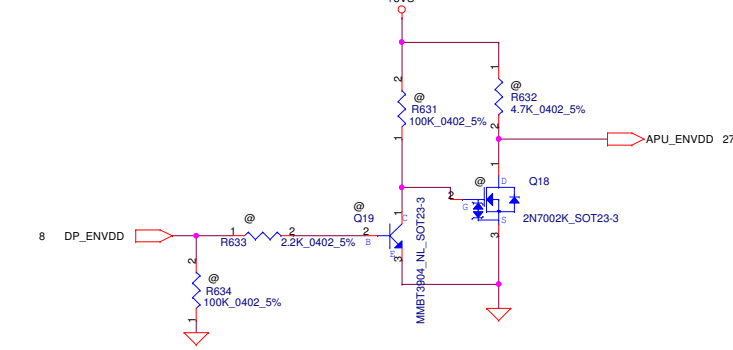
HDMI HPD From HDMI Conn



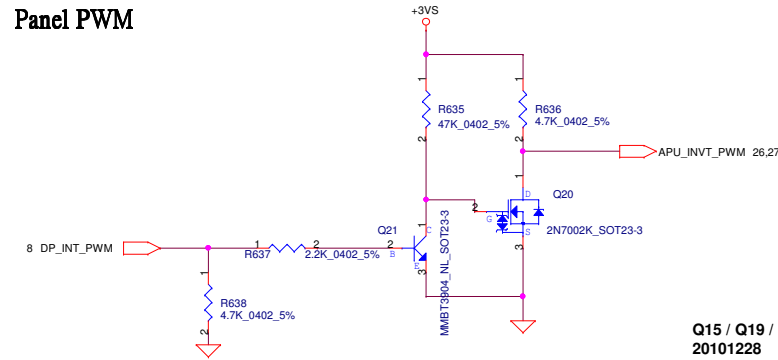
Panel ENBKL



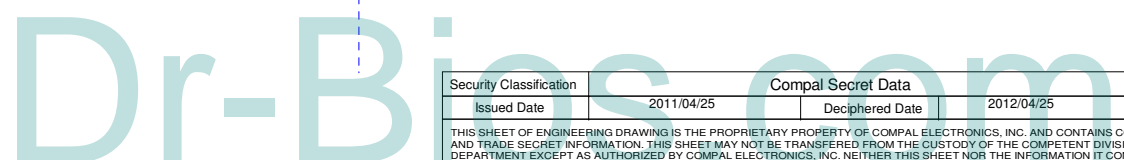
Panel ENVDD



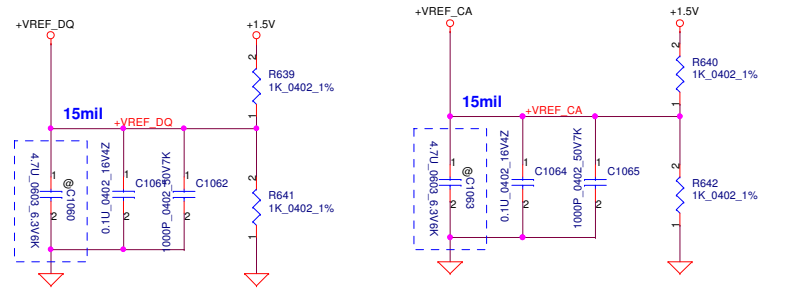
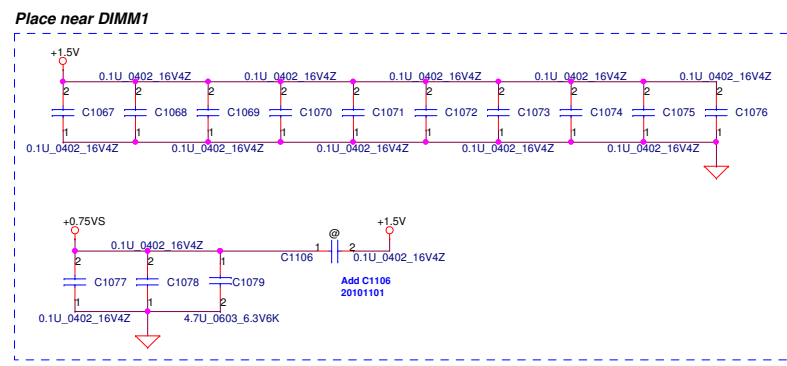
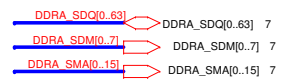
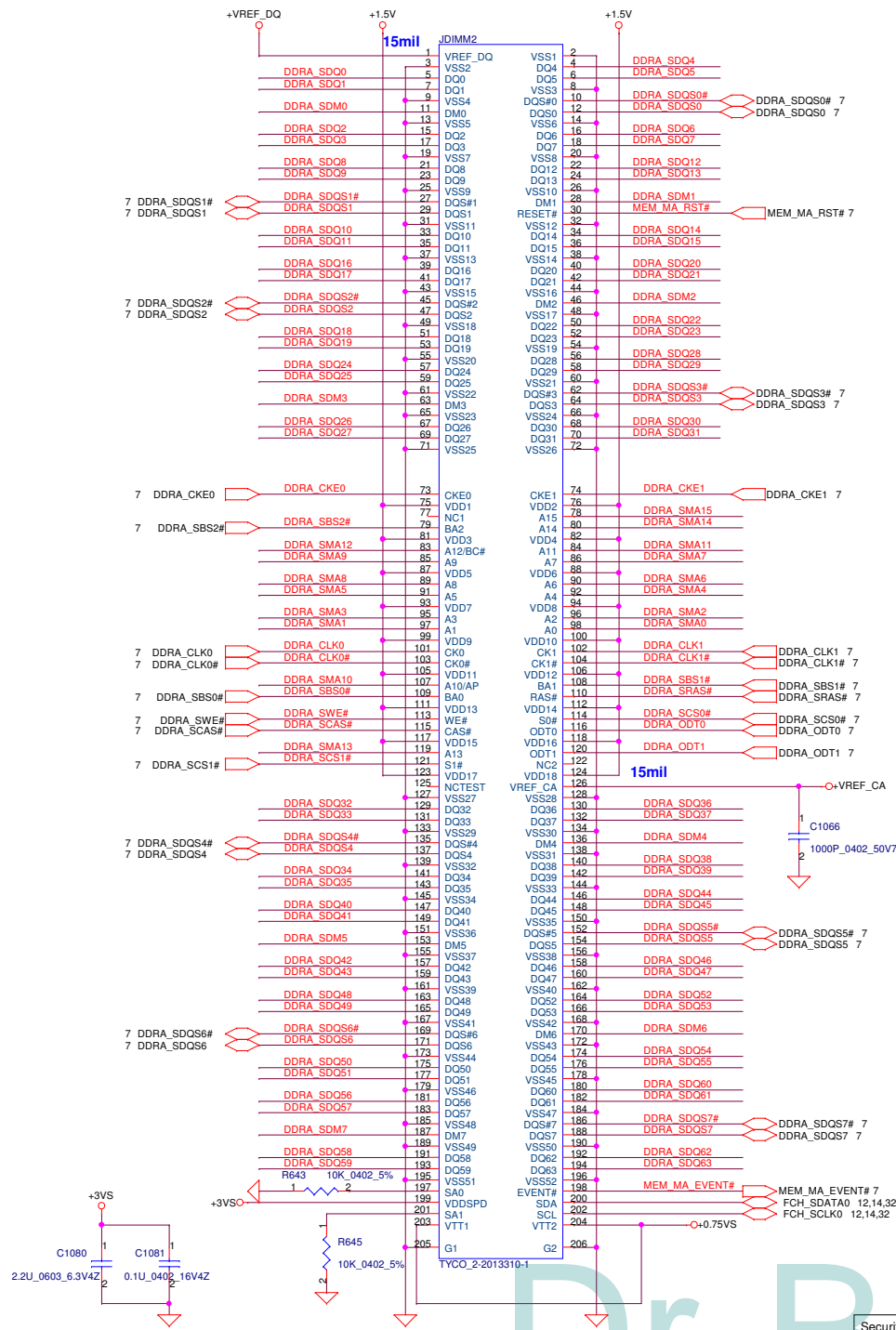
Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

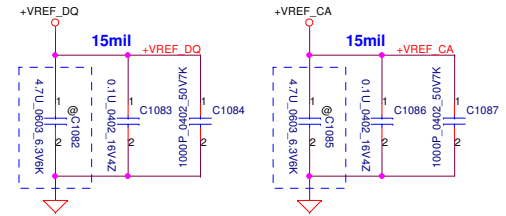
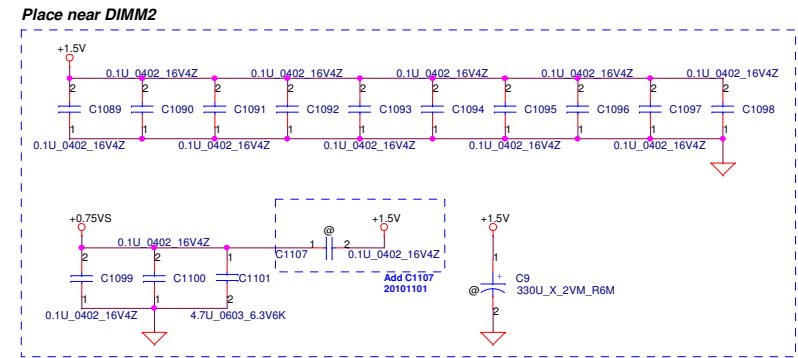
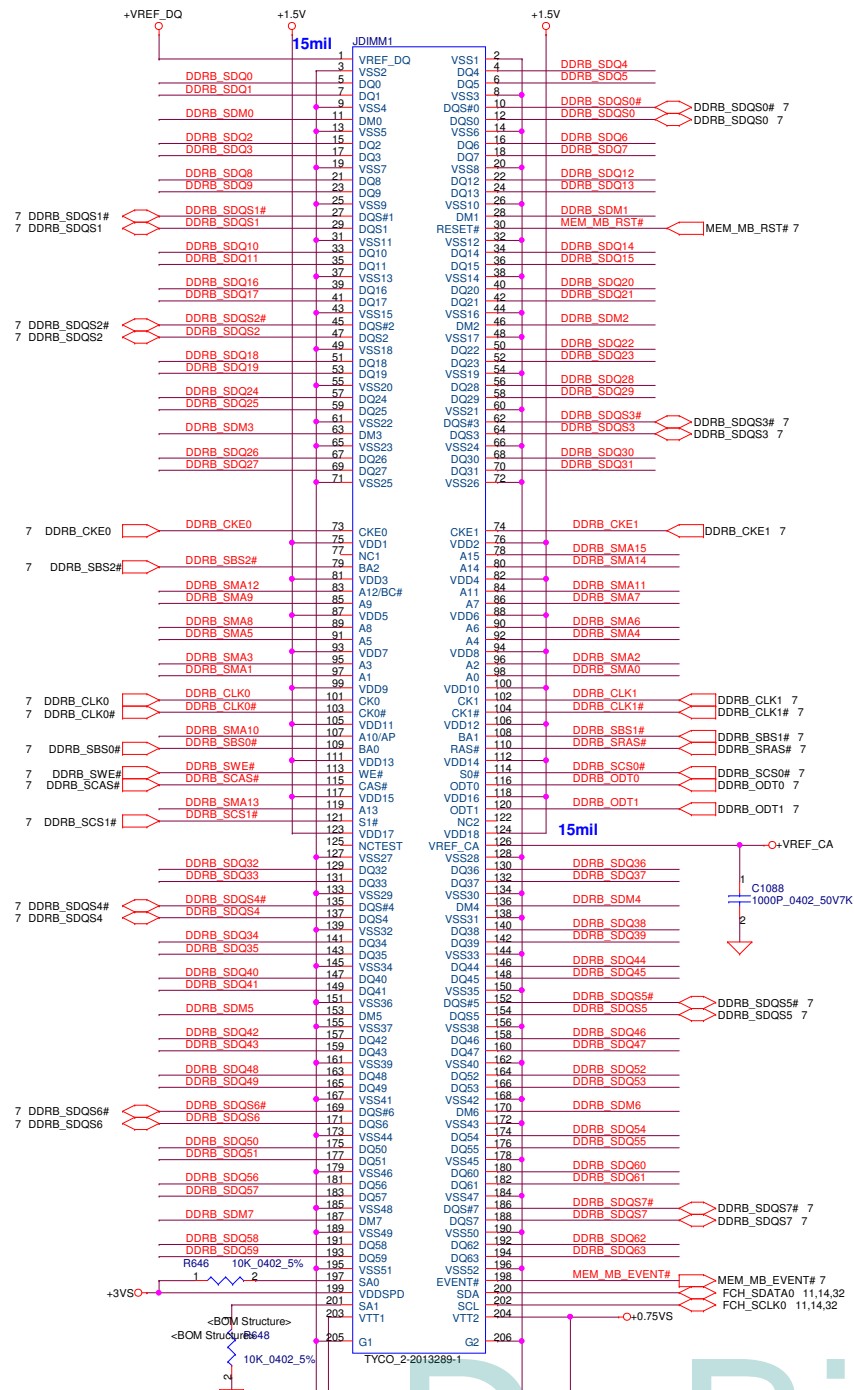


Security Classification	Compal Secret Data			Title	AMD FS1 Singal Level Shifter	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Document Number	QBL60 LA-7552P	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FCH DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	1.0	
				Date:	Monday, April 25, 2011	Sheet 10 of 53



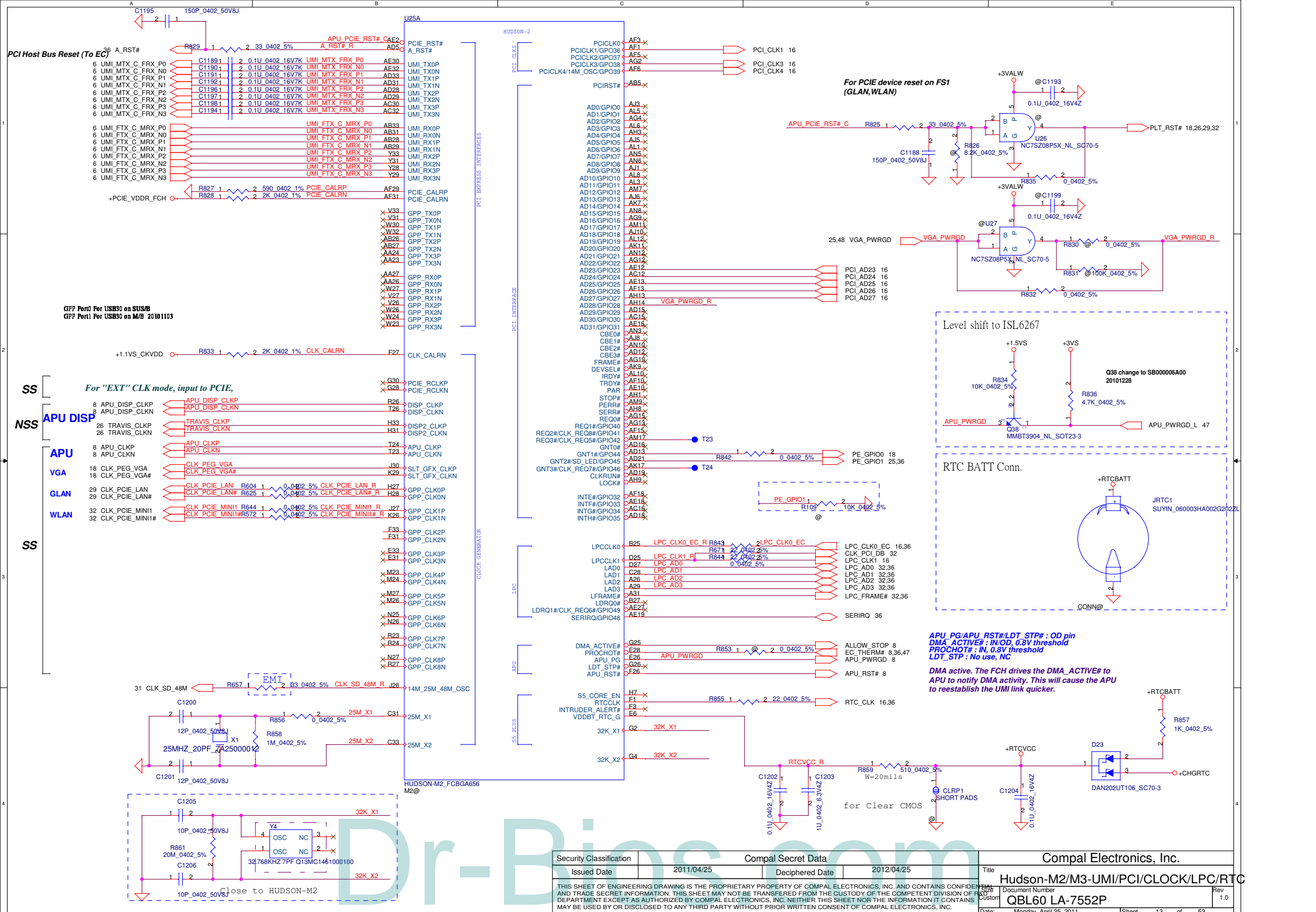
DIMM_A STD H:9.2mm
 <Address: 00>

Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	DDRIII SO-DIMM 1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number QBL60 LA-7552P Date: Monday, April 25, 2011
Date: Monday, April 25, 2011				Rev 1.0 Sheet 11 of 53



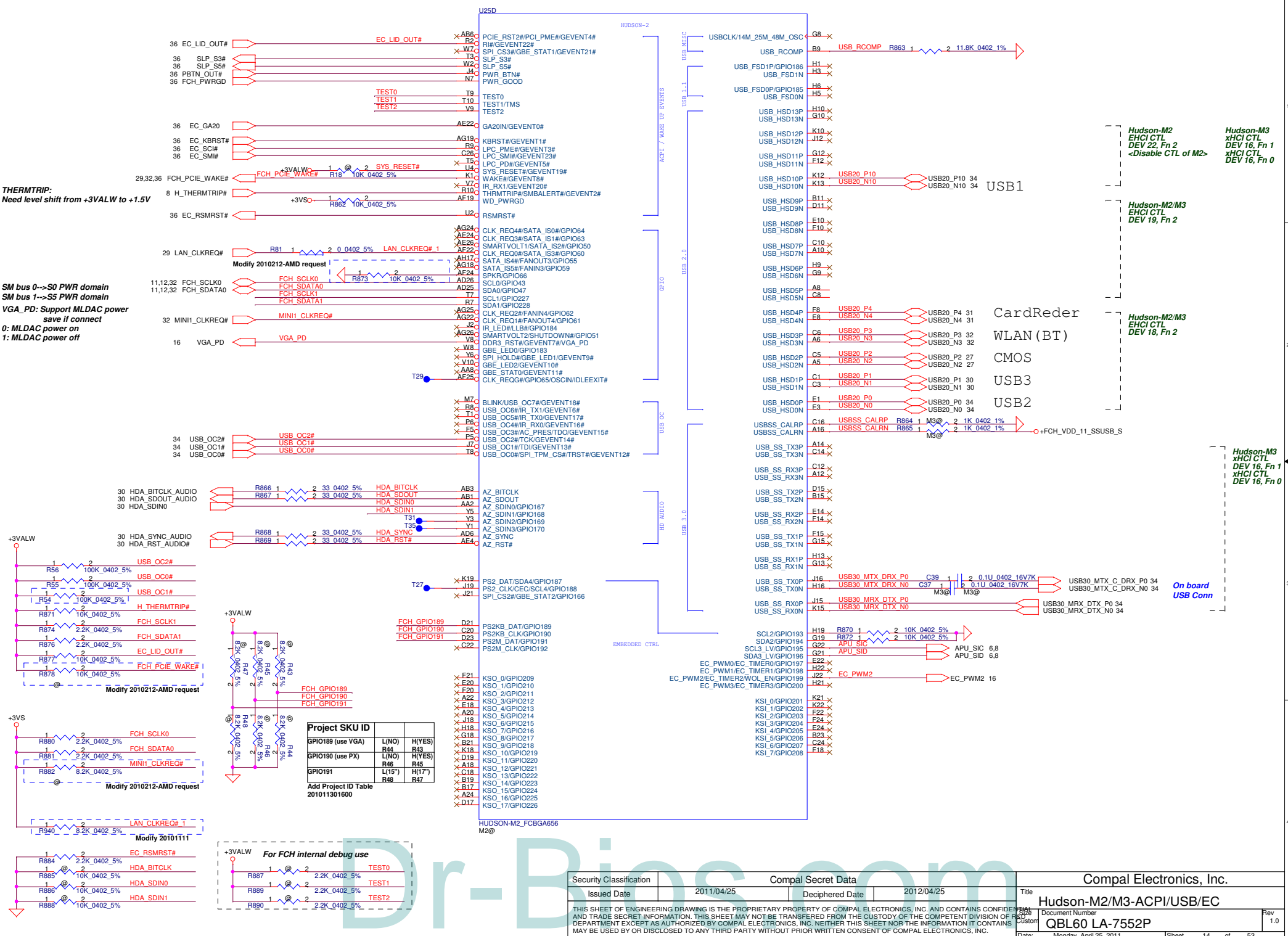
DIMM_B STD H:5.2mm
 <Address: 01>

Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev
QBL60 LA-7552P				1.0
Date:	Monday, April 25, 2011	Sheet	12	of 53



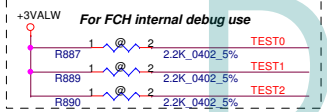
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	QBL60 LA-7552P
Date	Monday, April 25, 2011	Sheet	13 of 53	Rev	1.0

PCIE_RST2 : Reset PCIe device on Hudson2

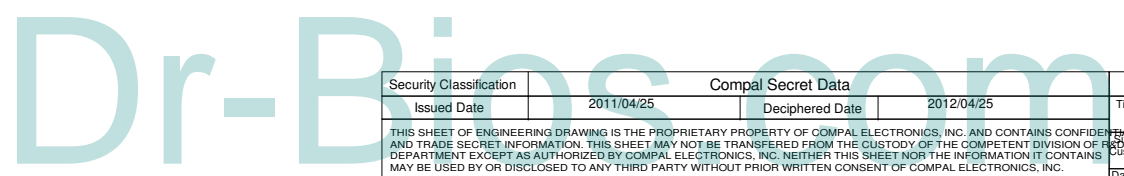
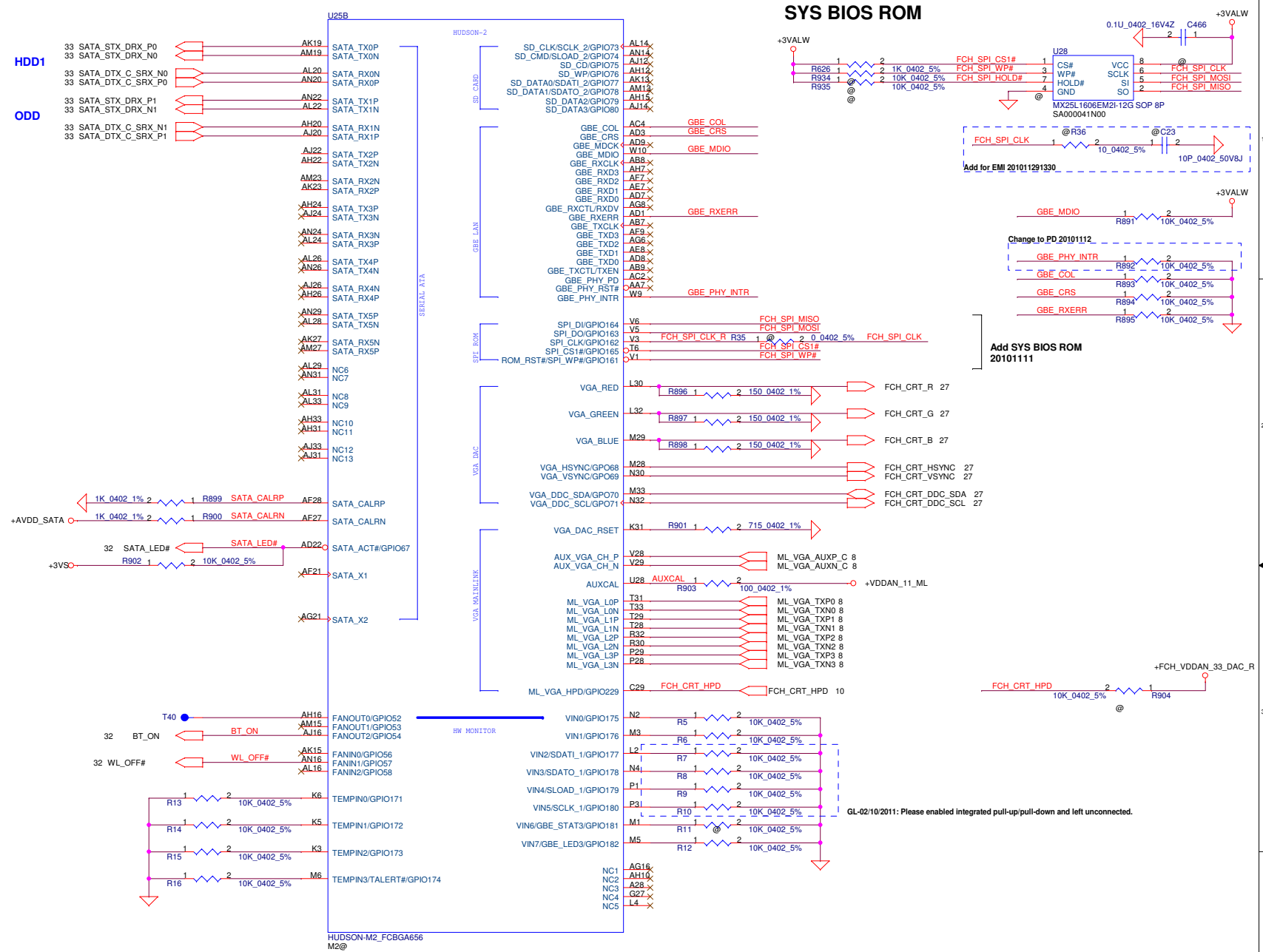


Project SKU ID	L(N)O	H(Y)ES
GPIO189 (use VGA)	R43	H(YES)
GPIO190 (use PX)	R46	R45
GPIO191	R48	H(17")

Add Project ID Table
201011301600



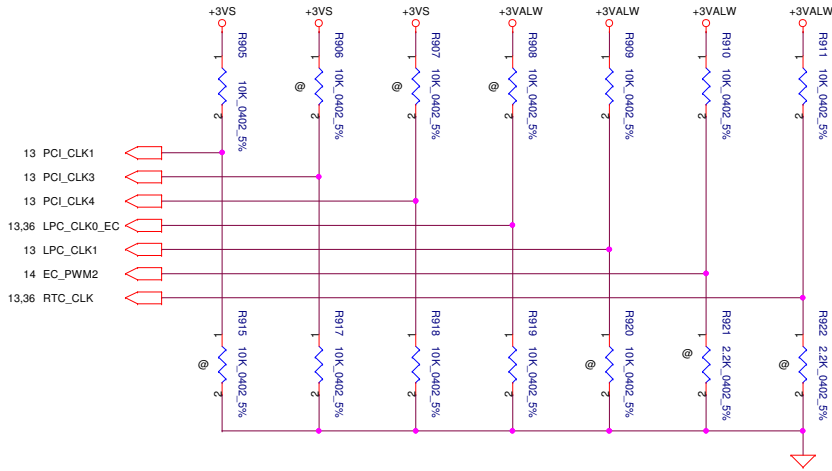
Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Hudson-M2/M3-ACPI/USB/EC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Hudson-M2/M3-ACPI/USB/EC Document Number QBL60 LA-7552P Rev 1.0
Date:	Monday, April 25, 2011	Sheet	14	of 53



Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Hudson-M2/M3-SATA/GBE/HWM
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Document Number	QBL60 LA-7552P			Rev 1.0
Date	Monday, April 25, 2011			Sheet 15 of 53

STRAP PINS

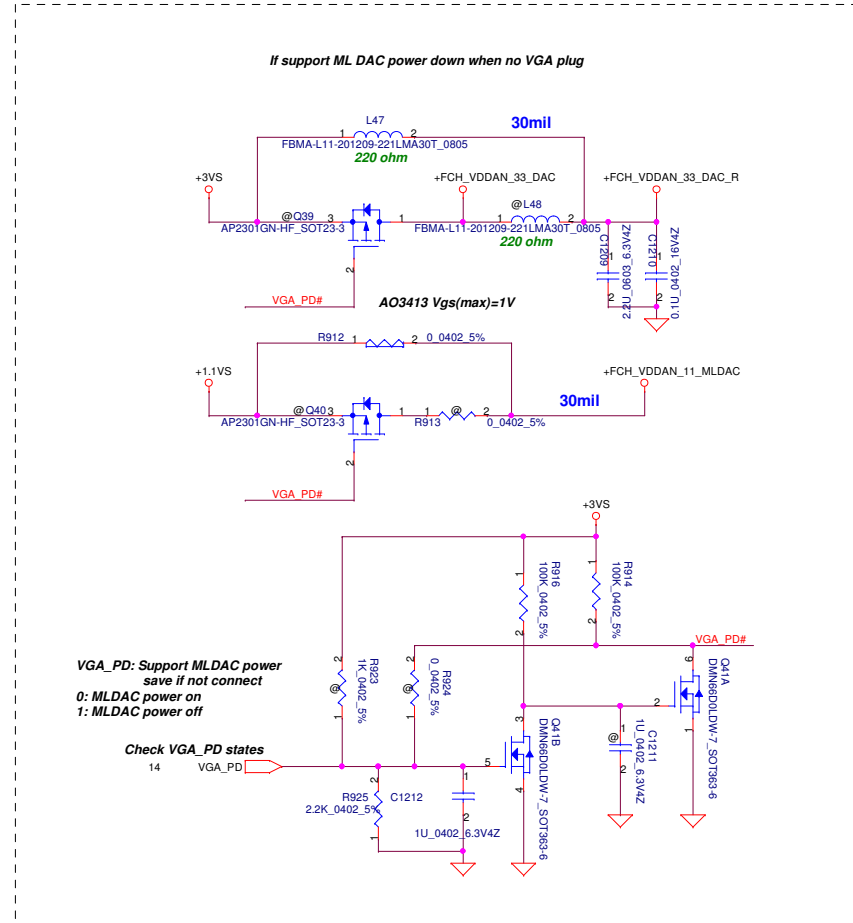
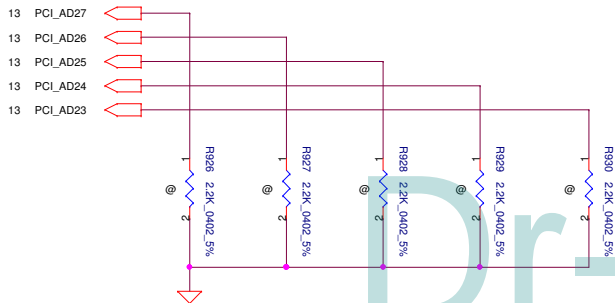
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



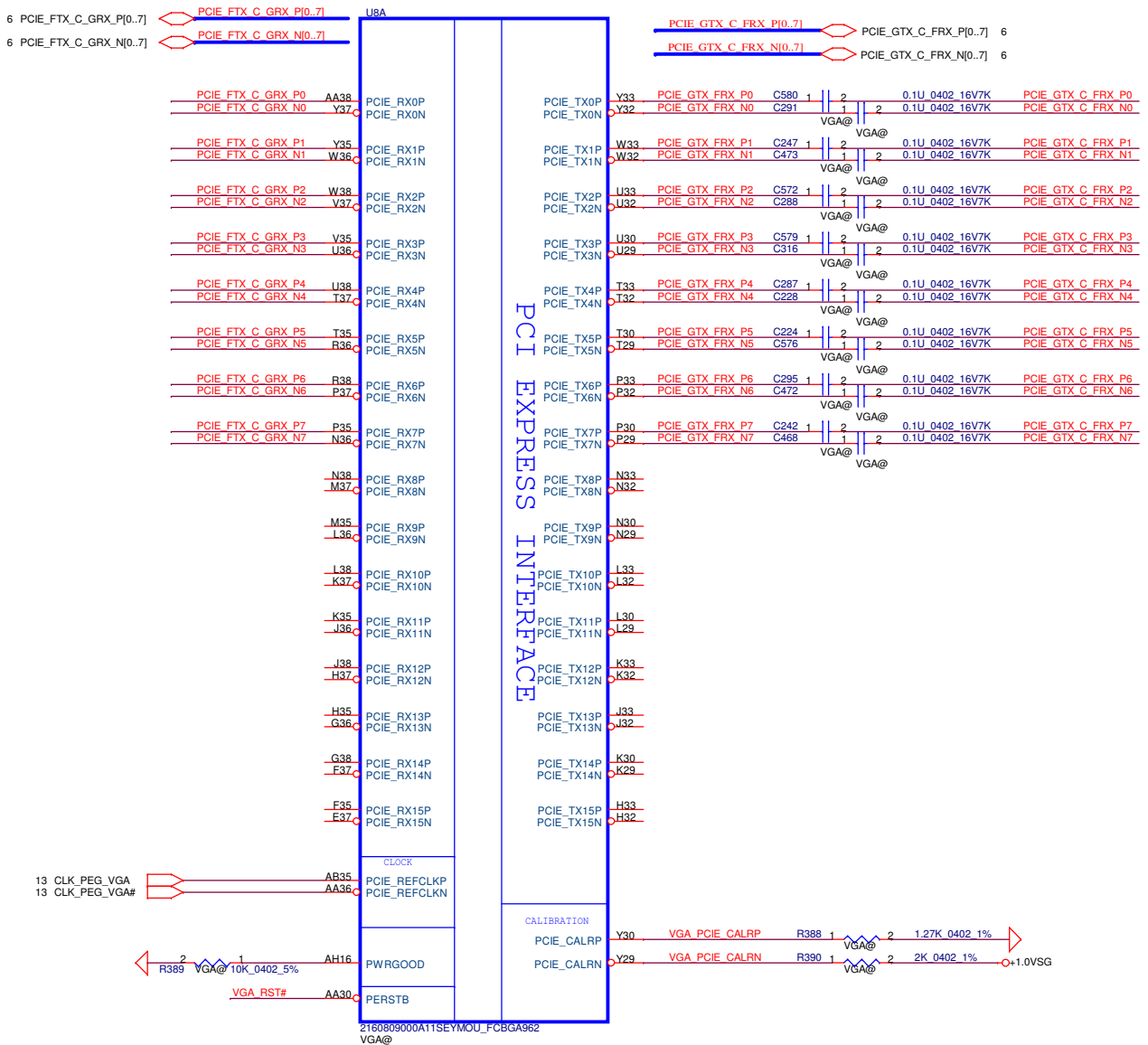
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23	
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



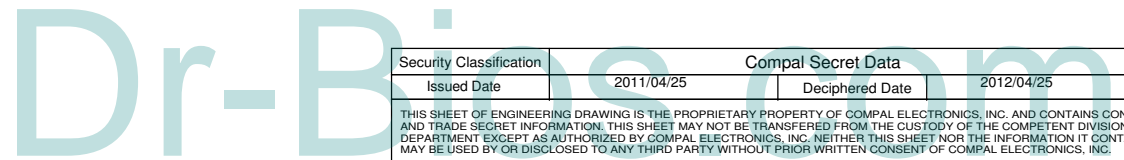
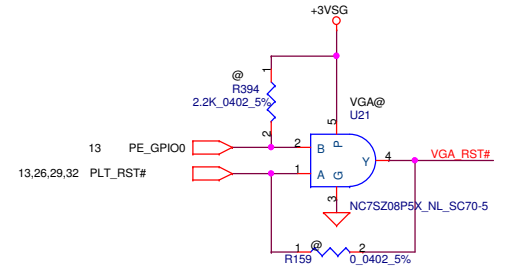
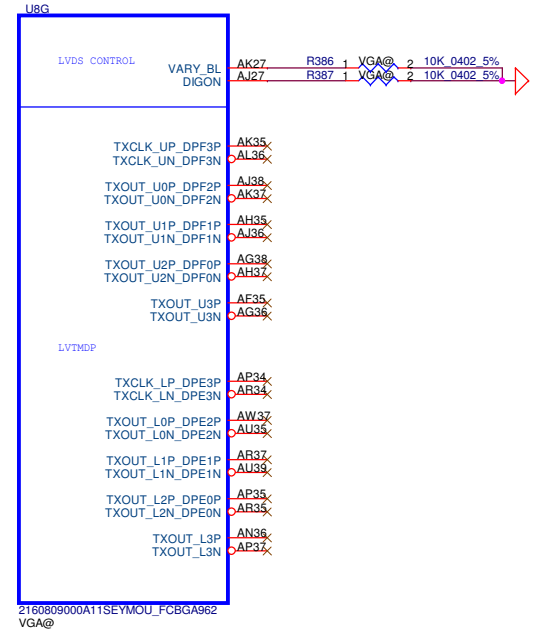
GFX PCIE LANE REVERSAL



For UMA Mux.

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	Vancouver_PCIE / LVDS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Custom	Document Number	QB160 LA-7552P		Rev
Date	Monday, April 25, 2011	Sheet	18	of	53

Strap Name	Pin Straps description <all Internal PD>	Setting
VIP_DEVICE_EN	V2SYNCK (GENLK_VSYNCK) VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPI09 VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPI00 Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	GPI01 PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPI013 GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	001
CONFIG[1]	GPI012	
CONFIG[0]	GPI011	
BIOS_ROM_EN	GPI022 Enable external BIOS ROM device (Internal PD) 0: Diabie, 1: Enable	0
AUD[1]	HSYNCK 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
AUD[0]	VSYNCK	
BIF_GEN2_EN	GPI02 0: Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNCK (GENLK_CLK) GPIO8 GPIO21 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

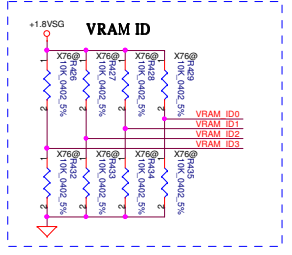
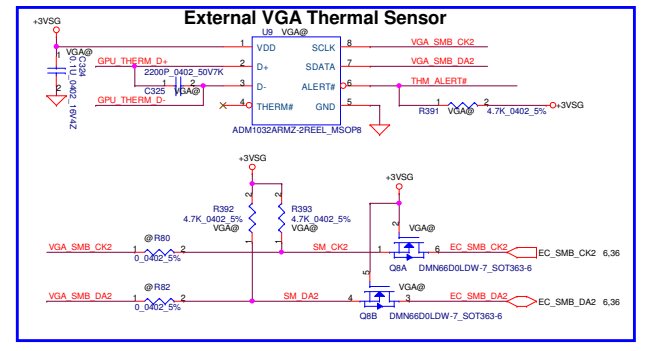
NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND



GPIO5 fast-power reduction: HW control will cause display disturb should use SW method control
GPIO6 voltage control signal, No use can NC!

Move to DDCCCLK_AUX3P,DDCDATA_AUX3N

GPIO7 Controls backlight on/off. Active High, need external PD
If GPIO22 High, GPIO 11-13 ~CFG[0:2] Config ROM type, GPU has internal PD

GPIO6,15,16,20 Voltage control signal GPIO6,15 no use can NC
Thermal monitor interrupt Critical temperature fault

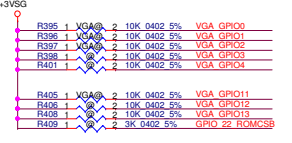
Reserved

External BIOS device ON(1)/OFF(0) Inter PD

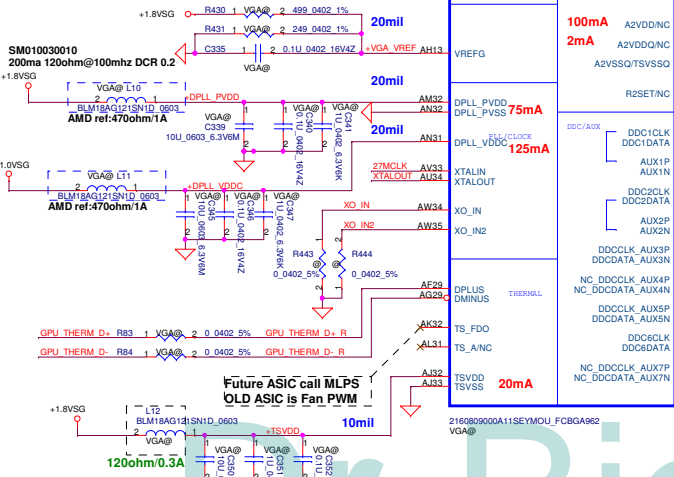
Internal Debug no use can floating

ON(1)/OFF(0) Stereo Sync no use can NC

For ATI Cross fire no use can NC



VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	SA19004530 64M16x8	0	0	0	0
	K4W1G1646G-BC11				
Samsung	SA0000470A0 128M16x8	0	0	1	0
	K4W2G1646G-BC11				
Hynix	HA000041S60 64M16x8	0	1	0	0
	H5TQ16630PFR-11C				
Hynix	HA00003Y030 128M16x8	0	1	0	1
	H5TQ26630PFR-11C				

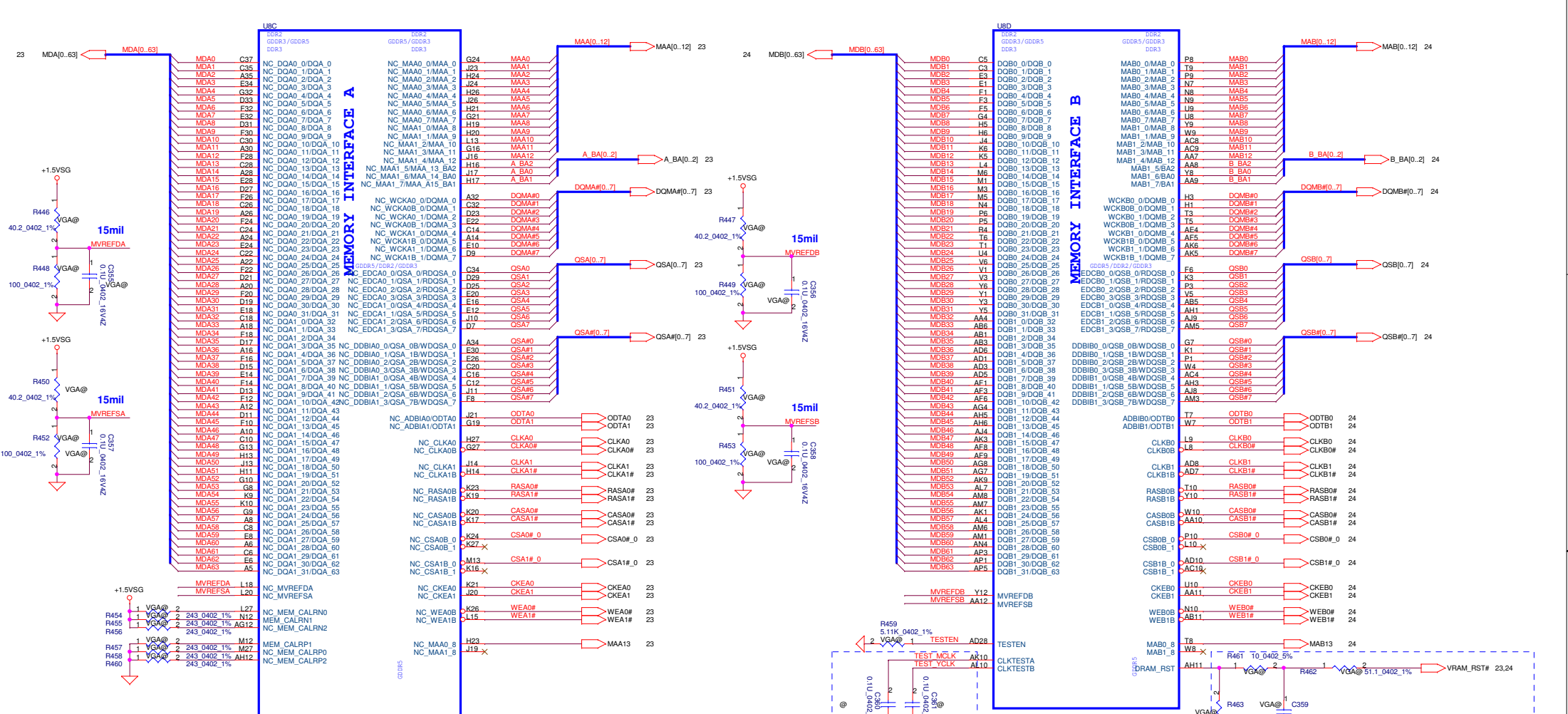


NC on Park, Robson and Seymour

Future ASIC call MLPS
QLD ASIC is Fan PWM

NC on Park, Robson and Seymour

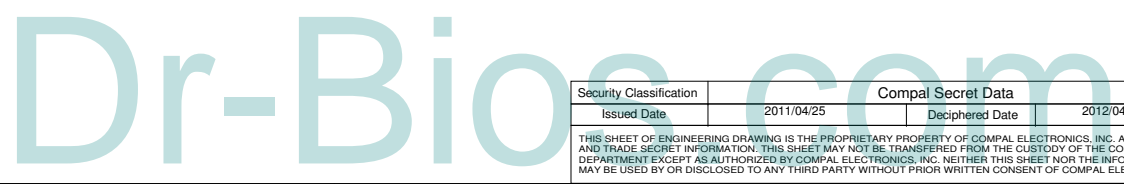
GPIO8 Serial-ROM output from ROM, if GPIO22 High, GPIO 11-13 ~CFG[0:2]
GPIO9 Serial-ROM input to ROM, Config ROM type, GPU has internal PD
GPIO10 Serial-ROM clock to ROM, if GPIO22 Low, GPIO 11-13 ~CFG[0:2]
GPIO22 external BIOS-ROM enable, Config Primary memory-aperture size
CFG[3:0] 128MB 000
256MB 001 *
64MB 010
GPIO8,GPIO9,GPIO10 no use can NC
GPIO22 Enable need 3K PH, no use must NC

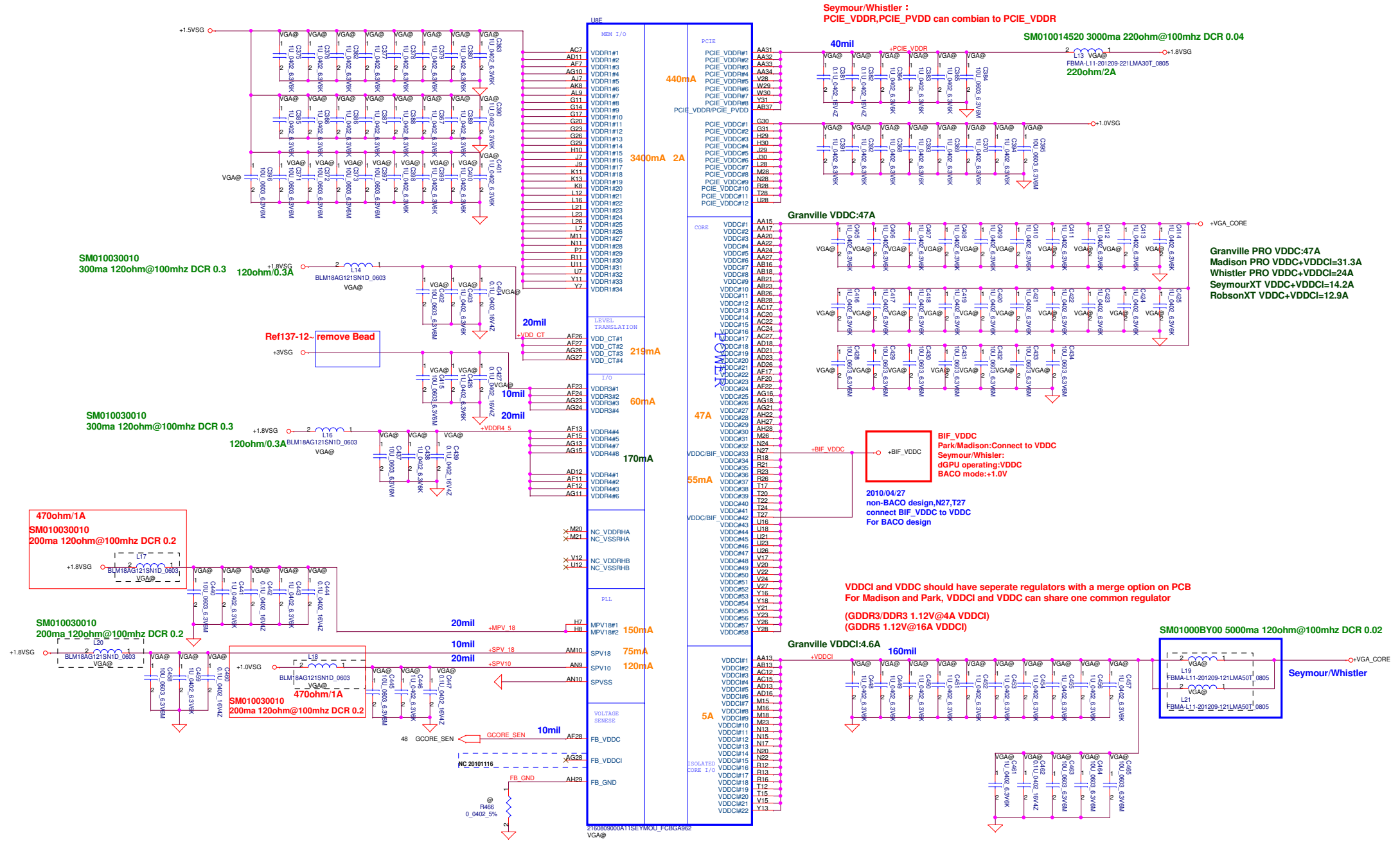


Note:
route 50ohms single-ended
and 100ohms diff
and keep short
REF137-03 suggest

Park&Seymour is single channel for memory (channel B only)

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2012/04/25	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Document Number QBL60 LA-7552P				Rev 1.0	
Date: Monday, April 25, 2011				Sheet 20 of 53	





Seymour/Whistler :
PCIE_VDDR, PCIE_PVDD can combian to PCIE_VDDR

SM010014520 3000ma 220ohm@100mhz DCR 0.04

40mil
+PCIE_VDDR
FBMA-L1-201209-221LMA30T_0805
220ohm/2A

SM010030010
300ma 120ohm@100mhz DCR 0.3

SM010030010
300ma 120ohm@100mhz DCR 0.3

SM010030010
300ma 120ohm@100mhz DCR 0.3

SM010030010
300ma 120ohm@100mhz DCR 0.3

SM010030010
300ma 120ohm@100mhz DCR 0.3

SM010030010
300ma 120ohm@100mhz DCR 0.3

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

Granville VDDC:47A

Granville PRO VDDC:47A
Madison PRO VDDC+VDDCI=31.3A
Whistler PRO VDDC+VDDCI=24A
SeymourXT VDDC+VDDCI=14.2A
RobsonXT VDDC+VDDCI=12.9A

BIF_VDDC
Park/Madison: Connect to VDDC
Seymour/Whistler:
dGPU operating: VDDC
BACO mode: +1.0V

2010/04/27
non-BACO design, N27, T27
connect BIF_VDDC to VDDC
For BACO design

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

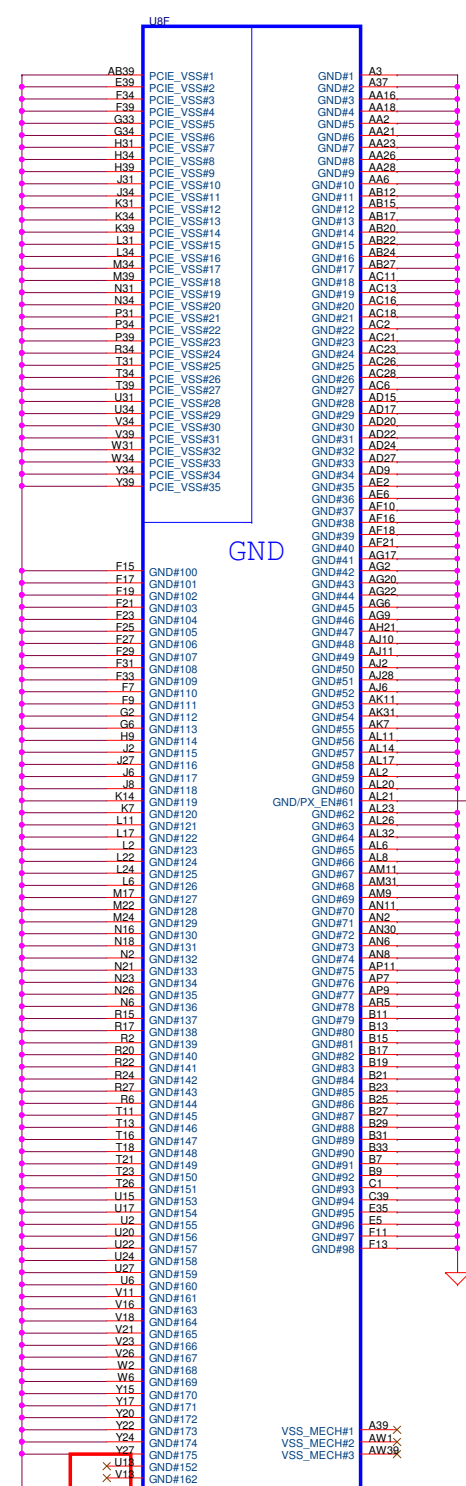
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)

Granville VDDCI:4.6A

SM01000BY00 5000ma 120ohm@100mhz DCR 0.02

Seymour/Whistler

Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Vancouver Power/GND		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE CONTENTS DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						
Size	Custom	Document Number	QBL60 LA-7552P		Rev	1.0
Date:	Monday, April 25, 2011	Sheet	21	of	53	



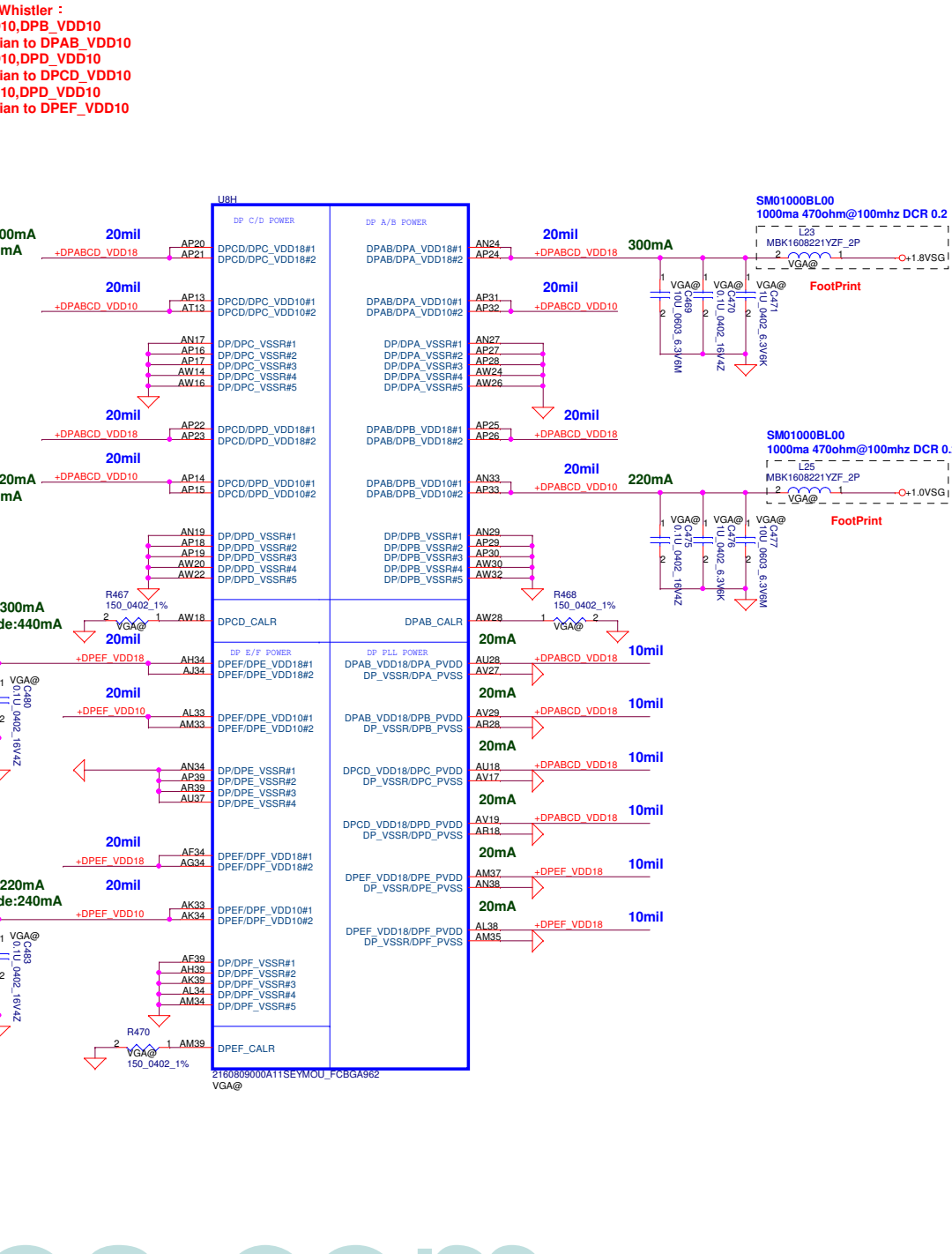
DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
 can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
 can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
 can combian to DPEF_VDD18

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
 can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
 can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
 can combian to DPEF_VDD10

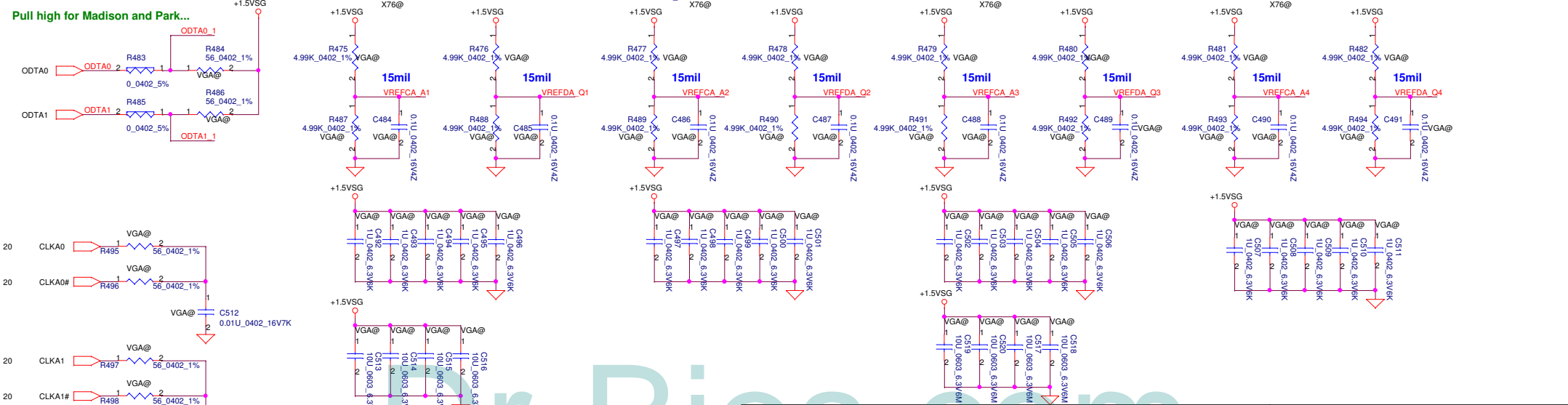
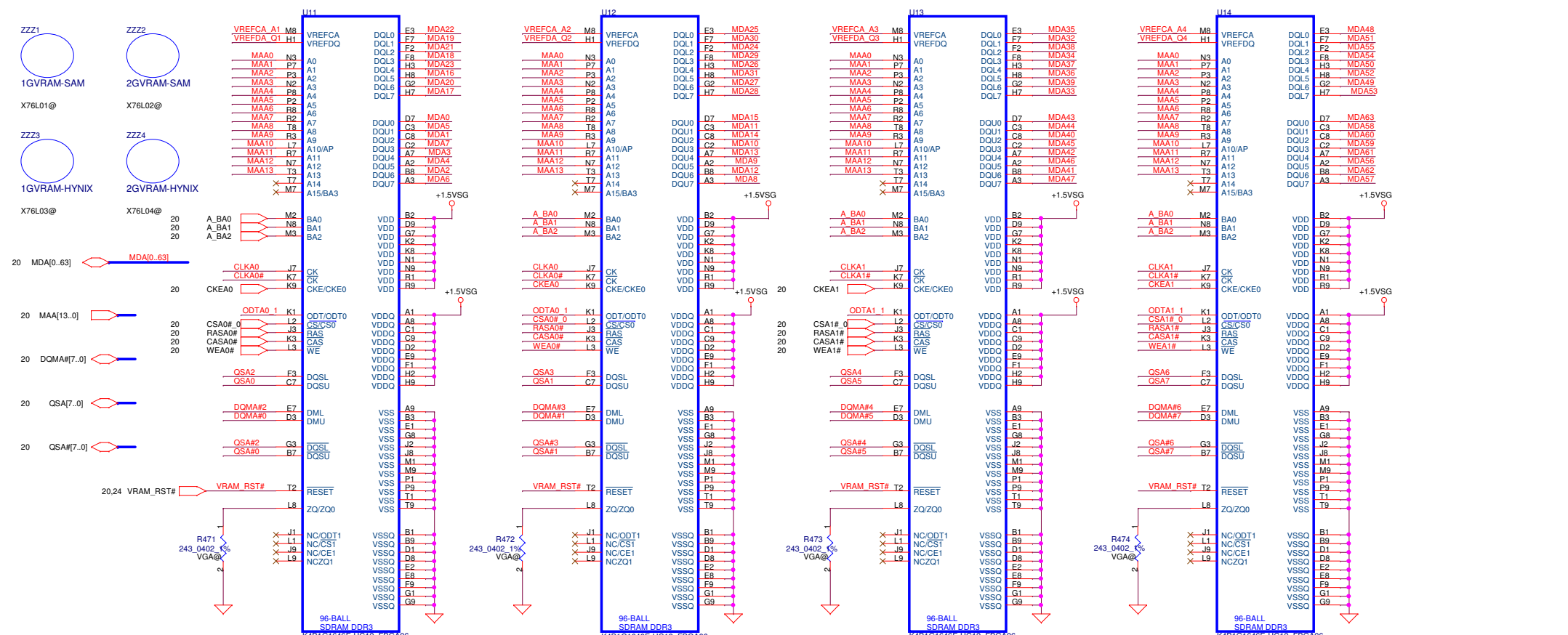
DPx-VSSR,DPx_PVSS can combian to DP_VSSR
 (Manhattan should have individual GND)
 where x is A,B,C,D,E,F

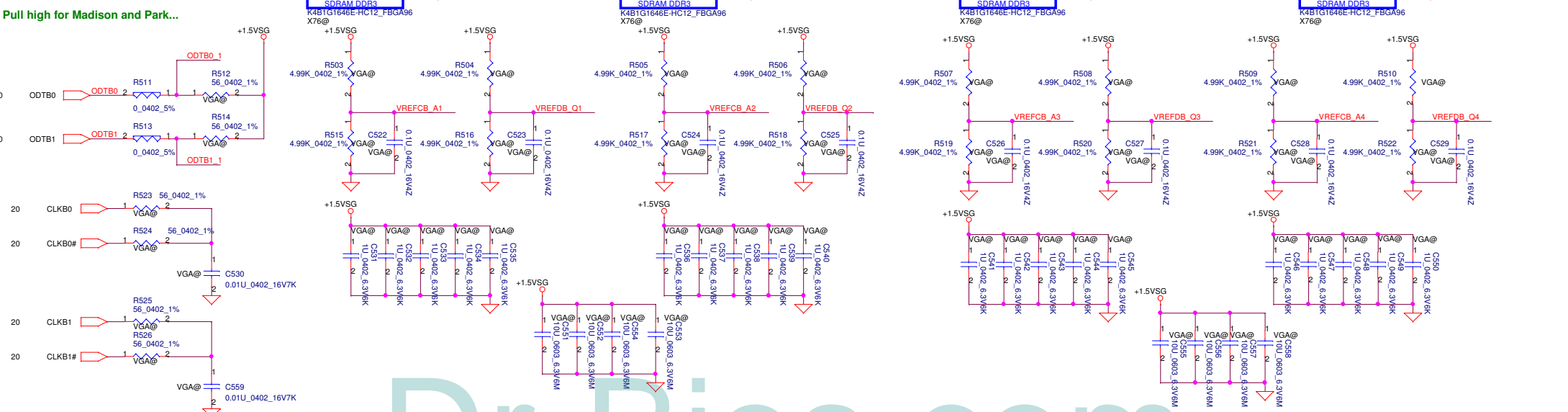
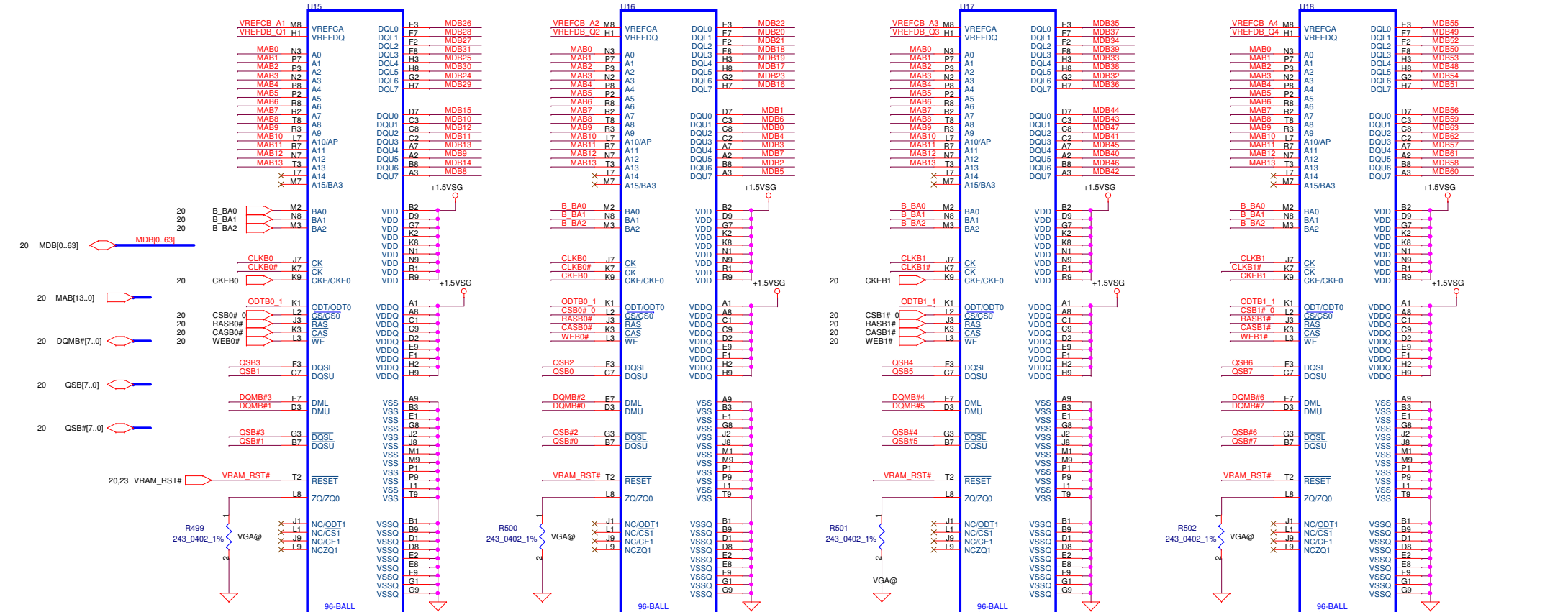
Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
 use to control discreate GPU regulators
 for power express BACO mode
Support BACO:
 output High3.3V:turn off regulators (BACO mode on)
 output Low0V:turn on regulators (BACO mode off)
 need PD resistor
no support BACO:
 left NC

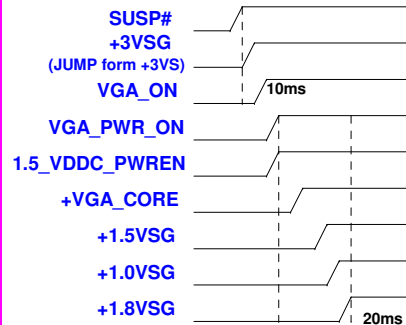


Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Compal Electronics, Inc. Vancouver Power/GND Document Number QBL60 LA-7552P Rev 1.0	
Date:	Monday, April 25, 2011	Sheet	22	of 53

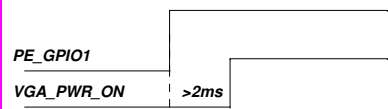




Power Sequence of Whistler and Seymour



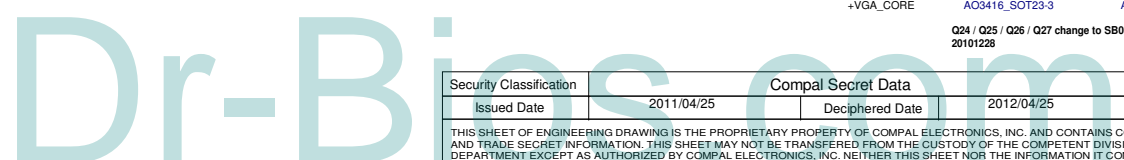
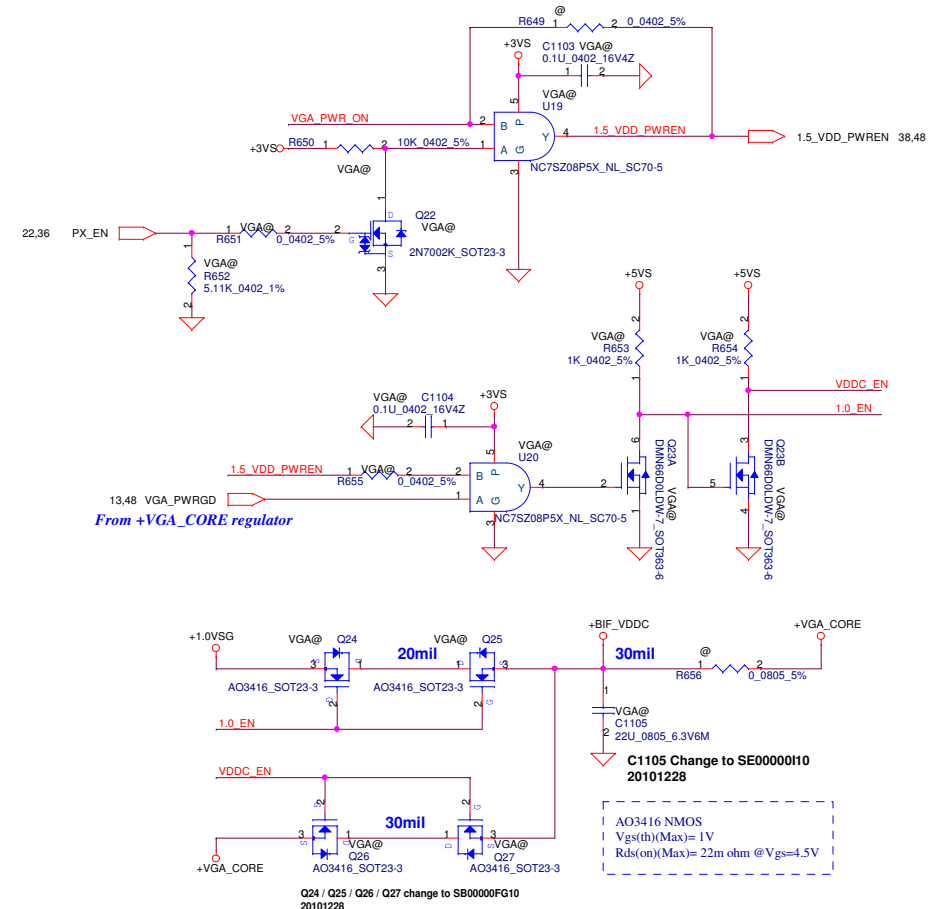
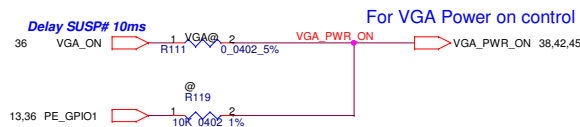
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

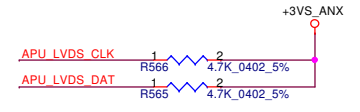
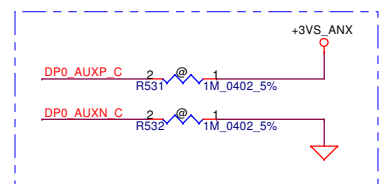
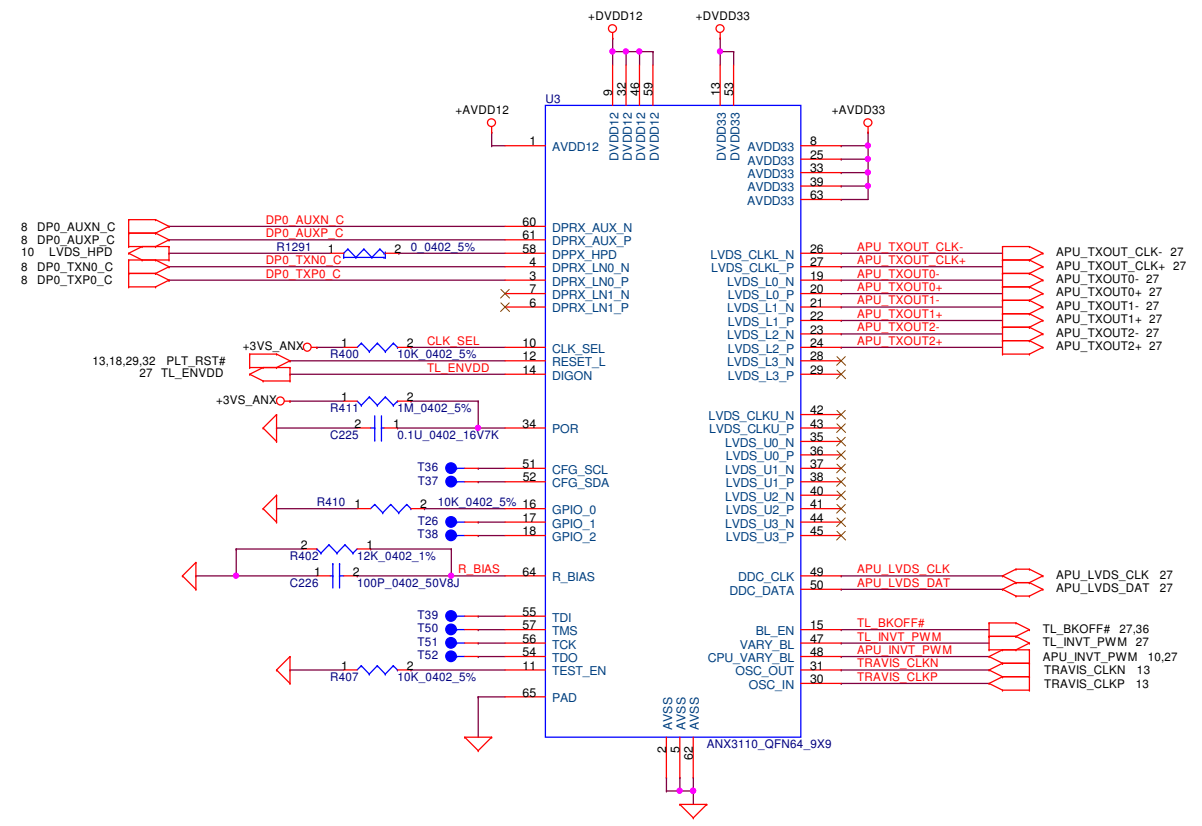
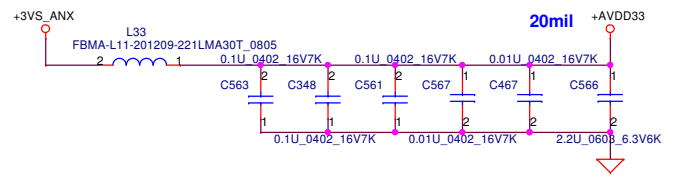
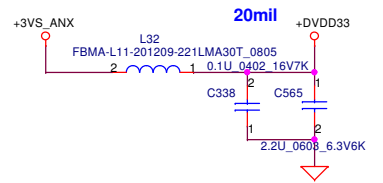
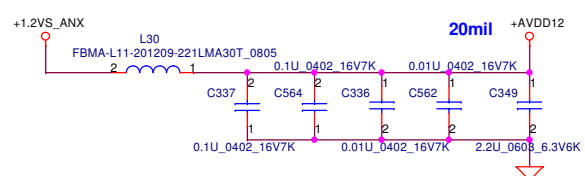
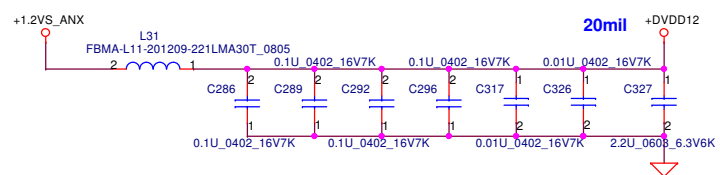
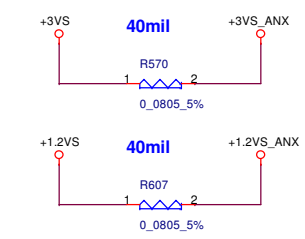


VGA Muxless with BACO Status Mapping table

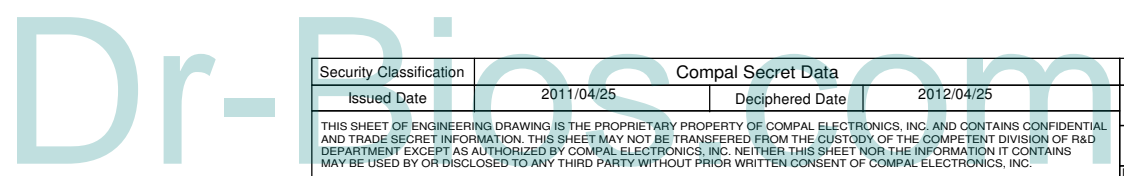
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
VGA_PWR_ON source signal	Whistler
+3.3VSG	VGA_ON
+1.8VSG	SUSP#
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN





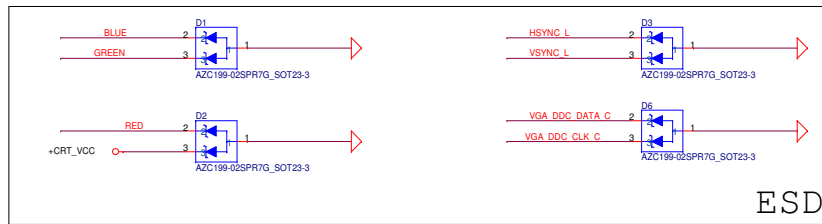
Place via on each trace bus and let resistor very close the via



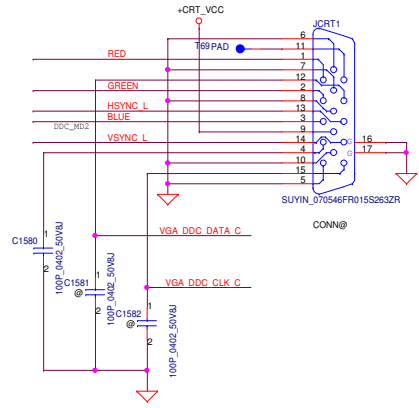
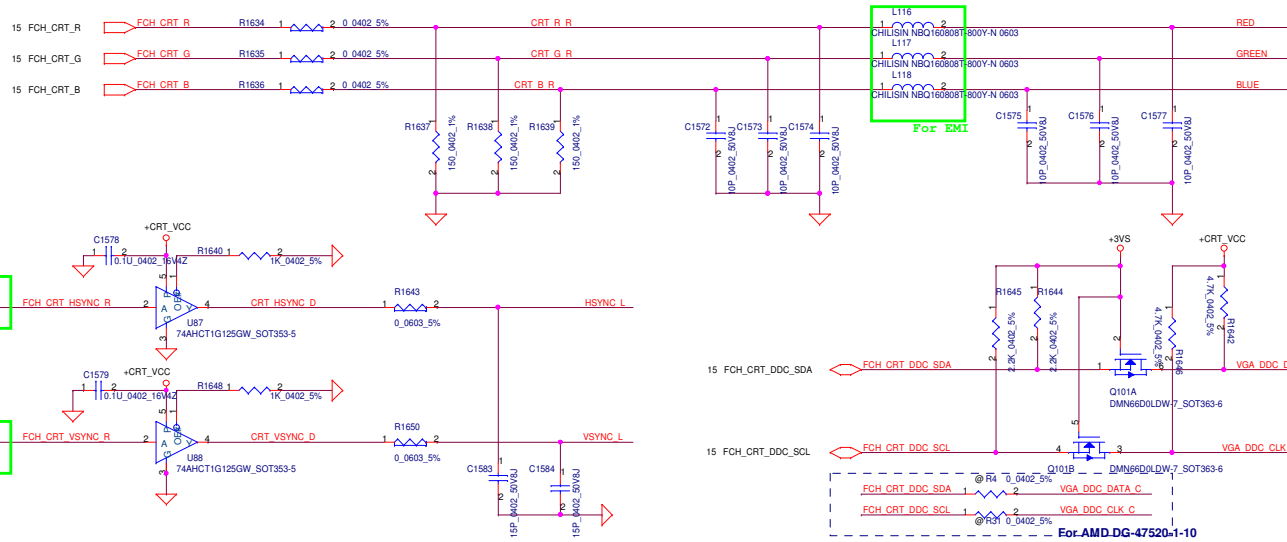
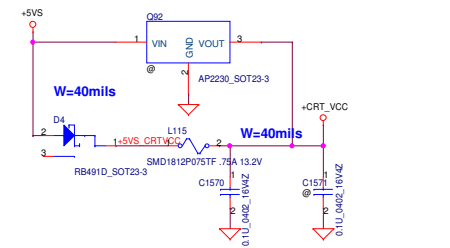
Security Classification		Compal Secret Data	
Issued Date	2011/04/25	Deciphered Date	2012/04/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.		
LVDS Translator-ANX3110		
Size	Document Number	Rev
Custom	QBL60 LA-7552P	1.0
Date:	Monday, April 25, 2011	Sheet 26 of 53

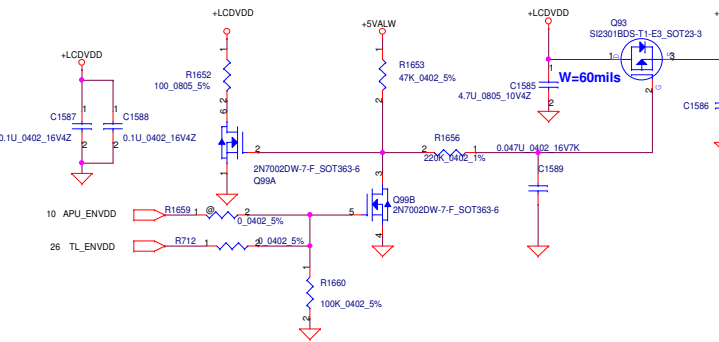
CRT



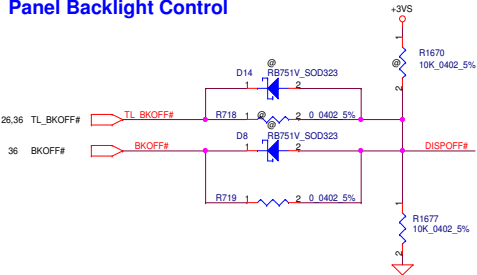
ESD



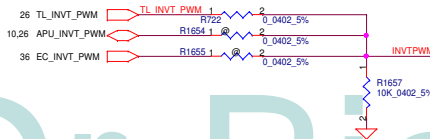
Panel LCDVDD Control



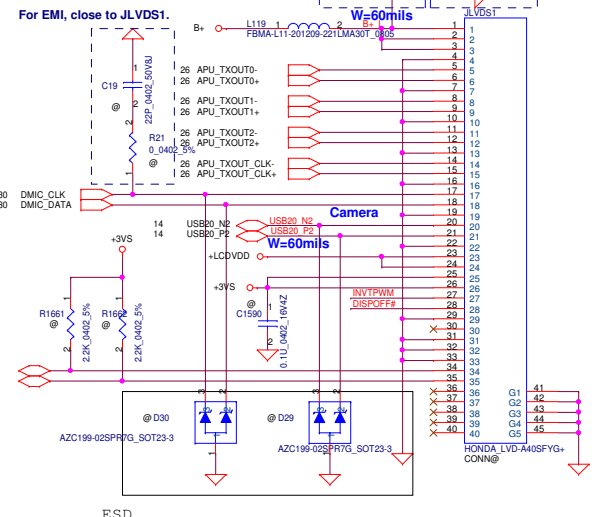
Panel Backlight Control



Panel PWM Control

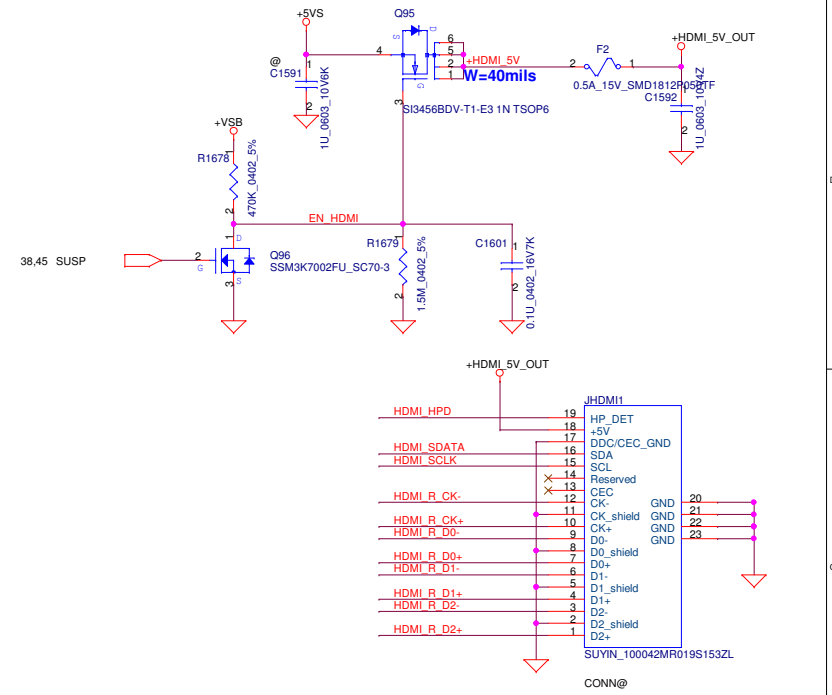
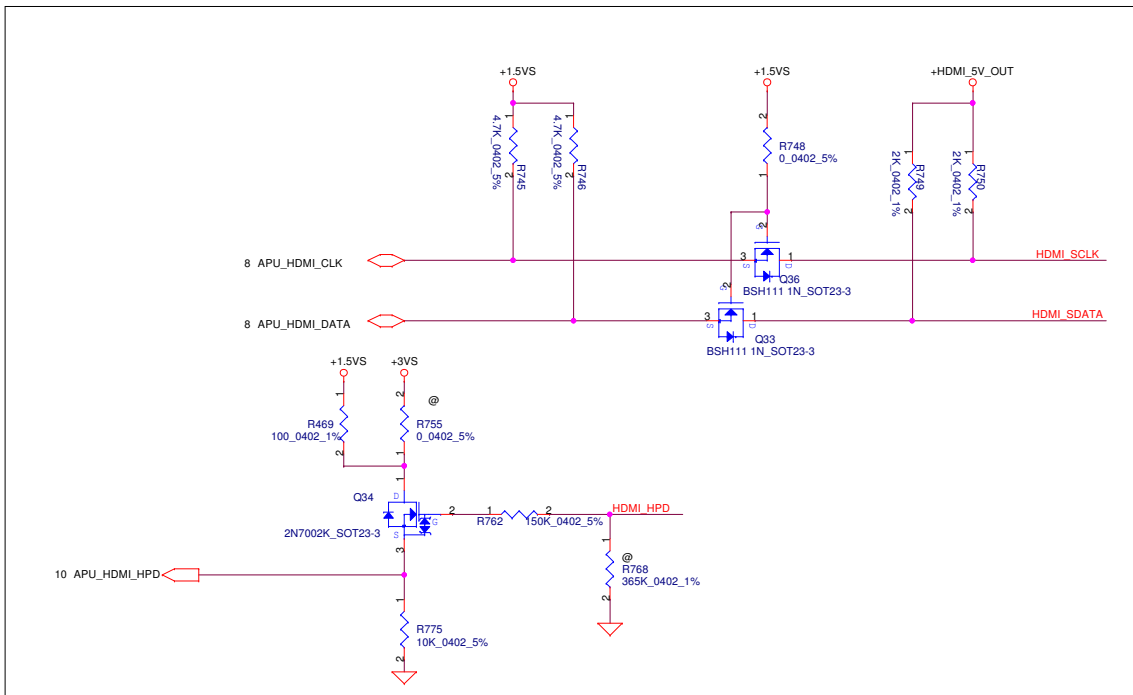


For EMI, close to JLVDS1.



ESD

Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Issued Date	2011/04/25	P10-LVDS/CRT CONN	
Deciphered Date	2012/04/25	Size	Document Number
		QBL60 LA-7552P	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Date	Monday, April 25, 2011
		Sheet	27 of 53

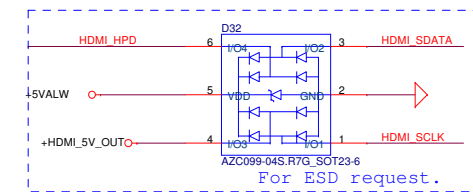
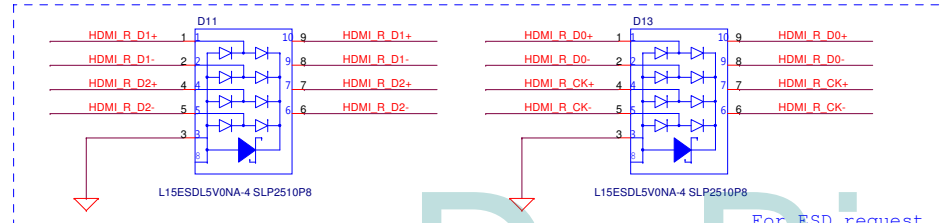
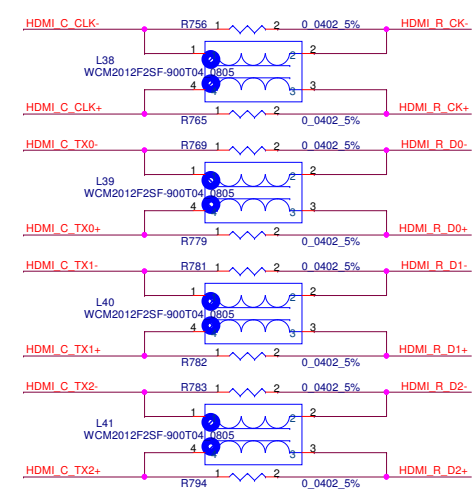
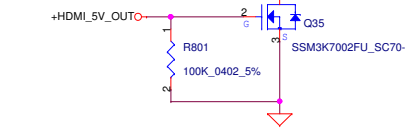


Near the connector

UMA use 604 ohm
VGA use 499 ohm

6	PCIe_FTX_GRX_N12	C1186	2	1	0.1U_0402_16V7K	HDMI_C_TX2-	R784	1	2	604_0402_1%
6	PCIe_FTX_GRX_P12	C1187	2	1	0.1U_0402_16V7K	HDMI_C_TX2+	R786	1	2	604_0402_1%
6	PCIe_FTX_GRX_N13	C1188	2	1	0.1U_0402_16V7K	HDMI_C_TX1-	R788	1	2	604_0402_1%
6	PCIe_FTX_GRX_P13	C1189	2	1	0.1U_0402_16V7K	HDMI_C_TX1+	R790	1	2	604_0402_1%
6	PCIe_FTX_GRX_N14	C1170	2	1	0.1U_0402_16V7K	HDMI_C_TX0-	R792	1	2	604_0402_1%
6	PCIe_FTX_GRX_P14	C1171	2	1	0.1U_0402_16V7K	HDMI_C_TX0+	R795	1	2	604_0402_1%
6	PCIe_FTX_GRX_N15	C1172	2	1	0.1U_0402_16V7K	HDMI_C_CLK-	R797	1	2	604_0402_1%
6	PCIe_FTX_GRX_P15	C1173	2	1	0.1U_0402_16V7K	HDMI_C_CLK+	R799	1	2	604_0402_1%

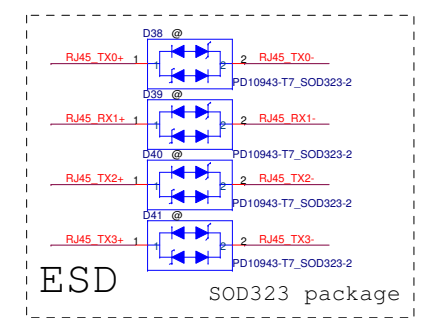
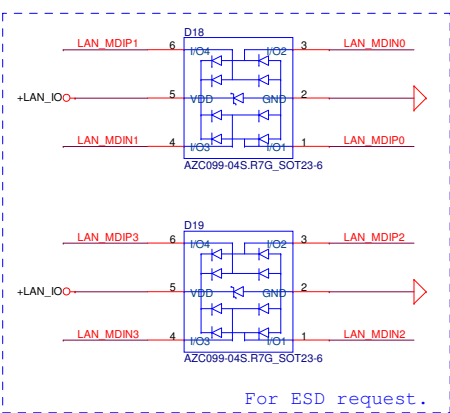
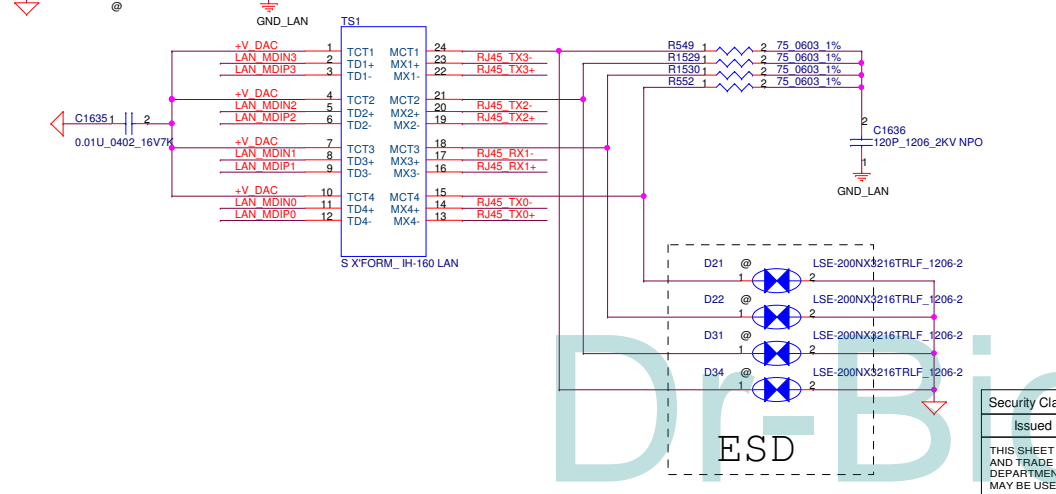
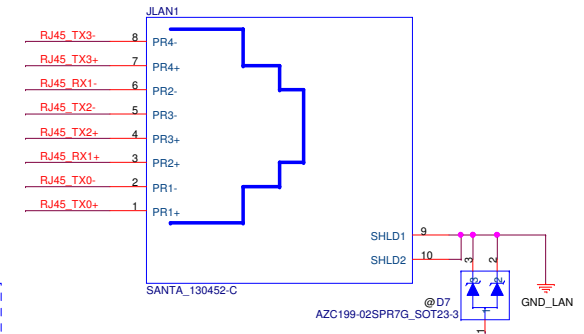
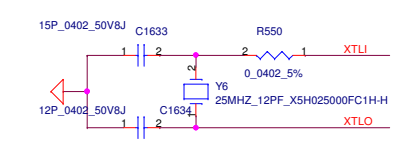
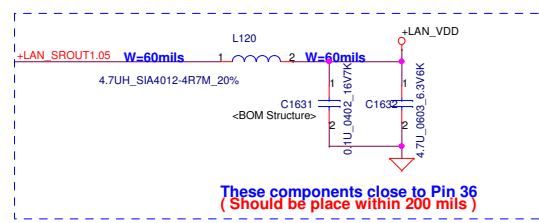
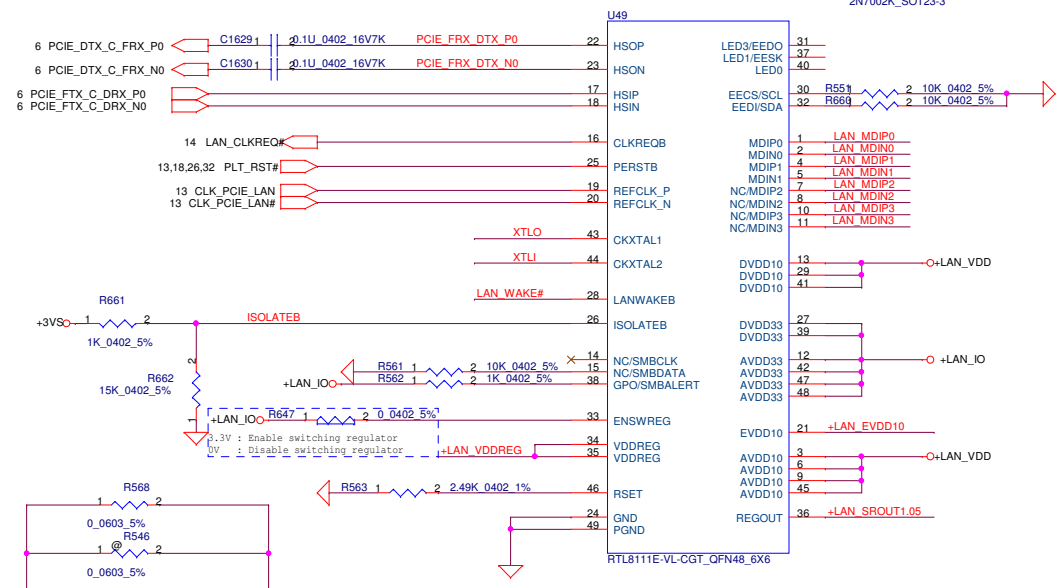
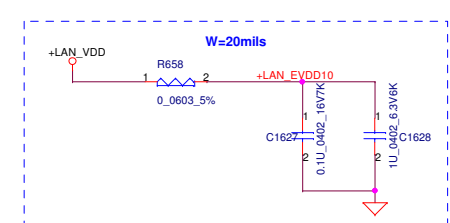
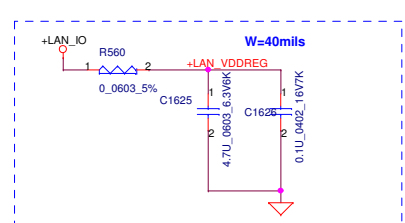
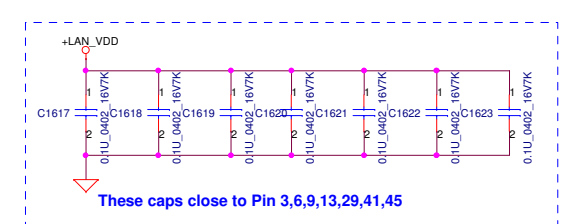
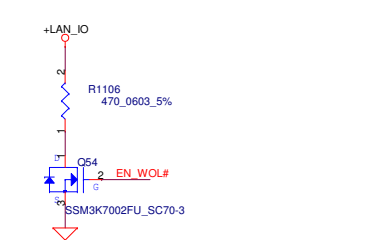
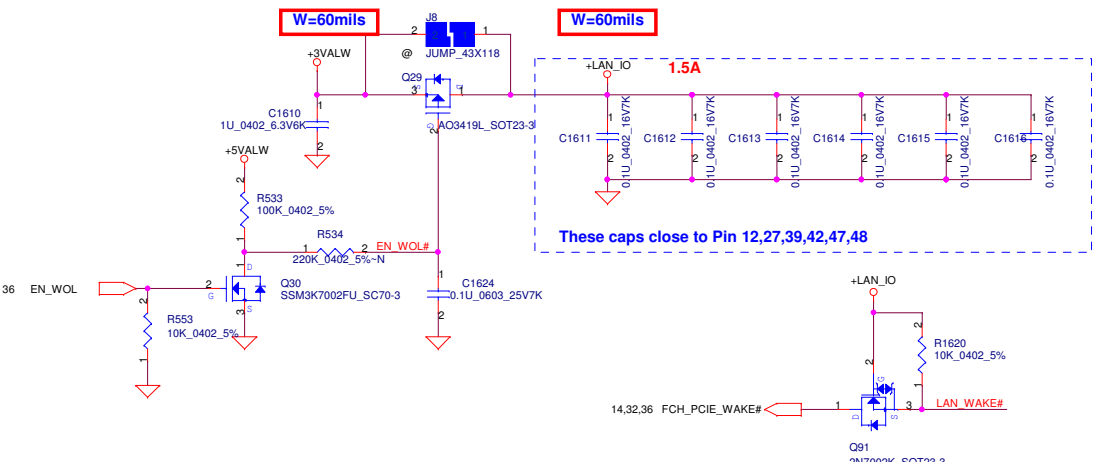
From APU



For ESD request.

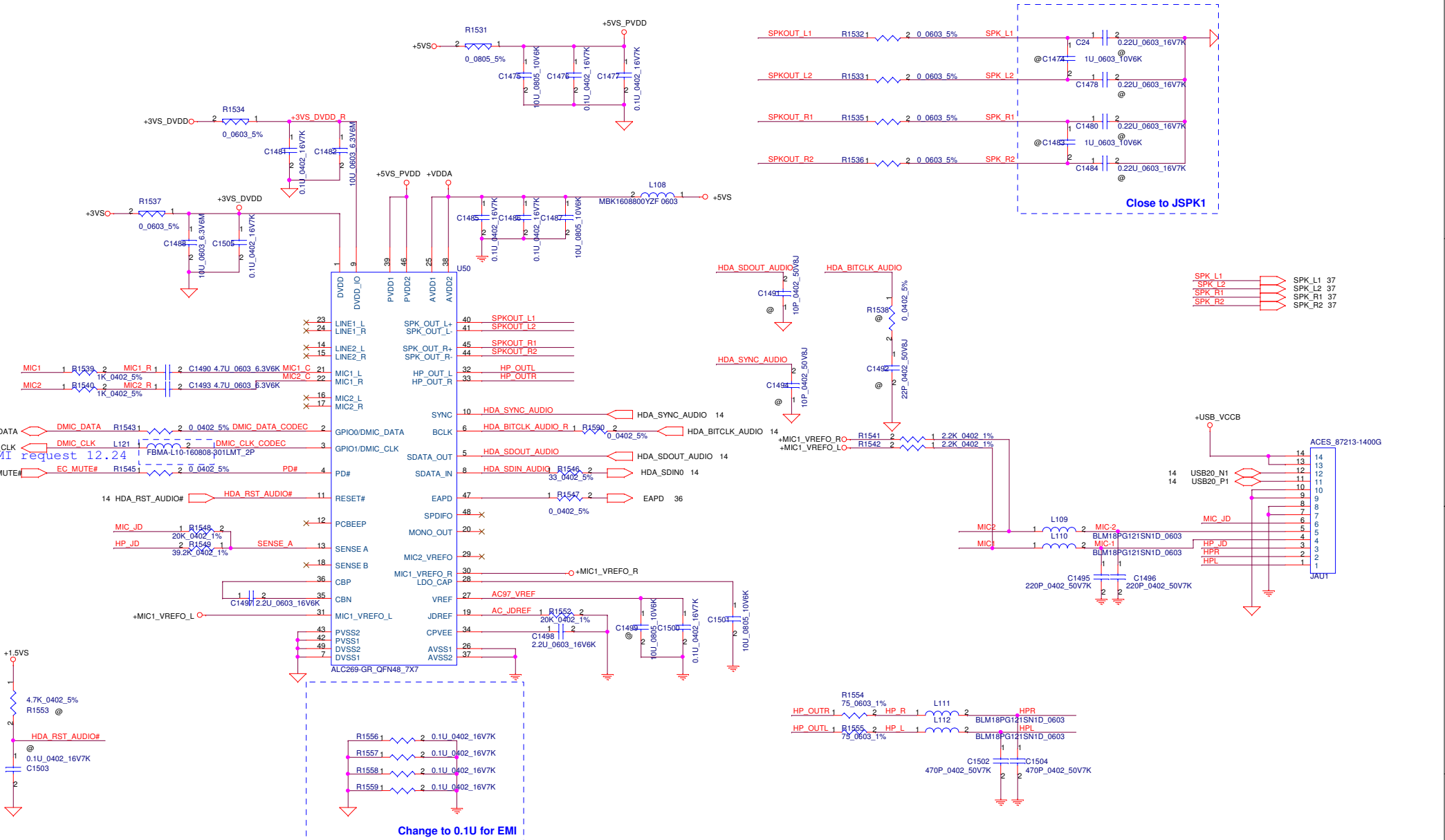
For ESD request.

Security Classification	Compal Secret Data	Title	HDMI Connector	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				QBL60 LA-7552P
Date: Monday, April 25, 2011				Rev 1.0
Sheet 28 of 53				



Security Classification	Compal Secret Data		
Issued Date	2011/04/25	Deciphered Date	2012/04/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

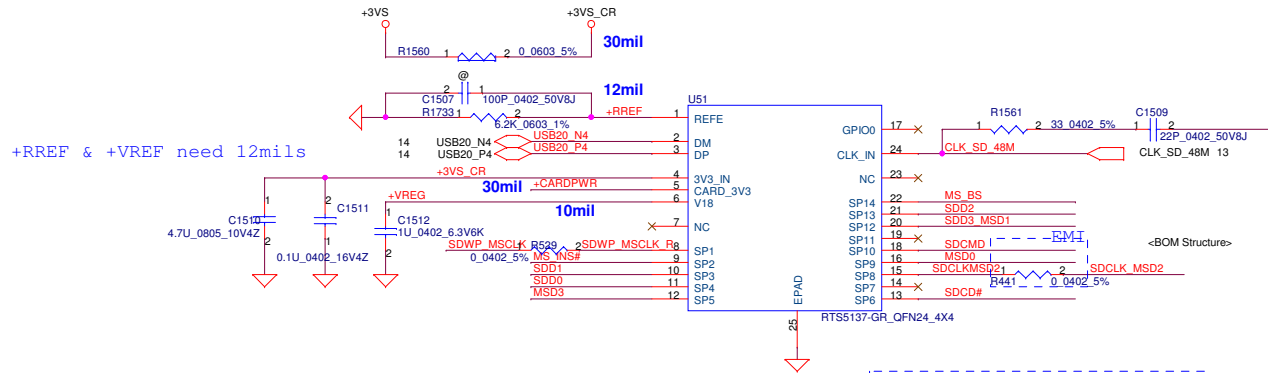
Compal Electronics, Inc.	
Title	
P25-LAN RTL8111E	
Revision	1.0
Customer	QBL60 LA-7552P
Date	Monday, April 25, 2011
Sheet	29 of 53



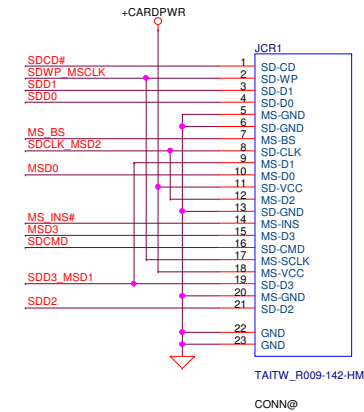
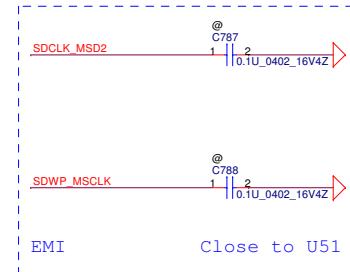
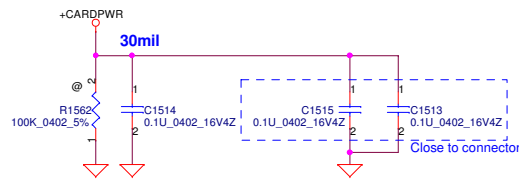
Dr-Bios.com

Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.
Issued Date	2011/04/25	Deciphered Date	2012/04/25
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>		Part Number QBL60 LA-7552P	Rev 1.0
Date:	Monday, April 25, 2011	Sheet	30 of 53

Card Reader RTS5137 (only SD/MMC/MS function)



Card Reader Connector

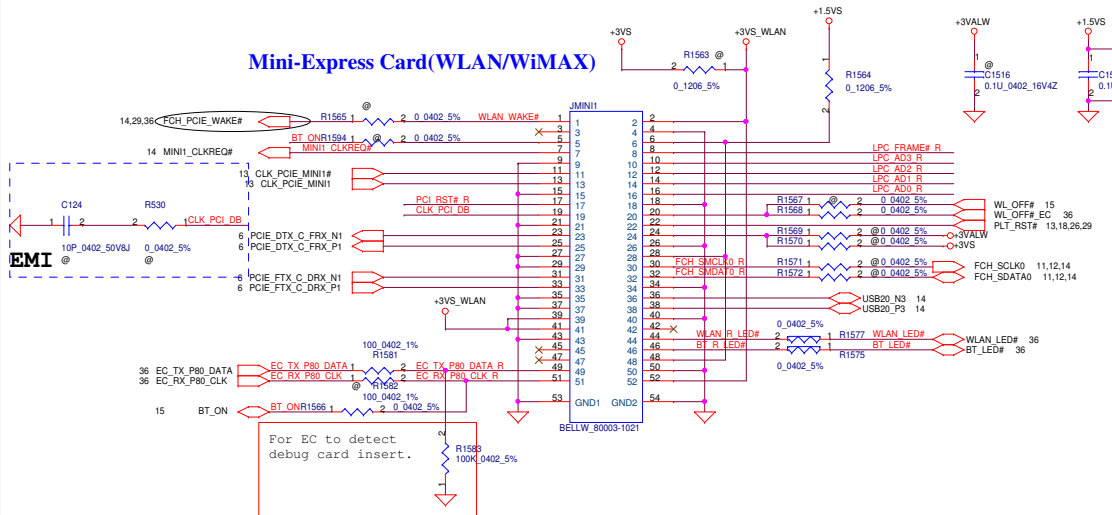


Dr-Bios.com

Security Classification	2011/04/25	Compal Secret Data	2012/04/25	Title	Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Rev	P27-RTS5137 Media Card Controller	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc Number	QBL60 LA-7552P	Rev 1.0
				Date:	Monday, April 25, 2011	Sheet 31 of 53

Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)

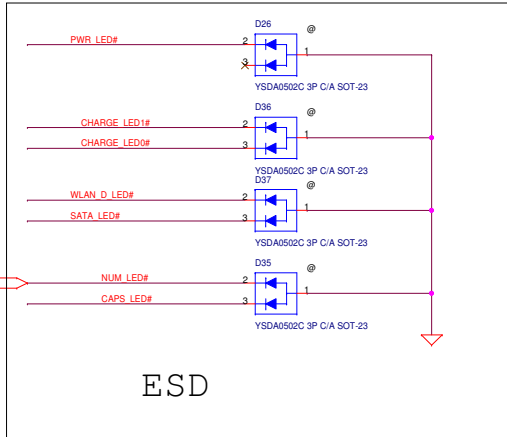
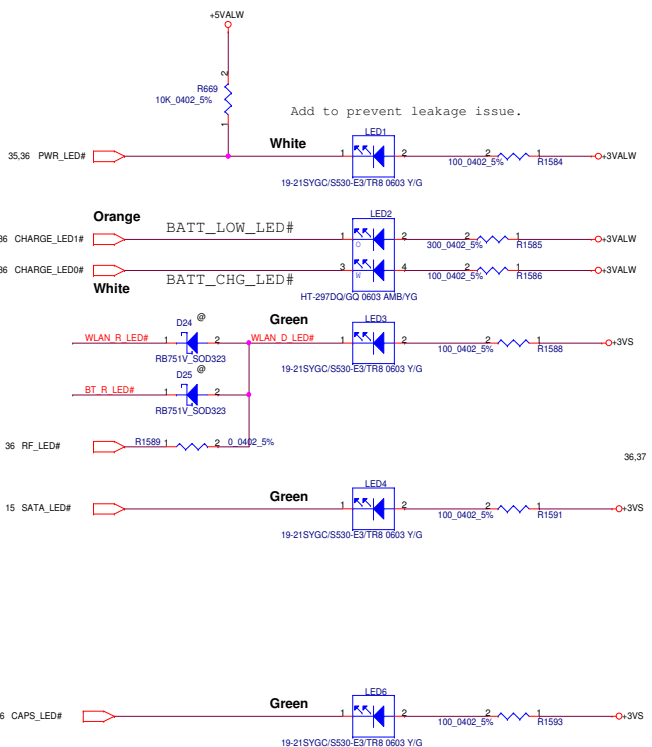


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R1573	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	13,36
LPC_AD3 R	R1574	1	2	0.0402 5%	LPC_AD3	LPC_AD3	13,36
LPC_AD2 R	R1576	1	2	0.0402 5%	LPC_AD2	LPC_AD2	13,36
LPC_AD1 R	R1578	1	2	0.0402 5%	LPC_AD1	LPC_AD1	13,36
LPC_AD0 R	R1579	1	2	0.0402 5%	LPC_AD0	LPC_AD0	13,36
PLT_RST#	R1580	1	2	0.0402 5%	PLT_RST#	PLT_RST#	13
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB	13

For EC to detect debug card insert.

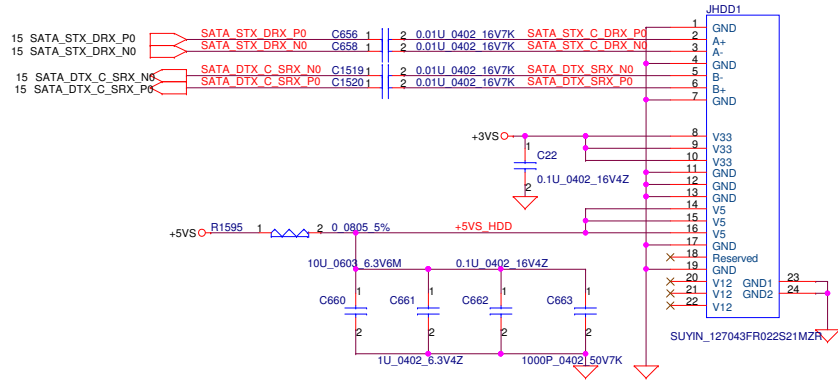
LED



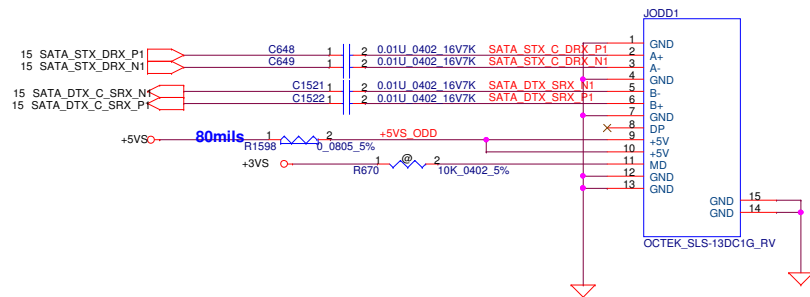
ESD

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/04/25		2012/04/25		P28-Mini PCI/E/LD	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number	
		QBL60 LA-7552P		Rev 1.0	
Date		Monday, April 25, 2011		Sheet 32 of 53	

SATA HDD Conn.

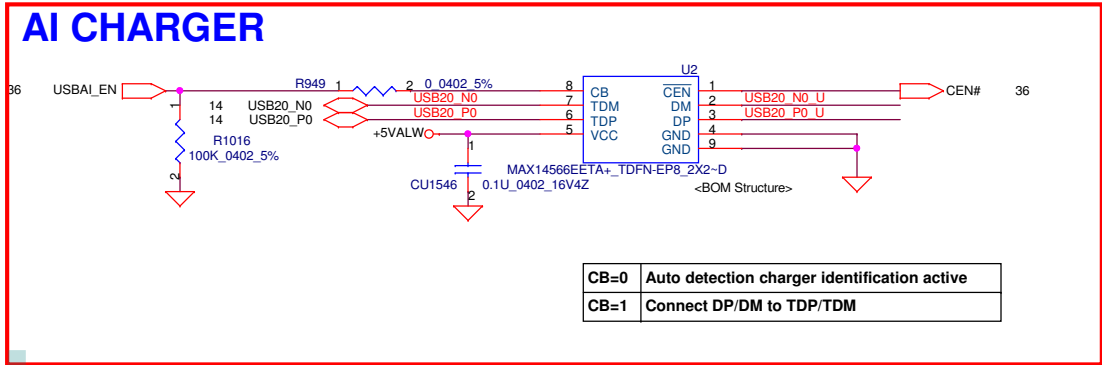
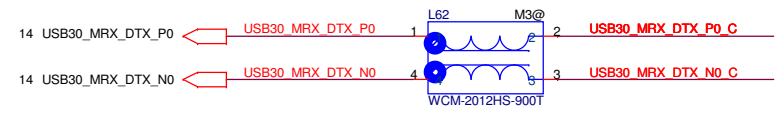
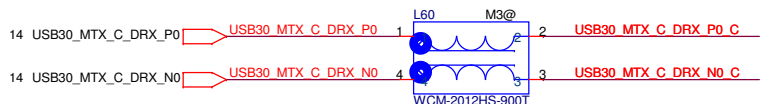
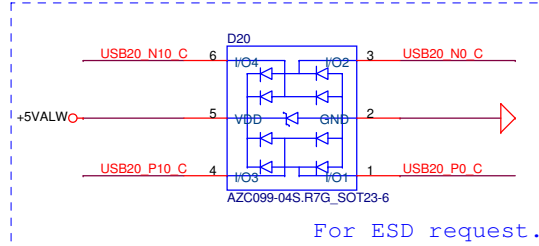
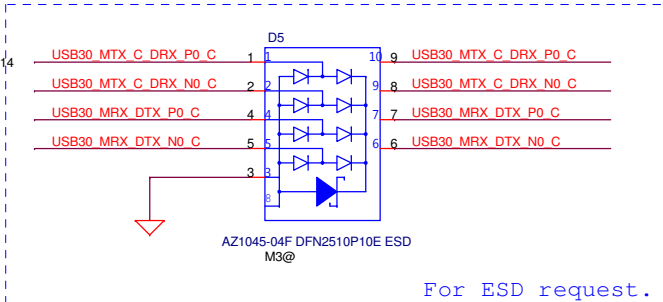
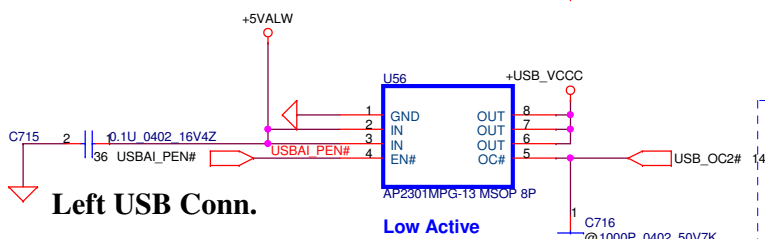
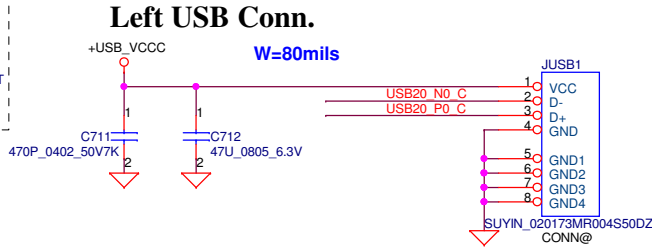
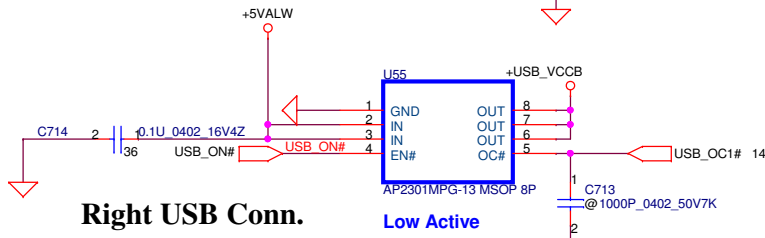
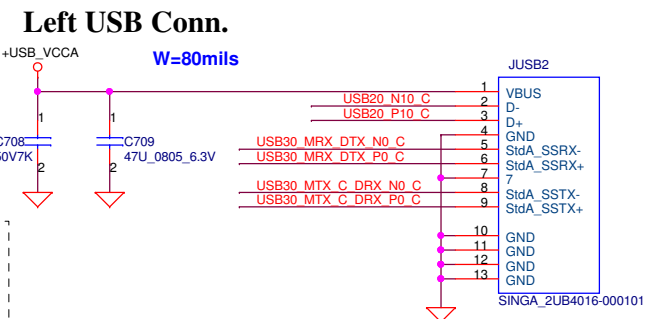
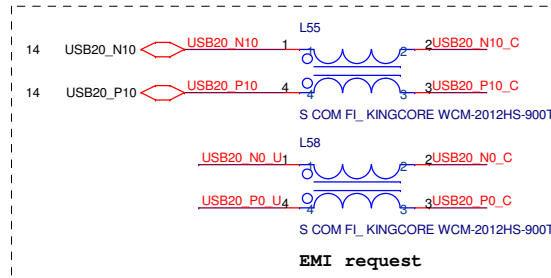
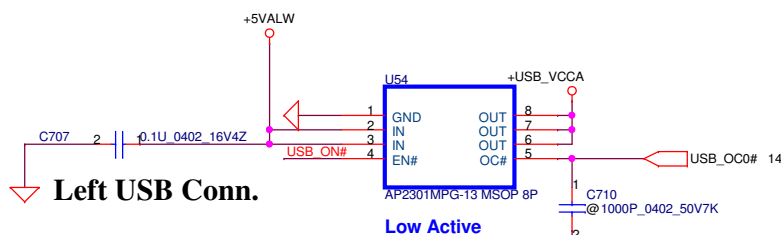


SATA ODD FFC Conn.



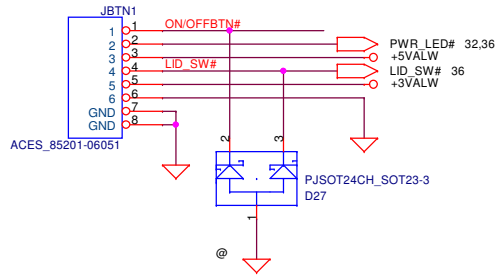
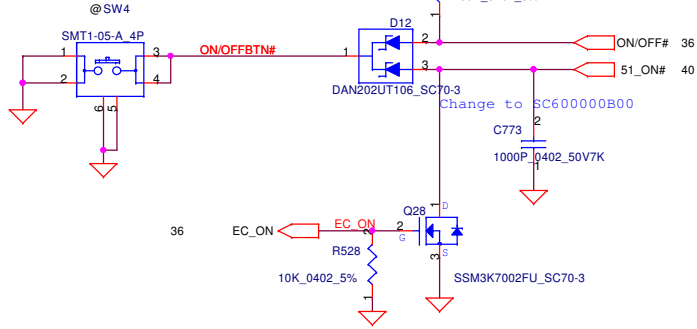
Dr-Bios.com

Security Classification	2011/04/25	Deciphered Date	2012/04/25	Title	Compal Electronics, Inc.
Issued Date				P29-HDD & ODD CONN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTS B DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				QBL60 LA-7552P	1.0
				Date: Monday, April 25, 2011	Sheet 33 of 53

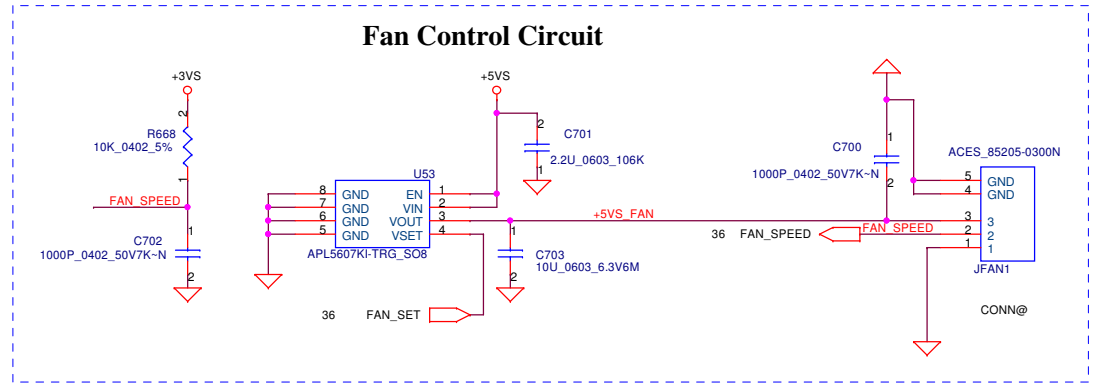


ON/OFF switch Power Button

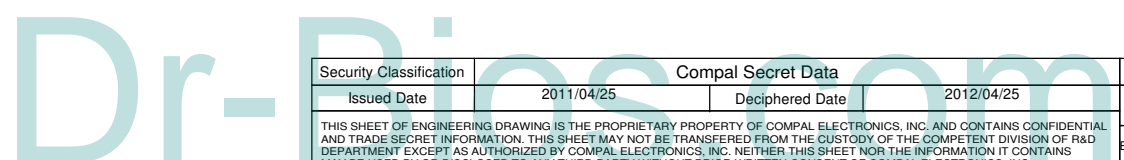
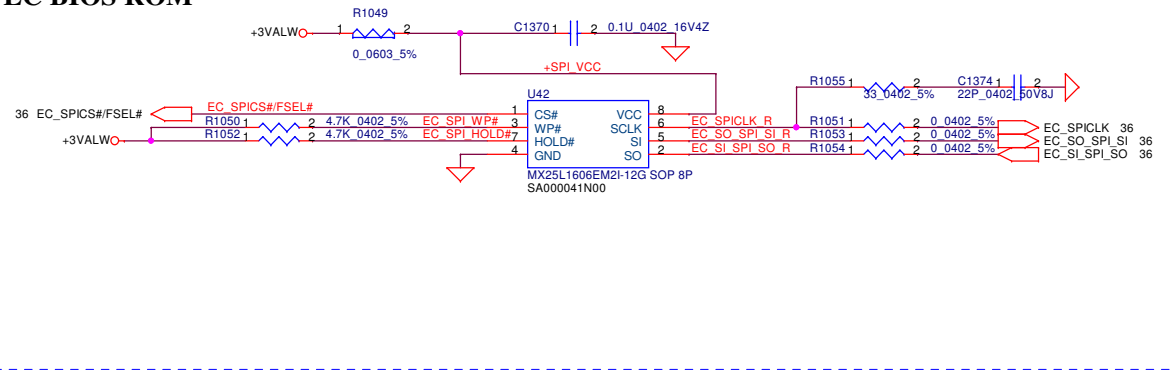
Place SW4 on Bottom Side.



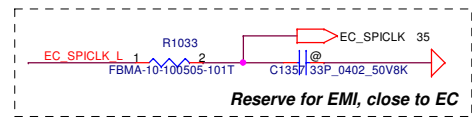
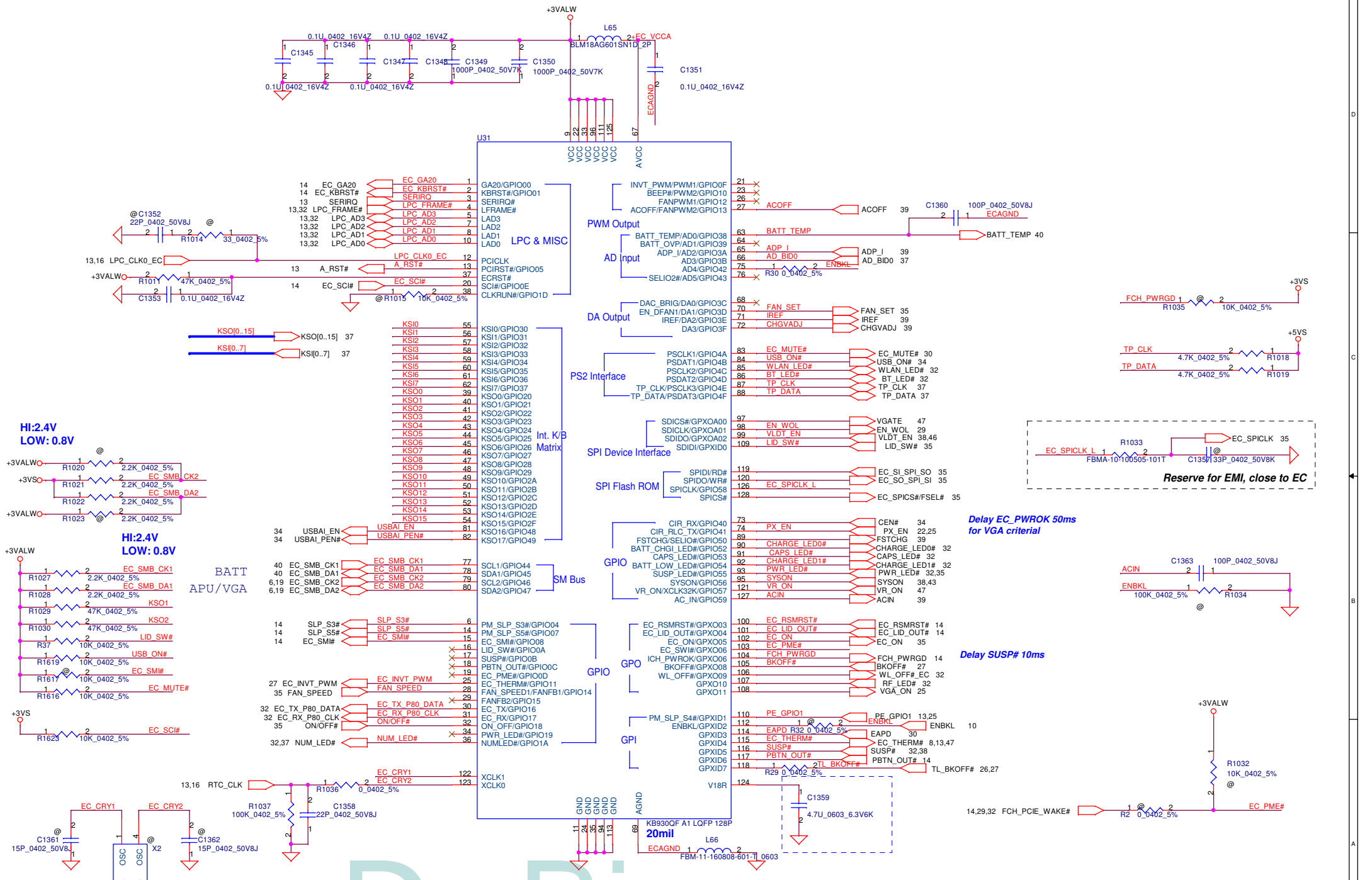
Fan Control Circuit



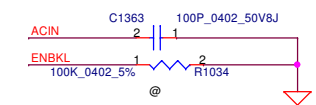
EC BIOS ROM



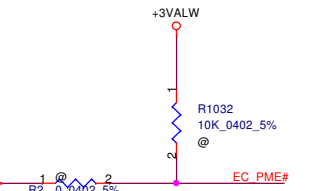
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
				P31-KB /SW/TP/Lid	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				QBL60 LA-7552P	
				Date:	Monday, April 25, 2011
				Sheet	35 of 53
				Rev	1.0



Delay EC_PWROK 50ms for VGA criteria

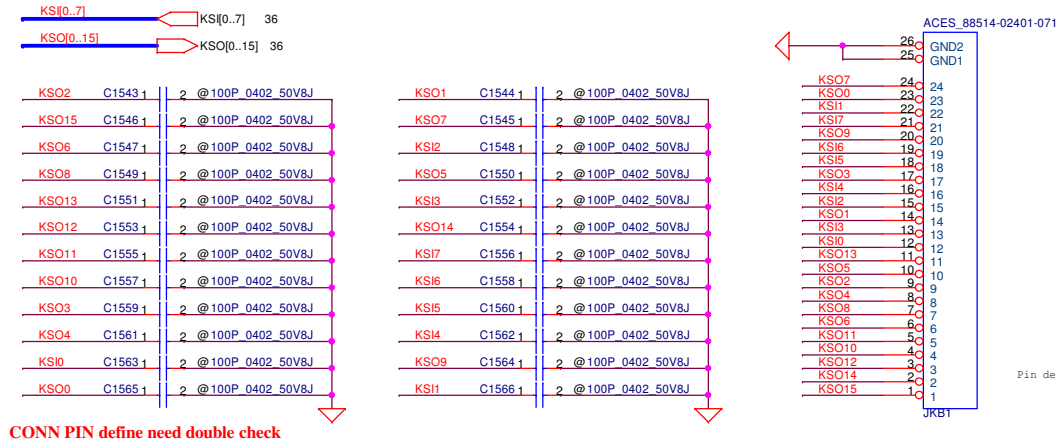


Delay SUSP# 10ms

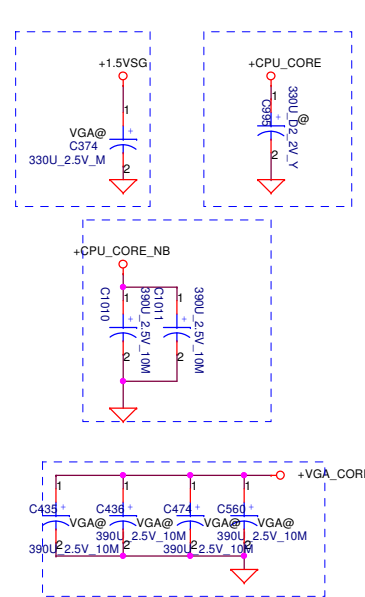


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				EC ENE KB930	
Size	Document Number	Date:		Rev	1.0
B	QBL60 LA-7552P	Monday, April 25, 2011		Sheet	36 of 53

INT_KBD Conn.

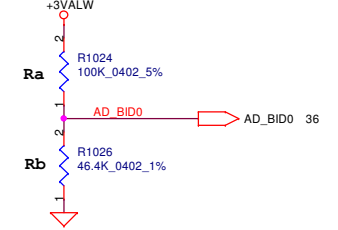


CONN PIN define need double check

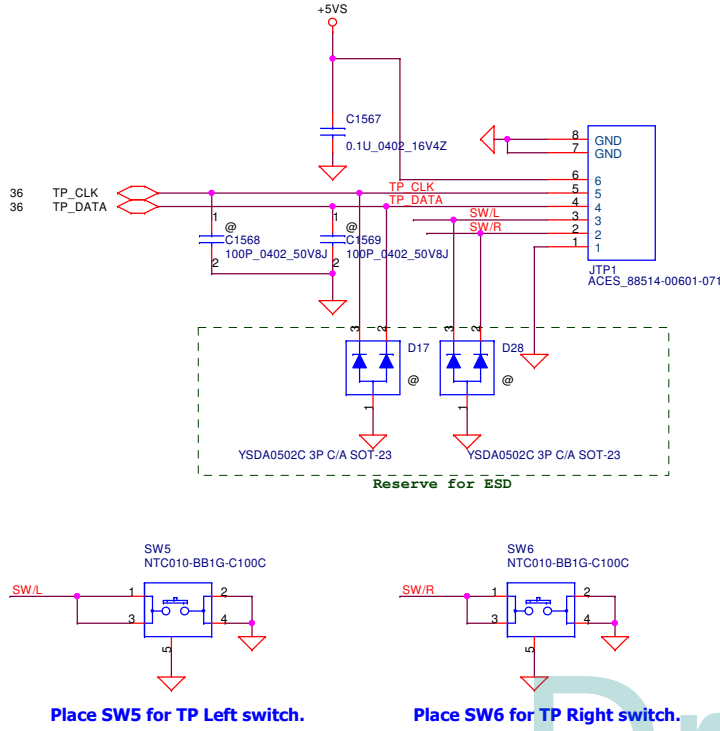


ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R10 PR	100K	46.4K	1.045V
3	Reserve	100K	56.2K	1.187V

Analog Board ID definition

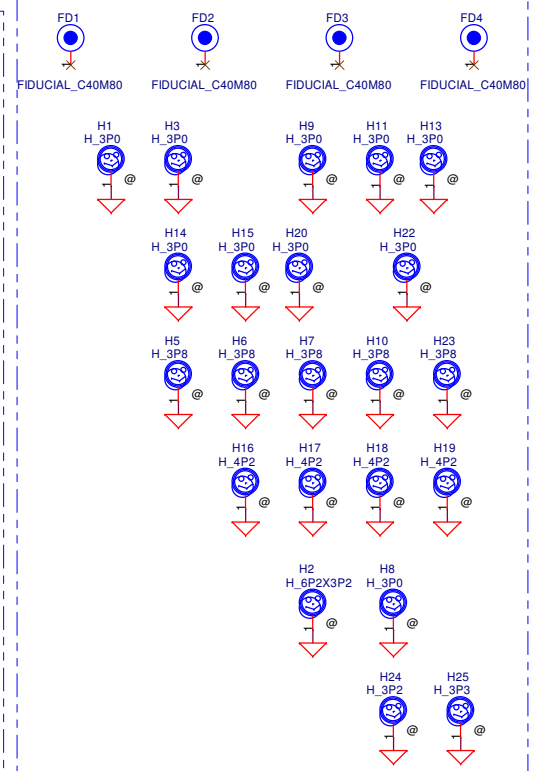
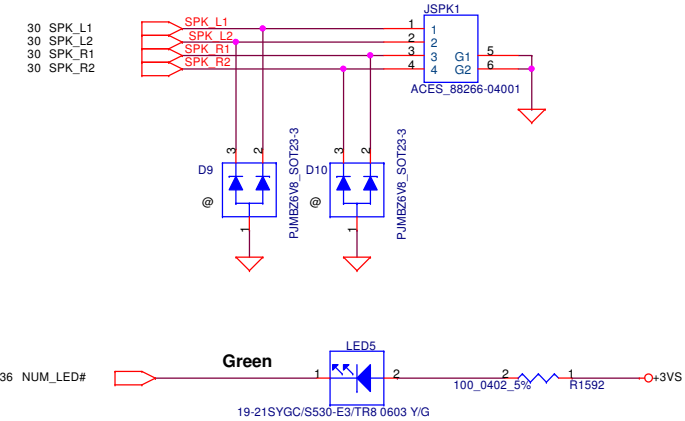


To TP/B Conn.



Place SW5 for TP Left switch.

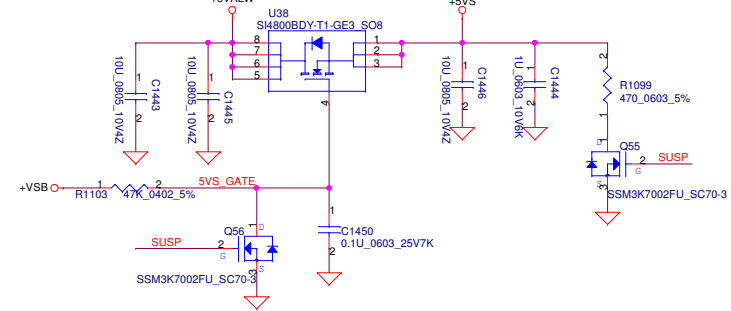
Place SW6 for TP Right switch.



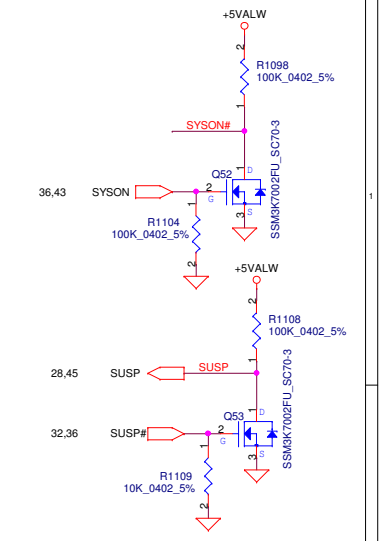
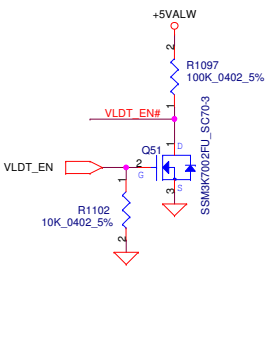
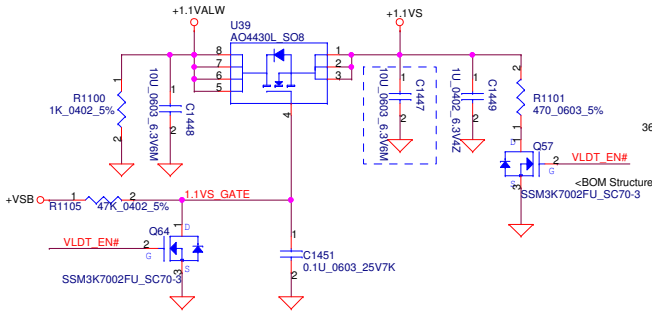
Security Classification	Compal Secret Data	
Issued Date	2011/04/25	Deciphered Date
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		

Compal Electronics, Inc.		
Title		
P33-Other IO/USB (right)		
Size	Document Number	Rev
Custom	QBL60 LA-7552P	1.0
Date:	Monday, April 25, 2011	Sheet 37 of 53

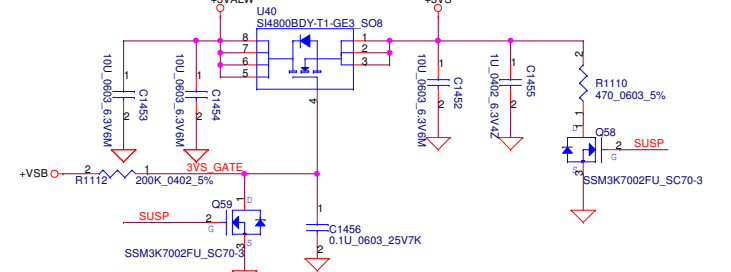
+5VALW TO +5VS (5A)



+1.1VALW TO +1.1VS (1.1A)

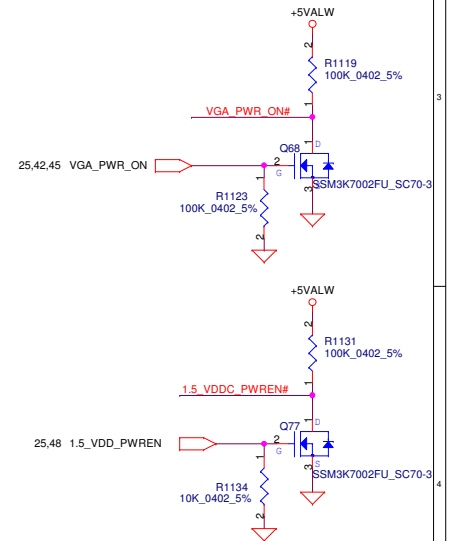
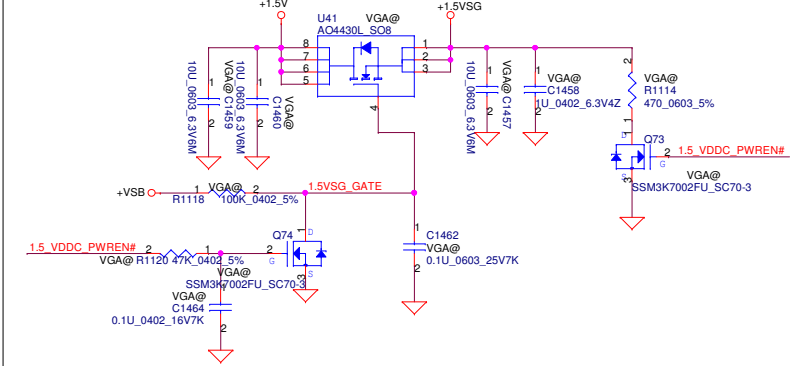


+3VALW TO +3VS (3.3A)

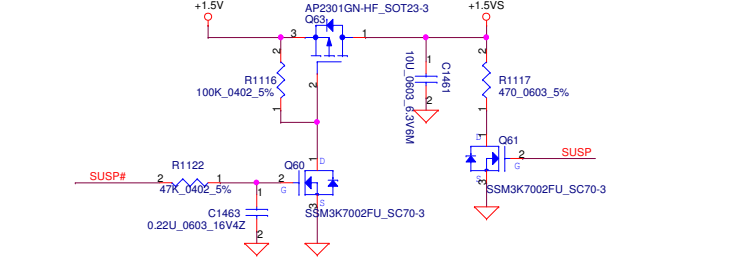


VGA Power

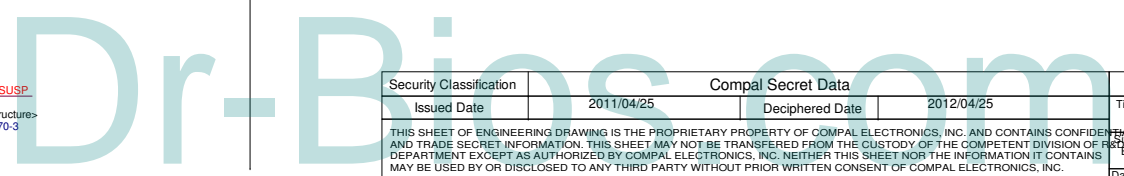
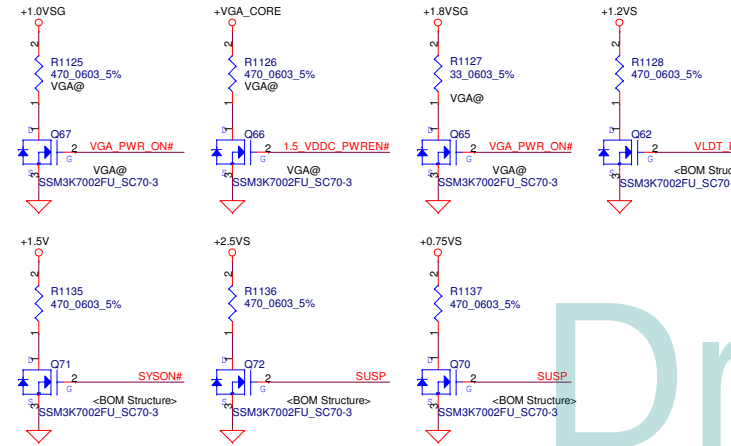
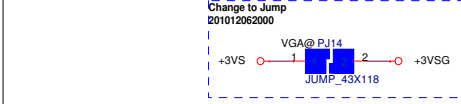
+1.5V to +1.5VSG (1.5A)



+1.5V TO +1.5VS (1.5A)

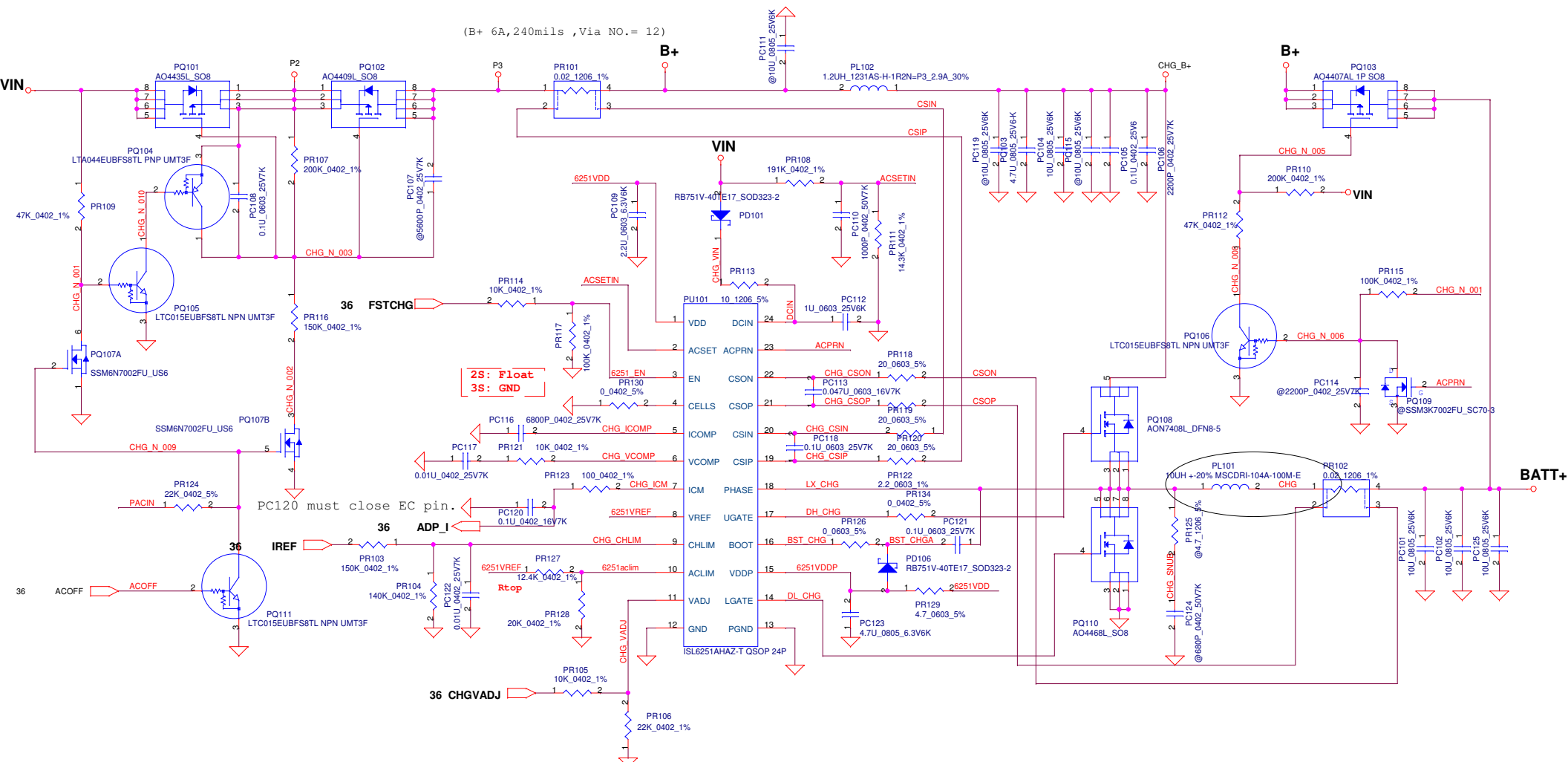


+3VS to +3VSG (3.3A)



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	DC Interface	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTS B DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Document Number	QBL60 LA-7552P			Rev	1.0
Date	Monday, April 25, 2011		Sheet	38 of 53	

(B+ 6A,240mils ,Via NO.= 12)



2S: Float
3S: GND

PC120 must close EC pin.

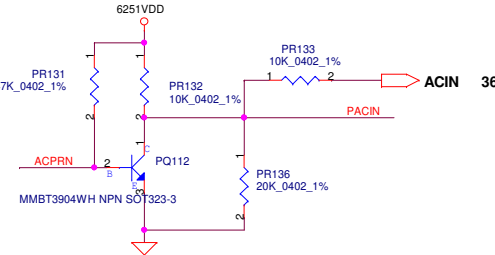
PC120 must close EC pin.

CP= 85%*I_{ada};
 I_{ada}=0~4.737A (90W); CP=4.03A; where R_{acdet}=0.020ohm, where R_{top}=12.4K
 90W for Dis: R_{top}:SD00000AJ80
 I_{ada}=0~3.421A (65W); CP=2.91A; where R_{acdet}=0.020ohm, where R_{top}=226K
 65W for UMA: R_{top}:SD034226380
 Astro2010_01_15 need confirm P/N

CP mode
 Va_{clim}=V_{REF}*(R_{bot}//R_{internal}/(R_{top}//R_{internal}+R_{bot}//R_{internal}))
 when 90W Va_{clim}=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
 when 65W Va_{clim}=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
 I_{input}=(1/R_{acdet})*(0.05*Va_{clim}/V_{REF}+0.05)
 when 90W, I_{input}=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
 when 65W, I_{input}=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

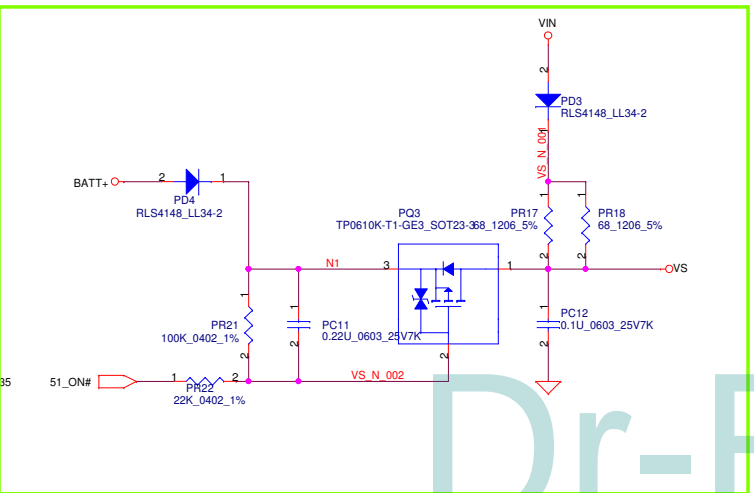
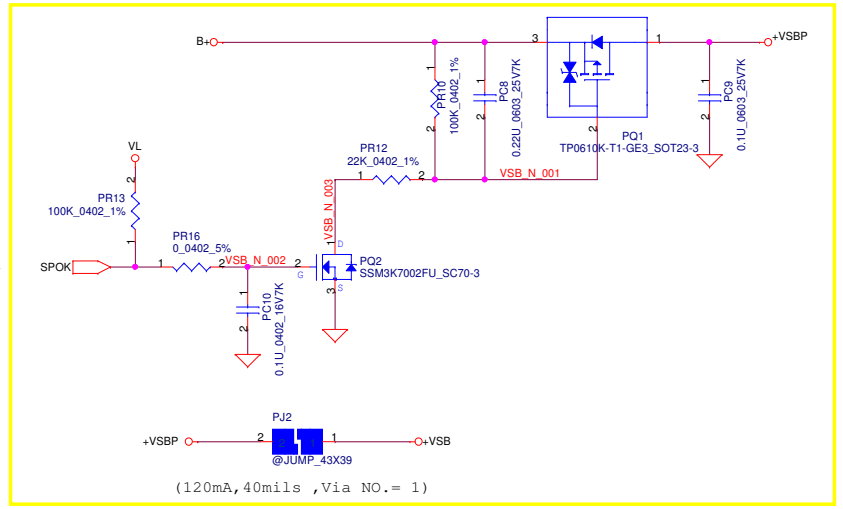
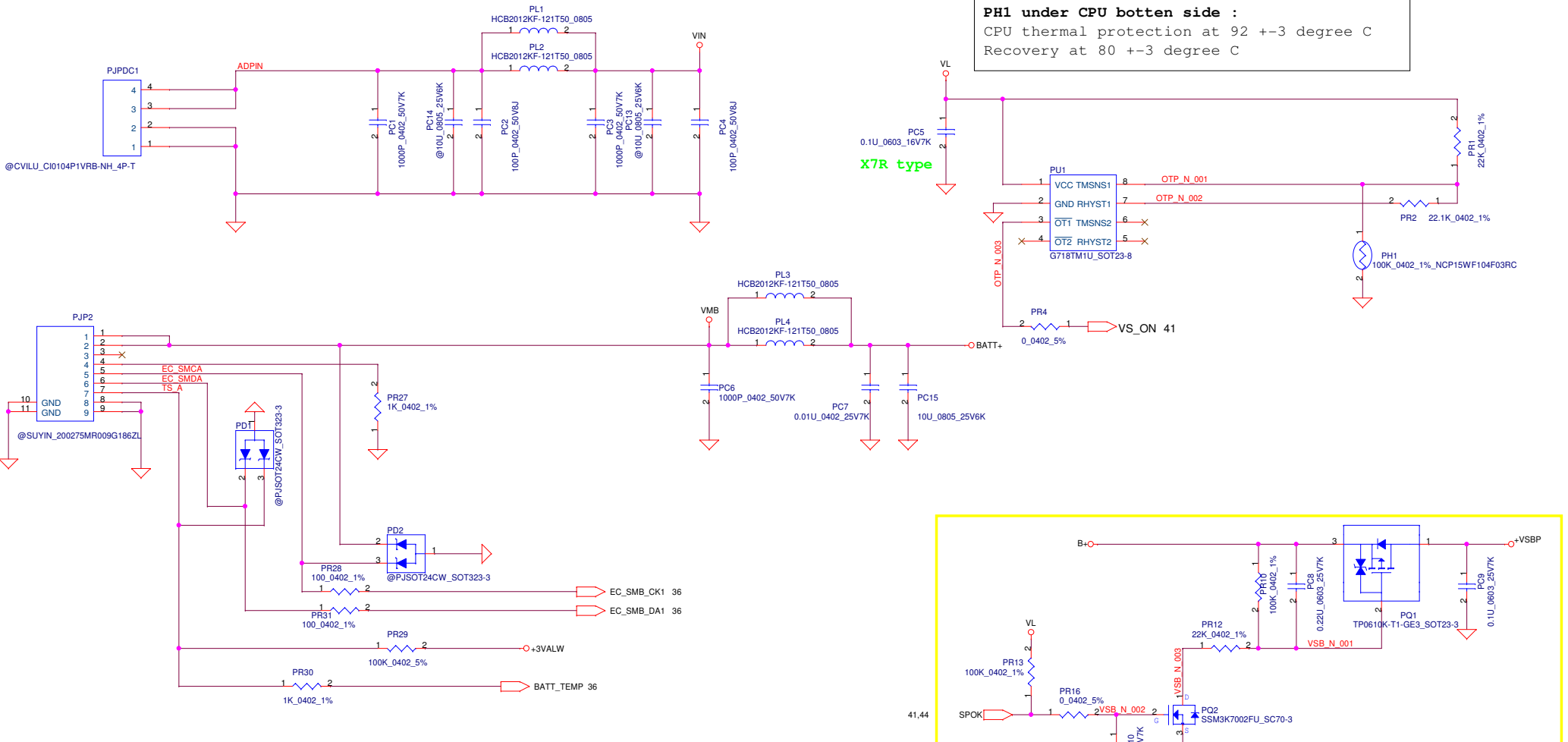
CC=0.25A-3A
 I_{REF}=1.016*I_{charge}
 I_{REF}=0.254V-3.048V
 V_{CHLIM} need over 95mV

CHGVADJ=(V _{cell} -4)/0.10627	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V

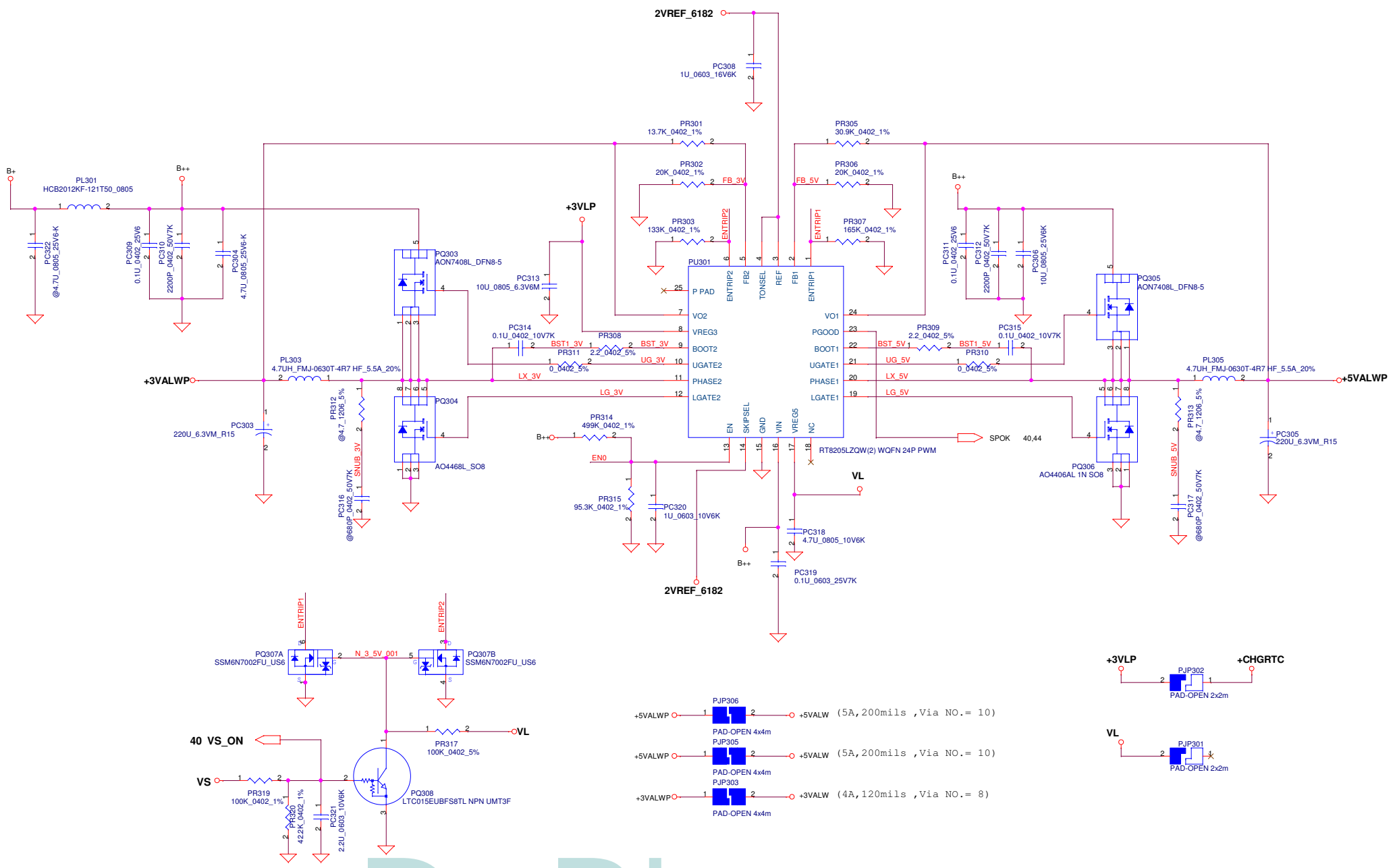


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CHARGER	
Size	Document Number	NCL61 LA-6321P/M/B		Rev	
Date:	Monday, April 25, 2011	Sheet	39	of 53	

PH1 under CPU bottom side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C

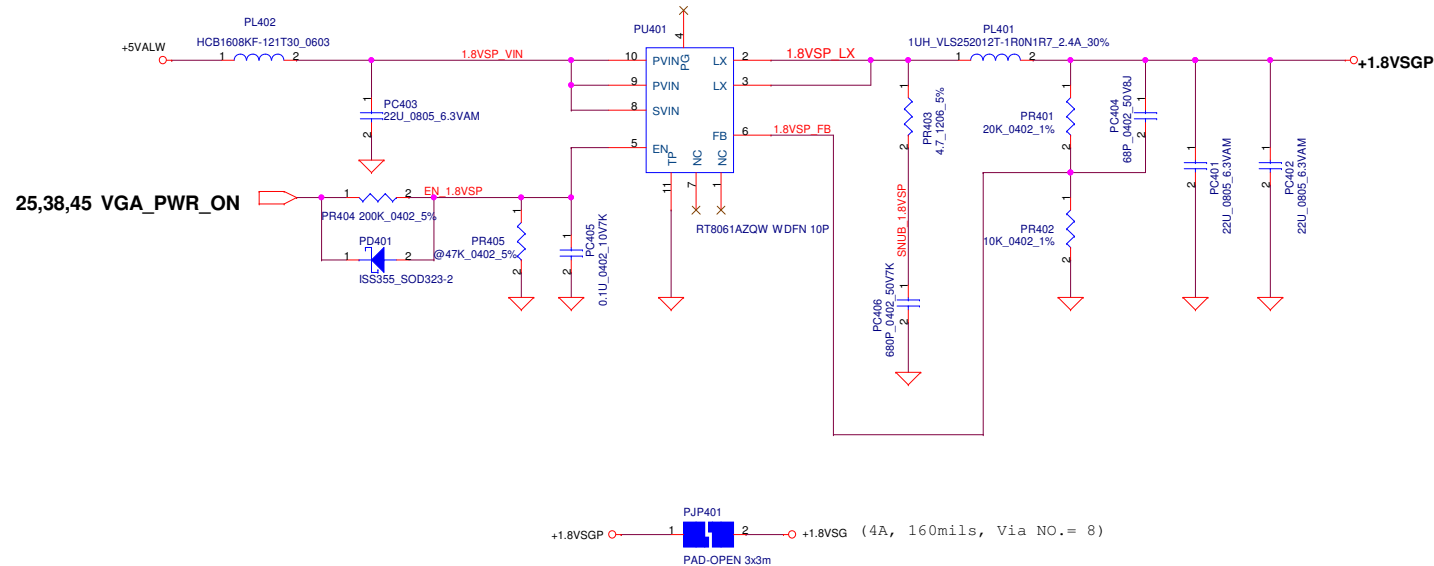


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				NCL61 LA-632IP M/B	
				Date:	Monday, April 25, 2011
				Sheet	40 of 53
				Rev	1.0



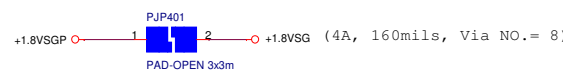
EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data	Title	3.3VALWP/5VALWP	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev
Date: Monday, April 25, 2011				1.0
Sheet 41 of 53				



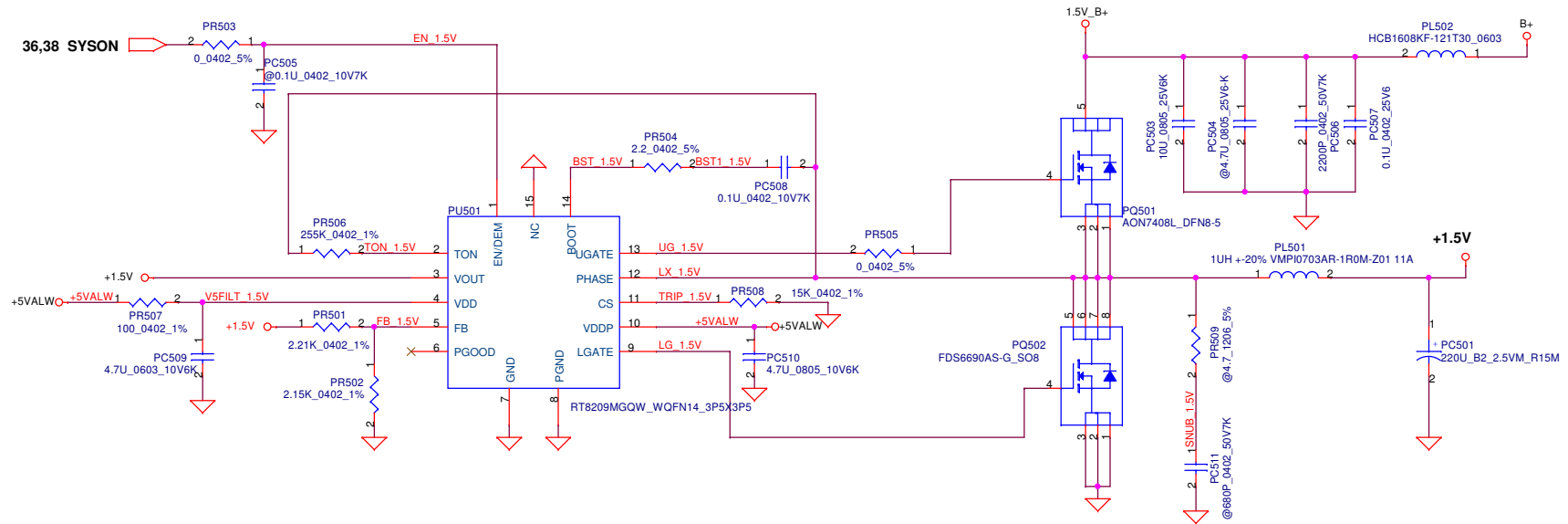
$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$

25,38,45 VGA_PWR_ON

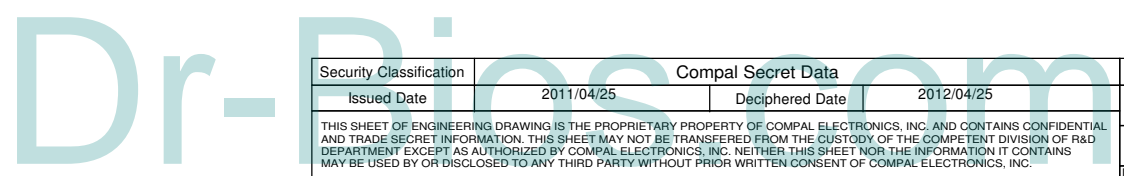


Dr-Bios.com

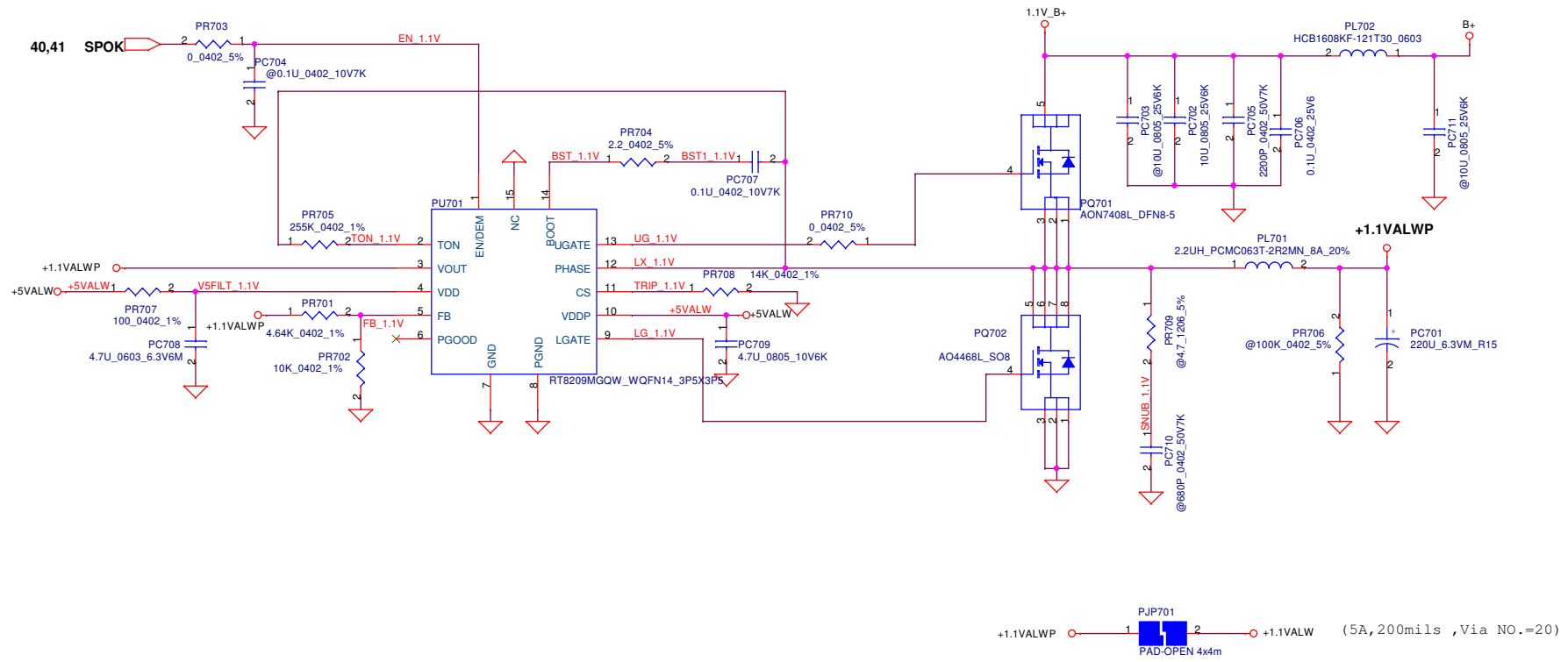
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				NCL61 LA-6321P M/B	
				Rev	1.0
				Date:	Monday, April 25, 2011
				Sheet	42 of 53



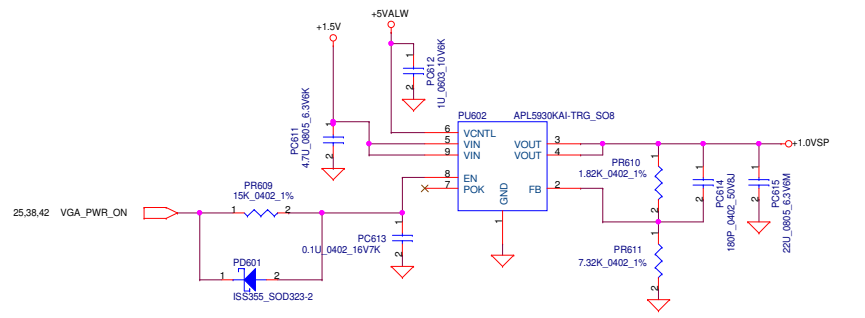
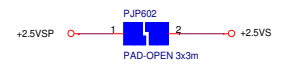
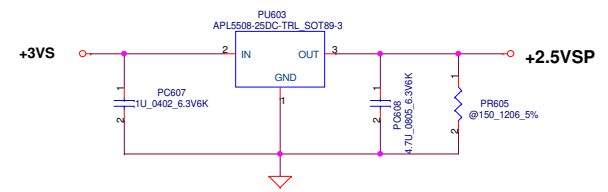
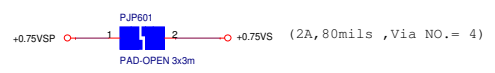
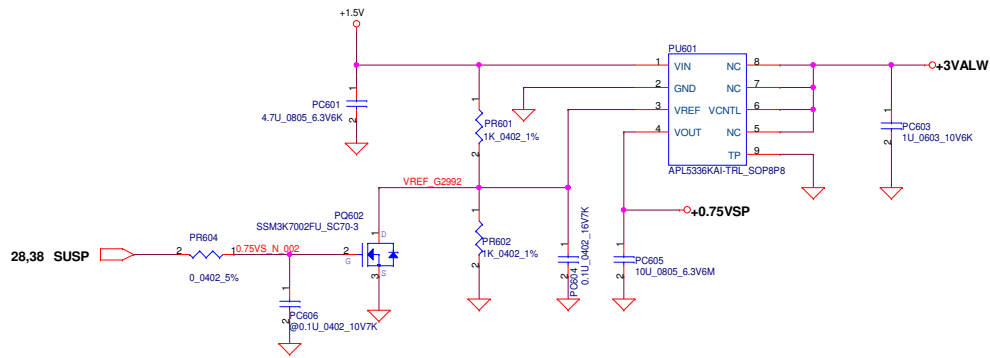
(8A,320mils ,Via NO.= 16)



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				+1.5VP	
Size	Document Number			Rev	
	QBL60 LA-7552P			1.0	
Date:	Monday, April 25, 2011	Sheet	43	of	53

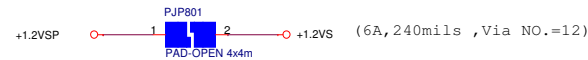
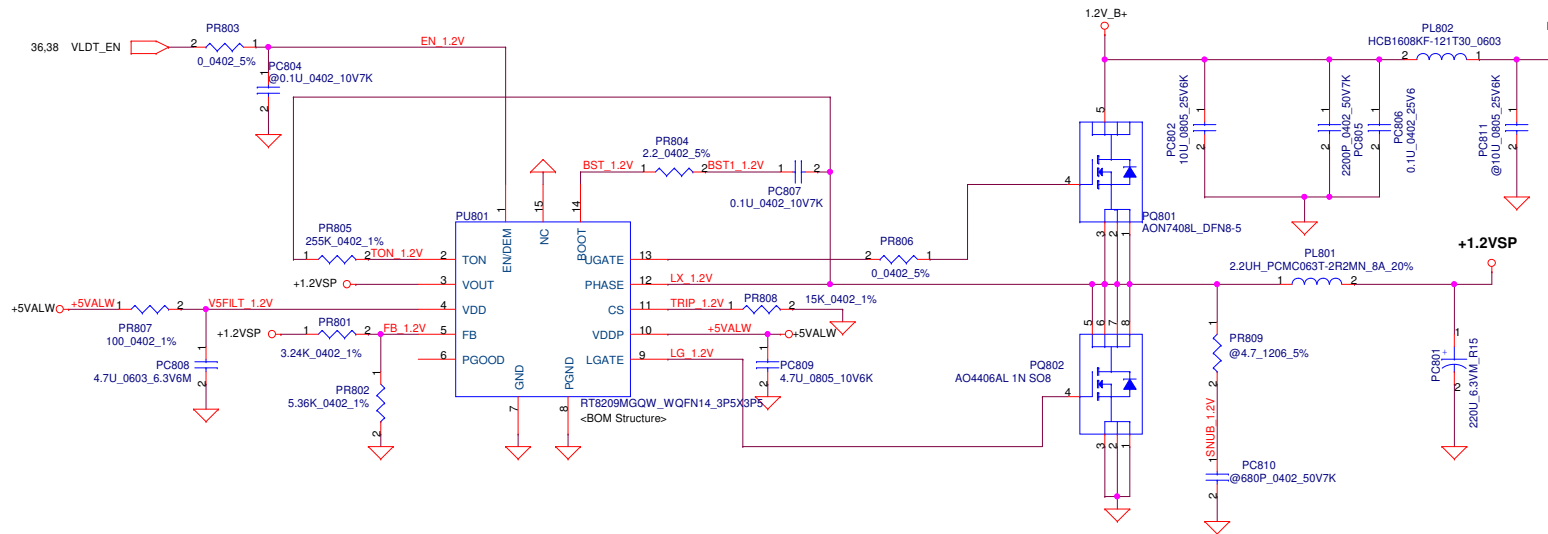


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	PWR+1.1VALWP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Custom	Document Number	QBL60 LA-7552P		Rev
Date:	Monday, April 25, 2011	Sheet	44	of	53



Security Classification	Compal Secret Data		Compal Electronics, Inc. PWR 0.75VSP/1.0VSP/2.5VSP	
Issued Date	2011/04/25	Deciphered Date		
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				
Size	Document Number	Date		Rev
	QBL60 LA-7552P	Monday, April 25, 2011		1.0
		Sheet	45 of 53	

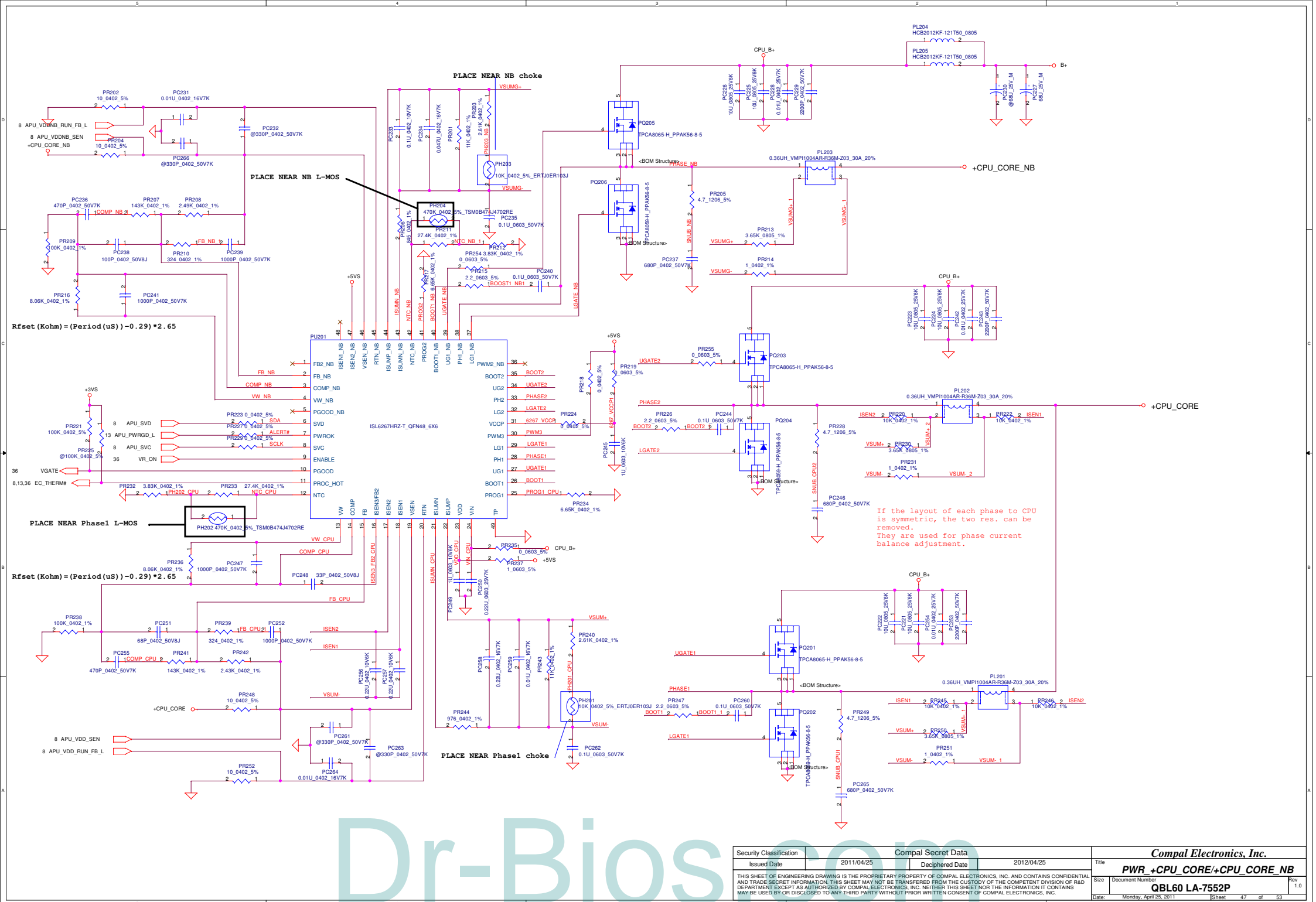
Dr-Bios.com



Dr-Bios.com

Security Classification	Compal Secret Data		
Issued Date	2011/04/25	Deciphered Date	2012/04/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.			
+1.2VSP			
Title	Document Number	Rev	
	NCL61 LA-6321P M/B	1.0	
Date: Monday, April 25, 2011	Sheet	46	of 53



$$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$$

$$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$$

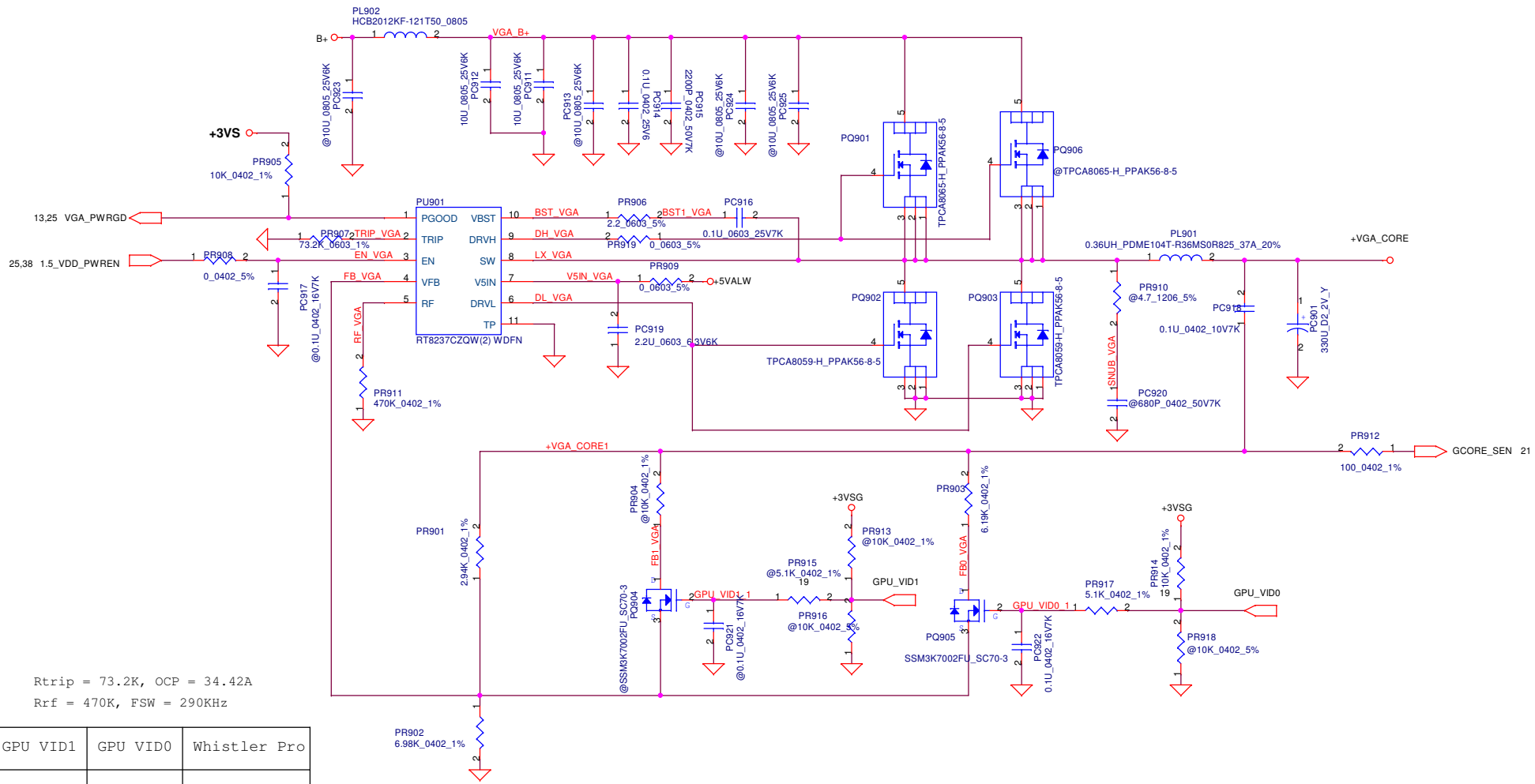
If the layout of each phase to CPU is symmetric, the two res. can be removed. They are used for phase current balance adjustment.

Dr-Bios.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
				PWR_+CPU_CORE/+CPU_CORE_NB	
				Size	Document Number
				QBL60 LA-7552P	
				Date	Monday, April 25, 2011
				Sheet	47 of 53

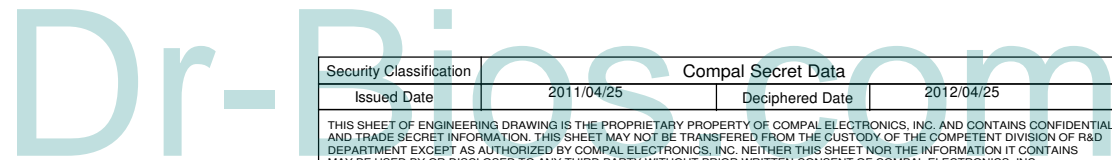
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Rev 1.0



Rtrip = 73.2K, OCP = 34.42A
 Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

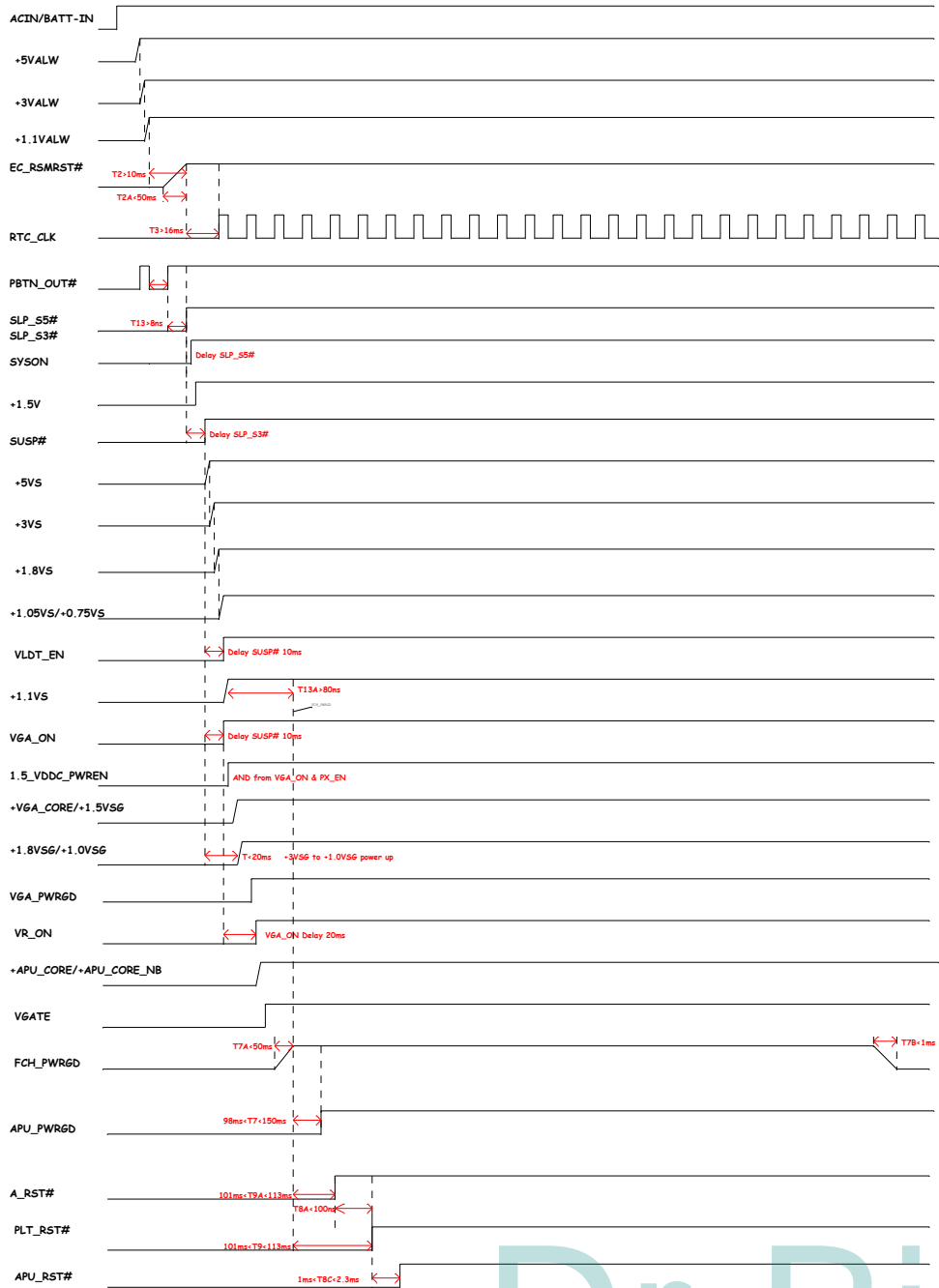


Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				0BL60 LA-7552P
				1 of 1
				0216 Monday, 4/20/2014 10:00:49 AM

Dr. Bios.com

POWER SEQUENCE



Signal	Value	Unit
APU_RST#	1ms	TBC ± 2.3ms
PLT_RST#	101ms	T9 ± 113ms
A_RST#	101ms	T8 ± 113ms
APU_PWRGD	98ns	T7 ± 150ms
FCH_PWRGD	177ns	T7 ± 50ms
VR_ON	20ms	V6A_ON Delay
V6A_ON	10ms	Delay SUSP#
+1.1VS	80ms	T13 ± 80ms
VLDT_EN	10ms	Delay SUSP#
+1.05VS/-0.75VS		
+1.8VS		
+3VS		
+5VS		
SUSP#		
+1.5V		
SYSON		
SLP_S3#		
SLP_S5#		
PBTN_OUT#		
RTC_CLK		
EC_RSTMRST#		
+1.1VALW		
+3VALW		
+5VALW		
ACIN/BATT-IN		

Dr-Bios.com

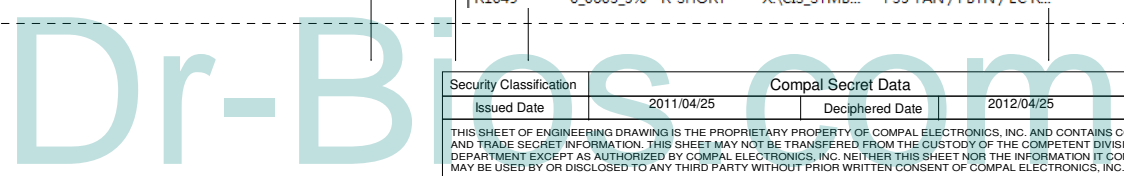
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD request	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	HW-PIR1
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Document Number QBL60 LA-7552P
Date: Monday, April 25, 2011				Rev 1.0
Sheet 51 of 53				

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI request	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uF	03/29	ER
2		For share ROM request	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI request	0.2	PG#34	D5 change to SC300001Y00	03/29	ER
4		For +3VS leakage from CRT	0.21	PG#27	Add Q101,R1644,R1645 Del R4,R31	03/31	ER
5		For Crystal EA	0.21	PG#13	Y4 change to SJ100007N00 (32.768KHZ 7PF)	03/31	ER
6		For HDMI EA	0.21	PG#34	D32.5 change to connect +5VALW from +5VS	03/31	ER
7		For EMC team requirement (ISN).	0.22	PG#29	Change C1636 from 1000pF to 120pF.	04/19	PR
8		For Thermal team recommend.	0.22	PG#19	Add R78, R79 and reserve R80, R82.	04/19	PR
9		Reserve PX_EN signal.	0.22	PG#36	Reserve PX_EN in EC pin 74.	04/19	PR
10		Follow ME BOM.	0.22	PG#11 PG#12	Swap the location of JDIMM1 & JDIMM2.	04/19	PR
11		Don't use for MP.	0.22	PG#35	Unstuff SW4.	04/19	PR
12		Update Board ID for PR (R1.0).	0.22	PG#37	Change R1026 to 46.4K ohm.	04/19	PR
13		DFM team requirement.	0.22	PG#35	Delete SW3.	04/19	PR
14		DMC team requirement.	0.23	PG#29	Reserve D7 between GND_LAN and GND.	04/21	PR
15		Don't use for MP.	0.23	PG#29	Unstuff C1193.	04/21	PR
16		Key Part list is updated from the customer.	0.23	PG#4	Update U25 (M3-FCH) P/N to SA000043ID0 (S IC 218-0755042 A13 02G050005815 T88!)	04/21	PR
17		Key Part list is updated from the customer.	0.23	PG#13	Update U25 (M2-FCH) P/N to SA000042C80 (S IC 218-0755046 A13 02G050005814 T88!)	04/21	PR
18		Update TS1 as ER build Memo.	0.23	PG#29	Change TS1 from SP050005L00 to SP050006F00. (S X'FORM_IH-160 LAN)	04/21	PR
19		For VGA Sequence.	0.23	PG#38	Change R1127 from 470 ohm to 33 ohm.	04/21	PR
20		Prevent the leakage from CRT monitor.	0.23	PG#27	Add R1644, R1645, Q101 and Del R4, R31.	04/21	PR
21		DFB team requirement.	0.23	PG#34	Del R664-R667 and R672-R675.	04/21	PR
22		ESD team requirement.	0.23	PG#34	Change D5 from SC300001D00 (YSCLAMP0524P SLP25I0P8) to SC300001Y00 (AZ1045-04F DFN2510P10E ESD).	04/21	PR
23		DMC team requirement.	0.23	PG#29	Change the ground of D21, D22, D31, D34 and H8. from GND_LAN to LAN.	04/22	PR
24		DMC team requirement.	0.23	PG#19	Add R83, R84.	04/22	PR
25		DMC team requirement.	1.0	PG#13	Change R657 from 22 ohm to 33 ohm.	04/25	PR
26		DMC team requirement.	1.0	PG#13	Stuff R1561 to 33 ohm and C1509 to 22pF.	04/25	PR
27							

Security Classification		Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				QBL60 LA-7552P	1.0
Date: Monday, April 25, 2011				Sheet	52 of 53

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Reduce the component count for MP.	1.0		Change below the footprints from 0 ohm to R short.	04/25	PR
2					Reference Value Source Part Source Library Page		
3					R537 0_0402_5% R-SHORT X\CIS_SYMB... P06-FS1 PCIE/UMI/TSI		
4					R538 0_0402_5% R-SHORT X\CIS_SYMB... P06-FS1 PCIE/UMI/TSI		
5					R591 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
6					R598 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
7					R606 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
8					R608 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
9					R611 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
10					R81 0_0402_5% R-SHORT X\CIS_SYMB... P14-HUDSON-M2 GPL...		
11					R912 0_0402_5% R-SHORT X\CIS_SYMB... P16-HUDSON-M2 STR...		
12					R1145 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
13					R1148 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
14					R19 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
15					R20 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
16					R22 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
17					R23 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
18					R24 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
19					R25 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
20					R26 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
21					R27 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
22					R28 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
23					R937 0_0805_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
24					R938 0_0805_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
25					R941 0_0805_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
26					R945 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
27					R483 0_0402_5% R-SHORT X\CIS_SYMB... P23-VRAM_DDR3 / CH...		
					R485 0_0402_5% R-SHORT X\CIS_SYMB... P23-VRAM_DDR3 / CH...		
					R511 0_0402_5% R-SHORT X\CIS_SYMB... P24-VRAM_DDR3 / CH...		
					R513 0_0402_5% R-SHORT X\CIS_SYMB... P24-VRAM_DDR3 / CH...		
					R1291 0_0402_5% R-SHORT X\CIS_SYMB... P26-LVDS Translator-A...		
					R570 0_0805_5% R-SHORT X\CIS_SYMB... P26-LVDS Translator-A...		
					R607 0_0805_5% R-SHORT X\CIS_SYMB... P26-LVDS Translator-A...		
					R1634 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1635 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1636 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1641 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1643 0_0603_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1650 0_0603_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1651 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R560 0_0603_5% R-SHORT X\CIS_SYMB... P29-LAN Realtek RTL81...		
					R647 0_0402_5% R-SHORT X\CIS_SYMB... P29-LAN Realtek RTL81...		
					R658 0_0603_5% R-SHORT X\CIS_SYMB... P29-LAN Realtek RTL81...		
					R1531 0_0805_5% R-SHORT X\CIS_SYMB... P30-HD AUDIO CODEC...		
					R1534 0_0603_5% R-SHORT X\CIS_SYMB... P30-HD AUDIO CODEC...		
					R1537 0_0603_5% R-SHORT X\CIS_SYMB... P30-HD AUDIO CODEC...		
					R1560 0_0603_5% R-SHORT X\CIS_SYMB... P31-RTS5137 Media C...		
					R1573 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1574 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1575 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1576 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1577 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1578 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1579 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1580 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1595 0_0805_5% R-SHORT X\CIS_SYMB... P33-HDD & ODD CONN		
					R1598 0_0805_5% R-SHORT X\CIS_SYMB... P33-HDD & ODD CONN		
					R1049 0_0603_5% R-SHORT X\CIS_SYMB... P35-FAN / PBTN / EC R...		



Security Classification	Compal Secret Data	Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number	Rev
		QBL60 LA-7552P	1.0
		Date: Monday, April 25, 2011	Sheet 53 of 53

Compal Electronics, Inc.

HW-PIR3

QBL60 LA-7552P