

Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-16

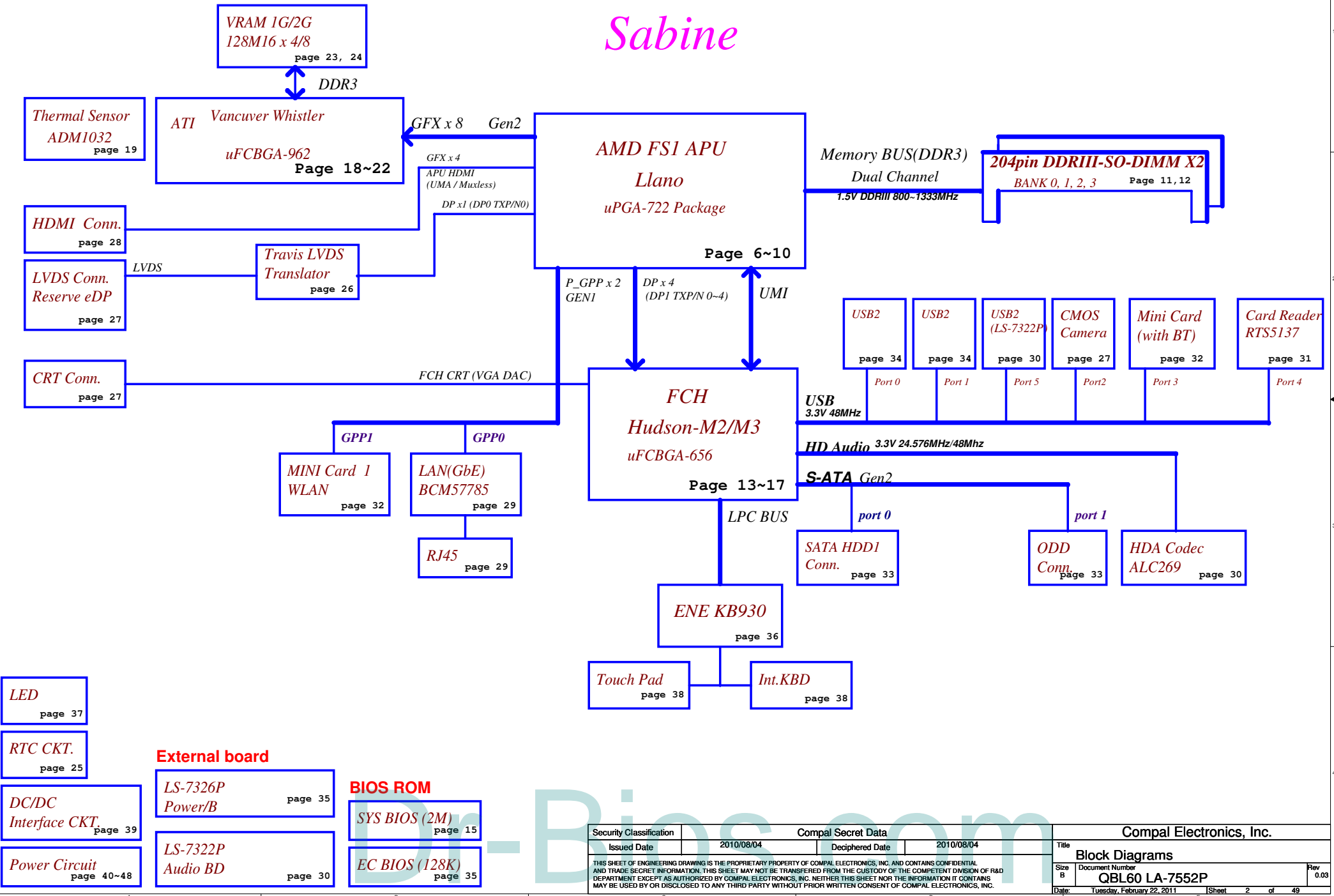
LA-7552P REV: 0.03

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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title		
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					QBL60 LA-7552P	0.03
				Date:	Tuesday, February 22, 2011	Sheet 1 of 49

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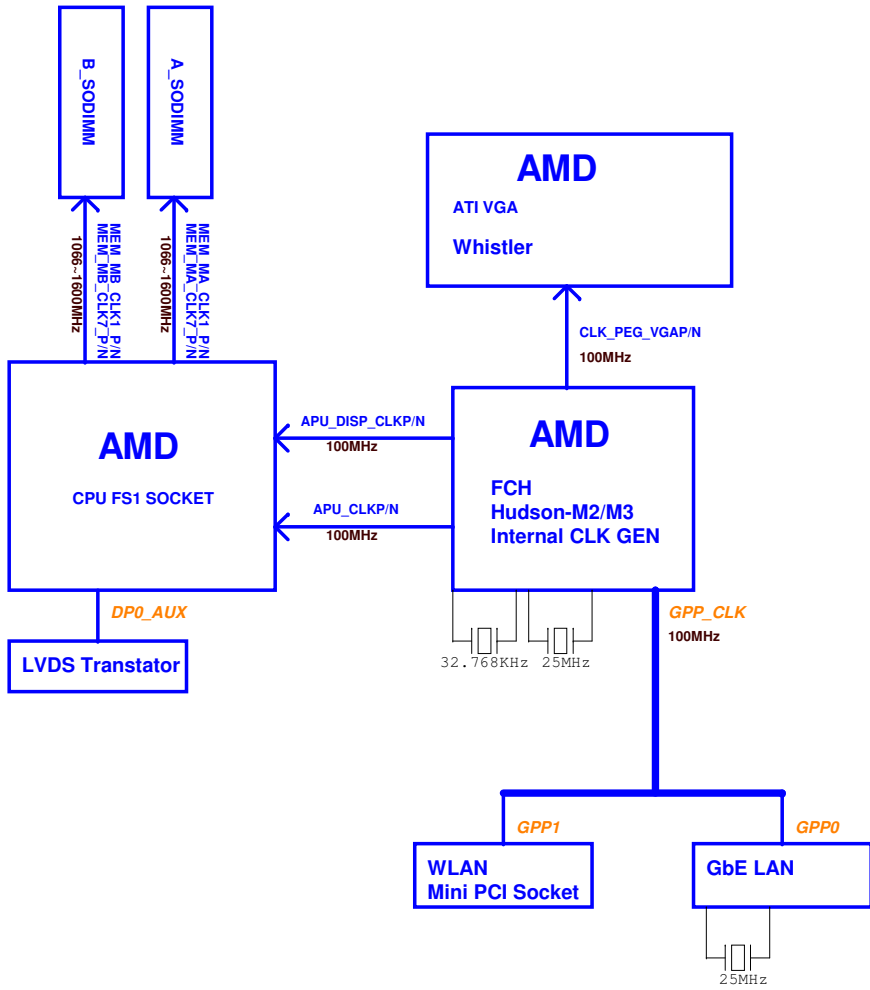
Model Name : QBL60

Sabine

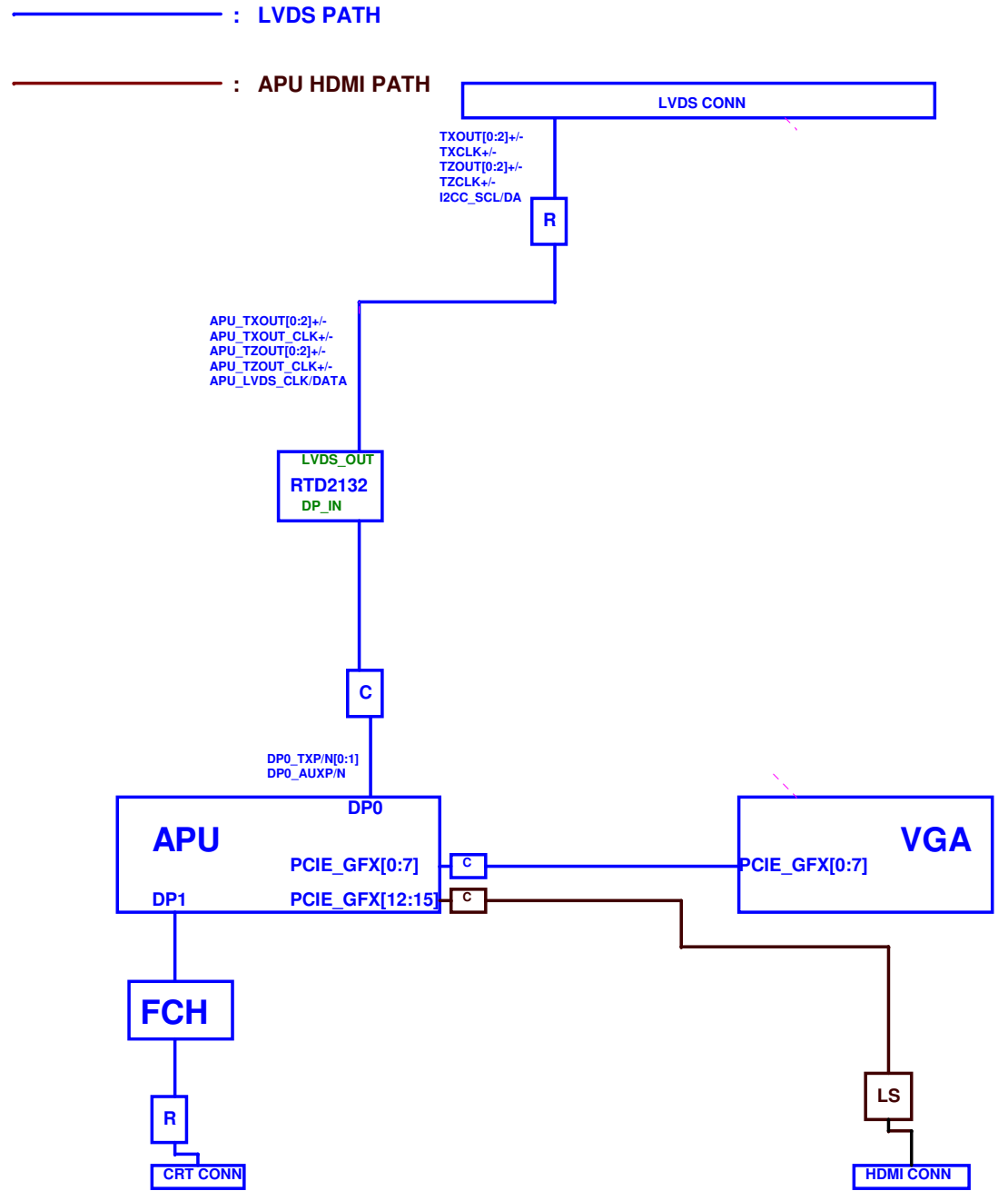


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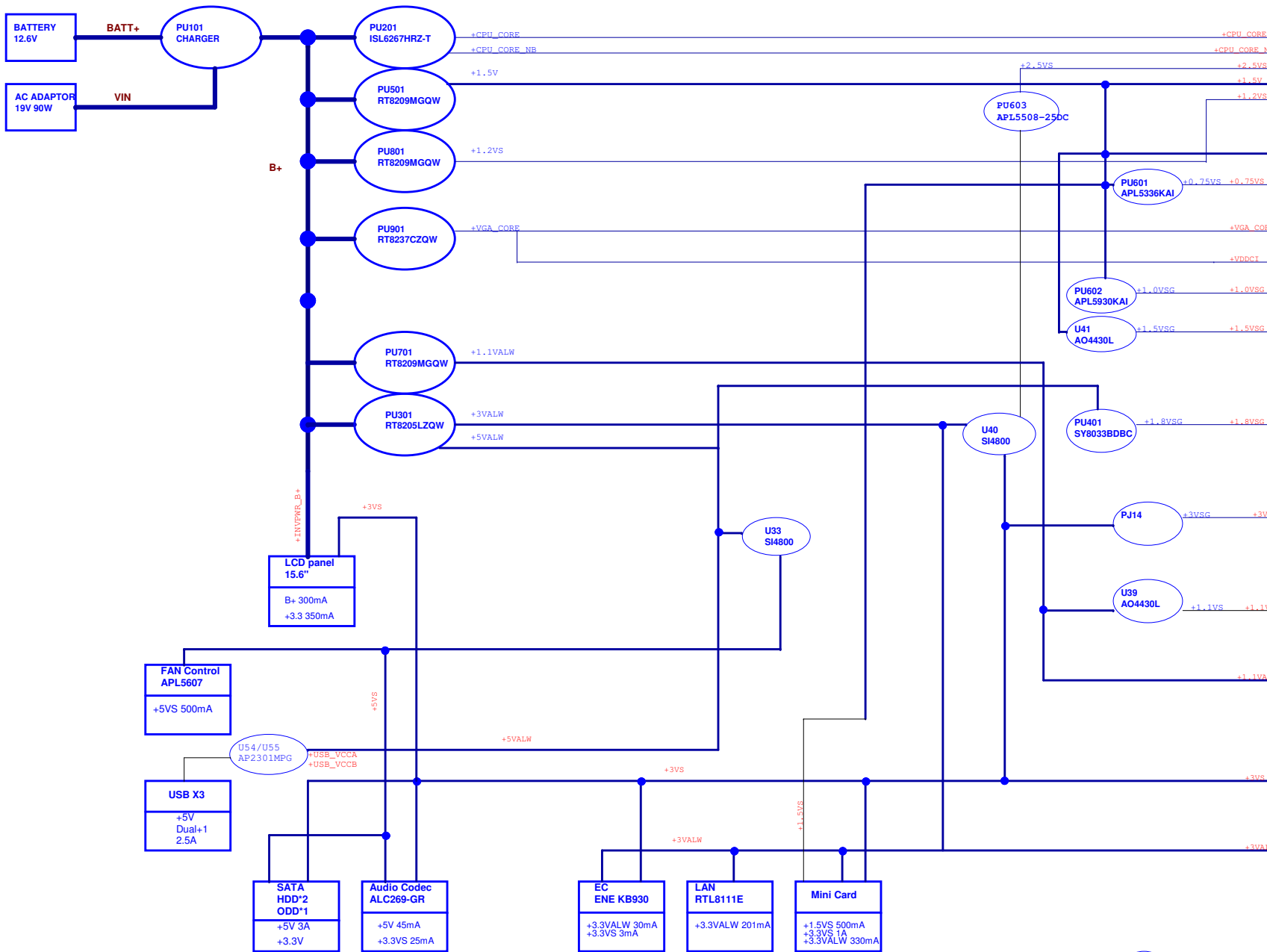
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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AMD APU FS1	
0.7~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A

RAM DDRIII SODIMMx2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCI_VDDC: 2000 mA DP[A]E_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1D1: 100 mA VDD2D1: 50 mA AZVDDC: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCI_VDDC: 40 mA MPV18: 150 mA SPV18: 75 mA PCI_VDDR: 400 mA DP[A]F_VDD18: 920 mA DP[A]F_PVDD: 120 mA
+3VSG	AZVDD: 130 mA VDDR3: 60 mA

VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIE: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G



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18 PCIE_GTX_C_FRX_P[0..7]

18 PCIE_GTX_C_FRX_N[0..7]

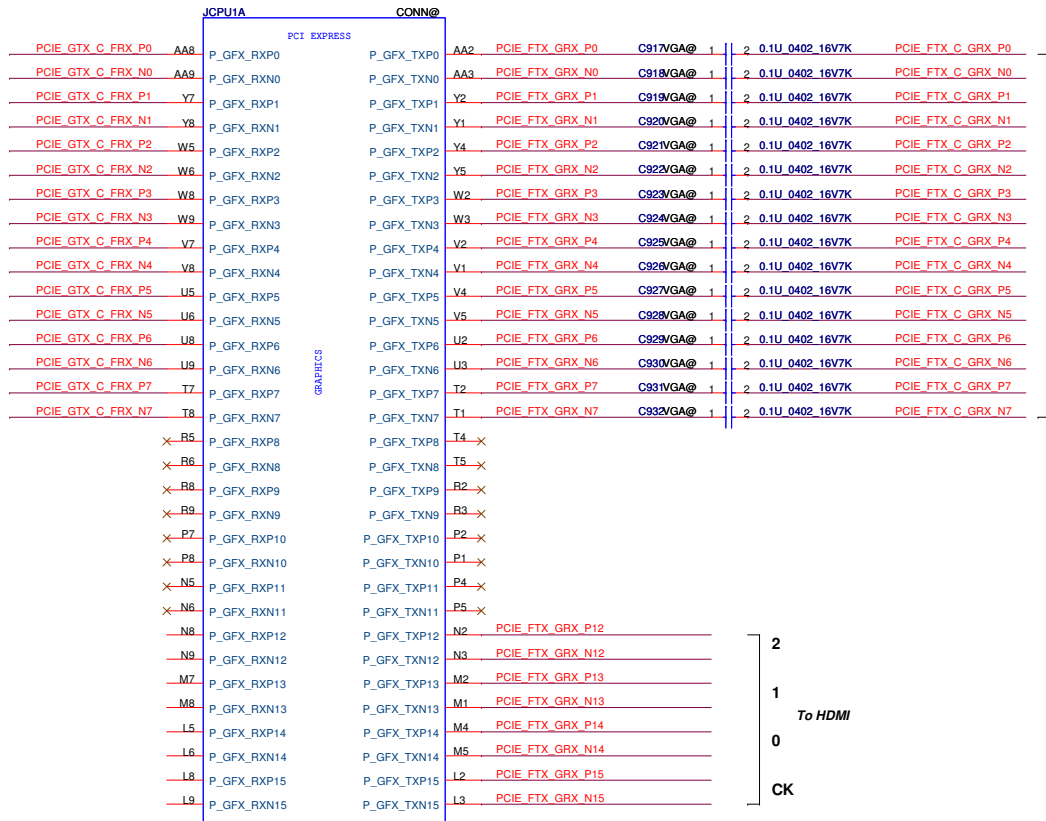
PCIE_FTX_C_GRX_P[0..7] 18

PCIE_FTX_C_GRX_N[0..7] 18

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28

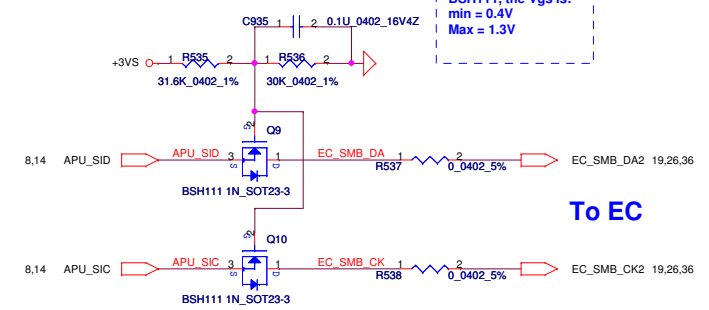
PCIE_FTX_GRX_N[12..15] 28



For UMA Mux.

To HDMI
CK

CPU TSI interface level shift

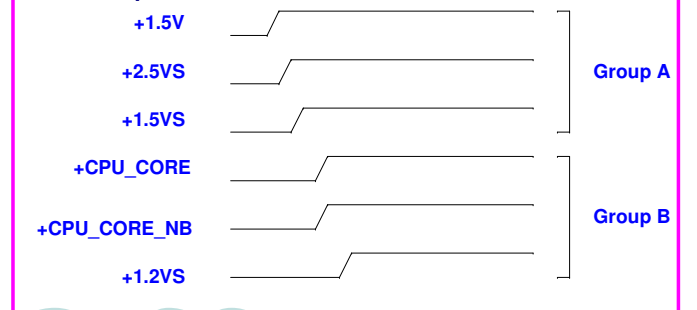


To EC

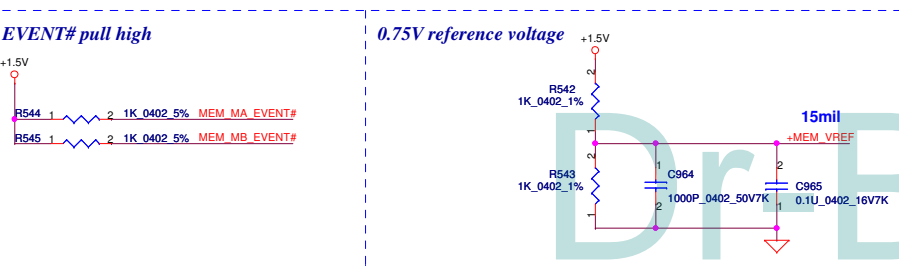
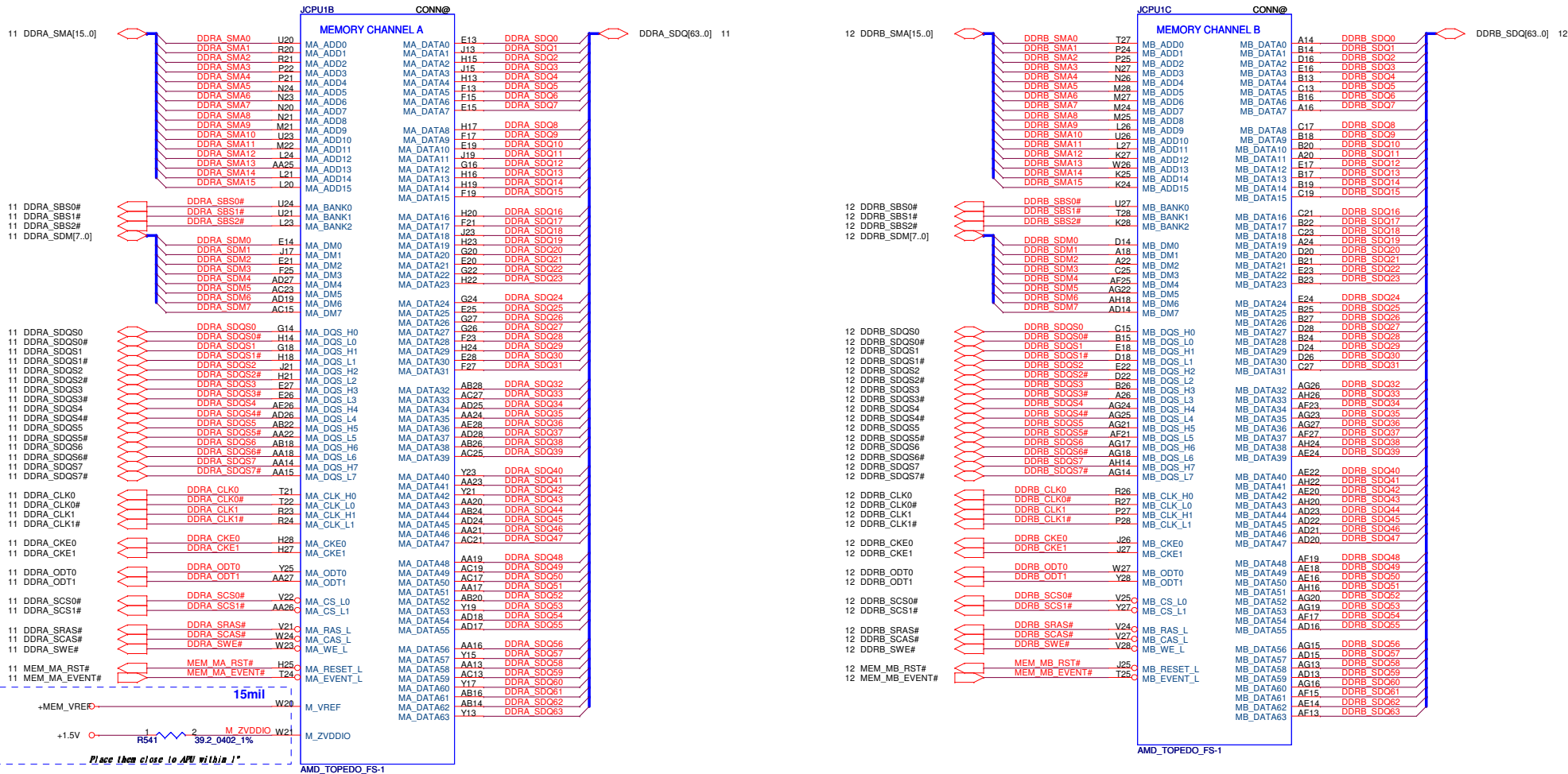


GLAN
WLAN

Power Sequence of APU



Security Classification	Compal Secret Data		Title	
Issued Date	2010/08/04	Deciphered Date	2010/08/04	AMD FS1 PCIE / UMI / TSI
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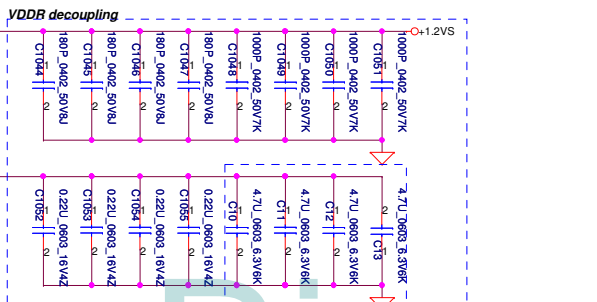
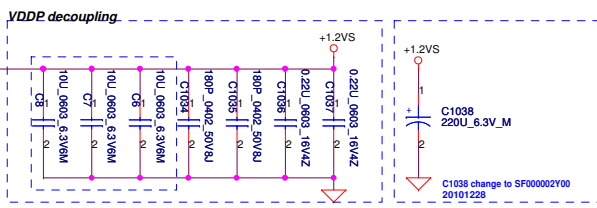
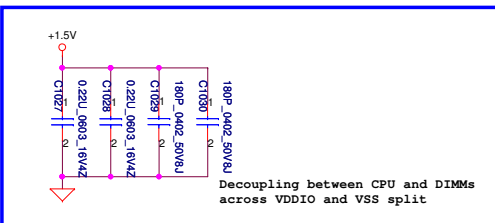
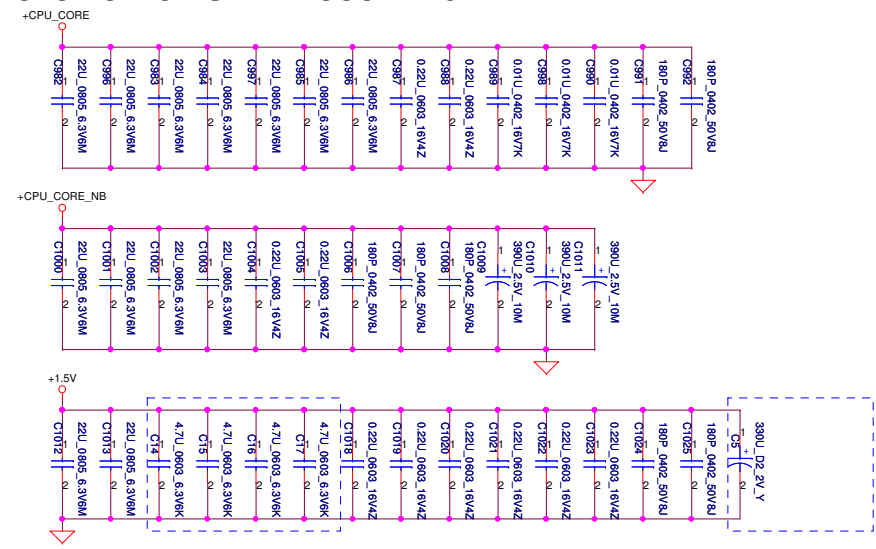
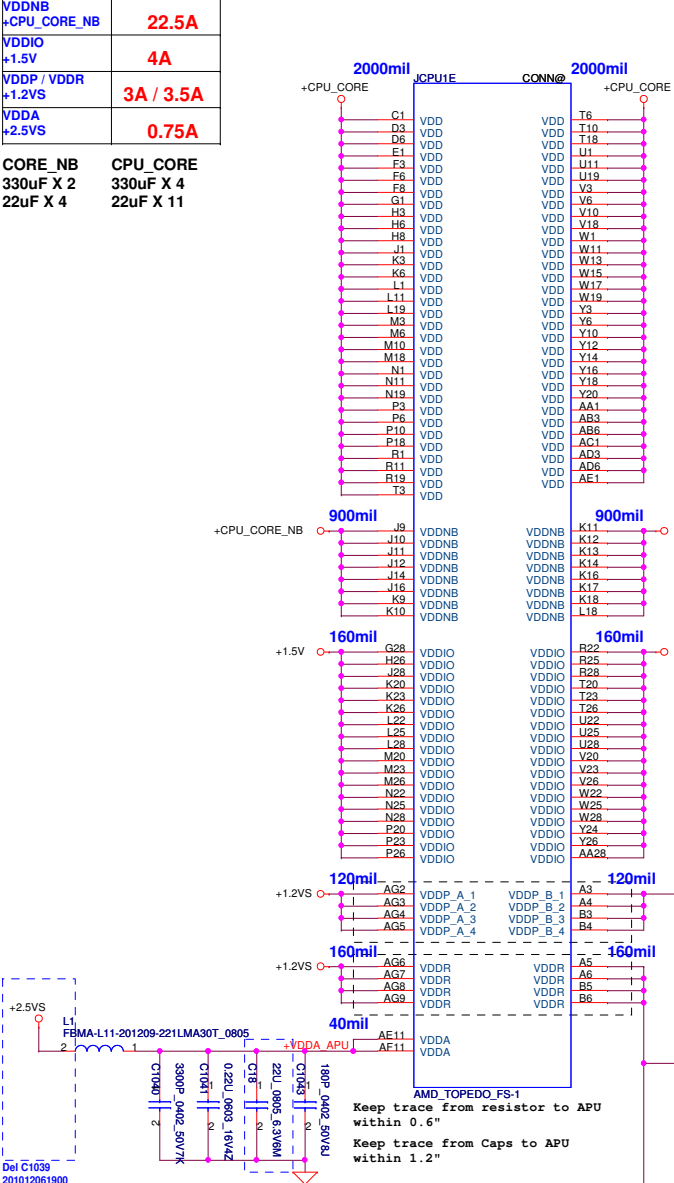


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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB CPU_CORE
330uF X 2 330uF X 4
22uF X 4 22uF X 11

CPU BOTTOM SIDE DECOUPLING



JCPU1F	CONN@
A7	T11
A13	T19
A15	T4
A17	L7
A19	L10
A21	L18
A23	V9
A25	V11
B7	V19
C4	W4
C10	W7
C14	W10
C16	W12
C18	W14
C20	W16
C22	W18
C24	Y9
C26	Y2
C28	AA4
C28	AA7
D13	AB9
D17	AB13
D19	AB15
D21	AB17
D23	AB19
D25	AB21
D27	AB23
E4	AB25
E10	AB27
E12	AC4
F3	AC7
F11	AC10
F14	AC12
F16	AC14
F18	AC16
F20	AC18
F22	AC20
F24	AC22
F26	AC24
F28	AC26
G4	AC28
G8	AD9
G12	AD11
G15	AD13
G17	AE7
G19	AE13
G21	AE15
G23	AE17
G25	AE19
J4	AE21
J8	AE23
J12	AE25
J20	AE27
J22	AF3
J24	AF6
K18	AF9
L4	AF12
L7	AF14
L10	AF16
M9	AF18
M11	AF20
M19	AF22
N4	AF24
N7	AF26
N10	AF28
N18	AG10
P9	AH5
P11	AH8
P19	AH13
R4	AH15
R7	AH17
R10	AH19
R18	AH21
T9	AH23
	AH25

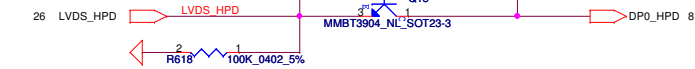
Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3				180pF x 4
10nF x 3		4.7uF x 4				
		0.22uF x 6				
		180pF x 4				

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HPD

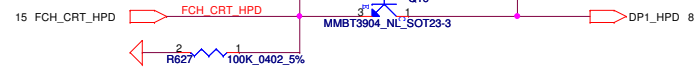
Translator HPD

From Translator



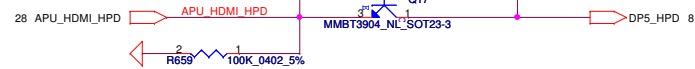
CRT HPD

From FCH

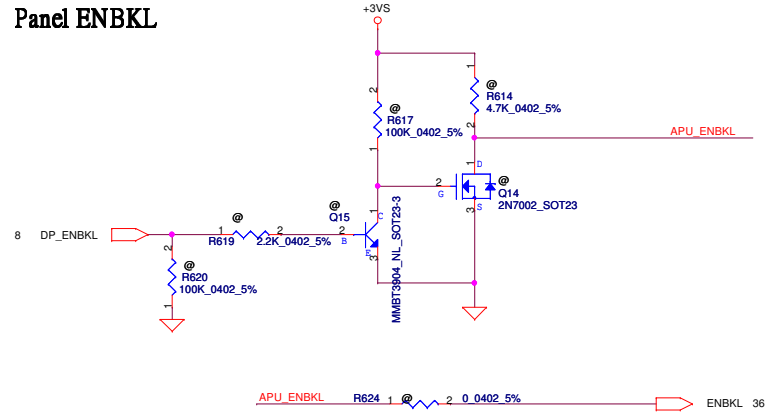


HDMI HPD

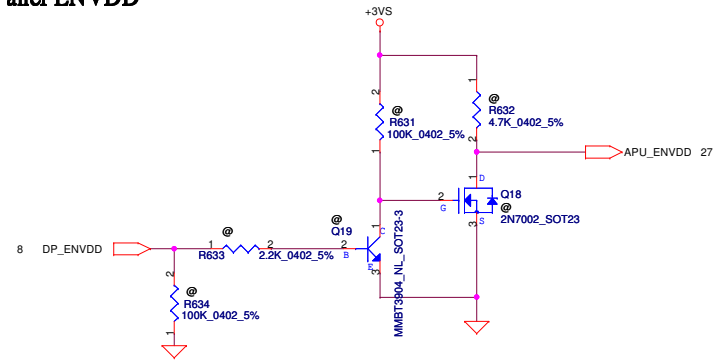
From HDMI Conn



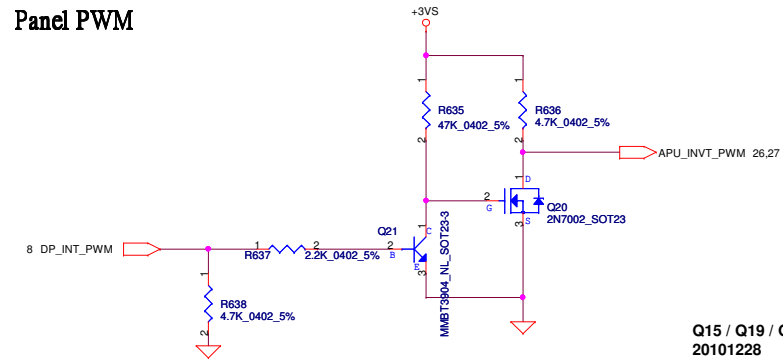
Panel ENBKL



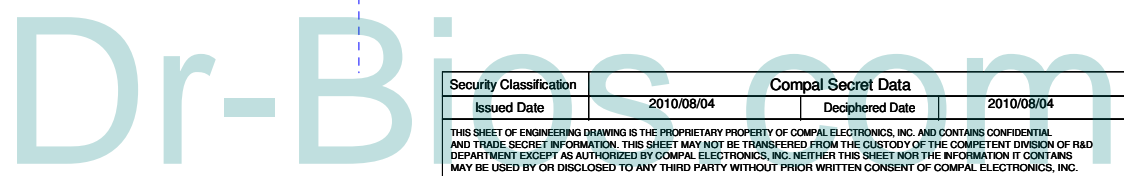
Panel ENVDD



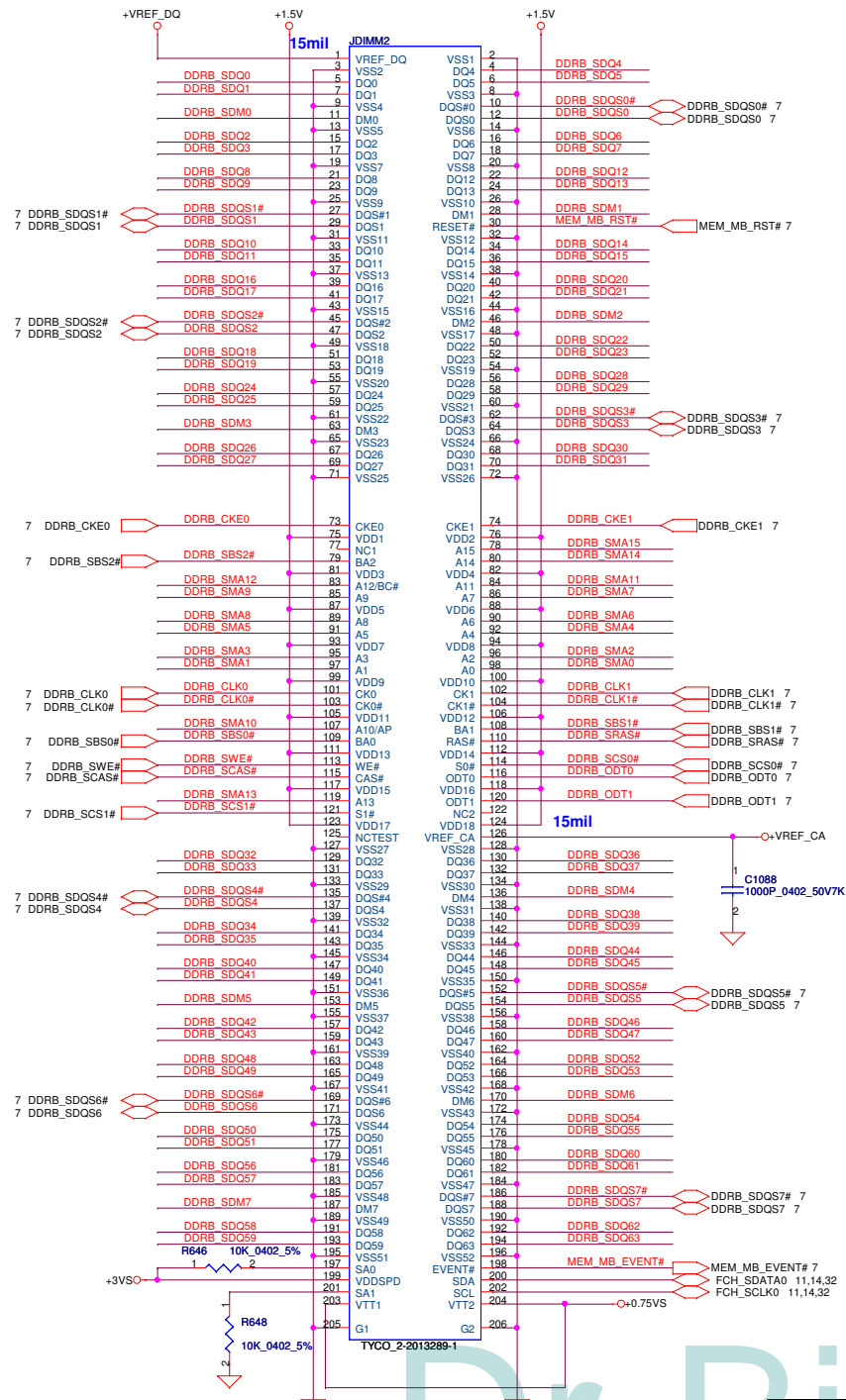
Panel PWM

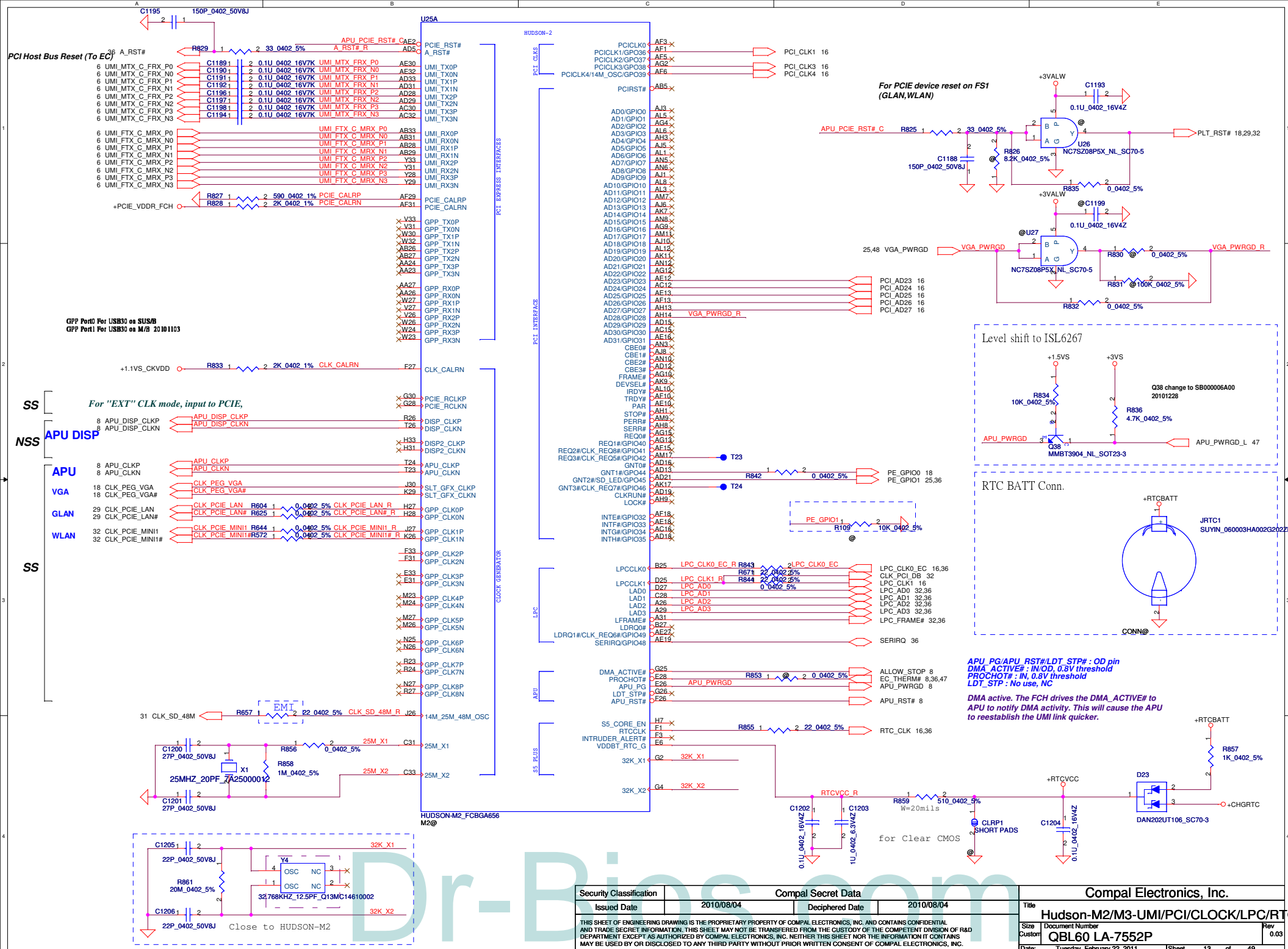


Q15 / Q19 / Q21 change to SB000006A00
20101228



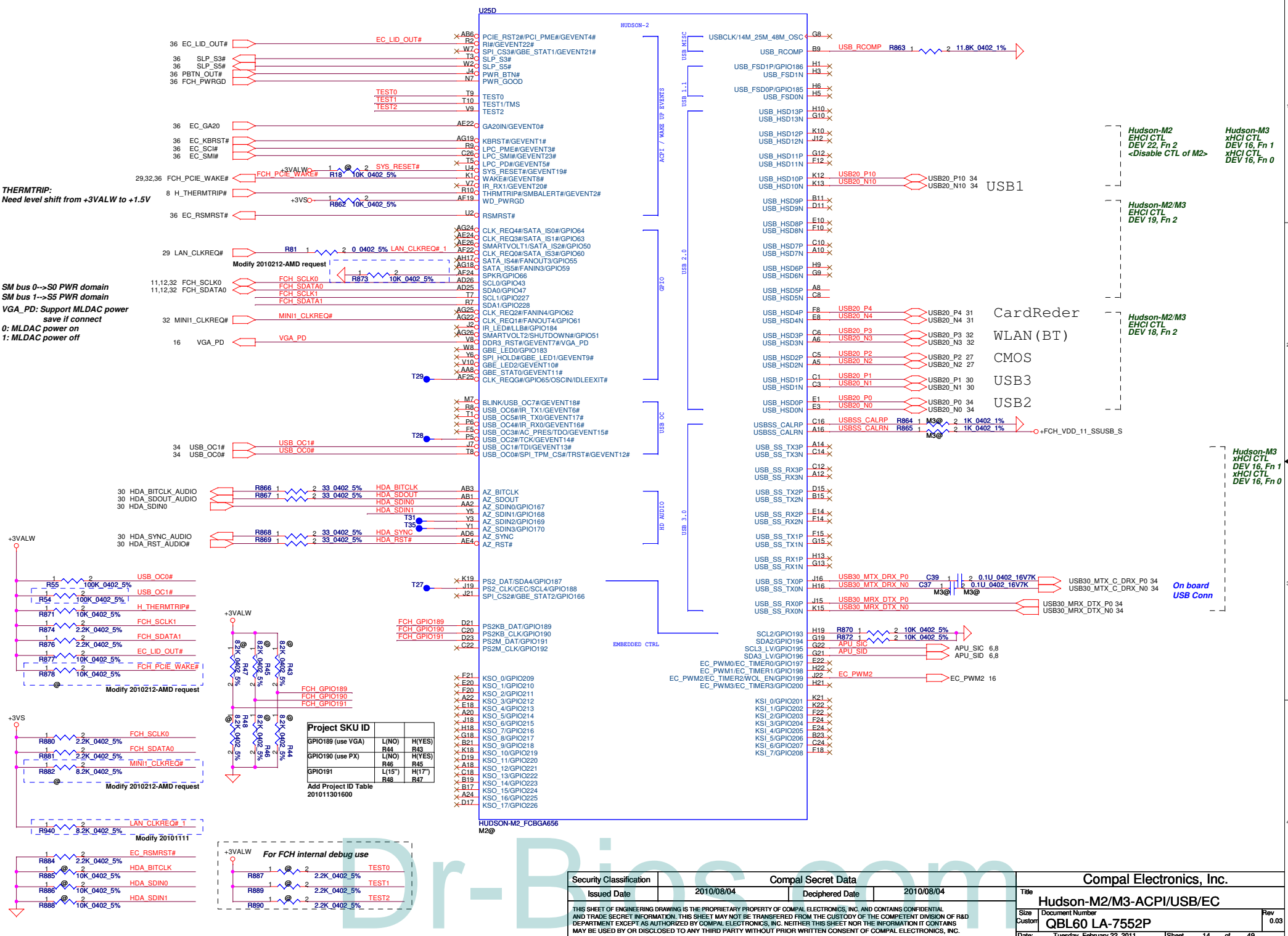
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	AMD FS1 Singal Level Shifter	
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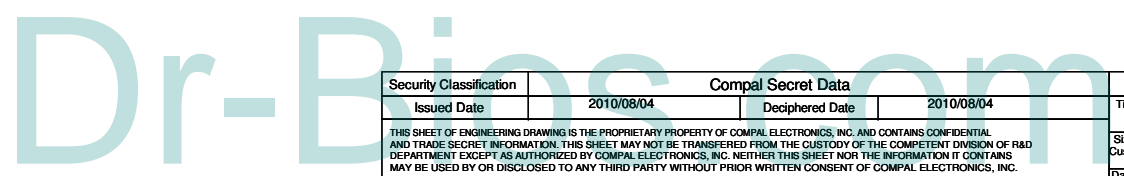
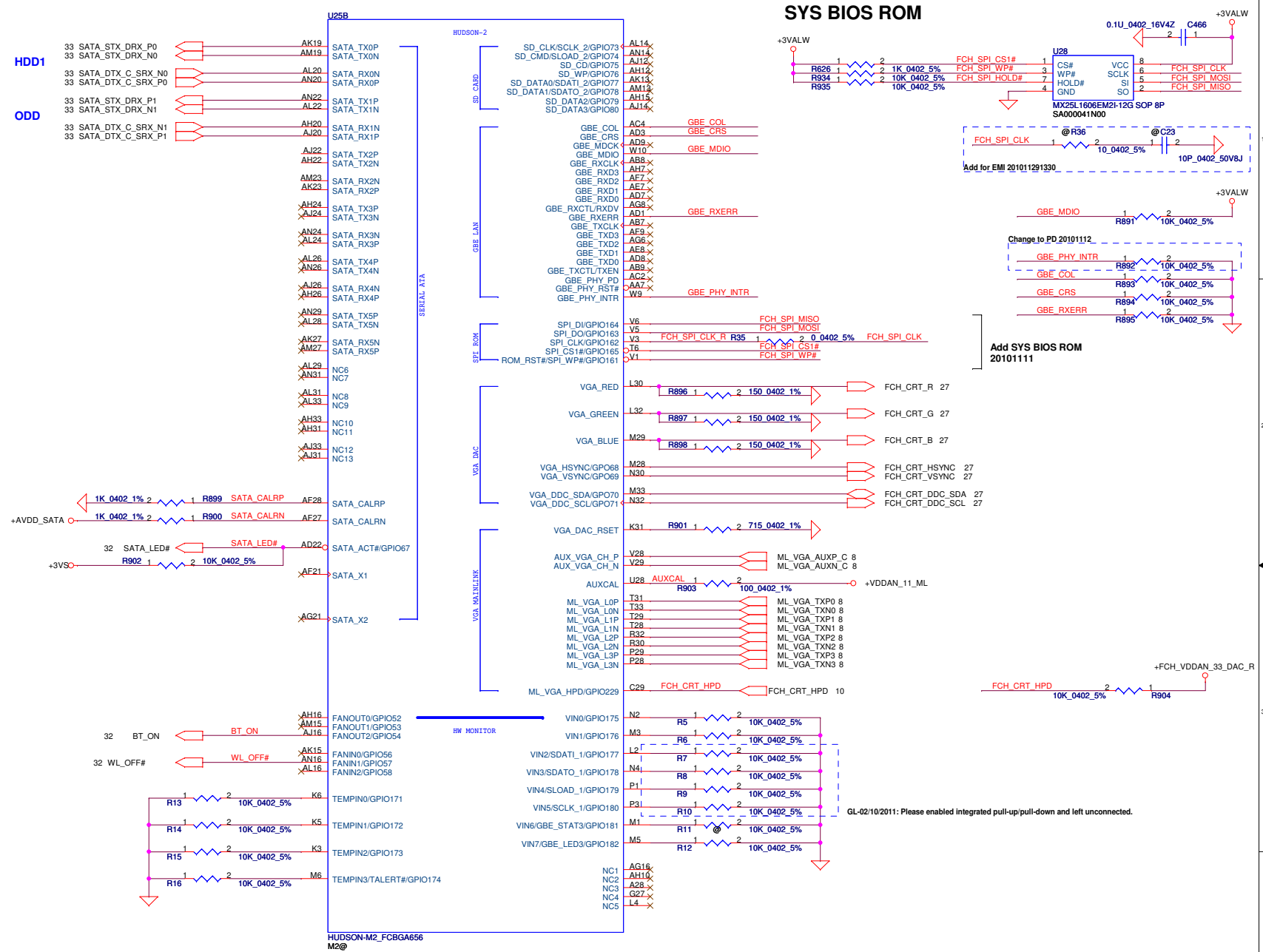


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PCIE_RST2 : Reset PCIe device on Hudson2



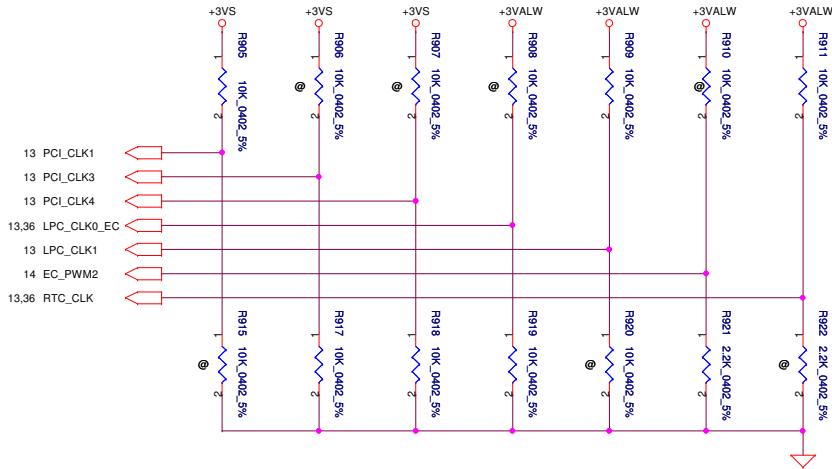
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Hudson-M2/M3-ACPI/USB/EC
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STRAP PINS

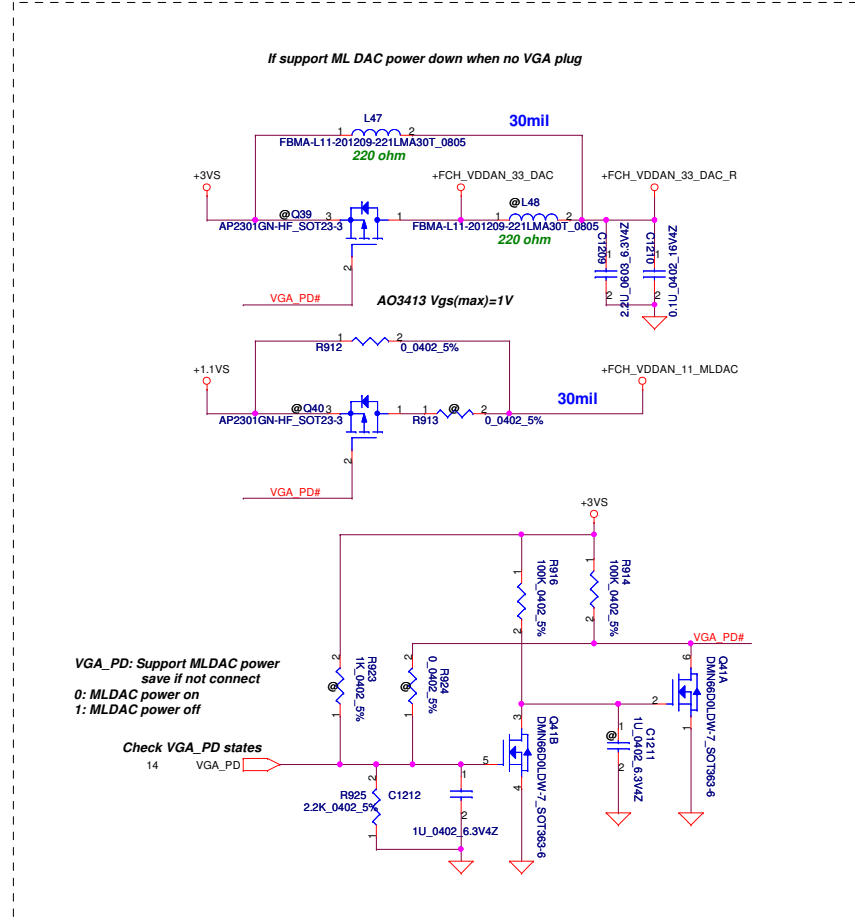
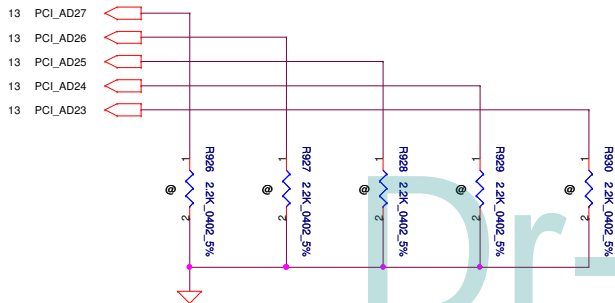
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

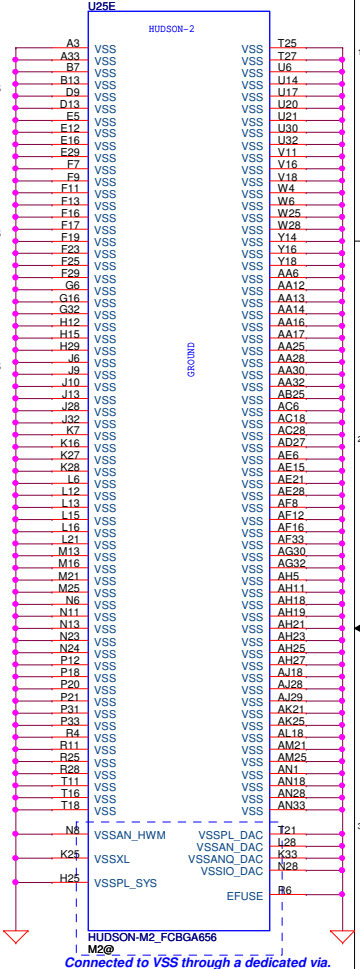
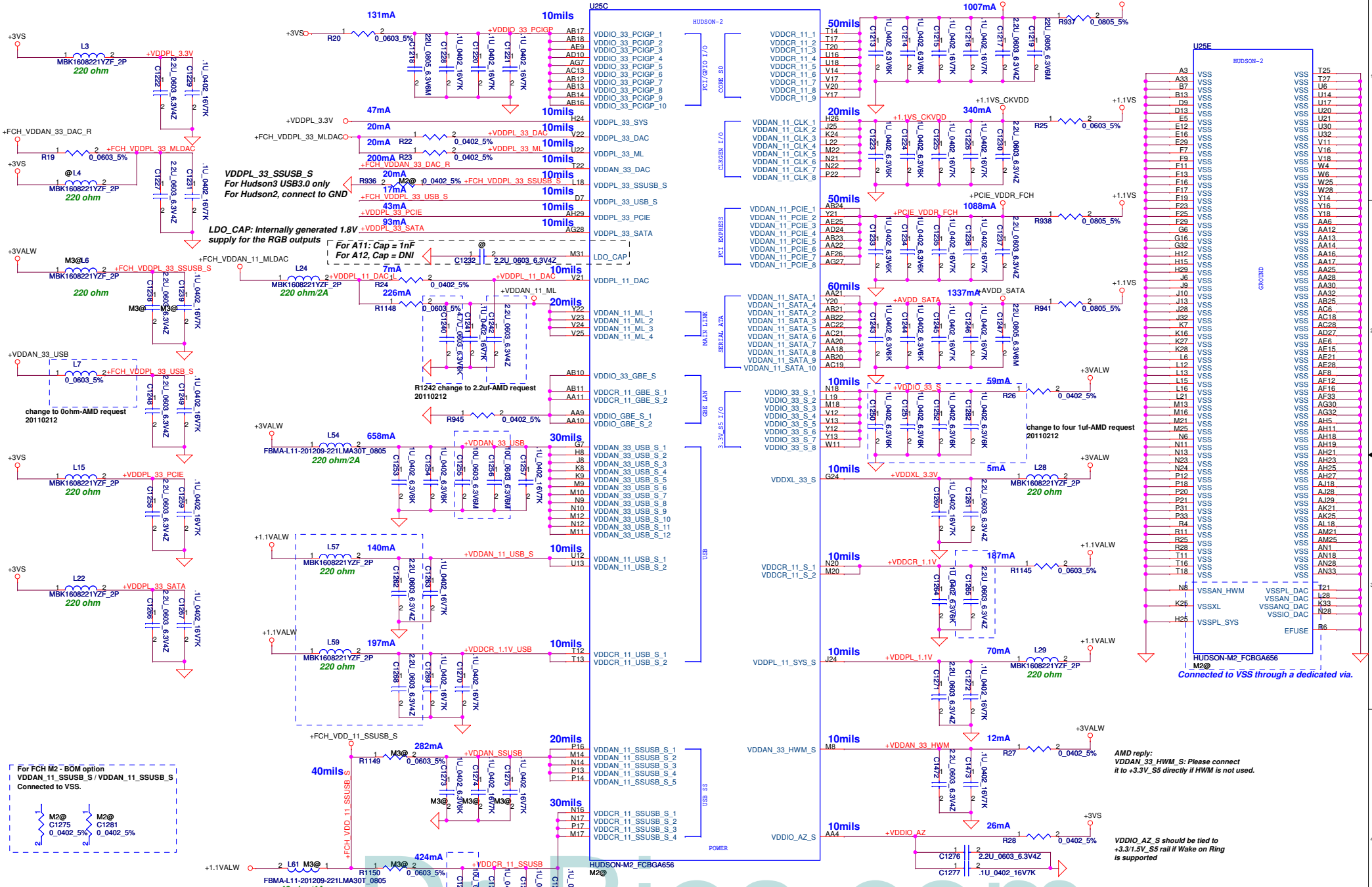
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23	
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



C1218 / C1219 / C1247 Change to SE00000110

20101228



For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S
Connected to VSS.

AMD reply:
VDDAN_HWM_S: Please connect
it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to
+3.3V_S5 rail if Wake on Ring
is supported

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Compal Electronics, Inc.	
Hudson-M2/M3-POWER/GND	
Rev	0.03

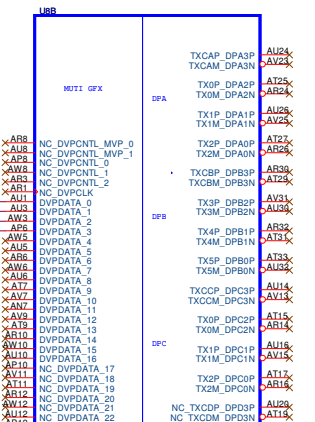
Strap Name	Pin Straps description <all Internal PD>	Setting
VIP_DEVICE_EN (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on V#A0_0 during reset 1: V#A0_0 to determine whether or not a VIP slave device	0
VGA_DIS	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010	001
CONFIG[1]		
CONFIG[0]		
BIOS_ROM_EN	GPIO22 0: Disable, 1: Enable	0
AUD[1]	HSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected;	00
AUD[0]	VSYNC 11: Audio for both DisplayPort and HDMI	
BIF_GEN2_EN	GPIO2 0: Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

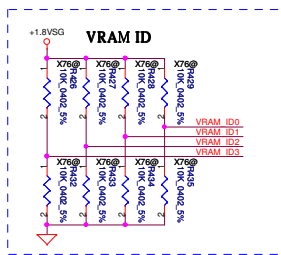
Global Swap Lock on Multiple GPUs



NC on Park, Robson and Seymour

NC on Park, Robson and Seymour

Not share via for other GND



GPIO5 fast-power reduction: HW control will cause display disturb should use SW method control

GPIO6 voltage control signal, No use can NC!

Move to DDCCLK_AUX3P,DDCCDATA_AUX3N, DDCCLK_AUX3P,DDCCDATA_AUX3N

GPIO7 Controls backlight on/off. Active High, need external PD

If GPIO22 High, GPIO 11-13 -> CFG[0:2] Config ROM type, GPU has internal PD

GPIO6,15,16,20 Voltage control signal, GPIO6,15 no use can NC

Thermal monitor interrupt Critical temperature fault

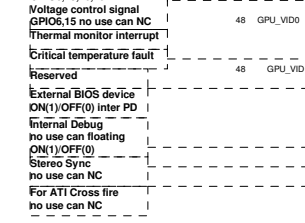
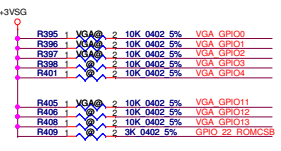
Reserved

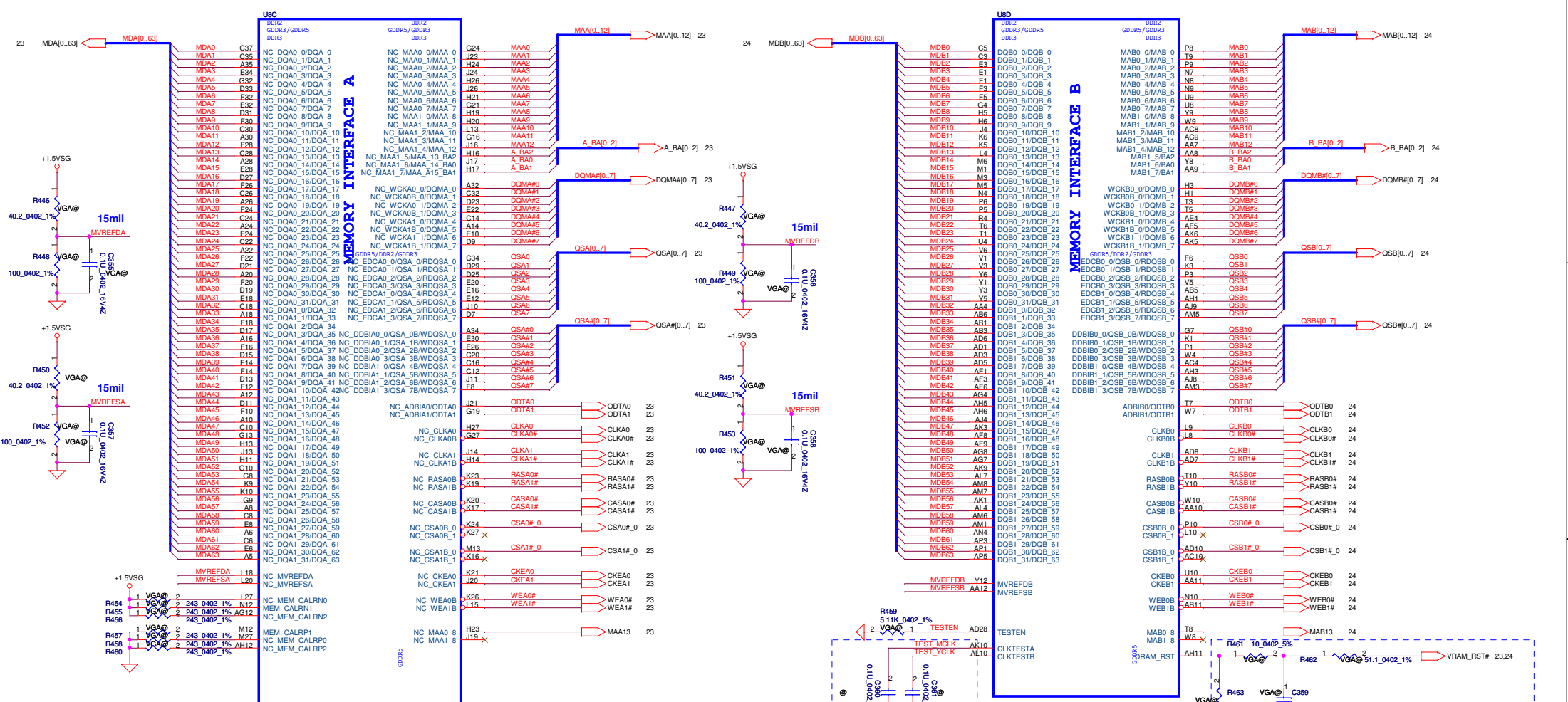
External BIOS device ON(1)/OFF(0) Inter PD

Internal Debug no use can floating ON(1)/OFF(0) no use can NC

Stereo Sync no use can NC

For ATI Cross fire no use can NC

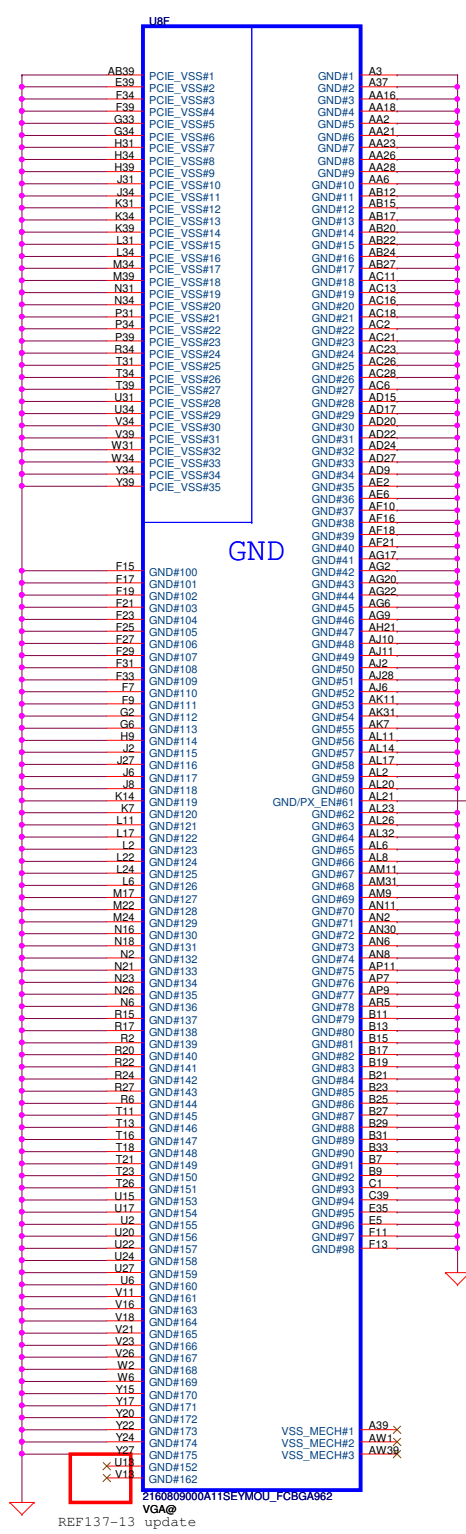




Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

Note:
route 50ohms single-ended and 100ohms diff and keep short
REF137-03 suggest

Park&Seymour is single channel for memory (channel B only)

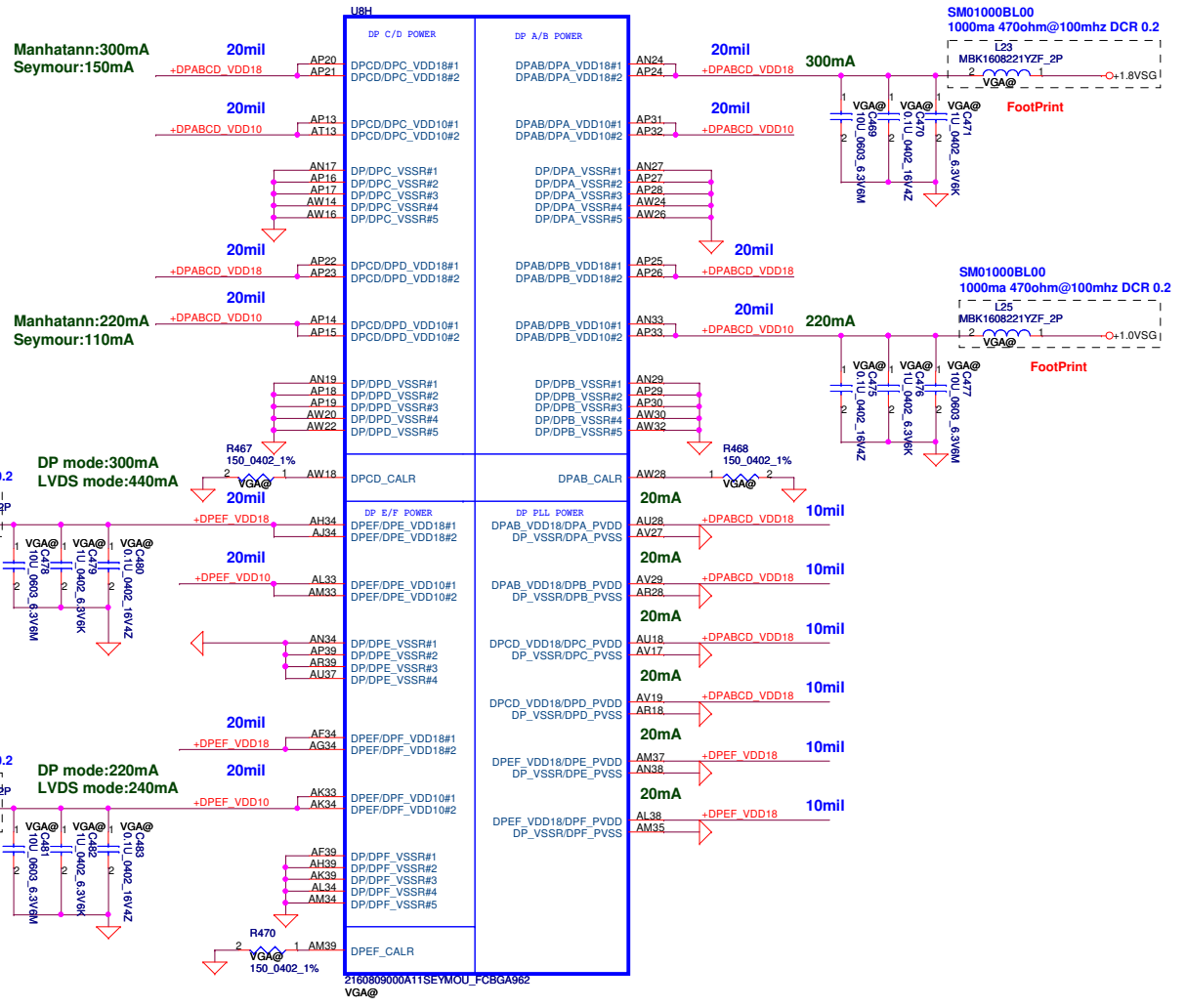


DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD can combian to DPAB_VDD18
 DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD can combian to DPCD_VDD18
 (DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
 DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD can combian to DPEF_VDD18

Seymour/Whistler :
 DPA_VDD10,DPB_VDD10 can combian to DPAB_VDD10
 DPC_VDD10,DPD_VDD10 can combian to DPCD_VDD10
 DPE_VDD10,DPD_VDD10 can combian to DPEF_VDD10

DPx-VSSR,DPx_PVSS can combian to DP_VSSR (Manhattan should have individual GND) where x is A,B,C,D,E,F

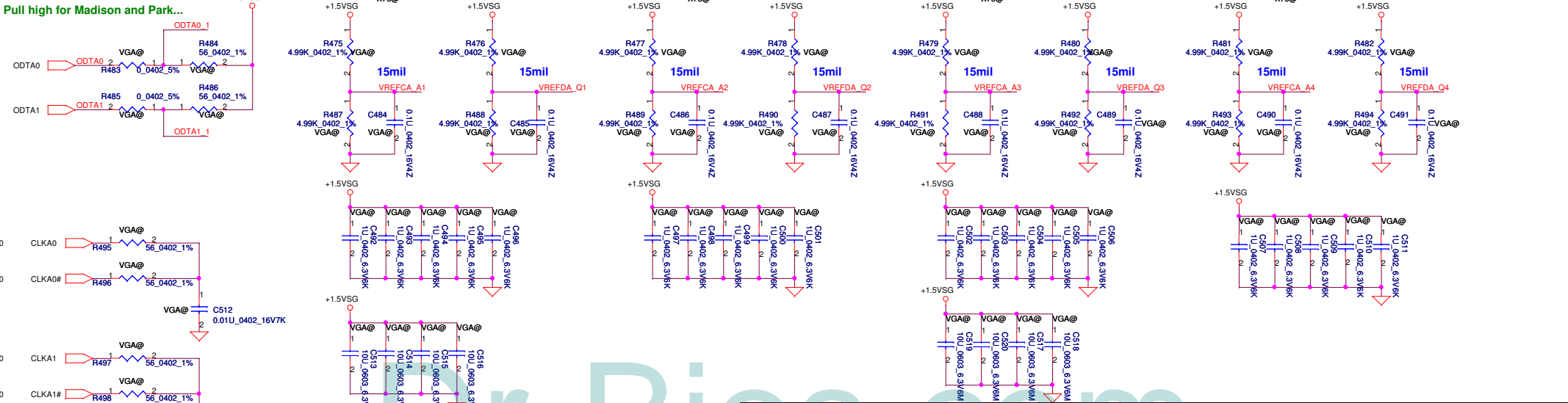
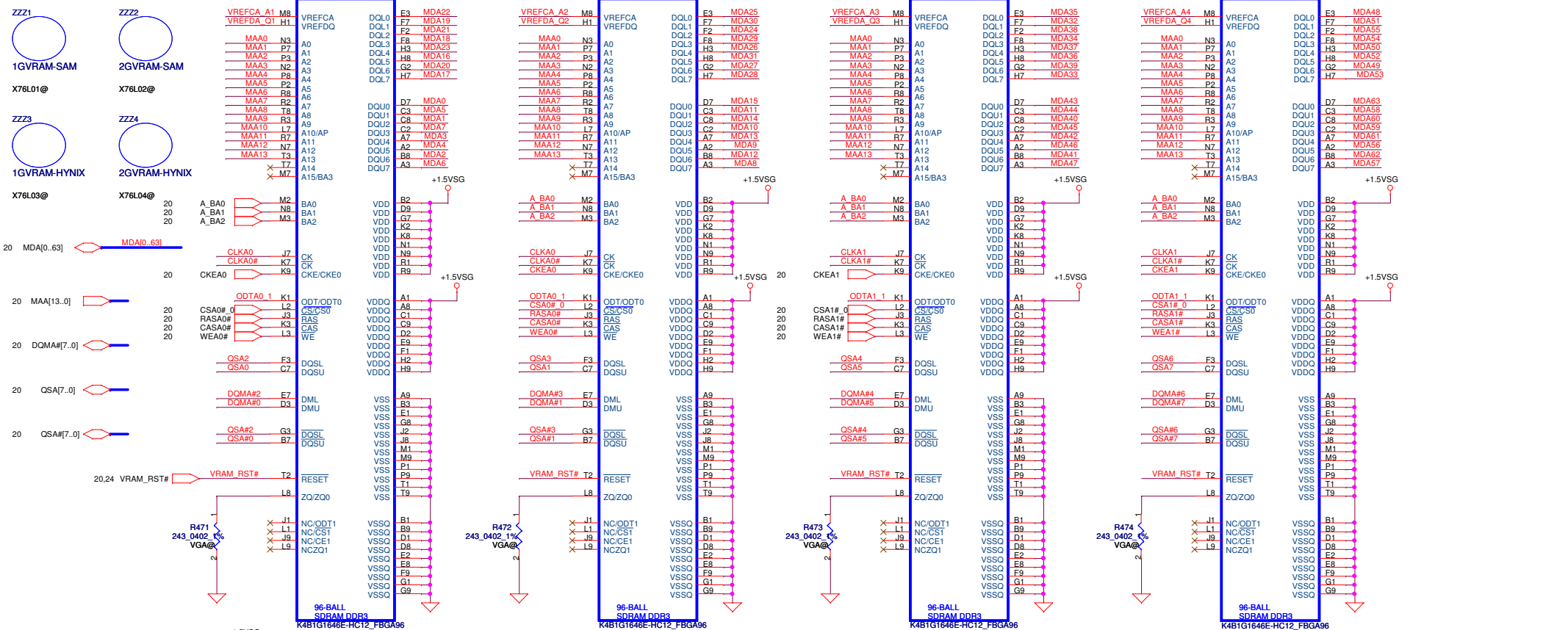
Park/Madison :AL21left NC
 Seymour/Whistler:
 AL21:PX_EN use to control discreate GPU regulators for power express BACO mode
 Support BACO: output High3.3V:turn off regulators (BACO mode on) output Low0V:turn on regulators (BACO mode off) need PD resistor
 No support BACO: left NC



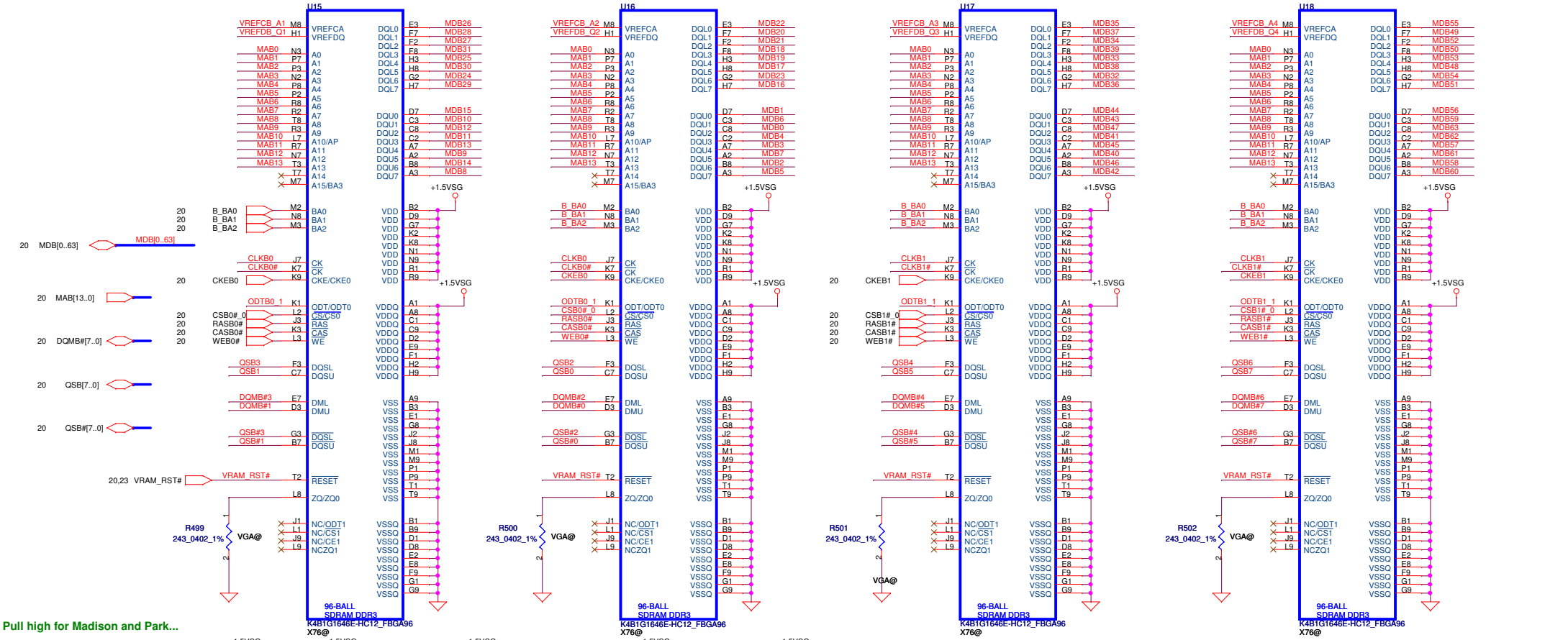
Security Classification	Compal Secret Data	
Issued Date	2010/07/12	Deciphered Date
		2012/07/12

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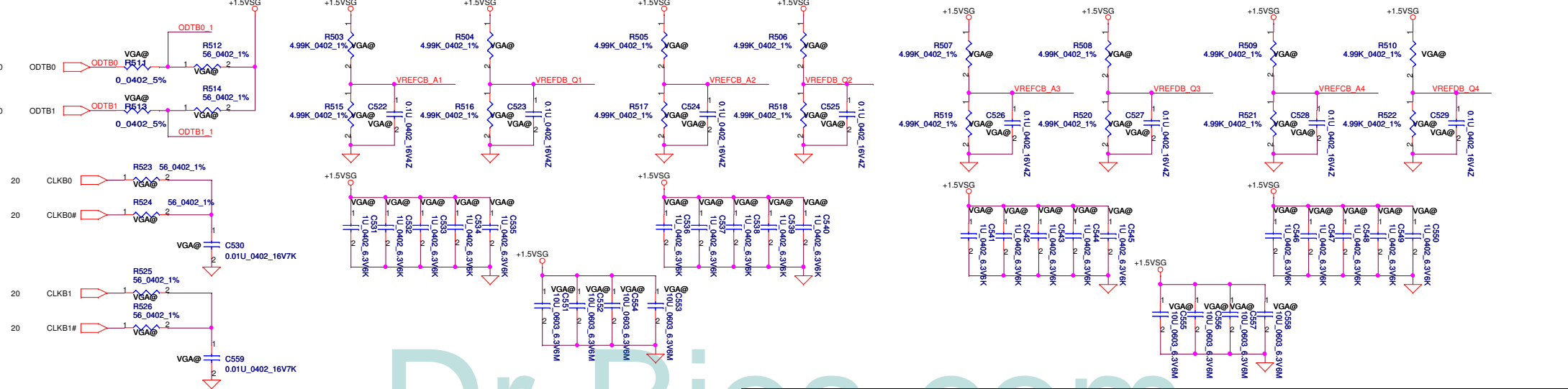
Compal Electronics, Inc.		
Title	Vancouver Power/GND	
Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03
Date:	Tuesday, February 22, 2011	Sheet 22 of 49



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title
				VRAM DDR3 / Channel A
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				QBL60 LA-7552P
				Rev 0.03
				Date: Tuesday, February 22, 2011
				Sheet 23 of 49

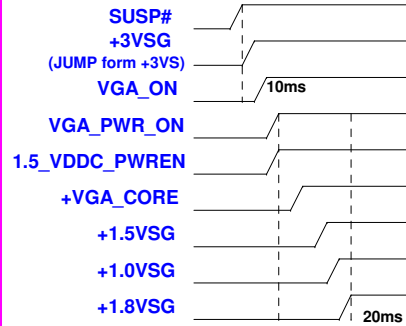


Pull high for Madison and Park...

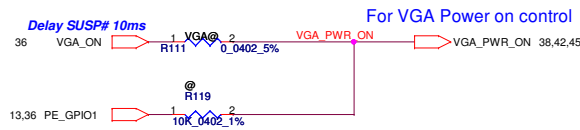
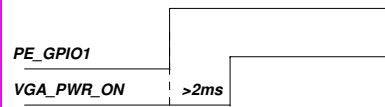


Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/12	VRAM_DDR3 / Channel B	
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				Sheet	24 of 49

Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

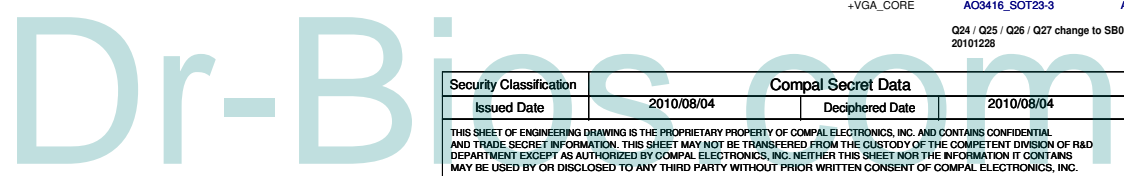
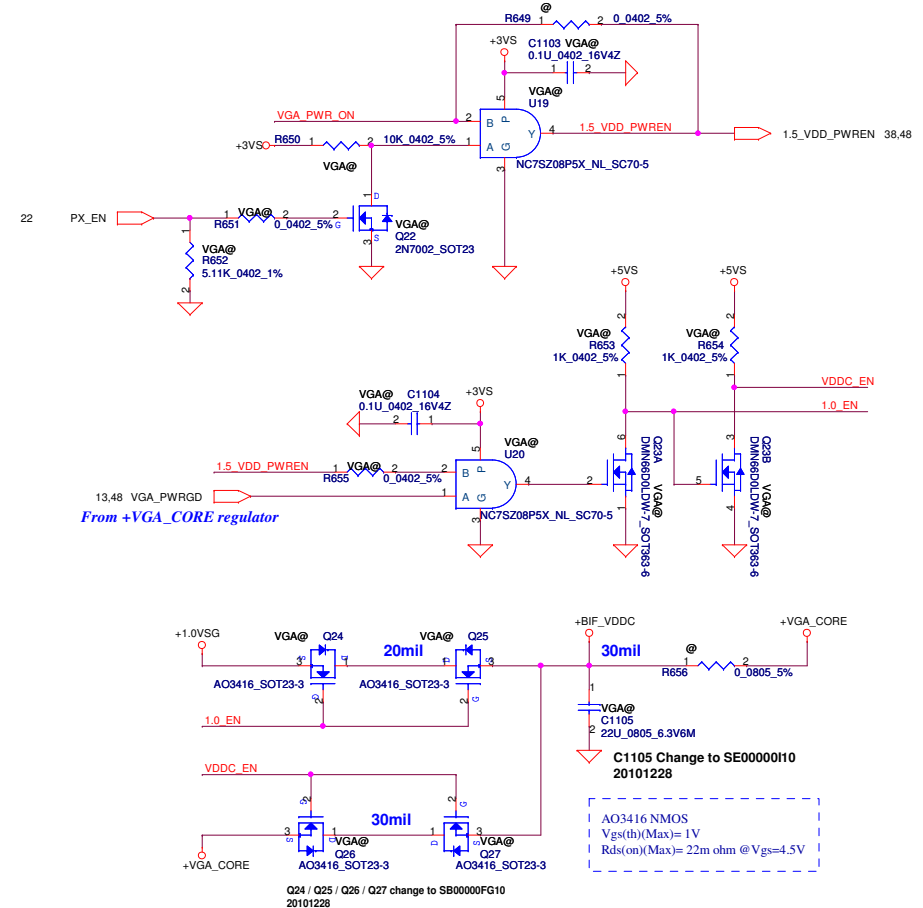


VGA Muxless with BACO Status Mapping table

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

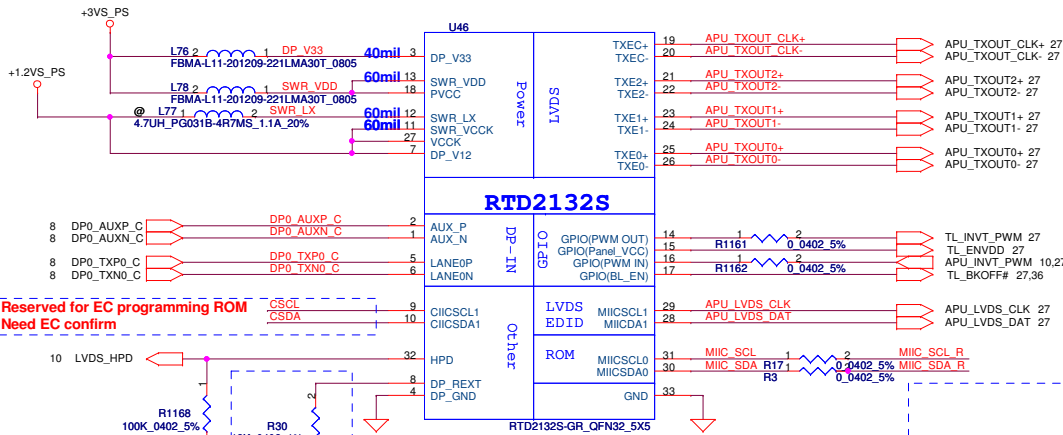
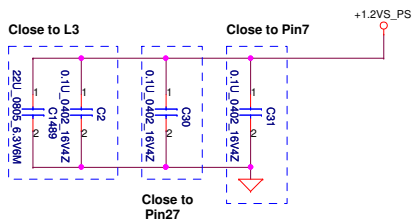
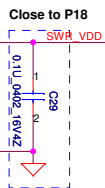
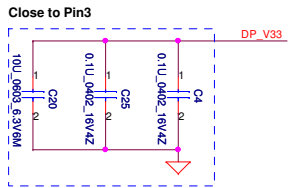
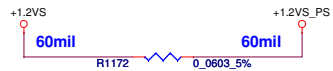
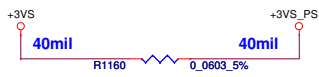
VGA_PWR_ON source signal	Whistler
+3.3VSG	VGA_ON
+1.8VSG	SUSP#
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



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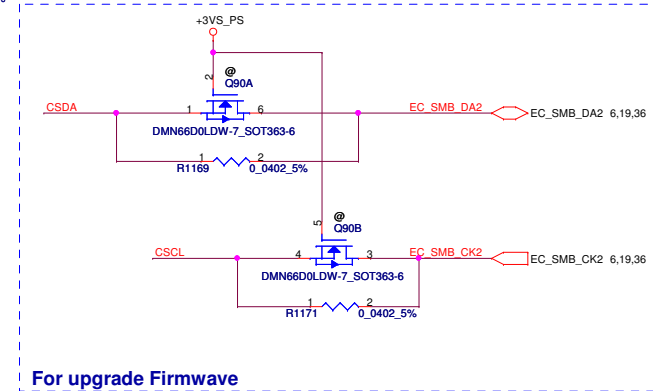
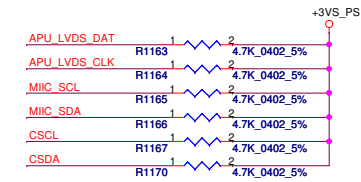
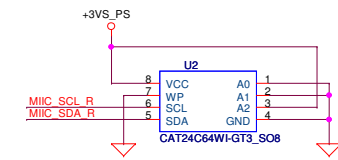
Compal Electronics, Inc.		
Title	VGA power sequence and BACO	
Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03
Date:	Tuesday, February 22, 2011	Sheet 25 of 49



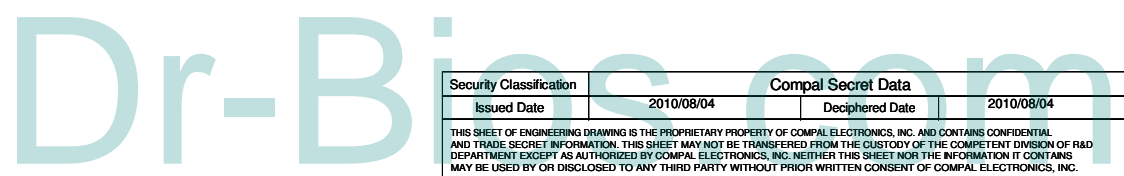
Reserved for EC programming ROM
Need EC confirm

Change to 12Kohm 1% (DG ref.)
20101114

EEROM

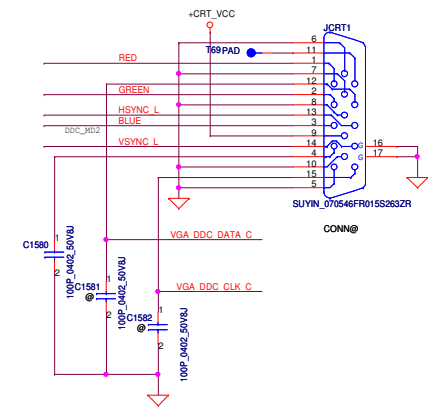
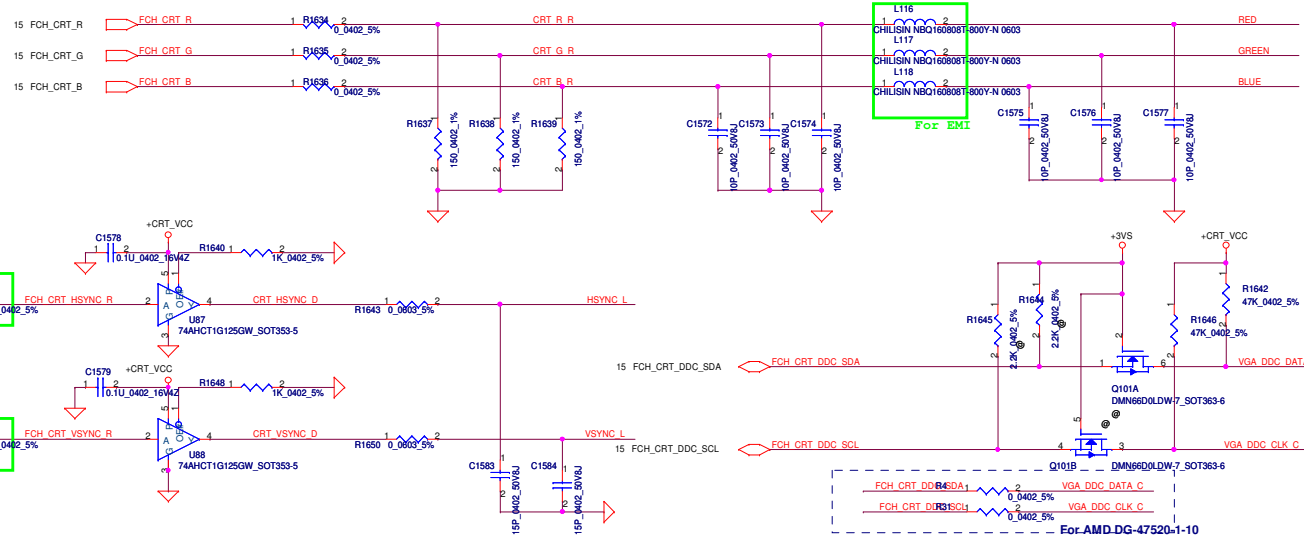
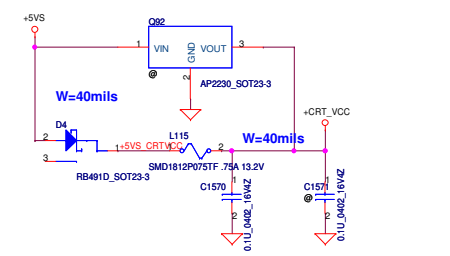
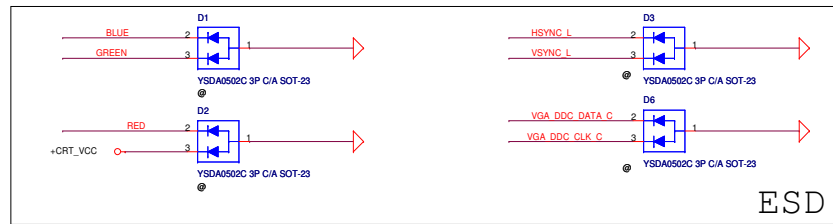


For upgrade Firmwave

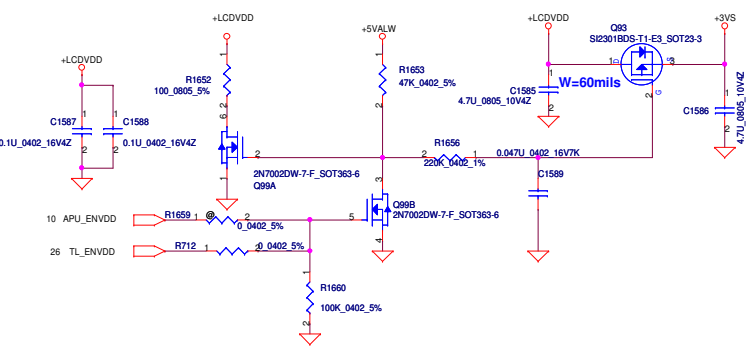


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Title	LVDS Translator - RTD2132S		
Size	Document Number	Rev	
Custom	QBL60 LA-7552P	0.03	
Date:	Tuesday, February 22, 2011	Sheet	26 of 49

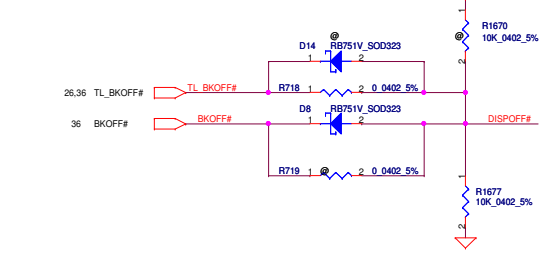
CRT



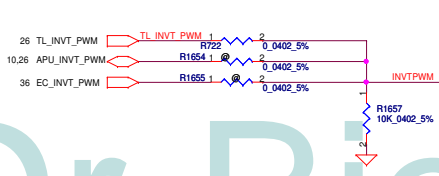
Panel LCDVDD Control



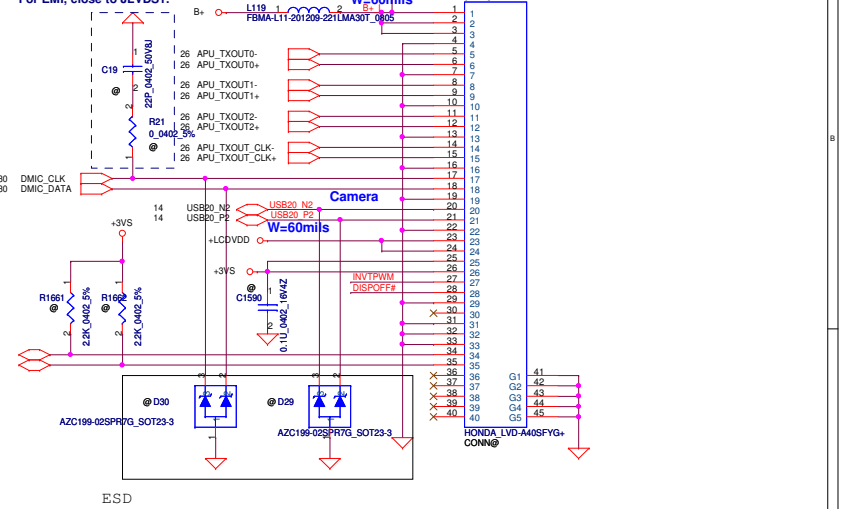
Panel Backlight Control



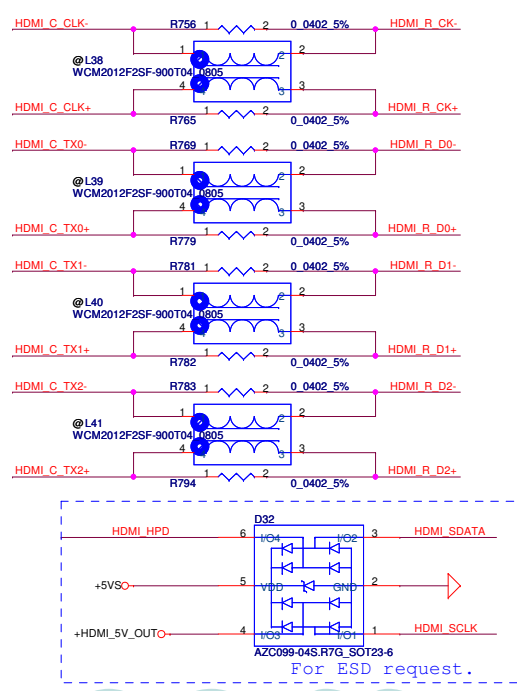
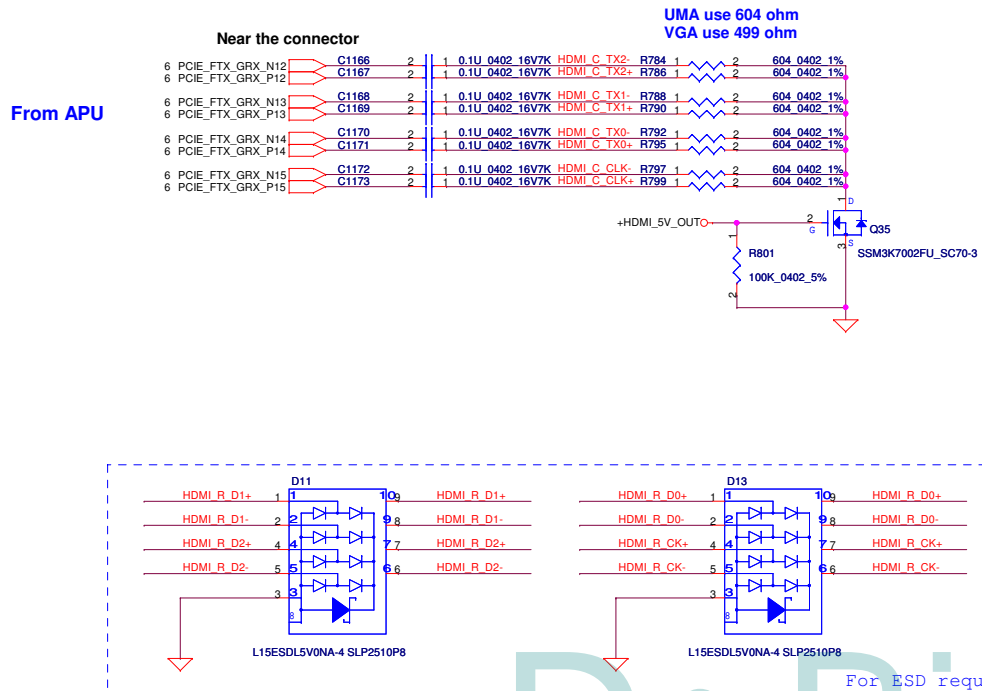
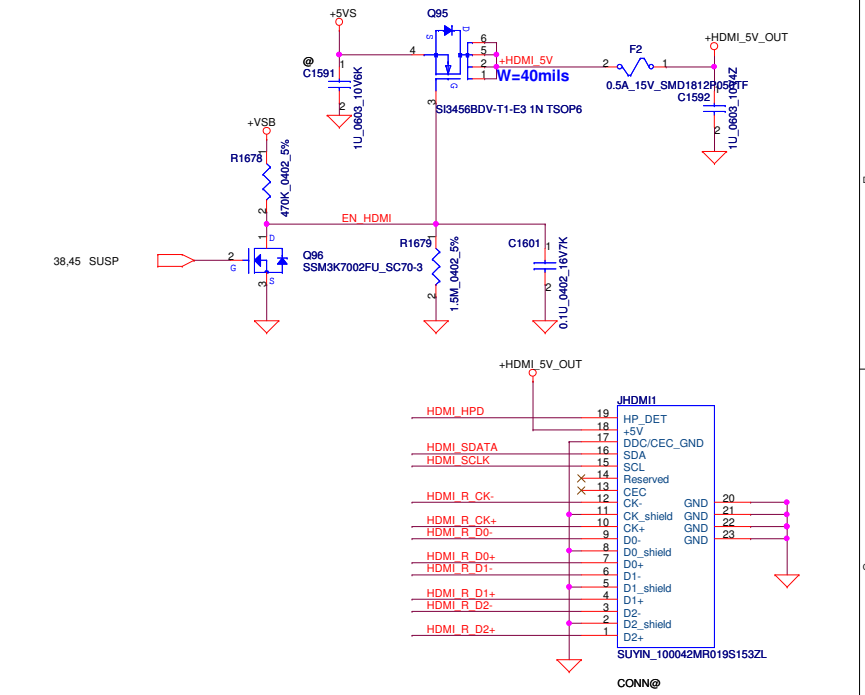
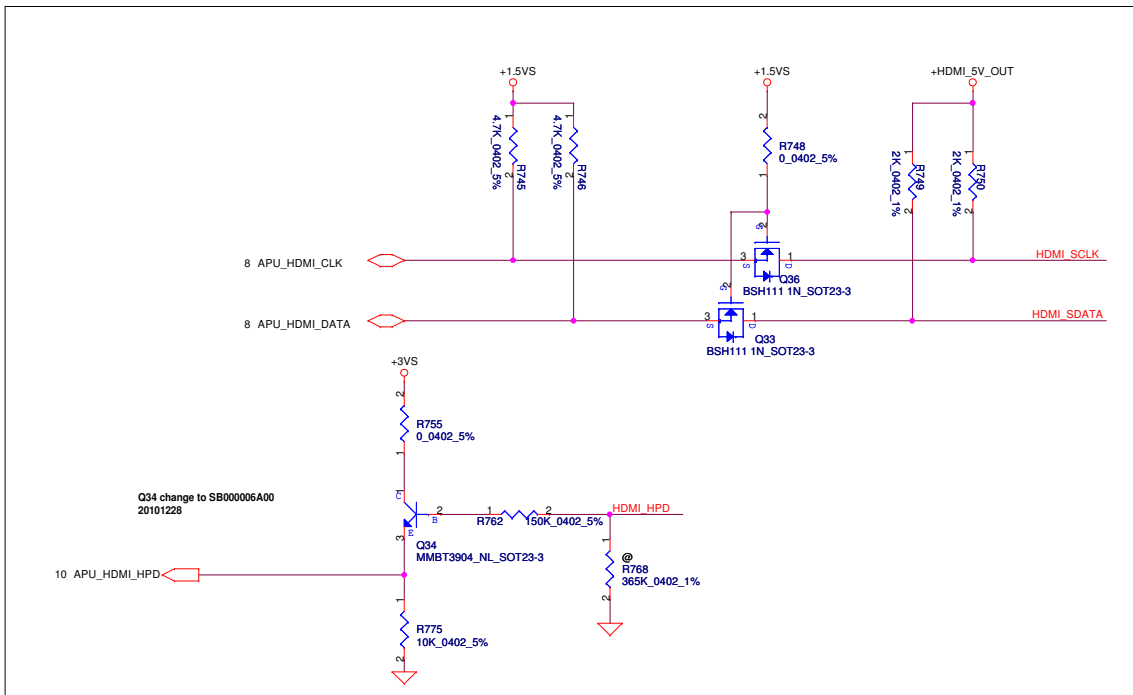
Panel PWM Control



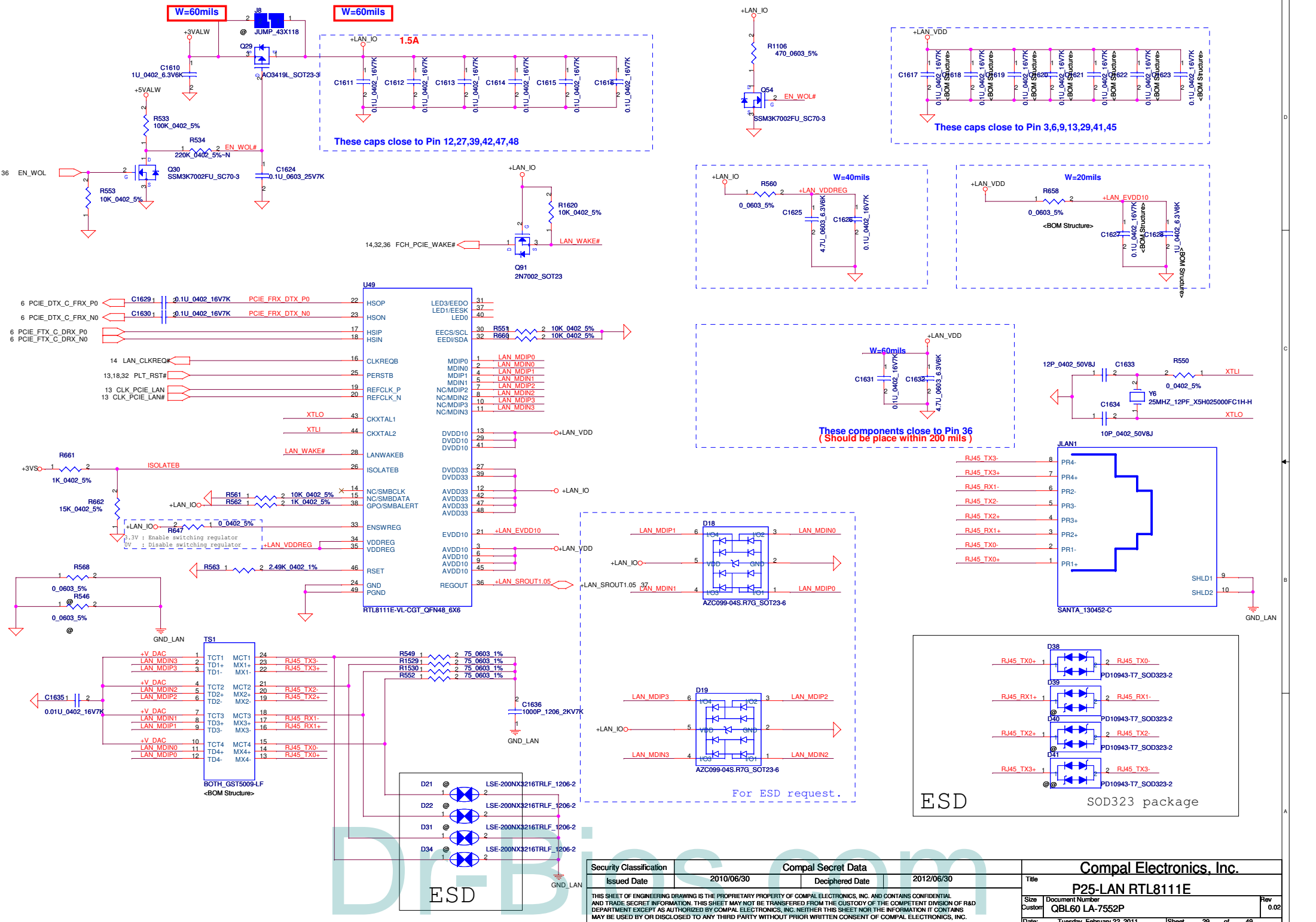
For EMI, close to JLVDS1.



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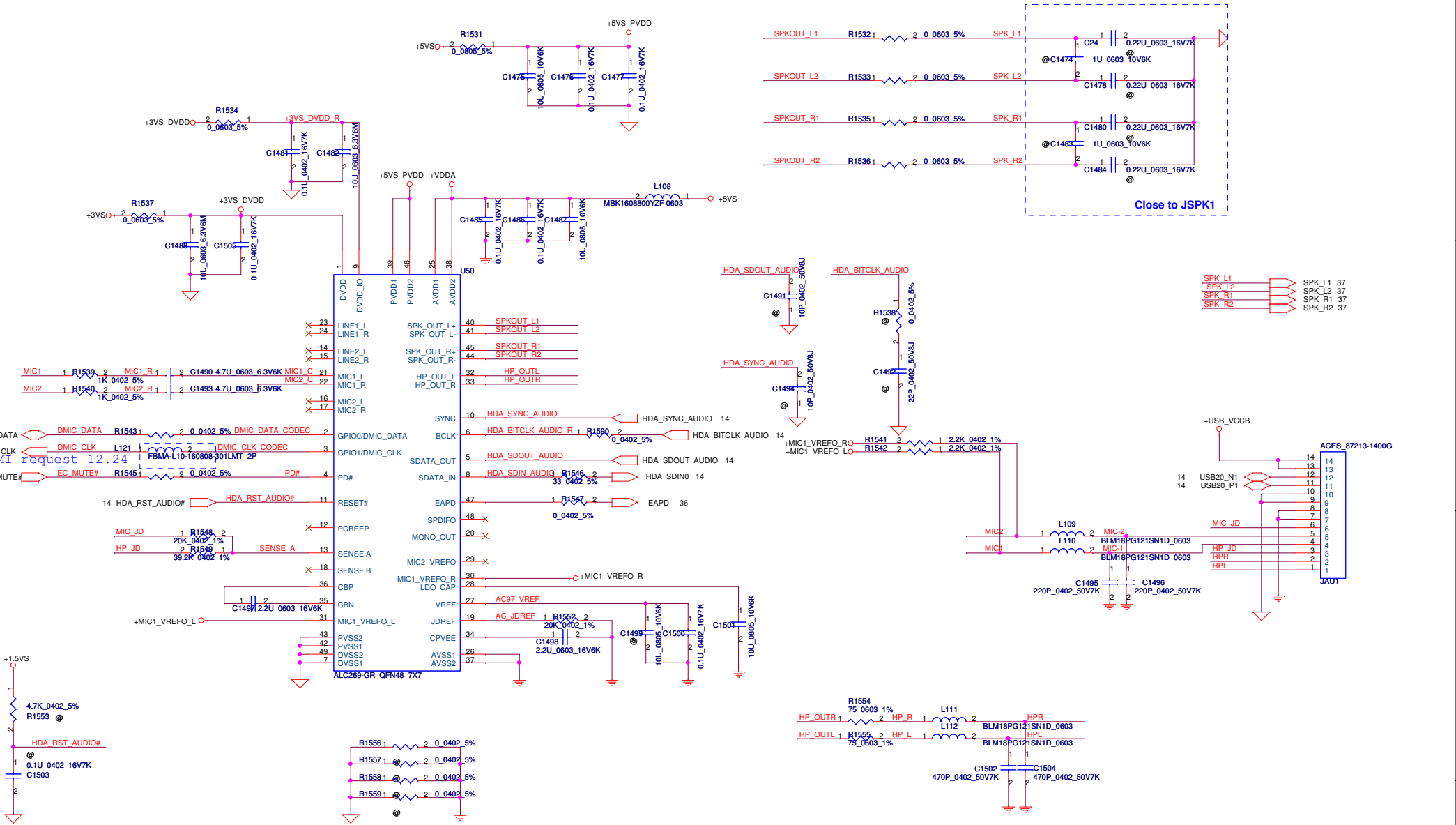
Security Classification	Compal Secret Data	Title	HDMI Connector	
Issued Date	2010/08/04	Deciphered Date	2010/08/04	Rev
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		Date:	Tuesday, February 22, 2011	1 Sheet 28 of 49



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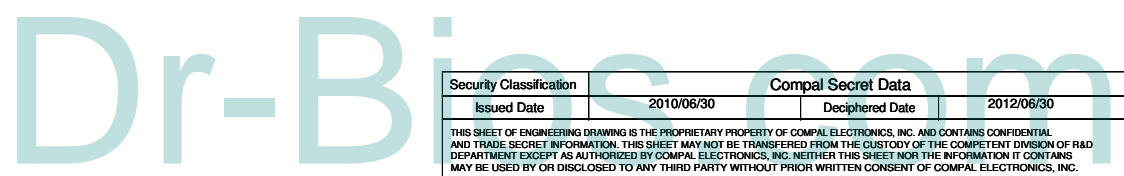
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Size			P25-LAN RTL8111E	
Customer	Document Number	Rev		
QBL60	LA-7552P	0.02		
Date:	Tuesday, February 22, 2011	Sheet	29	of 49



Close to JSPK1

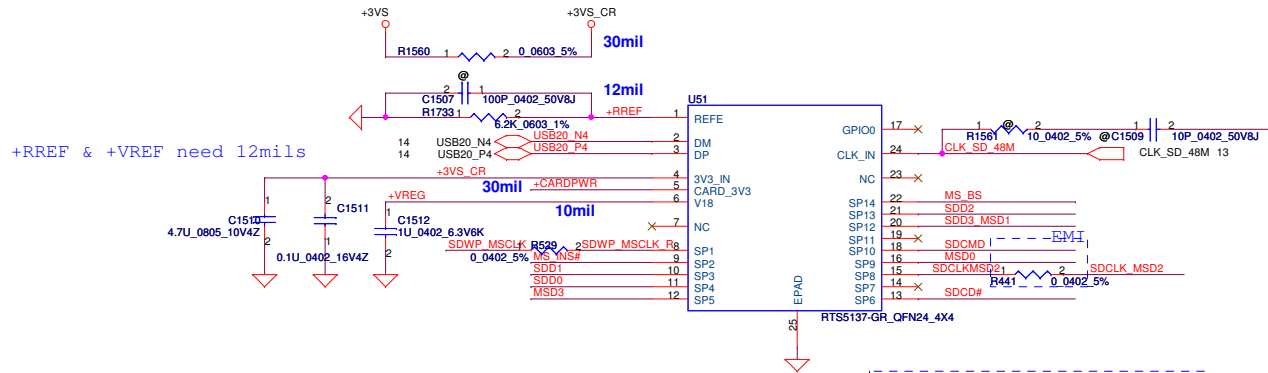
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- SPK L2 → SPK L2 37
- SPK R1 → SPK R1 37
- SPK R2 → SPK R2 37

ACES_87213-1400G

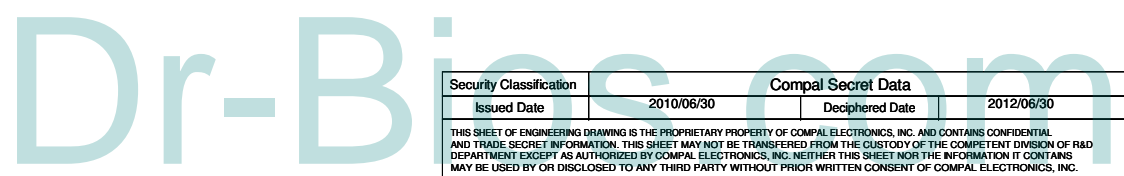
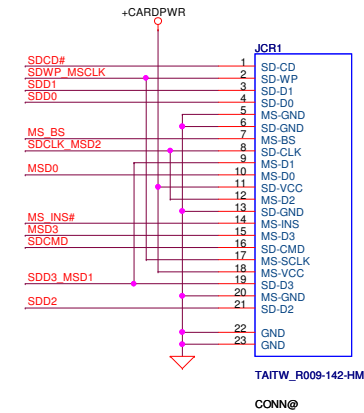
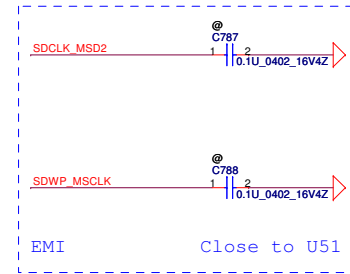
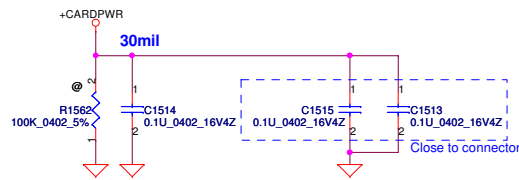


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Size	Document Number	Rev			
Customer	QBL60 LA-7552P	0.03			
Date:	Tuesday, February 22, 2011	Sheet	30	of 49	

Card Reader RTS5137 (only SD/MMC/MS function)



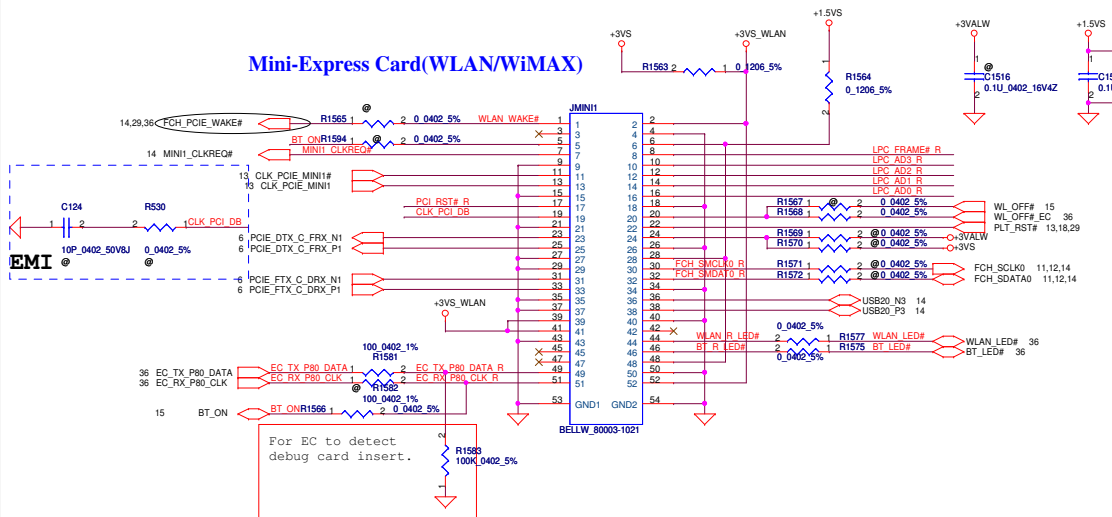
Card Reader Connector



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Size	Document Number	Rev		0.03	
Custom	QBL60 LA-752P				
Date:	Tuesday, February 22, 2011	Sheet	31	of	49

Mini-Express Card for WLAN/WiMAX(Half)

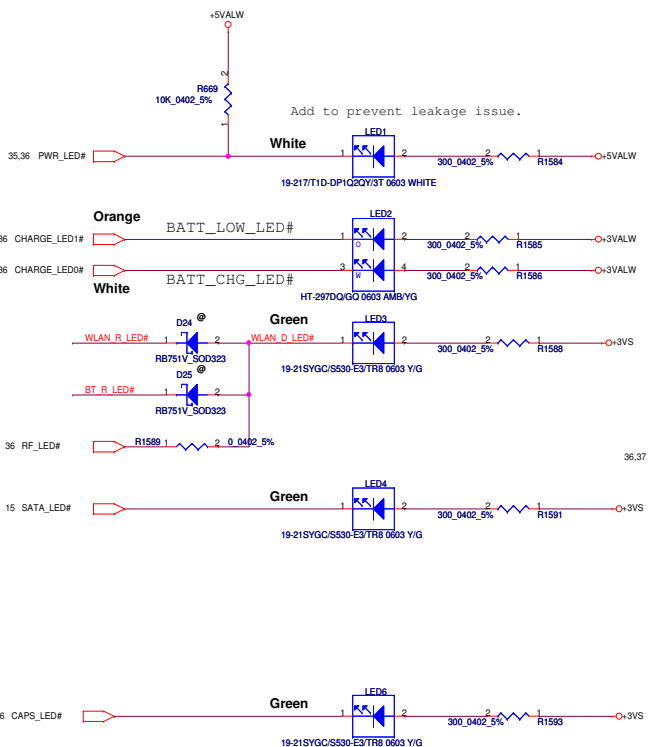
Mini-Express Card(WLAN/WiMAX)



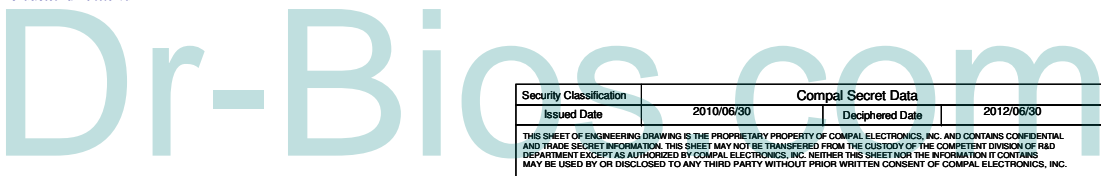
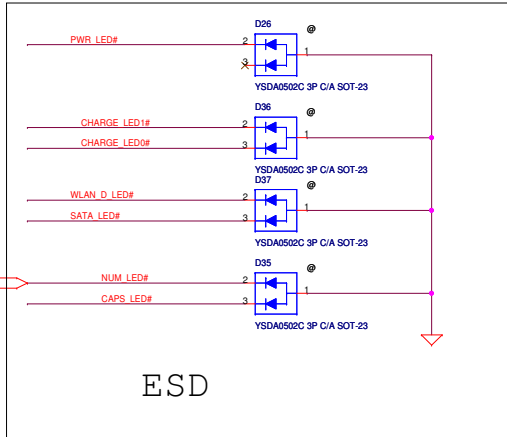
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R1573	1	2	0.0402_5%	LPC_FRAME#	LPC_FRAME#	13.36
LPC_AD3 R	R1574	1	2	0.0402_5%	LPC_AD3	LPC_AD3	13.36
LPC_AD2 R	R1576	1	2	0.0402_5%	LPC_AD2	LPC_AD2	13.36
LPC_AD1 R	R1578	1	2	0.0402_5%	LPC_AD1	LPC_AD1	13.36
LPC_ADD R	R1579	1	2	0.0402_5%	LPC_ADD	LPC_ADD	13.36
PCI_RST# R	R1580	1	2	0.0402_5%	PLT_RST#	PLT_RST#	13
CLK_PCIE_DB					CLK_PCIE_DB	CLK_PCIE_DB	13

LED

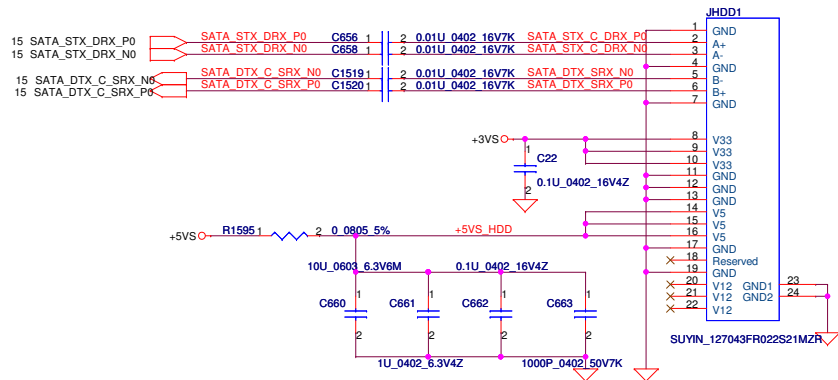


ESD

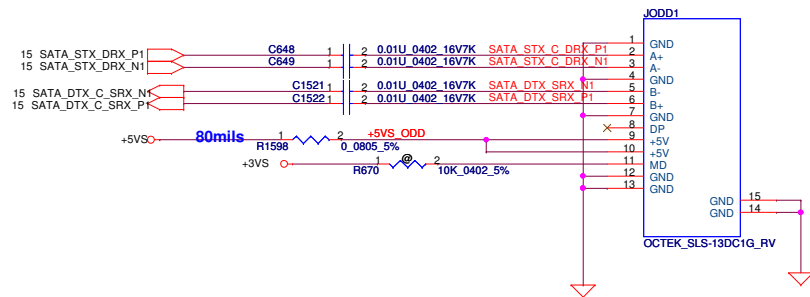


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				P28-Mini PCIE/LED	
				QBL60 LA-7552P	
				Date:	Rev
				Tuesday, February 22, 2011	0.03
				Sheet	of
				32	49

SATA HDD Conn.

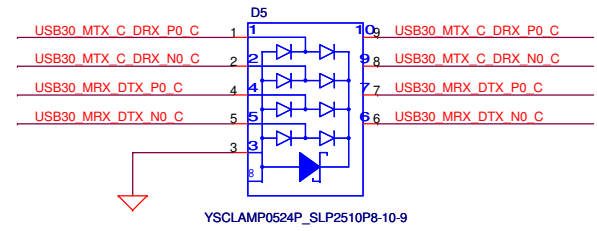
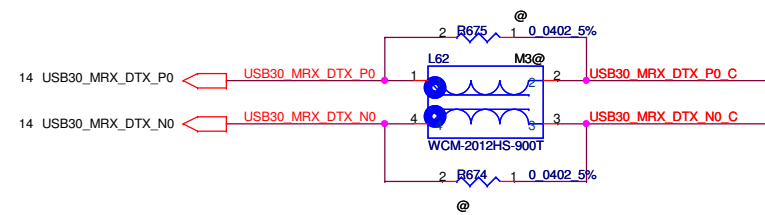
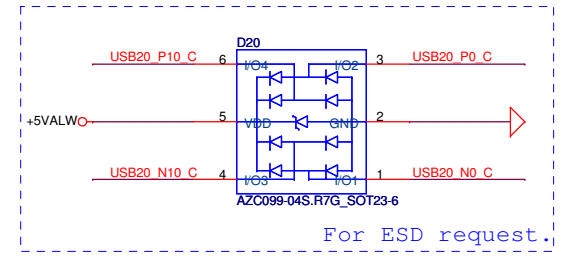
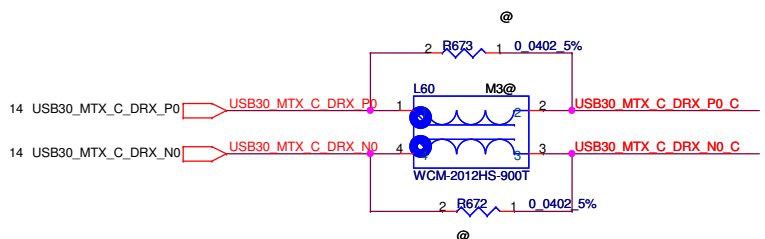
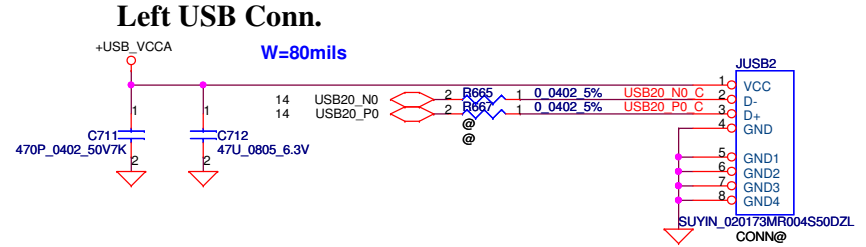
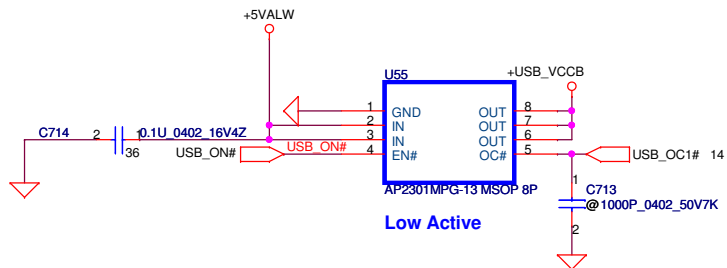
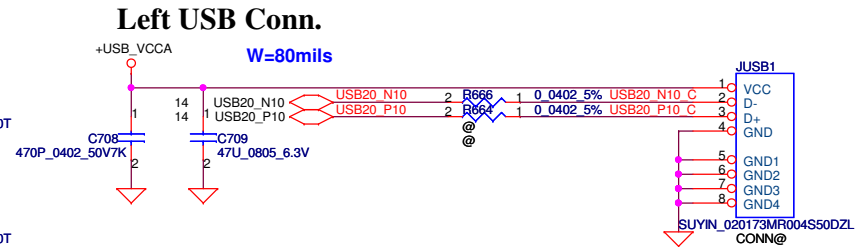
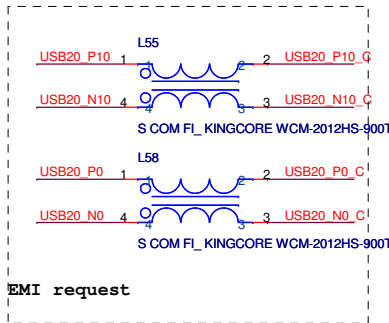
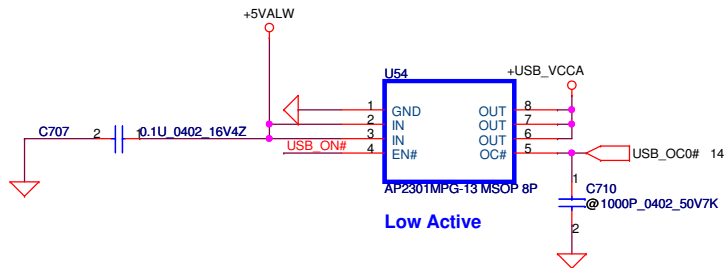


SATA ODD FFC Conn.



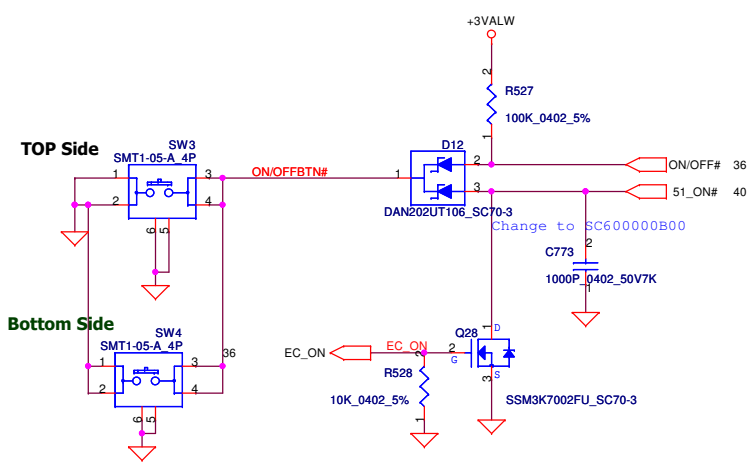
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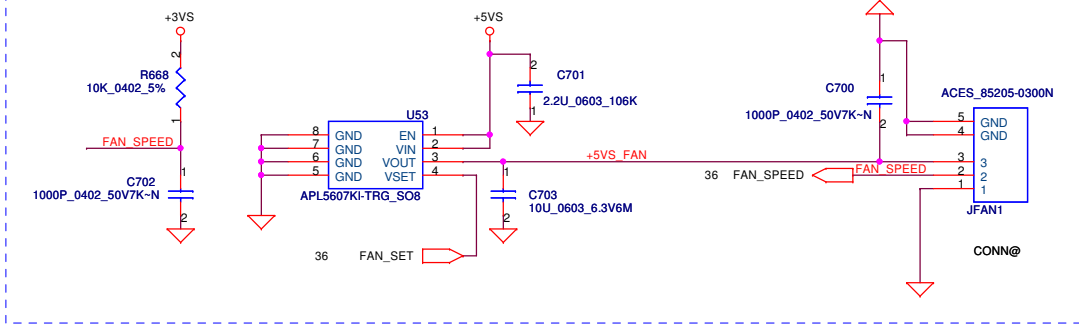


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				Custom	QBL60 LA-7552P
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				Rev	0.03

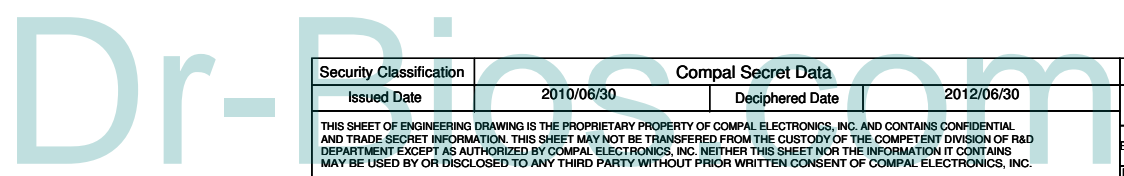
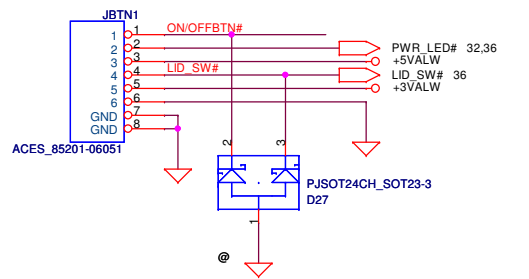
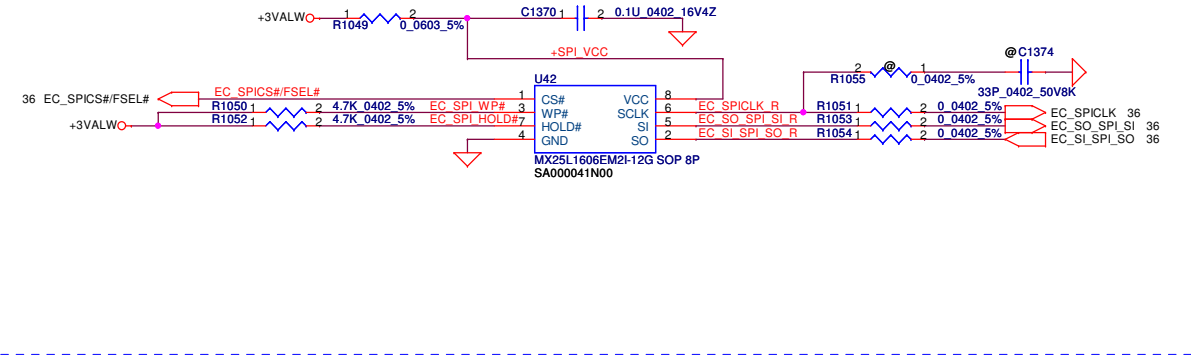
ON/OFF switch Power Button



Fan Control Circuit

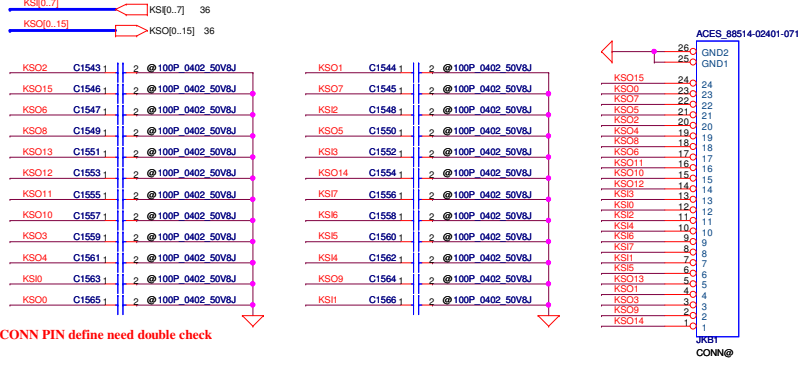


EC BIOS ROM

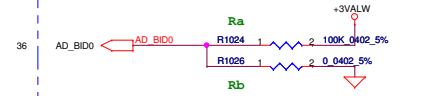


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				B	QBL60 LA-7552P
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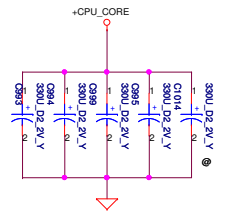
INT_KBD Conn.



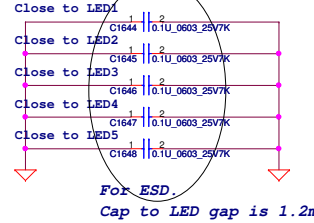
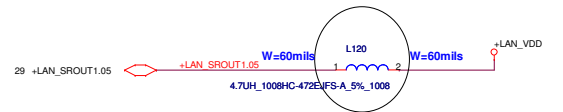
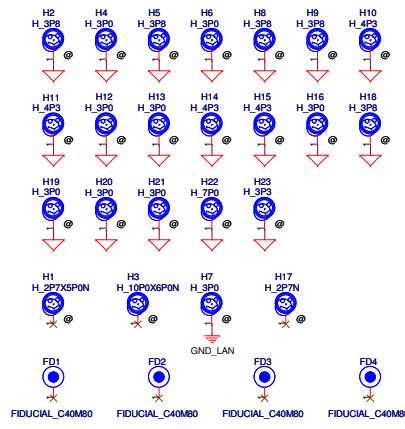
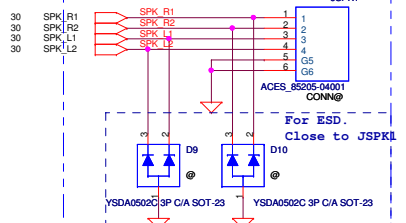
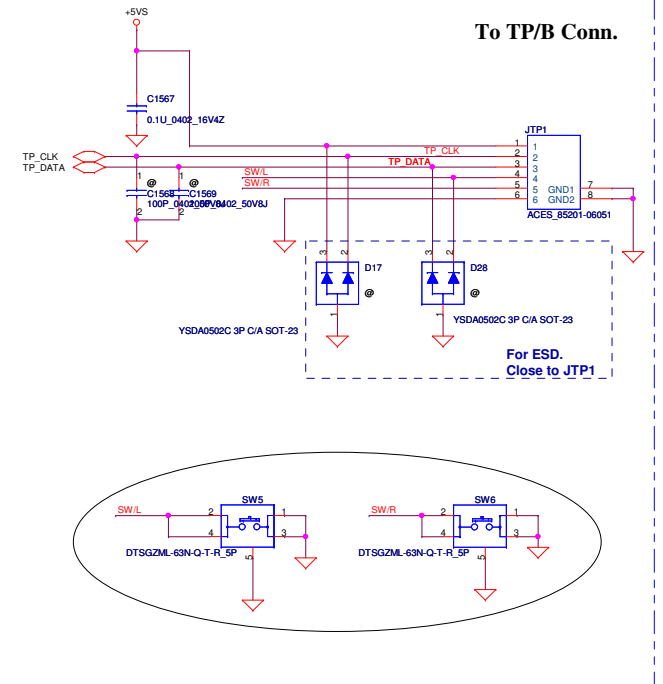
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V



P9 FS1 PWR/GND

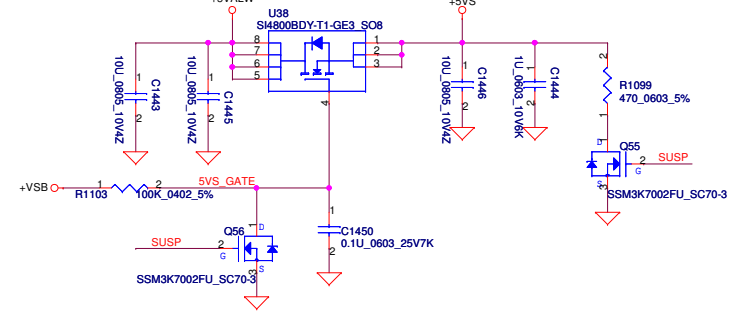


To TP/B Conn.

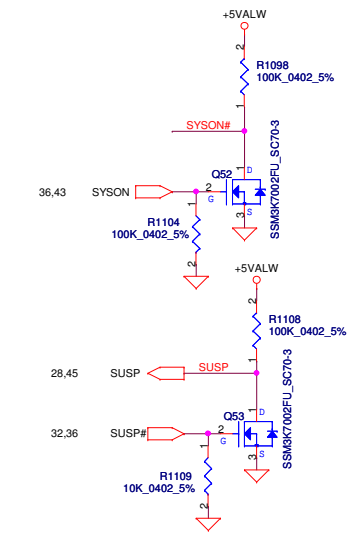
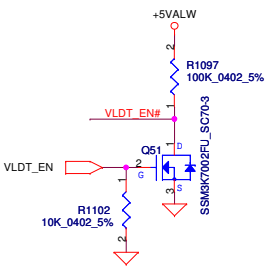
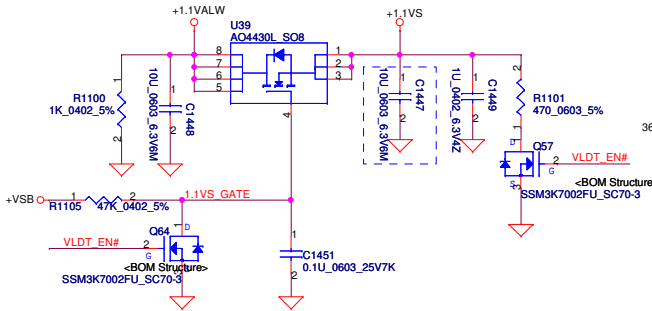


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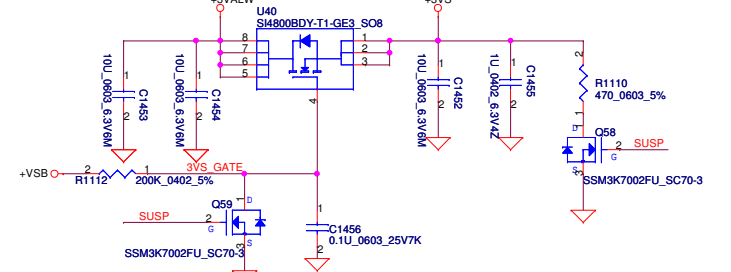
+5VALW TO +5VS (5A)



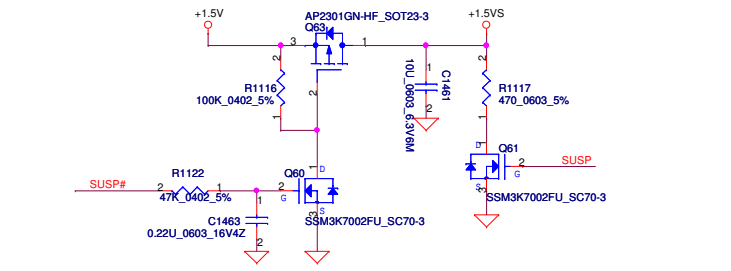
+1.1VALW TO +1.1VS (1.1A)



+3VALW TO +3VS (3.3A)

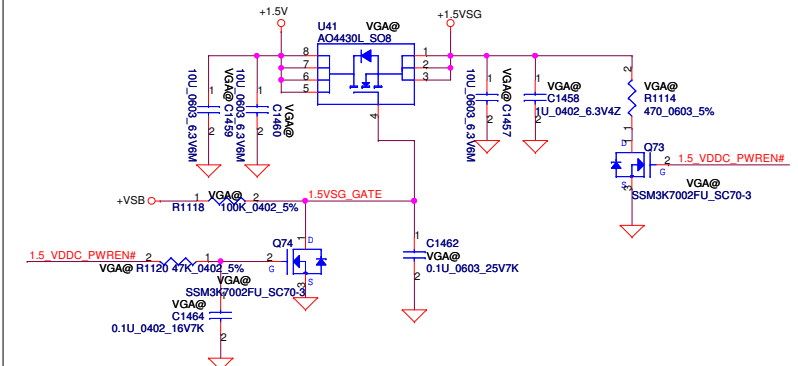


+1.5V TO +1.5VS (1.5A)

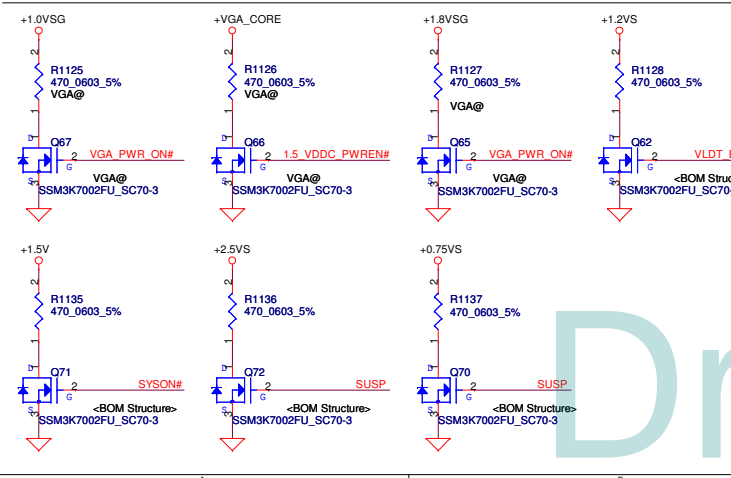
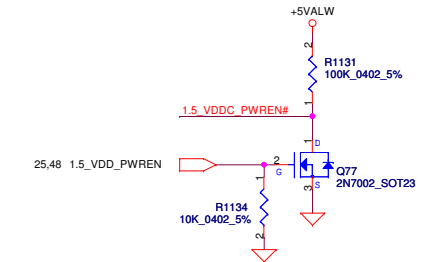
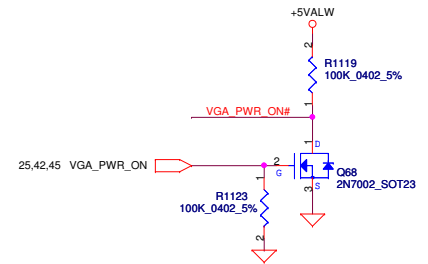
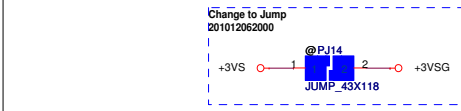


VGA Power

+1.5V to +1.5VSG (1.5A)

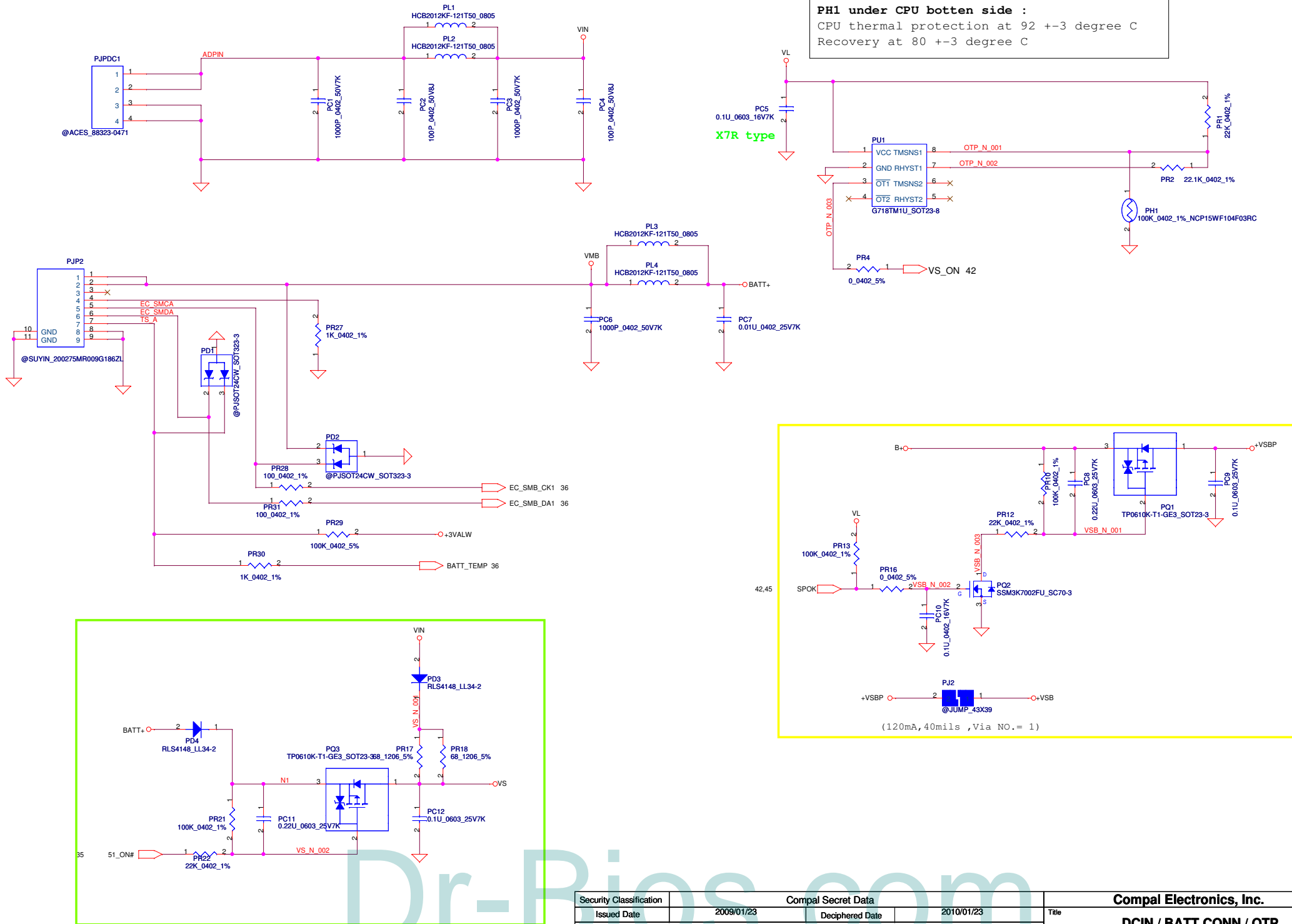


+3VS to +3VSG (3.3A)



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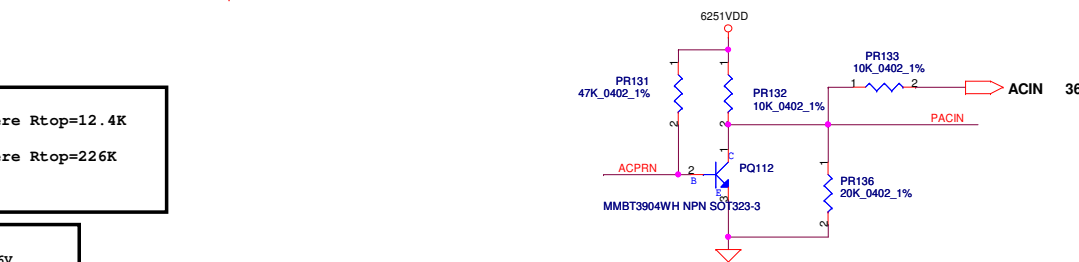
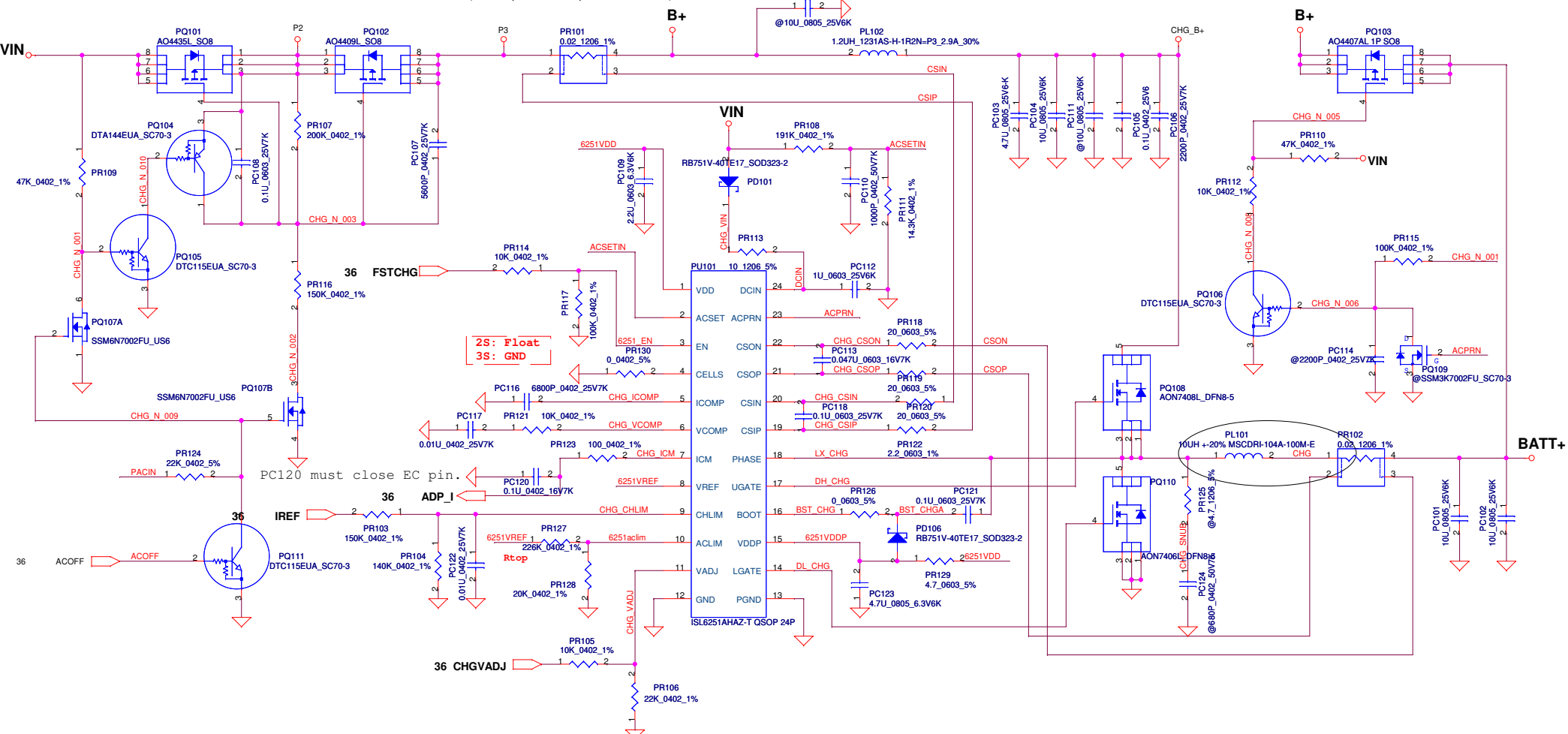
PH1 under CPU botten side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C



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Title DCIN / BATT CONN / OTP		
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(B+ 6A,240mils ,Via NO.= 12)



$CP = 85\% \cdot I_{ada}$;
 $I_{ada} = 0 \sim 4.737A$ (90W); $CP = 4.03A$; where $R_{acdet} = 0.020\Omega$, where $R_{top} = 12.4K$
 90W for Dis: $R_{top} = SD00000AJ80$
 $I_{ada} = 0 \sim 3.421A$ (65W); $CP = 2.91A$; where $R_{acdet} = 0.020\Omega$, where $R_{top} = 226K$
 65W for UMA: $R_{top} = SD034226380$
 Astro2010_01_15 need confirm P/N

CP mode
 $V_{aclim} = V_{REF} \cdot (R_{bot} / R_{internal} / (R_{top} / R_{internal} + R_{bot} / R_{internal}))$
 when 90W $V_{aclim} = 2.39 \cdot (20K / 152K) / (20K / 152K + 12.4K / 152K) = 1.44966V$
 when 65W $V_{aclim} = 2.39 \cdot (20K / 152K) / (20K / 152K + 226K / 152K) = 0.38914V$
 $I_{input} = (1 / R_{acdet}) \cdot ((0.05 \cdot V_{aclim} / V_{REF} + 0.05))$
 when 90W, $I_{input} = (1 / 0.02) \cdot (0.05 + 1.44966 / 2.39 + 0.05) = 4.02A$
 when 65W, $I_{input} = (1 / 0.02) \cdot (0.05 + 0.38914 / 2.39 + 0.05) = 2.92A$

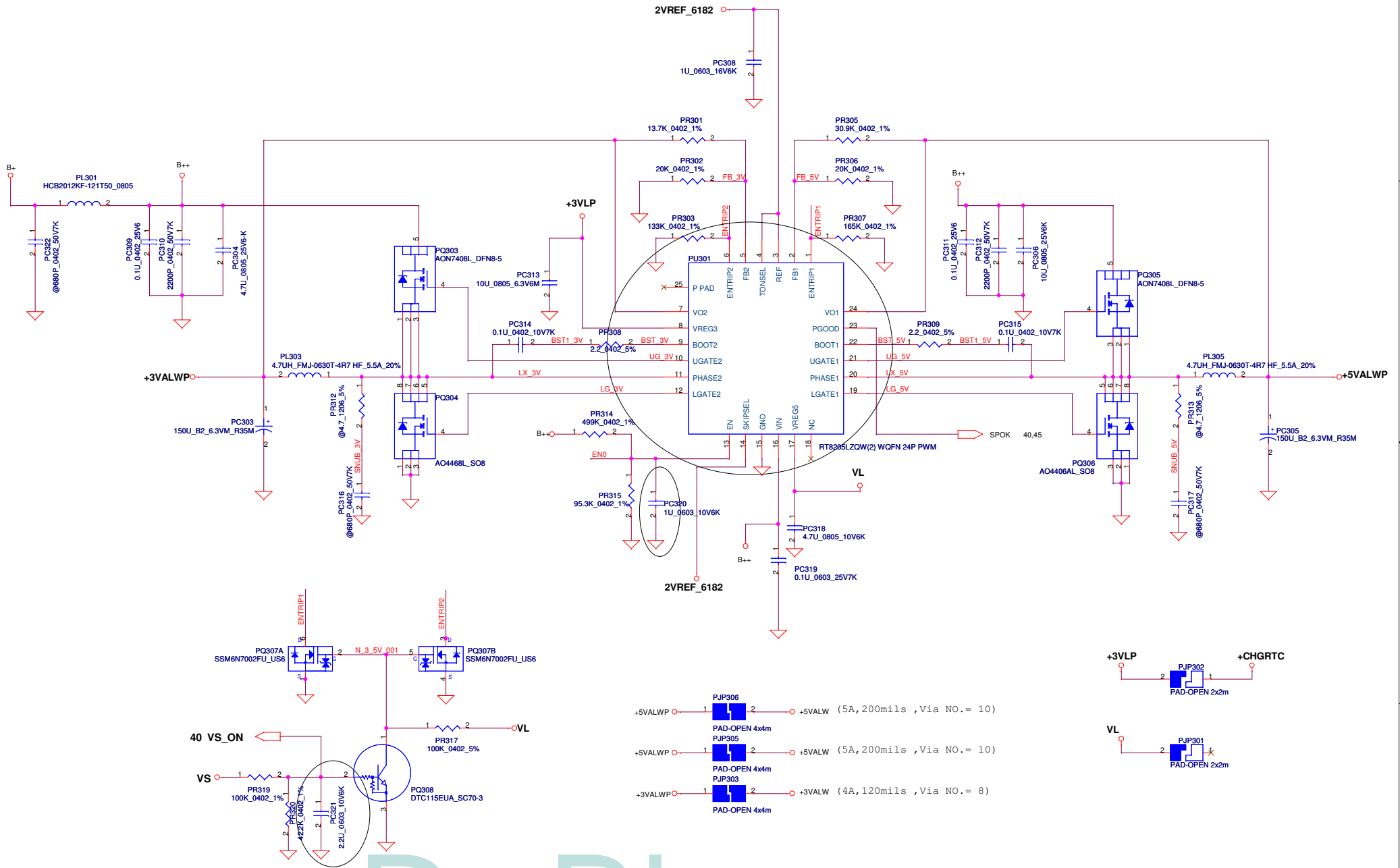
CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V

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		2010/01/23

Compal Electronics, Inc.		
Title		
CHARGER		
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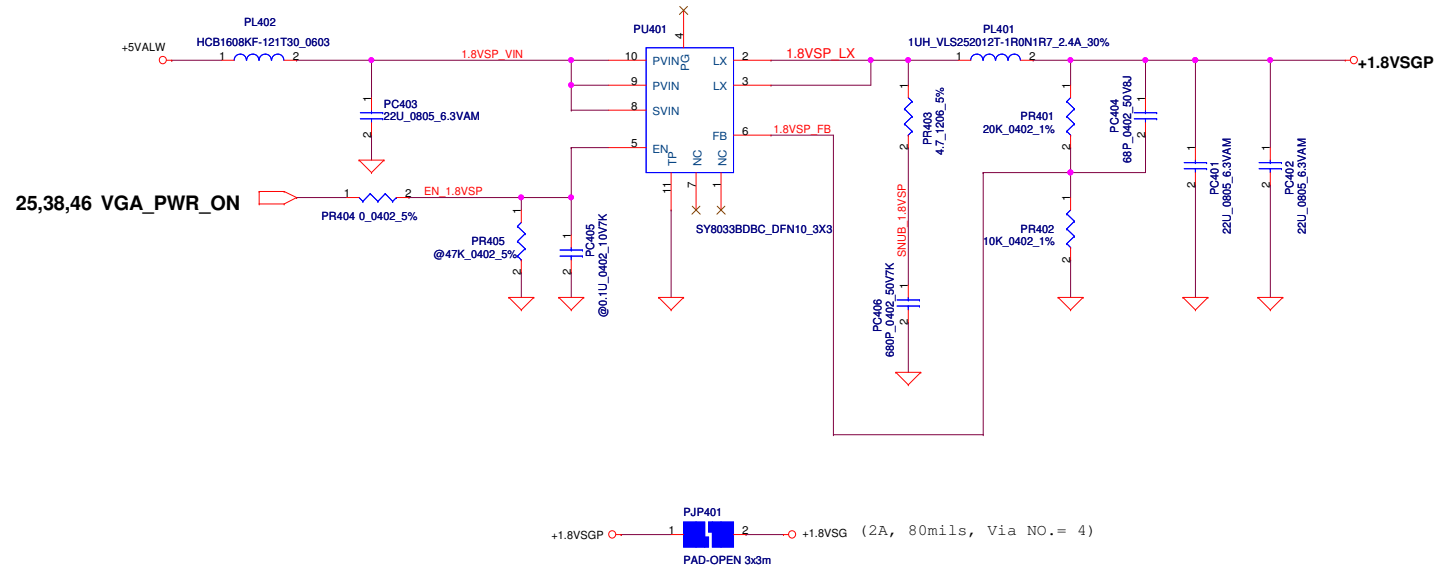
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EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

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		2008/08/02
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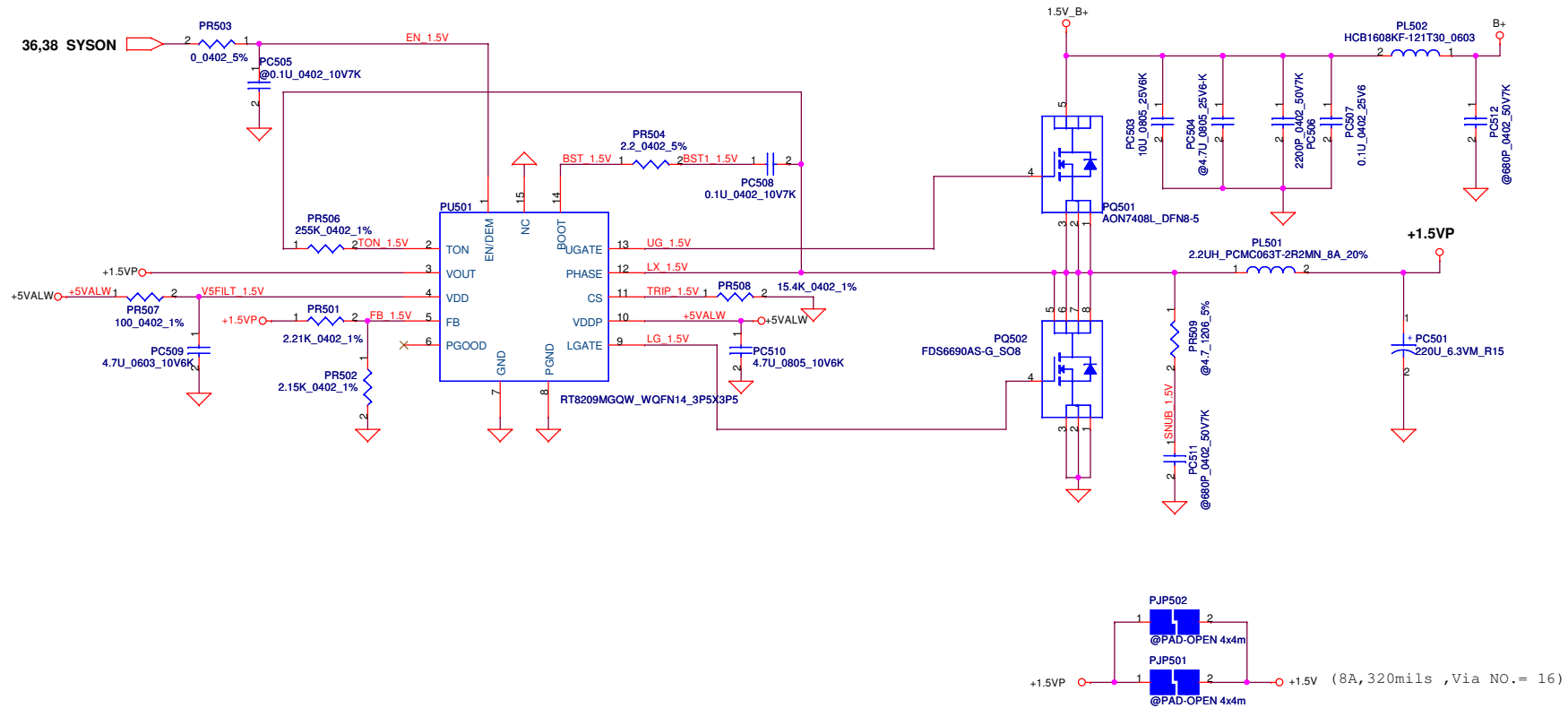
Title		
3.3VALWP/5VALWP		
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<Vo=1.8V> VFB=0.6V
 $V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$

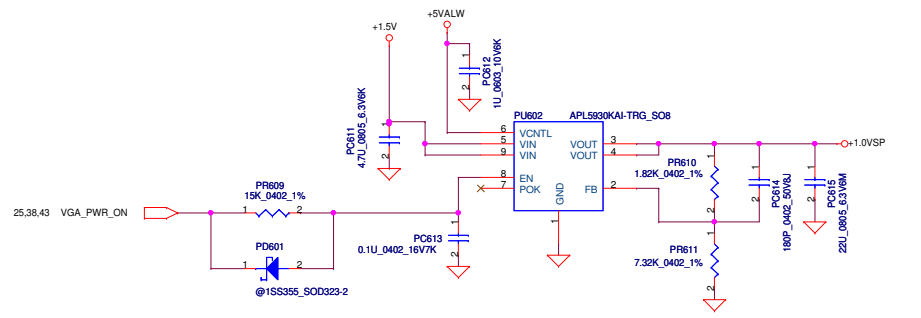
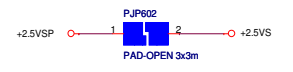
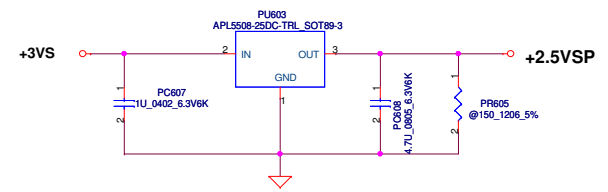
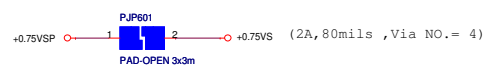
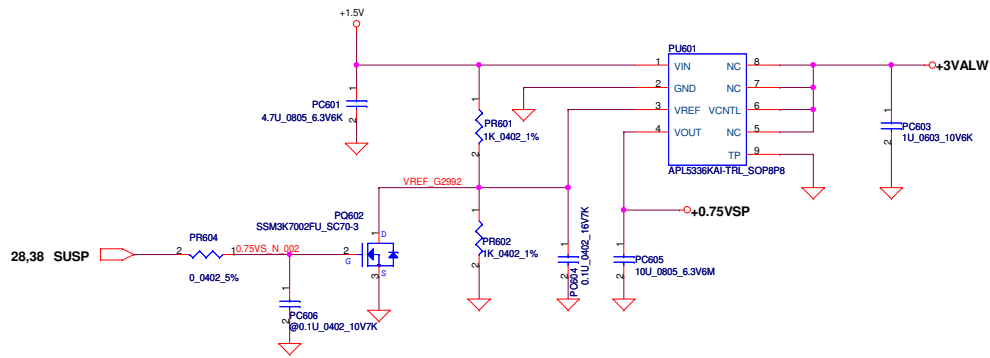
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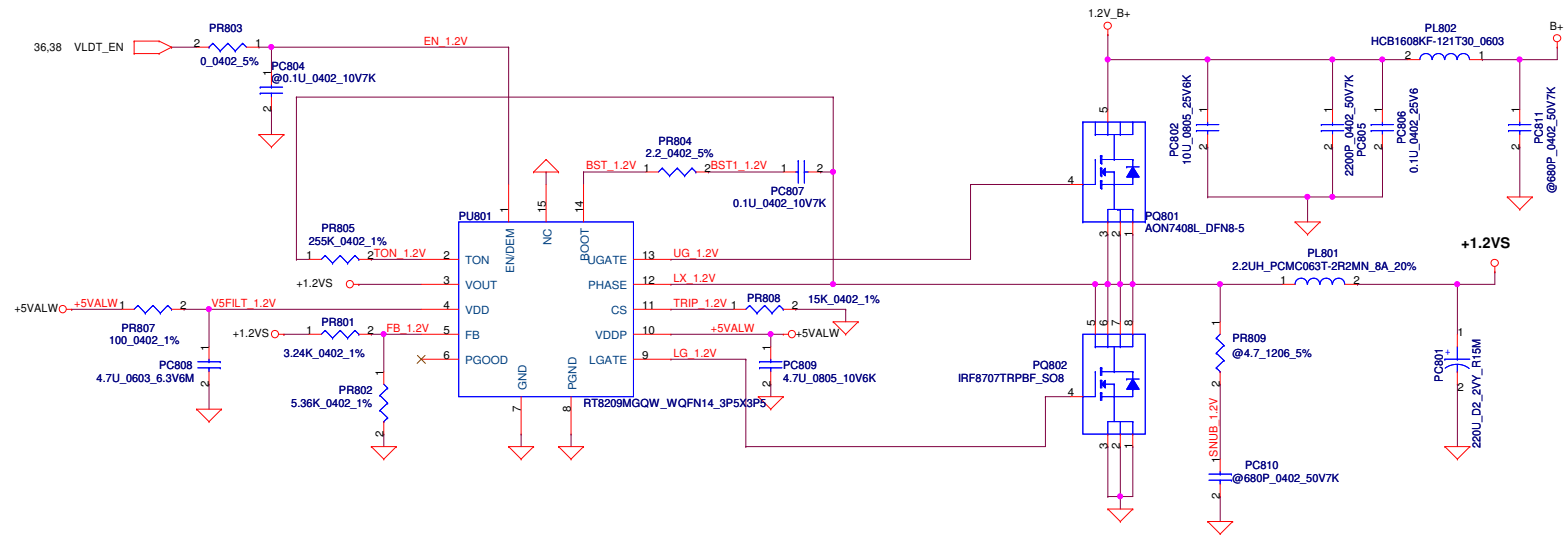
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				Size	Document Number
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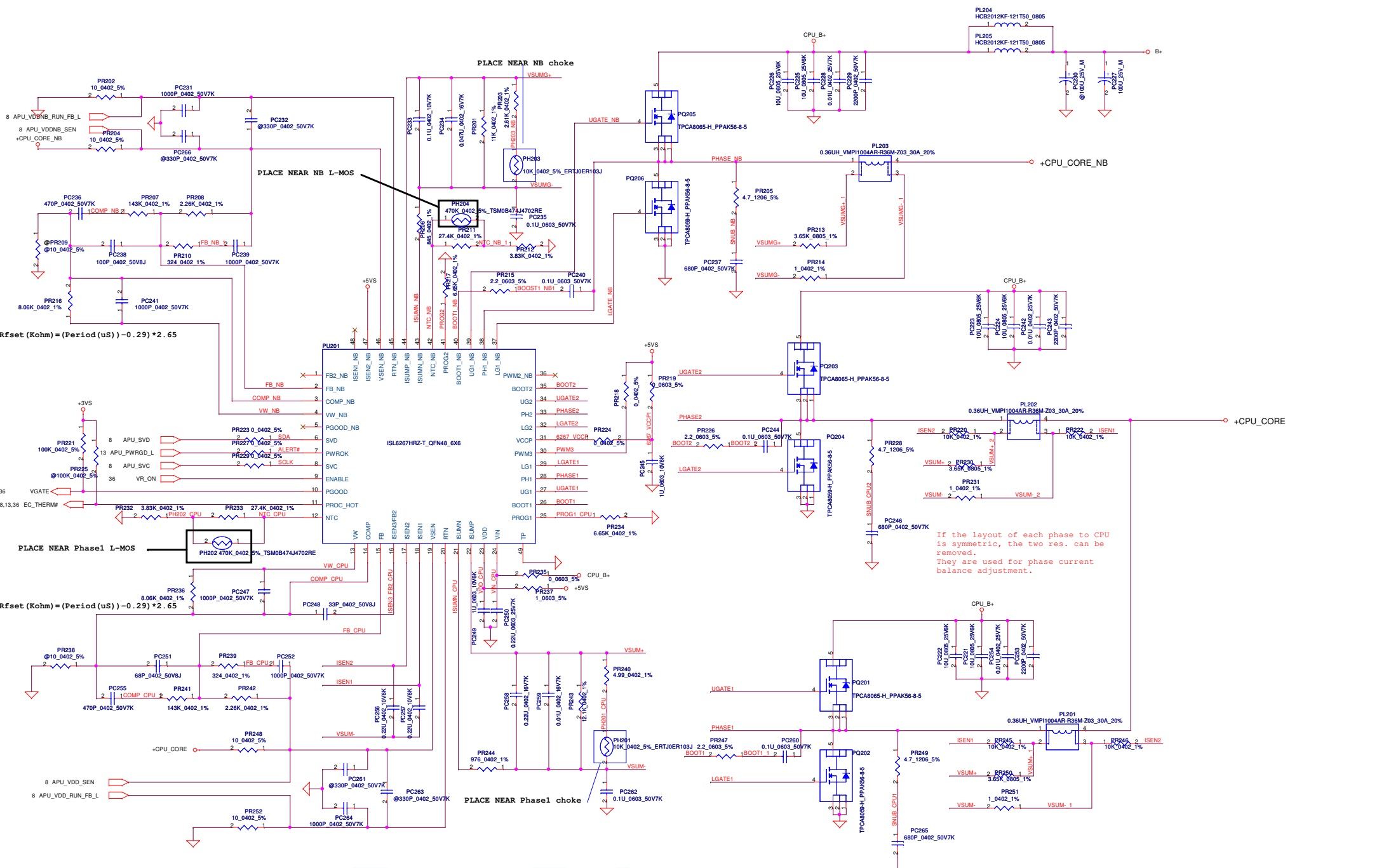
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Issued Date	2006/11/23	Deciphered Date		
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	NCL61 LA-6321P M/B			0.1	
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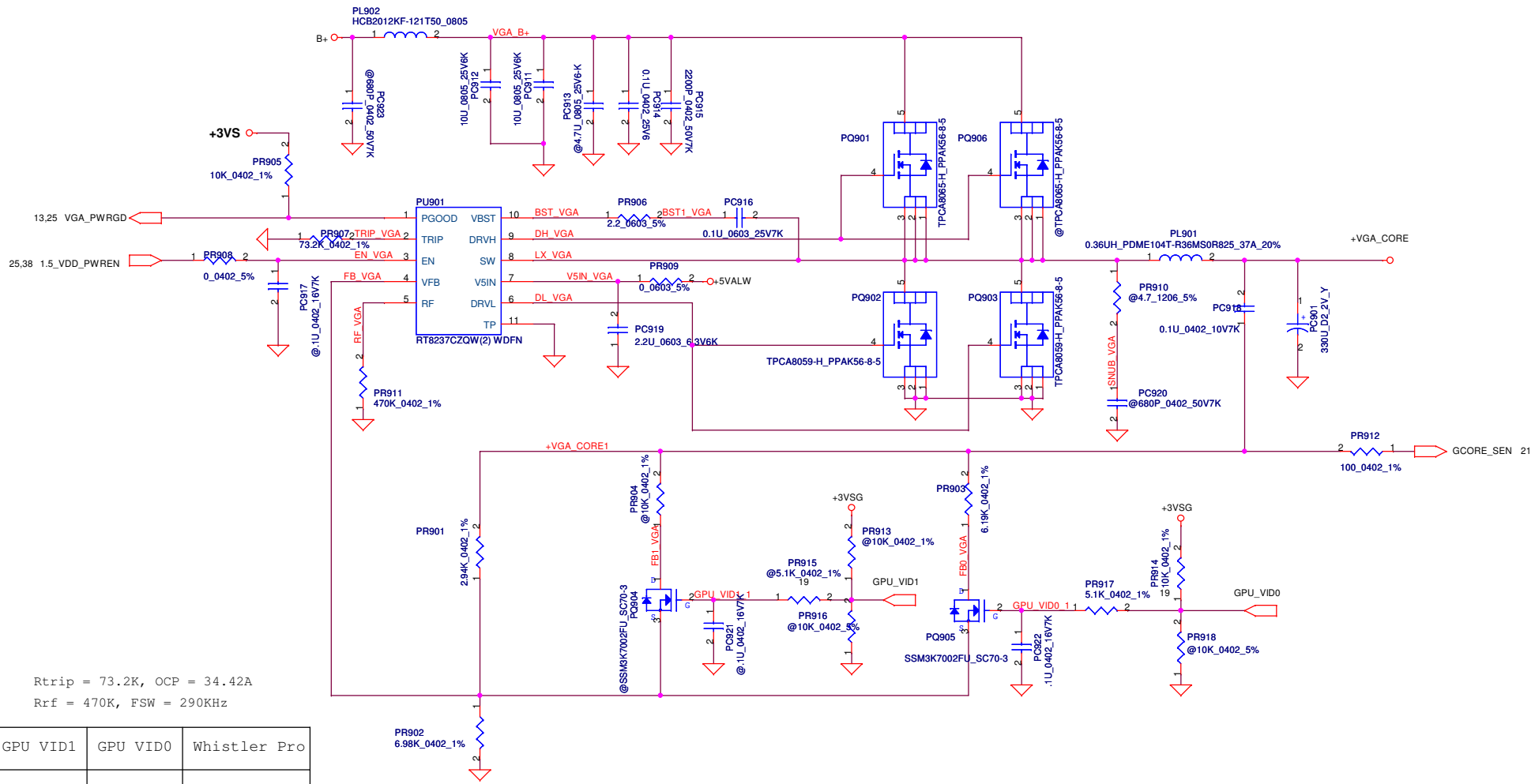
$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$

$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$

If the layout of each phase to CPU is symmetric, the two res. can be removed. They are used for phase current balance adjustment.

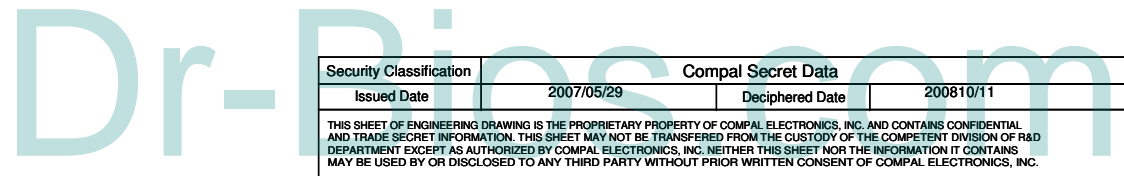


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Issued Date	2010/1/11	Deciphered Date	2011/11/11	
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PWR_+CPU_CORE/+CPU_CORE_NB				
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Rtrip = 73.2K, OCP = 34.42A
 Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

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