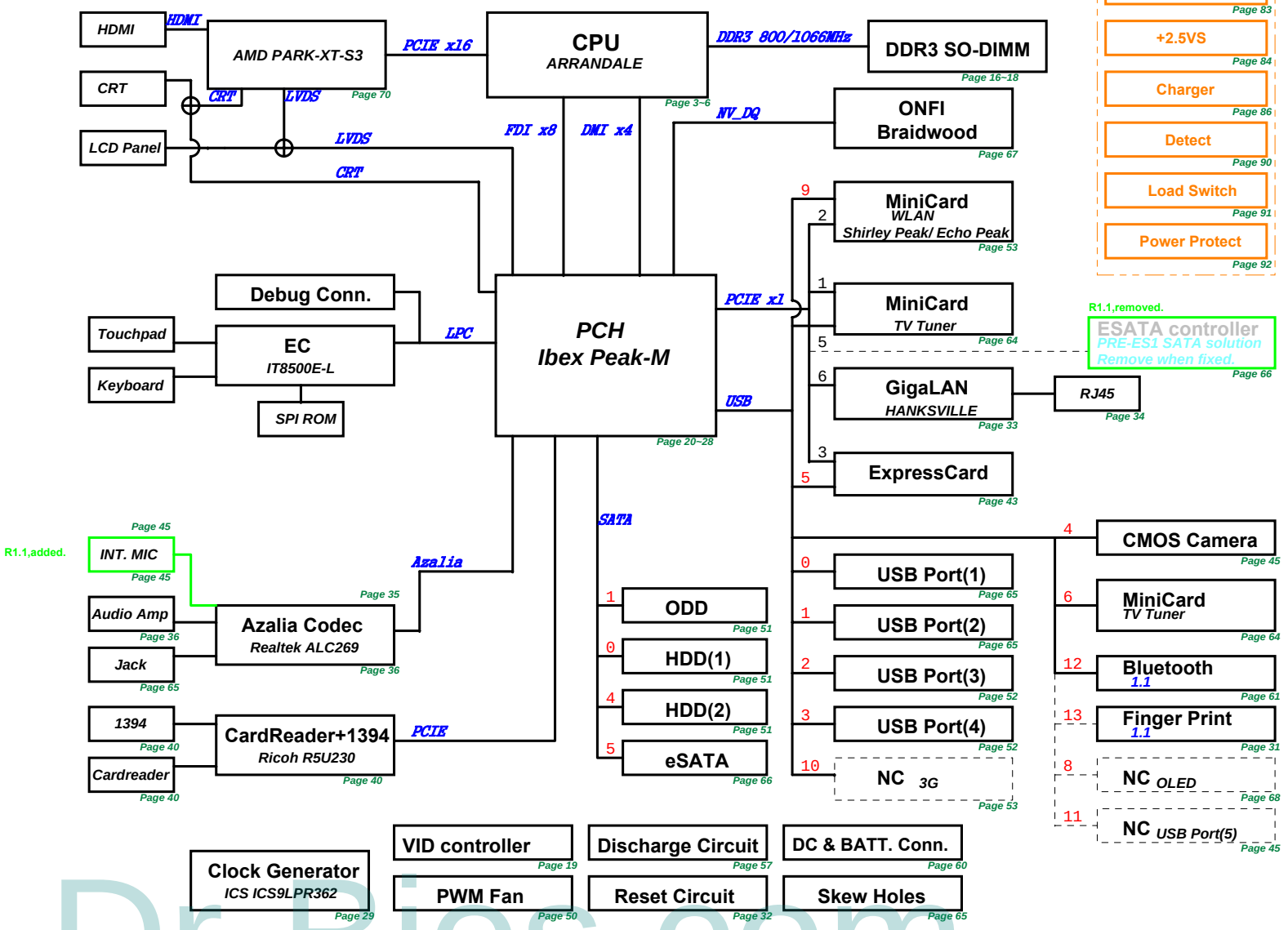
K42F SCHEMATIC For BOM Rev1.0

BLOCK DIAGRAM



ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: Modim Zhang

Size	Project Name	Rev
C	K42F	1.0

Date: Tuesday, November 10, 2009 Sheet 1 of 59

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAYPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	-	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	-	-	+3VS
GPIO 49	GPO	GPU_RST#	-	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	-	-	+5VS
GPIO 53	GPO	-	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	GPO	-	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	-	-	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC IT8512

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		-
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	SUSC_EC#
GPB1	O	SUSB_EC#
GPB2		-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RC_IN#
GPB7	O	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5		OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0		-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPF0		-
GPF1		-
GPF2	I	EXP_GATE#
GPF3		-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7		-
GPG0		-
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1		-
GPH2	O	GFX_VR_ON
GPH3	O	BAT_LEARN
GPH4		-
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6		-
GPI7		-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	TP_LED
GPJ5		-

EC IT8301

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2		-
GPIO3		-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12	O	ME_PWROK
GPIO13		-
GPIO14	O	ME_SLP_M_EC#
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
Clock Generator(ICS9LPR362)	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
VID Controller(ASM8272)	0011011x (36)
WiFi/WiMax	N/A
EC Master (SMB1)	
SM-Bus Device	**SM-Bus Address**
CPU Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	ESATA (for pre-ES1)
PCIE 6	GLAN
PCIE 7	
PCIE 8	

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	NewCard
USB 6	Minicard TV Tuner
USB 7	
USB 8	
USB 9	WLAN
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

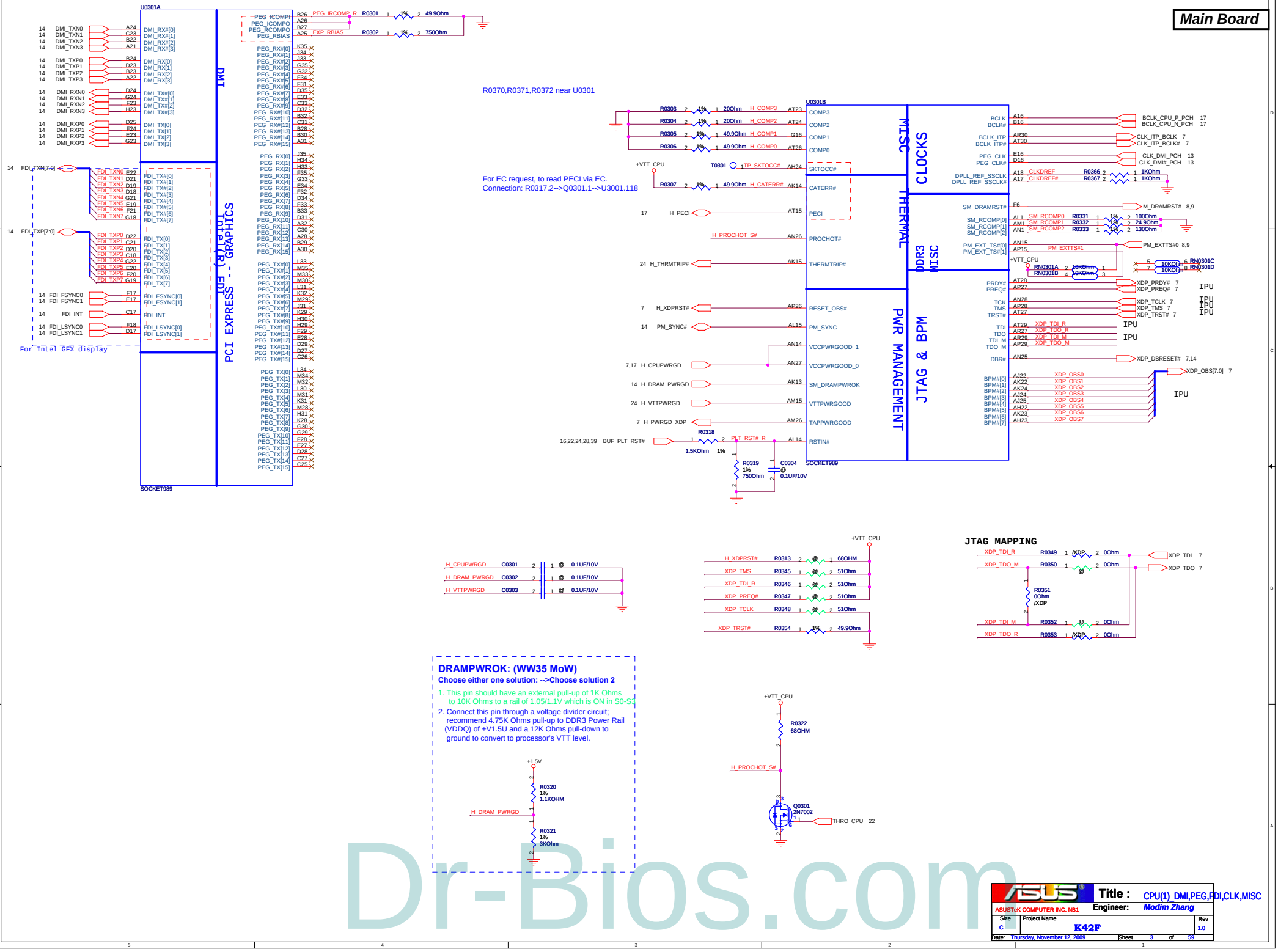
ASUSTeK COMPUTER INC. NB4

Title : System Setting

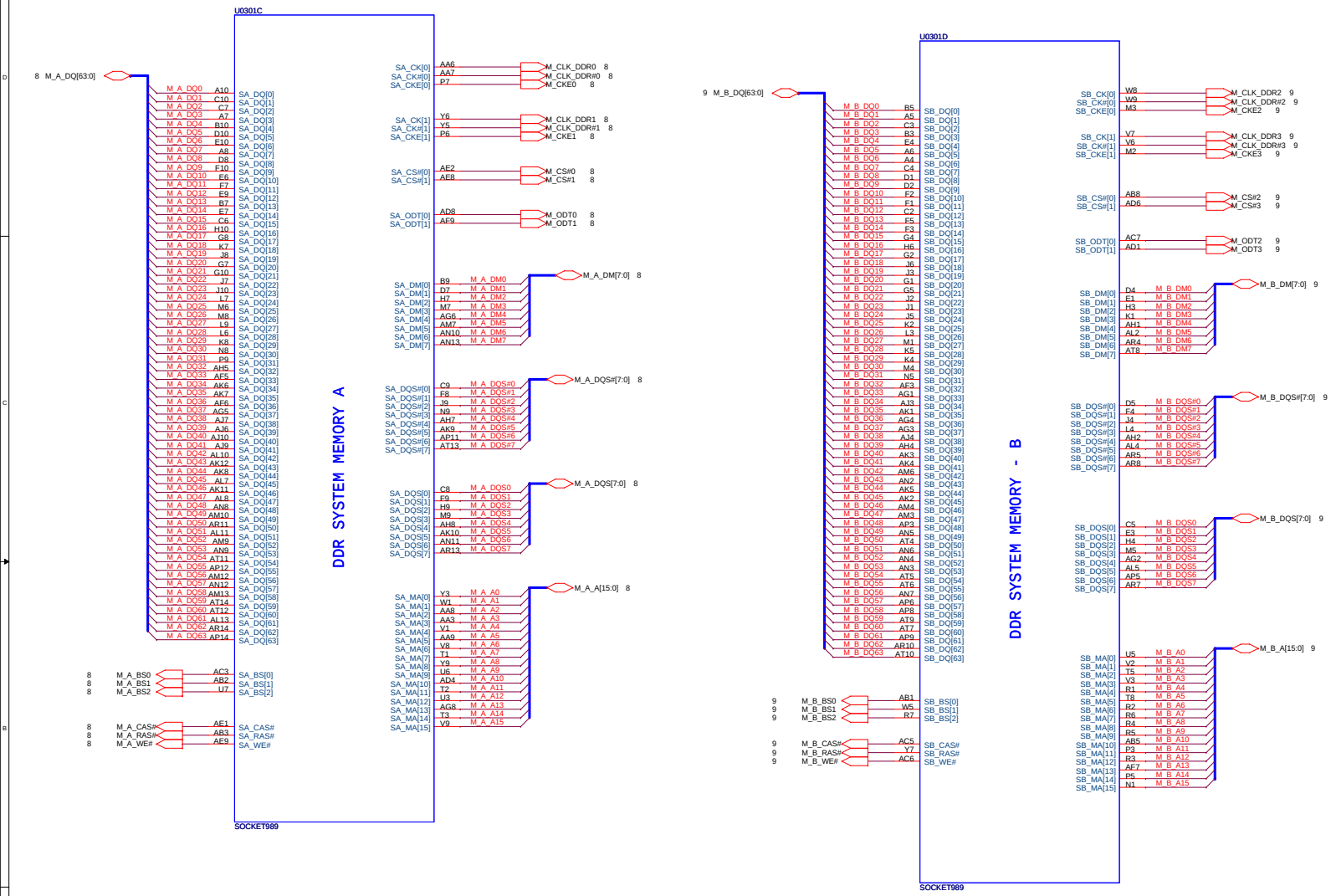
Engineer: Modim Zhang

Size	Project Name	Rev
C	K42F	1.0

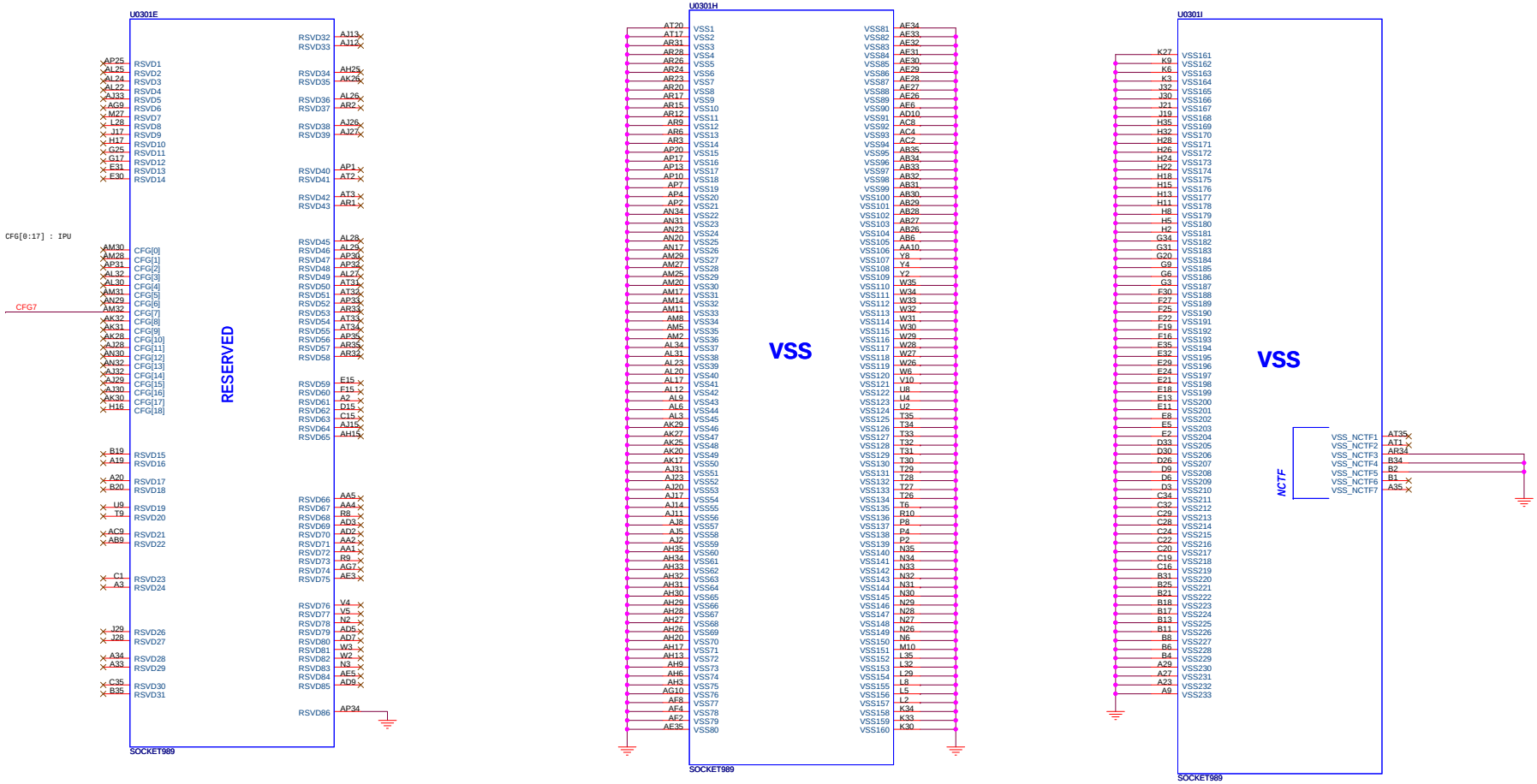
Date: Tuesday, November 10, 2009 Sheet 2 of 59



ASUSTeK COMPUTER INC. NB1	Title :	CPU(1) DMI,PEG,FDI,CLK,MISC
	Engineer:	Modim Zhang
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 3 of 59	



ASUSTeK COMPUTER INC. NB1	Title : CPU(2)_DDR3	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 4 of 59	



CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

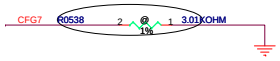
CFG[3]: PCIE Static Numbering Lane Reversal.(Arrandale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.
CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
- 1: No lane reversal
- 0: Reversal

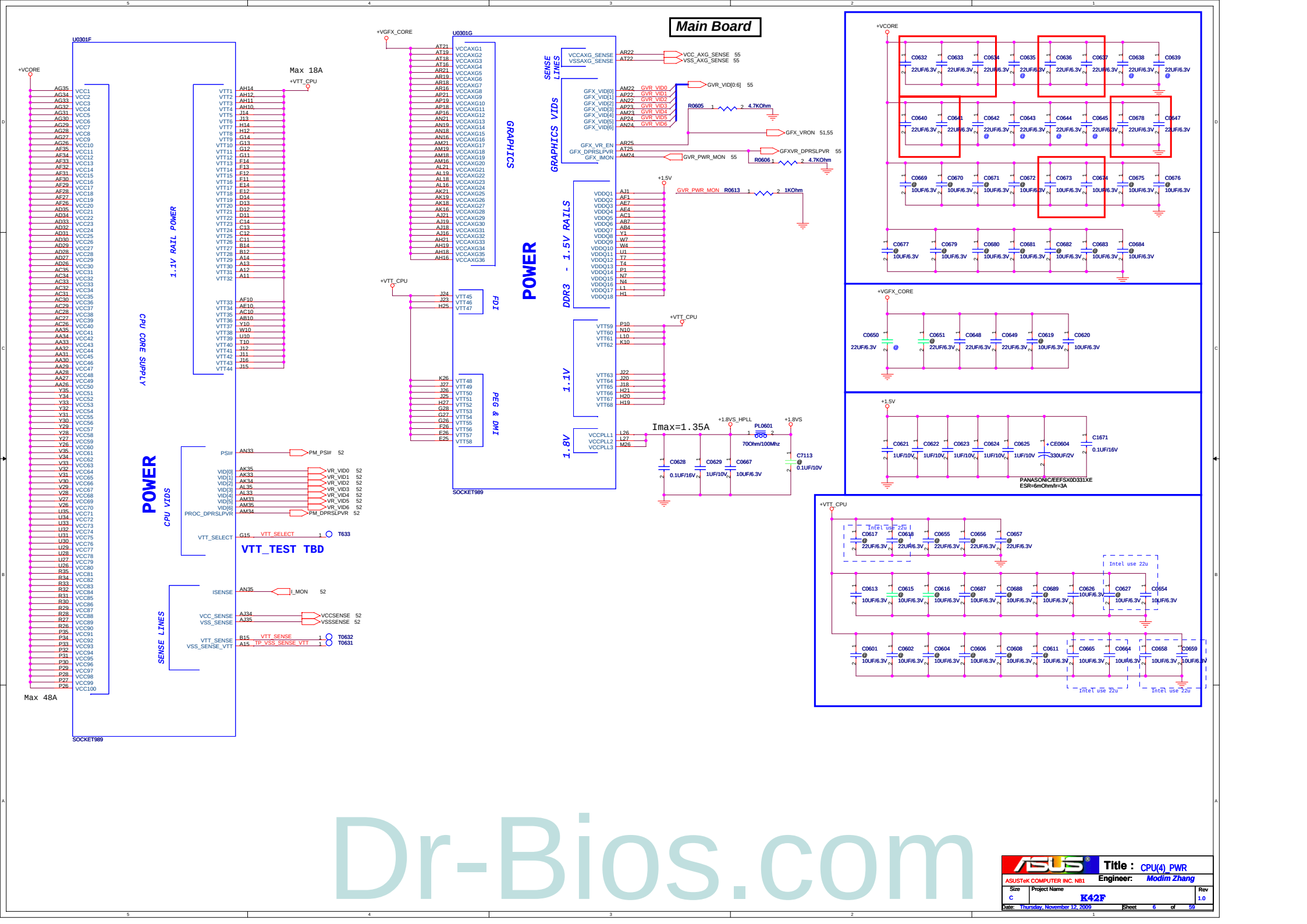
CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.
CFG[17:5] - Reserved configuration pins.
Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

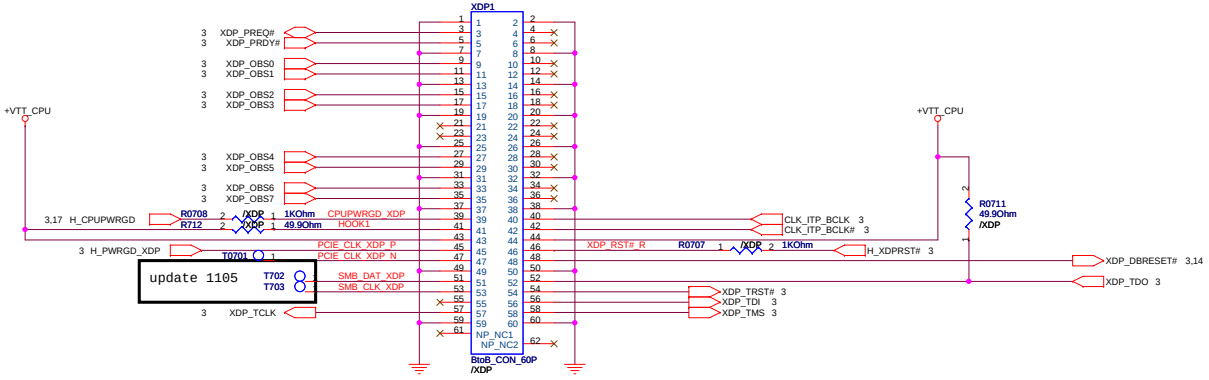
CFG[1:0] - PCI Express* Port Bifucation:
- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.
CFG[3] – Reserved (Used by Arrandale Pporcessors for PCI Express* Static Lane Numbering Reversal)
CFG[11:4] - Reserved configuration pins.
CFG[12] - N/A on Clarksfield processors.
CFG[17:13] - Reserved configuration pins.
Note: Hardware straps are sampled after RSTIN# de-assertion.

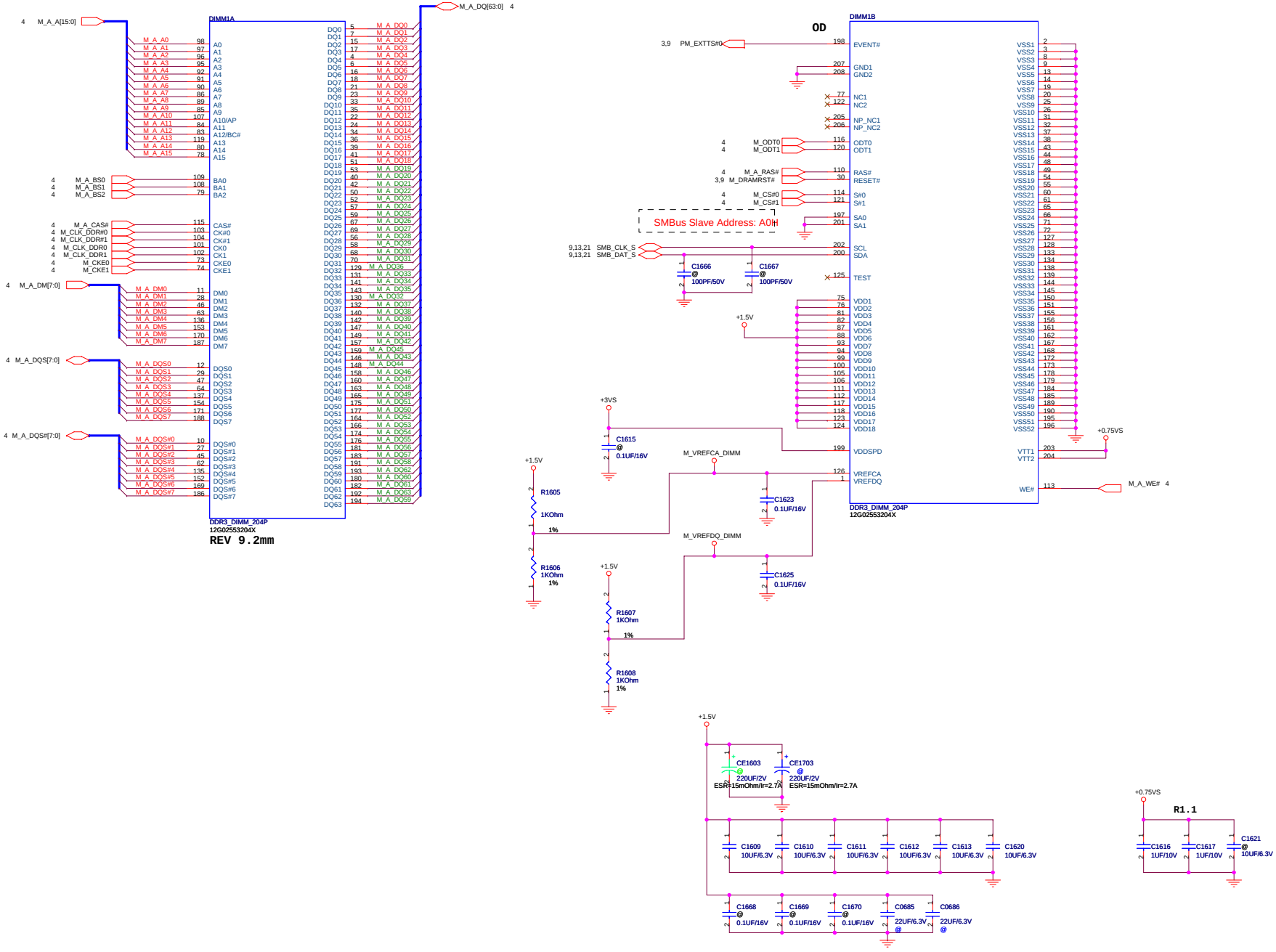
ASUSTeK COMPUTER INC. NB1	Title : CPU(3)_CFG,RSVD,GND	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 5 of 59	


Main Board
U0301F
U0301G
SOCKET989
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
GRAPHICS
GRAPHICS VIDS
SENSE LINES
DDR3 - 1.5V RAILS
1.1V
1.8V
FDI
PEG & DMI
VTT_TEST TBD
Max 18A
Max 48A
Imax=1.35A
PANASONIC/EEFSX0D331XE
ESR=6mOhm/Ir=3A
Intel use 22u
Dr-Bios.com
ASUSTeK COMPUTER INC. NB1
Title : CPU(4)_PWR
Engineer: Modim Zhang
Project Name K42F
Rev 1.0
Date: Thursday, November 12, 2009
Sheet 6 of 59

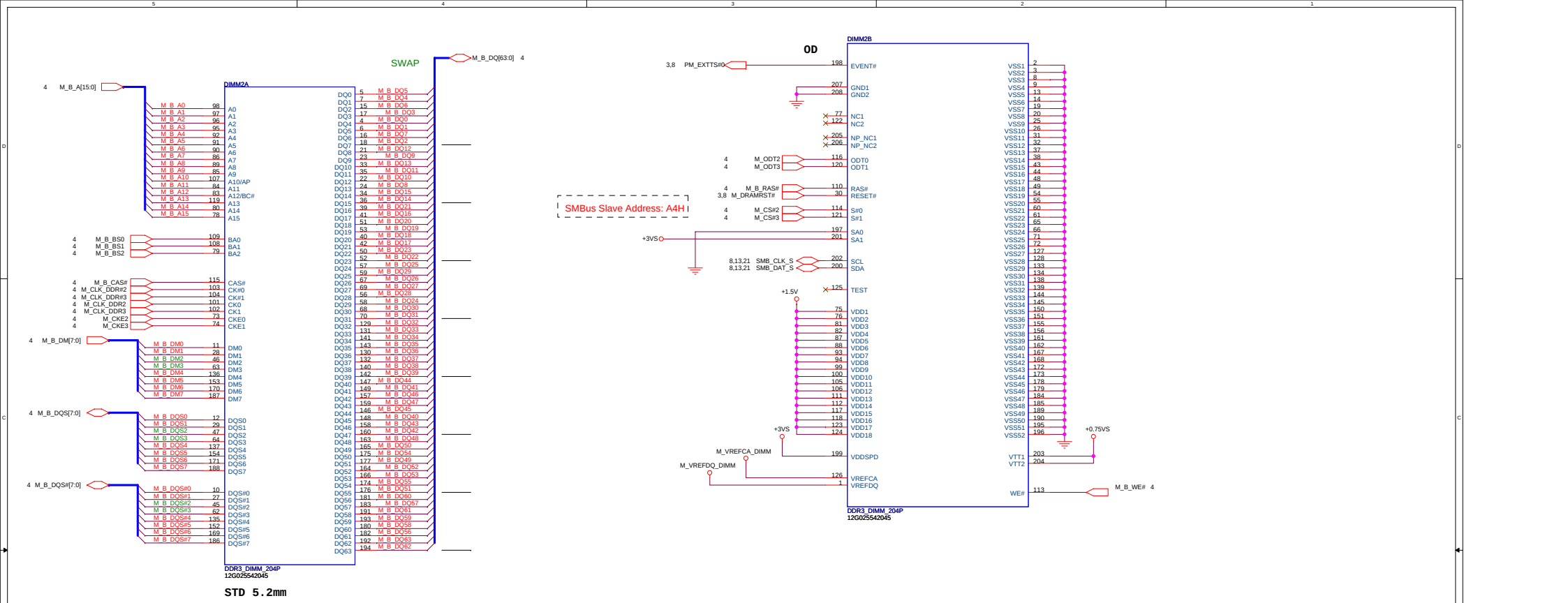
CPU XDP connector



ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 7 of 59	

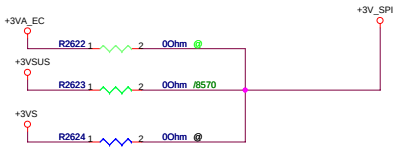


ASUSTeK COMPUTER INC. NB6	Title	DDR3 SO-DIMM_0	
	Engineer:	Modim Zhang	
Size: C	Project Name: K42F		Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 8 of 59		

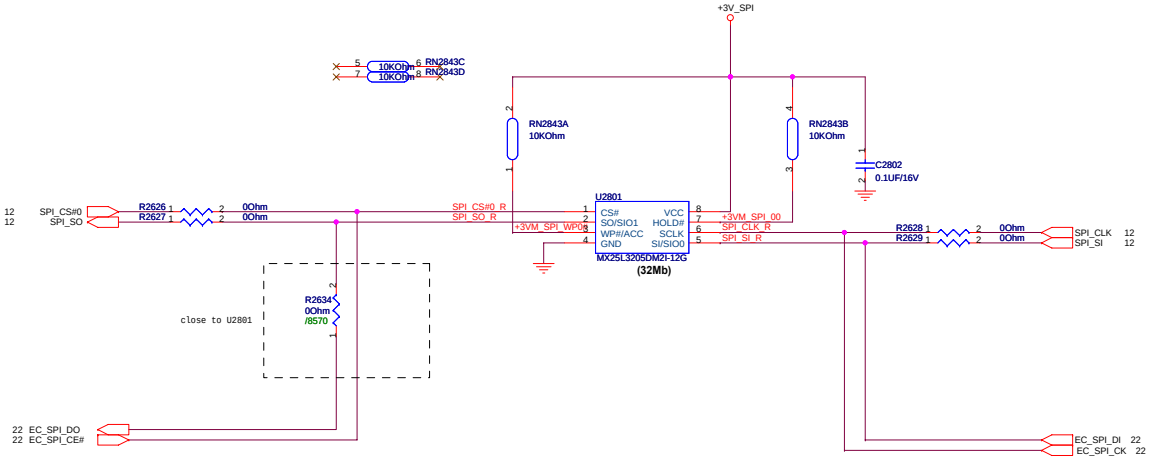


ASUSTeK COMPUTER INC. NB6	Title: DDR3 SO-DIMM_1	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 9 of 59	

PCH SPI ROM



PCH SPI ROM



ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 10 of 59	

Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. **NOTE:** This signal should not be pulled low.
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts.If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDATA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDATA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high

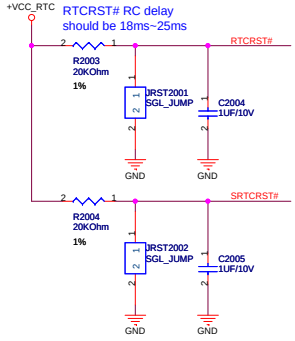
Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN#/GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. **NOTE:** Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. **NOTE:** This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. **NOTE:** A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

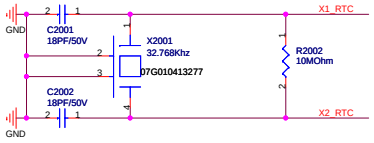
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

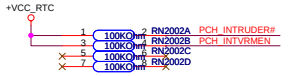


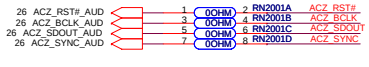
DG2.0 P297
RTCRST# and SRTCRST# can not be shorted together

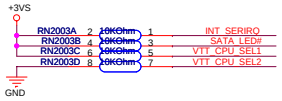
Strap information:

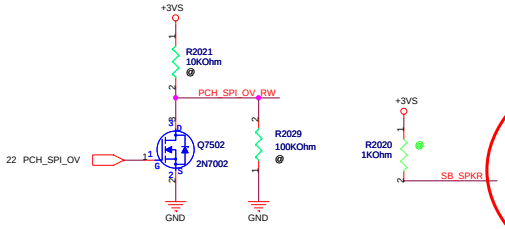
	H	L
ACZ_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_SI: iTPM strap. (IPD)	Enable	Disable
PCH_INTVRMEN Integrated 1.05 V VRM Enable /Disable	Enable	Disable

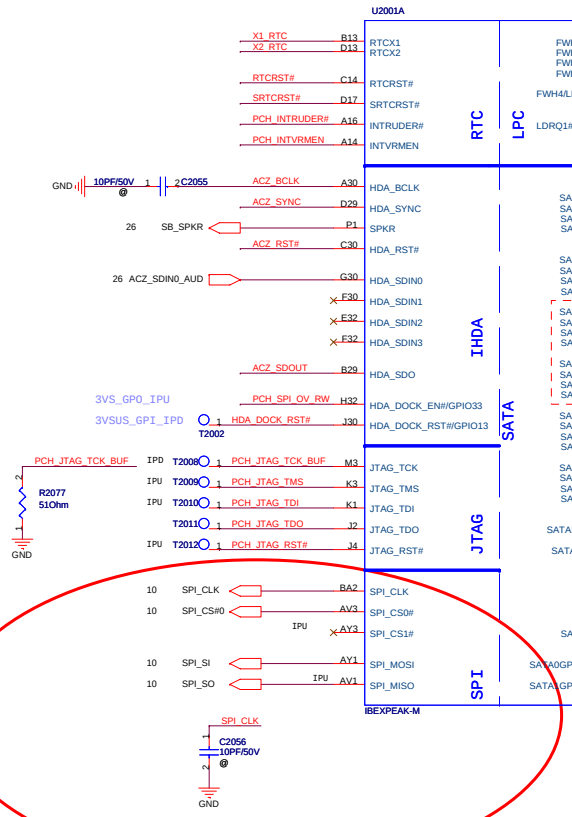








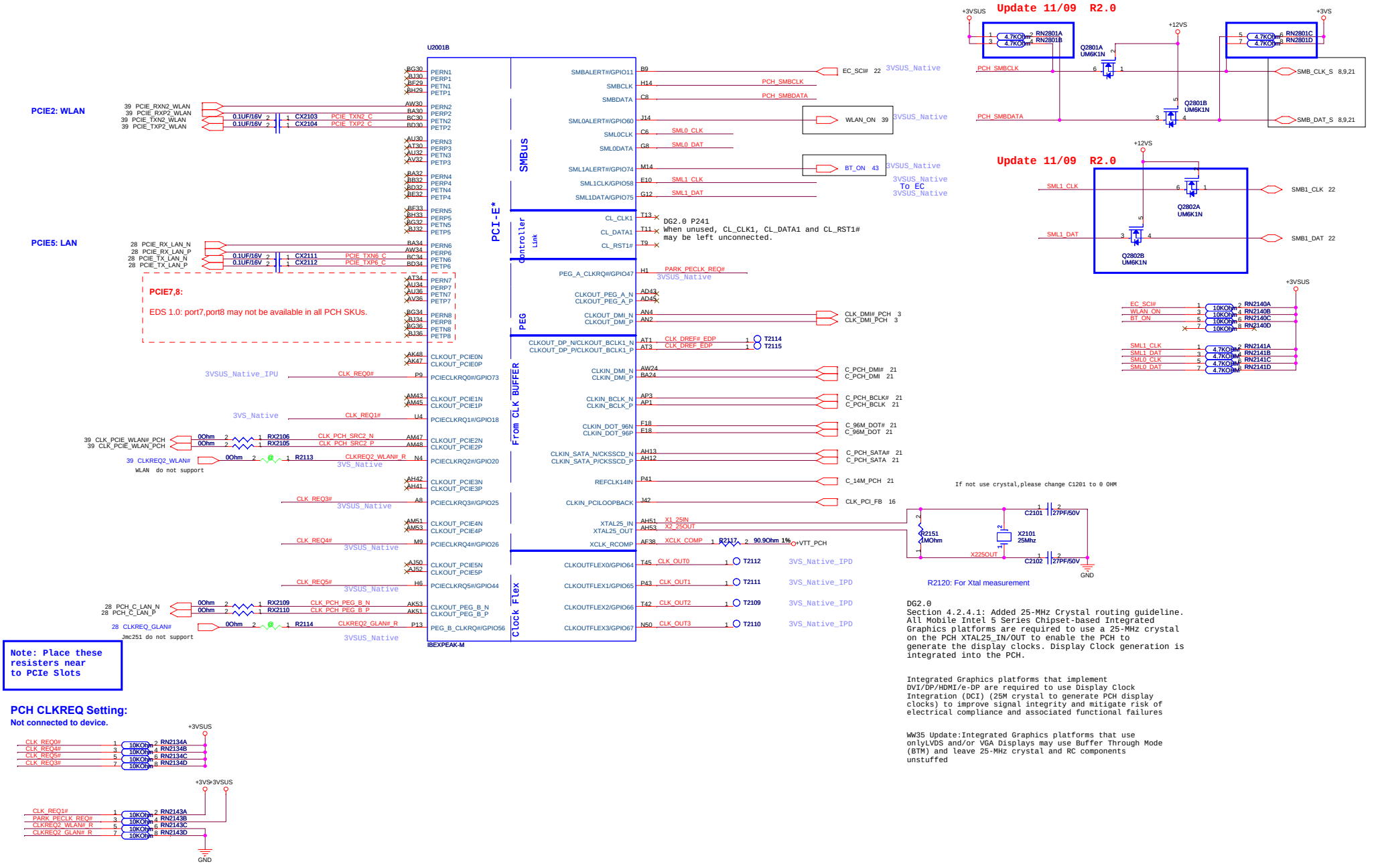




PCH SPI ROM

CUT OFF

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(1)SATA,IHDA,RTC,LPC	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 12 of 59	


Update 11/09 R2.0
U2001B
PCIE2: WLAN
PCIE5: LAN
PCIE7,8:
EDS 1.0: port7,port8 may not be available in all PCH SKUs.
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M
DG2.0 P241
When unused, CL_CLK1, CL_DATA1 and CL_RST1# may be left unconnected.
Update 11/09 R2.0
Note: Place these resisters near to PCIe Slots
PCH CLKREQ Setting:
Not connected to device.
If not use crystal,please change C1201 to 0 OHM
R2120: For Xtal measurement
DG2.0
Section 4.2.4.1: Added 25-MHz Crystal routing guideline. All Mobile Intel 5 Series Chipset-based Integrated Graphics platforms are required to use a 25-MHz crystal on the PCH XTAL25_IN/OUT to enable the PCH to generate the display clocks. Display Clock generation is integrated into the PCH.
Integrated Graphics platforms that implement DVI/DP/HDMI/e-DP are required to use Display Clock Integration (DCI) (25M crystal to generate PCH display clocks) to improve signal integrity and mitigate risk of electrical compliance and associated functional failures
WW35 Update:Integrated Graphics platforms that use onlyLVDS and/or VGA Displays may use Buffer Through Mode (BTM) and leave 25-MHz crystal and RC components unstuffed
Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG
ASUSTeK COMPUTER INC. NB6
Engineer: Modim Zhang
Size C
Project Name K42F
Rev 1.0
Date: Thursday, November 12, 2009
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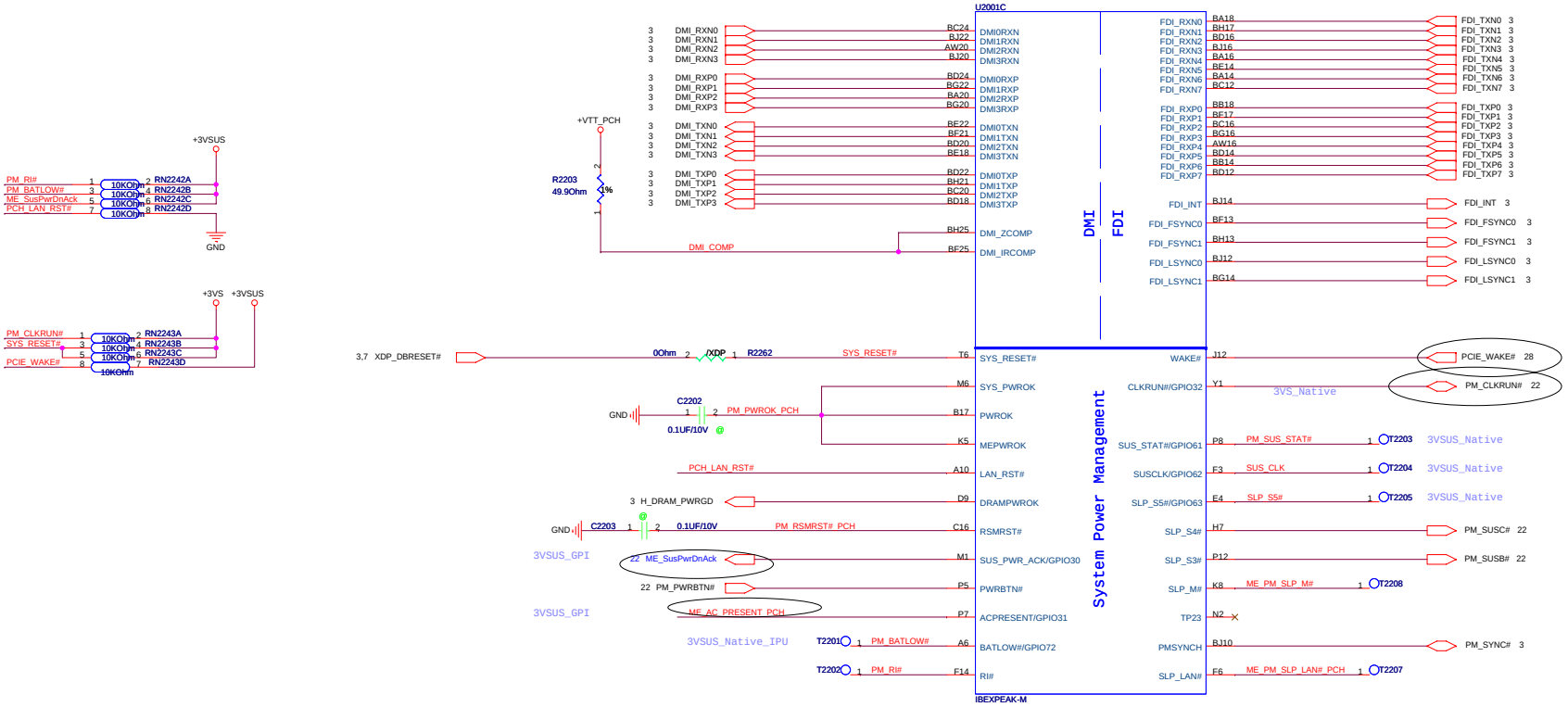
pre-ES1 not support
Reversal Feature



R1.1,item L15

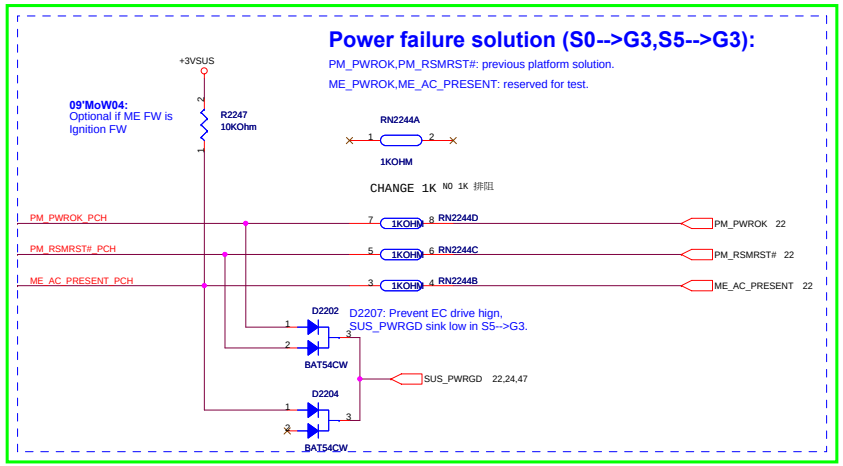


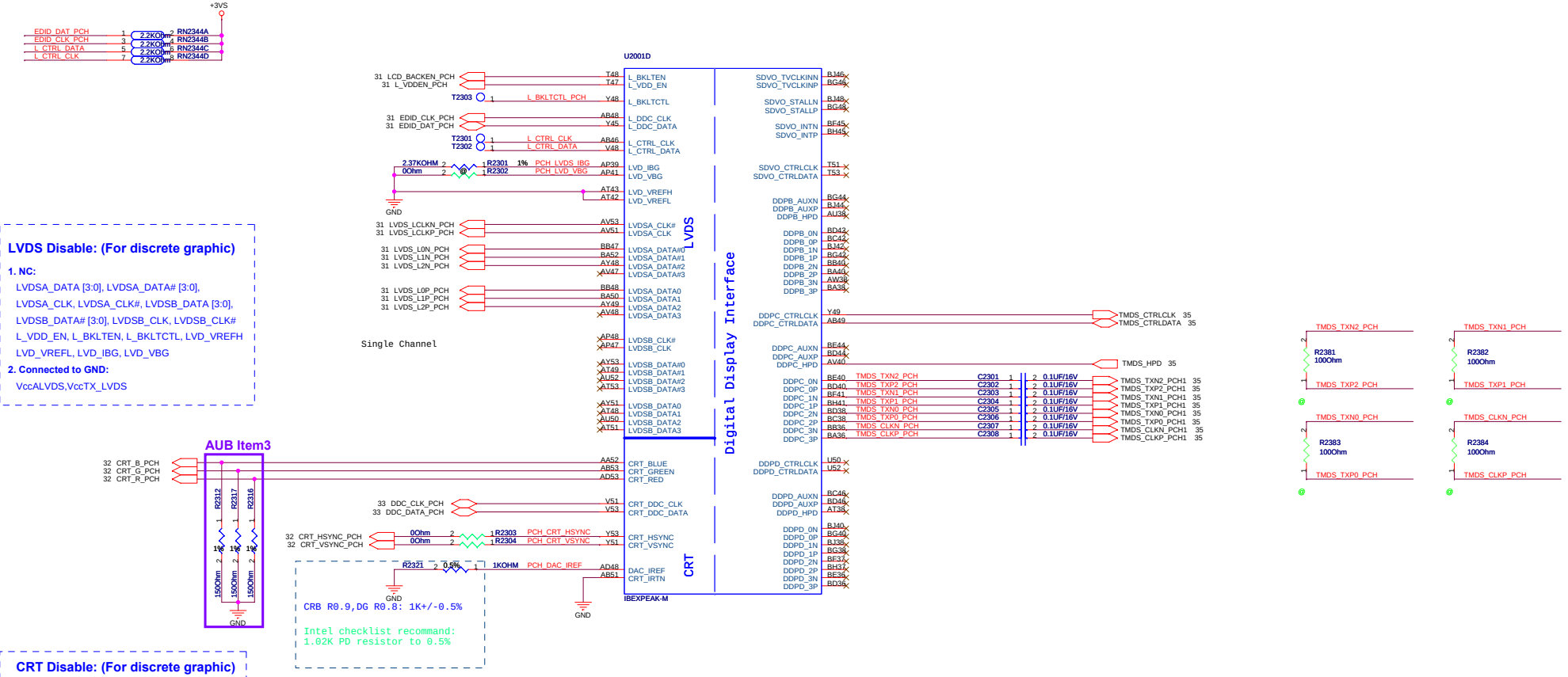
Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required **Note:** Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) **Note:** If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required **Note:** If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(3)_FDI,DMI,SYS PWR	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 14 of 59	



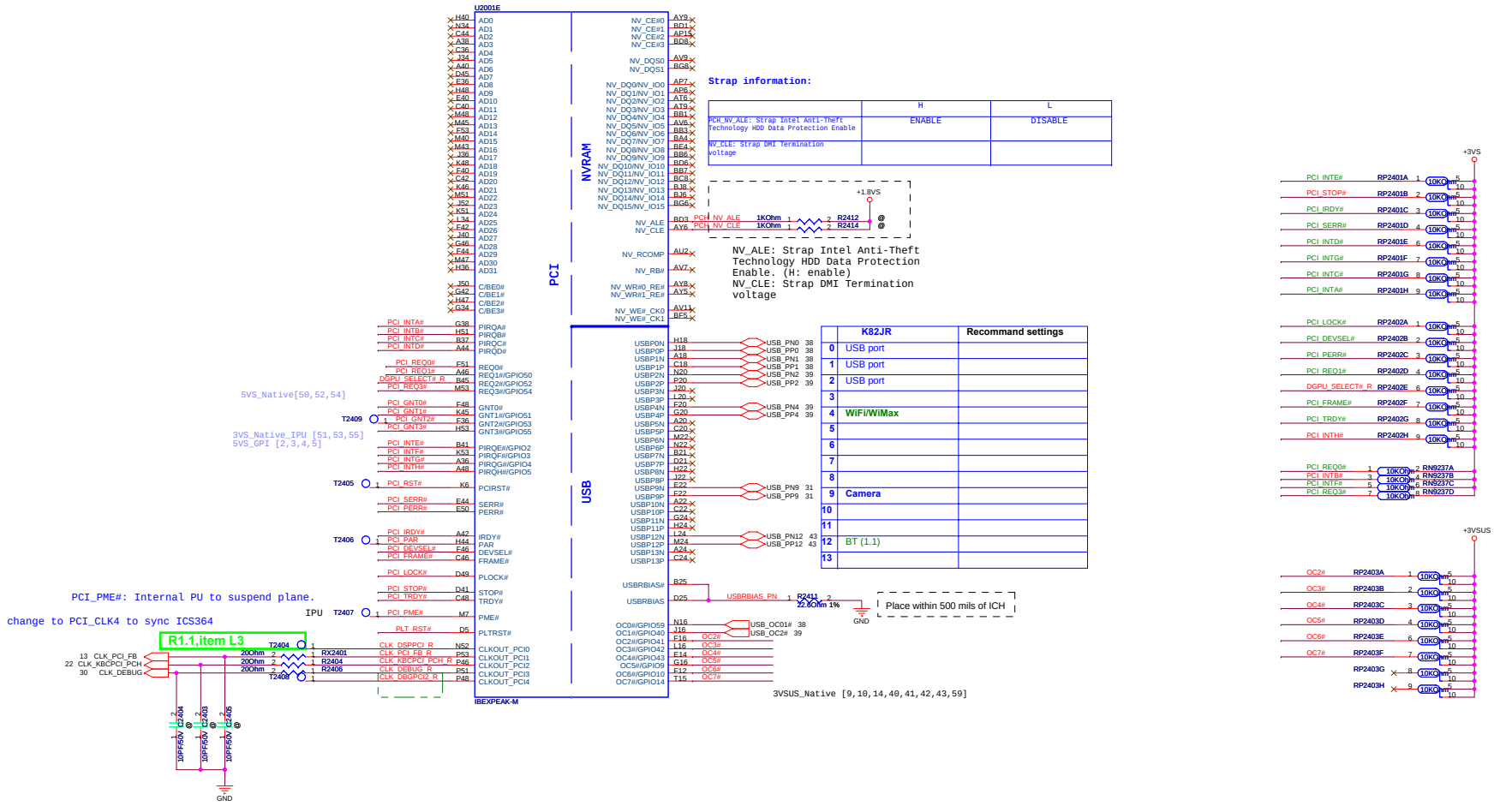
LVDS Disable: (For discrete graphic)

1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(4)_DP,LVDS,CRT	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 15 of 59	



GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap

PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

ASUSTeK COMPUTER INC. NB6

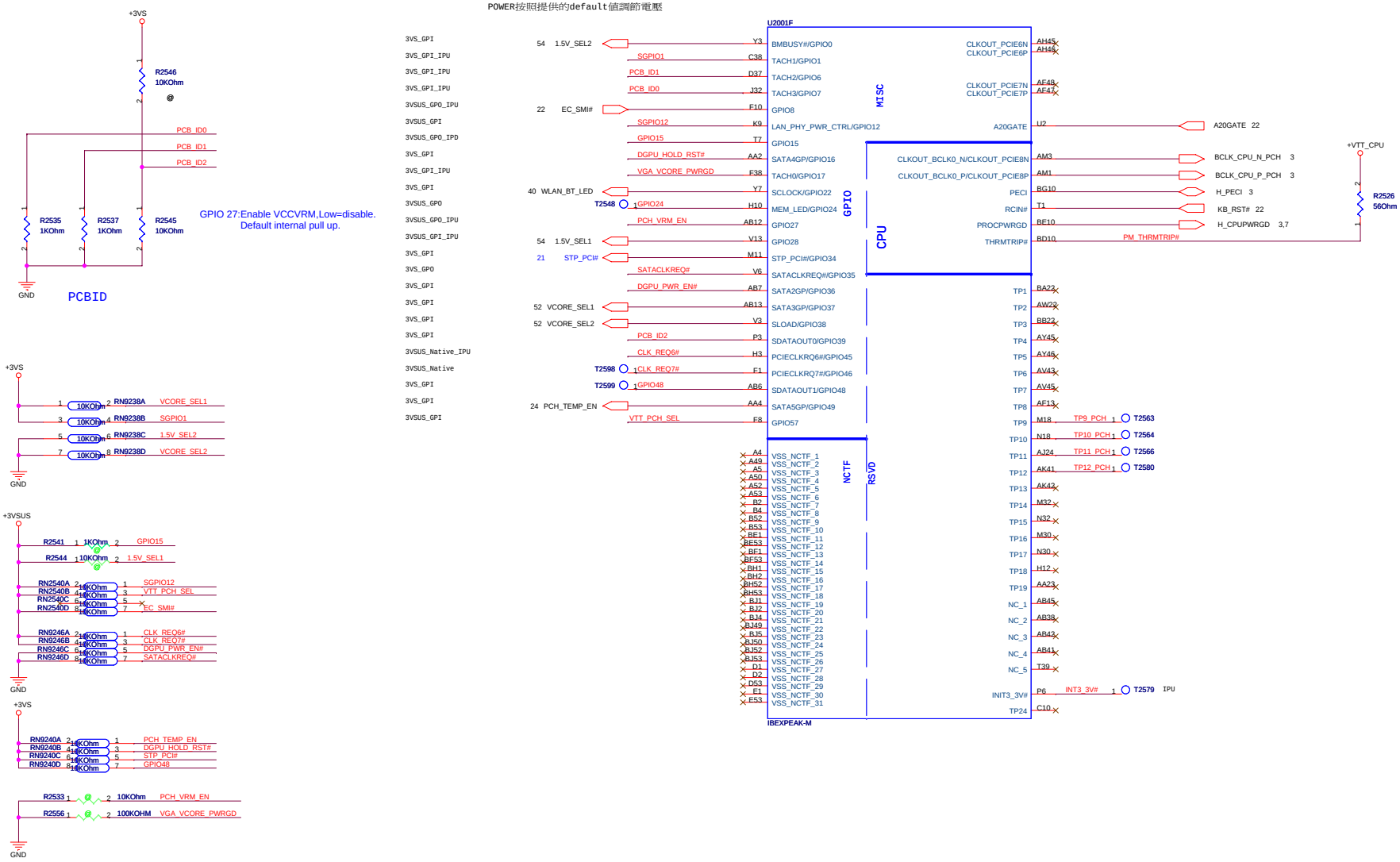
Title : PCH_IBEX(5)_PCI,NVRAM,USB

Engineer: Modim Zhang

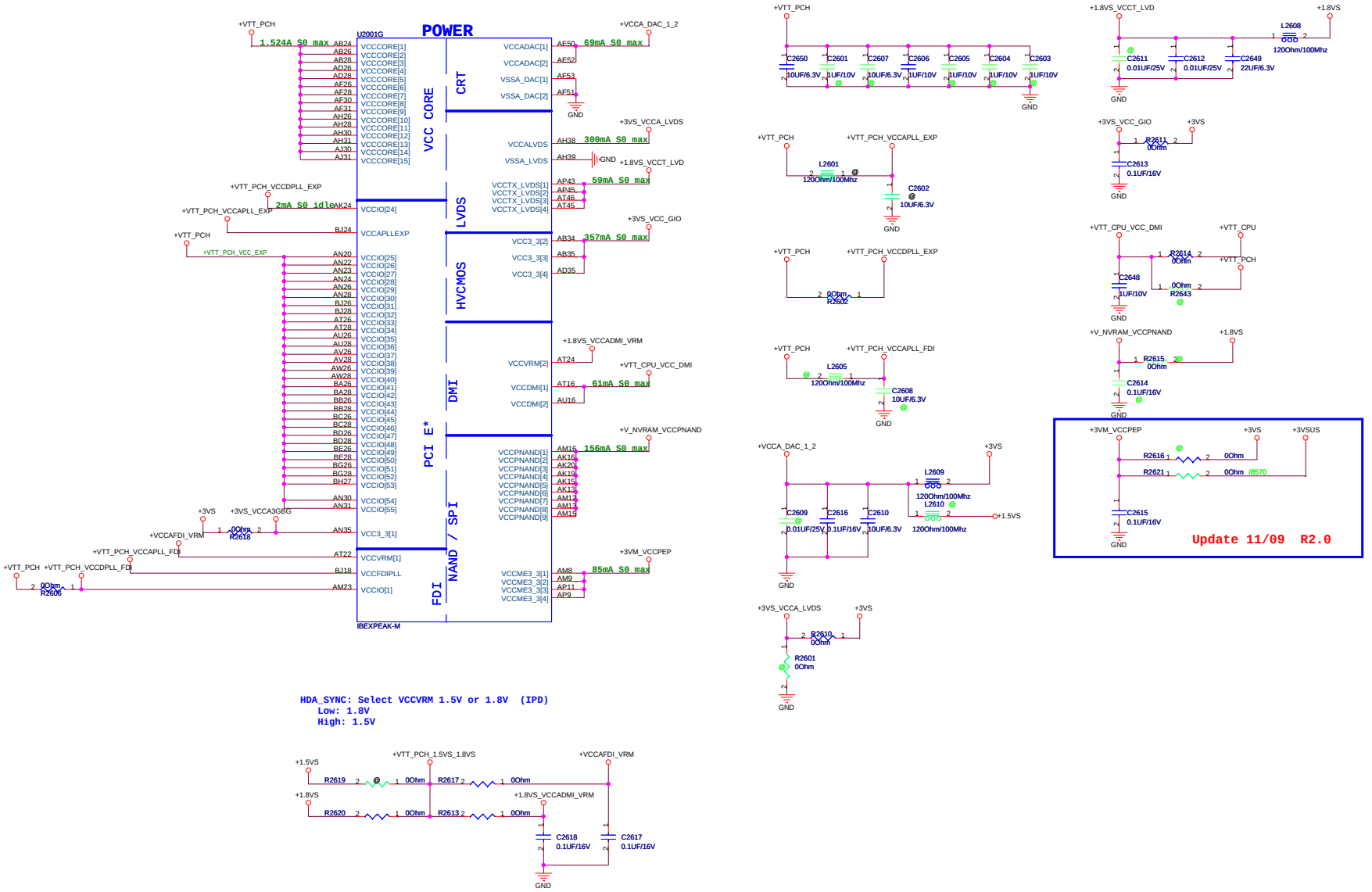
Size: A2 | Project Name: K42F | Rev: 1.0

Date: Thursday, November 12, 2009 | Sheet 16 of 59

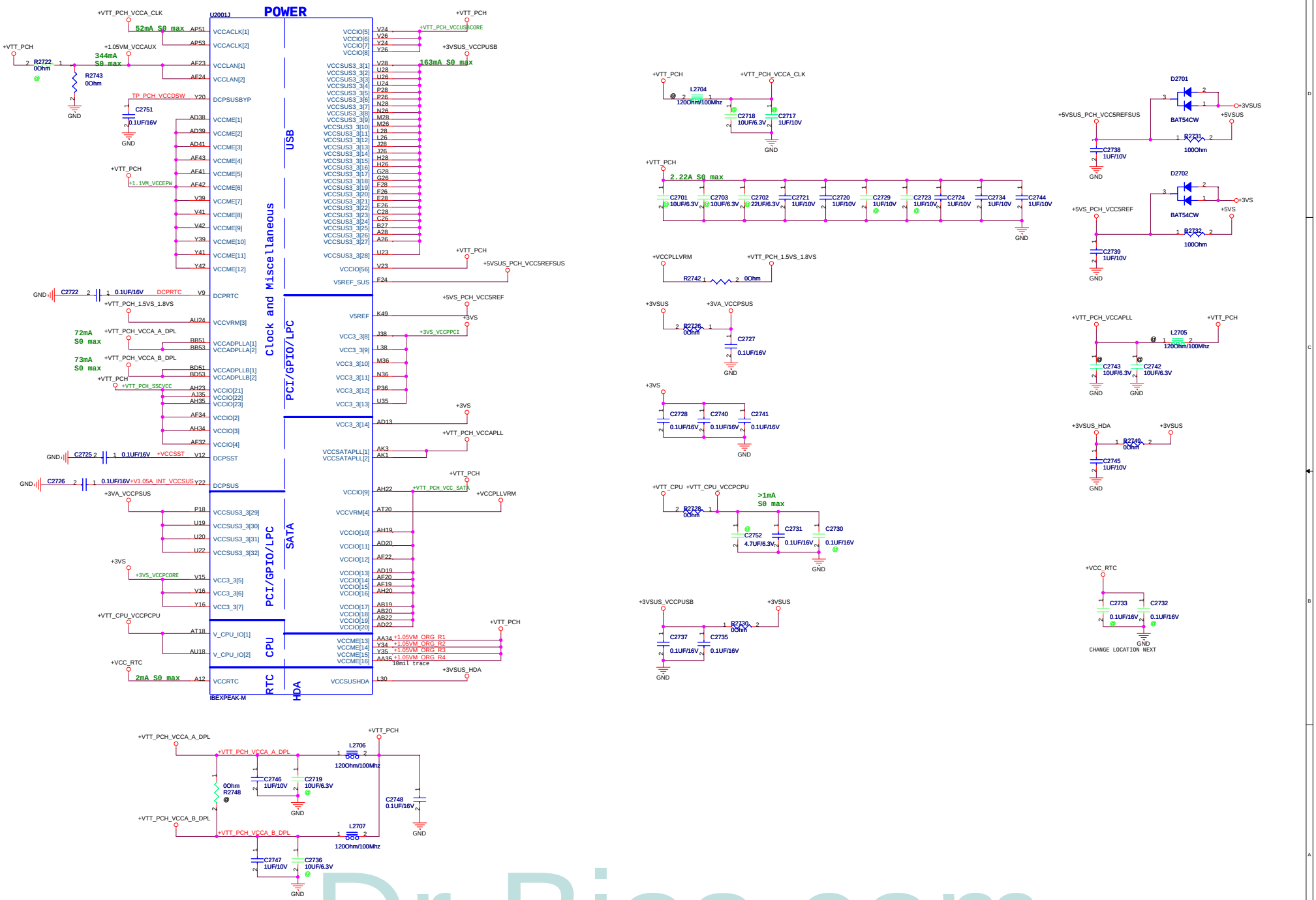
POWER按照提供的default值調節電壓



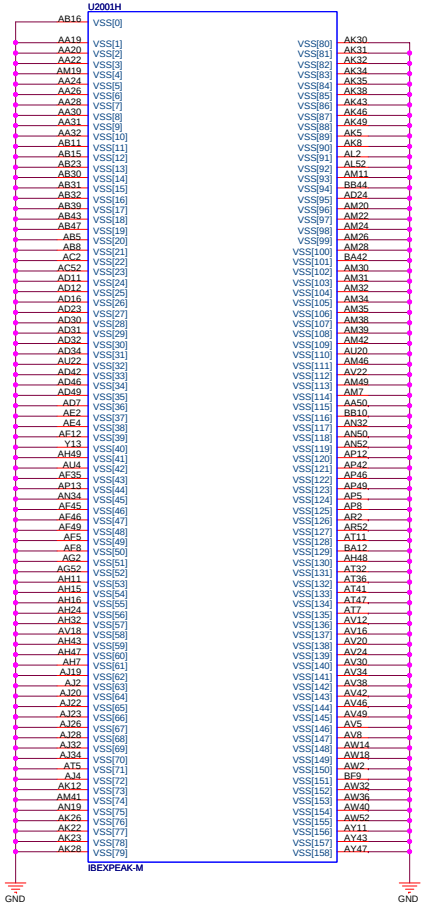
ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(6)CPU,GPIO,MISC	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 17 of 59	

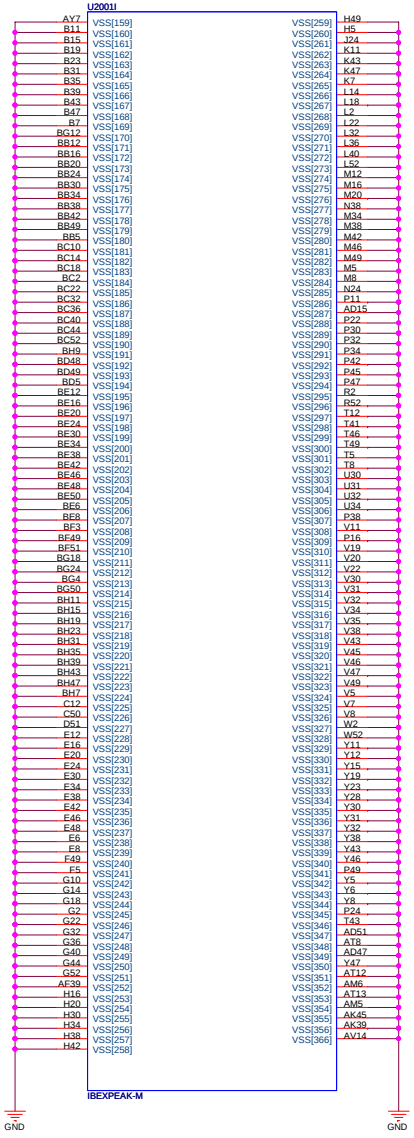


ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(7)_POWER,GND	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 18 of 59	



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(8)_POWER,GND	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 19 of 59	





ASUSTeK COMPUTER INC. NB6

Title : PCH GND

Engineer: Modim Zhang

Size	Project Name	Rev
C	K42F	1.0

Date: Tuesday, November 10, 2009 Sheet 20 of 59

1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

CR1 1MOhm /X
CX1 14.31818Mhz
C_XIN
C_XOUT
CC4 12PF/50V
CC5 12PF/50V
GND

+3VS
CL1 120Ohm/100Mhz
+3V_CLK
CC9 0.1UF/16V @
VDDxx
min:3.135V max: 3.465V
I: 135mV
CC13 10UF/6.3V c0805_h57
CC12 0.1UF/16V
CC14 0.1UF/16V
CC15 0.1UF/16V
CC16 0.1UF/16V
CC17 0.1UF/16V
CC18 0.1UF/16V
CC19 0.1UF/16V
CC20 0.1UF/16V
+3V_CLK_VDDA
CL3 120Ohm/100Mhz
CC22 0.1UF/16V

CU1
ICS9LPRS427CGLFT

1	VDD1	25MHz/FREERUN	56
2	GND1	PCI&PCIEX_STOP#	55
3	PEREQ1#	CPU_STOP#	54
4	PEREQ2#	REF0/FSLC	53
5	FS4/PCICLK0	DOC_PEREQ3#	52
6	GND2	GND4	51
7	VDDPCI	X1	50
8	ITP_EN/PCICLK_F0	X2	49
9	SEL12_48#/12_48MHz	VDDREF	48
10	Vtt_PwrGd/PD#	SDATA	47
11	VDD2	SCLK	46
12	FSLA/USB_48MHz	GND5	45
13	GND3	CPUT_LR0	44
14	DOTT_96MHzLR	CPUC_LR0	43
15	DOTC_96MHzLR	VDDCPU	42
16	FSLB	CPUT_LR1	41
17	PCIeT_LR0	CPUC_LR1	40
18	PCIeC_LR0	RESET#	39
19	PCIeT_LR1	GNDA	38
20	PCIeC_LR1	VDDA	37
21	VDDPCIEX1	CPUITPT_LR2/PCIeT_LR6	36
22	PCIeT_LR2	CPUITPC_LR2/PCIeC_LR6	35
23	PCIeC_LR2	VDDPCIEX3	34
24	PCIeT_LR3	PCIeT_LR5	33
25	PCIeC_LR3	PCIeC_LR5	32
26	SATACLKT_LR	PCIeT_LR4	31
27	SATACLKC_LR	PCIeC_LR4	30
28	VDDPCIEX2	GND6	29

PEREQ1#
C_REQ#_WLAN
FS4
C_PCI_SB_R
C_48M_R
CLK_EN
C_FSLA
C_FSLB
13 C_96M_DOT
13 C_96M_DOT#
13 C_PCH_DMI
13 C_PCH_DMI#
13 C_PCH_SATA
13 C_PCH_SATA#
C_25M_LAN_R 33Ohm CR6 /X → C_25M_LAN 28, STP_PCI# 17
STP_CPU#
C_FSLC 33Ohm CR3 → C_14M_PCH 13
C_REQ#_LAN
C_XIN
C_XOUT
SMB_DAT_S 8,9,13
SMB_CLK_S 8,9,13
C_PCH_BCLK 13
C_PCH_BCLK# 13
C_DXP CT1
C_DXP# CT2

C2933 /EMI/X 10PF/50V
C2934 /EMI/X 10PF/50V

+3VS
CR14 10KOhm
CLK_EN
CR16 100KOhm
CC31 0.1UF/16V /X
52 CLK_EN#
CQ2 2N7002

CR10 10KOhm
CR12 10KOhm @
CR13 10KOhm @
CR15 10KOhm
CR17 10KOhm

STP_CPU# CR19 10KOhm
C_48M_R CR11 10KOhm @

FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133
0	1	0	200

C_REQ#_LAN CRN2A
C_REQ#_WLAN CRN2B
PEREQ1# CRN2C
C_PCI_SB_R CRN2D
10KOhm

FS4 CR23 /X 10KOhm
CR18 10KOhm

<Variant Name>

ASUSTek Computer INC.
Title : ICS9LPRS427C
Engineer: Modim Zhang
Size A3
Project Name K42F
Rev 1.0
Date: Thursday, November 12, 2009
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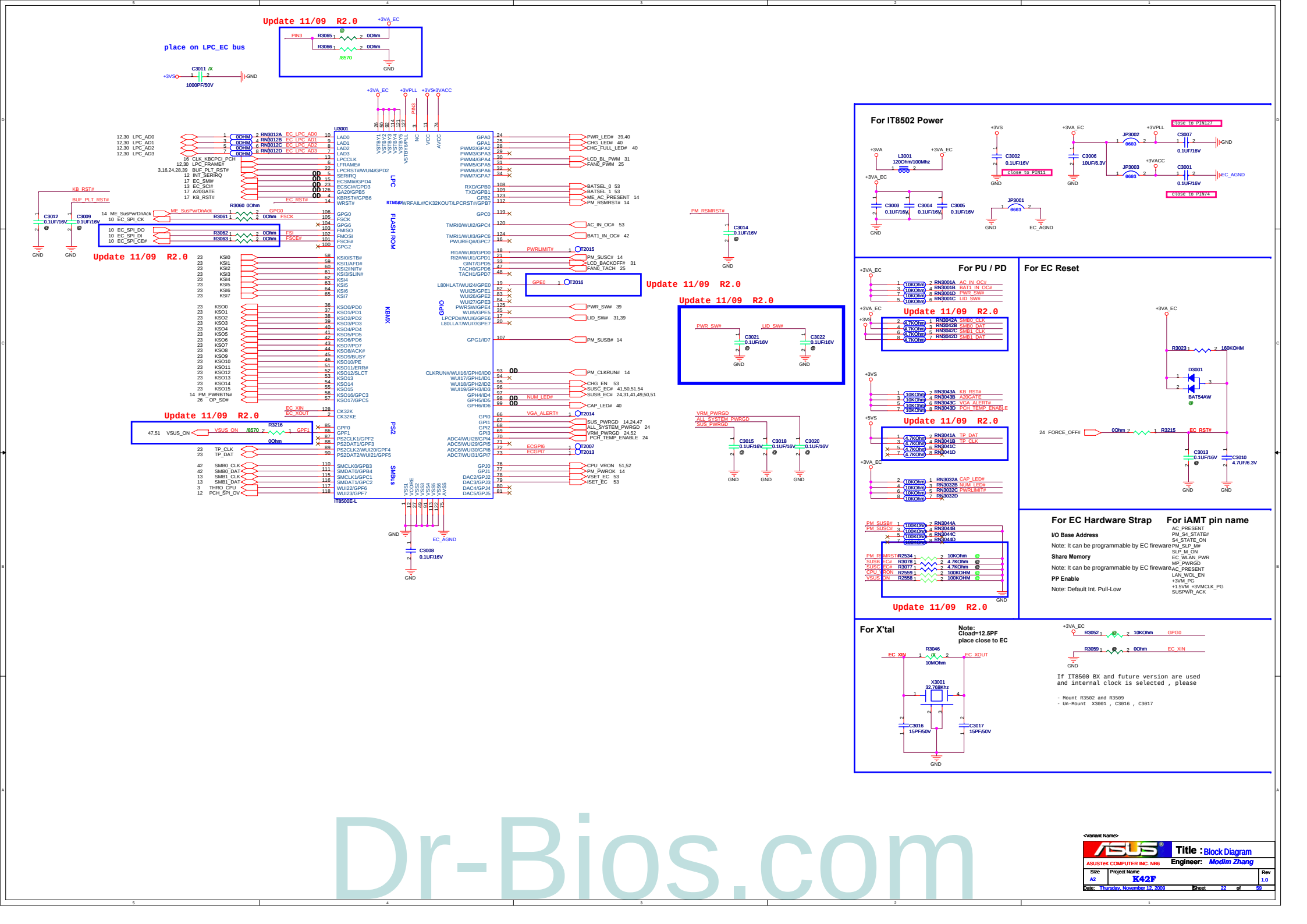
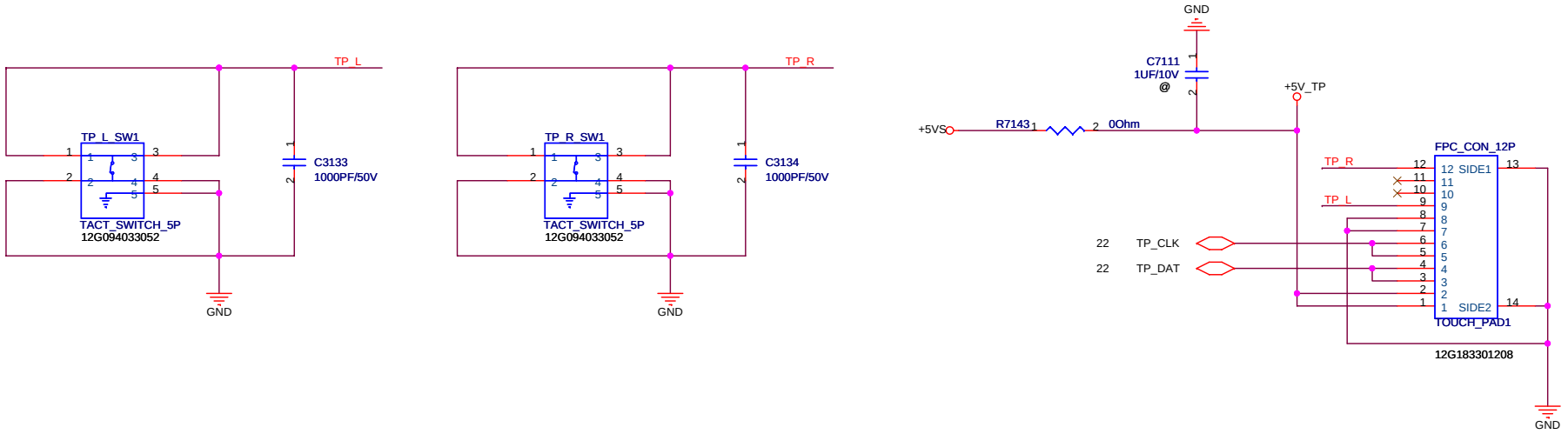
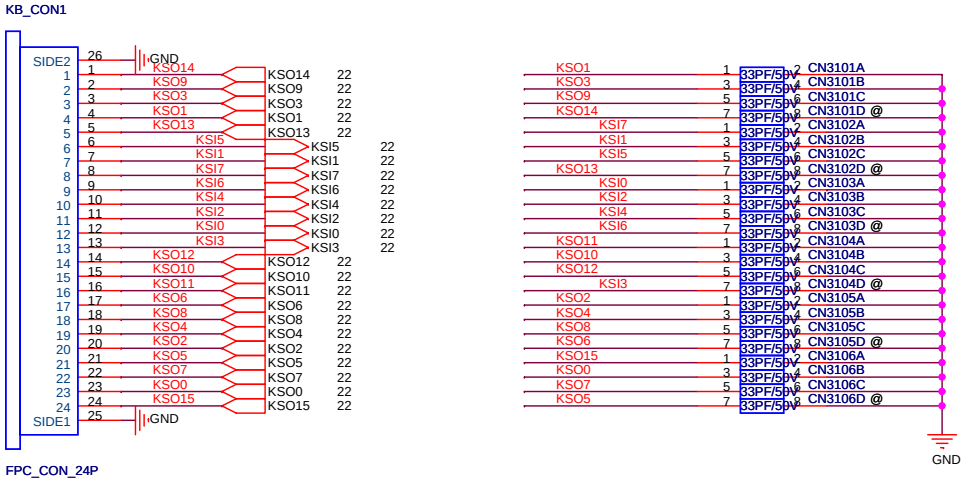

Update 11/09 R2.0
place on LPC_EC bus
U3001
IT8500E-L
LPC
FLASH ROM
KBMX
GPIO
PS2
SMBUS
For IT8502 Power
For PU / PD
For EC Reset
For EC Hardware Strap
I/O Base Address
Share Memory
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
For X'tal
Note:
Cload=12.5PF
place close to EC
If IT8500 RX and future version are used
and internal clock is selected , please
- Mount R3502 and R3509
- Un-Mount X3001 , C3016 , C3017
<Variant Name>
Title : Block Diagram
ASUSTeK COMPUTER INC. NB6
Engineer: Modim Zhang
Size A2
Project Name K42F
Rev 1.0
Date: Thursday, November 12, 2009
Sheet 22 of 59

TouchPad



Keyboard Connector

EMI Request



<Variant Name>

Title : Block Diagram

ASUSTeK COMPUTER INC. NB6

Engineer: Modim Zhang

Size	Project Name	Rev
Custom	K42F	1.0

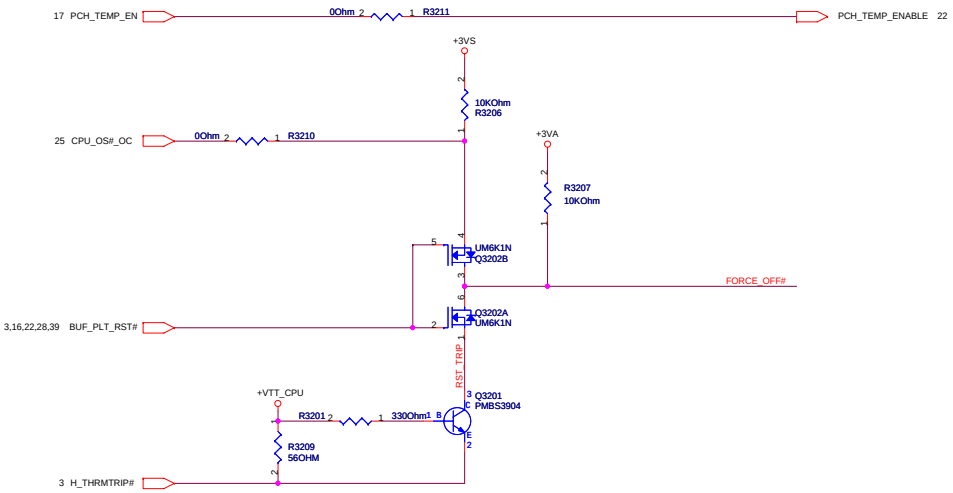
Date: Thursday, November 12, 2009 Sheet 23 of 59

Thermal Policy

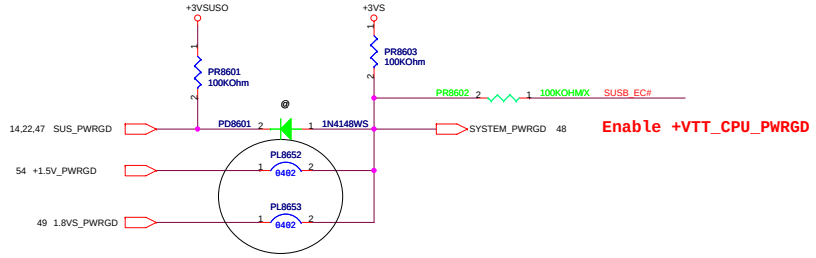
Input 1(sensor)

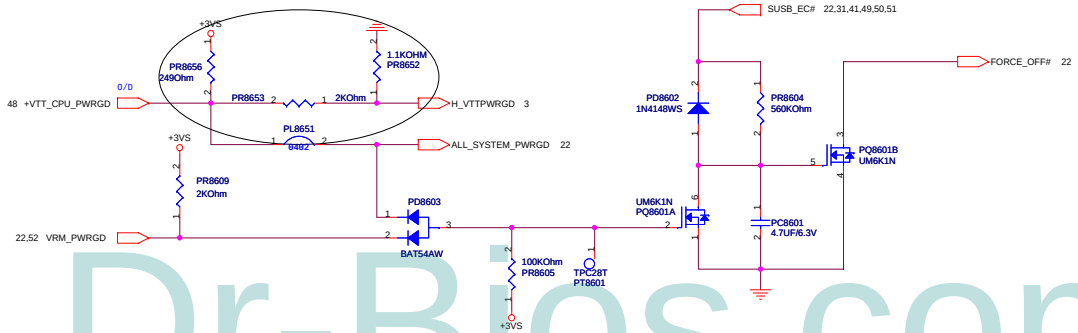
Input 2(thermtrip)

Output (shut down)



POWER GOOD DETECTER

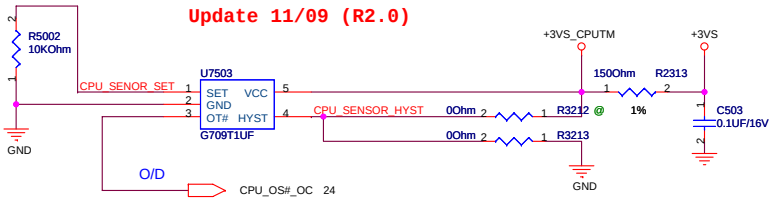




ASUSTeK COMPUTER INC. NB4	Title : Forceoff#_PWRGD_Thermal	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 24 of 59	

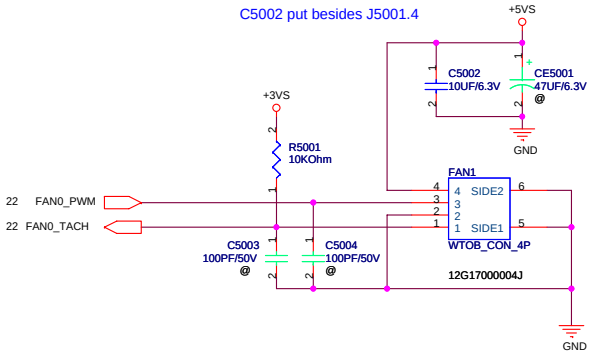
GPU Thermal Sensor

CPU Thermal Sensor



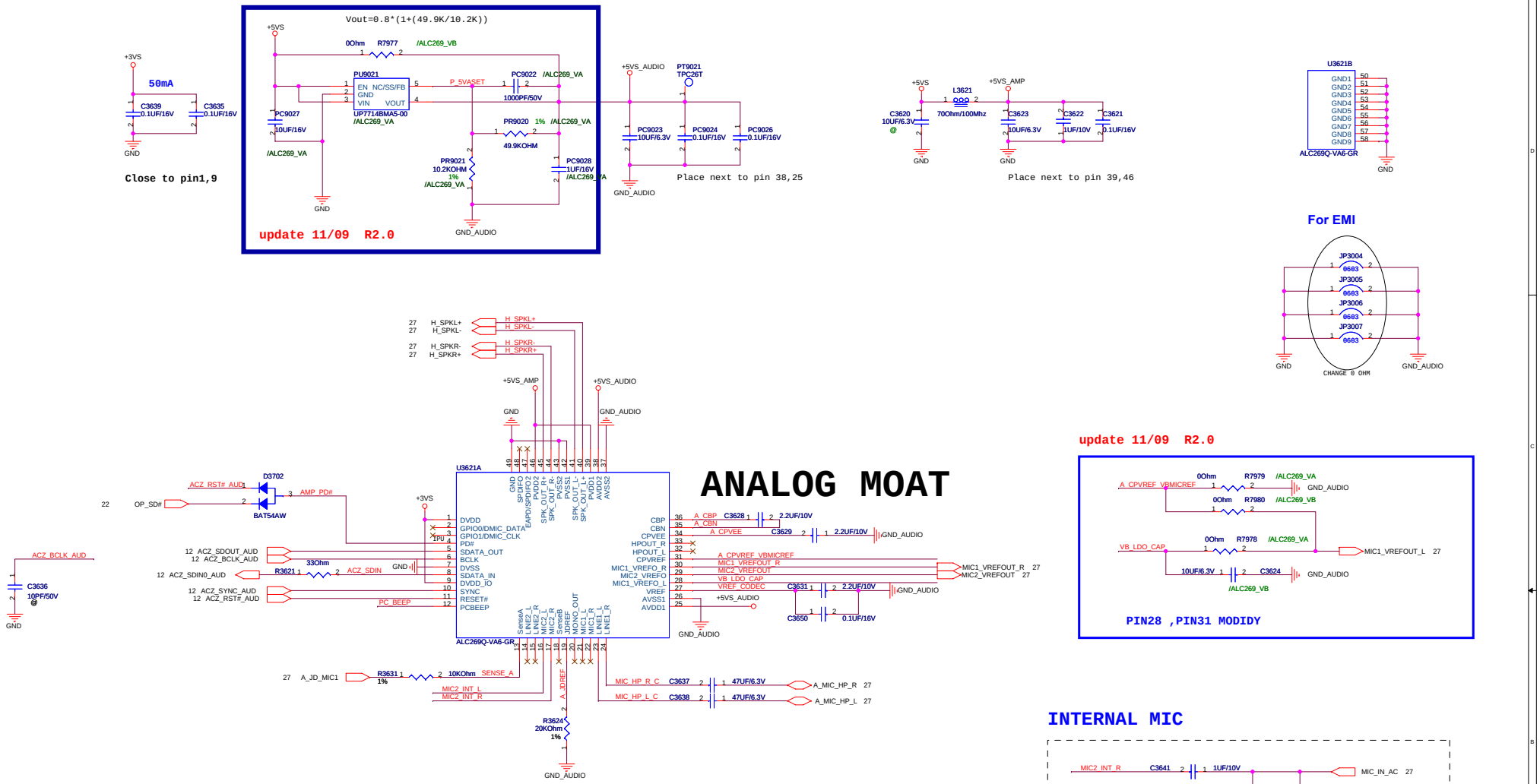
PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.

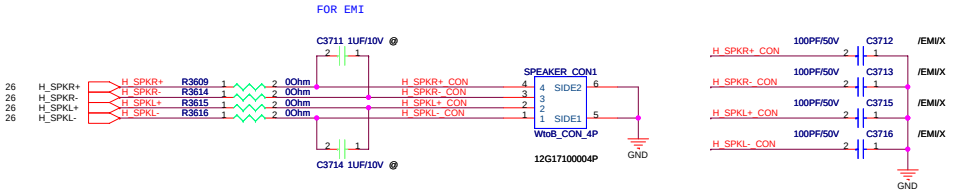


ASUSTeK COMPUTER INC	Title : AR8131	
	Engineer:	
Size: Custom	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 25 of 59	

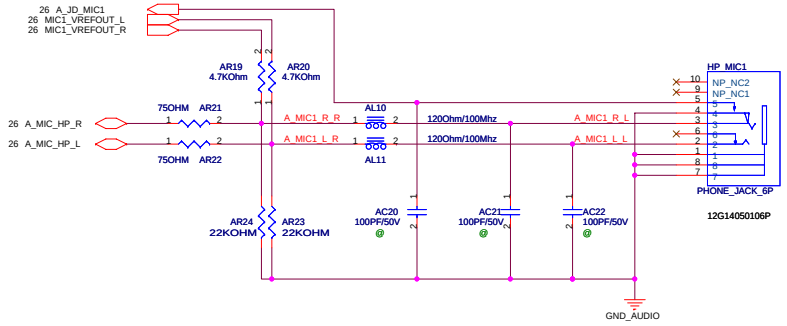
ANALOG MOAT



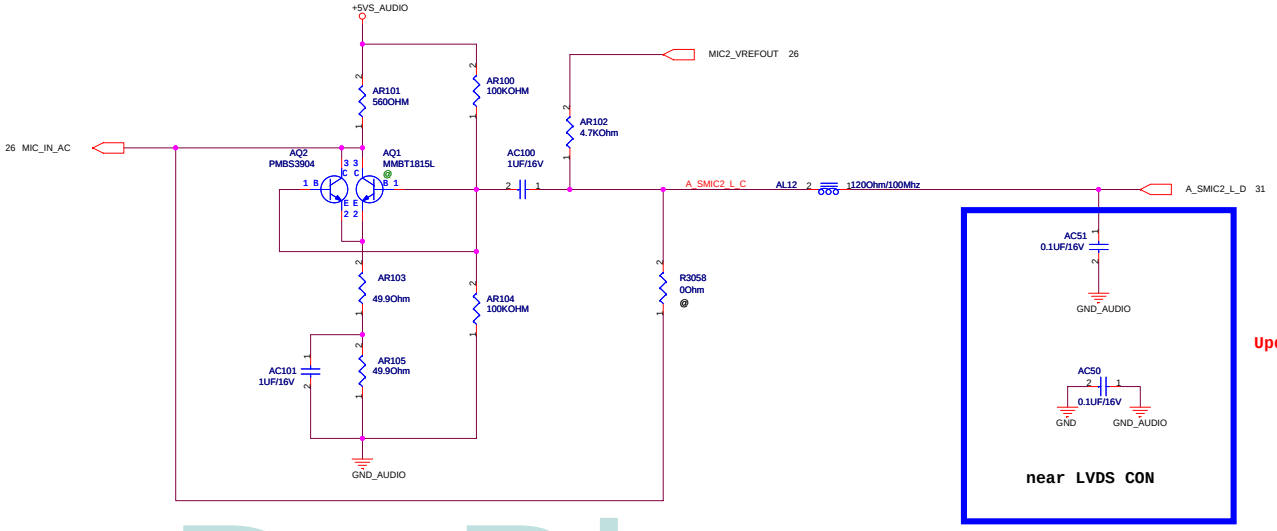
SPEAKER



HP and MIC

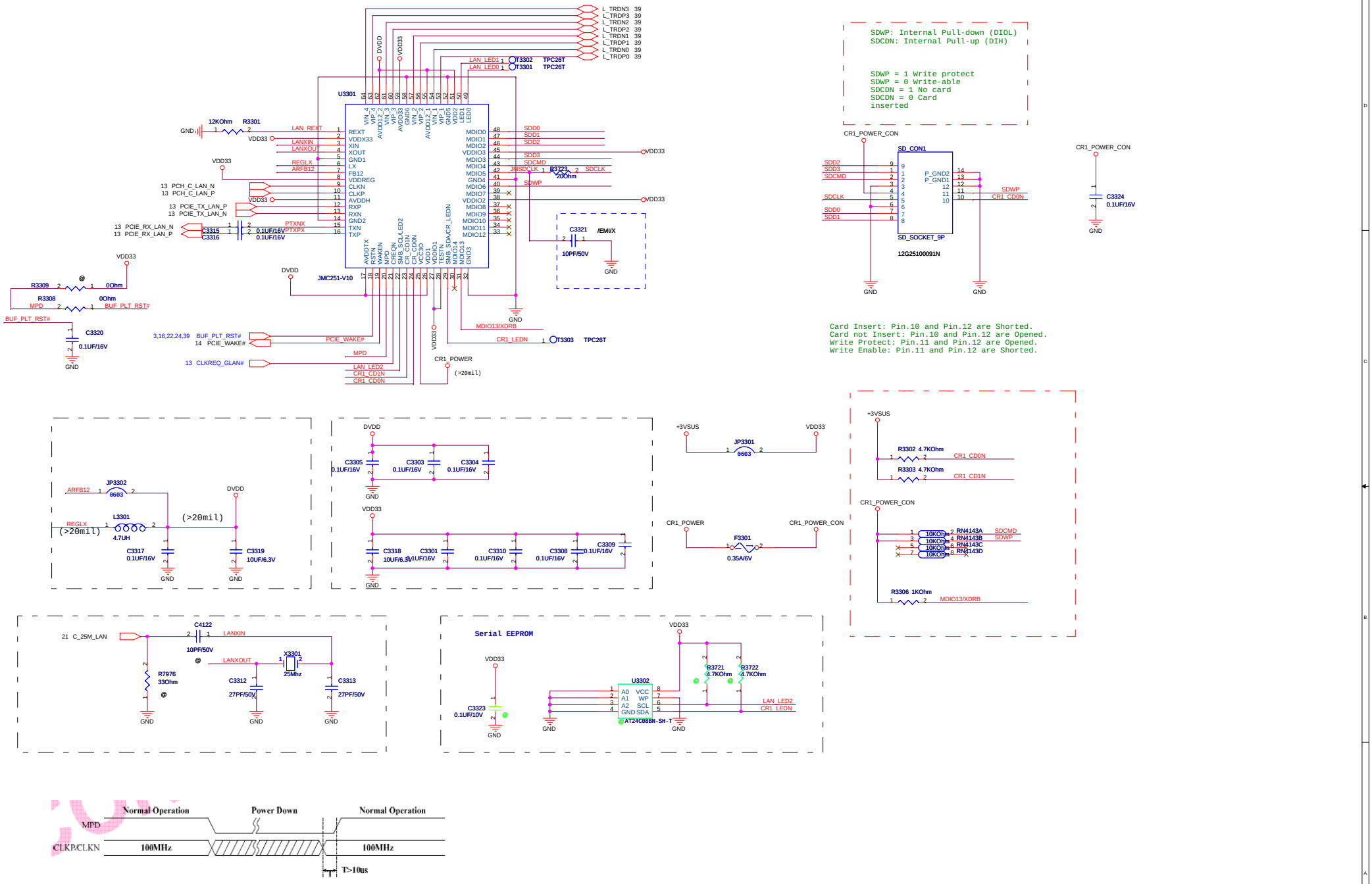


Internal MIC and AMP

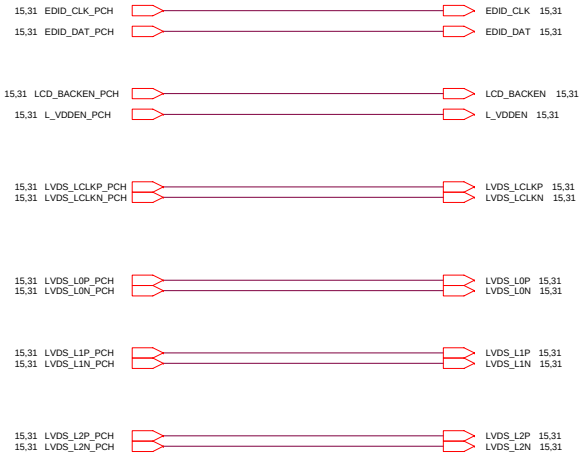


Update 11/09 R2.0

ASUSTeK COMPUTER INC. NB2	Title :	
	Engineer:	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 27 of 59	

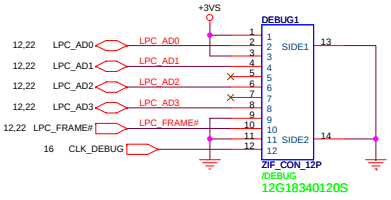


ASUSTeK COMPUTER INC. NB4	Title : LAN-AR8131	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 28 of 59	

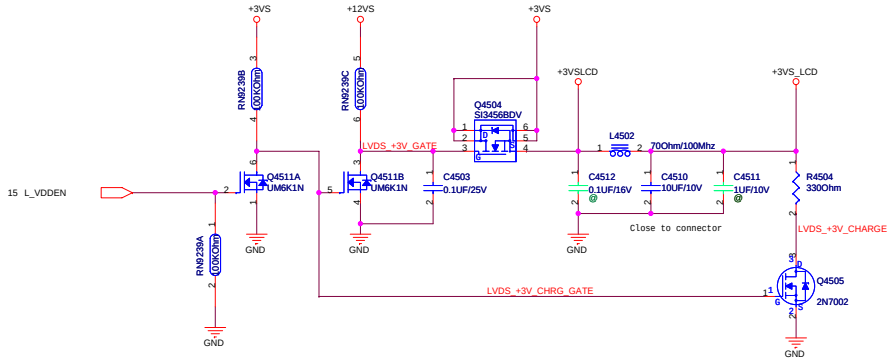


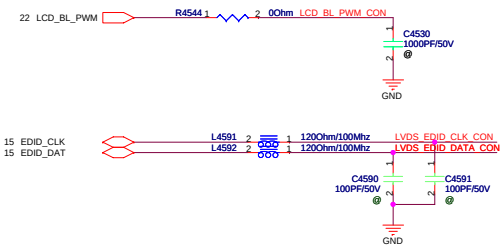
ASUSTeK COMPUTER INC. NB4	Title : CB_NewCard	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 29 of 59	

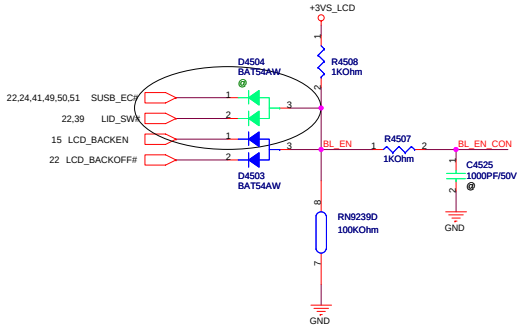
LPC Debug Port

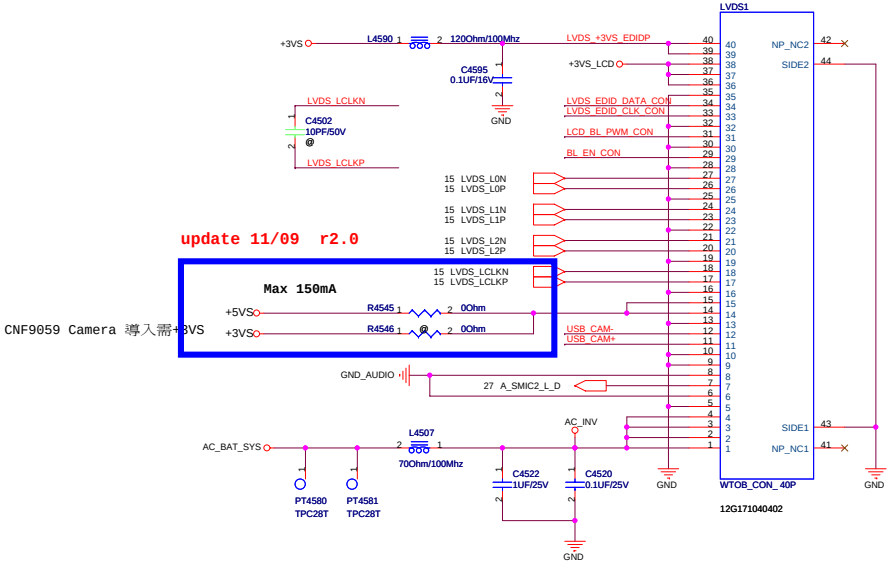


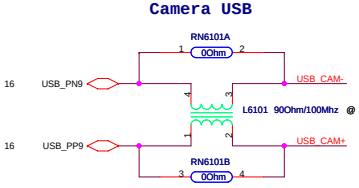
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 30 of 59	

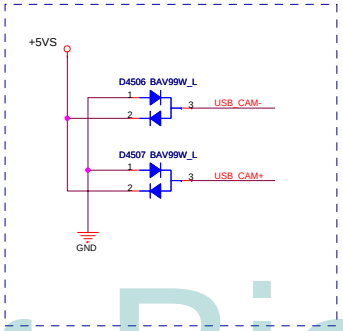


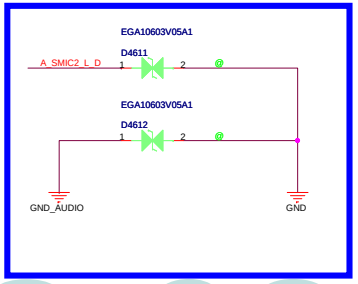




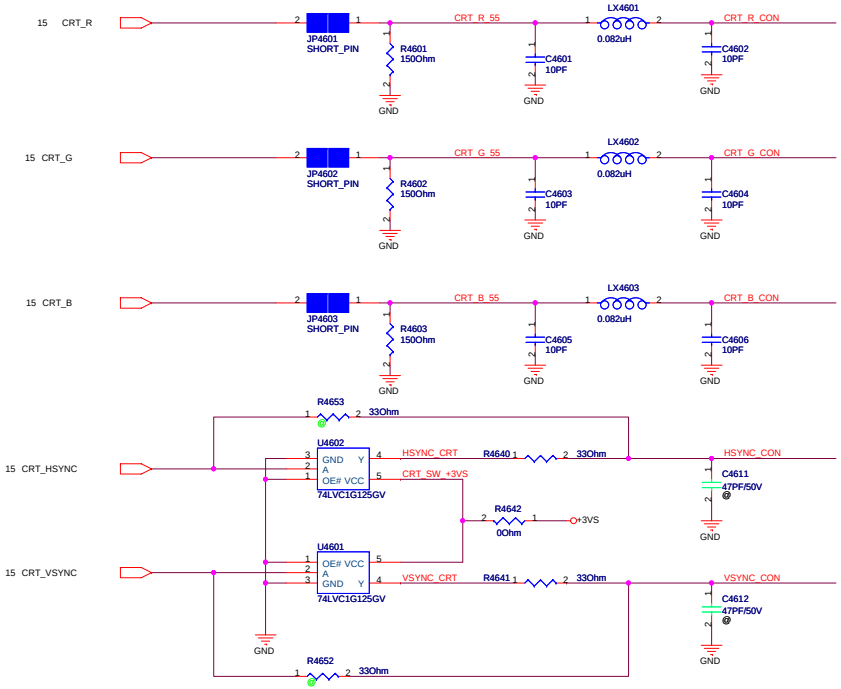


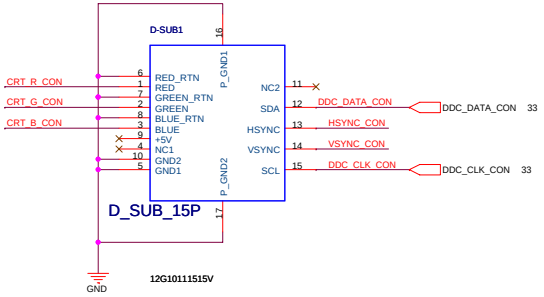


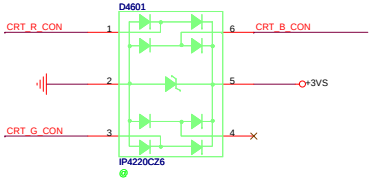


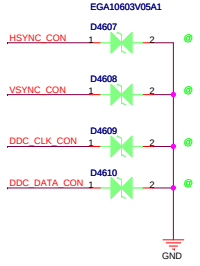


ASUSTeK COMPUTER INC. NB1	Title: LVDS & Inverter CON	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 31 of 59	

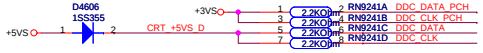


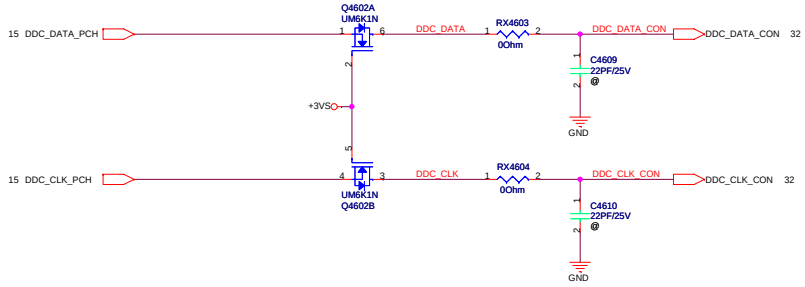




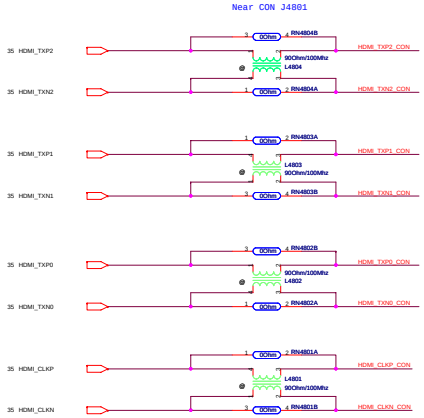


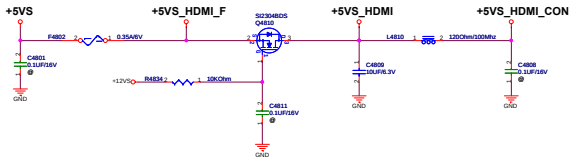
ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 32 of 59	

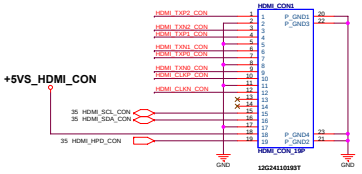




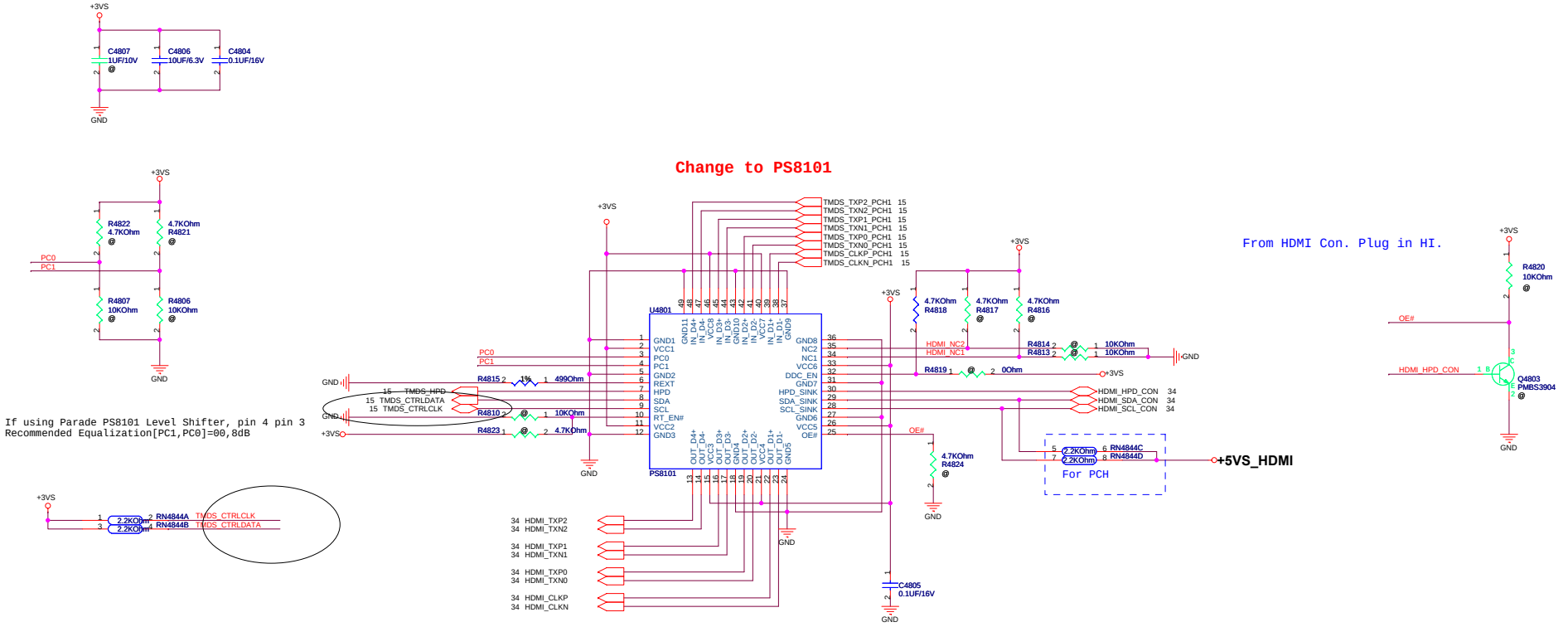
ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 33 of 59	







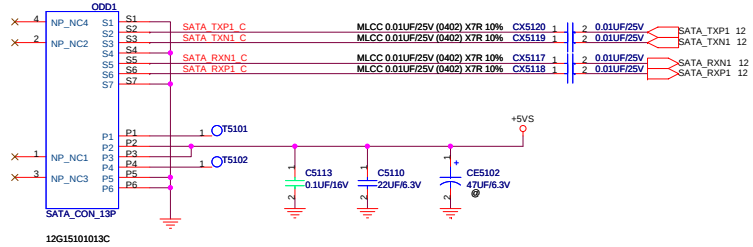
ASUSTeK COMPUTER INC. MB4	Title : TV_HDMI	
	Engineer: Modim Zhang	
Size: D	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 34 of 39	



ASUSTeK COMPUTER INC. NB4	Title : TV ****	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 35 of 59	

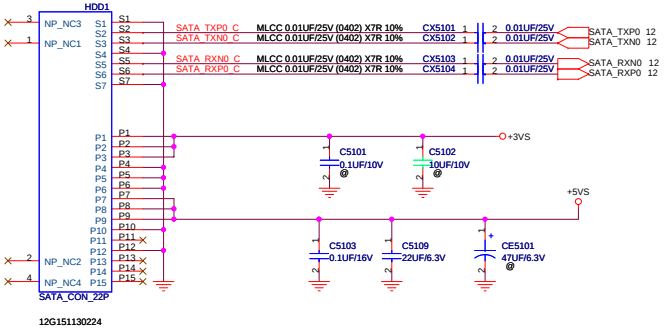
ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 36 of 59	

ODD



12G15101013C

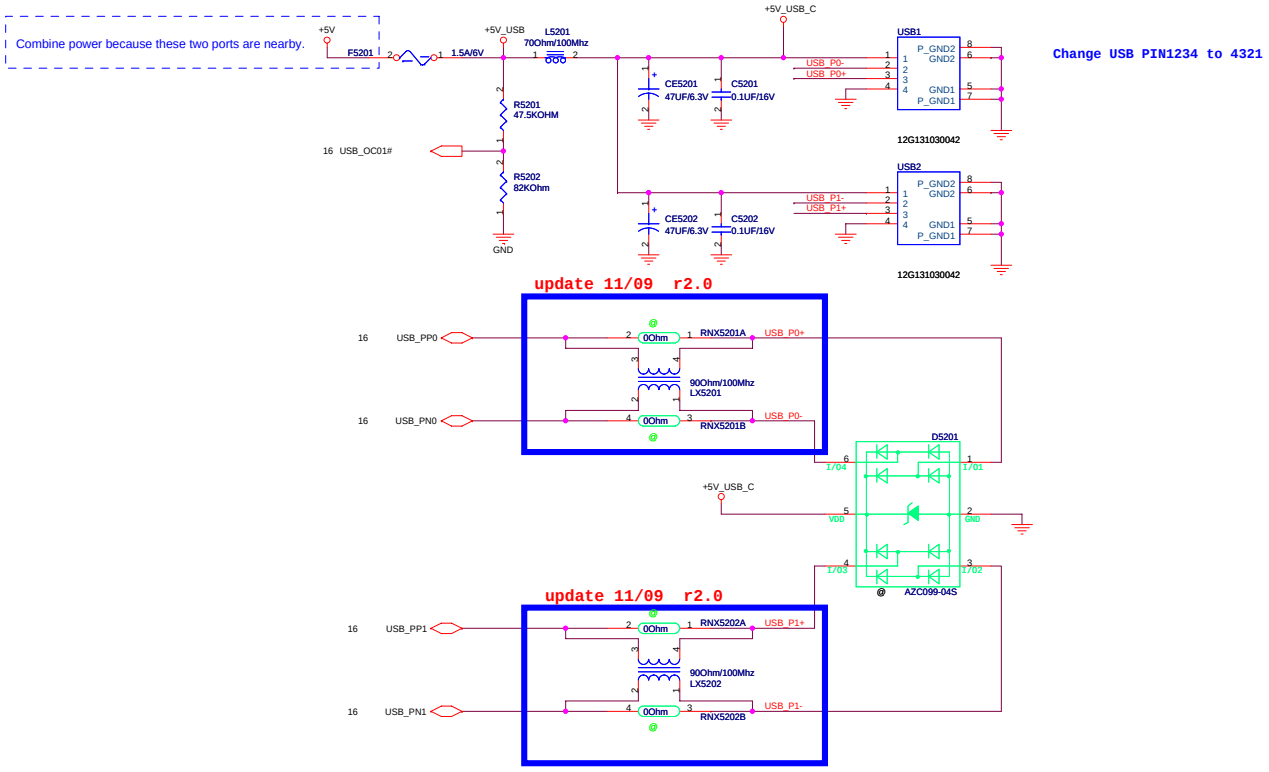
HDD (1st)



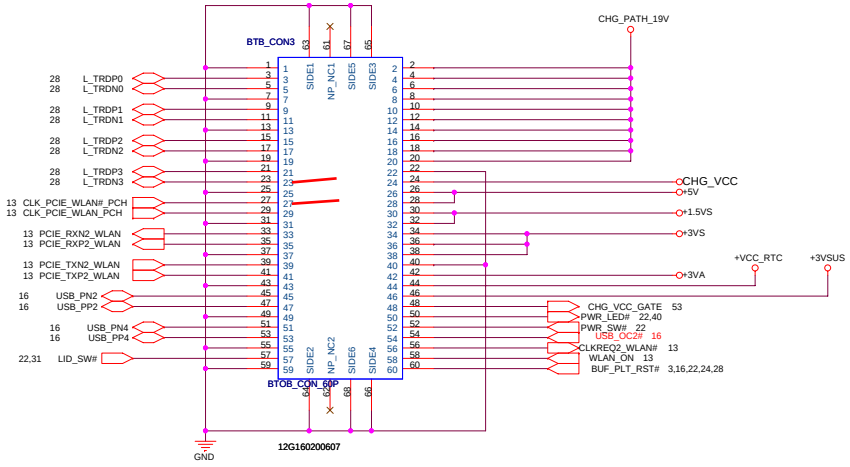
12G151130224

ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 37 of 59	

USB ports

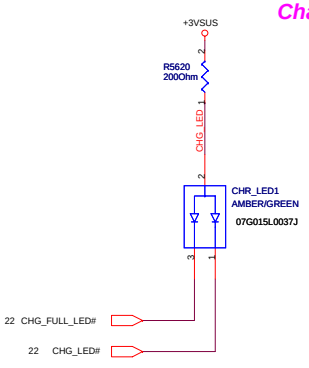


ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *2	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 38 of 59	

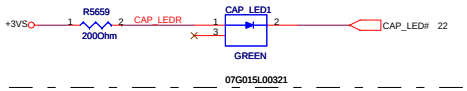


ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 39 of 59	

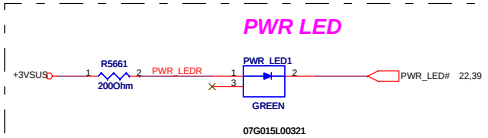
Charge LED



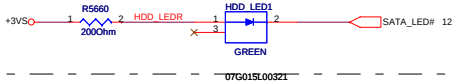
Cap. Lock LED



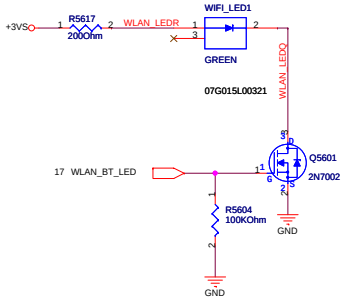
PWR LED



HDD LED



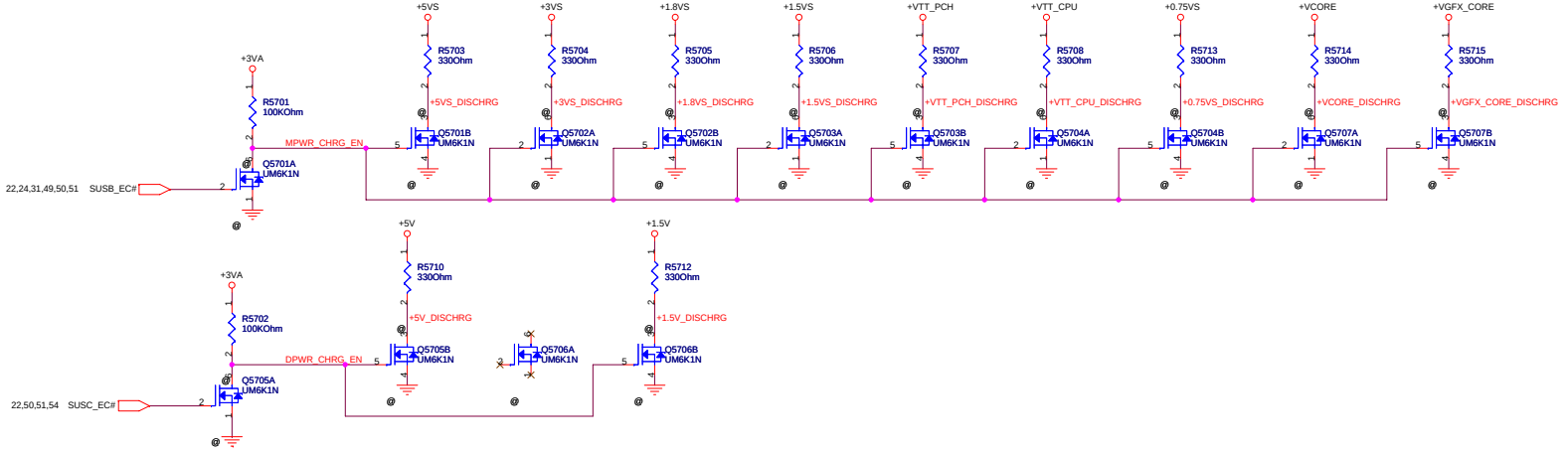
WLAN LED



ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 40 of 59	

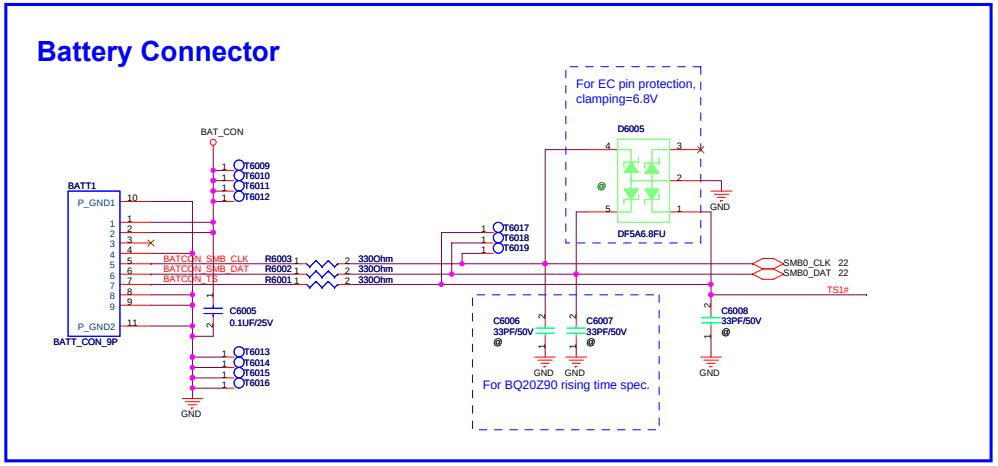
Main Board

Remove +2.5Vs is for ATI GFX

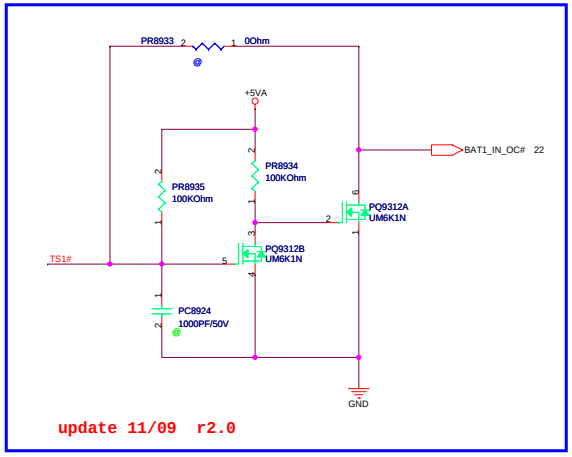


ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 41 of 59	

Battery Connector



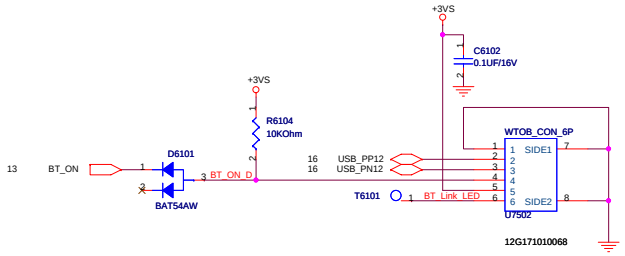
Battery IN DETECT



update 11/09 r2.0

ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 42 of 59	

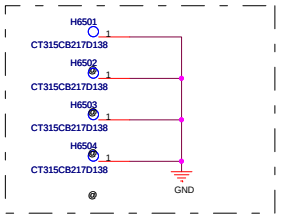
BLUETOOTH



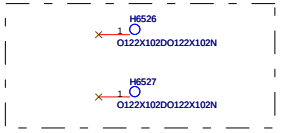
ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 43 of 59	

Main Board

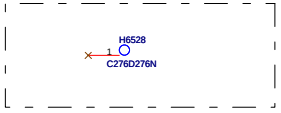
For CPU

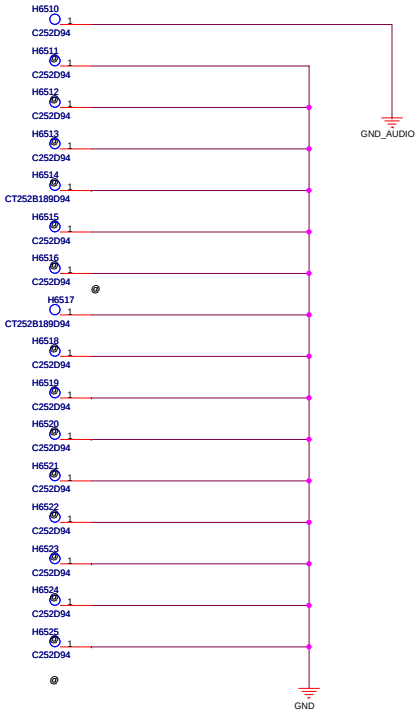


For 橢圓定位孔



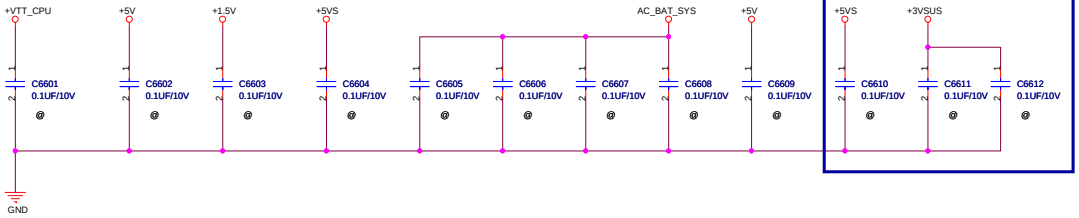
HDD 呼吸孔



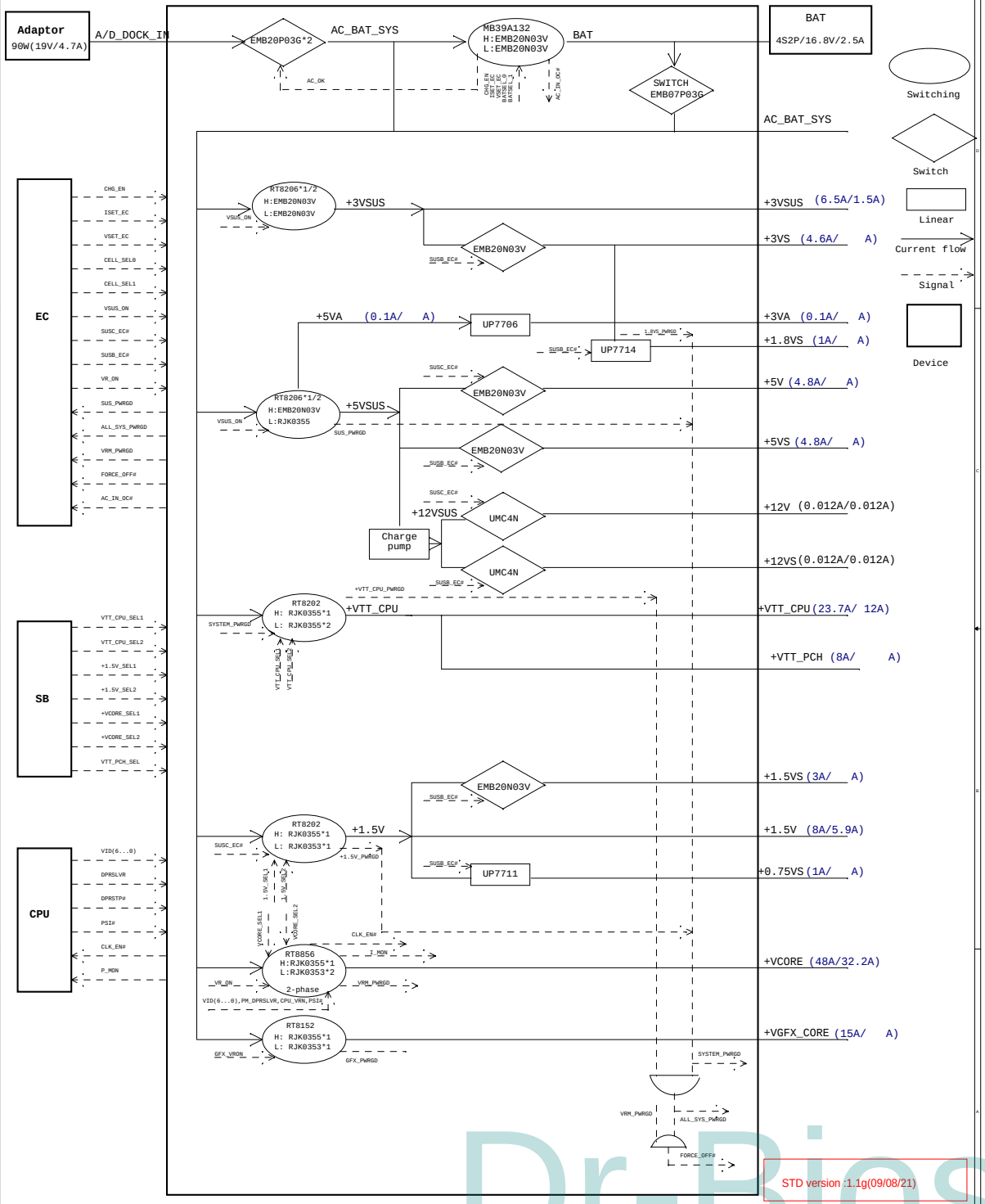


ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 44 of 59	

Update EMI CAP 1110



ASUSTeK COMPUTER INC. NB4	Title : EMI	
	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 45 of 59	


Adaptor
90W(19V/4.7A)
A/D_DOCK_IN
EMB20P03G*2
AC_BAT_SYS
MB39A132
H:EMB20N03V
L:EMB20N03V
BAT
BAT
4S2P/16.8V/2.5A
SWITCH
EMB07P03G
AC_OK
Switching
Switch
Linear
Current flow
Signal
Device
EC
SB
CPU
RT8206*1/2
H:EMB20N03V
L:EMB20N03V
+3VSUS
+3VSUS (6.5A/1.5A)
EMB20N03V
+3VS (4.6A/ A)
+5VA (0.1A/ A)
UP7706
+3VA (0.1A/ A)
UP7714
+1.8VS (1A/ A)
+5V (4.8A/ A)
RT8206*1/2
H:EMB20N03V
L:RJK0355
+5VSUS
+5VS (4.8A/ A)
+12VSUS
Charge pump
UMC4N
+12V (0.012A/0.012A)
+12VS(0.012A/0.012A)
RT8202
H: RJK0355*1
L: RJK0355*2
+VTT_CPU
+VTT_CPU(23.7A/ 12A)
+VTT_PCH (8A/ A)
+1.5VS (3A/ A)
RT8202
H: RJK0355*1
L: RJK0353*1
+1.5V
+1.5V (8A/5.9A)
UP7711
+0.75VS (1A/ A)
RT8856
H:RJK0355*1
L:RJK0353*2
2-phase
+VCORE (48A/32.2A)
RT8152
H: RJK0355*1
L: RJK0353*1
+VGFX_CORE (15A/ A)
STD version :1.1g(09/08/21)
Title : Power_FLOW
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
Rev
1.0
Date: Tuesday, November 10, 2009
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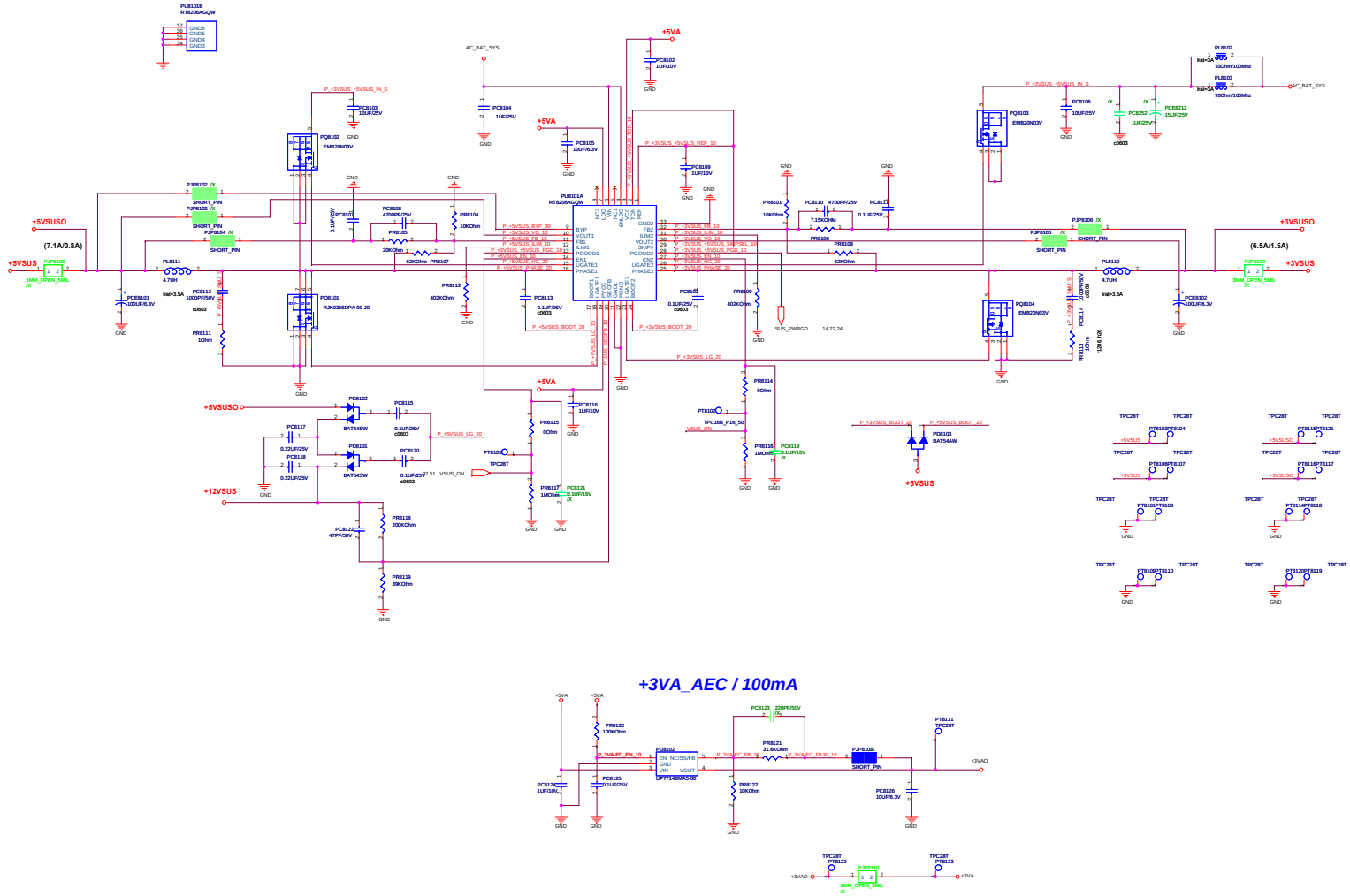

Power stage	+3VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =1.375A	
2. Ripple Current:	
I rip =1.152A	
I spec=2.5A ×1 pcs	
3. Dynamic:	
Ipeak=(vin-vo)*D/(L*Fsw)=1.55A	
ESR / 1 pcs =15mohm	
△V =23.25mV	
3. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
4. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm	(Vgs=4.5 V)
I cont = 8 A	(T =25 ℃)
I peak = 32A	(Pause ＜10 us)
L-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm	(Vgs=4.5 V)
I cont = 8 A	(T =25 ℃)
I peak = 32 A	(Pause ＜10 us)

Power stage	+5VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =2.082A	
2. Ripple Current:	
I rip =1.012A	
I spec=2.5A ×1	
3. Dynamic:	
Ipeak=(vin-vo)*D/(L*Fsw)=2.58A	
ESR / 1 pcs =15 mohm	
△V =38.72mV	
3. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
4. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm	(Vgs=4.5 V)
I cont = 8 A	(T =25 ℃)
I peak = 32A	(Pause ＜10 us)
L-side MOSFET: RJK0355DPA-00-J0 WPAK	
Rds(ON)= 11.8 mohm	(Vgs=4.5 V)
I cont = 30 A	(T =25 ℃)
I peak = 120 A	(Pause ＜10 us)

Controller	+3VSUS
1. Voltage & Current:	
+3VSUS=3.3V@3A	
2. Frequency:	
fosc=375KHz	
3. OCP:	
Set PR8109=402Kohm	
Iocp=8.74A	
4. Soft start time:	
Tss=2ms	
5.Inrush Current:	
C total = 100 uF	
I inrush= 0.165 A	

Controller	+5VSUS
1. Voltage & Current:	
+5VSUS=5V@3A	
2. Frequency:	
fosc=300KHz	
3. OCP:	
Set PR8112=402Kohm	
Iocp=17A	
8. Soft start time:	
Tss=2ms	
10.Inrush Current:	
C total = 100 uF	
I inrush= 0.275 A	

ASUSTeK Computer INC

Title : Power +5SUS&+3VSUS&+12VSUS

Engineer: Modin Zhang

Size	Project Name	Rev
Custom	K42F	1.0

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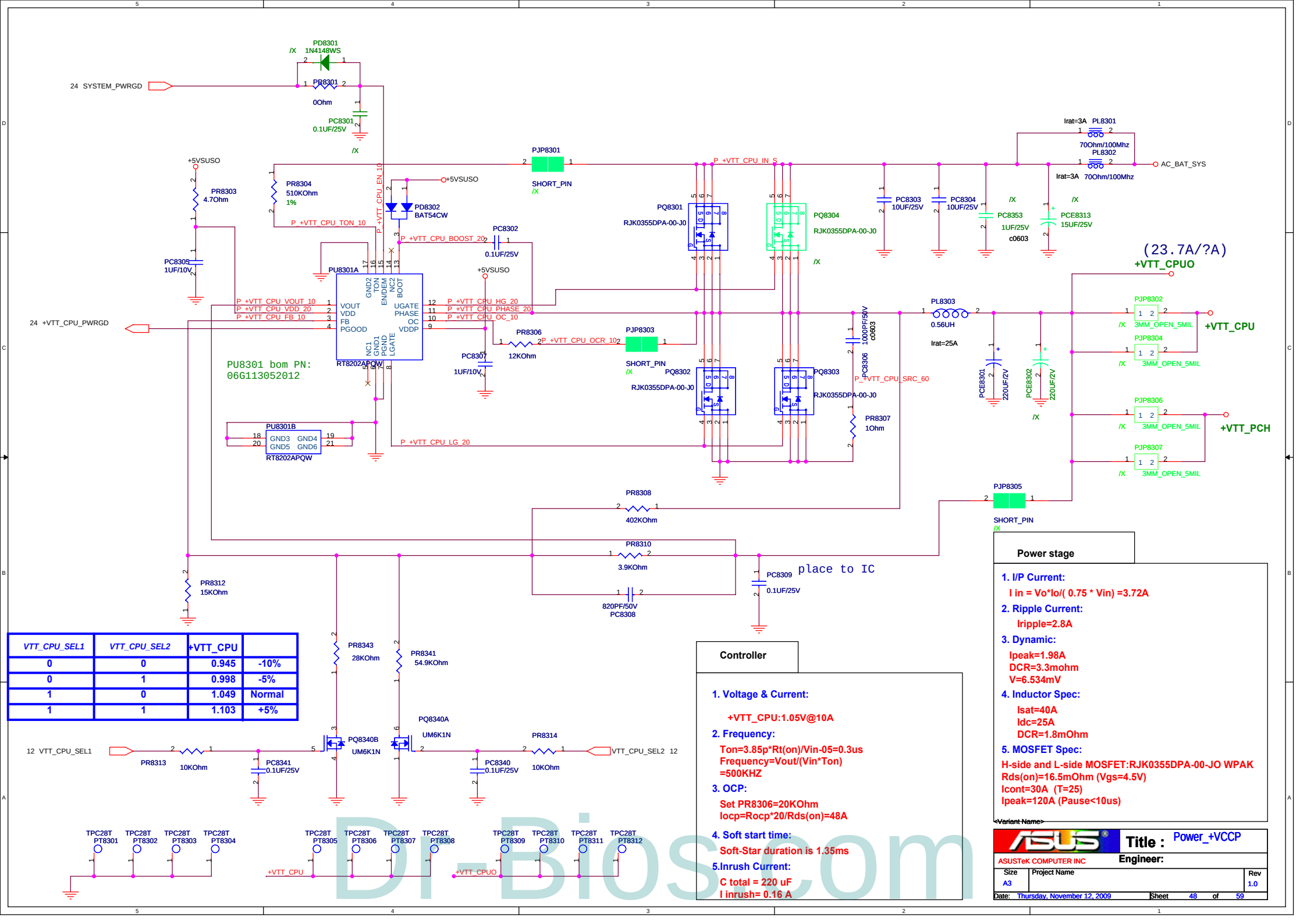


VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

Controller

1. Voltage & Current:

   +VTT_CPU:1.05V@10A

2. Frequency:

   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   Set PR8306=20KOhm
   Iocp=Rocp*20/Rds(on)=48A

4. Soft start time:

   Soft-Star duration is 1.35ms

5. Inrush Current:

   C total = 220 uF
   I inrush= 0.16 A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =3.72A

2. Ripple Current:

   Iripple=2.8A

3. Dynamic:

   Ipeak=1.98A
   DCR=3.3mohm
   V=6.534mV

4. Inductor Spec:

   Isat=40A
   Idc=25A
   DCR=1.8mOhm

5. MOSFET Spec:

   H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

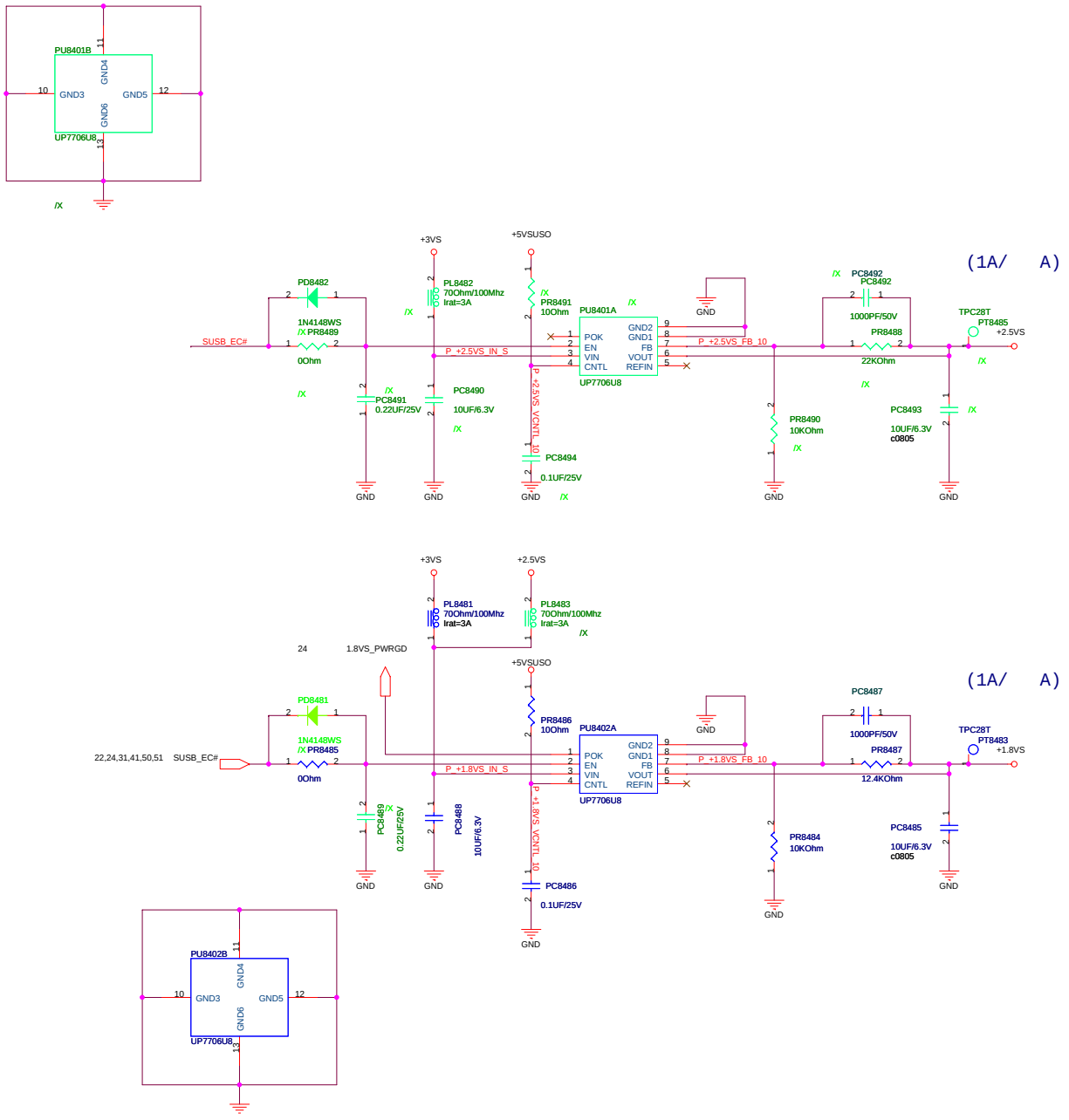
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer:

Size	Project Name	Rev
A3		1.0

Date: Thursday, November 12, 2009 Sheet 48 of 59



<Variant Name>

ASUSTeK COMPUTER INC

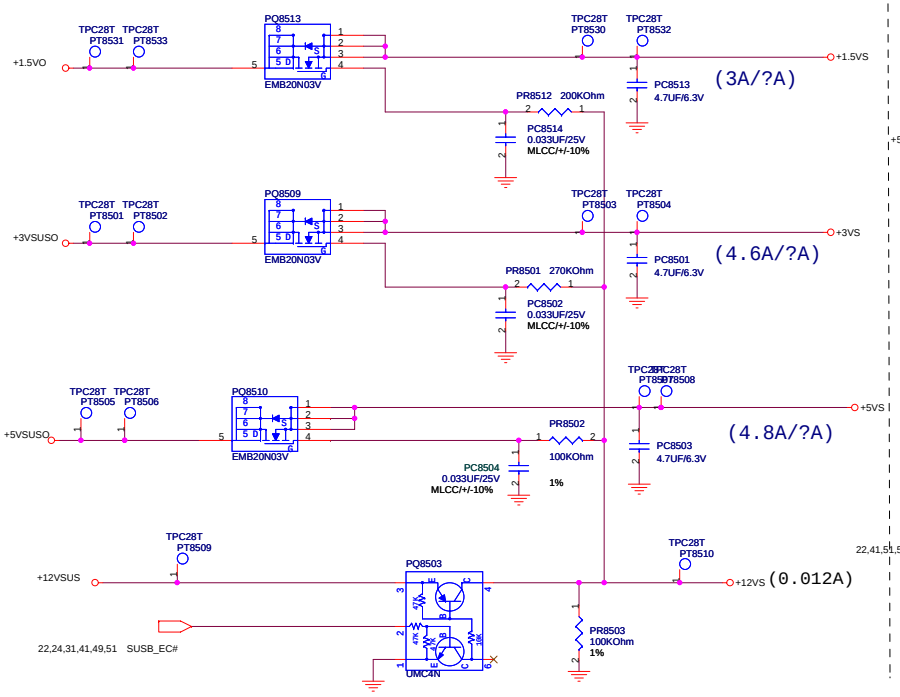
Title : Power_+1.8V&+0.9V

Engineer:

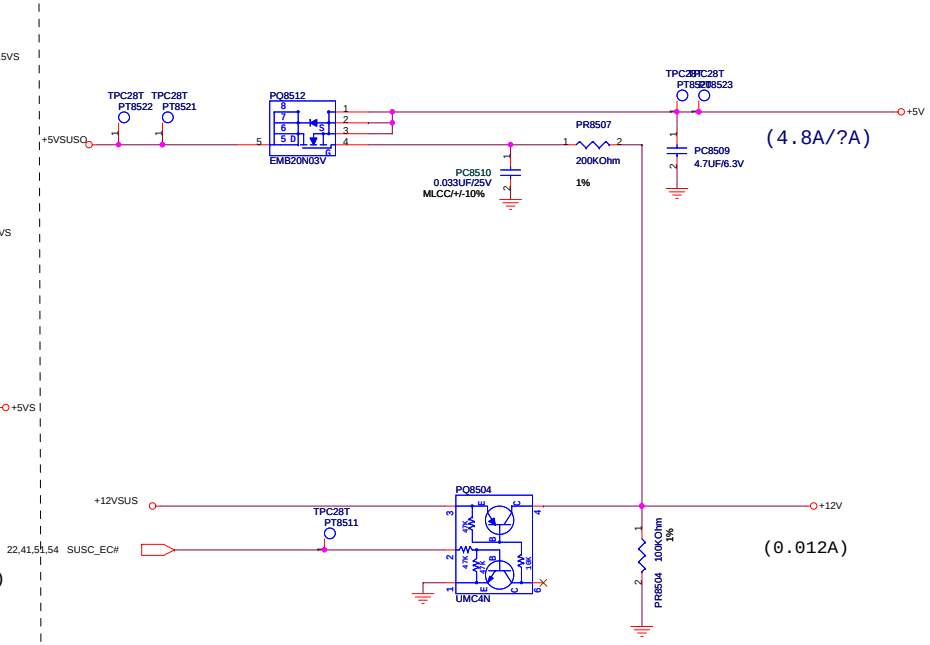
Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009 Sheet 49 of 59

SUSB#_PWR POWER



SUSC#_PWR POWER



<variant_name>

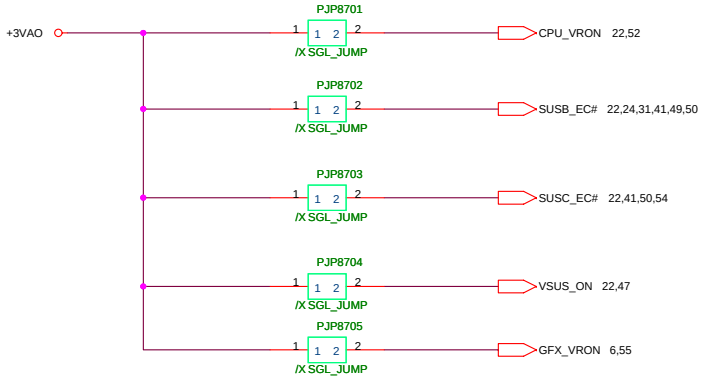
ASUSTeK COMPUTER INC

Title : Power_Load_Switch

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009 Sheet 50 of 59



<Variant Name>

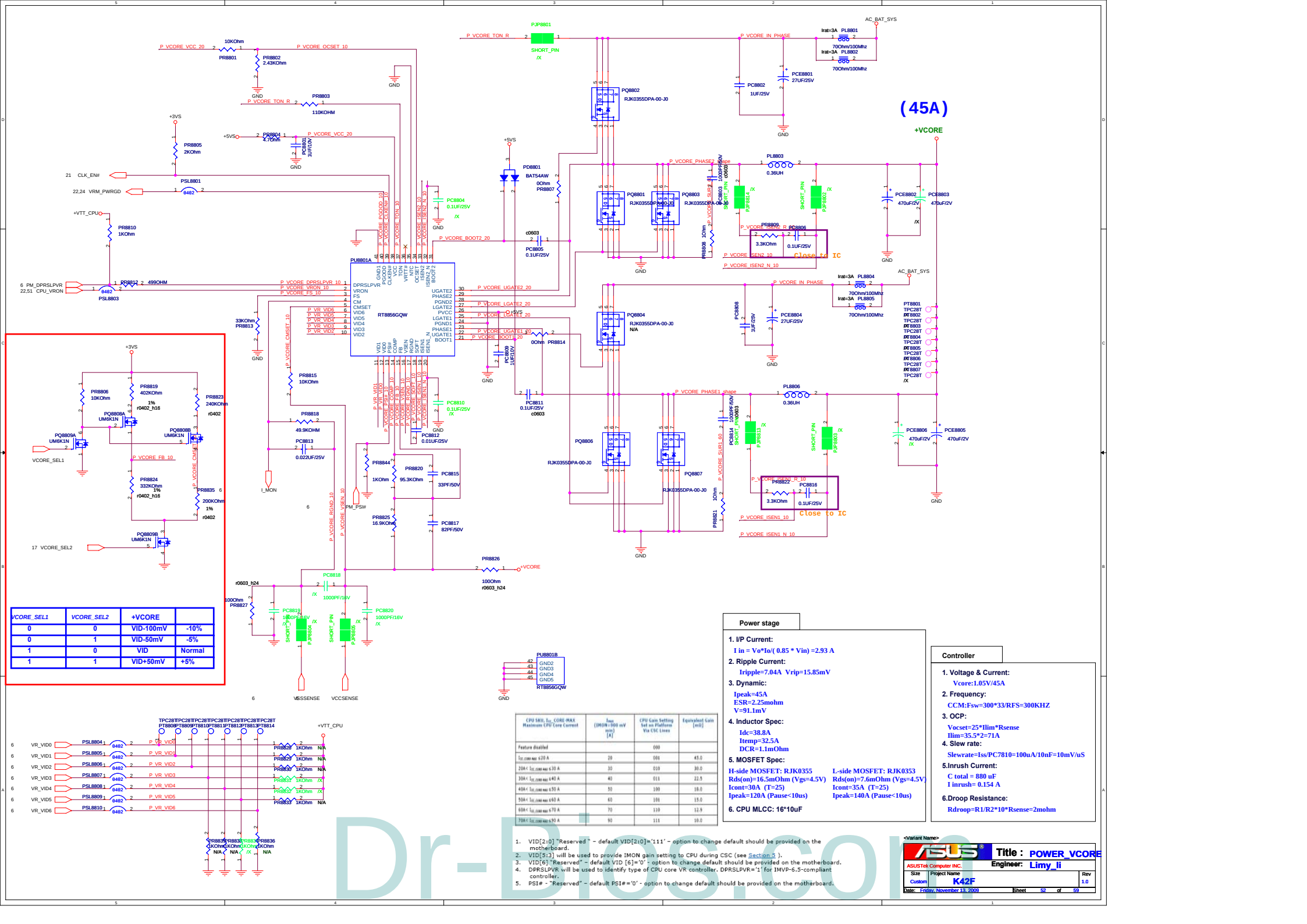
ASUSTeK COMPUTER INC

Title : Power_for_test

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009 Sheet 51 of 59



VCORE_SEL1	VCORE_SEL2	+VCORE	
0	0	VID-100mV	-10%
0	1	VID-50mV	-5%
1	0	VID	Normal
1	1	VID+50mV	+5%

CPU SKU, I_{TDC} CORE-MAX Maximum CPU Core Current	I_{MAX} (IMON=900 mV min) [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain (mΩ)
Feature Disabled		000	
$I_{TDC,CORE,MAX}$ ≤20 A	20	001	45.0
20A< $I_{TDC,CORE,MAX}$ ≤30 A	30	010	30.0
30A< $I_{TDC,CORE,MAX}$ ≤40 A	40	011	22.5
40A< $I_{TDC,CORE,MAX}$ ≤50 A	50	100	18.0
50A< $I_{TDC,CORE,MAX}$ ≤60 A	60	101	15.0
60A< $I_{TDC,CORE,MAX}$ ≤70 A	70	110	12.9
70A< $I_{TDC,CORE,MAX}$ ≤90 A	90	111	10.0

1. VID[2:0] "Reserved " – default VID[2:0]='111' – option to change default should be provided on the motherboard.
2. VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
3. VID[6] "Reserved" – default VID [6]='0' – option to change default should be provided on the motherboard.
4. DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR='1' for IMVP-6.5-compliant controller.
5. PSI# - "Reserved" – default PSI#='0' – option to change default should be provided on the motherboard.

Power stage

1. I/P Current:
   I in = Vo*Io/(0.85 * Vin) =2.93 A
2. Ripple Current:
   Iripple=7.04A Vrip=15.85mV
3. Dynamic:
   Ipeak=45A
   ESR=2.25mohm
   V=91.1mV
4. Inductor Spec:
   Idc=38.8A
   Itemp=32.5A
   DCR=1.1mOhm
5. MOSFET Spec:
   H-side MOSFET: RJK0355
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)
   L-side MOSFET: RJK0353
   Rds(on)=7.6mOhm (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)
6. CPU MLCC: 16*10uF

Controller

1. Voltage & Current:
   Vcore:1.05V/45A
2. Frequency:
   CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
   Vcset=25*Ilim*Rsense
   Ilim=35.5*2=71A
4. Slew rate:
   Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5. Inrush Current:
   C total = 880 uF
   I inrush= 0.154 A
6. Droop Resistance:
   Rdroop=R1/R2*10*Rsense=2mohm

<Variant Name>

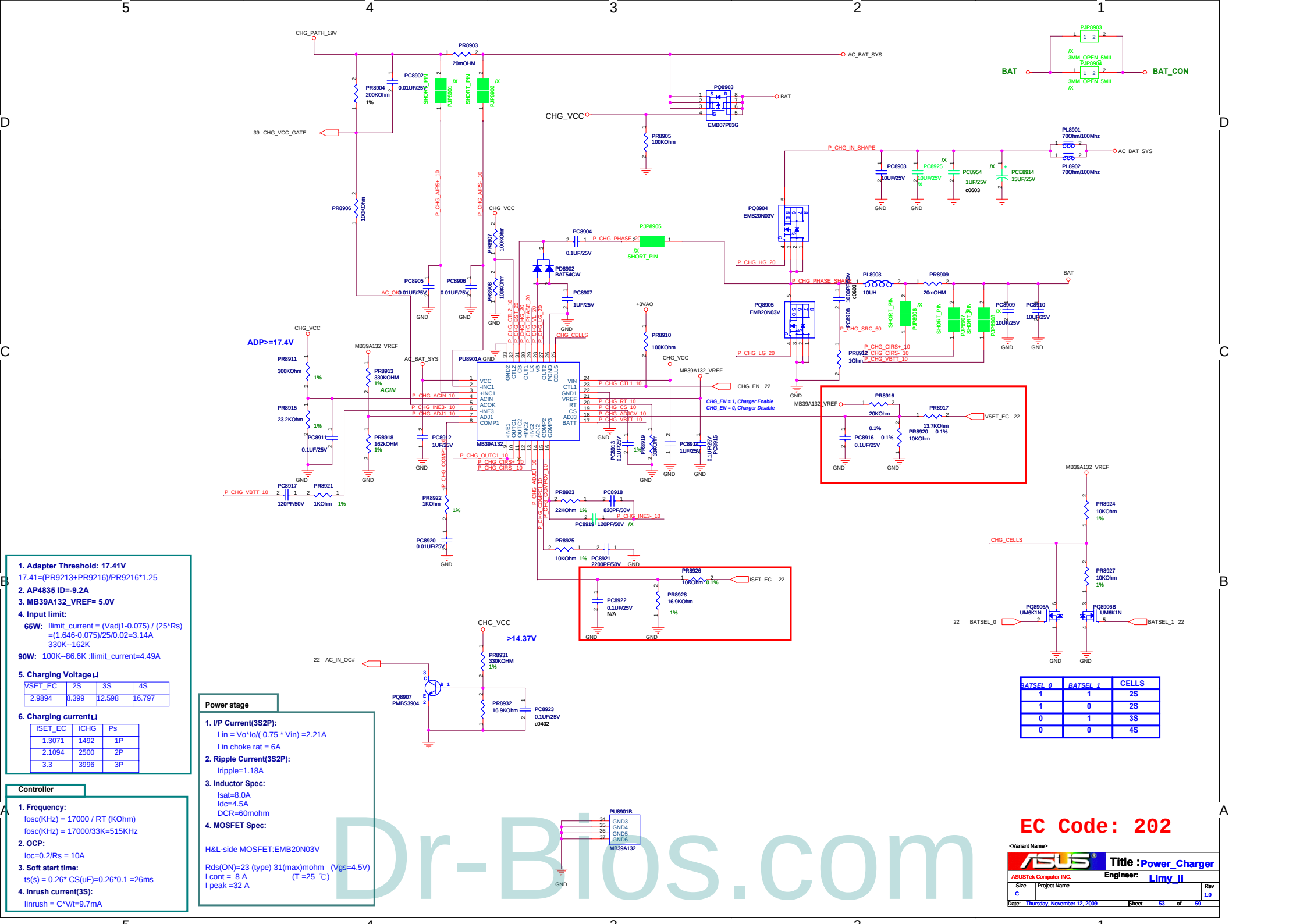
ASUSTeK Computer INC.

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
Custom	K42F	1.0

Date: Friday, November 13, 2009 Sheet 52 of 59



BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

1. Adapter Threshold: 17.41V

17.41=(PR9213+PR9216)/PR9216*1.25

2. AP4835 ID=-9.2A

3. MB39A132_VREF= 5.0V

4. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25/0.02=3.14A
330K--162K

90W: 100K--86.6K :Ilimit_current=4.49A

5. Charging Voltage

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

6. Charging current

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:

fosc(KHz) = 17000 / RT (KOhm)

fosc(KHz) = 17000/33K=515KHz

2. OCP:

Ioc=0.2/Rs = 10A

3. Soft start time:

ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms

4. Inrush current(3S):

Iinrush = C*V/t=9.7mA

Power stage

1. I/P Current(3S2P):

I in = Vo*Io/(0.75 * Vin) =2.21A

I in choke rat = 6A

2. Ripple Current(3S2P):

Iripple=1.18A

3. Inductor Spec:

Isat=8.0A
Idc=4.5A
DCR=60mohm

4. MOSFET Spec:

H&L-side MOSFET:EMB20N03V

Rds(ON)=23 (type) 31(max)mohm (Vgs=4.5V)
I cont = 8 A (T =25 ℃)
I peak =32 A

EC Code: 202

<Variant Name>

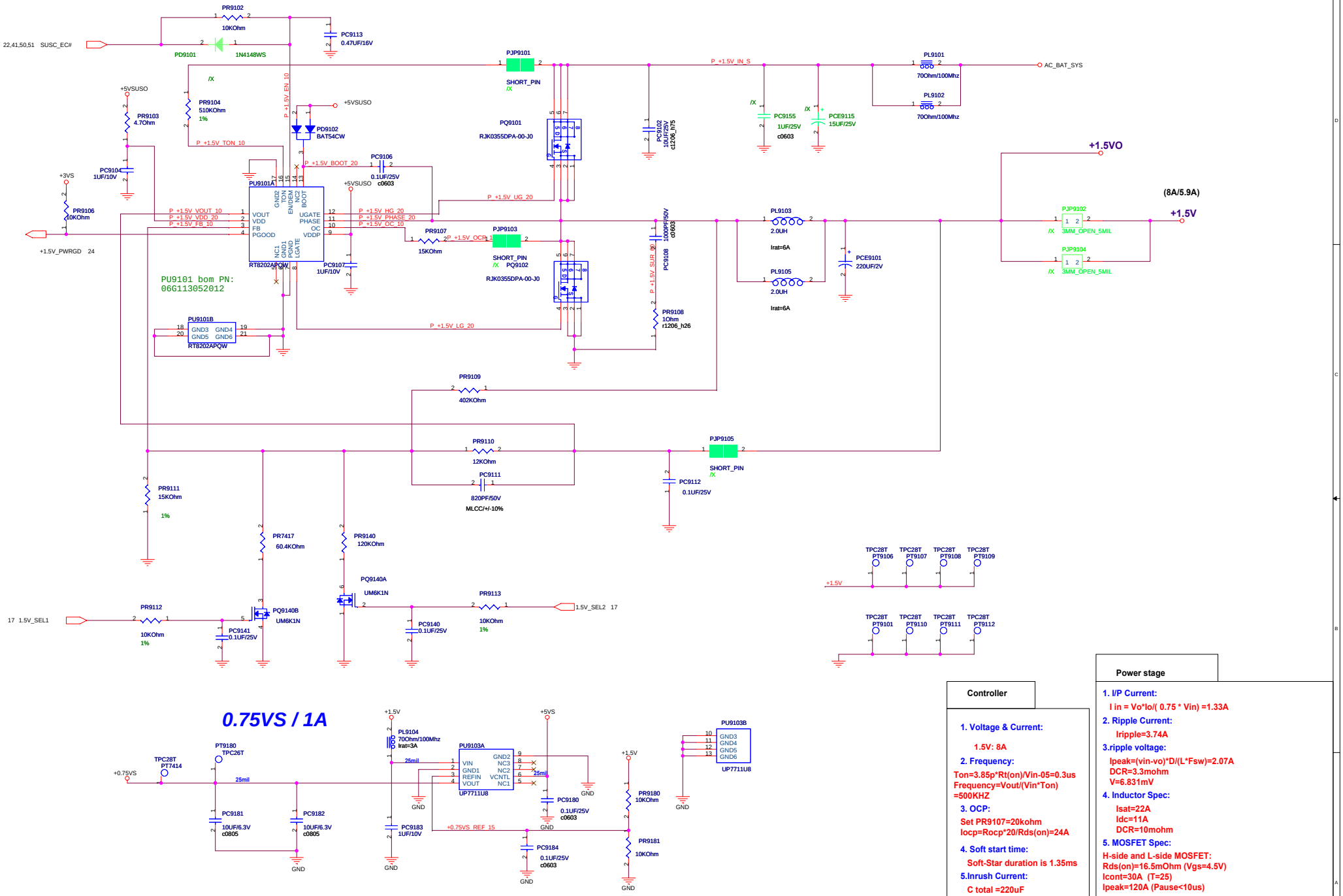
Title : Power_Charger

ASUSTek Computer INC.

Engineer: Limy_li

Size	Project Name	Rev
C		1.0

Date: Thursday, November 12, 2009 Sheet 53 of 59



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

Controller

1. Voltage & Current:
   1.5V: 8A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR9107=20kohm
   Iocp=Rocp*20/Rds(on)=24A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33A
2. Ripple Current:
   Iripple=3.74A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=10mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

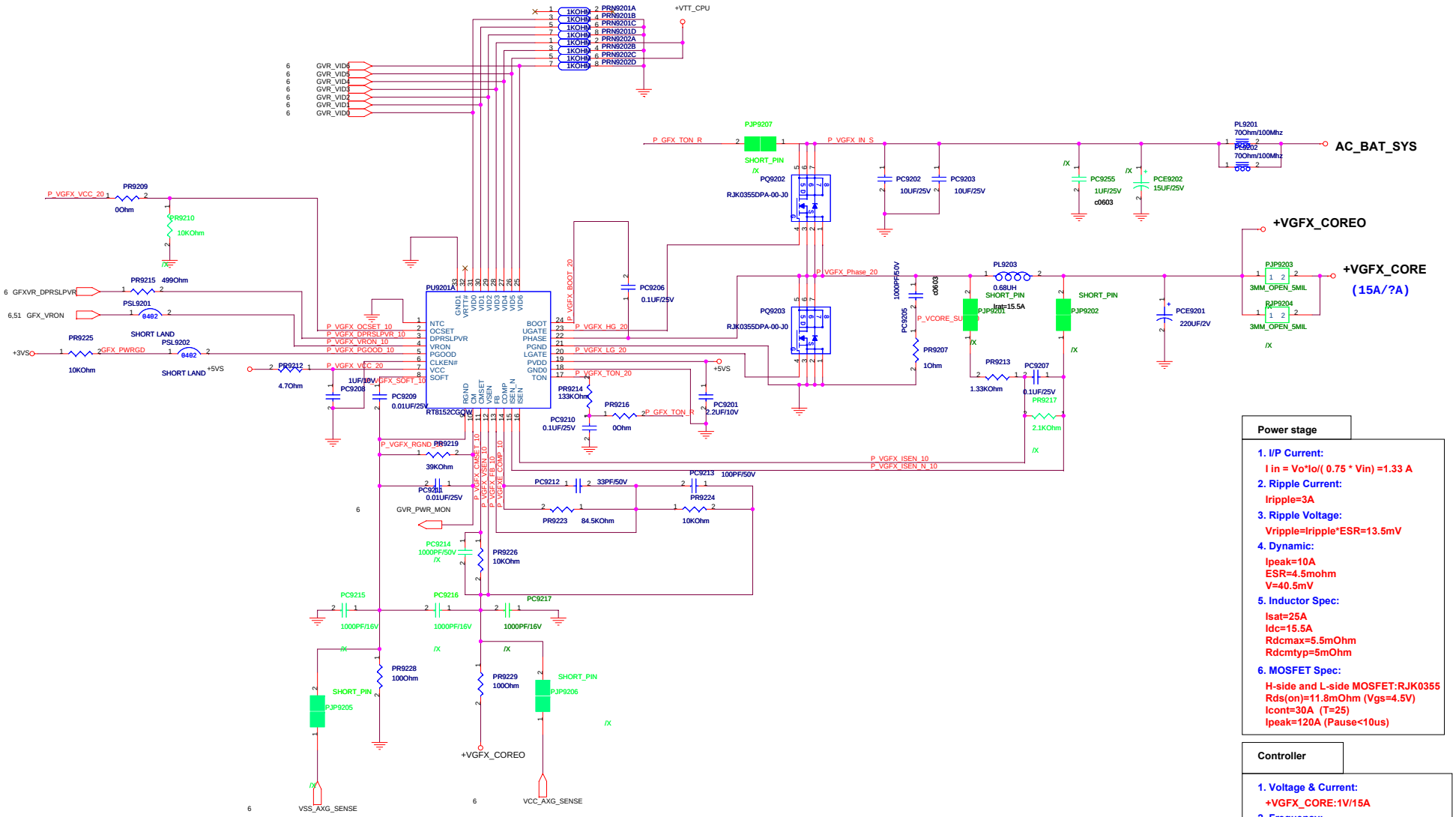
ASUSTeK COMPUTER INC

Title : +1.5V

Engineer:

Size	Project Name	Rev
C	K42F	1.0

Date: Thursday, November 12, 2009 Sheet 54 of 59



Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=10A
   ESR=4.5mohm
   V=40.5mV
5. Inductor Spec:
   Isat=25A
   Idc=15.5A
   Rdcmax=5.5mOhm
   Rdcmtyp=5mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

Controller

1. Voltage & Current:
   +VGFX_CORE:1V/15A
2. Frequency:
   Ton=Cton*(Rton+6.5K)
   Cton=16.26PF
   fsw=309KHZ
3. OCP:
   Vocsest=40%Ilim%Rsense
   Imax=30A
4. On time:
   Ton=Tsw*(Vfb+0.075)/Vin=354ns
5. LoadLine:
   Rdroop=Ai%Rsense%R1/R2
   =7mohm

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Modim Zhang

Size	Project Name	Rev
C	K42F	1.0

Date: Thursday, November 12, 2009 Sheet 55 of 59

VTT_CPU_SEL1 Default : H
VTT_CPU_SEL2 Default : L

VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

VCORE_SEL1 Default : H
VCORE_SEL2 Default : L

VCORE_SEL1	VCORE_SEL2	+VCORE	
0	0	VID-100mV	-10%
0	1	VID-50mV	-5%
1	0	VID	Normal
1	1	VID+50mV	+5%

1.5V_SEL1 Default : H
1.5V_SEL2 Default : L

1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VCCP

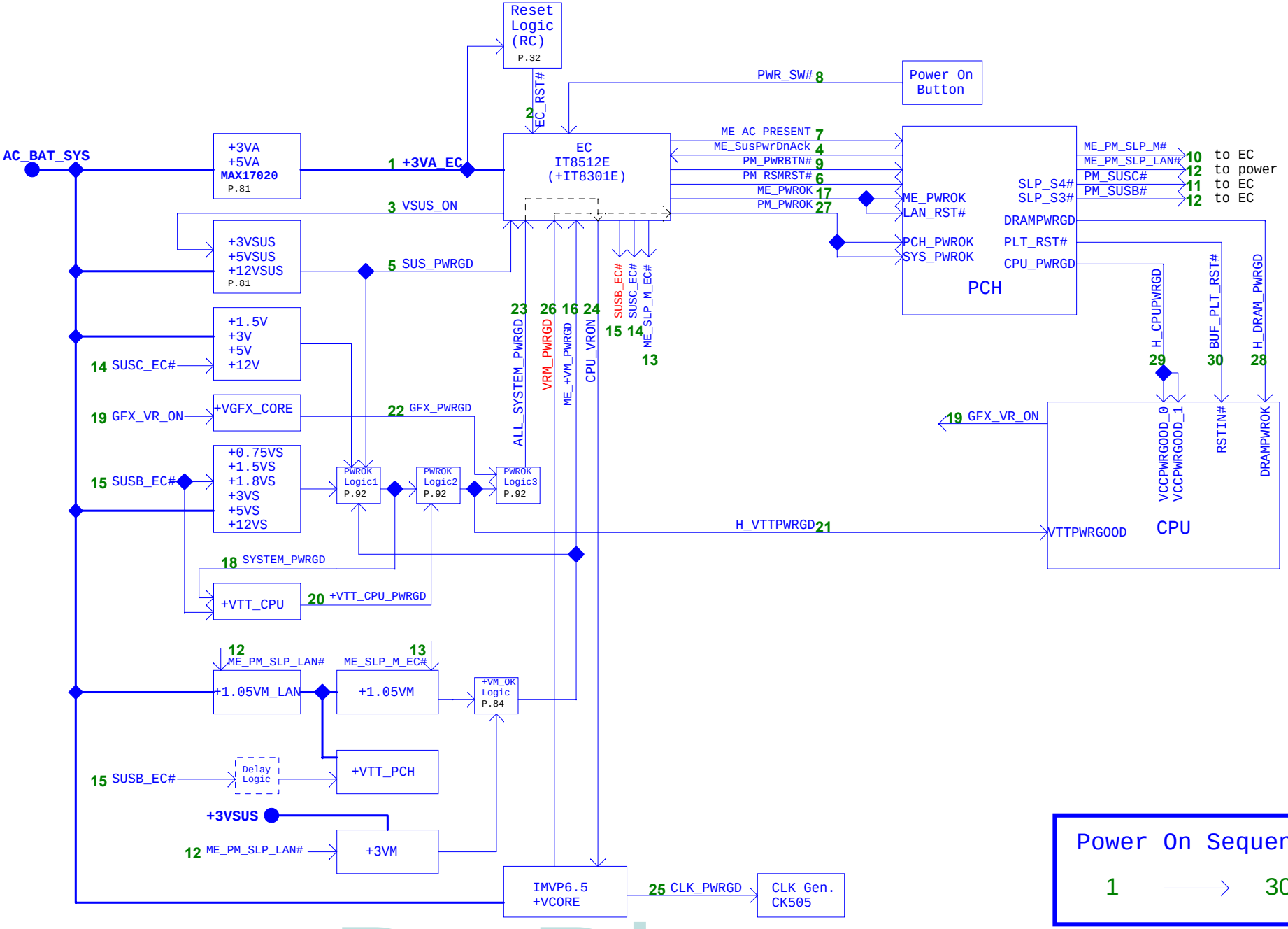
Engineer:

Size	Project Name	
A3		

Date: Tuesday, November 10, 2009 Sheet 56 of 59

AC-IN Mode

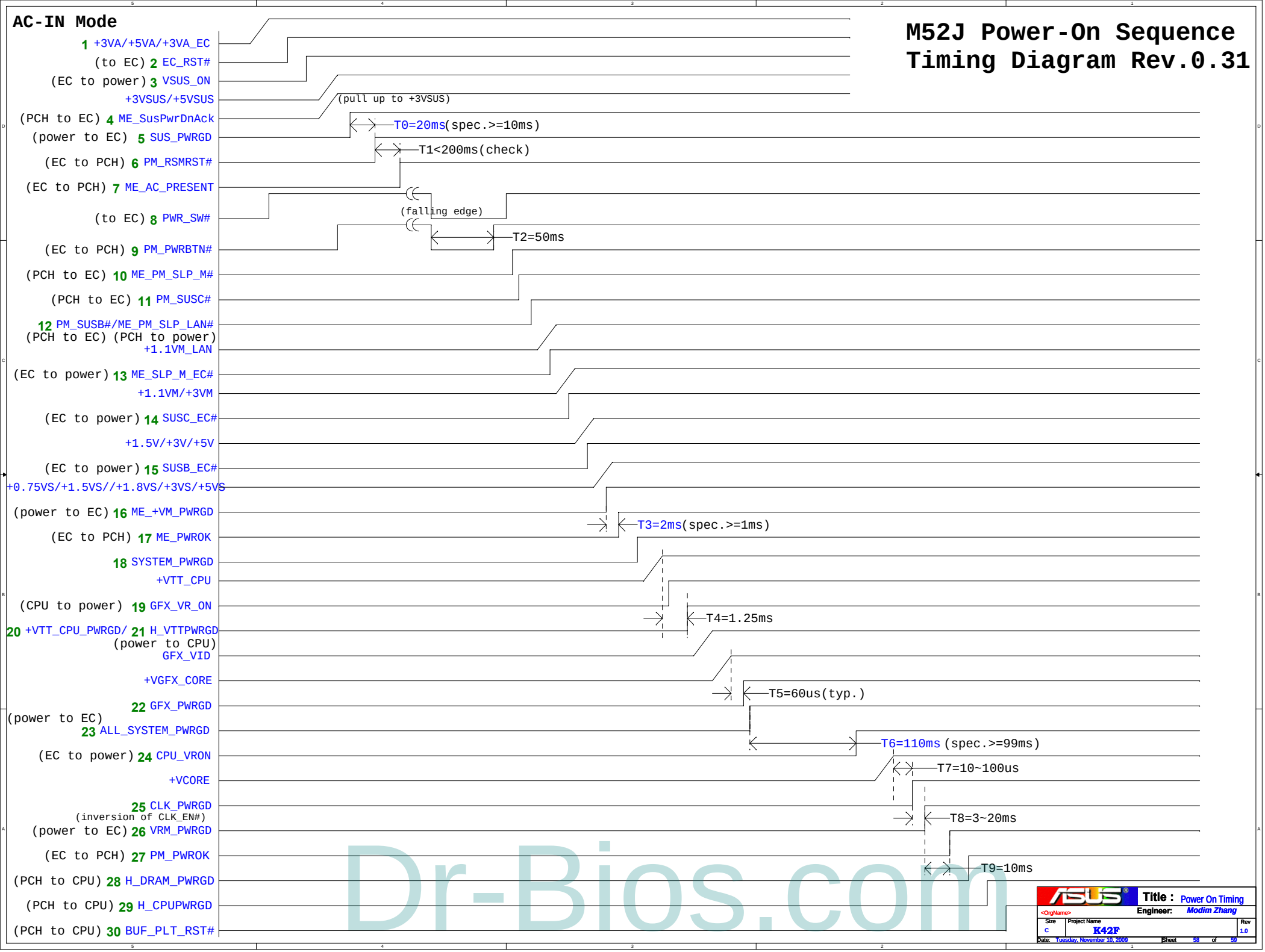
M52J Power On Sequence Diagram Rev. 0.31



ASUSTeK COMPUTER INC.
Title : POWER SEQUENCE
Engineer: Modim Zhang
Size C | Project Name K42F | Rev 1.0
Date: Tuesday, November 10, 2009 | Sheet 57 of 59

M52J Power-On Sequence Timing Diagram Rev.0.31

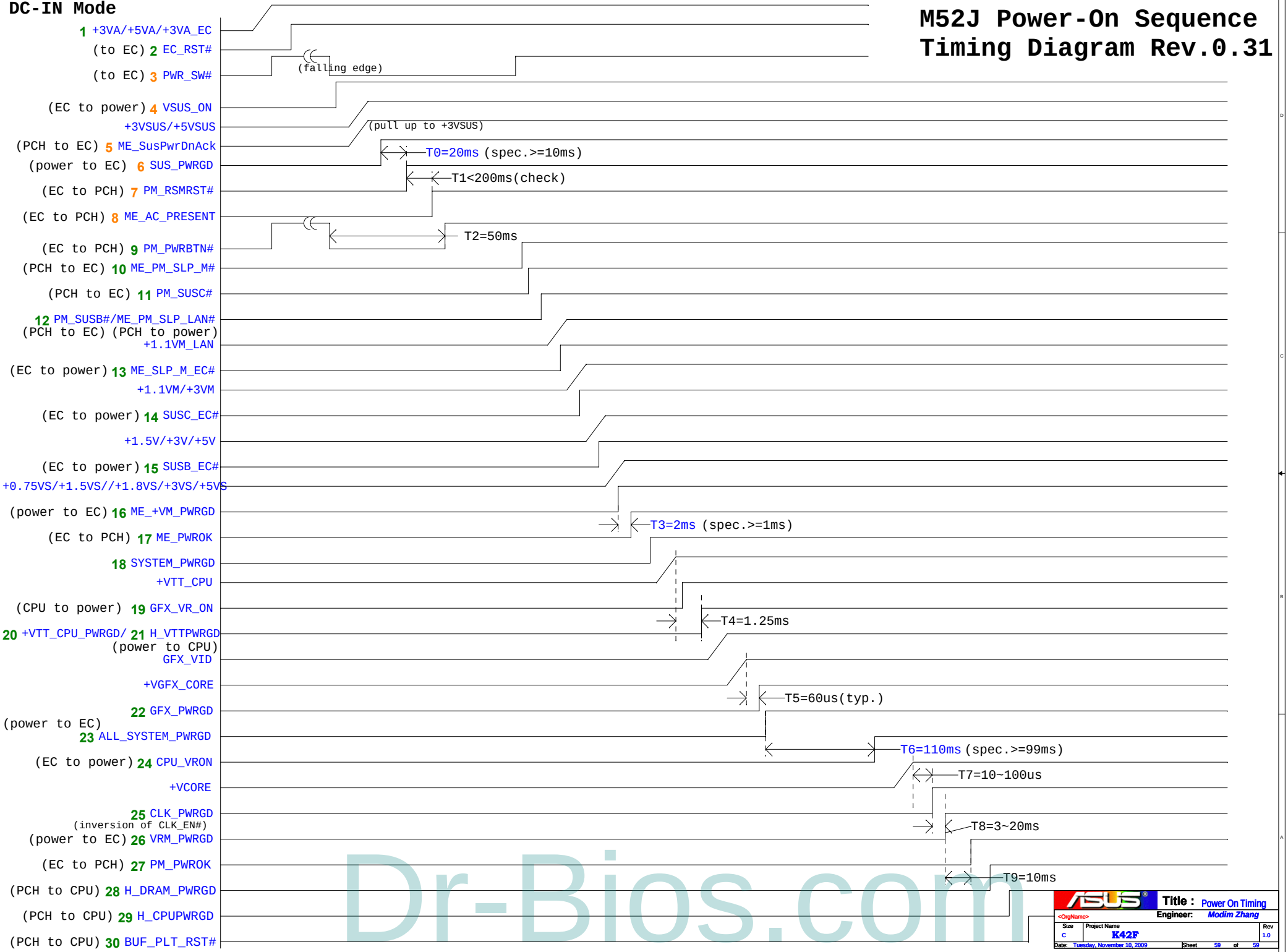
AC-IN Mode



ASUS	Title : Power On Timing	
<OrgName>	Engineer: Modim Zhang	
Size: C	Project Name: K42F	Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 58 of 59	

M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode



ASUS	Title : Power On Timing		
<OrgName>	Engineer: Modim Zhang		
Size: C	Project Name: K42F		Rev: 1.0
Date: Tuesday, November 10, 2009	Sheet 59 of 59		