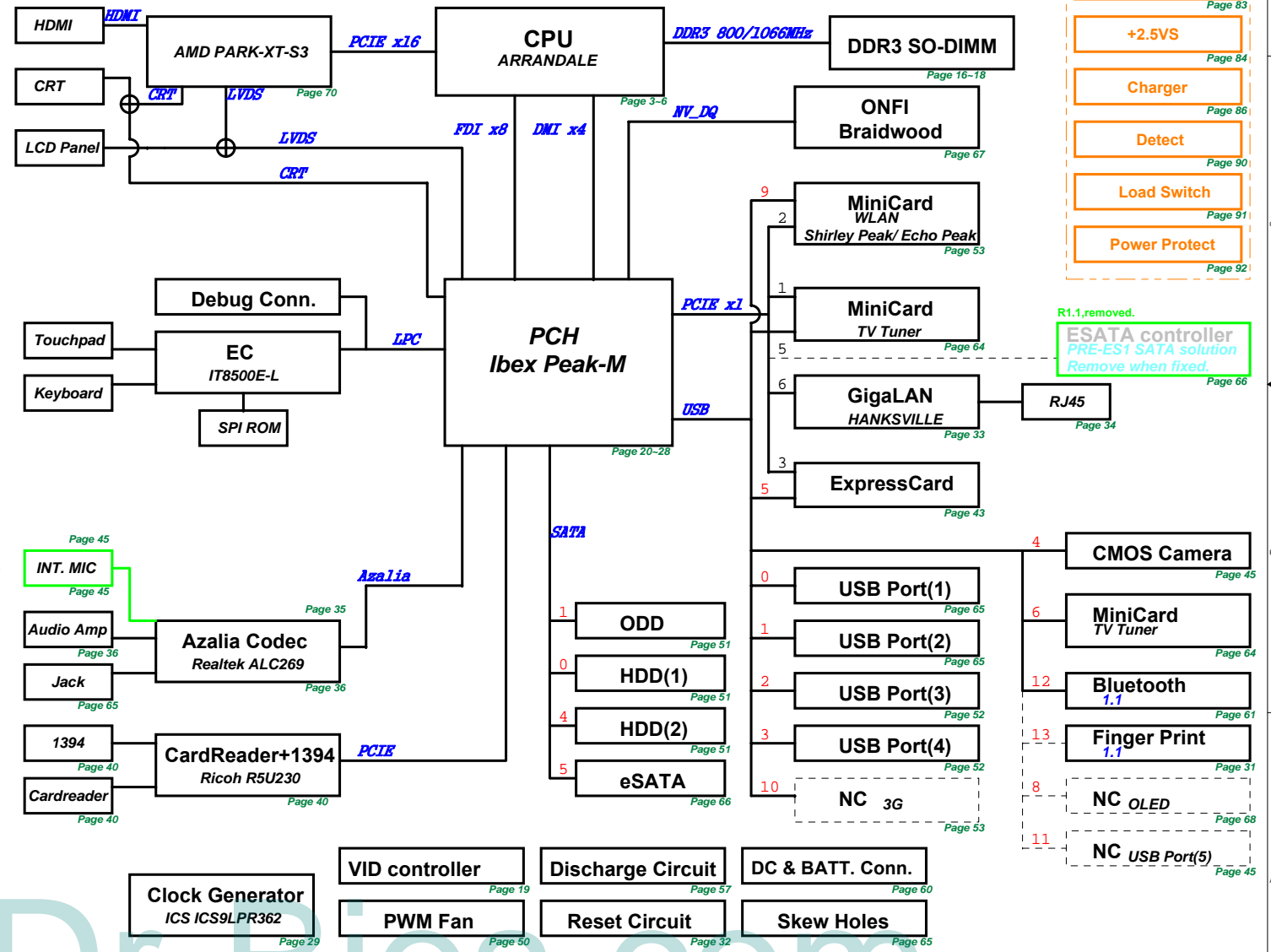


K42F SCHEMATIC For BOM Rev1.0

- 01_Block Diagram
- 02_System Setting
- 03_CPU(1)_DMI, PEG, FDI, CLK, MISC
- 04_CPU(2)_DDR3
- 05_CPU(3)_CFG, GND, Thermal Diode
- 06_CPU(4)_PWR
- 07_CPU(5)_XDP
- 08_DDR3 SO-DIMM_0
- 09_DDR3 SO-DIMM_1
- 10_PCH_SFI_ROM
- 11_PCH_STRAP
- 12_PCH_IBEX(1)_SATA, IHDA, RTC, LPC
- 13_PCH_IBEX(2)_PCIE, CLK, SMB, PEG
- 14_PCH_IBEX(3)_FDI, DMI, SYS_PWR
- 15_PCH_IBEX(4)_DP, LVDS, CRT
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- 49.Power_t1_8VS
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- 55.Power_WGFX_CORE
- 56.Power Control
- 57.Power On Sequence
- 58.Power On Timing--AC mode
- 59.Power On Timing--DC mode

BLOCK DIAGRAM

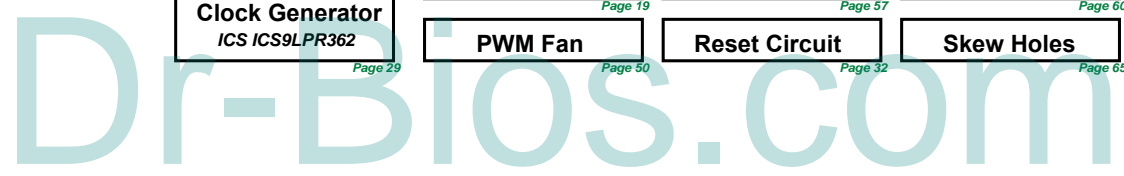


Power

- VCORE Page 80
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- 1.5VS & 1.05VS Page 82
- DDR & VTT Page 83
- +2.5VS Page 84
- Charger Page 86
- Detect Page 90
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- Power Protect Page 92

R1.1, removed.
ESATA controller
 PRE-ES1 SATA solution
 Remove when fixed.

R1.1, added.



PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAYPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	-	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSENT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	-	-	+3VS
GPIO 49	GPO	GPU_RST#	-	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	-	-	+5VS
GPIO 53	GPO	-	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	GPO	-	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU (DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	-	-	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC IT8512

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	CHG_LED#
GPA2	-	-
GPA3	-	-
GPA4	0	LCD_BL_PWM
GPA5	0	FAN0_PWM
GPA6	-	-
GPA7	-	-
GPB0	0	SUSC_EC#
GPB1	0	SUSB_EC#
GPB2	-	-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RC_IN#
GPB7	0	PM_RSMRST#
GPC0	-	-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	-	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	-	-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	-	-
GPE0	0	VSUS_ON
GPE1	0	EGAD (IT8301 Address/Data connect)
GPE2	0	EGCS (IT8301 Cycle Start connect)
GPE3	0	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPFO	-	-
GPF1	-	-
GPF2	I	EXP_GATE#
GPF3	-	-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	0	THRO_CPU
GPF7	-	-
GPFO	-	-
GPB1	I	PM_SUSB#
GPB2	-	-
GPB6	-	-
GPH0	IO	PM_CLKRUN#
GPH1	-	-
GPH2	0	GFX_VR_ON
GPH3	0	BAT_LEARN
GPH4	-	-
GPH5	0	NUM_LED#
GPH6	0	CAP_LED#
GPI0	-	-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6	-	-
GPI7	-	-
GPJ0	0	CPU_VRON
GPJ1	0	PM_PWROK
GPJ2	0	VSET_EC
GPJ3	0	ISET_EC
GPJ4	0	TP_LED
GPJ5	-	-

EC IT8301

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2	-	-
GPIO3	-	-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	O	ME_PWROK
GPIO13	-	-
GPIO14	O	ME_SLP_M_EC#
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
GPIO31	-	-
GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO36	-	-
GPIO37	-	-

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
Clock Generator(IC95LPR362)	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
VID Controller(ASM8272)	0011011x (36)
WiFi/WiMax	N/A
EC Master (SMB1)	
SM-Bus Device	SM-Bus Address
CPU Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

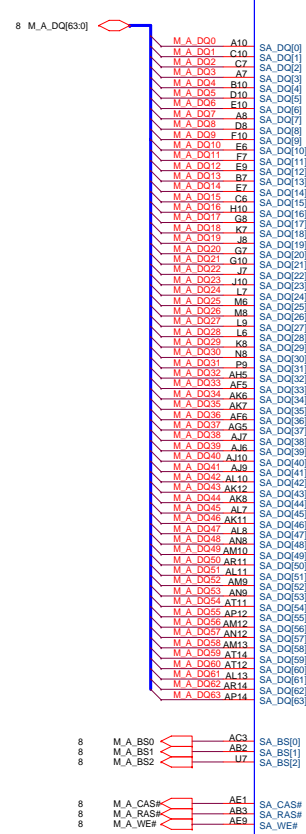
PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	-
PCIE 5	ESATA (for pre-ES1)
PCIE 6	GLAN
PCIE 7	-
PCIE 8	-

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	NewCard
USB 6	Minicard TV Tuner
USB 7	-
USB 8	-
USB 9	WLAN
USB 10	-
USB 11	-
USB 12	Bluetooth
USB 13	Finger Printer

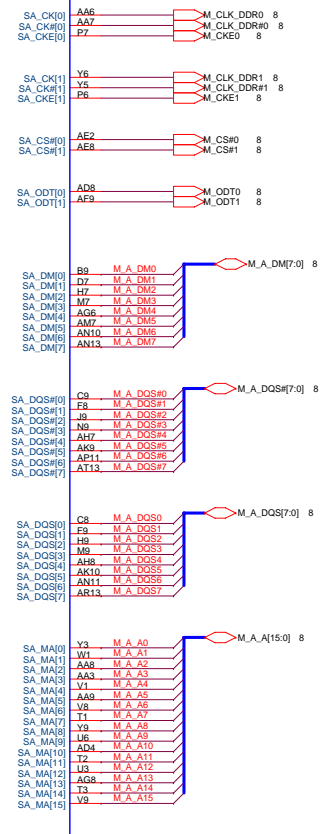
SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

ASUS Title : System Setting
 ASUSTeK COMPUTER INC. NBI Engineer: Modim Zhang
 Size C Project Name K42F Rev 1.0
 Date: Tuesday, November 10, 2009 Sheet 2 of 59

U301C

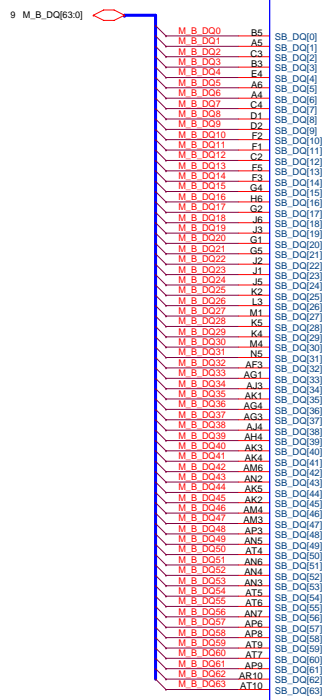


DDR SYSTEM MEMORY - A



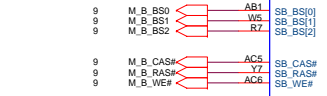
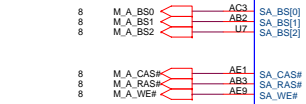
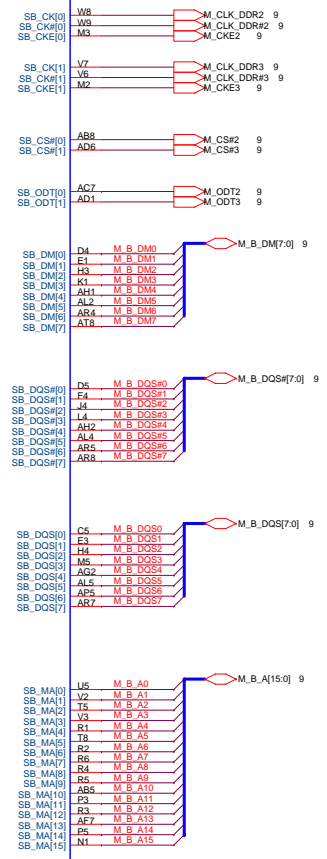
SOCKET989

U301D

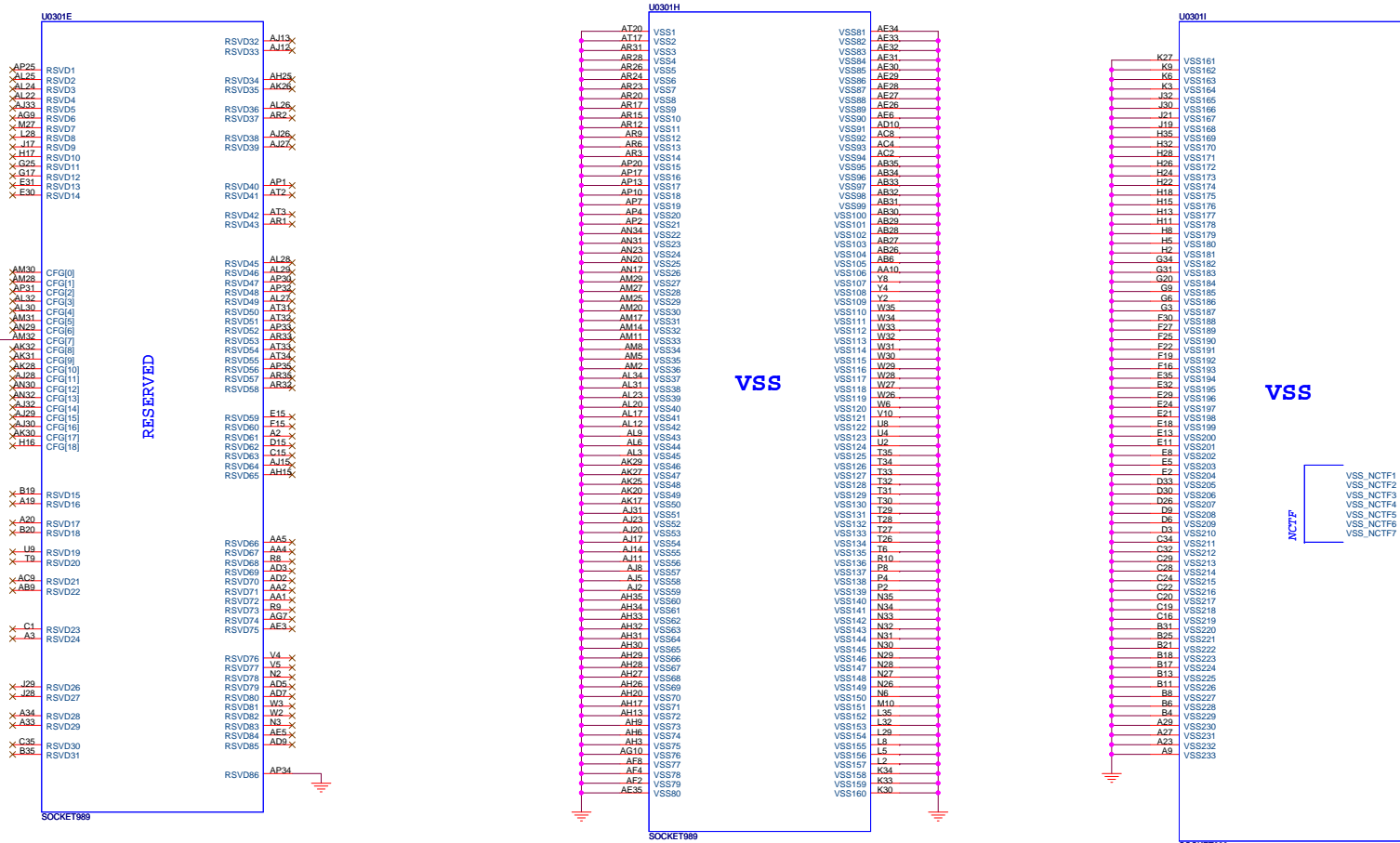


DDR SYSTEM MEMORY - B

SOCKET989



Dr-Bios.com



CFG strapping information:

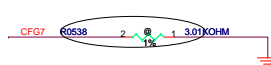
CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
 - 11 = 1 x 16 PEG (Default)
 - 10 = 2 x 8 PEG

CFG[3]: PCIe Static Numbering Lane Reversal.(Arrandale Only)
 - 1: Normal Operation (Default)
 - 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale Only)
 - 1: Disabled - No Physical Display Port attached to Embedded DisplayPort
 - 0: Enabled - An external Display Port device is connected to the Embedded DisplayPort

CFG[7]: Fixed for PCI Express 2.0 (later specifications) (Clarksfield)
 Clarksfield (only for early samples pre-E53) - Connected to GND with 3.01K Ohm/5% resistor for a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburdale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.
 Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.

CFG[3] - PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.

- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.

CFG[17:5] - Reserved configuration pins.

Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifurcation:

- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.

CFG[3] - Reserved (Used by Arrandale Pprocessors for PCI Express* Static Lane Numbering Reversal)

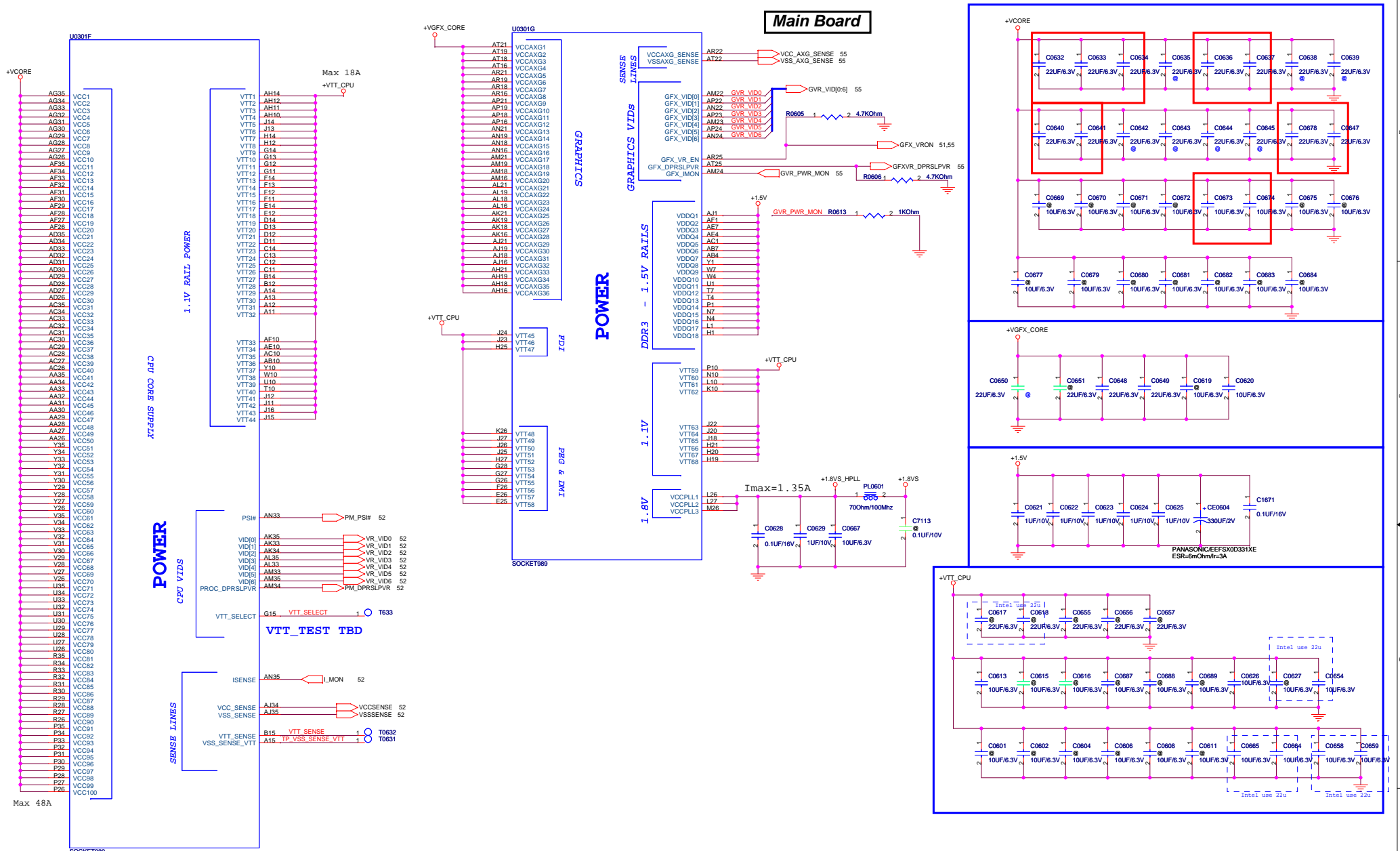
CFG[11:4] - Reserved configuration pins.

CFG[12] - N/A on Clarksfield processors.

CFG[17:13] - Reserved configuration pins.

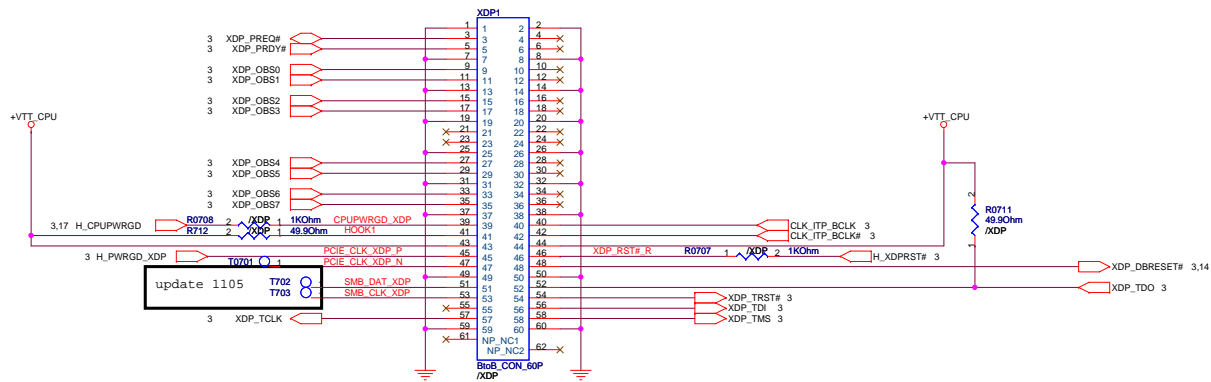
Note: Hardware straps are sampled after RSTIN# de-assertion.

Main Board

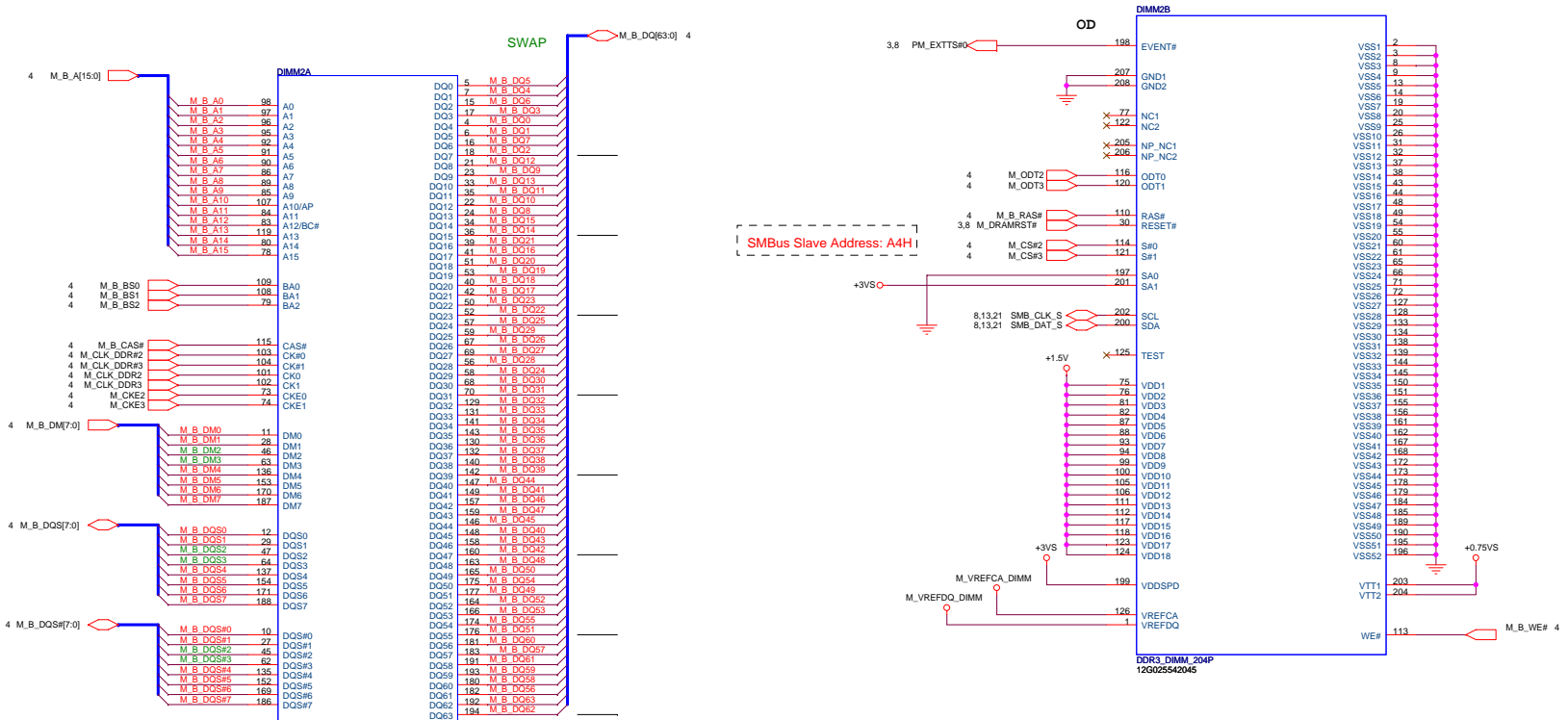


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CPU XDP connector

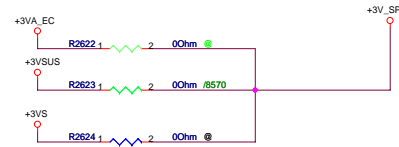


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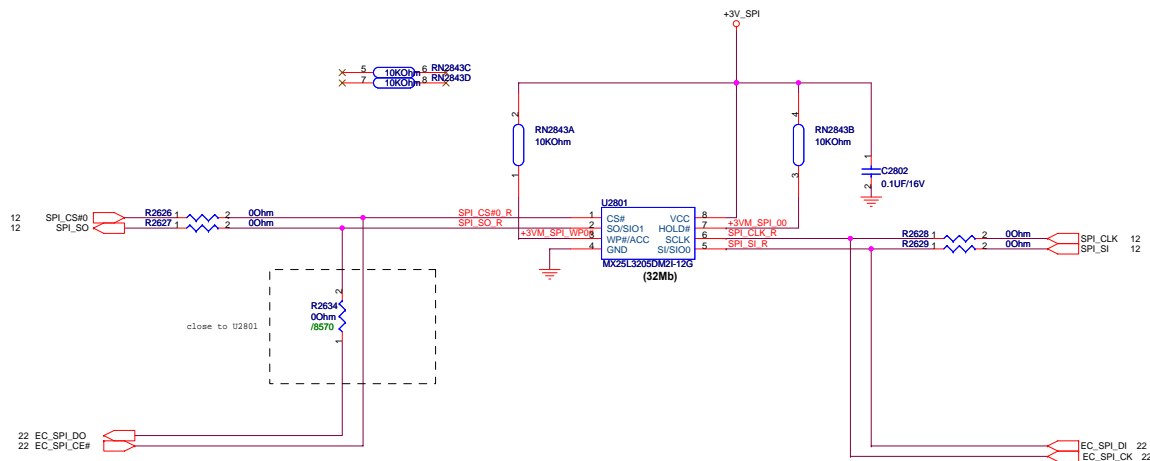


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PCH SPI ROM



PCH SPI ROM



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Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# de-asserts. NOTE: This signal should not be pulled low.
GNT[3]# / GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high.

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment															
GNT1# / GPIO1	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 1). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <table border="1"> <thead> <tr> <th>Bit11</th> <th>Bit 10</th> <th>Boot BIOS Destination</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC, however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	PCI																
1	1	SPI																
0	0	LPC																

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDATA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDATA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

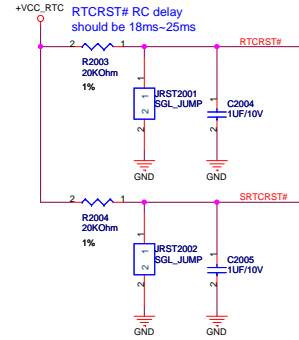
Signal	Usage	When Sampled	Comment															
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <table border="1"> <thead> <tr> <th>Bit11</th> <th>Bit 10</th> <th>Boot BIOS Destination</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC, however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	PCI																
1	1	SPI																
0	0	LPC																
GNT2# / GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.															
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high.															

Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN# / GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/debug environments ONLY. NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDD	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. NOTE: This signal should not be pulled high.
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. NOTE: This signal should not be pulled low.
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYHC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. NOTE: A strong pull up may be needed for GPIO functionality.
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS clear function

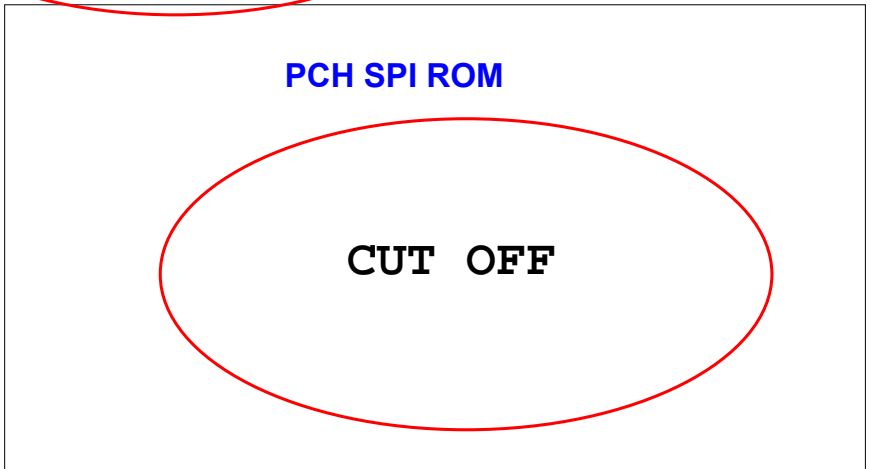
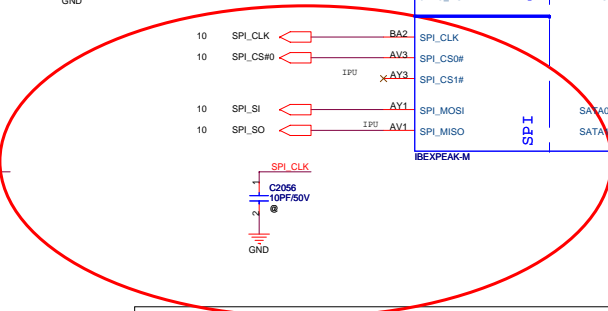
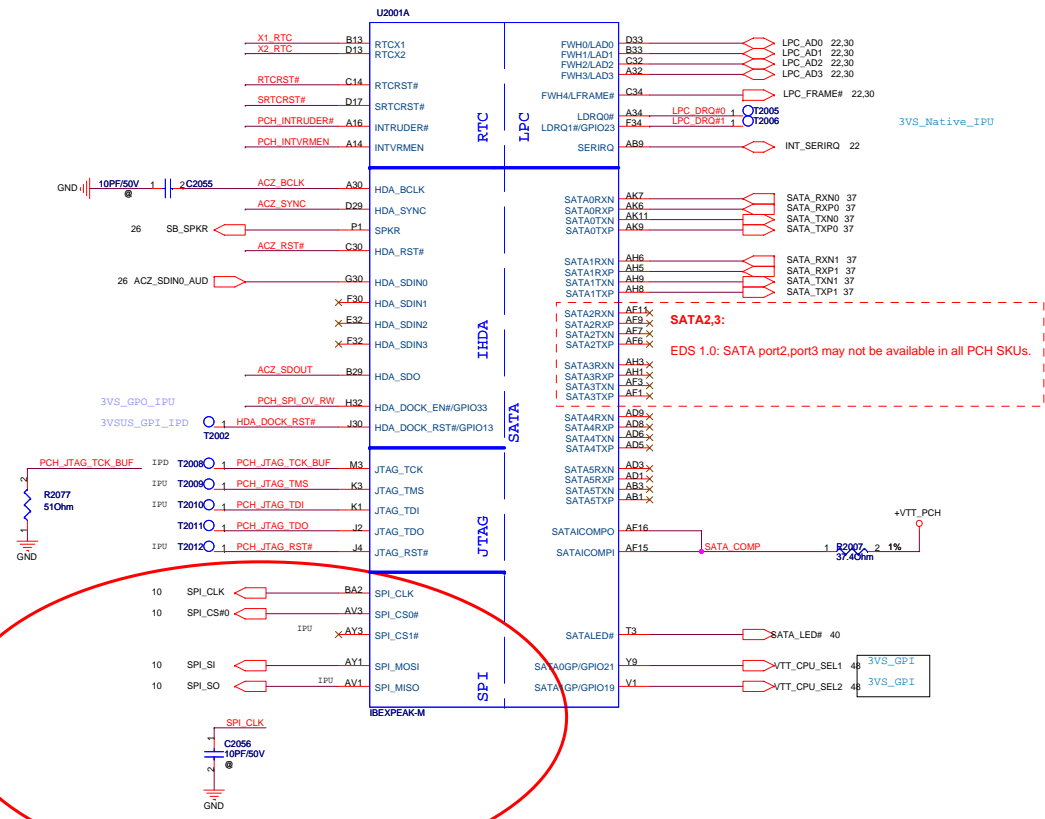
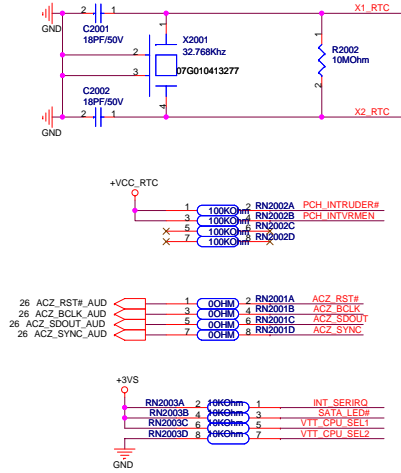
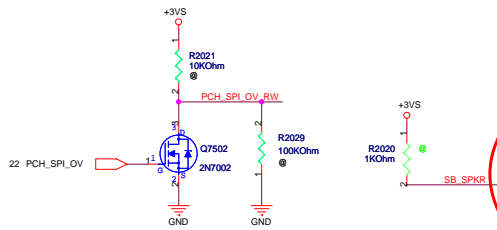
CMOS Settings		JRST2001		TPM Settings		JRST2002	
Clear CMOS	Shunt	Clear ME RTC Registers	Shunt	Clear ME RTC Registers	Shunt	Clear ME RTC Registers	Shunt
Keep CMOS	Open (Default)	Keep ME RTC Registers	Open (Default)	Keep ME RTC Registers	Open (Default)	Keep ME RTC Registers	Open (Default)



DG2.0 P297
RTRCRST# and SRTRCRST# can not be shorted together

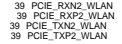
Strap information:

	B	L
ACZ_SYNC: Select VCCVBR 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_SI: ITPW strap. (IPB)	Enable	Disable
PCH_INTVRMEN: Integrated 1.05 V VSM Enable /Disable	Enable	Disable

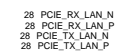


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PCIE2: WLAN



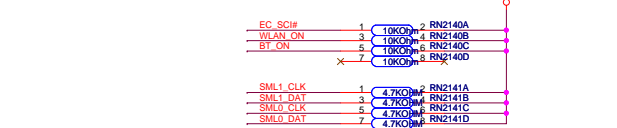
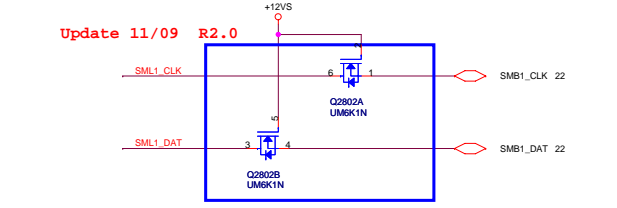
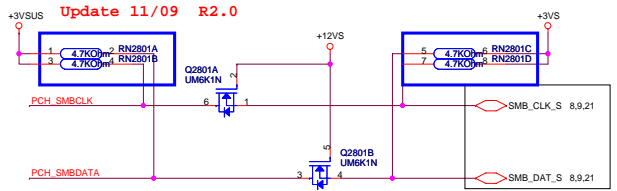
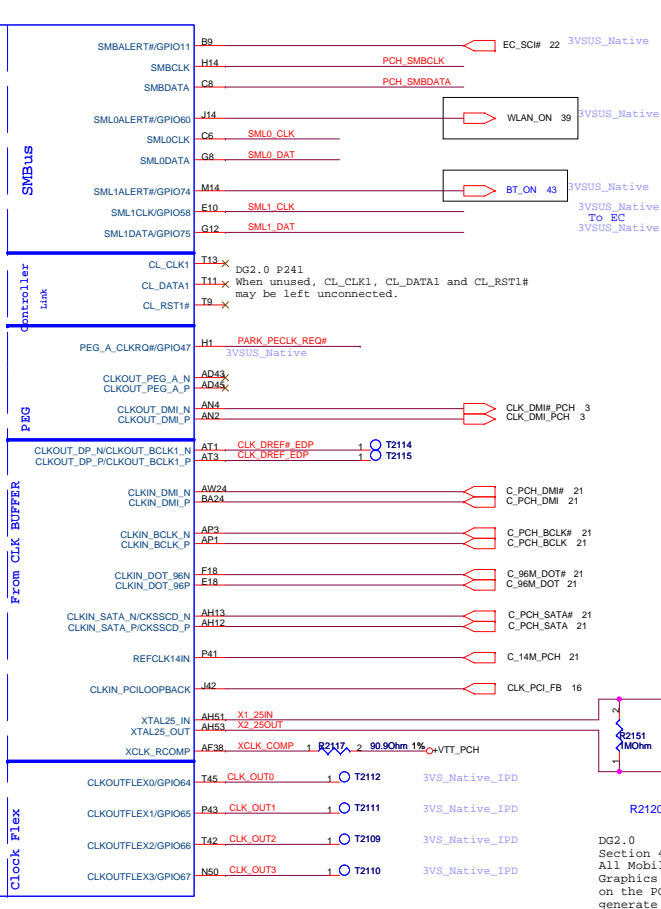
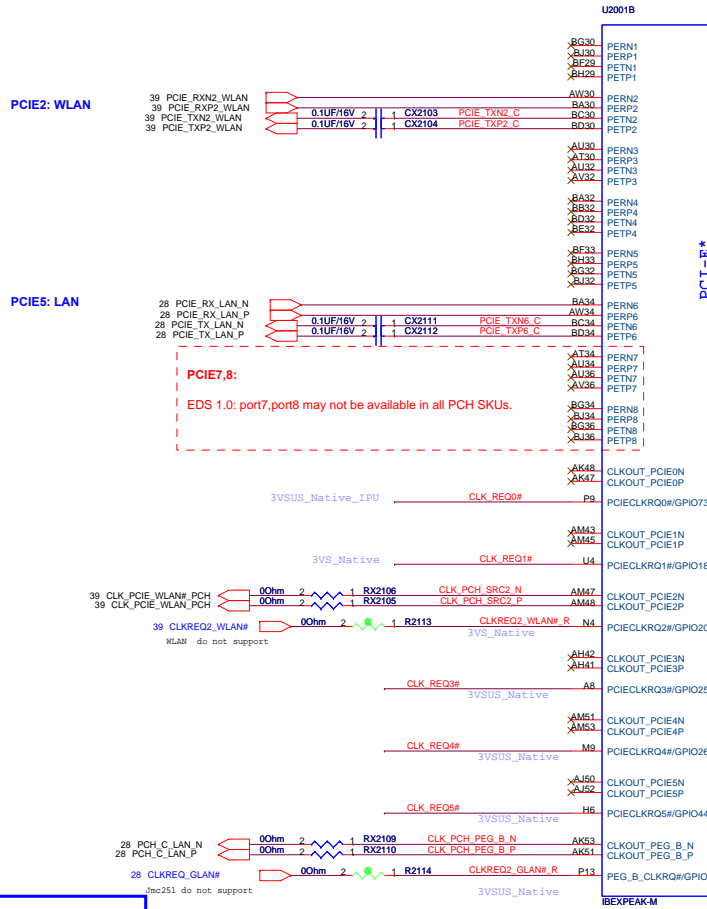
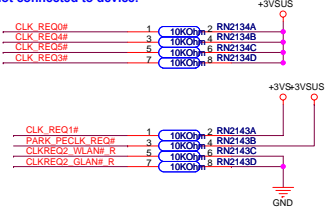
PCIE5: LAN



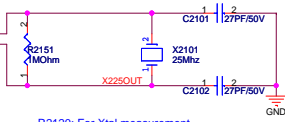
PCIE7,8:
EDS 1.0: port7,port8 may not be available in all PCH SKUs.

Note: Place these resistors near to PCIe Slots

PCH CLKREQ Setting:
Not connected to device.



If not use crystal, please change C1201 to 0 Ohm



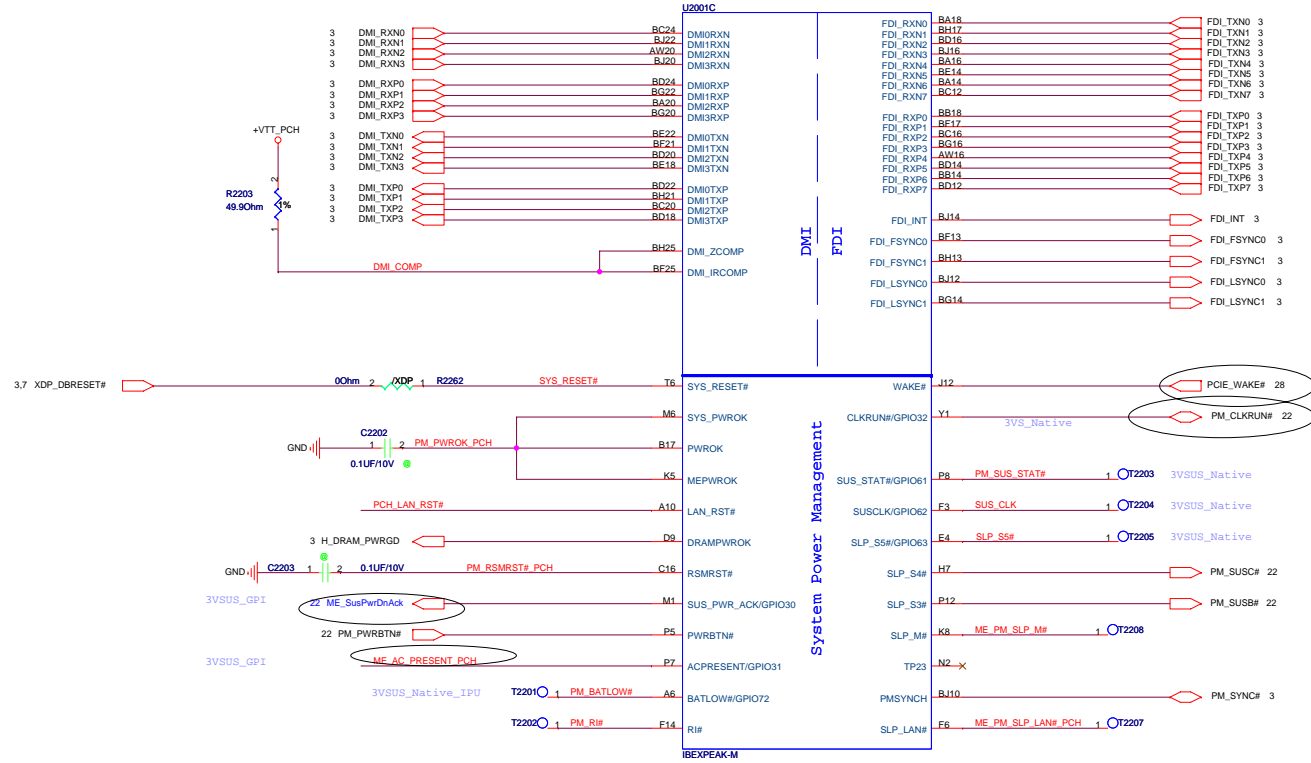
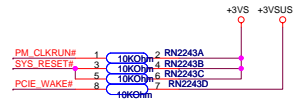
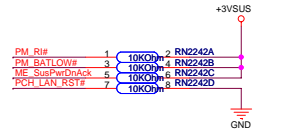
R2120: For Xtal measurement

DG2.0 Section 4.2.4.1: Added 25-MHz Crystal routing guideline. All Mobile Intel 5 Series Chipset-based Integrated Graphics platforms are required to use a 25-MHz crystal on the PCH XTAL25_IN/OUT to enable the PCH to generate the display clocks. Display Clock generation is integrated into the PCH.

Integrated Graphics platforms that implement DVI/DP/HDMI/e-DP are required to use Display Clock Integration (DCI) (25M crystal to generate PCH display clocks) to improve signal integrity and mitigate risk of electrical compliance and associated functional failures

WW35 Update: Integrated Graphics platforms that use only iVDS and/or VGA Displays may use Buffer Through Mode (BTM) and leave 25-MHz crystal and RC components unattached

pre-ES1 not support
Reversal Feature



R1.1,item L15

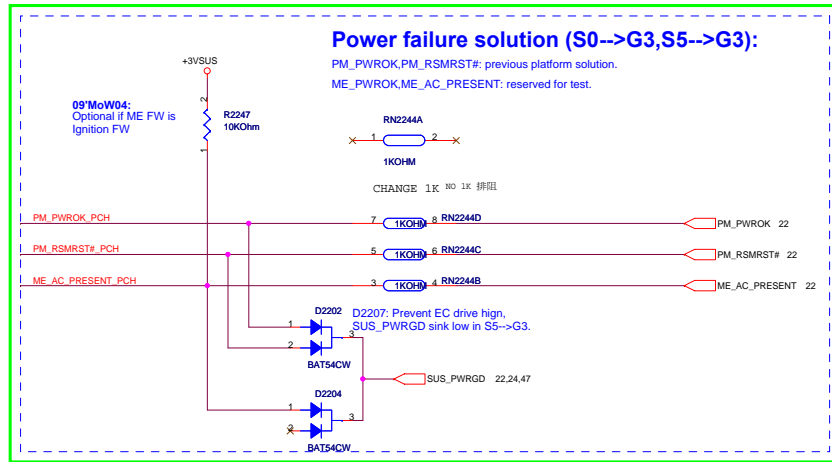


Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AHT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required Note: Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) Notes: If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required Note: If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective.

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.

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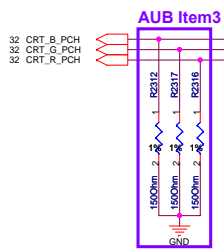
LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
 LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
 LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
 L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
 LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

VccALVDS, VccTX_LVDS



CRT Disable: (For discrete graphic)

1. NC:

CRT_RED, CRT_GREEN, CRT_BLUE
 CRT_HSYNC, CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

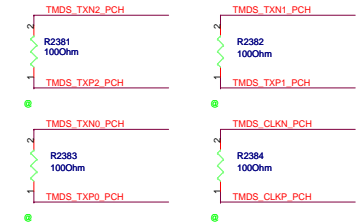
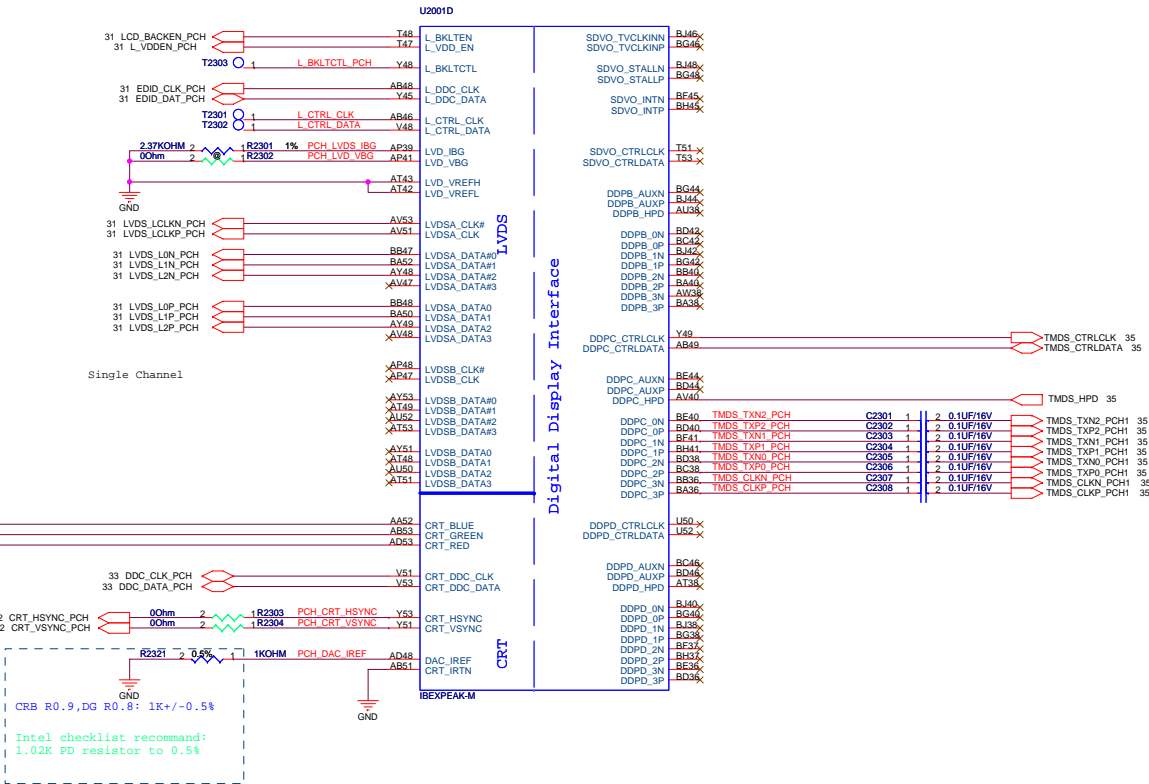
DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

VCCADAC



U2001E

xH40 AD0
 xN44 AD1
 xC44 AD2
 xA38 AD3
 xC36 AD4
 xJ34 AD5
 xA46 AD6
 xA46 AD7
 xE36 AD8
 xH48 AD9
 xE40 AD10
 xC40 AD11
 xM48 AD12
 xM45 AD13
 xF40 AD14
 xM40 AD15
 xA40 AD16
 xJ40 AD17
 xK48 AD18
 xF40 AD19
 xC42 AD20
 xK46 AD21
 xM51 AD22
 xJ52 AD23
 xK41 AD24
 xL34 AD25
 xF42 AD26
 xJ40 AD27
 xG46 AD28
 xF44 AD29
 xM47 AD30
 xH36 AD31
 xJ40 C/BE0#
 xC42 C/BE1#
 xH47 C/BE2#
 xG34 C/BE3#

NVRAM

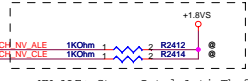
PCI

USB

NV_CE10 AY3#
 NV_CE11 BD1#
 NV_CE12 AE1#
 NV_CE13 BDB#
 NV_DQ00 AV3#
 NV_DQ01 BQ6#
 NV_DQ02V_J00 AP7#
 NV_DQ1NV_J01 APE#
 NV_DQ2NV_J02 ATE#
 NV_DQ3NV_J03 ABE#
 NV_DQ4NV_J04 ABE#
 NV_DQ5NV_J05 AVE#
 NV_DQ6NV_J06 ABE#
 NV_DQ7NV_J07 BA4#
 NV_DQ8NV_J08 ABE#
 NV_DQ9NV_J09 ABE#
 NV_DQ10NV_J10 ABE#
 NV_DQ11NV_J11 ABE#
 NV_DQ12NV_J12 ABE#
 NV_DQ13NV_J13 ABE#
 NV_DQ14NV_J14 ABE#
 NV_DQ15NV_J15 ABE#

Strap information:

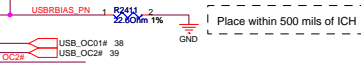
	H	L
PCH/NV_ALE# Strap Intel Anti-Theft Technology HDD Data Protection Enable	ENABLE	DISABLE
NV_CLE# Strap DMI Termination Voltage		



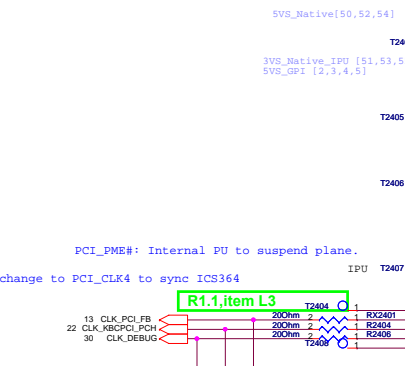
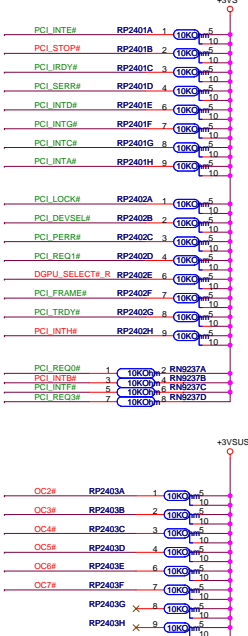
NV_ALE: Strap Intel Anti-Theft Technology HDD Data Protection Enable. (H: enable)
 NV_CLE: Strap DMI Termination voltage

NV_RC0MP# AU2#
 NV_RB# AVZ#
 NV_WR0_RE# AV2#
 NV_WR1_RE# AX#
 NV_WEB_CK0 AV11#
 NV_WEB_CK1 BE#

K82JR	Recommend settings
0	USB port
1	USB port
2	USB port
3	USB port
4	WiFi/WiMax
5	
6	
7	
8	
9	Camera
10	
11	
12	BT (1.1)
13	



3VSUS_Native [9,10,14,40,41,42,43,59]



GNT0#,GNT1#: Boot BIOS Strap.

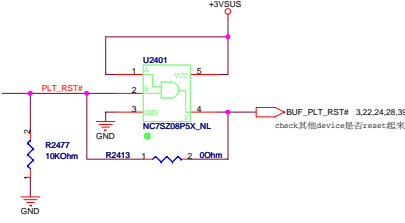
Boot BIOS Strap		Boot BIOS Location
PCI_GNT1#	PCI_GNT0#	
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

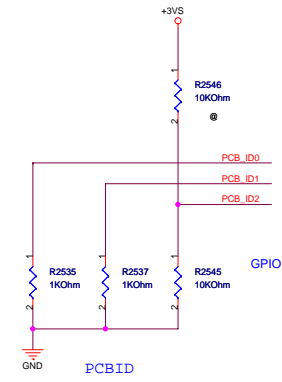
Sampled on rising edge of PWROK.

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

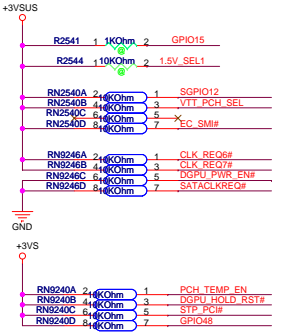
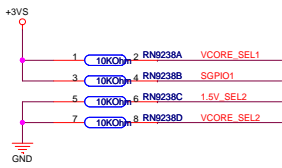
Low=Enabled A16 swap override/ Top-Block swap override

High=Default



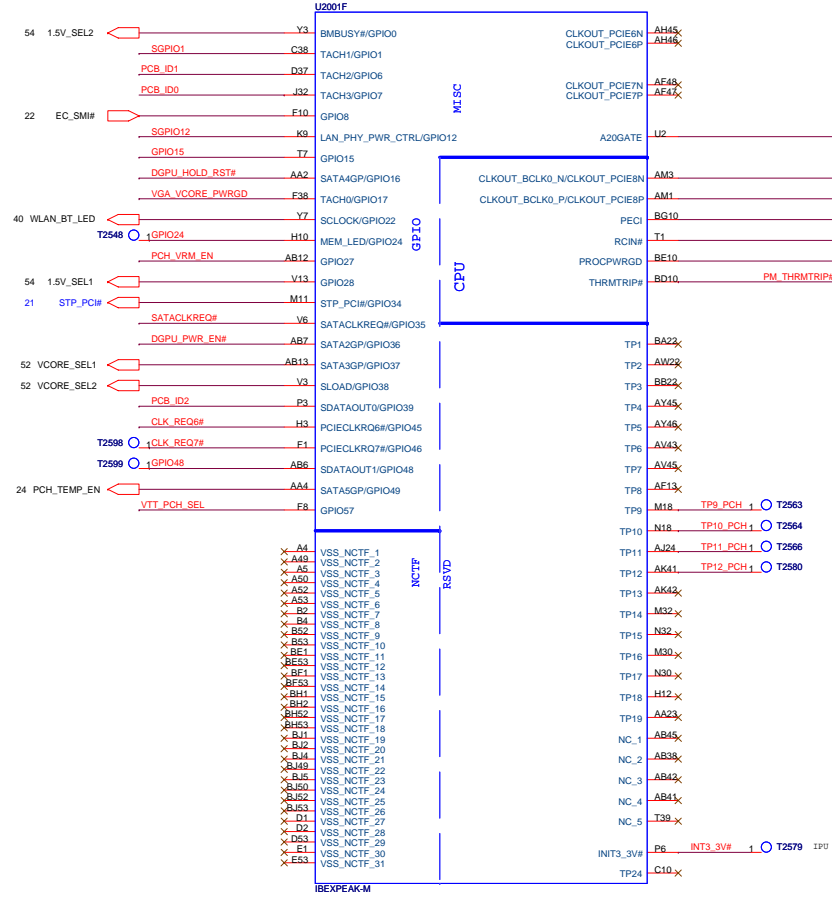


GPIO 27.Enable VCCVRM.Low=disable.
Default internal pull up.

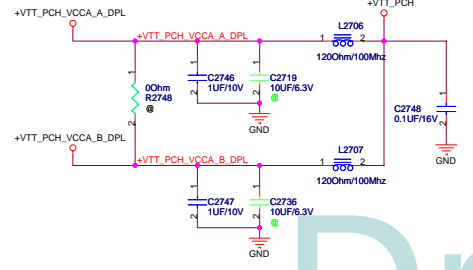
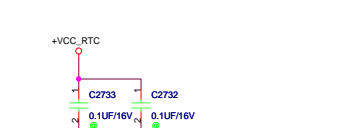
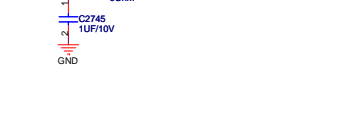
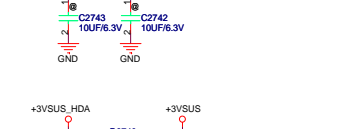
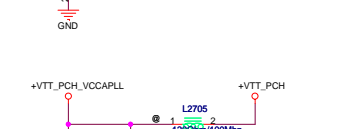
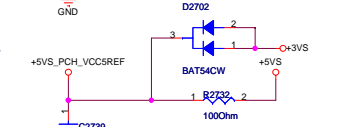
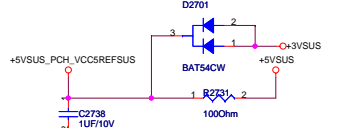
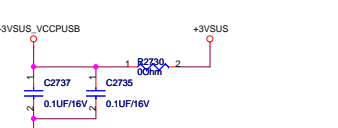
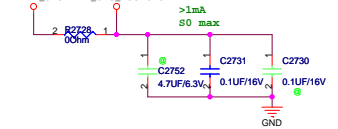
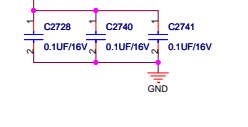
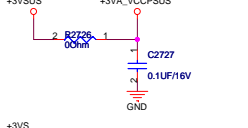
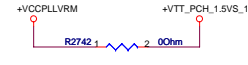
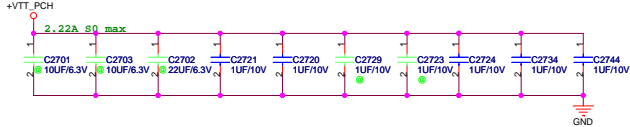
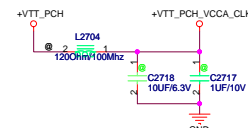
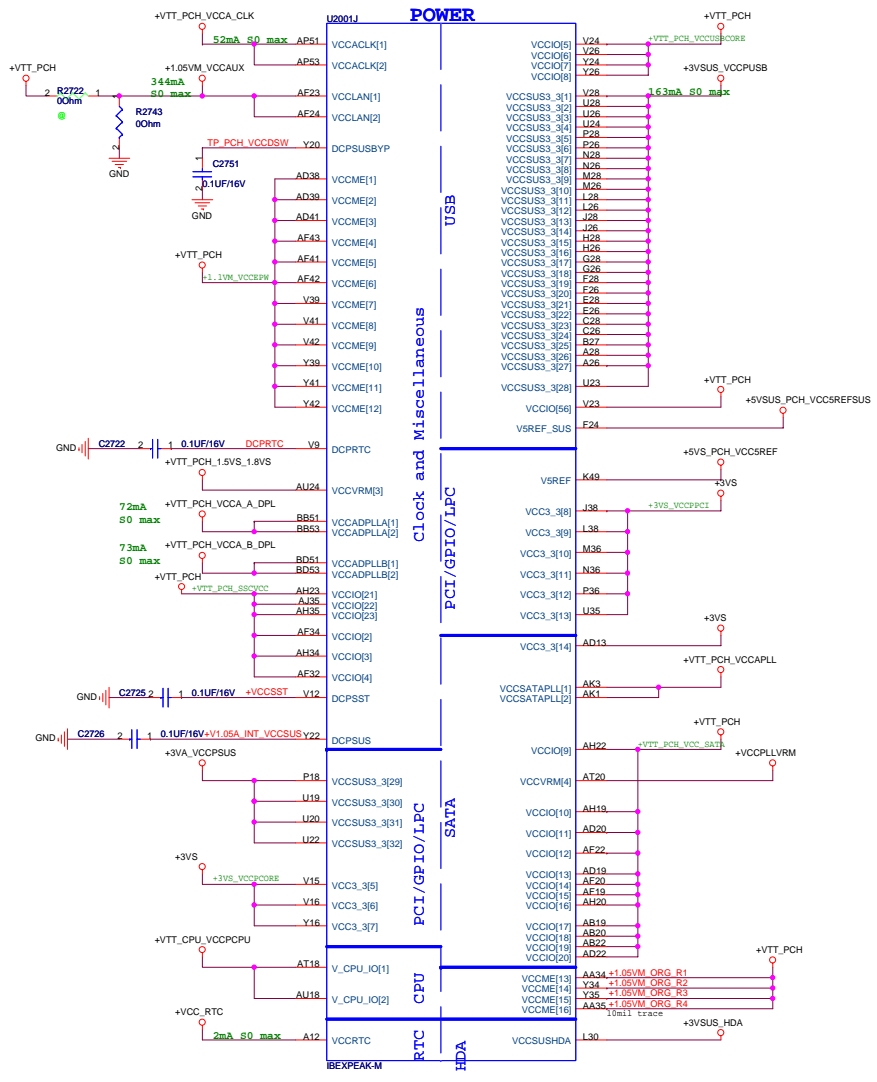


POWER按照提供的default 值調節電壓

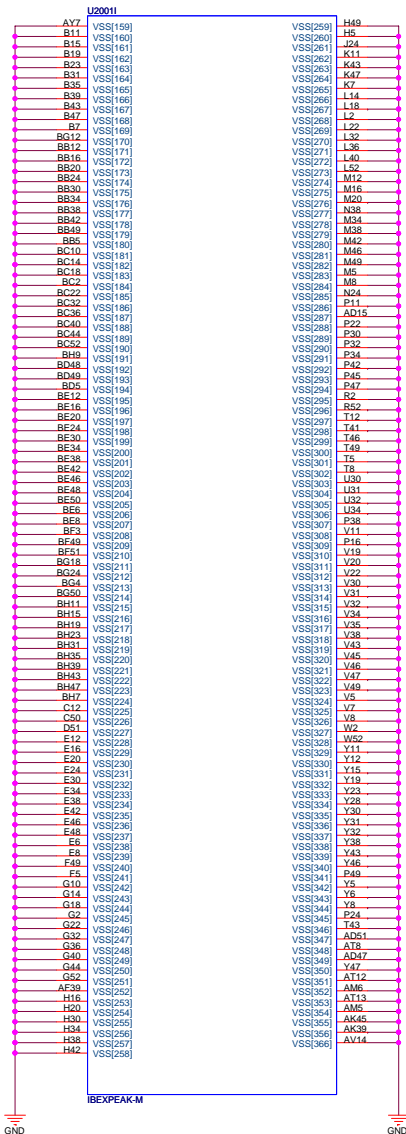
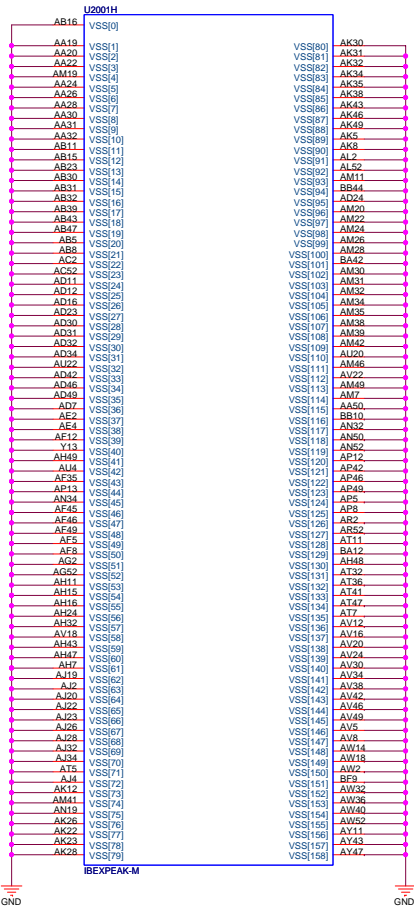
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- 3VS_GP1_I1PU
- 3VS_GP1_I2PU
- 3VS_GP1_I3PU
- 3VSUS_GPO_I1PU
- 3VSUS_GP1
- 3VSUS_GPO_I1PD
- 3VSUS_GP1
- 3VSUS_GPO
- 3VSUS_GPO_I1PU
- 3VSUS_GP1_I1PU
- 3VSUS_GP1
- 3VSUS_GPO
- 3VSUS_GPO_I1PU
- 3VSUS_GP1
- 3VSUS_GPO
- 3VSUS_GPO_I1PU
- 3VSUS_Native
- 3VSUS_Native
- 3VSUS_GP1
- 3VSUS_GP1
- 3VSUS_GP1
- 3VSUS_Native_TPU
- 3VSUS_Native
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- 3VSUS_GP1
- 3VSUS_GP1



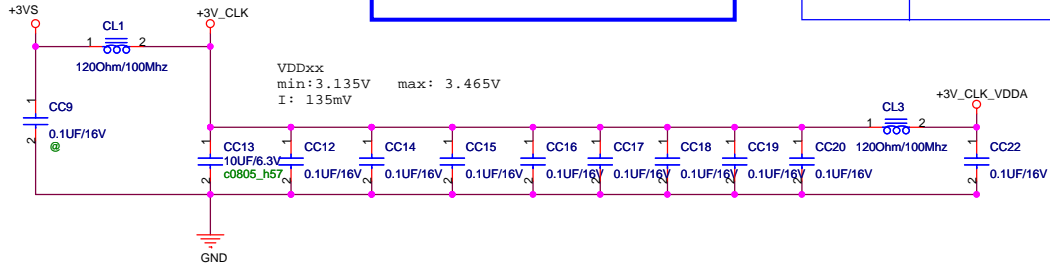
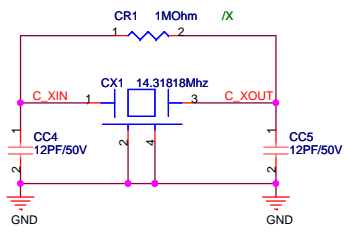
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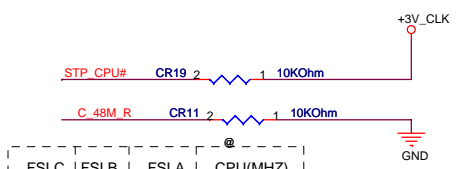
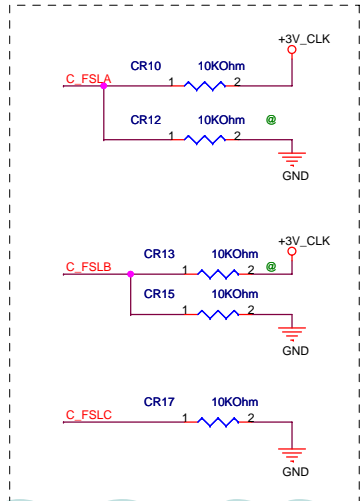
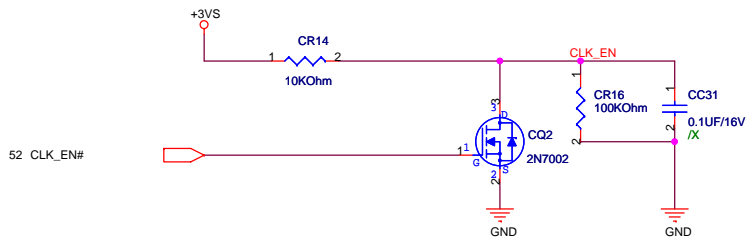
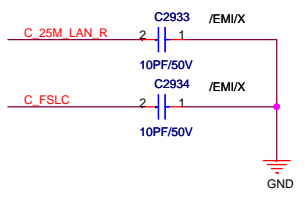
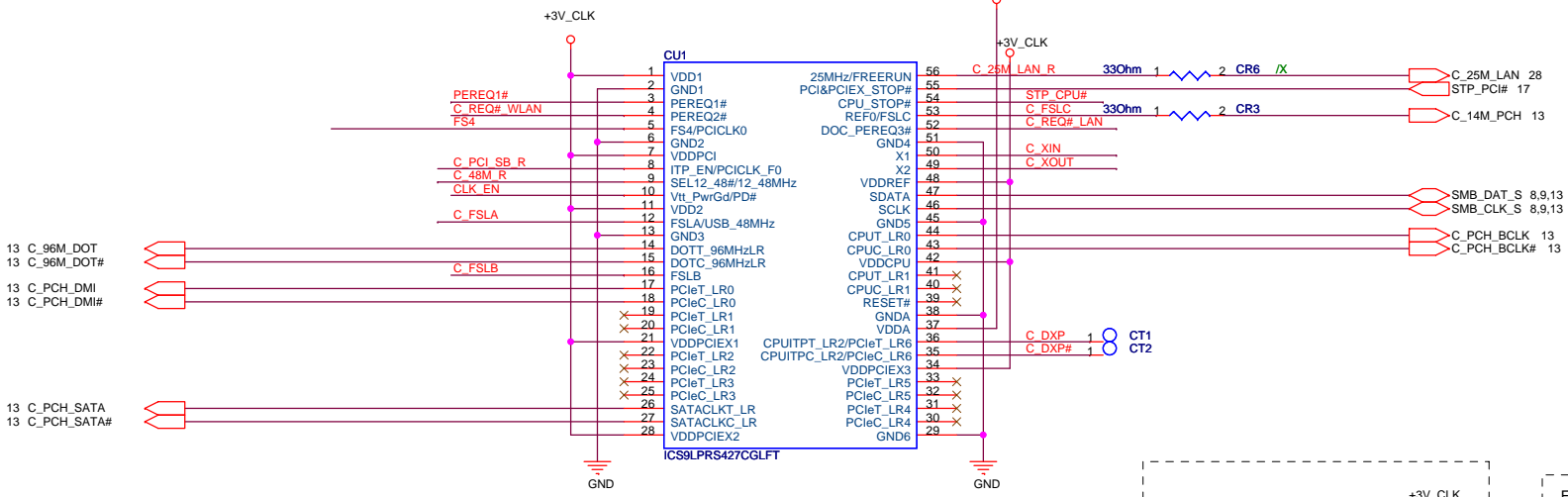
Dr-Bios.com



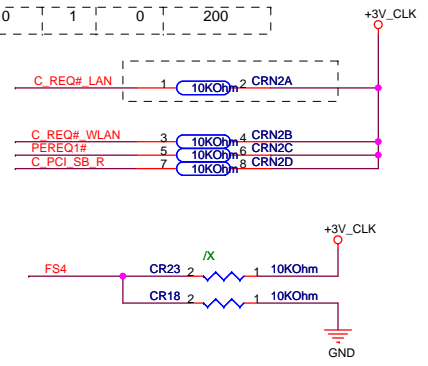
1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

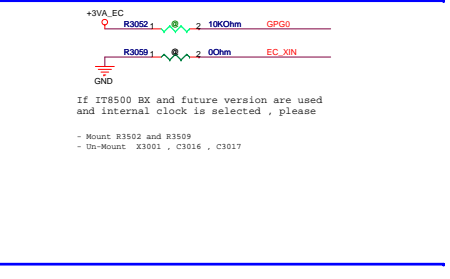
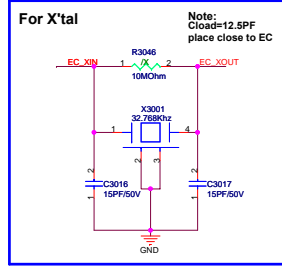
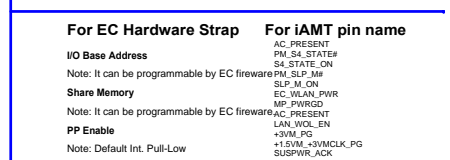
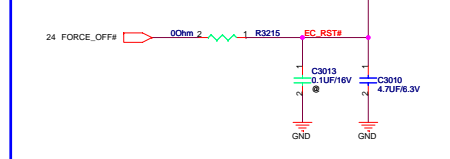
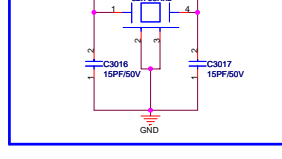
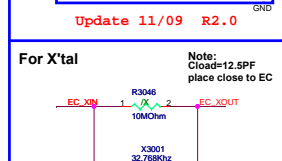
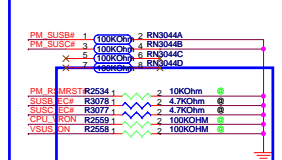
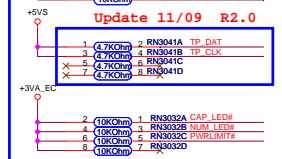
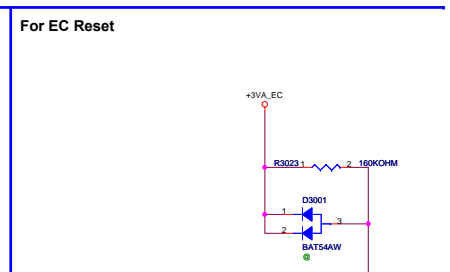
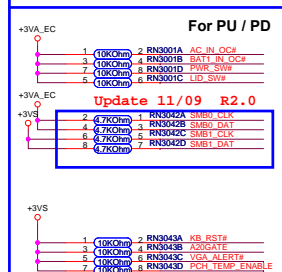
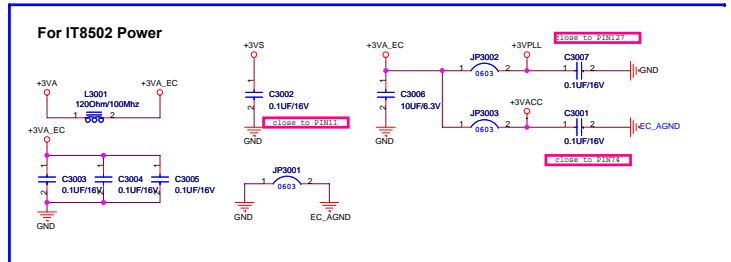
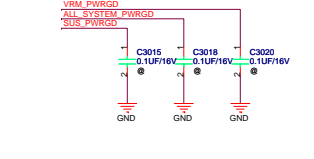
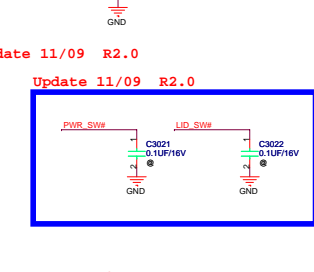
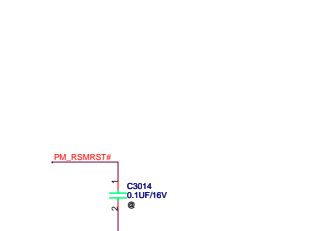
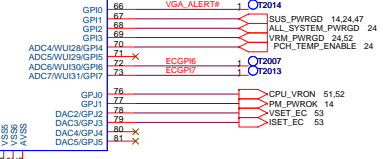
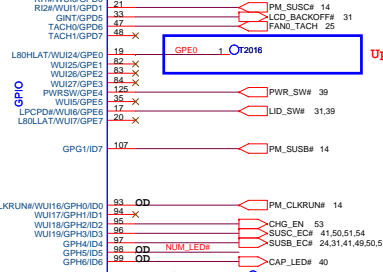
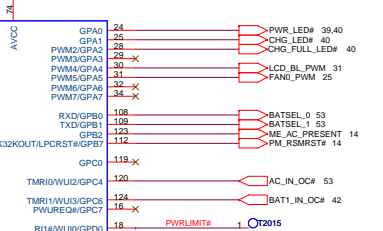
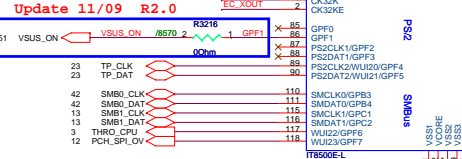
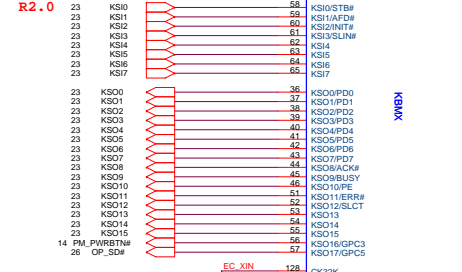
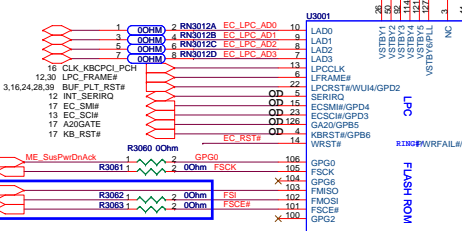
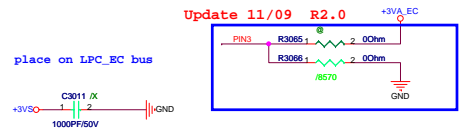
FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)



FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133
0	1	0	200

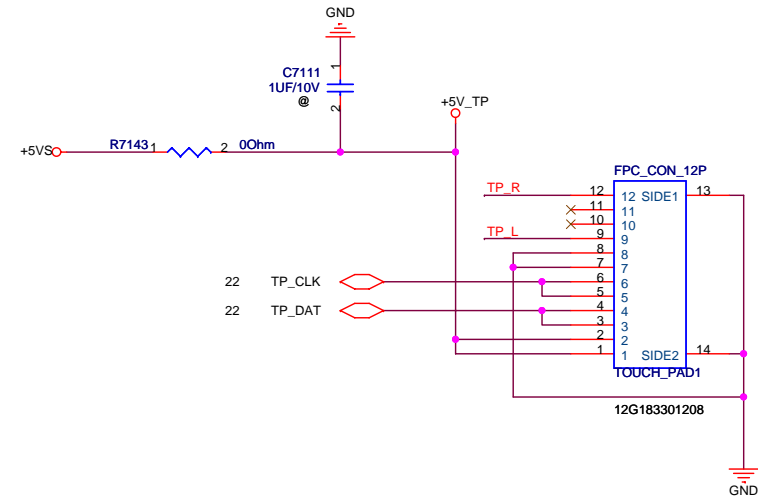
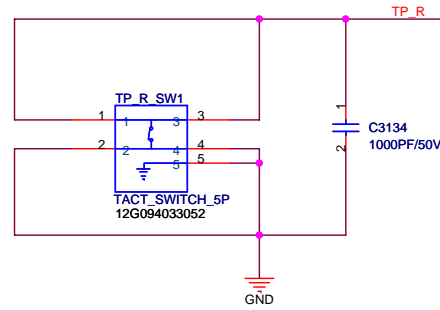
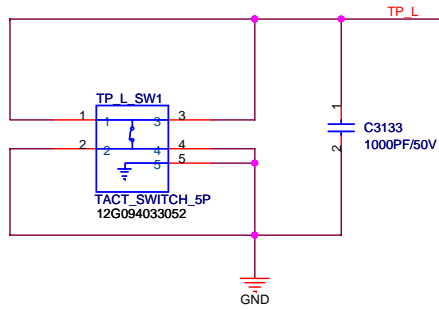


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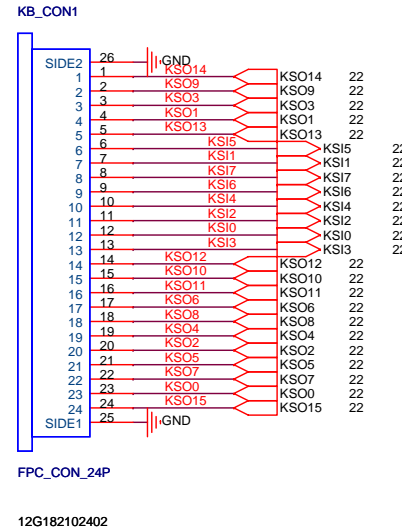


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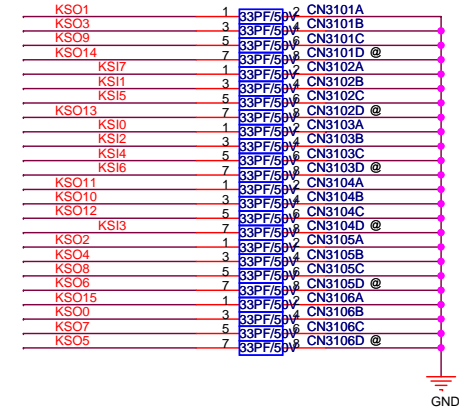
TouchPad



Keyboard Connector



EMI Request



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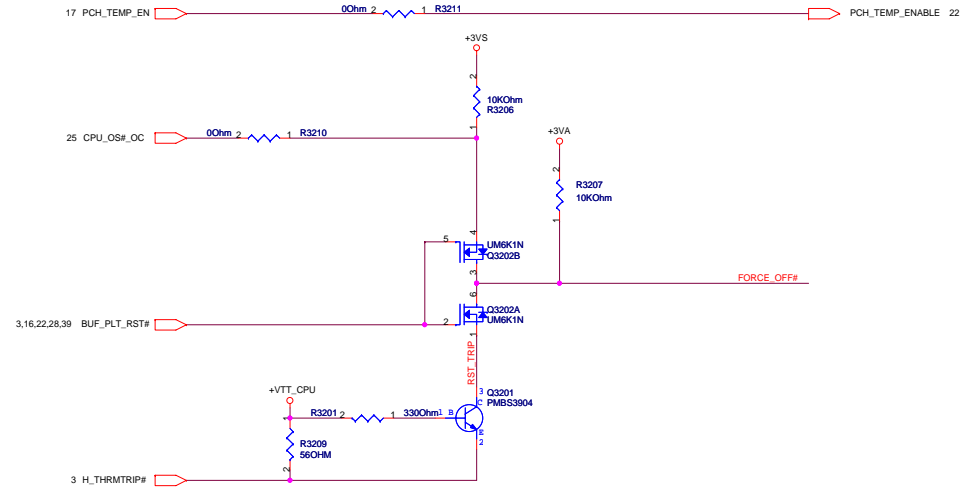
<Variant Name>

Thermal Policy

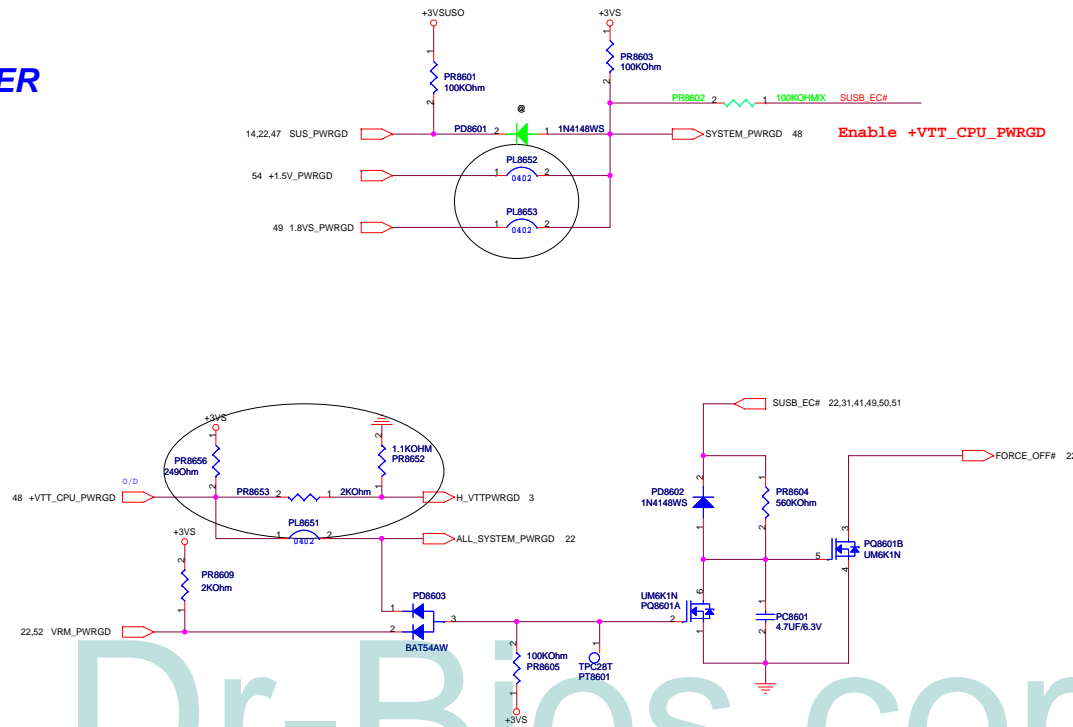
Input 1(sensor)

Input 2(thermtrip)

Output (shut down)



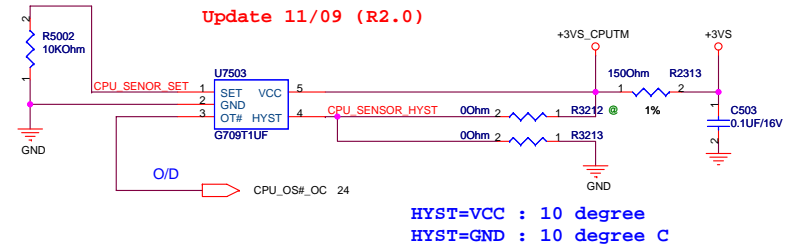
POWER GOOD DETECTOR



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GPU Thermal Sensor

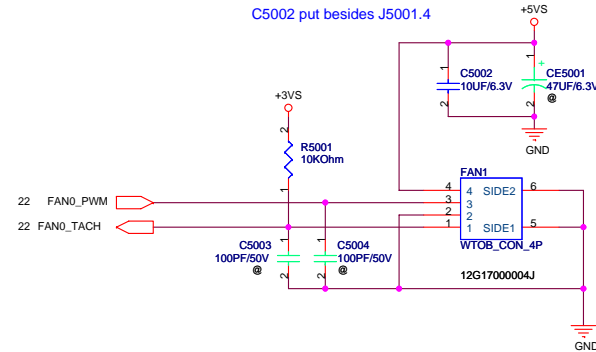
CPU Thermal Sensor



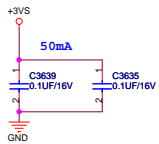
U7503 under CPU socket

PWM Fan

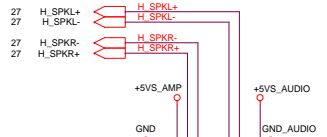
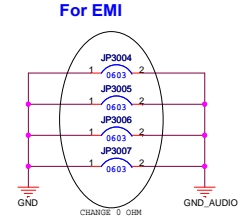
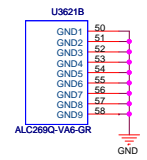
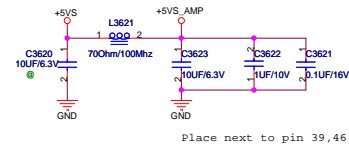
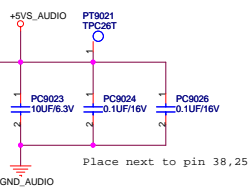
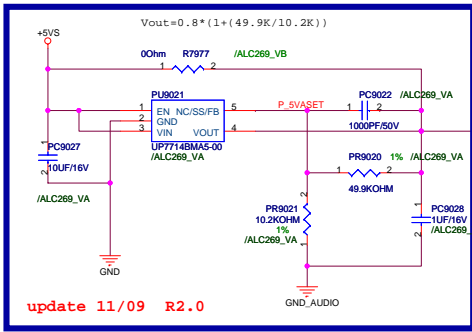
Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.



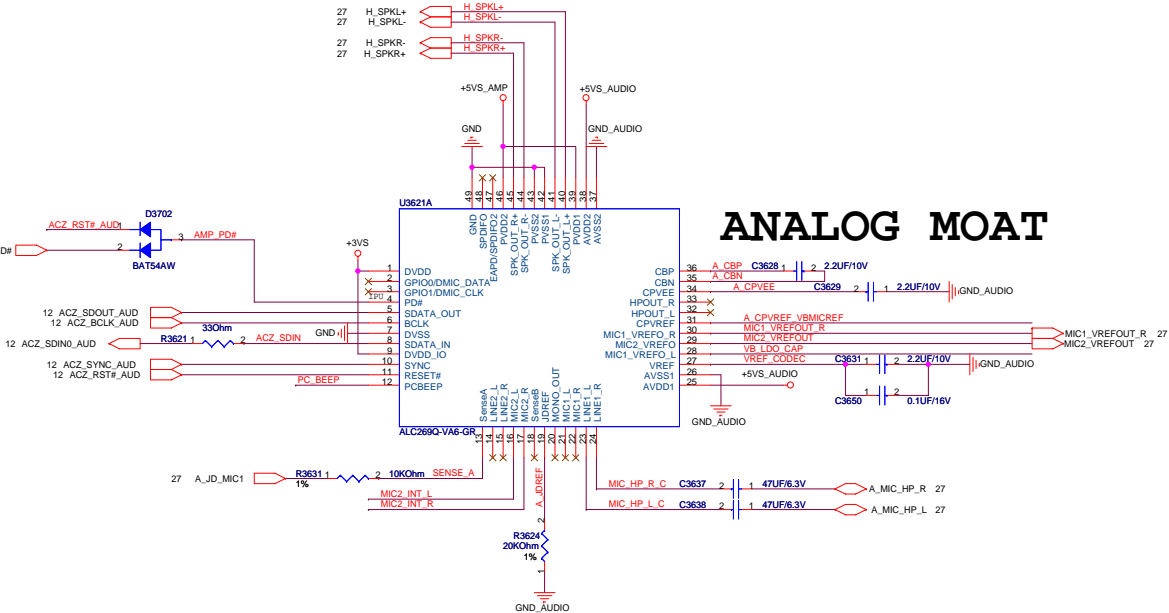
ASUS		Title : AR8131	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	K42F	1.0	
Date: Thursday, November 12, 2009		Sheet	25 of 59



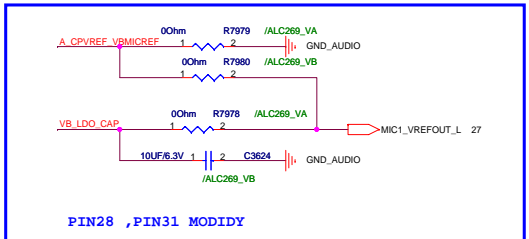
Close to pin1,9



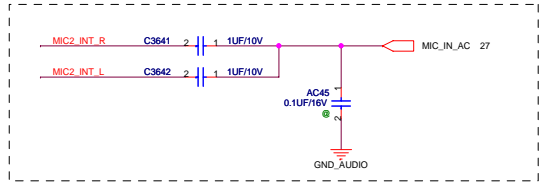
ANALOG MOAT



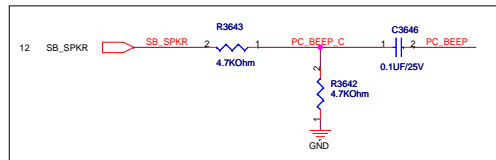
update 11/09 R2.0



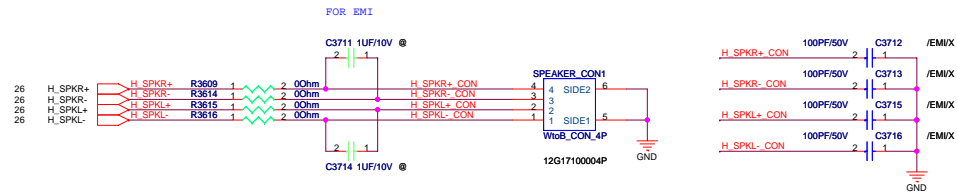
INTERNAL MIC



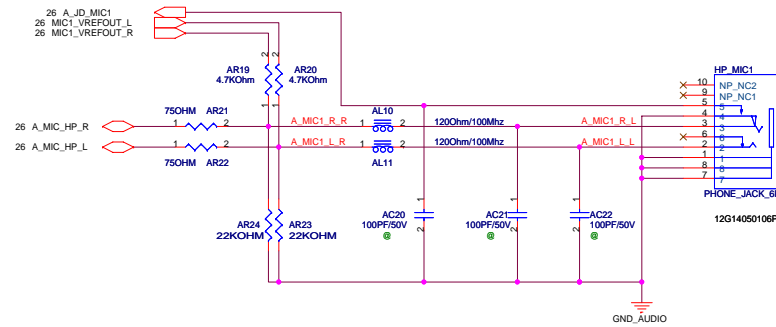
PC BEEP



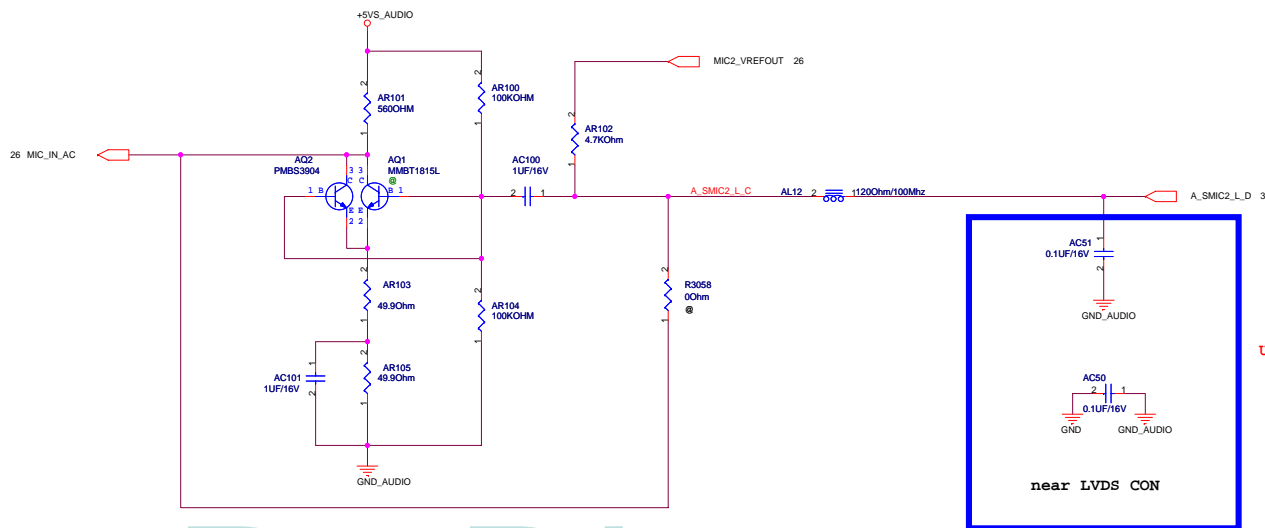
SPEAKER



HP and MIC

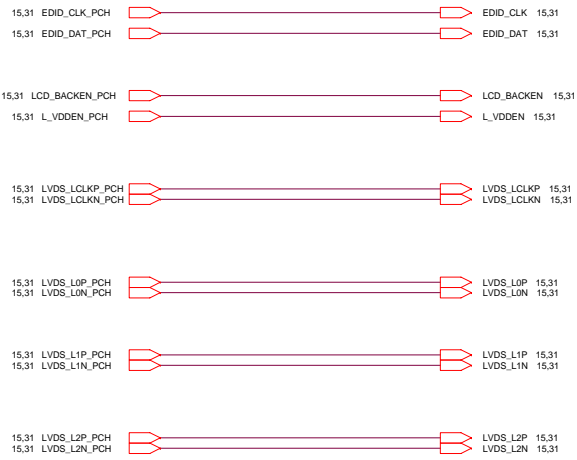


Internal MIC and AMP



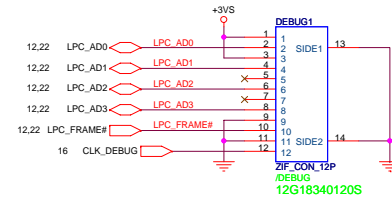
Update 11/09 R2.0

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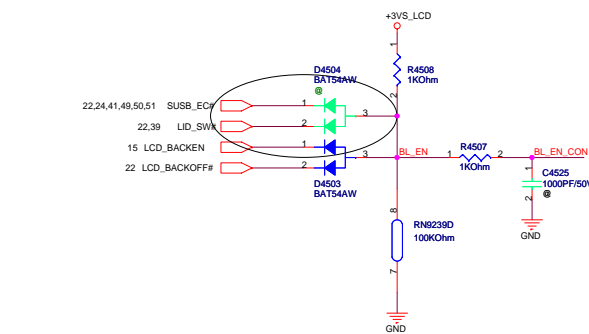
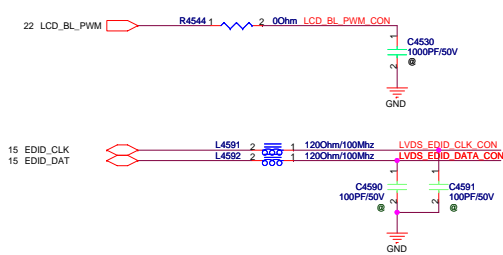
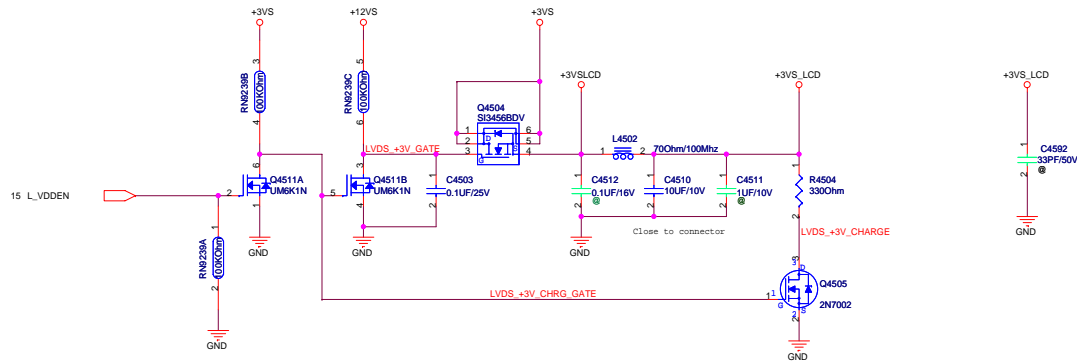


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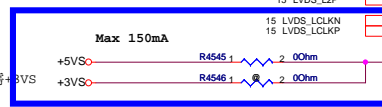
LPC Debug Port



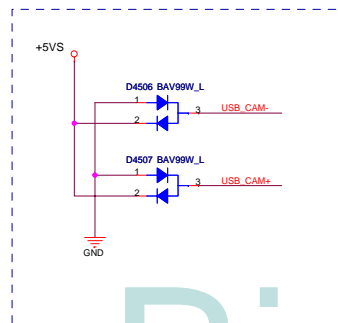
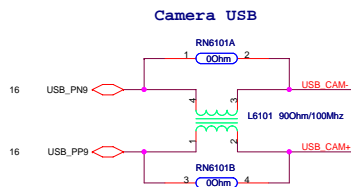
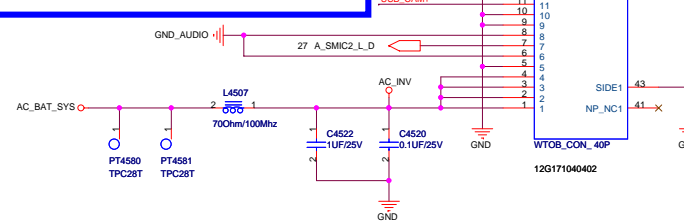
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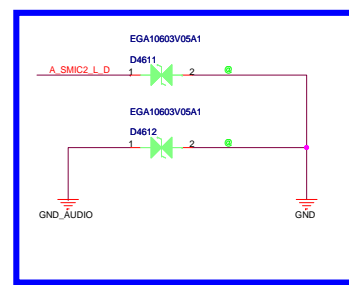
update 11/09 r2.0



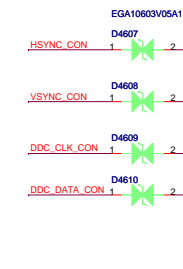
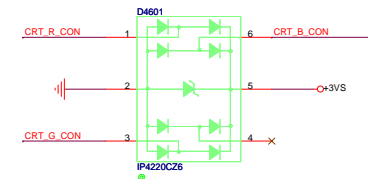
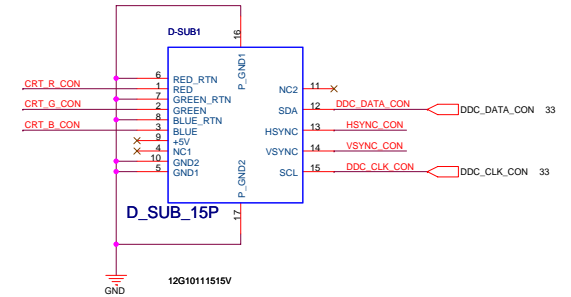
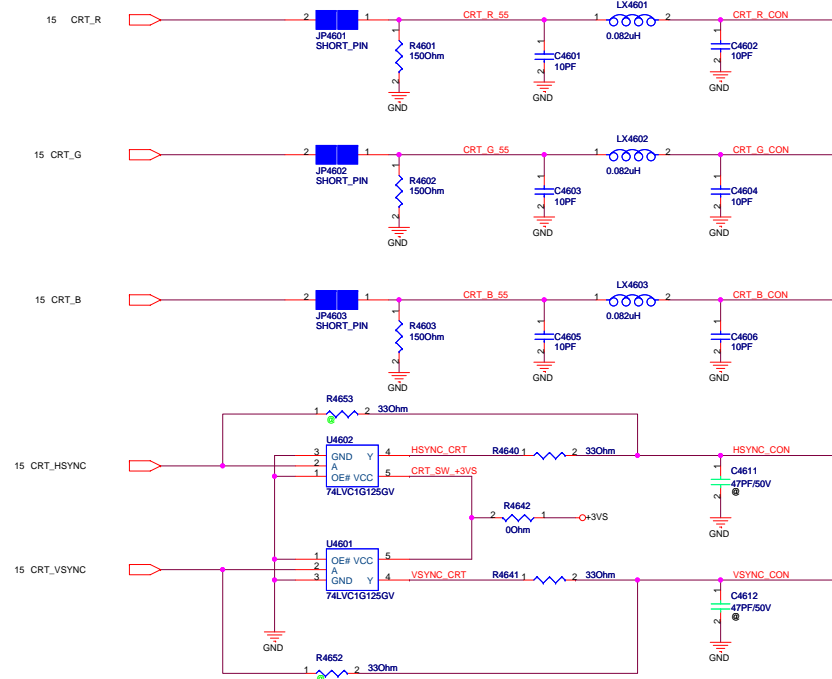
CNF9059 Camera 導入需



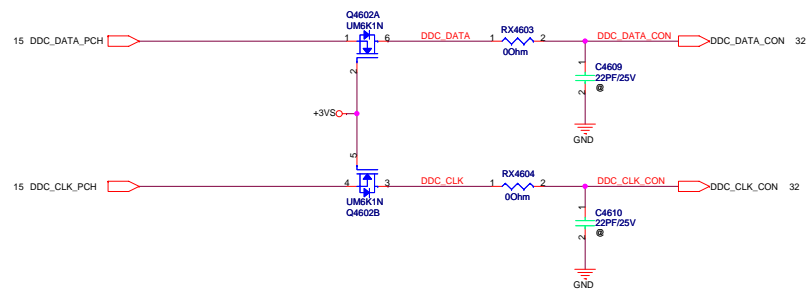
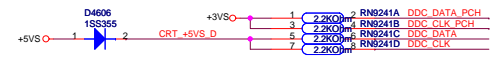
update 11/09 r2.0



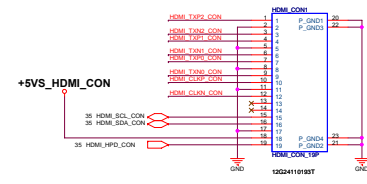
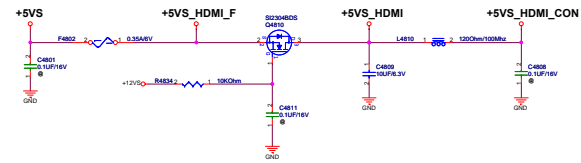
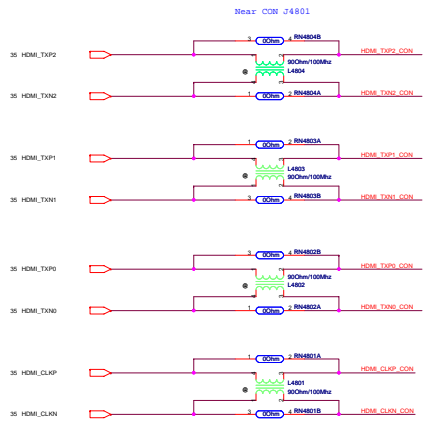
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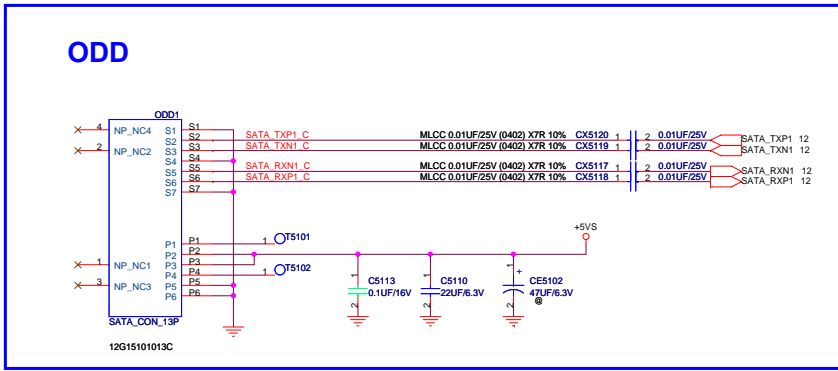
Dr-Bios.com



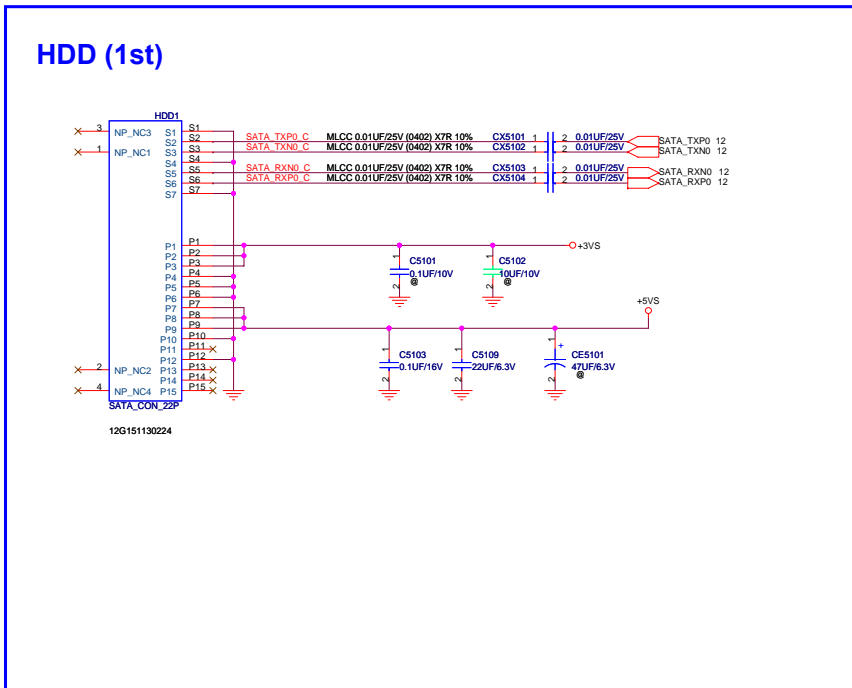


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ODD

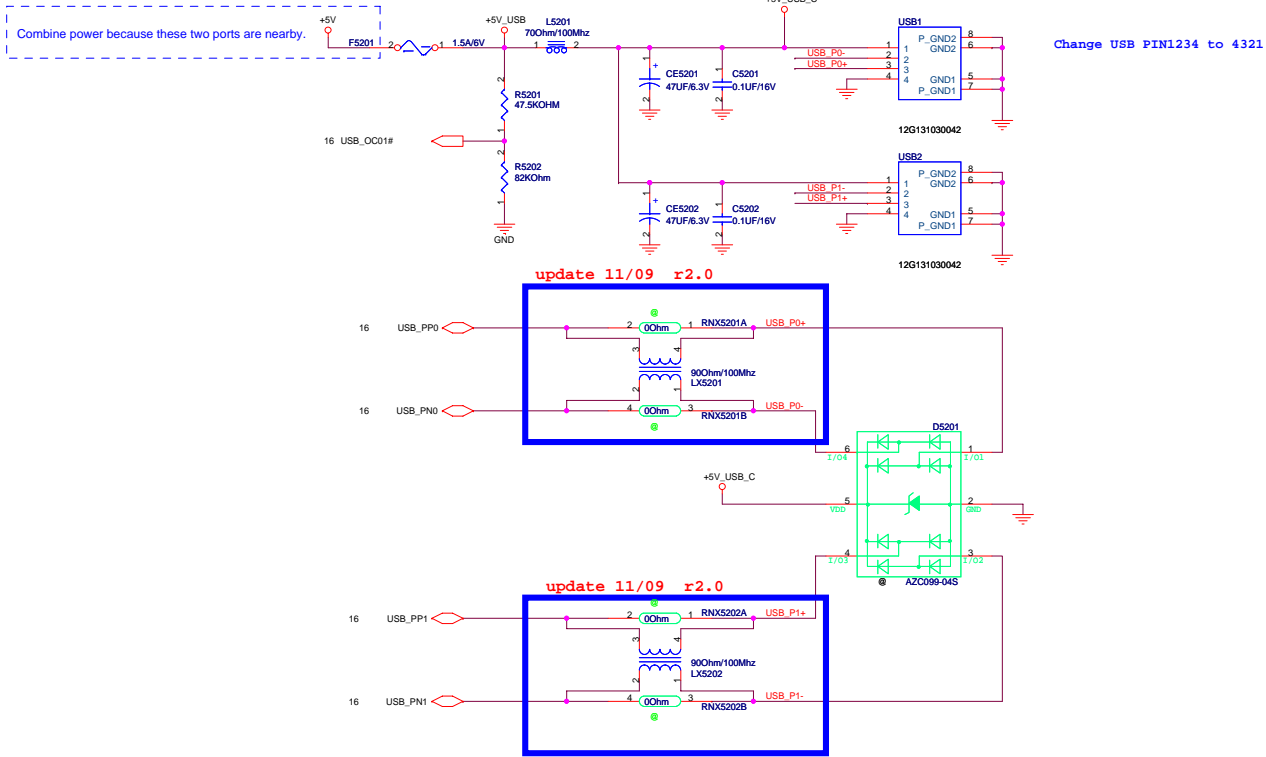


HDD (1st)

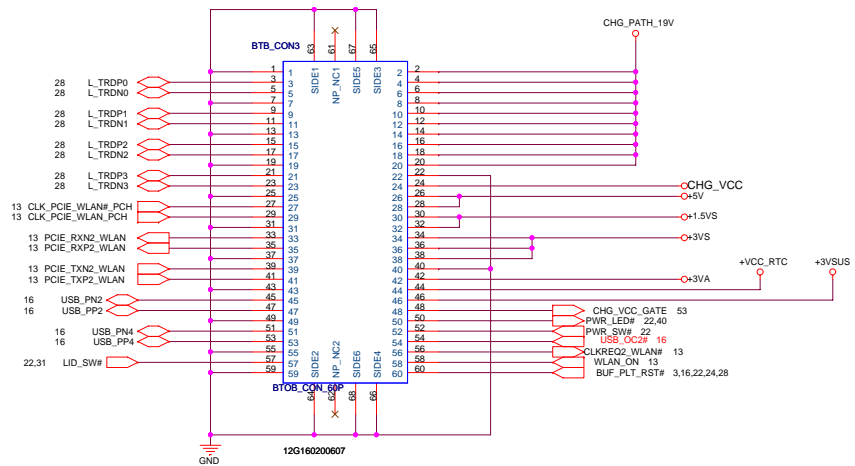


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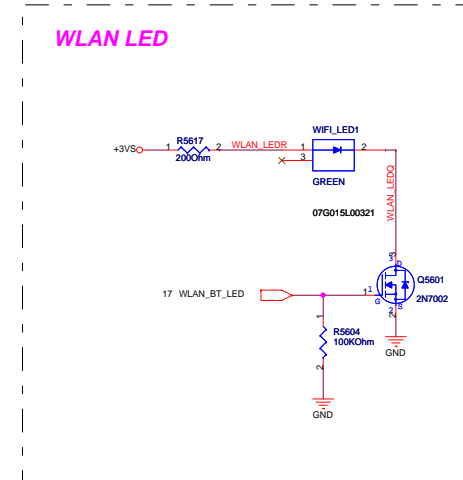
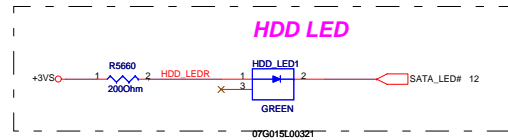
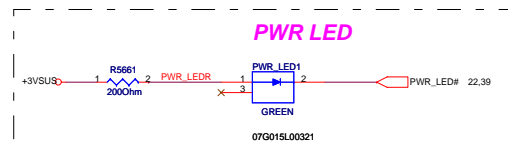
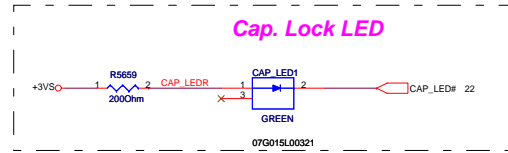
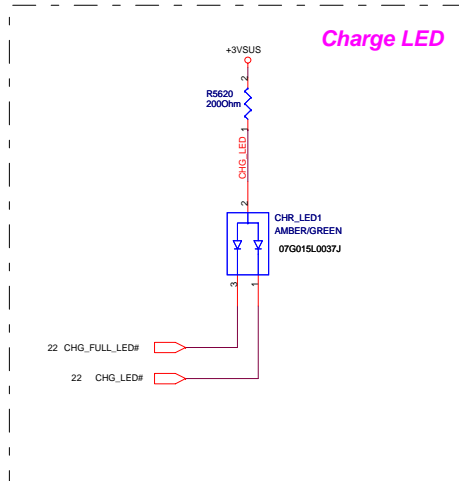
USB ports



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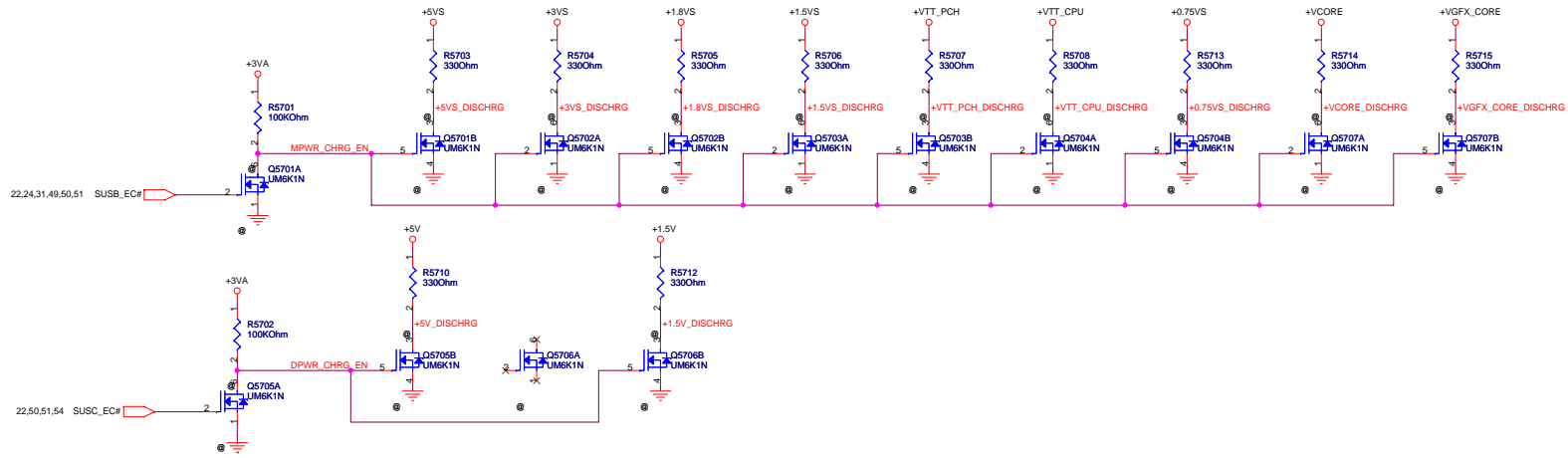


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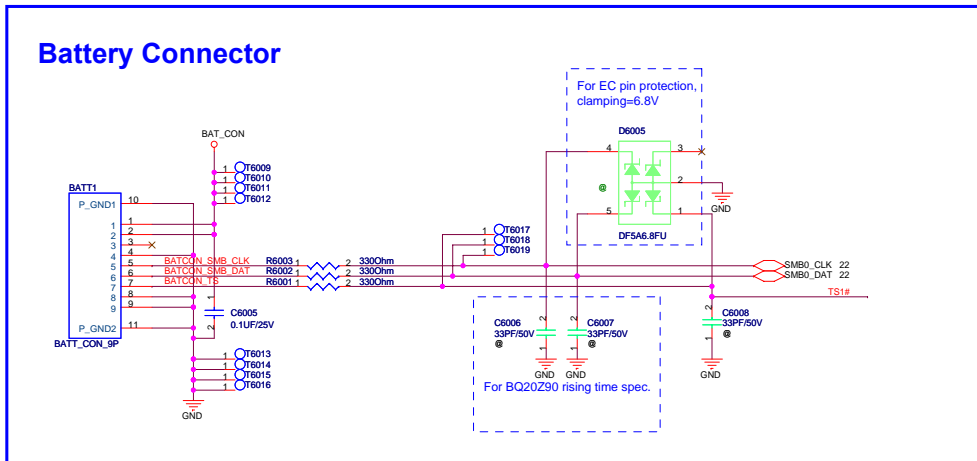


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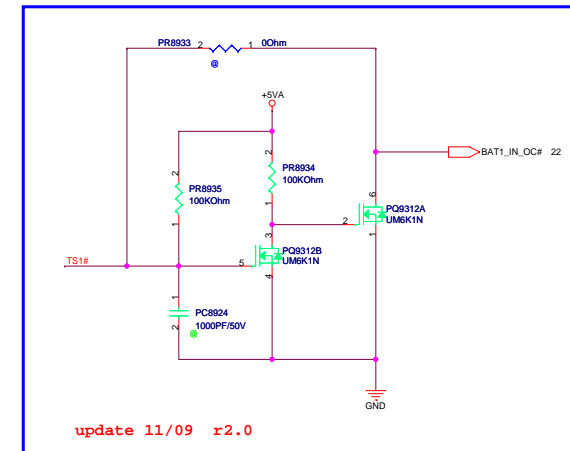
Remove +2.5Vs is for ATI GFX



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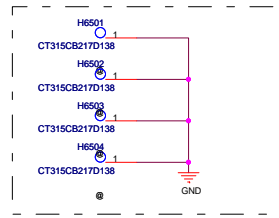
Battery IN DETECT



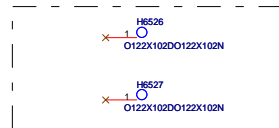
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Main Board

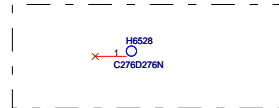
For CPU



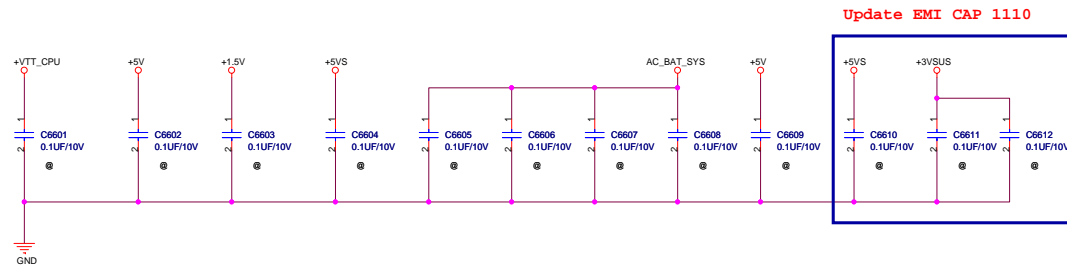
For 橢圓定位孔



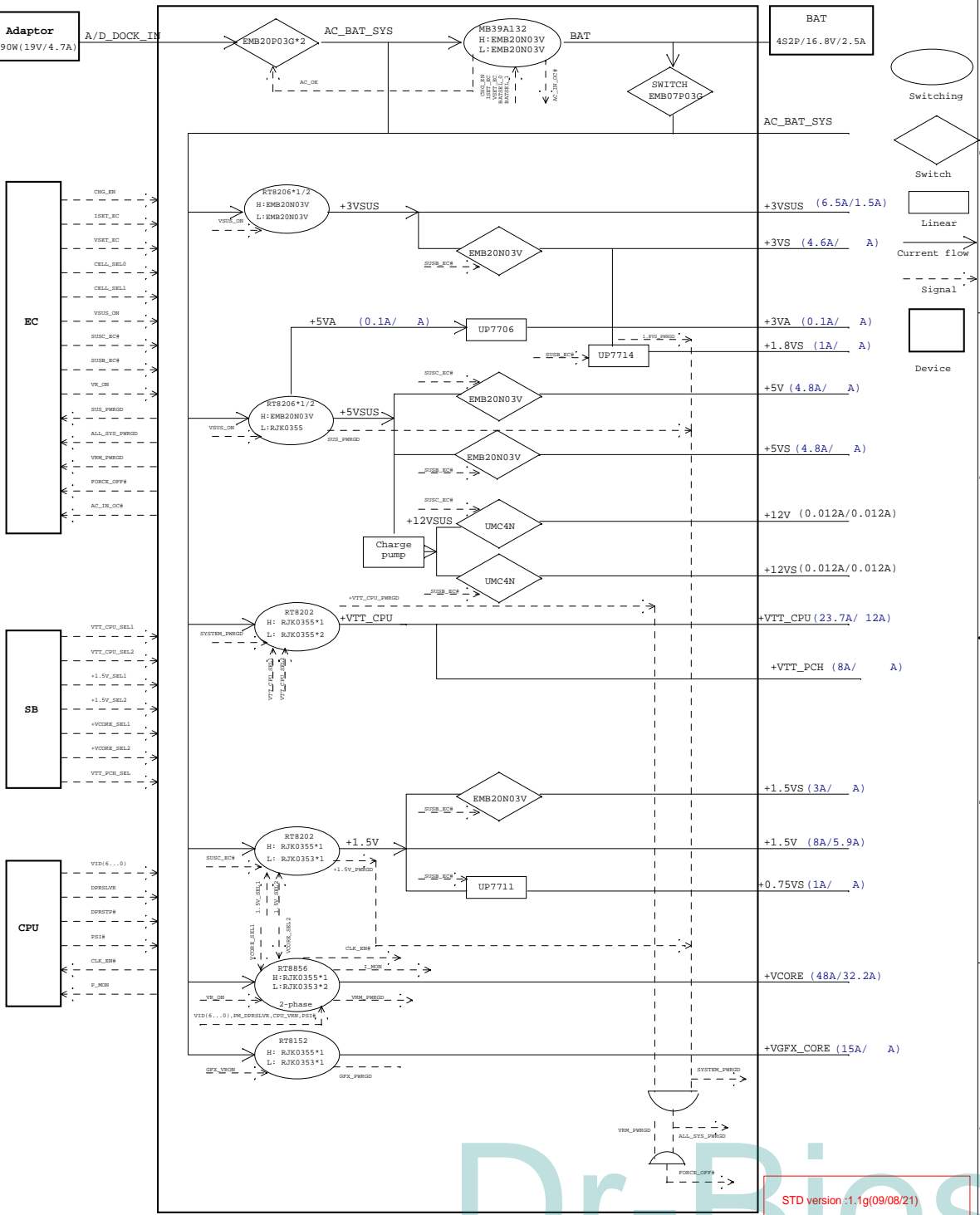
HDD 呼吸孔



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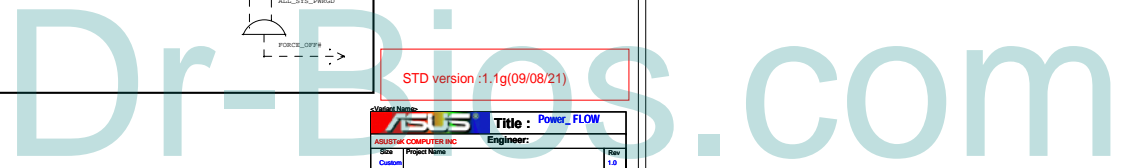


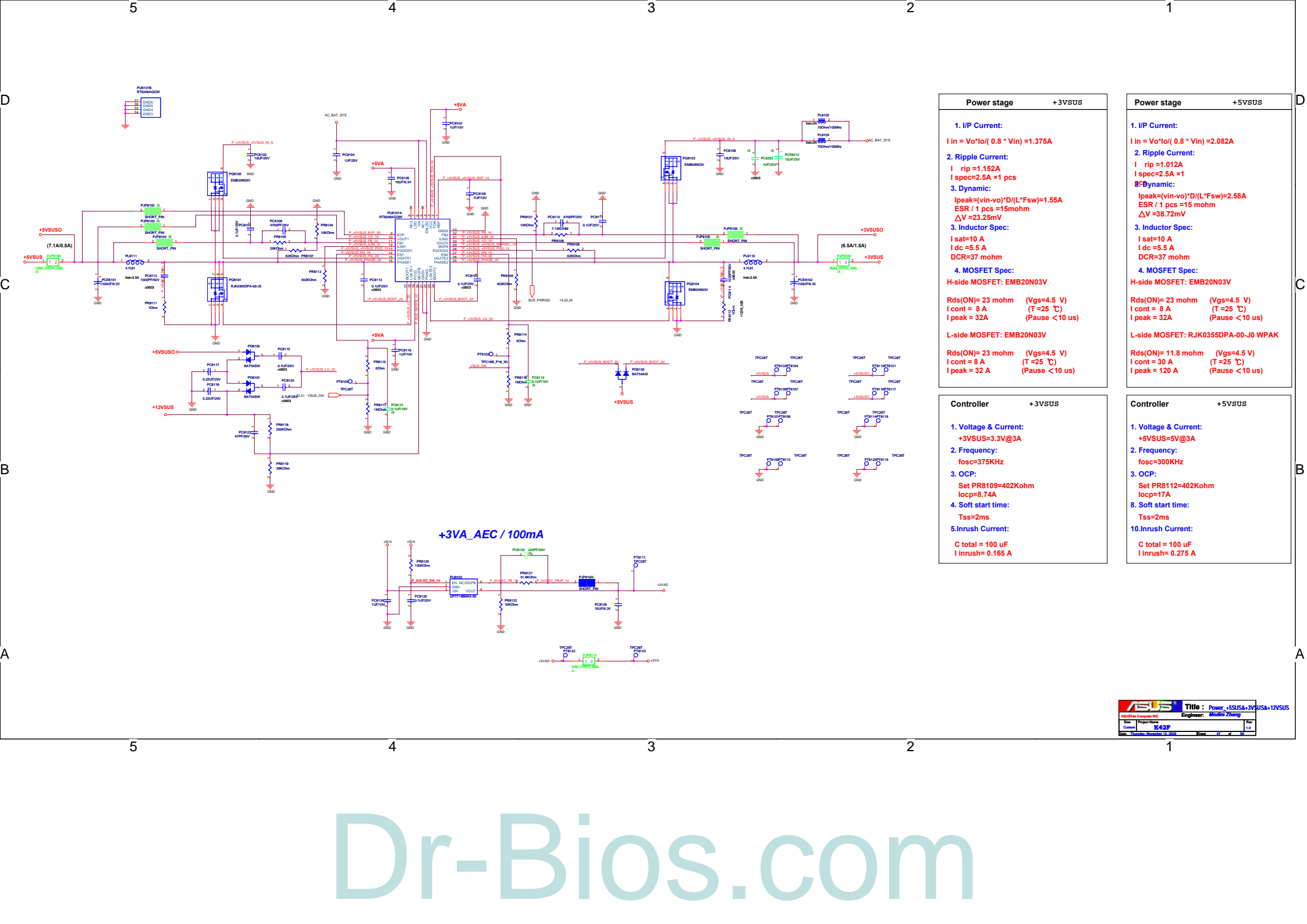
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○ Switching
 ◇ Switch
 □ Linear
 → Current flow
 - - - Signal
 □ Device

STD version:1.1g(09/08/21)



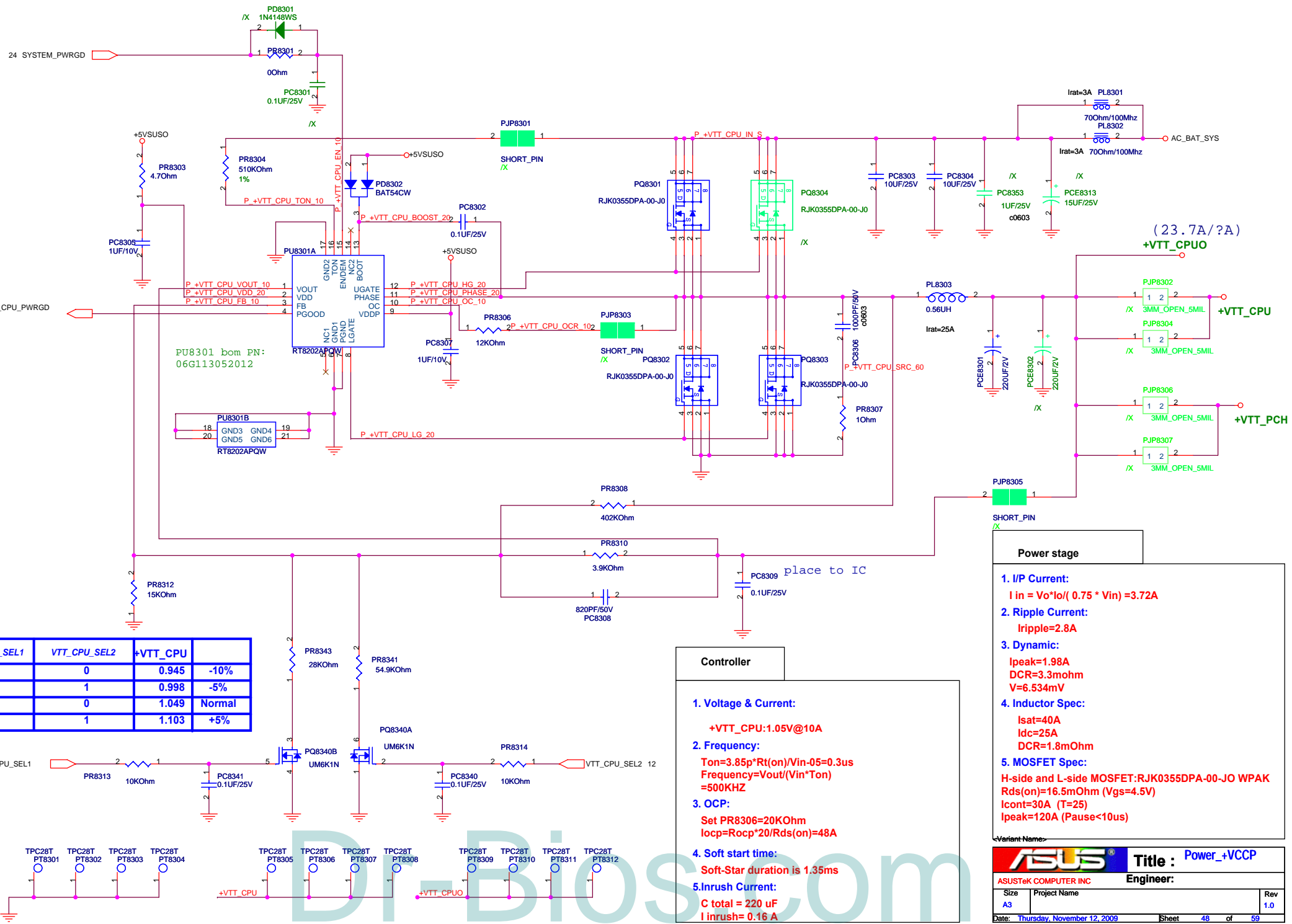


Power stage	+3VSUS
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.375A$	
2. Ripple Current: $I_{rip} = 1.152A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$	
3. Dynamic: $I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 1.55A$ $ESR / 1 \text{ pcs} = 15 \text{ mohm}$ $\Delta V = 23.25 \text{ mV}$	
3. Inductor Spec: $I_{sat} = 10 A$ $I_{dc} = 5.5 A$ $DCR = 37 \text{ mohm}$	
4. MOSFET Spec: H-side MOSFET: EMB20N03V $R_{ds(ON)} = 23 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 8 A$ ($T = 25^\circ C$) $I_{peak} = 32 A$ (Pause < 10 us)	
L-side MOSFET: EMB20N03V $R_{ds(ON)} = 23 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 8 A$ ($T = 25^\circ C$) $I_{peak} = 32 A$ (Pause < 10 us)	

Power stage	+5VSUS
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.082A$	
2. Ripple Current: $I_{rip} = 1.012A$ $I_{spec} = 2.5A \times 1$ Dynamic: $I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 2.58A$ $ESR / 1 \text{ pcs} = 15 \text{ mohm}$ $\Delta V = 38.72 \text{ mV}$	
3. Inductor Spec: $I_{sat} = 10 A$ $I_{dc} = 5.5 A$ $DCR = 37 \text{ mohm}$	
4. MOSFET Spec: H-side MOSFET: EMB20N03V $R_{ds(ON)} = 23 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 8 A$ ($T = 25^\circ C$) $I_{peak} = 32 A$ (Pause < 10 us)	
L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 30 A$ ($T = 25^\circ C$) $I_{peak} = 120 A$ (Pause < 10 us)	

Controller	+3VSUS
1. Voltage & Current: $+3VSUS = 3.3V @ 3A$	
2. Frequency: $f_{osc} = 375 \text{ KHz}$	
3. OCP: Set PR8109=402Kohm $I_{ocp} = 8.74A$	
4. Soft start time: $T_{ss} = 2 \text{ ms}$	
5. Inrush Current: $C_{total} = 100 \text{ uF}$ $I_{inrush} = 0.165 A$	

Controller	+5VSUS
1. Voltage & Current: $+5VSUS = 5V @ 3A$	
2. Frequency: $f_{osc} = 300 \text{ KHz}$	
3. OCP: Set PR8112=402Kohm $I_{ocp} = 17A$	
8. Soft start time: $T_{ss} = 2 \text{ ms}$	
10. Inrush Current: $C_{total} = 100 \text{ uF}$ $I_{inrush} = 0.275 A$	



VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

Controller

- Voltage & Current:**
+VTT_CPU: 1.05V@10A
- Frequency:**
Ton=3.85p*Rt(on)/Vin-0.5=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ
- OCP:**
Set PR8306=20Kohm
Iocp=Rocp*20/Rds(on)=48A
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush duration:**
C total = 220 uF
I inrush= 0.16 A

Power stage

- I/P Current:**
I in = Vo*Io/(0.75 * Vin) = 3.72A
- Ripple Current:**
Iripple=2.8A
- Dynamic:**
Ipeak=1.98A
DCR=3.3mohm
V=6.534mV
- Inductor Spec:**
Isat=40A
Idc=25A
DCR=1.8mOhm
- MOSFET Spec:**
H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

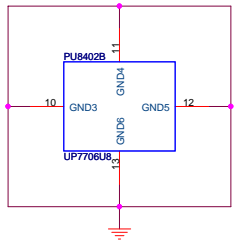
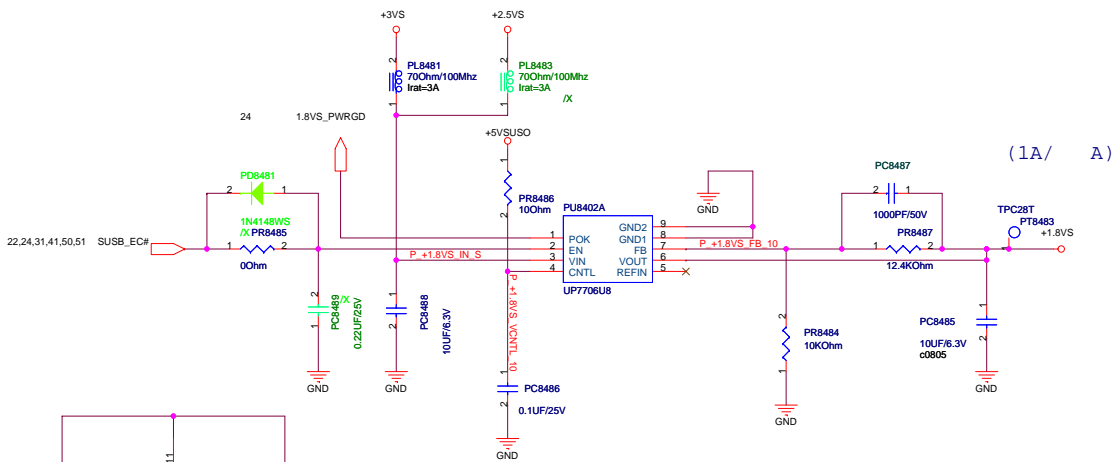
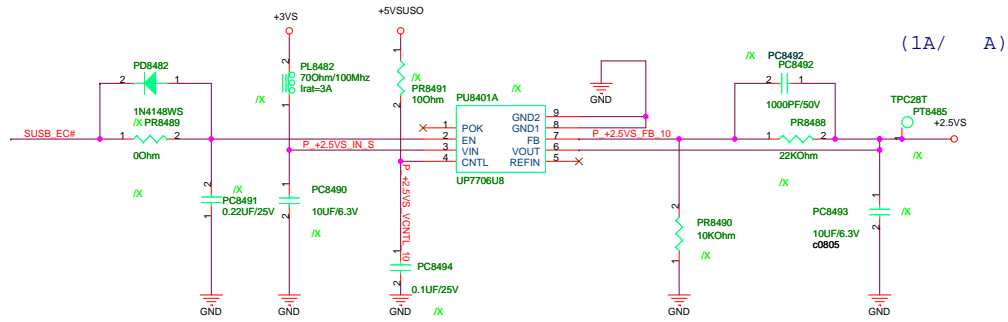
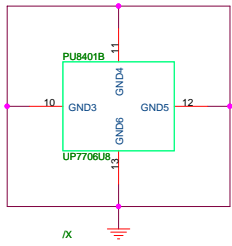
Variant Name: _____

ASUS Title : Power_+VCCP

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
A3		1.0

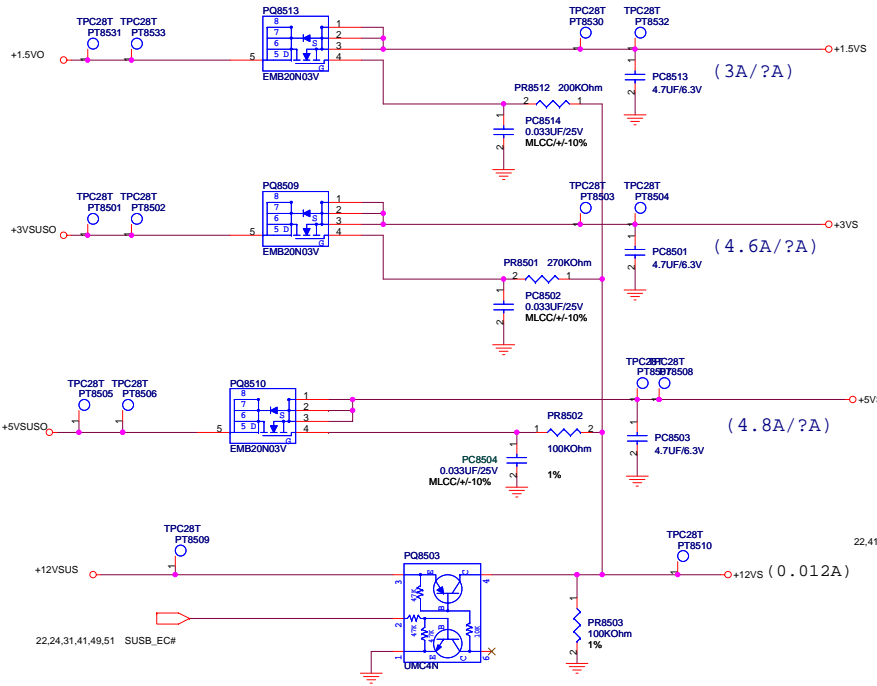
Date: Thursday, November 12, 2009 Sheet 48 of 59



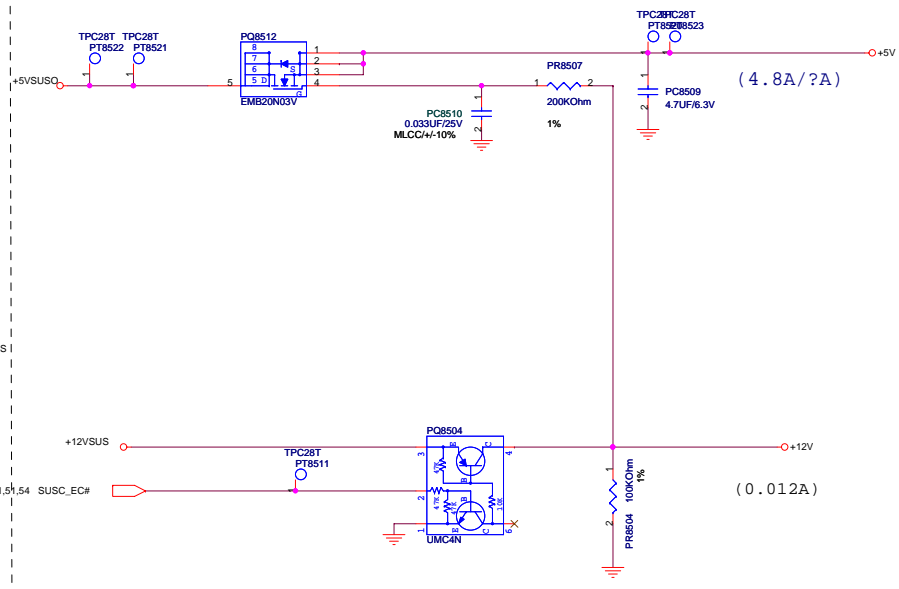
Dr-Bios.com

<Variant Name>		ASUS		Title : Power_+1.8V&+0.9V	
ASUSTeK COMPUTER INC		Engineer:			
Size	Project Name			Rev	
Custom				1.0	
Date: Thursday, November 12, 2009		Sheet 49 of 59			

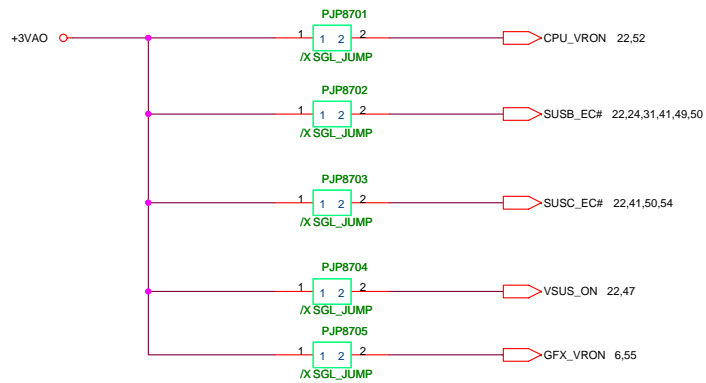
SUSB#_PWR POWER



SUSC#_PWR POWER

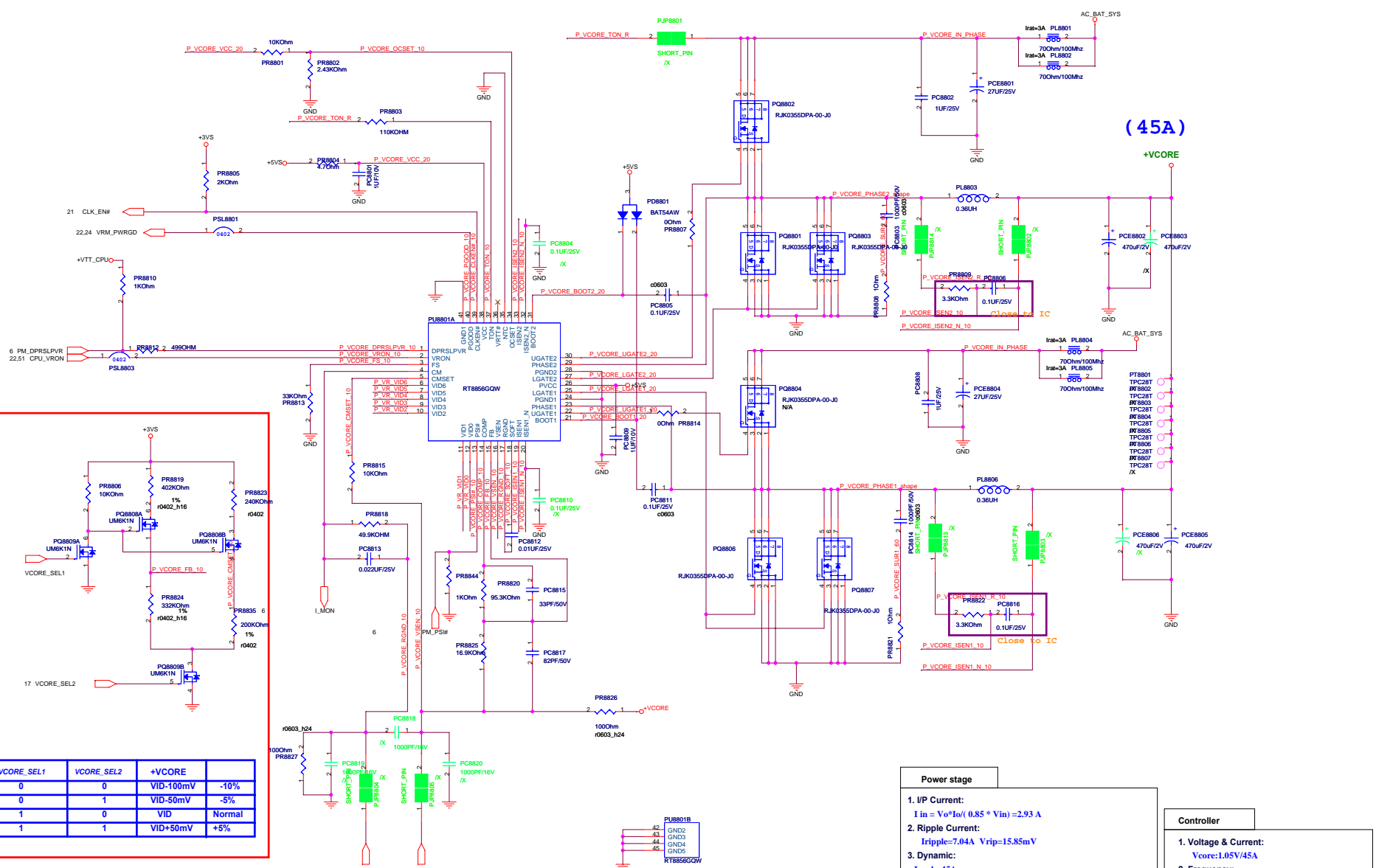


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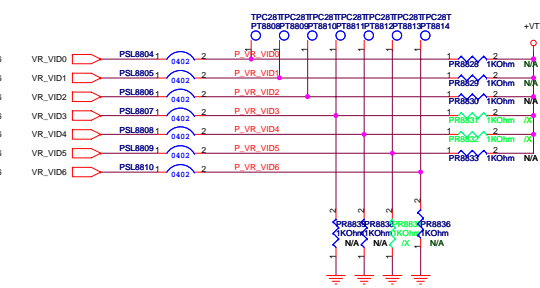
Dr-Bios.com

<Variant Name>		ASUS		Title :Power_for_test	
ASUSTeK COMPUTER INC		Engineer:			
Size	Project Name			Rev	
Custom				1.0	
Date:	Thursday, November 12, 2009	Sheet	51	of	59



(45A)
+Vcore

Vcore_sel1	Vcore_sel2	+Vcore	
0	0	VID-100mV	-10%
0	1	VID-50mV	-5%
1	0	VID	Normal
1	1	VID+50mV	+5%



CPU SKU	I _{core} MAX	I _{core} (IMON)	CPU Gain Setting	Equivalent Gain
Maximum CPU Core Current	(IMON = 300 mV)	max [A]	Set on Platform Via CPU Limiter	(mΩ)
Feature disabled			000	
100 core max @ 20 A	20	0.00		43.0
200 core max @ 20 A	30	0.00		30.0
300 core max @ 20 A	40	0.11		22.5
400 core max @ 20 A	50	0.10		18.0
500 core max @ 20 A	60	0.10		15.0
600 core max @ 20 A	70	0.10		12.9
700 core max @ 20 A	80	0.11		10.0

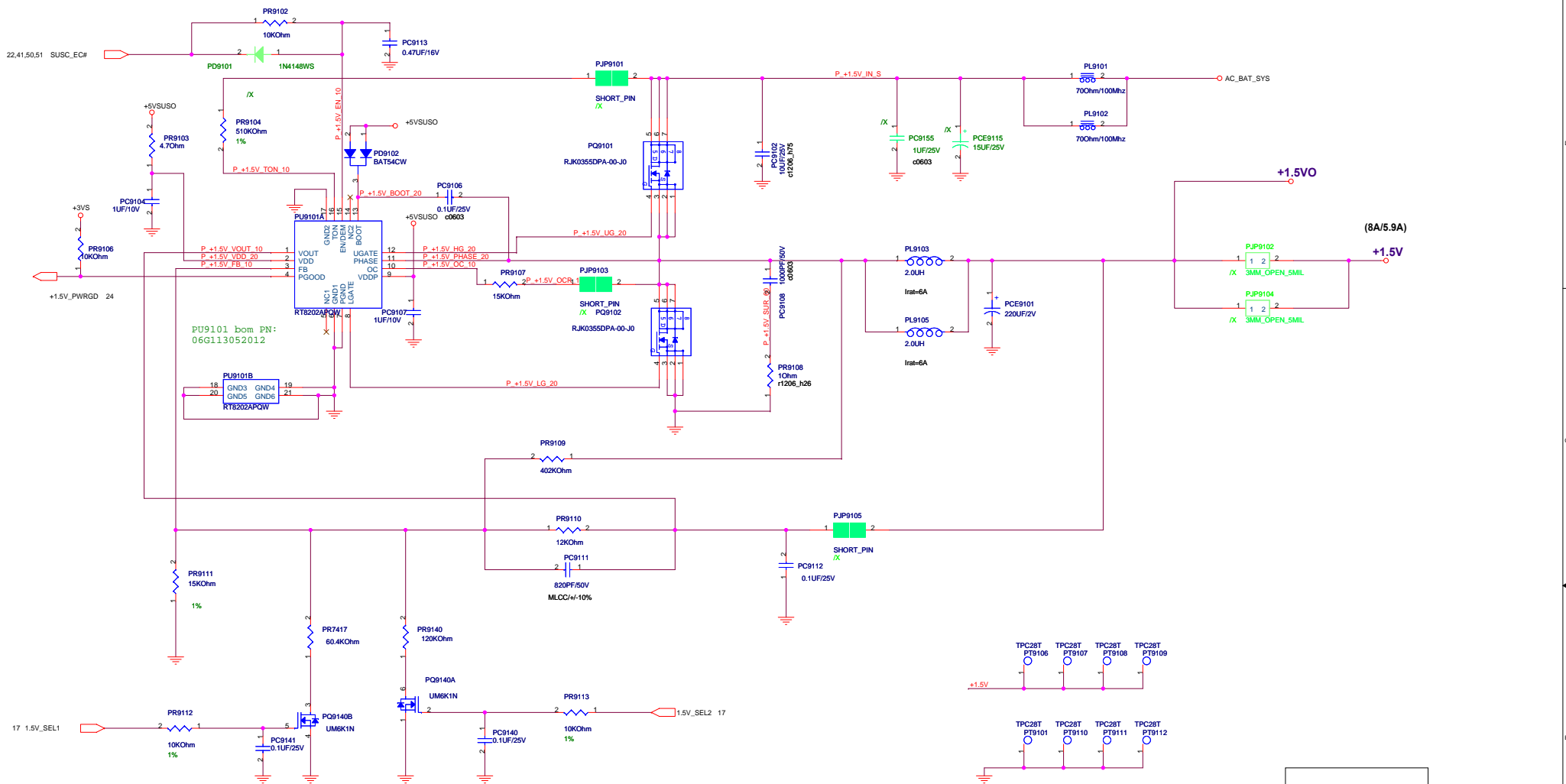
Power stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.85 \cdot V_{in}) = 2.93 \text{ A}$
- Ripple Current:**
 $I_{ripple} = 7.04 \text{ A}$ $V_{ripple} = 15.85 \text{ mV}$
- Dynamic:**
 $I_{peak} = 45 \text{ A}$
 $E_{SR} = 2.35 \text{ mJ}$
 $V = 91.1 \text{ mV}$
- Inductor Spec:**
 $I_{dc} = 38.8 \text{ A}$
 $I_{temp} = 32.5 \text{ A}$
 $DCR = 1.1 \text{ m}\Omega$
- MOSFET Spec:**
 H-side MOSFET: RJK0355 L-side MOSFET: RJK0353
 $R_{ds(on)} = 16.5 \text{ m}\Omega$ (V_{gs}=4.5V) $R_{ds(on)} = 7.6 \text{ m}\Omega$ (V_{gs}=4.5V)
 $I_{cont} = 30 \text{ A}$ (T=25) $I_{peak} = 35 \text{ A}$ (T=25)
 $I_{cpu} = 120 \text{ A}$ (Pause<10us) $I_{peak} = 140 \text{ A}$ (Pause<10us)
- CPU MLCC: 16*10uF**

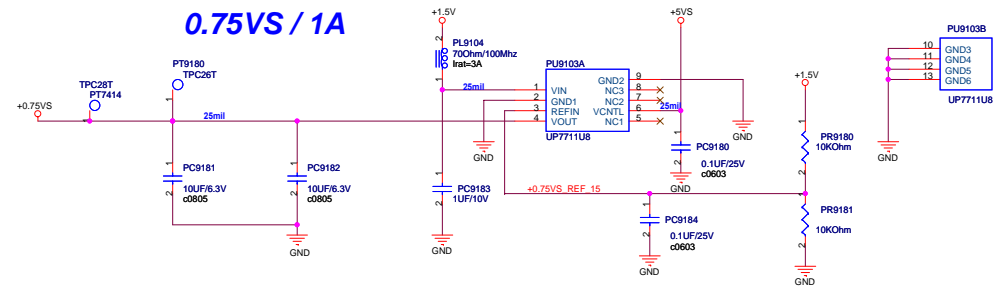
Controller

- Voltage & Current:**
 $V_{core} = 1.05 \text{ V} / 45 \text{ A}$
- Frequency:**
 $CCM: F_{sw} = 300 \cdot 33 / R_{FS} = 300 \text{ KHZ}$
 $V = 91.1 \text{ mV}$
- OCP:**
 $V_{ocet} = 25 \cdot I_{lim} \cdot R_{sense}$
 $I_{lim} = 35.5 \cdot 2 = 71 \text{ A}$
- Slew rate:**
 $Slewrate = I_{ss} / PC7810 = 100 \mu\text{A} / 10 \text{ nF} = 10 \text{ mV/us}$
- Inrush Current:**
 $C_{total} = 880 \mu\text{F}$
 $I_{inrush} = 0.15 \text{ A}$
- Droop Resistance:**
 $R_{droop} = R1 / R2 \cdot 10 \cdot R_{sense} = 2 \text{ m}\Omega$

- VID[2:0] "Reserved" - default VID[2:0]='111' - option to change default should be provided on the motherboard.
- VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
- VID[6] "Reserved" - default VID [6]='0' - option to change default should be provided on the motherboard.
- DPRSLPVR will be used to identify type of CPU core VR controller, DPRSLPVR='1' for IMVP-6.5-compliant controller.
- PSI# - "Reserved" - default PSI#='0' - option to change default should be provided on the motherboard.



0.75VS / 1A



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

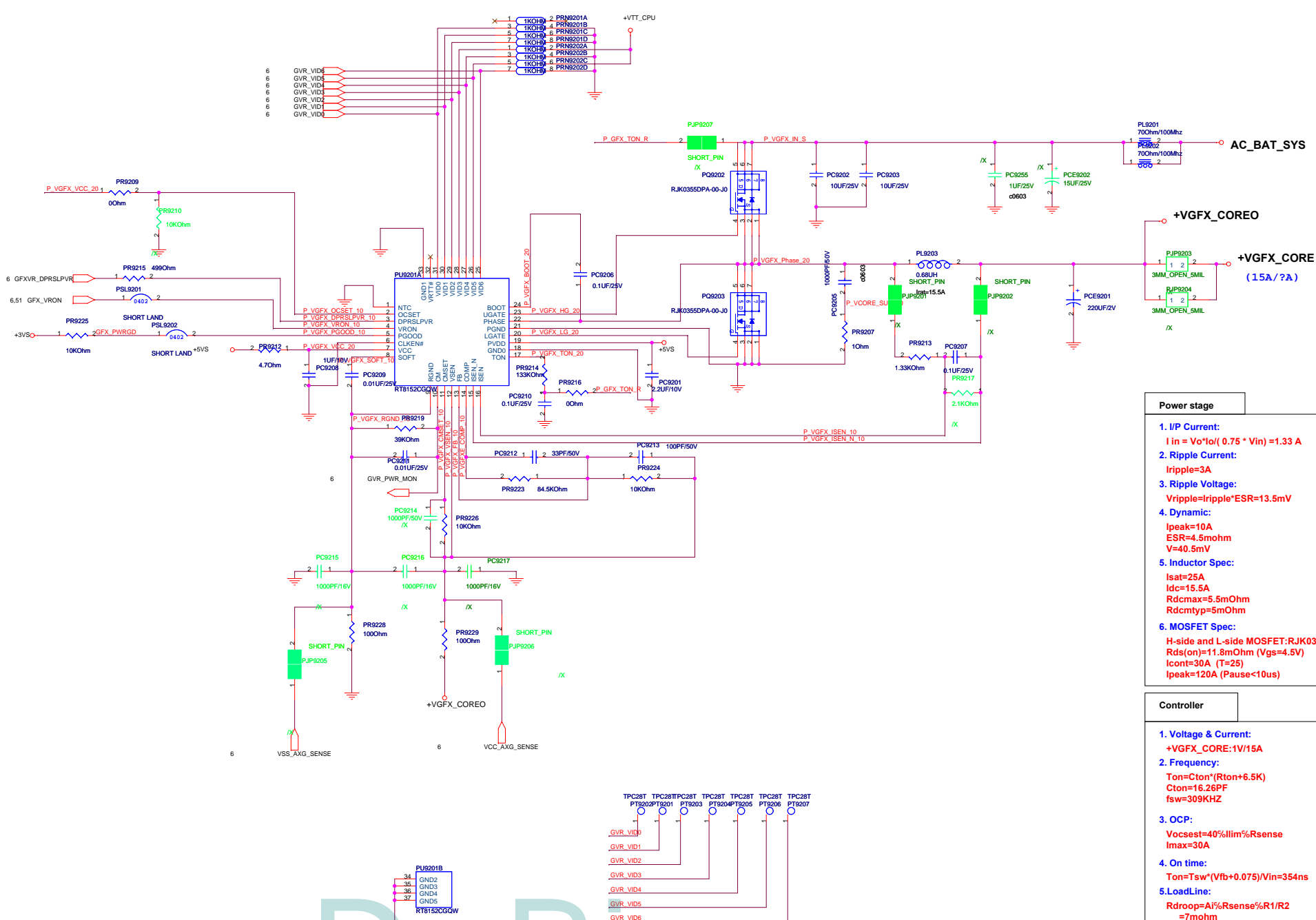
Controller

- Voltage & Current:**
1.5V: 8A
- Frequency:**
Ton=3.85p*RT(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ
- OCp:**
Set PR9107=20kohm
Iocp=Rocp*20/Rds(on)=24A
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush Current:**
C total =220uF
I inrush=0.163A

Power stage

- I/P Current:**
I in = Vo*Io/(0.75 * Vin) =1.33A
- Ripple Current:**
Iripple=3.74A
- ripple voltage:**
Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
DCR=3.3mohm
V=6.831mV
- Inductor Spec:**
Isat=22A
Idc=11A
DCR=10mohm
- MOSFET Spec:**
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

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Power stage

- 1. I/P Current:**
 $I_{in} = V_o / I_o (0.75 * V_{in}) = 1.33 A$
- 2. Ripple Current:**
 $I_{ripple} = 3A$
- 3. Ripple Voltage:**
 $V_{ripple} = I_{ripple} * ESR = 13.5mV$
- 4. Dynamic:**
 $I_{peak} = 10A$
 $ESR = 4.5mohm$
 $V = 40.5mV$
- 5. Inductor Spec:**
 $I_{sat} = 25A$
 $I_{dc} = 15.5A$
 $R_{dcmax} = 5.5mOhm$
 $R_{dc} = 5mOhm$
- 6. MOSFET Spec:**
 H-side and L-side MOSFET: RJK0355
 $R_{ds(on)} = 11.8mOhm (V_{gs} = 4.5V)$
 $I_{cont} = 30A (T = 25)$
 $I_{peak} = 120A (Pause < 10us)$

Controller

- 1. Voltage & Current:**
 $+VGFX_CORE: 1V/15A$
- 2. Frequency:**
 $Ton = C_{ton} * (R_{ton} + 6.5K)$
 $C_{ton} = 16.26PF$
 $f_{sw} = 309KHZ$
- 3. OCP:**
 $V_{ocst} = 40% I_{lim} * R_{sense}$
 $I_{max} = 30A$
- 4. On time:**
 $Ton = T_{sw} * (V_{fb} + 0.075) / V_{in} = 354ns$
- 5. Load Line:**
 $R_{droop} = A * I * R_{sense} * R1 / R2 = 7mohm$



VTT_CPU_SEL1 Default : H
VTT_CPU_SEL2 Default : L

VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

VCORE_SEL1 Default : H
VCORE_SEL2 Default : L

VCORE_SEL1	VCORE_SEL2	+VCORE	
0	0	VID-100mV	-10%
0	1	VID-50mV	-5%
1	0	VID	Normal
1	1	VID+50mV	+5%

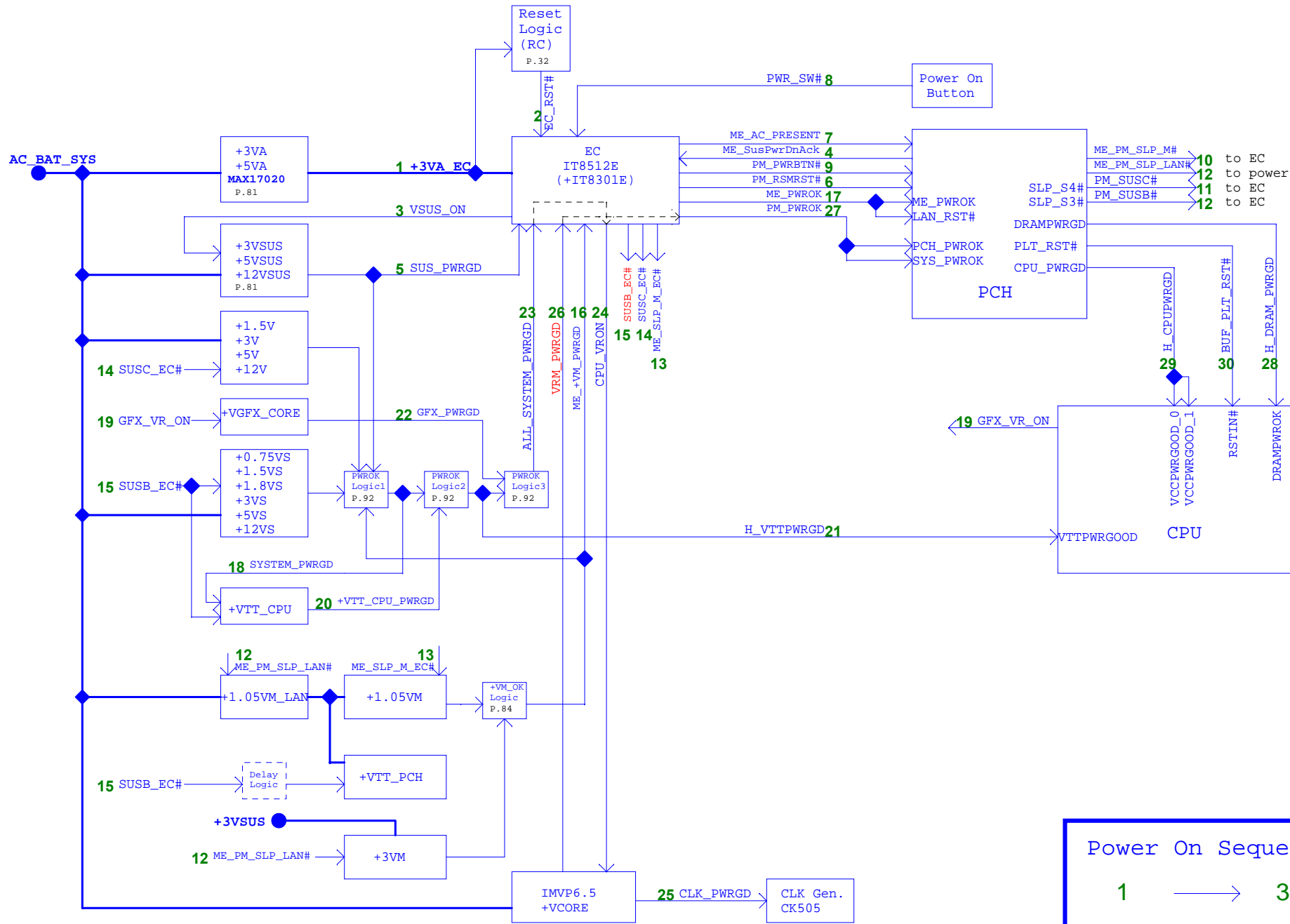
1.5V_SEL1 Default : H
1.5V_SEL2 Default : L

1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

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<Variant Name>

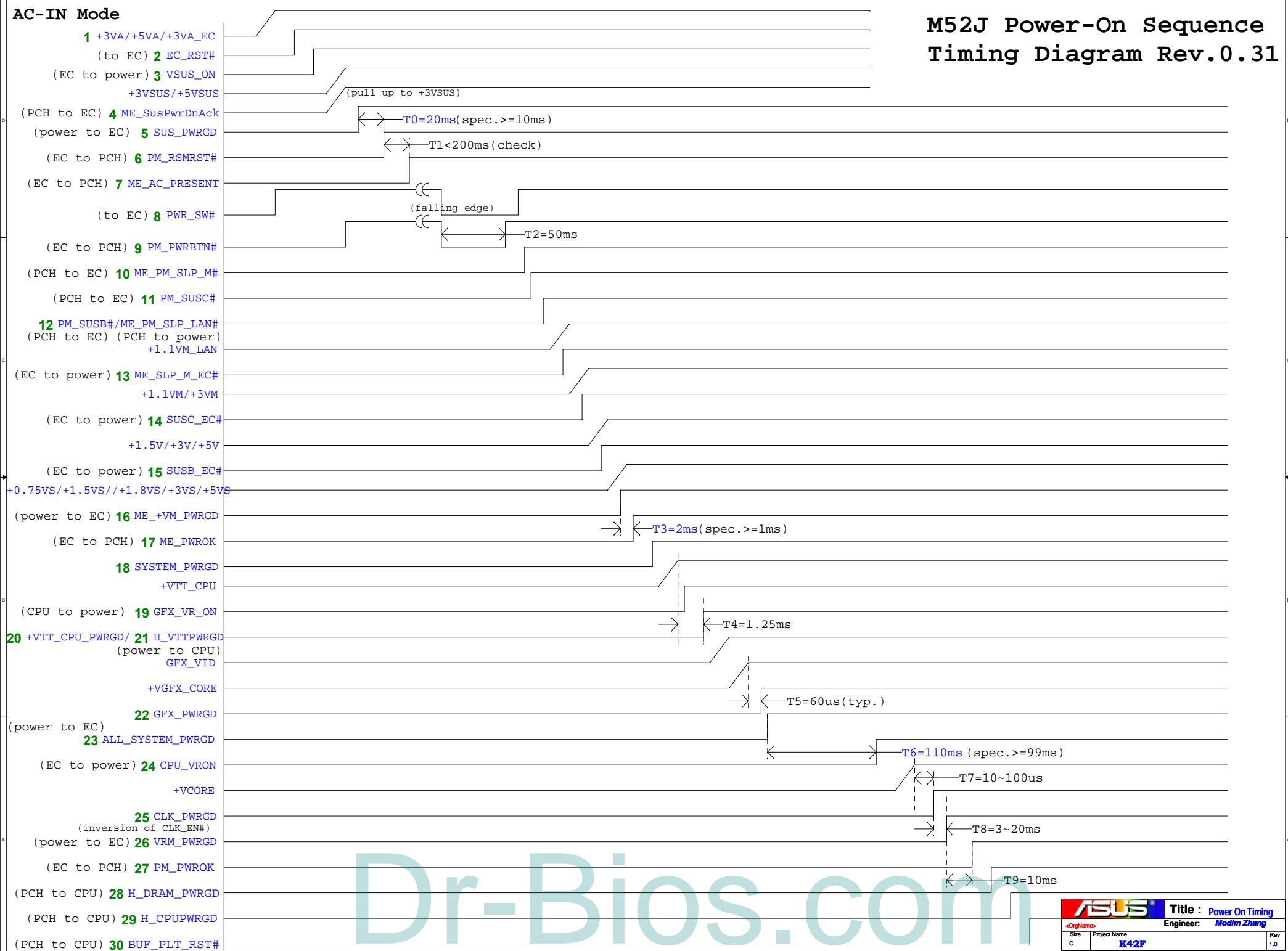
		Title : Power_VCCP
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	
A3		
Date:	Tuesday, November 10, 2009	Sheet 56 of 59



Power On Sequence
 1 → 30

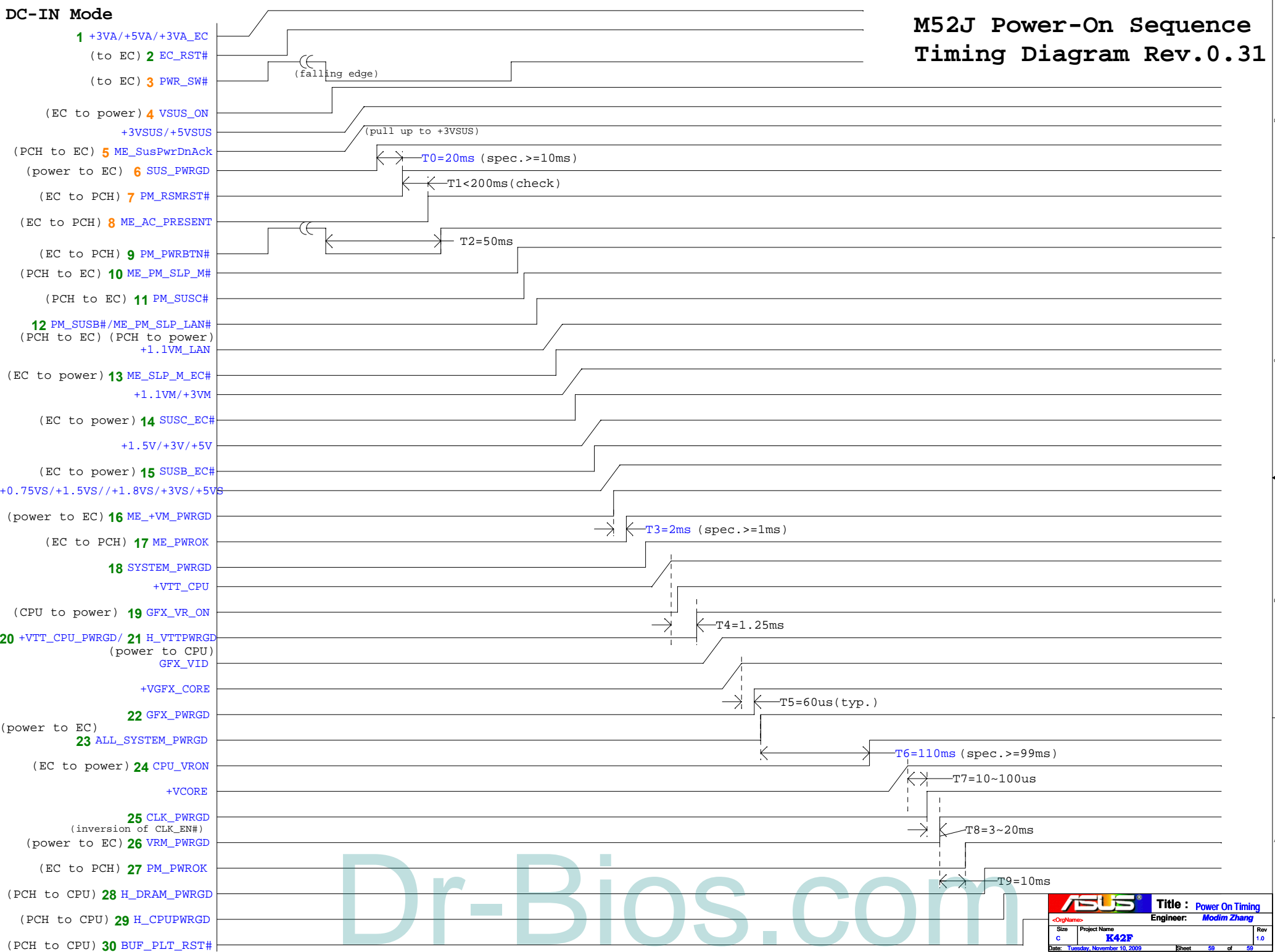
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M52J Power-On Sequence Timing Diagram Rev.0.31



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M52J Power-On Sequence Timing Diagram Rev.0.31



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