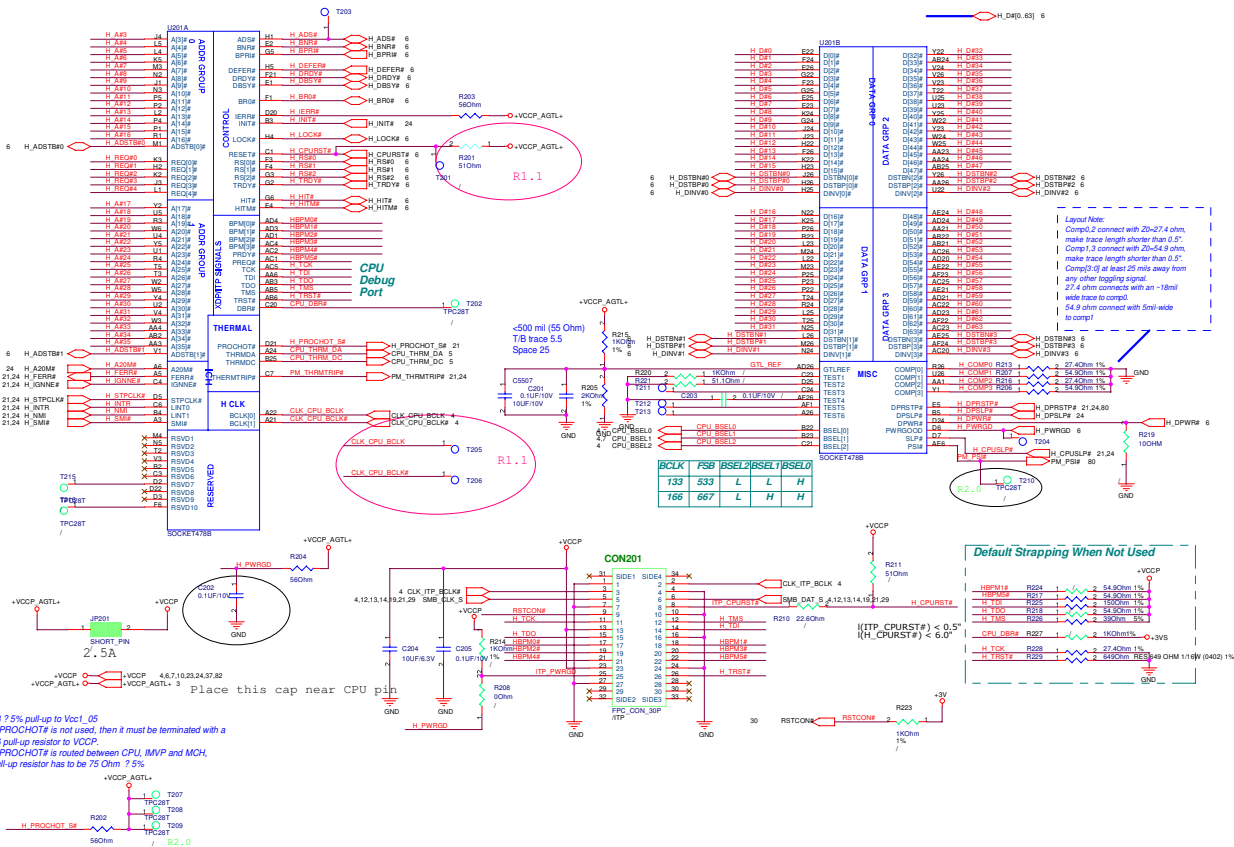


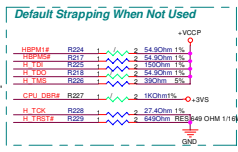
ASUS		Title : Block Diagram	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
B	FSV		1.0
Date: #B#	#B# 23 2007	Sheet	1 of 94

www.Dr-Bios.com

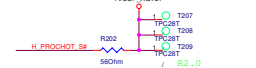


Layout Note:
 Comp2,2 connect with $20\text{-}27.4\ \mu\text{m}$,
 make trace length shorter than $0.5''$.
 Comp1,5 connect with $20\text{-}4.8\ \mu\text{m}$,
 make trace length shorter than $0.5''$.
 Comp3,3 at least 25 mils away from
 any other logging signal.
 27.4 μm connects with an -18mil
 wide trace to comp1.
 54.8 μm connect with 5mil wide
 to comp1.

BCLK	FSB	BSEL1	BSEL2
133	533	L	L
166	667	L	H

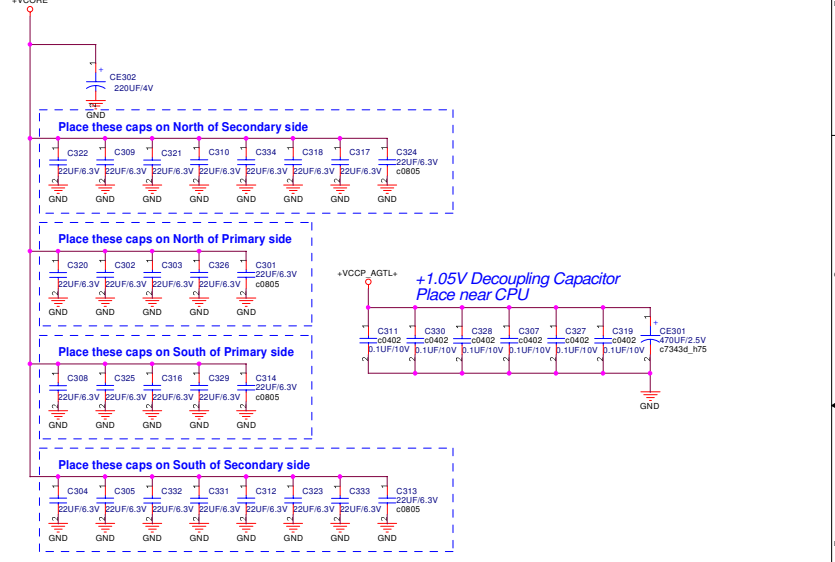
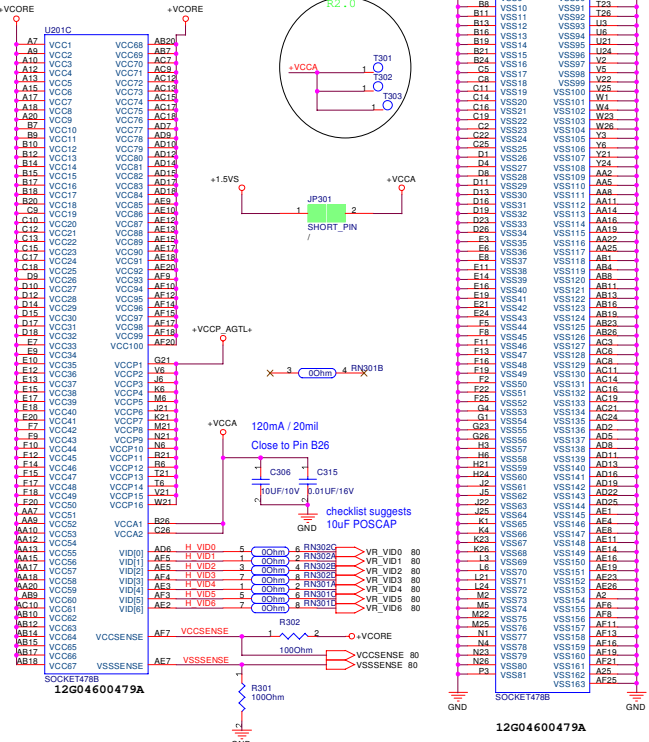


68 $\pm 5\%$ pull-up to V_{cc1_05}
 If PROCHOT# is not used, then it must be terminated with a
 56 pull-up resistor to VCCP.
 If PROCHOT# is routed between CPU, IMVP and MCH,
 pull-up resistor has to be 75 Ohm $\pm 5\%$.



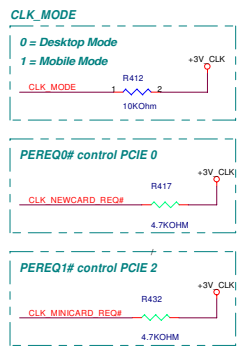
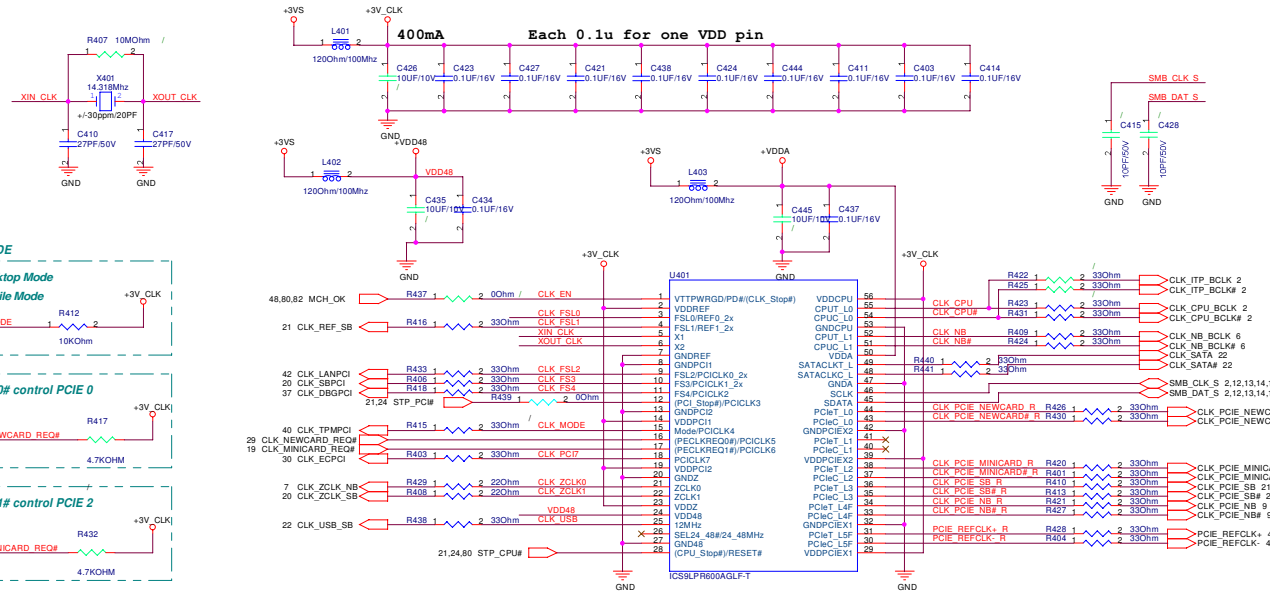
YUNAH FSB667			
LFM	TYP	HFM	
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

YUNAH FSB667			
Min	TYP	Max	
VCCP	0.997V	1.05V	1.102V
Min	TYP	Max	
ICCP			2.5A

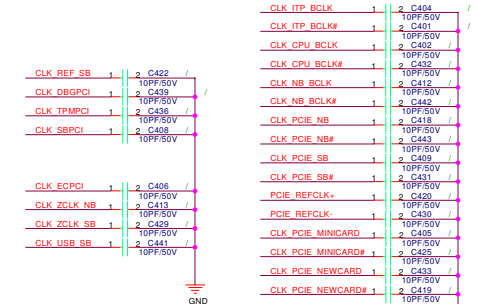
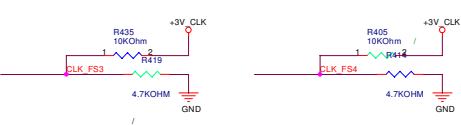
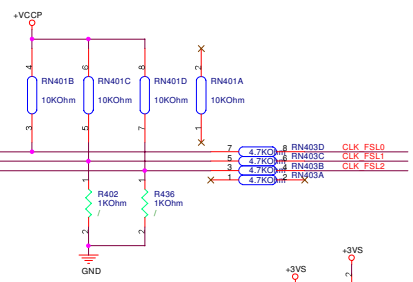


Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils with 7 mils spacing, with trace impedance of 20±27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

ASUS		Title : Yonah CPU (2)
ASUSTAK COMPUTER INC.		Engineer: Hawk Zhu
Size	Project Name	Rev
A3	FSV	1.0
Date: 11/8	11/13/23, 2007	Sheet 9 of 94



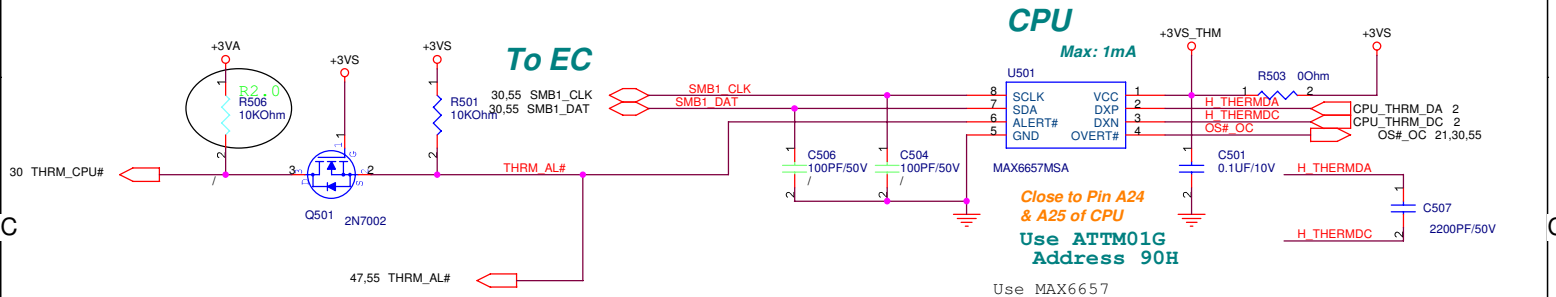
FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



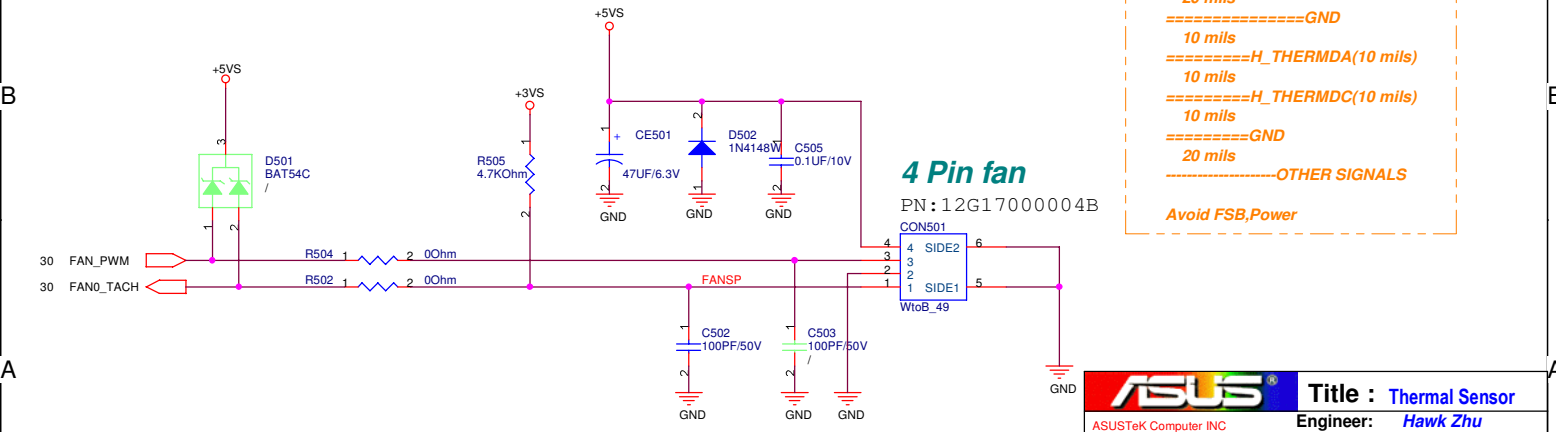
ASUS Title : Clock GEN
 ASUSTek Computer INC Engineer: Hawk Zhu
 Size Project Name
 A3 FSV
 Date: 11/18/23, 2007 Sheet 4 of 34

www.Dr-Bios.com

Thermal Sensor



DC FAN Control



Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS

20 mils

=====GND

10 mils

=====H_THERMDA(10 mils)

10 mils

=====H_THERMDC(10 mils)

10 mils

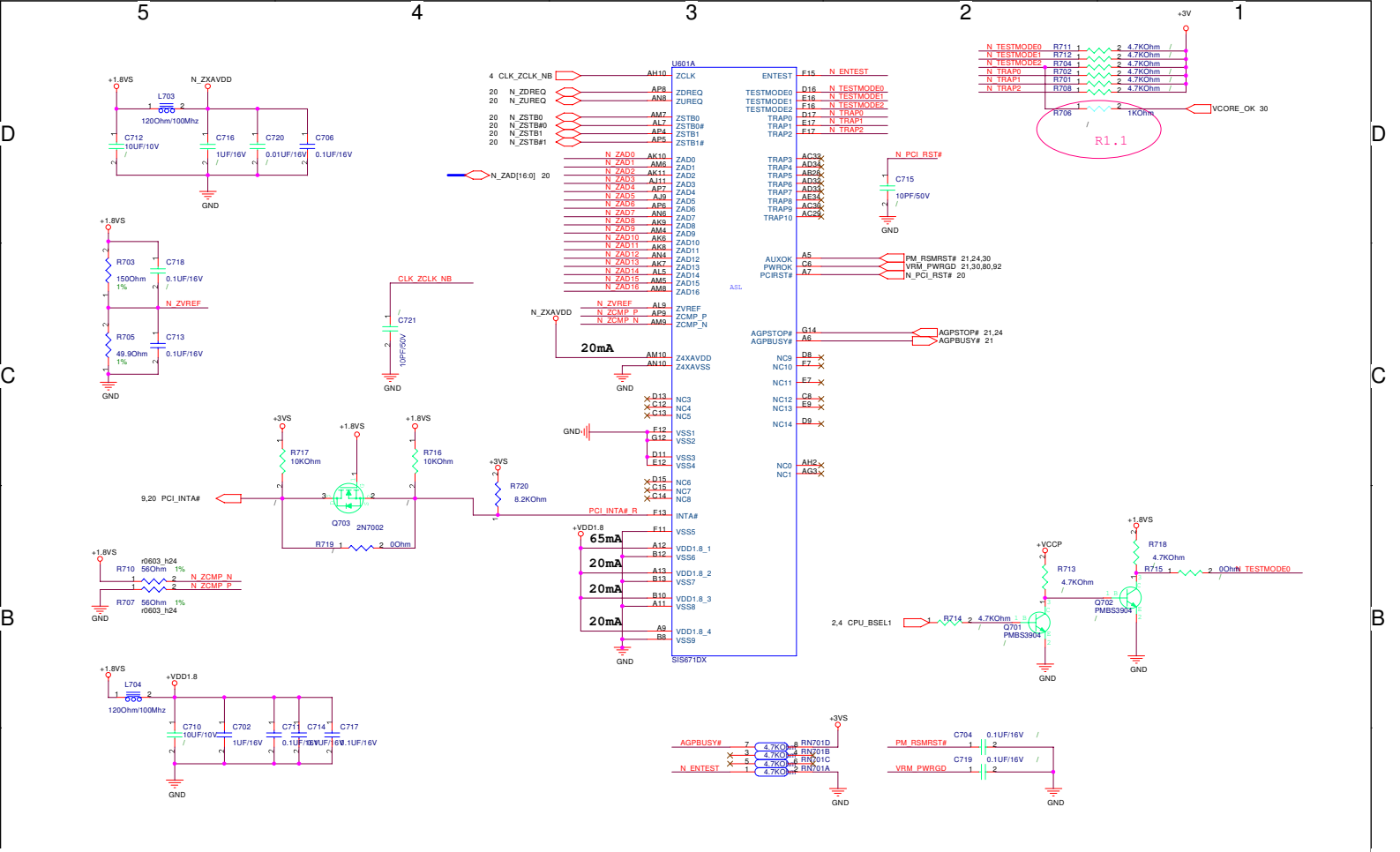
=====GND

20 mils

-----OTHER SIGNALS

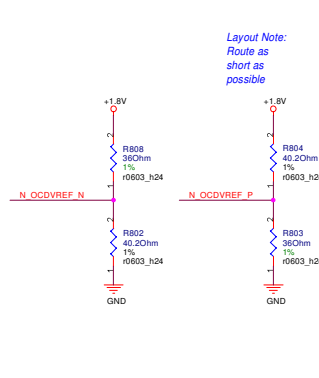
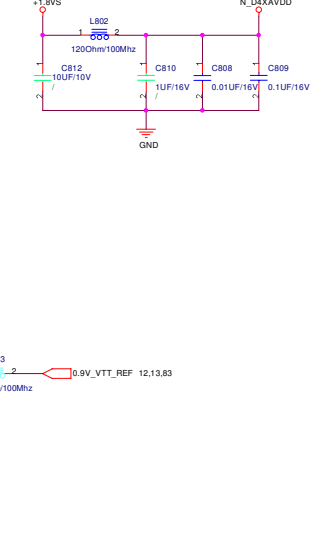
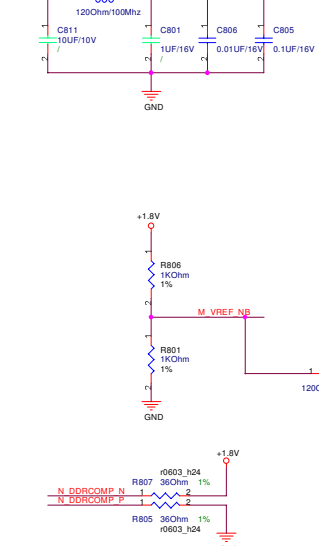
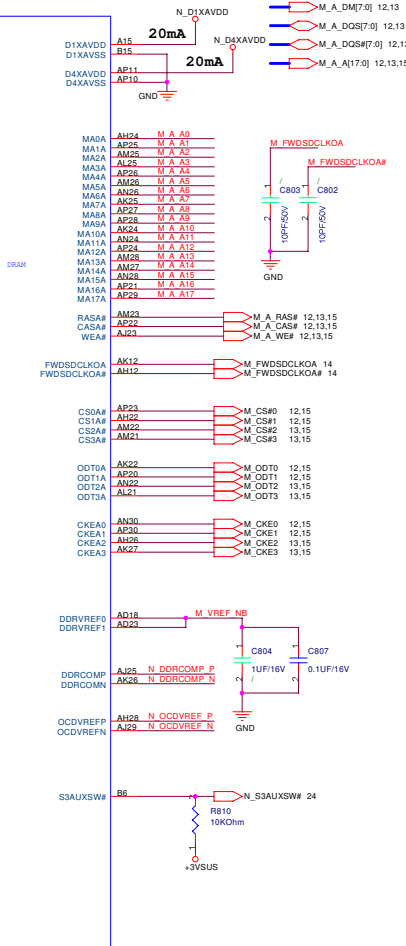
Avoid FSB,Power

ASUS		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A4	Project Name F5V	Date: 星期四 四月 23, 2007	Rev 1.0
		Sheet 5 of 94	



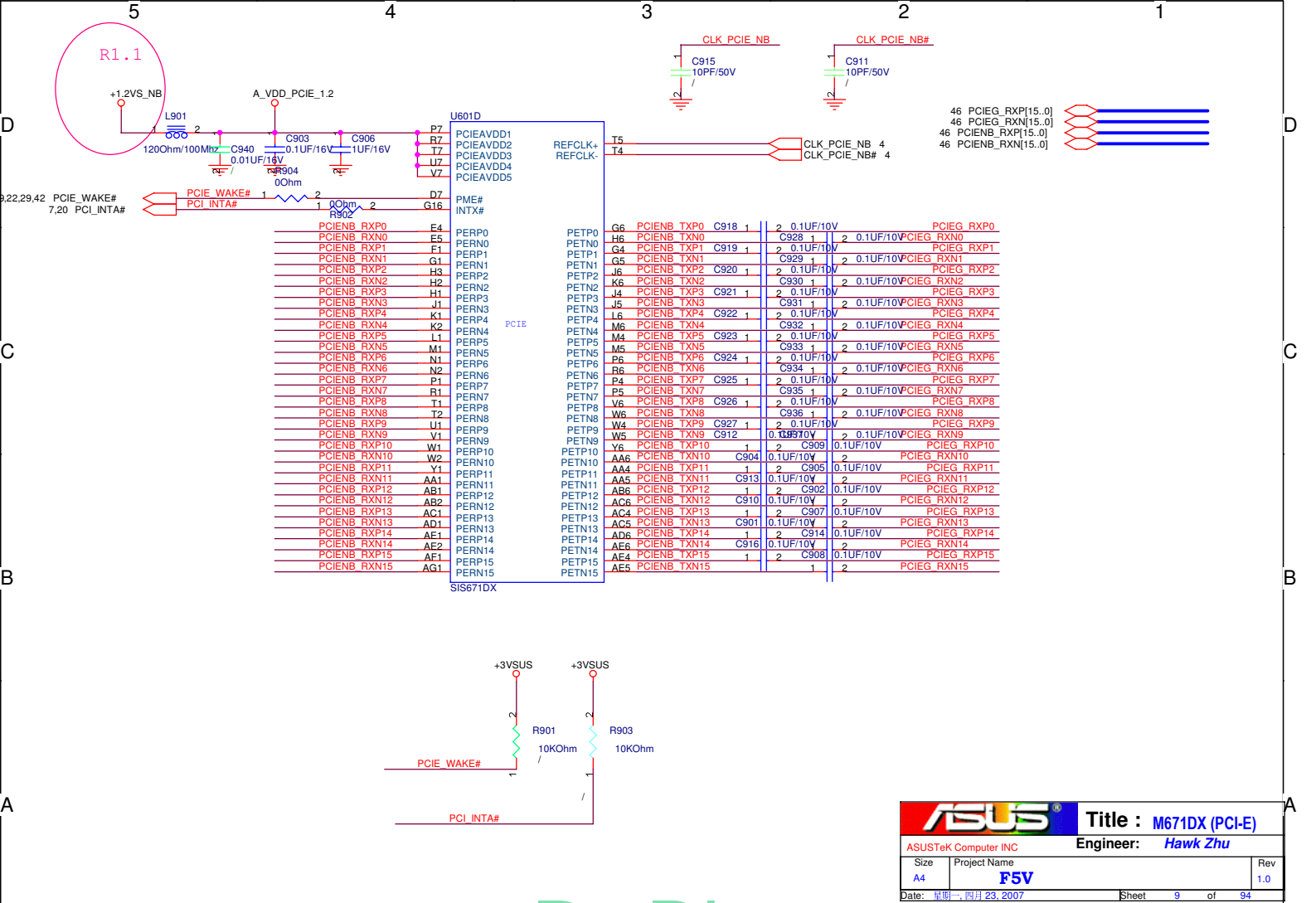
ASUS		Title M671DX(MuTIOL&VGA)	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size	Project Name	Rev	
A3	FSV	1.0	
Date: 10/11/2007		Sheet	7 of 94

M_A_DQ00	AD31	MD9A
M_A_DQ01	AD30	MD9A
M_A_DQ02	AG34	MD2A
M_A_DQ03	AE29	MD5A
M_A_DQ04	AE32	MD5A
M_A_DQ05	AE34	MD5A
M_A_DQ06	AE31	MD5A
M_A_DQ07	AE30	MD5A
M_A_DQ08	AD28	DM8A
M_A_DQ09	AE32	DD50A
M_A_DQ09B	AE33	DD50AA
M_A_DQ09	AE28	MD8A
M_A_DQ10	AH31	MD10A
M_A_DQ11	AK30	MD11A
M_A_DQ12	AE30	MD12A
M_A_DQ13	AG32	MD12A
M_A_DQ14	AK32	MD13A
M_A_DQ15	AJ31	MD15A
M_A_DQ16	AH34	MD14A
M_A_DQ17	AH32	DM11A
M_A_DQ18	AH32	DD51A
M_A_DQ19	AK32	MD18A
M_A_DQ20	AK32	MD18A
M_A_DQ21	AK32	MD18A
M_A_DQ22	AK29	MD21A
M_A_DQ23	AL31	MD23A
M_A_DQ24	AK30	MD24A
M_A_DQ25	AK31	MD25A
M_A_DQ26	AK29	MD25A
M_A_DQ27	AK29	MD25A
M_A_DQ28	AK28	MD31A
M_A_DQ29	AK29	MD31A
M_A_DQ30	AK30	DM33A
M_A_DQ31	AK31	DD33A
M_A_DQ32	AK20	MD32A
M_A_DQ33	AK20	MD32A
M_A_DQ34	AM19	MD34A
M_A_DQ35	AH18	MD35A
M_A_DQ36	AN20	MD35A
M_A_DQ37	AJ21	MD37A
M_A_DQ38	AH20	MD38A
M_A_DQ39	AH20	MD38A
M_A_DQ40	AK21	DM44A
M_A_DQ41	AK19	DD44A
M_A_DQ42	AK18	DD44A
M_A_DQ43	AK17	MD41A
M_A_DQ44	AP18	MD43A
M_A_DQ45	AP18	MD43A
M_A_DQ46	AN18	MD45A
M_A_DQ47	AP17	MD47A
M_A_DQ48	AM18	DM5A
M_A_DQ49	AL17	DD55A
M_A_DQ50	AM17	DD55A
M_A_DQ48	AN16	MD48A
M_A_DQ49	AK16	MD48A
M_A_DQ50	AN14	MD49A
M_A_DQ51	AJ15	MD51A
M_A_DQ52	AP16	MD52A
M_A_DQ53	AM16	MD53A
M_A_DQ54	AK15	MD54A
M_A_DQ55	AP14	MD55A
M_A_DQ56	AH16	MD56A
M_A_DQ57	AL15	DM6A
M_A_DQ58	AM15	DD6A
M_A_DQ59	AM15	DD6AA
M_A_DQ56	AL13	MD56A
M_A_DQ57	AM12	MD57A
M_A_DQ58	AM12	MD57A
M_A_DQ59	AJ14	MD58A
M_A_DQ60	AM14	MD59A
M_A_DQ61	AK14	MD51A
M_A_DQ62	AM12	MD52A
M_A_DQ63	AH14	MD53A
M_A_DQ64	AK13	MD54A
M_A_DQ65	AP12	DM7A
M_A_DQ66	AP13	DD7A



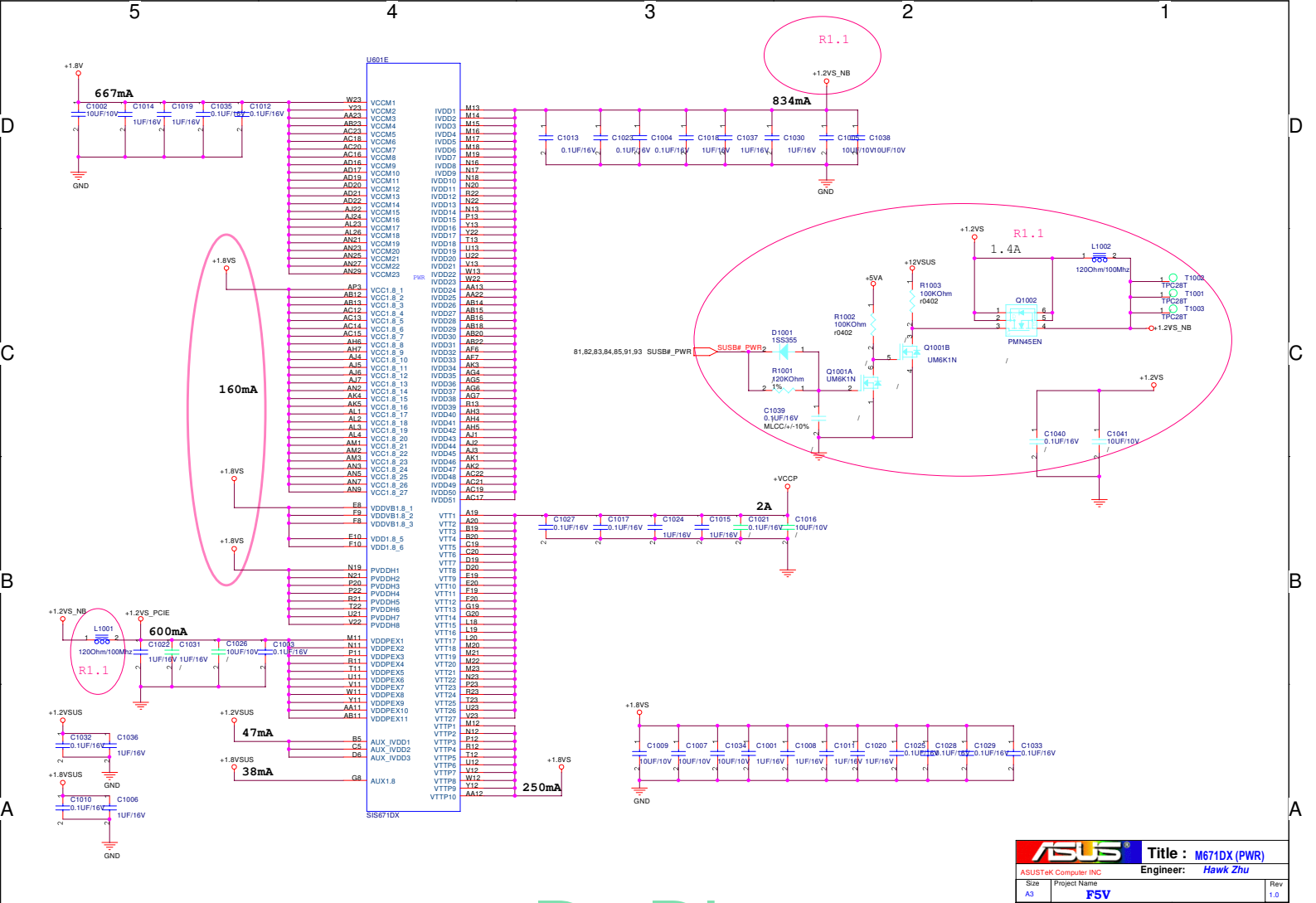
Layout Note:
Route as short as possible

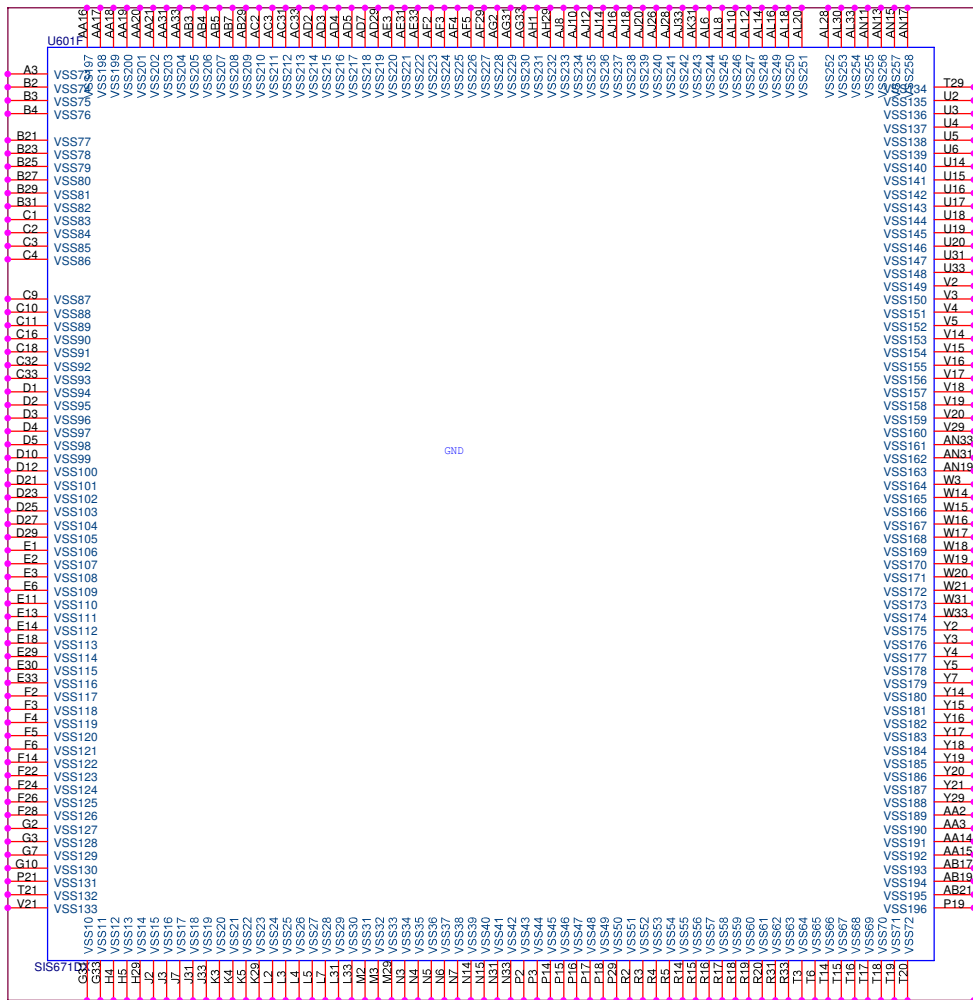
ASUS		Title: M671DX (DDR2)
ASUSTek Computer INC	Engineer: Hawk Zhu	Rev: 1.0
Size: A3	Project Name: F5V	Date: 11/11/23/2007
Sheet 8 of 94		



www.Dr-Bios.com

ASUS Title : M671DX (PCI-E)
 ASUSTeK Computer INC Engineer: Hawk Zhu
 Size: A4 Project Name: F5V Rev: 1.0
 Date: 星期一, 四月 23, 2007 Sheet: 9 of 94

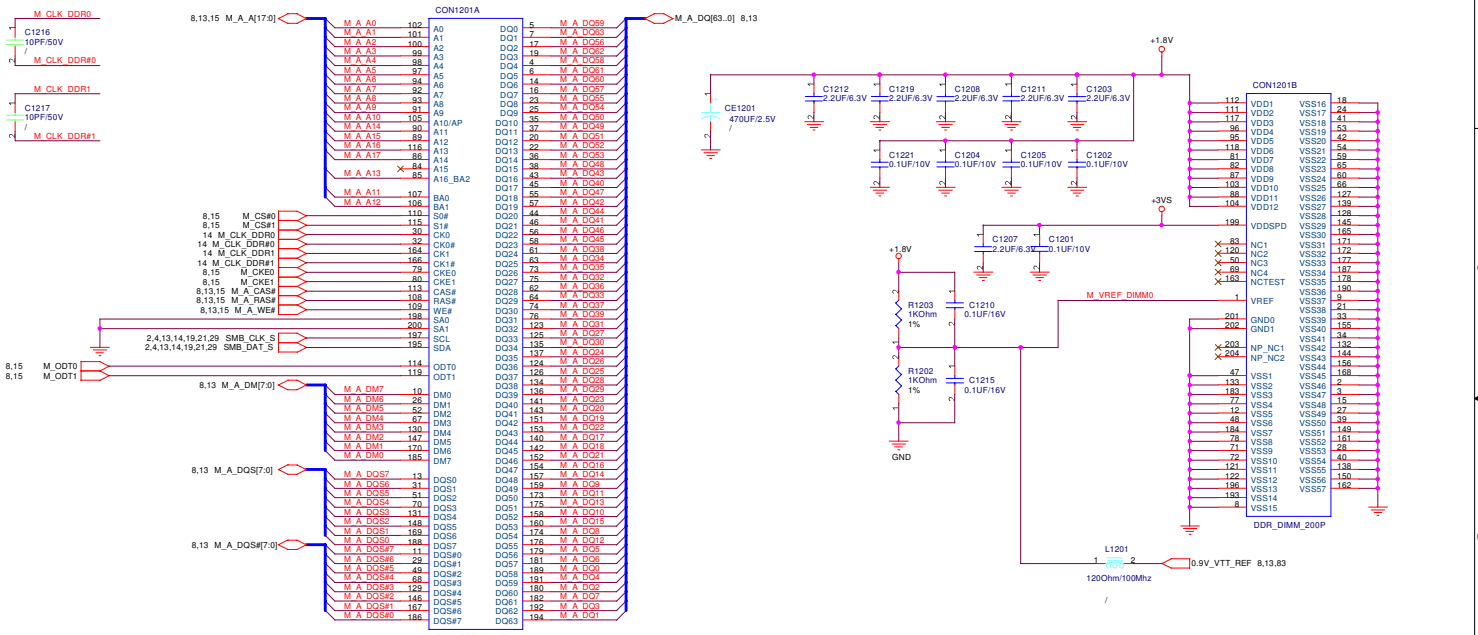




		Title : M671DX (GND)	
ASUSTeK Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A4	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet	11 of 94

www.Dr-Bios.com

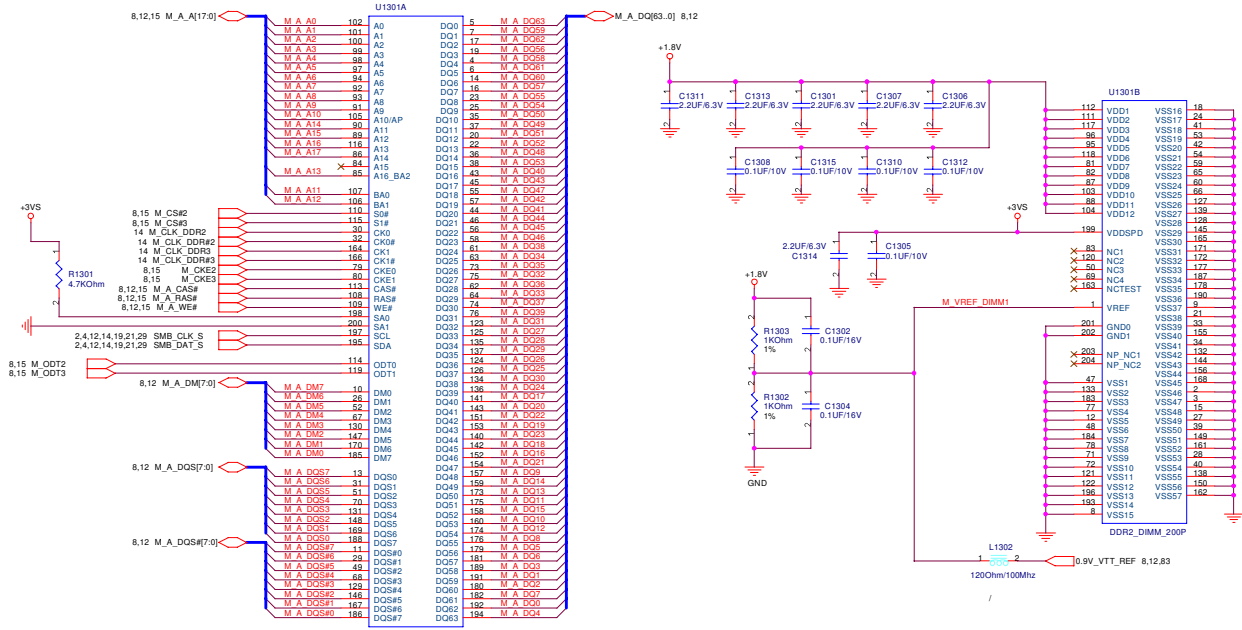
TOP



PN:12G025122006

ASUS		Title : DDR2 SO-DIMM1
ASUSTek Computer INC		Engineer: Hawk Zhu
Size	Project Name	Rev
A3	FSV	1.0
Date: 11/18/23	Sheet	12 of 34

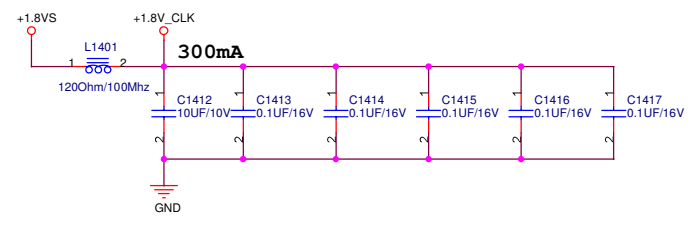
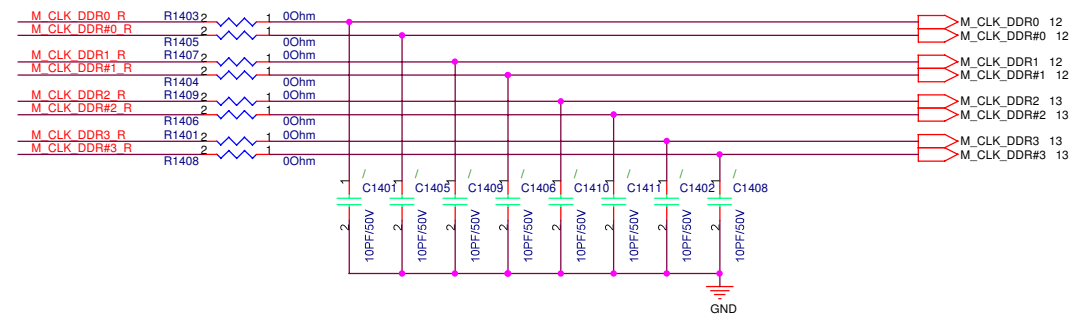
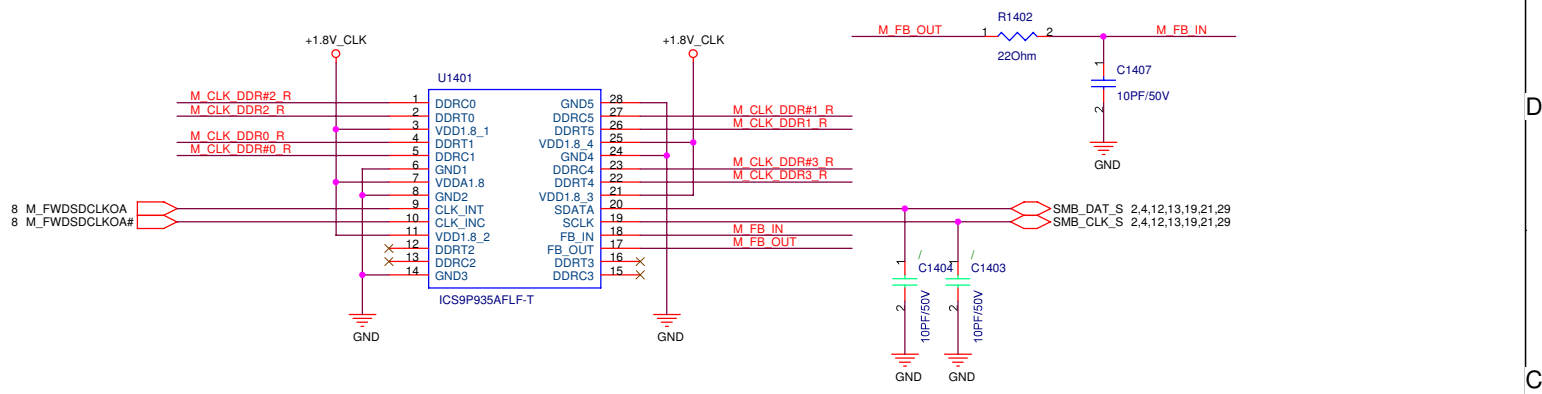
www.Dr-Bios.com



DDR2_DIMM200P
 PN:12G025C22002

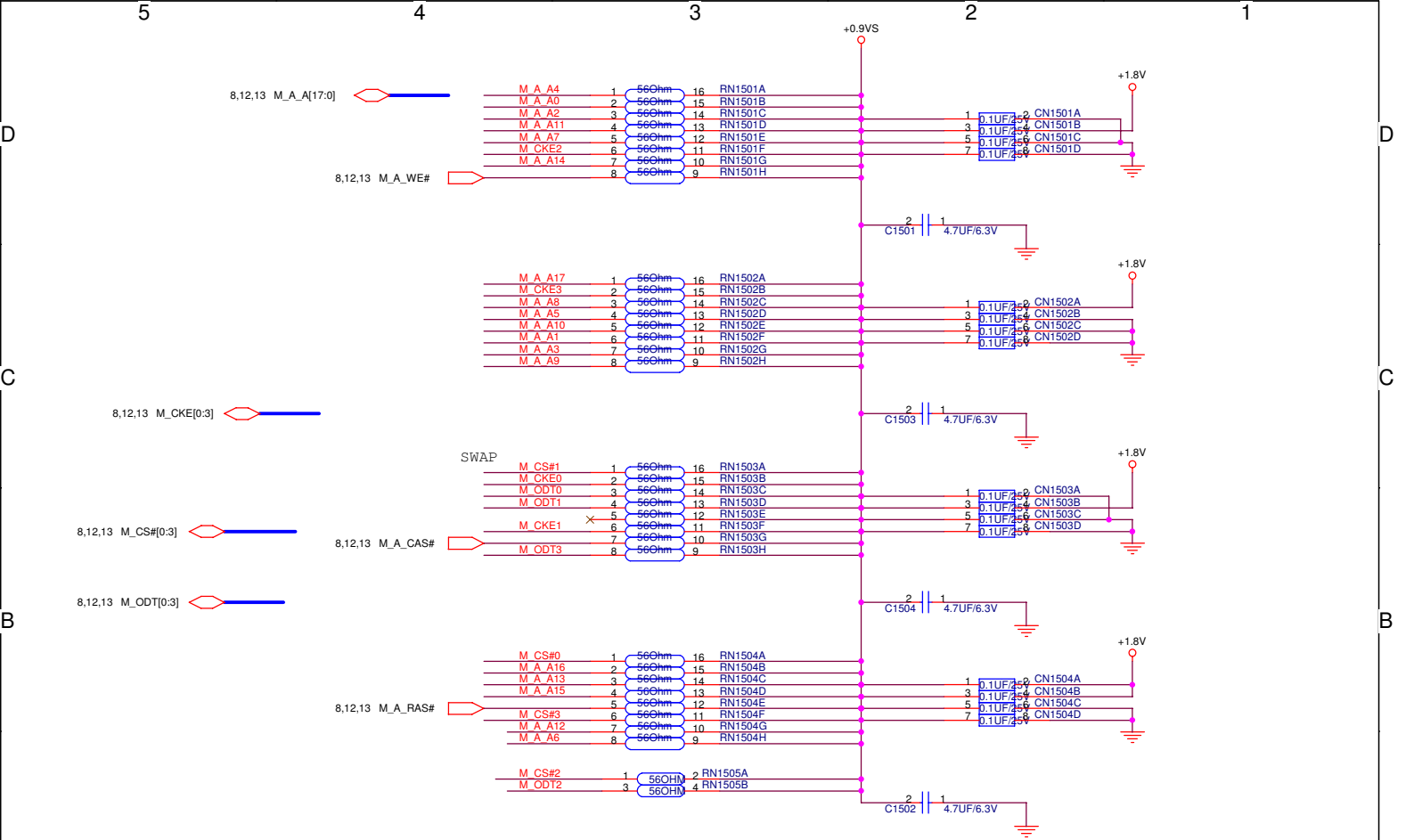
- M_CLK_DDR2
- C1303 10PF/5.0V
- M_CLK_DDR#2
- M_CLK_DDR3
- C1309 10PF/5.0V
- M_CLK_DDR#3

ASUS Title : DDR2 SO-DIMM2
 ASUSTek Computer INC Engineer: Hawk Zhu
 Size Project Name Rev
 A3 RSV
 Date: 08/14/07 Sheet 19 of 34



ASUS		Title : DDR2 BUFFER	
ASUSTeK Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A4	Project Name F5V		Rev 1.0
Date: 星期四, 四月 23, 2007		Sheet 14 of 94	


www.Dr-Bios.com



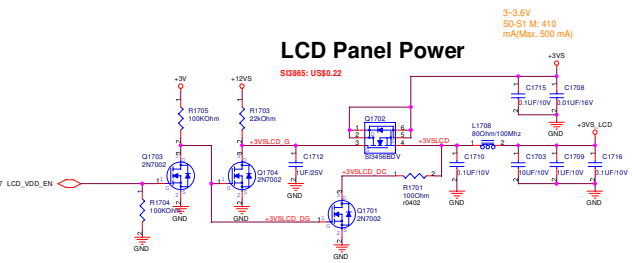
		Title :DDR2 TERMINATION	
ASUSTeK Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A4	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet 15 of 94	

www.Dr-Bios.com

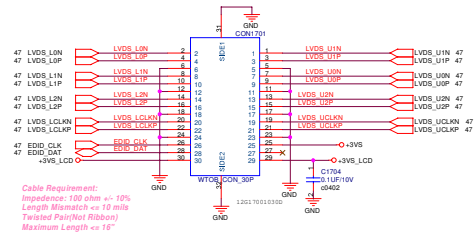
www.Dr-Bios.com

		Title : SIS	
ASUSTek Computer Inc.		Engineer: Hawk Zhu	
Size	Project Name	Rev	
C	FSV		1.0
Date: 2007-08-29 20:07	Sheet: 16	of	24

LCD Panel Power



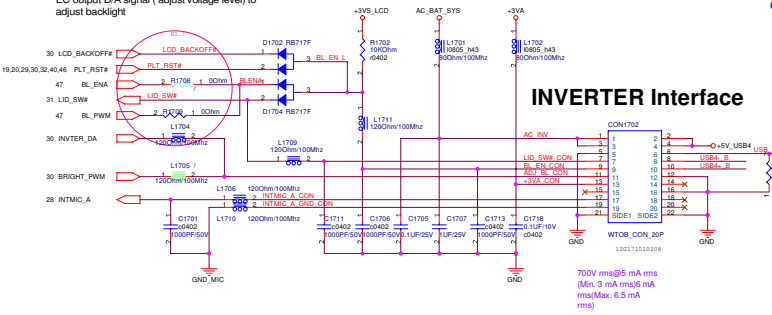
LCD LVDS Interface



Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 1ft

LCD Backlight Control

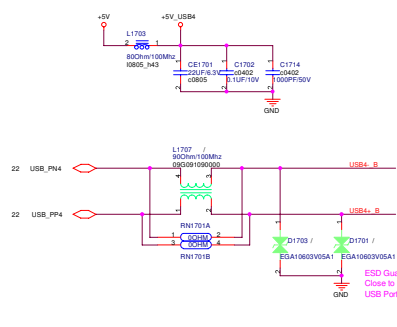
BIOS
 LCD_BACKOFF#
 When user push "F7+F7" button
 BIOS active this pin to turn
 On/Off backlight
 EC
 INVERTER_DA
 EC output D/A signal (adjust voltage level) to
 adjust backlight



INVERTER Interface

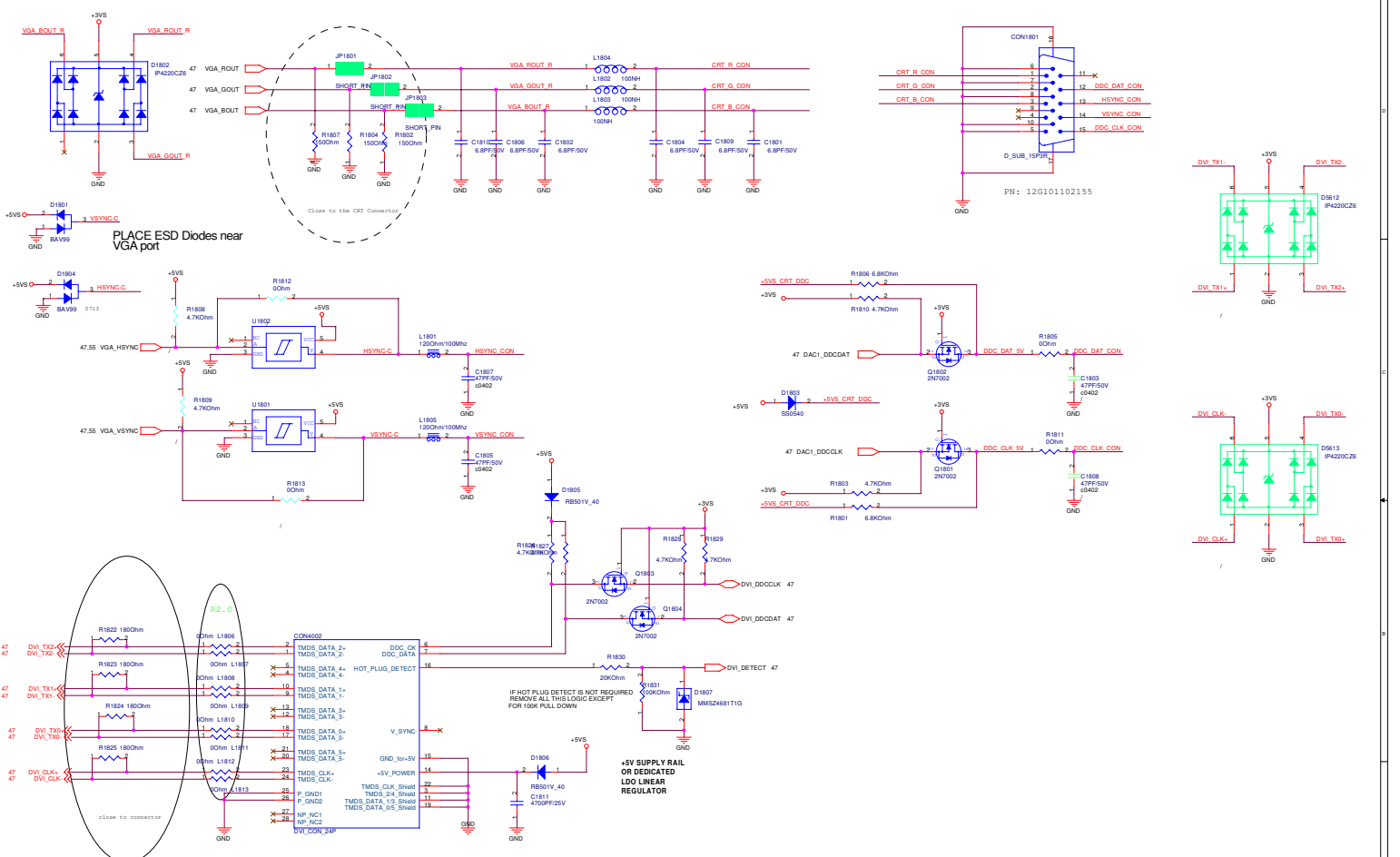
700V rms@5 mA rms
 (Min. 3 mA rms@5 mA rms)
 (Max. 6.5 mA rms)

USB4
 For
 CMOS
 Camera



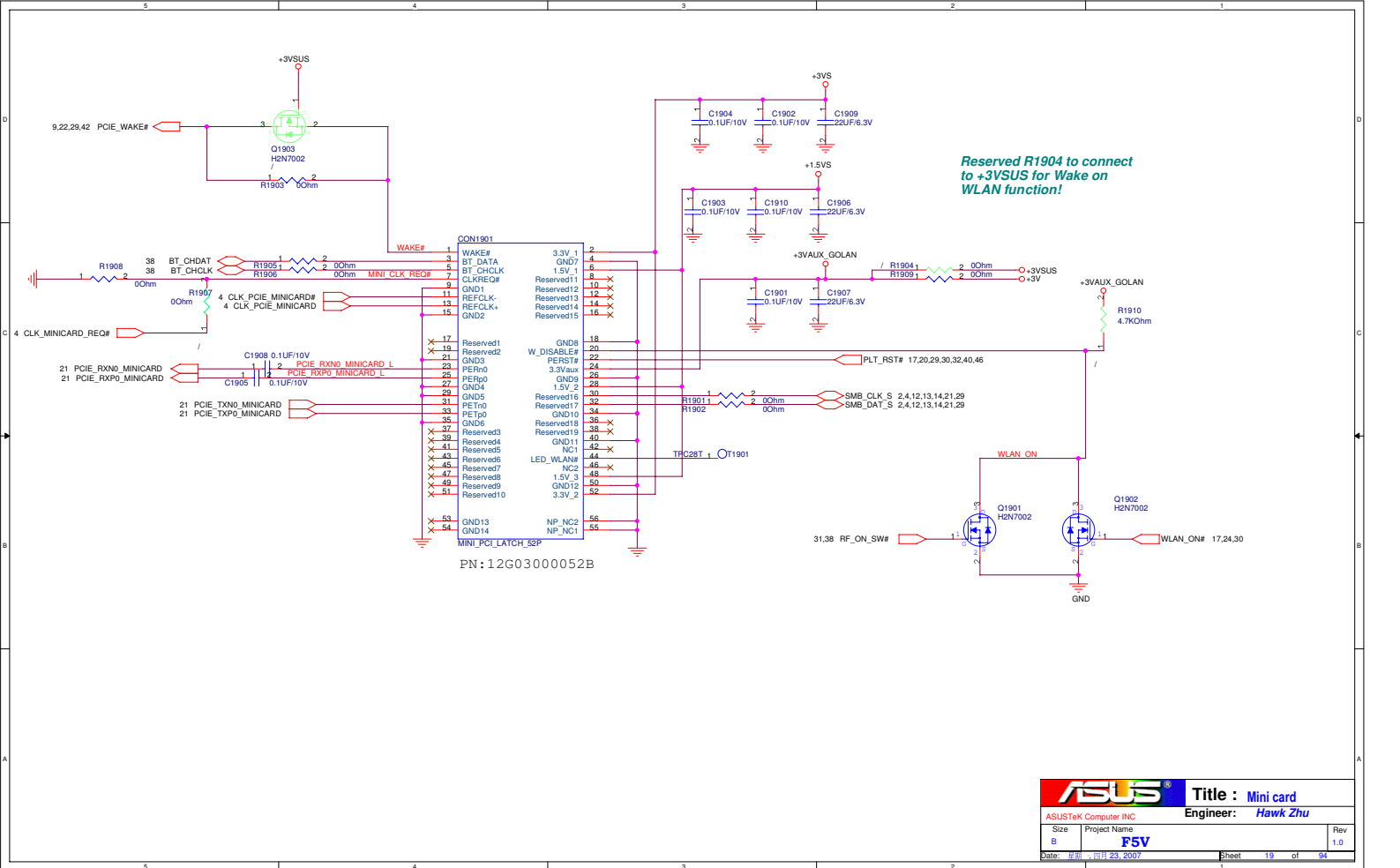
www.Dr-Bios.com

ASUS		Title : LVDS	
ASUSTek Computer Inc.		Engineer: Hawk Zhu	
BSZ	Project Name		Rev
C	FSV		1.0
Date: 2011-01-25-2007		Sheet: 17	of 24



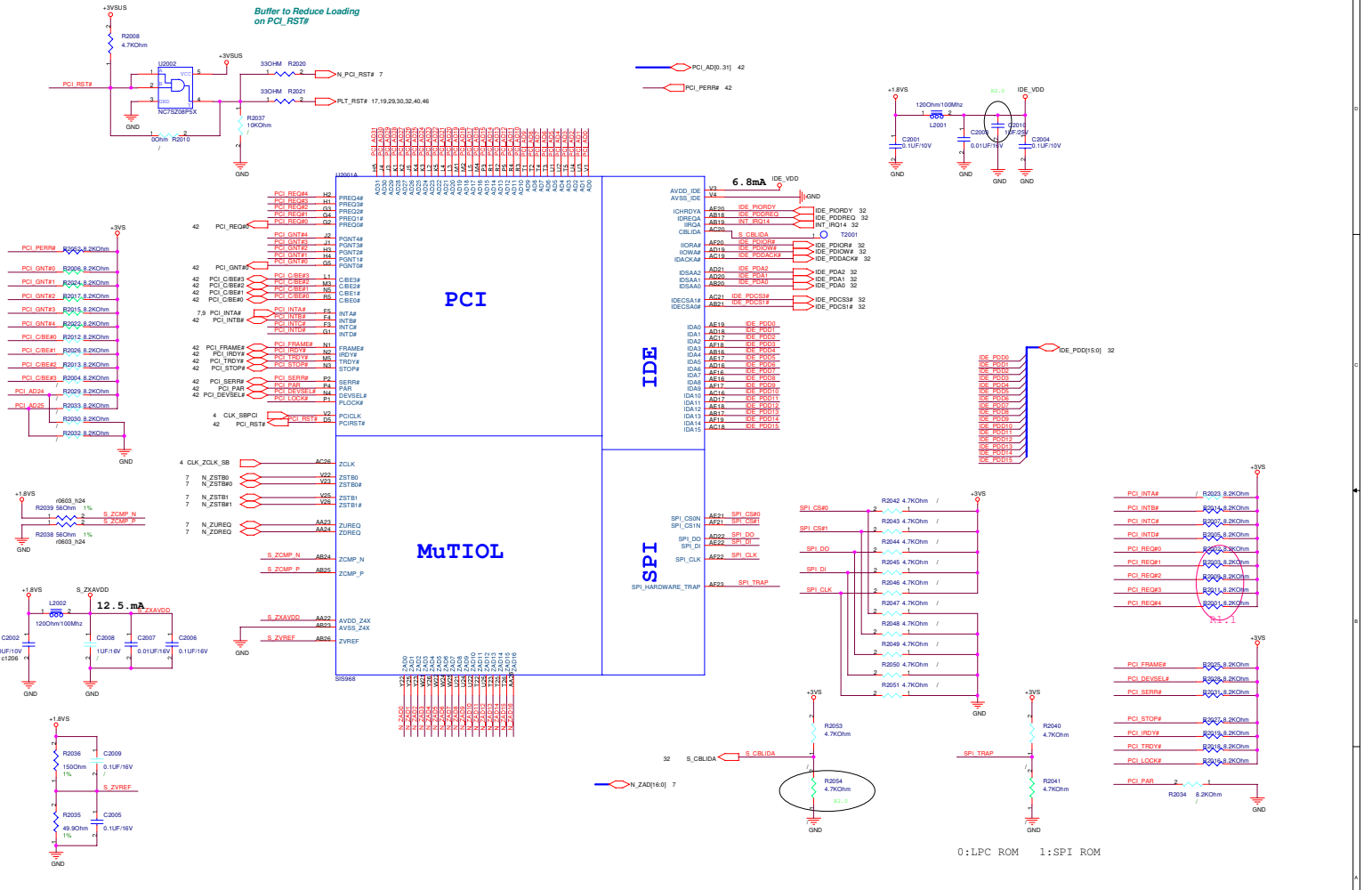
www.Dr-Bios.com

ASUS		Title : CRT&DVI	
ASUSTek Computer INC.		Engineer : Hawk Zhu	
Rev	Project Name	Rev	Rev
1	FSV	1.0	1.0
Date: 08-10-2007	Sheet: 18	of	24



ASUS		Title : Mini card	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
B	FSV		1.0
Date: # [] [] [] 23 2007	Sheet	19	of 94

www.Dr-Bios.com

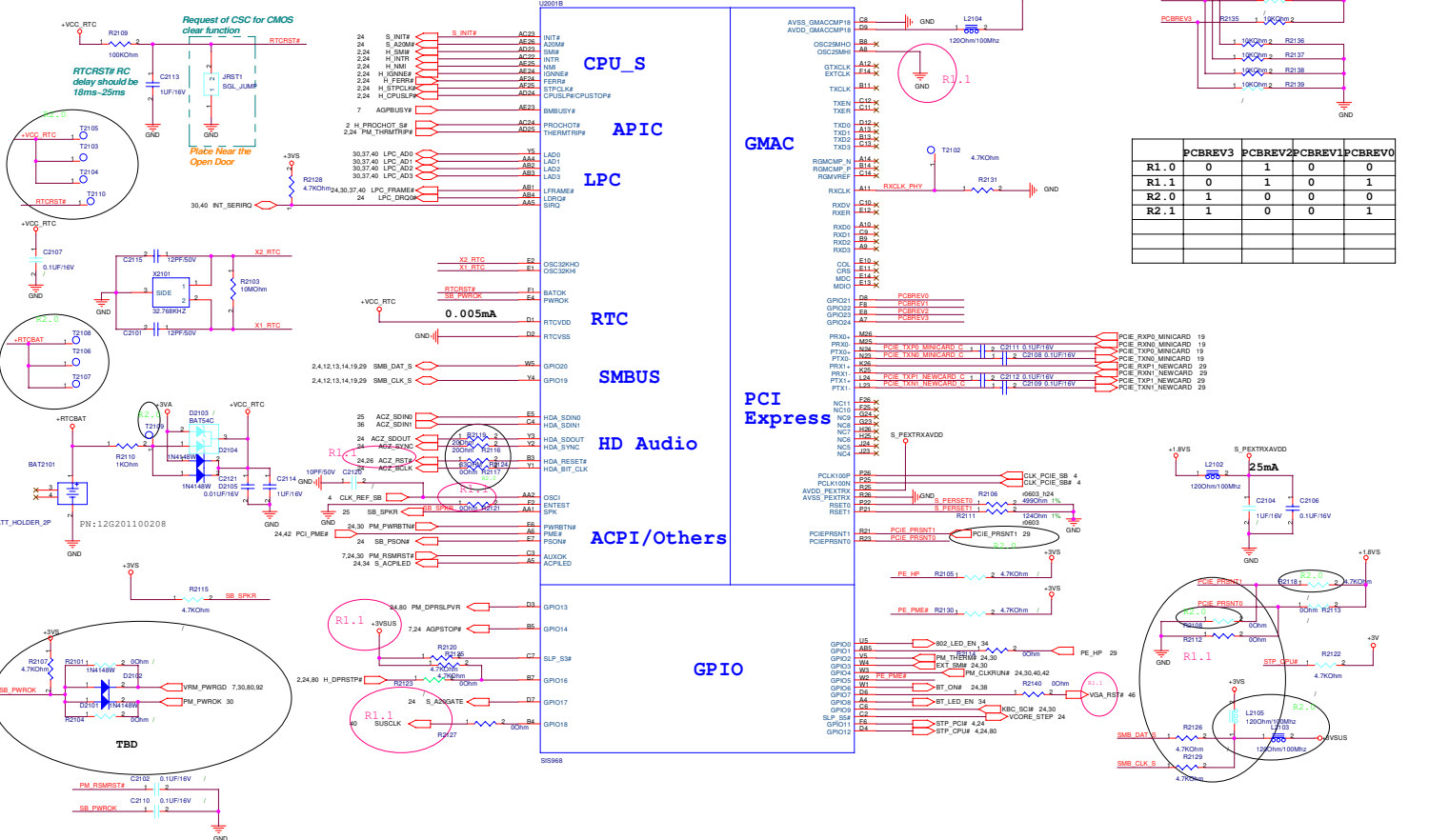
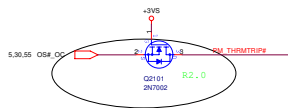


www.Dr-Bios.com

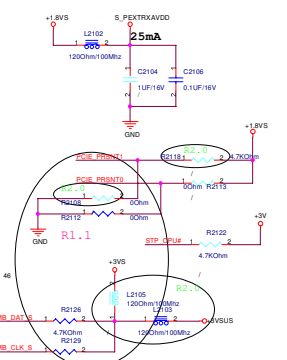
ASUS Title : 968 IDE/SPI/PCI/MuTIOL(1)

ASUSTeK COMPUTER INC. (NT) Engineer: Kaxidy Jiang

Size	Project Name	Rev
CS: ME	FSV	1.0
CS: ME	11/23/2007	Sheet 25 of 34

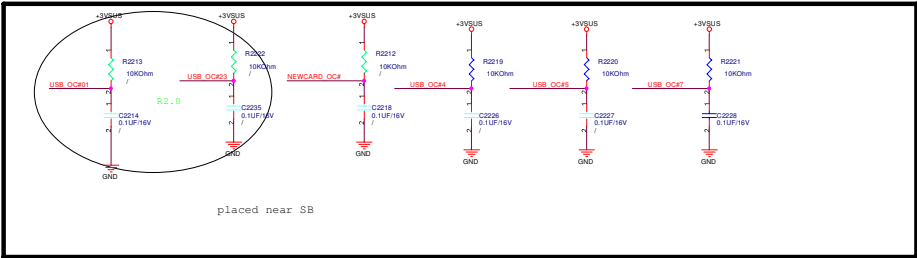
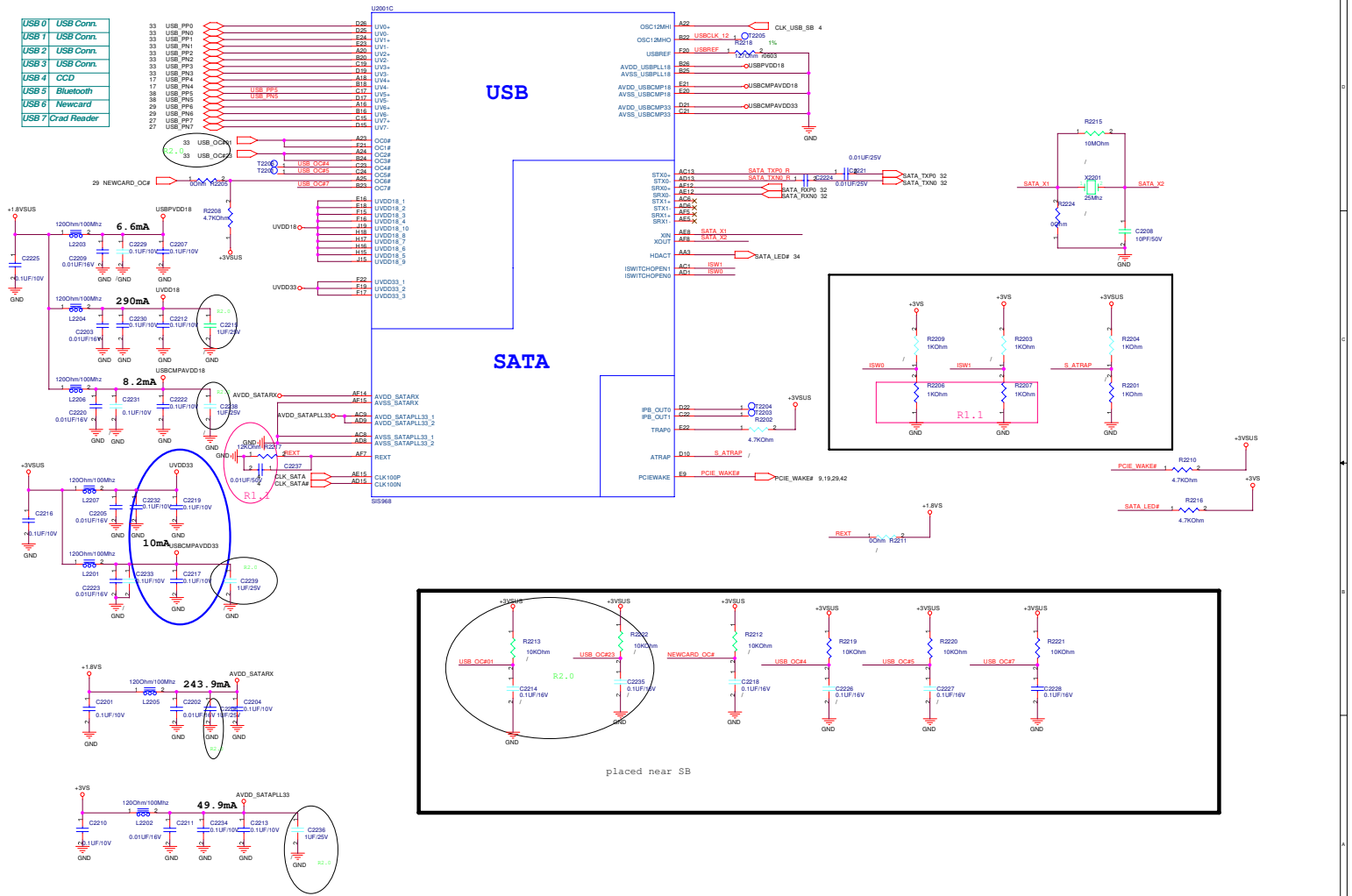


	PCBREV3	PCBREV2	PCBREV1	PCBREV0
R1.0	0	1	0	1
R2.0	1	0	0	0
R2.1	1	0	0	1



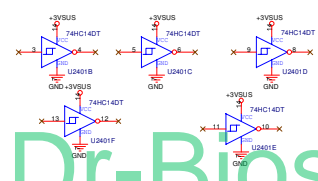
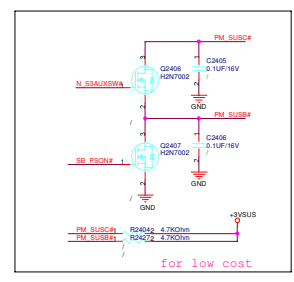
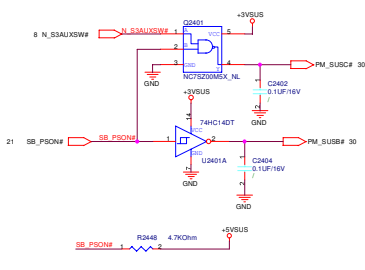
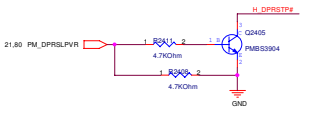
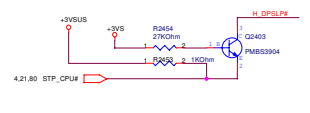
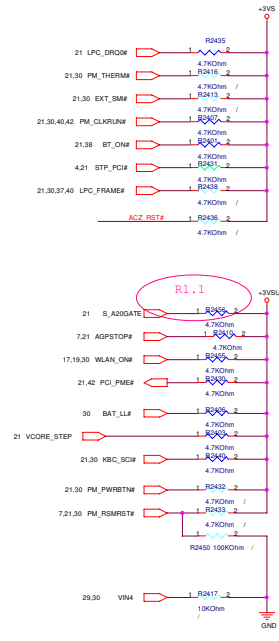
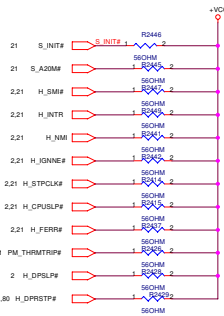
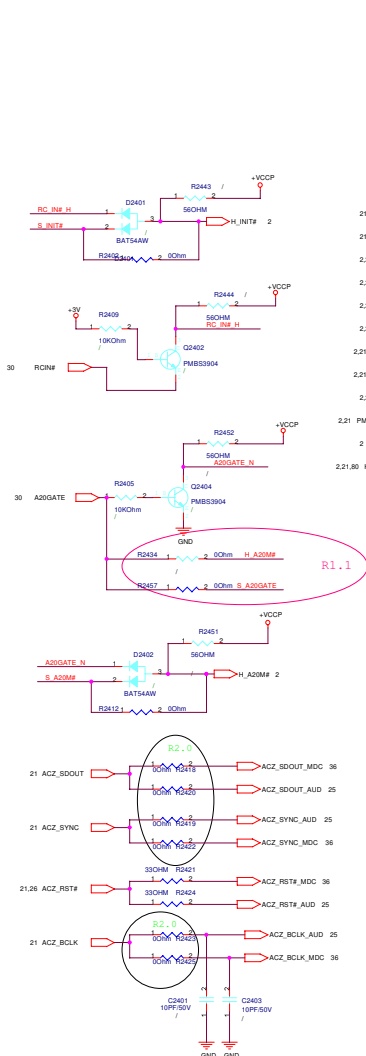
ASUS 8-PCIE(AUDIO/ACPI/GPIO2) Title
 ASUS COMPUTER INC. NET Engineer: Kaxidy Jjiang
 S/Sa Project Name: F5V
 C Date: 2011/03/20/2011 B/Sap 21 of 24

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	CCD
USB 5	Bluetooth
USB 6	Newcard
USB 7	Crad Reader



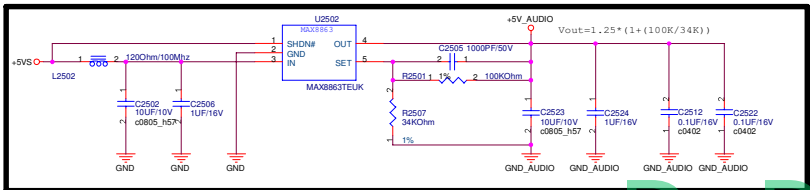
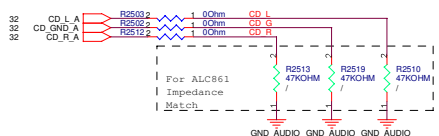
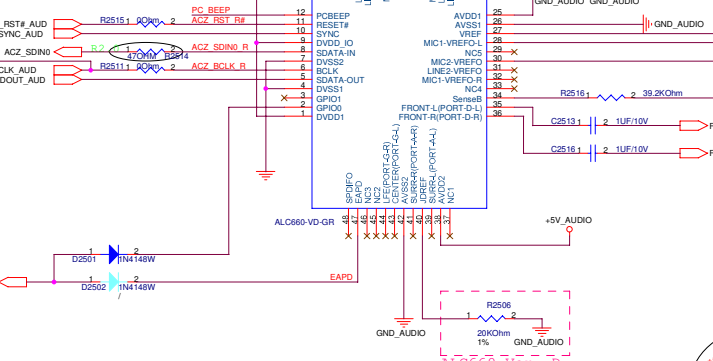
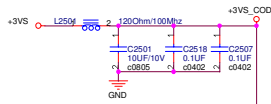
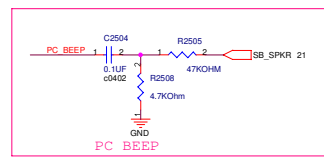
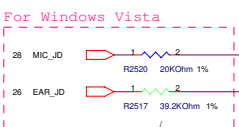
www.Dr-Bios.com

ASUS		Title : 968 USB/SATA(3)	
ASUSTEK COMPUTER INC. NBY			
Src	Project Name	Rev	
C	FSV	1.0	
Date: 11/11/2011			



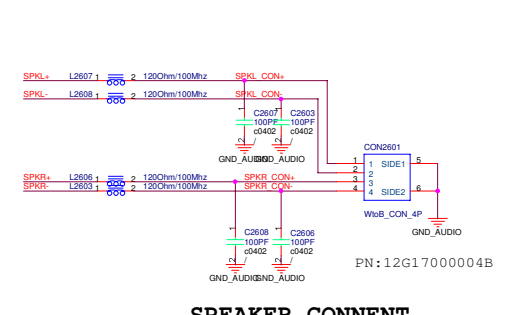
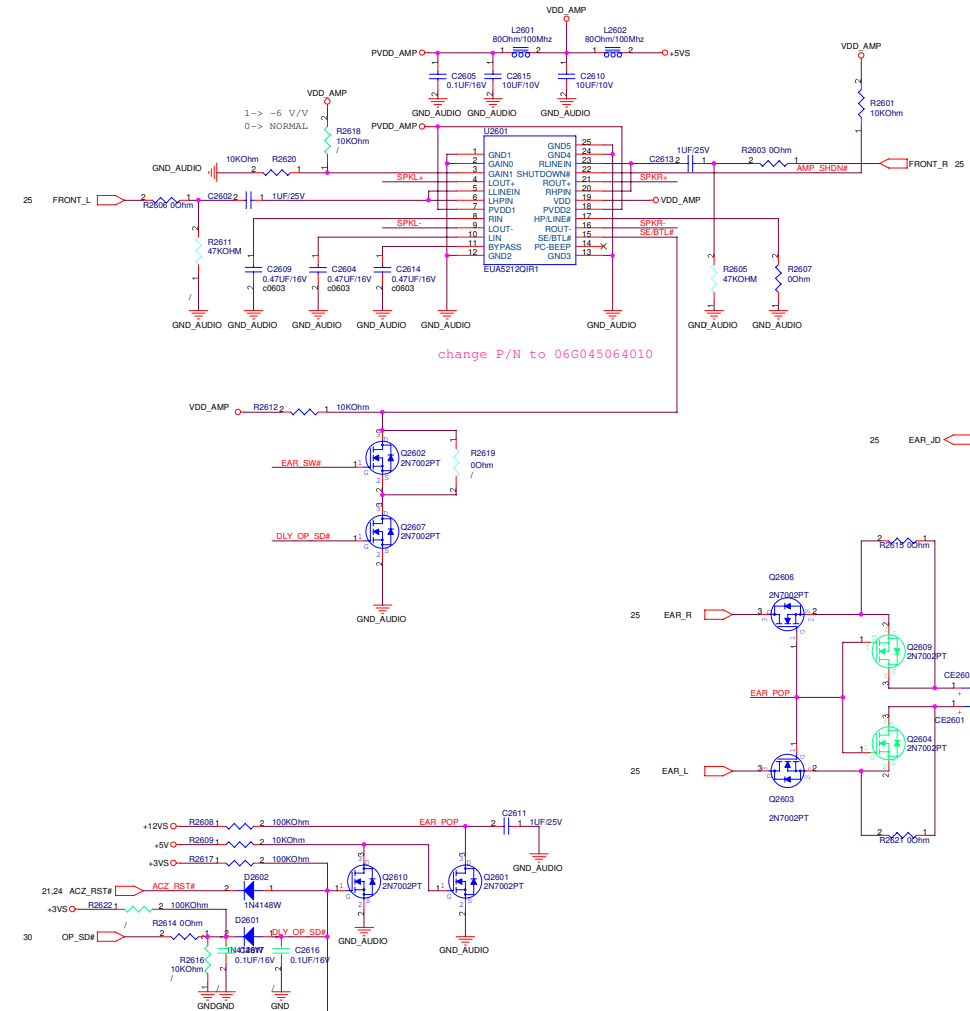
www.Dr-Bios.com

26 EAR_R
26 EAR_L

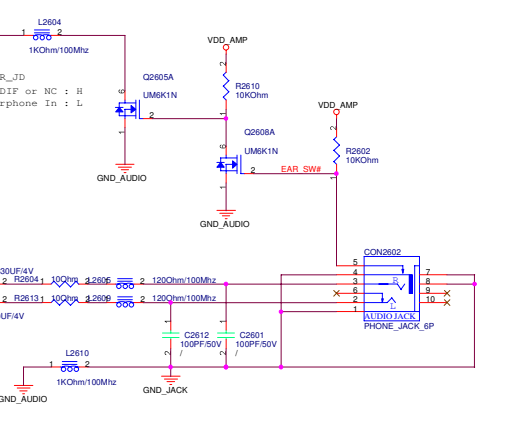
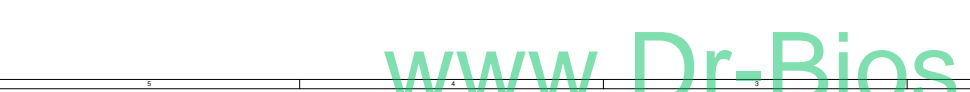


ASUS Title : AZALIA
Engineer: Kaxidy Jiang
Project Name: F5V
Date: 03/23/2007 Sheet 25 of 94

www.Dr-Bios.com

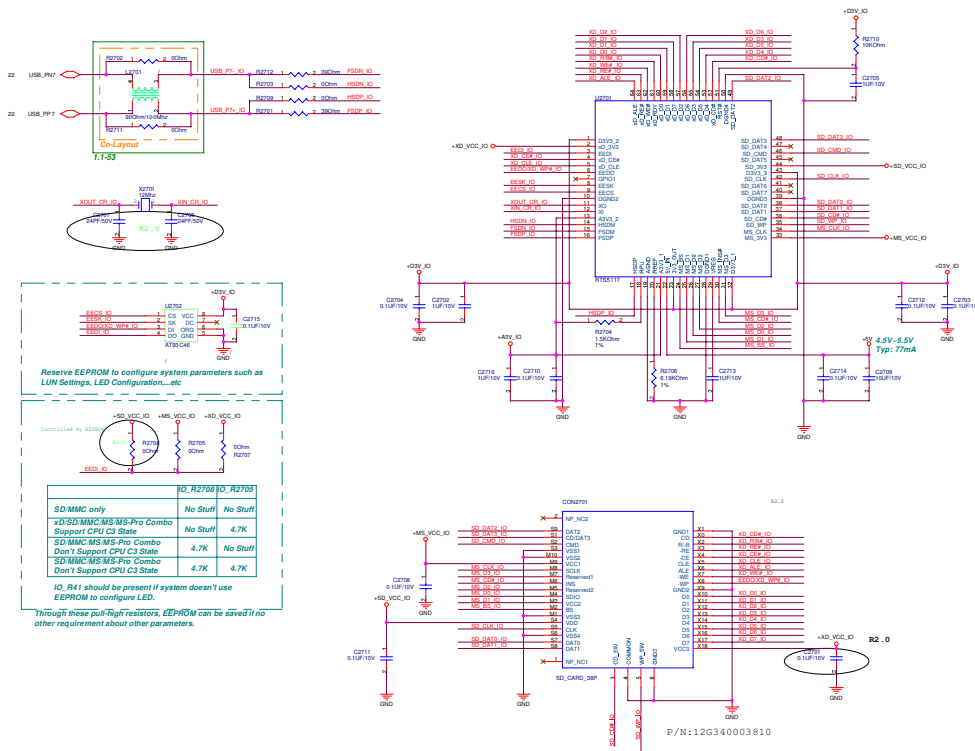


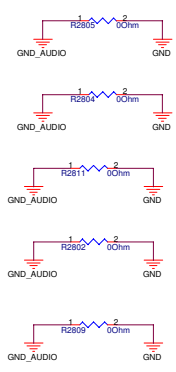
SPEAKER CONNET



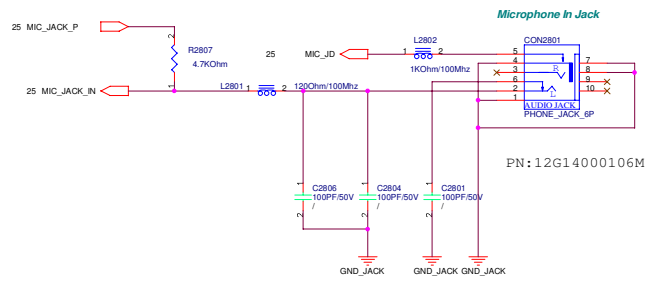
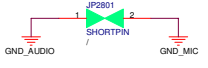
ASUS		Title : AMPLIFIER 2 CHANNEL	
-<OrigName>		Engineer: Kaxidy Jiang	
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 11/19/23/2007	Sheet 26	of 34	

www.Dr-Bios.com

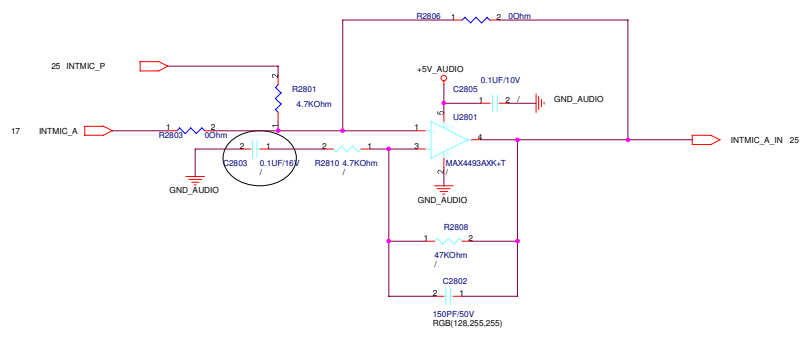




INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



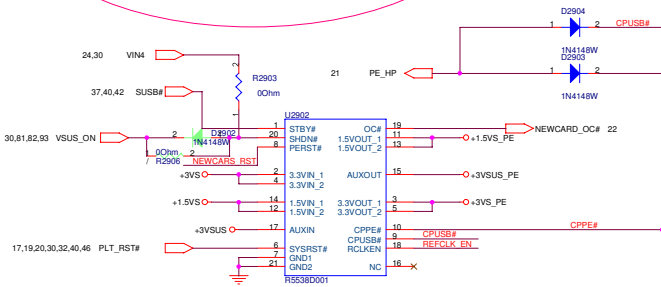
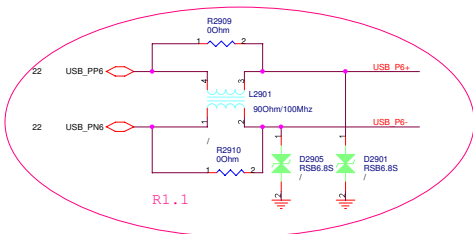
Pre-AMP For Test Function



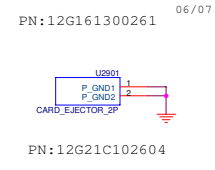
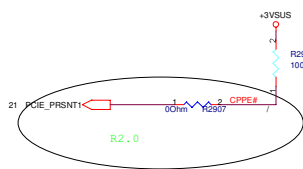
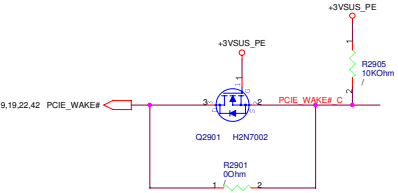
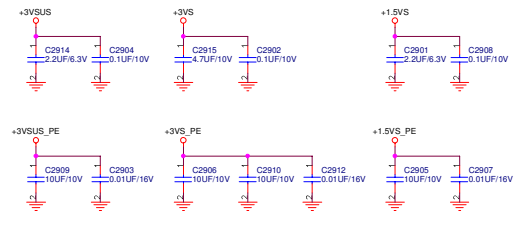
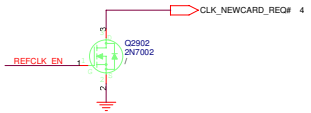
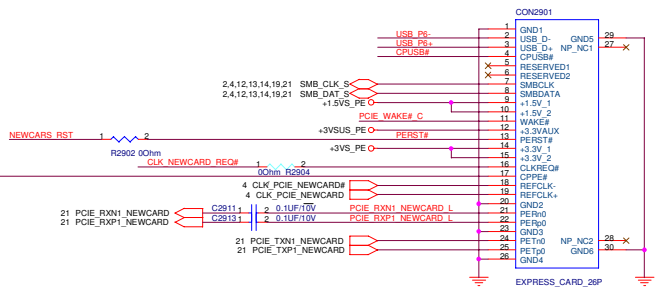
ASUS		Title : MIC.LINE-IN JACK	
-OrigName-		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 11/19/2007		Sheet 28	of 94

www.Dr-Bios.com

FOR SWAP



!ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V



<Variant Names>

ASUS		Title : NEWCARD	
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Date	Rev
Custom	FSV	11/11/2007	1.0
		Sheet	29 of 34

www.Dr-Bios.com

For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
don't connect to Battery
Connector.

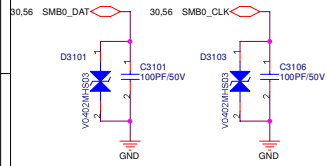
Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
must connect to Battery
Connector.

Note:

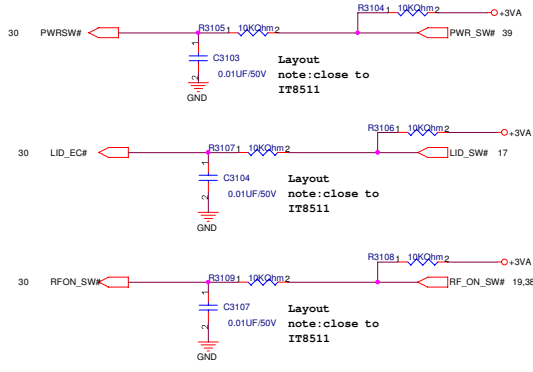
When we plug in or plug out the
battery, it may cause a spike to
damage the EC and gas gauge. It
needed to add these varistors to
protect those pins.

close to connector



For Switch

For Switch



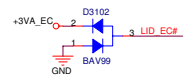
PWR SWITCH

LID SWITCH

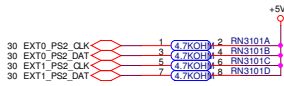
RF SWITCH

Note:

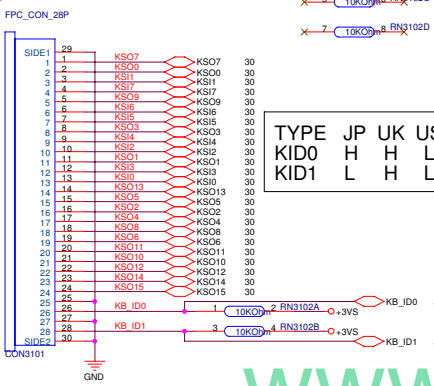
This LID_EC# is a signal
from inverter board, it is
easy to cause high voltage
damage when plugging
inverter board connector to
M/B with AC present. It
needed to add bidirectional
diode to protect this pin.



For External PS/2 I/F

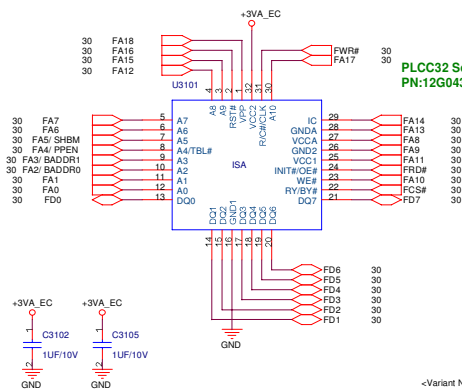


For Keyboard



TYPE JP UK US
KID0 H H L
KID1 L H L

For 4M bits ISA ROM



Note:

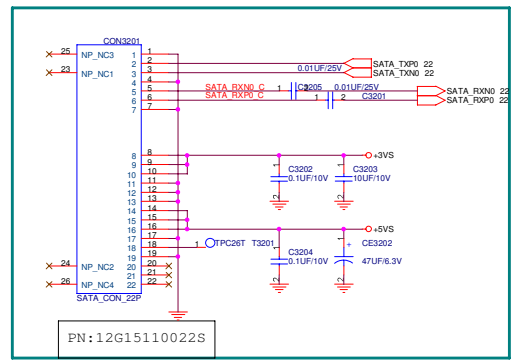
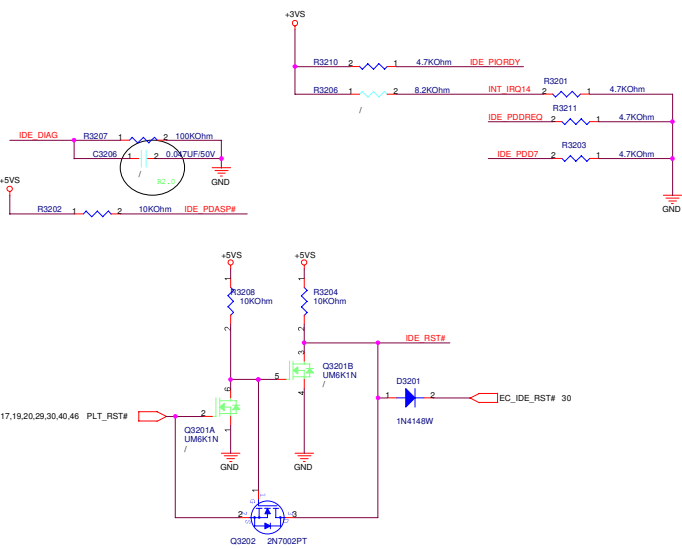
If you use 8M bits ROM, you need
to connect FA19 to EC side.

PLCC32 Socket
PN:12G04300032F

SST-PLCC32 4Mbits Flash ROM
PN:05G001027221

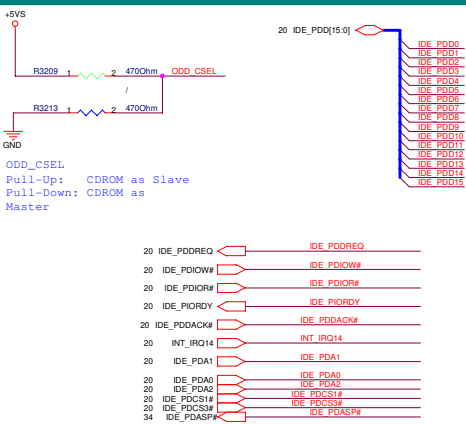
<-Variant Name>

ASUS		Title :KB&ISA ROM	
ASUSTek COMPUTER INC. NBI		Engineer: Kaxidy Jiang	
Size	Project Name	Rev	1.0
Custom	F5V		
Date: 01/01 - 01/11 23, 2007		Sheet	31 of 94

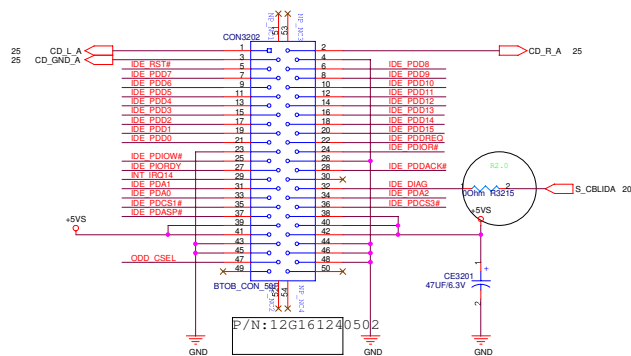


Dafault

SATA



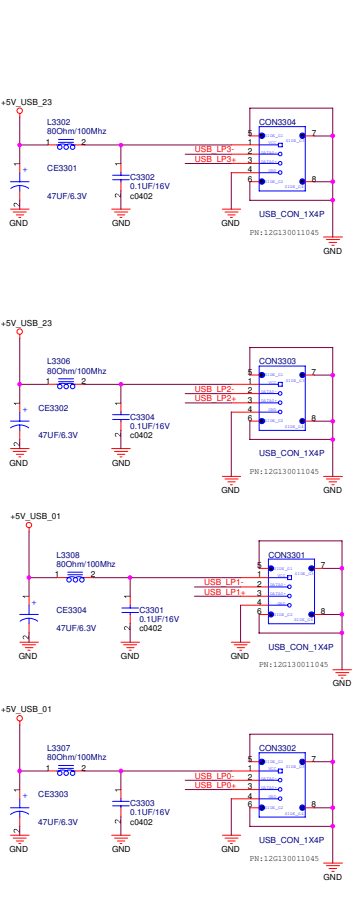
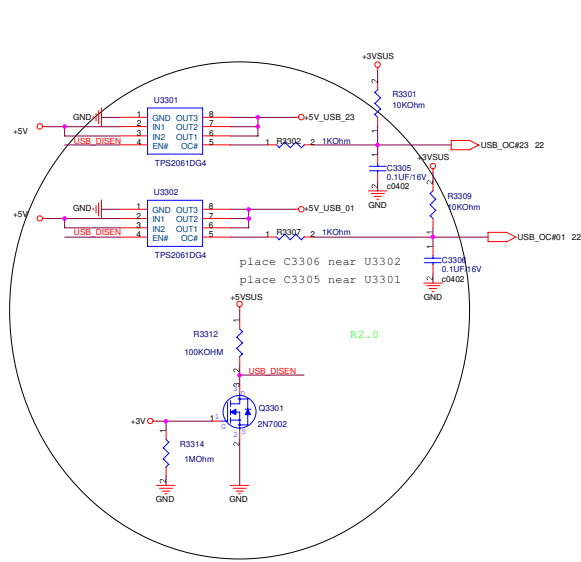
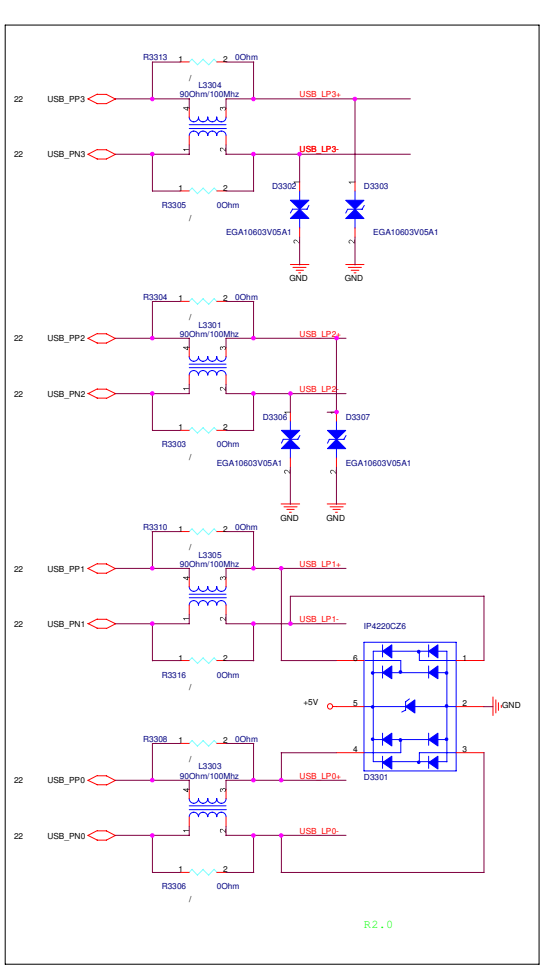
CD-ROM



<Variant Name>

ASUS		Title : HDD & CD-ROM	
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	1.0
Custom	FSV		
Date: 2007.11.23		Sheet	42 of 94

www.Dr-Bios.com

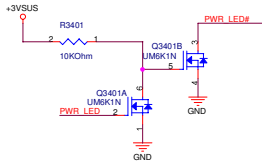
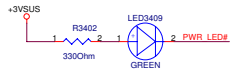


<Variant Name>

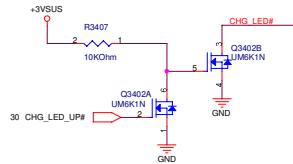
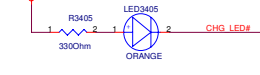
ASUS		Title : USB CONN	
ASUSTeK COMPUTER INC. NBI		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
Custom	F5V		1.0
Date: #01-10TH 23, 2007		Sheet	33 of 84

www.Dr-Bios.com

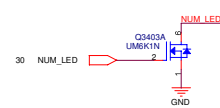
For POWER LED



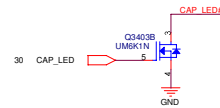
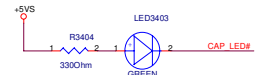
BATTERY LED



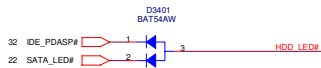
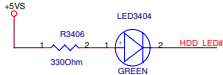
Num Lock



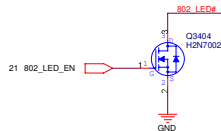
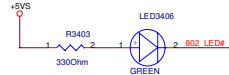
Cap Lock



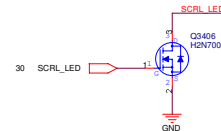
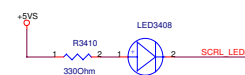
SATA/IDE LED



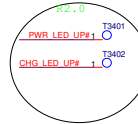
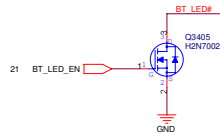
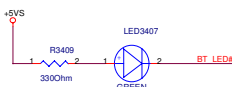
Wireless LED



Scroll Lock



BT LED



www.Dr-Bios.com

<Variant Name>

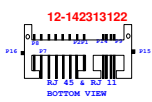
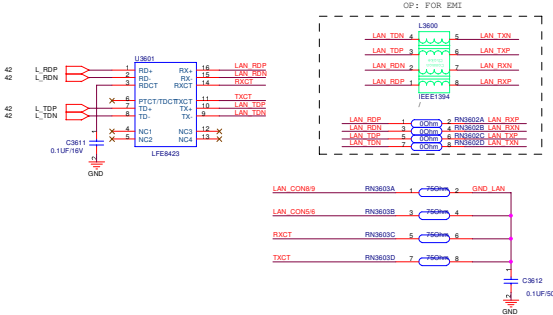
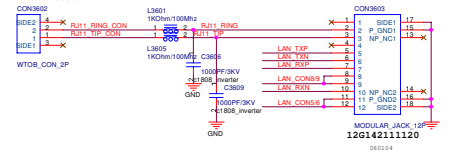
ASUS		Title : LED	
ASUSTeK COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/11/2007	Sheet	34	of 34



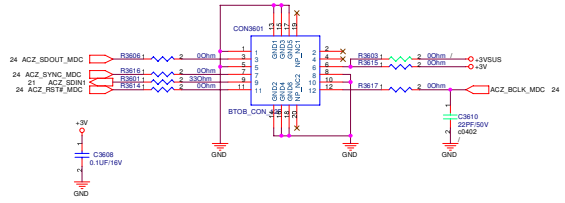
www.Dr-Bios.com

LAN PORT

12G17100002E

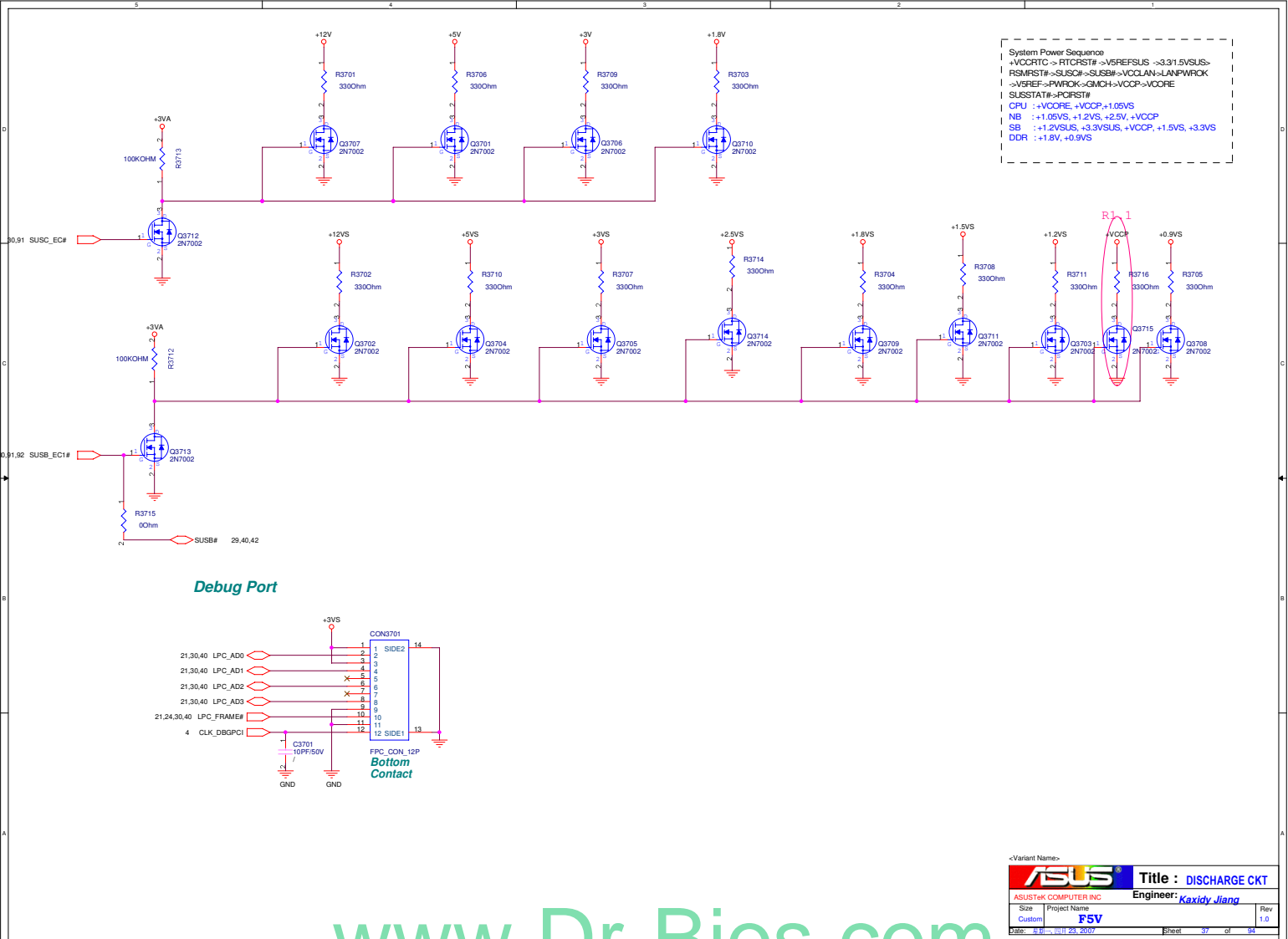


MDC

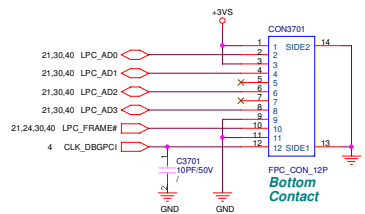


www.Dr-Bios.com

ASUS		Title : RJ11+AS & MDC	
ASUSTEK COMPUTER INC		Engineer: <i>Kaxidy Jjiang</i>	
Size	Project Name	Rev	
C	FSV	1.0	
Doc: 818	10/28/2007	Sheet: 35	of 34



Debug Port



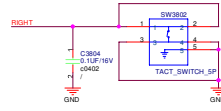
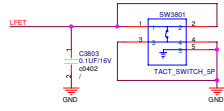
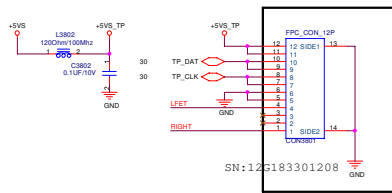
<Variant Names>

ASUS		Title : DISCHARGE CKT	
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/11/2007		Sheet	37 of 34

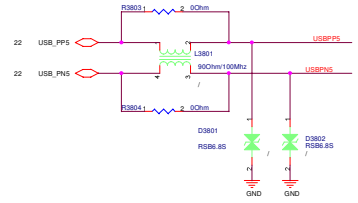
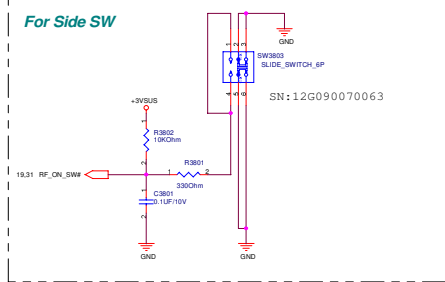
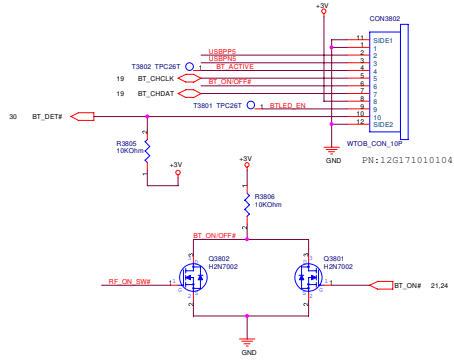
www.Dr-Bios.com

Touch-Pad

R1.1



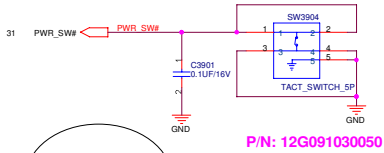
For Bluetooth



www.Dr-Bios.com

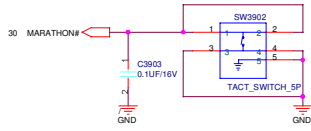
ASUS		Title :BT&TP
ASUSTeK COMPUTERS INC. NET		Engineer:Kaxidy-Jiang
Sira	Project Name	Rev
C	FSV	1.0
Code: 10133-8007	ESDsn	38 of 34

Power SW.

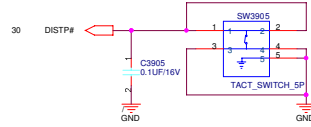


P/N: 12G091030050

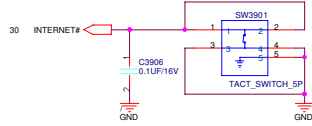
Marathon SW.



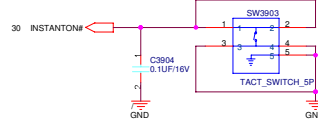
Disable Touch Pad SW.



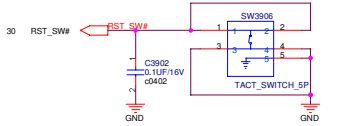
Internet SW.



IstantON SW.



RESET SW.

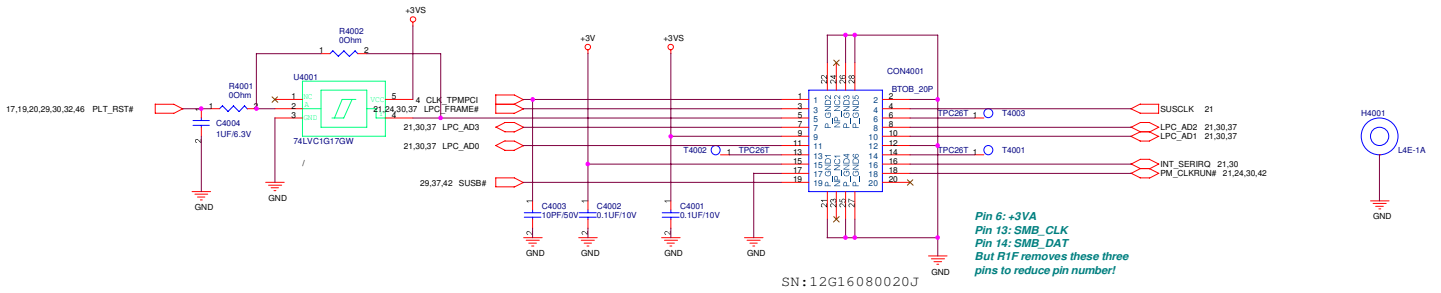


P/N: 12G091030050

<Variant Name>

ASUS		Title : SWITCH	
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy jiang</i>	
Size: Custom	Project Name: FSV	Rev: 1.0	
Date: 2007.11.23	Sheet: 39	of 94	

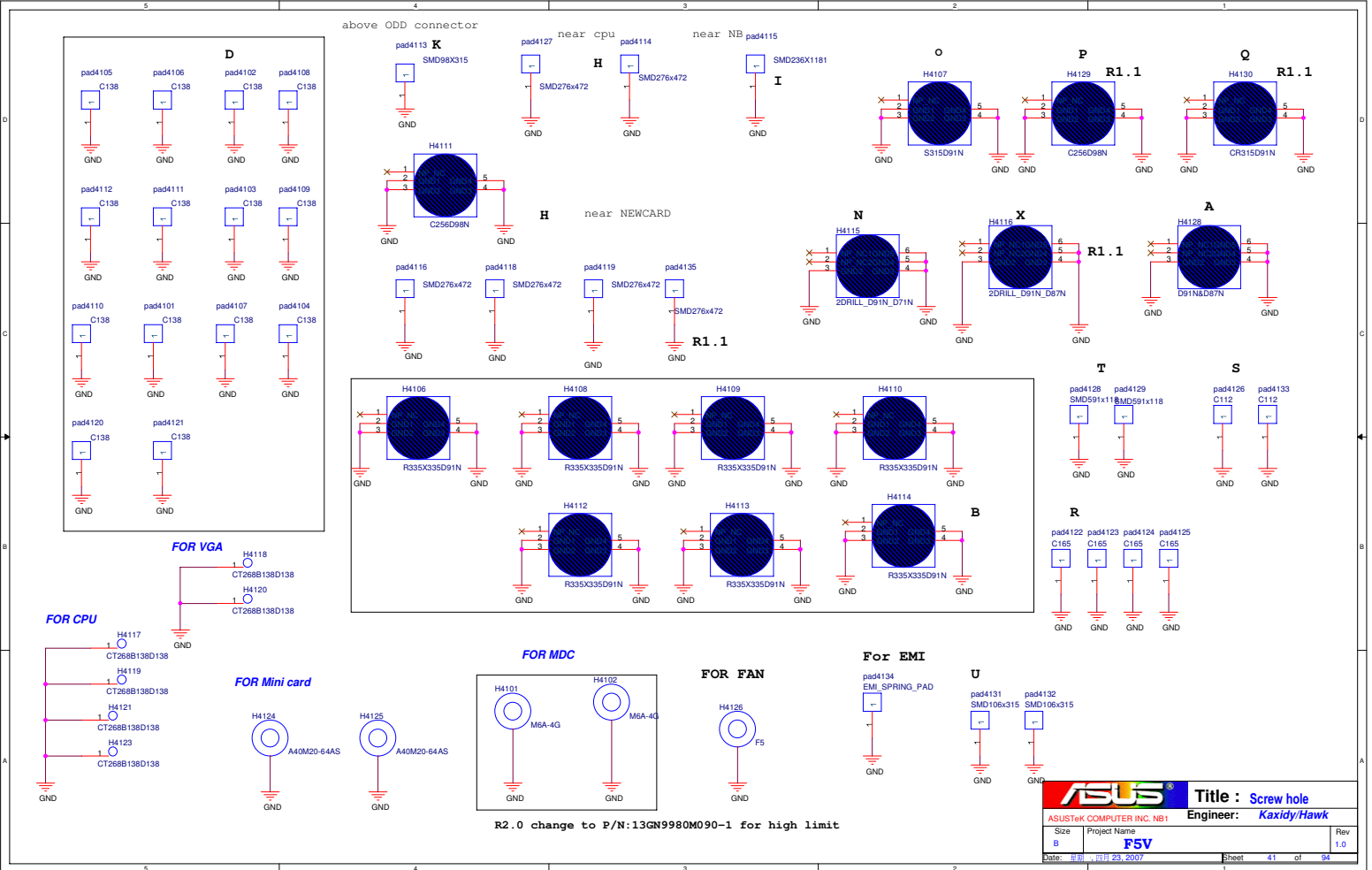
For TPM Module



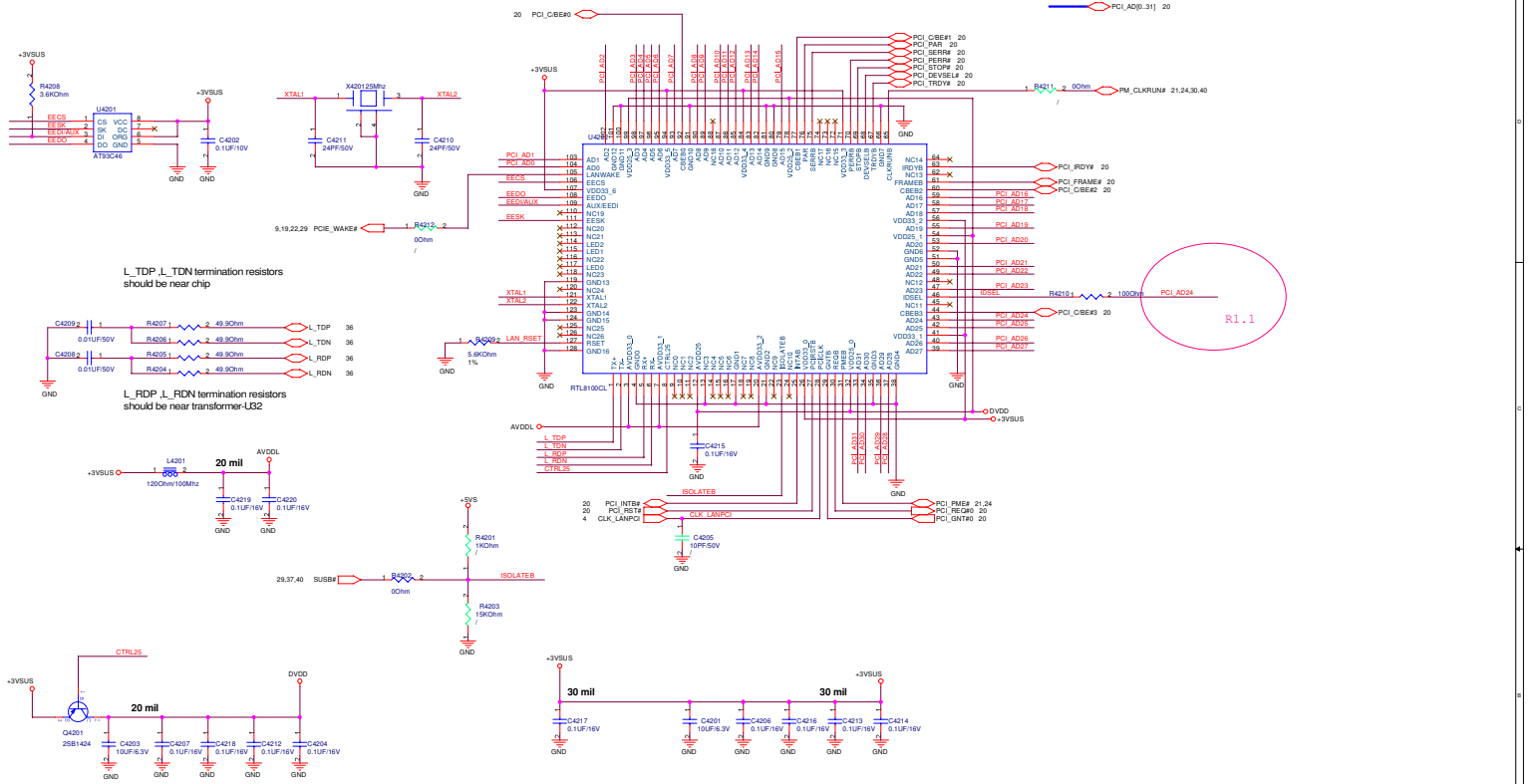
<Variant Name>

ASUS		Title : TPM
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy Jiang
Size	Project Name	Rev
Custom	FSV	1.0
Date: 2007.11.23	Sheet	46 of 94

www.Dr-Bios.com



www.Dr-Bios.com



www.Dr-Bios.com

ASUS		Title : LAN	
ASUSTeK COMPUTER INC. (TAIPEI)		Engineer: KaxidyHawk	
Size	Project Name	Rev	
C	FSV	1.0	
Date: 08-10-2007	Sheet: 41	of	49

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 43 of 94

www.Dr-Bios.com

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 44 of 94

www.Dr-Bios.com

D

D

C


C

B

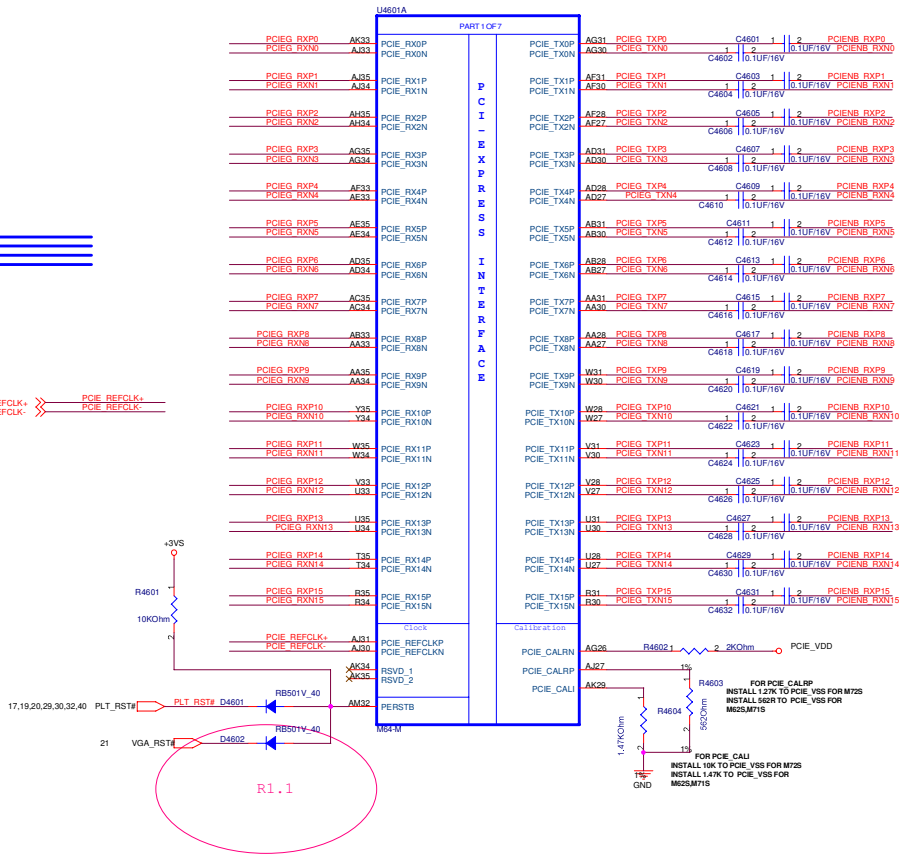
B

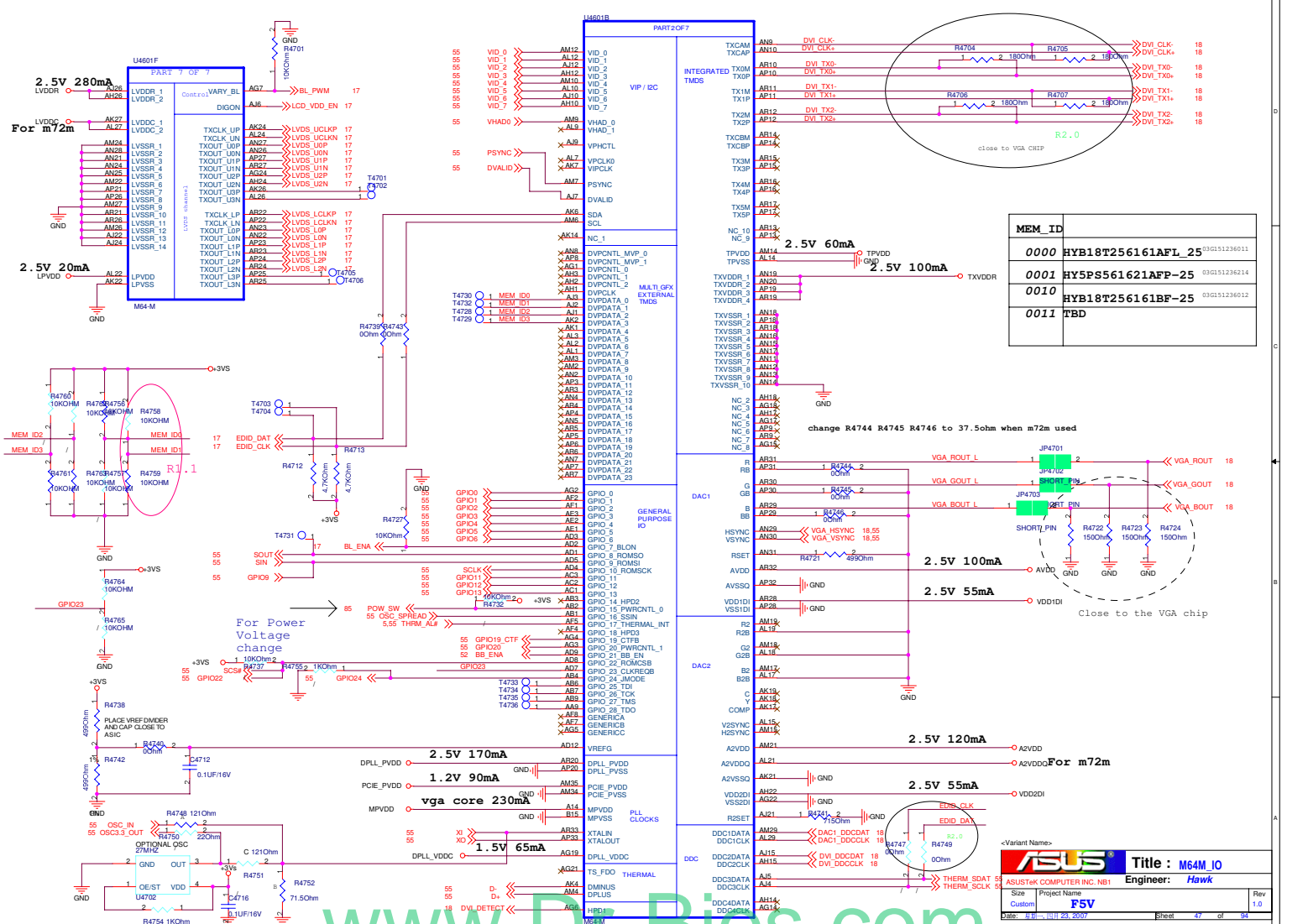
A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 45 of 94

www.Dr-Bios.com



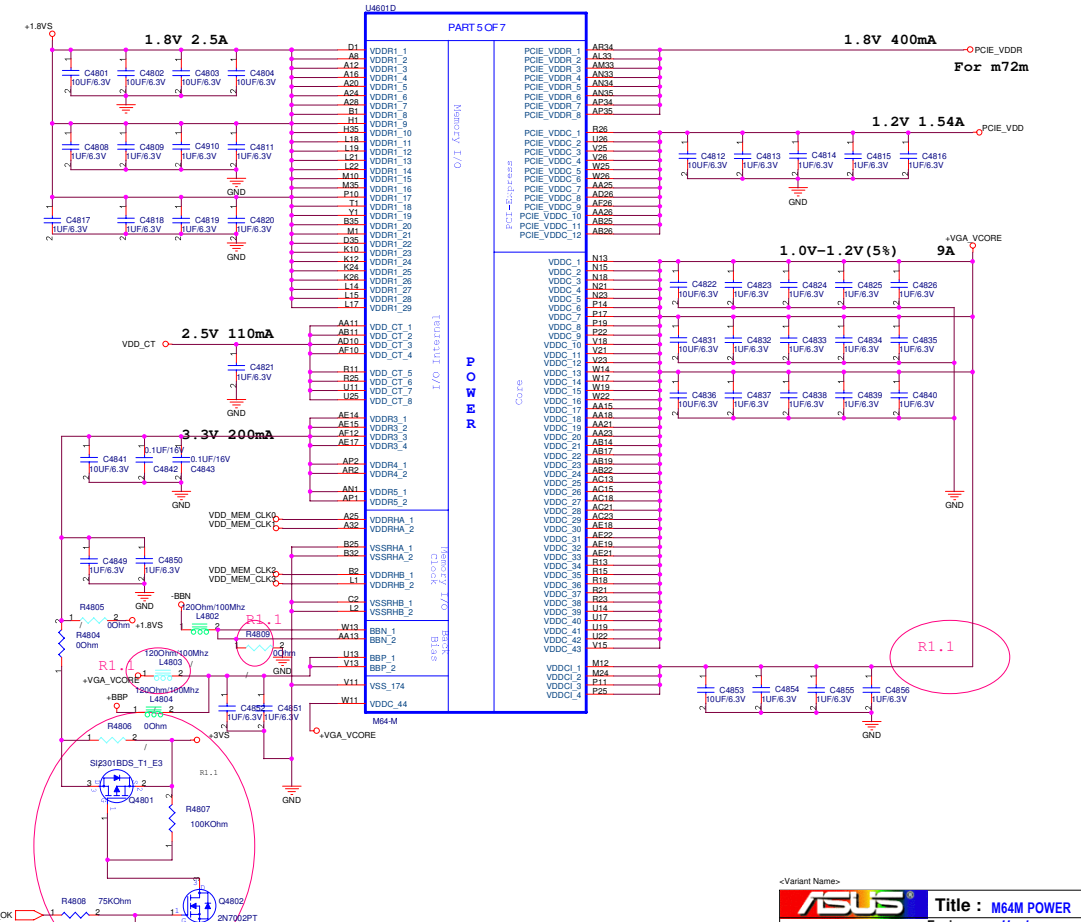


MEM ID	
0000	HYB18T256161AFL_25 03G151236011
0001	HY5PS561621AFP-25 03G151236214
0010	HYB18T256161BF-25 03G151236012
0011	TBD

ASUS		Title : M64M IO	
ASUSTeK COMPUTER INC. NBI		Engineer: Hawk	
Size	Project Name	Date	Rev
FSV			1.0
Date: 11/23/2007		Sheet 47 of 94	

www.Dr-Bios.com

P34	PCIE_VSS_1	VSS_65	L33
P35	PCIE_VSS_2	VSS_66	M3
P36	PCIE_VSS_3	VSS_67	M8
P37	PCIE_VSS_4	VSS_68	K28
P38	PCIE_VSS_5	VSS_69	M2
P39	PCIE_VSS_6	VSS_70	N14
P40	PCIE_VSS_7	VSS_71	N17
P41	PCIE_VSS_8	VSS_72	N19
P42	PCIE_VSS_9	VSS_73	N22
P43	PCIE_VSS_10	VSS_74	N25
P44	PCIE_VSS_11	VSS_75	N3
P45	PCIE_VSS_12	VSS_76	N5
P46	PCIE_VSS_13	VSS_77	R5
P47	PCIE_VSS_14	VSS_78	U8
P48	PCIE_VSS_15	VSS_79	P13
P49	PCIE_VSS_16	VSS_80	E14
P50	PCIE_VSS_17	VSS_81	E18
P51	PCIE_VSS_18	VSS_82	E23
P52	PCIE_VSS_19	VSS_83	E28
P53	PCIE_VSS_20	VSS_84	E34
P54	PCIE_VSS_21	VSS_85	E39
P55	PCIE_VSS_22	VSS_86	E45
P56	PCIE_VSS_23	VSS_87	U8
P57	PCIE_VSS_24	VSS_88	E10
P58	PCIE_VSS_25	VSS_89	E15
P59	PCIE_VSS_26	VSS_90	E21
P60	PCIE_VSS_27	VSS_91	E27
P61	PCIE_VSS_28	VSS_92	E33
P62	PCIE_VSS_29	VSS_93	E39
P63	PCIE_VSS_30	VSS_94	V3
P64	PCIE_VSS_31	VSS_95	K43
P65	PCIE_VSS_32	VSS_96	L10
P66	PCIE_VSS_33	VSS_97	L17
P67	PCIE_VSS_34	VSS_98	L15
P68	PCIE_VSS_35	VSS_99	L18
P69	PCIE_VSS_36	VSS_100	U21
P70	PCIE_VSS_37	VSS_101	V7
P71	PCIE_VSS_38	VSS_102	M3
P72	PCIE_VSS_39	VSS_103	V10
P73	PCIE_VSS_40	VSS_104	V10
P74	PCIE_VSS_41	VSS_105	V14
P75	PCIE_VSS_42	VSS_106	V17
P76	PCIE_VSS_43	VSS_107	V19
P77	PCIE_VSS_44	VSS_108	V22
P78	PCIE_VSS_45	VSS_109	V25
P79	PCIE_VSS_46	VSS_110	V27
A2	VSS_1	VSS_111	W1
A3	VSS_2	VSS_112	W10
A4	VSS_3	VSS_113	W15
A5	VSS_4	VSS_114	W18
A6	VSS_5	VSS_115	W21
A7	VSS_6	VSS_116	W23
A8	VSS_7	VSS_117	W26
A9	VSS_8	VSS_118	W29
A10	VSS_9	VSS_119	W32
A11	VSS_10	VSS_120	W35
A12	VSS_11	VSS_121	W38
A13	VSS_12	VSS_122	W41
A14	VSS_13	VSS_123	W44
A15	VSS_14	VSS_124	W47
A16	VSS_15	VSS_125	W50
A17	VSS_16	VSS_126	W53
A18	VSS_17	VSS_127	W56
A19	VSS_18	VSS_128	W59
A20	VSS_19	VSS_129	W62
A21	VSS_20	VSS_130	W65
A22	VSS_21	VSS_131	W68
A23	VSS_22	VSS_132	W71
A24	VSS_23	VSS_133	W74
A25	VSS_24	VSS_134	W77
A26	VSS_25	VSS_135	W80
A27	VSS_26	VSS_136	W83
A28	VSS_27	VSS_137	W86
A29	VSS_28	VSS_138	W89
A30	VSS_29	VSS_139	W92
A31	VSS_30	VSS_140	W95
A32	VSS_31	VSS_141	W98
A33	VSS_32	VSS_142	W101
A34	VSS_33	VSS_143	W104
A35	VSS_34	VSS_144	W107
A36	VSS_35	VSS_145	W110
A37	VSS_36	VSS_146	W113
A38	VSS_37	VSS_147	W116
A39	VSS_38	VSS_148	W119
A40	VSS_39	VSS_149	W122
A41	VSS_40	VSS_150	W125
A42	VSS_41	VSS_151	W128
A43	VSS_42	VSS_152	W131
A44	VSS_43	VSS_153	W134
A45	VSS_44	VSS_154	W137
A46	VSS_45	VSS_155	W140
A47	VSS_46	VSS_156	W143
A48	VSS_47	VSS_157	W146
A49	VSS_48	VSS_158	W149
A50	VSS_49	VSS_159	W152
A51	VSS_50	VSS_160	W155
A52	VSS_51	VSS_161	W158
A53	VSS_52	VSS_162	W161
A54	VSS_53	VSS_163	W164
A55	VSS_54	VSS_164	W167
A56	VSS_55	VSS_165	W170
A57	VSS_56	VSS_166	W173
A58	VSS_57	VSS_167	W176
A59	VSS_58	VSS_168	W179
A60	VSS_59	VSS_169	W182
A61	VSS_60	VSS_170	W185
A62	VSS_61	VSS_171	W188
A63	VSS_62	VSS_172	W191
A64	VSS_63	VSS_173	W194
A65	VSS_64	VSS_174	W197



<Variant Name>
ASUS Title : M64M POWER
 ASUSTeK COMPUTER INC. NBI Engineer: Hawk
 Size Project Name
 Custom FSV
 Date: 11/11/2007 Sheet 48 of 94

D

D

C


C

B

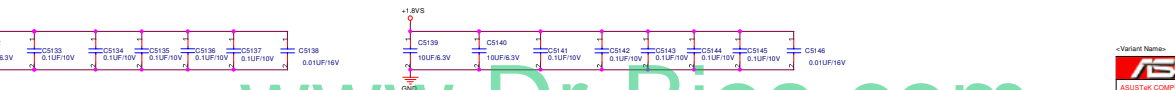
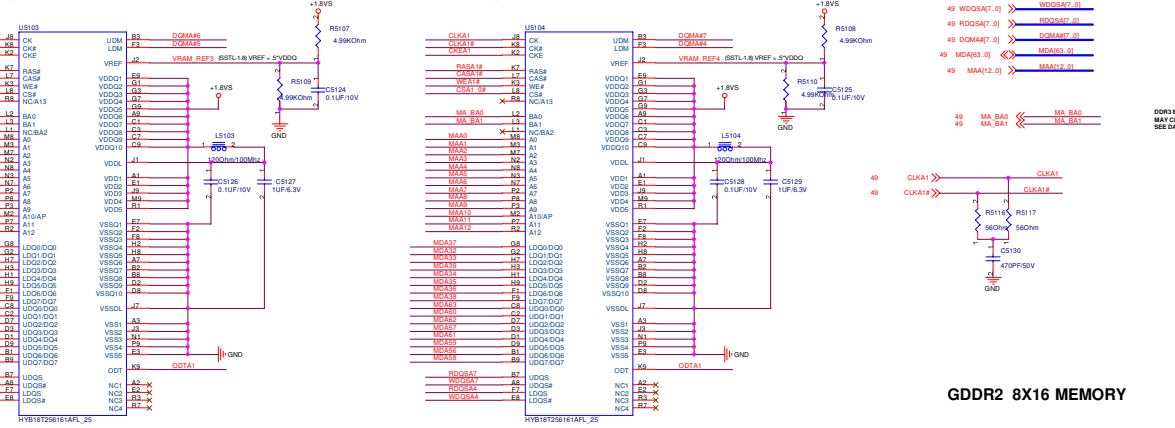
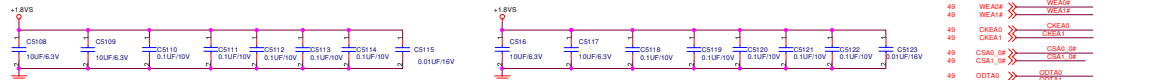
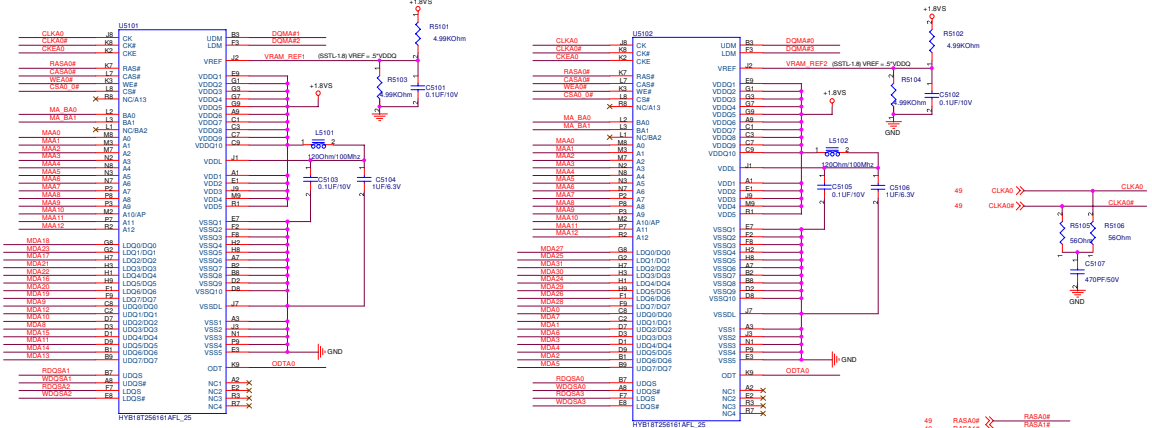
B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 50 of 94

www.Dr-Bios.com



GDDR2 8X16 MEMORY

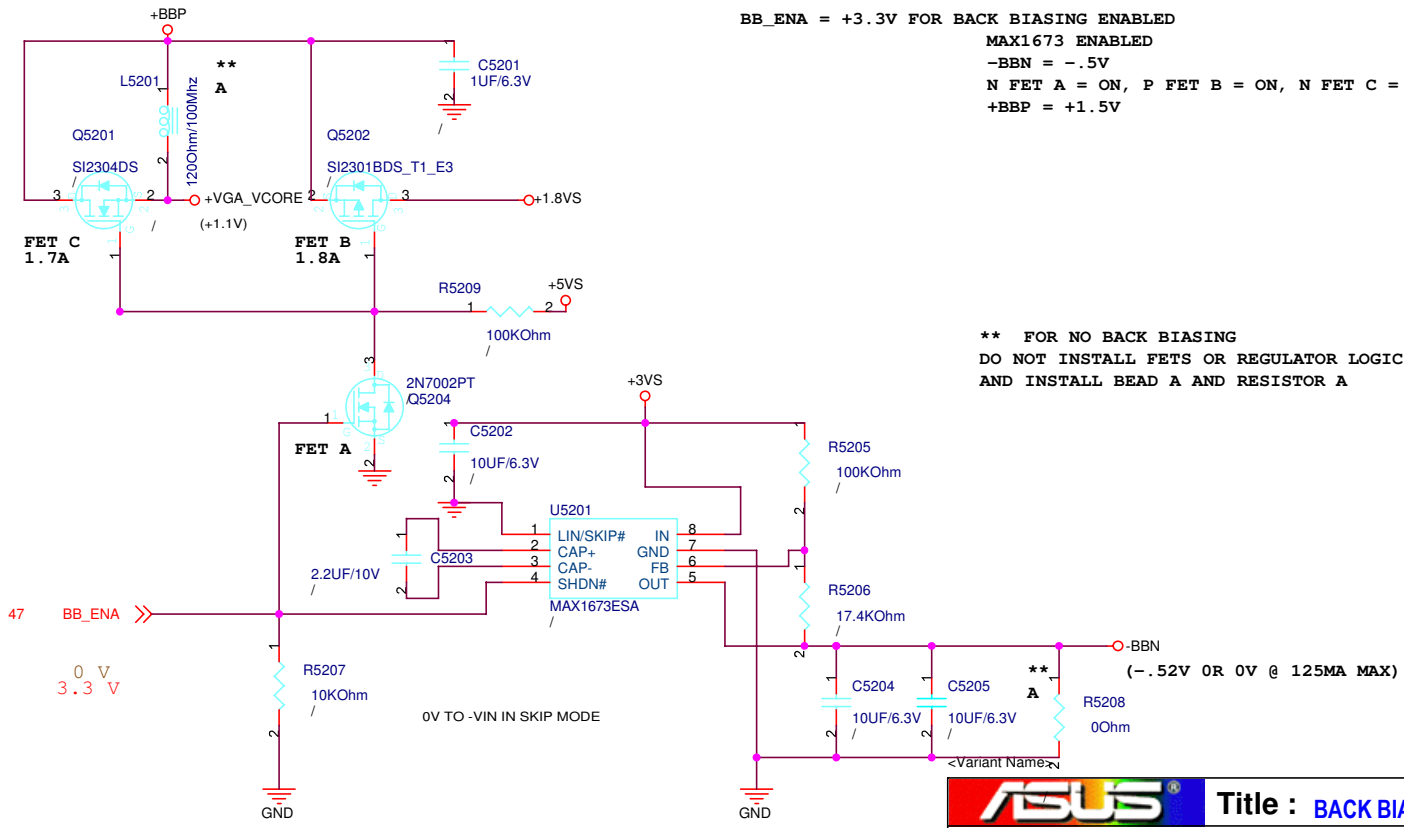
DRR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN REVISIONS AND MPSS.
SEE DATA BOOK FOR LATEST INFORMATION

RAS#0	1	1210Ω	2	RS111
RAS#1	1	1210Ω	2	RS112
CAS#0	1	1210Ω	2	RS113
CAS#1	1	1210Ω	2	RS114
WE#0	1	1210Ω	2	RS115
WE#1	1	1210Ω	2	RS116
CS#0	0	1210Ω	2	RS119
CS#1	0	1210Ω	2	RS120
CKE#0	1	1210Ω	2	RS121
CKE#1	1	1210Ω	2	RS122
CLKA0	0	60kΩ	2	RS123
CLKA1	0	60kΩ	2	RS124
CLKB0	0	60kΩ	2	RS125
CLKB1	0	60kΩ	2	RS126

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

BB_ENA = 0V FOR BACK BIASING DISABLED
 MAX1673 SHUTDOWN
 -BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
 N FET A = OFF, P FET B = OFF, N FET C = ON
 +BBP = VDD_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
 MAX1673 ENABLED
 -BBN = -.5V
 N FET A = ON, P FET B = ON, N FET C = OFF
 +BBP = +1.5V



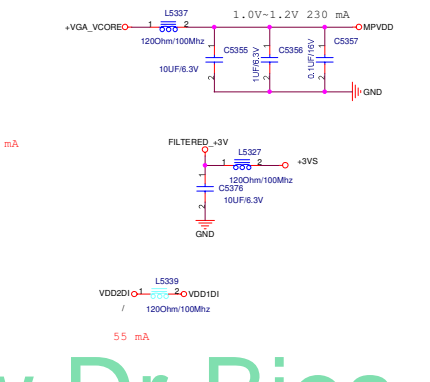
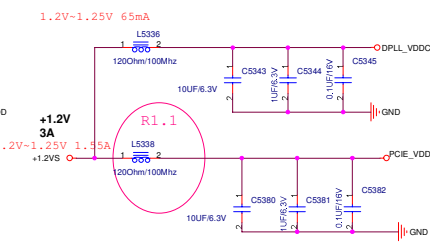
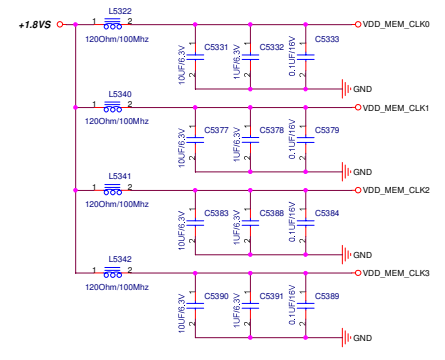
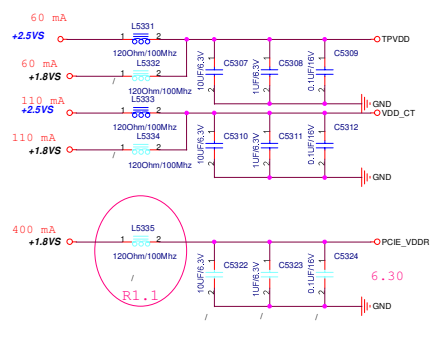
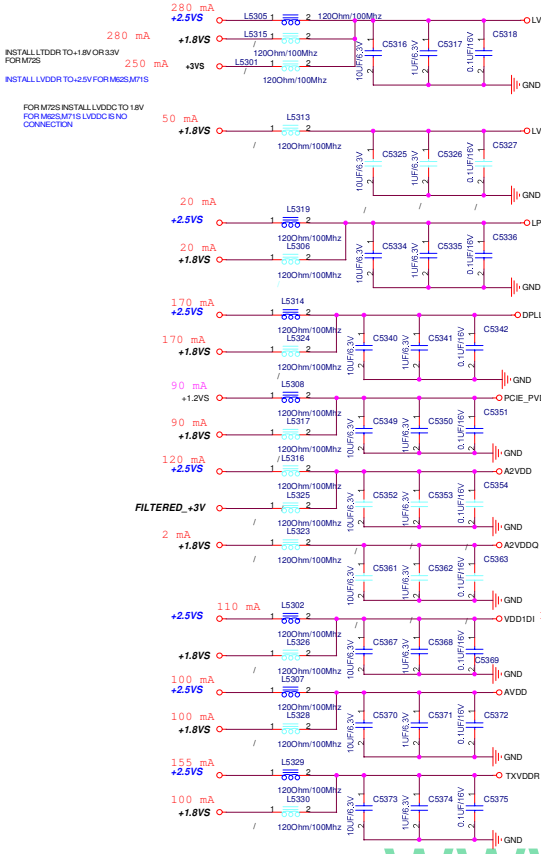
ASUS		Title : BACK BIAS	
ASUSTek COMPUTER INC. NB1		Engineer: Hawk	
Size A	Project Name F5V	Date: 星期一, 四月 23, 2007	Rev 1.0
		Sheet 52 of 94	

**COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED**

LTPVSS18 DVSSDI TPVSS MPVSS
* PCIE_PVSS PVSS A2VSSQ AVSSQ

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP


280 mA
+2.5VS
INSTALL LDDR TO +1.8V OR 3.3V
FORMS
250 mA
INSTALL LVDDR TO +2.5V FORMS
FORMS
FOR M2S INSTALL LVDDC TO 1.8V
FOR M2S M7S LVDDC IS NO
CONNECTION

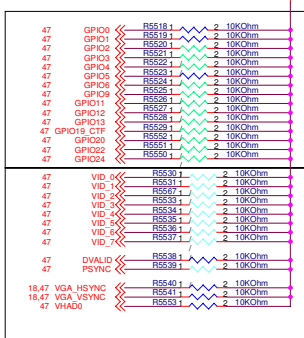
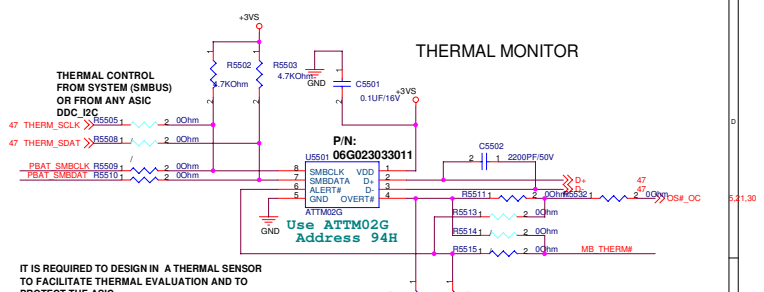
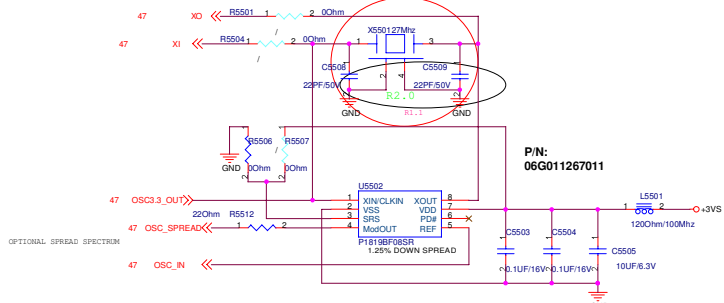


www.Dr-Bios.com

ASUS		Title : IO capacitor	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name		Rev
Custom	FSV		1.0
Date: 11/23/2007	Sheet	53	of 94

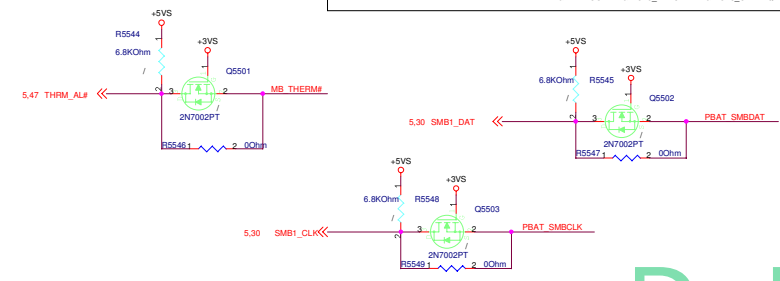
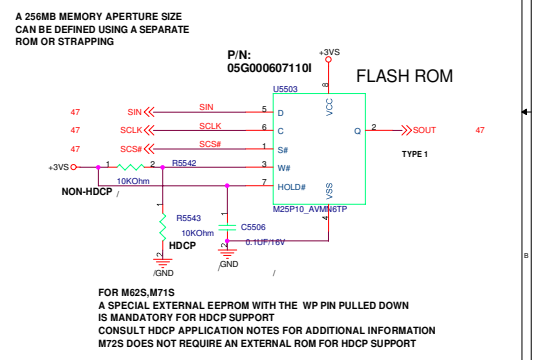
www.Dr-Bios.com

-Variant Name-		
	Title : VRAN2	
ASUSTEK COMPUTERS INC. NET	Engineer: HAWK	
Size	Project Name	Rev
C	FSV	1.0
Code: 001 - 011 38 8007	Sheet	04 of 04



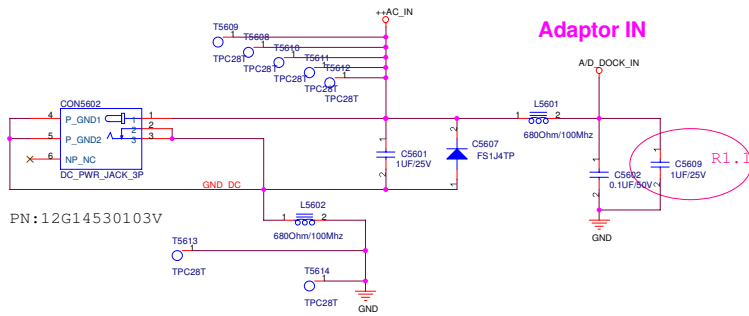
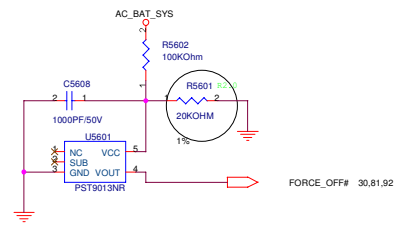
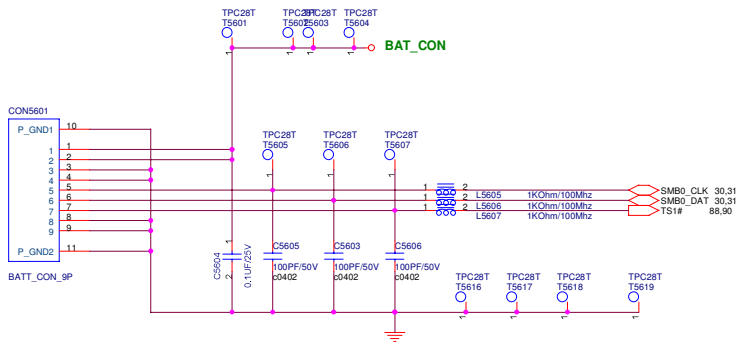
CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			0 - DO NOT INSTALL RESISTOR	1 - INSTALL 10K RESISTOR
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M62S M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
GPIO2	GPIO2	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_BIAS_RD_1.0	GPIO16.5	BIAS CURRENT FOR PCIE PHY PLL	0 1	X X
BIOS_ROM_EN	GPIO19_CT#	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3.0)	GPIO13:11.5	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0	0
BIF_VGA_DIS	PSYNC	VGA ENABLED	NA	0
MEM_TYPE	UNUSED GPIO	MEMORY TYPE, MAKE AND SIZE INFO	X X X	X X X

ATI RESERVED CONFIGURATION STRAPS										
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET										
VID0	VID2	VID3	VID4	VID5	VID7	HSYNC	GPIO8	DVALID	GPIO2	GPIO3
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET										
GENERIC0C GPIO18_HPDI3 GPIO23_CLKREQ0B										



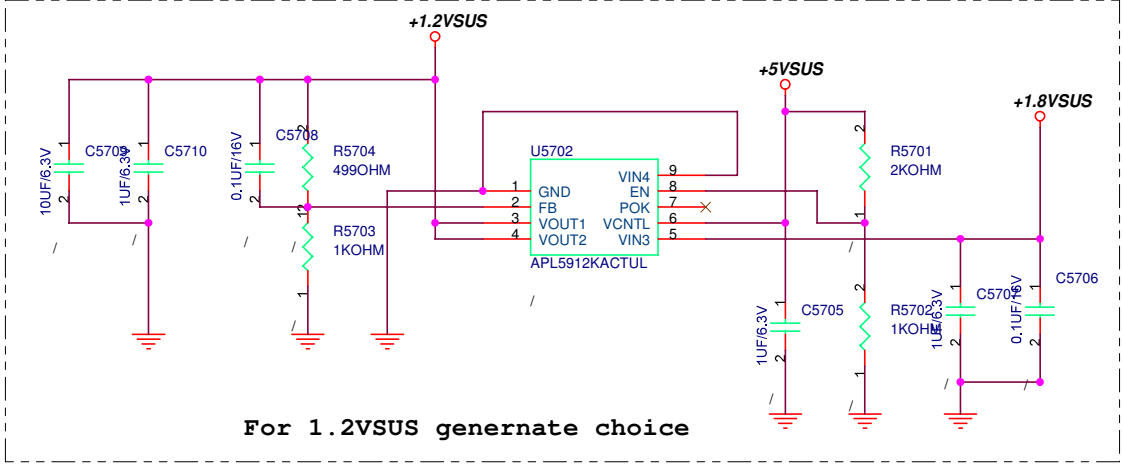
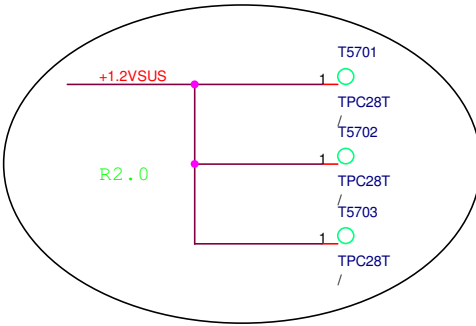
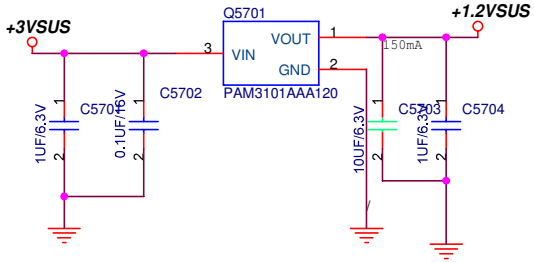
COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

ASUS		Title : SS STRAPS
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk Kazidy
Size: Custom	Project Name: FSV	Rev: 1.0
Date: 11/11/2007	Sheet: 55	of 94



ASUS		Title : AC/BAT JACK	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name		Rev
B	F5V		1.0
Date: # [0] [0] [0] 23 2007	Sheet 56 of 94		

www.Dr-Bios.com



For 1.2VSUS generate choice

ASUS		Title : +1.2VSUS
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期四 四月 23, 2007	Sheet 57 of 94	

www.Dr-Bios.com

D

D

C


C

B

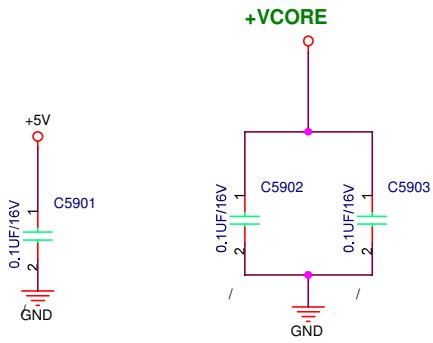
B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 58 of 94

www.Dr-Bios.com



		Title : EMI
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk
Size A	Project Name F5V	Rev 1.0
Date: 星期四 四月 23, 2007	2	Sheet 59 of 94

www.Dr-Bios.com

1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.
2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#.
3. P7 unmount R706
4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]
5. P21 change R2121 to 00hm
add R2124(330hm) for ACZ_RST# according to 968 ACT.
add R2108/R2112(00hm) for PCIEPRST#/1 according to sis ACT
ADD GMAC OSC25MHZ to GND according to sis ACT.
unmount L2103, mount L2105 according to spec.
unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
change GPIO17 from VIN4 to S_A20GATE, add R2127(00hm) for reserve SUSCLK
6. P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage
7. P22 change R2217 to 12KOhm, add C2237(22pF) for SATA REXT according to 968 ACT.
8. P24 add R2434 for A20GATE to H_A20M#, add R2457 for A20GATE to S_A20GATE, add R2456 to PU S_A20GATE
9. P29 add R2909/R2910(00hm), unmount L2901 for EMI.
10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .
delete D3004 for DDR power are not SUS power,
add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,
Add R3019 for INSTANTON#
11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost
12. P37 mount R3716/Q3715 for +VCCP discharge
13. P42 change IDSEL to PCI_AD24
14. P46 add D4602 for VGA_RST#
15. P48 unmount L4803/R4809, delete L4801
unmount R4806, mount Q4801/R4807/Q4802/R4808
16. P53 change L5335/L5338 to match the current.
17. P55 change X5501 to +-10ppm to follow spec, add C5508/C5509 to match X5501
18. P56 add C5609 for over current damaging charge IC.
19. P4 Change C440 from 0.1UF to 0.22UF
20. P10 change L1001 to 2A to match the current, Add +1.2VS delay circuit.
21. P21 Add VGA_RST# to GPIO7, add R2140 for VGA_RST#.
22. P47 Unmount R4759, mount R4758 for Vram changed from 03G151236011 to 03G151236012.

F5VL

1. P2/3 change CPU socket to P
2. P32 delete R3205/R3212
3. P59 add C5902/C5903 for EMI

- R2.0
1. P29 mount R2907, connect PCIE_PRSNT1 to CFFP#
 2. P21 unmount R2108, mount R2118, change R2118 from 00hm to 4.7KOhm but unmount R2118
 2. P27 change R2708 to 00hm and mount it to not support C3 mode
 3. P33422 add two TPS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply
 4. P21 add R2141 to connect OS#_OC to PM_THERMTRIP#, change R2141 to Q2101
 5. P30 change C3009/C3003 to 6.8pF
 6. P27 change C2706/C2707 to 24pF
 7. P55 change C5508/C5509 to 22pF
 8. P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301
 9. P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3
 10. P30 change Q3003 PU from +5V to +5VS
 11. P5 unmount R506
 12. P56 change R5601 to 20KOhm
 13. P20 unmount R2054, add and mount C2010
 - P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206
 14. P27 change 4in1 cardreader
 15. P47 mount R4704/R4705/R4706/R4707
P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839, change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813
 16. P21 Unmount L2105, mount L2103
 17. P21 change R2116 from 330hm to 200hm, change R2117 from 330hm to 00hm, change R2119 from 330hm to 200hm
P24 change R2418 from 330hm to 00hm, change R2420 from 330hm to 00hm, change R2419 from 330hm to 00hm, change R2422 from 330hm to 00hm, change R2423 from 330hm to 00hm, change R2425 from 330hm to 00hm
P25 change R2514 from 330hm to 470hm

www.Dr-Bios.com

		Title : BLANK	
ASUSTek COMPUTER INC. (NEI)		Engineer: KaxidyHawk	
Ver	Project Name	Rev	
1.0	F5VL	1.0	
Date: 2011-08-25 2:07	Sheet: 60	of	64

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 61 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 62 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 63 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 64 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 65 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 66 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 67 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 68 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 69 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 70 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 71 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 72 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 73 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 74 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 75 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 76 of 94

www.Dr-Bios.com

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期四 四月 23, 2007		Sheet 77 of 94

www.Dr-Bios.com

D

D

C


C

B

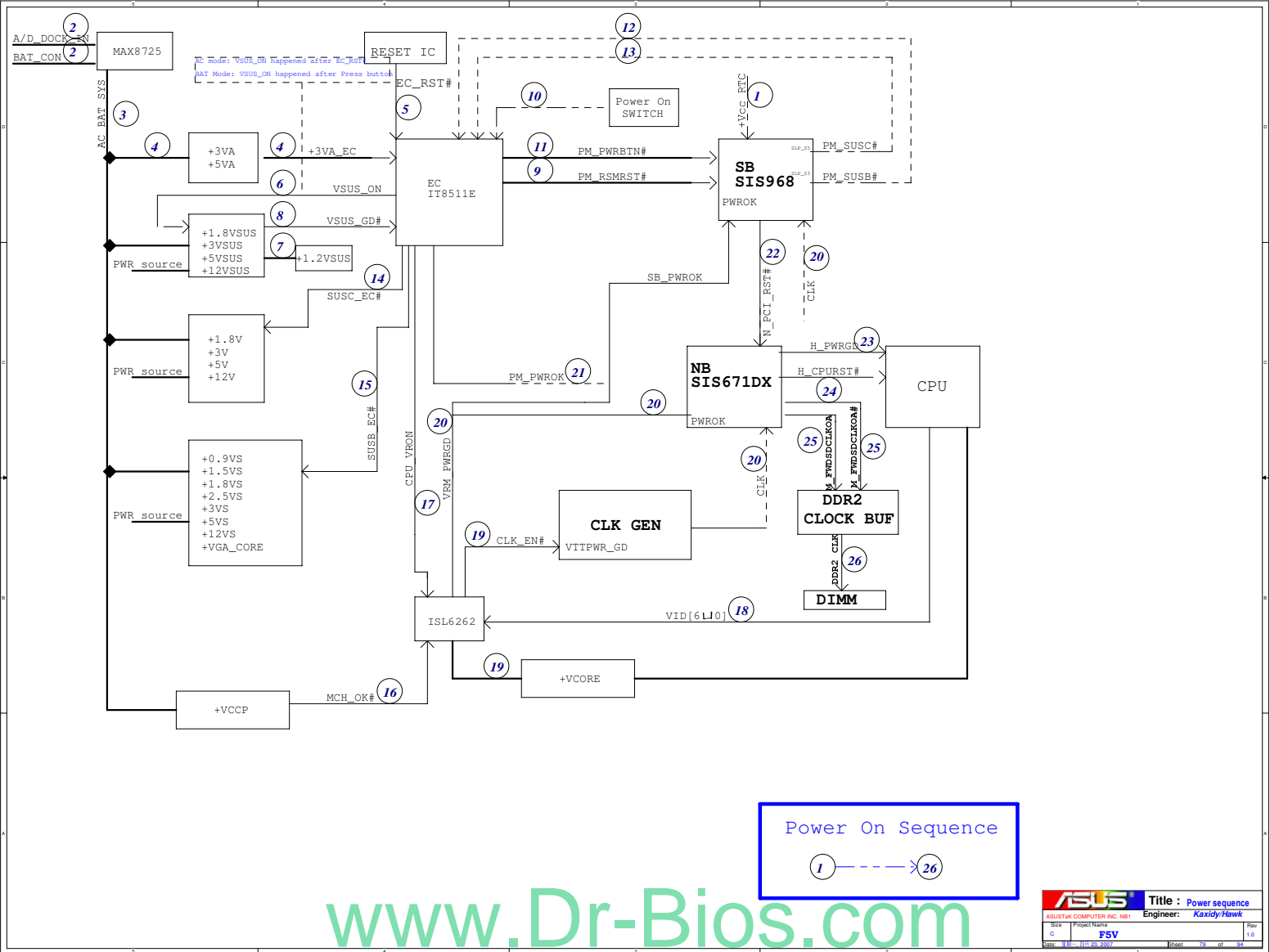
B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk
Size	Project Name	Rev
A	F5V	1.0
Date: 星期二, 四月 23, 2007		Sheet 78 of 94

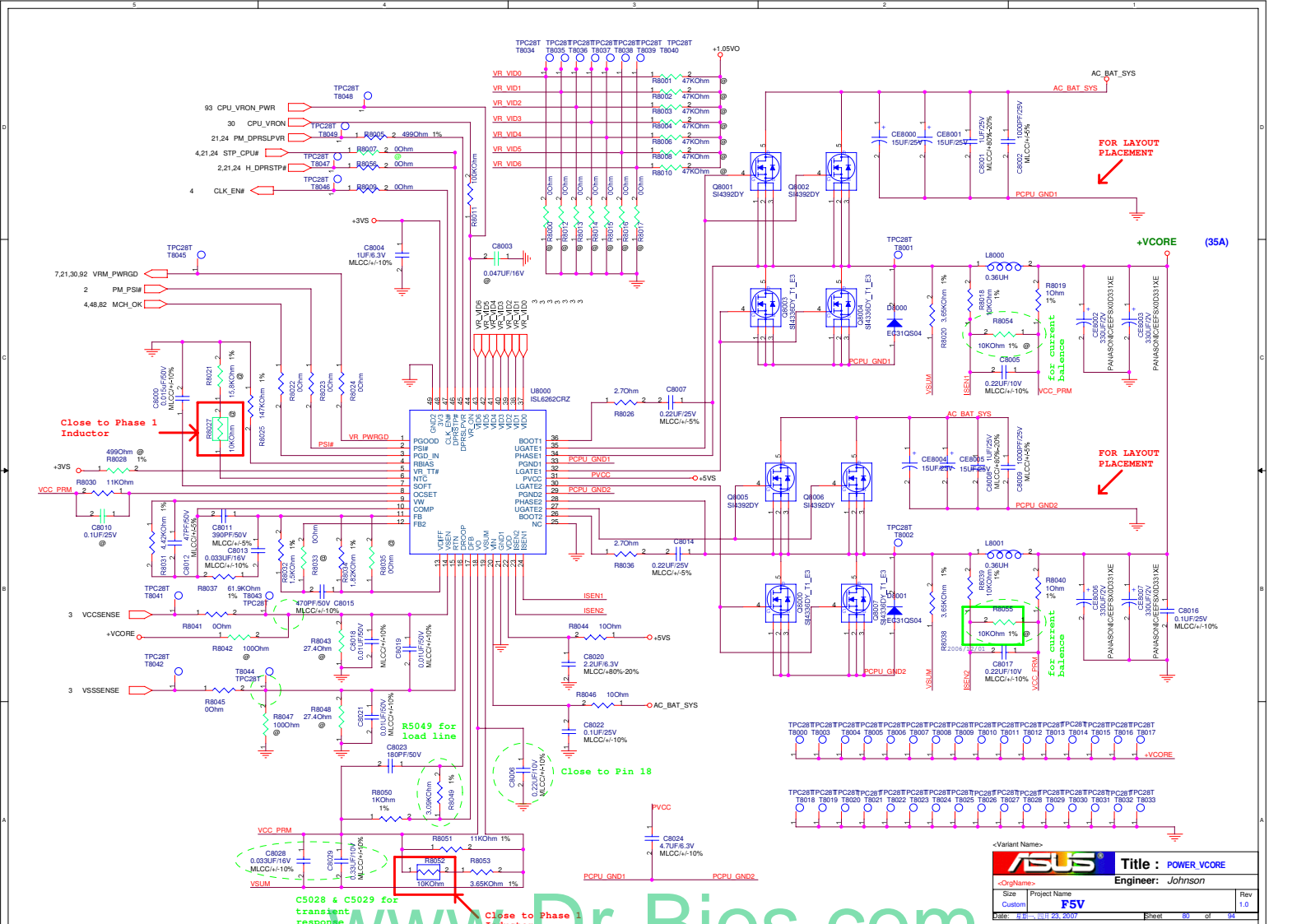
www.Dr-Bios.com



Power On Sequence
 1 -----> 26

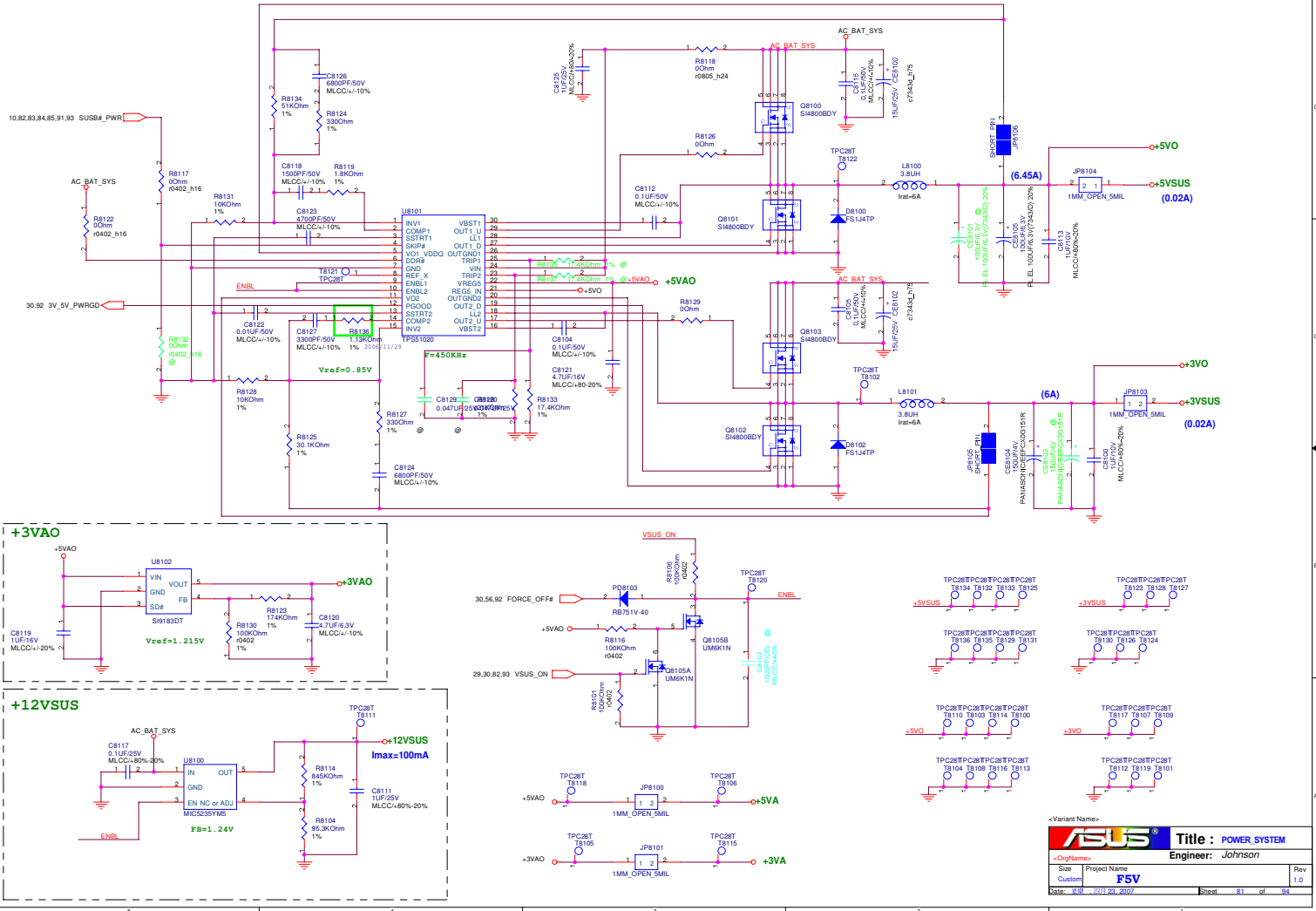
www.Dr-Bios.com

ASUS		Title : Power sequence	
ASUSTeK COMPUTER INC. (BEL)		Engineer: Kaxidy/Hawk	
Size	Project Name	Rev	
C	FSV	1.0	
Date: 2011-01-25 20:07	Sheet: 29	of	34

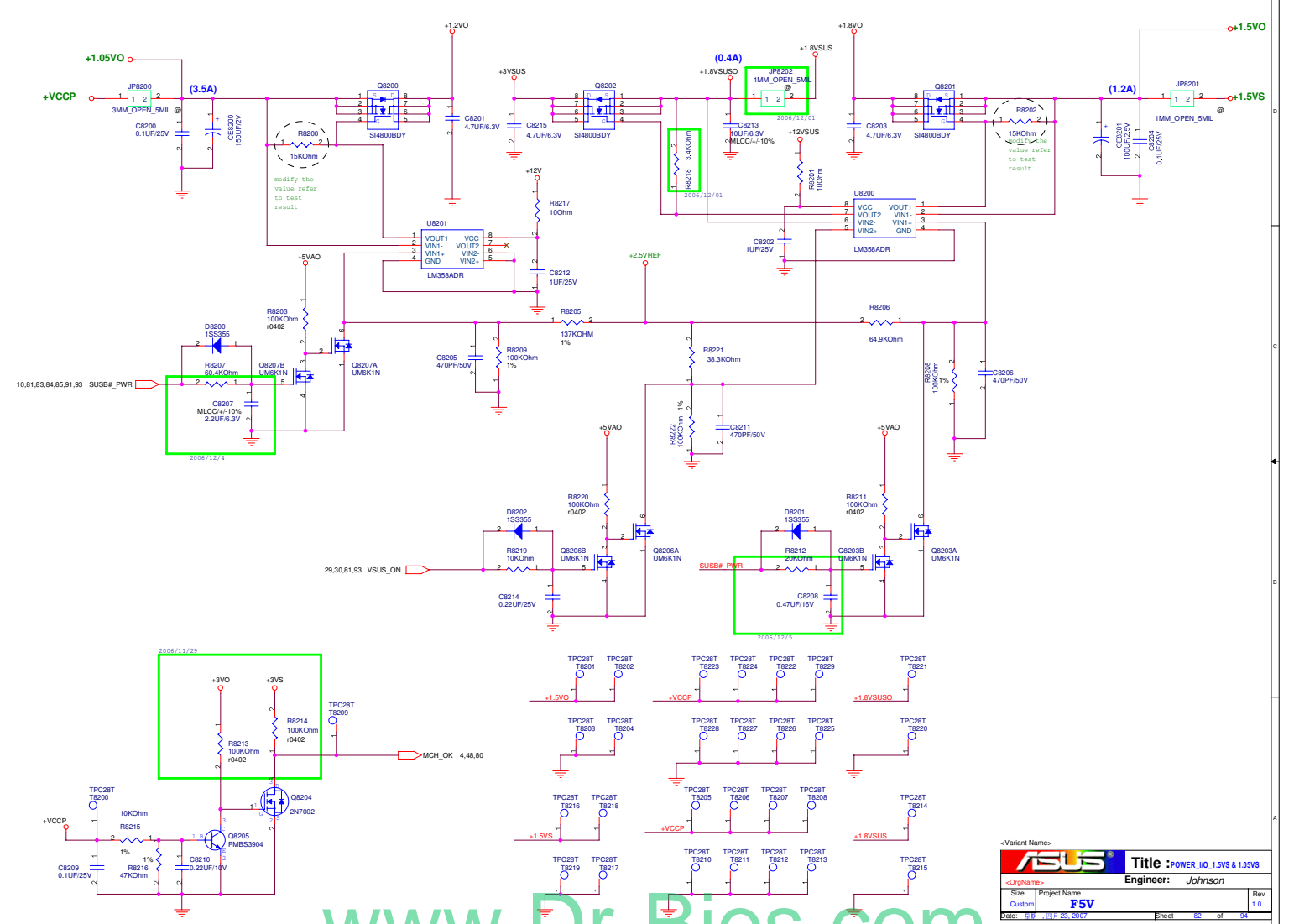


ASUS		Title : POWER_VCORE	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 11/11/2007	Sheet: 80	of 94	

www.Dr-Bios.com



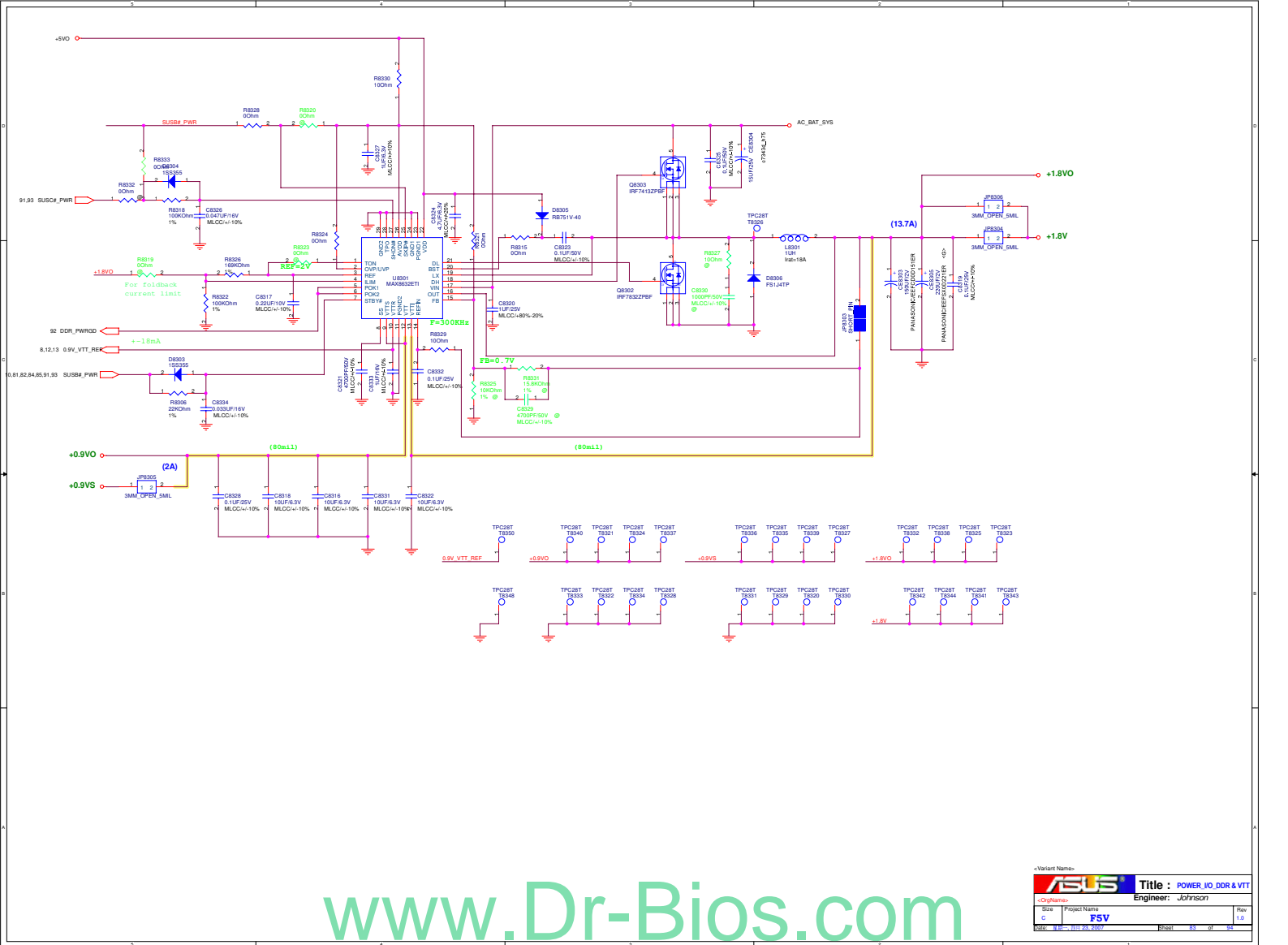
www.Dr-Bios.com



www.Dr-Bios.com

<Variant Name>

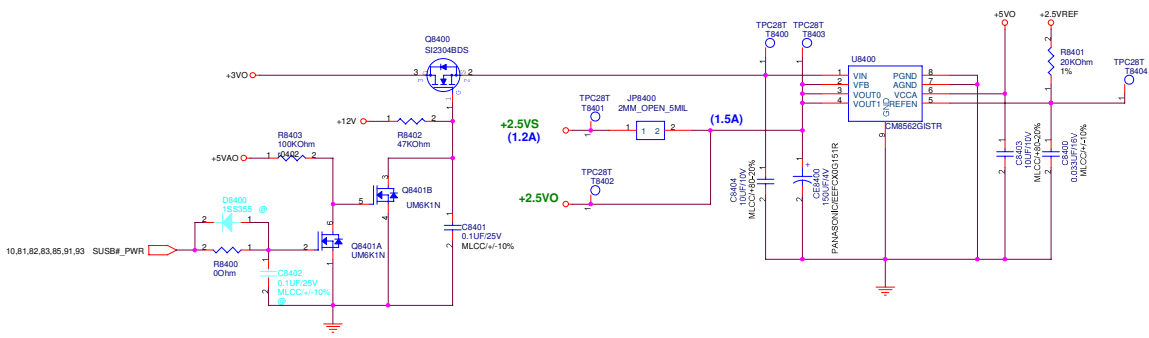
ASUS		Title : POWER_IO_1.5VS & 1.05VS
Size		Engineer: Johnson
Custom	Project Name	Rev 1.0
Date: 11/23/2007	FSV	Sheet 02 of 04



www.Dr-Bios.com

-Variant Name-		ASUS		Title : POWER_IO_DDR & VTT	
-Originals-		Engineer: Johnson			
Sr	Project Name	Rev			
C	FSV	1.0			
DATE: 08/11/2007	ESK: 81	of 84			

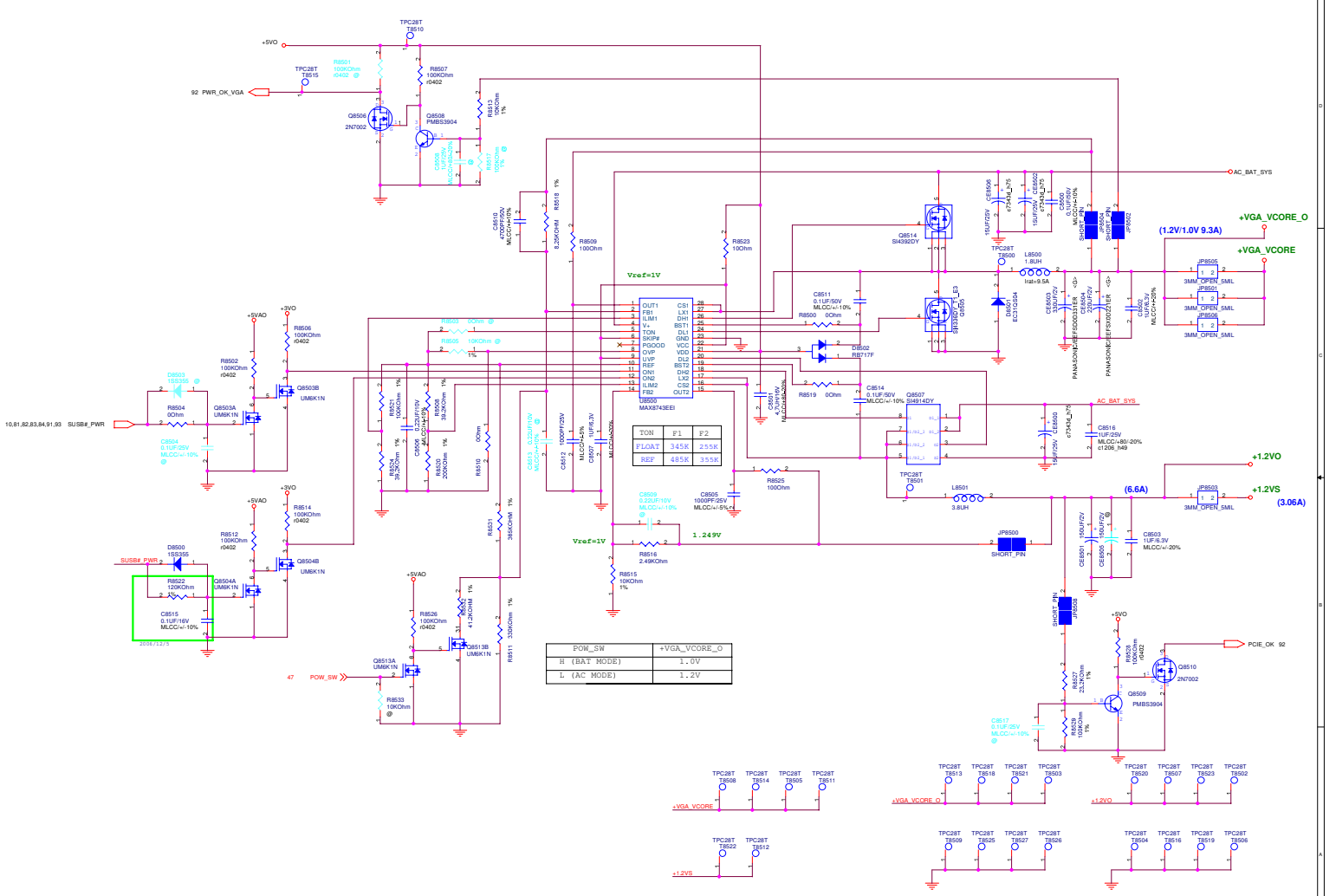
+2.5VS



<Variant Name>

		Title : POWER_IO_+3VA & +2.5V
Engineer: Johnson		
Size	Project Name	Rev
Custom	F5V	1.0
Date: 11/11/2007	Sheet	84 of 94

www.Dr-Bios.com




www.Dr-Bios.com

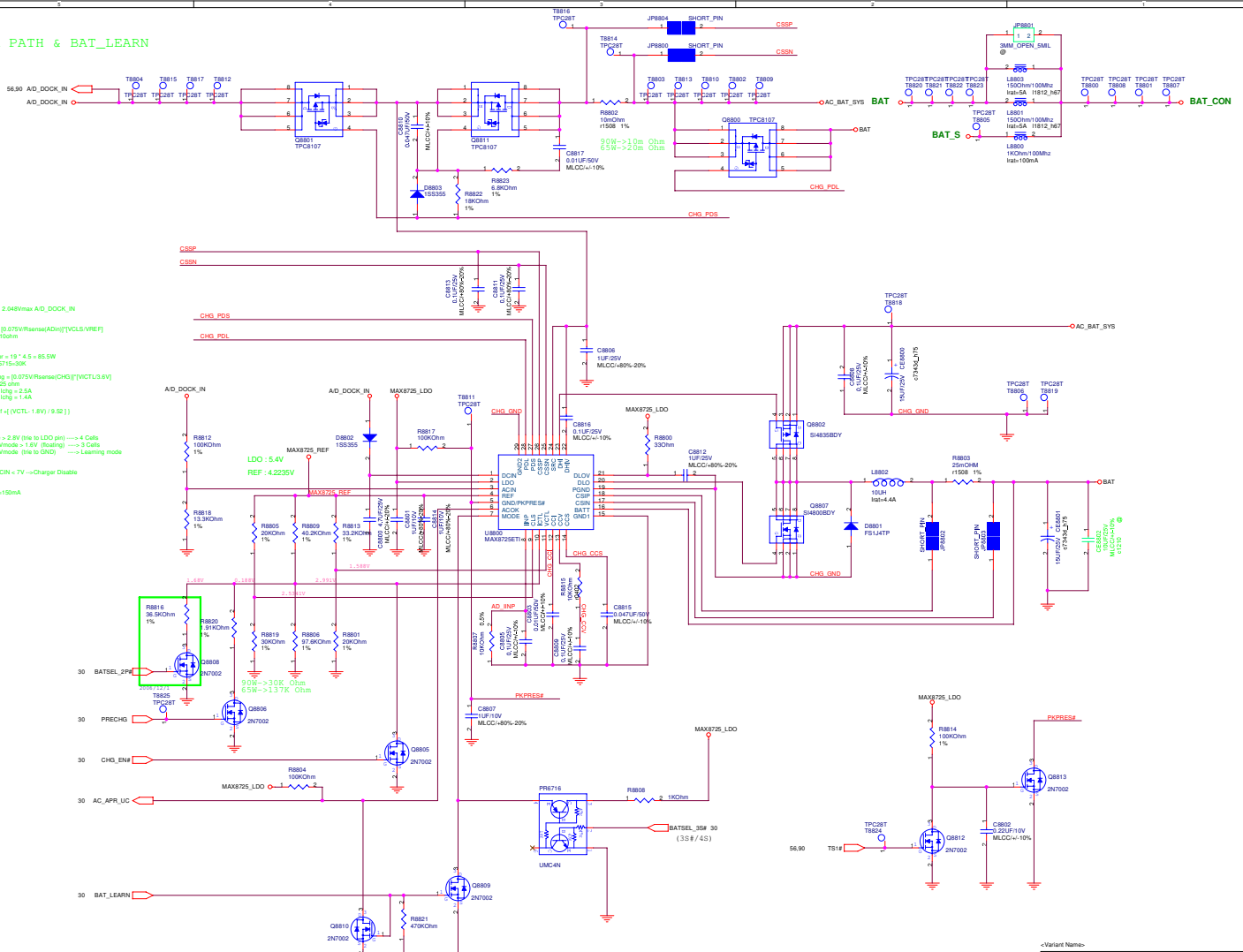
<Variant Name>		Title : NA	
<OrgName>		Engineer: <i>Johnson</i>	
Size	Project Name	Rev	
B	F5V	1.0	
Date: # 01	01/18/23, 2007	Sheet	86 of 94

www.Dr-Bios.com

www.Dr-Bios.com

<Variant Name>		
		Title : <i>N/A</i>
<OrigName>		Engineer: <i>Johnson</i>
Size	Project Name	Rev
Custom	F5V	1.0
Date: 11/11/2007		Sheet 87 of 94

POWER PATH & BAT_LEARN




VC_N Threshold > 0.049Vmax AD_DOCK_IN
 > 17.44V active
 Adapter (In/ma) = [0.075V/Rsense/Adm]/[VCL5/VREF]
 Rsense=Adm/0.075
 VCL5=2.534V
 => 100mA/0.45A
 => Constant Power = 13.145 + 85.5W
 => RST to 200/257/1530K
 Charge Current Ichg = [0.075V/Rsense/CHG]/[VCTL3.6V]
 Rsense=CHG/0.075
 VCTL=3V => Ichg = 2.5A
 VCTL=1.588V => Ichg = 1.4A
 Mode pin: Vinode > 2.8V (pin to LDO pin) => 4 Cells
 2.0 > Vinode > 1.8V (Booting) => 3 Cells
 0.8 > Vinode (pin to DND) => Learning mode
 VICT=0.8V or DCIN = 7V => Charger Disable
 Precharge current=150mA

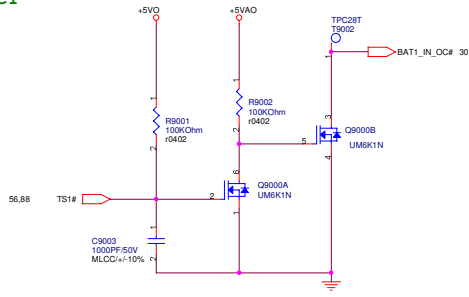
www.Dr-Bios.com

ASUS		Title :POWER CHARGER
-		Engineer: Johnson
Size	Project Name	Rev
C	F5V	1.0
Date: 08/11/2007	EScan	88 of 84

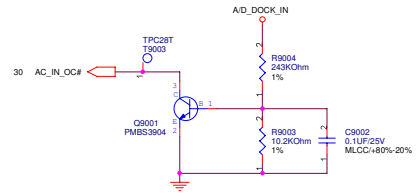
www.Dr-Bios.com

<Variant Name>		
		Title : <i>N/A</i>
<OrigName>		Engineer: <i>Johnson</i>
Size	Project Name	Rev
Custom	FSV	1.0
Date: 11/11/2007		Sheet 89 of 94

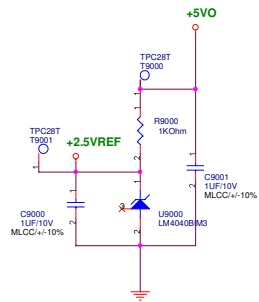
BATTERY IN DETECT



ADAPTER IN DETECT



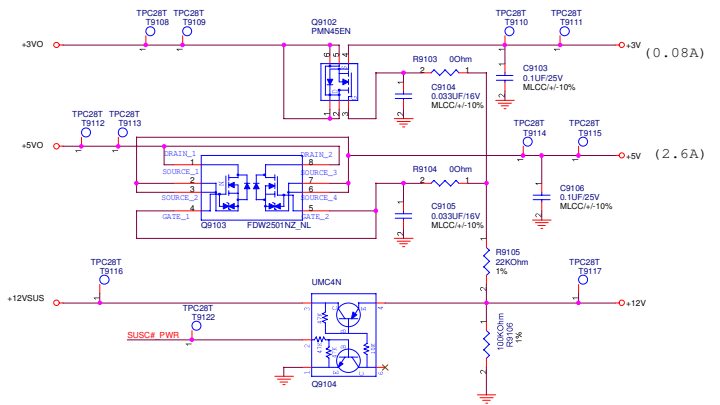
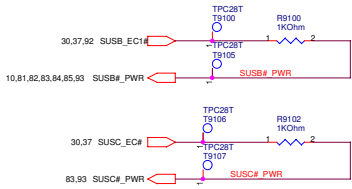
+2.5VREF



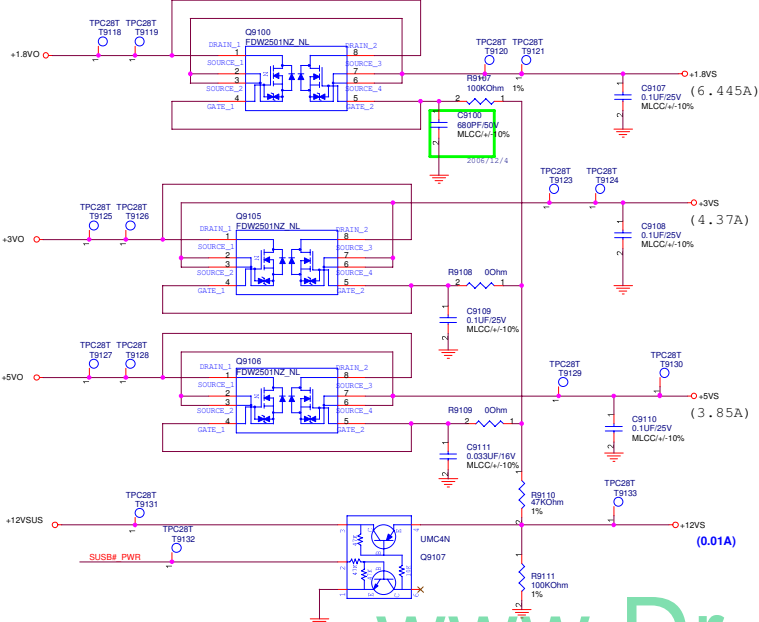
<Variant Name>

		Title : POWER_DETECT
		Engineer: Johnson
Size	Project Name	Rev
Custom	FSV	1.0
Date: 2007-11-23 2007		Sheet 90 of 94

SUSC#_STAGE POWER



SUSB#_PWR POWER

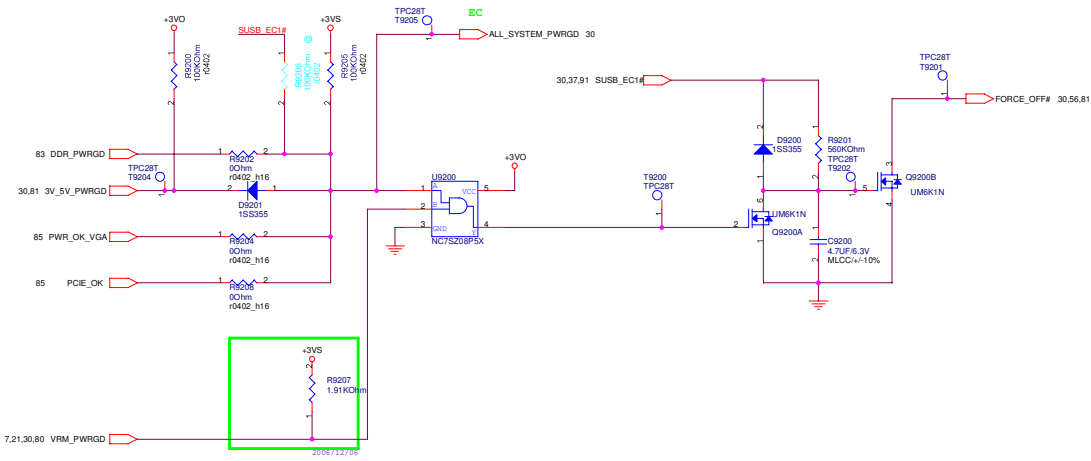


<Variant Name>

ASUS		Title :POWER_LOAD_SWITCH	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 11/11/2007	Sheet: 81	of 94	

www.Dr-Bios.com

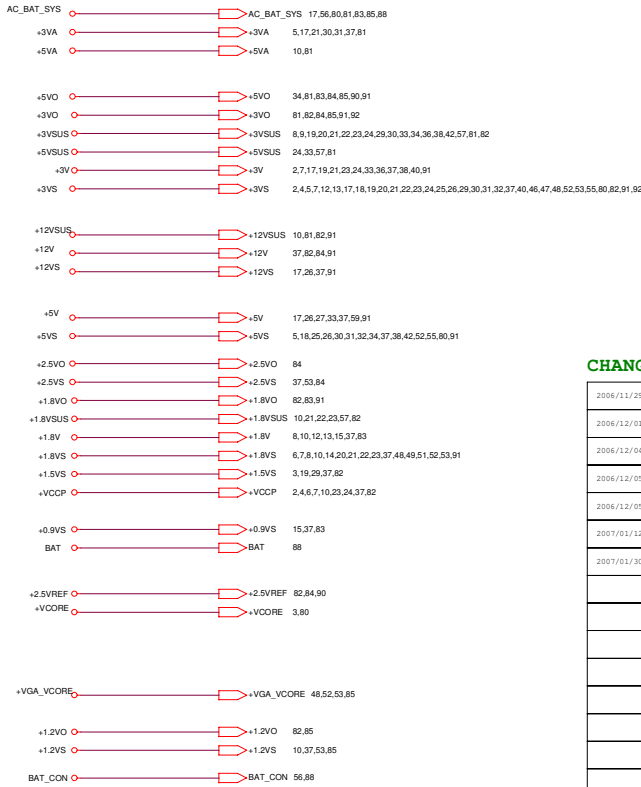
POWER GOOD DETECTOR



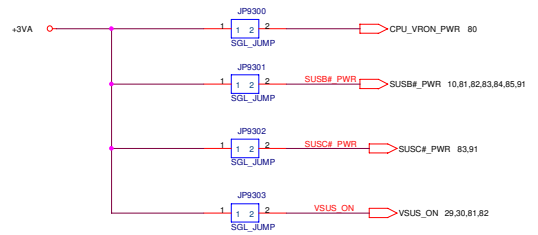
<Variant Name>

		Title :POWER_PROTECT	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 11/11/2007	Sheet	62	of 94

www.Dr-Bios.com



FOR POWER TEST



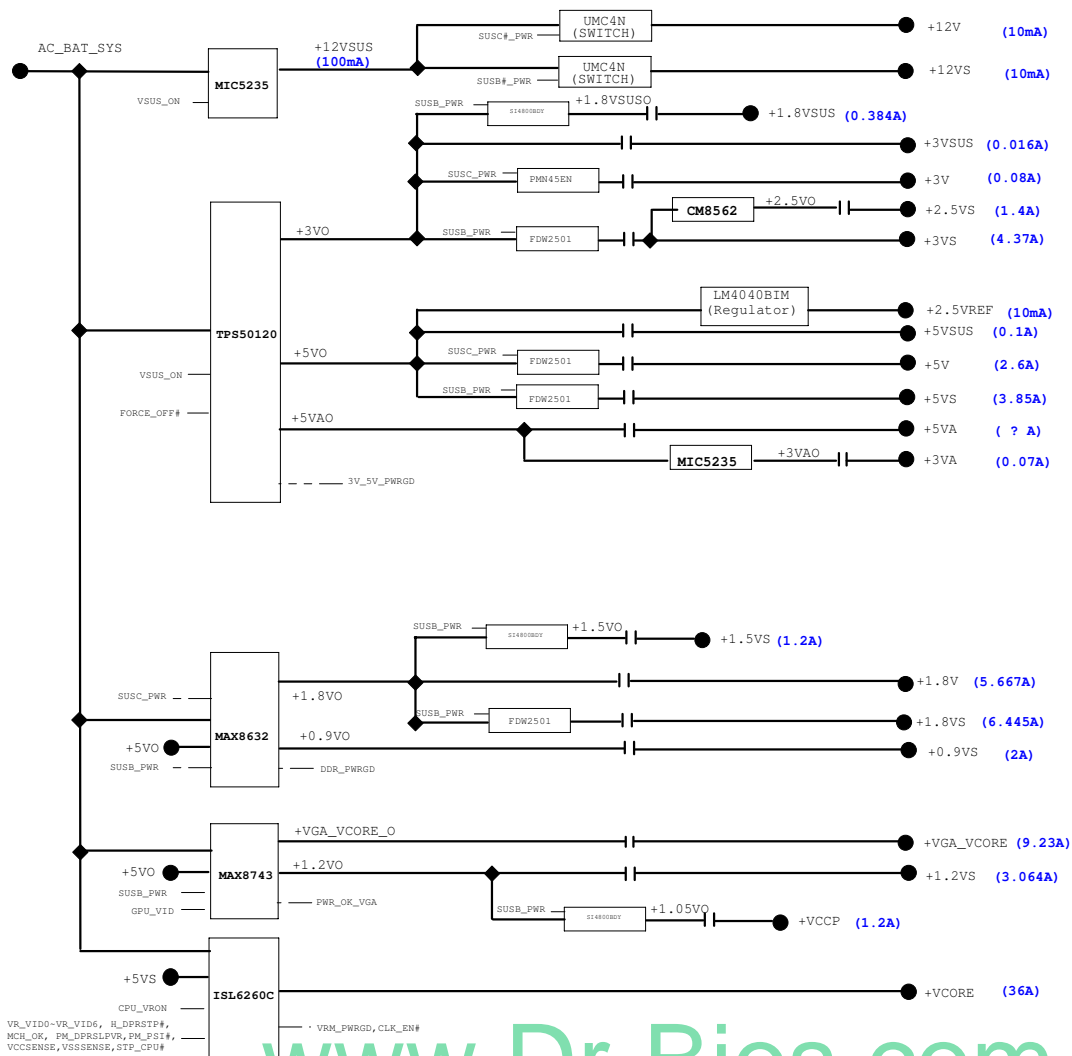
CHANGE LIST

2006/11/29	1. Pull high R8213 to +3V0 . 2. change C8334 to 0.1uF, 3.change R8136 to 1.13KOhm
2006/12/01	1. change R8218 to 3.4KOhm, 2. add JP8202, 3. delete R8855, 4.add Q8808 & R8816
2006/12/04	1. change C8207 to 2.2uF & R8207 to 60.4KOhm , 2. delete R8855, 3.change C8910 to 680pF
2006/12/05	1. change C8208 to 0.47uF & R8212 to 20KOhm, 2. change C8515 to 0.1uF & R8522 to 120KOhm.
2006/12/05	1.change R9207 to 1.91KOhm
2007/01/12	1. change input cap footprint, 2. add necessary TP.
2007/01/30	1. C8207 to 2.2uF/6.3V

<-Variant Name>

Title : POWER SIGNAL
Engineer: Johnson

Size	Project Name	Rev
Custom	FSV	1.0
Date: 11/29/2007	Sheet 93	of 94



www.Dr-Bios.com

ASUS		Title :POWER_FLOWCHART	
Engineer: Johnson			
Rev	Project Name	Rev	
1.0	FSV	1.0	
Date: 11/10/2007	Sheet	14	of 14