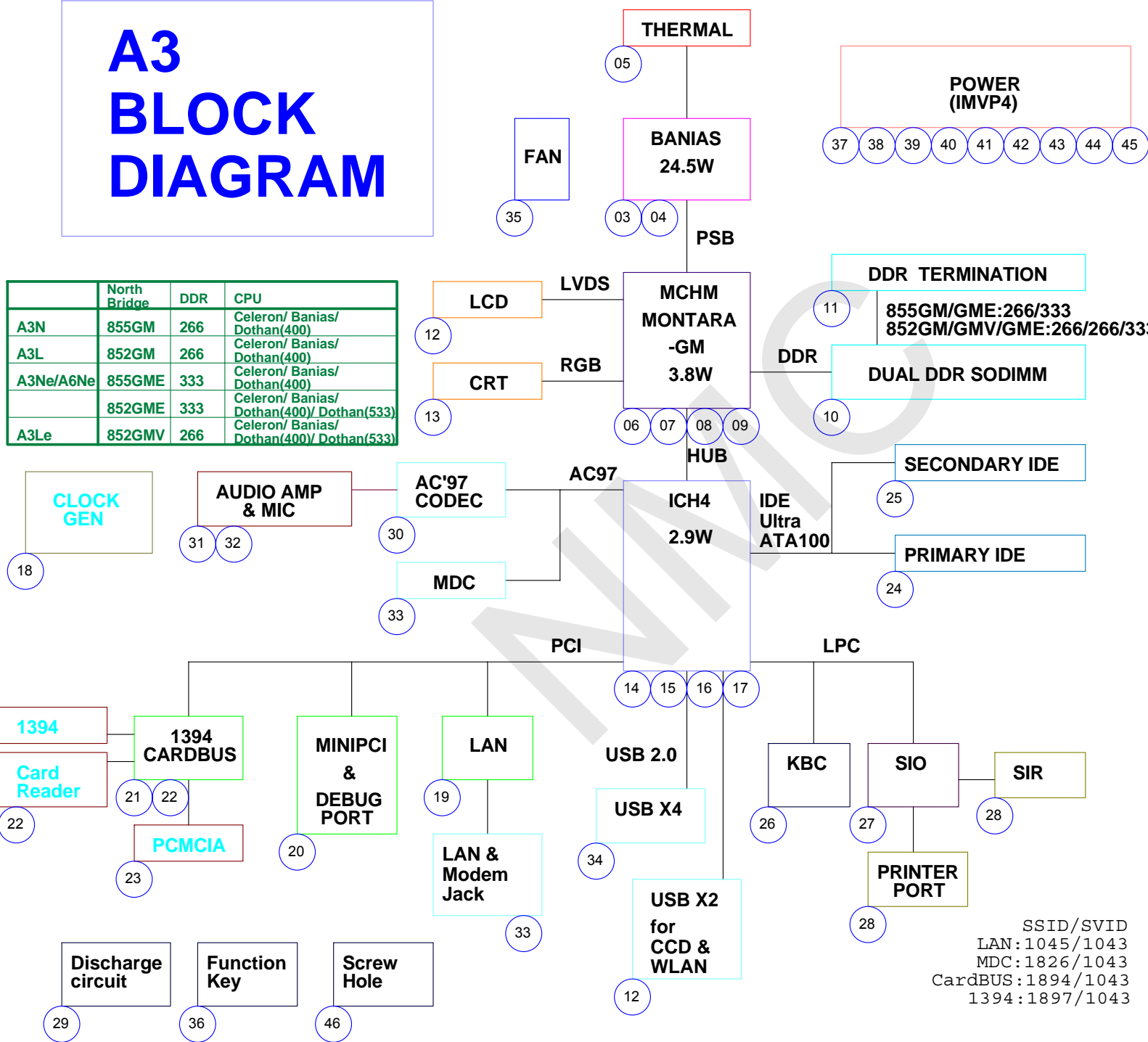


A3 BLOCK DIAGRAM



	North Bridge	DDR	CPU
A3N	855GM	266	Celeron/ Banias/ Dothan(400)
A3L	852GM	266	Celeron/ Banias/ Dothan(400)
A3Ne/A6Ne	855GME	333	Celeron/ Banias/ Dothan(400)
	852GME	333	Celeron/ Banias/ Dothan(400)/ Dothan(533)
A3Le	852GMV	266	Celeron/ Banias/ Dothan(400)/ Dothan(533)

FILE LIST

01

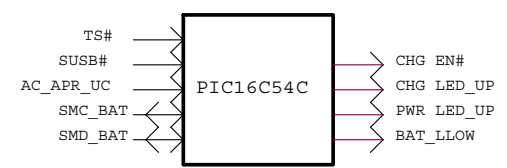
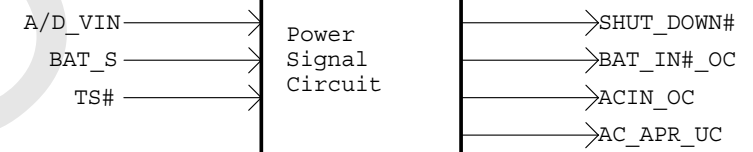
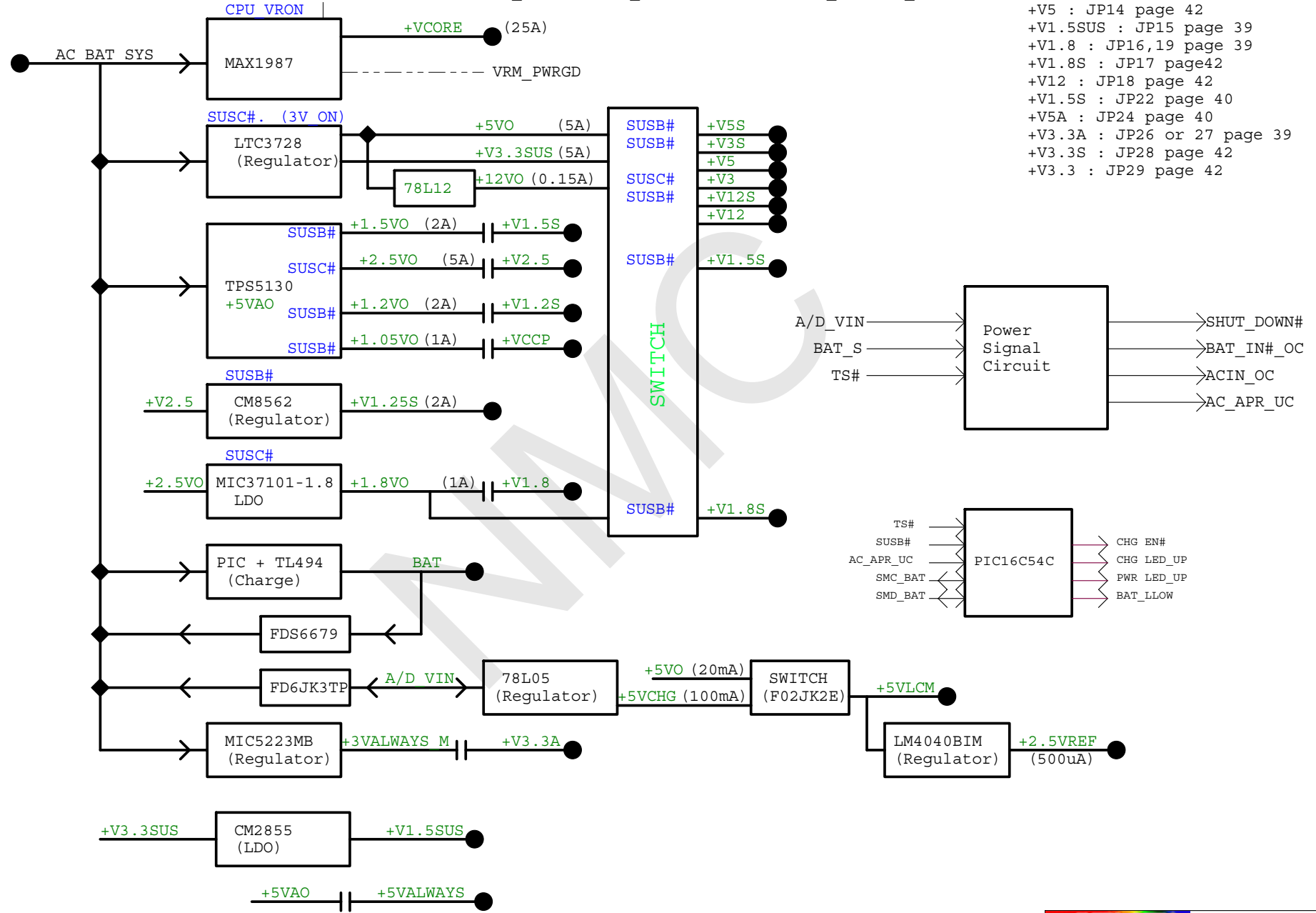
- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-BANIAS(HOST)
- 04_CPU-BANIAS(PWR)
- 05_THERMAL
- 06_NB-MCHM(DDR)
- 07_NB-MCHM(HOST)
- 08_NB-MCHM(VGA)
- 09_NB-MCHM(PWR)
- 10_DUAL DDR SODIMM
- 11_DDR TERMINATION
- 12_LVDS & BACKLIGHT
- 13_CRT CONNECTOR
- 14_ICH4-M(HUB_PCI)
- 15_ICH4-M(H_U_IDE_PM)
- 16_ICH4-M(PWR)
- 17_ICH4-M_PULLUP
- 18_CLOCK-ICS950815
- 19_LAN-RTL8100CL
- 20_MINIPCI
- 21_CB1394-R5C593(1)
- 22_CB1394-R5C593(2)
- 23_PCMCIA SOCKET
- 24_IDE-HD
- 25_IDE-ODD
- 26_KBC-M38857
- 27_SIO-ITE7805
- 28_IR&LPT_PORT
- 29_DISCHARGE CIRCUIT
- 30_CODEC-ALC650
- 31_AUDIO AMP
- 32_MIC
- 33_MDC&RJ45&RJ11
- 34_USB
- 35_FAN&Audio DJ
- 36_FUNCTION KEY
- 37_PWR & RESET SEQ
- 38_VCORE
- 39_1.25V&1.8V
- 40_2.5V&1.5V&1.35V&1.05V
- 41_SYSTEM
- 42_LOAD SWITCH
- 43_CHARGER
- 44_PIC16C54
- 45_BATLOW/SD#
- 46_SCREW HOLE & M/B SETTING
- 47_REVISION(1)
- 48_REVISION(2)
- 49_REVISION(3)
- 50_REVISION(4)
- 51_BLOCK DIAGRAM 5E
- 52_BLOCK DIAGRAM 7H
- 53_Part Reference 1
- 54_Part Reference 2
- 55_Power Net Reference

SSID/SVID
LAN: 1045/1043
MDC: 1826/1043
CardBUS: 1894/1043
1394: 1897/1043

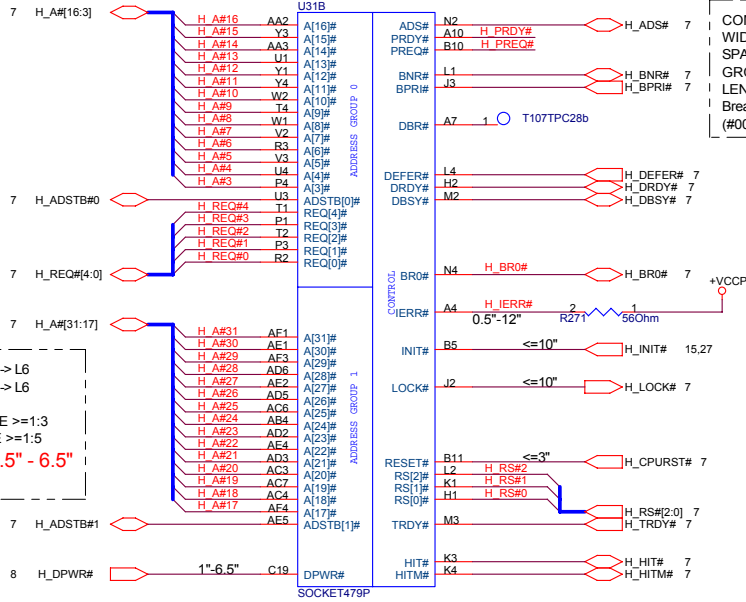
System work voltage
 Adapter in : 19.5 ~ 18.5 V
 Battery in : 16.8 ~ 11.6V

- +V1.25S : JP4,5 page 39
- +V2.5 : JP6 page 40
- +V1.2S : JP7 page 40
- +VCCP : JP9 page 40
- +V5S : JP13 page 42
- +V5 : JP14 page 42
- +V1.5SUS : JP15 page 39
- +V1.8 : JP16,19 page 39
- +V1.8S : JP17 page 42
- +V12 : JP18 page 42
- +V1.5S : JP22 page 40
- +V5A : JP24 page 40
- +V3.3A : JP26 or 27 page 39
- +V3.3S : JP28 page 42
- +V3.3 : JP29 page 42

----- VR_VID0-VR_VID5
 ----- PM_STPCPU#, PM DPRSLPVR., PCI#, MCH_OK., CLK_EN#



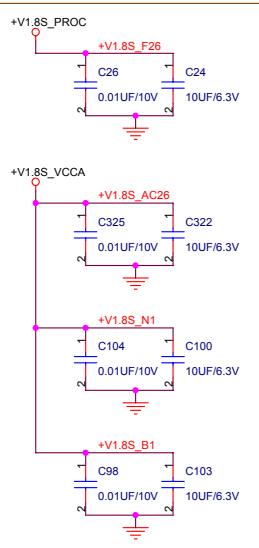
CPU Pin A1 need to be enlarged(M)



ADDR GROUP 0 -> L6
 ADDR GROUP 1 -> L6
 STROBE SPACE >=1.3
 GROUP SPACE >=1.5
 LENGTH: 0.5" - 6.5" (#0012)

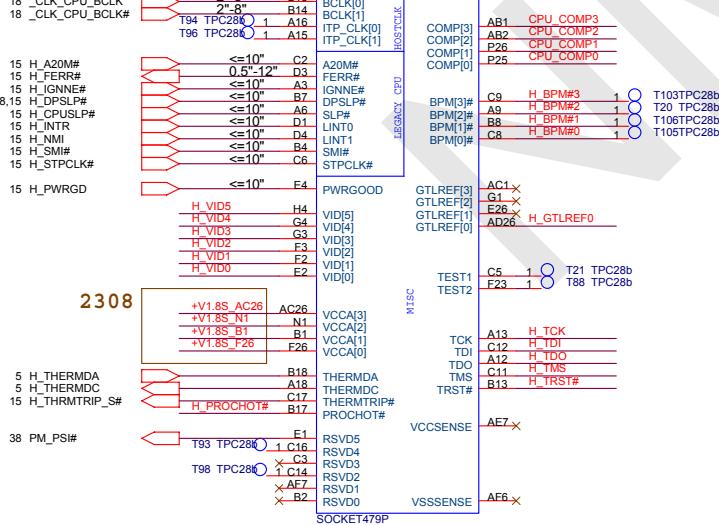
T92 TPC288 1 CLK_CPU_BCLK
 T95 TPC288 1 CLK_CPU_BCLK#

CPU PLL CIRCUITS
 1.71V - 1.89V(+/- 5%)
 SO-S1M: 0.3A

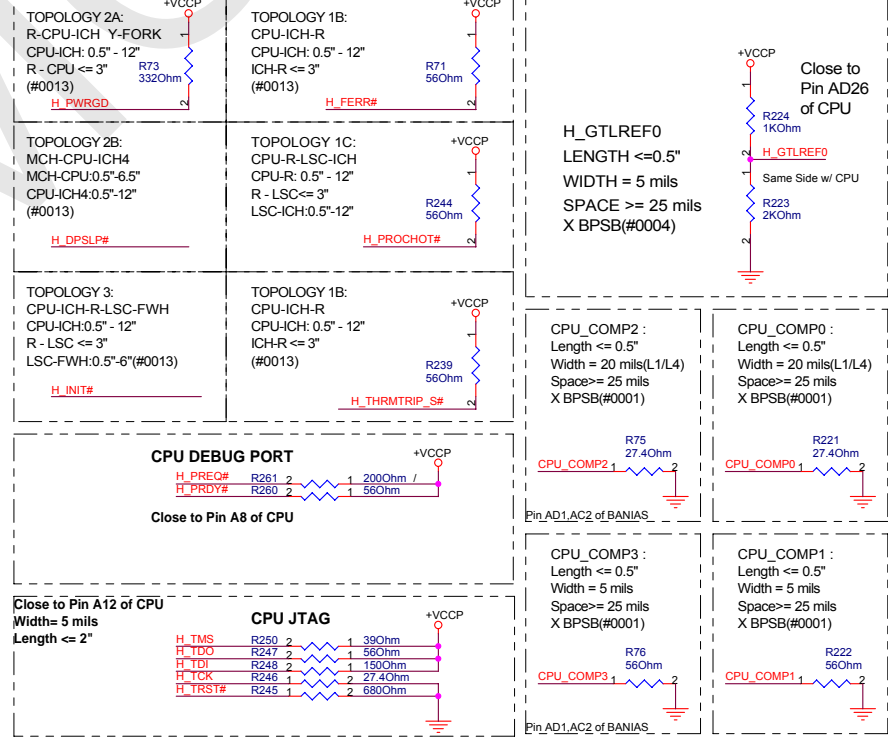


2025 2308

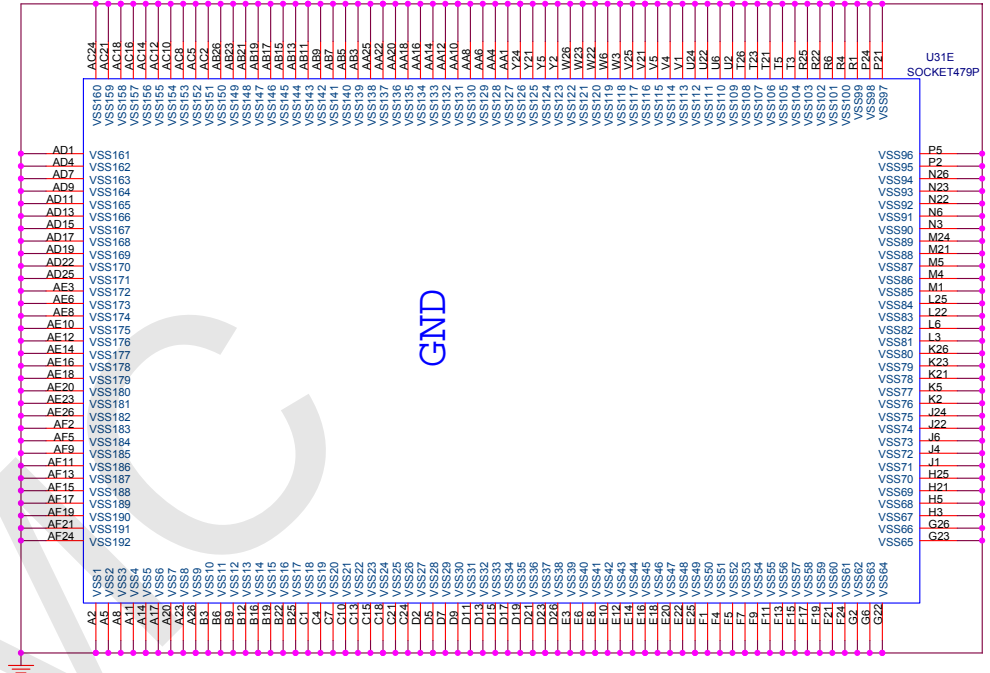
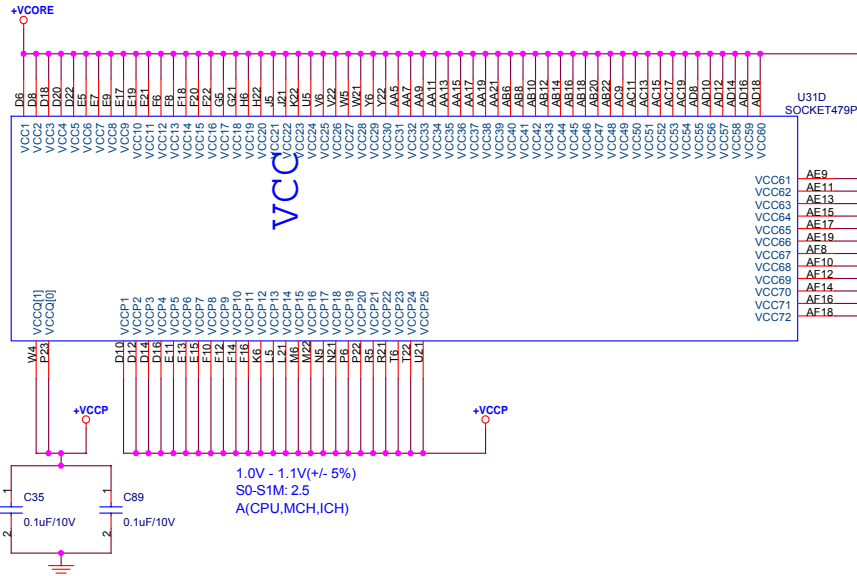
2308



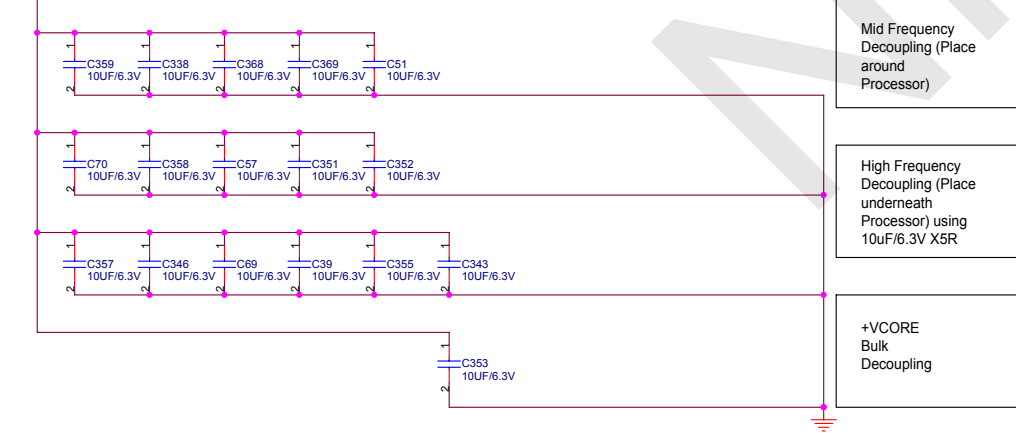
	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4		Pin 1,2	



HFM(1.3GHz-1.7GHz): 1.468V
 LFM(600MHz): 0.956V
 0.745V - 1.356V(+/- 1.5%)
 C0: 25 A
 C3: 7.59A
 C4: 0.9A

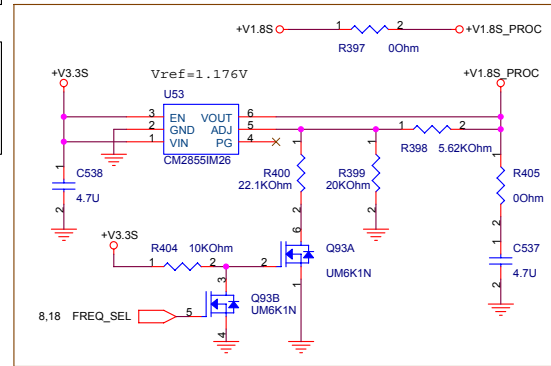
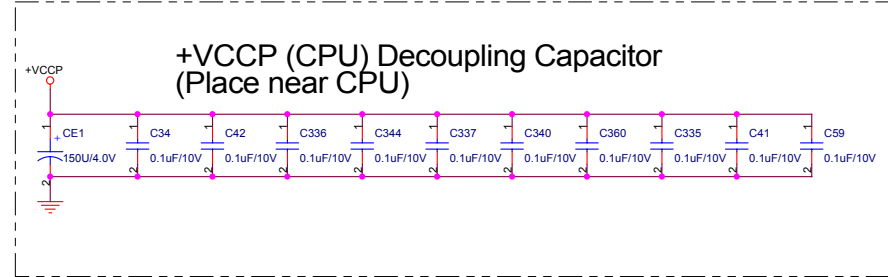


CPU VCORE Decoupling Capacitor



M3N : Four 200 uF are located in IMVP4
 A3N : Delete 10uF/6.3V from 35pcs to 17pcs

- Mid Frequency Decoupling (Place around Processor)
- High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R
- +VCORE Bulk Decoupling

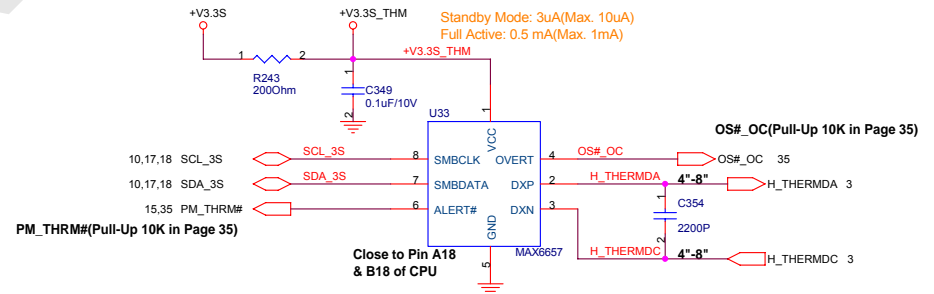


2308
 For A3N/A3NE/A3L:
 Load R397
 For A3LE:
 Load C537, C538, Q93, R398, R399, R400, R404, R405, U53

Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
 12 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 12 mils
 -----OTHER SIGNALS

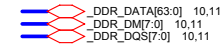
Avoid BPSB,Power



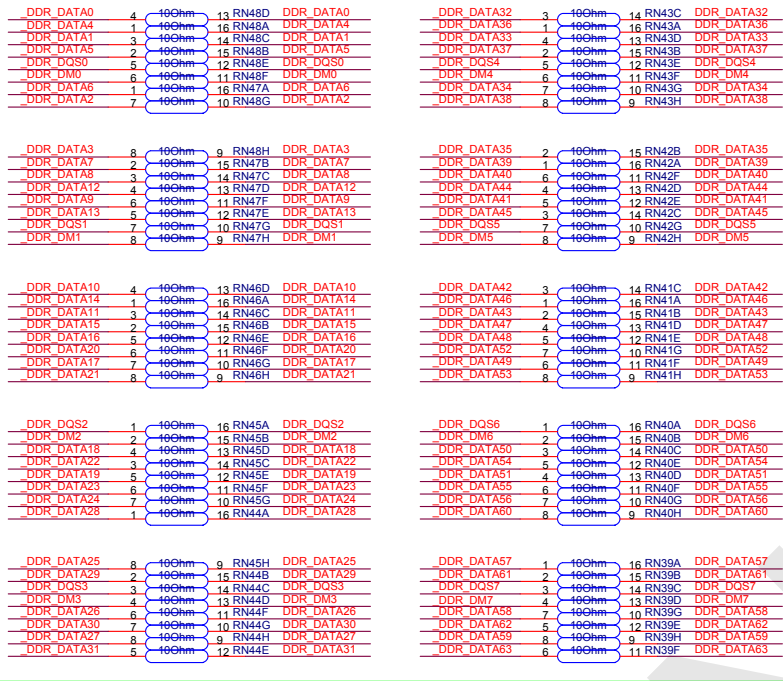
3.8W

Thermal Power: ~ 3.8W

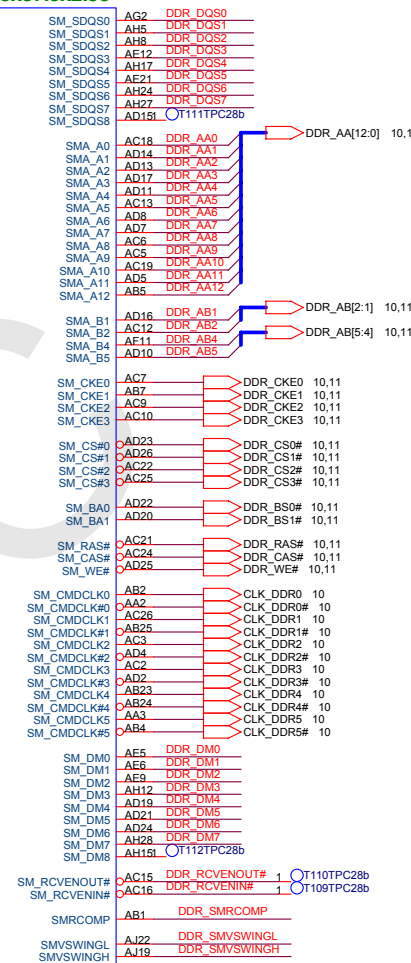
LxWxH=37.5x37.5x2.58



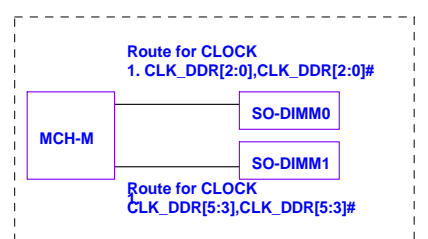
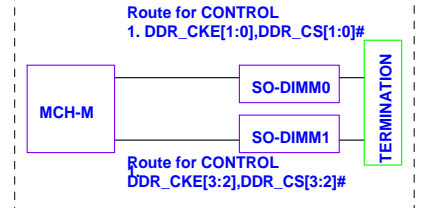
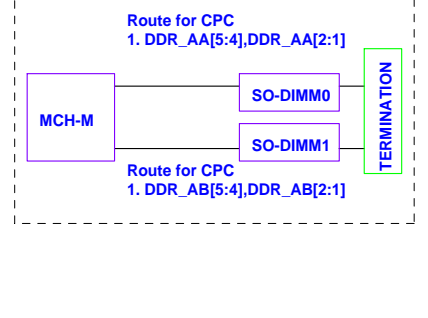
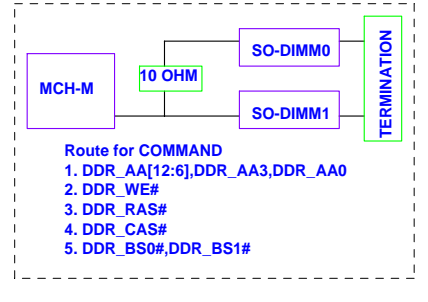
1107



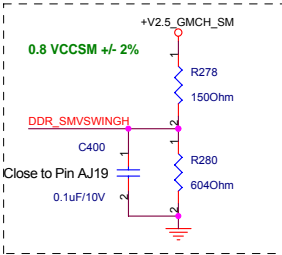
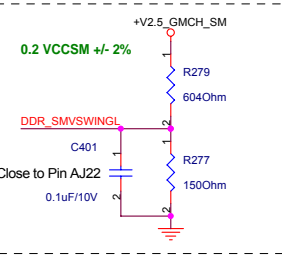
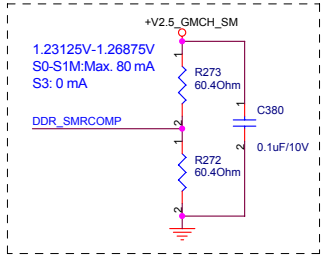
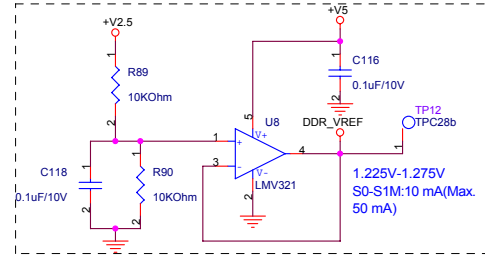
DDR SYSTEM MEMORY



(MCH-Sighting041)
M-GM system memory interface generates single pulse CKE events which may cause intermittent hangs and display corruptions when using Micron and Infineon SO-DIMMs.



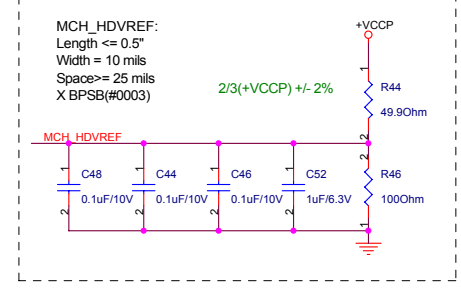
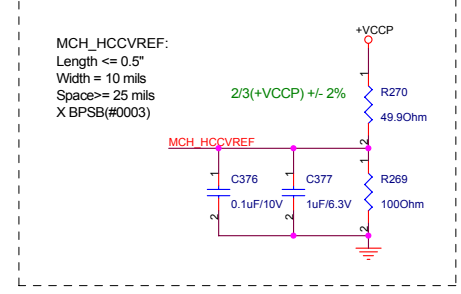
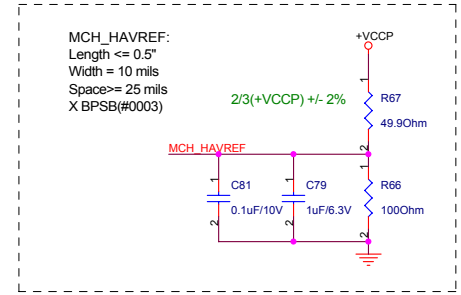
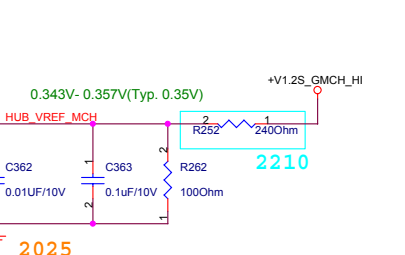
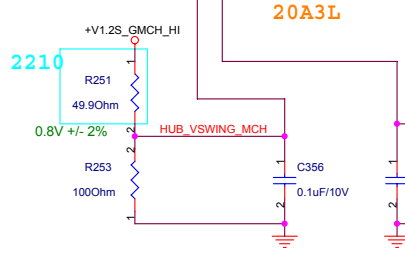
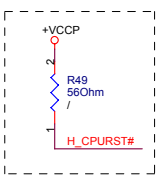
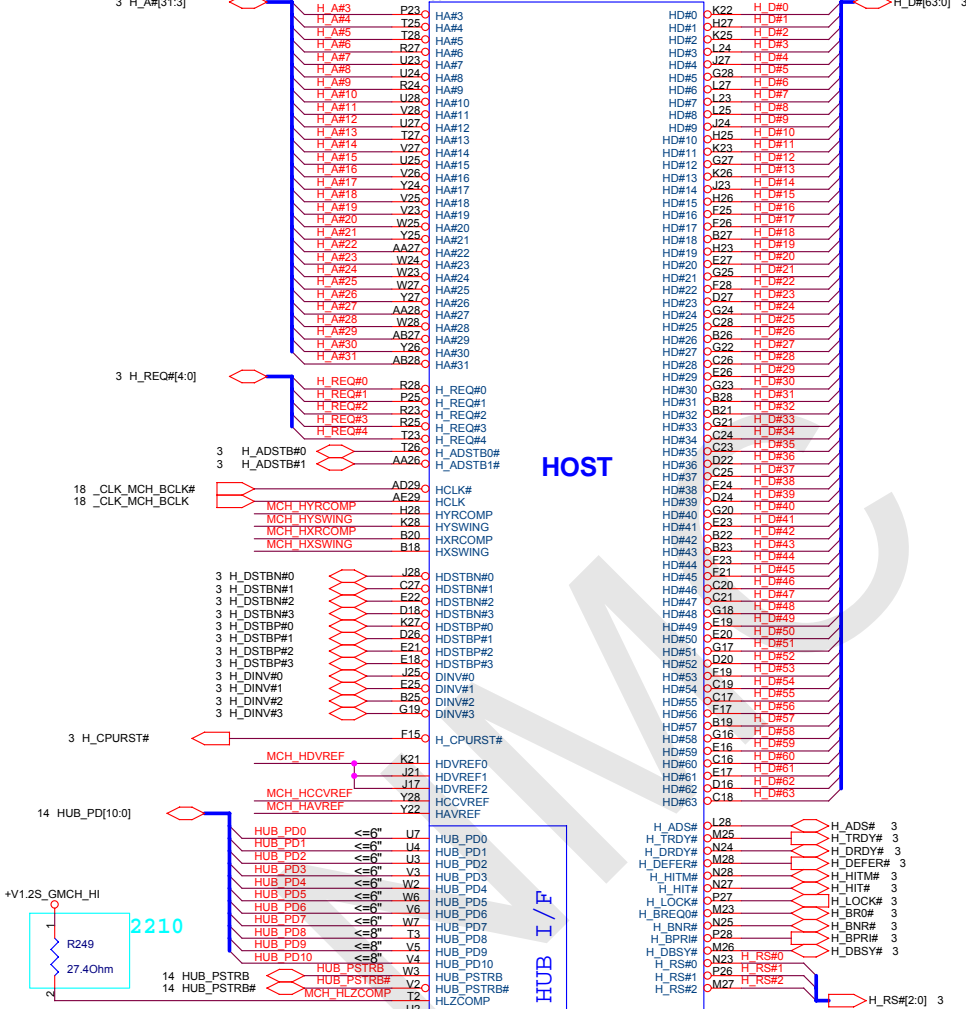
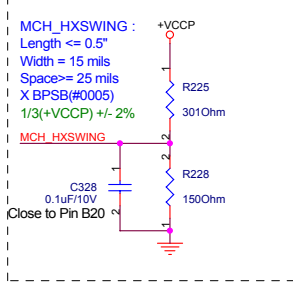
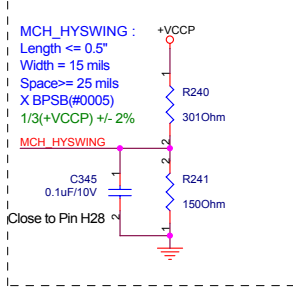
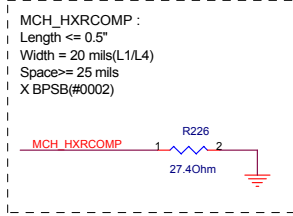
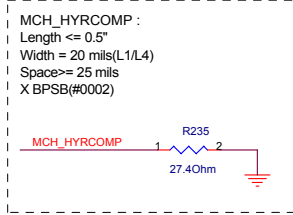
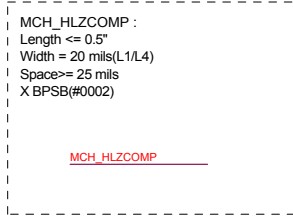
Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.



20A3L

1.23125V-1.26875V
SO-S1M:Max. 80 mA
S3: 0 mA

LxWxH=37.5x37.5x2.58



2210

R249 :	27.4ohm (10-003412704) for 855GM/852GM
	37.4ohm (10-003413704) for 855GME
	48.7ohm (10-003414807) for 852GME/852GMV

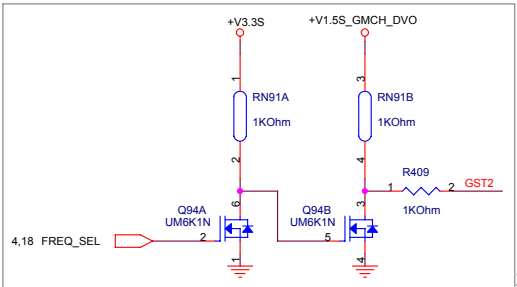
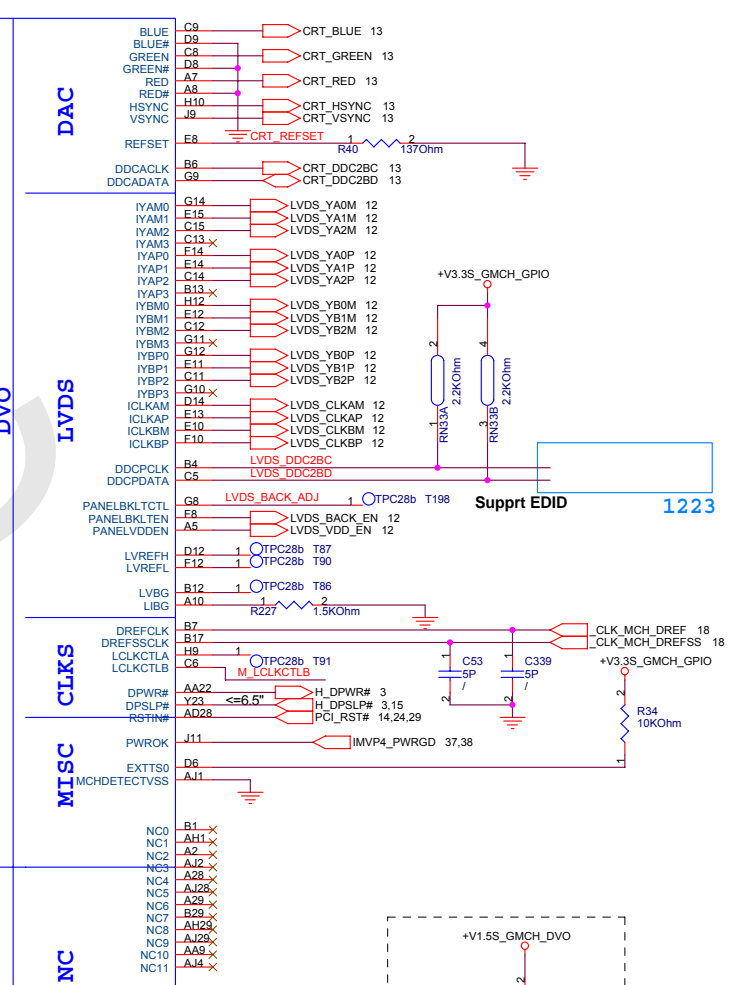
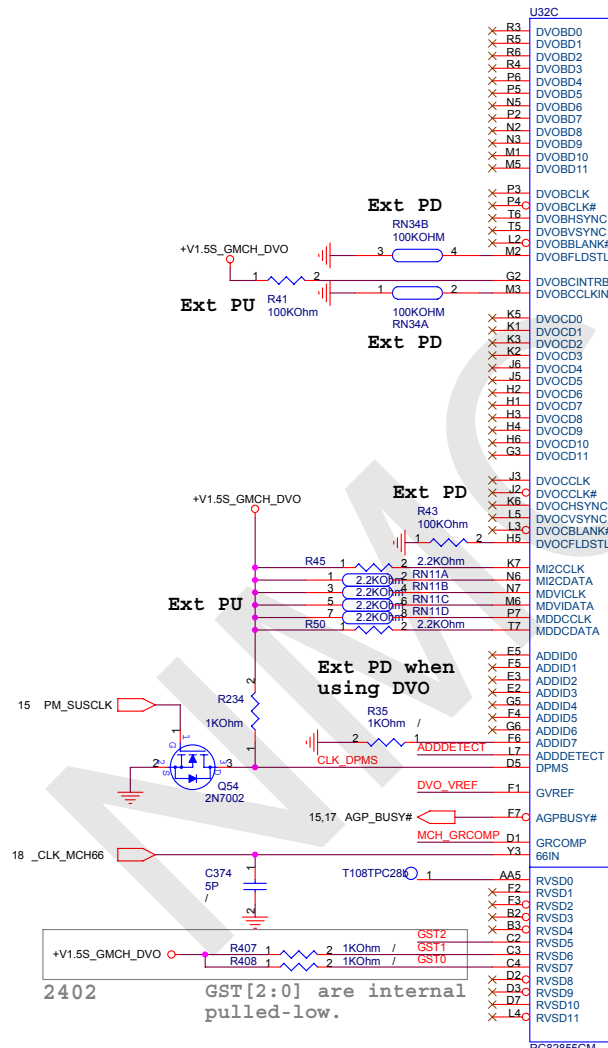
2210

R251 :	49.9ohm (10-003414909) for 855GM/852GM
	68.1ohm (10-003416801) for 855GME
	86.6ohm (10-003418606) for 852GME/852GMV

2210

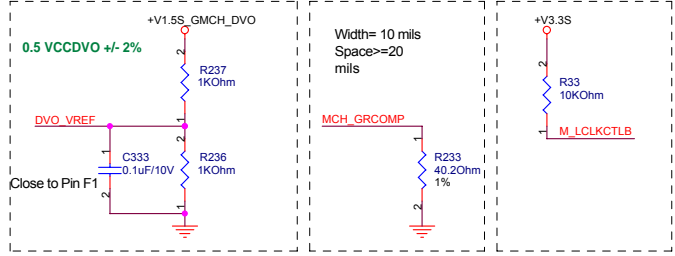
R252 :	240ohm (10-003412410) for 855GM/852GM
	287ohm (10-003412817) for 855GME
	324ohm (10-003413214) for 852GME/852GMV

U32D	RG82855GM		
C1	VSS0	VSS84	T16
G1	VSS1	VSS85	AA16
L1	VSS2	VSS86	AE16
A1	VSS3	VSS87	A17
AA1	VSS4	D17	H17
AE1	VSS5	VSS88	H17
R2	VSS6	VSS89	N17
AG3	VSS7	VSS90	R17
AG3	VSS7	VSS91	R17
AJ3	VSS8	VSS92	U17
DA	VSS9	VSS93	AB17
G4	VSS10	VSS94	AC17
K4	VSS11	VSS95	F18
T4	VSS12	VSS96	J18
WA	VSS13	VSS97	AA18
AA4	VSS14	VSS98	AG18
AC4	VSS15	VSS99	A19
AE4	VSS16	VSS100	D19
AE4	VSS16	VSS101	H19
AE4	VSS16	VSS102	AB19
AE4	VSS16	VSS103	AE19
AE4	VSS16	VSS104	F20
AE4	VSS16	VSS105	V20
AE4	VSS16	VSS106	J20
AE4	VSS16	VSS107	AA20
AE4	VSS16	VSS108	AC20
AE4	VSS16	VSS109	A21
AE4	VSS16	VSS110	D21
AE4	VSS16	VSS111	H21
AE4	VSS16	VSS112	M21
AE4	VSS16	VSS113	Q21
AE4	VSS16	VSS114	T21
AE4	VSS16	VSS115	V21
AE4	VSS16	VSS116	Y21
AE4	VSS16	VSS117	AB21
AE4	VSS16	VSS118	AG21
AE4	VSS16	VSS119	B24
AE4	VSS16	VSS120	B24
AE4	VSS16	VSS121	F22
AE4	VSS16	VSS122	J22
AE4	VSS16	VSS123	L22
AE4	VSS16	VSS124	N22
AE4	VSS16	VSS125	R22
AE4	VSS16	VSS126	U22
AE4	VSS16	VSS127	W22
AE4	VSS16	VSS128	AE22
AE4	VSS16	VSS129	A23
AE4	VSS16	VSS130	D23
AE4	VSS16	VSS131	AA23
AE4	VSS16	VSS132	AC23
AE4	VSS16	VSS133	AJ23
AE4	VSS16	VSS134	F24
AE4	VSS16	VSS135	H24
AE4	VSS16	VSS136	K24
AE4	VSS16	VSS137	M24
AE4	VSS16	VSS138	P24
AE4	VSS16	VSS139	T24
AE4	VSS16	VSS140	Y24
AE4	VSS16	VSS141	AA24
AE4	VSS16	VSS142	AG24
AE4	VSS16	VSS143	A25
AE4	VSS16	VSS144	D25
AE4	VSS16	VSS145	AA25
AE4	VSS16	VSS146	AE25
AE4	VSS16	VSS147	G26
AE4	VSS16	VSS148	J26
AE4	VSS16	VSS149	L26
AE4	VSS16	VSS150	N26
AE4	VSS16	VSS151	R26
AE4	VSS16	VSS152	U26
AE4	VSS16	VSS153	W26
AE4	VSS16	VSS154	AB26
AE4	VSS16	VSS155	A27
AE4	VSS16	VSS156	F27
AE4	VSS16	VSS157	AC27
AE4	VSS16	VSS158	AJ27
AE4	VSS16	VSS159	AG28
AE4	VSS16	VSS160	AE28
AE4	VSS16	VSS161	C29
AE4	VSS16	VSS162	C29
AE4	VSS16	VSS163	E29
AE4	VSS16	VSS164	C29
AE4	VSS16	VSS165	J29
AE4	VSS16	VSS166	L29
AE4	VSS16	VSS167	N29
AE4	VSS16	VSS168	U29

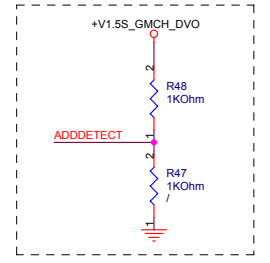


2402

When no using DVO



20A3L

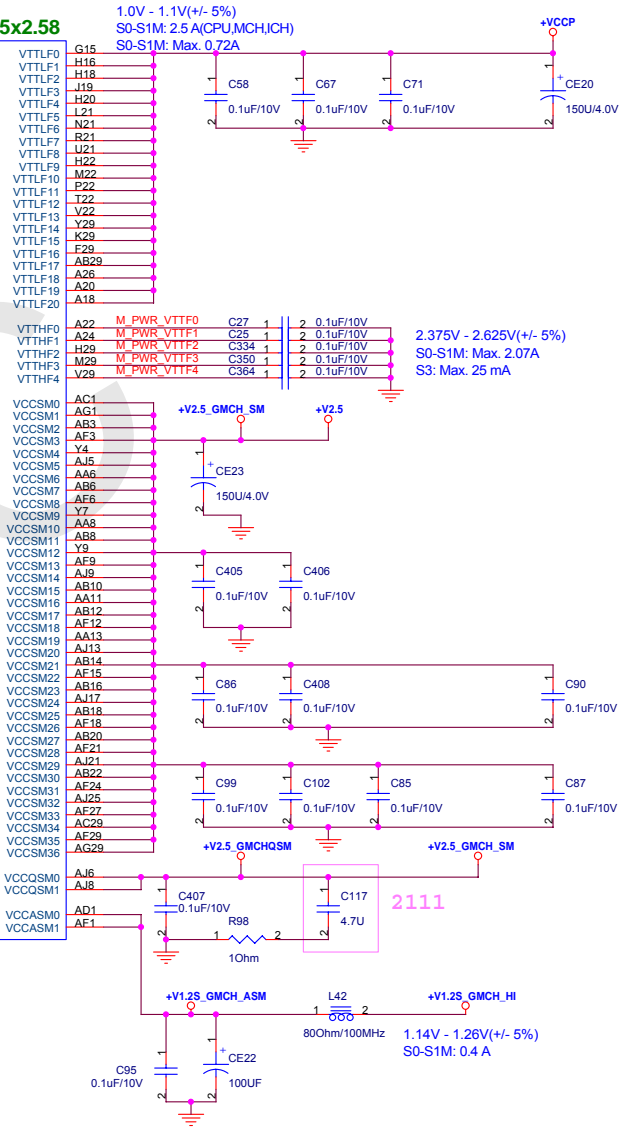


(MCH-Sighting041)
The core supply (1.2V) should be powered up a minimum of 1ms before the DVO and GPIO IO (1.5V and 3.3V) voltage rails.

LxWxH=37.5x37.5x2.58

POWER

- J15 VCC0
- P13 VCC1
- T13 VCC2
- N14 VCC3
- R14 VCC4
- U14 VCC5
- P18 VCC6
- T18 VCC7
- AA15 VCC8
- N16 VCC9
- R16 VCC10
- U16 VCC11
- P17 VCC12
- T17 VCC13
- AA17 VCC14
- AA19 VCC15
- W21 VCC16
- H14 VCC17
- V1 VCCCHL0
- Y1 VCCCHL1
- W5 VCCCHL2
- U6 VCCCHL3
- U8 VCCCHL4
- W8 VCCCHL5
- V7 VCCCHL6
- V9 VCCCHL7
- D29 VCCADPLL
- Y2 VCCAGPLL
- A6 VCCADPLLA
- B16 VCCADPLLB
- E1 VCCDVO_0
- J1 VCCDVO_1
- N1 VCCDVO_2
- E4 VCCDVO_3
- J4 VCCDVO_4
- M4 VCCDVO_5
- E6 VCCDVO_6
- H7 VCCDVO_7
- J8 VCCDVO_8
- L8 VCCDVO_9
- M8 VCCDVO_10
- N8 VCCDVO_11
- R8 VCCDVO_12
- K9 VCCDVO_13
- M9 VCCDVO_14
- P9 VCCDVO_15
- A9 VCCADAC0
- B9 VCCADAC1
- B8 VSSADAC
- A11 VCCALVDS
- B11 VSSALVDS
- G13 VCCDLVDS0
- B14 VCCDLVDS1
- J13 VCCDLVDS2
- B15 VCCDLVDS3
- F9 VCTXLVDS0
- B10 VCTXLVDS1
- D10 VCTXLVDS2
- A12 VCTXLVDS3
- A3 VCCGPIO_0
- A4 VCCGPIO_1



20A3L

2209

NB
VCC,VCCASM,VCCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB:
855GM/852GM: 1.2V
855GME: 1.35V
852GME/852GMV: 1.5V

Caution:
L2 be placed between Pin U9 and U13

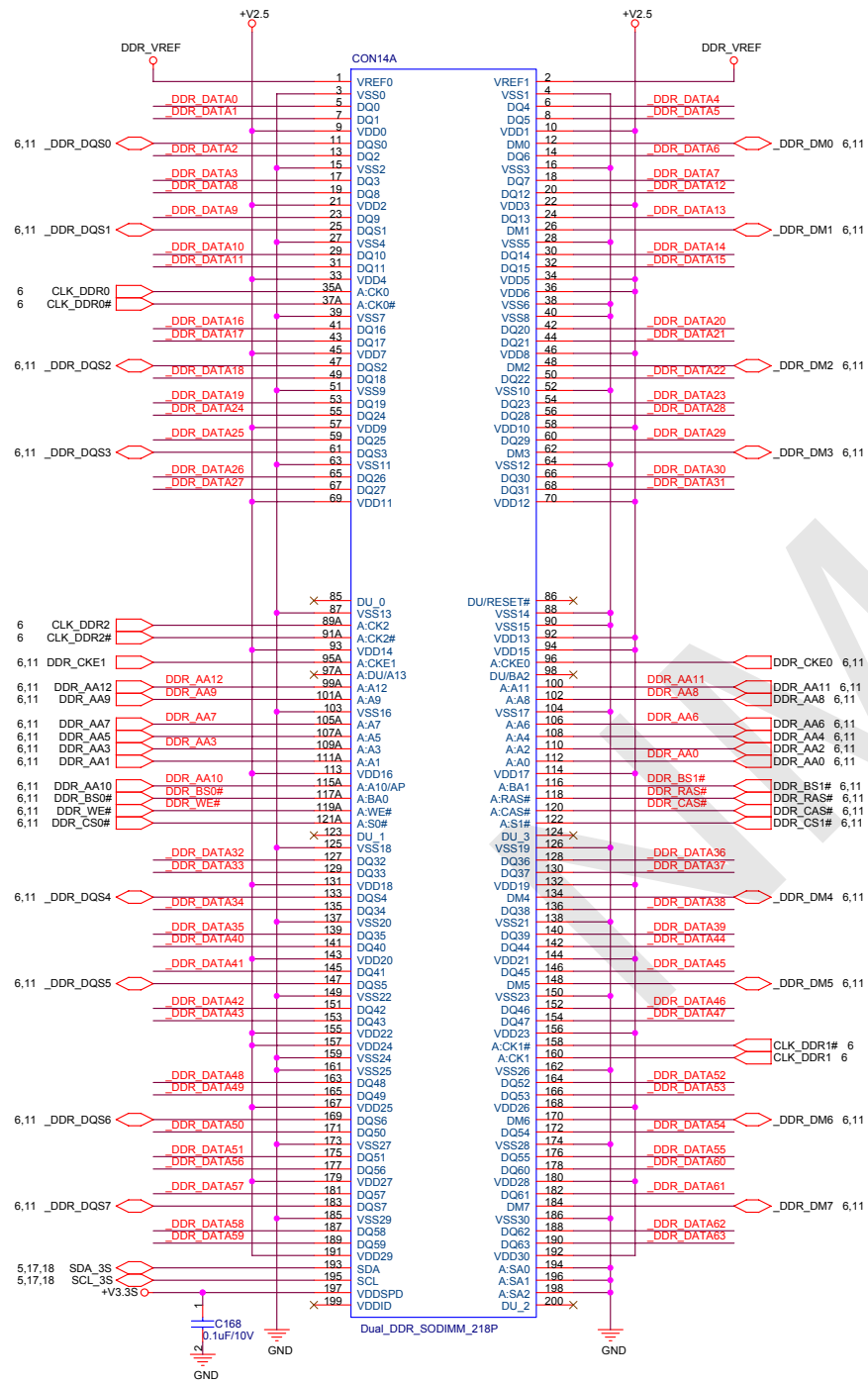
Caution:
There is no vias between Pin B8 and C99,C100 (It means C99,C100 must be in same layer with MCHM)

Caution:
There is no vias between Pin B11 and C106,C107 (It means C106,C107 must be in same layer with MCHM)

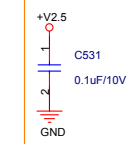
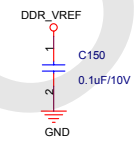
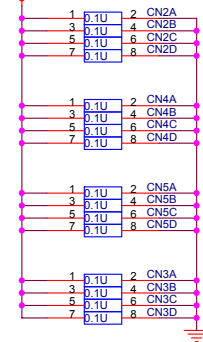
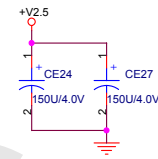
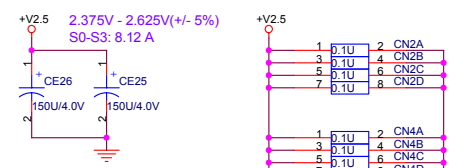
2218

2218

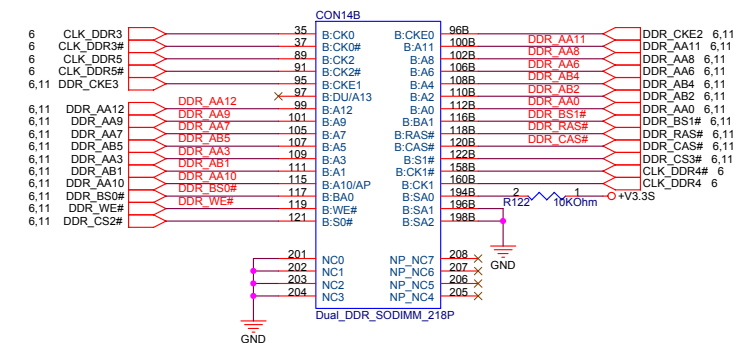
6.11 _DDR_DATA[63:0]



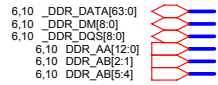
FOR +V2.5 DECOUPLING



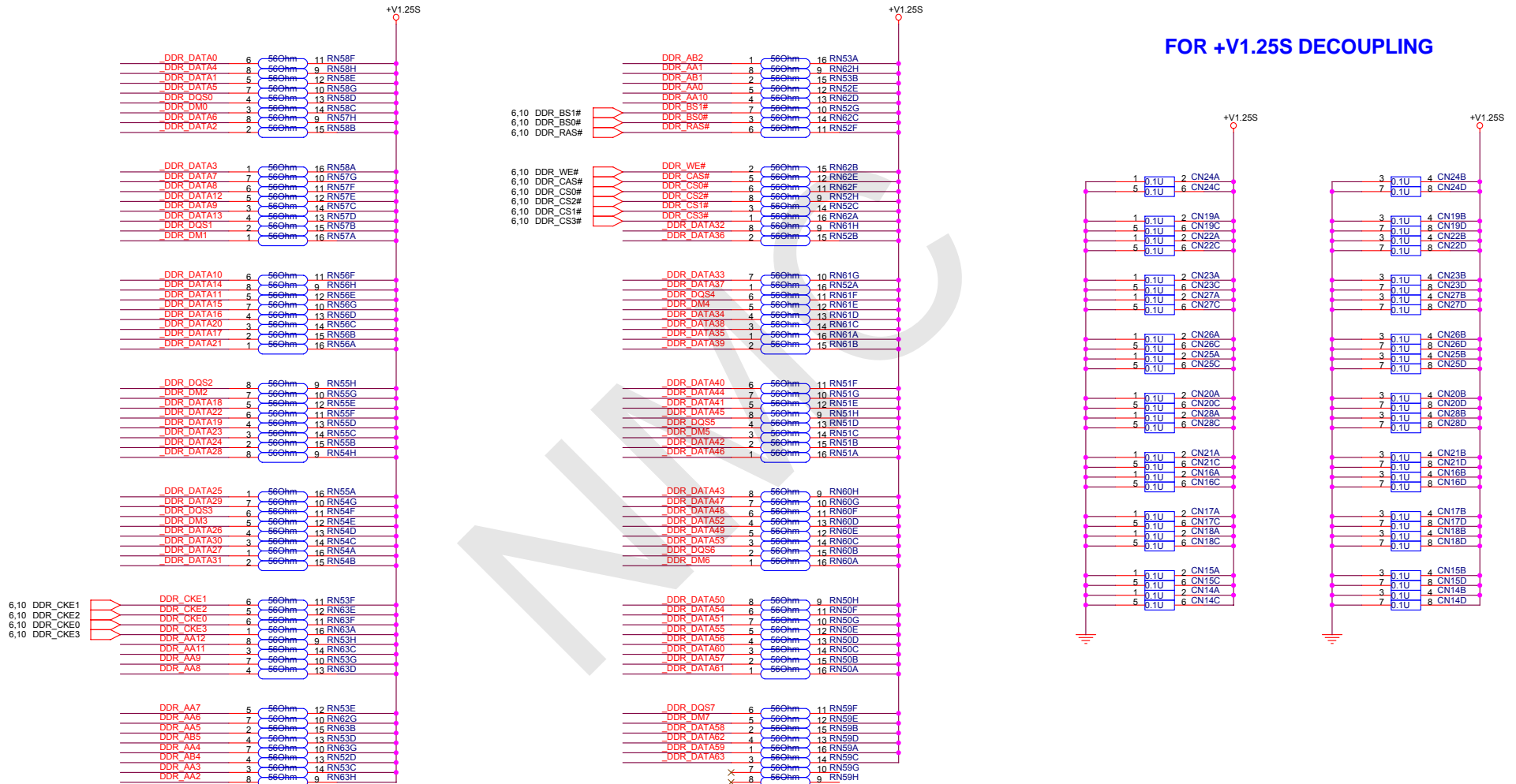
2024
EMI : Close to DDR
socket power plane
of +V2.5



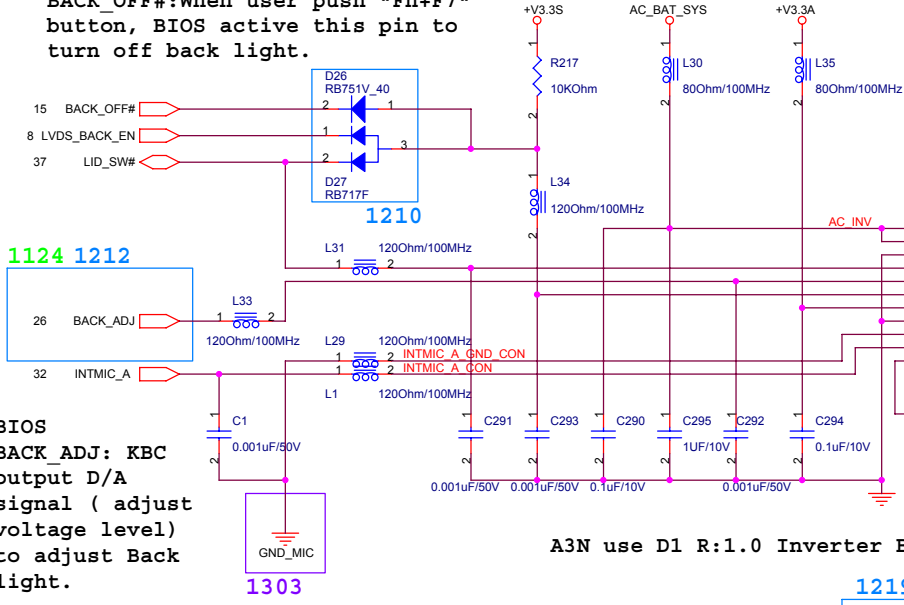
DDR TERMINATION



FOR +V1.25S DECOUPLING



BIOS
BACK_OFF#:When user push "Fn+F7"
 button, BIOS active this pin to
 turn off back light.



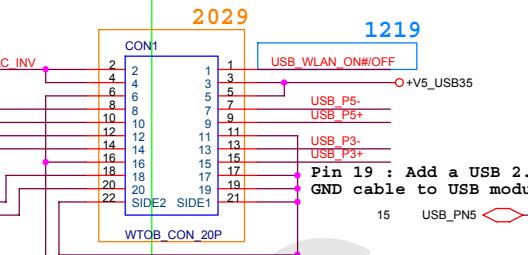
1124 1212

BIOS
BACK_ADJ: KBC
 output D/A
 signal (adjust
 voltage level)
 to adjust Back
 light.

1303

A3N use D1 R:1.0 Inverter Board

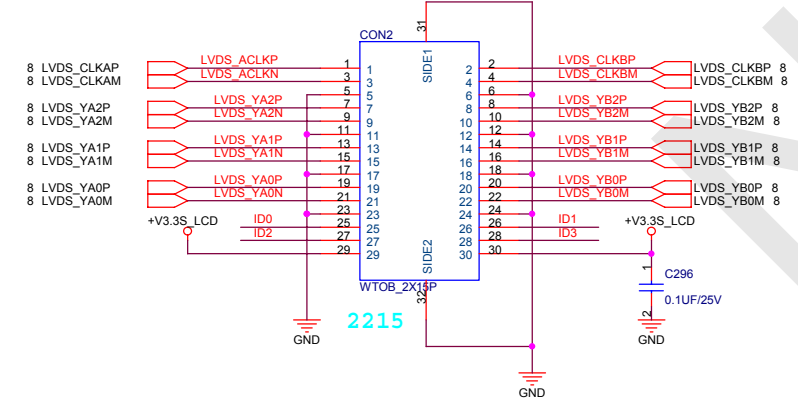
1128



USB PORT 3 for CAMERA

USB PORT 5 for WLAN

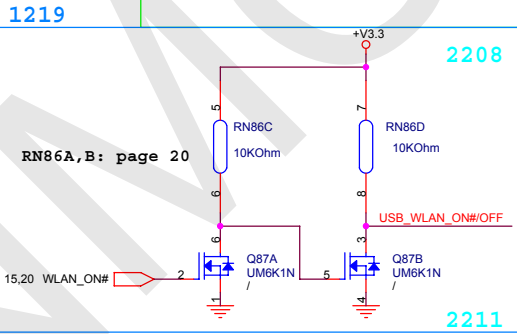
LCD CABLE ID:	PID3	PID2	PID1	PID0
14.1 XGA	1	1	1	1
15.1 XGA	1	1	0	1
15.1 SXGA+	1	0	1	1



LCD Power

SI3865: US\$0.22

1136

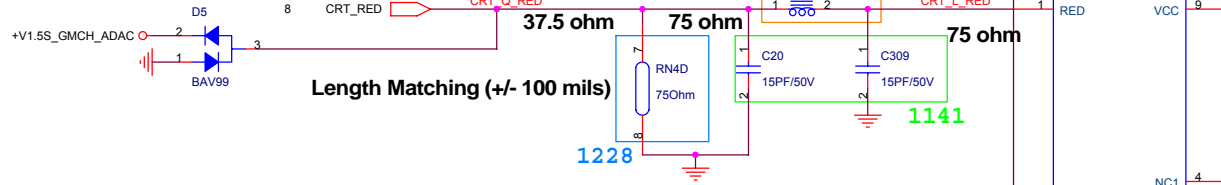


RN86A,B: page 20

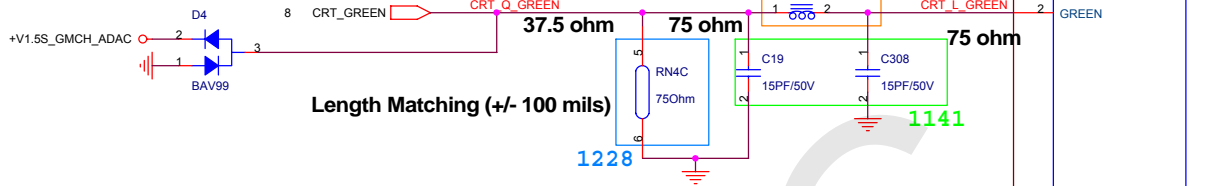
1223

Place Pi-Filter close to CRT
(<= 200 mils)

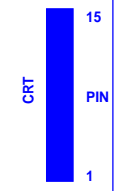
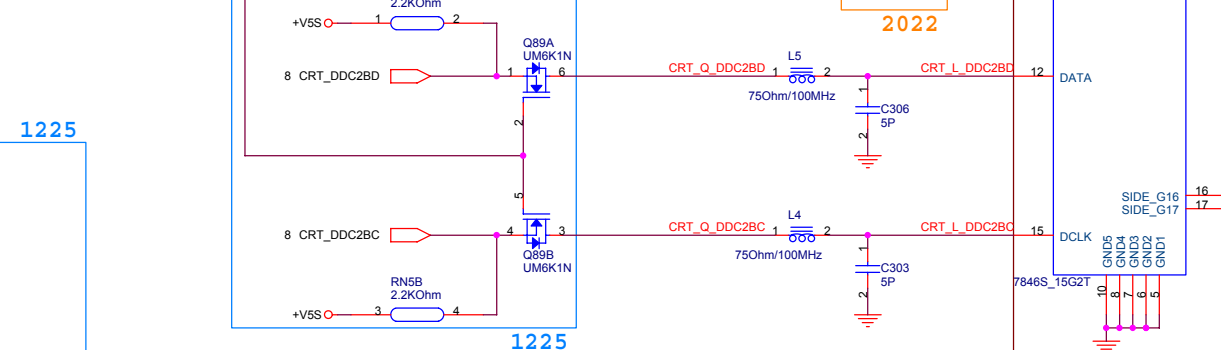
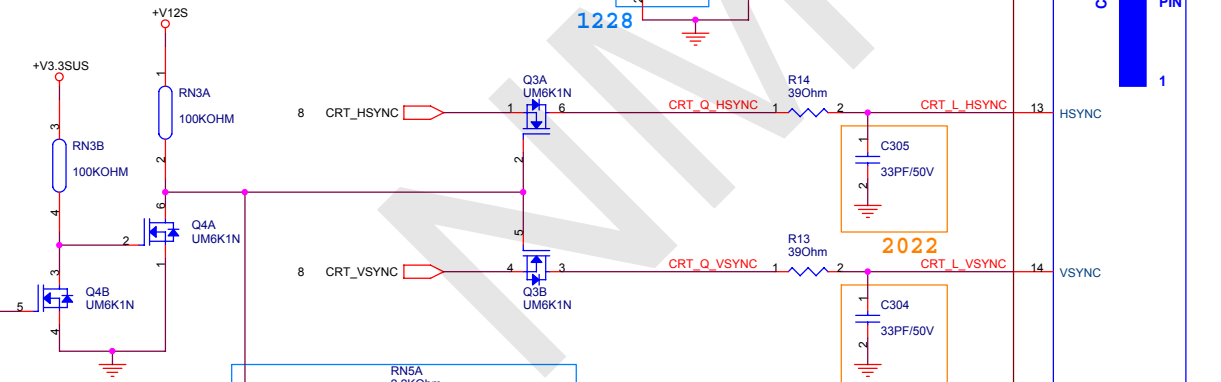
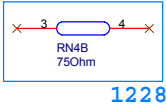
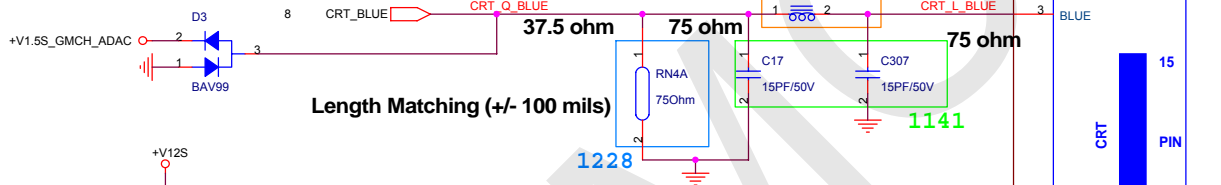
Guarded by GND (Space >= 20mils)



Guarded by GND (Space >= 20mils)



Guarded by GND (Space >= 20mils)



1115 2309
2222 2408

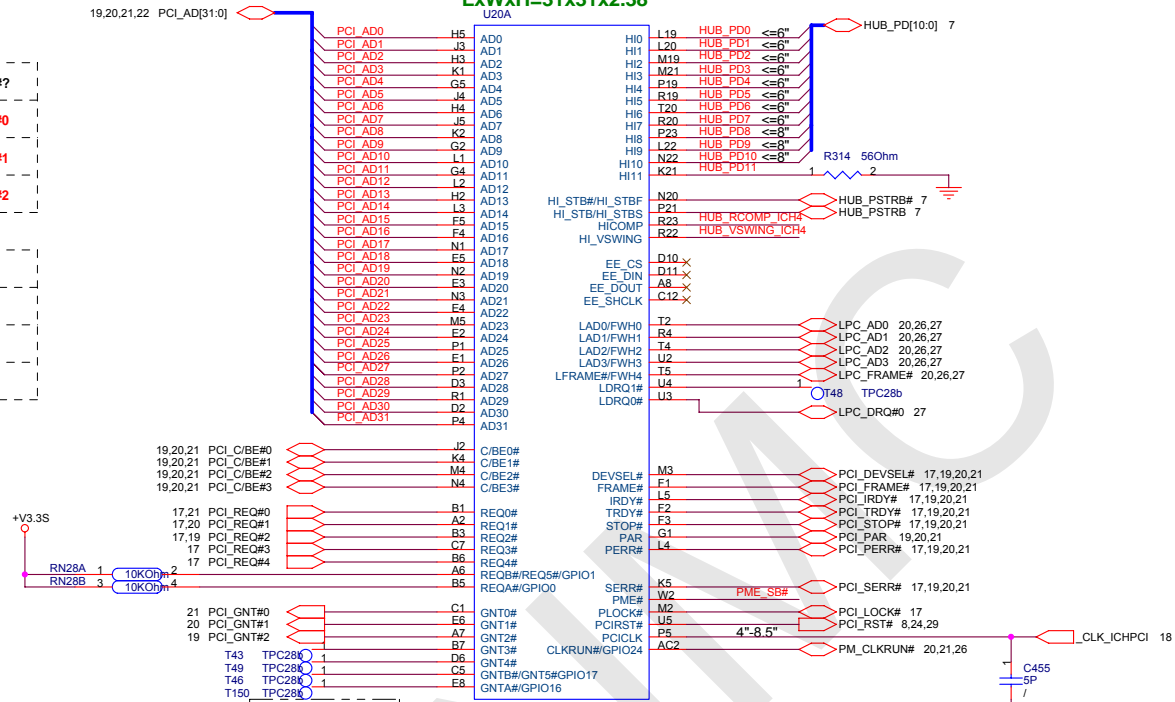
Use Daisy-Chain Topology

LxWxH=31x31x2.38

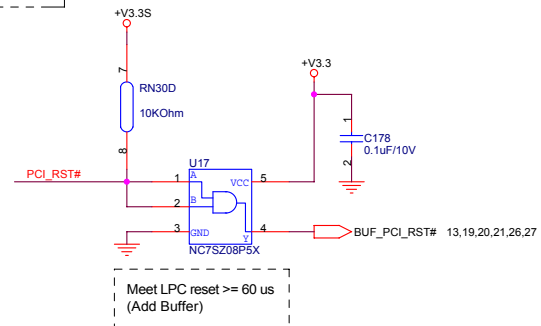
U20A

PCI_REQ#	PCI_REQ#?
CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL	PCI_AD?
CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

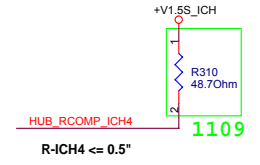


ICH4 pin E8
Strap Option
Default: Pull-High 20K
Pull-Down for BIOS
TOP-BLOCK SWAP

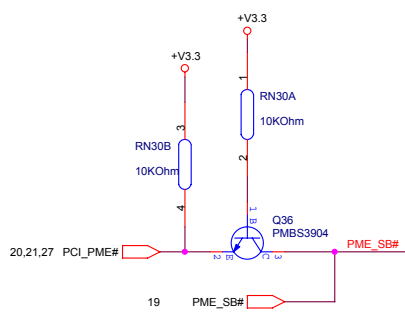
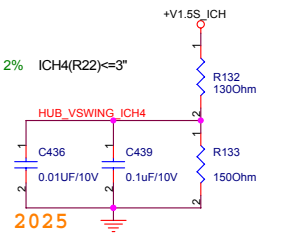


Meet LPC reset >= 60 us
(Add Buffer)

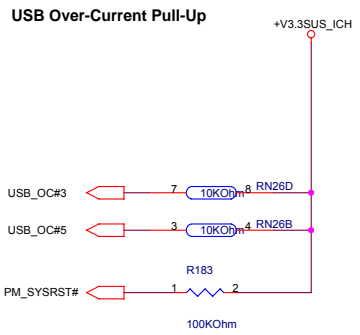
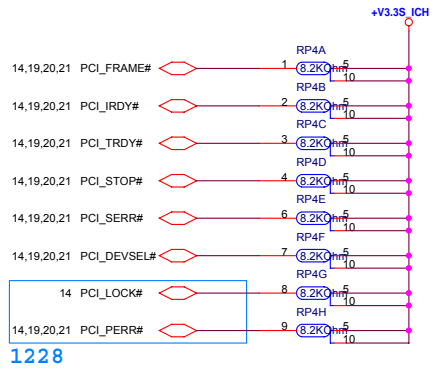
Strap Option
Default: Pull-Down
Pull-High for Hub
Interface 1.5
Buffer Mode
ICH4 USE



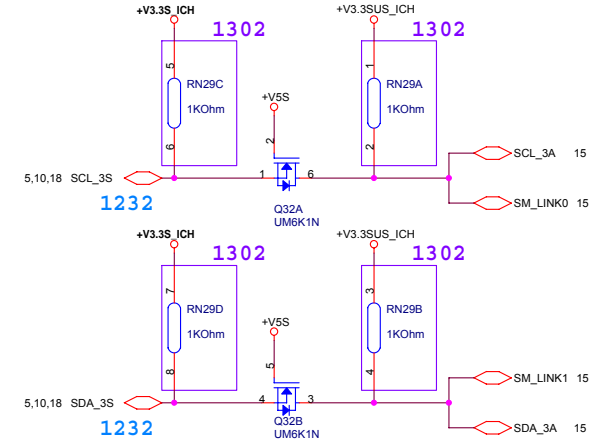
Caution:
The VREF of HUB interface is 0.35V
The VSWING of HUB interface is 0.8V
But in Intel CRB, their naming
convention will make people
confused.



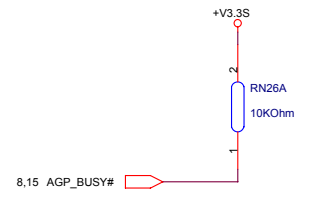
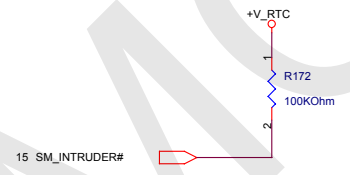
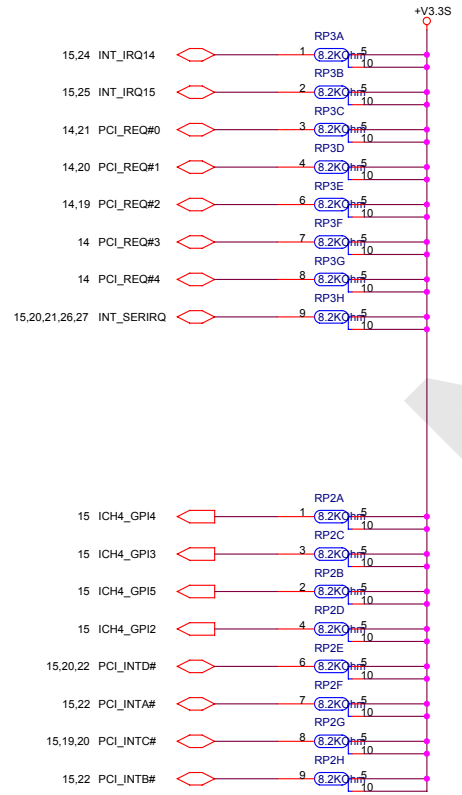
pull up to VccSus3_3 by
internal pull-up resistor



ICH4 SMLink & SMBus must be tied together

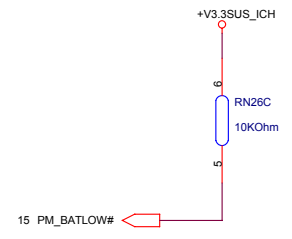


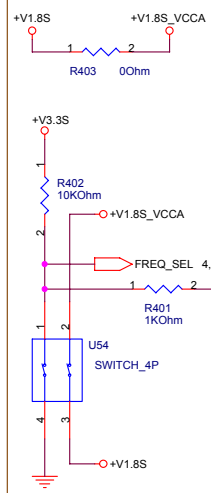
Can Swap



BATTERY LOW

ICH4

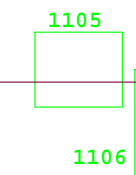




CLK_EN# is OD for MAX1987



FS4	FS3	FUNCTION
0	0	100MHz
0	1	133MHz (D)
1	0	200MHz
1	1	166MHz



For A3LE:
Load R401, R402, U54

For A3N/A3NE/A3L:
Load R403, R368

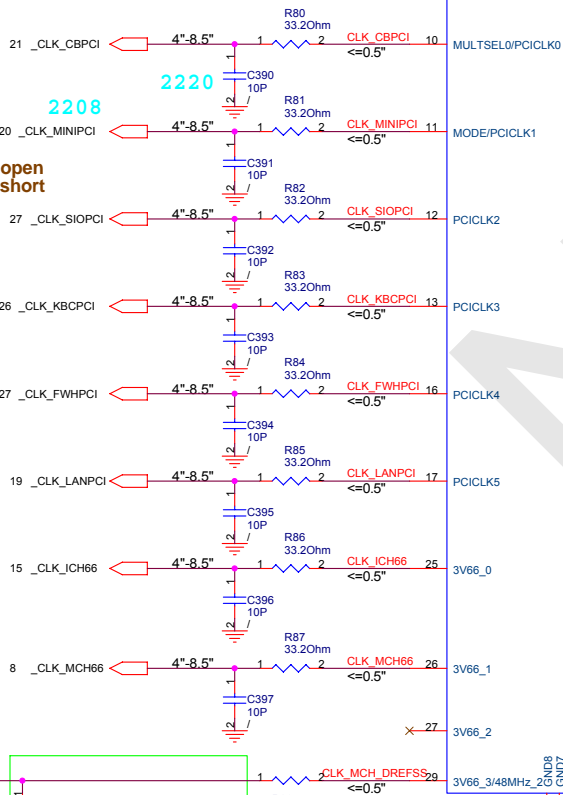
1(H): FSB Freq=133MHz & VCCA[0]=1.5V
4(L): FSB Freq=100MHz & VCCA[0]=1.8V

2: Dothan(533) CPU
3: Celeron/Banias /Dothan(400) CPU

U54 switch to 1, pin1 & 4 open
U54 switch to 4, pin1 & 4 short

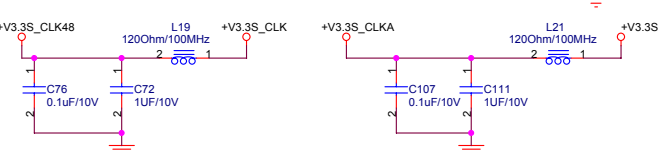
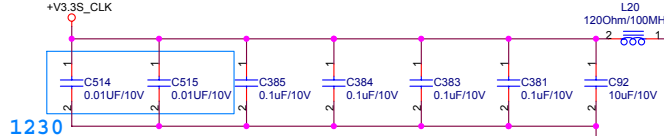
CLK33 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: same as CLK66

CLK66 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: +/- 100 mils



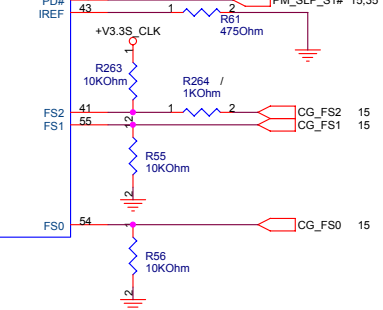
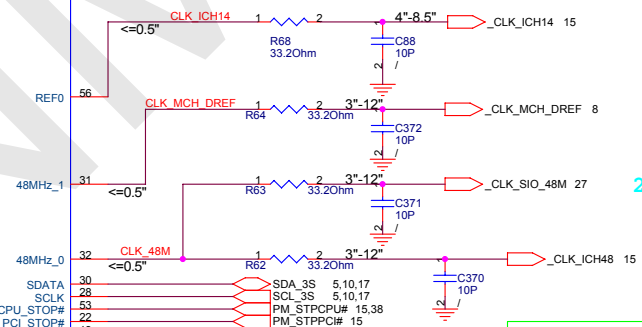
I2C address: D2H
3.3V +/- 5%
S1M: 40 mA
S0: 360 mA

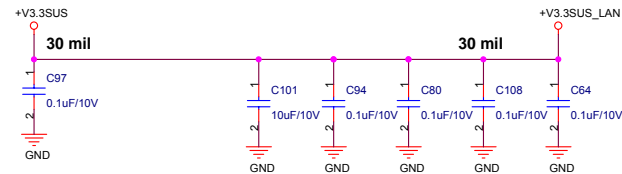
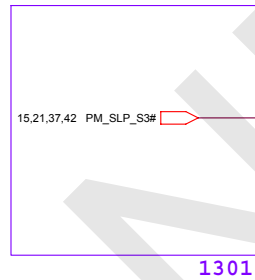
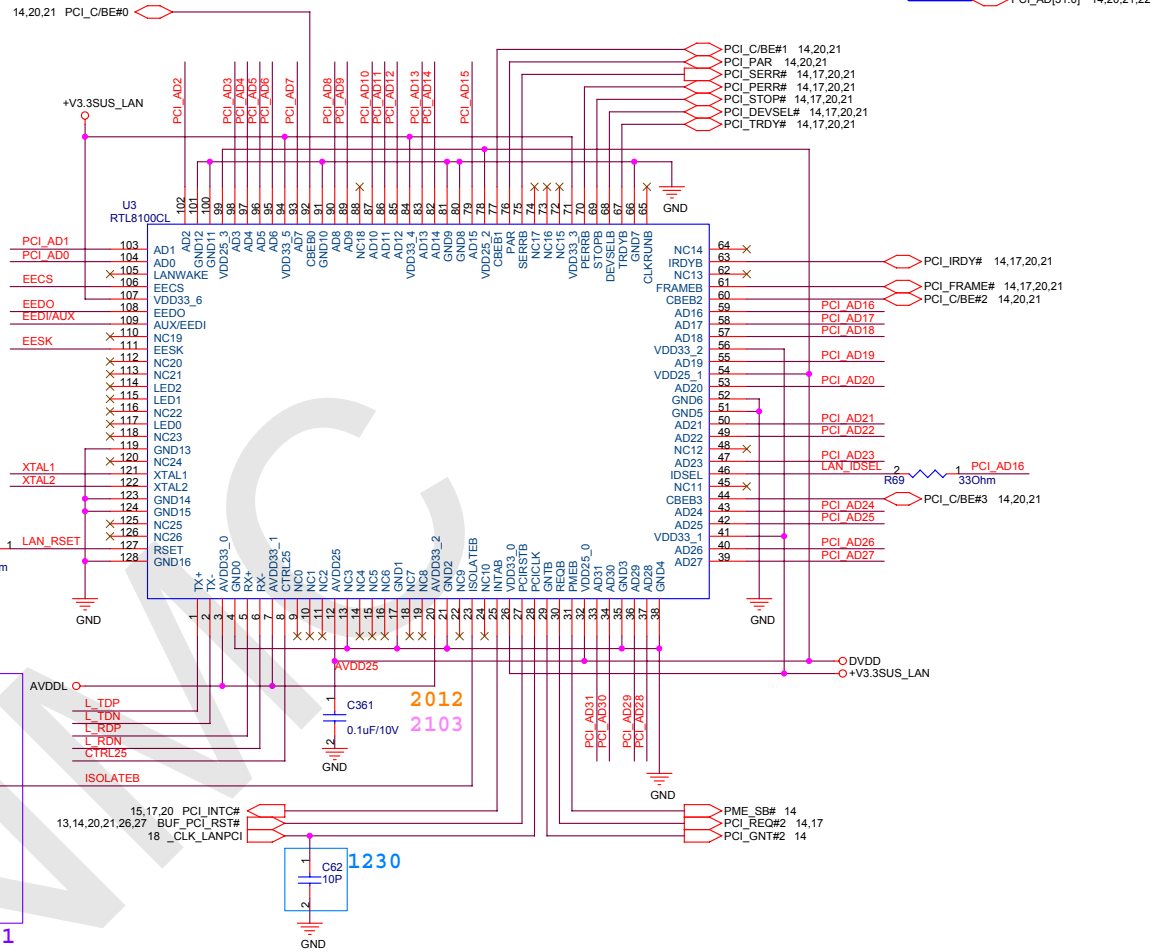
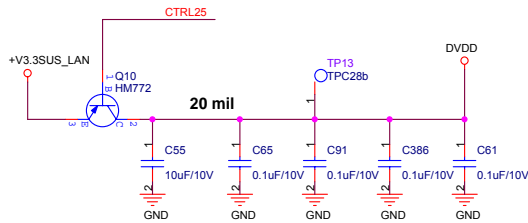
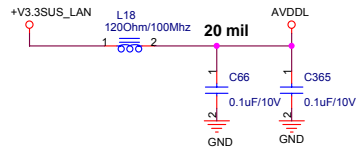
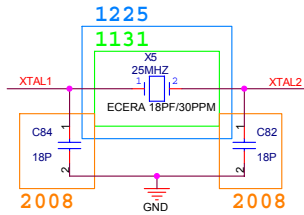
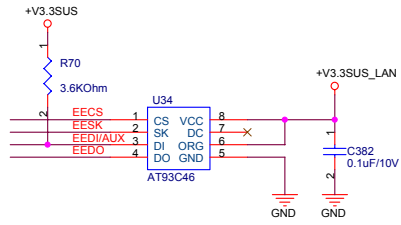
FS1	FS0	FUNCTION
0	0	66 MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz

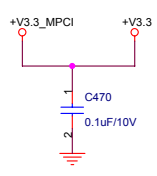
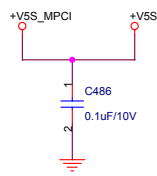
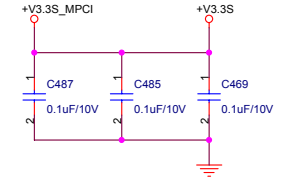
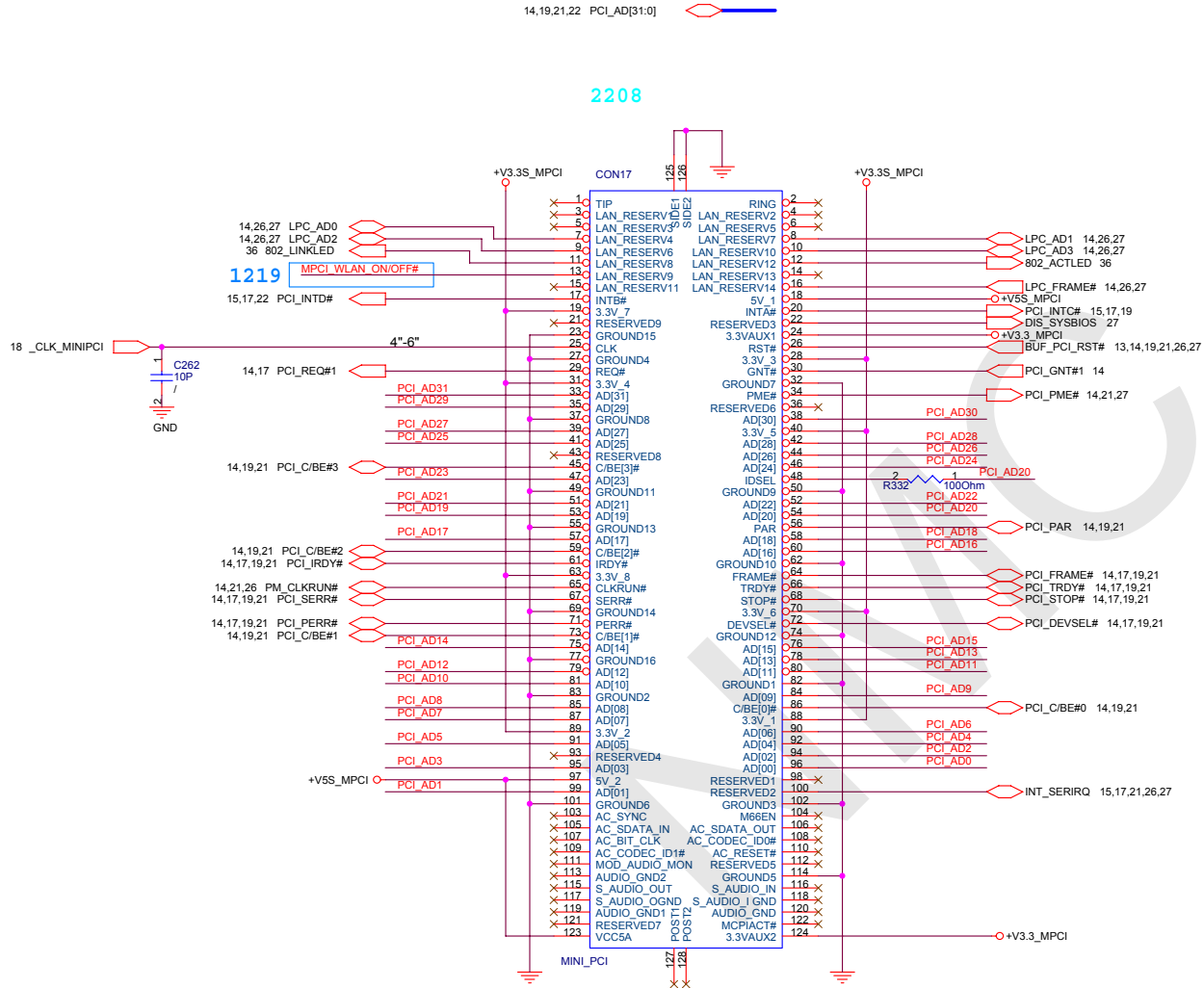


CLK_CPU_BCLK# must be low in C3

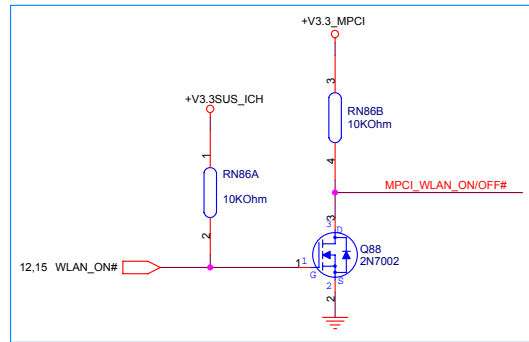
HOST_CLK GROUP
In L3 or L6
Pair Width/Space: 4/4 mils
Group Space: >= 25 mils
Length Match: +/- 10 mils



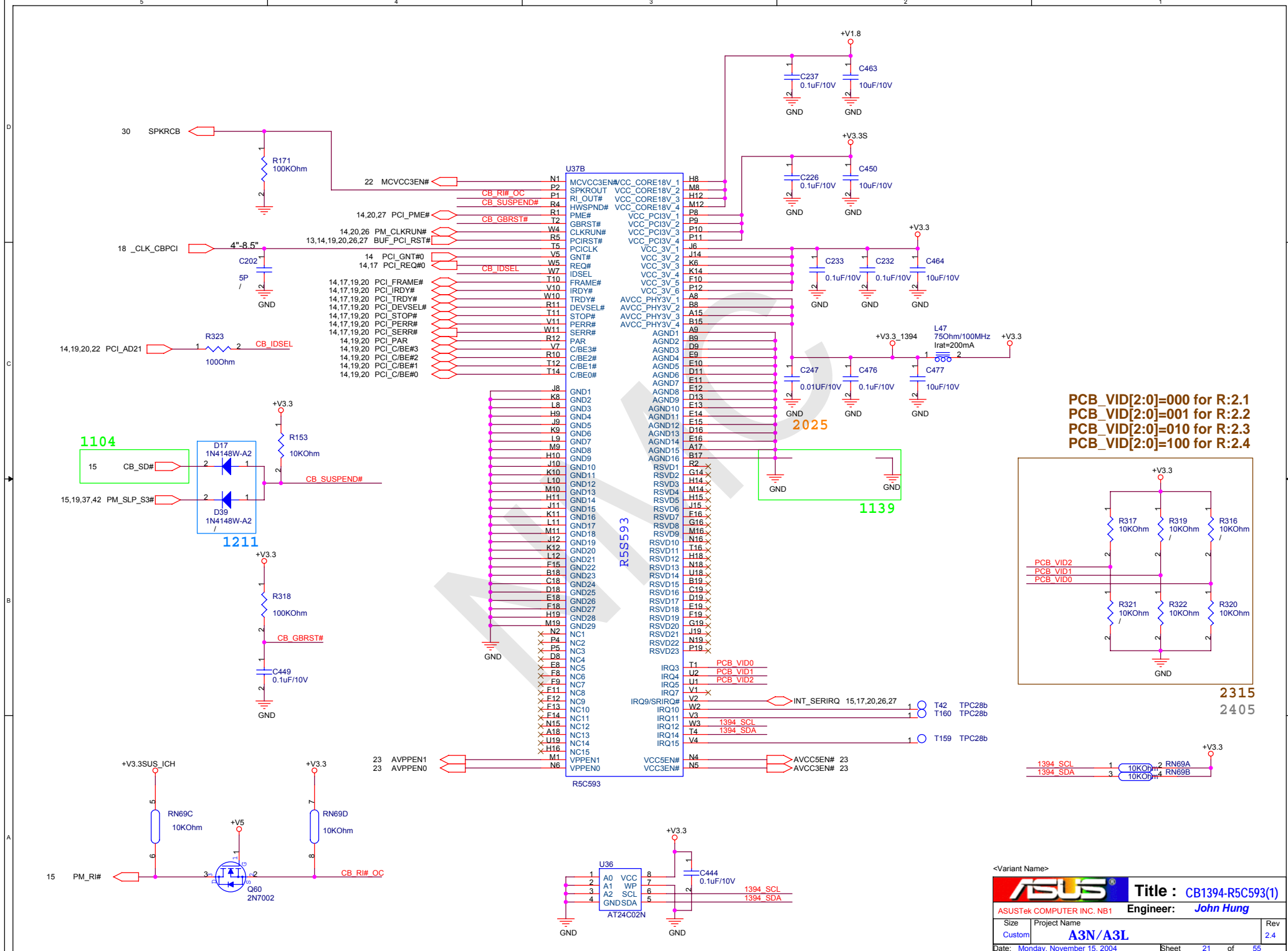




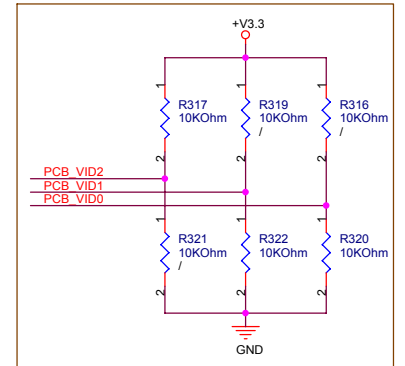
Intel Calexico(802.11a+802.11b)
 802.11b Tx: 500-526 mA Rx: 280-299 mA Sleep: 30 mA
 802.11a Tx: 435-475 mA Rx:310-327 mA Sleep: 30 mA



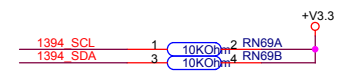
1219

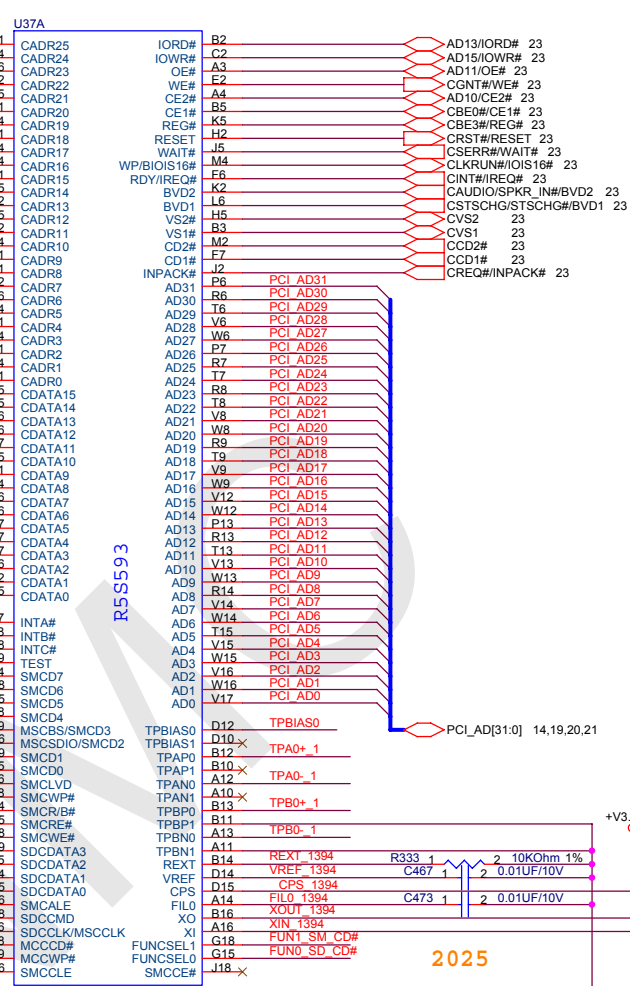
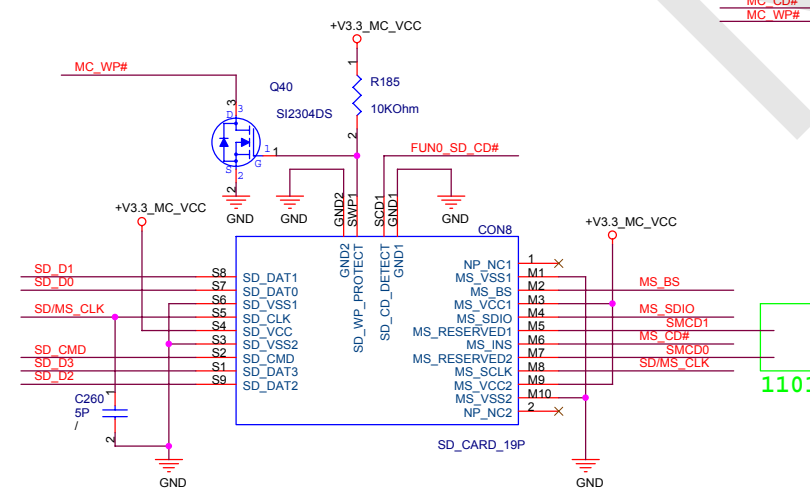
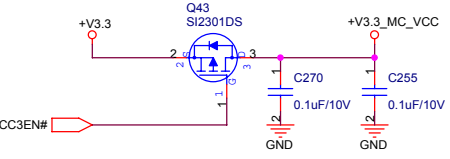
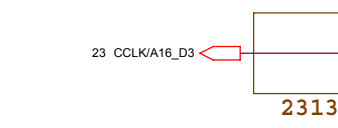


PCB_VID[2:0]=000 for R:2.1
 PCB_VID[2:0]=001 for R:2.2
 PCB_VID[2:0]=010 for R:2.3
 PCB_VID[2:0]=100 for R:2.4



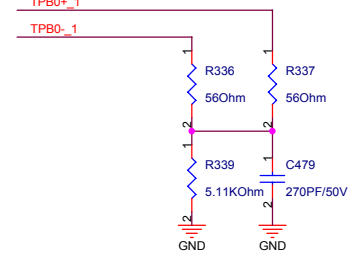
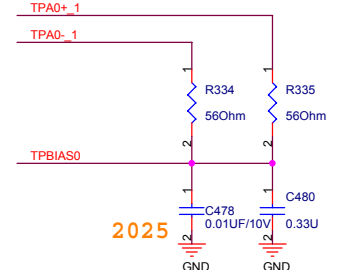
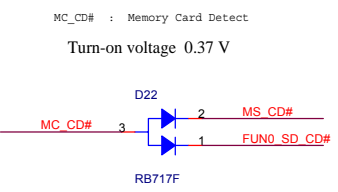
2315
 2405



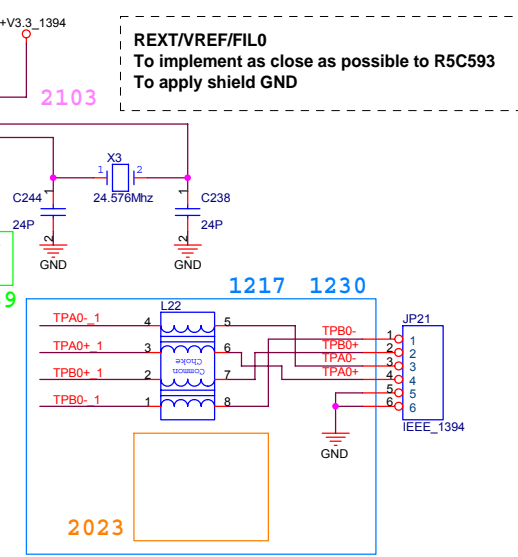


Memory Card Detect

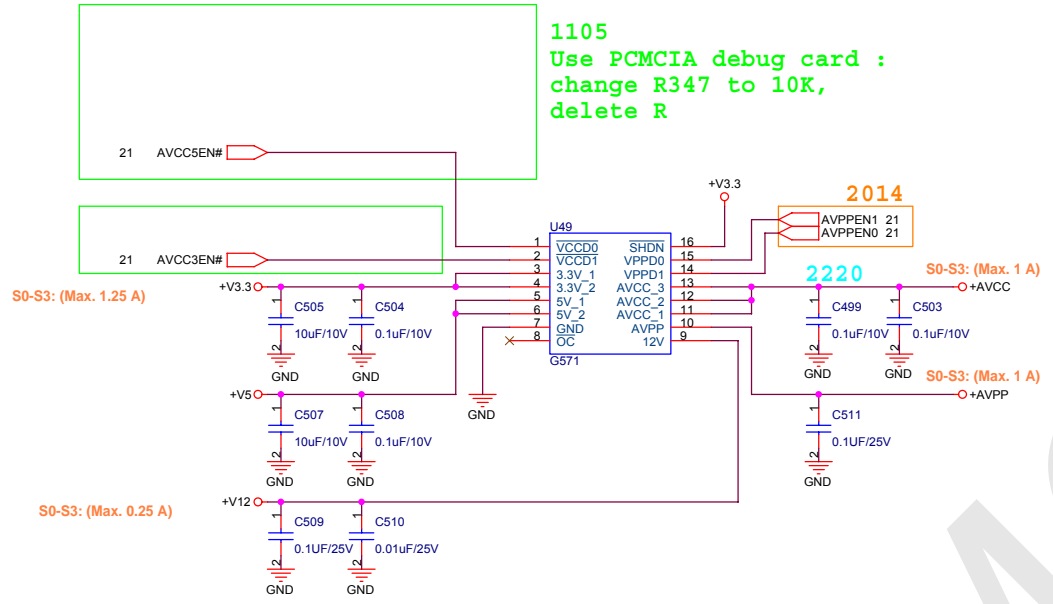
FUNSEL1	FUNSEL0	Function
0	0	Not Support
0	1	SmartMedia
1	0	MMC/SD
1	1	Memory Stick



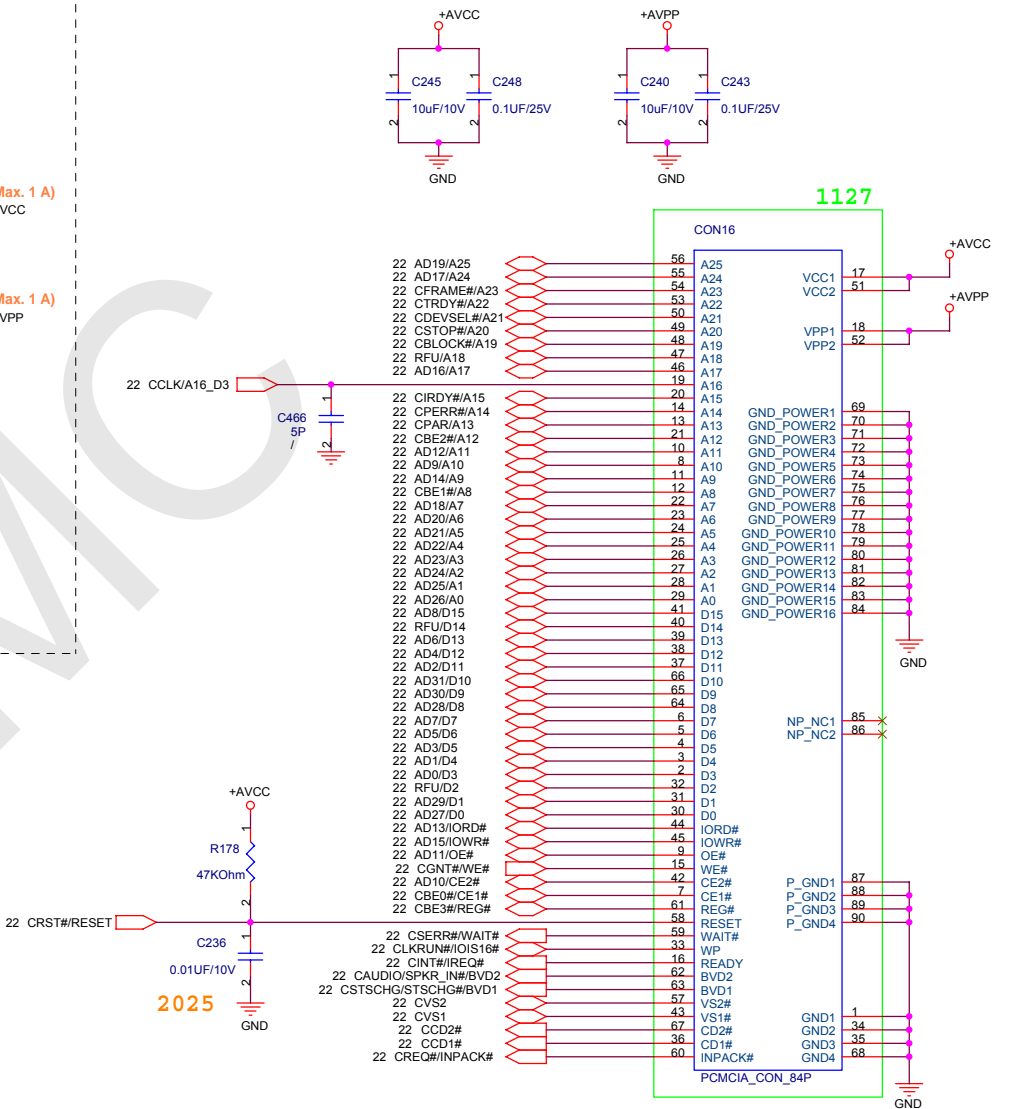
REXT/VREF/FILO
To implement as close as possible to R5C593
To apply shield GND



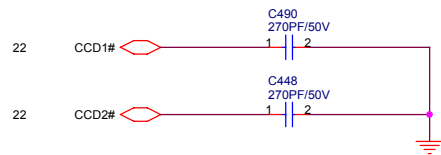
CB POWER SWITCH



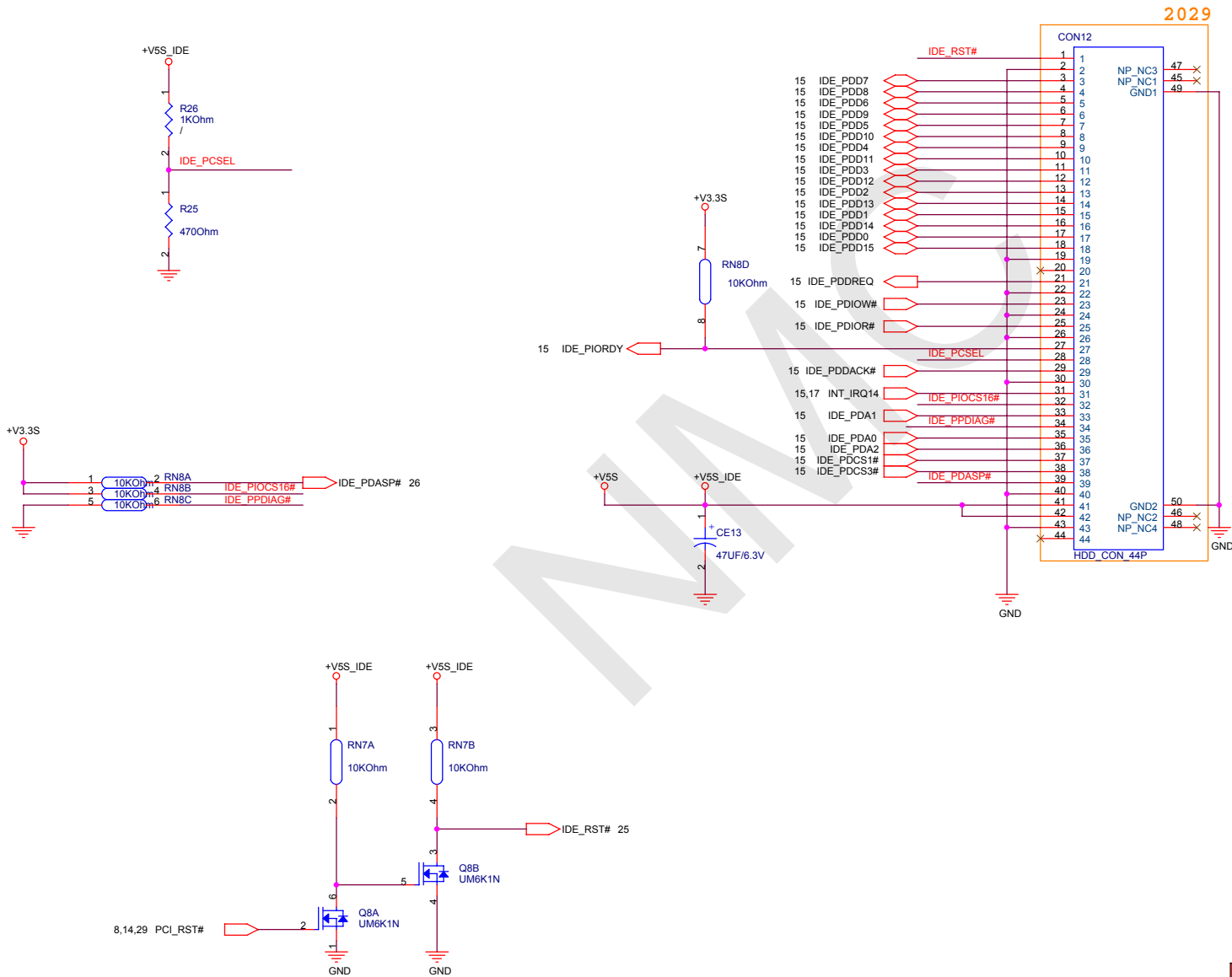
CB SOCKET



CB DE-BOUNCE

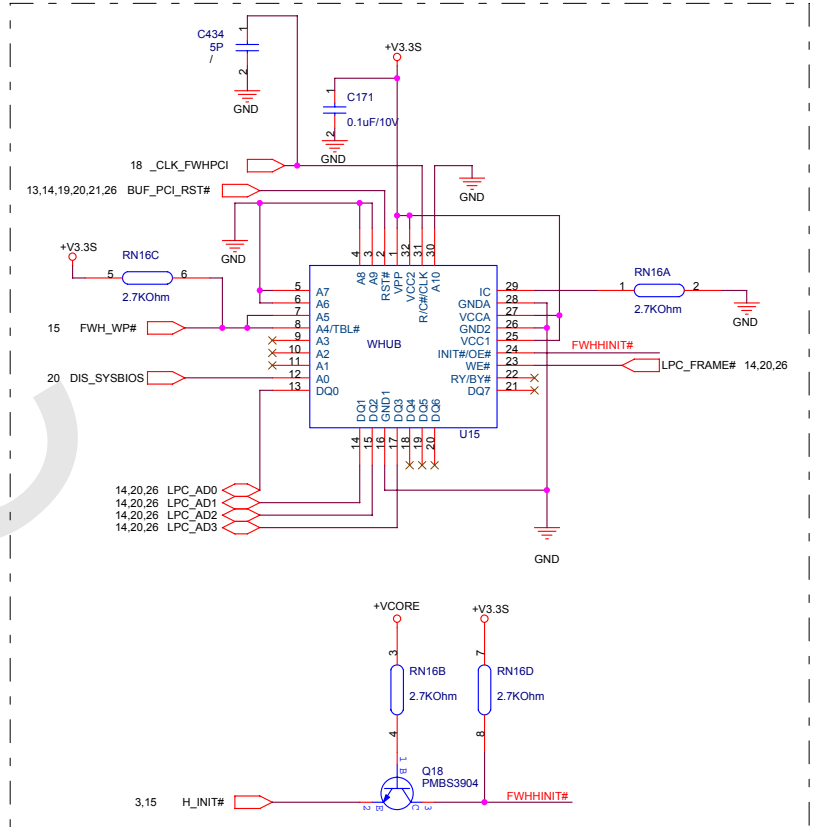
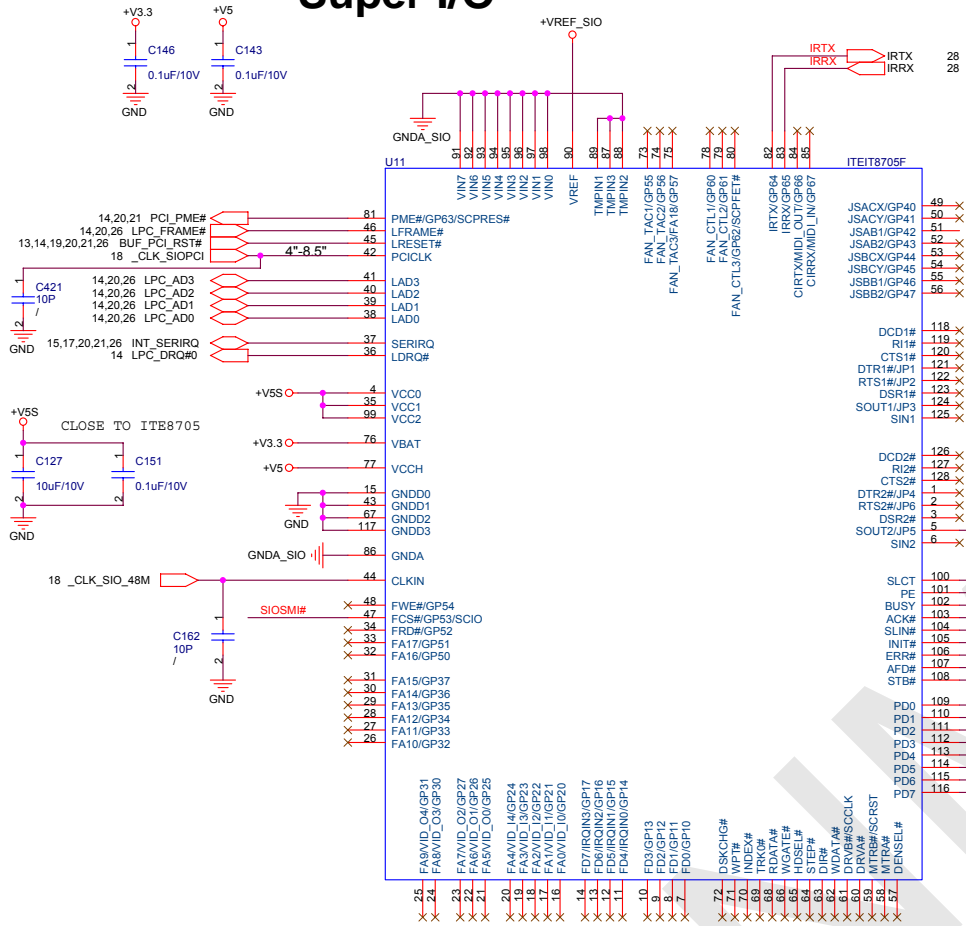


<Variant Name>

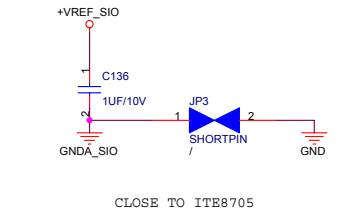
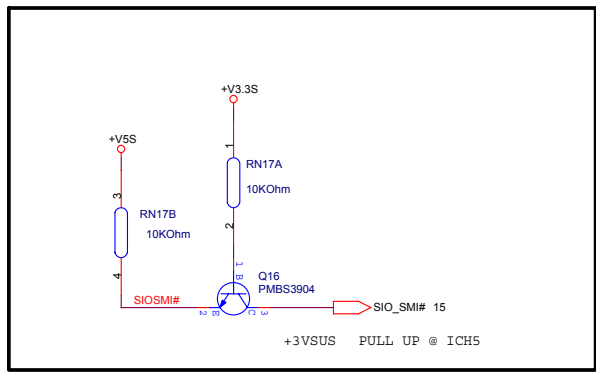


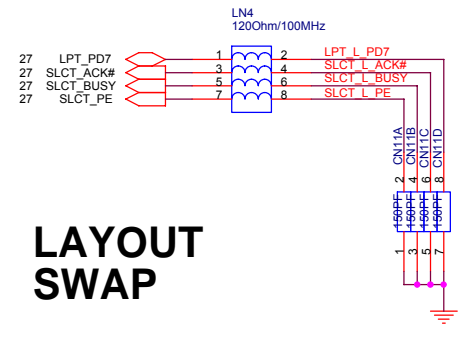
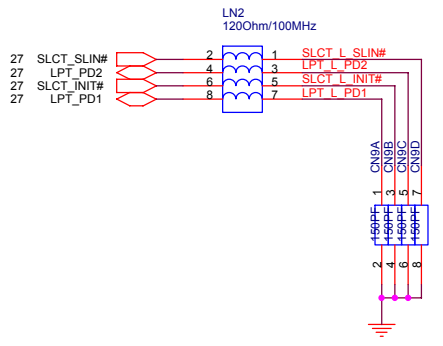
2029

Super I/O 2208

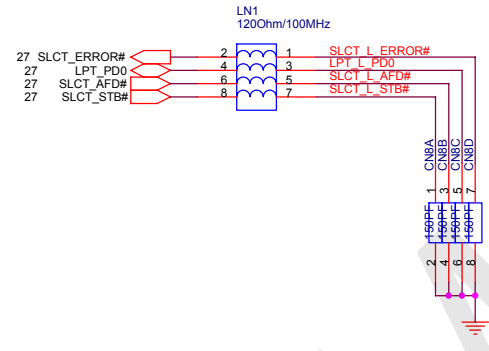
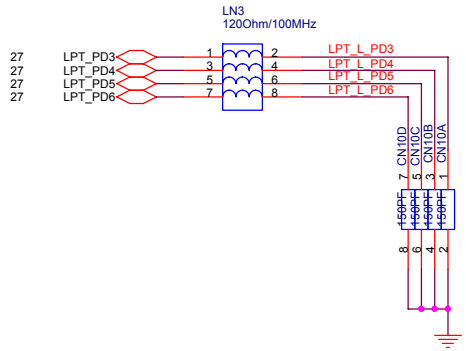


**P24: Add FWH ROM P/N:
05-001017122**

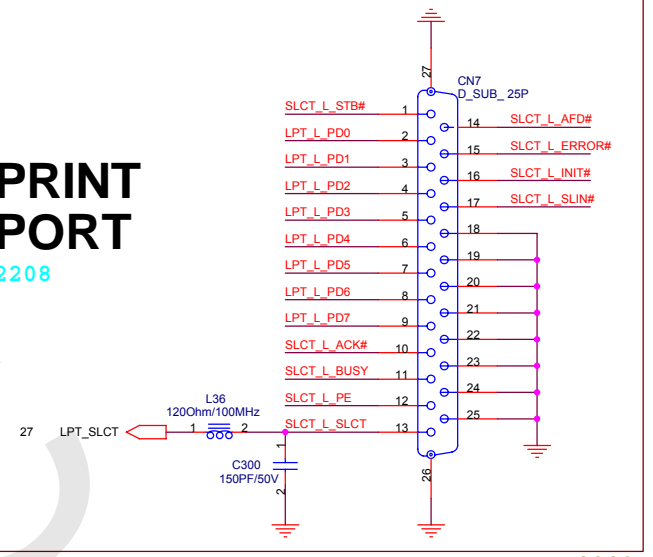




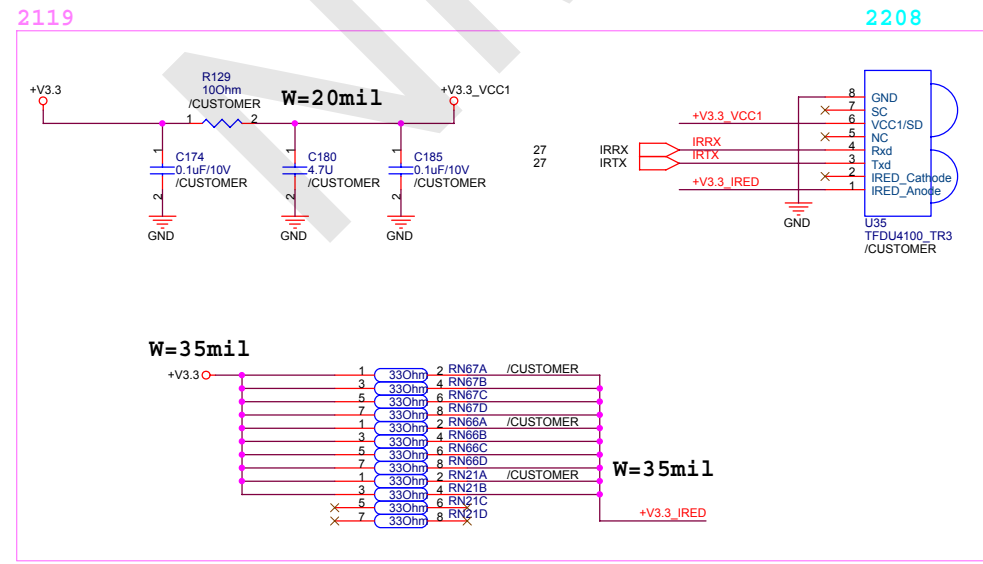
LAYOUT SWAP



PRINT PORT
2208



2309
2222 2408

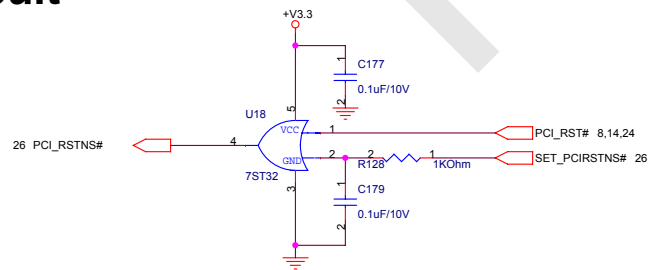


PCMCIA DEBUG Card

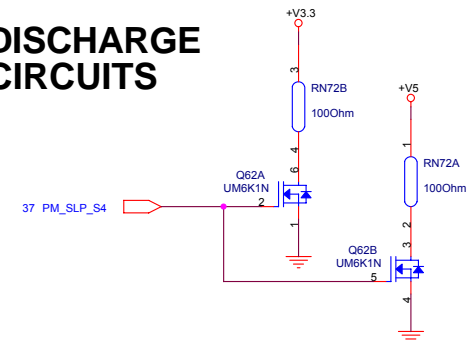


1105

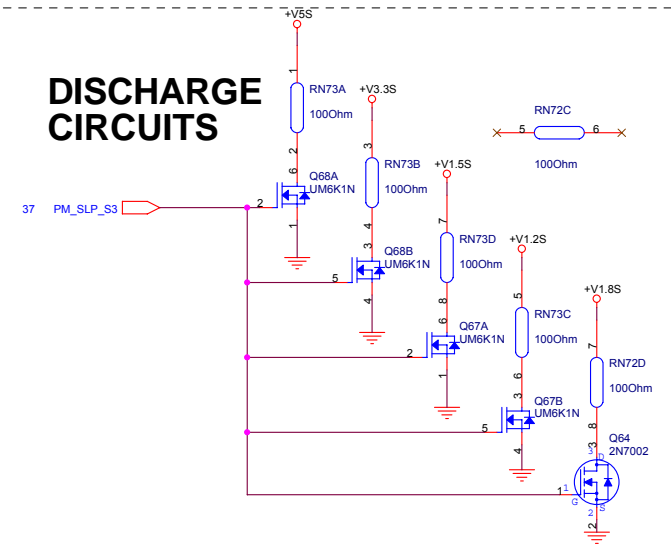
PCI_RSTNS# Gen Circuit

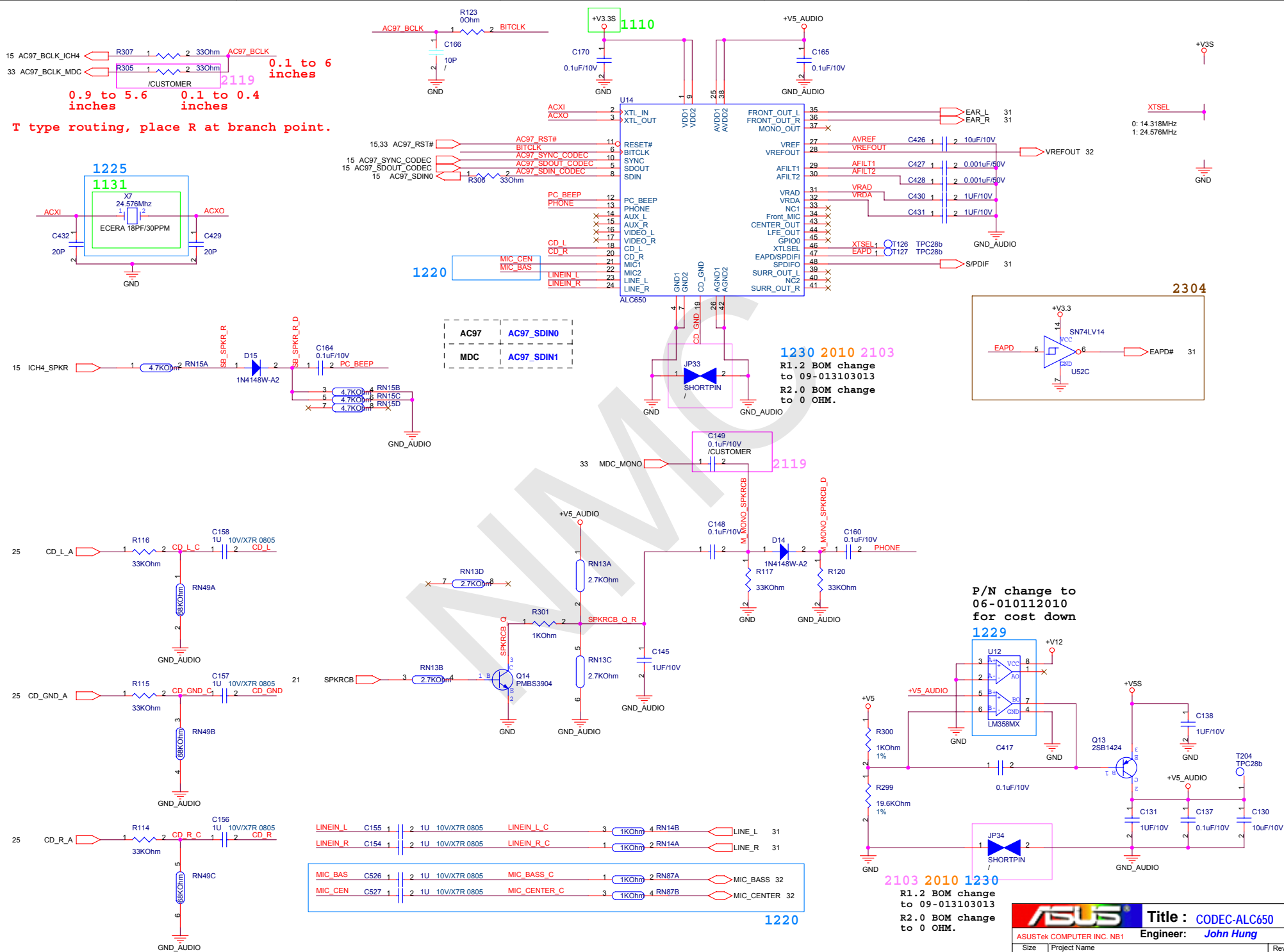


DISCHARGE CIRCUITS



DISCHARGE CIRCUITS



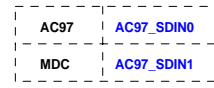
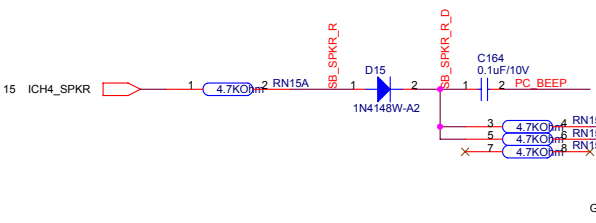
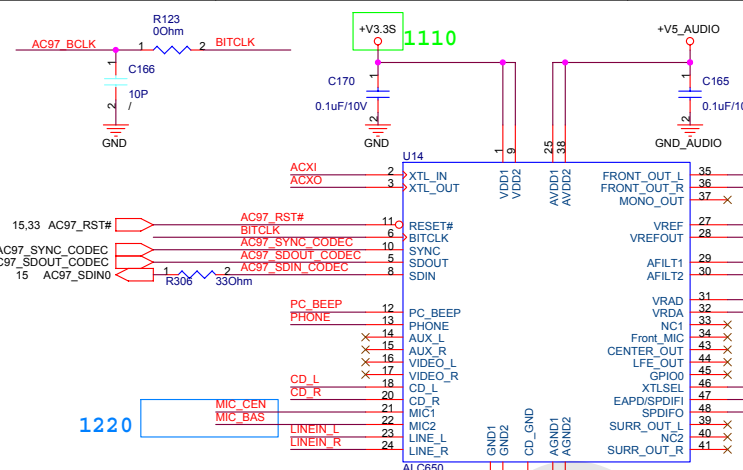
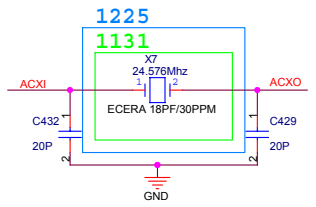


15 AC97_BCLK_ICH4
33 AC97_BCLK_MDC

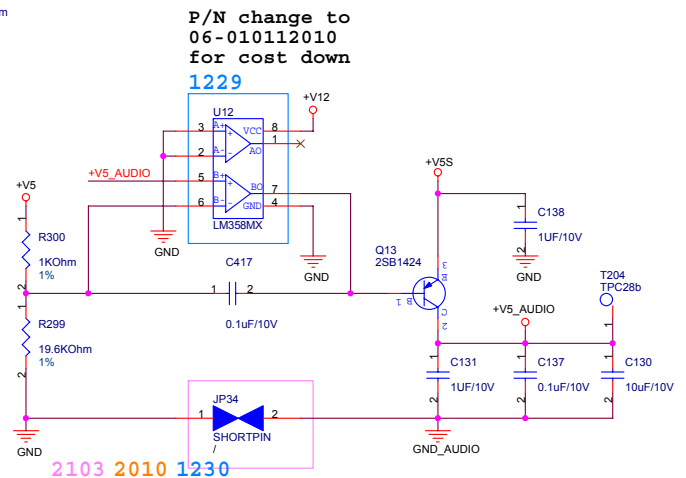
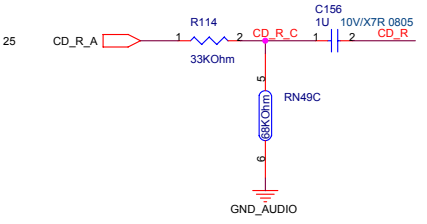
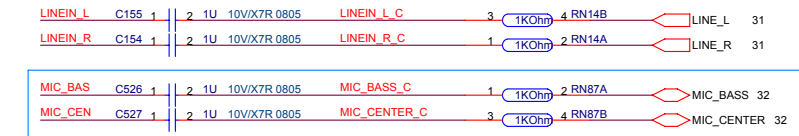
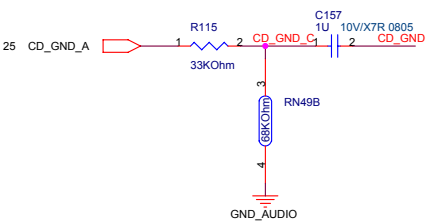
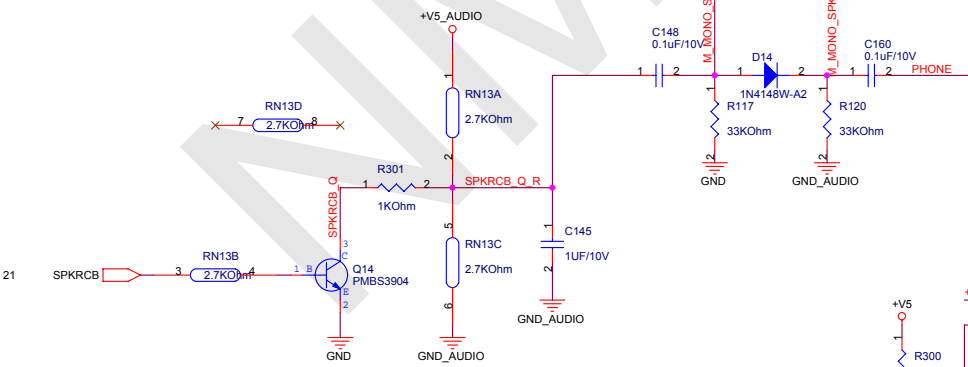
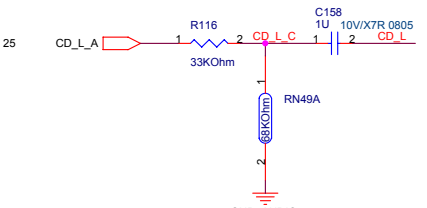
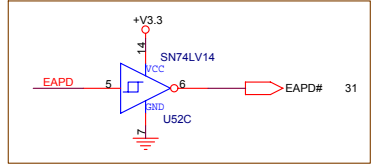
R307 1 2 330hm AC97_BCLK
R305 1 2 330hm /CUSTOMER

0.1 to 6 inches
0.9 to 5.6 inches
0.1 to 0.4 inches

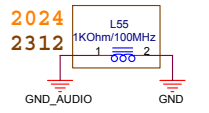
T type routing, place R at branch point.



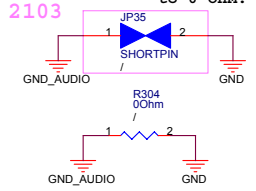
1230 2010 2103
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.



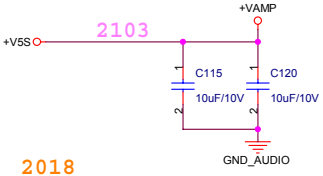
2103 2010 1230
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.



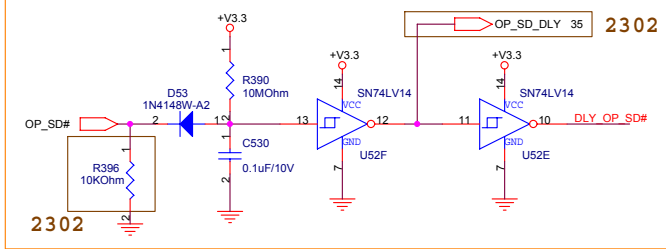
1230
2010
2103



$f(\text{highpass}) = \frac{1}{2 * 3.14 * R * C} = 73$
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V (11-041210721), but 100uF is too big for A3N, so change to 47uF.



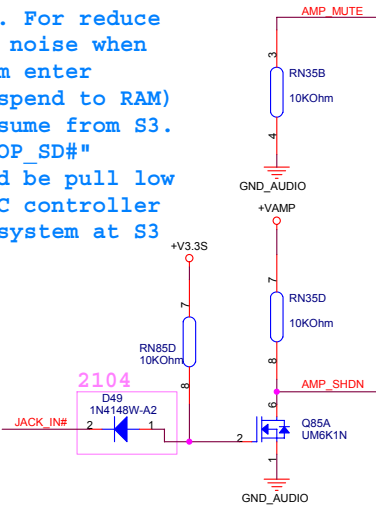
2018



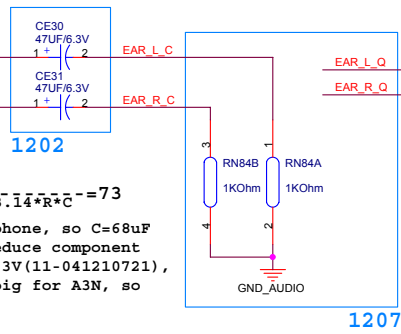
2302

R:1.2. For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.

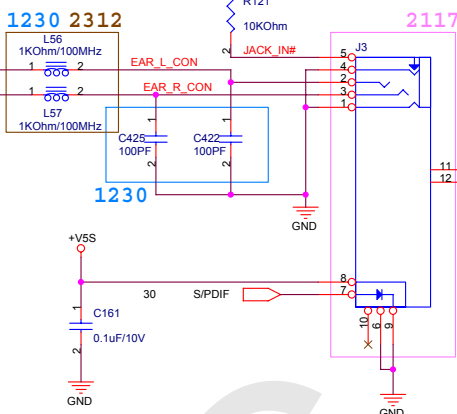
1207



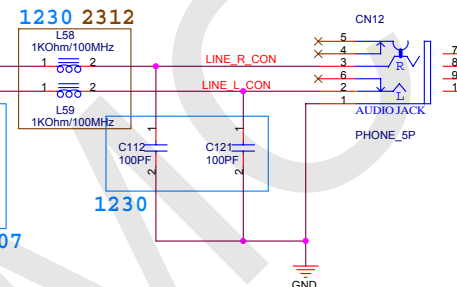
R:2.1 Use "OP_SD#", speaker will have "POP" noise after logo display when turn on system. Don't use "OP_SD#".



1207



1230

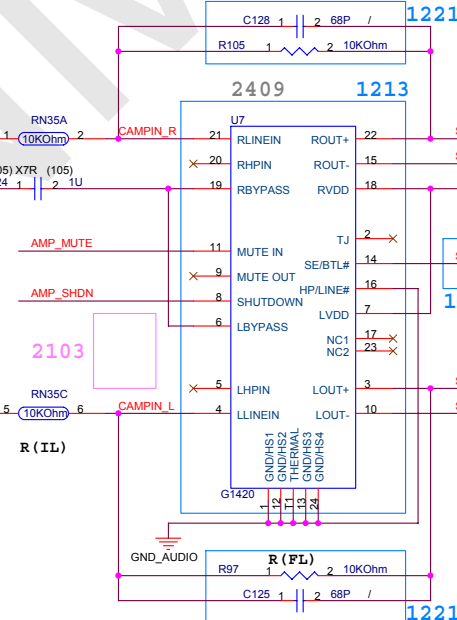
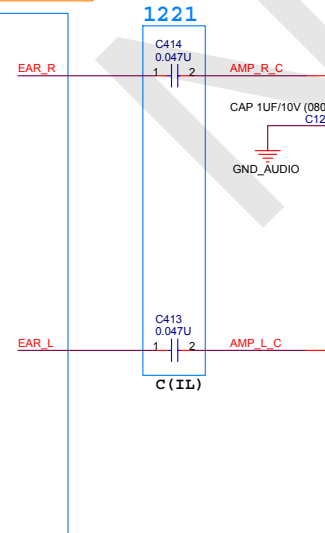


1230

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

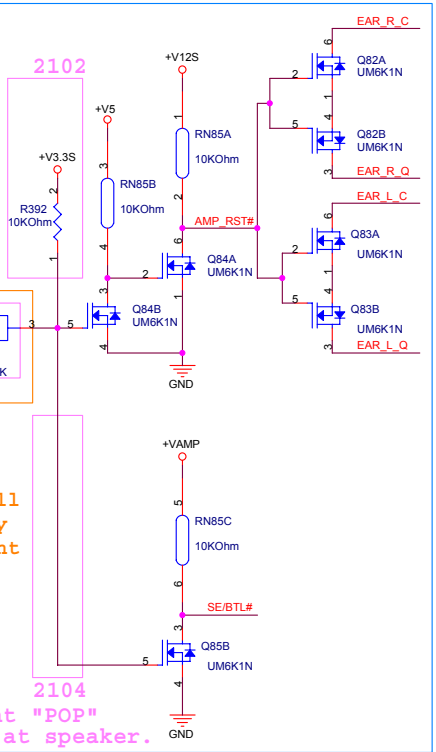
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.

Prevent "POP" noise at speaker.

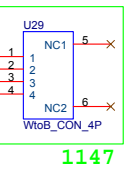


$f(\text{highpass}) = \frac{1}{2 * 3.14 * C(IL) * R(IL)} = 500$
 $f(\text{lowpass}) = \frac{1}{2 * 3.14 * C(150P) * R(10K)} = 106K$

BTL Gain=-2
R(FL) 10K
R(IL) 10K
=V
Speaker W=V*V
=2*2
=4ohm
=1W
Can use 1W(4ohm) speaker



1207

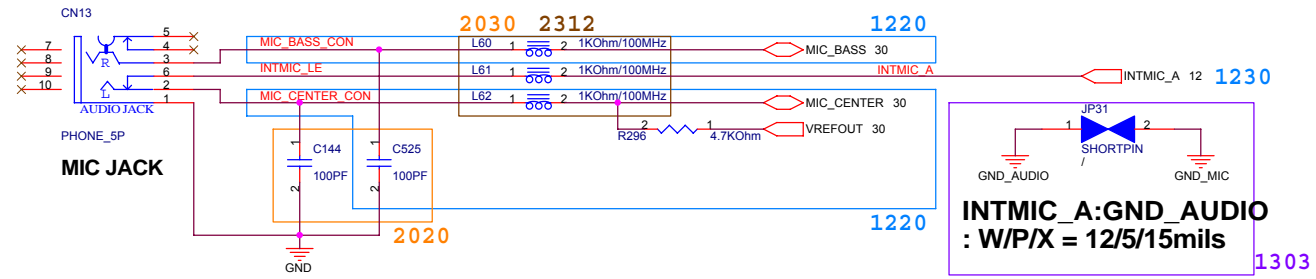


1147

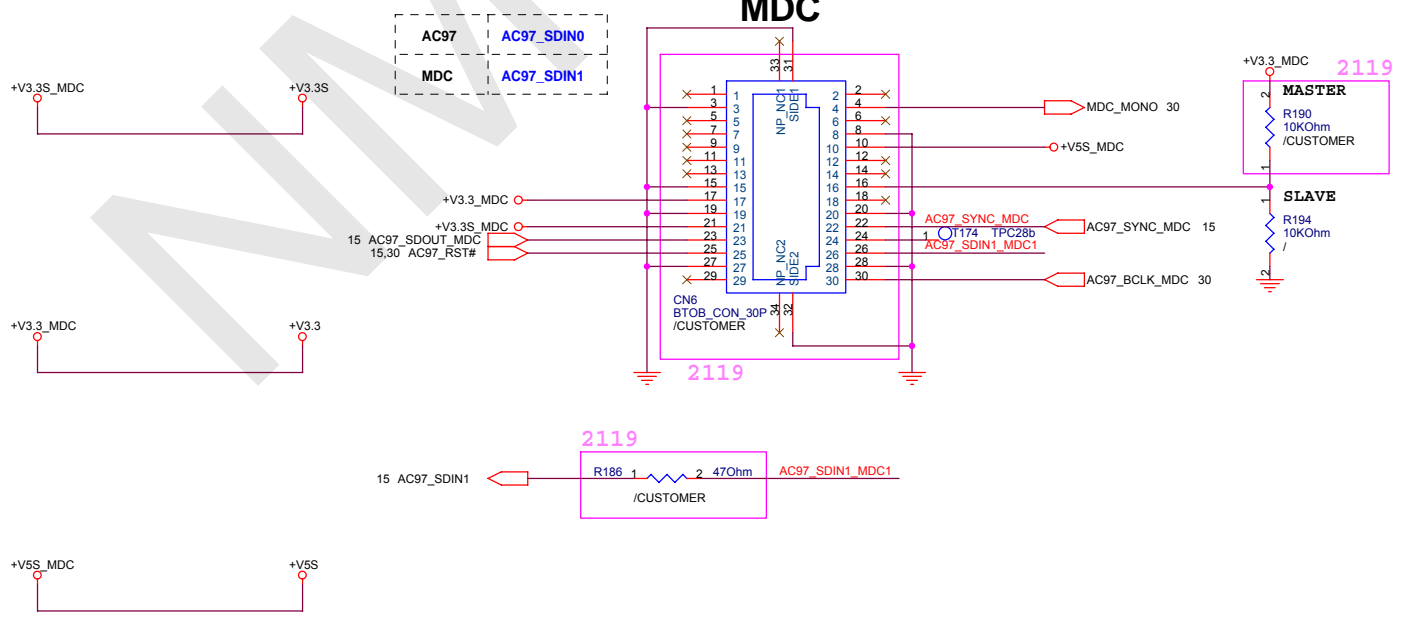
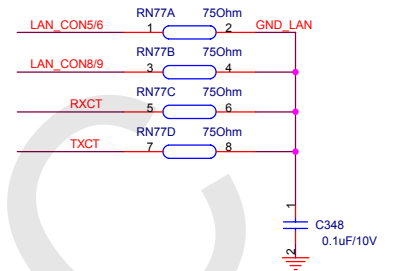
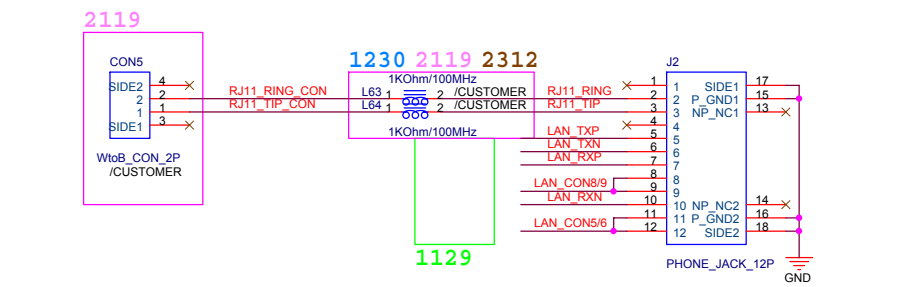
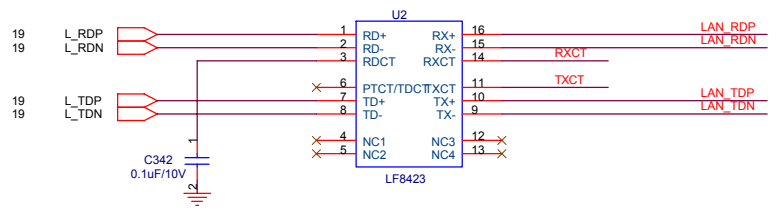
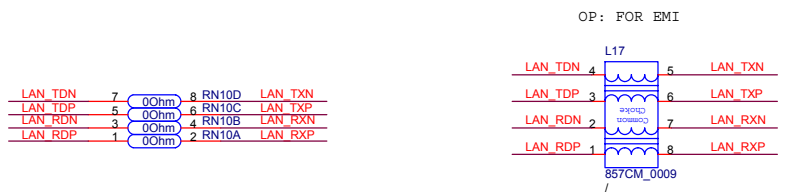
1220

MIC OP CIRCUIT

MIC JACK



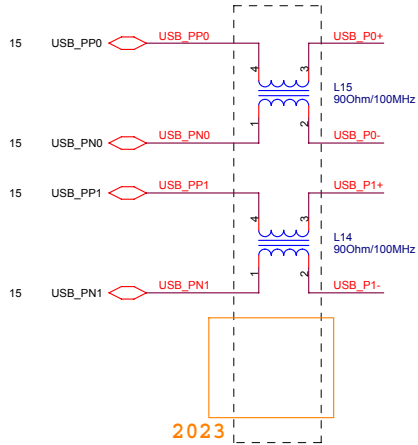
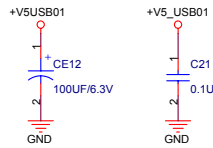
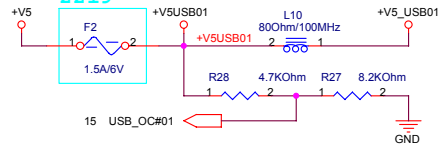
ASUS		Title :	
ASUSTek COMPUTER INC. NB1		Engineer: <i>John Hung</i>	
Size	Project Name		Rev
Custom	A3N/A3L		2.4
Date: Monday, November 15, 2004		Sheet	32 of 55



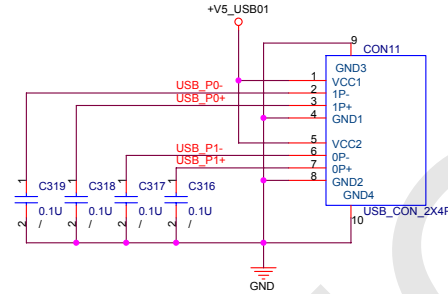
MDC		ASUS®		Title :	
ASUSTek COMPUTER INC. NB1		Engineer: John Hung			
Size	Project Name	Rev			
Custom	A3N/A3L	2.4			
Date: Monday, November 15, 2004	Sheet 33 of 55				

VPLP R:2.2 use 07-014110900 (2nd source is 07-014110201)

2219



2023
R & L Co-Lay



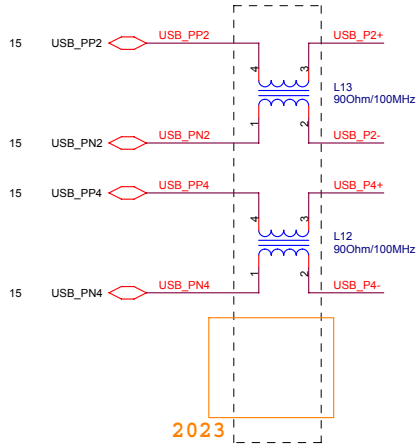
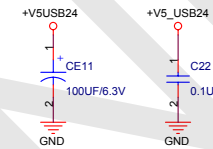
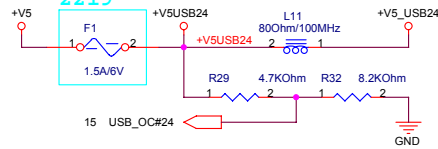
USB PORT 0 & PORT 1

1128

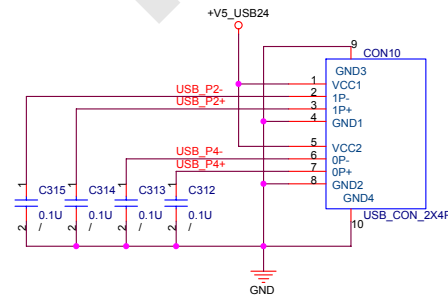
USB PORT 3 for CAMERA
Change to page 12

VPLP R:2.2 use 07-014110900 (2nd source is 07-014110201)

2219



2023
R & L Co-Lay



USB PORT 2 & PORT 4

1128

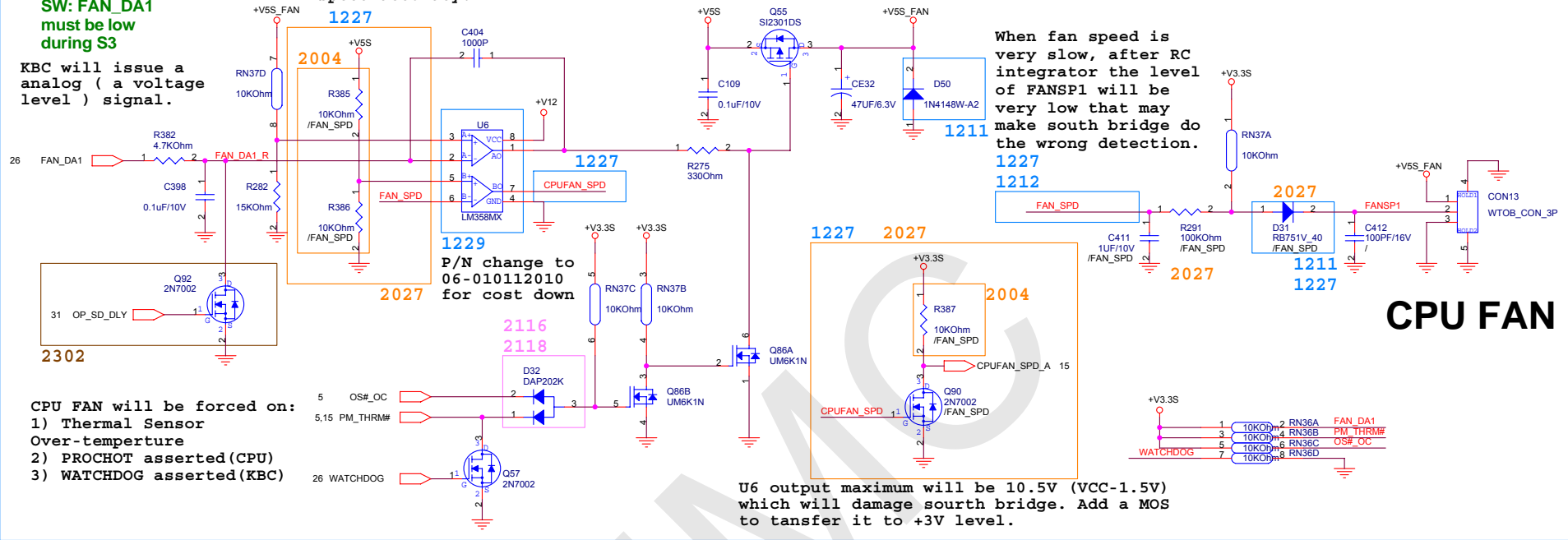
USB PORT 5 for WLAN
Change to page 12

Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.



When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN

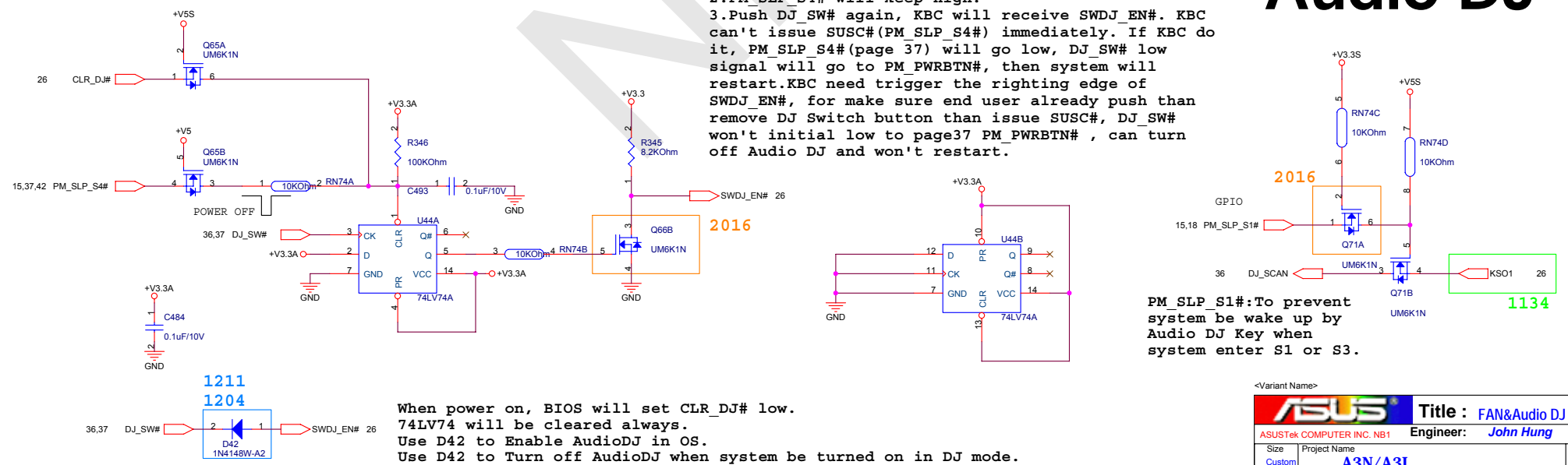
- CPU FAN will be forced on:
- 1) Thermal Sensor Over-temperature
 - 2) PROCHOT asserted(CPU)
 - 3) WATCHDOG asserted(KBC)

U6 output maximum will be 10.5V (VCC-1.5V) which will damage south bridge. Add a MOS to transfer it to +3V level.

SWDJ_EN# function :

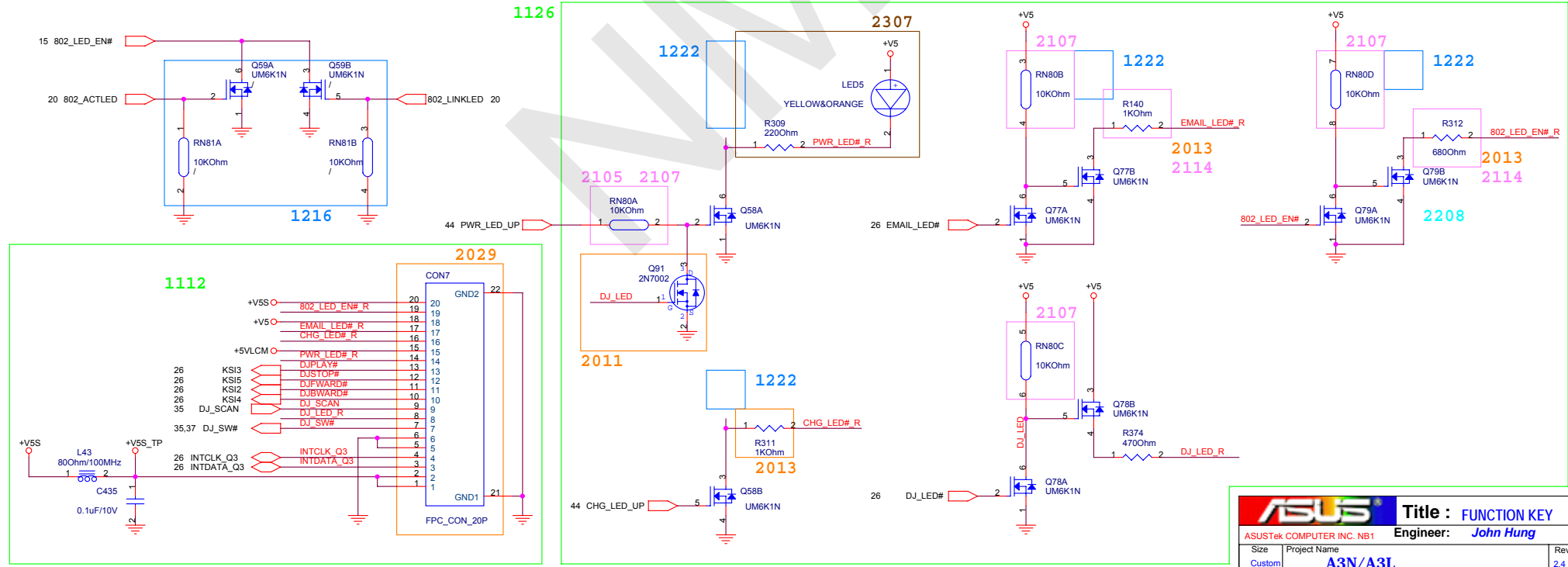
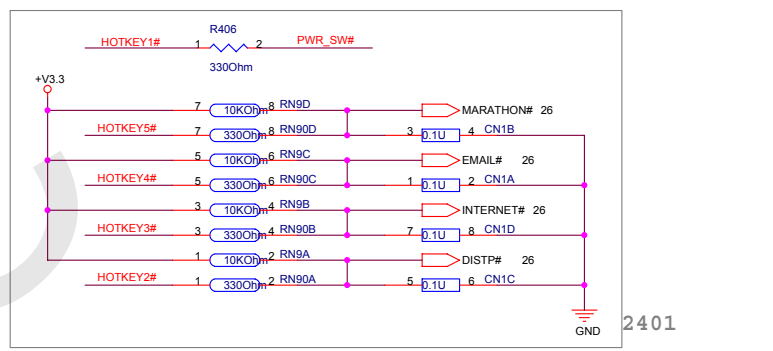
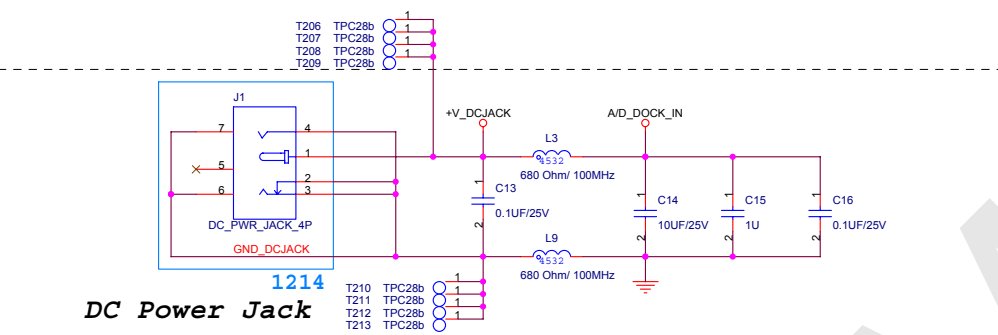
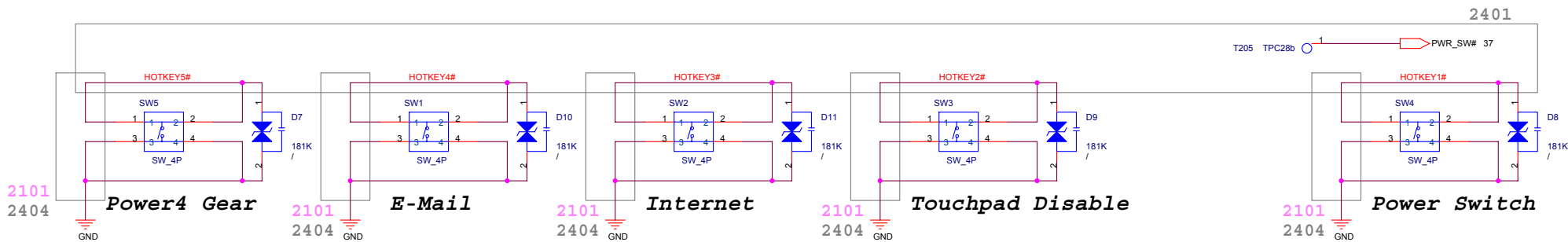
1. Push DJ_SW#, turn on Audio DJ.
2. PM_SLP_S4# will keep high.
3. Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart. KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN#, can turn off Audio DJ and won't restart.

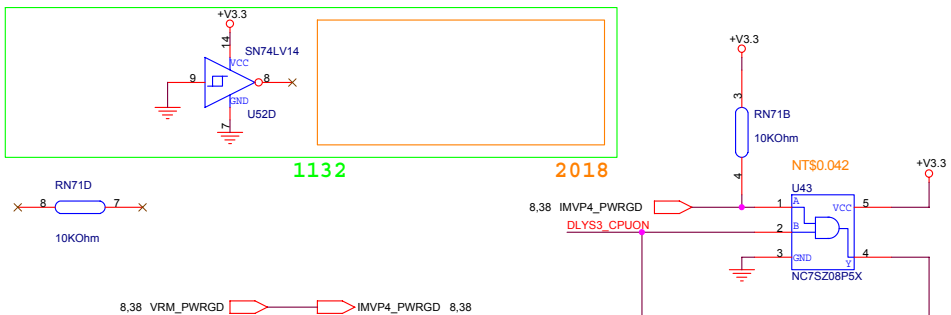
Audio DJ



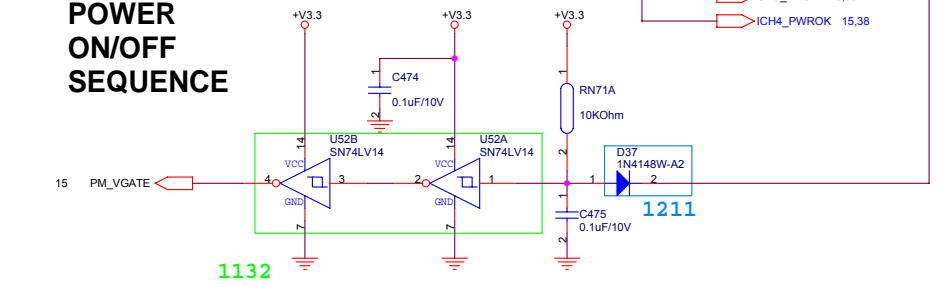
PM_SLP_S1#: To prevent system be wake up by Audio DJ Key when system enter S1 or S3.

When power on, BIOS will set CLR_DJ# low. 74LV74 will be cleared always. Use D42 to Enable AudioDJ in OS. Use D42 to Turn off AudioDJ when system be turned on in DJ mode.

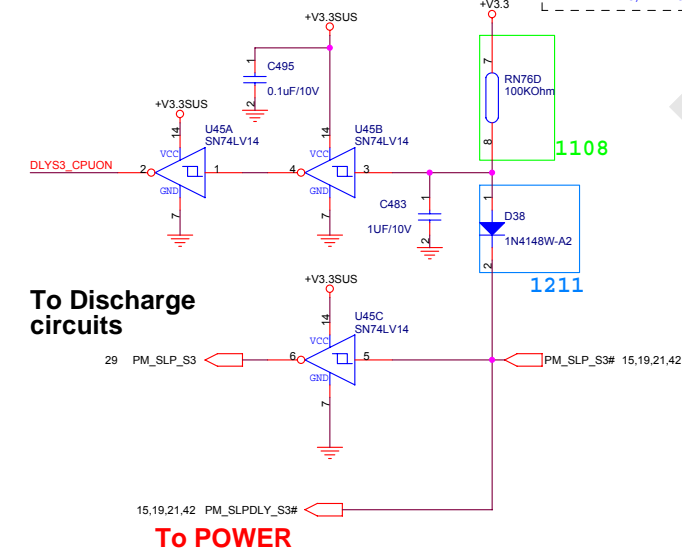




POWER ON/OFF SEQUENCE

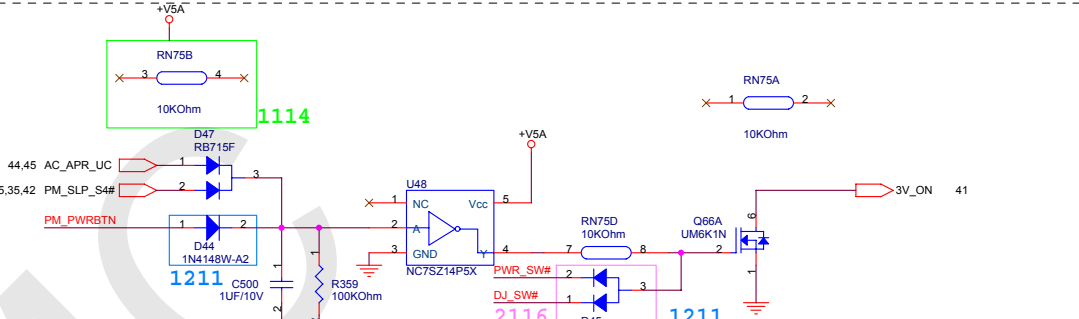
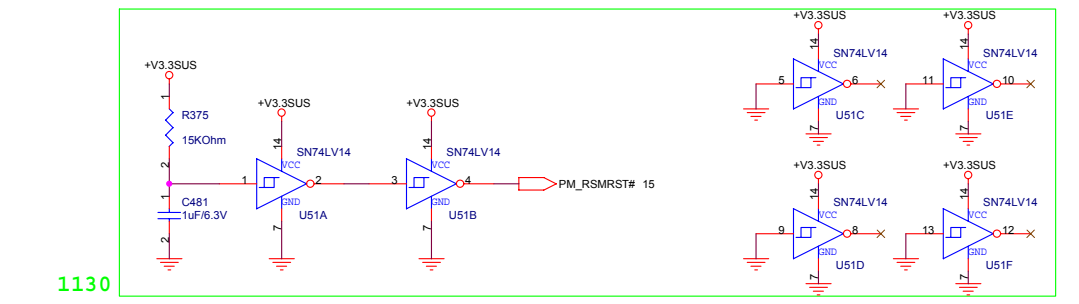


System Power Sequence
 +VCCRTC -> RTCRST# -> V5REFSUS -> 3.3/1.8VSUS ->
 RSMRST# -> SLP_S4# -> SLP_S3# -> VCCLAN -> LANPWROK
 -> V5REF -> VCC -> VCORE -> PWROK -> VGATE
 SUSSTAT# -> PCIRST#
 CPU : +VCORE, +VCCP, +V1.8S
 NB : +V1.2S, +V1.5S, +2.5V, +VCCP
 SB : +V1.5SUS, +V3.3SUS, +VCCP, +V1.5S, +V3.3S
 DDR : +V2.5, +V1.25, +V1.25S

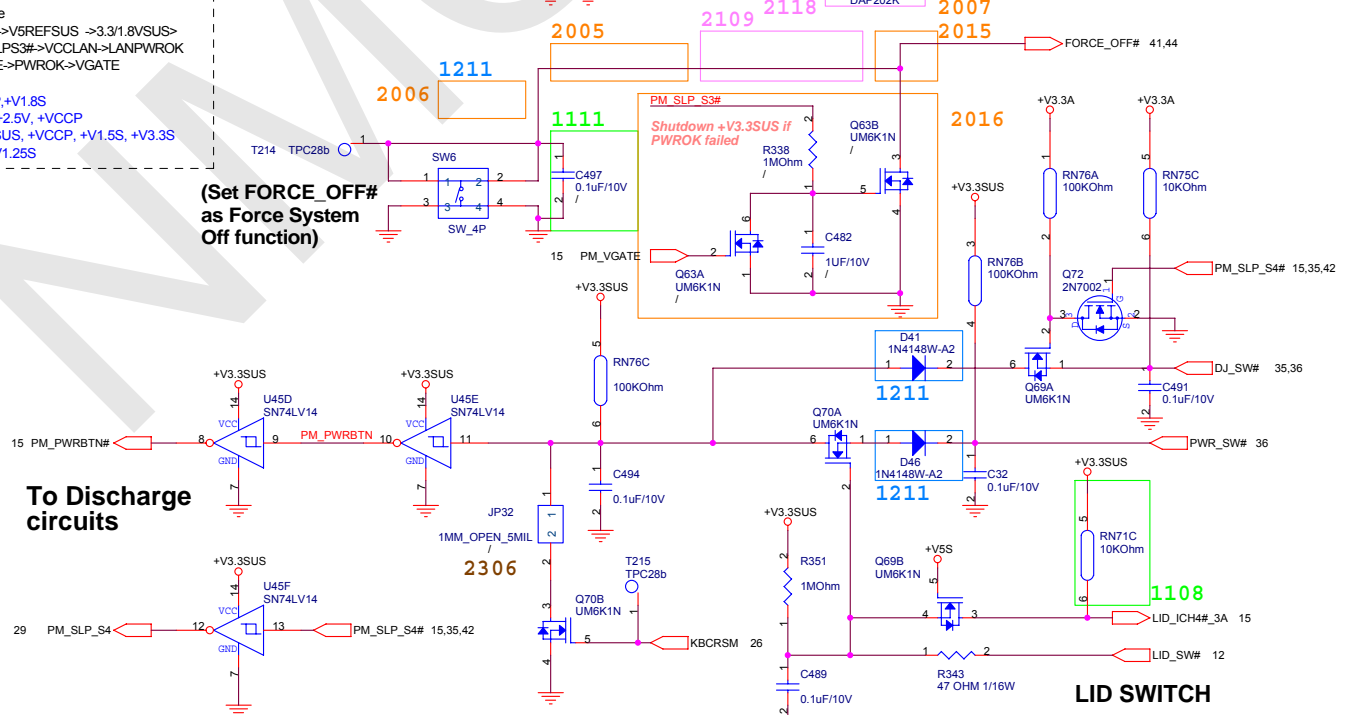


To Discharge circuits

To POWER



(Set FORCE_OFF# as Force System Off function)



To Discharge circuits

LID SWITCH

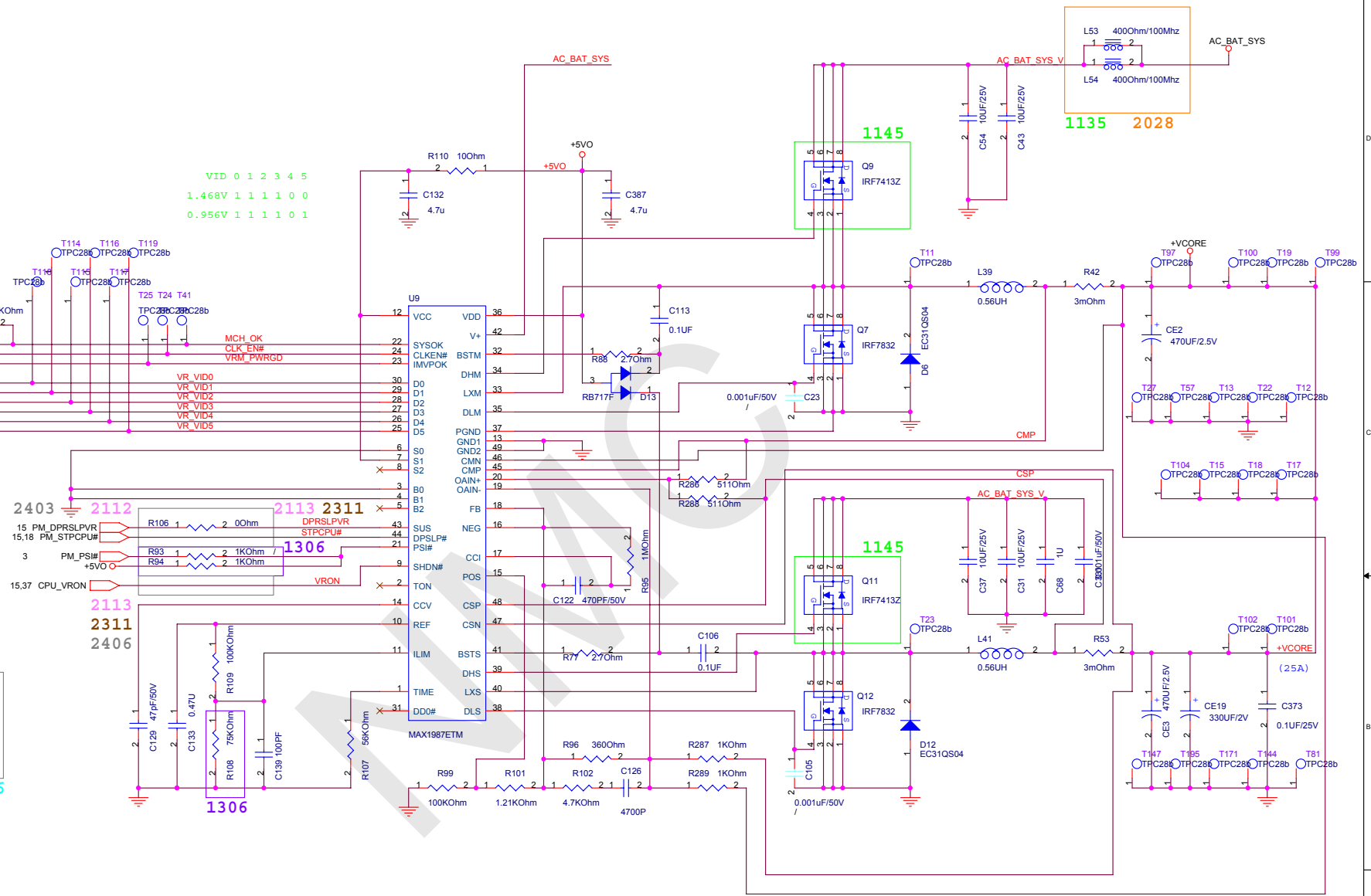
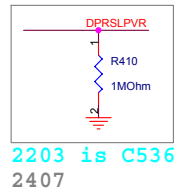
KBCRSM will issue low when system on & BIOS work normally. Issue high when system on & BIOS don't work, then system will off after 4 seconds to protect system. Issue a high pulse to wake up system from S3 state by push any key.

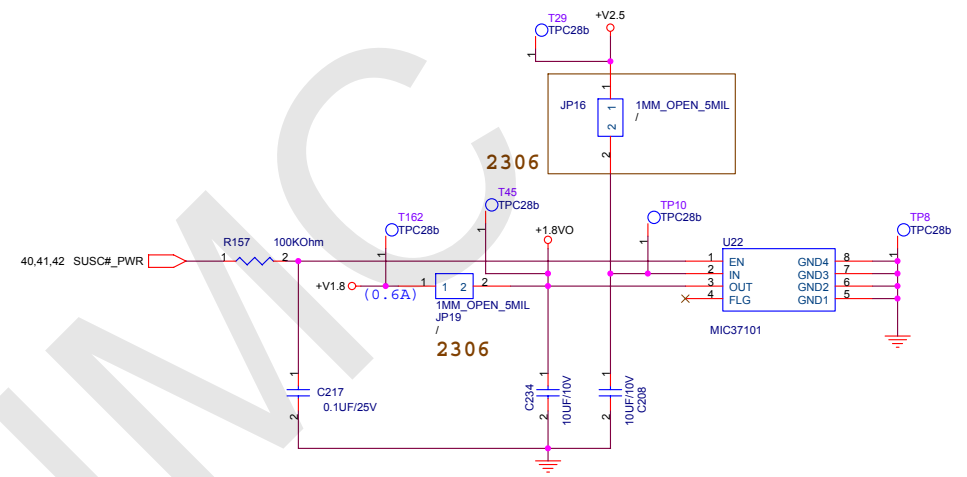
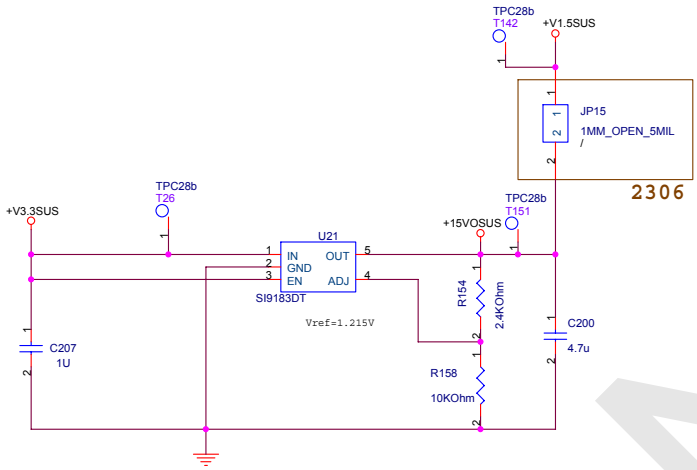
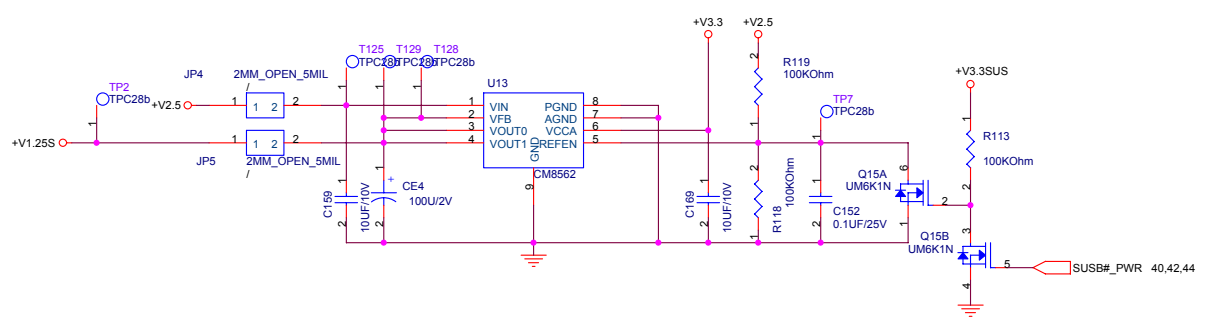
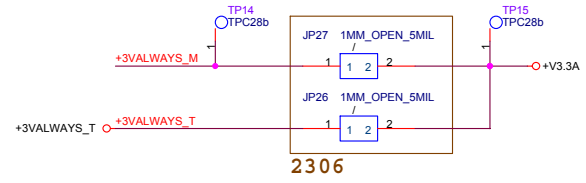
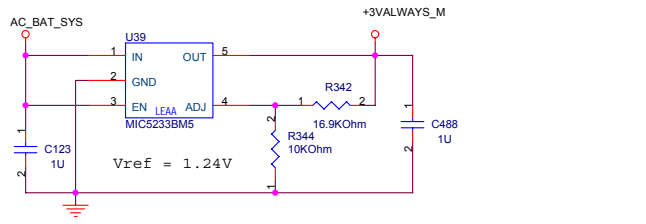
VID 0 1 2 3 4 5
 1.468V 1 1 1 1 0 0
 0.956V 1 1 1 1 0 1

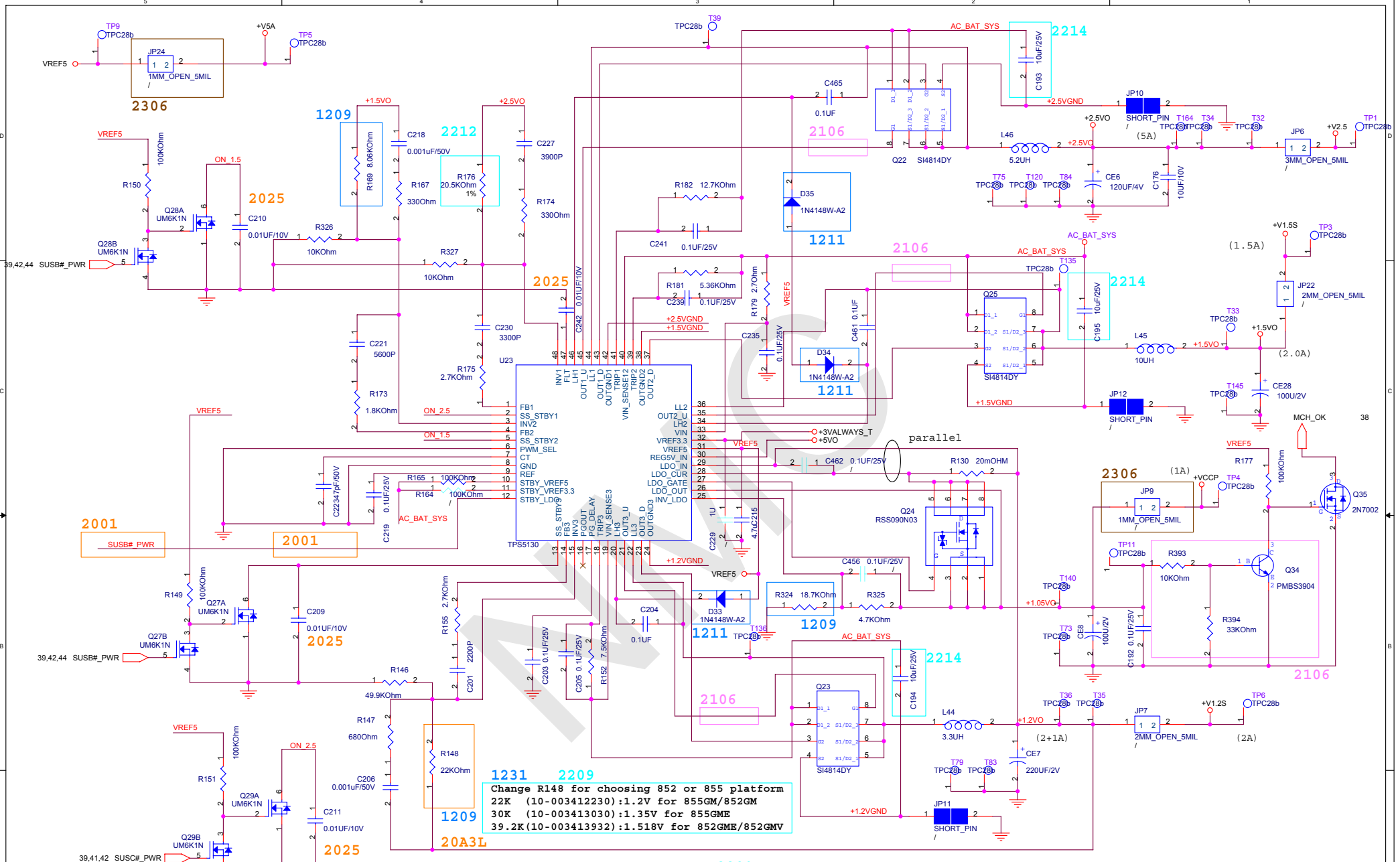
2001

40	MCH_OK
18	CLK_EN#
8,37	VRM_PWRGD
3	VR_VID0
3	VR_VID1
3	VR_VID2
3	VR_VID3
3	VR_VID4
3	VR_VID5

T121	TPC28b	STPCPU#
T123	TPC28b	DPRSPLV#
T122	TPC28b	VRON
T217	TPC28b	PM_PSI#





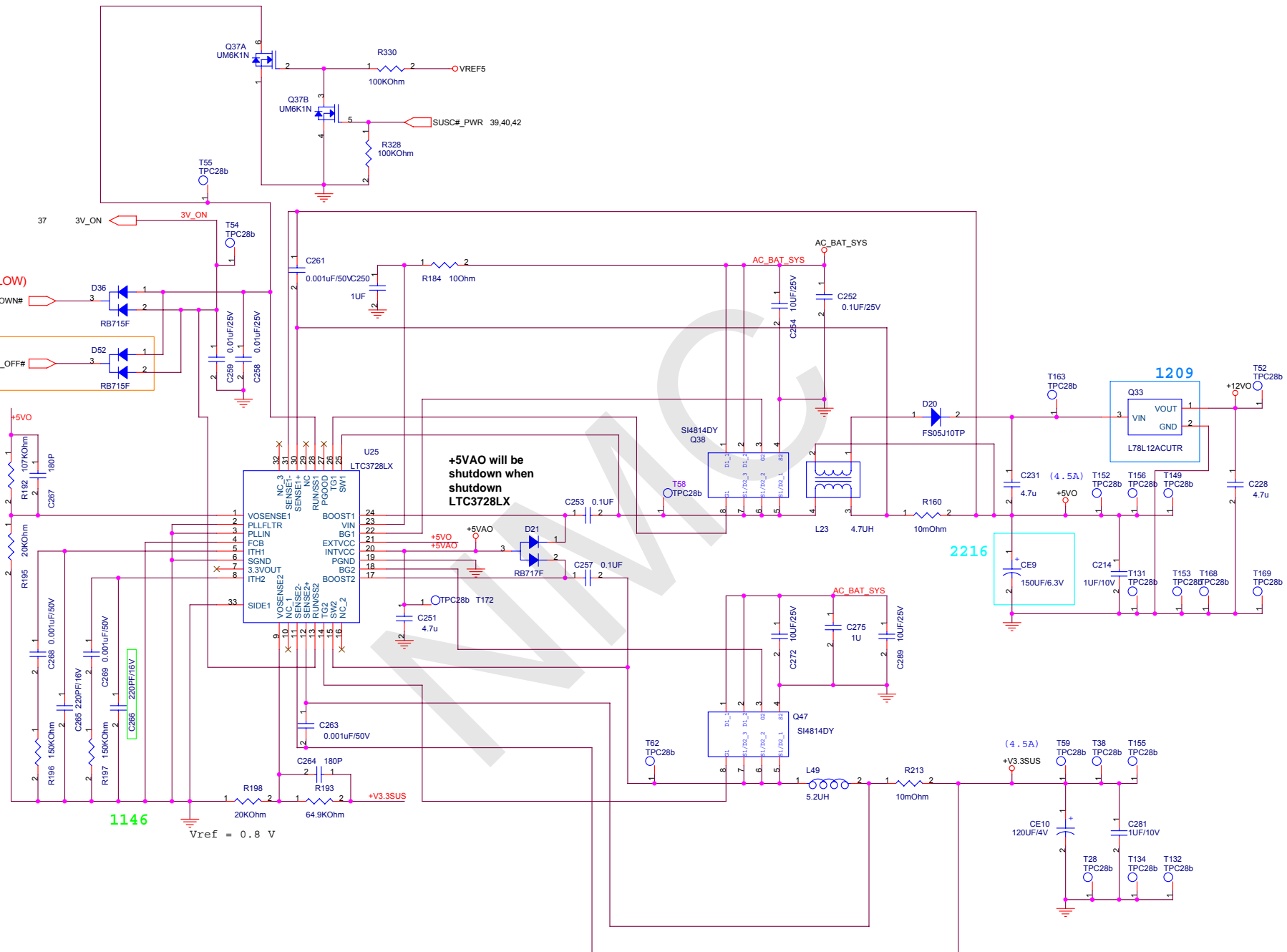


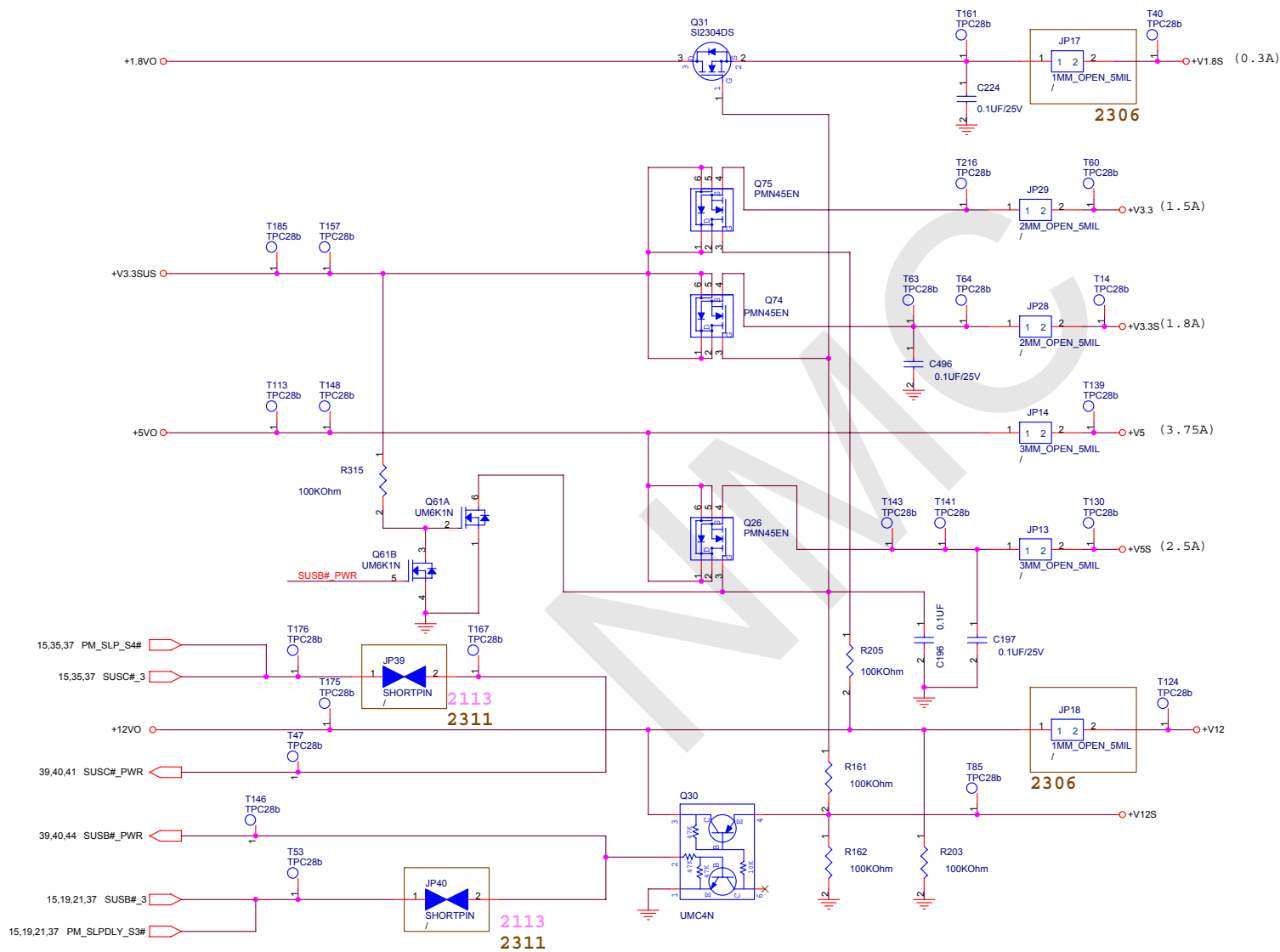
CPU

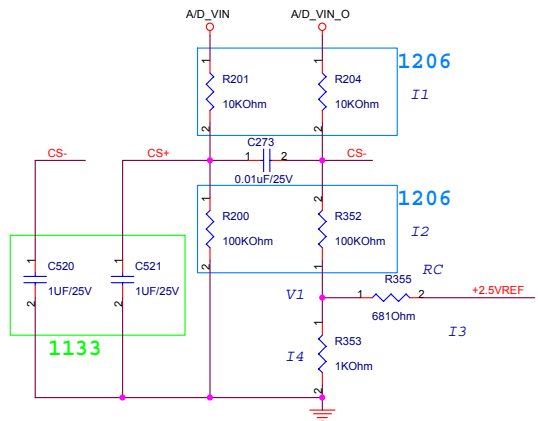
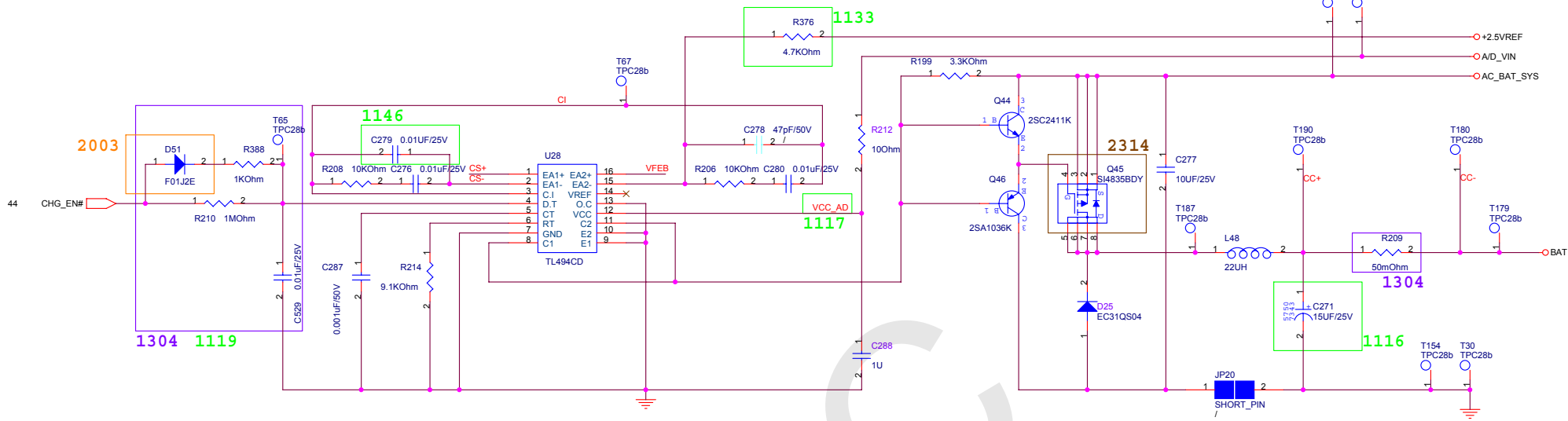
	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4			Pin 1,2

NB
 VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB:
 855GM/852GM: 1.2V
 855GME: 1.35V
 852GME/852GMV: 1.5V

(BAT LOW)
45 SHUT_DOWN#
2005
37.44 FORCE_OFF#

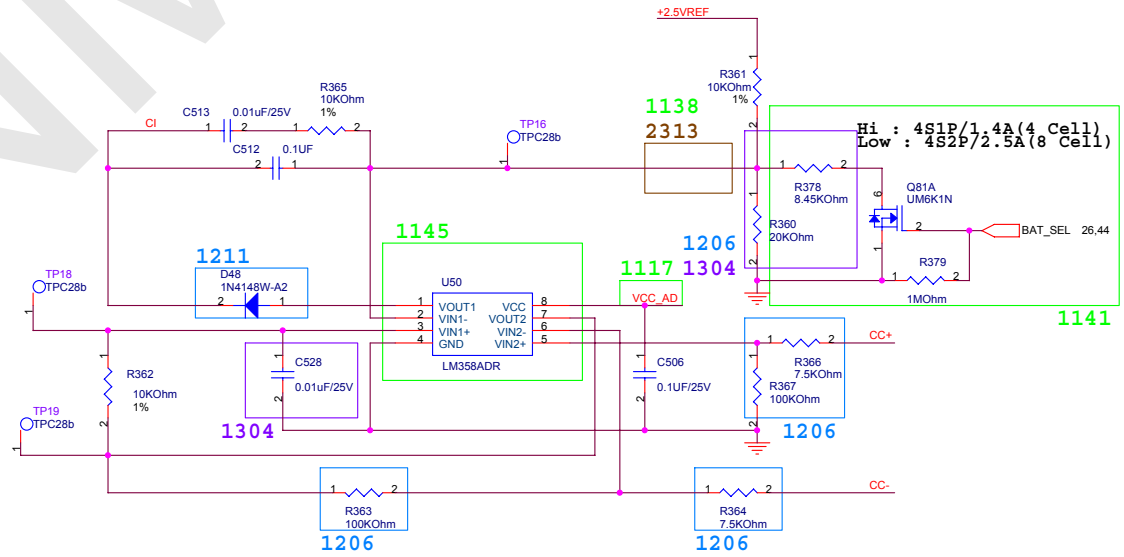
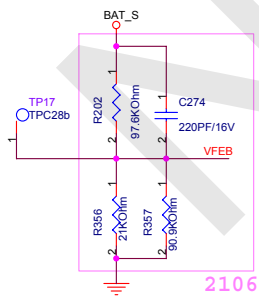


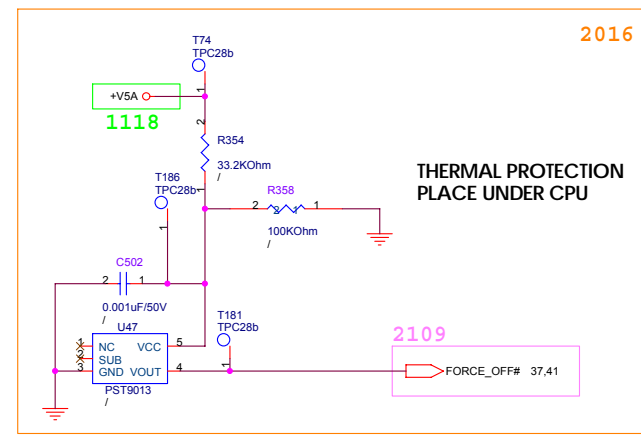
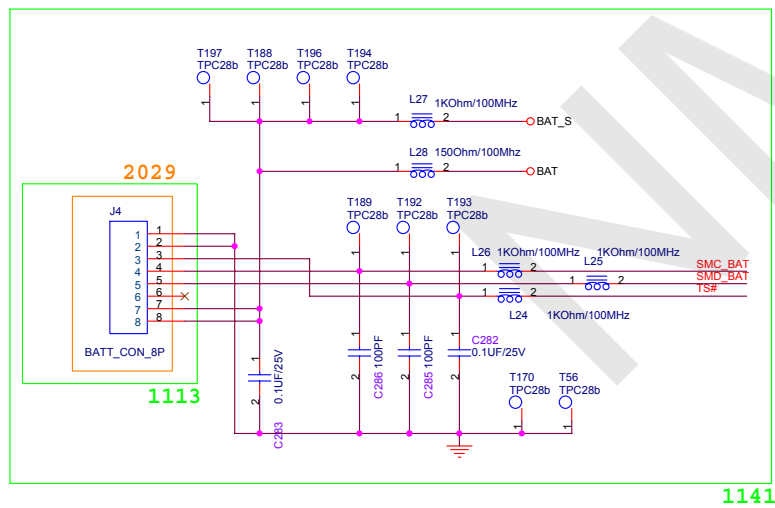
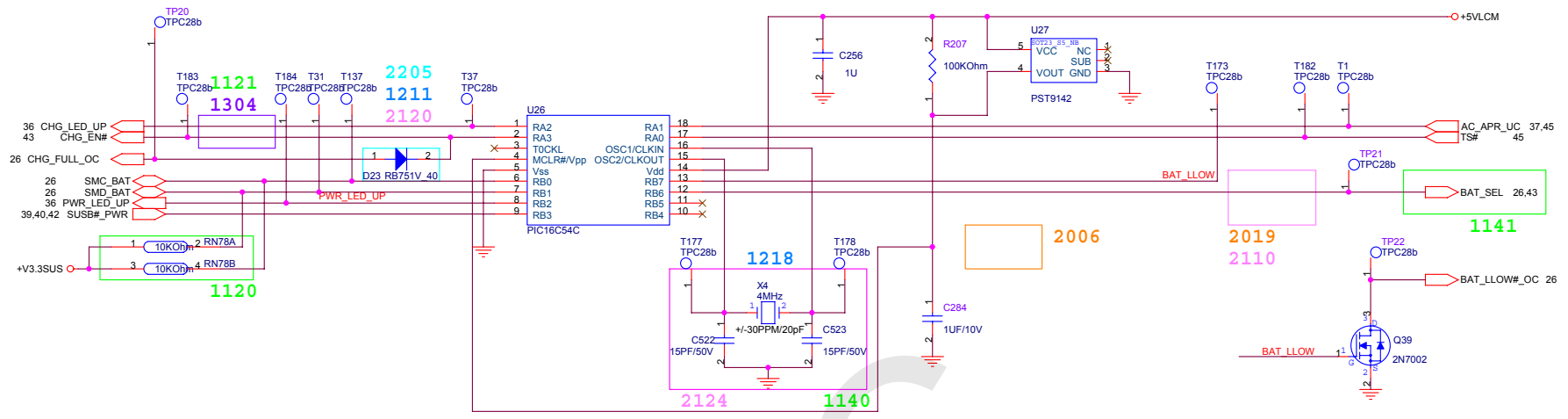


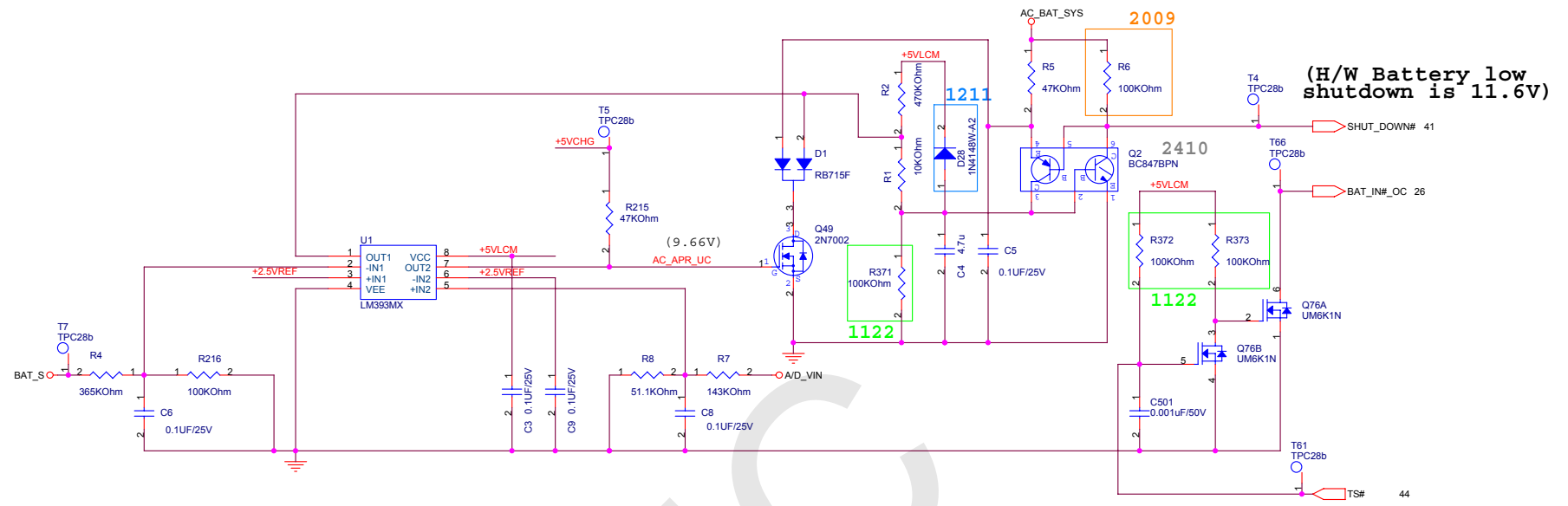


Current sharing = 3.1A

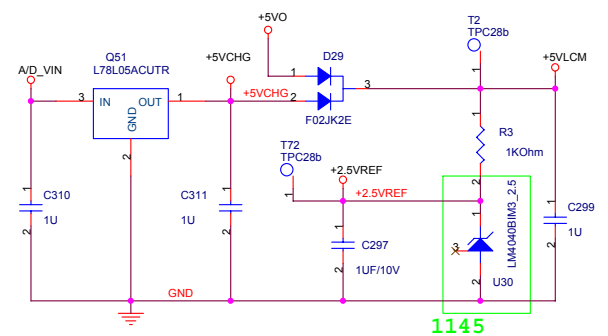
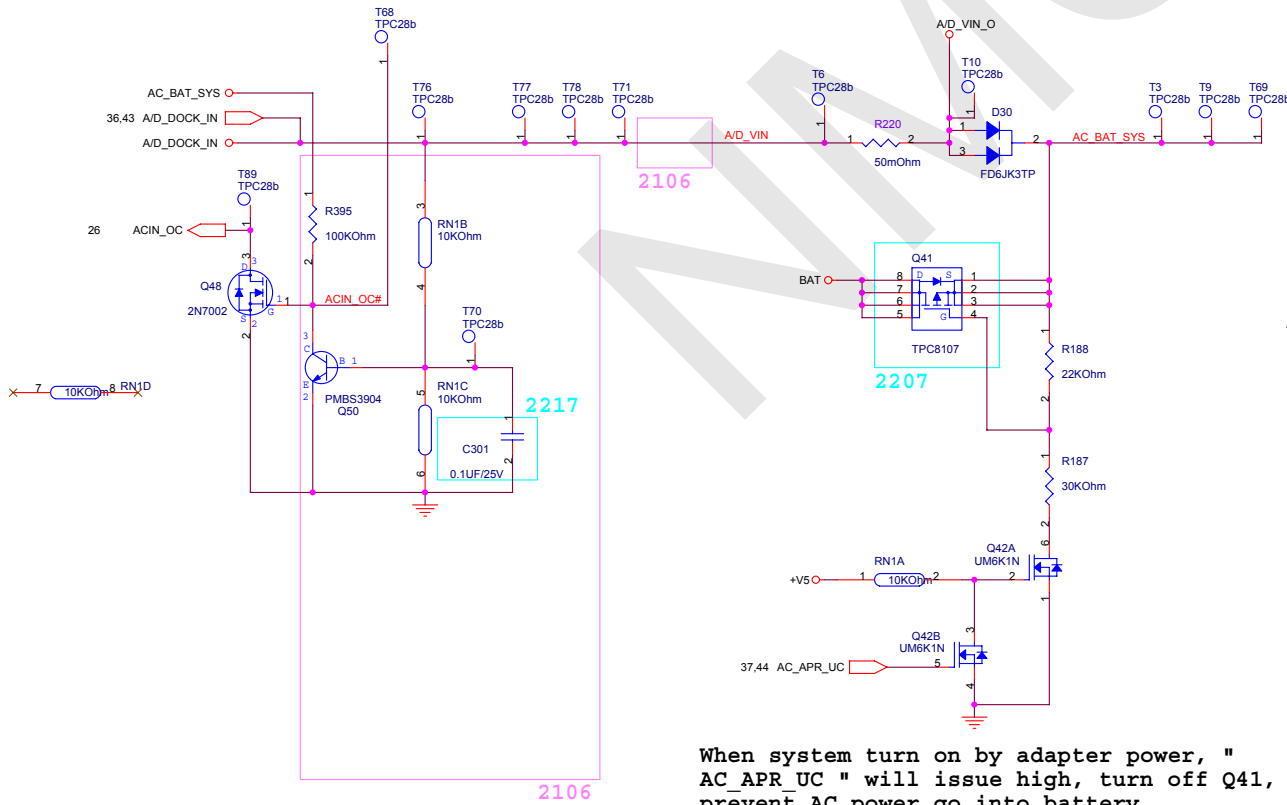
$A/D_VIN=19V$ $A/D_VIN_O=19V-3.1A*50\text{ohm}=18.845V$
 $CS+=CS-=19*(100/110)=17.272727V$
 $I1=(18.845V-17.272727V)/10K=0.15723mA$
 $V1=17.272727V-(0.15723mA*100K)=1.5497V$
 $I4=1.5497V/1K=1.5497mA$
 $I3=1.5497mA-0.15723mA=1.39247mA$
 $RC=(2.5V-1.5497V)/1.39247mA=681\text{ ohm}$





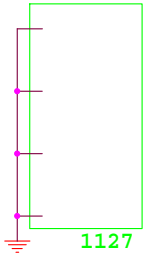


(H/W Battery low shutdown is 11.6V)

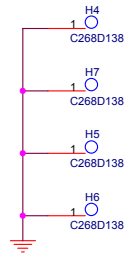
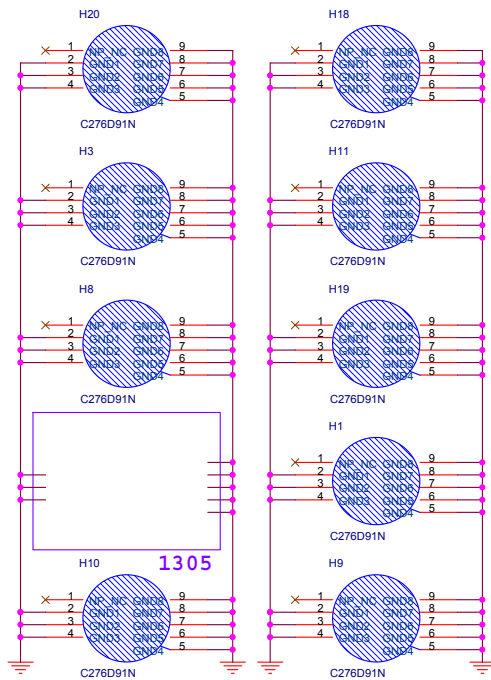
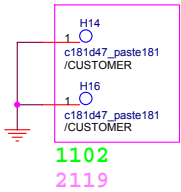


When system turn on by adapter power, "AC APR UC" will issue high, turn off Q41, to prevent AC power go into battery.

SCREW HOLE



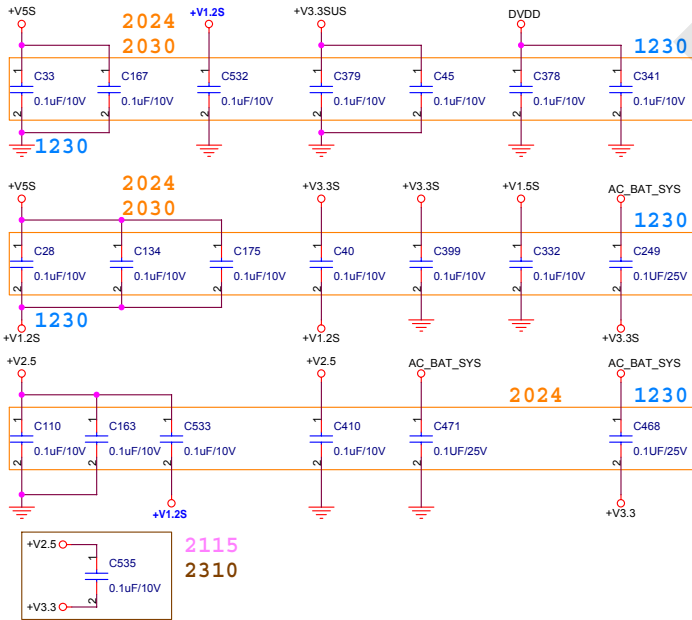
For MDC module



CPU Throttling(BIOS setting): 100 degree C.
 System shutdown(BIOS setting) : 110 degree C.
 H/W shutdown(page 44, U47 , no load) : 105 degree C(need fine turn R354).

Short Pad location:
 Page37: JP32
 Page39: JP4,5,15,16,19,26,27
 Page40: JP6,7,9,22,24
 Page42: JP13,14,17,18,28,29

EMI



Don't Short Pad: JP26
 JP4:+V2.5 --Power In
 JP5:+V1.25S
 JP6:+V2.5
 JP7:+V1.2S
 JP9:+VCCP
 JP13:+V5S
 JP14:+V5
 JP15:+V1.5SUS
 JP16:+V2.5 --Power IN
 JP17:+V1.8S
 JP18:+V12
 JP19:+V1.8
 JP22:+V1.5S
 JP24: VREF5-->+V5A
 JP26:+3VALWAYS T-->+V3.3A (open)
 JP27:+3VALWAYS M-->+V3.3A (short)
 JP28:+V3.3S
 JP29:+V3.3
 JP32:KBCRSM

PCB STACK-UP

PCB THICKNESS: 1.6 mm

- L1 TOP
- L2 VCC
- L3 GND
- L4 BOT

IMPEDEANCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	20 mils
37.5 OHM	WIDTH
TOP/BOT	12 mils
42 OHM	WIDTH
TOP/BOT	10 mils
55 OHM	WIDTH
TOP/BOT	5 mils
Differential	
70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 5 mils
90 OHM	WIDTH/SPACE
TOP/BOT	7 mils/ 10 mils
100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#

CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

Rev	Date	Description
R1.0	03/12/19	1. Initial release.
R1.1 Green Block	04/02/03	<p>1. Connect SDD0,SDD1 for RICOH request. Page 22.</p> <p>2. Add MDC screw hole P/N & footprint. Page 46.</p> <p>3. Connect CardBus chip INTC to PCI_INTD#. page 22.</p> <p>4. Change CB_SD# location from KBC to ICH4 GPIO25. page 15,21,26.</p> <p>5. Delete PCMCIA debug card function. page 18,23,29.</p> <p>6. Host clock frequency select failed.Add a pull-down R to FS3 so that FS[4:3]=00 and Host clock frequency=100MHz. page18.</p> <p>7. Load wrong value. Change RN39-RN48 from 560hm to 100hm. page 6.</p> <p>8. Load wrong value. Change pull-up RN . page 37.</p> <p>9. The value in M3N schematic is wrong. Change HUB_RCOMP_ICH4 pull-up R from 48.7KOhm to 48.70hm. page 14.</p> <p>10. Modify +V3S to +V3.3S. page 30.</p> <p>11. Can not boot in battery mode.Remove C497. page 37.</p> <p>12. Modify 20-pin connector pin define and add DJ_LED function for new touchpad. page 26,36.</p> <p>13. Due to height limitation, change BATT CONN. page 44.</p> <p>14. Remove the pull-up RN75B because AC_APR_UC has been pulled-up in page 45. page 37.</p> <p>15. Change CRT CONN because the original one was reversed. page 12.</p> <p>16. C271 change form 10UF/25V/X5R to 15UF/25V/POSCAP. page 43.</p> <p>17. U50 VCC change from +5VLCM to VCC_AD(19V). page 43.</p> <p>18. For wrong connection, change R354 pull-up power plane from +5VO to +5VA. page 44.</p> <p>19. Change R210 from 47K to 470K/0402. page 43.</p> <p>20. Add RN78 to pull high SMC BAT and SMD BAT, and add UM6K1N to prevent leakage current into KBC. page 26,44.</p> <p>21. For Power RD request, add R370 to CHG_EN#. page 44.</p> <p>22. Replace RN32 with 3 single 100K resistor. page 45.</p> <p>23. Change KB CONN pin definition because R1.0 was reversed. page 26.</p> <p>24. Remove INVTER_A from KBC and load L33 because BIOS RD decide to use NB to control the pannel backlight. page 12,26.</p> <p>25. Because P67/AN8 of KBC38857 cannot receive PWM signal, move CPUFAN_SPD_A to P57/DA2/PWM11 of KBC38857. page 26.</p> <p>26. Change LEDs' power to 5V level. page 36.</p> <p>27. Modify PCMCIA socket footprint. page 23,46.</p> <p>28. Combine connector : Change CON1,delete CON3,CON4. page 12, 34.</p> <p>29. Swap LAN connection(J2 pin5-12) for wrong connecting. page 33.</p> <p>30. Modify PM_RSMRST# circuit. page 37.</p> <p>31. For cost down, change X5,X7. page 19,30.</p> <p>32. Combine two NC7SZ14P5 into one SN74LV14APWR for cost down.page 37.</p> <p>33. To reduce jitter when charging, add R376,C520&C521. page 43.</p> <p>34. For M6N R1.1 wrong connection, change Audio DJ DJ_SCAN pin from KSO4 to KSO1. page 26,35.</p> <p>35. For Power RD request, add two beads L53&L54 at Vin Side. page 38.</p> <p>36. Modify EDID and panel ID optional circuit. page 12.</p> <p>37. Change CLR_DJ# to P53 because P54 of M38857 cannot be configured as output. page 26.</p> <p>38. Add R377 for Power RD request. page 43.</p> <p>39. Based on Ricoh's suggestion, remove CB_AGND and connect all AGND to generic GND. page 21,22.</p> <p>40. For cost down, change X4. page 44.</p> <p>41. Modify for battery 4S2P and 4S1P application. page 26,43,44.</p> <p>42. For EMI RD request, change Cap of CRT Pi-filter from 3.3pF to 15pF. page 13.</p> <p>43. Delete spread spectrum IC ICS91718 circuit because few model use it and not easy to buy. page 18.</p>

Rev	Date	Description
R1.1 Green Block	04/02/03	<p>44. Change C172 & C173 from 22pF to 5pF and unload R125 to obtain more accurate 8MHz frequency. page 26.</p> <p>45. For cost down, Power RD request to change Q9&Q11 to 07-005198012, U30 to 06-006002411, and U50 to 06-010112010. page 38,43,45.</p> <p>46. For Power RD request, change , C266 from 33pF to 220pF, C279 from 0.1uF to 0.01uF. page 41,43.</p> <p>47. Change U29 P/N for ME. page 31.</p>
R1.2 Blue Block	04/02/19	<p>1. LAN_RST# changes to 10K Ohm pull-down to GND. Page 15.</p> <p>2. To be able to hear low frequency in headphone mode, change C423 & C424 from 10uF/10V to CE30,CE31 47uF/6.3V. Page 31.</p> <p>3. Pull high BAT_IN#_OC, whose OC means Open Collector, to +V3.3 at KBC. Page 26.</p> <p>4. There is only one SS0540 in A3N, change to 1SS355. page 35.</p> <p>5. The power of LCD EEPROM connect to +V3.3S_LCD. When BIOS want to read EEPROM data, the EEPROM is still OFF,because +V3.3S_LCD is not enabled at this moment. Change EEPROM power to +V3.3S. page 12.</p> <p>6. Change R360,R363,R364,R366,R367,R378 value for charger at C.C. mode and change R200,R201,R204,R352 at C.S. mode to get more accurate current limit value. page 43.</p> <p>7. Add de-POP(reduce pop noise) circuit. page 31.</p> <p>8. Change Fan control function from PWM mode to DC mode. page 35.</p> <p>9. Based on Power RD's request, change Q33,R169,R148,R324. page 40,41.</p> <p>10. SSN can not turn on some panels since its diodes in inverter circuit have higher forward voltage. Follow S5N, change DAP202K and 1SS35 in inverter circuit to Schottky diode RB717F and RB751V-40 respectively. page 12.</p> <p>11. Electrical characteristics of diode 1SS35 and 1N4148-A2 can be compatible, but 1N4148-A2 has lower price. For cost down, change 1SS35 to 1N4148-A2. page 12,16,21,35,37,40,43,44,45.</p> <p>12. Change "Back light adjust" function from North Bridge to KBC. Change "CUPFAN_SPD_A" from KBC to ICH4 for BIOS request. page 8,12,26,35.</p> <p>13. For cost down, change audio AMP from APA2020A to G1420. page 31.</p> <p>14. A3N R1.1 uses the same AC_IN jack as L3F, which was found easy to be damaged. Change it to solder one used on A2. page 36.</p> <p>15. Follow M6N and WIN to modify RTC circuit. page 15.</p> <p>16. Un-mount Q59 and RN81 to control WLAN led directly from SB's GPIO pin: 802_LED_EN#. page 36.</p> <p>17. Swap 1394 TPB0+/-,TPA0+/- for smoother layout. page 22.</p> <p>18. X4 is dip type and at top side which may be lost in SMT IR re-flow for bottom side. Change X4 to SMD type. page 44.</p> <p>19. Add mini-PCI and USB WLAN hardware disable circuit page 12,15,20.</p> <p>20. QT report a bug: The "Center/Subwoofer Speaker Out" is invalid after setting "Number of Speakers" to 6-channel mode for 5.1 speaker output and then executed "Speaker Test". Modify relative circuit. page 30,32.</p> <p>21. Fine tune audio amp low-pass frequency. page 31.</p> <p>22. Delete RN79 because after experiment we find it can be un-mounted. page 36.</p> <p>23. Remove LCD EDID relative circuit. page 8,12.</p> <p>24. Combin R191,R308,R380 and R381 into 4R8P RN88. page 26.</p> <p>25. Follow SSN to modify CRT_DDC circuit to prevent current leakage. page 13.</p> <p>26. Although crystal DIP type is cheaper than SMD type, but costs more manpower. Change X5 and X7 back to SMD type. page 19,30.</p> <p>27. Improve accuracy of reading fan speed. page 35.</p> <p>28. Swap RN4 and pin8,9 of RP4 for smoother layout. page 13,17.</p> <p>29. For cost down, change U6 and U12 NS LM358MX (06-010008000) to TI LM358ADR (06-010112010). page 30,35.</p> <p>30. For EMI RD's request to modify BOM. page 18,19,22,30,31,32,33,46.</p> <p>31. Add description of choosing 855GM or 852GM/GME/GMV platform by changing R148. page 40.</p> <p>32. Debug code will stop at "A0" or "06". Modify SMBus layout: 1. Daisy chain routing. 2.Don't cross power plane when the trace refer to power plane. Page 17.</p>

Rev	Date	Description
R1.3 Purple Block	04/03/11	<p>1. Pin23, ISOLATEB, of LAN 8100CL need to be low in S3. Follow MB P4PE-X to connect it with PM_SLP_S3#. page 19.</p> <p>2. Debug Code will stop at "13". Change SMBus Pull-High RN29 from 4.7KOhm(0402) to 1KOhm(0603). page 17.</p> <p>3. Improve MIC layout. page 12,32.</p> <p>4. For Power RD's request to modify charger circuit. page 43,44.</p> <p>5. Delete screw hole H2, to prevent CN7 short with H2. Layout engineer create a new screw hole. page 46.</p> <p>6. For Power RD's request to modify BOM. Change R108 from 100K to 75K for OCP, un-mount R93 and mount R94 to meet Intel CPU spec. page 38.</p>
R2.0 Orange Block	04/04/15	<p>1. Sometimes Debug Code will stop at "00" in ON/OFF test. Modify power sequence circuit , delete R163. page 38,40.</p> <p>2. Based on request came from factory to update all testpoints' symbol because all testpins are changed from 75mil to 68mil. All pages that include test points.</p> <p>3. Power team request, cost down D51 part. page43.</p> <p>4. Fine-tune R385,R386 and R387 to get more accurate level of fan ON/OFF detection. page35.</p> <p>5. When system with battery only. System can't be power on after push Force OFF button SW6. Because SW6 connect to SHUT_DOWN#, but this signal will be latch low(power design: when battery low, page 46 : battery low detect circuit will issue low than latch it.) when it is at low state. Don't connect SHUT_DOWN# to SW6 at page 37.(SHUT_DOWN# already connected to 3V_ON at page 41. Connect SW6 to U25, and change D40 to 1N4148(delete at item 2015). Page 37.</p> <p>6. Because A3N use SW6 as "Force OFF" button ,not "Reset" button. We don't need connect SW6 to PIC16C54C. Delete D24.page37,44.</p> <p>7. Can't turn on Audio DJ when system only with battery and no adapter. Because +V3.3SUS will be turn off when system only with battery. Need turn on +V3.3SUS by connect DJ_SW# to 3V_ON. Change D45 to DAP202K. Page 37.</p> <p>8. LAN crystal accurate is 39.2ppm, it can't meet spec. +/-30ppm). Change from 15pF to 18pF to meet spec. page 19.</p> <p>9. Some system can't boot by battery only. Because signal "SHUTDOWN#" be latch at low state. Change R6 value from 470K to 100K. Page 45.</p> <p>10.QT bug : Noise occur from headphone via speaker out jack. Change R124,R298,R285 from Bead to 0 ohm. Page 30,31.</p> <p>11.The Power LED should not be bright when enabled Audio DJ in power off mode. Page 36.</p> <p>12.The inductor will cause the 2.5V power control loop unstable. Change L40 to R389 Page 19.</p> <p>13. Balance the LED Brightness. Fine tune R value,R140 470-->220,R311,R312 470-->1K. Page 36.</p> <p>14. G571(U49) 593 Control Signal(U37) VPPD0 : VPPEN1 VPPD1 : VPPEN0 Otherwise, CardBus Card may be destroyed. Page 23.</p> <p>15. When issue OTP RESET#, system can't be turn off & display white screen. Because LTC3728 can't be shutdown by only put low 3V_ON. Need shutdown +V3.3SUS & +5VO at the same time. Delete D40. Page 37.</p> <p>16. Change Q63,Q66,Q71 and no load Q63,R338,C482,R354,R358,C502,U47 for cost down. page 35,37,44.</p> <p>17. Add test point for Taipei Factory request. page 6,12,15,16,19,30,36,37,38,39,42,43,44</p> <p>18. QT bug: Pop noise can be heard via headphone when system boot, restart and resume from S3. Modify De-Pop circuit. page 31,37.</p> <p>19. Taipei factory request : Add R391 for different battery charge current test at 8 cells and 4 cells. Page44.</p>

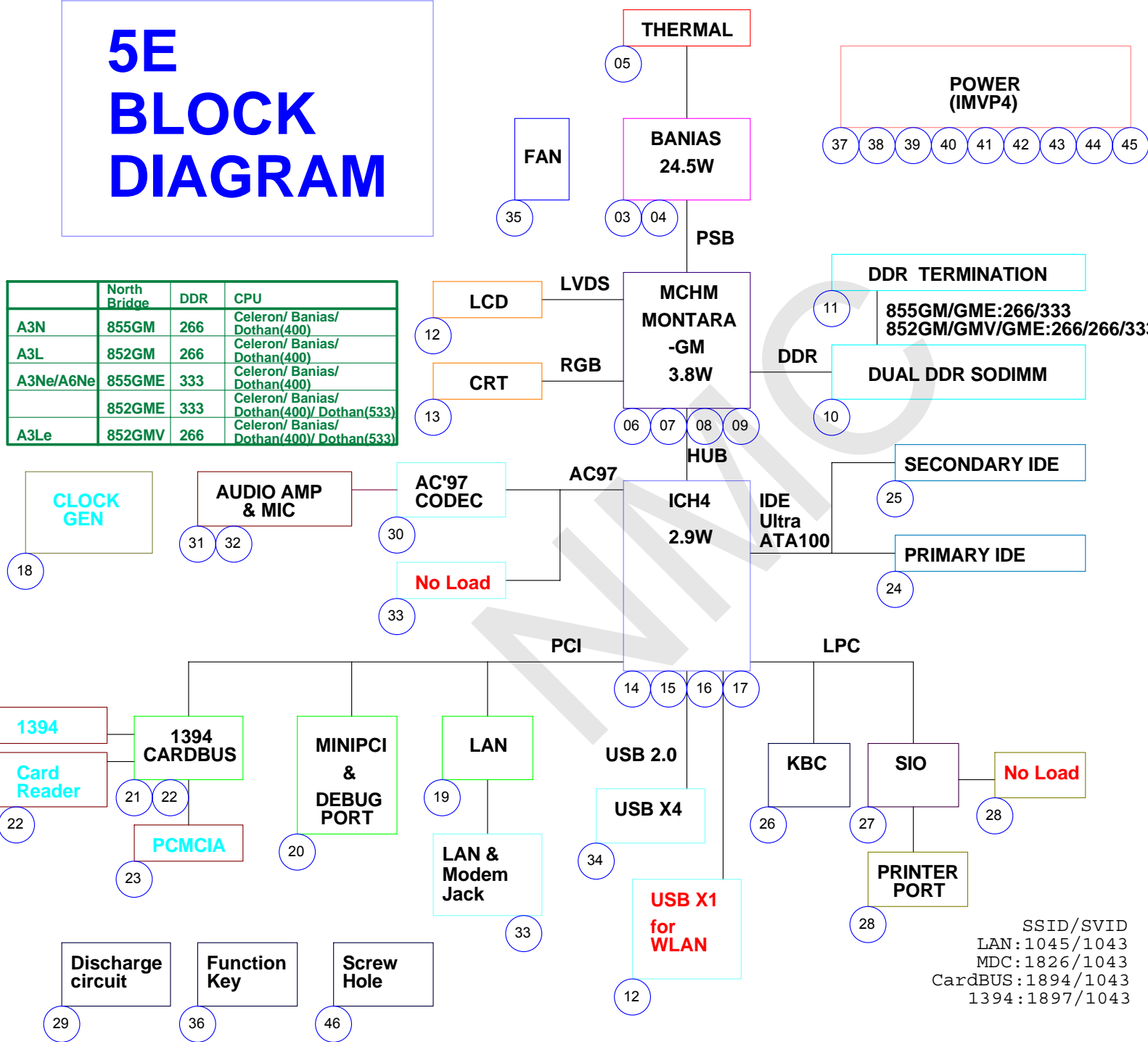
Rev	Date	Description
R2.0 Orange Block	04/04/27	<p>20. EMI request, load C144, C525. page 32.</p> <p>21. ICH4 GPIO [24:43] , default state is output high, if PID_[0:3] be connected to GND by LCD cable, these GPIO will issue +V3.3 (default output high) short to GND during system power on. Add R=2.2K to prevent this kind of situation. Page 15.</p> <p>22. Measurement team Problem: VGA EA fail below items 1,V-SYNC:under shoot over 30% of high level voltage range. 2,H-SYNC:over shoot over 30% of high level voltage range, under shoot over 30% of high level voltage range. Change Change C304, C305 from 5pF to 33pF. Page 13.</p> <p>23. EMI request use Choke on USB & 1394 ports. Delete option R, don't co-layout. Page 22,34.</p> <p>24. EMI request : Add C531,C532,C533,C535. Delete C147,C433. Change C110,C163 connection. Change C410 location. Change C378,C379,C410,C163,C110 to 0.1uF/10V. Change C471,C468 to 0.1uF/25V. Change C45,C33,C28,C134,C332,C399,C341 to 0.1uF/10V and don't load. Change C40 to 0.1uF/10V. Change C249 to 0.1uF/25V and don't load. Page 10,46. Change R104 from 0 ohm to bead. Page 31.</p> <p>25. Change C26,C98,C104,C325 (page3) , C362 (page7) , C324,C329 (page9) , C436 (page14) , C190,C441 (page16) , C366,C367 (page19) , C247 (page21) , C467,C473,C478 (page22) , C236 (page23) , C209,C210,C211,C242 (page40) , C40 to 0.1uF/25V to 0.01uF/10V. Use 10V is OK.</p> <p>26. Measurement team Problem: VGA EA fail in rise time and fall time of RGB signal at resolution 1024X768 at 60Hz. Change L6,L7,L8 from 750hm/100MHz to 700hm/100MHz. Page 13.</p> <p>27. Load FAN on/off component : /FAN_SPD. page 35.</p> <p>28. Change L53,L54 from 09-012400000 to 09-012400001 for cost down. page38.</p> <p>29. CON1,CON7,CON12,CON15 and J4 change to formal P/N. page 12,24,25,36,44.</p> <p>30. For EMI RD's request, change R384 from 0 ohm to Ferrite bead, and add EMI capacitors: C28,C33,C45,C134,C167,C175,C332,C341,C399,C249. Page 32,46.</p> <p>A3L. For A3L platform : change U32 to 852GM, R148. page 6,7,8,9,40.</p>
R2.1 Pink Block	04/05/14	<p>1. For ESD test fail at switch, If we want to use ESD protect diode, we can't connect switch pin 1&2, pin3&4 to make sure the energy will go through ESD diode : SW1-5. page36.</p> <p>2. Forget pull high at D54.3. Add R392 pull high to +V3.3S. page 31.</p> <p>3. For cost down. Delete R=0 OHM. R389,R331,R124,R298,R285,R281,R276 (no load),R290 (no load) . page 19,22,30,31</p> <p>4. QT report that a "pop" noise occurs when booting. This is because the timing of OP_SD# to control audio AMP ON. Change D49 from DAP2020K to 1N4148W-A2 to control the AMP shutdown only the JACK_IN#, and control SE/BTL# by D54.3. page 31.</p> <p>5. In audio DJ mode, DJ_LED turns on Q91 and PWR_LED_UP will connect to GND which may damage PIC. Use RN80A to prevent it. page 36.</p> <p>6. Power RD modification: Delete 0 Ohm: R135,R136,R137 Delete U24, change Q34 to 3904 and add R393,R394. Change R202,R356,R357 BOM to modify BAT CV tolerance to more accurate. Delet Q5,Q1,C18,R9,R10,RN2 and add R395. page 40,43,45.</p> <p>7. Swap RN80 for smoother layout. page 36.</p> <p>8. QT bug: when booting or being idle, two A3 with USB CCD module will sometimes appear "Hi-speed device plug into low-speed hub" in Windows XP/2000. Adjust USBBIAS and USBBIAS# external resistor R138 from 18.2ohm to 22.6ohm. page 15.</p>

Rev	Date	Description
R2.1 Pink Block	04/07/16	<p>9. For TPE_ENG Power RD's request to unify OTP_RESET#, FORCE_OFF#_SW and FORCE_OFF# into single name: FORCE_OFF#. page 37,44.</p> <p>10. About 2019 item, factory don't need it now. Delete R391. page 44.</p> <p>11. C117 don't need use 25V, change to 4.7uF/10V. page 9.</p> <p>12. Factory found that there are two A3 systems will fail at On Off test. Net " PM DPRSLPVR" will be issued wrong status by Vcore Power IC MAX1987 when system on . Add a 20pF at R106.2 or change R106 from 1K to 0 OHM can solve this issue. Change R106 to 0 OHM. Page 38.</p> <p>13. Power request. Don't need use 1K ohm, change R100,R292,R329,R168 from 1K to 0 ohm. Page 38,42.</p> <p>14. Fine tune E-mail LED (R140 : from 220 to 1K)& Wireless LED (R312 : from 1K to 680) for customer's request. Page 36.</p> <p>15. Because C535 will touch with the boss of C mechanical part. Don't load C535. Page 46.</p> <p>16. Even we pull down pin 1 or pin 2 of DAP202K, the UM6K1N is still possible to be turn on. It is because that the maximum forward voltage of DAP202K is 1.2V but the gate threshold voltage of UM6K1N is 0.8V-1.5V. Change D32,D45 and D54 from DAP202K to RB717F since the maximum forward voltage of RB717F is only 0.37V. Page 31,35,37.</p> <p>17. Phone jack (P/N: 12-140001087) used in A3N/L has been phased out. The vendor suggests us to use 12-140001088 as substitution. Page 31.</p> <p>18. As R2.1 item 16, we changed D32,D45 and D54 from DAP202K to RB717F. But SMT reports that RB717F has smaller package than DAP202K such that may cause connection between RB717F and pad failed. In A3 design, the forward current will be no more than 0.5mA. According to DAP202K forward characteristics, it's impossible to reach the minimum threshold voltage of UM6K1N (0.8V). So it's safe to change D32, D45 and D54 from RB717F back to DAP202K. Page 31,35,37.</p> <p>19. 5E customer doesn't need the MDC and SIR function, so A3L removes the relative components: R30, R31, R129, R143, R144, R186, R190, R305, RN21, RN66, RN67, C149, C174, C180, C185, CN6, CON5, H14, H16, U35. Page 15,28,30,33,46.</p> <p>20. D23 uses DIODE 1N4148W-A2 but its larger forward voltage may makes KBC M38857 detect error. Change it to Schottky diode SS0540 that has smaller forward voltage. Page 44.</p> <p>21. Taipei SMT reports that X2 (07-010303271) has open risk, and recommends us to use 07-010303273 as first source, 07-010303271 and 07-010703273 as second source for manufacturability improve. Page 15.</p> <p>22. Factory found that there are some X4 part don't work. Change C522,C533 from 33pF to 15pF. Page 44.</p>

Rev	Date	Description
R2.2 Light Blue Block	04/09/22	<p>3. Refer to R2.1 item 12, reserve C536 but load 1M ohm for PM DPRSLPVR. Page 38.</p> <p>6. Modify layout footprint for R:2.1 item 21. Page 15.</p> <p>7. Based on Power RD's request, change Q41 from 07-005151010 to 07-005159010 for cost down. Page 45.</p> <p>8. 7H Project VFLP : Remove Super I/O : U11,C143,C146,C127,C151,C136,R103,RN17,Q16,R82,R63. Page 27,18. Remove Printer Port : LN1, LN2, LN3, LN4, CN8, CN9, CN10, CN11, L36, CN7, C300. Page 28. Remove IR: R129,U35,C174,C180,C185,RN21,RN66,RN67. Page 28. Remove MiniPCI Port : CON17,C487,C485,C469,C486,C470,R332,R81. Page 20,18. Remove WLAN function : RN86,Q87,Q88,Q79,R312. Page 12,20,36. Remove USB CMOS camera & USB WLAN function : CE29,L51,L52,L50,C11,C12. Page 12. Set normal type ODD as master : No load R127, Load R126. Page 25.</p> <p>9. Power "VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPELLA,VCCADPLL" have different defined value in datasheet and RDDP. Confirmed with Intel FAE to get the final correct value, and will be phased in on R2.2 and R:2.4 BOM. Page 9,40.</p> <p>10. R249,R251,R252 will have different value based on different North Bridge. All the corresponding values are listed in Page 7 and will be phase in on R2.2 and R:2.4 BOM. Page 7.</p> <p>11. Because Vendor (CC&C) can't support hardware On/Off WLAN module function, don't load Q87 at R:2.2 & R2.4. Page 12.</p> <p>12. Factory found that there are some DDR SO-DIMM(UNIFOSA,MOSEL)will fail during Memory test of Run-In test. Change R176 from 19.6K to 20.5K 1%, fine tune +V2.5 from 2.5V to 2.592V. Add SO-DIMM noise margin at R:2.2 & R:2.4. Page 40.</p> <p>13.For 5E customer,don't need USB CMOS camera,no load L51,C12. Page12.</p> <p>14. Change C193,194,195 for 7H customer's request about the gap between these capacitors and Mechanical C part. Change Cap from 2.5mm height(11-03B210621) to 2.0mm(11-031110621). Page 40.</p> <p>15. For M/E request, add a second source 12-172010300 on CON2. Page 12.</p> <p>16. Change CE9 for 7H customer's request about the gap between these capacitors and Mechanical C part. Change Cap from 2.8mm height(11-08D210711) to 1.8mm(11-08D215706). Page 41.</p> <p>17.When the system temperature rise high due to the system running at heavy loading. The leak current(IR) of D30 schottky diode will be increased, the H/W AC detect circuit will make a wrong state. Net " ACIN_OC " will issue " high". Change C301 from 0.1uF to 1Kohm, it can solve this problem. Make sure it will issue "low" at this moment. Page 45.</p> <p>18. For the request from 7H customer, change CE15,CE18 from Tantalum capacitor (11-015000220) to Oxi capacitor. Page 9. 2004/9/29 : Change at VPLP R:2.2, A3L R:2.4,A3Le R:2.4,A3Ne R:2.4.</p> <p>19. For the request from 7H customer, follow the USB spec. , one port max current is 0.5A, so two ports max current is 1A. Change F1,F2 from 1.5A/6V polyswitch to 1.1A/6V polyswitch, P/N is 07-014110900 (2nd source is 07-014110201). Change at VPLP R:2.2 only. Page 34</p> <p>20. 7H customer found that there are some VPLP system use Bufferlo WLI-CB-AG54 Wireless LAN PC-card will fail at some channel when connect to Access Point. Add C390 with 10pF and change C499 from 0.1uF to 1000pF (11-034110241) to reduce clock and power noise. Modify VPLP BOM only. Page 18,23.</p> <p>21. +V5A will issue leakage current to +V3.3SUS by U48.4 --> D45 --> RN76B when plug in Battery module only. Change C379 from 0.1uF to 1K ohm (10-004401020). Page 46.</p> <p>22. The position pin of CON9 & CN7 are base on 1.2mm PCB design, but A3& A6 PCB is 1.6mm. Modify the length of position pin of these connector (CON9: 12-101102154 , CN7:12-10110025I). Page 13,28.</p>
	04/10/01	
	04/10/14	
	04/10/22	

Rev	Date	Description
R2.3 Brown Block	04/07/23	<p>1. For Vendor request : Pin footprint diameter is 1.0mm+/-0.05, but ASUS rule is diameter*diameter = (L*L+W*W). Modify Battery Connector J1 as vendor spec. **NO FIX**. Page 44.</p> <p>2. For Thermal RD request : Let the fan be off before BIOS control because it can let user doesn't feel the fan on-off noise obvious while system boot. Use OP_SD_DLY to control it. Page 31,35.</p> <p>3. None (the same as R:2.2 item 1)</p> <p>4. QT Bug: Noise occurred during system resume from S1. The timing of DLY_OP_SD# and AC97_RST# still can not prevent the pop noise. Realtek recommends to use pin47 EAPD to substitute AC97_RST#. This pin can be controlled by codec driver to meet our timing request. Page 30,31.</p> <p>5. Change D23 to SCHOTTKY RB751V-40 to decrease part type. Page 44.</p> <p>6. Modify short pad for factory's request. page 37(JP32), page 39(JP15,16,19,26,27), page 40(JP9,24), page 42(JP17,18).</p> <p>7. For A3 series ID2 power switch, add a Blue LED,change R309 from 470 ohm to 220 ohm. Page 36.</p> <p>8. Add CPU +VCCA power switch circuit to meet Celeron/ Banias/ Dothan(400)/ Dothan(533) CPU spec. Page 3,4,18.</p> <p>9. Base on Factory SMT request : modify CN7 & CN9 footprint (only for 1.6mm thickness PCB). page 13,28.</p> <p>10. Re-load C535 because the position is changed and will not touch with boss of C mechanical part. page 46.</p> <p>11. Modify R106, R100, R292, R329, R168 to Short Pin JP36, JP37, JP38, JP39, JP40 for power function parts cost down. page 38,42.</p> <p>12. To synchronize the parts in the schematic with BOM, change R104, R302, R303, R91, R92, R384, R111, R112, R31, R30 to L55, L56, L57, L58, L59, L60, L61, L62, L63, L64. page 31,32,33.</p> <p>13. Remove 0 ohm: R377 and R180 for cost down. page 22,43.</p> <p>14. Based on Power RD's request, change Q45 from 07-005151010 to 07-005159010 for cost down. Page 43.</p> <p>15. BIOS RD request to distinguish PCB version by reading PCB_VID[2:0]. Change PCB_VID[2:0] configuration and add descriptions. Page 21.</p> <p>*. Because R:2.4 item 2. We can't phase in R:2.3.</p>
R2.4 Gray Block	04/08/27	<p>1. To improve ESD margin. Add De-Bounce circuit. Page 36.</p> <p>2. Add GST[2:0] strap circuit for supporting Dothan 533 CPU. Page 8.</p> <p>3. Taipei Factory repored that some A3N systems still failed(13/5000) in resuming from suspend to RAM. Power RD request to change JP36 back to R106 and change the value to 100K ohm. Page 38.</p> <p>4. For EMI request. Connect switch pin 1&2, pin3&4 of SW1-5. page36.</p> <p>5. Change PCB VID for R.2.4 page 21.</p> <p>6. Remove JP37 and JP39. page36.</p> <p>7. As R2.4 item 3, Power RD find the root cause: When system booting or resuming from S3, the siganl " PM DPRSLPVR" from South Bridge, it will be floating in a short time(40ms) and cause +VCORE output wrong voltage(0.76V). Add a resistor 1M ohm between net " PM DPRSLPVR" and GND in order to keep PM DPRSLPVR at low state when floating. Add R106 = 0ohm and change C536 to R410 (1M ohm). page 38.</p>
	04/10/14	<p>8. The position pin of CON9 & CN7 are base on 1.2mm PCB design, but A3& A6 PCB is 1.6mm. Modify the length of position pin of these connector (CON9: 12-101102154 , CN7:12-10110025I). Page 13,28.</p> <p>9. For cost down , add 06-045021010 AUDIO AMP. TPA0102 (power is 1.5W)as first source and change original part (power is 2W) as second source. Page 31.</p> <p>10. For power team request. Change Q2 from UMZ1N(Not easy to buy it) to BC847BPN. Page 45.</p>

5E BLOCK DIAGRAM



	North Bridge	DDR	CPU
A3N	855GM	266	Celeron/ Banias/ Dothan(400)
A3L	852GM	266	Celeron/ Banias/ Dothan(400)
A3Ne/A6Ne	855GME	333	Celeron/ Banias/ Dothan(400)
	852GME	333	Celeron/ Banias/ Dothan(400)/ Dothan(533)
A3Le	852GMV	266	Celeron/ Banias/ Dothan(400)/ Dothan(533)

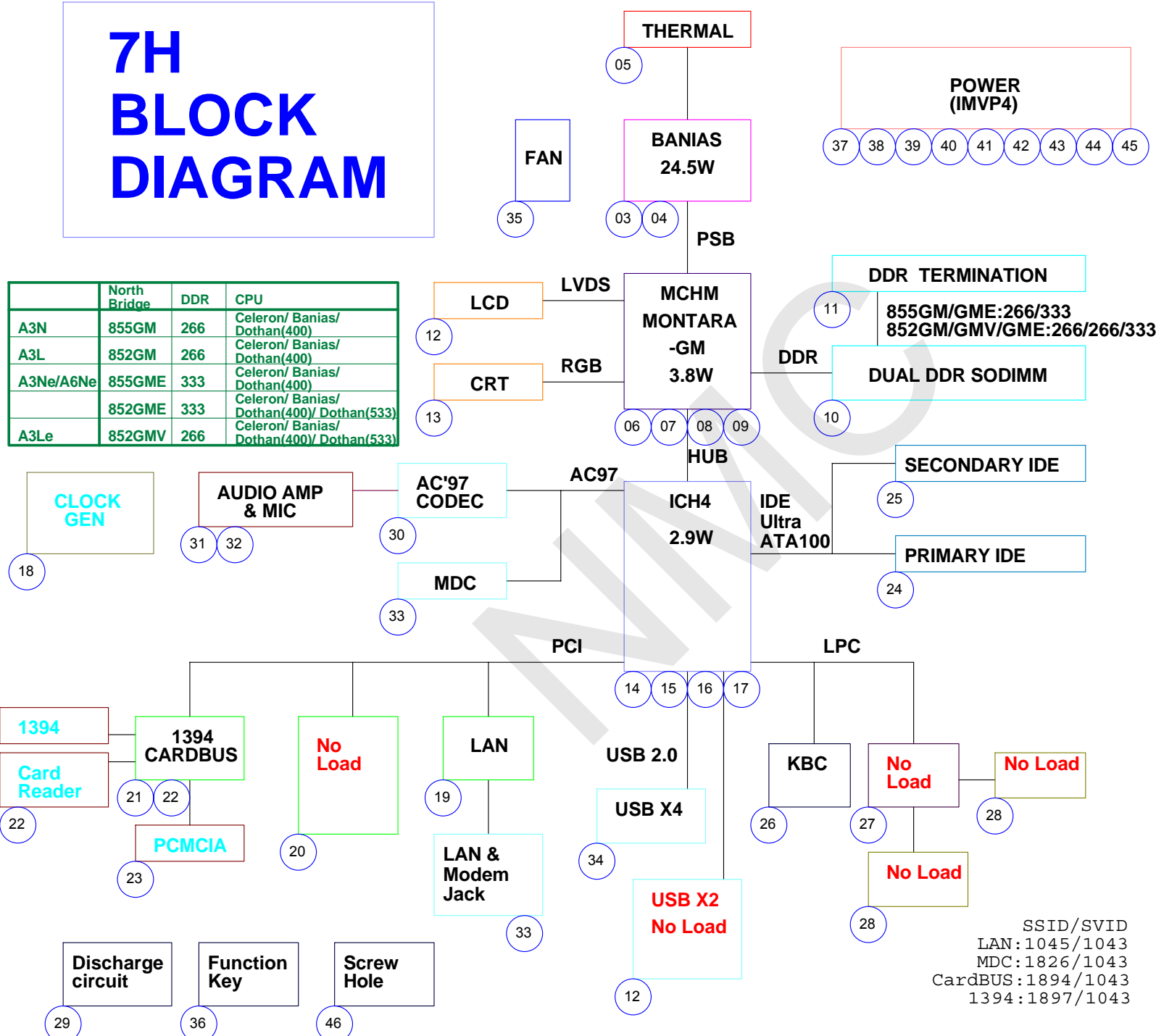
FILE LIST

01

- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-BANIAS(HOST)
- 04_CPU-BANIAS(PWR)
- 05_THERMAL
- 06_NB-MCHM(DDR)
- 07_NB-MCHM(HOST)
- 08_NB-MCHM(VGA)
- 09_NB-MCHM(PWR)
- 10_DUAL DDR SODIMM
- 11_DDR TERMINATION
- 12_LVDS & BACKLIGHT
- 13_CRT CONNECTOR
- 14_ICH4-M(HUB_PCI)
- 15_ICH4-M(H_U_IDE_PM)
- 16_ICH4-M(PWR)
- 17_ICH4-M_PULLUP
- 18_CLOCK-ICS950815
- 19_LAN-RTL8100CL
- 20_MINIPCI
- 21_CB1394-R5C593(1)
- 22_CB1394-R5C593(2)
- 23_PCMCIA SOCKET
- 24_IDE-HD
- 25_IDE-ODD
- 26_KBC-M38857
- 27_SIO-ITE7805
- 28_IR&LPT_PORT
- 29_DISCHARGE CIRCUIT
- 30_CODEC-ALC650
- 31_AUDIO AMP
- 32_MIC
- 33_MDC&RJ45&RJ11
- 34_USB
- 35_FAN&Audio DJ
- 36_FUNCTION KEY
- 37_PWR & RESET SEQ
- 38_VCORE
- 39_1.25V&1.8V
- 40_2.5V&1.5V&1.35V&1.05V
- 41_SYSTEM
- 42_LOAD SWITCH
- 43_CHARGER
- 44_PIC16C54
- 45_BATLOW/SD#
- 46_SCREW HOLE & M/B SETTING
- 47_REVISION(1)
- 48_REVISION(2)
- 49_REVISION(3)
- 50_REVISION(4)
- 51_BLOCK DIAGRAM 5E
- 52_BLOCK DIAGRAM 7H
- 53_Part Reference 1
- 54_Part Reference 2

SSID/SVID
LAN: 1045/1043
MDC: 1826/1043
CardBUS: 1894/1043
1394: 1897/1043

7H BLOCK DIAGRAM



FILE LIST 01

- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-BANIAS(HOST)
- 04_CPU-BANIAS(PWR)
- 05_THERMAL
- 06_NB-MCHM(DDR)
- 07_NB-MCHM(HOST)
- 08_NB-MCHM(VGA)
- 09_NB-MCHM(PWR)
- 10_DUAL DDR SODIMM
- 11_DDR TERMINATION
- 12_LVDS & BACKLIGHT
- 13_CRT CONNECTOR
- 14_ICH4-M(HUB_PCI)
- 15_ICH4-M(H_U_IDE_PM)
- 16_ICH4-M(PWR)
- 17_ICH4-M_PULLUP
- 18_CLOCK-ICS950815
- 19_LAN-RTL8100CL
- 20_MINIPCI
- 21_CB1394-R5C593(1)
- 22_CB1394-R5C593(2)
- 23_PCMCIA SOCKET
- 24_IDE-HD
- 25_IDE-ODD
- 26_KBC-M38857
- 27_SIO-ITE7805
- 28_IR&LPT_PORT
- 29_DISCHARGE CIRCUIT
- 30_CODEC-ALC650
- 31_AUDIO AMP
- 32_MIC
- 33_MDC&RJ45&RJ11
- 34_USB
- 35_FAN&Audio DJ
- 36_FUNCTION KEY
- 37_PWR & RESET SEQ
- 38_VCORE
- 39_1.25V&1.8V
- 40_2.5V&1.5V&1.35V&1.05V
- 41_SYSTEM
- 42_LOAD SWITCH
- 43_CHARGER
- 44_PIC16C54
- 45_BATLOW/SD#
- 46_SCREW HOLE & M/B SETTING
- 47_REVISION(1)
- 48_REVISION(2)
- 49_REVISION(3)
- 50_REVISION(4)
- 51_BLOCK DIAGRAM 5E
- 52_BLOCK DIAGRAM 7H
- 53_Part Reference 1
- 54_Part Reference 2
- 55_Power Net Reference

SSID/SVID
LAN: 1045/1043
MDC: 1826/1043
CardBUS: 1894/1043
1394: 1897/1043

+1.2V0 - Page 40
+1.05V0 - Page 40

+1.5V0 ○ ○ +1.5V0 40
+1.8V0 ○ ○ +1.8V0 39,42
+2.5V0 ○ ○ +2.5V0 40
+2.5VREF ○ ○ +2.5VREF 43,45
+3VALWAYS_M ○ ○ +3VALWAYS_M 39
+3VALWAYS_T ○ ○ +3VALWAYS_T 39,40
+5VAO ○ ○ +5VAO 41
+5VCHG ○ ○ +5VCHG 45
+5VLCM ○ ○ +5VLCM 36,44,45
+5VO ○ ○ +5VO 38,40,41,42,45
+12V0 ○ ○ +12V0 41,42
+15VOSUS ○ ○ +15VOSUS 39
+AVCC ○ ○ +AVCC 23
+AVPP ○ ○ +AVPP 23
+V1.2S ○ ○ +V1.2S 7,9,29,40,46
+V1.2S_GMCH_ASM ○ ○ +V1.2S_GMCH_ASM 9
+V1.2S_GMCH_CORE ○ ○ +V1.2S_GMCH_CORE 7,9,29,40,46
+V1.2S_GMCH_DPLLA ○ ○ +V1.2S_GMCH_DPLLA 9
+V1.2S_GMCH_DPLLB ○ ○ +V1.2S_GMCH_DPLLB 9
+V1.2S_GMCH_HI ○ ○ +V1.2S_GMCH_HI 7,9,29,40,46
+V1.5S_ICH ○ ○ +V1.5S_ICH 8,9,13,14,16,29,40,46
+V1.5S ○ ○ +V1.5S 8,9,13,14,16,29,40,46
+V1.5S_GMCH_ADAC ○ ○ +V1.5S_GMCH_ADAC 8,9,13,14,16,29,40,46
+V1.5S_GMCH_ALVDS ○ ○ +V1.5S_GMCH_ALVDS 8,9,13,14,16,29,40,46
+V1.5S_GMCH_DLVDSD ○ ○ +V1.5S_GMCH_DLVDSD 8,9,13,14,16,29,40,46
+V1.5S_GMCH_DVO ○ ○ +V1.5S_GMCH_DVO 8,9,13,14,16,29,40,46
+V1.5S_ICH ○ ○ +V1.5S_ICH 8,9,13,14,16,29,40,46
+V1.5S_ICHPLL ○ ○ +V1.5S_ICHPLL 8,9,13,14,16,29,40,46
+V1.5SUS ○ ○ +V1.5SUS 16,39
+V1.5SUS_ICH ○ ○ +V1.5SUS_ICH 16,39
+V1.8 ○ ○ +V1.8 21,39
+V1.8S ○ ○ +V1.8S 4,18,29,42
+V1.25S ○ ○ +V1.25S 11,39
+V1.8S_VCCA ○ ○ +V1.8S_VCCA 3,18
+V1.8S_PROC ○ ○ +V1.8S_PROC 3,4
+V2.5 ○ ○ +V2.5 6,9,10,39,40,46
+V2.5_GMCH_SM ○ ○ +V2.5_GMCH_SM 6,9,10,39,40,46
+V2.5_GMCH_TXLVDS ○ ○ +V2.5_GMCH_TXLVDS 9
+V2.5_GMCHQSM ○ ○ +V2.5_GMCHQSM 6,9,10,39,40,46
+V3.3 ○ ○ +V3.3 12,14,15,20,21,22,23,26,27,28,29,30,31,33,35,36,37,39,42,46
+V3.3_1394 ○ ○ +V3.3_1394 21,22
+V3.3_IRED - Page 28

+V3.3_MC_VCC ○ ○ +V3.3_MC_VCC 22
+V3.3_MDC ○ ○ +V3.3_MDC 12,14,15,20,21,22,23,26,27,28,29,30,31,33,35,36,37,39,42,46
+V3.3_MPCI ○ ○ +V3.3_MPCI 12,14,15,20,21,22,23,26,27,28,29,30,31,33,35,36,37,39,42,46
+V3.3_VCC1 ○ ○ +V3.3_VCC1 28
+V3.3A ○ ○ +V3.3A 12,15,35,37,39
+V3.3S ○ ○ +V3.3S 4,5,8,9,10,12,14,15,16,17,18,20,21,24,25,26,27,29,30,31,33,35,42,46
+V3.3S_CLK ○ ○ +V3.3S_CLK 18
+V3.3S_CLK48 ○ ○ +V3.3S_CLK48 18
+V3.3S_CLKA ○ ○ +V3.3S_CLKA 18
+V3.3S_GMCH_GPIO ○ ○ +V3.3S_GMCH_GPIO 4,5,8,9,10,12,14,15,16,17,18,20,21,24,25,26,27,29,30,31,33,35,42,46
+V3.3S_ICH ○ ○ +V3.3S_ICH 4,5,8,9,10,12,14,15,16,17,18,20,21,24,25,26,27,29,30,31,33,35,42,46
+V3.3S_LCD ○ ○ +V3.3S_LCD 12
+V3.3S_LCD_C ○ ○ +V3.3S_LCD_C 12
+V3.3S_MDC ○ ○ +V3.3S_MDC 4,5,8,9,10,12,14,15,16,17,18,20,21,24,25,26,27,29,30,31,33,35,42,46
+V3.3S_THM ○ ○ +V3.3S_THM 5
+V3.3SUS ○ ○ +V3.3SUS 13,15,16,17,19,20,21,26,37,39,41,42,44,46
+V3.3SUS_ICH ○ ○ +V3.3SUS_ICH 13,15,16,17,19,20,21,26,37,39,41,42,44,46
+V3.3SUS_LAN ○ ○ +V3.3SUS_LAN 13,15,16,17,19,20,21,26,37,39,41,42,44,46
+V5 ○ ○ +V5 6,12,21,23,26,27,29,30,31,34,35,36,42,45
+V5_AUDIO ○ ○ +V5_AUDIO 30
+V5_USB01 ○ ○ +V5_USB01 34
+V5_USB24 ○ ○ +V5_USB24 34
+V5_USB35 ○ ○ +V5_USB35 12
+V5A ○ ○ +V5A 37,40,44
+V5REF_ICH ○ ○ +V5REF_ICH 16
+V5REF_SUS_ICH ○ ○ +V5REF_SUS_ICH 16
+V5S ○ ○ +V5S 13,16,17,20,24,25,26,27,29,30,31,33,35,36,37,42,46
+V5S_FAN ○ ○ +V5S_FAN 35
+V5S_IDE ○ ○ +V5S_IDE 13,16,17,20,24,25,26,27,29,30,31,33,35,36,37,42,46
+V5S_MDC ○ ○ +V5S_MDC 13,16,17,20,24,25,26,27,29,30,31,33,35,36,37,42,46
+V5S_MPCI ○ ○ +V5S_MPCI 13,16,17,20,24,25,26,27,29,30,31,33,35,36,37,42,46
+V5S_TP ○ ○ +V5S_TP 36
+V5SUS ○ ○ +V5SUS 16,40
+V12 ○ ○ +V12 23,30,35,42
+V12S ○ ○ +V12S 12,13,31,42
+V2.5 ○ ○ +V2.5 6,9,10,39,40,46
+V5USB01 ○ ○ +V5USB01 34
+V5USB24 ○ ○ +V5USB24 34
+V_DCJACK ○ ○ +V_DCJACK 36
+V_RTC ○ ○ +V_RTC 15,16,17
+VAMP ○ ○ +VAMP 13,16,17,20,24,25,26,27,29,30,31,33,35,36,37,42,46
+VCCP ○ ○ +VCCP 3,4,7,9,16,40
+VCORE ○ ○ +VCORE 4,26,27,38
+VREF_SIO ○ ○ +VREF_SIO 27