1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MBP 15"MLB

08/18/2008

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7546	1	SCHEM,FIBBO,M98	SCH	CRITICAL	
820-2330	1	PCBF,FIBBO,M98	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Aug 18 01:48:34 2008

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

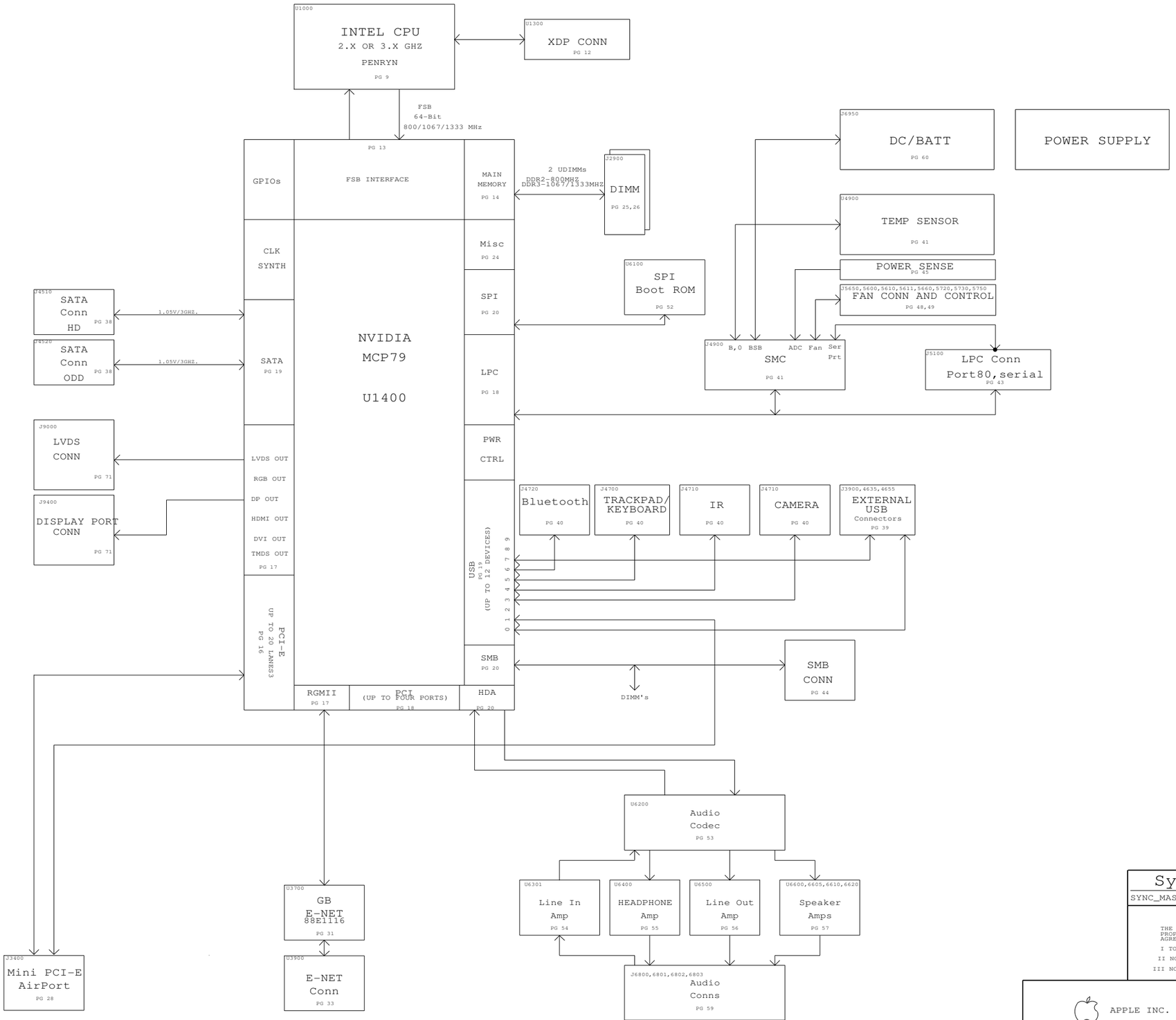
MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

APPLE INC.

TITLE
SCHEM,MBP 15MLB

DRAWING NUMBER 051-7546
REV. A.0.0
SHT 1 OF 96



System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT: 2 OF 96	

M98 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN(16.5V)
6A FUSE
LIO_DCIN_ISENSE
U5705
CHGR_EN (S5)
ENABLES
VIN
(PAGE 60)
VOUT
PBUS SUPPLY/ BATTERY CHARGER
ISL6258A U7000
D6905
D6905
PPVIN_G3H_P3V42G3H
PBUSB_VSENSE
Q5315
ENABLE 3.425V G3HOT LT3470 U6990 (PAGE 59)
PP3V42_G3H_REG
SMC PWRGD RN5VD30A-T U5000 (PAGE 43)
SMC_RESET_L
8A FUSE
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
SMC_GPU_VSENSE
U5498
GPU VCORE
VIN
VOUT
ISL6263B
EN_PSV
PGOOD
(PAGE 78)
GPUVCORE_IOUT
PPVCORE_GPU_REG
(18A MAX CURRENT)
PM_GPUVCORE_EN
GPUVCORE_PGOOD
CPUVTTS0_EN
VIN
EN_PSV
VOUT
1.05V
TPS51117 U7600 (PAG 66)
PGOOD
PPCPUVTT_S0_REG
(6A MAX CURRENT)
CPUVTTS0_PGOOD
U2830
VR_PWRGD_CLKEN
MCP79
CK_PWRGD
VRMPWRGD
PWRBTN#
PLTRST
PLT_RST_L
RSMRST#
MCP_PS_PWRGD
PWROK
CPUPWRGD(GPIO49)
CPU_PWRGD
U1400 (PAGE 14~22)
U2850
J6950
3S2P (9 TO 12.6V)
BATT_POS_F
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
U5715
SMC_BATT_ISENSE
U5400
SMC_CPU_VSENSE
PPVCORE_CPU_S0
CPU VCORE
VIN
VOUT
ISL9504B U7100
VR_ON
PGOOD
(PAGE 61)
CPUVCORE_IOUT
VR_PWRGD_CLKEN_L
IMVP_VR_ON_R
VR_PWRGOOD_DELAY
CPU PWRGOOD
U1000 (PAGE 10,11)
RESET*
PPBUS_G3H
Q7920
PP5V_S0_FET
P5VS0_SS
Q7900
PP5V_S3_FET
P5VS3_SS
MCP79
SLP_S5#(H17)
SLP_S3#(G17)
U1400 (PAGE 14~22)
P3V3S3_EN
P5VS3_EN
LIO_S3_EN
SMC
U4900
(PAGE 42)
P60(S5)
SMC_PM_G2_EN
U7859
P1V1GPU_EN
EN1 VIN VOUT1
1.103V(L/H)
PP1V1_S0GPU_REG
P1V8FB_EN
EN2 VOUT2
1.8V(R/H)
TPS51124 U9500 (PAGE 82)
PP1V8_GPU_REG
VIN
5V VOUT
(L/H)
PP5V_S5_REG
(8A MAX CURRENT)
3.3V VOUT
(R/H)
PP3V3_S5_REG
(5.5A MAX CURRENT)
TPS51125
EN0 U7201
(PAGE 62)
PGOOD1,2/VREG3
P3V3S5_EN
P5V3V3_S5_PGOOD
PP5V_S3
PP3V3_S5
PP1V05_S5_MCP
ISL8009 U7750 (PAGE 66)
V4
Q7910
PP3V3_S3_FET
P3V3S3_SS
Q7930
PP3V3_S0GPU_FET
P3V3S0_SS
Q7970
PP3V3_S0_FET
P3V3GPU_SS
Q3810
P3V3_ENET_FET
P3V3ENET_EN_L
U7400
VIN
EN/PSV
SC417 (PAGE 64)
ENL
VOUT
PGOOD
PP5V_RT_REG
P5V_RT_EN
P5V_RT_PGOOD
Q3805
WOW_EN
PM_WLAN_EN_L
Q3801
PM_ENET_EN
PM_ENET_EN_L
Q3800
WOL_EN
SMC_ADAPTER_EN
RC DELAY
PM_ENET_EN_L
BKLT_EN
VIN
GOSHAWK6P U9701
ENA
VOUT
(PAGE 84)
PPVOUT_S0_LCDBKLT
P1V2ENET_EN
ENETAVDD_EN
VINLTC3407
RUN2
RUN1
VOUT1
VOUT2
U3850 (PAGE 33)
PP1V9_ENET_REG
PP1V2_ENET_REG
PPVIN_S0_DDRREG_LDO
DDRREG_EN
DDRVTT_EN
VIN
VLDOIN
S5 1.8V
S3 0.9V
VOUT1
VOUT2
TPS51116 U7300 (PAGE 63)
PPDDR_S3_REG
(12A MAX CURRENT)
PPVTT_S0_DDR_LDO
PM_SLP_S3_L
RC DELAY
P5VRIGHT_EN
P1V8S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P5VS0_EN (S0)
P3V3S0_EN (S0)
PBUSVSENS_EN (S0)
PM_SLP_S3_DELAY_L (S0)
MCP_CORE
EN2
VOUT2
1.1V
EN1
VOUT1
ISL6236 U7500 (PAGE 65)
MCPCORES0_EN
MCPCPCORE_S0_REG
(25A MAX CURRENT)
P1V05S0_EN
PP5V_RT_REG
(5A MAX CURRENT)
SMC
RSMRST_OUT(P15)
PWRGD(P12)→99ms DLY
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PWR_BUTTON(P90)
P17(BTN_OUT)
RST
U4900 (PAGE 42)
PM_RSMRST_L
IMVP_VR_ON
PLT_RST
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
P1V05S0_PGOOD
P5VRIGHT_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P1V8S0_PGOOD
P1V5S0_PGOOD
S0PGOOD_PWROK
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
RST*
PP5V_S0
PP3V3_S0
PP1V5_S0_REG
V1
V2
V3
V4
LTC2900 U7870 (PAGE 68)

Power Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 3 OF 96	

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	4	96

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9334	PCBA,2.4GHZ,256SAM_VRAM,M98	M98_COMMON,EEE_0ZA,CPU_2_4GHZ,FB_256_SAMSUNG
630-9335	PCBA,2.4GHZ,256HYN_VRAM,M98	M98_COMMON,EEE_0ZB,CPU_2_4GHZ,FB_256_HYNIX
630-9336	PCBA,2.5GHZ,512SAM_VRAM,M98	M98_COMMON,EEE_0ZC,CPU_2_5GHZ,FB_512_SAMSUNG
630-9337	PCBA,2.5GHZ,512QIM_VRAM,M98	M98_COMMON,EEE_0ZD,CPU_2_5GHZ,FB_512_QIMONDA
630-9585	PCBA,2.8GHZ,512SAM_VRAM,M98	M98_COMMON,EEE_2NH,CPU_2_8GHZ,FB_512_SAMSUNG
630-9586	PCBA,2.8GHZ,512QIM_VRAM,M98	M98_COMMON,EEE_2NJ,CPU_2_8GHZ,FB_512_QIMONDA

M98 BOM Groups

BOM GROUP	BOM OPTIONS
M98_COMMON	ALTERNATE,COMMON,M98_COMMON1,M98_COMMON2,M98_COMMON3,M98_DEBUG,M98_PROGPARTS
M98_COMMON1	ONEWIRE_PU,ISL6258A,MEMRESET_HW,MEMRESET_MCP,MCP_B02,MCP_PROD,MCPSEQ_SMC
M98_COMMON2	BKLT_PLL_NOT,BMON_ENG,MIKEY,BOOT_MODE_USER,GPUVID_1P00V,MUXGFX
M98_COMMON3	DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_HW,DP_CA_DET_EG_PLD,MCP_CS1_NO
M98_DEBUG	SMC_DEBUG_YES,XDP,LPCPLUS,VREFMRGN
M98_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_QIMONDA	VRAM4,VRAM_512_QIMONDA

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZA]	CRITICAL	EEE_0ZA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZB]	CRITICAL	EEE_0ZB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZC]	CRITICAL	EEE_0ZC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZD]	CRITICAL	EEE_0ZD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2NH]	CRITICAL	EEE_2NH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2NJ]	CRITICAL	EEE_2NJ

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3639	1	IC,PDC,SLB4N,PRQ,2.4G,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3640	1	IC,PDC,SL3BX,PRQ,2.53G,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
338S0554	1	IC,GPU,55nm,NV G96-GS,BGA969,LF	U8000	CRITICAL	
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER,48P TQFP	U3700	CRITICAL	
338S0523	1	IC,FW643-06,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0600	1	IC,GMCP,MCP79-B01,35x35MM,BGA1437	U1400	CRITICAL	MCP_B01
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2289	1	IC,SMC,DEVELOPMENT,M98	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2366	1	IC,EFI ROM,DEVELOPMENT,M98	U6100	CRITICAL	BOOTROM_PROG
341S2272	1	IC,HDCP ROM,NVG96, 8 PIN SOIC,LF,HF	U8770	CRITICAL	HDCP_YES
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
338S0635	1	IC,GMCP,MCP79-B02,35x35MM,BGA1437	U1400	CRITICAL	MCP_B02
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3641	1	IC,PDC,SLB43,PRQ,2.8G,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_8GHZ
333S0482	4	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0481	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
353S1681	353S1294		ALL	LMV2011,DFAMP, GBW
152S0276	152S0683		ALL	Maglayers alt to Dale/Vishay
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0867		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
353S2312	353S1466		ALL	INTERSIL ALT TO INTERSIL
514-0612	514-0607		ALL	FOXLINK KCVR ALT TO FOXCONN
514-0613	514-0608		ALL	FOXLINK KCVR ALT TO FOXCONN
152S0915	152S0796		ALL	Maglayers alt to Cyntec IND

BOM Configuration

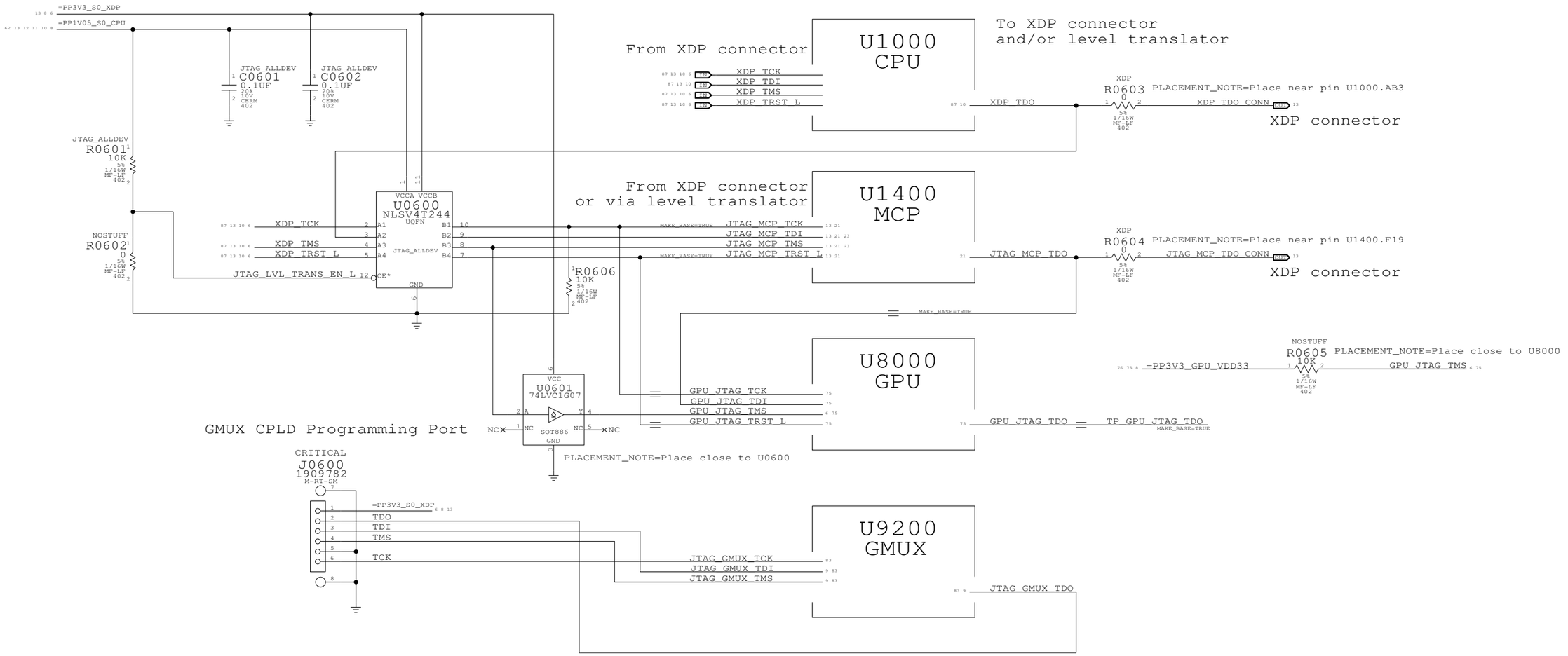
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	5	96

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 6 OF 96	

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	6 49	3 TPs per Fan
TRUE	FAN_LT_PWM	49	
TRUE	FAN_LT_TACH	49	
TRUE	FAN_RT_PWM	49	
TRUE	FAN_RT_TACH	49	5 TPs per Fan
TRUE	GND		

LVDS Connectors

FUNC_TEST

E561	TRUE	=PP3V3_S0_DDC_LCD	8 76 79
E562	TRUE	PP3V3_SW_LCD	79
E570	TRUE	BKL_SYNC	79 84
E571	TRUE	LVDS_DDC_CLK	79 80
E572	TRUE	LVDS_DDC_DATA	79 80
E577	TRUE	LVDS_CONN_A_DATA_N<0>	79 80 94
E566	TRUE	LVDS_CONN_A_DATA_P<0>	79 80 94
E574	TRUE	LVDS_CONN_A_DATA_N<1>	79 80 94
E565	TRUE	LVDS_CONN_A_DATA_P<1>	79 80 94
E573	TRUE	LVDS_CONN_A_DATA_N<2>	79 80 94
E575	TRUE	LVDS_CONN_A_DATA_P<2>	79 80 94
E567	TRUE	LVDS_CONN_A_CLK_F_N	79 94
E576	TRUE	LVDS_CONN_A_CLK_F_P	79 94
E579	TRUE	LVDS_CONN_B_DATA_N<0>	79 80 94
E581	TRUE	LVDS_CONN_B_DATA_P<0>	79 80 94
E583	TRUE	LVDS_CONN_B_DATA_N<1>	79 80 94
E582	TRUE	LVDS_CONN_B_DATA_P<1>	79 80 94
E580	TRUE	LVDS_CONN_B_DATA_N<2>	79 80 94
E588	TRUE	LVDS_CONN_B_DATA_P<2>	79 80 94
E584	TRUE	LVDS_CONN_B_CLK_F_N	79 94
E587	TRUE	LVDS_CONN_B_CLK_F_P	79 94
E591	TRUE	LED_RETURN_1	79 84
E590	TRUE	LED_RETURN_2	79 84
E597	TRUE	LED_RETURN_3	79 84
E598	TRUE	LED_RETURN_4	79 84
E599	TRUE	LED_RETURN_5	79 84
E592	TRUE	LED_RETURN_6	79 84

EXCARD Connector

FUNC_TEST

E641	TRUE	USB2_EXCARD_CONN_N	32 95
E642	TRUE	USB2_EXCARD_CONN_P	32 95
E643	TRUE	PCIE_CLK100M_EXCARD_CONN_N	32 95
E644	TRUE	PCIE_CLK100M_EXCARD_CONN_P	32 95
E649	TRUE	PCIE_EXCARD_R2D_N	32 89 95
E648	TRUE	PCIE_EXCARD_R2D_P	32 89 95
E647	TRUE	PCIE_EXCARD_D2R_P	17 32 89
E650	TRUE	PCIE_EXCARD_D2R_N	17 32 89
E646	TRUE	PP3V3_S3_EXCARD_SWITCH	32
E645	TRUE	PP3V3_S0_EXCARD_SWITCH	32
E651	TRUE	PP1V5_S0_EXCARD_SWITCH	32
E652	TRUE	PLT_RESET_SWITCH_L	32
E653	TRUE	EXCARD_CPPE_L	32
E655	TRUE	EXCARD_CPUSB_L	32
E654	TRUE	EXCARD_CLKREQ_CONN_L	32
E665	TRUE	SMBUS_MCP_0_CLK	13 21 45 90
E664	TRUE	SMBUS_MCP_0_DATA	13 21 45 90

Speaker Connectors

FUNC_TEST

E555	TRUE	BI_MIC_LO	58 59
E553	TRUE	BI_MIC_SHIELD	58 59
E556	TRUE	BI_MIC_HI	58 59
E560	TRUE	SPKRCONN_L_P_OUT	57 58 95
E558	TRUE	SPKRCONN_L_N_OUT	57 58 95
E554	TRUE	SPKRCONN_R_P_OUT	57 58 95
E559	TRUE	SPKRCONN_R_N_OUT	57 58 95
E557	TRUE	SPKRCONN_S_P_OUT	57 58 95
E561	TRUE	SPKRCONN_S_N_OUT	57 58 95
	TRUE	GND	6 TPs

SATA ODD Connectors

FUNC_TEST

E595	TRUE	PP5V_SW_ODD	39 4 TPs
E535	TRUE	SMC_ODD_DETECT	39 42
E539	TRUE	SATA_ODD_R2D_P	39 89
E537	TRUE	SATA_ODD_R2D_N	39 89
E532	TRUE	SATA_ODD_D2R_C_N	39 89
E592	TRUE	SATA_ODD_D2R_C_P	39 89
	TRUE	GND	5 TPs

POWER RAILS

E600	TRUE	PM_SLP_S3_L	21 34 37 42 44 68 81 83
E600	TRUE	PPBUS_G3H	8 46
E600	TRUE	PPBUS_CPU_IMVP_ISNS	8
E600	TRUE	PP3V42_G3H	7 8 43
E600	TRUE	PP5V_S3	8
E600	TRUE	PP5V_S0	8
E600	TRUE	PPVCORE_S0_CPU	8
E600	TRUE	PPVCORE_S0_MCP_REG	8
E600	TRUE	PPVCORE_S0_MCP	
E600	TRUE	PP3V3_S5	8 95
E600	TRUE	PP3V3_S3	8
E600	TRUE	PP3V3_S0	8 95
E600	TRUE	PP2V5_S0	8
E600	TRUE	PP1V2_S0	8
E600	TRUE	PP1V8_S0	8
E600	TRUE	PP1V8R1V5_S3	8
E600	TRUE	PP1V8R1V5_S0_FET	8
E600	TRUE	PPMCPDDR_ISNS	8
E600	TRUE	PP1V05_S0_REG	8
E600	TRUE	PP1V2R1V05_S5	8
E600	TRUE	PPCPUVTT_S0	8
E600	TRUE	PPCPUFSB_ISNS_R	
E600	TRUE	PP0V9R0V75_S0_DDRVTT	8
E600	TRUE	PP1V2R1V05_ENET	8
E600	TRUE	PP3V3_ENET_PHY	8
E600	TRUE	PPVP_FW	8
E600	TRUE	PP1V0_FW	8
E600	TRUE	PP3V3_S0GPU	8
E600	TRUE	PP1V1_S0GPU_REG	8
E600	TRUE	PP1V8_S0GPU_ISNS	8
E600	TRUE	PPVCORE_GPU	8
E600	TRUE	PP1V8_S0GPU_ISNS_R	8
E600	TRUE	PP3V3_S5_AVREF_SMC	42 43
E600	TRUE	PPVOUT_S0_LCDBKLT	79 84
E600	TRUE	PPDCIN_G3H	8
E600	TRUE	PPVTTDDR_S3	8
E600	TRUE	PP1V8_GPUIFPX	8

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 87
TRUE	FSB_ADS_L	10 14 87
TRUE	FSB_ADSTB_L<1..0>	10 14 87
TRUE	FSB_D_L<63..0>	10 14 87
TRUE	FSB_DINV_L<3..0>	10 14 87
TRUE	FSB_DSTB_L_N<3..0>	10 14 87
TRUE	FSB_DSTB_L_P<3..0>	10 14 87
TRUE	FSB_HIT_L	10 14 87
TRUE	FSB_HITM_L	10 14 87
TRUE	FSB_LOCK_L	10 14 87
TRUE	FSB_REQ_L<4..0>	10 14 87

IPD_FLEX_CONN

E725	TRUE	PP3V3_S3_LDO	51
E750	TRUE	PP18V5_S3	51
E755	TRUE	TPAD_GND_F	7 51
E750	TRUE	Z2_CS_L	50 51
E735	TRUE	Z2_DEBUG3	50 51
E735	TRUE	Z2_MOST	50 51
E735	TRUE	Z2_MISO	50 51
E735	TRUE	Z2_SCLK	50 51
E735	TRUE	Z2_BOOST_EN	51
E745	TRUE	Z2_HOST_INTN	50 51
E750	TRUE	Z2_BOOT_CFG1	50 51
E745	TRUE	Z2_CLKIN	50 51
E740	TRUE	Z2_KEY_ACT_L	50 51
E745	TRUE	Z2_RESET	50 51
E745	TRUE	PSOC_MISO	50 51
E744	TRUE	PSOC_MOSI	50 51
E745	TRUE	PSOC_SCLK	50 51
E745	TRUE	SMBUS_SMC_A_S3_SDA	45 93
E742	TRUE	SMBUS_SMC_A_S3_SCL	45 93
E740	TRUE	PSOC_F_CS_L	50 51
E735	TRUE	PICKB_L	50 51

KEYBOARD CONN

E710	TRUE	PP3V42_G3H	7 8 43
E725	TRUE	WS_KBD1	50
E735	TRUE	WS_KBD2	50
E735	TRUE	WS_KBD3	50
E735	TRUE	WS_KBD4	50
E733	TRUE	WS_KBD5	50
E733	TRUE	WS_KBD6	50
E730	TRUE	WS_KBD7	50
E730	TRUE	WS_KBD8	50
E729	TRUE	WS_KBD9	50
E729	TRUE	WS_KBD10	50
E729	TRUE	WS_KBD11	50
E729	TRUE	WS_KBD12	50
E729	TRUE	WS_KBD13	50
E729	TRUE	WS_KBD14	50
E729	TRUE	WS_KBD15_CAP	50
E725	TRUE	WS_KBD16_NUM	50
E725	TRUE	WS_KBD17	50
E715	TRUE	WS_KBD18	50
E715	TRUE	WS_KBD19	50
E715	TRUE	WS_KBD20	50
E715	TRUE	WS_KBD21	50
E715	TRUE	WS_KBD22	50
E715	TRUE	WS_KBD23	50
E715	TRUE	WS_KBD_ONOFF_L	50
E715	TRUE	WS_LEFT_SHIFT_KBD	50
E715	TRUE	WS_LEFT_OPTION_KBD	50
E715	TRUE	WS_CONTROL_KBD	50
E710	TRUE	KBDLED_ANODE	51
E760	TRUE	TPAD_GND_F	7 51

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE D | DRAWING NUMBER 051-7546 | REV. A.0.0

SCALE NONE | SHT 7 OF 96

"G3Hot" (Always-Present) Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3
=PPVIN_S0_CPUVTTS0
=PPBUS_S0_LCDBKLT
=PPBUS_S5_FWPWRSW
=PPVIN_GPU_GPUVCORE
=PPVIN_S5_CPU_IMVP_ISNS_R
=PPVIN_S0_P5VRTS0_MCPCORE
=PPVIN_S3_DDRREG
=PPVIN_S0GPU_P1V8P1V1
=PPVBAT_G3H_P3V42G3H
=PPVIN_S0_P1V05S5

=PPVIN_S5_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S5_CPU_IMVP

=PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_LIDSWITCH
=PP3V3_S5_SMC
=PP3V3_S5_LPCPLUS
=PPVIN_S5_SMCVREF
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_CHGR
=PP3V3_S5_RTC_D
=PP3V42_G3H_BATT
=PP3V42_G3H_TPAD
=PP3V42_G3H_BMON_ISNS
=PP3V42_G3H_CPUCOREISNS

5V Rails

=PP5V_S3_REG
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_SYSLED
=PP5V_S3_BTCAMERA
=PP5V_S3_WLAN
=PP5V_S3_IR
=PP5V_S3_DDRREG
=PP5V_S3_GPUVCORE
=PP5V_S3_RTUSB
=PP5V_S3_TPAD
=PP5V_S3_P1V05S0FET
=PP5V_S3_MCPDDRFET
=PP5V_S3_VTTCLAMP
=PP5V_S3_AUDIO_PWR

=PP5V_RT_REG
PP5V_S0
MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_CPU_IMVP
=PP5V_S0_CPUVTTS0
=PP5V_S0_KBDLED
=PP5V_S0GPU_P1V1P1V8_GPU
=PP5V_S0_LPCPLUS
=PP5V_S0_ODD
=PP5V_S0_HDD

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU

=PPMCPCORE_S0_REG
PPVCORE_S0_MCP_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP

3.3V-2.5V Rails

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_A01
=PP3V3_S5_ROM
=PP3V3_S5_MEMRESET
=PP3V3_S3_P3V3S3FET
=PP3V3_S5_LCD
=PP3V3_S0_P3V3S0FET
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S5_PWRCTL
=PP3V3_S5_P1V05FET
=PP3V3_S5_MCP
=PP3V3_S5_MCP_GPIO
=PP3V3_FW_LATEVG_ACTIVE
=PP3V3_S5_MCPPWRGD
=PP3V3_FW_LATEVG
=PP3V3_S5_P1V05ENETFET
=PP3V3_S5_P3V3ENETFET
=PP3V3_S5_DP_PORT_PWR

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_FW_REG
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_SMS
=PP3V3_S3_REMTHMSNS
=PP3V3_S3_TPAD
=PP3V3_S3_WLAN
=PP3V3_S3_MCP_GPIO
=PP3V3_S3_VREFMRGN
=PP3V3_S3_SMBUS_SMC_MGMT
=PP3V3_S3_EXCARD
=PP3V3_S3_P1V8S0

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_LPCPLUS
=PP3V3_S0_SMC
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_MCPDDRISNS
=PP3V3_S0_GPU1V8ISNS
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_IMVP
=PP3V3_S0_PWRCTL
=PP3V3_S0_DDC_LCD
=PP3V3_S0_XDP
=PP3V3_S0_MCPCOREISNS
=PPSPD_S0_MEM_A
=PPSPD_S0_MEM_B
=PP3V3_S0_SMBUS_MCP_0
=PP3V3_S0_GMUX
=PP3V3_S0_DPMUX
=PP3V3_S0_DPCONN
=PP3V3_S0_P1V2P2V5
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_HDCPROM
=PP3V3R1V5_S0_MCP_HDA
=PP3V3_S0_MCP_PLL_UF
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_MCP_DAC_UF
=PP3V3_S0_MCP
=PP3V3_S0_AUDIO
=PP3V3_S0_ODD
=PP3V3_S0_VMON
=PP3V3_S0_SMBUS_MCP_1
=PP3V3_FC_CON
=PP3V3_S0_EXCARD
=PP3V3_S0_LVDSDDCMUX
=PP3V3_S0_BATTCHARGERTMPSNSR
=PP3V3_GPU_SMBUS_SMC_0_S0
=PP3V3_S0_TPAD

=PP2V5_S0_REG
PP2V5_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE
=PP2V5_S0_GMUX

=PP1V2_S0_REG
PP1V2_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PP1V2_S0_GMUX

1.8V/DDR 1.5V Rails

=PP1V8_S0_REG
PP1V8_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
500 mA max supply
190 mA =PP3V3R1V8_S0_MCP_IFP_VDD

=PPDDR_S3_REG
PP1V8R1V5_S3
MIN_LINE_WIDTH=0.8 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_MCP_FET
=PPVIN_S0_DDRREG_LDO
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B
=PP1V5_S3_MEMRESET

=PP1V8R1V5_S0_FET
PP1V8R1V5_S0_FET
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
4771 mA =PPMCPDDR_ISNS_R
130 mA =PP1V5_S0_CPU
500 mA =PP1V5_S0_EXCARD
=PP1V5_S0_VMON
=PP1V5_FC_CON

=PP1V8R1V5_S0_MCP_MEM
PPMCPDDR_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_MEM_A
=PP1V5_S0_MEM_B
=PPMCPDDR_ISNS

=PP1V05_S0_FET
PP1V05_S0_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
1034 mA
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_HDMI_VDD
=PP1V05_S0_VMON

=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PEX_DVDD0
=PP1V05_S0_MCP_PEX_DVDD1

PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PEX_AVDD0
=PP1V05_S0_MCP_PEX_AVDD1

=PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_SATA_DVDD0

PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_SATA_AVDD0

=PP1V05_S5_MCP
PP1V2R1V05_S5 (1.1V for A01)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
241 mA max load
105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC
139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET
=PP1V05_S5_P1V05S0FET

=PPCPUVTT_S0_REG
PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
5300 mA
4500 mA =PP1V05_S0_CPU
=PP1V05_S0_SMC_LS
1182 mA =PP1V05_S0_MCP_FSB

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PP0V9R0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP
OR 0.75V

ENET Rails

=PP1V05_ENET_FET
PP1V2R1V05_ENET
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC
=PP1V05_ENET_MCP_RMGT
=PP1V05_ENET_PHY

=PP3V3_ENET_FET
PP3V3_ENET_PHY
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT
=PP3V3_ENET_PHY

"FW" (FireWire) Rails

=PPBUS_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVP_FW_PORT1
=PPVP_FW_PHY_CPS_FET

=PP3V3_FW_REG
=PP3V3_FW_FWPHY
=PP3V3_FW_P1V0FW

=PP1V0_FW_REG
PP1V0_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.00V
MAKE_BASE=TRUE
=PP1V0_FW_FWPHY

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_VDD33
=PP3V3_GPU_MIO
=PP3V3_GPU_LVDS_DDC
=PP3V3_GPU_PWRCTL
=PP3V3_GPU_VCORELOGIC
=PP3V3_GPU_P1V8S0

=PP1V1_S0GPU_REG
PP1V1_S0GPU_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE
=PP1V1_GPU_PEX_IOVDDQ
=PP1V1_GPU_PEX_IOVDD
=PP1V1_GPU_PEX_PLLXVDD
=PP1V1_GPU_PLLVDD
=PP1V1_GPU_H_PLLVDD
=PP1V1_GPU_VID_PLLVDD
=PP1V1_GPU_FBPLLAVDD
=PP1V1_GPU_IFPCD_IOVDD

=PP1V8_GPUIFPX_REG
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_IFPX

=PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_FB_VDD
=PP1V8_GPU_FB_VDDQ
=PP1V8_GPU_FBVDDQ
=PP1V8_GPU_FBIO

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PPVCORE_GPU

=PP1V8_GPU_REG
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V8_S0GPU_ISNS_R

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE D | DRAWING NUMBER 051-7546 | REV. A.0.0

SCALE NONE | SHT 8 OF 96

Thermal Module Holes

ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0983 STDOFF-4.5OD.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
Bottom Left GPU TM Hole
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98

Frame Holes

ZT0915 3R2P5 — 61 60 GND_BATT_CHGND
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0950 TH — GND_CHASSIS_FAN
SL-3.1X2.7-6CIR-NSP
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0990 3R2P5 — GND_CHASSIS_BATTCONN

=PP1V8_GPU_FB_VDDC — R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV — =PP1V8_GPU_FB_VREF_A 73
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV — =PP1V8_GPU_FB_VREF_B 74

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

24 22 14 8 =PP1V05_S0_MCP_FSB

NO STUFF R0950 220 5% 1/16W MF-LF 402	NO STUFF R0970 200 5% 1/16W MF-LF 402	NO STUFF R0990 150 1% 1/16W MF-LF 402
	NO STUFF R0960 62 5% 1/16W MF-LF 402	NO STUFF R0980 150 1% 1/16W MF-LF 402

87 62 14 10 CPU_DPRSTP_L
87 14 10 FSB_BREQ0_L
87 14 13 10 FSB_CPURST_L
87 14 10 CPU_INTR
87 14 10 CPU_NMI

Bosses for VRAM HS

ZT0951 4.0OD1.65H-M1.6X0.35
ZT0952 4.0OD1.65H-M1.6X0.35
ZT0953 4.0OD1.65H-M1.6X0.35

ZT0931 STDOFF-4.0OD3.0H-TH — VENICE
ZT0934 STDOFF-4.0OD3.0H-TH
ZT0932 STDOFF-4.0OD3.0H-TH — VENICE
ZT0935 STDOFF-4.0OD3.0H-TH
ZT0933 STDOFF-4.0OD3.0H-TH — VENICE

ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

9 NC_LVDS_B_DATAP<3> — LVDS_B_DATA_P<3>
9 NC_LVDS_B_DATAN<3> — LVDS_B_DATA_N<3>
9 NC_LVDS_A_DATAP<3> — LVDS_A_DATA_P<3>
9 NC_LVDS_A_DATAN<3> — LVDS_A_DATA_N<3>
(MAKE_BASE=TRUE, NO_TEST=TRUE)

TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P 18 89
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N 18 89
TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM 18
(MAKE_BASE=TRUE)

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3> 18 89
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3> 18 89
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3> 18 89
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3> 18 89
9 NC_LVDS_A_DATAP<3> — LVDS_A_DATA_P<3>
9 NC_LVDS_A_DATAN<3> — LVDS_A_DATA_N<3>
9 NC_LVDS_B_DATAP<3> — LVDS_B_DATA_P<3>
9 NC_LVDS_B_DATAN<3> — LVDS_B_DATA_N<3>
(MAKE_BASE=TRUE)

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L 62
87 11 CPU_VID<0..6> — IMVP6_VID<0..6> 62 87
87 10 CPU_BSEL<0..2> — =MCP_BSEL<0..2> 14
26 MEM_VTT_EN — =DDRVTT_EN 64 69
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB 21 44
(MAKE_BASE=TRUE)

GPU signals

89 70 PEG_D2R_P<0..15> — =PEG_D2R_P<0..15> 17
89 70 PEG_D2R_N<0..15> — =PEG_D2R_N<0..15> 17
89 70 PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15> 17
89 70 PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15> 17
(MAKE_BASE=TRUE)

95 32 PCIE_CLK100M_FC_P — TP_PCIE_CLK100M_PE4P 17
95 32 PCIE_CLK100M_FC_N — TP_PCIE_CLK100M_PE4N 17
95 32 PCIE_FC_R2D_C_P — TP_PCIE_PE4_R2D_CP 17
95 32 PCIE_FC_R2D_C_N — TP_PCIE_PE4_R2D_CN 17
32 FC_CLKREQ_L — TP_PE4_CLKREQ_L 17
32 FC_PRSNT_L — TP_PE4_PRSNT_L 17
95 32 PCIE_FC_D2R_P — TP_PCIE_PE4_D2RP 17
95 32 PCIE_FC_D2R_N — TP_PCIE_PE4_D2RN 17
(MAKE_BASE=TRUE)

GMUX ALIASES

83 LCD_BKLT_EN — LVDS_BKL_ON 85
89 80 DP_IG_ML_P<3> — =MCP_HDMI_TXC_P 18
89 80 DP_IG_ML_N<3> — =MCP_HDMI_TXC_N 18
89 80 DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2> 18
89 80 DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2> 18
80 76 DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK 18
80 76 DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA 18
DP_IG_HPD — =MCP_HDMI_HPD 18
68 PM_ALL_GPU_PGOOD — ALL_EG_PGOOD 83
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG 83
83 EG_RESET_L — GPU_RESET_L 70
(MAKE_BASE=TRUE)

83 6 JTAG_GMUX_TDI — GMUX_JTAG_TDI 19
83 6 JTAG_GMUX_TMS — GMUX_JTAG_TMS 19
83 6 JTAG_GMUX_TDO — GMUX_JTAG_TDO 17
18 LVDS_IG_BKL_ON — IG_BKLT_EN 83
18 LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN 83
(MAKE_BASE=TRUE)

TP_USB_EXTDP — USB_EXTD_P 20 90
TP_USB_EXTDN — USB_EXTD_N 20 90
TP_USB_MINIP — USB_MINI_P 20 90
TP_USB_MININ — USB_MINI_N 20 90
(MAKE_BASE=TRUE)

83 GMUX_INT — =DVI_HPD_GMUX_INT 18
(MAKE_BASE=TRUE)

R0903 0 5% 1/16W MF-LF 402
21 MCP_SPKR — SMC_MCP_SAFE_MODE 42

TP_MEM_A_A<15> — MEM_A_A<15> 28
TP_MEM_B_A<15> — MEM_B_A<15> 29
TP_USB_EXTCP — USB_EXTC_P 20 90
TP_USB_EXTCN — USB_EXTC_N 20 90
TP_CPU_PECI_MCP — CPU_PECI_MCP 14
TP_MCP_GPIO_17 — AUD_IP_PERIPHERAL_DET 17
(MAKE_BASE=TRUE)

26 17 PCIE_RESET_L — FC_RESET_L 32
(MAKE_BASE=TRUE)

AUDIO ALIASES

94 HDA_BITCLK — HDA_BIT_CLK 21 90
(MAKE_BASE=TRUE)

XW0900 SM
8 =PP5V_S3_AUDIO_PWR — 2 1 — PP5V_S3_AUDIO 54 56
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
XW0901 SM
2 1 — PP5V_S3_AUDIO_AMP 57
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

R0902 10K 5% 1/16W MF-LF 402
1 2 — AUD_IPHS_SWITCH_EN 19 59
MAKE_BASE=TRUE

ETHERNET ALIASES

34 =P3V3ENET_EN — PM_SLP_RMGT_L 21
34 =P1V05ENET_EN
33 =PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
33 =RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG 93
(MAKE_BASE=TRUE)

MCP79 PCIe PRSNT# Straps

These need work. Add other PRSNT# straps if needed. .

=PP1V05_S0_MCP_SATA_DVDD1 20
=PP1V05_S0_MCP_SATA_AVDD1 20

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L — OUT 17
R0927 0 5% 1/16W MF-LF 402 — NO STUFF — PEG_PRSNT_L — OUT 17
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L — IN 83
(MAKE_BASE=TRUE)

MCP_MII_PD — R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER 18
=MCP_MII_CRS 18
=MCP_MII_COL 18
(MAKE_BASE=TRUE)

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.09MM VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 9 OF 96	

OMIT

U1000
PENRYN
FCBGA
1 OF 4

ADDR GROUP0
FSB_A_L<3> J4 A3*
FSB_A_L<4> L5 A4*
FSB_A_L<5> L4 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M3 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L2 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> M1 ADSTB0*

REQ0 K3 FSB_REQ_L<0>
REQ1 H2 FSB_REQ_L<1>
REQ2 K2 FSB_REQ_L<2>
REQ3 J3 FSB_REQ_L<3>
REQ4 L1 FSB_REQ_L<4>

ADDR GROUP1
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U1 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W2 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> U2 A30*
FSB_A_L<31> V4 A31*
FSB_A_L<32> W3 A32*
FSB_A_L<33> AA4 A33*
FSB_A_L<34> AB2 A34*
FSB_A_L<35> AA3 A35*
FSB_ADSTB_L<1> V1 ADSTB1*

ICH
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED
TP_CPU_RSVD0 M4 RSVD0
TP_CPU_RSVD1 N5 RSVD1
TP_CPU_RSVD2 T2 RSVD2
TP_CPU_RSVD3 V3 RSVD3
TP_CPU_RSVD4 B2 RSVD4
TP_CPU_RSVD5 F6 RSVD5
TP_CPU_RSVD6 D2 RSVD6
TP_CPU_RSVD7 D22 RSVD7
TP_CPU_RSVD8 D3 RSVD8

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* E3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

=PP1V05_S0_CPU
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> G22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H22 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H23 D15*
FSB_DSTB_L_N<0> J26 DSTBN0*
FSB_DSTB_L_P<0> H26 DSTBP0*
FSB_DINV_L<0> H25 DINV0*

DATA GRP 1
FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L23 D20*
FSB_D_L<21> M24 D21*
FSB_D_L<22> L22 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P23 D25*
FSB_D_L<26> P22 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L25 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N25 D31*
FSB_DSTB_L_N<1> L26 DSTBN1*
FSB_DSTB_L_P<1> M26 DSTBP1*
FSB_DINV_L<1> N24 DINV1*

DATA GRP 2
D32* Y22 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* V23 FSB_D_L<36>
D37* T22 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U23 FSB_D_L<39>
D40* Y25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* W24 FSB_D_L<43>
D44* W25 FSB_D_L<44>
D45* AA23 FSB_D_L<45>
D46* AA24 FSB_D_L<46>
D47* AB25 FSB_D_L<47>
DSTBN2* Y26 FSB_DSTB_L_N<2>
DSTBP2* AA26 FSB_DSTB_L_P<2>
DINV2* U22 FSB_DINV_L<2>

DATA GRP 3
D48* AE24 FSB_D_L<48>
D49* AD24 FSB_D_L<49>
D50* AA21 FSB_D_L<50>
D51* AB22 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC26 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AC25 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AC22 FSB_D_L<60>
D61* AD23 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AC23 FSB_D_L<63>
DSTBN3* AE25 FSB_DSTB_L_N<3>
DSTBP3* AF24 FSB_DSTB_L_P<3>
DINV3* AC20 FSB_DINV_L<3>

MISC
GTLREF AD26 0.5" MAX LENGTH FOR CPU_GTLREF
TEST1 C23 CPU_TEST1
TEST2 D25 CPU_TEST2
TEST3 C24 TP_CPU_TEST3
TEST4 AF26 CPU_TEST4
TEST5 AF1 TP_CPU_TEST5
TEST6 A26 TP_CPU_TEST6
TEST7 C3 TP_CPU_TEST7
BSEL0 B22 CPU_BSEL<0>
BSEL1 B23 CPU_BSEL<1>
BSEL2 C21 CPU_BSEL<2>
COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L

=PP1V05_S0_CPU
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

R1020 54.9 1% 1/16W MF-LF 402 =PP1V05_S0_CPU
R1021 54.9 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
XDP_TMS
XDP_TDI
XDP_TDO
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
XDP_TCK
XDP_TRST_L

CPU FSB

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 10 OF 96	

(CPU CORE POWER)

=PPVCORE_S0_CPU 8 11 12 46

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
3 OF 4

VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 6 8 10 12 13 62

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26 C26

VID0	AD6	CPU_VID<0>	9 87
VID1	AF5	CPU_VID<1>	9 87
VID2	AE5	CPU_VID<2>	9 87
VID3	AF4	CPU_VID<3>	9 87
VID4	AE3	CPU_VID<4>	9 87
VID5	AF3	CPU_VID<5>	9 87
VID6	AE2	CPU_VID<6>	9 87
VCCSENSE	AF7	CPU_VCCSENSE_P	62 87
VSSSENSE	AE7	CPU_VCCSENSE_N	62 87

=PPVCORE_S0_CPU 8 11 12 46

R1100
100
1%
1/16W
ME-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
ME-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
4 OF 4

VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3 B1

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

CPU Power & Ground

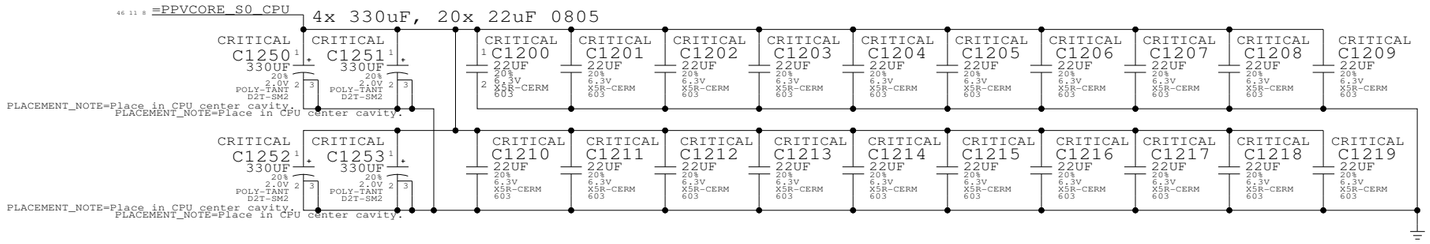
SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

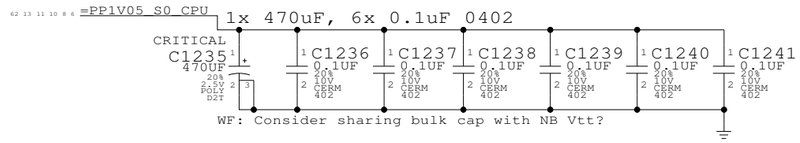
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 11 OF 96	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

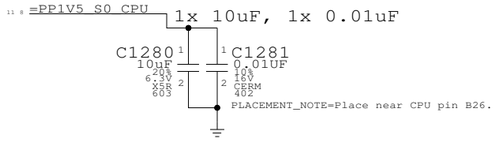
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

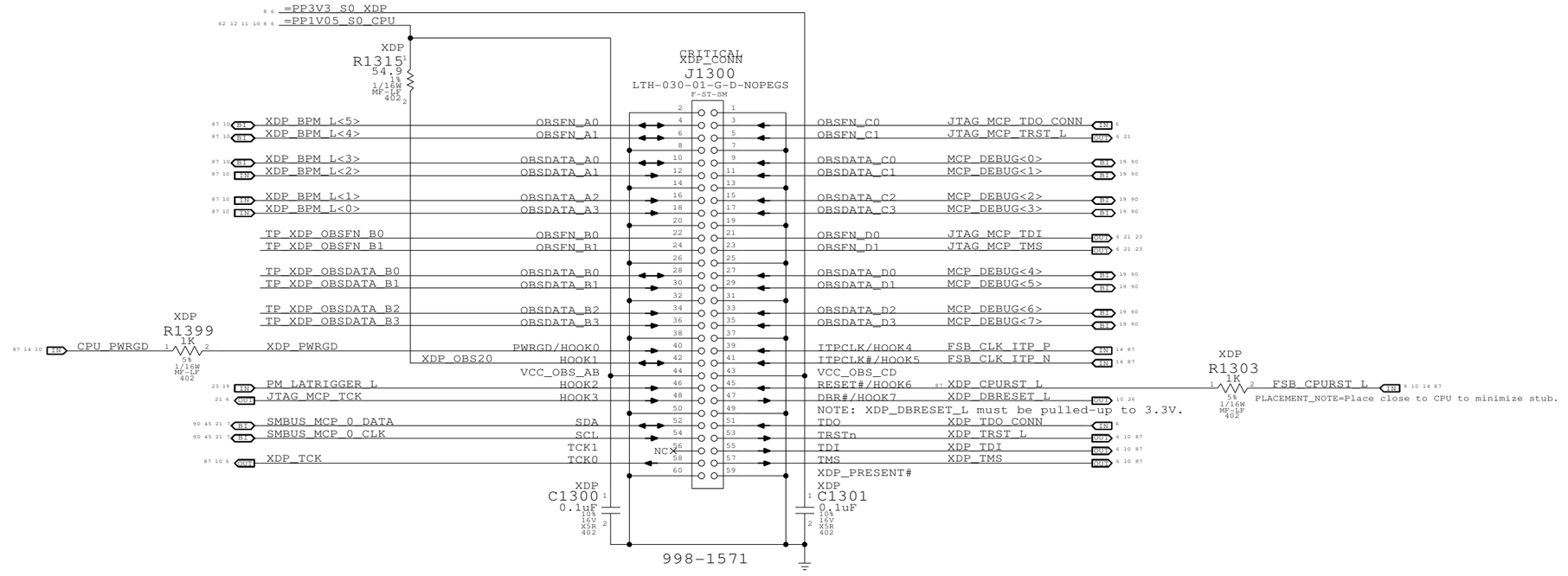
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 12 OF 96	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 13 OF 96	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
PP1V05_S0_MCP_PLL_FSB			
270 mA (A01)	206 mA	AG27	+V_DLL_DLCELL_AVDD
	20 mA	AH27	+V_PLL_MCLK
	29 mA	AG28	+V_PLL_FSB
	15 mA	AH28	+V_PLL_CPU
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	H40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	H41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	H43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
CPU_D61#	J40	FSB_D_L<61>	
CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	H38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

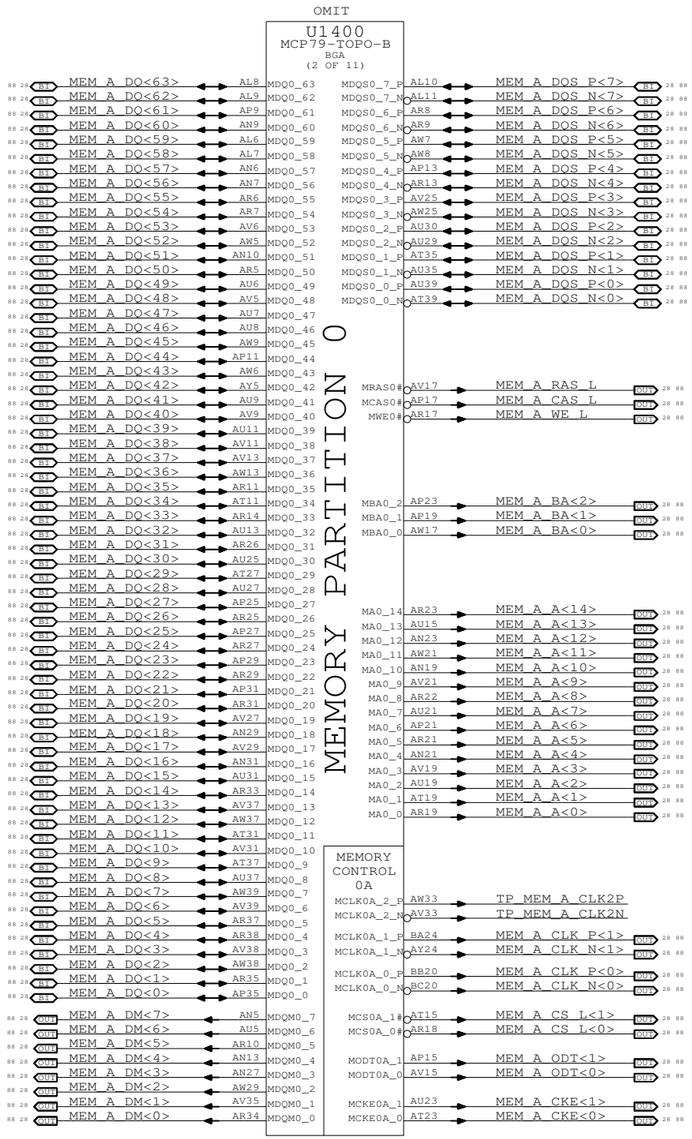
MCP CPU Interface

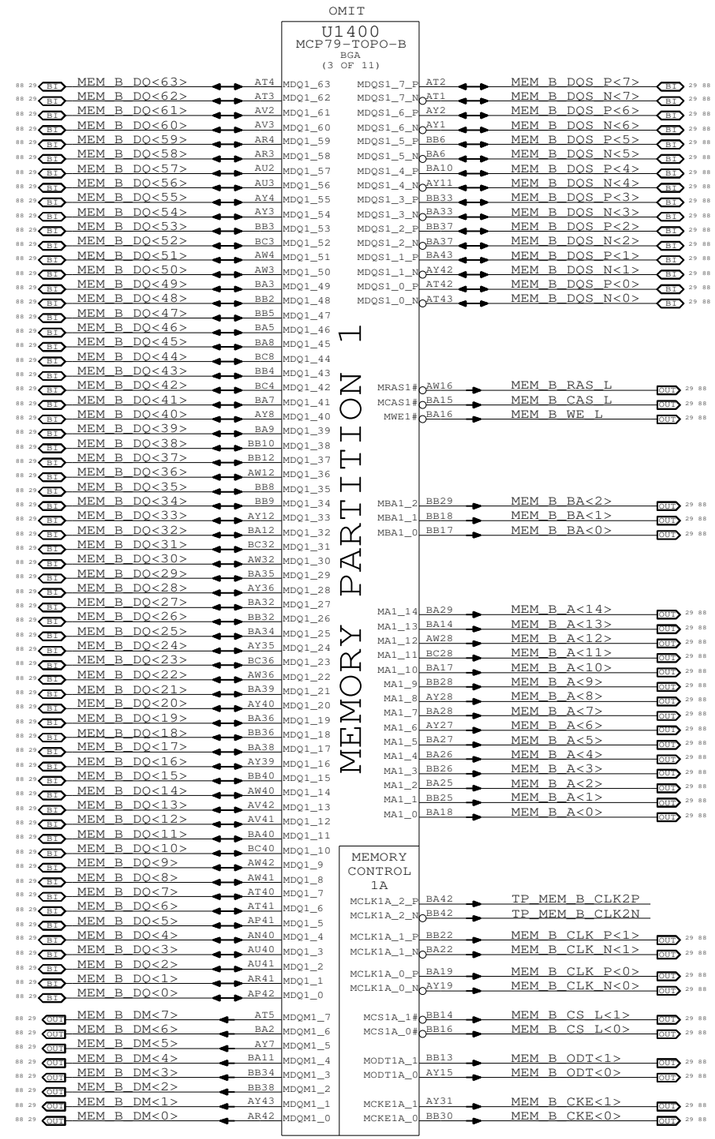
SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 14 OF 96	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).





MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 15 OF 96	

OMIT

U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
TP_MEM_A_CLK5N	AU34	MCLK0B_2_N	
TP_MEM_A_CLK4P	BB24	MCLK0B_1_P	
TP_MEM_A_CLK4N	BC22	MCLK0B_1_N	
TP_MEM_A_CLK3P	BA21	MCLK0B_0_P	
TP_MEM_A_CLK3N	BB21	MCLK0B_0_N	
TP_MEM_A_CS_L<2>	AU17	MCS0B_0#	
TP_MEM_A_CS_L<3>	AR17	MCS0B_1#	
TP_MEM_A_ODT<2>	AN17	MODT0B_0	
TP_MEM_A_ODT<3>	AN15	MODT0B_1	
TP_MEM_A_CKE<2>	AV23	MCKE0B_0	
TP_MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

		MCLK1B_2_P	BA41
		MCLK1B_2_N	BB41
		MCLK1B_1_P	AY23
		MCLK1B_1_N	BA23
		MCLK1B_0_P	BA20
		MCLK1B_0_N	AY20
		MCS1B_0#	BC16
		MCS1B_1#	BA13
		MODT1B_0	AY16
		MODT1B_1	BC13
		MCKE1B_0	BA30
		MCKE1B_1	BA31

TP_MEM_B_CLK5P			
TP_MEM_B_CLK5N			
TP_MEM_B_CLK4P			
TP_MEM_B_CLK4N			
TP_MEM_B_CLK3P			
TP_MEM_B_CLK3N			
TP_MEM_B_CS_L<2>			
TP_MEM_B_CS_L<3>			
TP_MEM_B_ODT<2>			
TP_MEM_B_ODT<3>			
TP_MEM_B_CKE<2>			
TP_MEM_B_CKE<3>			

24 16 8 =PP1V8R1V5_S0_MCP_MEM

R1610[1] 40.2 1% 1/16W MF-LF 402 2

R1611[1] 40.2 1% 1/16W MF-LF 402 2

24 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS
12 mA	U28	+V_PLL_DP
19 mA	U27	+V_PLL_CORE
39 mA	T28	+V_VPLL

88 MCP_MEM_COMP_VDD AN41 MEM_COMP_VDD
88 MCP_MEM_COMP_GND AM41 MEM_COMP_GND

MRESET0# AY32 → MCP_MEM_RESET_L (ONLY) 30
TP or NC for DDR2.

=PP1V8R1V5_S0_MCP_MEM 8 16 24
4771 mA (A01, DDR3)

		+VDD_MEM1	AM17
		+VDD_MEM2	AM19
		+VDD_MEM3	AM21
		+VDD_MEM4	AM23
		+VDD_MEM5	AM25
		+VDD_MEM6	AM27
		+VDD_MEM7	AM29
		+VDD_MEM8	AN16
		+VDD_MEM9	BC29
		+VDD_MEM10	AN20
		+VDD_MEM11	AN24
		+VDD_MEM12	AT17
		+VDD_MEM13	AP16
		+VDD_MEM14	AN22
		+VDD_MEM15	AP20
		+VDD_MEM16	AP24
		+VDD_MEM17	AV16
		+VDD_MEM18	AR16
		+VDD_MEM19	AR20
		+VDD_MEM20	AR24
		+VDD_MEM21	AW15
		+VDD_MEM22	AP22
		+VDD_MEM23	AP18
		+VDD_MEM24	AU16
		+VDD_MEM25	AN18
		+VDD_MEM26	AU24
		+VDD_MEM27	AT21
		+VDD_MEM28	AY29
		+VDD_MEM29	AV24
		+VDD_MEM30	AU20
		+VDD_MEM31	AU22
		+VDD_MEM32	AW27
		+VDD_MEM33	BC17
		+VDD_MEM34	AV20
		+VDD_MEM35	AY17
		+VDD_MEM36	AY18
		+VDD_MEM37	AM15
		+VDD_MEM38	AU18
		+VDD_MEM39	AY25
		+VDD_MEM40	AY26
		+VDD_MEM41	AW19
		+VDD_MEM42	AW24
		+VDD_MEM43	BC25
		+VDD_MEM44	AL30
		+VDD_MEM45	AM31

AA22	GND1	GND55	T33
AP12	GND2	GND56	T34
G30	GND3	GND57	T35
P10	GND4	GND58	T37
T10	GND5	GND59	T38
T6	GND6	GND60	T7
V10	GND7	GND61	T9
V34	GND8	GND62	U18
W5	GND9	GND63	U20
AA39	GND10	GND64	U22
AB22	GND11		
AB7	GND12		
AD22	GND13		
AE20	GND14		
AF24	GND15		
AG24	GND16		
AH35	GND17		
AK7	GND18		
AM28	GND19		
AT25	GND20		
AP30	GND21		
AR36	GND22		
AU10	GND23		
F28	GND24		
BC21	GND25		
AY9	GND26		
BC9	GND27		
D34	GND28		
F24	GND29		
G32	GND30		
H31	GND31		
K7	GND32		
M38	GND33		
M5	GND34		
M6	GND35		
M7	GND36		
M9	GND37		
N39	GND38		
N8	GND39		
P33	GND40		
P34	GND41		
P37	GND42		
P4	GND43		
P40	GND44		
P7	GND45		
R36	GND46		
R40	GND47		
R43	GND48		
R5	GND49		
T18	GND50		
T20	GND51		
AK11	GND52		
T24	GND53		
T26	GND54		

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 16 OF 96	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

=PEG_D2R_P<0>	F7	PE0_RX0_P	PE0_TX0_P	C5	=PEG_R2D_C_P<0>
=PEG_D2R_N<0>	E7	PE0_RX0_N	PE0_TX0_N	D4	=PEG_R2D_C_N<0>
=PEG_D2R_P<1>	D7	PE0_RX1_P	PE0_TX1_P	C4	=PEG_R2D_C_P<1>
=PEG_D2R_N<1>	C7	PE0_RX1_N	PE0_TX1_N	B4	=PEG_R2D_C_N<1>
=PEG_D2R_P<2>	E6	PE0_RX2_P	PE0_TX2_P	A4	=PEG_R2D_C_P<2>
=PEG_D2R_N<2>	F6	PE0_RX2_N	PE0_TX2_N	A3	=PEG_R2D_C_N<2>
=PEG_D2R_P<3>	E5	PE0_RX3_P	PE0_TX3_P	B3	=PEG_R2D_C_P<3>
=PEG_D2R_N<3>	F5	PE0_RX3_N	PE0_TX3_N	B2	=PEG_R2D_C_N<3>
=PEG_D2R_P<4>	E4	PE0_RX4_P	PE0_TX4_P	C1	=PEG_R2D_C_P<4>
=PEG_D2R_N<4>	E3	PE0_RX4_N	PE0_TX4_N	D1	=PEG_R2D_C_N<4>
=PEG_D2R_P<5>	C3	PE0_RX5_P	PE0_TX5_P	D2	=PEG_R2D_C_P<5>
=PEG_D2R_N<5>	D3	PE0_RX5_N	PE0_TX5_N	E1	=PEG_R2D_C_N<5>
=PEG_D2R_P<6>	G5	PE0_RX6_P	PE0_TX6_P	E2	=PEG_R2D_C_P<6>
=PEG_D2R_N<6>	H5	PE0_RX6_N	PE0_TX6_N	F2	=PEG_R2D_C_N<6>
=PEG_D2R_P<7>	J7	PE0_RX7_P	PE0_TX7_P	F3	=PEG_R2D_C_P<7>
=PEG_D2R_N<7>	J6	PE0_RX7_N	PE0_TX7_N	F4	=PEG_R2D_C_N<7>
=PEG_D2R_P<8>	J5	PE0_RX8_P	PE0_TX8_P	G3	=PEG_R2D_C_P<8>
=PEG_D2R_N<8>	J4	PE0_RX8_N	PE0_TX8_N	H4	=PEG_R2D_C_N<8>
=PEG_D2R_P<9>	L11	PE0_RX9_P	PE0_TX9_P	H3	=PEG_R2D_C_P<9>
=PEG_D2R_N<9>	L10	PE0_RX9_N	PE0_TX9_N	H2	=PEG_R2D_C_N<9>
=PEG_D2R_P<10>	L9	PE0_RX10_P	PE0_TX10_P	H1	=PEG_R2D_C_P<10>
=PEG_D2R_N<10>	L8	PE0_RX10_N	PE0_TX10_N	J1	=PEG_R2D_C_N<10>
=PEG_D2R_P<11>	L7	PE0_RX11_P	PE0_TX11_P	J2	=PEG_R2D_C_P<11>
=PEG_D2R_N<11>	L6	PE0_RX11_N	PE0_TX11_N	J3	=PEG_R2D_C_N<11>
=PEG_D2R_P<12>	N11	PE0_RX12_P	PE0_TX12_P	K2	=PEG_R2D_C_P<12>
=PEG_D2R_N<12>	N10	PE0_RX12_N	PE0_TX12_N	K3	=PEG_R2D_C_N<12>
=PEG_D2R_P<13>	N9	PE0_RX13_P	PE0_TX13_P	L4	=PEG_R2D_C_P<13>
=PEG_D2R_N<13>	P9	PE0_RX13_N	PE0_TX13_N	L3	=PEG_R2D_C_N<13>
=PEG_D2R_P<14>	N7	PE0_RX14_P	PE0_TX14_P	M4	=PEG_R2D_C_P<14>
=PEG_D2R_N<14>	N6	PE0_RX14_N	PE0_TX14_N	M3	=PEG_R2D_C_N<14>
=PEG_D2R_P<15>	N5	PE0_RX15_P	PE0_TX15_P	M2	=PEG_R2D_C_P<15>
=PEG_D2R_N<15>	N4	PE0_RX15_N	PE0_TX15_N	M1	=PEG_R2D_C_N<15>

PEG_PRSNT_L	C8	PE0_PRSNT_16#	Int PU
MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49	Int PU
PCIE_MINI_PRSNT_L	D9	PEB_PRSNT#	Int PU
FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50	Int PU
PCIE_FW_PRSNT_L	C10	PEC_PRSNT#	Int PU
EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51	Int PU
PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT#	Int PU
TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16	Int PU
TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46	Int PU
AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17	Int PU
GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47	Int PU
TP_MCP_GPIO_18	M17	PEG_CLKREQ#/GPIO_18	Int PU
GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48	Int PU
PCIE_WAKE_L	F17	PE_WAKE#	Int PU (S5)

			PE0_REFCLK_P	E11	PEG_CLK100M_P
			PE0_REFCLK_N	D11	PEG_CLK100M_N
			PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P
			PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N
			PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P
			PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N
			PE3_REFCLK_P	G13	PCIE_CLK100M_EXCARD_P
			PE3_REFCLK_N	F13	PCIE_CLK100M_EXCARD_N
			PE4_REFCLK_P	J13	TP_PCIE_CLK100M_PE4P
			PE4_REFCLK_N	H13	TP_PCIE_CLK100M_PE4N
			PE5_REFCLK_P	L14	TP_PCIE_CLK100M_PE5P
			PE5_REFCLK_N	K14	TP_PCIE_CLK100M_PE5N
			PE6_REFCLK_P	N14	TP_PCIE_CLK100M_PE6P
			PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N
			PEX_RST0#	K11	PCIE_RESET_L

PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8	PCIE_MINI_R2D_C_P
PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8	PCIE_MINI_R2D_C_N
PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8	PCIE_FW_R2D_C_P
PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8	PCIE_FW_R2D_C_N
PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	PE1_TX2_P	A7	PCIE_EXCARD_R2D_C_P
PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	PE1_TX2_N	B7	PCIE_EXCARD_R2D_C_N
TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP
TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6	TP_PCIE_PE4_R2D_CN

=PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

+DVDD0_PEX1	T17
+DVDD0_PEX2	W19
+DVDD0_PEX3	U17
+DVDD0_PEX4	V19
+DVDD0_PEX5	W16
+DVDD0_PEX6	W17
+DVDD0_PEX7	W18
+DVDD0_PEX8	U16

=PP1V05_S0_MCP_PEX_DVDD1

+DVDD1_PEX1	T19
+DVDD1_PEX2	U19

=PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

+V_PLL_PEX	T16

MCP_PEX_CLK_COMP

PEX_CLK_COMP	A11

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

=PP1V05_S0_MCP_PEX_AVDD0
206 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

+AVDD0_PEX1	Y12
+AVDD0_PEX2	AA12
+AVDD0_PEX3	AB12
+AVDD0_PEX4	M12
+AVDD0_PEX5	P12
+AVDD0_PEX6	R12
+AVDD0_PEX7	N12
+AVDD0_PEX8	T12
+AVDD0_PEX9	U12
+AVDD0_PEX10	AC12
+AVDD0_PEX11	AD12
+AVDD0_PEX12	V12
+AVDD0_PEX13	W12

=PP1V05_S0_MCP_PEX_AVDD1

+AVDD1_PEX1	M13
+AVDD1_PEX2	N13
+AVDD1_PEX3	P13

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

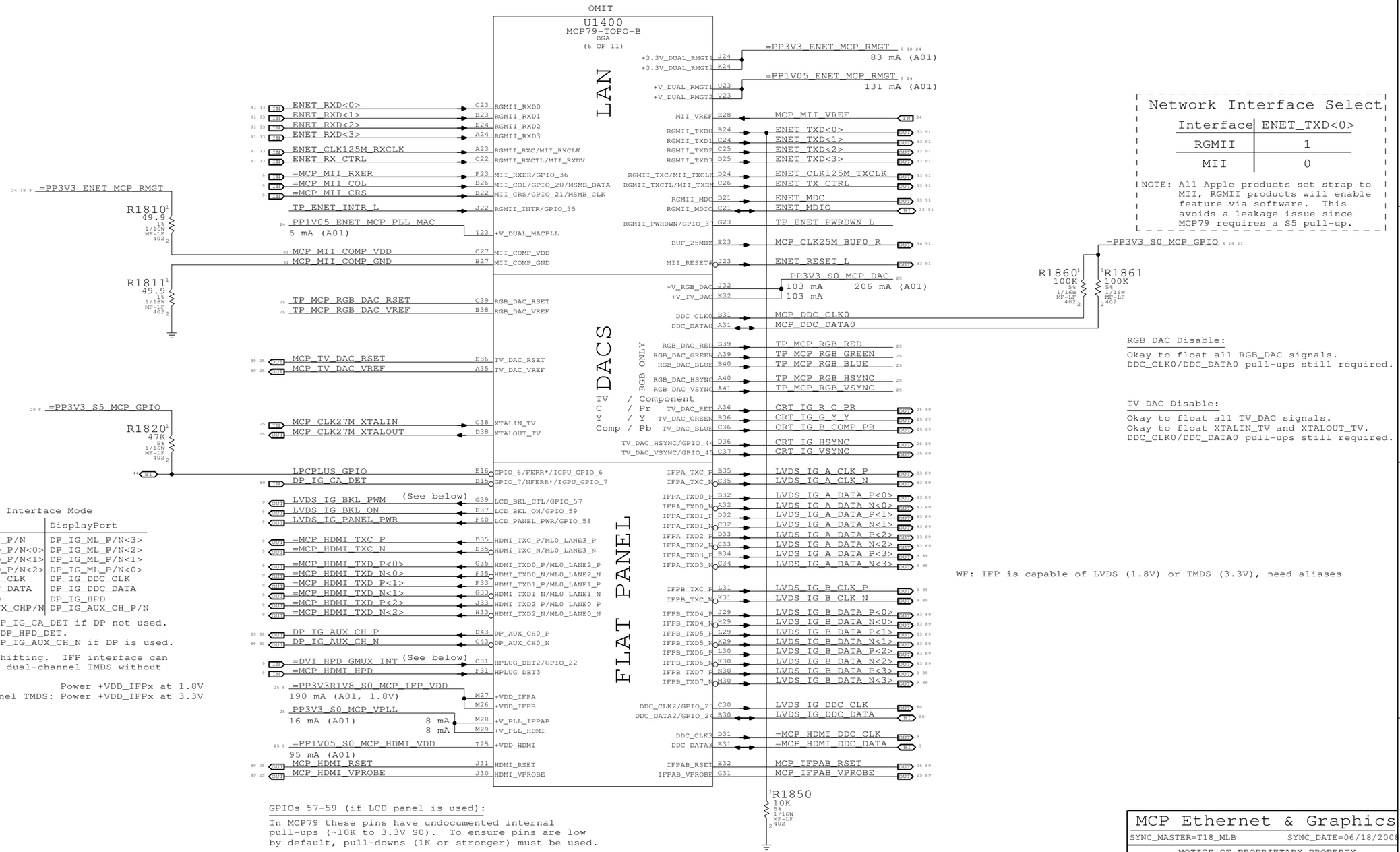
SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	17	96

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 18 OF 96	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

PCI_REQ0_L	T2	PCI_REQ0#	
PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2	
CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	
AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	
MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	
MCP_DEBUG<0>	AC3	PCI_AD0	
MCP_DEBUG<1>	AE10	PCI_AD1	
MCP_DEBUG<2>	AC4	PCI_AD2	
MCP_DEBUG<3>	AE11	PCI_AD3	
MCP_DEBUG<4>	AB3	PCI_AD4	
MCP_DEBUG<5>	AC6	PCI_AD5	
MCP_DEBUG<6>	AB2	PCI_AD6	
MCP_DEBUG<7>	AC7	PCI_AD7	
TP_PCI_AD<8>	AC8	PCI_AD8	
TP_PCI_AD<9>	AA2	PCI_AD9	
TP_PCI_AD<10>	AC9	PCI_AD10	
TP_PCI_AD<11>	AC10	PCI_AD11	
TP_PCI_AD<12>	AC11	PCI_AD12	
TP_PCI_AD<13>	AA1	PCI_AD13	
TP_PCI_AD<14>	AA5	PCI_AD14	
TP_PCI_AD<15>	Y5	PCI_AD15	
TP_PCI_AD<16>	W3	PCI_AD16	
TP_PCI_AD<17>	W6	PCI_AD17	
TP_PCI_AD<18>	W4	PCI_AD18	
TP_PCI_AD<19>	W7	PCI_AD19	
TP_PCI_AD<20>	V3	PCI_AD20	
TP_PCI_AD<21>	W8	PCI_AD21	
TP_PCI_AD<22>	V2	PCI_AD22	
TP_PCI_AD<23>	W9	PCI_AD23	
TP_PCI_AD<24>	U3	PCI_AD24	
TP_PCI_AD<25>	W11	PCI_AD25	
TP_PCI_AD<26>	U2	PCI_AD26	
TP_PCI_AD<27>	U5	PCI_AD27	
TP_PCI_AD<28>	U1	PCI_AD28	
TP_PCI_AD<29>	U6	PCI_AD29	
TP_PCI_AD<30>	T5	PCI_AD30	
TP_PCI_AD<31>	U7	PCI_AD31	
TP_PCI_INTW_L	P2	PCI_INTW#	
TP_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
TP_PCI_INTZ_L	N1	PCI_INTZ#	
TP_PCI_TRDY_L	Y3	PCI_TRDY#	
PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
FW_PME_L	AE2	LPC_DRQ1#/GPIO_19	Int PU
TP_LPC_DRQ0_L	AE1	LPC_DRQ0#	Int PU
LPC_SERIRQ	AE6	LPC_SERIRQ	Int PU

PCI_GNT0#	R3	TP_PCI_GNT0_L	
PCI_GNT1#/FANCTL2	U10	TP_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	OUT
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	OUT
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	OUT
PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	
PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	
PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	
PCI_FRAME#	Y4	TP_PCI_FRAME_L	
PCI_IRDY#	AA10	TP_PCI_IRDY_L	
PCI_PAR	Y1	TP_PCI_PAR	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L	
PCI_SERR#	AA7	TP_PCI_SERR_L	
PCI_STOP#	Y2	TP_PCI_STOP_L	
PCI_PME#/GPIO_30	T1	PM_LATRIGGER_L	OUT
Int PU (S5)			
PCI_RESET0#	R10	MEM_VTT_EN_R	OUT
PCI_RESET1#	R11	TP_PCI_RESET1_L	
PCI_CLK0	R6	TP_PCI_CLK0	
PCI_CLK1	R7	TP_PCI_CLK1	
PCI_CLK2	R8	PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	PCI_CLK33M_MCP	

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	LPC_FRAME_R_L	R1960 22	LPC_FRAME_L
LPC_PWRDWN#/GPIO_54/EXT_NMI	AE12	LPC_PWRDWN_L		
LPC_RESET0#	AE5	LPC_RESET_L		
LPC_AD0	AD3	LPC_AD_R<0>	R1950 22	LPC_AD<0>
LPC_AD1	AD2	LPC_AD_R<1>	R1951 22	LPC_AD<1>
LPC_AD2	AD1	LPC_AD_R<2>	R1952 22	LPC_AD<2>
LPC_AD3	AD5	LPC_AD_R<3>	R1953 22	LPC_AD<3>
LPC_CLK0	AE9	LPC_CLK33M_SMC_R		

All 22 ohm resistors: 5% 1/16W MF-LF 402

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

GND65	U24	GND98	Y26
GND66	U26	GND99	Y27
GND67	U39	GND100	AB18
GND68	U4	GND101	H34
GND69	U8	GND102	AB20
GND70	V16	GND103	AB21
GND71	V17	GND104	AB23
GND72	V18	GND105	AB24
GND73	V20	GND106	AB25
GND74	V22	GND107	AB26
GND75	V24	GND108	AB27
GND76	V26	GND109	AB28
GND77	V27	GND110	AB34
GND78	V28	GND111	AB37
GND79	V33	GND112	AB4
GND80	V37	GND113	AB40
GND81	V4	GND114	AC22
GND82	V40	GND115	AC36
GND83	V7	GND116	AC40
GND84	W20	GND117	AB33
GND85	W22	GND118	AC5
GND86	W24	GND119	AD16
GND87	W36	GND120	AD17
GND88	W40	GND121	AD18
GND89	W43	GND122	AD19
GND90	Y16	GND123	AD20
GND91	Y17	GND124	AD24
GND92	Y18	GND125	AD25
GND93	Y19	GND126	AD26
GND94	Y20	GND127	AD27
GND95	Y22	GND128	AD28
GND96	Y24	GND129	AD33
GND97	Y25	GND130	AD34

=PP3V3_S0_MCP_GPIO

MCP_RS232_SOUT_L	R1989	8.2K
PCI_REQ0_L	R1990	8.2K
PCI_REQ1_L	R1991	8.2K
CRTMUX_SEL_TV_L	R1992	8.2K
MCP_RS232_SIN_L	R1994	8.2K

5% 1/16W MF-LF 402

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE: NONE SHT 19 OF 96

OMIT

U1400
MCP79-TOPO-B
BGA
(8 OF 11)

SATA

SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P	
SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N	
SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N	
SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P	
SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P	
SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N	
SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N	
SATA_ODD_D2R_P	AK9	SATA_A1_RX_P	
TP_SATA_C_R2D_CP	AK2	SATA_B0_TX_P	
TP_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N	
TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N	
TP_SATA_C_D2RP	AJ1	SATA_B0_RX_P	
TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P	
TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N	
TP_SATA_D_D2RN	AL4	SATA_B1_RX_N	
TP_SATA_D_D2RP	AK3	SATA_B1_RX_P	
TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P	
TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N	
TP_SATA_E_D2RN	AM2	SATA_C0_RX_N	
TP_SATA_E_D2RP	AM3	SATA_C0_RX_P	
TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P	
TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N	
TP_SATA_F_D2RN	AN3	SATA_C1_RX_N	
TP_SATA_F_D2RP	AN2	SATA_C1_RX_P	
TP_MCP_SATALED_L	E12	SATA_LED#	
PP1V05_S0_MCP_PLL_SATA (84 mA (A01))	AE16	+V_PLL_SATA	
=PP1V05_S0_MCP_SATA_DVDD0 (43 mA (A01, DVDD0 & 1))	AF19	+DVDD0_SATA1	
Minimum 1.025V for Gen2 support	AG16	+DVDD0_SATA2	
	AG17	+DVDD0_SATA3	
	AG19	+DVDD0_SATA4	
=PP1V05_S0_MCP_SATA_DVDD1	AH17	+DVDD1_SATA1	
	AH19	+DVDD1_SATA2	
=PP1V05_S0_MCP_SATA_AVDD0 (127 mA (A01, AVDD0 & 1))	AJ12	+AVDD0_SATA1	
Minimum 1.025V for Gen2 support	AN11	+AVDD0_SATA2	
	AK12	+AVDD0_SATA3	
	AK13	+AVDD0_SATA4	
	AL12	+AVDD0_SATA5	
	AM11	+AVDD0_SATA6	
	AM12	+AVDD0_SATA7	
	AN12	+AVDD0_SATA8	
	AL13	+AVDD0_SATA9	
=PP1V05_S0_MCP_SATA_AVDD1	AN14	+AVDD1_SATA1	
	AL14	+AVDD1_SATA2	
	AM13	+AVDD1_SATA3	
	AM14	+AVDD1_SATA4	
MCP_SATA_TERMP	AE3	SATA_TERMP	

R2010 2.49K 1% 1/16W MF-LF 402

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

USB

External A			
USB0_P	C29	USB_EXTA_P	
USB0_N	D29	USB_EXTA_N	
AirPort (PCIe Mini-Card)			
USB1_P	C28	USB_MINI_P	
USB1_N	D28	USB_MINI_N	
External D			
USB2_P	A28	USB_EXTD_P	
USB2_N	B28	USB_EXTD_N	
Camera			
USB3_P	F29	USB_CAMERA_P	
USB3_N	G29	USB_CAMERA_N	
IR			
USB4_P	K27	USB_IR_P	
USB4_N	L27	USB_IR_N	
Geyser Trackpad/Keyboard			
USB5_P	J26	USB_TPAD_P	
USB5_N	J27	USB_TPAD_N	
Bluetooth			
USB6_P	F27	USB_BT_P	
USB6_N	G27	USB_BT_N	
External B			
USB7_P	D27	USB_EXTB_P	
USB7_N	E27	USB_EXTB_N	
ExpressCard			
USB8_P	K25	USB_EXCARD_P	
USB8_N	L25	USB_EXCARD_N	
External C			
USB9_P	H25	USB_EXTC_P	
USB9_N	J25	USB_EXTC_N	
USB10_P	F25	TP_USB_10P	
USB10_N	G25	TP_USB_10N	
USB11_P	K23	TP_USB_11P	
USB11_N	L23	TP_USB_11N	
USB_OC0#/GPIO_25	L21	USB_EXTA_OC_L	
USB_OC1#/GPIO_26	K21	USB_EXTB_OC_L	
USB_OC2#/GPIO_27/MGPIO	J21	USB_EXTC_OC_L	
USB_OC3#/GPIO_28/MGPIO	H21	EXCARD_OC_L	
+V_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB (19 mA (A01))	
USB_RBIAS_GND	A27	MCP_USB_RBIAS_GND	

=PP3V3_S5_MCP_GPIO

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

R2060 806 1% 1/16W MF-LF 402

GND131	AD35	GND132	AD37
GND133	AD38	GND134	AE22
GND135	AE24	GND136	AE39
GND137	AE4	GND138	AD6
GND139	AF16	GND140	AF17
GND141	AF18	GND142	AF20
GND143	AF22	GND144	AF26
GND145	AF27	GND146	AF28
GND147	AF33	GND148	AF34
GND149	AF37	GND150	AF40
GND151	AG18	GND152	AG20
GND153	AG22	GND154	AG26
GND155	AG36	GND156	AG40
GND157	AH18	GND158	AH20
GND159	AH22	GND160	AH24

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 20 OF 96	

OMIT

U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

HDA_SDIN0 → G15 HDA_SDATA_IN0 Int PD
TP_MLB_RAM_SIZE → J14 HDA_SDATA_IN1/GPIO_2/PS2_KB_CLK Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems) → J15 HDA_SDATA_IN2/GPIO_3/PS2_KB_DATA Int PD

=PP3V3R1V5_S0_MCP_HDA → R2110 49.9 1% 1/16W MF-LF 402 → MCP_HDA_PULLDN_COMP → A15 HDA_PULLDN_COMP

PP1V05_S0_MCP_PLL_NV 37 mA (A01)
20 mA → AE18 +V_PLL_NV_H
17 mA → AE17 +V_PLL_SP_SPREF

PP3V3_G3_RTC → R2120 49.9K 1% 1/16W MF-LF 402 → R2121 49.9K 1% 1/16W MF-LF 402

=SPI_CS1_R_L_USE_MLB → L24 GPIO_1/PWRDN_OK/SPI_CS1
SMC_ADAPTER_EN → L26 GPIO_12/SUS_STAT#/ACCLMTR
TP_SB_A20GATE → K13 A20GATE Int PU
TP_MCP_KBDRSTIN_L → L13 KBRDRSTIN# Int PU
SMC_WAKE_SCI_L → C19 SIO_PME# Int PU (S5)
SMC_RUNTIME_SCI_L → C18 EXT_SMI/GPIO_32# Int PU (S5)
SM_INTRUDER_L → B20 INTRUDER#
TP_MCP_LID_L → M25 LID# Int PU (S5)
PM_BATLOW_L → M24 LLB# Int PU (S5)
PM_DPRSLPVR → M22 CPU_DPRSLPVR
PM_PWRBTN_L → C16 PWRBTN# Int PU (S5)
PM_SYSRST_DEBOUNCE_L → D16 RSTBTN# Int PU
RTC_RST_L → C20 RTC_RST#
PM_RSMRST_L → D20 PWRGD_SB
MCP_PS_PWRGD → E20 PS_PWRGD
MCP_CPU_VLD → C17 CPU_VLD
JTAG_MCP_TDI → E19 JTAG_TDI Int PU
JTAG_MCP_TDO ← F19 JTAG_TDO
JTAG_MCP_TMS → J19 JTAG_TMS Int PU
JTAG_MCP_TRST_L → J18 JTAG_TRST# Int PU
JTAG_MCP_TCK → G19 JTAG_TCK
MCP_CLK25M_XTALIN → A16 XTALIN
MCP_CLK25M_XTALOUT ← B16 XTALOUT
RTC_CLK32K_XTALIN → A19 XTALIN_RTC
RTC_CLK32K_XTALOUT ← B19 XTALOUT_RTC

R2150 10K 5% 1/16W MF-LF 402 → GND
R2151 100K 5% 1/16W MF-LF 402 → GND

=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
R2160 8.2K 5% 1/16W MF-LF 402

+V_DUAL_HDA1 J16
+V_DUAL_HDA2 K16

HDA_SDATA_OUT F15 → R2170 22 5% 1/16W MF-LF 402 → HDA_SDOUT R → HDA_SDOUT
HDA_BITCLK E15 → R2171 22 5% 1/16W MF-LF 402 → HDA_BIT_CLK_R → HDA_BIT_CLK
HDA_RESET# K15 → R2172 22 5% 1/16W MF-LF 402 → HDA_RST_R_L → HDA_RST_L
HDA_SYNC L15 → R2173 22 5% 1/16W MF-LF 402 → HDA_SYNC_R → HDA_SYNC

MISC

HDA_DOCK_EN#/GPIO_4/PS2_MS_CLK K17 → MCP_GPIO_4
HDA_DOCK_RST#/GPIO_5/PS2_MS_DATA L17 → AUD_I2C_INT_L
SLP_S3# G17 → PM_SLP_S3_L
SLP_RMGT# J17 → PM_SLP_RMGT_L
SLP_S5# H17 → PM_SLP_S4_L
THERM_DIODE_P B11 → MCP_THMDIODE_P
THERM_DIODE_N C11 → MCP_THMDIODE_N
MCP_VID0/GPIO_13 L20 → MCP_VID<0>
MCP_VID1/GPIO_14 M20 → MCP_VID<1>
MCP_VID2/GPIO_15 M21 → MCP_VID<2>
SPKR C13 → MCP_SPKR
SMB_CLK0 L19 ↔ SMBUS_MCP_0_CLK
SMB_DATA0 K19 ↔ SMBUS_MCP_0_DATA
SMB_CLK1/MSMB_CLK G21 ↔ SMBUS_MCP_1_CLK
SMB_DATA1/MSMB_DATA F21 ↔ SMBUS_MCP_1_DATA
SMB_ALERT#/GPIO_64 M23 → AP_PWR_EN
(MGPIO2) FANRPM0/GPIO_60 B12 ← MEM_EVENT_L
FANCTL0/GPIO_61 A12 → ODD_PWR_EN_L
(MGPIO3) FANRPM1/GPIO_63 D12 ← SMC_IG_THROTTLE_L
FANCTL1/GPIO_62 C12 → ARB_DETECT
CPUVDD_EN D17 → MCP_CPUVDD_EN
SPI_CS0/GPIO_10 C14 → SPI_CS0_R_L
SPI_CLK/GPIO_11 D13 → SPI_CLK_R
SPI_DI/GPIO_8 C15 ← SPI_MISO
SPI_DO/GPIO_9 B14 → SPI_MOSI_R
SUS_CLK/GPIO_34 B18 → PM_CLK32K_SUSCLK_R
BUF_SIO_CLK AE7 → TP_MCP_BUF_SIO_CLK
TEST_MODE_EN K22 → MCP_TEST_MODE_EN
PKG_TEST L22

R2163 10K 5% 1/16W MF-LF 402 → GND
R2190 1K 1% 1/16W MF-LF 402 → GND

=PP3V3_S0_MCP
BOOT_MODE_SAFE
R2180 10K 5% 1/16W MF-LF 402 → GND
BOOT_MODE_USER
R2181 10K 5% 1/16W MF-LF 402 → GND

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_RST_R_L
HDA_SYNC_R

C2170 10PF 5% 50V CERM 402
C2172 10PF 5% 50V CERM 402
C2171 10PF 5% 50V CERM 402
C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO
R2140 10K 5% 1/16W MF-LF 402
R2141 10K 5% 1/16W MF-LF 402
R2142 10K 5% 1/16W MF-LF 402
R2143 10K 5% 1/16W MF-LF 402

MCP_GPIO_4
AUD_I2C_INT_L
MEM_EVENT_L
SMC_IG_THROTTLE_L
ARB_DETECT

R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO
R2154 100K 5% 1/16W MF-LF 402
AP_PWR_EN

MCP_VID<0>
MCP_VID<1>
MCP_VID<2>

R2155 22K 5% 1/16W MF-LF 402
R2156 22K 5% 1/16W MF-LF 402
R2157 22K 5% 1/16W MF-LF 402

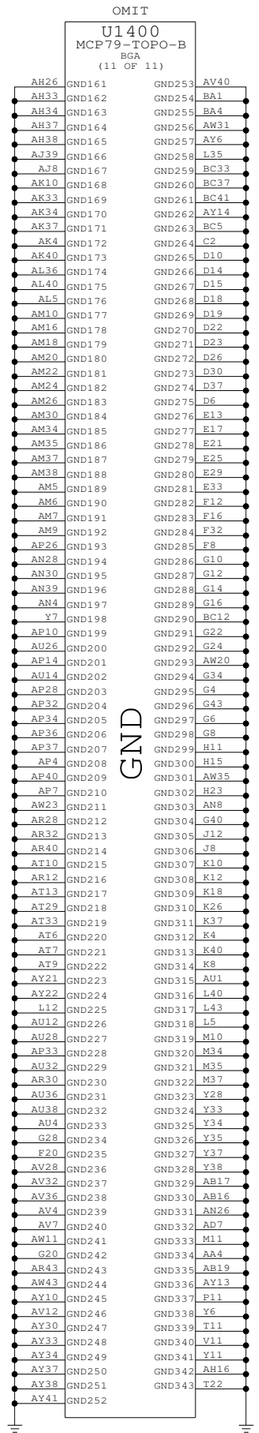
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 21 OF 96	



MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

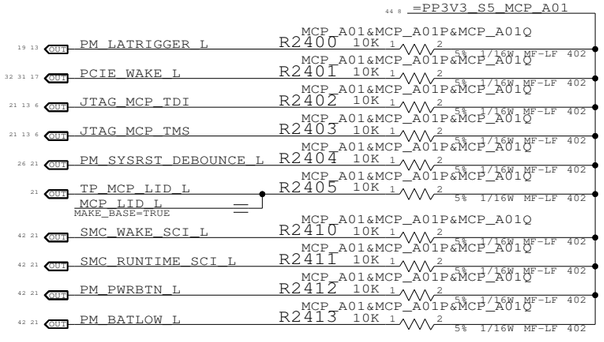
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 22 OF 96	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 23 OF 96	

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1uF 20% 10V CERM 402
C2526 0.1uF 20% 10V CERM 402

MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

=PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

=PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_ENET_MCP_PLL_MAC

5 mA (A01)

L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF
C2591 0.1UF 20% 10V CERM 402

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_AVDD_UF

333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 206 mA (A01)
VOLTAGE=1.05V

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 127 mA (A01)
VOLTAGE=1.05V

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_UF

562 mA (A01)

R2580 0.2 1% 1/6W MF 402-HP
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 270 mA (A01)
VOLTAGE=1.05V

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 20% 6.3V CERM 402-LF

L2582 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 84 mA (A01)
VOLTAGE=1.05V

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 84 mA (A01)
VOLTAGE=1.05V

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 87 mA (A01)
VOLTAGE=1.05V

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 37 mA (A01)
VOLTAGE=1.05V

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

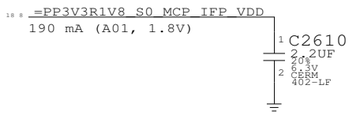
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

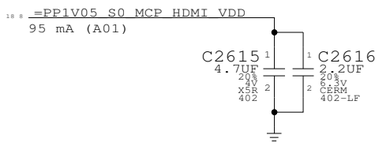
SCALE	SHT	OF
NONE	24	96

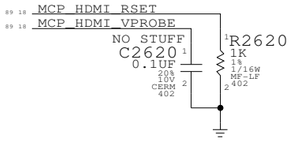
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

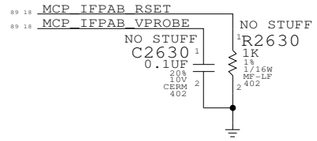
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

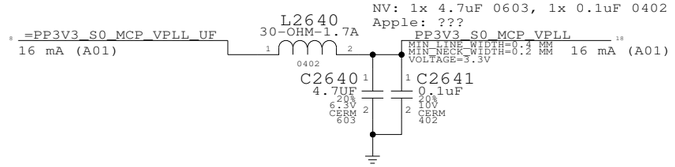




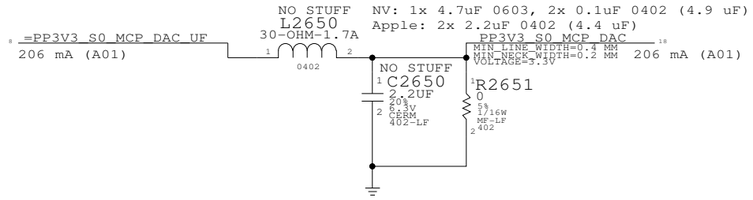




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NO STUFF
NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

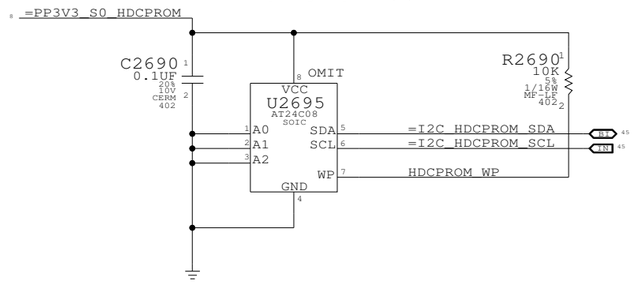


TP_MCP_RGB_RED	—	NC_MCP_RGB_RED
TP_MCP_RGB_GREEN	—	NC_MCP_RGB_GREEN
TP_MCP_RGB_BLUE	—	NC_MCP_RGB_BLUE
TP_MCP_RGB_HSYNC	—	NC_MCP_RGB_HSYNC
TP_MCP_RGB_VSYNC	—	NC_MCP_RGB_VSYNC
CRT_IG_R_C_PR	—	NC_CRT_IG_R_C_PR
CRT_IG_G_Y_Y	—	NC_CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB	—	NC_CRT_IG_B_COMP_PB
CRT_IG_HSYNC	—	NC_CRT_IG_HSYNC
CRT_IG_VSYNC	—	NC_CRT_IG_VSYNC
TP_MCP_RGB_DAC_RSET	—	NC_MCP_RGB_DAC_RSET
TP_MCP_RGB_DAC_VREF	—	NC_MCP_RGB_DAC_VREF
MCP_TV_DAC_RSET	—	NC_MCP_TV_DAC_RSET
MCP_TV_DAC_VREF	—	NC_MCP_TV_DAC_VREF
MCP_CLK27M_XTALIN	—	NC_MCP_CLK27M_XTALIN
MCP_CLK27M_XTALOUT	—	NC_MCP_CLK27M_XTALOUT

(all NC_ nets: MAKE_BASE=TRUE)

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.



Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

MCP Graphics Support

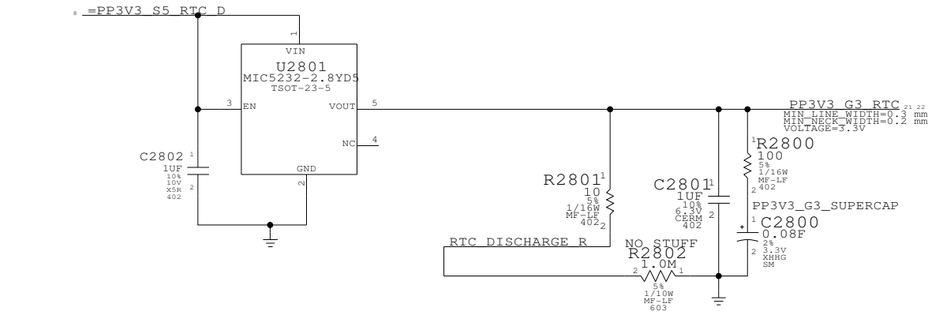
SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

APPLE INC.

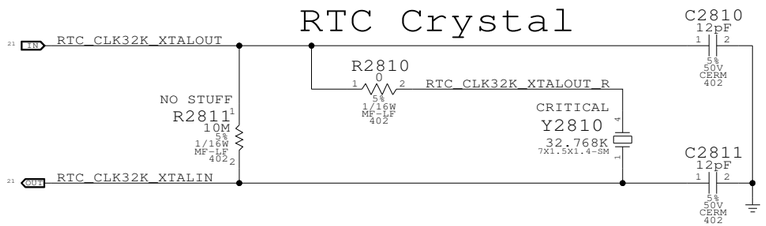
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	25	96

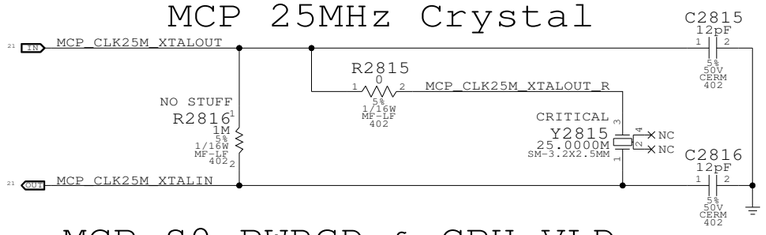
RTC Power Sources



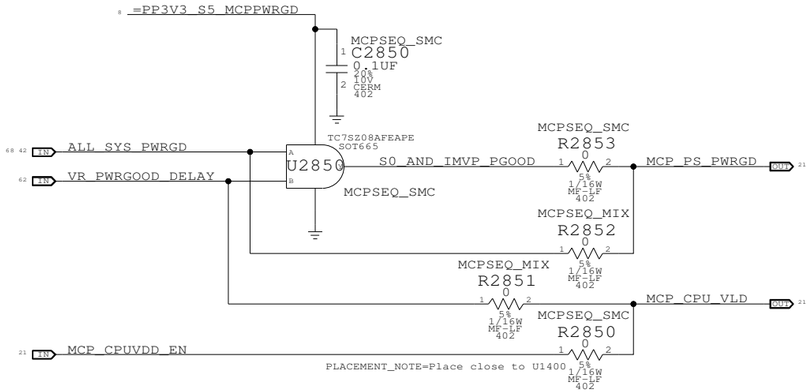
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

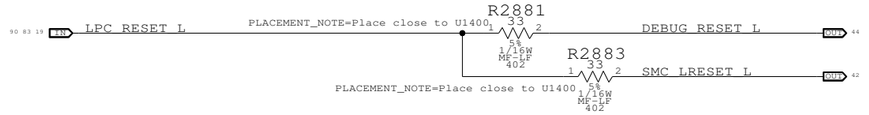
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

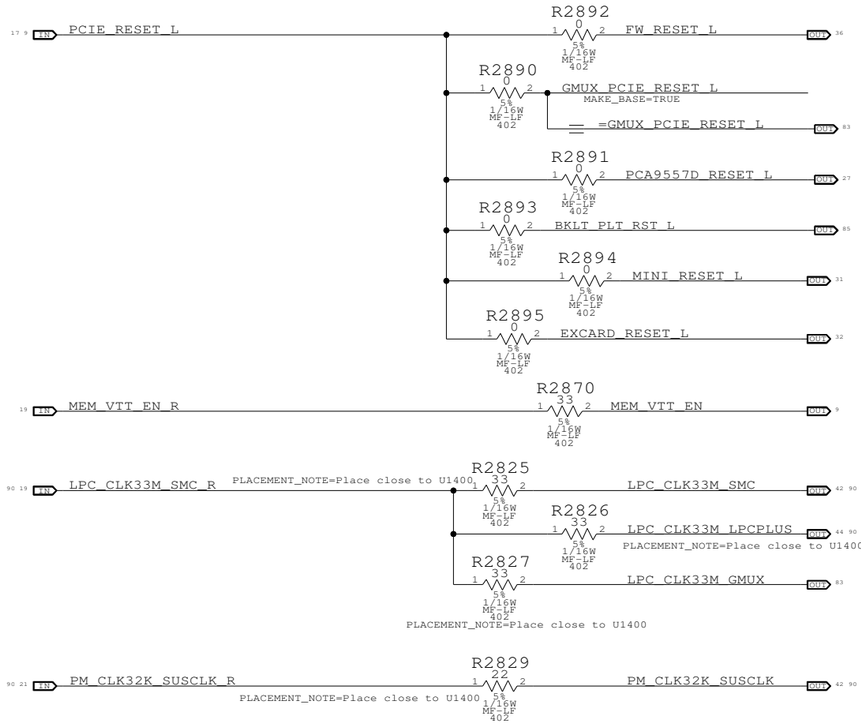
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

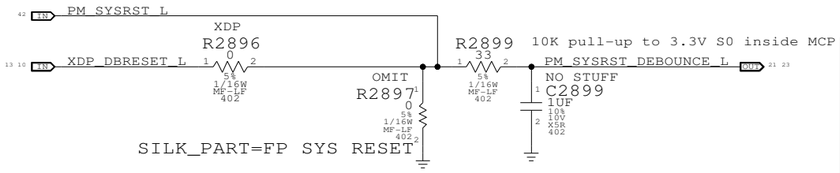
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc		
SYNC_MASTER=T18_MLB	SYNC_DATE=12/17/2007	

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 26 OF 96	

Page Notes

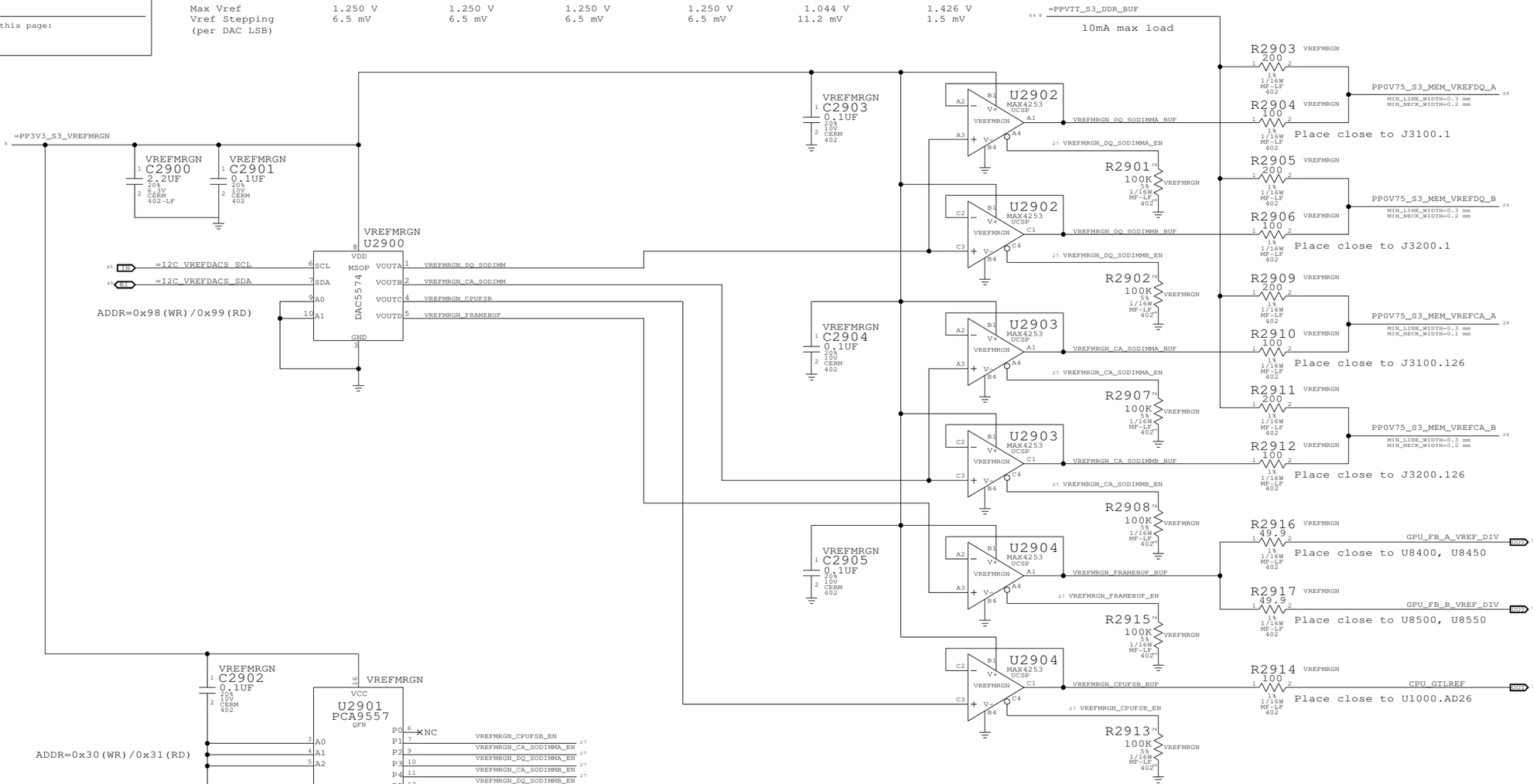
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 27 OF 96	

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

ROM options provided by this page:
(NONE)

=PP1V5_S0_MEM_A

=PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402

27 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_A_A<15>	9
	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	
		81	VDD	VDD	82		
	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	
	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	
		87	VDD	VDD	88		
	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	
	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	
		93	VDD	VDD	94		
	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	
	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	
		99	VDD	VDD	100		
	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	
	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	
		105	VDD	VDD	106		
	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	
	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	
		111	VDD	VDD	112		
	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	
	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	
		117	VDD	VDD	118		
	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	
	MEM_A_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
	MEM_A_DQ<33>	129	DQ32	DQ36	130	MEM_A_DQ<36>	
	MEM_A_DQ<32>	131	DQ33	DQ37	132	MEM_A_DQ<37>	
		133	VSS	VSS	134		
	MEM_A_DQS_N<4>	135	DQS4*	DM4	136	MEM_A_DM<4>	
	MEM_A_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_A_DQ<38>	
	MEM_A_DQ<34>	141	DQ34	DQ39	142	MEM_A_DQ<39>	
	MEM_A_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_A_DQ<47>	
	MEM_A_DQ<44>	147	DQ40	DQ45	148	MEM_A_DQ<40>	
	MEM_A_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_A_DQS_N<5>	
	MEM_A_DM<5>	153	DM5	DQS5	154	MEM_A_DQS_P<5>	
		155	VSS	VSS	156		
	MEM_A_DQ<45>	157	DQ42	DQ46	158	MEM_A_DQ<46>	
	MEM_A_DQ<42>	159	DQ43	DQ47	160	MEM_A_DQ<43>	
		161	VSS	VSS	162		
	MEM_A_DQ<52>	163	DQ48	DQ52	164	MEM_A_DQ<48>	
	MEM_A_DQ<51>	165	DQ49	DQ53	166	MEM_A_DQ<53>	
		167	VSS	VSS	168		
	MEM_A_DQS_N<6>	169	DQS6*	DM6	170	MEM_A_DM<6>	
	MEM_A_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_A_DQ<50>	
	MEM_A_DQ<55>	175	DQ50	DQ55	176	MEM_A_DQ<49>	
	MEM_A_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_A_DQ<57>	
	MEM_A_DQ<61>	181	DQ56	DQ61	182	MEM_A_DQ<56>	
	MEM_A_DQ<60>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_A_DQS_N<7>	
	MEM_A_DM<7>	187	DM7	DQS7	188	MEM_A_DQS_P<7>	
		189	VSS	VSS	190		
	MEM_A_DQ<58>	191	DQ58	DQ62	192	MEM_A_DQ<62>	
	MEM_A_DQ<59>	193	DQ59	DQ63	194	MEM_A_DQ<63>	
		195	VSS	VSS	196		
	MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	21 29 42
		199	VDDSPD	SDA	200	=I2C_SODIMMA_SDA	45
	MEM_A_SA<1>	201	SA1	SCL	202	=I2C_SODIMMA_SCL	45
		203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_A	8

516-0196
SPD ADDR=0xA0(WR)/0xA1(RD)

=PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S3_MEM_VREFCA_A 27

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
CRITICAL

		1	VREFDQ	VSS	2		
	MEM_A_DQ<0>	3	VSS	DQ4	4	MEM_A_DQ<4>	
	MEM_A_DQ<1>	5	DQ0	DQ5	6	MEM_A_DQ<5>	
		7	DQ1	VSS	8		
	MEM_A_DM<0>	9	VSS	DQS0*	10	MEM_A_DQS_N<0>	
		11	DM0	DQS0	12	MEM_A_DQS_P<0>	
	MEM_A_DQ<3>	13	VSS	VSS	14		
	MEM_A_DQ<2>	15	DQ2	DQ6	16	MEM_A_DQ<6>	
		17	DQ3	DQ7	18	MEM_A_DQ<7>	
	MEM_A_DQ<9>	19	VSS	VSS	20		
	MEM_A_DQ<13>	21	DQ8	DQ12	22	MEM_A_DQ<8>	
		23	DQ9	DQ13	24	MEM_A_DQ<12>	
		25	VSS	VSS	26		
	MEM_A_DQS_N<1>	27	DQS1*	DM1	28	MEM_A_DM<1>	
	MEM_A_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	29 30
		31	VSS	VSS	32		
	MEM_A_DQ<11>	33	DQ10	DQ14	34	MEM_A_DQ<15>	
	MEM_A_DQ<14>	35	DQ11	DQ15	36	MEM_A_DQ<10>	
		37	VSS	VSS	38		
	MEM_A_DQ<16>	39	DQ16	DQ20	40	MEM_A_DQ<21>	
	MEM_A_DQ<18>	41	DQ17	DQ21	42	MEM_A_DQ<20>	
		43	VSS	VSS	44		
	MEM_A_DQS_N<2>	45	DQS2*	DM2	46	MEM_A_DM<2>	
	MEM_A_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_A_DQ<17>	
	MEM_A_DQ<23>	51	DQ18	DQ23	52	MEM_A_DQ<22>	
	MEM_A_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_A_DQ<29>	
	MEM_A_DQ<24>	57	DQ24	DQ29	58	MEM_A_DQ<28>	
	MEM_A_DQ<30>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_A_DQS_N<3>	
	MEM_A_DM<3>	63	DM3	DQS3	64	MEM_A_DQS_P<3>	
		65	VSS	VSS	66		
	MEM_A_DQ<27>	67	DQ26	DQ30	68	MEM_A_DQ<26>	
	MEM_A_DQ<25>	69	DQ27	DQ31	70	MEM_A_DQ<31>	
		71	VSS	VSS	72		

516-0196

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 28 OF 96	

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

8 =PP1V5_S0_MEM_B
8 =PP1V5_S3_MEM_B

C3210 C3211 C3212 C3213 C3214 C3215 C3216 C3217 C3218 C3219 C3220 C3221 C3222 C3223
0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603

27 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3 KEY

MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>
	75	VDD	VDD	76	
	77	NC	A15	78	MEM_B_A<15>
MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>
	81	VDD	VDD	82	
MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>
MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>
	87	VDD	VDD	88	
MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>
MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>
	93	VDD	VDD	94	
MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>
MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>
	99	VDD	VDD	100	
MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>
MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>
	105	VDD	VDD	106	
MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>
MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L
	111	VDD	VDD	112	
MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>
MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>
	117	VDD	VDD	118	
MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>
MEM_B_CS_L<1>	121	S1*	NC	122	
	123	VDD	VDD	124	
	125	TEST	VREFCA	126	
	127	VSS	VSS	128	
MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33>
MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36>
	133	VSS	VSS	134	
MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>
MEM_B_DQS_P<4>	137	DQS4	VSS	138	
	139	VSS	DQ38	140	MEM_B_DQ<38>
MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>
MEM_B_DQ<35>	143	DQ35	VSS	144	
	145	VSS	DQ44	146	MEM_B_DQ<44>
MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45>
MEM_B_DQ<40>	149	DQ41	VSS	150	
	151	VSS	DQS5*	152	MEM_B_DQS_N<5>
MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>
	155	VSS	VSS	156	
MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47>
MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46>
	161	VSS	VSS	162	
MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48>
MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54>
	167	VSS	VSS	168	
MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>
MEM_B_DQS_P<6>	171	DQS6	VSS	172	
	173	VSS	DQ54	174	MEM_B_DQ<53>
MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50>
MEM_B_DQ<51>	177	DQ51	VSS	178	
	179	VSS	DQ60	180	MEM_B_DQ<60>
MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>
MEM_B_DQ<57>	183	DQ57	VSS	184	
	185	VSS	DQS7*	186	MEM_B_DQS_N<7>
MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>
	189	VSS	VSS	190	
MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58>
MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62>
	195	VSS	VSS	196	
MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L
	199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA
MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL
	203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B
	205	MTG PIN	MTG PIN	206	
	207	MTG PIN	MTG PIN	208	
	209	MTG PIN	MTG PIN	210	
	211	MTG PIN	MTG PIN	212	

MTG PINS

516s0704

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF

8 =PPSPD_S0_MEM_B

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3 CRITICAL KEY

	1	VREFDQ	VSS	2	
MEM_B_DQ<0>	3	VSS	DQ4	4	MEM_B_DQ<4>
MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>
	7	DQ1	VSS	8	
MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>
	11	DM0	DQS0	12	MEM_B_DQS_P<0>
MEM_B_DQ<2>	13	VSS	VSS	14	
MEM_B_DQ<3>	15	DQ2	DQ6	16	MEM_B_DQ<6>
	17	DQ3	DQ7	18	MEM_B_DQ<7>
MEM_B_DQ<28>	19	VSS	VSS	20	
MEM_B_DQ<24>	21	DQ8	DQ12	22	MEM_B_DQ<29>
	23	DQ9	DQ13	24	MEM_B_DQ<25>
MEM_B_DQS_N<3>	25	VSS	VSS	26	
MEM_B_DQS_P<3>	27	DQS1*	DM1	28	MEM_B_DM<3>
	29	DQS1	RESET*	30	MEM_RESET_L
MEM_B_DQ<31>	31	VSS	VSS	32	
MEM_B_DQ<30>	33	DQ10	DQ14	34	MEM_B_DQ<26>
	35	DQ11	DQ15	36	MEM_B_DQ<27>
MEM_B_DQ<9>	37	VSS	VSS	38	
MEM_B_DQ<8>	39	DQ16	DQ20	40	MEM_B_DQ<13>
	41	DQ17	DQ21	42	MEM_B_DQ<12>
MEM_B_DQS_N<1>	43	VSS	VSS	44	
MEM_B_DQS_P<1>	45	DQS2*	DM2	46	MEM_B_DM<1>
	47	DQS2	VSS	48	
MEM_B_DQ<15>	49	VSS	DQ22	50	MEM_B_DQ<14>
MEM_B_DQ<10>	51	DQ18	DQ23	52	MEM_B_DQ<11>
	53	DQ19	VSS	54	
MEM_B_DQ<21>	55	VSS	DQ28	56	MEM_B_DQ<20>
MEM_B_DQ<17>	57	DQ24	DQ29	58	MEM_B_DQ<16>
	59	DQ25	VSS	60	
MEM_B_DM<2>	61	VSS	DQS3*	62	MEM_B_DQS_N<2>
	63	DM3	DQS3	64	MEM_B_DQS_P<2>
MEM_B_DQ<18>	65	VSS	VSS	66	
MEM_B_DQ<22>	67	DQ26	DQ30	68	MEM_B_DQ<19>
	69	DQ27	DQ31	70	MEM_B_DQ<23>
	71	VSS	VSS	72	

516s0704

PP0V75_S3_MEM_VREFCA_B 27

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

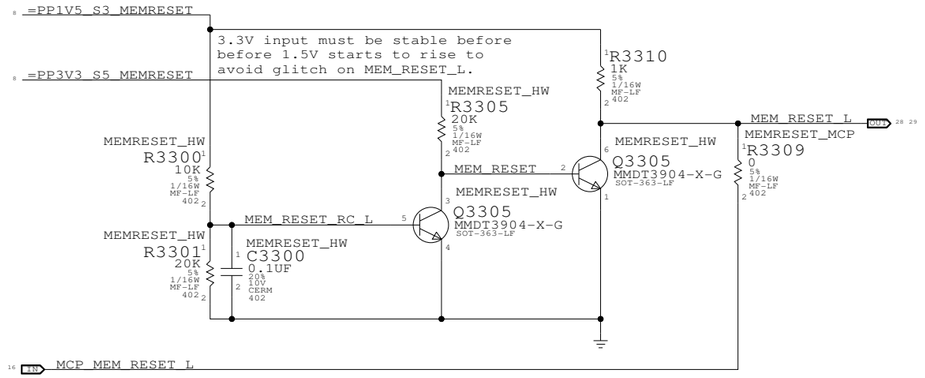
SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 29 OF 96	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support		
SYNC_MASTER=T18_MLB	SYNC_DATE=06/18/2008	

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 30 OF 96	

PCIE_MINI_PRSNT_L

Q3401
SSM6N15FEAPE
SOT563

AP_PWR_EN

MINI_CLKREQ_L

Q3401
SSM6N15FEAPE
SOT563

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_L
PCIE_WAKE_L
NC
NC

PLACEMENT_NOTE=Place close to J3401.

C3431
0.1uF
10% 16V X5R 402
PCIE_MINI_R2D_C_P

C3430
0.1uF
10% 16V X5R 402
PCIE_MINI_R2D_C_N

PLACEMENT_NOTE=Place close to J3401.

AIRPORT

L3401
90-OHM-100MA
DLP11S

PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N

PLACEMENT_NOTE=Place close to J3401.

1000 mA peak
750 mA nominal max
L3404
FERR-120-OHM-1.5A
0402-LF

PP5V_WLAN
PP5V_WLAN_F

C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
C3420 10UF 20% 10V X5R 805

PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.
PLACEMENT_NOTE=Place close to Q3450.

Q3450
FDC606P_G
SOT-6

C3450 0.1UF 10% 16V X5R 402
C3451 0.033UF 10% 16V X5R 402
R3450 100K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402

P5VWLAN_SS
PM_WLAN_EN_L
=PP5V_S3_WLAN

5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

PP5V_S3_BTCAMERA_F
I2C_ALS_SDA
I2C_ALS_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

275 mA peak
206 mA nominal max
L3405
FERR-120-OHM-1.5A
0402-LF

C3452 0.1uF 20% 10V CERM 402

=PP5V_S3_BTCAMERA

ALS
CAMERA

L3402
90-OHM
DLP0NS

USB_CAMERA_P
USB_CAMERA_N

PLACEMENT_NOTE=Place close to J3401.

BLUETOOTH

L3403
90-OHM
DLP0NS

USB_BT_P
USB_BT_N

PLACEMENT_NOTE=Place close to J3401.

=PP3V3_S3_WLAN
PP5V_WLAN_F

U3402
74LVC1G17DRL
SOT-553

TC7SZ08AFEAPE
SOT665
U3401

MINI_RESET_CONN_L
WLAN_SMIT_BUF
WLAN_SMIT_RC
MINI_RESET_L

R3453 33K 5% 1/16W MF-LF 402
R3454 62K 5% 1/16W MF-LF 402
C3453 1UF 10% 6.3V CERM 402

NC
NC

Right Clutch Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 31 OF 96	

EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

32 =PP3V3_S3_EXCARD
C3530 0.1uF 20% 10V CERM 402
C3531 10uF 20% 6.3V X5R 603

32 =PP1V5_S0_EXCARD
C3534 0.1uF 20% 10V CERM 402
C3535 10uF 20% 6.3V X5R 603

L3502
90-OHM DLP0NS

90 29 BI USB_EXCARD_N 4 3 USB2_EXCARD_CONN_N 7 32 95
90 29 BI USB_EXCARD_P 1 2 USB2_EXCARD_CONN_P 7 32 95
PLACEMENT_NOTE=Place close to J3500

L3503
90-OHM-100MA
DLP11S

89 17 IN PCIE_CLK100M_EXCARD_N 4 3 PCIE_CLK100M_EXCARD_CONN_N 7 32 95
89 17 IN PCIE_CLK100M_EXCARD_P 1 2 PCIE_CLK100M_EXCARD_CONN_P 7 32 95
PLACEMENT_NOTE=Place close to J3500

PLACEMENT_NOTE=Place close to J3500
C3571 0.1uF 10% 16V X5R 402
89 17 IN PCIE_EXCARD_R2D_C_N PCIE_EXCARD_R2D_N 7 32 89 95
89 17 IN PCIE_EXCARD_R2D_C_P PCIE_EXCARD_R2D_P 7 32 89 95
C3570 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place close to J3500

CRITICAL
J3500
502250-8727
F-RT-SM

95 89 32 7 PCIE_EXCARD_R2D_N → 4
89 17 7 OUT PCIE_EXCARD_D2R_P → 6
95 32 7 PCIE_CLK100M_EXCARD_CONN_N → 10
32 7 EXCARD_CLKREQ_CONN_L → 12
32 7 PP3V3_S0_EXCARD_SWITCH → 14
32 7 PP3V3_S3_EXCARD_SWITCH → 16
32 7 PP1V5_S0_EXCARD_SWITCH → 18
42 BI =SMBUS_EXCARD_SDA → 20
32 7 EXCARD_CPUSB_L → 24
95 32 7 USB2_EXCARD_CONN_N → 26
NCX 22
XNC 23
2 8 29

1 3 PCIE_EXCARD_R2D_P 7 32 89 95
5 PCIE_EXCARD_D2R_N OUT 7 17 89
7 PCIE_CLK100M_EXCARD_CONN_P 7 32 95
9 EXCARD_CPPE_L 7 32
11 PP3V3_S0_EXCARD_SWITCH 7 32
13 PLT_RESET_SWITCH_L 7 32
15 PCIE_WAKE_L OUT 17 23 31
17 PP1V5_S0_EXCARD_SWITCH 7 32
19 =SMBUS_EXCARD_SCL BI 45
21 USB2_EXCARD_CONN_P 7 32 95

32 7 EXCARD_CPPE_L R3501 0.1 MF-LF 402 2 5% 1/16W PCIE_EXCARD_PRSNT_L 17

OUTPUT DECOUPLING

CRITICAL
U3500
TPS2231

32 =PP3V3_S3_EXCARD → 17 AUXIN
32 =PP3V3_S0_EXCARD → 2 VIN3P3
32 =PP1V5_S0_EXCARD → 12 VIN1P5
42 IN SMC_EXCARD_PWR_EN → 20 SHDN*
TP_EXCARD_STBY_L → 1 STBY*
24 IN EXCARD_RESET_L → 6 SYSRST*
43 28 IN EXCARD_OC_L → 19 OC*
NC 4 NC0
NC 5 NC1
NC 13 NC2
NC 14 NC3
NC 16 NC4
7 GND
AUXOUT 15
VOUT3P3 3
VOUT1P5 11
PERST* 8
CPPE* 10
CPUSB* 9
RCLKEN 18 EXCARD_RCLKEN 32
THRML_PAD 21

R3500 0.1 MF-LF 402 2 5% 1/16W EXCARD_SHDN_L_R

PP3V3_S3_EXCARD_SWITCH 7 32
VOLTAGE=3.3V MIN_LINE_WIDTH=.3mm MIN_NECK_WIDTH=0.2mm
C3500 0.1uF 20% 10V CERM 402
C3503 10uF 20% 6.3V X5R 603

PP3V3_S0_EXCARD_SWITCH 7 32
VOLTAGE=3.3V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3501 0.1uF 10% 16V X5R 402
C3504 10uF 20% 6.3V X5R 603

PP1V5_S0_EXCARD_SWITCH 7 32
VOLTAGE=1.5V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3502 0.1uF 10% 16V X5R 402
C3505 10uF 20% 6.3V X5R 603

PLT_RESET_SWITCH_L 7 32
EXCARD_CPPE_L 7 32
EXCARD_CPUSB_L 7 32

CRITICAL
J3501
503219-0221
M-ST-SM

9 OUT FC_CLKREQ_L → 1
95 9 IN PCIE_CLK100M_FC_P → 3
95 9 IN PCIE_CLK100M_FC_N → 5
95 9 IN PCIE_FC_R2D_C_P → 11
95 9 IN PCIE_FC_R2D_C_N → 13
95 9 OUT PCIE_FC_D2R_P → 17
95 9 OUT PCIE_FC_D2R_N → 19
2 4 6 8 XNC 10 =PP3V3_FC_CONN 8 12 XNC 14 XNC 16 =PP1V5_FC_CONN 8 18 XNC 20 FC_PRSNT_L OUT 9 22 FC_RESET_L OUT 9
24 23 25 26
VENICE

VENICE
C3573 0.1uF 10% 16V X5R 402 PCIE_FC_R2D_P
C3572 0.1uF 10% 16V X5R 402 PCIE_FC_R2D_N
PLACEMENT_NOTE=Place close to J3501.

Venice Connector

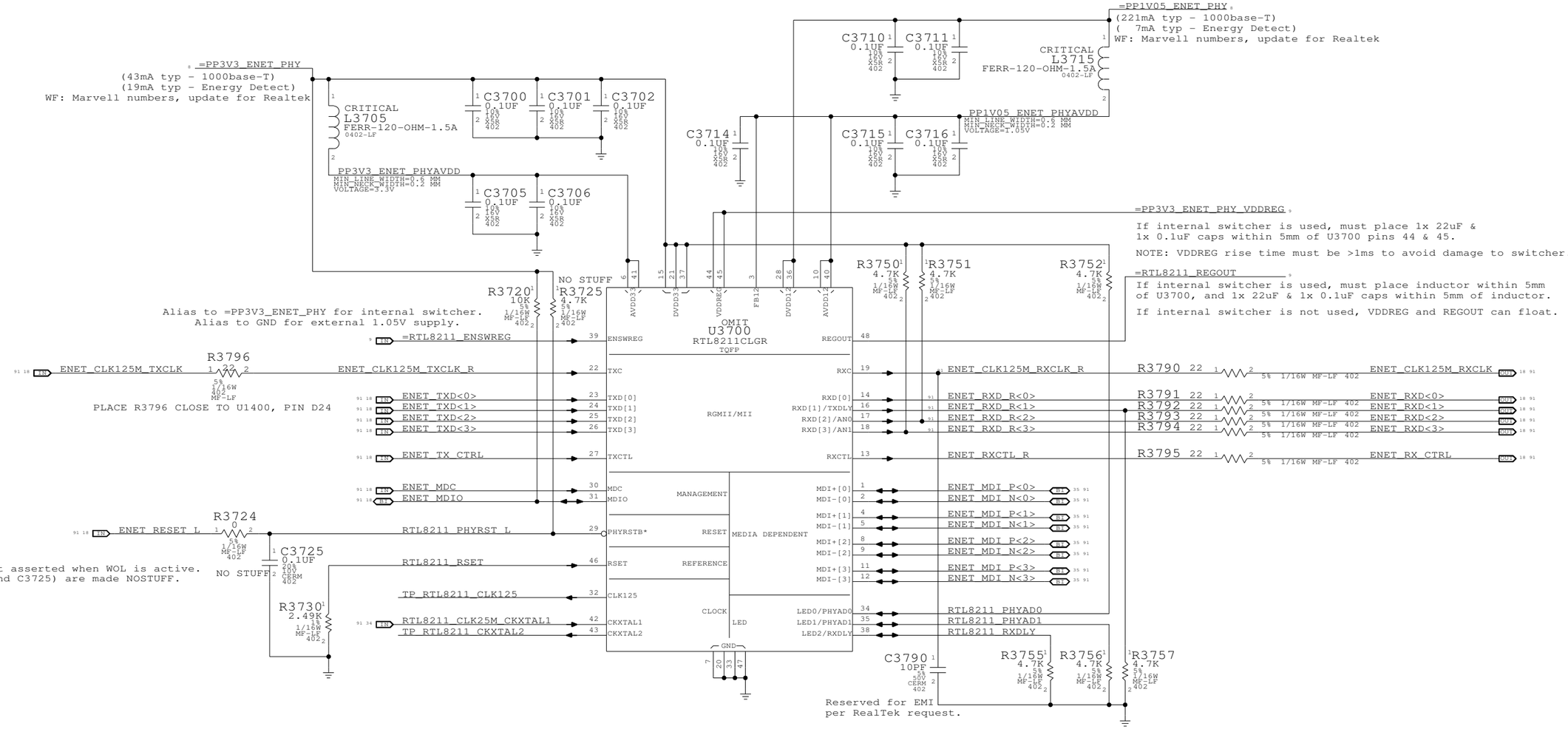
32 =PP3V3_S3_EXCARD
32 7 EXCARD_CPUSB_L → 1
32 7 EXCARD_CPPE_L → 2
U3551 74HC1G00GWDG SC70-5 5 3
SMC_EXCARD_CP OUT 42 43
C3550 0.1uF 20% 10V CERM 402

32 =PP3V3_S0_EXCARD
R3561 100K 1% 1/16W MF-LF 402
32 EXCARD_RCLKEN → 1
EXCARD_CLKREQ_CONN → 2
U3560 74HC1G00GWDG SC70-5 5 3
EXCARD_CLKREQ_L OUT 17
32 7 EXCARD_CLKREQ_CONN_L → B1
U3561 SN74LVC1G04YZPR BGA A2 C2 C1
C3560 0.1uF 20% 10V CERM 402

ExpressCard Connector
SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 32 OF 96	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

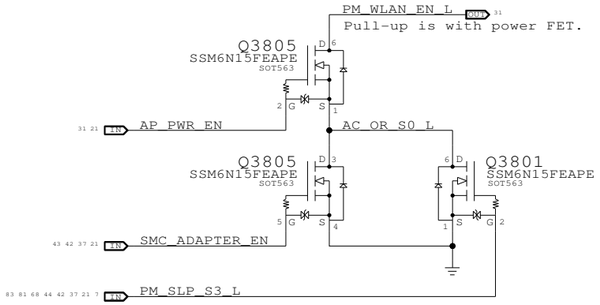
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 33 OF 96	

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

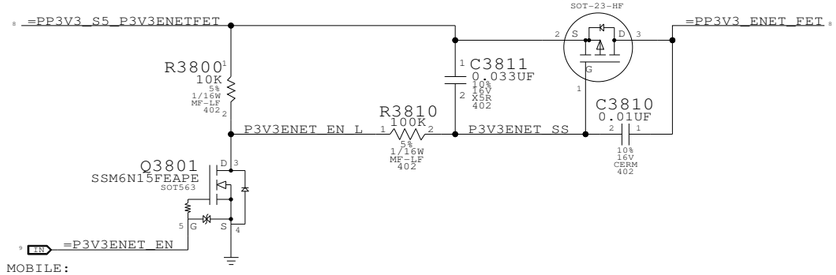
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL
Q3810
NTR4101P
SOT-23-HF



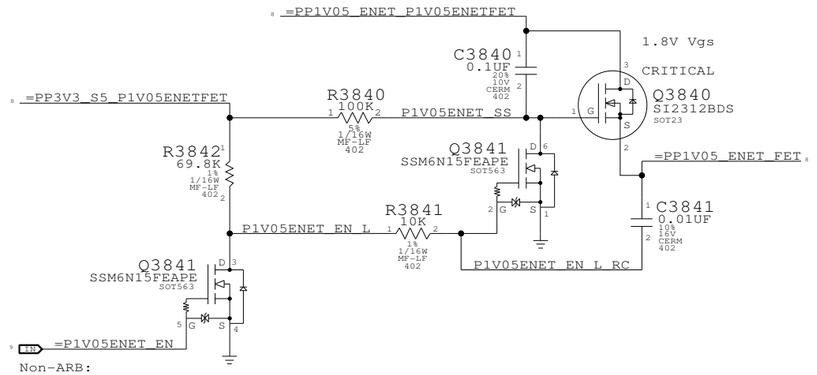
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

1.8V Vgs

CRITICAL
Q3840
SI2312BDS
SOT23

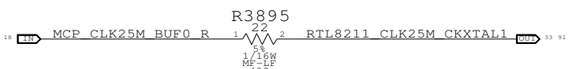


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

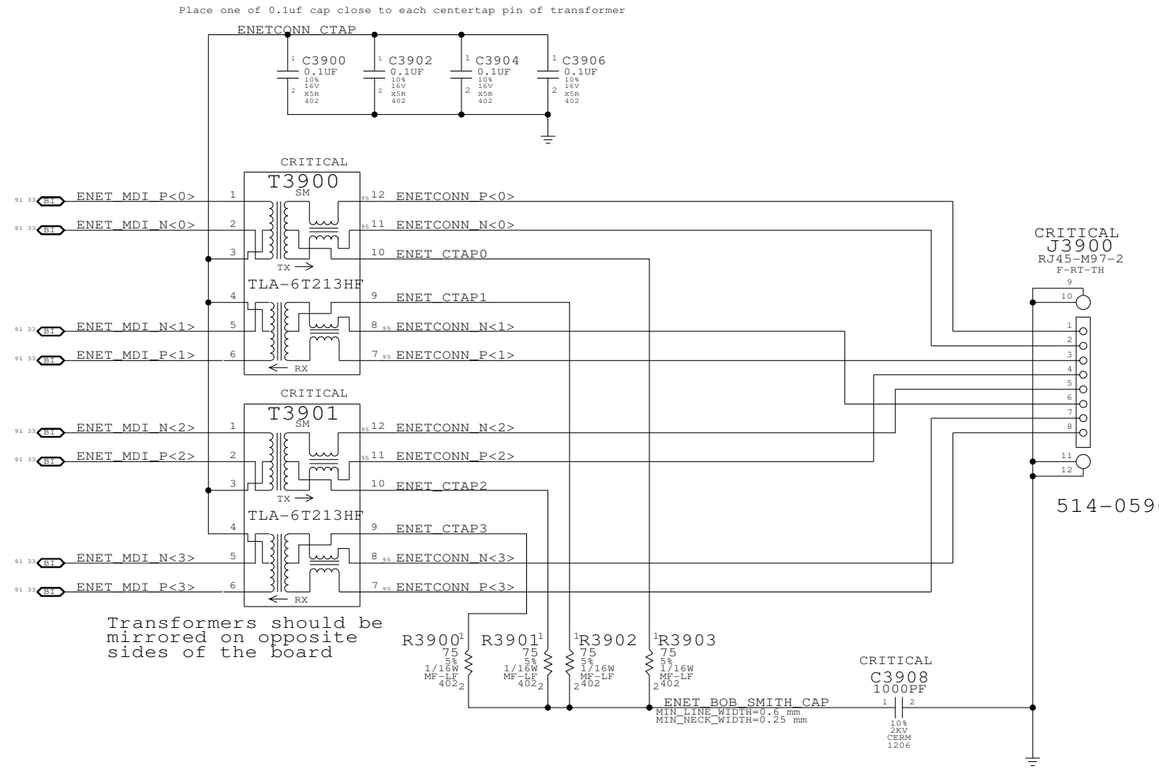
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 34 OF 96	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

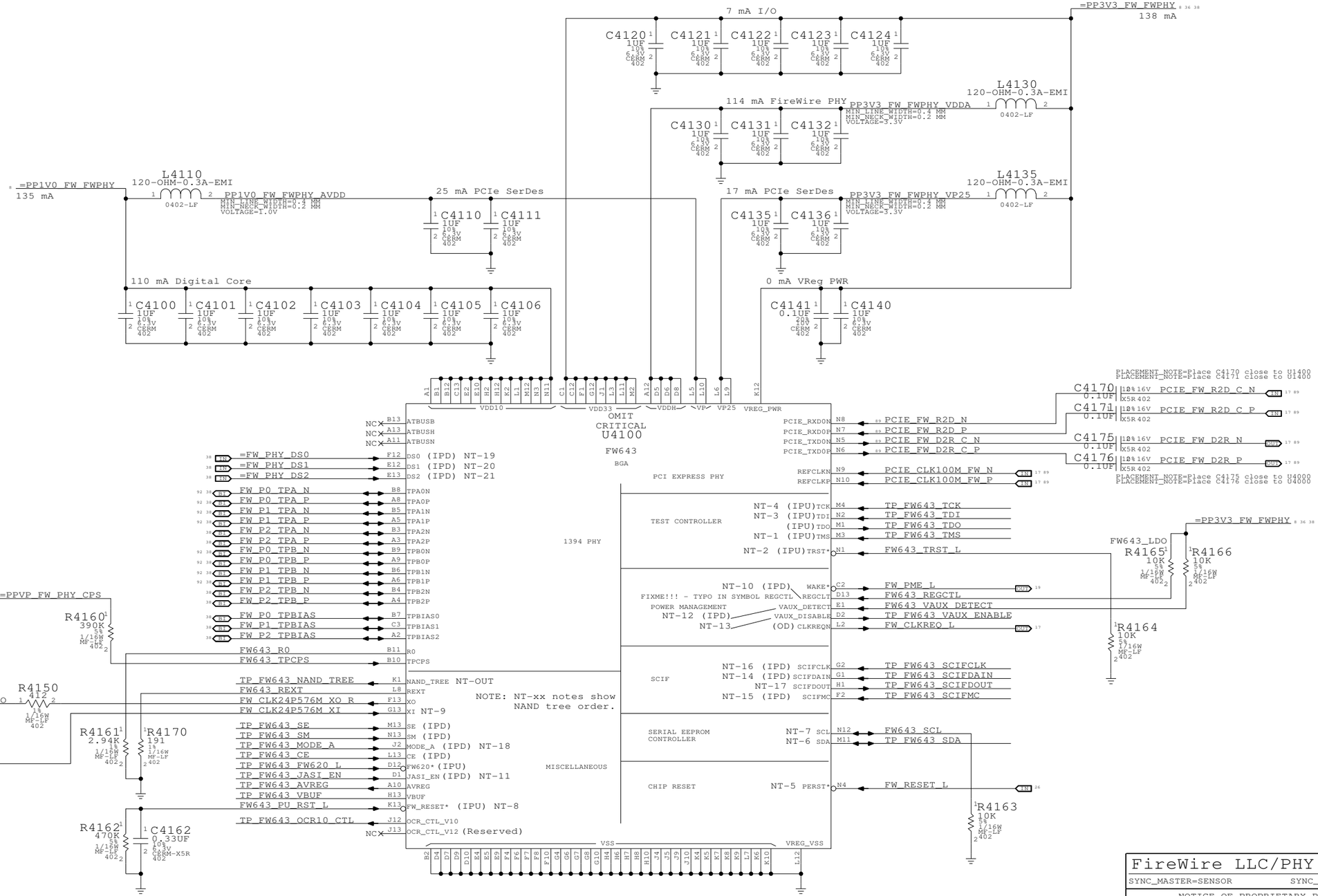


Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 35 OF 96	



FireWire LLC/PHY (FW643)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 36 OF 96	

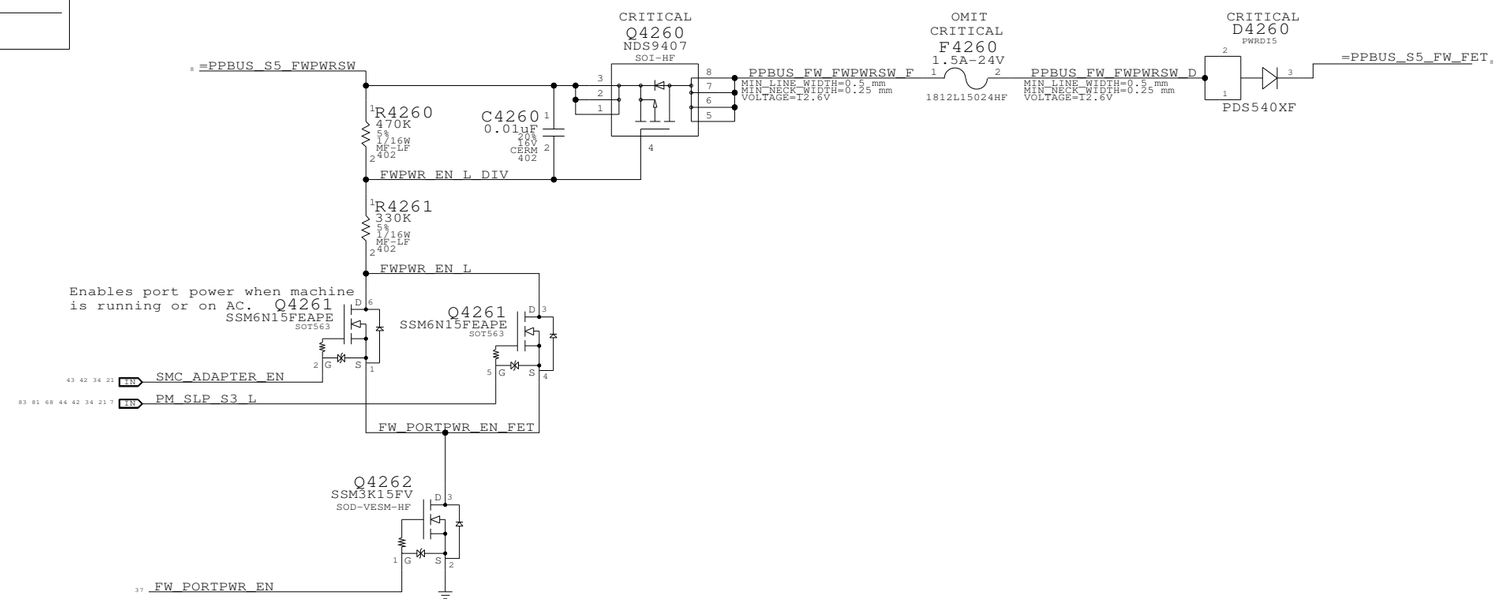
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

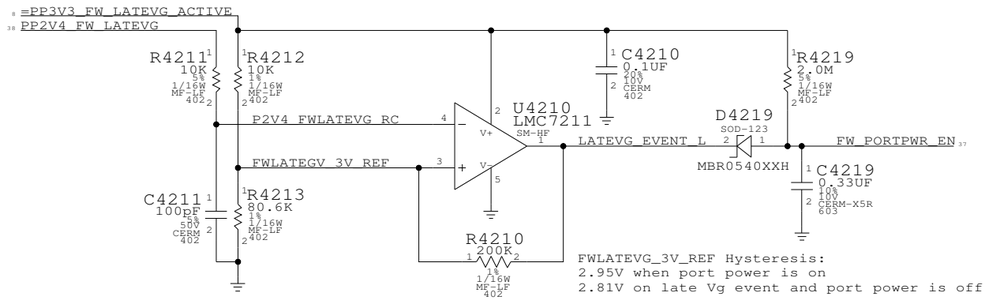
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
740S0080	1	LITTLEFUSE, 1.5A RESETTABLE 24V	F4260	CRITICAL	

FireWire Port Power

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 37 OF 96	

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

=PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE = =FW_PHY_DS0

FWPHY_DS2 MAKE_BASE=TRUE = =FW_PHY_DS2

FWPHY_DS1 MAKE_BASE=TRUE = =FW_PHY_DS1

R4381 10K 1% 1/16W MF-LF 402

FW_P0_TPBIAS = NC_FW0_TPBIAS MAKE_BASE=TRUE

FW_P2_TPBIAS = NC_FW2_TPBIAS MAKE_BASE=TRUE

FW_P0_TPA_N = NC_FW0_TPAN MAKE_BASE=TRUE

FW_P0_TPA_P = NC_FW0_TPAP MAKE_BASE=TRUE

FW_P2_TPA_N = NC_FW2_TPAN MAKE_BASE=TRUE

FW_P2_TPA_P = NC_FW2_TPAP MAKE_BASE=TRUE

FW_P0_TPB_N = NC_FW0_TPBN MAKE_BASE=TRUE

FW_P0_TPB_P = NC_FW0_TPBP MAKE_BASE=TRUE

FW_P2_TPB_N = NC_FW2_TPBN MAKE_BASE=TRUE

FW_P2_TPB_P = NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 16V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

FW_P1_TPA_P = FW_PORT1_TPA_P MAKE_BASE=TRUE

FW_P1_TPA_N = FW_PORT1_TPA_N MAKE_BASE=TRUE

FW_P1_TPB_P = FW_PORT1_TPB_P MAKE_BASE=TRUE

FW_P1_TPB_N = FW_PORT1_TPB_N MAKE_BASE=TRUE

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

=PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW SOT-363 (SYM-VER1)

PPVP_FW_CPS MAKE_BASE=TRUE MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=12.6V = =PPVP_FW_PHY_CPS

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

=PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

"Snapback" & "Late VG" Protection

PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363

C4311 0.01uF 10% 50V X7R 402

DP4310 BAV99DW-X-G SOT-363

C4310 0.01uF 10% 50V X7R 402

FW_PORT1_TPB_N

FW_PORT1_TPB_P

FW_PORT1_TPA_N

FW_PORT1_TPA_P

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

DP4311 BAV99DW-X-G SOT-363

C4313 0.01uF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

=PPVP_FW_PORT1

CRITICAL
L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1
BILINGUAL

CRITICAL
J4310 1394B-M97 F-RT-TH1

1	TPB-	TPB(R)
9	TPB+	TPB<R>
2	TPA-	TPA(R)
8	VP	
NC	VC	
6	VG	
3	TPA-	TPA-
5	TPA+	TPA<R>
4	TPA+	TPA(R)
10	CABLE OUTER SHLD	
11		
12	CHASSIS GND	
13		
14		
15		

OUTPUT

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

INPUT

514S0605

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power

=PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V

CRITICAL
D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

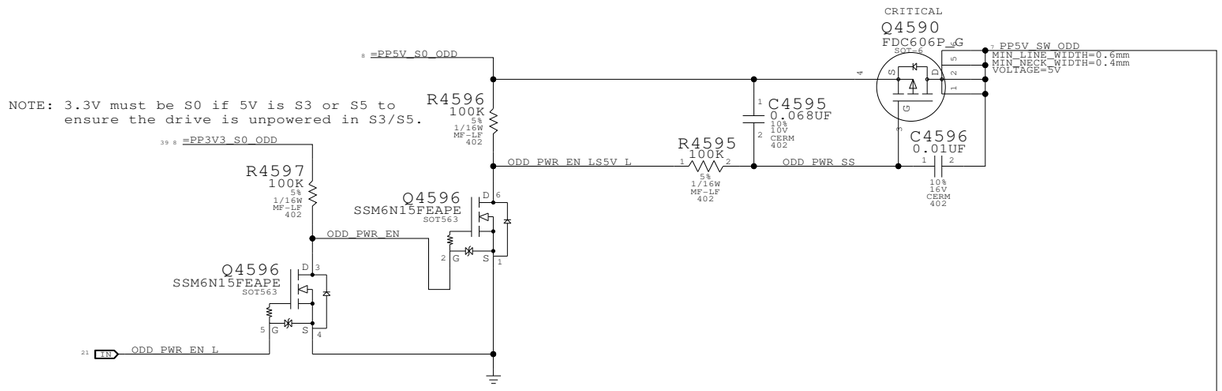
FireWire Ports

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

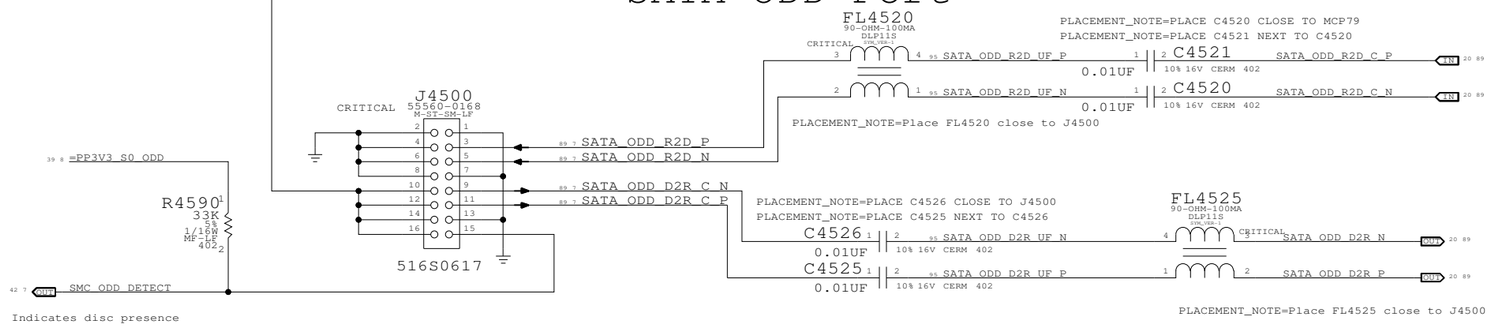
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 38 OF 96	

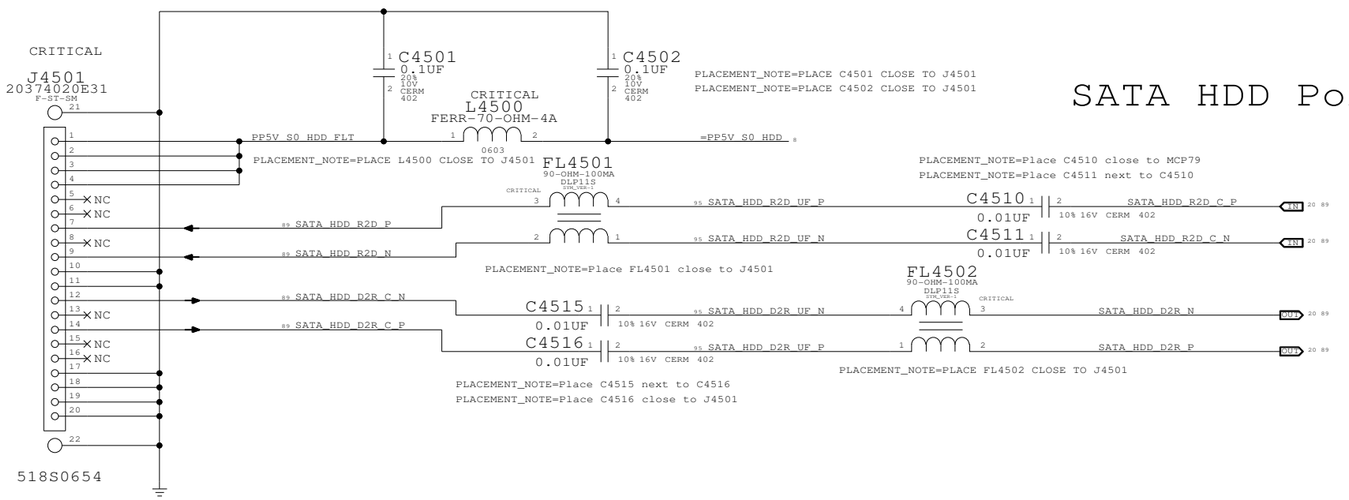
ODD Power Control



SATA ODD Port



SATA HDD Port



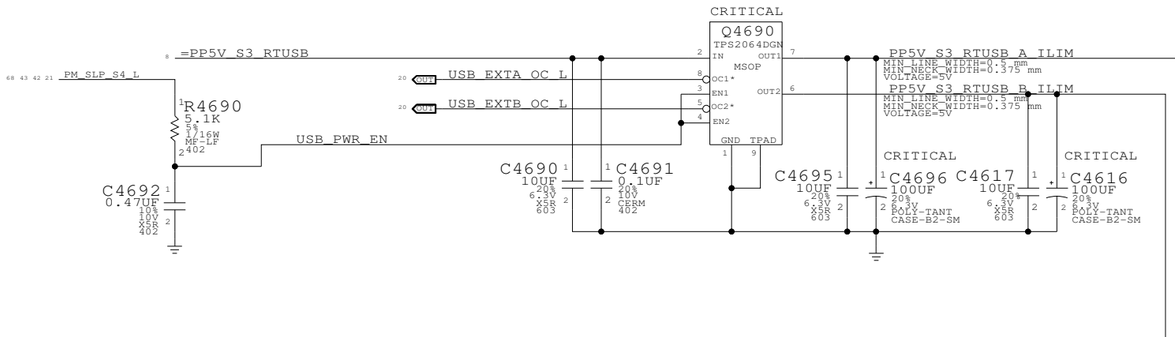
SATA Connectors

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

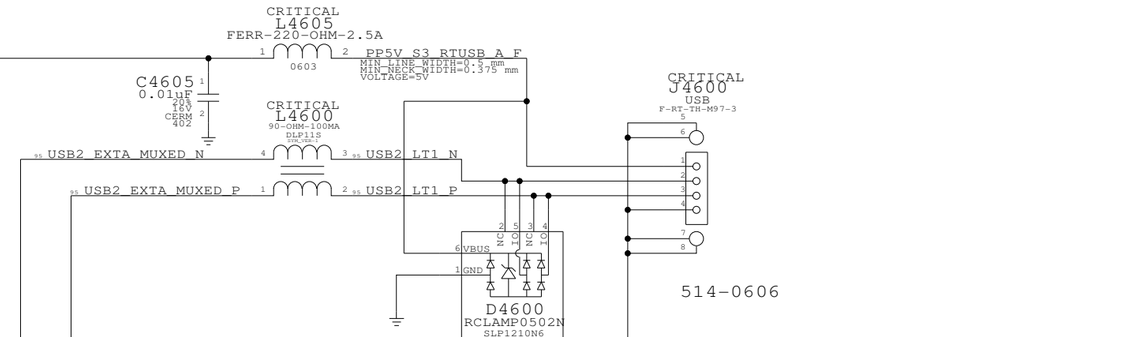
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 39 OF 96	

Port Power Switch

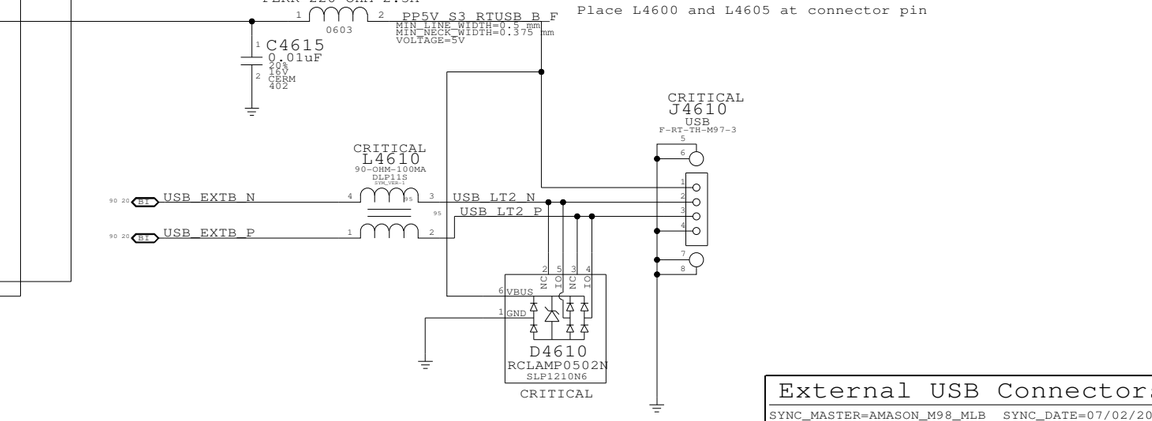


Left USB Port A

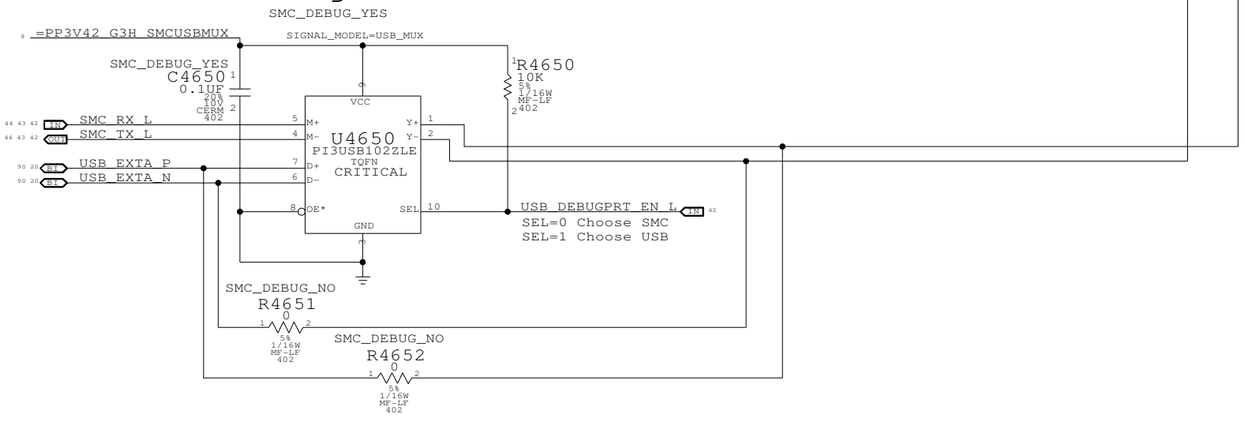


We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin



USB/SMC Debug Mux



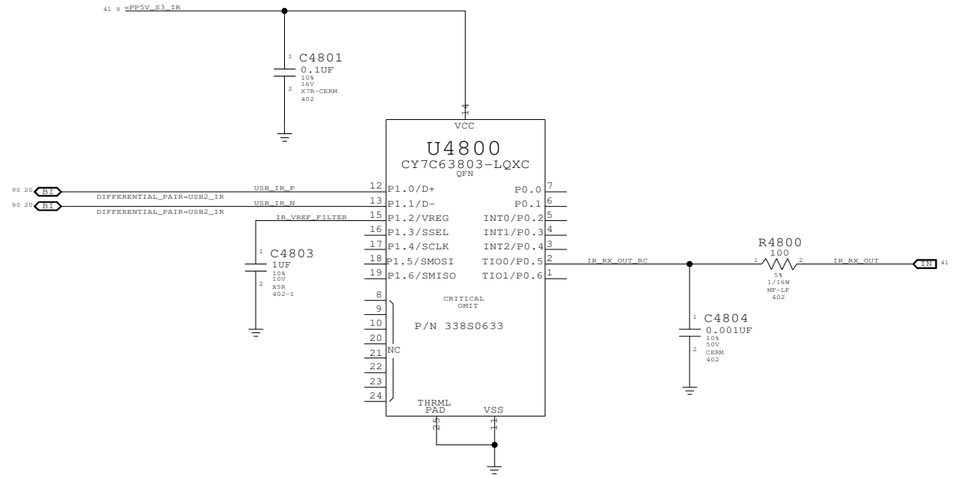
Left USB Port B

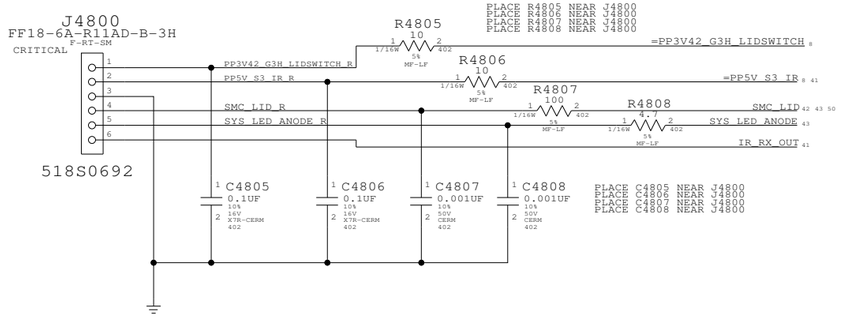
External USB Connectors

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 40 OF 96	





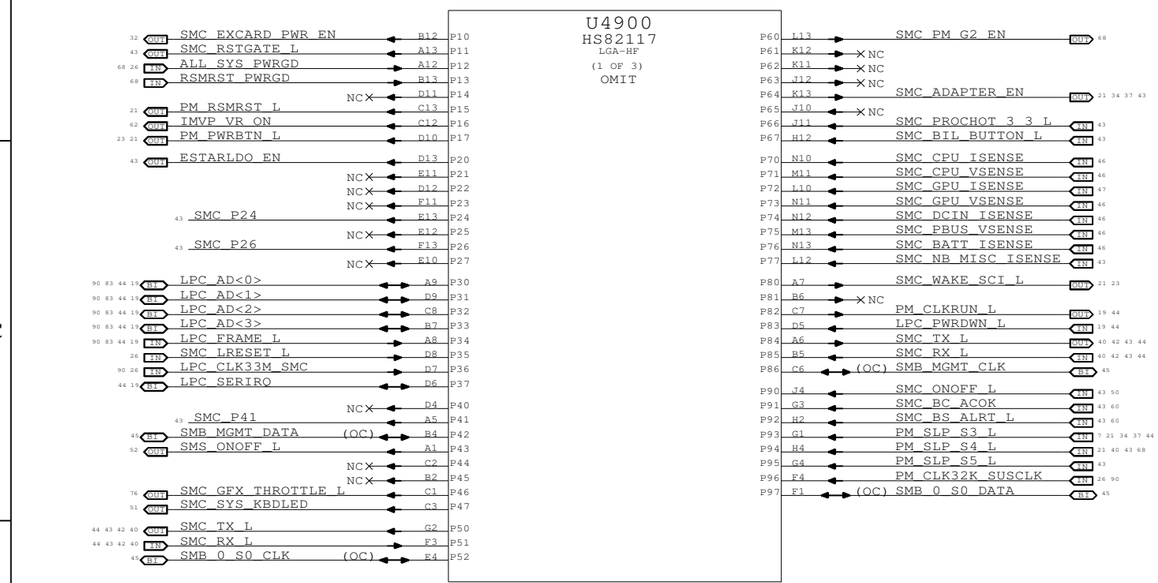
Front Flex Support

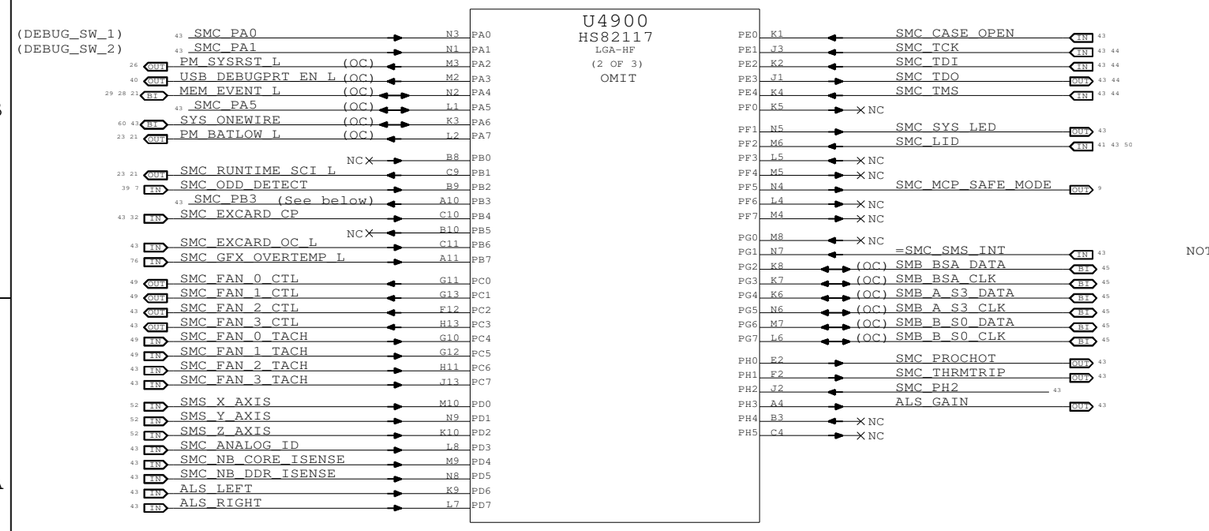
SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 41 OF 96	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

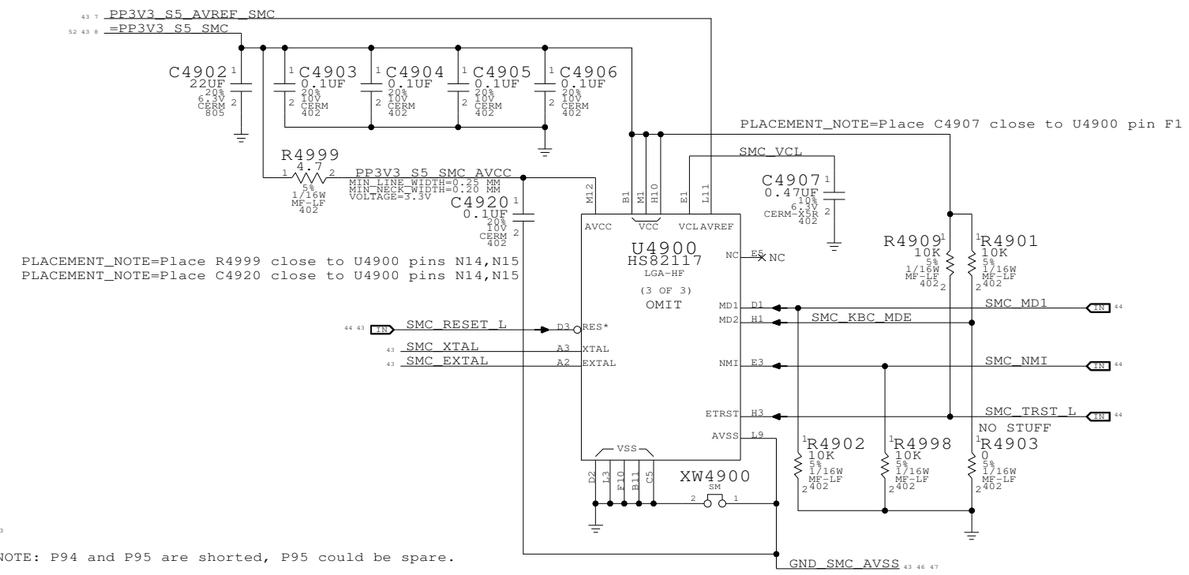




(DEBUG_SW_1)
(DEBUG_SW_2)

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

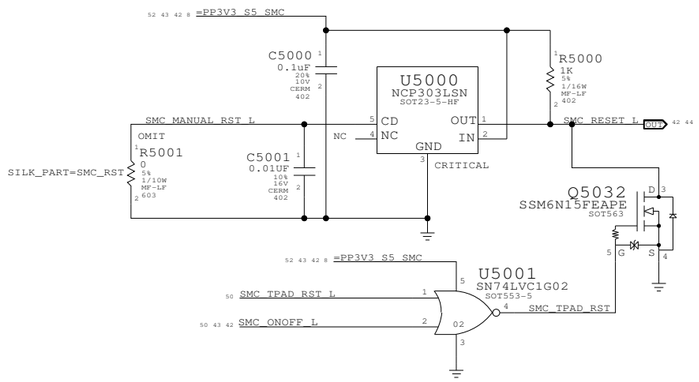
NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC	
SYNC_MASTER=T18_MLB	SYNC_DATE=06/18/2008

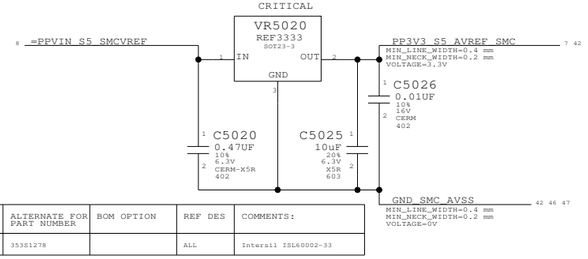
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 42 OF 96	

SMC Reset "Button" / Brownout Detect

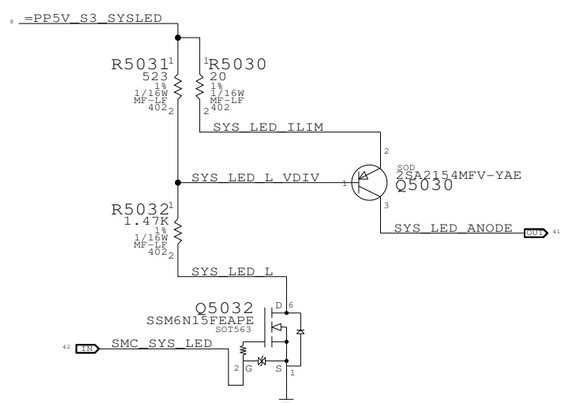


SMC AVREF Supply

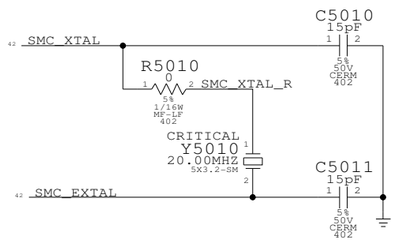


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL6002-33

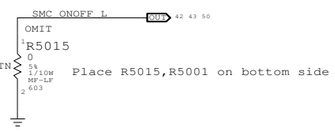
System (Sleep) LED Circuit



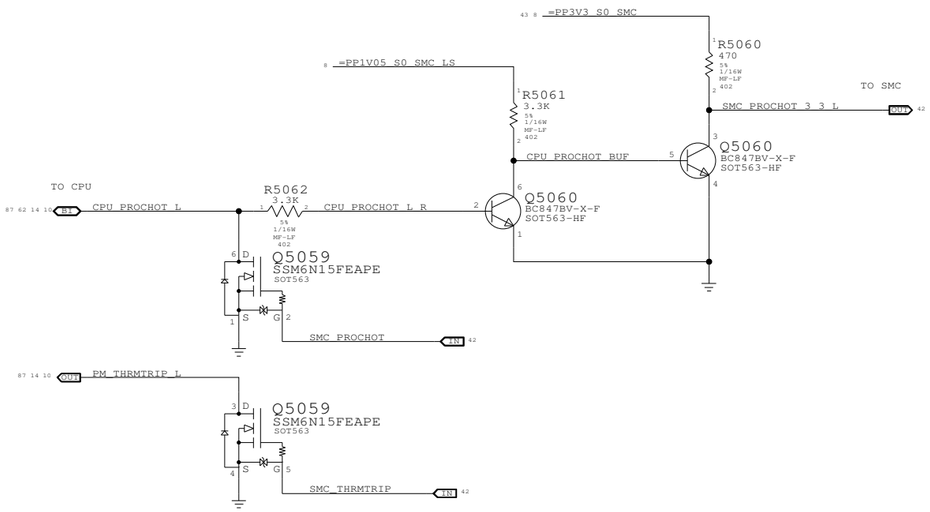
SMC Crystal Circuit



Debug Power "Button"



SMC FSB to 3.3V Level Shifting



SMC Support

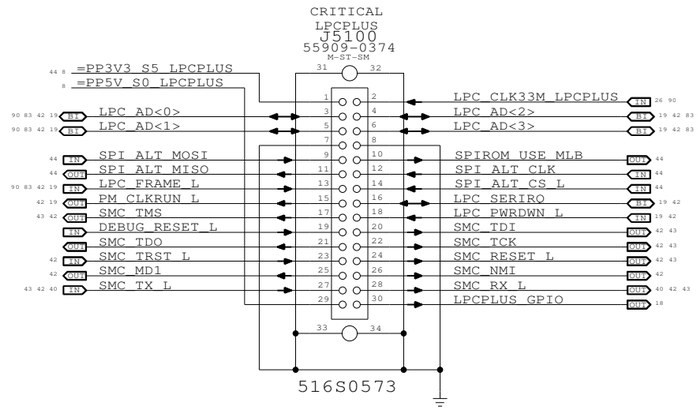
SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 43 OF 96	

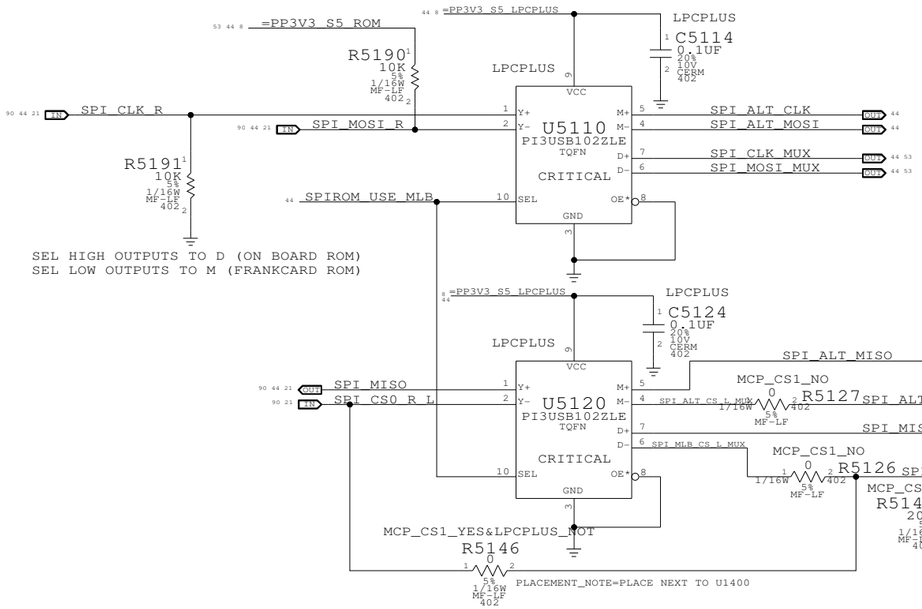
Place R5015,R5001 on bottom side

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

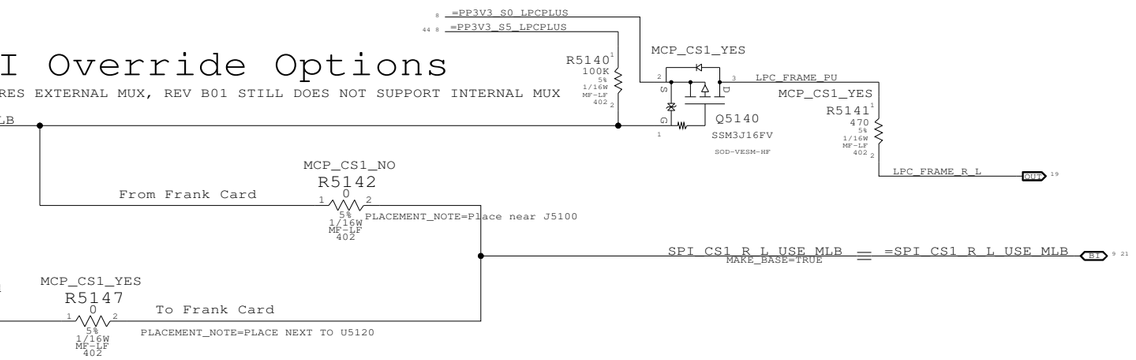


MCP79 Internal SPI MUX Support

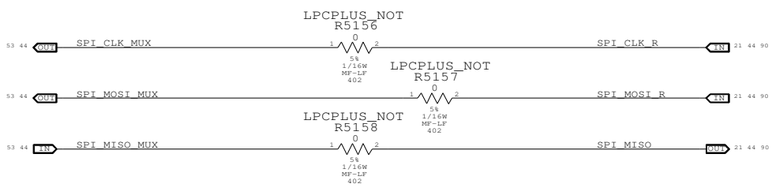
NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

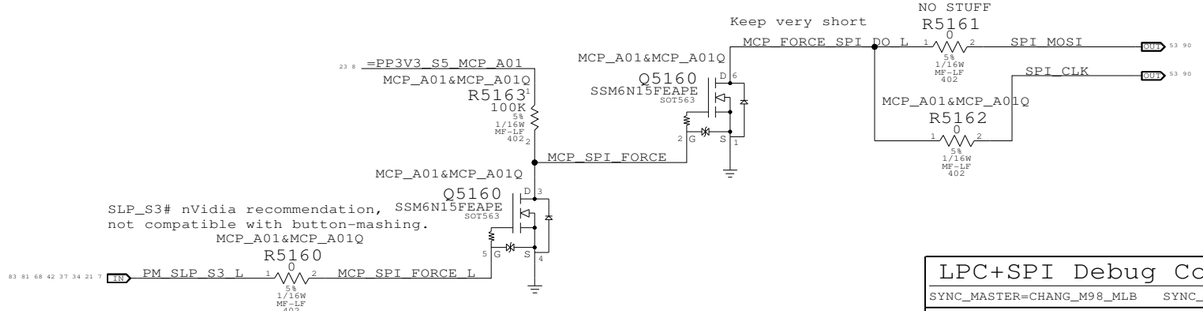


SPI MUX BYPASS



SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED.NOT NEEDED FOR B01 OR LATER.



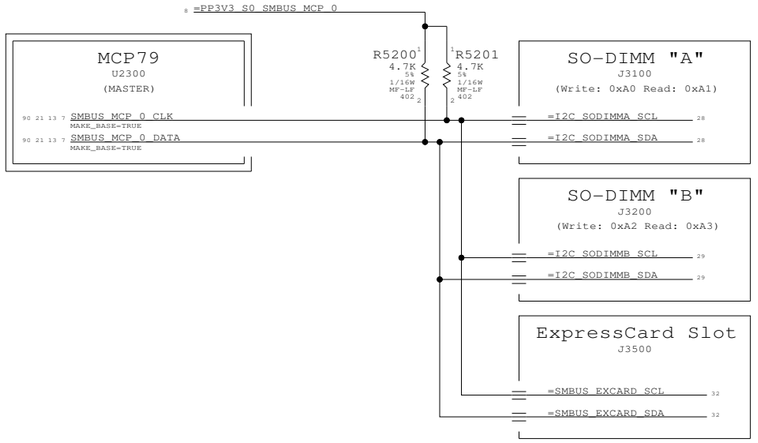
LPC+SPI Debug Connector

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

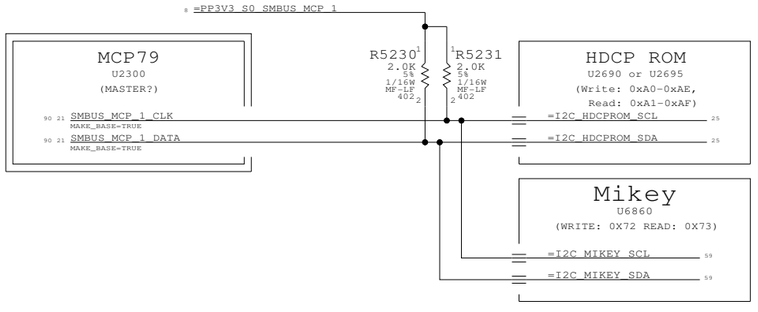
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 44 OF 96	

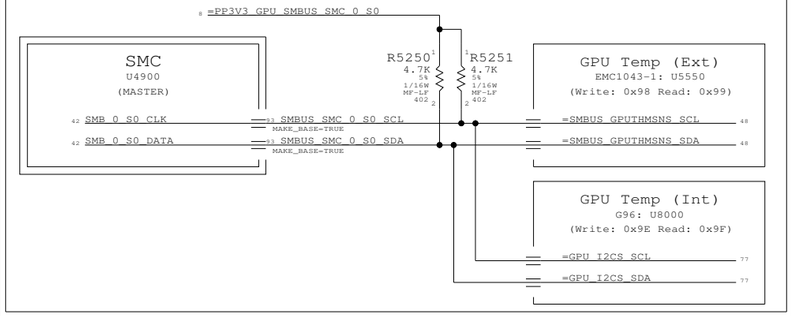
MCP79 SMBus "0" Connections



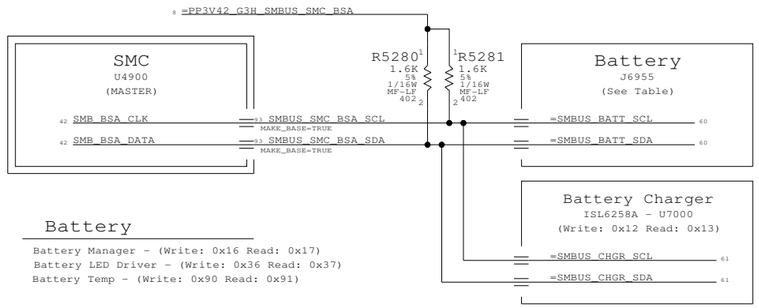
MCP79 SMBus "1" Connections



SMC "0" SMBus Connections



SMC "Battery A" SMBus Connections

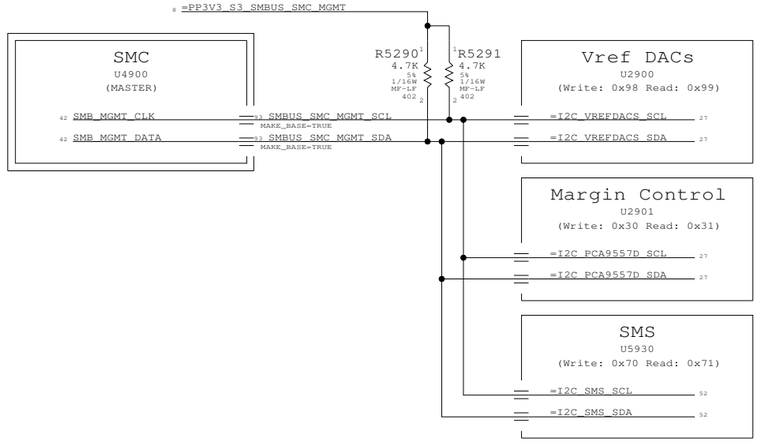


Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

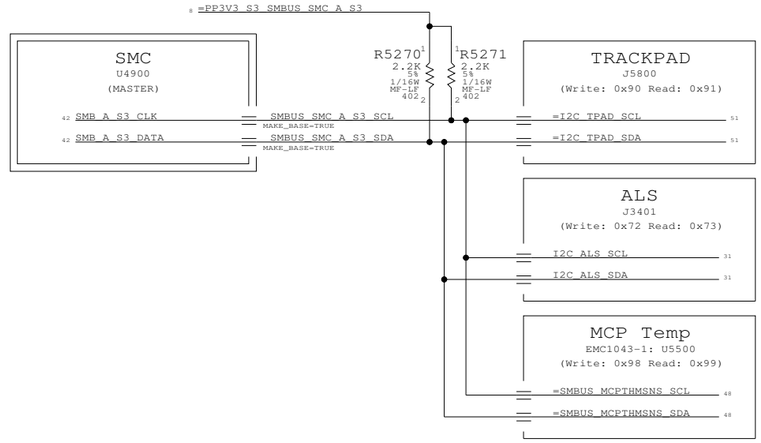
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

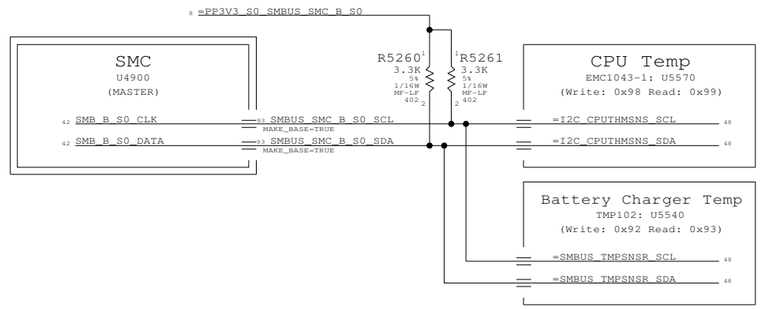


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



M98 SMBus Connections

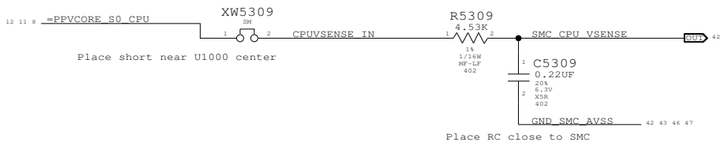
SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

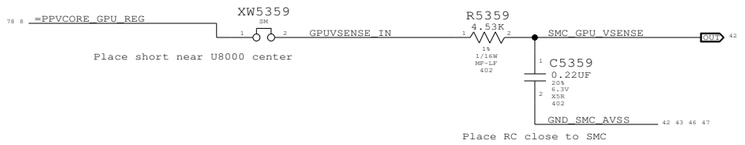
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	45	96

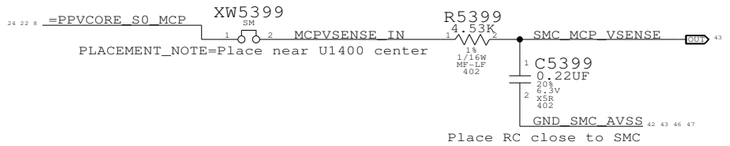
CPU Voltage Sense / Filter



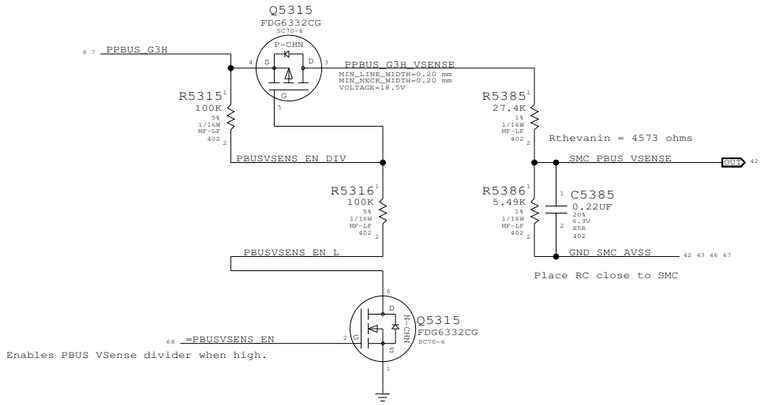
GPU Voltage Sense / Filter



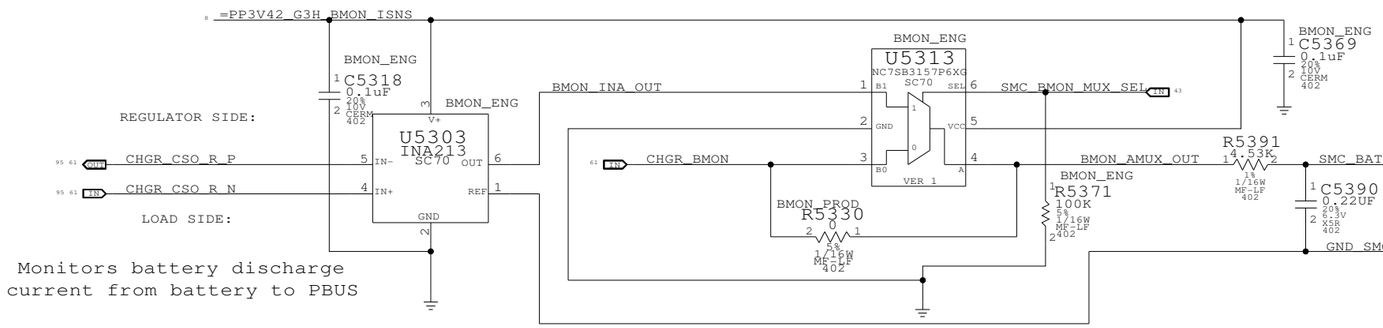
MCP Voltage Sense / Filter



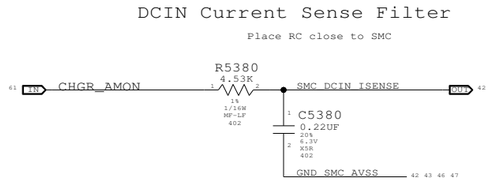
PBUS Voltage Sense & Filter



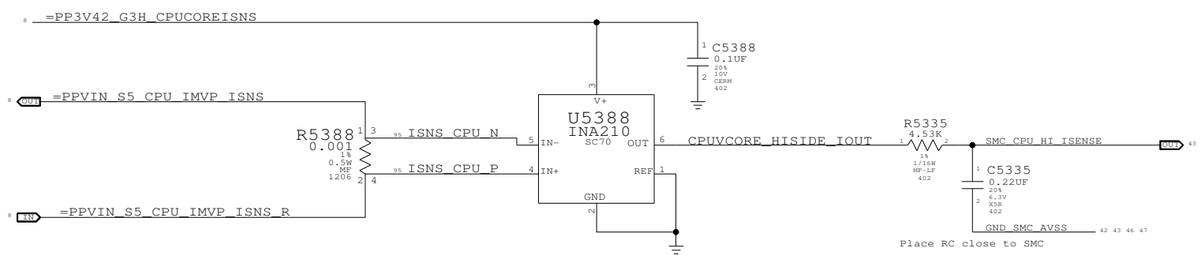
BMON Current Sense - Entire circuit must be near SMC (U4900)



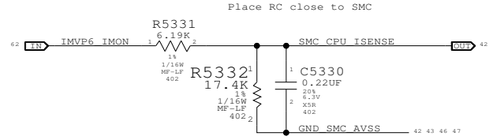
DCIN Current Sense Filter



CPU VCore High Side Current Sensor



CPU VCore Load Side Current Sense / Filter



Current & Voltage Sensing

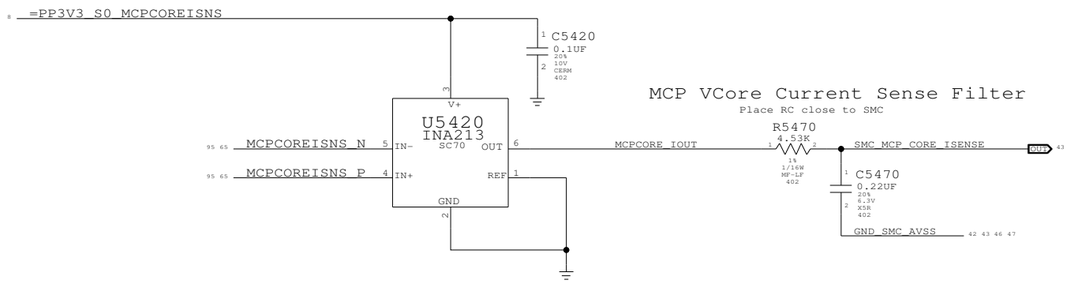
SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

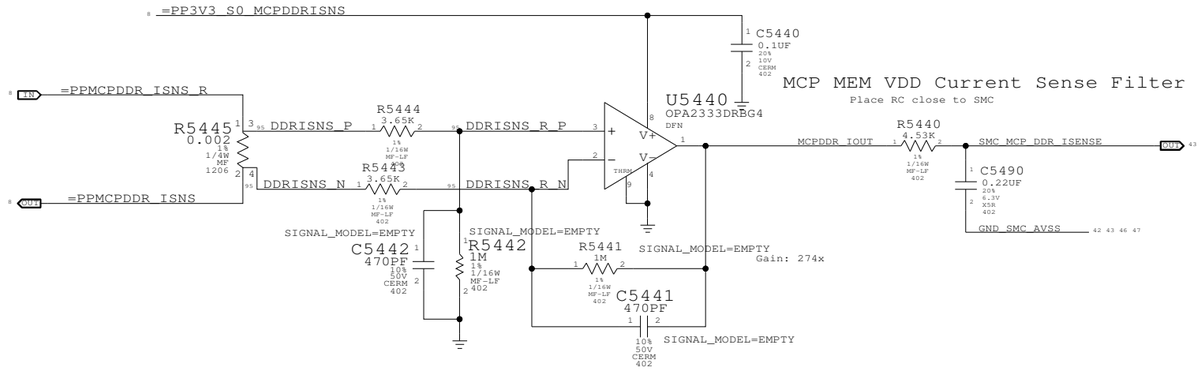
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	46	96

MCP VCore Current Sense



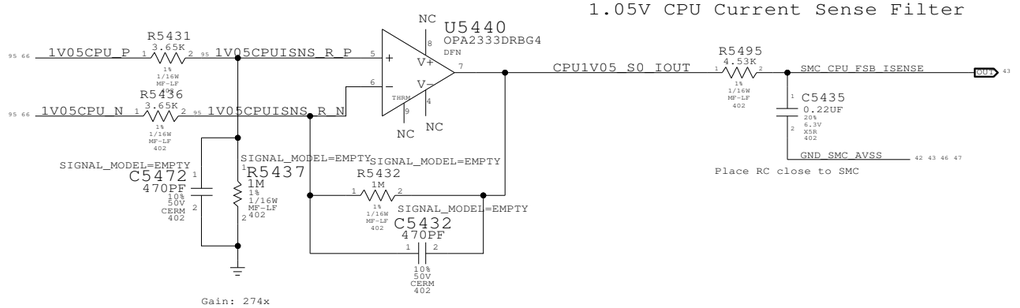
MCP MEM VDD Current Sense



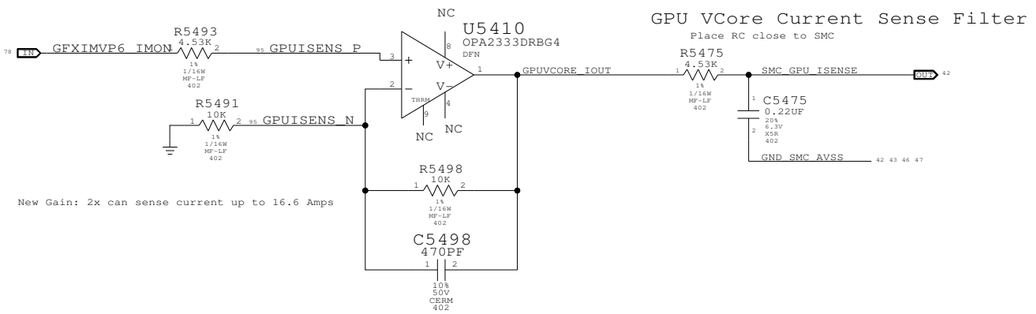
OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense

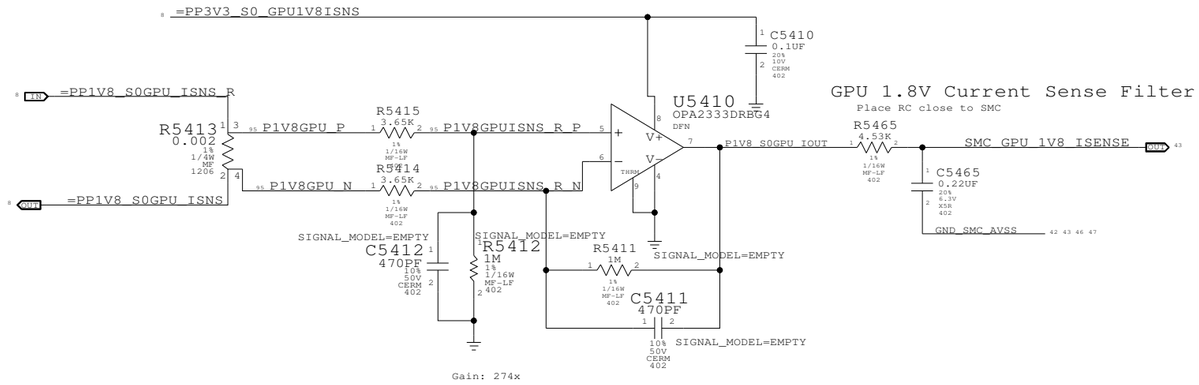


GPU VCore Current Sense



GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

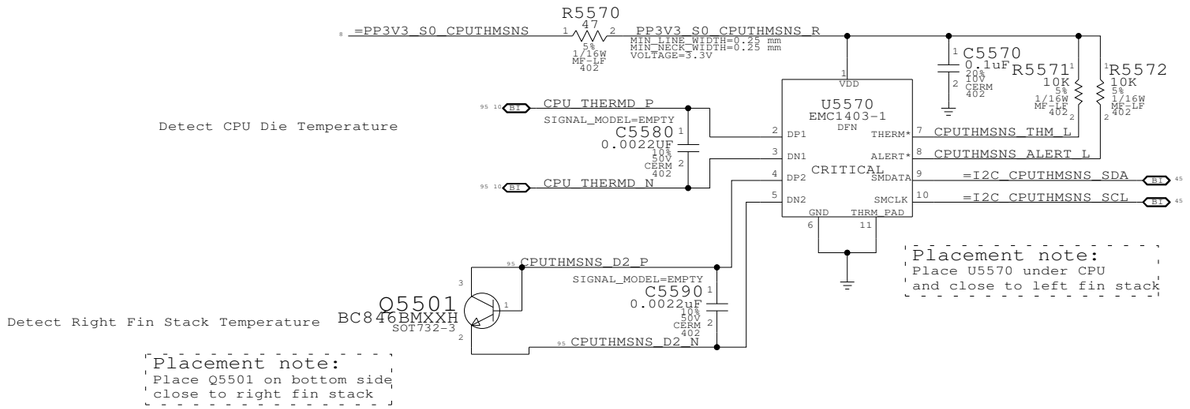
GPU 1.8V Current Sense



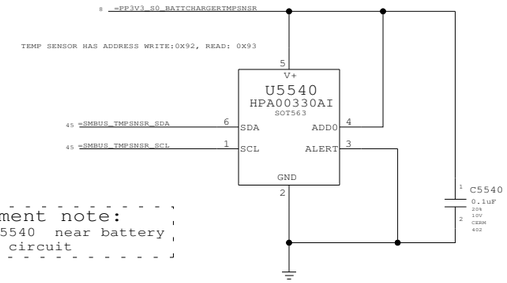
Current Sensing		
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
	SCALE: NONE	SHT 47 OF 96	

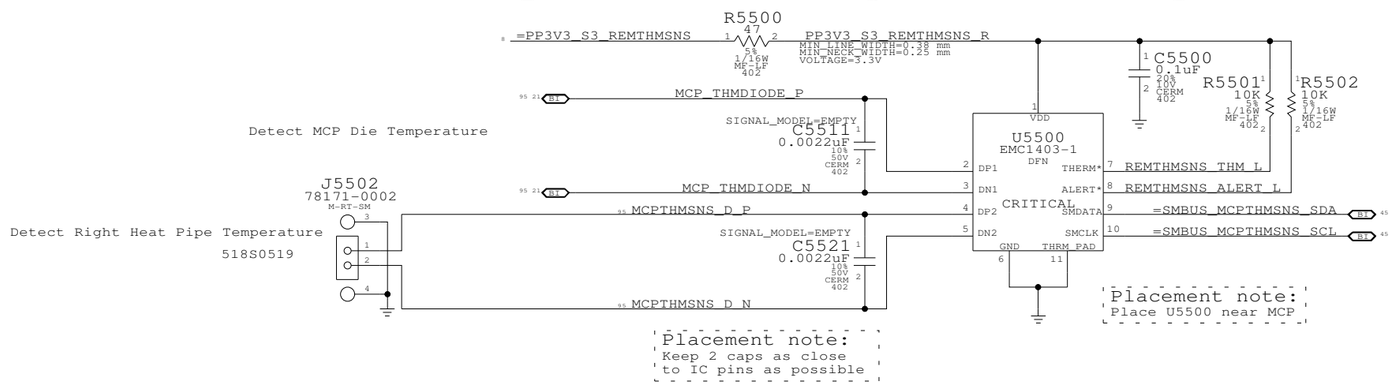
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity

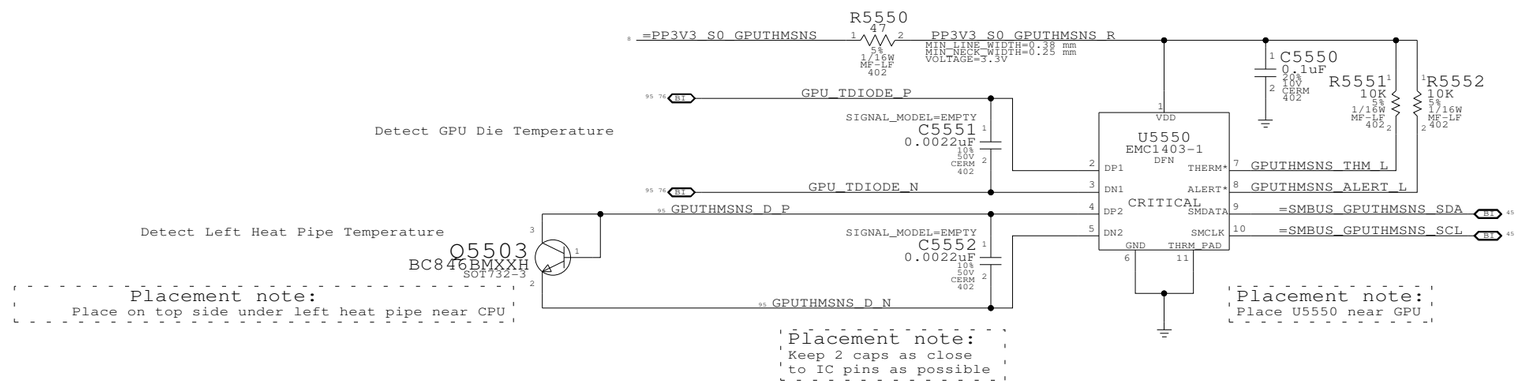


MCP Proximity/MCP Die/Right Heat Pipe



Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



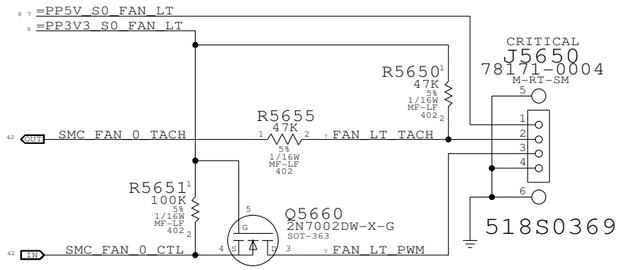
Thermal Sensors

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

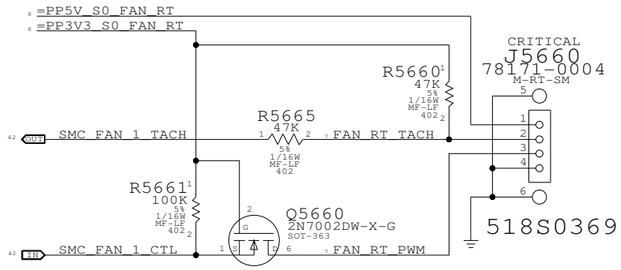
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 48 OF 96	

Left Fan



Right Fan



Fan Connectors

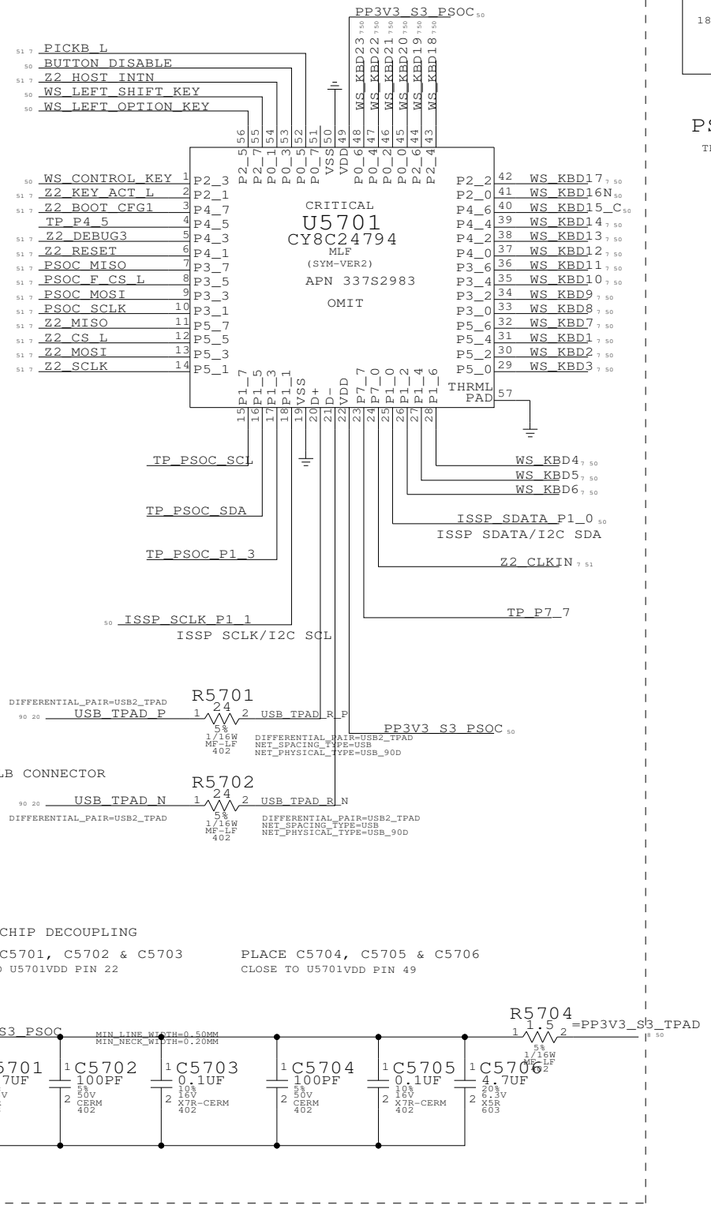
SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 49 OF 96	

PSOC USB CONTROLLER

USB INTERFACES TO MLB TRACKPAD PICK BUTTONS
SPI HOST TO Z2 KEYBOARD SCANNER



U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701VDD PIN 22

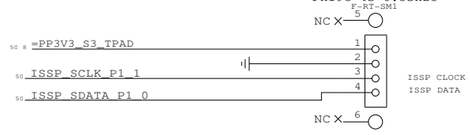
PLACE C5704, C5705 & C5706
CLOSE TO U5701VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

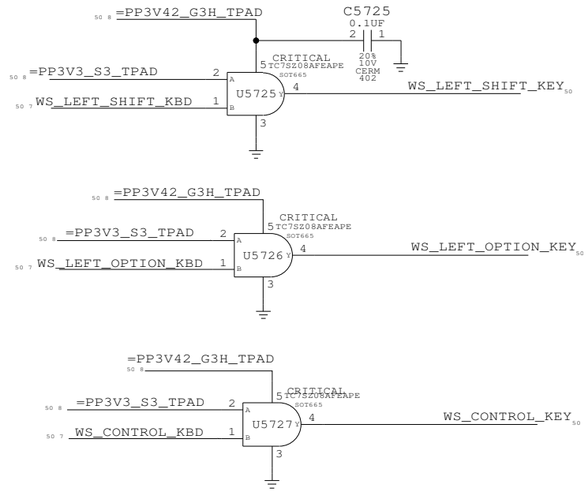
PSOC PROGRAMMING CONNECTOR

TPAD_DEBUG
APN 518S0430

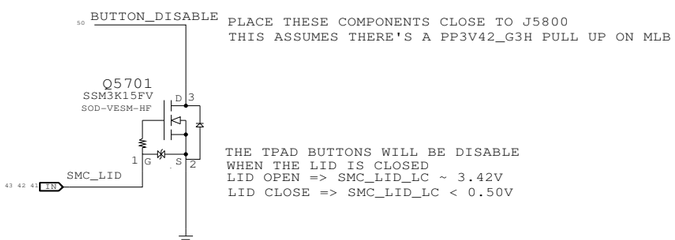
TEST POINTS ARE FOR ON BOARD PROGRAMMING



ISOLATION CIRCUIT



TPAD BUTTONS DISABLE

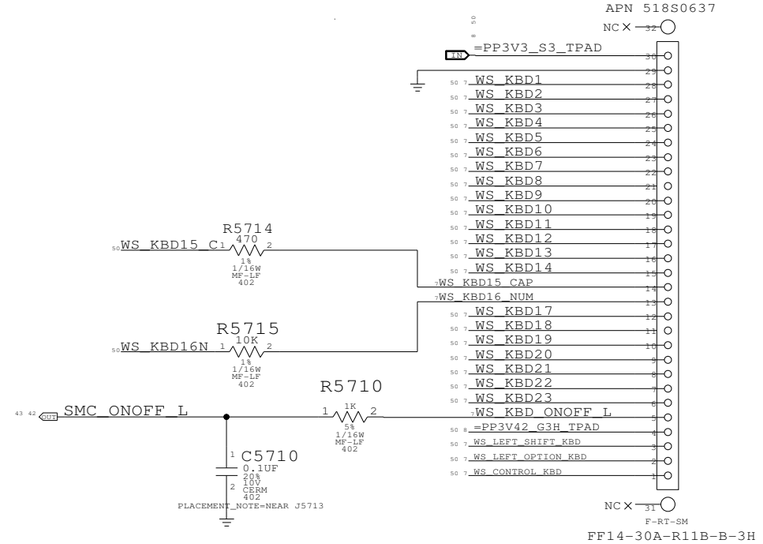


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

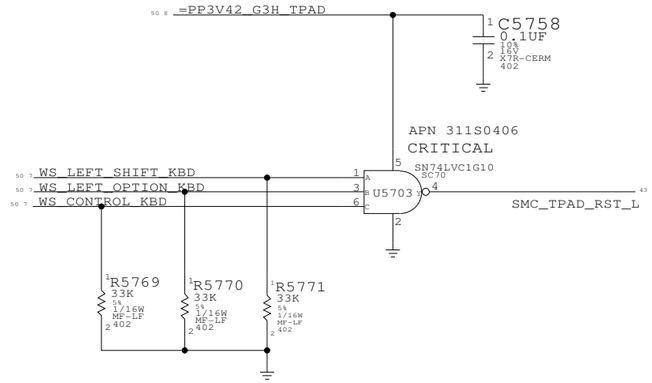
KEYBOARD CONNECTOR

J5713
APN 518S0637



FF14-30A-R11B-B-3H

SMC_MANUAL_RESET LOGIC



WELLSPRING 1

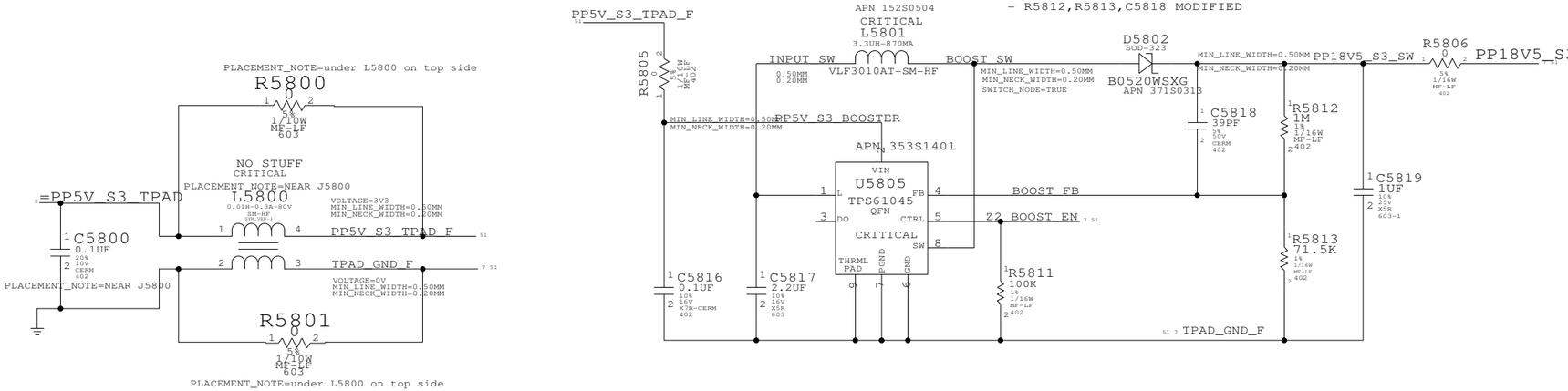
SYNC_MASTER=AMASON_M93 SYNC_DATE=06/18/2008

APPLE INC.

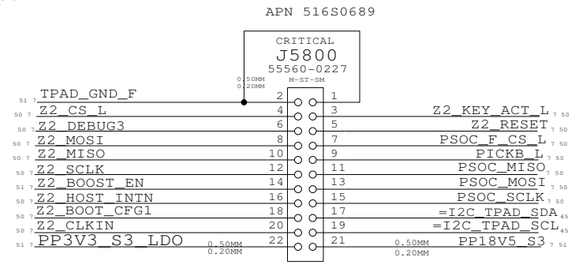
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 50 OF 96	

BOOSTER +18.5VDC FOR SENSORS

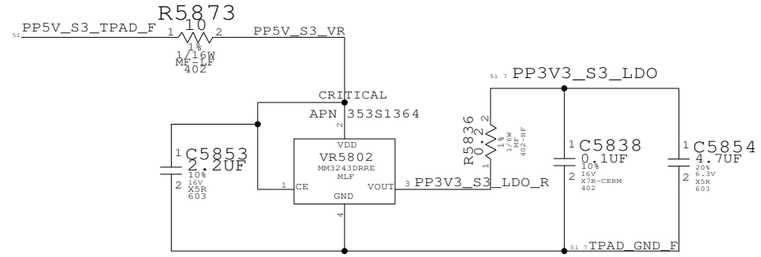
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



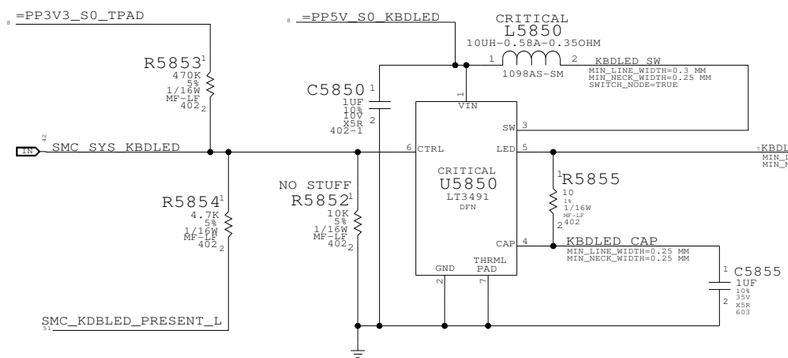
3V3 LDO FOR IPD

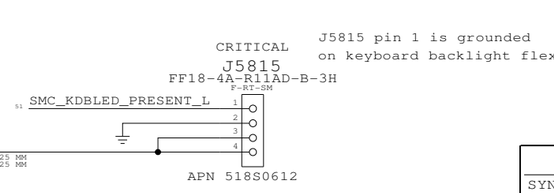


Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

WELLSPRING 2

SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008

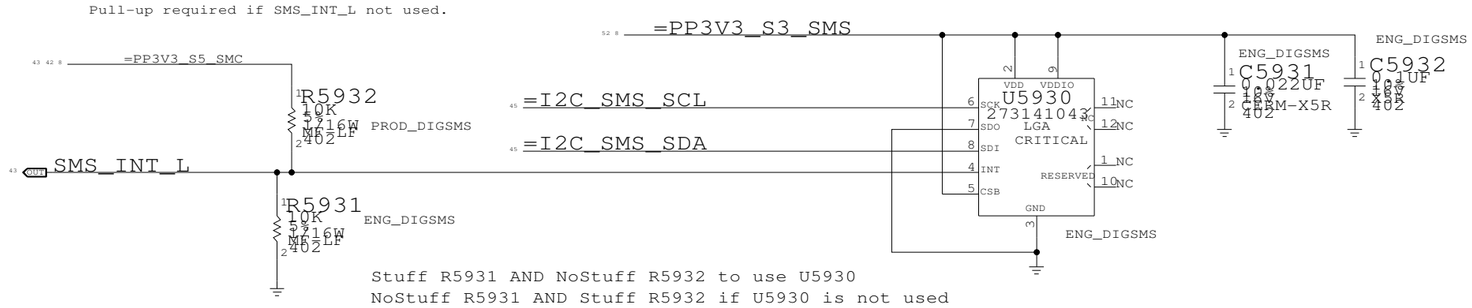
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

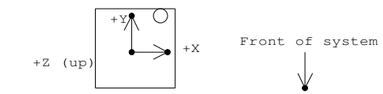
SCALE: NONE

SHT 51 OF 96

Digital SMS



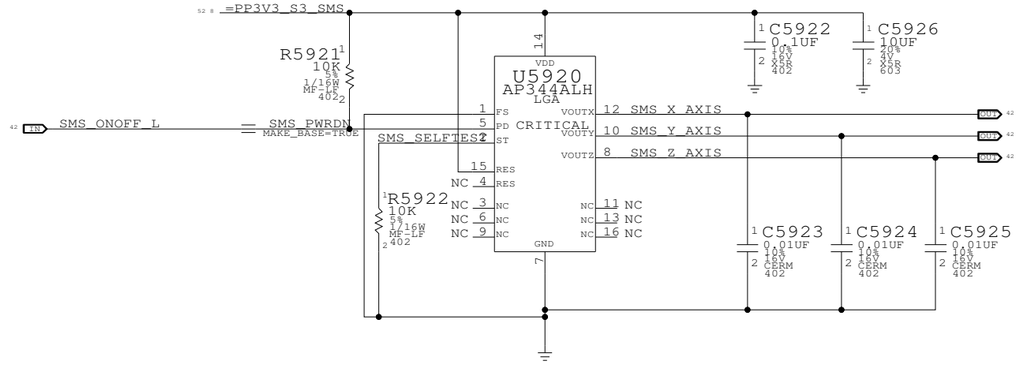
Desired orientation when placed on board top-side:



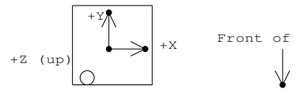
Circle indicates pin 1 location when placed in correct orientation

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



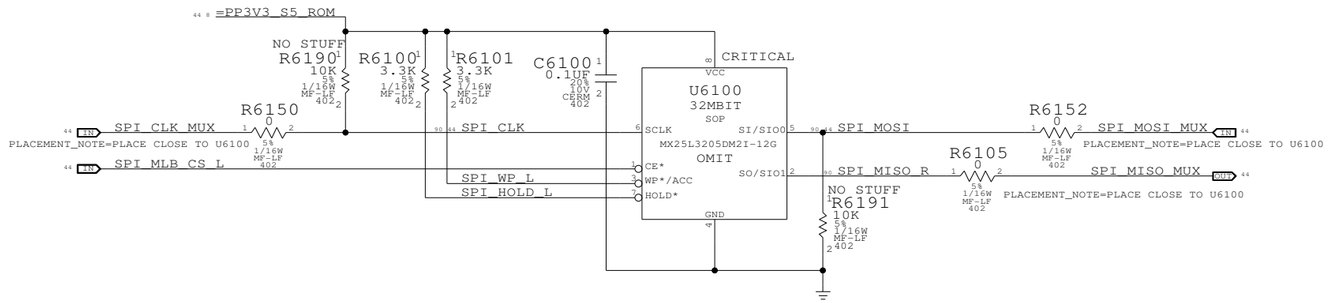
Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 52 OF 96	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

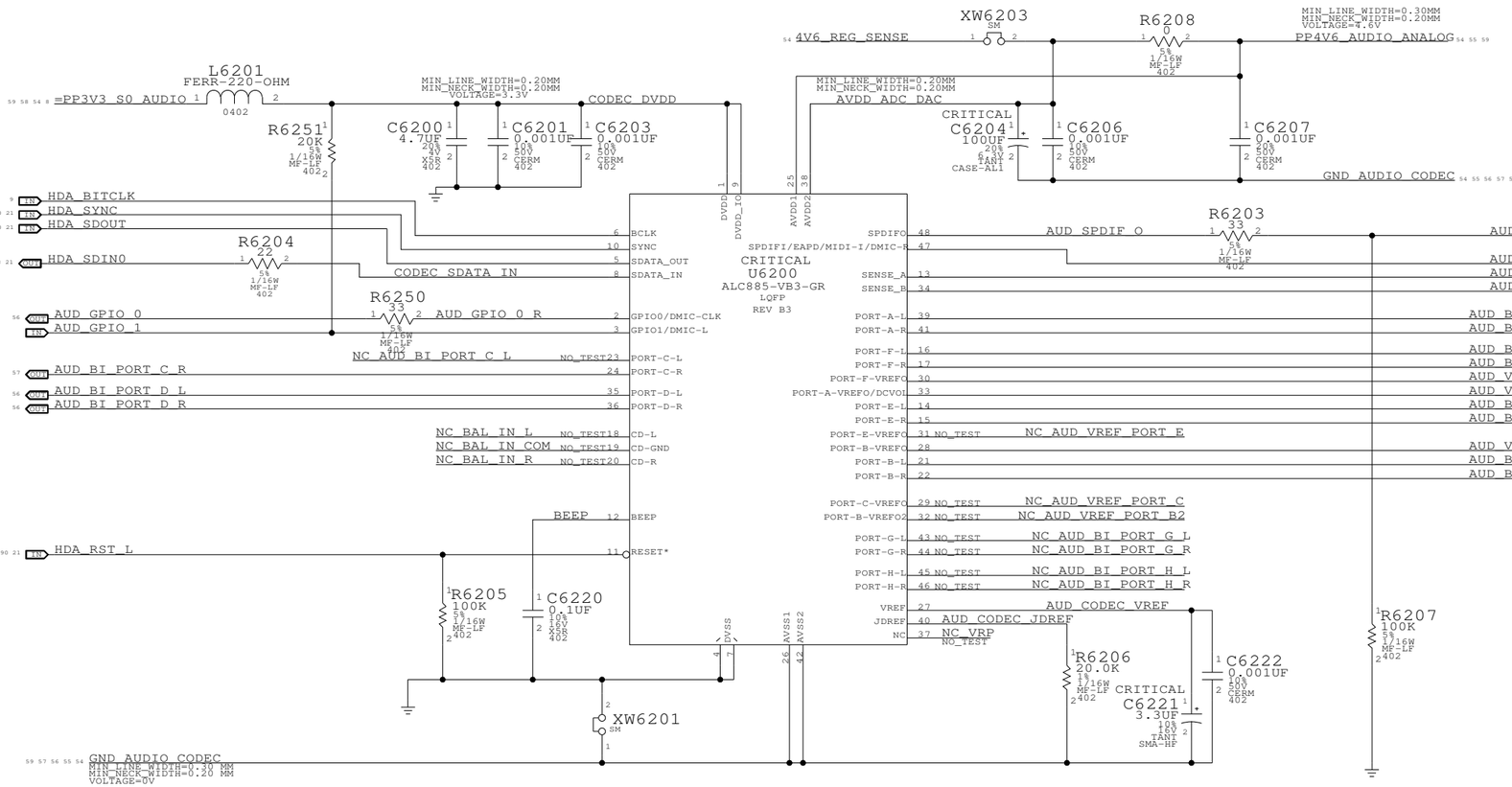
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	53	96

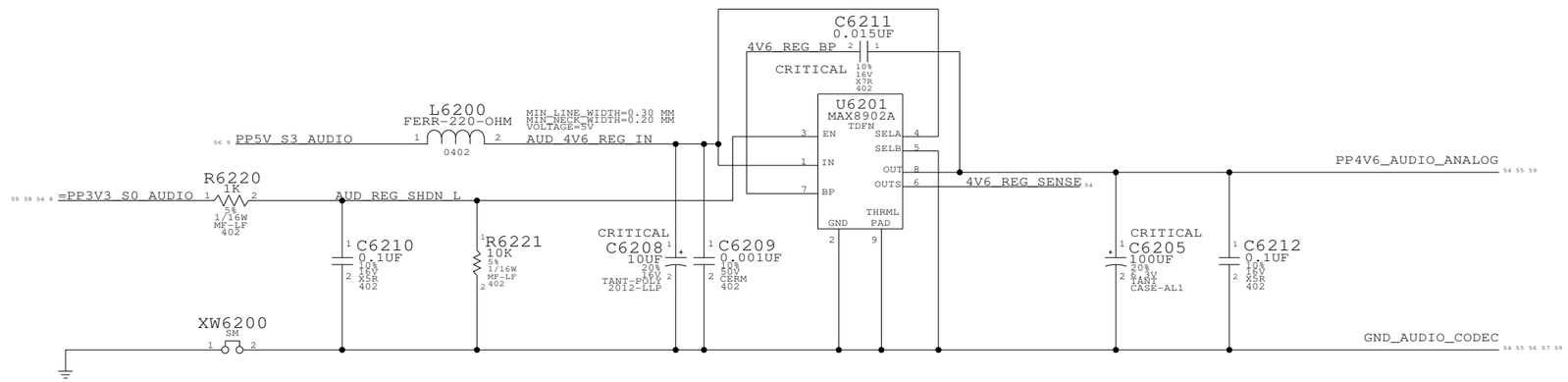
AUDIO CODEC

APPLE P/N 353S1527



AUDIO 4.6V REGULATOR

APPLE P/N 353S1897



AUDIO:CODEC

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

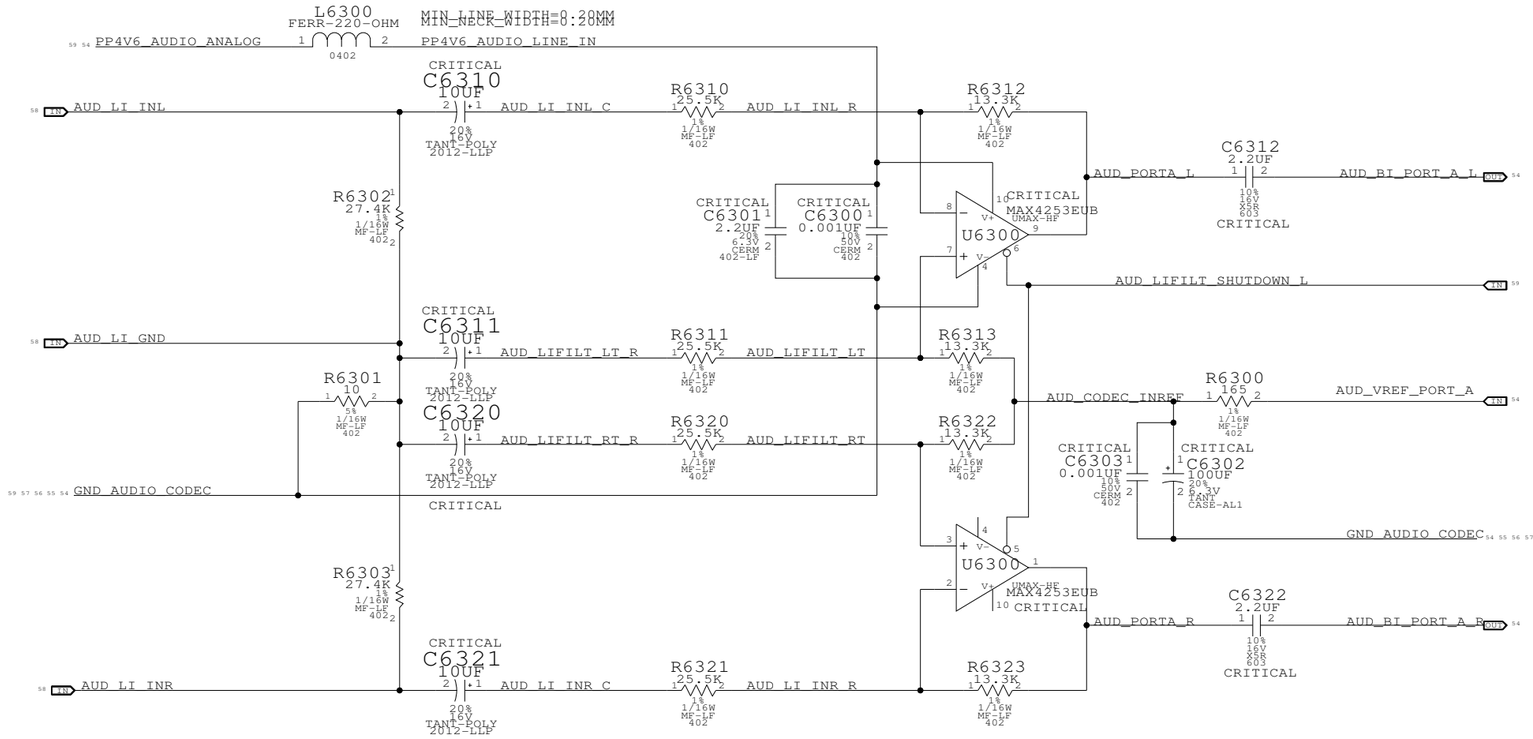
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 54 OF 96	

Pseudo-Diff Line-In Filter
GAIN = -5.4DB AV = 0.52
FC = 1.8 HZ



AUDIO: LINE IN

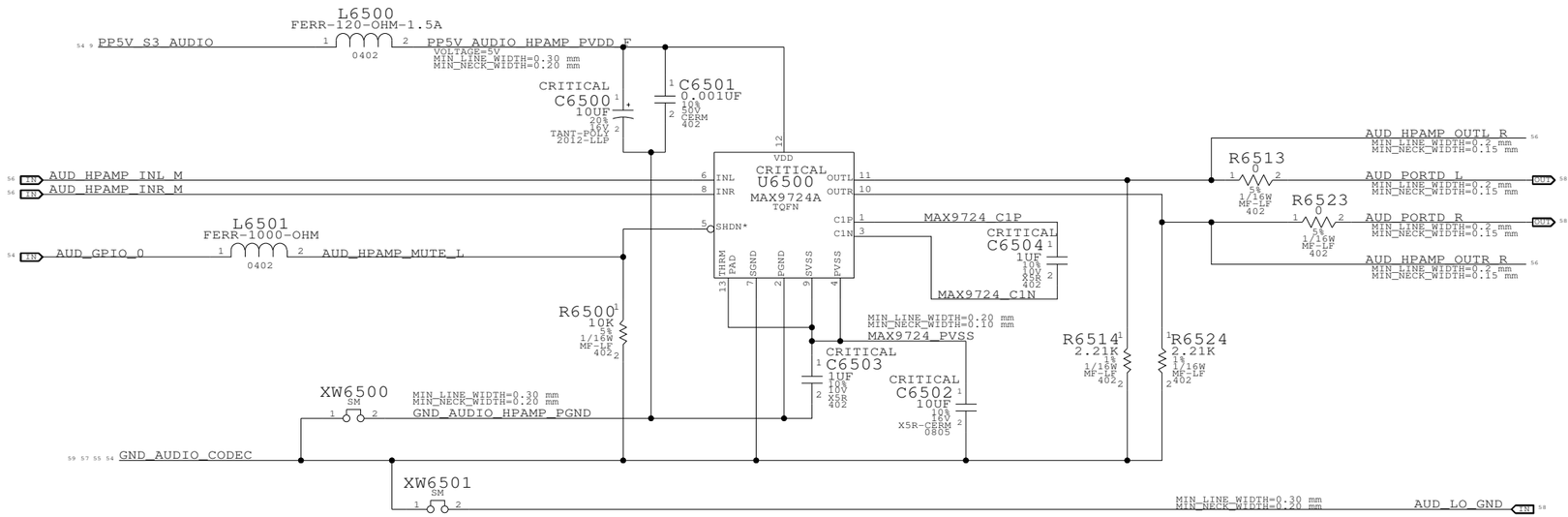
SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 55 OF 96	

Headphone Amplifier (MAX9724A)

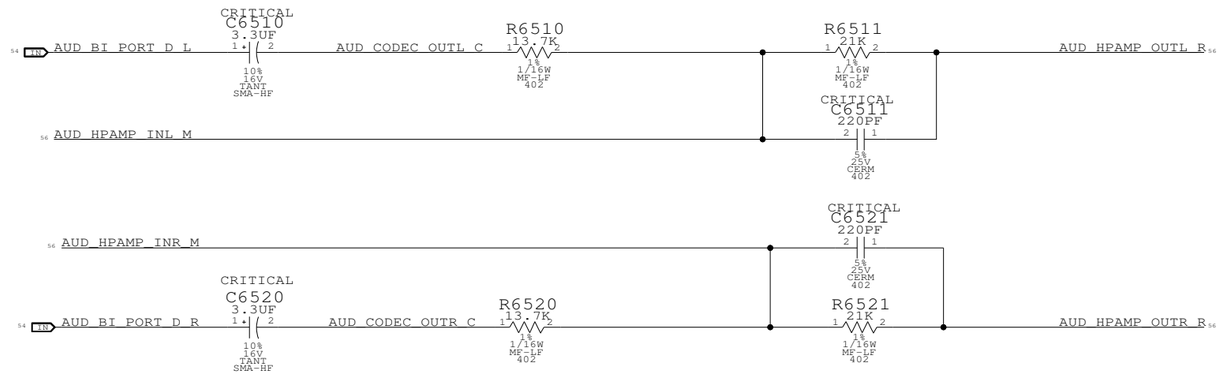
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 56 OF 96	

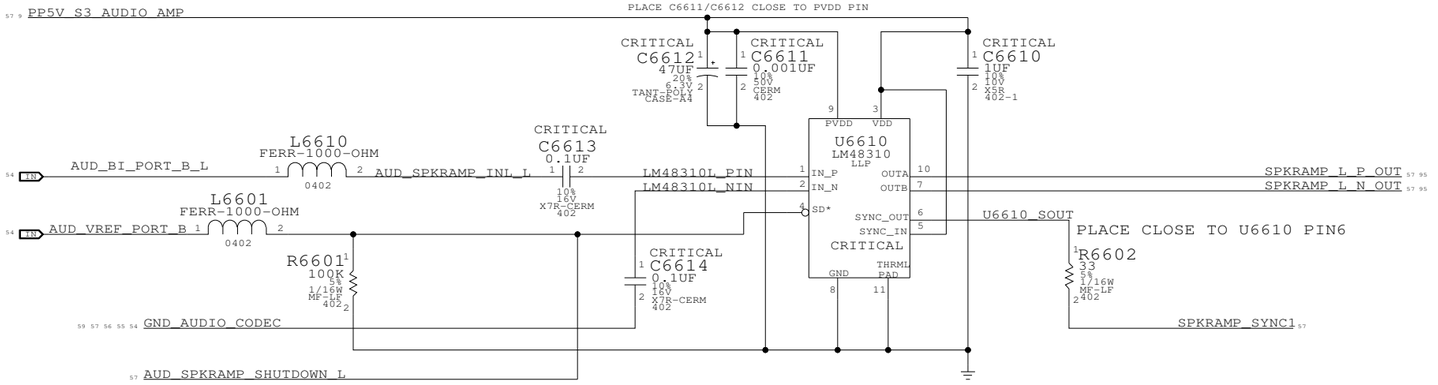
2X MONO SPEAKER AMPLIFIERS (LM48310)

APN: 353S1901

GAIN = 12DB

79Hz < FC (L&R) < 93Hz

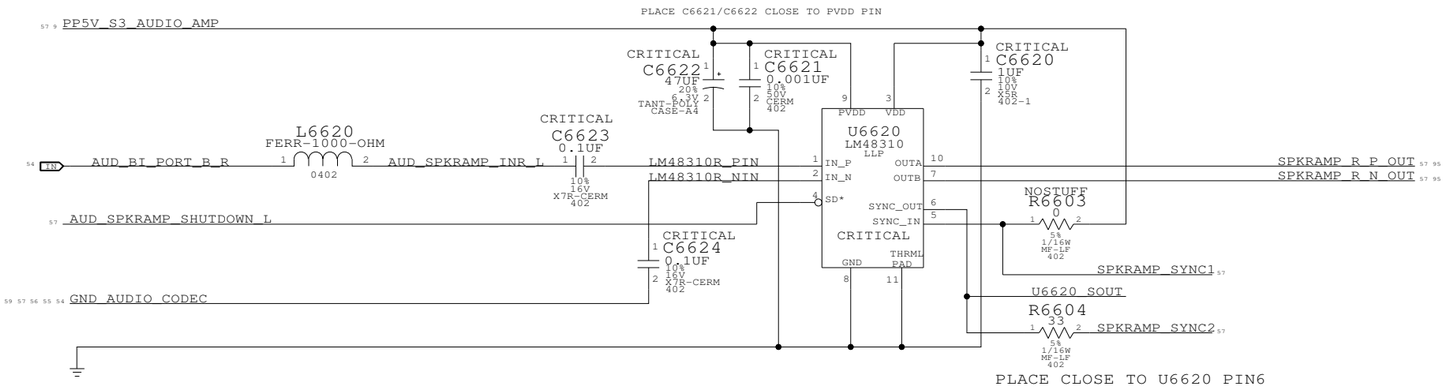
53Hz < FC (SUB) < 62Hz



SPEAKER CHECKPOINTS

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_L_P_OUT — R6610 0 5% 1/16W MF-LF 402 — SPKRCONN_L_P_OUT

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_L_N_OUT — R6611 0 5% 1/16W MF-LF 402 — SPKRCONN_L_N_OUT

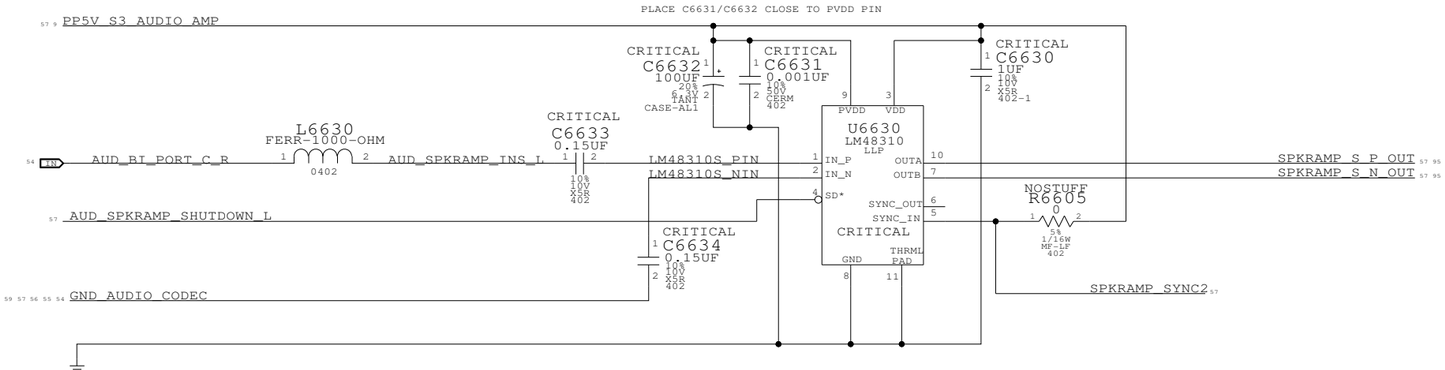


MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_R_P_OUT — R6620 0 5% 1/16W MF-LF 402 — SPKRCONN_R_P_OUT

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_R_N_OUT — R6621 0 5% 1/16W MF-LF 402 — SPKRCONN_R_N_OUT

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_S_P_OUT — R6630 0 5% 1/16W MF-LF 402 — SPKRCONN_S_P_OUT

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_S_N_OUT — R6631 0 5% 1/16W MF-LF 402 — SPKRCONN_S_N_OUT



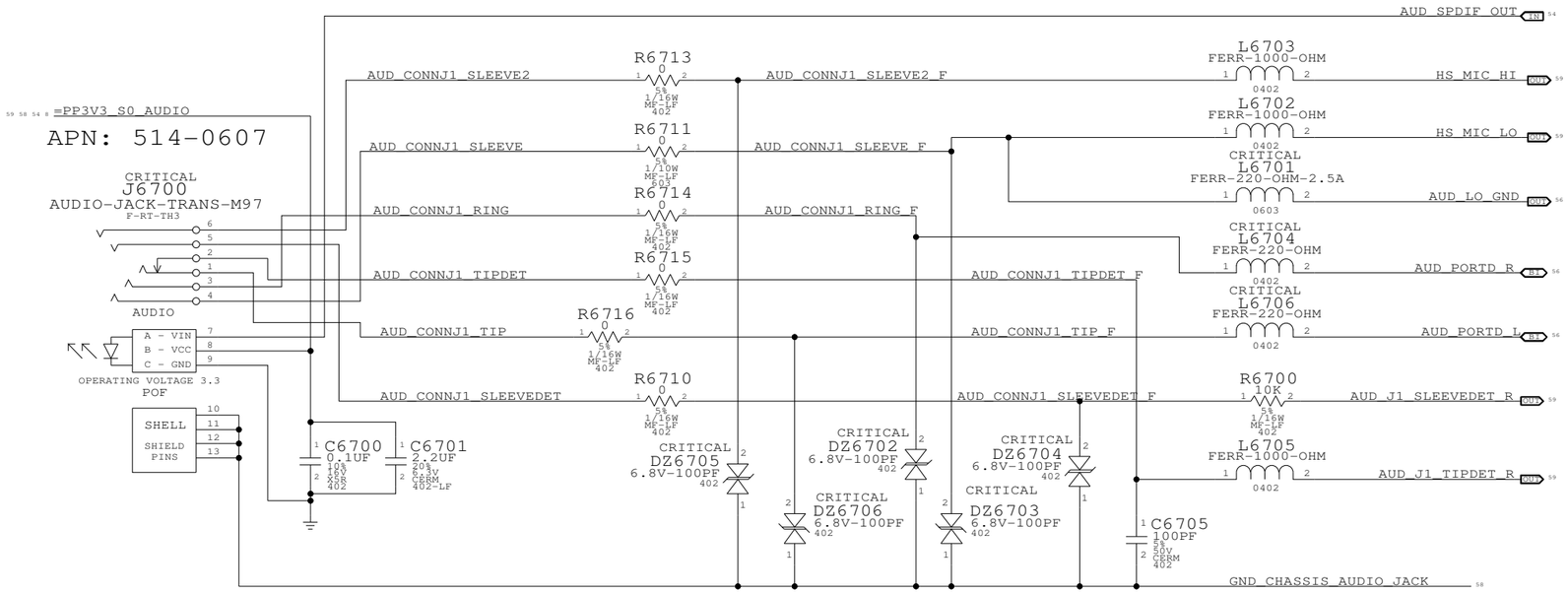
AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 57 OF 96	

AUDIO JACK 1 LO/HP JACK, SPDIF TX

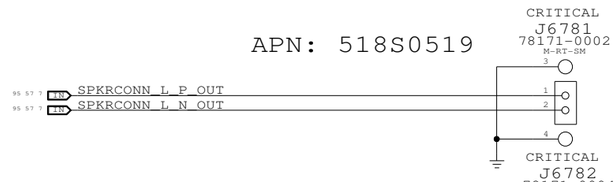


MIC CONNECTOR

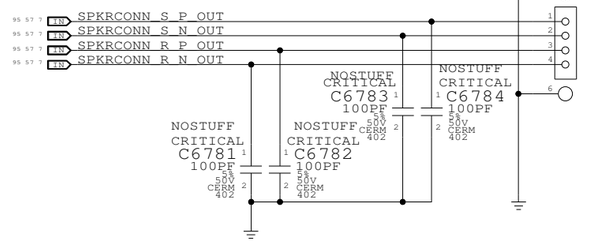
APN: 518S0520

SPEAKER CONNECTOR

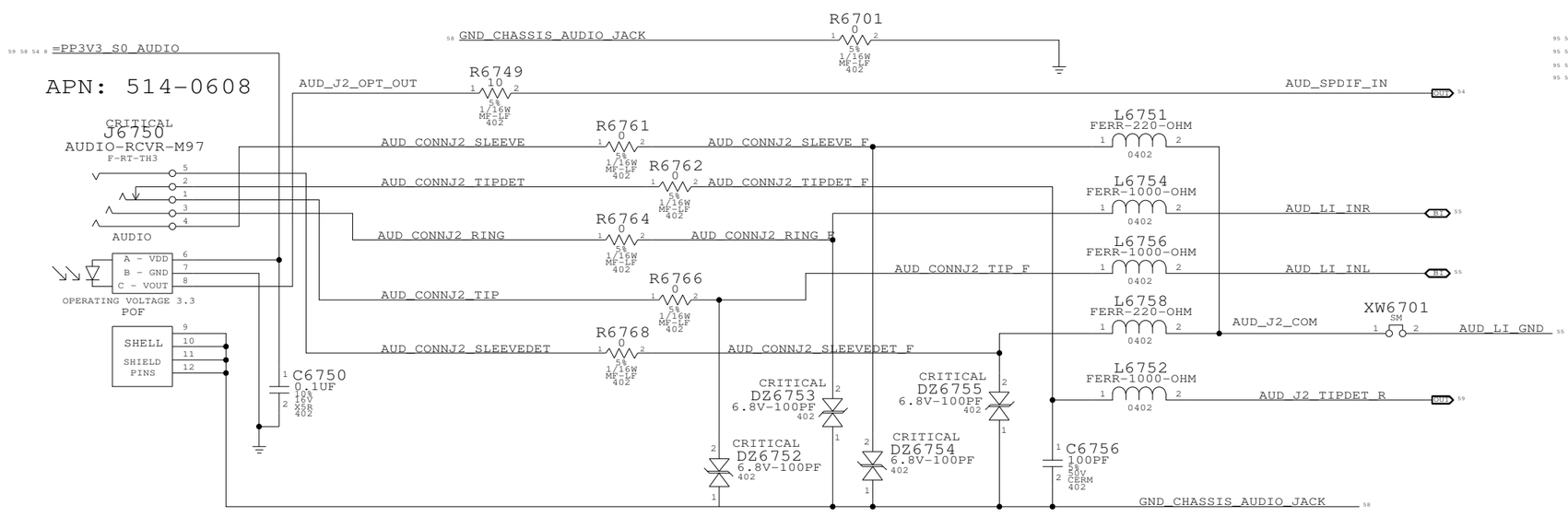
APN: 518S0519



APN: 518S0521



RETURN FOR HF NOISE



AUDIO JACK 2 LINE IN JACK, SPDIF RX

AUDIO: JACKS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 58 OF 96	

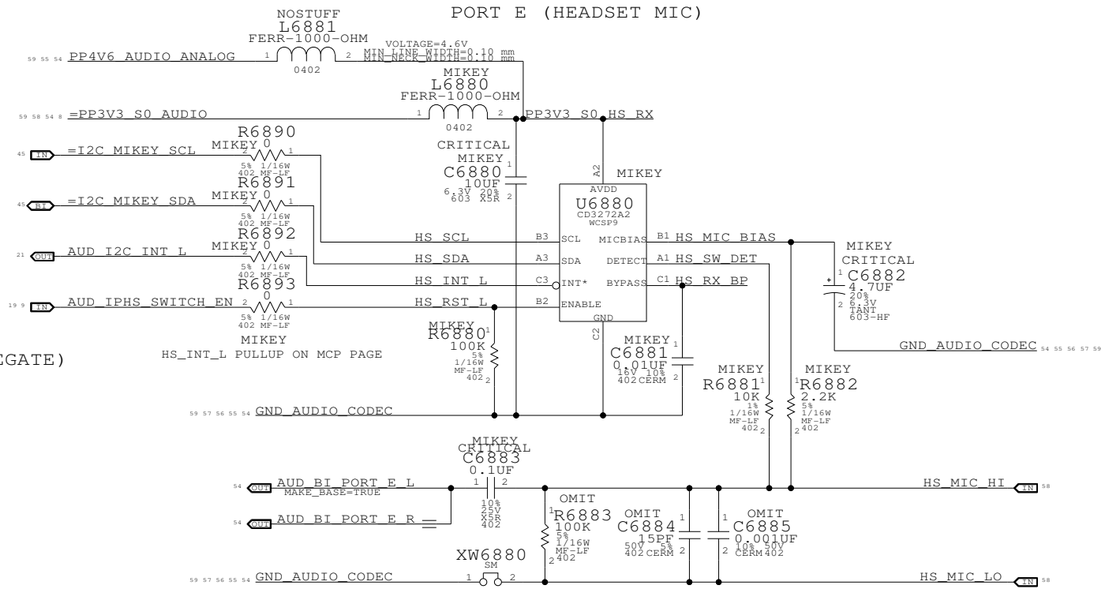
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SATELLITES	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SUB	0X0F (15)	0X05 (05)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)		0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

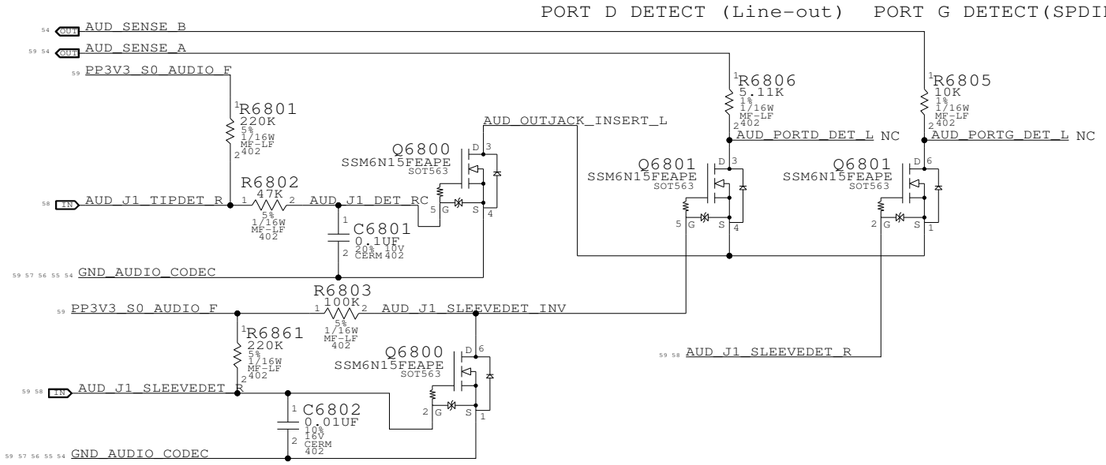
FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
BUILT-IN MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT E (HEADSET MIC)



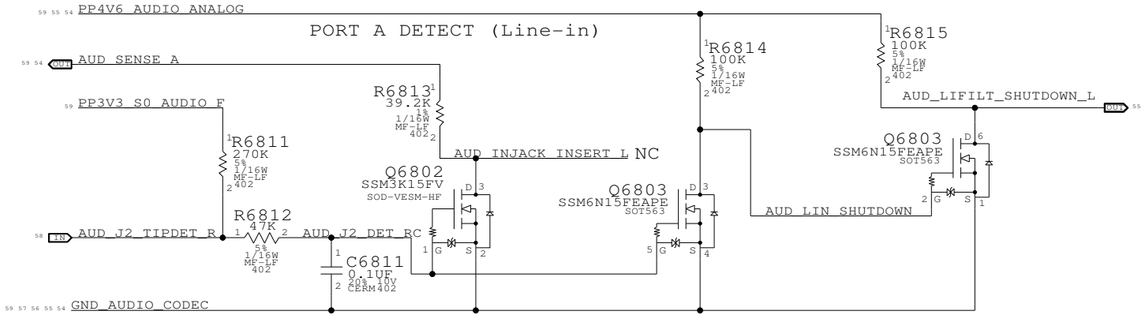
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6883	MIKEY
131S1513	1	15PF 5% 0402 CAPACITOR	C6884	MIKEY
132S0045	1	100PF 10% 0402 CAPACITOR	C6885	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6883	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6884	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6885	NOMIKEY

PORT D DETECT (Line-out) PORT G DETECT(SPDIF DELEGATE)

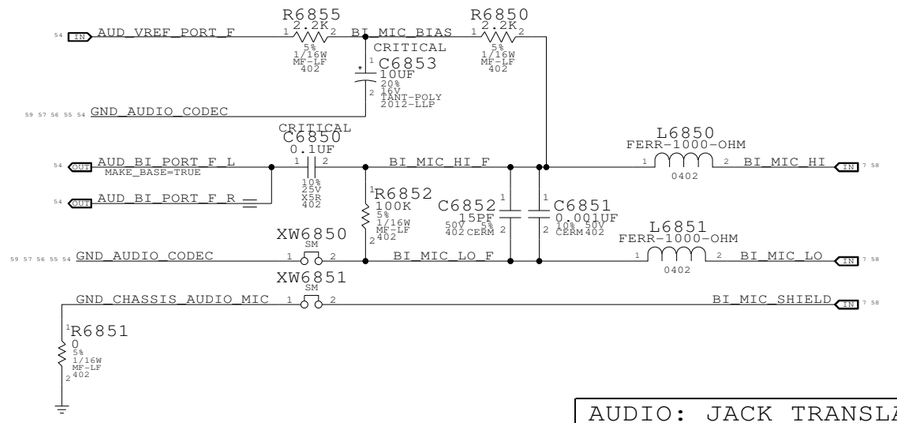


LINE_IN AMP SHUTDOWN CONTROL

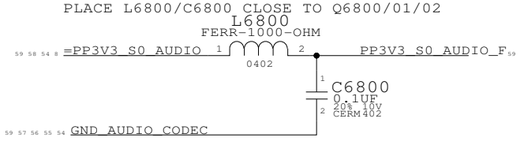
PORT A DETECT (Line-in)



PORT F (BUILT-IN MIC)



PLACE L6800/C6800 CLOSE TO Q6800/01/02



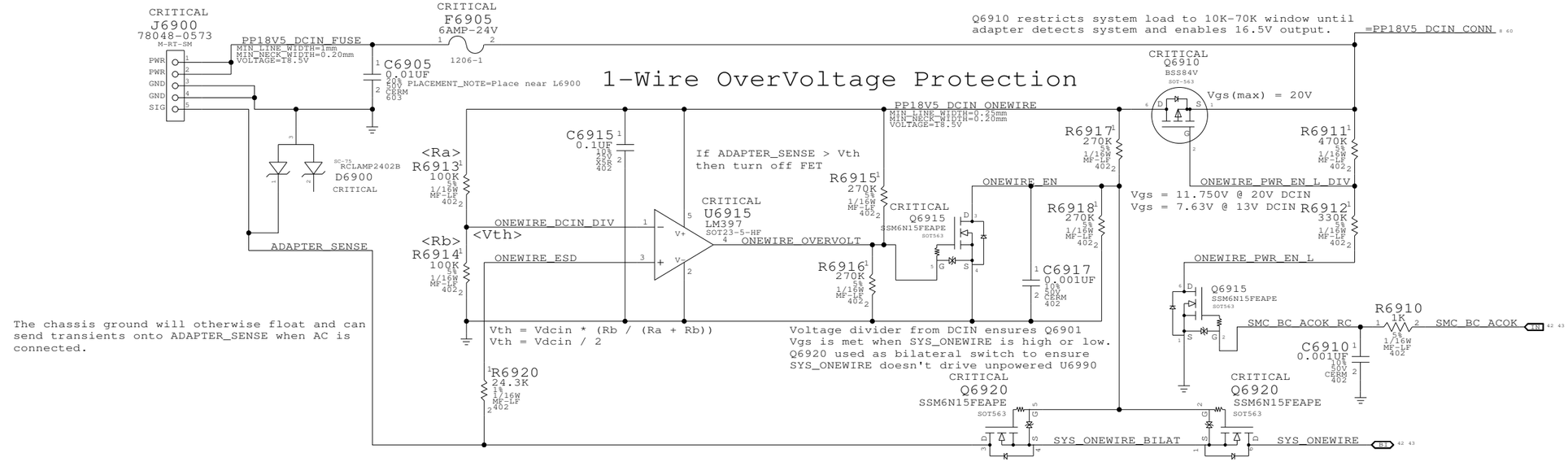
AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

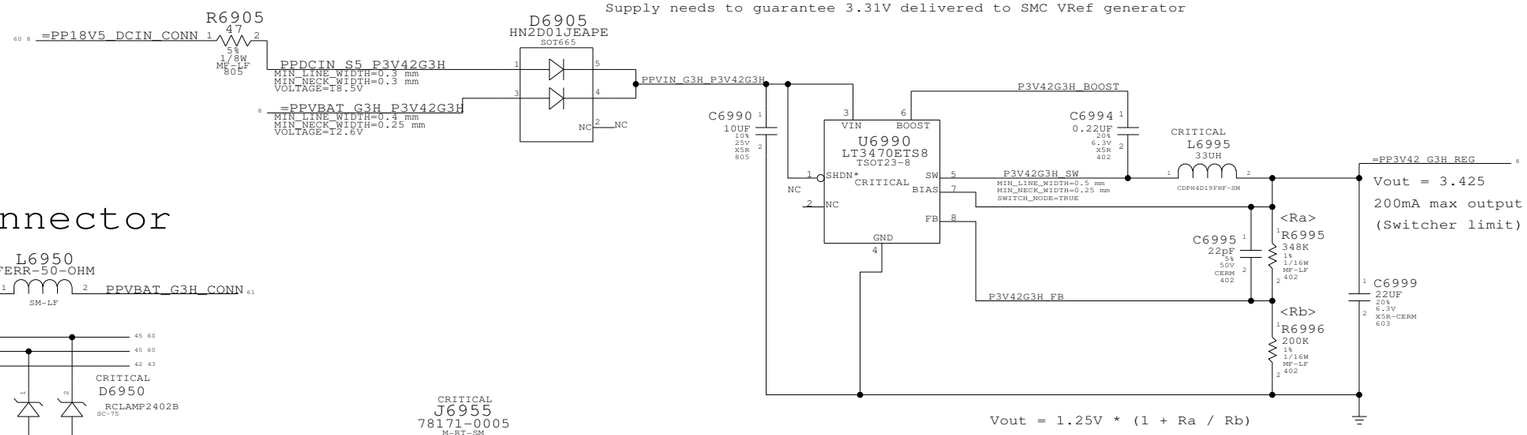
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 59 OF 96	

MagSafe DC Power Jack

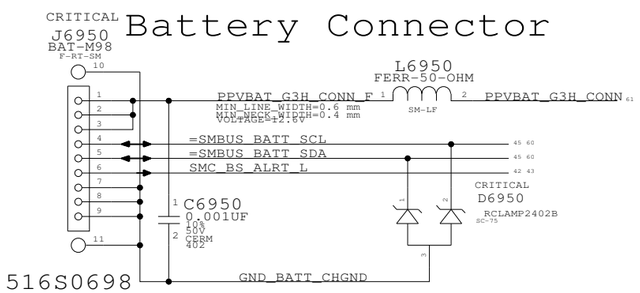


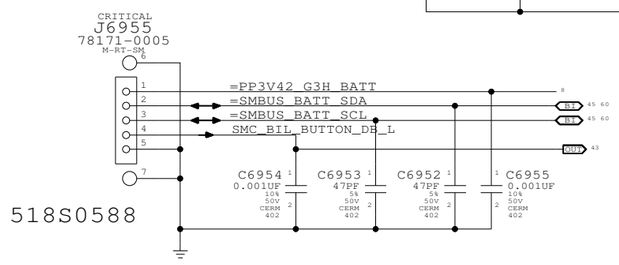
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Battery Connector





DC-In & Battery Connectors

SYNC_MASTER=T18_MLB SYNC_DATE=12/06/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

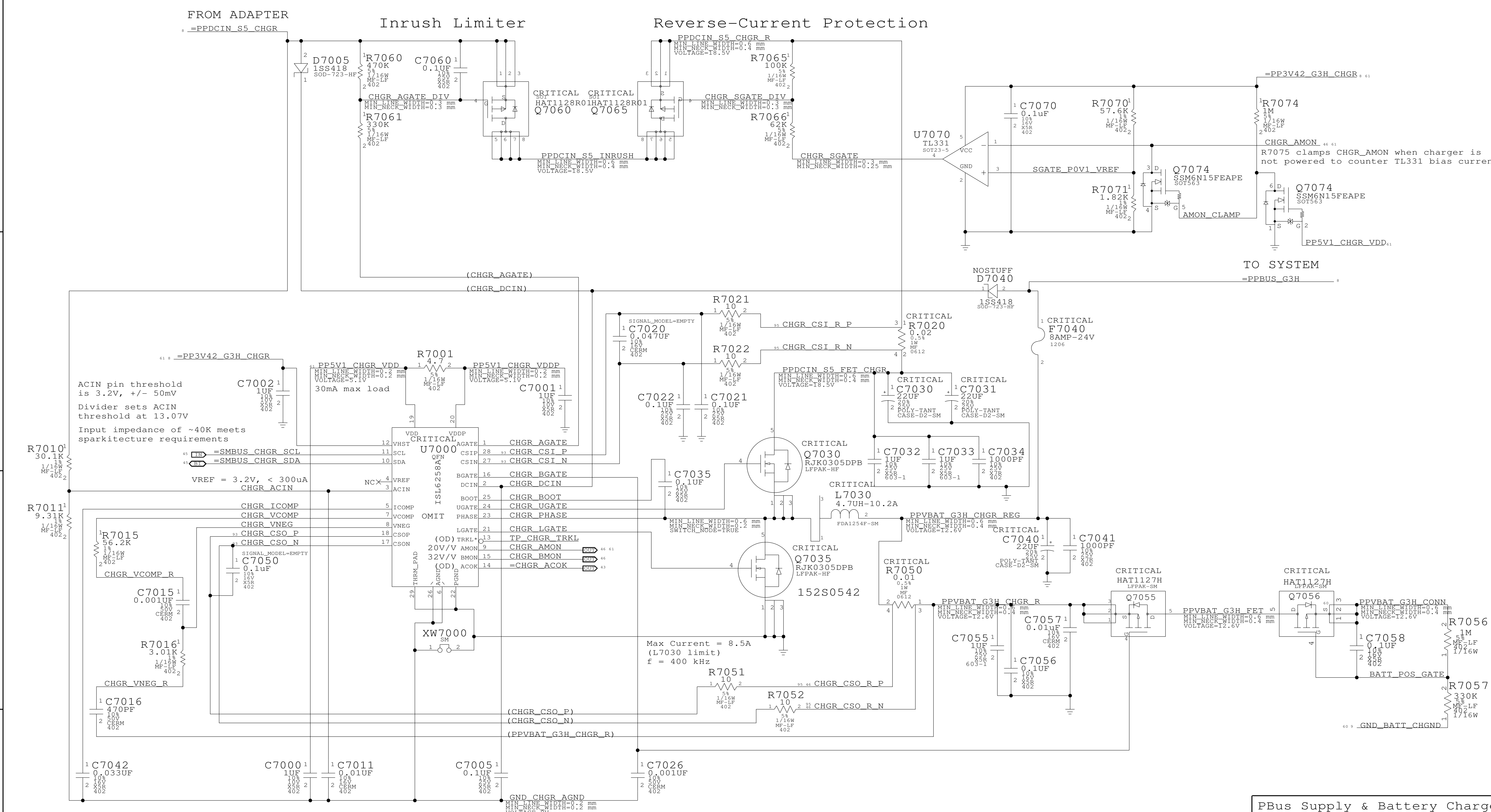
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 60 OF 96	



M99 differences from last sync on 12/02/07 to T18 MLB:

1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1811	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE D | DRAWING NUMBER 051-7546 | REV. A.0.0

SCALE NONE | SHT 61 OF 96

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

Place R7131 Between L7100,L7101 and CPU

NO STUFF

SIGNAL_MODEL=EMPTY

IMVP6_VR_ON	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM

IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

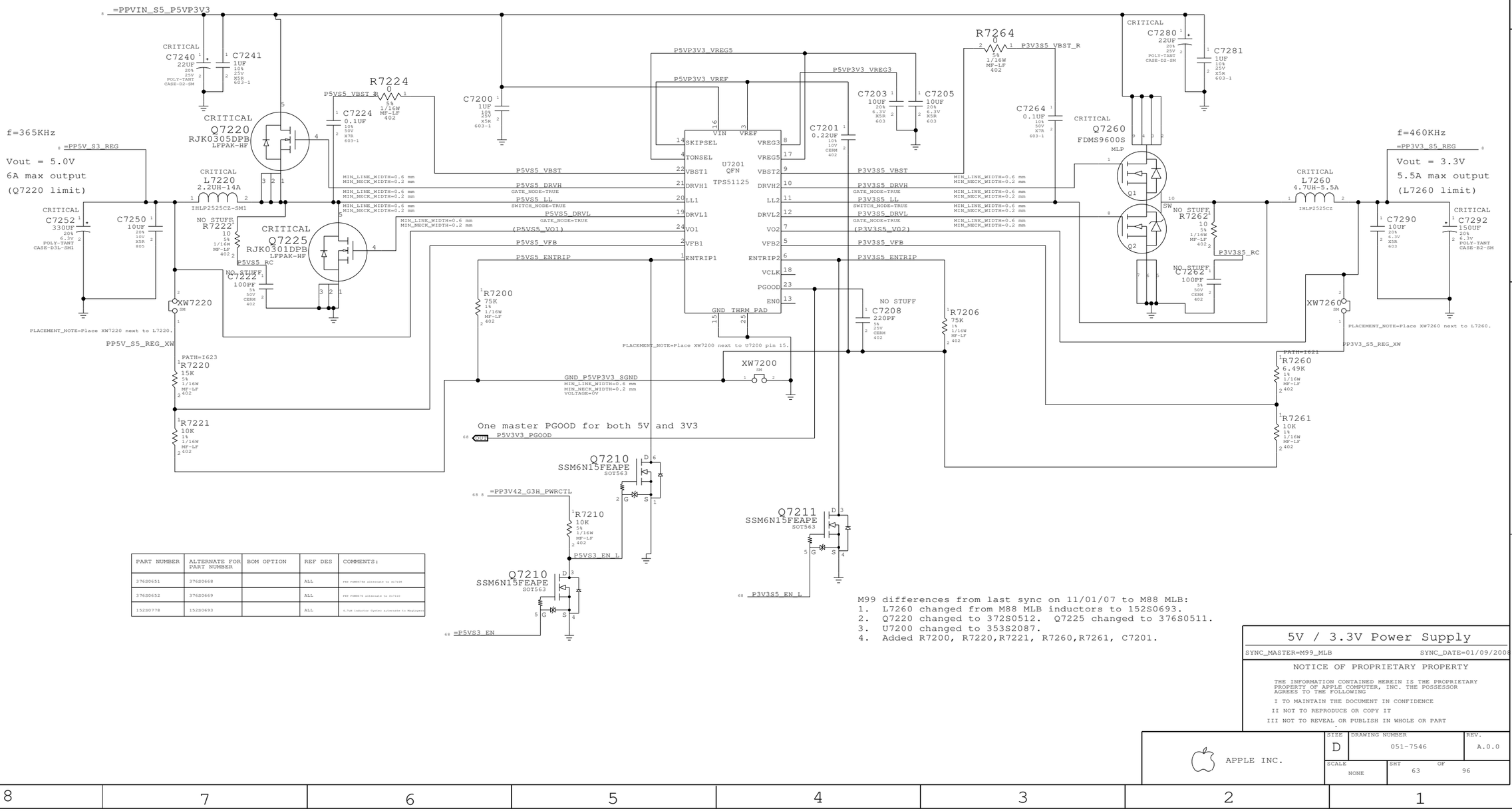
IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 62 OF 96	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0651	376S0668		ALL	FET FDMS7660 alternate to SiC7108
376S0652	376S0669		ALL	FET FDMS9678 alternate to SiC7112
152S0778	152S0693		ALL	4.7uH inductor Cyntec sytovate to Maghapsi

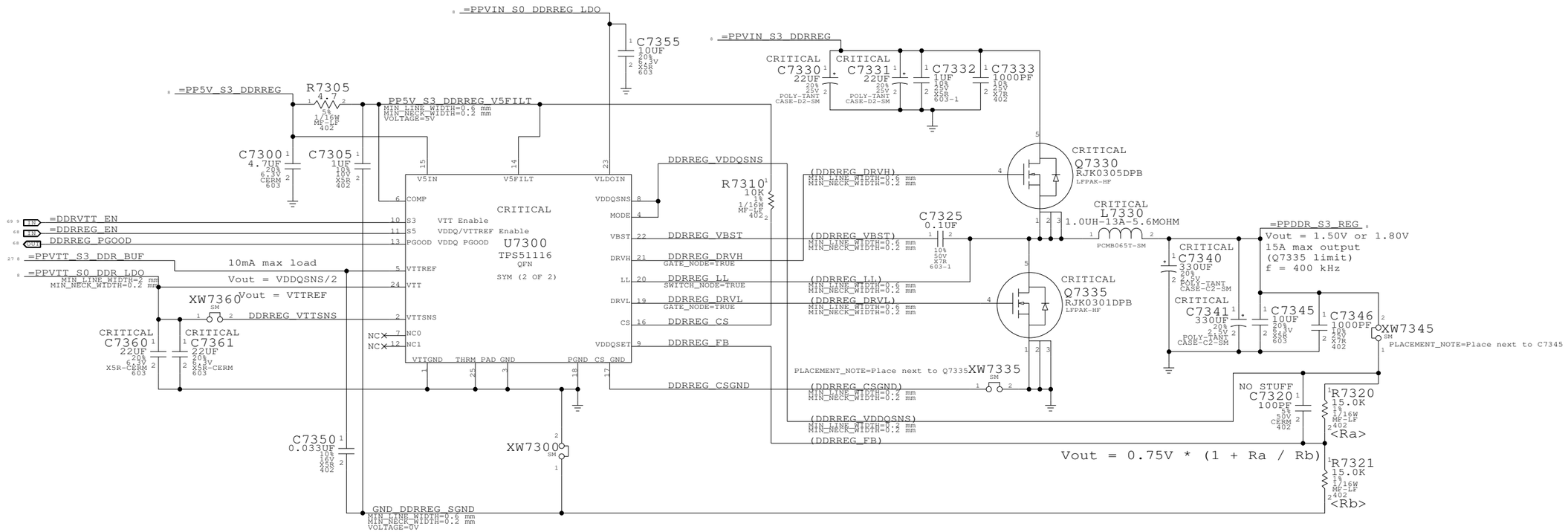
M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220,R7221, R7260,R7261, C7201.

5V / 3.3V Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=01/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 63 OF 96	

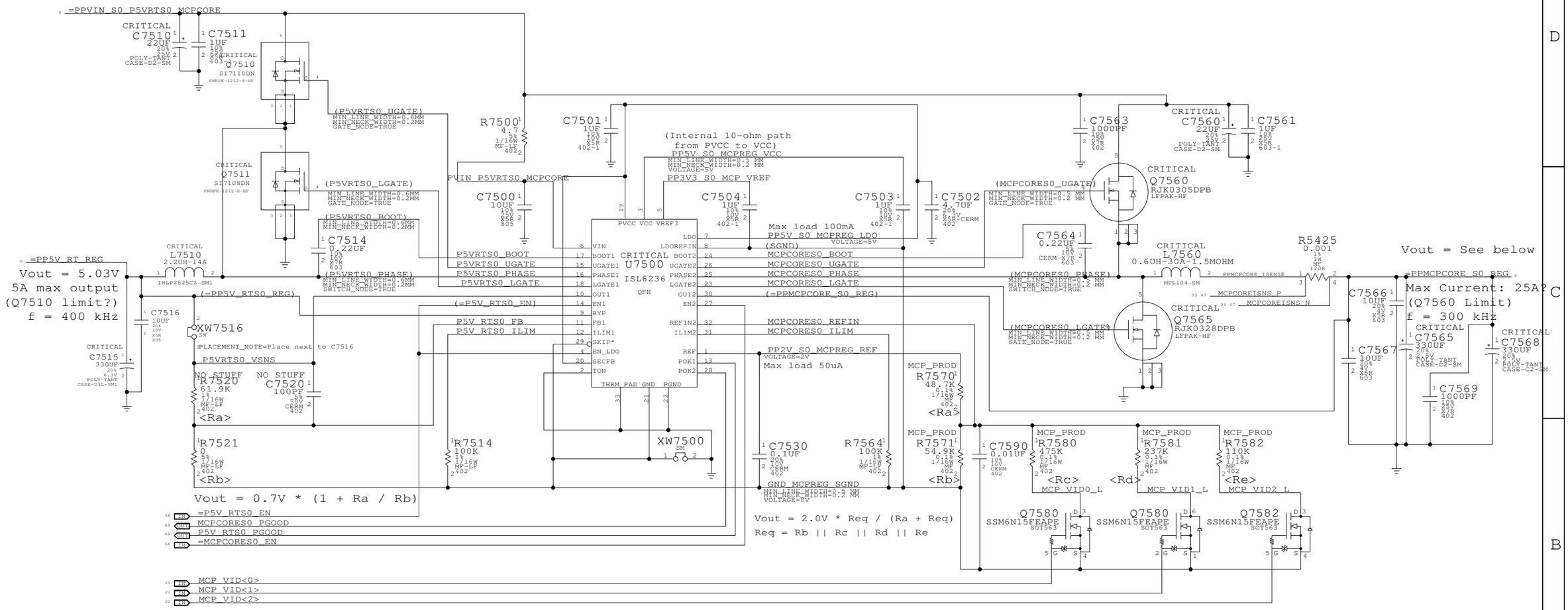


1.5V DDR3 Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/13/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 64 OF 96	



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

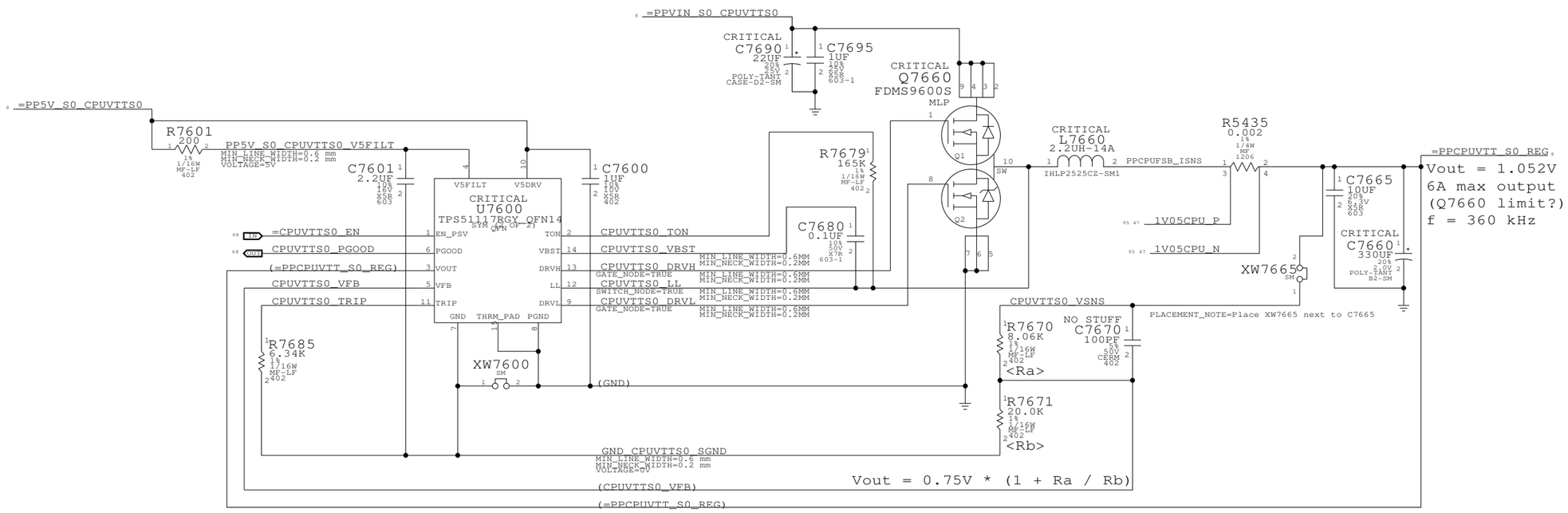
VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

1.05V / MCP Core Regulator

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 65 OF 96	



M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

CPU VTT Power Supply

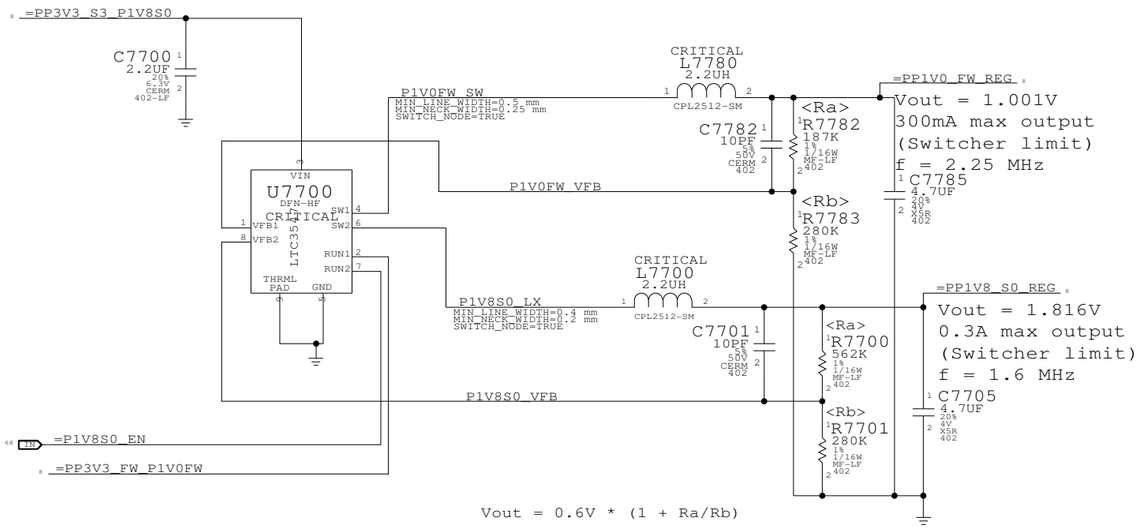
SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 66 OF 96	

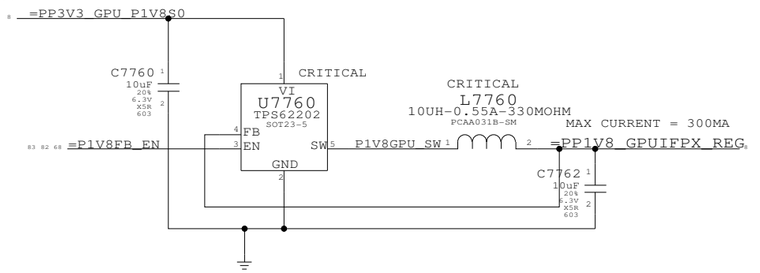
1.8V S0 Switcher / 1.0VFW SWITCHER

S5 power required for output discharge feature

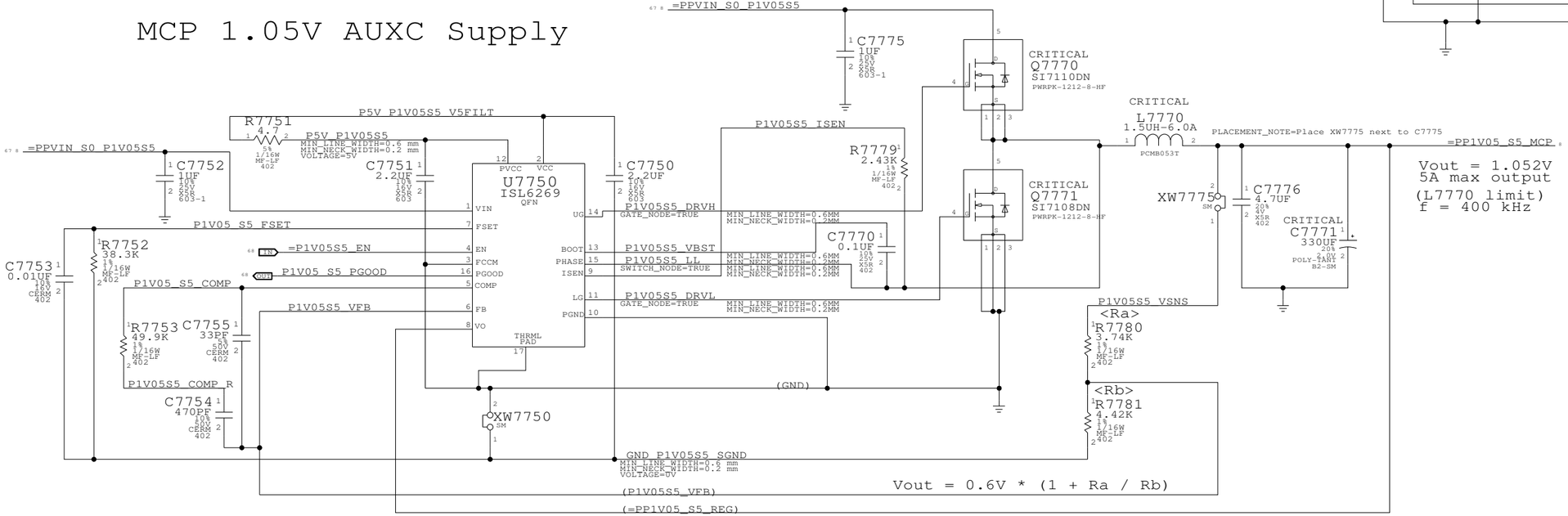


1.8V S0 Switcher

INPUT RAIL IS 3.3V S0



MCP 1.05V AUXC Supply



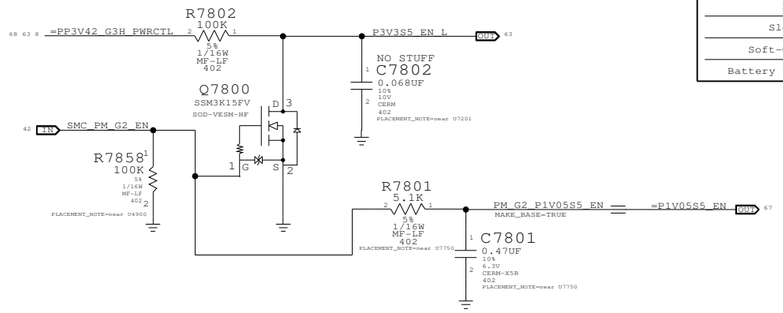
Misc Power Supplies

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

APPLE INC.

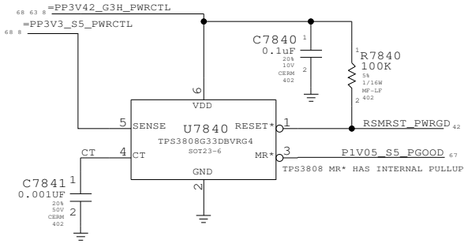
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 67 OF 96	

3.3V 1,05V S5 ENABLE

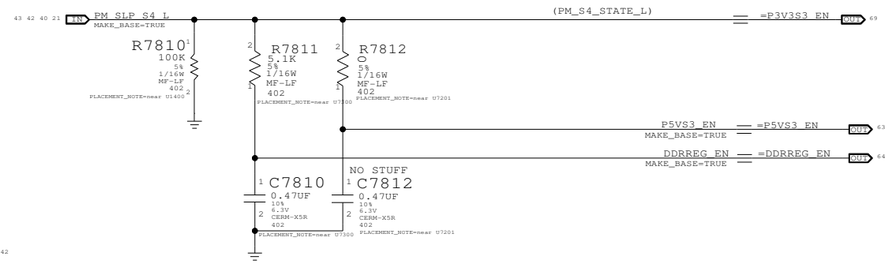


State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

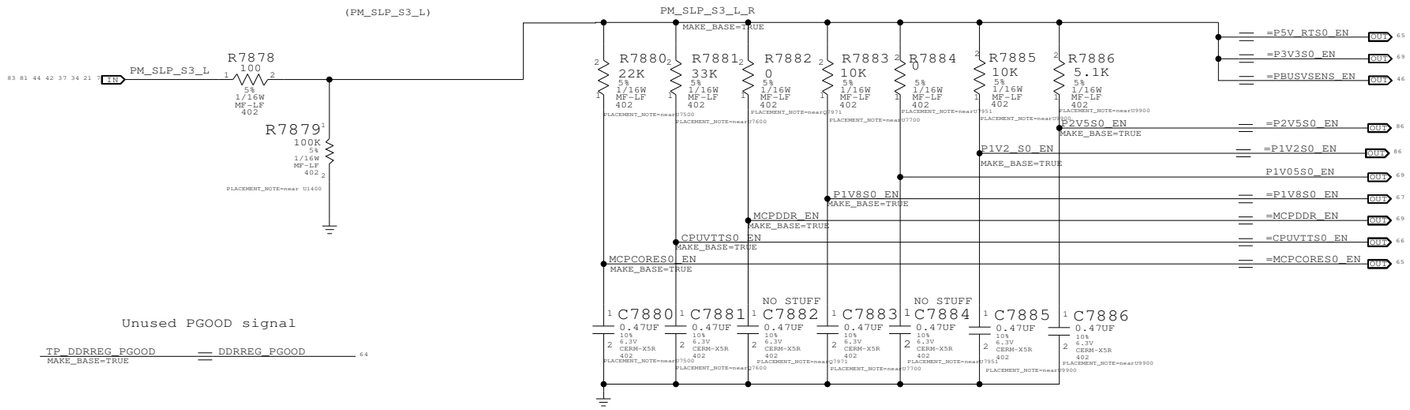
S5 rail PWRGD



3.3V,5V S3 ENABLE

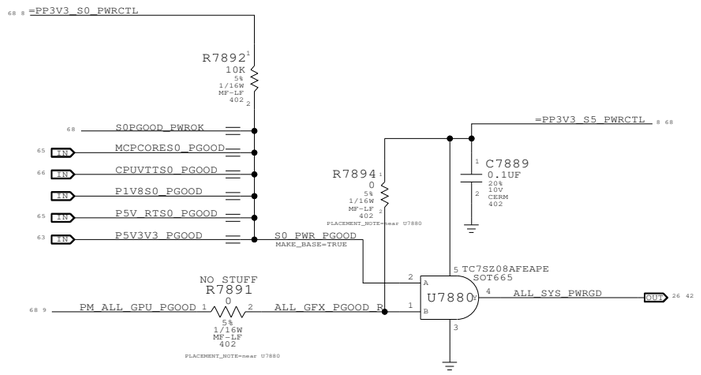


S0 ENABLE



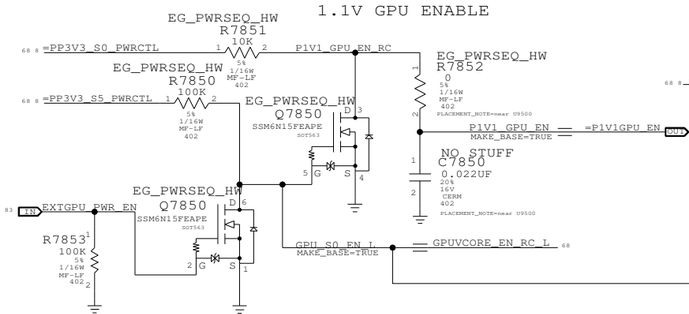
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

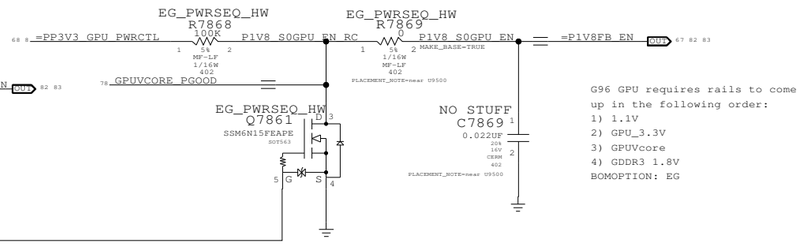


Unused PGOOD signal

1.1V GPU ENABLE



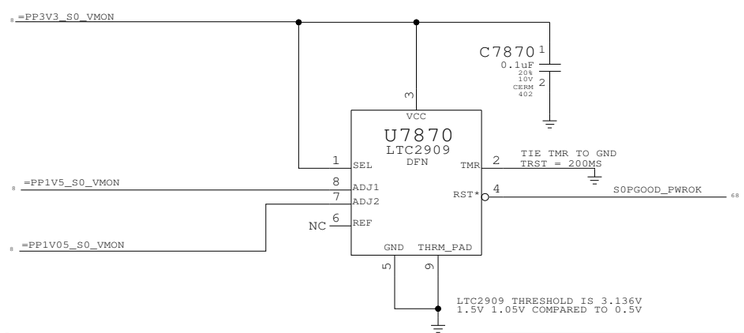
Graphic MEM ENABLE



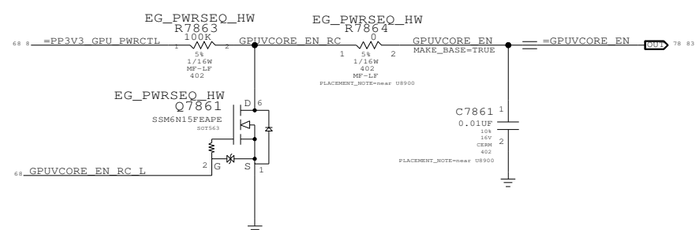
G96 GPU requires rails to come up in the following order:
1) 1.1V
2) GPU_3.3V
3) GPUVcore
4) GDDR3 1.8V
BOMOPTION: EG

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

place XW0402 if needed to save trace space for pin 7,8



GPUVCORE ENABLE



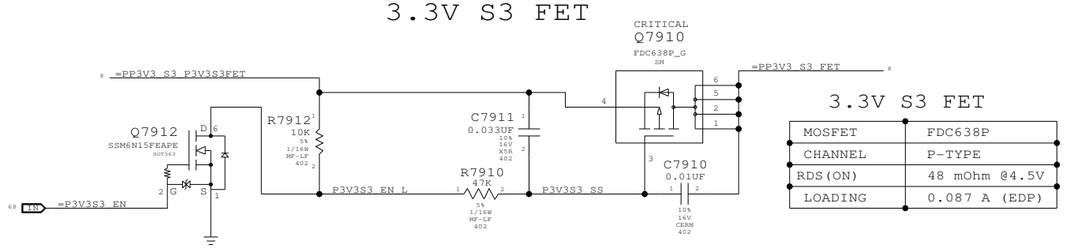
EXT GPU PWRGD Pullup

Power Control
SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT: 68	OF: 96

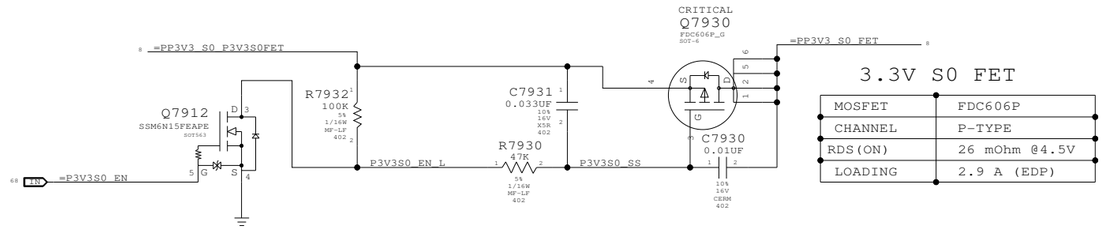
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

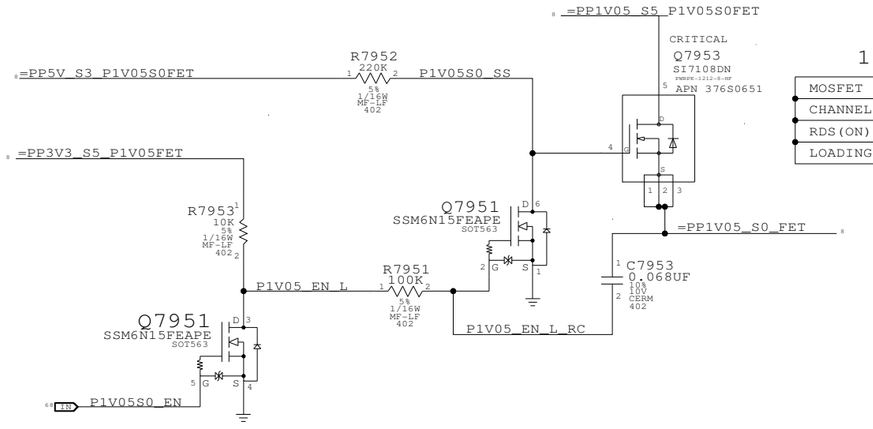
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

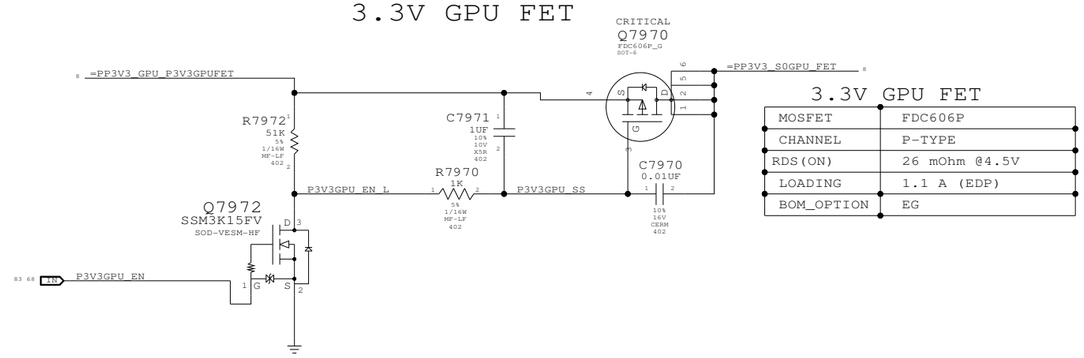
1.05V S0 FET



1.05V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	2.1 A (EDP)

3.3V GPU FET



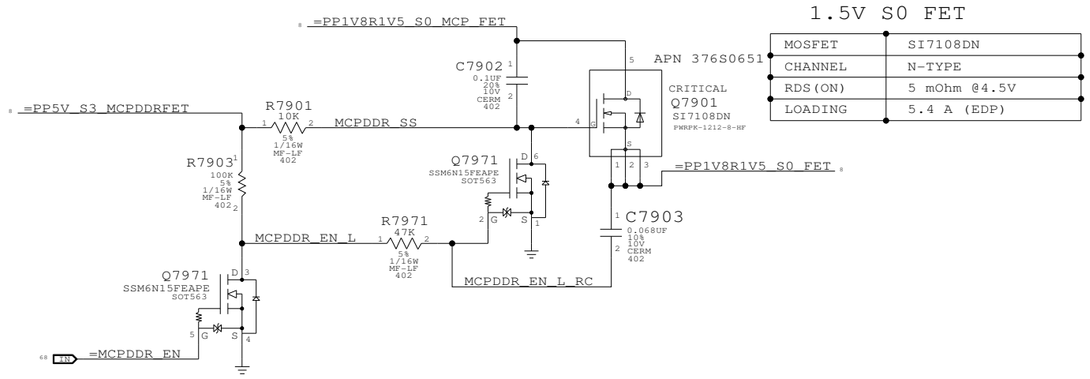
3.3V GPU FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

MCP79 DDR FETs

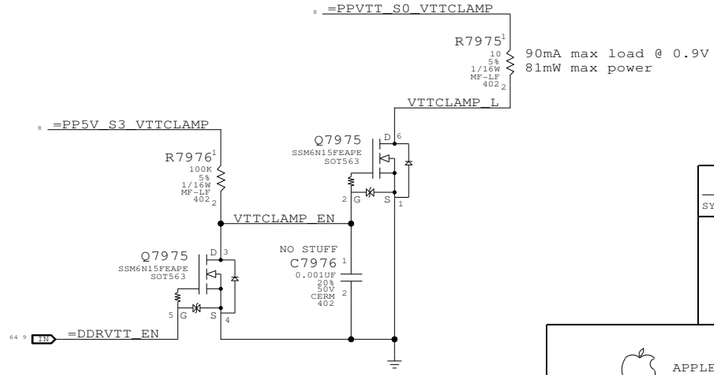
MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

1.5V S0 FET



1.5V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)



Power FETs

SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 69 OF 96	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V1_GPU_PEX_PLLXVDD
=PP1V1_GPU_PEX_IOVDDQ
=PP1V1_GPU_PEX_IOVDD

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 0.1UF 20% 10V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA

L8015 10NH-600MA 0603

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

OMIT

U8000
NB9P-GS
BGA
SYMBOL 2 OF 9

H32	PEX_IOVDD1	AK16
M7	PEX_IOVDD2	AK17
P6	PEX_IOVDD3	AK21
P7	PEX_IOVDD4	AK24
R7	PEX_IOVDD5	AK27
U7		
V6		
AB7		
AD6	PEX_IOVDDQ1	AG11
AF6	PEX_IOVDDQ2	AG12
AG6	PEX_IOVDDQ3	AG13
AJ5	PEX_IOVDDQ4	AG15
D35	PEX_IOVDDQ5	AG16
AK15	PEX_IOVDDQ6	AG17
AL7	PEX_IOVDDQ7	AG18
E7	PEX_IOVDDQ8	AG22
E35	PEX_IOVDDQ9	AG23
F7	PEX_IOVDDQ10	AG24
A2	PEX_IOVDDQ11	AG25
	PEX_IOVDDQ12	AG26
	PEX_IOVDDQ13	AJ14
	PEX_IOVDDQ14	AJ15
	PEX_IOVDDQ15	AJ19
	PEX_IOVDDQ16	AJ21
	PEX_IOVDDQ17	AJ22
	PEX_IOVDDQ18	AJ24
	PEX_IOVDDQ19	AJ25
	PEX_IOVDDQ20	AJ27
	PEX_IOVDDQ21	AK18
	PEX_IOVDDQ22	AK20
	PEX_IOVDDQ23	AK23
	PEX_IOVDDQ24	AK26
	PEX_IOVDDQ25	AL16
	PEX_PLLVDD	AG14
	VDD_SENSE	AD20
	GND_SENSE	AD19

NC

GPU_VDD_SENSE
GPU_GND_SENSE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0	PEX_TX0 AL17
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AN17	PEX_RX0*	PEX_TX0* AM17
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AN19	PEX_RX1	PEX_TX1 AM18
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19	PEX_RX1*	PEX_TX1* AM19
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AR19	PEX_RX2	PEX_TX2 AL19
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AR20	PEX_RX2*	PEX_TX2* AK19
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AP20	PEX_RX3	PEX_TX3 AL20
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AN20	PEX_RX3*	PEX_TX3* AM20
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AN22	PEX_RX4	PEX_TX4 AM21
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AP22	PEX_RX4*	PEX_TX4* AM22
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AR22	PEX_RX5	PEX_TX5 AL22
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AR23	PEX_RX5*	PEX_TX5* AK22
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AP23	PEX_RX6	PEX_TX6 AL23
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AN23	PEX_RX6*	PEX_TX6* AM23
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AN25	PEX_RX7	PEX_TX7 AM24
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AP25	PEX_RX7*	PEX_TX7* AM25
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AR25	PEX_RX8	PEX_TX8 AL25
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AR26	PEX_RX8*	PEX_TX8* AK25
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AP26	PEX_RX9	PEX_TX9 AL26
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AN26	PEX_RX9*	PEX_TX9* AM26
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AN28	PEX_RX10	PEX_TX10 AM27
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AP28	PEX_RX10*	PEX_TX10* AM28
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AR28	PEX_RX11	PEX_TX11 AL28
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29	PEX_RX11*	PEX_TX11* AK28
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AP29	PEX_RX12	PEX_TX12 AK29
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AN29	PEX_RX12*	PEX_TX12* AL29
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AN31	PEX_RX13	PEX_TX13 AM29
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AP31	PEX_RX13*	PEX_TX13* AM30
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AR31	PEX_RX14	PEX_TX14 AM31
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32	PEX_RX14*	PEX_TX14* AM32
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AR34	PEX_RX15	PEX_TX15 AN32
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34	PEX_RX15*	PEX_TX15* AP32

All 0.1uF: 10% 16V X5R 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 1 OF 9

PEG_CLK100M_P		PEX_REFCLK AR16
PEG_CLK100M_N		PEX_REFCLK* AR17
GPU_RESET_L	R8020 0 5% 1/16W MF-LF 402	GPU_RESET_R_L PEX_RST* AM16
	TP_PEX_CLKREQ_L	PEX_CLKREQ* AR13
		PEX_TSTCLK_OUT AJ17 → PEX_TSTCLK_P
		PEX_TSTCLK_OUT* AJ18 → PEX_TSTCLK_N
	R8060 200 1% 1/16W MF-LF 402	
		PEX_TERMP AG21 → PEX_TERMP_PD
	R8050 2.49K 1% 1/16W MF-LF 402	
		PEX_RFU1 AG19 NC
		PEX_RFU2 AG20 NC

PEG_D2R_C_P<0>	C8055 0.1uF	C8056 0.1uF	PEG_D2R_N<0>
PEG_D2R_C_P<1>	C8057 0.1uF	C8058 0.1uF	PEG_D2R_N<1>
PEG_D2R_C_P<2>	C8059 0.1uF	C8060 0.1uF	PEG_D2R_N<2>
PEG_D2R_C_P<3>	C8061 0.1uF	C8062 0.1uF	PEG_D2R_N<3>
PEG_D2R_C_P<4>	C8063 0.1uF	C8064 0.1uF	PEG_D2R_N<4>
PEG_D2R_C_P<5>	C8065 0.1uF	C8066 0.1uF	PEG_D2R_N<5>
PEG_D2R_C_P<6>	C8067 0.1uF	C8068 0.1uF	PEG_D2R_N<6>
PEG_D2R_C_P<7>	C8069 0.1uF	C8070 0.1uF	PEG_D2R_N<7>
PEG_D2R_C_P<8>	C8071 0.1uF	C8072 0.1uF	PEG_D2R_N<8>
PEG_D2R_C_P<9>	C8073 0.1uF	C8074 0.1uF	PEG_D2R_N<9>
PEG_D2R_C_P<10>	C8075 0.1uF	C8076 0.1uF	PEG_D2R_N<10>
PEG_D2R_C_P<11>	C8077 0.1uF	C8078 0.1uF	PEG_D2R_N<11>
PEG_D2R_C_P<12>	C8079 0.1uF	C8080 0.1uF	PEG_D2R_N<12>
PEG_D2R_C_P<13>	C8081 0.1uF	C8082 0.1uF	PEG_D2R_N<13>
PEG_D2R_C_P<14>	C8083 0.1uF	C8084 0.1uF	PEG_D2R_N<14>
PEG_D2R_C_P<15>	C8085 0.1uF	C8086 0.1uF	PEG_D2R_N<15>

All 0.1uF: 10% 16V X5R 402

NV G96 PCI-E

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 70 OF 96	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402

C8103 C8104 C8105 C8106 C8107 0.47UF 10% 6.3V CERM-X5R 402

C8108 C8109 C8110 C8111 C8112 0.47UF 10% 6.3V CERM-X5R 402

C8113 C8114 C8115 C8116 C8117 0.1UF 20% 10V CERM 402

C8118 C8119 C8120 C8121 C8122 0.1UF 20% 10V CERM 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 9 OF 9

VDD

L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17

V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20

U8000
NB9P-GS
BGA
SYMBOL 8 OF 9

GND

B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16

V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30

=PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603

C8156 C8157 C8158 C8159 C8160 C8161 0.1UF 20% 10V CERM 402
C8162 C8163 C8164 C8165 C8166 C8167 0.1UF 20% 10V CERM 402
C8168 C8169 C8170 C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 7 OF 9

FBVDDQ

B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16

J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31

NV G96 Core/FB Power

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 71 OF 96	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U8000
NB9P-GS
BGA
SYMBOL 3 OF 9

OMIT

U8000
NB9P-GS
BGA
SYMBOL 4 OF 9

PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

NO STUFF

GPU_FB_VREF

NV G96 Frame Buffer I/F

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

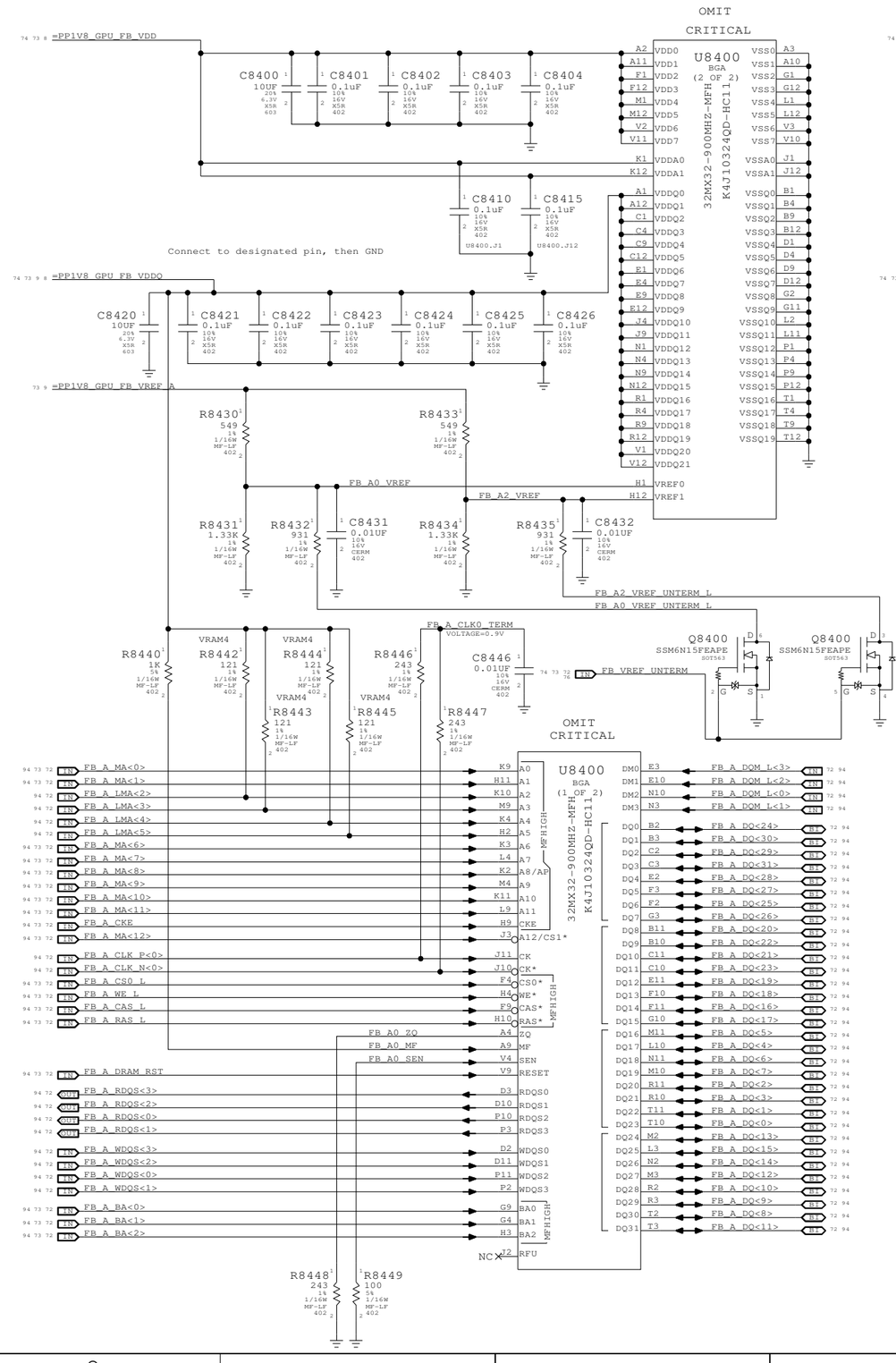
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 72 OF 96	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

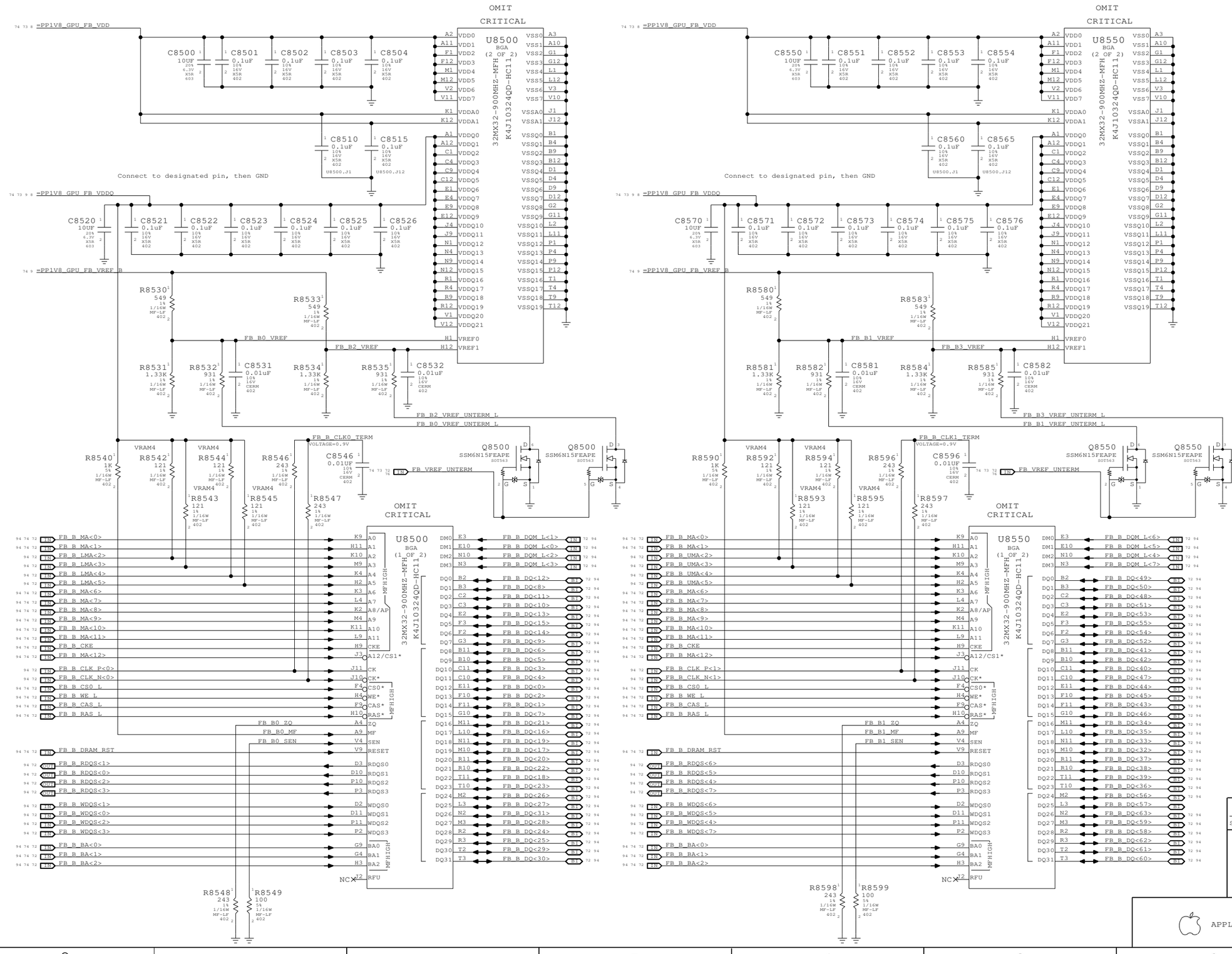
BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 73 OF 96	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 74 OF 96	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
=PP3V3_GPU_VDD33

OMIT
U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

J9 VDD33_1
J10 VDD33_2
J11 VDD33_3
J12 VDD33_4
J13 VDD33_5

=PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

J25 RFU0 NC
J26 RFU1 NC
AK14 RFU0_GND
K9 RFU1_GND

GPU_ROM_CS_L → C3 ROM_CS*
GPU_ROM_SCLK → D4 ROM_SCLK
GPU_ROM_SI → D3 ROM_SI
GPU_ROM_SO → C4 ROM_SO

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

GPU_STRAP_REF_3V3_PD → N9 STRAP_REF_3V3
GPU_STRAP_REF_MIOB_PD → M9 STRAP_REF_MIOB (IPD)

=PP3V3_GPU_MIO

R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1uF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402

GPU_TESTMODE_PD → AP35 TESTMODE
GPU_MIOA_VREF → N5 MIOA_VREF
GPU_MIOB_VREF → AF1 MIOB_VREF
GPU_MIOA_PD_VDDQ → U5 MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND → T5 MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ → AA7 MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND → AA6 MIOB_CAL_PU_GND

L8630 FERR-220-OHM 0402
=PP1V1_GPU_PLLVDD
PP1V1_GPU_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

L8635 FERR-220-OHM 0402
=PP1V1_GPU_H_PLLVDD
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

L8640 FERR-220-OHM 0402
=PP1V1_GPU_VID_PLLVDD
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

AF9 SP_PLLVDD
AE9 PLLVDD
AD9 VID_PLLVDD

GPU_XTALIN (IN) → B1 XTAL_IN
GPU_XTALOUT (OUT) → B2 XTAL_OUT
GPU_XTALOUTBUFF (OUT) → D1 XTAL_OUTBUFF
GPU_XTALSSIN (IN) → D2 XTAL_SSIN

GPIO0	K1	GPU_GPIO_0	B1
GPIO1	K2	GPU_GPIO_1	B1
GPIO2	K3	GPU_GPIO_2	B1
GPIO3	H3	GPU_GPIO_3	B1
GPIO4	H2	GPU_GPIO_4	B1
GPIO5	H1	GPU_GPIO_5	B1
GPIO6	H4	GPU_GPIO_6	B1
GPIO7	H5	GPU_GPIO_7	B1
GPIO8	H6	GPU_GPIO_8	B1
GPIO9	J7	GPU_GPIO_9	B1
GPIO10	K4	GPU_GPIO_10	B1
GPIO11	K5	GPU_GPIO_11	B1
GPIO12	H7	GPU_GPIO_12	B1
GPIO13	J4	GPU_GPIO_13	B1
GPIO14	J6	GPU_GPIO_14	B1
GPIO15	L1	GPU_GPIO_15	B1
GPIO16	L2	GPU_GPIO_16	B1
GPIO17	L4	GPU_GPIO_17	B1
GPIO18	M4	GPU_GPIO_18	B1
GPIO19	L7	GPU_GPIO_19	B1
GPIO20	L5	GPU_GPIO_20	B1
GPIO21	K6	GPU_GPIO_21	B1
GPIO22	L6	GPU_GPIO_22	B1
GPIO23	M6	GPU_GPIO_23	B1
HDA_SDI	C7	GPU_HDA_SDI	MUX
HDA_SDO	B7	GPU_HDA_SDO	MUX
HDA_SYNC	A7	GPU_HDA_SYNC	MUX
HDA_BCLK	D7	GPU_HDA_BCLK	MUX
HDA_RST*	D6	GPU_HDA_RST_L	MUX
SPDIF	A5	GPU_SPDIF	IN
BUFRST*	A4	TP_GPU_BUFRST_L	MUX
JTAG_TCK	AP14	GPU_JTAG_TCK	IN
JTAG_TDI	AN14	GPU_JTAG_TDI	IN
JTAG_TDO	AN16	GPU_JTAG_TDO	MUX
JTAG_TMS	AR14	GPU_JTAG_TMS	IN
JTAG_TRST*	AP16	GPU_JTAG_TRST_L	IN
MIOA_CLKIN	N4	GPU_MIOA_CLKIN	IN
MIOA_CLKOUT	R4	GPU_MIOA_CLKOUT_P	B1
MIOA_CLKOUT*	T4	GPU_MIOA_CLKOUT_N	B1
MIOA_CTL3	P5	GPU_MIOA_CTL3	B1
MIOA_DE	N2	GPU_MIOA_DE	B1
MIOA_D0	N1	GPU_MIOA_D<0>	B1
MIOA_D1	P4	GPU_MIOA_D<1>	B1
MIOA_D2	P1	GPU_MIOA_D<2>	B1
MIOA_D3	P2	GPU_MIOA_D<3>	B1
MIOA_D4	P3	GPU_MIOA_D<4>	B1
MIOA_D5	T3	GPU_MIOA_D<5>	B1
MIOA_D6	T2	GPU_MIOA_D<6>	B1
MIOA_D7	T1	GPU_MIOA_D<7>	B1
MIOA_D8	U4	GPU_MIOA_D<8>	B1
MIOA_D9	U1	GPU_MIOA_D<9>	B1
MIOA_D10	U2	GPU_MIOA_D<10>	B1
MIOA_D11	U3	GPU_MIOA_D<11>	B1
MIOA_D12	R6	GPU_MIOA_D<12>	B1
MIOA_D13	T6	GPU_MIOA_D<13>	B1
MIOA_D14	N6	GPU_MIOA_D<14>	B1
MIOA_HSYNC	N3	GPU_MIOA_HSYNC	B1
MIOA_VSYNC	L3	GPU_MIOA_VSYNC	B1
MIOB_CLKIN	AE1	GPU_MIOB_CLKIN	IN
MIOB_CLKOUT	V4	GPU_MIOB_CLKOUT_P	B1
MIOB_CLKOUT*	W4	GPU_MIOB_CLKOUT_N	B1
MIOB_CTL3	W3	GPU_MIOB_CTL3	B1
MIOB_DE	Y5	GPU_MIOB_DE	B1
MIOB_D0	Y1	GPU_MIOB_D<0>	B1
MIOB_D1	Y2	GPU_MIOB_D<1>	B1
MIOB_D2	Y3	GPU_MIOB_D<2>	B1
MIOB_D3	AB3	GPU_MIOB_D<3>	B1
MIOB_D4	AB2	GPU_MIOB_D<4>	B1
MIOB_D5	AB1	GPU_MIOB_D<5>	B1
MIOB_D6	AC4	GPU_MIOB_D<6>	B1
MIOB_D7	AC1	GPU_MIOB_D<7>	B1
MIOB_D8	AC2	GPU_MIOB_D<8>	B1
MIOB_D9	AC3	GPU_MIOB_D<9>	B1
MIOB_D10	AE3	GPU_MIOB_D<10>	B1
MIOB_D11	AE2	GPU_MIOB_D<11>	B1
MIOB_D12	U6	GPU_MIOB_D<12>	B1
MIOB_D13	W6	GPU_MIOB_D<13>	B1
MIOB_D14	Y6	GPU_MIOB_D<14>	B1
MIOB_D15	W5	GPU_STRAP<0>	B1
MIOB_D16	W7	GPU_STRAP<1>	B1
MIOB_D17	V7	GPU_STRAP<2>	B1
MIOB_HSYNC	W1	GPU_MIOB_HSYNC	B1
MIOB_VSYNC	W2	GPU_MIOB_VSYNC	B1
THERMDP	B5	GPU_THERMD_P	PSI
THERMDN	B4	GPU_THERMD_N	OUT
PGOOD_OUT*	C5	TP_GPU_PGOOD_OUT_L	OUT

NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 75 OF 96	

GPIOs

Native Func

GPU_GPIO_0	GP	NC_GPU_GPIO_0	
GPU_GPIO_1	HPDC	DP_EG_HPD	IN
GPU_GPIO_2	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM	
GPU_GPIO_3	LCD0_VDD	EG_LCD_PWR_EN	76 83
GPU_GPIO_4	LCD0_BL_EN	EG_BKLT_EN	76 83
GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	
GPU_GPIO_7	VID2/MEM_VID	GPIO7_FBVDD_ALTVO	76 82
GPU_GPIO_8	THERM	SMC_GFX_OVERTEMP_R_L	76
GPU_GPIO_9	FAN_PWM	SMC_GFX_THROTTLE_R_L	76
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	72 73 74 76
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	OUT 78
GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	OUT 78
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	OUT 78
GPU_GPIO_14	PWR_CTL1	TP_GPU_VCORE_VID3	

GPIOs

Native Func

GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET	76
GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	
GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	
GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	
GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	
GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	
GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	
GPU_GPIO_23	GP	NC_GPU_GPIO_23	

Renamed signals

GPU_XTALOUT		GPU_XTALOUT
GPU_CLK27M		GPU_XTALIN
GPU_CLK27M_SS		GPU_XTALSSIN
GPU_TDIODE_P		GPU_THERMD_P
GPU_TDIODE_N		GPU_THERMD_N
LVDS_EG_DDC_CLK		GPU_I2CA_SCL
LVDS_EG_DDC_DATA		GPU_I2CA_SDA
DP_EG_DDC_CLK		GPU_I2CB_SCL
DP_EG_DDC_DATA		GPU_I2CB_SDA

Unused I2C Buses

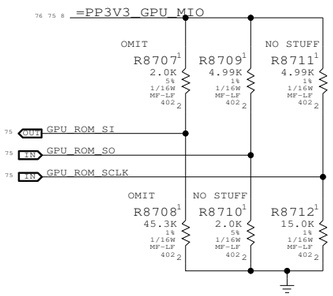
NC_GPU_I2CC_SCL	NO_TEST=TRUE	GPU_I2CC_SCL
NC_GPU_I2CC_SDA	NO_TEST=TRUE	GPU_I2CC_SDA
NC_GPU_I2CD_SCL	NO_TEST=TRUE	GPU_I2CD_SCL
NC_GPU_I2CD_SDA	NO_TEST=TRUE	GPU_I2CD_SDA
NC_GPU_I2CE_SCL	NO_TEST=TRUE	GPU_I2CE_SCL
NC_GPU_I2CE_SDA	NO_TEST=TRUE	GPU_I2CE_SDA
NC_GPU_I2CH_SCL	NO_TEST=TRUE	GPU_I2CH_SDA
NC_GPU_I2CH_SDA	NO_TEST=TRUE	GPU_I2CH_SCL

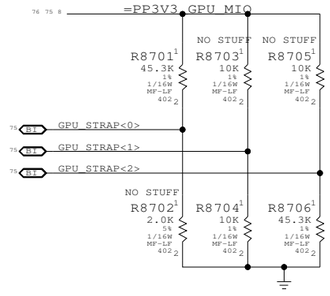
I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Unused signals

NC_GPU_SPDIF	NO_TEST=TRUE	GPU_SPDIF
NC_CPU_HDA_SDI	NO_TEST=TRUE	GPU_HDA_SDI
NC_CPU_HDA_SDO	NO_TEST=TRUE	GPU_HDA_SDO
NC_CPU_HDA_SYNC	NO_TEST=TRUE	GPU_HDA_SYNC
NC_CPU_HDA_BCLK	NO_TEST=TRUE	GPU_HDA_BCLK
NC_CPU_HDA_RST_L	NO_TEST=TRUE	GPU_HDA_RST_L
NC_FBA_MA<13>	NO_TEST=TRUE	FB_A_MA<13>
NC_FBB_MA<13>	NO_TEST=TRUE	FB_B_MA<13>
NC_FBA_CMD28	NO_TEST=TRUE	TP_FBA_CMD28
NC_FBC_CMD28	NO_TEST=TRUE	TP_FBC_CMD28
NC_FBA_CMD29	NO_TEST=TRUE	TP_FBA_CMD29
NC_FBC_CMD29	NO_TEST=TRUE	TP_FBC_CMD29
NC_FBA_CMD30	NO_TEST=TRUE	TP_FBA_CMD30
NC_FBC_CMD30	NO_TEST=TRUE	TP_FBC_CMD30
NC_GPU_ROM_CS_L	NO_TEST=TRUE	GPU_ROM_CS_L
NC_FB_A_CS1_L	NO_TEST=TRUE	FB_A_CS1_L
NC_FB_B_CS1_L	NO_TEST=TRUE	FB_B_CS1_L
TP_LVDS_EG_B_CLK_P		LVDS_EG_B_CLK_P
TP_LVDS_EG_B_CLK_N		LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3>	NO_TEST=TRUE	LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>	NO_TEST=TRUE	LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3>	NO_TEST=TRUE	LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>	NO_TEST=TRUE	LVDS_EG_B_DATA_N<3>

Config Straps





Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

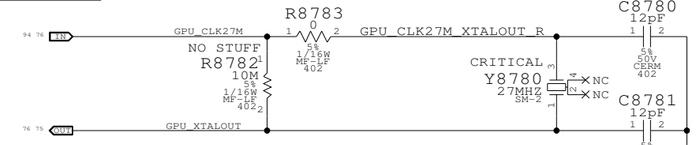
Strap S1/S2 Bit[3:0]	PU/PD	Rval
0 0000	PD	5k
1 0001	PD	10k
2 0010	PD	15k
3 0011	PD	20k
4 0100	PD	25k
5 0101	PD	30k
6 0110	PD	35k
7 0111	PD	45k

Strap S1/S2 Bit[3:0]	PU/PD	Rval
8 1000	PU	5k
9 1001	PU	10k
A 1010	PU	15k
B 1011	PU	20k
C 1100	PU	25k
D 1101	PU	30k
E 1110	PU	35k
F 1111	PU	45k

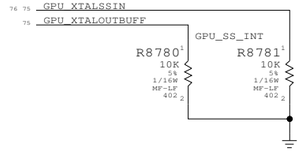
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA

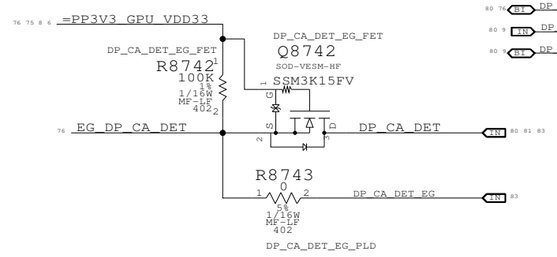
G96 HDCP ROM APN is 341S2272, blank device is 335S0574.

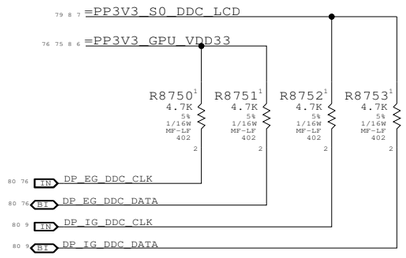
GPU 27MHz Crystal

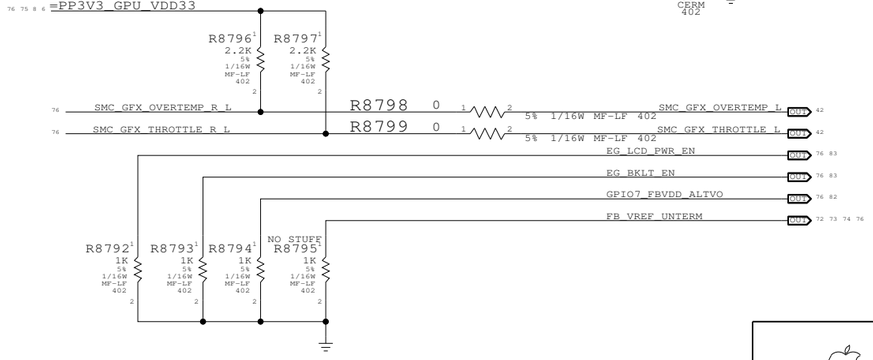


Unused Clocks









G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P		GPU_MIOA_CLKOUT_P
NC_GPU_MIOA_CLKOUT_N		GPU_MIOA_CLKOUT_N
NC_GPU_MIOA_CTL3	NO_TEST=TRUE	GPU_MIOA_CTL3
TP_GPU_MIOA_DE		GPU_MIOA_DE
TP_GPU_MIOA_D<9..0>		GPU_MIOA_D<9..0>
NC_GPU_MIOA_CLKIN	NO_TEST=TRUE	GPU_MIOA_CLKIN
NC_GPU_MIOA_D<14..10>	NO_TEST=TRUE	GPU_MIOA_D<14..10>
NC_GPU_MIOA_HSYNC	NO_TEST=TRUE	GPU_MIOA_HSYNC
NC_GPU_MIOA_VSYNC	NO_TEST=TRUE	GPU_MIOA_VSYNC
NC_GPU_MIOB_CLKIN	NO_TEST=TRUE	GPU_MIOB_CLKIN
NC_GPU_MIOB_CLKOUT_P	NO_TEST=TRUE	GPU_MIOB_CLKOUT_P
NC_GPU_MIOB_CLKOUT_N	NO_TEST=TRUE	GPU_MIOB_CLKOUT_N
NC_GPU_MIOB_CTL3	NO_TEST=TRUE	GPU_MIOB_CTL3
NC_GPU_MIOB_DE	NO_TEST=TRUE	GPU_MIOB_DE
NC_GPU_MIOB_D<14..0>	NO_TEST=TRUE	GPU_MIOB_D<14..0>
NC_GPU_MIOB_VSYNC	NO_TEST=TRUE	GPU_MIOB_VSYNC
NC_GPU_MIOB_HSYNC	NO_TEST=TRUE	GPU_MIOB_HSYNC

Isolation FETs for DP MUX inputs

G96 GPIOs & Straps

SYNC_MASTER=MUXGFX SYNC_DATE=07/09/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 76 OF 96	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET ??
GPU_IFPCD_RSET ??
GPU_IFPAB_RSET ??

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

=PP1V1_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AJ8
Place at AK8

PP1V1_GPU_IFPCD_IOVDD_F ??
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM 0402
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F ??
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F ??
PP1V8_GPU_IFPEF_PLLVDD_F ??

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

OMIT

U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPCD_PLLVDD	IFPA_TXD3	AK11
AK7	IFPCD_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
		IFPC_AUX	AP2
		IFPC_AUX*	AN3
		IFPC_L0	AM7
		IFPC_L0*	AM6
		IFPC_L1	AL5
		IFPC_L1*	AM5
		IFPC_L2	AM3
		IFPC_L2*	AM4
		IFPC_L3	AP1
		IFPC_L3*	AR2
		IFPD_AUX	AP4 NC
		IFPD_AUX*	AN4 NC
		IFPD_L0	AR8 NC
		IFPD_L0*	AP7 NC
		IFPD_L1	AP6 NC
		IFPD_L1*	AN6 NC
		IFPD_L2	AR5 NC
		IFPD_L2*	AR4 NC
		IFPD_L3	AR3 NC
		IFPD_L3*	AP3 NC
		IFPE_AUX	AE4 NC
		IFPE_AUX*	AD4 NC
		IFPE_L0	AE8 NC
		IFPE_L0*	AD8 NC
		IFPE_L1	AE6 NC
		IFPE_L1*	AD6 NC
		IFPE_L2	AE5 NC
		IFPE_L2*	AD5 NC
		IFPE_L3	AE3 NC
		IFPE_L3*	AD3 NC
		IFPF_AUX	AF3 NC
		IFPF_AUX*	AG3 NC
		IFPF_L0	AL2 NC
		IFPF_L0*	AK2 NC
		IFPF_L1	AJ2 NC
		IFPF_L1*	AJ1 NC
		IFPF_L2	AH2 NC
		IFPF_L2*	AH1 NC
		IFPF_L3	AG2 NC
		IFPF_L3*	AG1 NC
AJ12	DACA_VDD	DACA_RED	AM15 NC
		DACA_GREEN	AM14 NC
		DACA_BLUE	AL14 NC
AK12	DACA_VREF	DACA_HSYNC	AM13 NC
AJ13	DACA_RSET	DACA_VSYNC	AL13 NC
AC6	DACB_VDD	DACB_RED	AA4 NC
		DACB_GREEN	AA3 NC
		DACB_BLUE	Y4 NC
AC5	DACB_VREF	DACB_CSYNC	AB5
AB6	DACB_RSET		
AG7	DACC_VDD	DACC_RED	AK4 NC
		DACC_GREEN	AL4 NC
		DACC_BLUE	AK3 NC
AF6	DACC_VREF	DACC_HSYNC	AM1 NC
AG7	DACC_RSET	DACC_VSYNC	AN2 NC

GPU_I2CA_SCL B1 → G1 I2CA_SCL
GPU_I2CA_SDA B1 → G4 I2CA_SDA
GPU_I2CC_SCL B1 → E3 I2CC_SCL
GPU_I2CC_SDA B1 → E4 I2CC_SDA
=GPU_I2CS_SCL B1 → E2 I2CS_SCL
=GPU_I2CS_SDA B1 → E1 I2CS_SDA
GPU_I2CH_SCL B1 → F6 I2CH_SCL
GPU_I2CH_SDA B1 → G6 I2CH_SDA
GPU_I2CB_SCL B1 → G3 I2CB_SCL
GPU_I2CB_SDA B1 → G2 I2CB_SDA
GPU_I2CD_SCL B1 → F4 I2CD_SCL
GPU_I2CD_SDA B1 → G5 I2CD_SDA
GPU_I2CE_SCL B1 → D5 I2CE_SCL
GPU_I2CE_SDA B1 → E5 I2CE_SDA

LVDS_EG_A_CLK_P → CONN 83 94
LVDS_EG_A_CLK_N → CONN 83 94
LVDS_EG_A_DATA_P<0> → CONN 83 94
LVDS_EG_A_DATA_N<0> → CONN 83 94
LVDS_EG_A_DATA_P<1> → CONN 83 94
LVDS_EG_A_DATA_N<1> → CONN 83 94
LVDS_EG_A_DATA_P<2> → CONN 83 94
LVDS_EG_A_DATA_N<2> → CONN 83 94
LVDS_EG_A_DATA_P<3> → CONN 76
LVDS_EG_A_DATA_N<3> → CONN 76
LVDS_EG_B_CLK_P → CONN 76
LVDS_EG_B_CLK_N → CONN 76
LVDS_EG_B_DATA_P<0> → CONN 83 94
LVDS_EG_B_DATA_N<0> → CONN 83 94
LVDS_EG_B_DATA_P<1> → CONN 83 94
LVDS_EG_B_DATA_N<1> → CONN 83 94
LVDS_EG_B_DATA_P<2> → CONN 83 94
LVDS_EG_B_DATA_N<2> → CONN 83 94
LVDS_EG_B_DATA_P<3> → CONN 76
LVDS_EG_B_DATA_N<3> → CONN 76
DP_EG_AUX_CH_P → CONN 80 94
DP_EG_AUX_CH_N → CONN 80 94
DP_EG_ML_P<0> → CONN 80 94
DP_EG_ML_N<0> → CONN 80 94
DP_EG_ML_P<1> → CONN 80 94
DP_EG_ML_N<1> → CONN 80 94
DP_EG_ML_P<2> → CONN 80 94
DP_EG_ML_N<2> → CONN 80 94
DP_EG_ML_P<3> → CONN 80 94
DP_EG_ML_N<3> → CONN 80 94

NO STUFF
R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402

NV G96 Video Interfaces

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

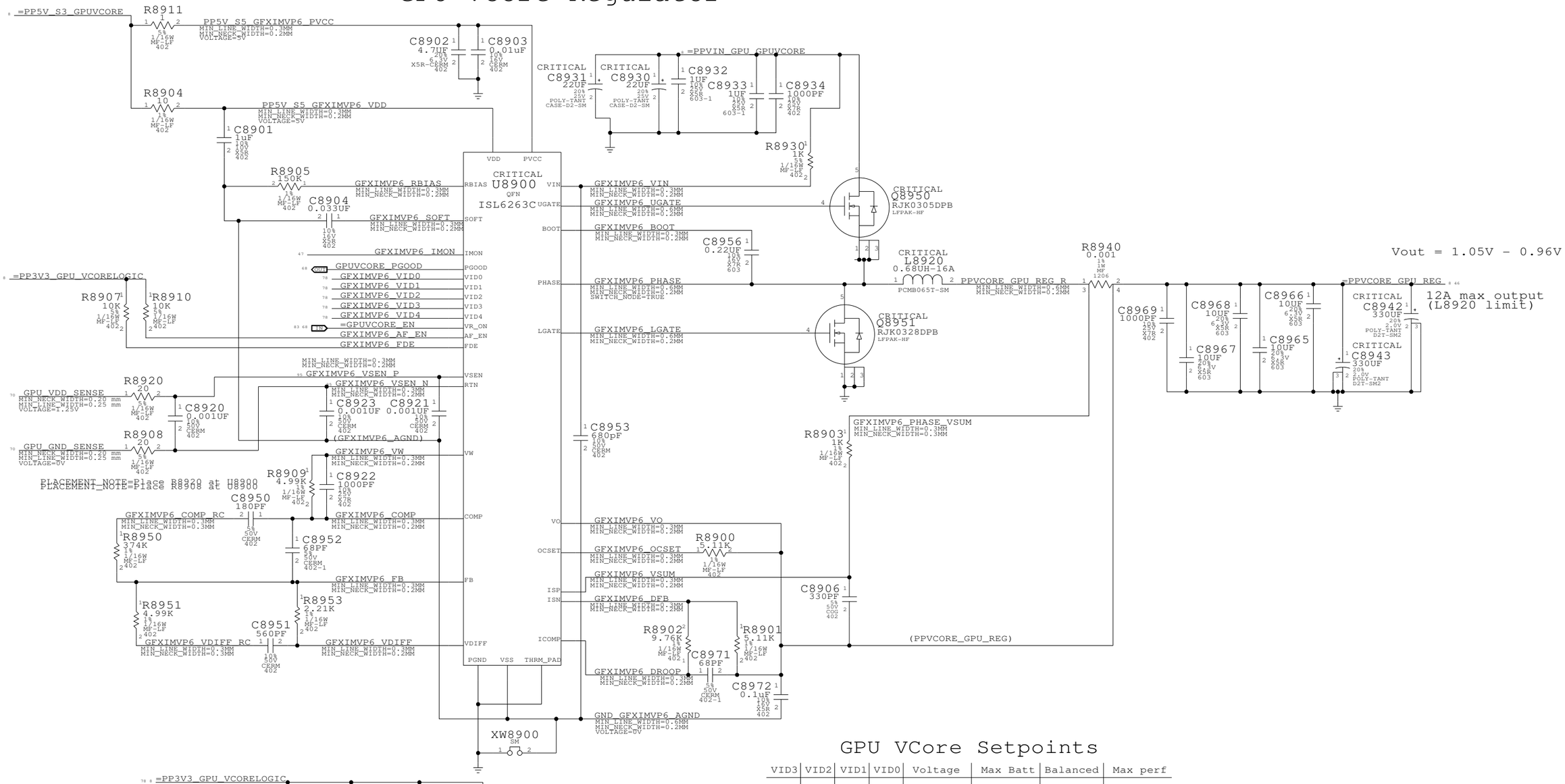
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 77 OF 96	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	M98		-
1	1	1	0	0.92700V	-	M98	-
1	0	1	1	1.00425V	-	-	M98

Other VID states may not be valid

M98 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G84M) Core Supply

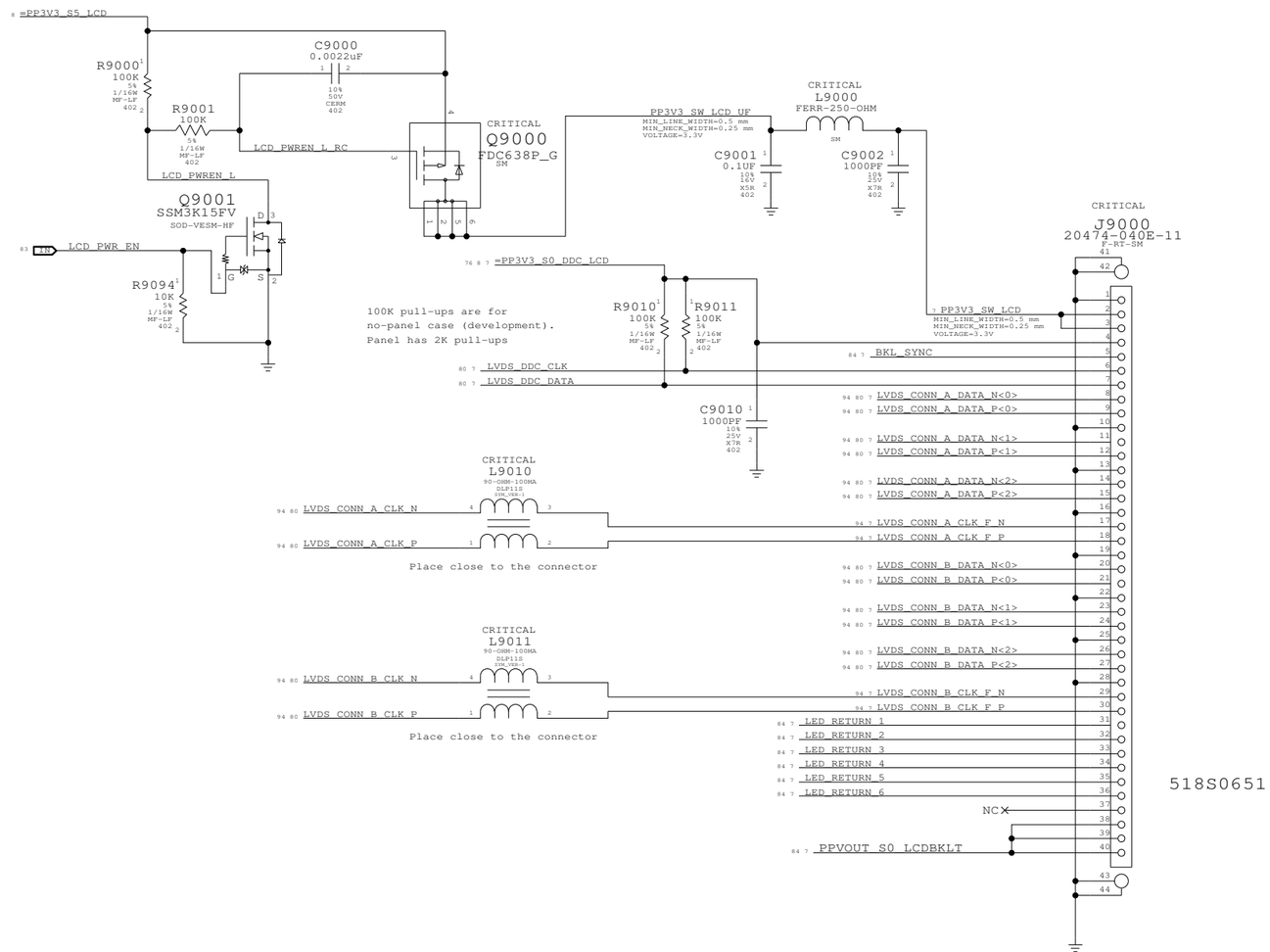
SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 78 OF 96

LCD (LVDS) INTERFACE



518S0651

LVDS Display Connector

SYNC_MASTER=MUXGFX SYNC_DATE=02/25/2008

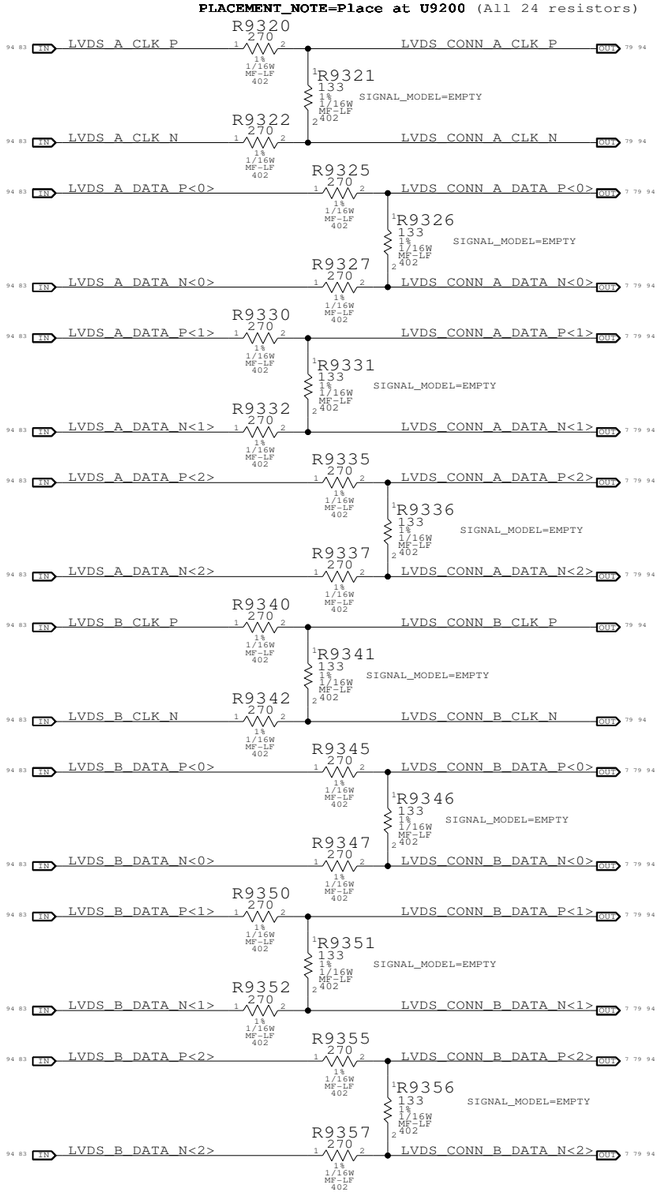
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 79 OF 96	

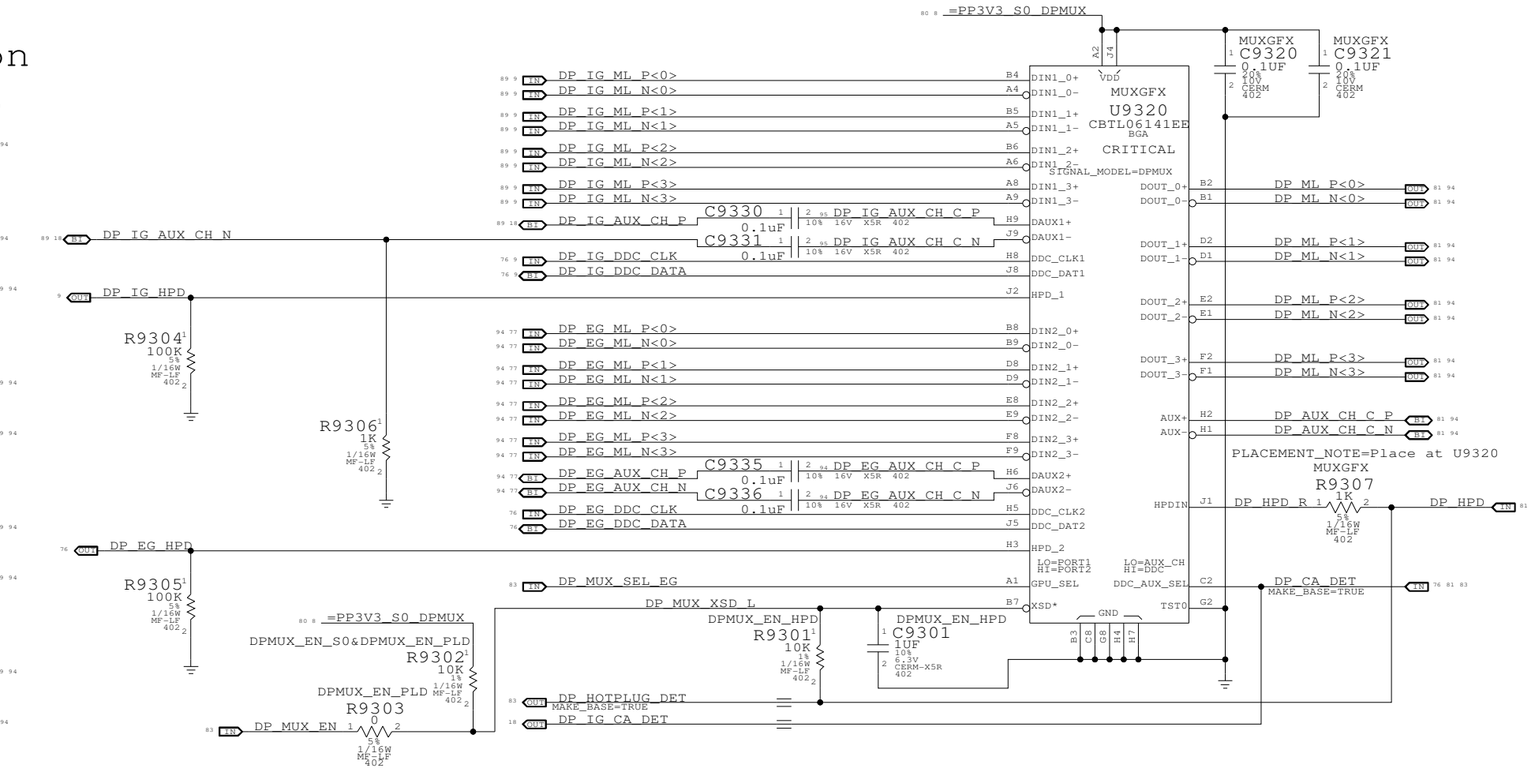
LVDS Transmitter Termination

All emulated LVDS outputs require this termination

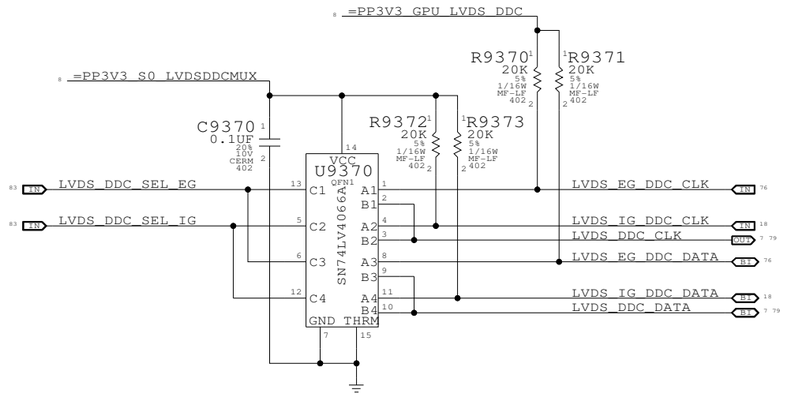
PLACEMENT_NOTE=Place at U9200 (All 24 resistors)



DisplayPort Mux



LVDS DDC MUX



Muxed Graphics Support

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 80 OF 96	

Port Power Switch

U9480 TPS2051B SOT23 (CRITICAL)
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L
C9480 10UF 20% 6.3V X5K 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
C9486 22UF 20% 6.3V X5R-CERM 603 (CRITICAL)
L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 20% 50V CERM 603
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
R9420 100K 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

HDMI_CEC
R9425 1M 5% 1/16W MF-LF 402
R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402
FL9403 12-OHM-100MA TCM1210-4SM

CRITICAL J9400 DSPLYPRT-M97-2 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS	
2	DP_HPD	1	GND
4	DP_C_A_DET	3	ML_LANE0P
6	HDMI_CEC	5	ML_LANE0N
8	GND	7	GND
10	ML_LANE3P	9	ML_LANE1P
12	ML_LANE3N	11	ML_LANE1N
14	GND	13	GND
16	AUX_CHP	15	ML_LANE2P
18	AUX_CHN	17	ML_LANE2N
20	DP_PWR	19	RETURN

SHIELD PINS

DP_ML_P<3> C9414 0.1uF 10% 16V X5R 402 → DP_ML_C_P<3> → DP_ML_CONN_P<3>
DP_ML_N<3> C9415 0.1uF 10% 16V X5R 402 → DP_ML_C_N<3> → DP_ML_CONN_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402
R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402
FL9400 12-OHM-100MA TCM1210-4SM
FL9401 12-OHM-100MA TCM1210-4SM
FL9402 12-OHM-100MA TCM1210-4SM
R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

DP_ML_C_P<0> C9410 0.1uF 10% 16V X5R 402 → DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF 10% 16V X5R 402 → DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF 10% 16V X5R 402 → DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF 10% 16V X5R 402 → DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF 10% 16V X5R 402 → DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF 10% 16V X5R 402 → DP_ML_N<2>

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
R9422 1M 5% 1/16W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

R9421 100K 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

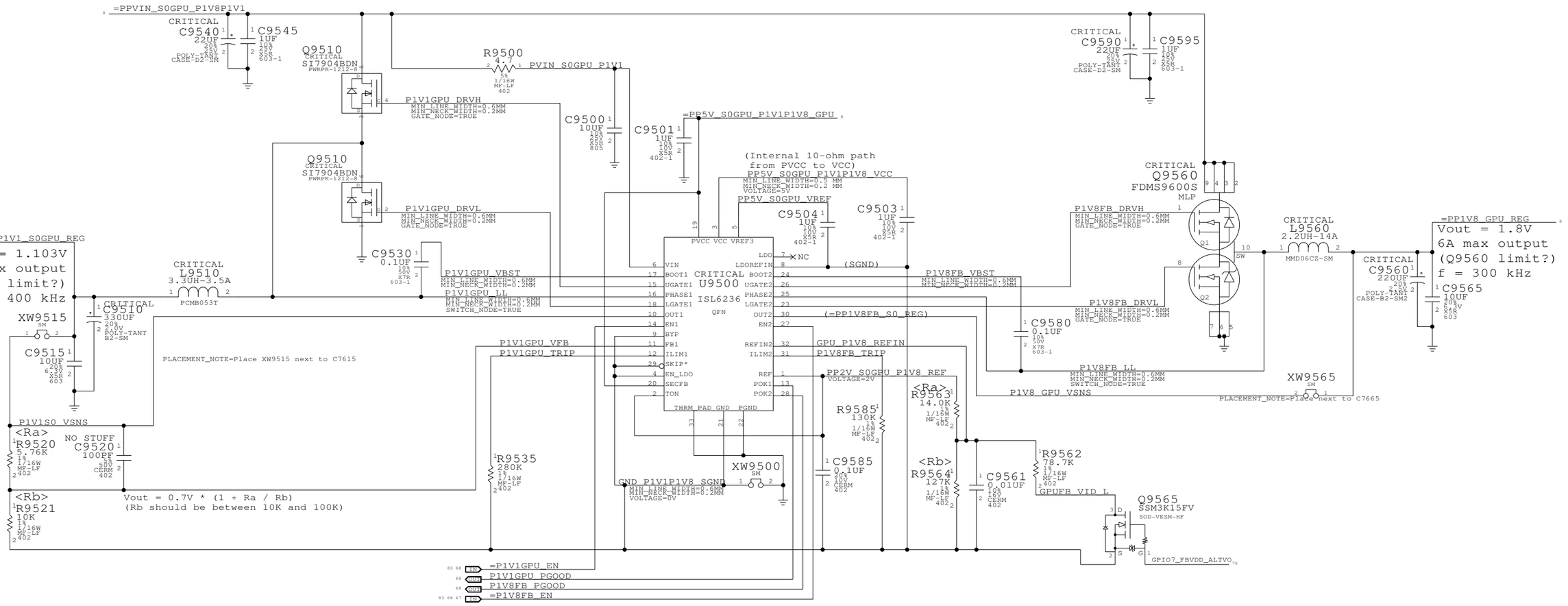
=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/16W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

DisplayPort Connector

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 81 OF 96	



1.1V / 1V8 FB Power Supply

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 82 OF 96	

GMUX CPLD

=PP3V3_S0_GMUX
C9610 0.1UF 20% 10V CERM 402
C9621 0.1UF 20% 10V CERM 402
C9622 0.1UF 20% 10V CERM 402
C9623 0.1UF 20% 10V CERM 402
C9624 0.1UF 20% 10V CERM 402
C9625 0.1UF 20% 10V CERM 402
C9626 0.1UF 20% 10V CERM 402
C9628 0.1UF 20% 10V CERM 402
C9629 0.1UF 20% 10V CERM 402
C9630 0.1UF 20% 10V CERM 402

=PP2V5_S0_GMUX
C9611 0.1UF 20% 10V CERM 402
C9612 0.1UF 20% 10V CERM 402
C9613 0.1UF 20% 10V CERM 402
C9614 0.1UF 20% 10V CERM 402
C9615 0.1UF 20% 10V CERM 402
C9616 0.1UF 20% 10V CERM 402
C9617 0.1UF 20% 10V CERM 402

=PP1V2_S0_GMUX
C9600 4.7UF 20% 10V X5R 402
C9604 0.1UF 20% 10V CERM 402
C9605 0.1UF 20% 10V CERM 402
C9606 0.1UF 20% 10V CERM 402
C9607 0.1UF 20% 10V CERM 402
C9608 0.1UF 20% 10V CERM 402
C9609 0.1UF 20% 10V CERM 402

=PP3V3_S0_GMUX
L9631 FERR-220-OHM 0402
PP3V3_S0_ULC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C9631 0.1UF 20% 10V CERM 402
L9627 FERR-220-OHM 0402
PP3V3_S0_LRC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C9627 0.1UF 20% 10V CERM 402

R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402
NO STUFF R9641 10K 1% 1/16W MF-LF 402
NO STUFF R9646 10K 1% 1/16W MF-LF 402
NO STUFF R9647 10K 1% 1/16W MF-LF 402

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO0: B5
VCCIO1: B7 A12
VCCIO2: C14
VCCIO3: F3
VCCIO4: M12 M9
VCCIO5: M3 N5
VCCIO6: M1
VCCIO7: C3 F2
VCCJ: K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

OMIT CRITICAL
U9600 XP28 CSBGA-HF

83 6	JTAG_GMUX_TCK	K14	TCK	
9	IN JTAG_GMUX_TDI	L13	TDI	
9	OUT JTAG_GMUX_TDO	K13	TDO	
9	IN JTAG_GMUX_TMS	L12	TMS	
	GMUX_TOE	K2	TOE	
	GMUX_CFG0	K1	CFG0	
9	OUT LCD_BKLT_EN	P2	PB2A	BANK5
84 83	OUT LCD_BKLT_PWM	N2	PB2B	
83 80	OUT LVDS_DDC_SEL_EG	P4	PB14A	
83 80	OUT LVDS_DDC_SEL_IG	N4	PB14B	
80	OUT DP_MUX_EN	N3	PB15A (OD)	
83 80	OUT DP_MUX_SEL_EG	M4	PB15B	
83 9	OUT EG_RESET_L	P5	PB16A	
83	OUT EG_RAIL1_EN	M5	PB16B	
83	OUT EG_RAIL2_EN	P6	PB17A	
83	OUT EG_RAIL3_EN	M6	PB17B	
83	OUT EG_RAIL4_EN	P7	PB18A	
83 9	OUT EG_CLKREQ_OUT_L	M7	PB18B (OD)	
76	OUT DP_CA_DET_EG	N7	PB19A	
76	OUT LCD_PWR_EN	N8	PB19B	
90 44 42 14	BI LPC_AD<0>	P9	PB20A	BANK4
90 44 42 14	BI LPC_AD<1>	N9	PB20B	
90 44 42 14	BI LPC_AD<2>	P10	PB30A	
90 44 42 14	BI LPC_AD<3>	M10	PB30B	
90 44 42 14	BI LPC_FRAME_L	P12	PB31A	
90 26 19	IN LPC_RESET_L	P13	PB31B	
26	IN LPC_CLK33M_GMUX	N12	PB32A	
83 9	OUT GMUX_INT	P14	PB32B	
89 83 18	IN LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
89 83 18	IN LVDS_IG_B_DATA_N<2>	B2	PL2B	
	TP_GMUX_PL10A	C2	PL10A	
	TP_GMUX_PL10B	D3	PL10B	
89 83 18	IN LVDS_IG_A_DATA_P<0>	D1	PL11A	
89 83 18	IN LVDS_IG_A_DATA_N<0>	E1	PL11B	
89 83 18	IN LVDS_IG_A_DATA_P<1>	D2	PL12A	
89 83 18	IN LVDS_IG_A_DATA_N<1>	E3	PL12B	
89 83 18	IN LVDS_IG_A_DATA_P<2>	F1	PL13A	
89 83 18	IN LVDS_IG_A_DATA_N<2>	G1	PL13B	
89 83 18	IN LVDS_IG_B_DATA_P<0>	F3	PL14A	
89 83 18	IN LVDS_IG_B_DATA_N<0>	G2	PL14B	
89 83 18	IN LVDS_IG_B_DATA_P<1>	H2	PL15A	
89 83 18	IN LVDS_IG_B_DATA_N<1>	G3	PL15B	
89 83 18	IN LVDS_IG_A_CLK_P	H1	PL16A	
89 83 18	IN LVDS_IG_A_CLK_N	H3	PL16B	
	OUT LVDS_MUX_SEL_EG	L1	PL18A	BANK6
	TP_GMUX_PL18B_VSYNC	L3	PL18B	
24	IN =GMUX_PCIE_RESET_L	K3	PL19A	
81	IN GMUX_PM_SLP_S3_L	L2	PL19B	
7	IN ALL_EG_PGOOD	N1	PL32A	
84	IN EG_CLKREQ_IN_L	P1	PL32B	

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

PT2A	A2	LVDS_B_DATA_P<0>	OUT 80 94	BANK0
PT2B	A3	LVDS_B_DATA_N<0>	OUT 80 94	
PT3A	A1	LVDS_B_DATA_P<1>	OUT 80 94	
PT3B	B3	LVDS_B_DATA_N<1>	OUT 80 94	
PT4A	C5	LVDS_B_DATA_P<2>	OUT 80 94	
PT4B	A5	LVDS_B_DATA_N<2>	OUT 80 94	
PT14A	B6	EG_PWRSEQ_EN	OUT 83	
PT14B	C7	GMUX_DEBUG_RESET_L	OUT 83	
PT15A	A6	LVDS_A_CLK_P	OUT 80 94	
PT15B	A7	LVDS_A_CLK_N	OUT 80 94	
PT16A	C8	LVDS_B_CLK_P	OUT 80 94	
PT16B	C9	LVDS_B_CLK_N	OUT 80 94	
PT17A	A8	LVDS_A_DATA_P<0>	OUT 80 94	
PT17B	B9	LVDS_A_DATA_N<0>	OUT 80 94	
PT18A	A9	LVDS_A_DATA_P<1>	OUT 80 94	
PT18B	C10	LVDS_A_DATA_N<1>	OUT 80 94	
PT19A	B10	LVDS_A_DATA_P<2>	OUT 80 94	
PT19B	A10	LVDS_A_DATA_N<2>	OUT 80 94	
PT20A	A11	TP_GMUX_PT20A		BANK1
PT20B	B12	TP_GMUX_PT20B		
PT32A	B13	TP_GMUX_PT32A		
PT32B	A13	TP_GMUX_PT32B		
PR2A	A14	DP_CA_DET	IN 76 80 81	BANK2
PR2B	B14	DP_HOTPLUG_DET	IN 80	
PR10A	D12	LVDS_EG_A_DATA_P<0>	IN 77 83 94	
PR10B	D13	LVDS_EG_A_DATA_N<0>	IN 77 83 94	
PR11A	D14	LVDS_EG_A_DATA_P<1>	IN 77 83 94	
PR11B	E14	LVDS_EG_A_DATA_N<1>	IN 77 83 94	
PR12A	E12	LVDS_EG_A_DATA_P<2>	IN 77 83 94	
PR12B	F12	LVDS_EG_A_DATA_N<2>	IN 77 83 94	
PR13A	F14	LVDS_EG_B_DATA_P<0>	IN 77 83 94	
PR13B	G14	LVDS_EG_B_DATA_N<0>	IN 77 83 94	
PR14A	G12	LVDS_EG_B_DATA_P<1>	IN 77 83 94	
PR14B	G13	LVDS_EG_B_DATA_N<1>	IN 77 83 94	
PR15A	H13	LVDS_EG_B_DATA_P<2>	IN 77 83 94	
PR15B	H12	LVDS_EG_B_DATA_N<2>	IN 77 83 94	
PR16A	H14	LVDS_EG_A_CLK_P	IN 77 83 94	
PR16B	J12	LVDS_EG_A_CLK_N	IN 77 83 94	
PR18A	L14	IG_LCD_PWR_EN	IN 9	BANK3
PR18B	M13	EG_LCD_PWR_EN	IN 76	
PR30A	N14	IG_BKLT_EN	IN 9	
PR30B	N13	EG_BKLT_EN	IN 76	

GND: J1 B8 C6 C12 C13 H13 H14 H10 H6 F3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_8K_BLANK
341S2350	1	IC,CPLD,LATTICE,132CSBGA,M98	U9600	CRITICAL	GMUX_PROG

PM_SLP_S3_L Isolation

83 8 =PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
42 37 34 21 7 81 68 44 IN PM_SLP_S3_L
GMUX_PM_SLP_S3_L 83
MAKE_BASE=TRUE
EG_PWRSEQ_EN 83

GMUX_JTAG_TCK Inversion

83 6 JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L IN 17

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

89 83 18	LVDS_IG_A_CLK_P	R9650	100 1% 1/16W MF-LF 402	LVDS_IG_A_CLK_N 18 83 89
89 83 18	LVDS_IG_A_DATA_P<0>	R9651	100 1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<0> 18 83 89
89 83 18	LVDS_IG_A_DATA_P<1>	R9652	100 1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<1> 18 83 89
89 83 18	LVDS_IG_A_DATA_P<2>	R9653	100 1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<2> 18 83 89
89 83 18	LVDS_IG_B_DATA_P<0>	R9654	100 1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<0> 18 83 89
89 83 18	LVDS_IG_B_DATA_P<1>	R9655	100 1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<1> 18 83 89
89 83 18	LVDS_IG_B_DATA_P<2>	R9656	100 1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<2> 18 83 89
94 83 77	LVDS_EG_A_CLK_P	R9660	100 1% 1/16W MF-LF 402	LVDS_EG_A_CLK_N 77 83 94
94 83 77	LVDS_EG_A_DATA_P<0>	R9661	100 1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<0> 77 83 94
94 83 77	LVDS_EG_A_DATA_P<1>	R9662	100 1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<1> 77 83 94
94 83 77	LVDS_EG_A_DATA_P<2>	R9663	100 1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<2> 77 83 94
94 83 77	LVDS_EG_B_DATA_P<0>	R9664	100 1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<0> 77 83 94
94 83 77	LVDS_EG_B_DATA_P<1>	R9665	100 1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<1> 77 83 94
94 83 77	LVDS_EG_B_DATA_P<2>	R9666	100 1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<2> 77 83 94

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX
83 GMUX_DEBUG_RESET_L R9680 1K 5% 1/16W MF-LF 402
83 6 JTAG_GMUX_TCK R9690 4.7K 5% 1/16W MF-LF 402
83 9 EG_CLKREQ_OUT_L R9695 10K 5% 1/16W MF-LF 402
NO STUFF R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9200

Required Pulldowns

83 80	DP_MUX_SEL_EG	R9681	10K 5% 1/16W MF-LF 402
83 80	LVDS_DDC_SEL_IG	R9682	10K 5% 1/16W MF-LF 402
83 80	LVDS_DDC_SEL_EG	R9683	10K 5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF
83 9 EG_RESET_L R9691 100K 5% 1/16W MF-LF 402
83 9 GMUX_INT R9692 20K 5% 1/16W MF-LF 402
84 83 LCD_BKLT_PWM R9693 100K 5% 1/16W MF-LF 402
83 EG_CLKREQ_IN_L R9694 100K 5% 1/16W MF-LF 402

EG_PWRSEQ_HW
R9630 0 5% 1/16W MF-LF 402 EXTGPU_PWR_EN OUT 68
83 EG_RAIL1_EN
EG_PWRSEQ_GMUX
R9631 0 5% 1/16W MF-LF 402 =P1V1GPU_EN OUT 68 82
83 EG_RAIL2_EN
EG_PWRSEQ_GMUX
R9632 0 5% 1/16W MF-LF 402 P3V3GPU_EN OUT 68 69
83 EG_RAIL3_EN
EG_PWRSEQ_GMUX
R9633 0 5% 1/16W MF-LF 402 =GPUVCORE_EN OUT 68 78
83 EG_RAIL4_EN
EG_PWRSEQ_GMUX
R9634 0 5% 1/16W MF-LF 402 =P1V8FB_EN OUT 67 68 82

The MAKE BASE properties for these signals are on the POWER CONTROL page.

NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

Graphics MUX (GMUX)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 83 OF 96	

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PPBUS_S0_LCDBKLT_PWR
VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.4 mm

R9730 0.1 1% 1/16W MF 402-HF

PPVIN_S0_LCDBKLT_BUF
VOLTAGE=12.6V
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.5MM

CRITICAL
C9701 10UF 10% 25V X5R 805
PLACEMENT_NOTE=Place near L9701

CRITICAL
L9701
22UH-2.5A
IHLP2525CZ-SM

PPVOUT_S0_LCDBKLT_SW
VOLTAGE=30V
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm
SWITCH_NODE=TRUE

PLACEMENT_NOTE=Place near Q9701
D9701
DO222-SM
STPS1H100MF

PLACEMENT_NOTE=Place near C9710
PLACEMENT_NOTE=Place near J9000

CRITICAL
C9709 2.2UF 10% 100V X7R 1210
CRITICAL
C9710 2.2UF 10% 100V X7R 1210

R9701 100 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near PPVOUT_S0_LCDBKLT_SW

Q9701
FDC5612
SSOT6

BOOST_FET_CNTL
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.6MM

4 PLACEMENT_NOTE=Place near C9709
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.5MM

XW9701
SM
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9701

GND_BKL_PWRGND
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.5MM

BKL_VIN
C9702 0.1UF 10% 25V X5R 402

BOOST_SINK
PLACEMENT_NOTE=Place near C9709 and Q9701
GND_BKL_PWRGND

R9704 100 1% 1/16W MF-LF 402
R9702 0.4 1% 1/16W MF 402
R9715 0.4 1% 1/16W MF 402

XW9702
SM
GND_BKL_PWRGND_X
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.5MM
PLACEMENT_NOTE=Place near C9709 and Q9701

BKL_VREF_4V9

R9731 187K 1% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR

BKLT_EN
BKL_SYNC
BKLT_PLL
R9734 0 5% 1/16W MF-LF 402
BKL_VSYNC

R9707 3.01K 1% 1/16W MF-LF 402
C9703 1UF 10% 10V X5R 402
C9713 0.1UF 10% 25V X5R 402
R9705 100K 5% 1/16W MF-LF 402
R9706 10K 5% 1/16W MF-LF 402

*R9702 AND R9715 PIN 1 SHOULD BE PLACED NEAR C9709 PIN 2
C9712 47PF 5% 50V CERM 402 NOSTUFF

U9701
GOSHAWK6P
QFN

VIN	3		
VREF	4	DRV	1
ENA	5	ISWSEN	2 BKL_ISWSEN
VSYNC	17	ISEN1	10 BKL_ISEN1
ISET	8	ISEN2	11 BKL_ISEN2
RT	6	ISEN3	12 BKL_ISEN3
SSTCMP	7	ISEN4	14 BKL_ISEN4
DIM	20	ISEN5	15 BKL_ISEN5
LPF	19	ISEN6	16 BKL_ISEN6
LRT	18	VSEN	9
GNDA	13	THRM_PAD	21

PPVOUT_S0_LCDBKLT
VOLTAGE=30V
MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.5 mm

R9717 10.2 0.1% 1/16W TF 402
LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm

R9718 10.2 0.1% 1/16W TF 402
LED_RETURN_5

R9719 10.2 0.1% 1/16W TF 402
LED_RETURN_4

R9720 10.2 0.1% 1/16W TF 402
LED_RETURN_3

R9721 10.2 0.1% 1/16W TF 402
LED_RETURN_2

R9722 10.2 0.1% 1/16W TF 402
LED_RETURN_1

PLACEMENT_NOTE=Away from Q9701
BKL_ISET
R9708 100K 1% 1/16W MF-LF 402
R9709 1K 1% 1/16W MF-LF 402
R9703 2.0M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Away from Q9701
BKL_RT

PLACEMENT_NOTE=Away from Q9701
BKL_SSTCMP
BKL_SSTCMP_RC
C9705 0.01UF 20% 16V CERM 402

BKLT_PWM_RC
R9733 0 5% 1/16W MF-LF 402
BKL_DIM
C9706 0.0022UF 10% 50V CERM 402 NOSTUFF
C9714 1UF 10% 10V X5R 402 NOSTUFF
BKL_LPF
BKL_LRT

BKL_VREF_4V9
R9713 0 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Away from Q9701
BKLT_PLL_NOT
PLACEMENT_NOTE=Away from Q9701
GND_BKL_PWRGND

BKLT_PLL
R9714 10K 5% 1/16W MF-LF 402
BKLT_PLL
C9707 2.2UF 20% 6.3V CERM 402-LF
BKLT_PLL
BKL_LRT_RC
C9708 0.1UF 10% 25V X5R 402

R9727 75K 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Away from Q9701

CRITICAL
Q9702
NTUD3127CXXG
SOT-963
P-CHN
BKL_VREF_4V9
BKL_VREF_IN_4V9
R9700 100K 1% 1/16W MF-LF 402
BKL_PWR_EN_L
R9710 10K 1% 1/16W MF-LF 402

CRITICAL
Q9702
NTUD3127CXXG
SOT-963
N-CHN
LCD_BKLT_PWM
R9711 30.1K 1% 1/16W MF-LF 402

PPVOUT_S0_LCDBKLT
R9723 1.2M 1% 1/10W MF-LF 603
BKL_VSEN
R9724 71.5K 1% 1/16W MF-LF 402

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

LCD BACKLIGHT DRIVER

SYNC_MASTER=YITE_M98_MLB
SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT: 84	OF: 96

Q9806 FDC638APZ_SBMS001 PPBUS S0 LCDBkLT FET

SSOT6-HF

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

8 IN =PPBUS_S0_LCDBKLT
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

F9800
2AMP-32V
0402-HF

PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

R9808
301K
1% 1/16W MF-LF 402

C9802
0.1UF
10% 16V X5R 402

PPBUS_S0_LCDBKLT_EN_DIV

R9809
147K
1% 1/16W MF-LF 402

PPBUS_S0_LCDBKLT_EN_L

Q9807
SSM6N15FEAPE
SOT563

85 9 IN LVDS_BKL_ON

BKLT_EN_L

Q9807
SSM6N15FEAPE
SOT563

26 IN BKLT_PLT_RST_L

PPBUS_S0_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
OUT 84

LVDS_BKL_ON 9 85

R9840
4.7K
5% 1/16W MF-LF 402

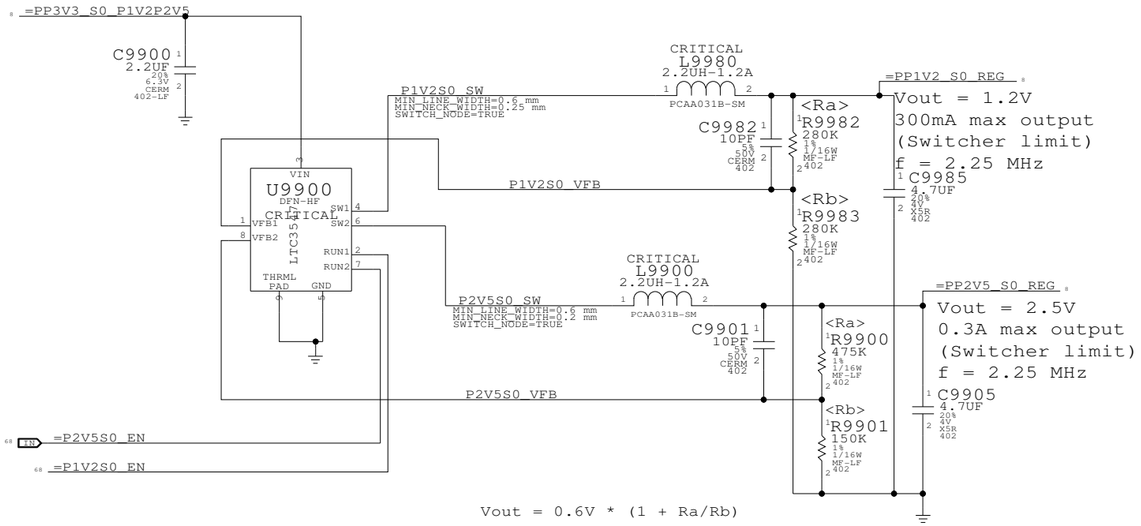
LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 85 OF 96	

2.5V/1.2V S3 Switcher



Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 86 OF 96	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 43 62
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 43
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 62
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 62
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 27
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 62
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 62
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 62
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	62
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	62

CPU/FSB Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 87 OF 96

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE: NONE SHT 88 OF 96

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	70
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	70
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 70
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 70
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 70
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 70
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	70
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	70
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	31 95
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	31 95
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 31
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 31
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 31
	PCIE_90D	PCIE	PCIE_FW_R2D_P	36
	PCIE_90D	PCIE	PCIE_FW_R2D_N	36
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 36
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 36
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	36
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 32 95
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 32 95
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 32
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 32
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 32
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 32
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 70
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 70
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 31
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 36
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 36
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 32
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 32
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 25
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 25
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 25
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 25
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 25
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 25
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 25
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 80
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 80
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 80
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 80
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 25
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 25
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 83
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 83
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 83
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 83
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 83
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 83
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 25
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 25
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 39
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 39
	SATA_100D	SATA	SATA_HDD_R2D_P	39
	SATA_100D	SATA	SATA_HDD_R2D_N	39
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 39
	SATA_100D	SATA	SATA_HDD_D2R_N	20 39
	SATA_100D	SATA	SATA_HDD_D2R_C_P	39
	SATA_100D	SATA	SATA_HDD_D2R_C_N	39
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 39
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 39
	SATA_100D	SATA	SATA_ODD_R2D_P	7 39
	SATA_100D	SATA	SATA_ODD_R2D_N	7 39
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 39
	SATA_100D	SATA	SATA_ODD_D2R_N	20 39
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 39
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 39
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	89	96

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 42 44 83
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 42 44 83
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26 83
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 26
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26 42
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 44
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 40
	USB_90D	USB	USB_EXTA_N	20 40
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 31
	USB_90D	USB	USB_CAMERA_N	20 31
USB_BT	USB_90D	USB	USB_BT_P	20 31
	USB_90D	USB	USB_BT_N	20 31
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
	USB_90D	USB	USB_TPAD_N	20 50
USB_IR	USB_90D	USB	USB_IR_P	20 41
	USB_90D	USB	USB_IR_N	20 41
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 40
	USB_90D	USB	USB_EXTB_N	20 40
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 32
	USB_90D	USB	USB_EXCARD_N	20 32
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
	USB_90D	USB	USB_EXTC_N	9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 45
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 45
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 45
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 54
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 54
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 54
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 54
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 44
	SPI_55S	SPI	SPI_CLK	44 53
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 44
	SPI_55S	SPI	SPI_MOSI	44 53
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 44
	SPI_55S	SPI	SPI_MISO_R	53
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 44
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE: NONE SHT: 90 OF 96

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 34
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	33 34
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 33
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 33
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	33
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 33
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 33
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 33
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 33
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 33
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 33
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	33 35
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	33 35

Ethernet Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 91 OF 96	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P 36 38
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N 36 38
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P 36 38
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N 36 38
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P 36 38
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N 36 38
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P 36 38
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N 36 38

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	92	96

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 7 45
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 7 45
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 45
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 45
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 45
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 45
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 45
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 45
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 45
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 45

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 61
	1TO1_DIFFPAIR		CHGR_CSI_N 61
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 61
	1TO1_DIFFPAIR		CHGR_CSO_N 61

SMC Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-7546 | REV. A.0.0

SCALE NONE | SHT 93 OF 96

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:
Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_ED	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L
FB_AB_CMD_ED	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
(CK505_DOT96)	CLK_SLOW_5SS	CLK_SLOW	GPU_CLK27M
CK505_CLK27MSS	CLK_SLOW_5SS	CLK_SLOW	GPU_CLK27M_SS
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_ED	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L
FB_CD_CMD_ED	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>

GPU (G96) Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 94 OF 96	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0> 35
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0> 35
	SATA_100D	SATA	SATA_ODD_R2D_UF_P 39
	SATA_100D	SATA	SATA_ODD_R2D_UF_N 39
	SATA_100D	SATA	SATA_ODD_D2R_UF_P 39
	SATA_100D	SATA	SATA_ODD_D2R_UF_N 39
	SATA_100D	SATA	SATA_HDD_D2R_UF_P 39
	SATA_100D	SATA	SATA_HDD_D2R_UF_N 39
	SATA_100D	SATA	SATA_HDD_R2D_UF_P 39
	SATA_100D	SATA	SATA_HDD_R2D_UF_N 39
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P 78
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P 47 65
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N 47 65
CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 48
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 48
CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P 10 48
	THERM_1TO1_55S	THERM	CPU_THERMD_N 10 48
GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P 48
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N 48
GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P 48 76
	THERM_1TO1_55S	THERM	GPU_TDIODE_N 48 76
MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P 48
	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N 48
MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P 21 48
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N 21 48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P 47
	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P 47
	SENSE_1TO1_55S	SENSE	DDRISNS_R_N 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P 47
	SENSE_1TO1_55S	SENSE	GPUISENS_N 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P 47 66
	SENSE_1TO1_55S	SENSE	1V05CPU_N 47 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P 47
	SENSE_1TO1_55S	SENSE	DDRISNS_N 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P 47
	SENSE_1TO1_55S	SENSE	P1V8GPU_N 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P 46
	SENSE_1TO1_55S	SENSE	ISNS_CPU_N 46
		GND	GND
		SB_POWER	PP3V3_S5 7 8
		SB_POWER	PP3V3_S0 7 8
		SB_POWER	PP1V5_S0
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P 47
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N 47

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P 7 32 89
(PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N 7 32 89
	PCIE_90D	PCIE	PCIE_MINI_R2D_P 31 89
(PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_N 31 89
(PCIE_MINI)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P 61
	1TO1_DIFFPAIR		CHGR_CSI_R_N 61
	1TO1_DIFFPAIR		CHGR_CSO_R_P 46 61
	1TO1_DIFFPAIR		CHGR_CSO_R_N 46 61
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P 40
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N 40
(USB_EXTA)	USB_90D	USB	USB2_LT1_P 40
(USB_EXTA)	USB_90D	USB	USB2_LT1_N 40
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P 31
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N 31
	USB_90D	USB	CONN_USB2_BT_P 31
	USB_90D	USB	CONN_USB2_BT_N 31
	USB_90D	USB	USB_LT2_P 40
	USB_90D	USB	USB_LT2_N 40
	USB_90D	USB	USB2_EXCARD_CONN_P 7 32
	USB_90D	USB	USB2_EXCARD_CONN_N 7 32
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P 80
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N 80
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P 9 32
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N 9 32
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P 9 32
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N 9 32
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P 9 32
	PCIE_90D	PCIE	PCIE_FC_D2R_N 9 32
	PCIE_90D	PCIE	PCIE_FC_R2D_P 32
	PCIE_90D	PCIE	PCIE_FC_R2D_N 32
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N 7 32
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P 7 32
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_P_OUT 7 57 58
	DIFFPAIR	AUDIO	SPKRCONN_L_N_OUT 7 57 58
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_P_OUT 7 57 58
	DIFFPAIR	AUDIO	SPKRCONN_S_N_OUT 7 57 58
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_P_OUT 7 57 58
	DIFFPAIR	AUDIO	SPKRCONN_R_N_OUT 7 57 58
	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT 57
	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT 57
	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT 57
	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT 57
	DIFFPAIR	AUDIO	SPKRAMP_S_P_OUT 57
	DIFFPAIR	AUDIO	SPKRAMP_S_N_OUT 57

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_90D	TOP			0.09 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	ISL4,ISL9						
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	ISL3,ISL10	N					
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL4,ISL9						
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD	ISL3,ISL10	N					
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Project Specific Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	95	96

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	14 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M99_MLB SYNC_DATE=01/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 96 OF 96