

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2012-02-23

J11 MLB PIB SCHEMATIC

2.6.0

02/23/12

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37	SSD CONNECTOR	J13_MLB	11/18/2011
38	External A USB3 Connector	J13_MLB	10/06/2011
39	LIO CONNECTORS	N/A	N/A
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42	LPC+SPI Debug Connector	K21_MLB	12/13/2010
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44	Voltage & Load Side Current Sensing	J13_MLB	09/15/2011
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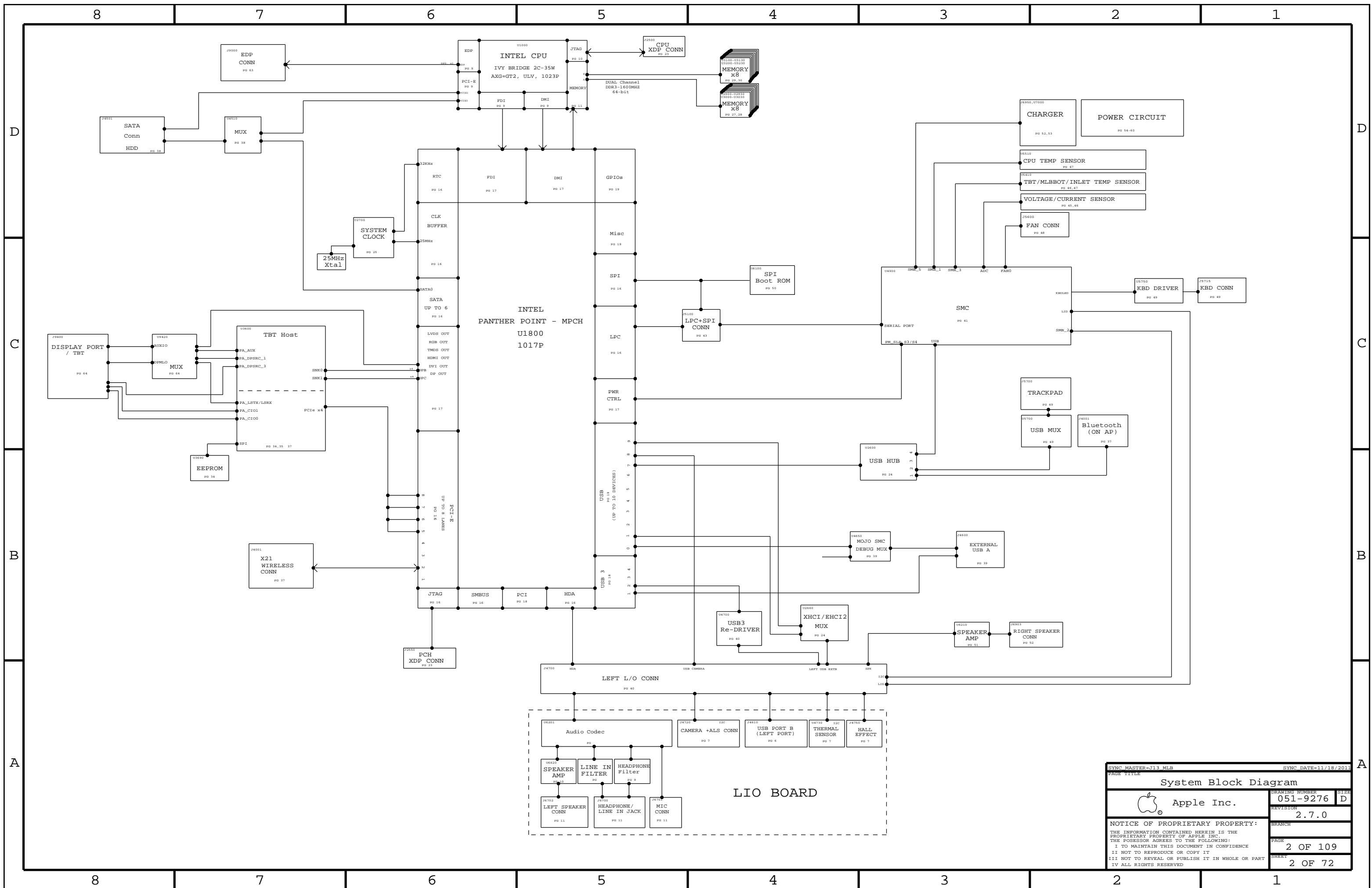
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9276	1	SCHEM_MLB_J11	SCH	CRITICAL	
820-3209	1	PCBF_MLB_J11	PCB	CRITICAL	

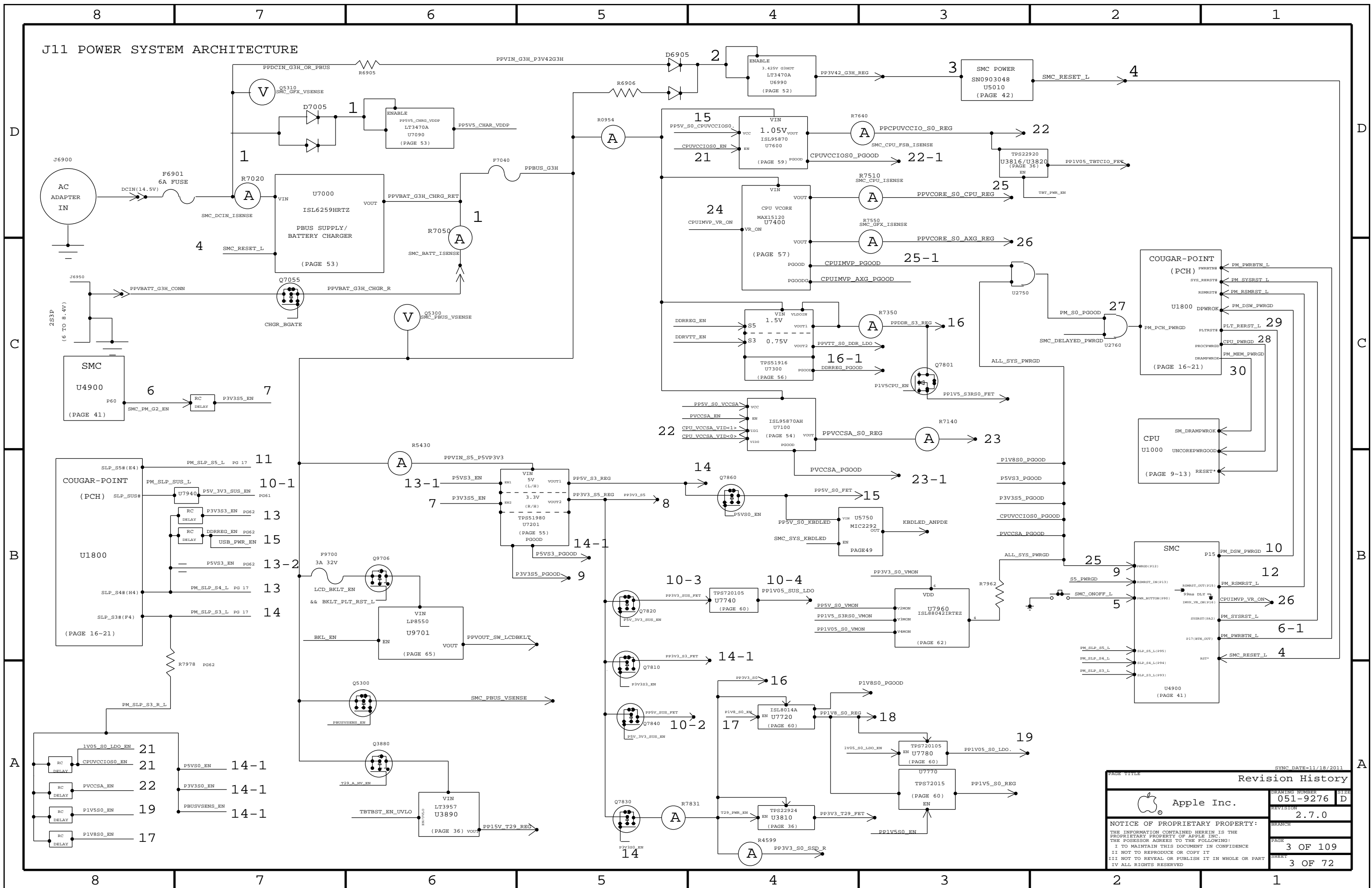
PRODUCT SAFETY REQUIREMENTS:
 PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
 PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
 NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE		SCHEM_MLB_J11	
	DRAWING NUMBER	051-9276	SIZE D
	REVISION	2.7.0	
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SYNC MASTER=113 MLB		SYNC DATE=11/18/2011	
PAGE TITLE			
System Block Diagram			
Apple Inc.	DRAWING NUMBER	051-9276	SIZE
	REVISION	2.7.0	D
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J11 POWER SYSTEM ARCHITECTURE



Revision History		
Apple Inc.	Drawing Number	051-9276
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BOM Variants


BOM NUMBER	BOM NAME	BOM OPTIONS
639-3469	PCBA_MLB,1.5GHZ,HY 4GB,J11	J11_OBNPTS,CP01.5GHZ,EEEE:DVKL,DDR3:HYNIX_4GB
639-3470	PCBA_MLB,1.5GHZ,SA 4GB,J11	J11_OBNPTS,CP01.5GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB
639-3473	PCBA_MLB,1.5GHZ,HY 8GB,J11	J11_OBNPTS,CP01.5GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB
639-3659	PCBA_MLB,1.5GHZ,EL 8GB,J11	J11_OBNPTS,CP01.5GHZ,EEEE:FOV3,DDR3:ELPIDA_8GB
639-3471	PCBA_MLB,1.7GHZ,HY 4GB,J11	J11_OBNPTS,CP01.7GHZ,EEEE:DVKL,DDR3:HYNIX_4GB
639-3472	PCBA_MLB,1.7GHZ,SA 4GB,J11	J11_OBNPTS,CP01.7GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB
639-3775	PCBA_MLB,1.7GHZ,EL 4GB,J11	J11_OBNPTS,CP01.7GHZ,EEEE:F27J,DDR3:ELPIDA_4GB
639-3474	PCBA_MLB,1.7GHZ,HY 8GB,J11	J11_OBNPTS,CP01.7GHZ,EEEE:FOV4,DDR3:HYNIX_8GB
639-3774	PCBA_MLB,1.7GHZ,SA 8GB,J11	J11_OBNPTS,CP01.7GHZ,EEEE:F27D,DDR3:SAMSUNG_8GB
639-3660	PCBA_MLB,1.7GHZ,EL 8GB,J11	J11_OBNPTS,CP01.7GHZ,EEEE:FOV4,DDR3:ELPIDA_8GB
639-3776	PCBA_MLB,2.0GHZ,HY 4GB,J11	J11_OBNPTS,CP01.2.0GHZ,EEEE:F27K,DDR3:HYNIX_4GB
639-3778	PCBA_MLB,2.0GHZ,SA 4GB,J11	J11_OBNPTS,CP01.2.0GHZ,EEEE:F27D,DDR3:SAMSUNG_4GB
639-3780	PCBA_MLB,2.0GHZ,EL 4GB,J11	J11_OBNPTS,CP01.2.0GHZ,EEEE:F27H,DDR3:ELPIDA_4GB
639-3777	PCBA_MLB,2.0GHZ,HY 8GB,J11	J11_OBNPTS,CP01.2.0GHZ,EEEE:F27C,DDR3:HYNIX_8GB
639-3779	PCBA_MLB,2.0GHZ,SA 8GB,J11	J11_OBNPTS,CP01.2.0GHZ,EEEE:F27F,DDR3:SAMSUNG_8GB
639-3781	PCBA_MLB,2.0GHZ,EL 8GB,J11	J11_OBNPTS,CP01.2.0GHZ,EEEE:F27J,DDR3:ELPIDA_8GB
085-3937	J11 MLB DEVELOPMENT BOM	J11_DEVEL:BNB
607-9089	CMN PTS,PCBA_MLB,J11	J11_CMNPTS
939-0479	PCBA_MLB,1.9GHZ,HY 4GB,J11	J11_OBNPTS,CP01.9GHZ,EEEE:DVKL,DDR3:HYNIX_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_DVKL]	CRITICAL	EEEE:DVKL
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_DYKH]	CRITICAL	EEEE:DYKH
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_DYKF]	CRITICAL	EEEE:DYKF
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_DYKG]	CRITICAL	EEEE:DYKG
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_FOV3]	CRITICAL	EEEE:FOV3
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_FOV4]	CRITICAL	EEEE:FOV4
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F279]	CRITICAL	EEEE:F279
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27C]	CRITICAL	EEEE:F27C
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27D]	CRITICAL	EEEE:F27D
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27F]	CRITICAL	EEEE:F27F
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27G]	CRITICAL	EEEE:F27G
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27H]	CRITICAL	EEEE:F27H
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27J]	CRITICAL	EEEE:F27J
825-7670	1	LABEL,TEXT_MLB,K21/K78	[EEEE_F27K]	CRITICAL	EEEE:F27K

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3937	1	J11 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9089	1	CMN PTS,PCBA_MLB,J11	CMNPTS	CRITICAL	J11_CMNPTS

SYNC MASTER=K21_MLB		SYNC DATE=11/16/2016	
K78 BOM Variants			
 Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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J11 BOM GROUPS

BOM GROUP	BOM OPTIONS
J11_COMMON	ALTERNATE,COMMON,J11_MISC,J11_DEBUG:ENG,J11_PROGPARTS,USBHUB2513B,EDP:YES,PCH_C1
J11_MISC	HUB_3NONREM,TWT,MMS:YES,CPUMEM_SLD:NO,PPSV5_DCIN:NO,TPAD_PCH:NO,SKIP_SV3V3:INAUDIBLE,BTFWR:84,TBTWV:F15V,LVDSR3_JW:YES,AXL_ACOUSTICS:NO
J11_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J11_DEVEL:ENG	ALTERNATE,BELT:ENG,XDP_CORE,XDP_PCH,DEVRWF_DAC,VREFDQ:MLX1,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDKLTISNS_PROD
J11_DEVEL:PVT	XDP_CORE
J11_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP_XDP_CPU:BPM,LPCPLUS
J11_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP_LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDKLTISNS_PROD
J11_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP_LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDKLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
3350865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2K3QFN	U3690	CRITICAL	TBTROM:BLANK
34183526	1	IC,EEPROM,Cactus Ridge (V1.2) DIB, J11/J13	U3690	CRITICAL	TBTROM:PROG
33801098	1	IC,SMC12-A3,40MHZ/50MHZ,933,933,197WGA	U4900	CRITICAL	SMC:BLANK
34183434	1	IC,SMC,DIB,J11	U4900	CRITICAL	SMC:PROG
3350809	1	64 MBIT SPI SERIAL FLASH, 1.8V, 1.579GA	U6100	CRITICAL	BOOTROM:BLANK
3350803	1	64 MBIT SPI SERIAL FLASH, 1.8V, 1.579GA	U6100	CRITICAL	BOOTROM:BLANK
34183527	1	IC,EFI ROM,DIB,J11/J13	U6100	CRITICAL	BOOTROM:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37600855	37600613		ALL	Diodes alt to Toshiba
37600977	37600859		ALL	Diodes alt to Toshiba
37600972	37600612		ALL	Resistor alt to Toshiba
13800676	13800691		ALL	Murata alt to Samsung
37100709	37100652		ALL	MDP alt to BXP
13800671	13800673		ALL	Taiyo alt to Murata
15201085	15201307		ALL	Toko alt to Cytac
15201462	15201295		ALL	Toko alt to NEC inductor
13800684	13800660		ALL	Murata alt to Taiyo Yuden
13800703	13800648		ALL	Murata alt to Taiyo Yuden
15201493	15201300		ALL	Colicraft MAS274 alt to Murata
15200566	15201301		ALL	Dala/Vishay alt to Cytac
35303238	35301428		ALL	Intersil alt to OPA2333
37200186	37200185		ALL	MDP alt to Diodes
19700431	19700432		ALL	200W Spsom alt to MDC
37601053	37600604		ALL	Diodes alt to Fairchild
37600855	37600613		ALL	Diodes alt to Toshiba
37600903	37600796		ALL	Fairchild alt to Siliconix
37100713	37100558		ALL	Diodes alt to ST Micro
12803333	998-4435		ALL	Sanyo alt to Kemet
12803257	998-4435		ALL	Sanyo High Voltage Polymer alt
998-4715	998-4435		ALL	Kemet Rectangular Design alt
998-4716	998-4435		ALL	Kemet Plute Design alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2	DIE REV	CFG 3
4GB	0	A	0
8GB	1	B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB_QBP8,ES2,K0.1.5.17W,2+2.0.95,4M,ULV8	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB_QC98,Q8,L1.1.7.17W,2+2.1.05,3M,ULV8G	U1000	CRITICAL	CPU:1.7GHZ
337S4296	1	IVB_QC98,Q8,L1.2.0.17W,2+2.1.15,4M,ULV8G	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB_QBP8,ES2,K0.1.5.17W,2+2.0.95,4M,ULV8GA	U1000	CRITICAL	CPU:1.5GHZTDP
337S4299	1	IVB_QC98,Q8,L1.1.7.17W,2+2.1.05,3M,ULV8G	U1000	CRITICAL	CPU:1.7GHZTDP
337S4296	1	IVB_QC98,Q8,L1.2.0.17W,2+2.1.15,4M,ULV8G	U1000	CRITICAL	CPU:2.0GHZTDP
337S4297	1	IVB_QC98,Q8,L1.1.9.17W,2+2.1.15,4M,ULV8G	U1000	CRITICAL	CPU:1.9GHZ
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-Q8,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,Q877,C1,Q8	U1800	CRITICAL	PCH_C1
337S4275	1	IC,PCH,PPT-MB,Q877,C1,Q8	U1800	CRITICAL	PCH_C1TDP
336S1108	1	IC,TBT,CR-4C,LP,ES3,288 PCBGA,12X12MM	U3600	CRITICAL	TWT

333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GENMA,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GENMA,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GENMA,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GENMA,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB

607-6811	1	ASSEMBLY,SUBASBY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL6259,BATCHCHARGER,3A,4CANM,QFN28	U7000	CRITICAL	
946-3116	1	MLB,DTMAX UV EB 0.22 GRAM,K78	GL0E	CRITICAL	

PD Module Parts

806-3706	1	CAN, TOPSIDE, COVER, ALT, J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN, TOPSIDE, FENCE, ALT, J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3214	1	CAN, TOPSIDE, J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3216	1	CAN, MDP, J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD, USB, MLB, J11/J13	USBCAN	CRITICAL	
806-3142	1	CAN, TWT, J11/J13	TBTFWENCE	CRITICAL	
806-3215	1	CAN, COVER, TWT, J11/J13	TBTFCOVER	CRITICAL	

SYMC PARTS:J11_MBR_8008_002 SYMC DATE:11/09/2011

PAGE TITLE

BOM Configuration

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DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST	TP	NC
PP3V3 WLAN F (Need 6 TPs)	36 41	
WiFi EVENT L	36 40 41	
PCIE AP R2D N	36 68	
PCIE AP R2D P	36 68	
PCIE CLK100M AP N	16 36 68	
PCIE CLK100M AP P	16 36 68	
USB BT CONN P	36 67	
USB BT CONN N	36 67	
PCIE AP D2R P	16 36 68	
PCIE AP D2R N	16 36 68	
PCIE WAKE L	17 36	
AP RESET CONN L	36	
AP CLKREQ O L	36	
PP3V3 S3RS4 BT F	36	

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST	TP	NC
PP3V3 S0 SSD FLT (Need 5 TPs)	37	
SATA SSD D2R P	37 67	
SATA SSD D2R N	37 67	
SATA SSD R2D N	37 67	
SATA SSD R2D P	37 67	
SMC OOB1 RX L	37 40	
SMC OOB1 TX L	37 40 41	
PCIE SSD D2R N<1>	8 37 65	
PCIE SSD D2R P<1>	8 37 65	
PCIE SSD R2D N<1>	37 65	
PCIE SSD R2D P<1>	37 65	
PCIE CLK100M SSD N	16 37 65	
PCIE CLK100M SSD P	16 37 65	
SSD CLKREQ L	16 37	
SSD RESET L	28 37	
SATA PCIE SEL	37	
SSD P3V3S0 EN	37	

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST	TP	NC
PP3V42 G3H ONEWIRE	7 39	
PP3V3 S0 AUDIO	7 39	
PP3V3R1V5 S0 AUDIO	7 39	
SYS ONEWIRE	39 40	
SMC BC ACOK	39 40 41	
USB PWR EN	39 39 61	
I2C LIO SDA	39 43	
I2C LIO SCL	39 43	
I2C MIKEY SCL	39 43	
I2C MIKEY SDA	39 43	
AUD IPHS SWITCH EN	25 39	
AUD IP PERIPHERAL DET	18 39	
AUD I2C INT L	18 39	
AUD GPIO 3	39 60	
SPKRAMP INR N	39 50 71	
SPKRAMP INR P	39 50 71	
USB EXTB N	24 39 67	
USB EXTB P	24 39 67	
USB CAMERA N	18 39 67	
USB CAMERA P	18 39 67	
HDA SDOUT	16 39 68	
HDA BIT CLK	16 39 68	
HDA SDIN0	16 39 68	
USB EXTB OC L	23 39	
HDA RST L	16 39 68	
HDA SYNC	16 39 68	
USB3 EXTB RX RC N	39 67	
USB3 EXTB RX RC P	39 67	
USB3 EXTB TX C P	39 67	
USB3 EXTB TX C N	39 67	

(Need to add 5 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST	TP	NC
PP3V3 S5 LPCPLUS	7 42	
PP5V S0 LPCPLUS	7 42	
LPC AD<3..0>	16 40 42 68	
SPI ALT MOSI	42	
SPI ALT MISO	42	
LPC FRAME L	16 40 42 68	
PM CLKRUN L	17 40 42	
SMC TMS	40 41 42	
LPCPLUS RESET L	25 42 68	
SMC TDO	40 41 42	
TP SMC TRST L	42	
TP SMC MD1	42	
SMC TX L	40 41 42	
LPC CLK33M LPCPLUS	25 42 68	
SPIROM USE MLB	19 42 49	
SPI ALT CLK	42	
SPI ALT CS L	42	
LPC SERIRO	16 40 42	
LPC PWRDWN L	17 25 40 42	
SMC TDI	40 41 42	
SMC TCK	40 41 42	
SMC RESET L	40 41 42 62	
SMC ROMBOOT	41 42	
SMC RX L	40 41 42	
LPCPLUS GPIO	19 42	

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST	TP	NC
PP5V S0 FAN	7 47	
FAN RT TACH	47	
FAN RT PWM	47	

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST	TP	NC
SMC PME S4 WAKE L	40 41 48	
PP5V TPAD FILT	48	
PP3V42 G3H TPAD	7 48	
PP3V3 TPAD CONN	48	
USB TPAD P	48 67	
USB TPAD N	48 67	
I2C TPAD SDA	43 48	
I2C TPAD SCL	43 48	
SMC ONOFF L	40 41 48	
SMC LID	40 41 48 51	
SMC TPAD RST L	41 48	

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST	TP	NC
PP18V5 DCIN CONN	7 51	(Need 4 TPs)
PP5V S3 LIO CONN	7 51	(Need 3 TPs)

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST	TP	NC
SPKRAMP ROUT P	50 51 71	
SPKRAMP ROUT N	50 51 71	

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST	TP	NC
PPVBAT G3H CONN	51 52	(Need 4 TPs)
SMBUS BATT SCL	43 51	
SMBUS BATT SDA	43 51	
SYS DETECT L	51	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST	TP	NC
PPVOUT SW LCDBKLT	62 64	(Need 2 TPs)
PP3V3 SW LCD	62	(Need 2 TPs)
I2C TCON SDA R	62	
LED RETURN 6	62 64	
LED RETURN 5	62 64	
LED RETURN 4	62 64	
LED RETURN 3	62 64	
LED RETURN 2	62 64	
LED RETURN 1	62 64	
DP INT HPD CONN	62 64	
DP INT AUX CH C N	62 65	
DP INT AUX CH C P	62 65	
DP INT ML F P<0>	62 65	
DP INT ML F N<0>	62 65	
I2C TCON SCL R	62	

(Need to add 5 GND TPs)

J5715: KB BKLT Connector

FUNC_TEST	TP	NC
KBDLED FB	48	
KBDLED ANODE	48	

(Need to add 2 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST	TP	NC
SMC LID R	51	
PP3V42 G3H HALL	7 51	

Misc Voltages & Control Signals

FUNC_TEST	TP	NC
PPBUS G3H	7 51	
PPVIN SW TBTBST	7 35	
PPBUS S5 HS COMPUTING ISNS	7	
PPDCIN G3H	7	
PP3V42 G3H	7	
PPVRTC G3H	7	
PP5V S5	7	
PP5V SUS	7	
PP3V3 S5	7 71	
PP3V3 SUS	7	
PP3V3 S3	7	
PP1V8 S0	7	
PP3V3 S0	7 71	
PP1V5 S3	7 66	
PP1V5 S3RS0	7 66	
PP1V5 S0	7	
PP1V05 S0	7	
PPVTDDR S3	7	
PPOV75 S0 DDRVTT	7	
PPVCCSA S0 CPU	7	
PP1V05 SUS	7	
PP15V TBT	7	
PP3V3 TBTLC	7	
PP1V05 TBTLC	7 35	
PP1V05 S0 PCH VCCADPLL	7	
PPVCCORE S0 CPU	7	
PPVCCORE S0 AXG	7	
PP1V5 S3 CPU VCCDQ	7	
PP1V05 S0 CPU VCCPOE	7	
PP1V8 S0 CPU VCCPLL R	7	
PP1V05 TBTCTIO	7	
PPBUS S5 HS OTHER ISNS	7	
PPDCIN G3H ISOL	7	
PP5V S3	7	
PP5V S0	7	
PP3V3 S4	7	

(Need to add 27 GND TPs)

FUNC_TEST	TP	NC
NC EDP TXP<0..3>		TP EDP TX P<0..3>
MAKE_BASE=TRUE		
NC EDP TXN<0..3>		TP EDP TX N<0..3>
MAKE_BASE=TRUE		
NC EDP AUXP		TP EDP AUX P
MAKE_BASE=TRUE		
NC EDP AUXN		TP EDP AUX N
MAKE_BASE=TRUE		
NC CPU THERMDA		TP CPU THERMDA
MAKE_BASE=TRUE		
NC CPU THERMDC		TP CPU THERMDC
MAKE_BASE=TRUE		
NC CPU RSVD<30..45>		TP CPU RSVD<30..45>
MAKE_BASE=TRUE		
NC CPU RSVD<8..27>		TP CPU RSVD<8..27>
MAKE_BASE=TRUE		

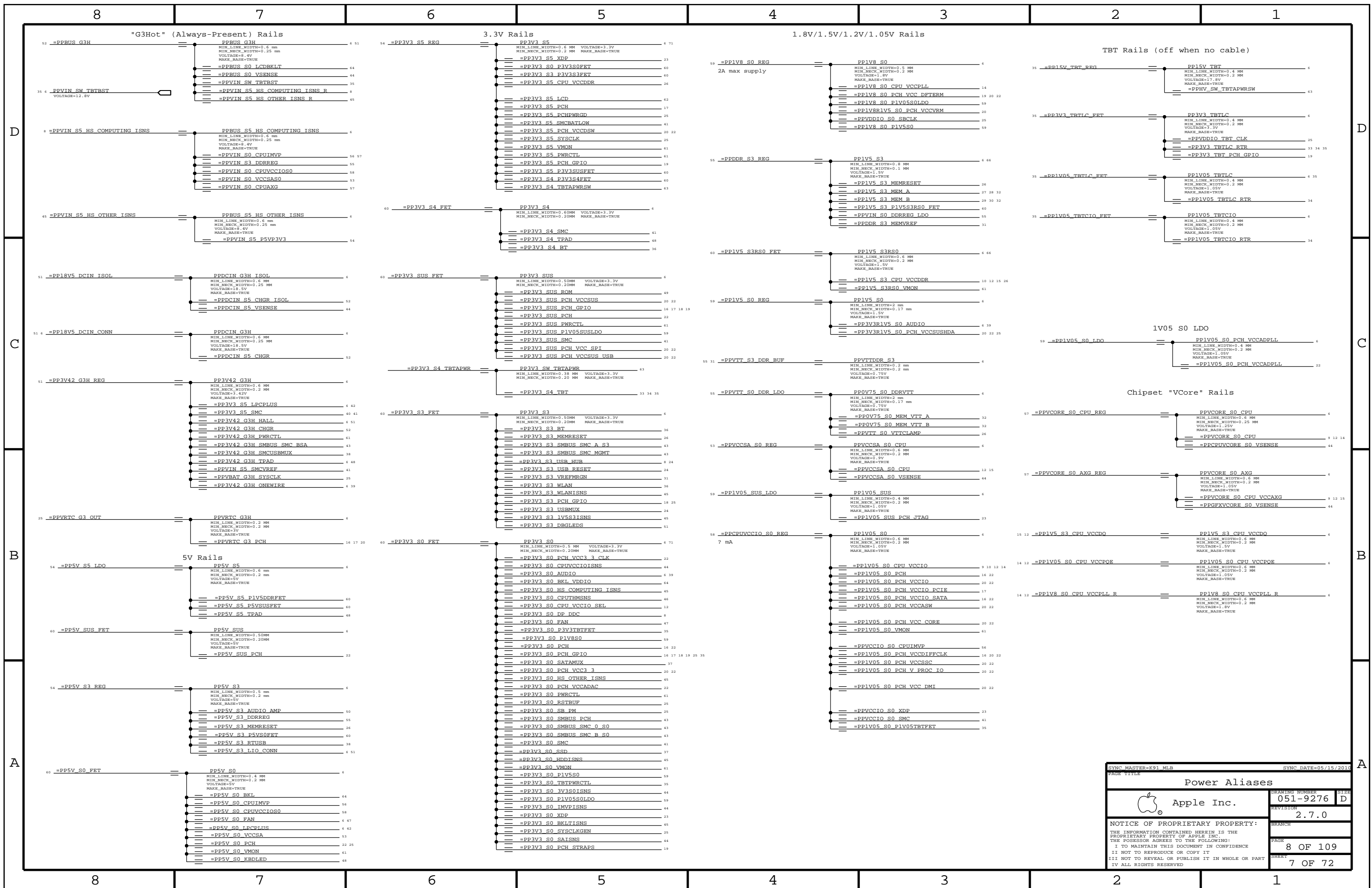
TP	FUNC_TEST	NC
TP PCIE CLK100M PE4N		NC PCIE CLK100M PE4N
TP PCIE CLK100M PE4P		NC PCIE CLK100M PE4P
TP PCIE CLK100M PE4N		NC PCIE CLK100M PE4N
TP PCIE CLK100M PE4P		NC PCIE CLK100M PE4P
TP PCIE CLK100M PE5N		NC PCIE CLK100M PE5N
TP PCIE CLK100M PE5P		NC PCIE CLK100M PE5P
TP PCIE CLK100M PE6N		NC PCIE CLK100M PE6N
TP PCIE CLK100M PE6P		NC PCIE CLK100M PE6P
TP PCIE CLK100M PE7N		NC PCIE CLK100M PE7N
TP PCIE CLK100M PE7P		NC PCIE CLK100M PE7P
TP EBI0C P1 3		NC EBI0C P1 3
TP SATA B D2RN		NC SATA B D2RN
TP SATA B D2RP		NC SATA B D2RP
TP SATA B R2D CN		NC SATA B R2D CN
TP SATA B R2D CP		NC SATA B R2D CP
TP SATA D D2RN		NC SATA D D2RN
TP SATA D D2RP		NC SATA D D2RP
TP SATA D R2D CN		NC SATA D R2D CN
TP SATA D R2D CP		NC SATA D R2D CP
TP SATA E D2RN		NC SATA E D2RN
TP SATA E D2RP		NC SATA E D2RP
TP SATA E R2D CN		NC SATA E R2D CN
TP SATA E R2D CP		NC SATA E R2D CP
TP SATA F D2RN		NC SATA F D2RN
TP SATA F D2RP		NC SATA F D2RP
TP SATA F R2D CN		NC SATA F R2D CN
TP SATA F R2D CP		NC SATA F R2D CP

NO_TEST Nets

NO_TEST	TP	NC
VCCS0A0_SREF	53	
VCCS0A0_SET1_B	53	
VCCS0A0_SET0	53	
VCCS0A0_SET1	53	
NC_CRT_IG_BLUE		TP CRT_IG_BLUE
NC_CRT_IG_GREEN		TP CRT_IG_GREEN
NC_CRT_IG_RED		TP CRT_IG_RED
NC_CRT_IG_DDC_CLK		TP CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA		TP CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC		TP CRT_IG_HSYNC
NC_CRT_IG_VSYNC		TP CRT_IG_VSYNC
NC_LVDS_IG_CTRL_CLK		TP LVDS_IG_CTRL_CLK
NC_LVDS_IG_CTRL_DATA		TP LVDS_IG_CTRL_DATA
NC_PCH_LVDS_VBI		TP PCH_LVDS_VBI
NC_HDA_SDI0		TP HDA_SDI0
NC_HDA_SDI2		TP HDA_SDI2
NC_HDA_SDI3		TP HDA_SDI3
NC_PCI_PME_L		TP PCI_PME_L
NC_PCI_CLK33M_OUT3		TP PCI_CLK33M_OUT3
NC_CLINK_CLK		TP CLINK_CLK
NC_CLINK_DATA		TP CLINK_DATA
NC_CLINK_RESET_L		TP CLINK_RESET_L
NC_PCH_CLK100M_PERN		TP PCIE_CLK100M_PERN
NC_PCH_CLK100M_PERP		TP PCIE_CLK100M_PERP
NC_SVDO_TVCLKIN		TP SVDO_TVCLKIN
NC_SVDO_TVCLKIND		TP SVDO_TVCLKIND
NC_SVDO_STALIN		TP SVDO_STALIN
NC_SVDO_STALIP		TP SVDO_STALIP
NC_SVDO_INTN		TP SVDO_INTN
NC_SVDO_INTP		TP SVDO_INTP
NC_TP_XDP_PCH_OBSPN_A<0..1>		TP XDP_PCH_OBSPN_A<0..1>
NC_TP_XDP_PCH_OBSPN_B<0..1>		TP XDP_PCH_OBSPN_B<0..1>
NC_TP_XDP_PCH_HOOK2		TP XDP_PCH_HOOK2
NC_TP_XDP_PCH_HOOK3		TP XDP_PCH_HOOK3
NC_TP_XDP_PCH_OBSPN_D<0..1>		TP XDP_PCH_OBSPN_D<0..1>
NC_TP_XDP_PCH_HOOK4		TP XDP_PCH_HOOK4
NC_TP_XDP_PCH_HOOK5		TP XDP_PCH_HOOK5
NC_PCH_GPI064_CLKOUTFLEK0		TP PCH_GPI064_CLKOUTFLEK0
NC_PCH_GPI065_CLKOUTFLEK1		TP PCH_GPI065_CLKOUTFLEK1
NC_PCH_GPI066_CLKOUTFLEK2		TP PCH_GPI066_CLKOUTFLEK2
NC_PCH_GPI067_CLKOUTFLEK3		TP PCH_GPI067_CLKOUTFLEK3

TP	FUNC_TEST	NC
TP PCH_TP18		NC_PCH_TP18
TP PCH_TP17		NC_PCH_TP17
TP PCH_TP16		NC_PCH_TP16
TP PCH_TP15		NC_PCH_TP15
TP PCH_TP14		NC_PCH_TP14
TP PCH_TP13		NC_PCH_TP13
TP PCH_TP12		NC_PCH_TP12
TP PCH_TP10		NC_PCH_TP10
TP PCH_TP9		NC_PCH_TP9
TP PCH_TP8		NC_PCH_TP8
TP PCH_TP7		NC_PCH_TP7
TP PCH_TP6		NC_PCH_TP6
TP PCH_TP5		NC_PCH_TP5
TP PCH_TP4		NC_PCH_TP4
TP PCH_TP3		NC_PCH_TP3
TP PCH_TP2		NC_PCH_TP2
TP PCH_TP1		NC_PCH_TP1
SMC_BH_ALARM_L		NC_SMC_BH_ALARM_L

SYNC MASTER=(K99 MLB) SYNC DATE=(02/16/2010)
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Functional Test / No Test
 Apple Inc.
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Power Aliases

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

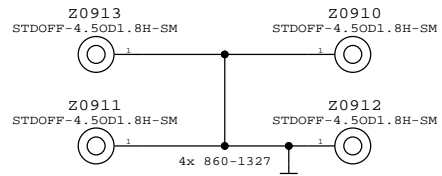
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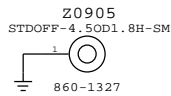
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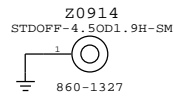
CPU Heat Sink Mounting Bosses



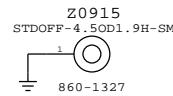
Fan Boss



X21 Boss

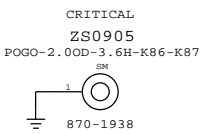


SSD Boss

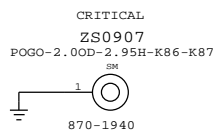


EMI I/O Pogo Pins

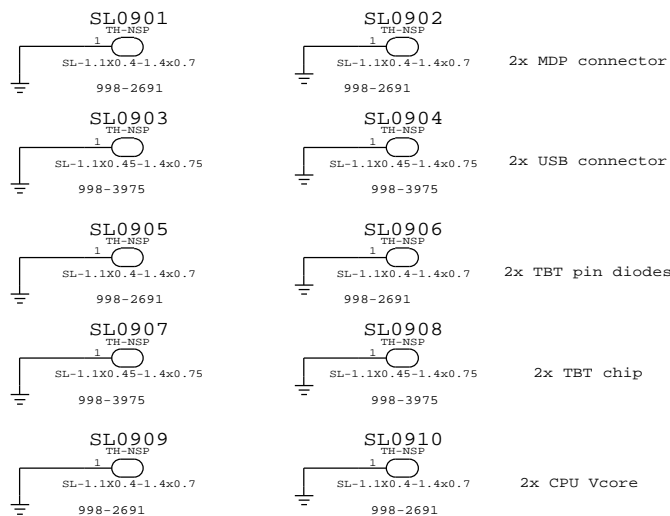
DisplayPort Pogo



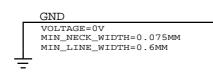
USB/SD Card Pogo



Can Slots

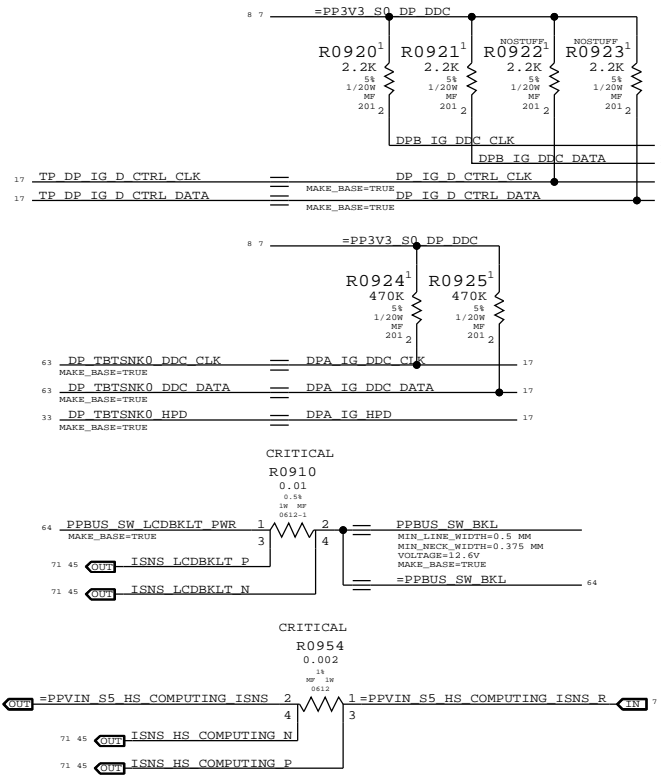


Digital Ground

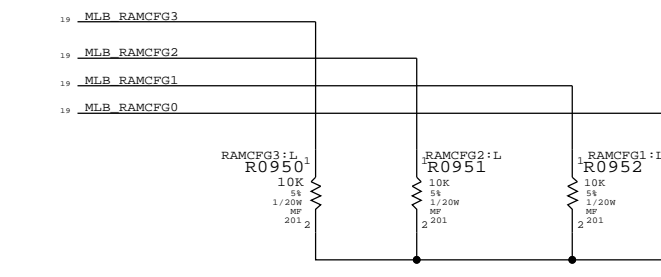
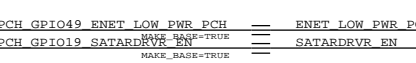
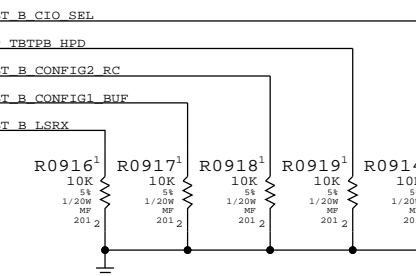
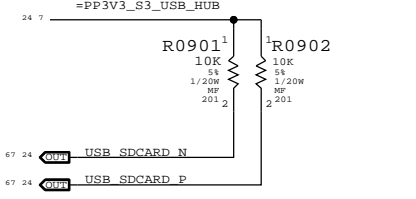


CPU signals

Table of CPU signals including MEMVTT EN, DDRVTT EN, DP TBT/SNK0 AUXCH C P, PCIE CLK100M ENET N, PEG CLK100M P, USB EXTC P, TBT B R2D C P<0>, DP TBT/PB ML C P<1>, PCIE CLK100M FW N, and PCIE FW R2D C P.



UNUSED SDCARD USB Aliases



TBT DP Ports

Table of TBT DP Ports aliases including DPB IG HPD, TP DP IG C MLN<3..0>, DPB IG AUX CH P, DPB IG AUX CH N, TP DP IG D HPD, DP TBT/PB AUXCH C P, DP TBT/PB AUXCH C N, TP DP IG B MLN<3..0>, TP DP IG B MLN<3..0>, NC PCIE 5 R2D CP, NC PCIE 6 R2D CP, NC PCIE 7 R2D CP, NC PCIE 8 R2D CP, NC PCIE 5 R2D CN, NC PCIE 6 R2D CN, NC PCIE 7 R2D CN, NC PCIE 8 R2D CN, NC PCIE 5 D2RP, NC PCIE 6 D2RP, NC PCIE 7 D2RP, NC PCIE 8 D2RP, NC PCIE 5 D2RN, NC PCIE 6 D2RN, NC PCIE 7 D2RN, NC PCIE 8 D2RN, TP LVDS IG B CLK P, TP LVDS IG B CLKN, NC LVDS IG B DATAP<0..3>, NC LVDS IG B DATAN<0..3>, NC LVDS IG A DATAP<3>, NC LVDS IG A DATAN<3>, LCD BKLT PWM, LCD IG PWR EN, LCD BKLT EN, SATA ODD R2D C P, SATA ODD R2D C N, SATA ODD D2R P, SATA ODD D2R N, SMC SYS LED, IR RX OUT RC, TP PIV5S3RS0 RAMP DONE, and TP DDRREG PGOOD.

LVDS Aliases

SATA Aliases

SMC Aliases

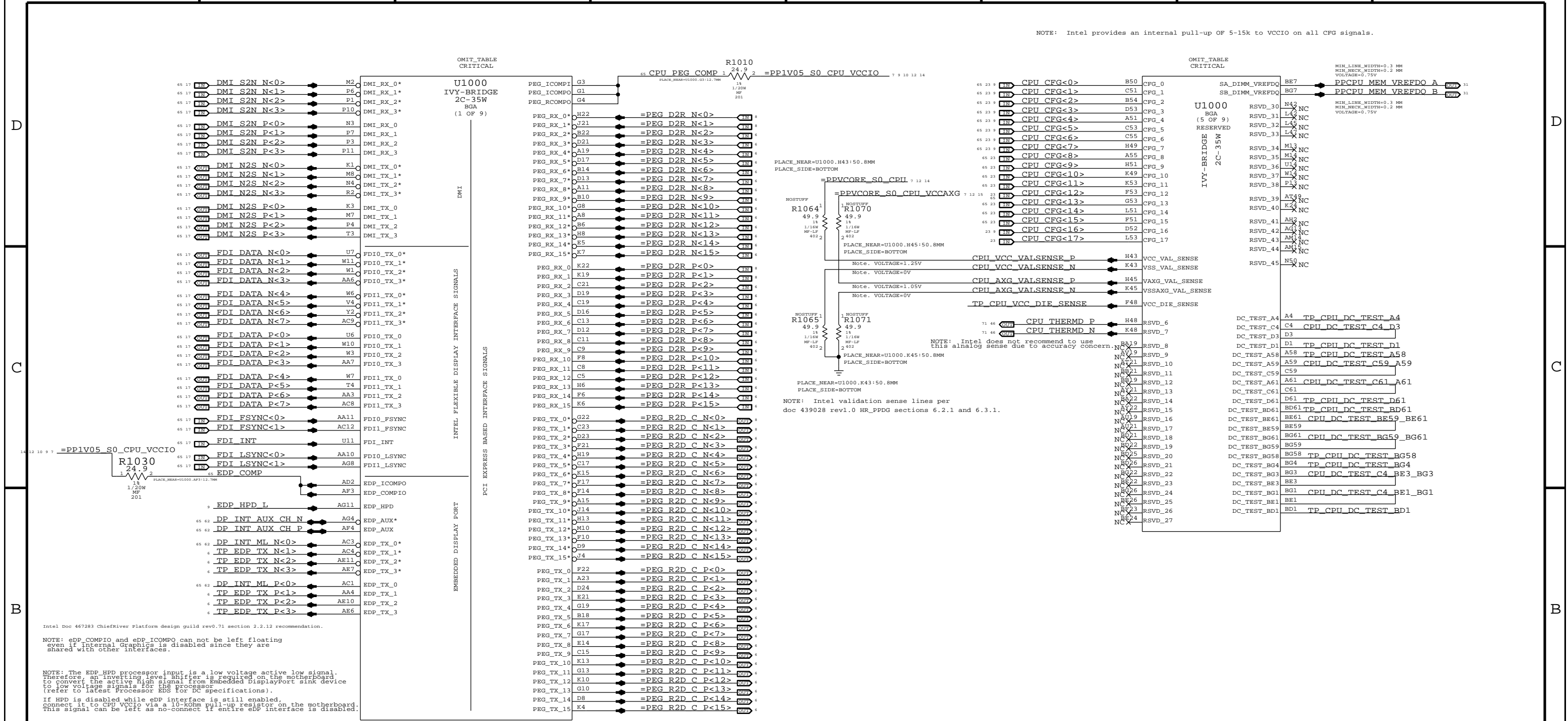
Unused PGOOD signal

Signal Aliases table with Apple Inc. logo, drawing number 051-9276, revision 2.7.0, and page 9 of 109. Includes a notice of proprietary property.

NOTE: Intel provides an internal pull-up of 5-15k to VCCIO on all CFG signals.

D
C
B
A

D
C
B
A



Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

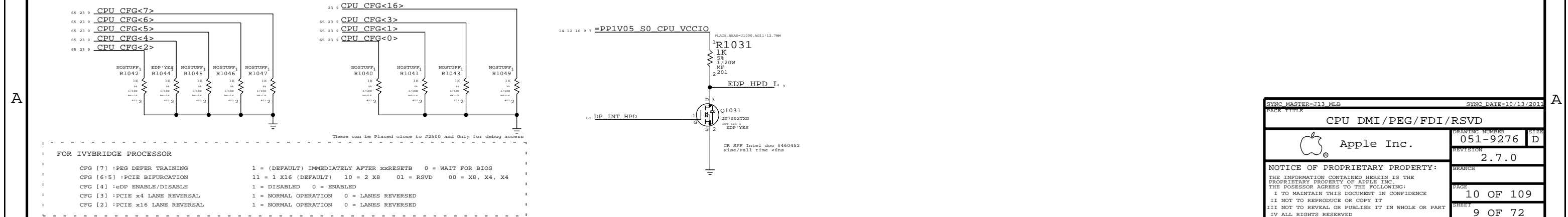
NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor. (refer to latest Processor for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

A

A



FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

SYNC MASTER=113 M.L.B. SYNC DATE=10/13/2011

CPU DMI / PEG / FDI / RSVD

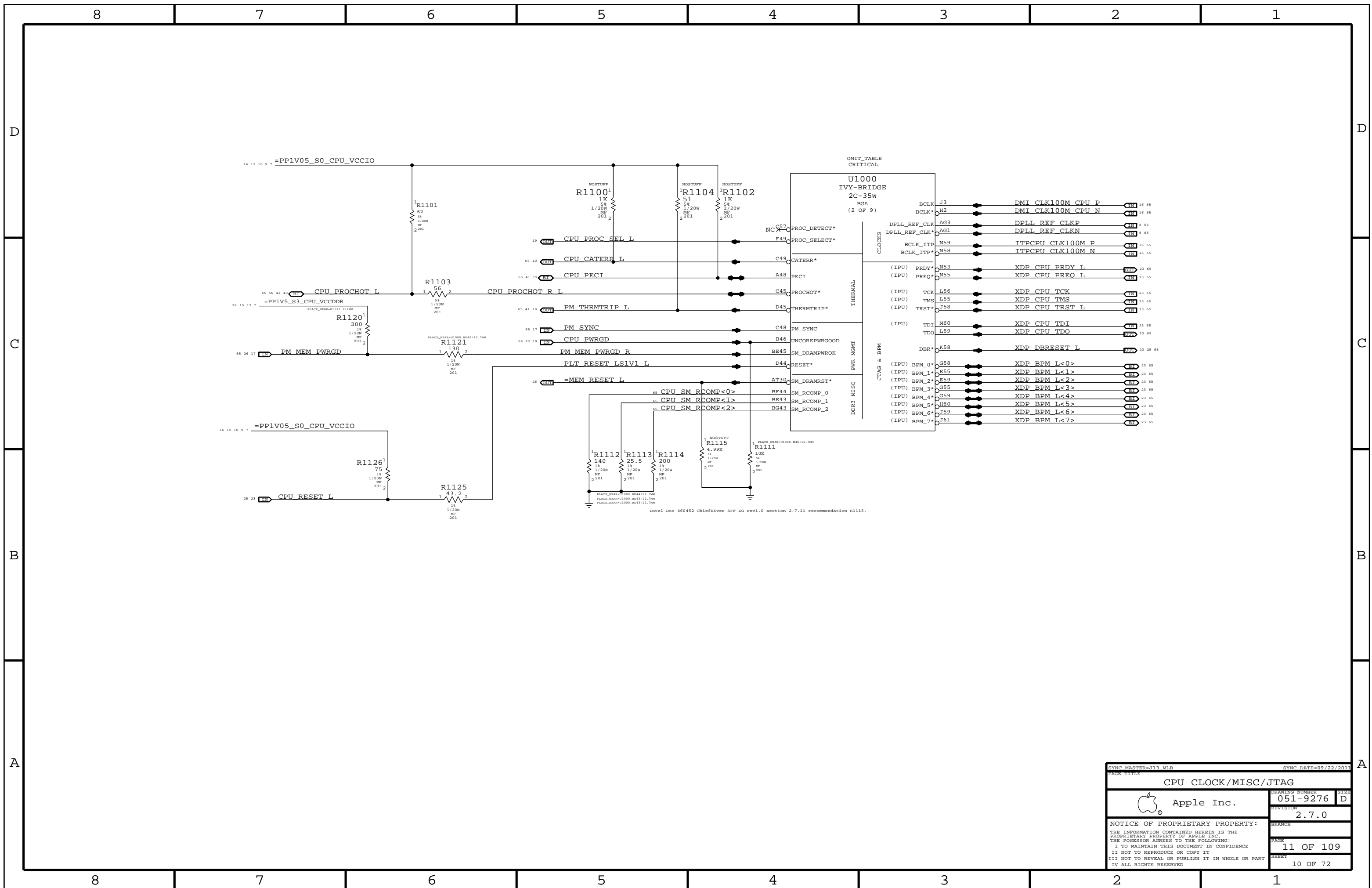
Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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PAGE: 10 OF 109 SHEET: 9 OF 72

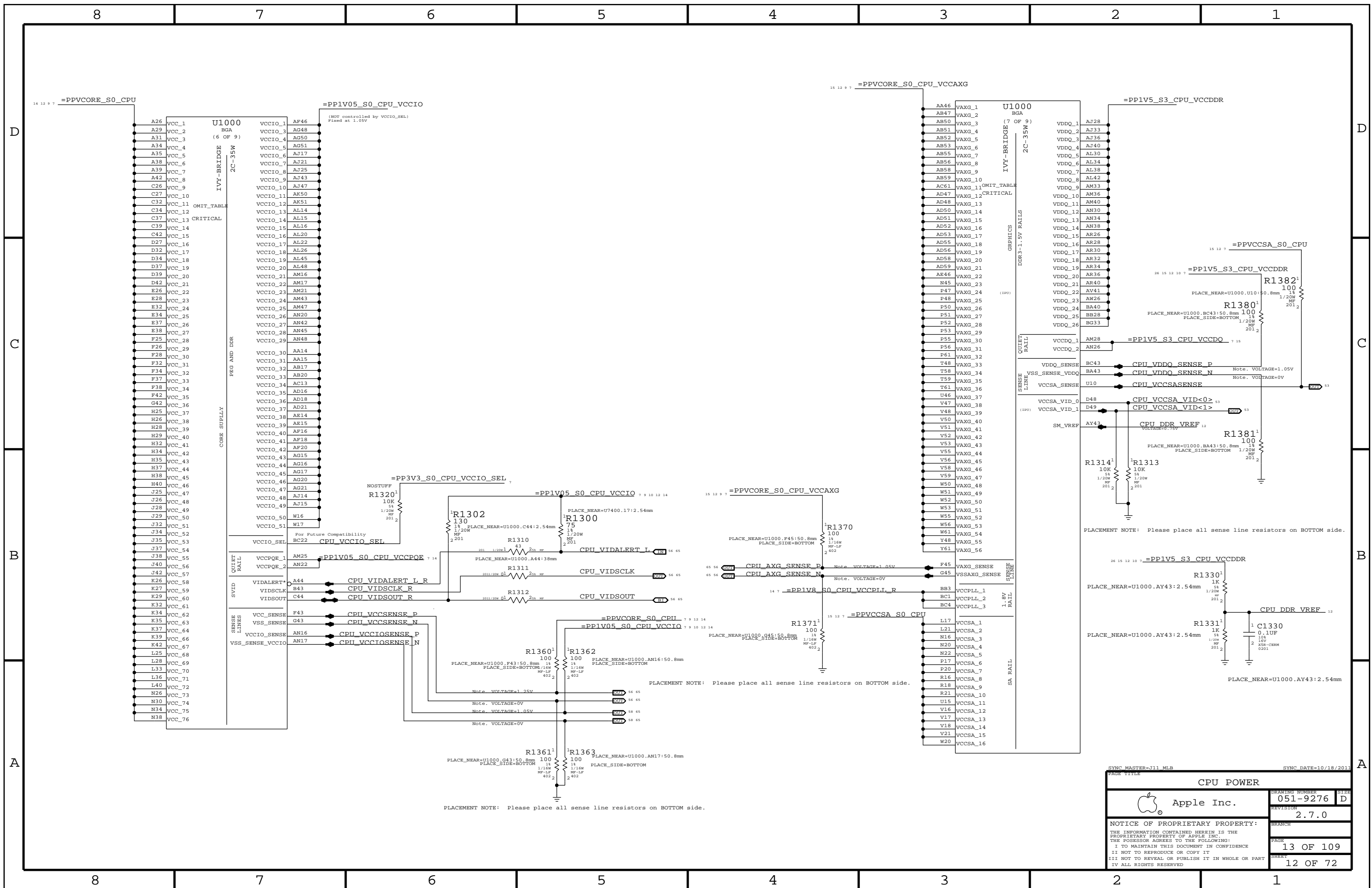


SYNC MASTER=J13 MLB		SYNC DATE=09/22/2011	
PAGE TITLE CPU CLOCK/MISC/JTAG			
DRAWING NUMBER 051-9276		SIZE D	
REVISION 2.7.0		BRANCH	
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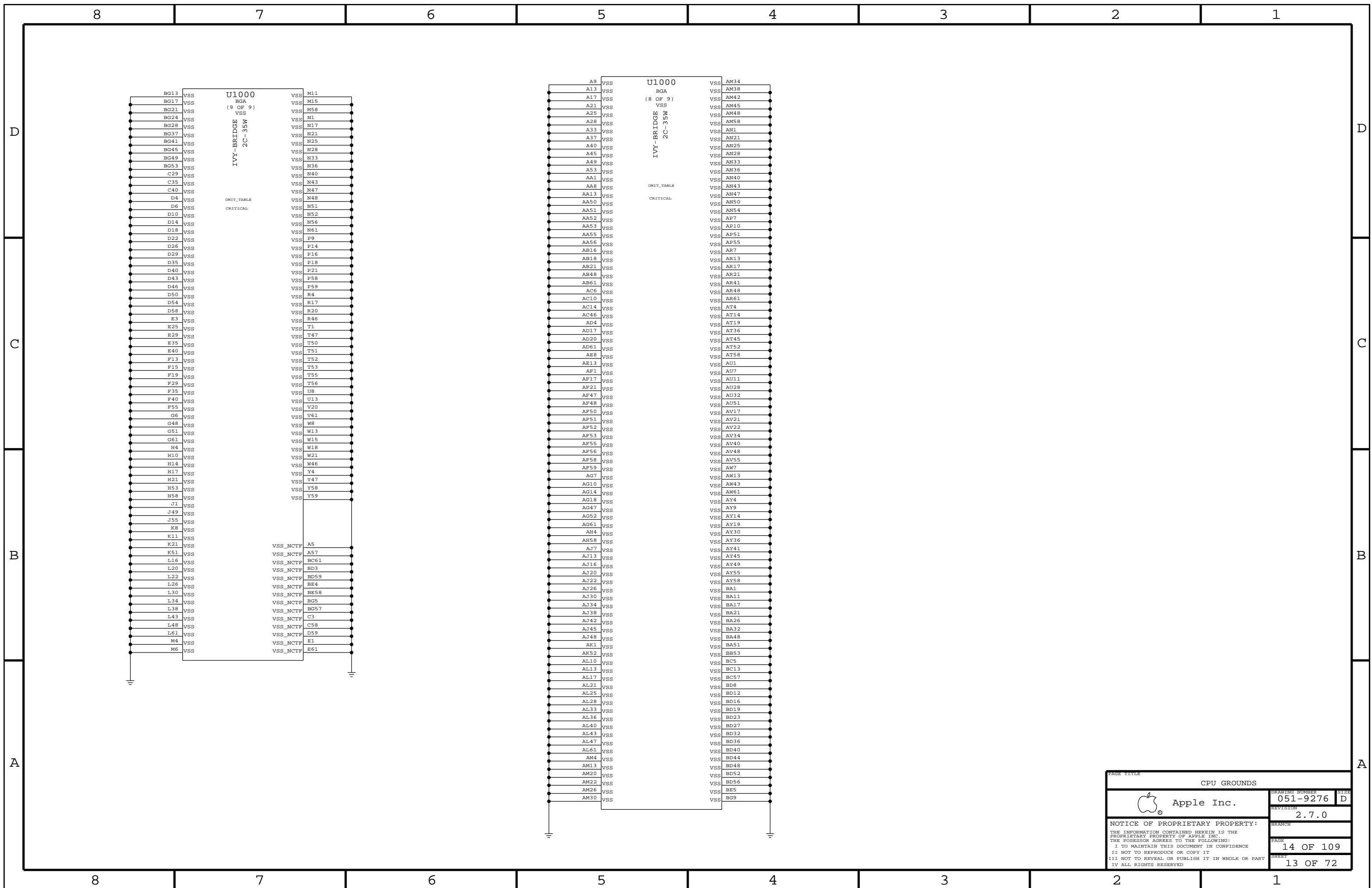


SYNC DATE=12/13/2016

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CPU POWER			DRAWING NUMBER	051-9276	SIZE
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			PAGE	13 OF 109	
			SHEET	12 OF 72	



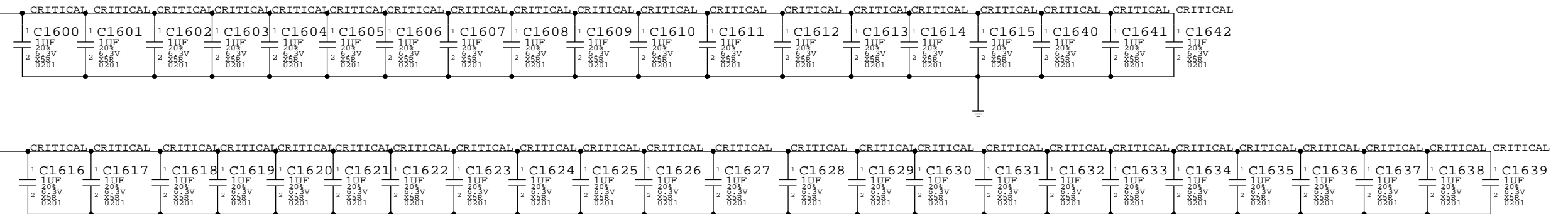
PAGE TITLE		CPU GROUNDS	
	DRAWING NUMBER	051-9276	SIZE
	REVISION	2.7.0	D
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		PAGE	14 OF 109
		SHEET	13 OF 72

Processor Load Line : -2.9 mOhms

CPU VCORE DECOUPLING

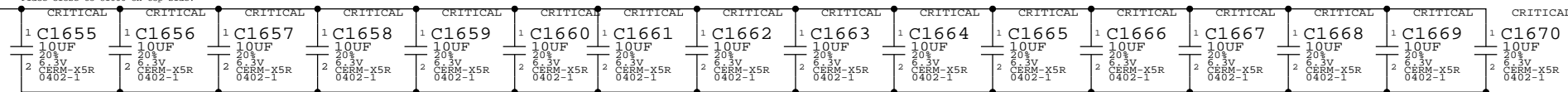
Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU



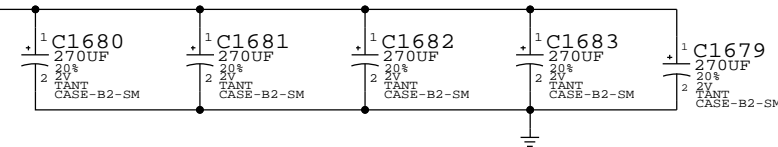
PLACEMENT_NOTE (C1655-C1666):

Place close to U1000 on top side.



PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):



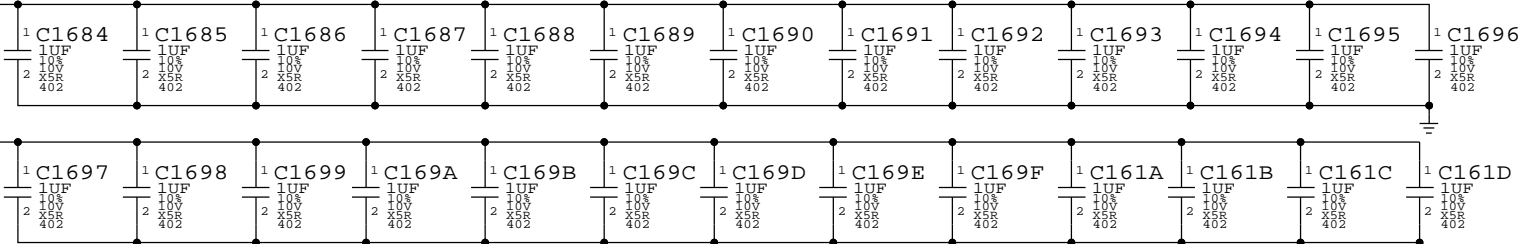
CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C1679):

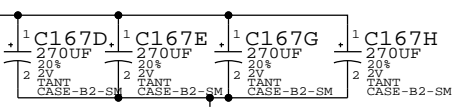
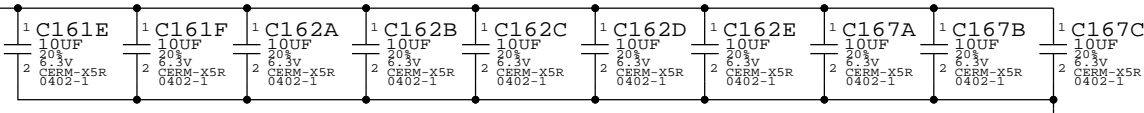
Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

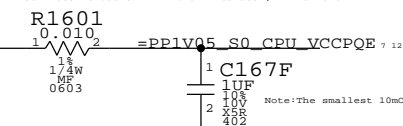


PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF



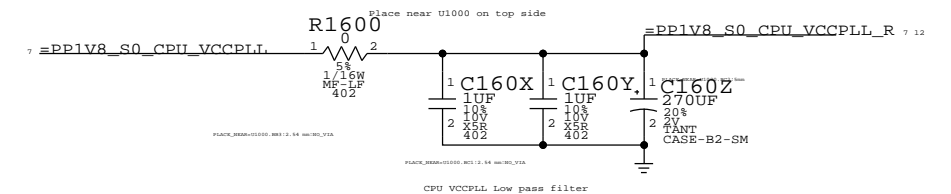
Note: The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side



CPU VCCPLL Low pass filter

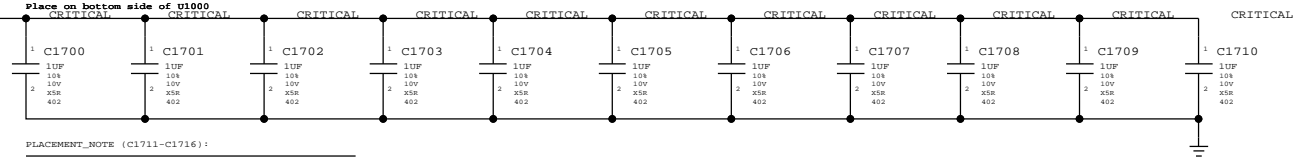
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VAXG DECOUPLING

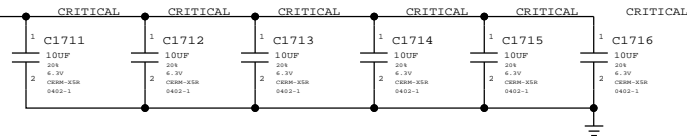
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no-stuff), 4x 470uF(2 no-stuff)

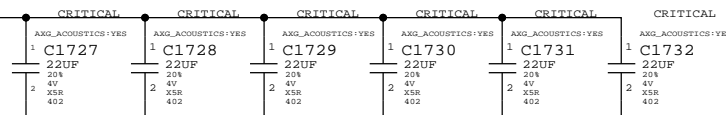
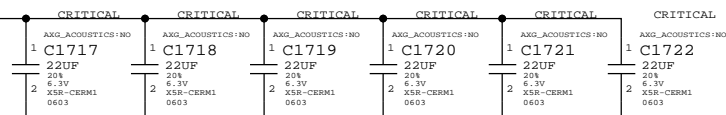
PLACEMENT_NOTE (C1700-C1710):



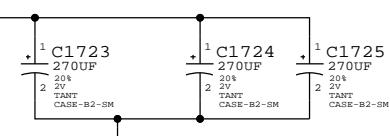
PLACEMENT_NOTE (C1711-C1716):



PLACEMENT_NOTE (C1717-C1722):



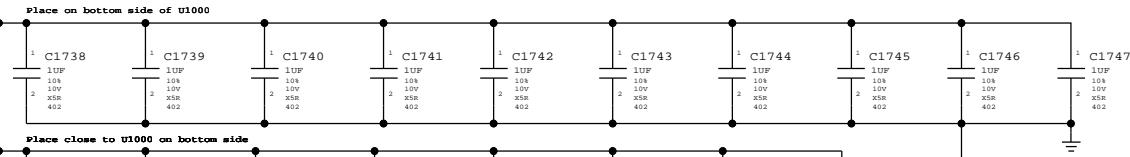
PLACEMENT_NOTE (C1723-C1724):



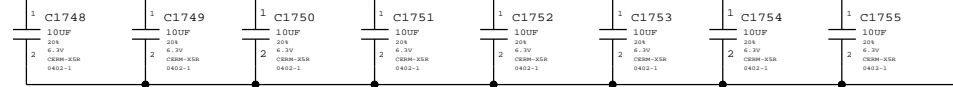
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

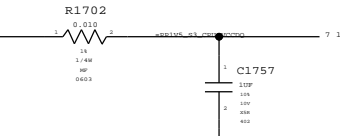
PLACEMENT_NOTE (C1738-C1747):



Place close to U1000 on bottom side



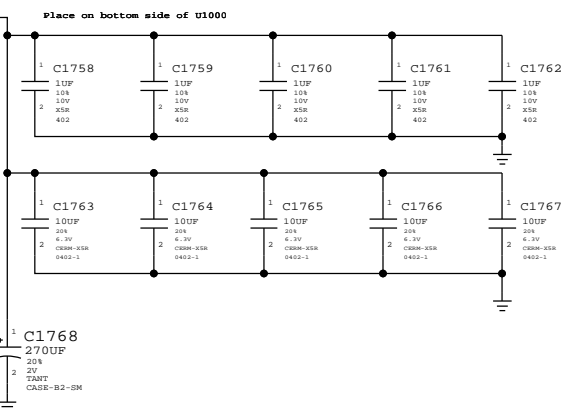
Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



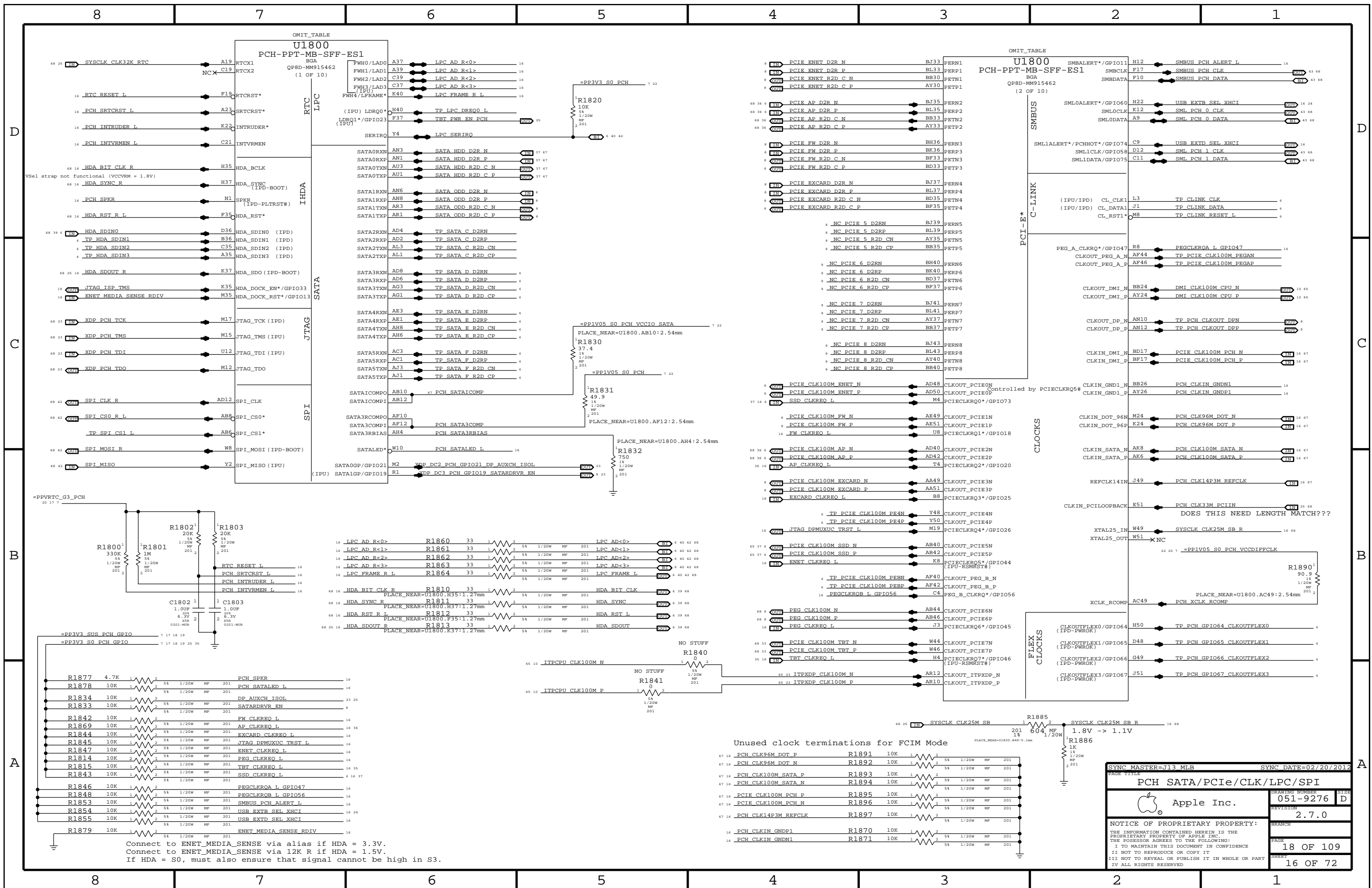
CPU VCCSA DECOUPLING

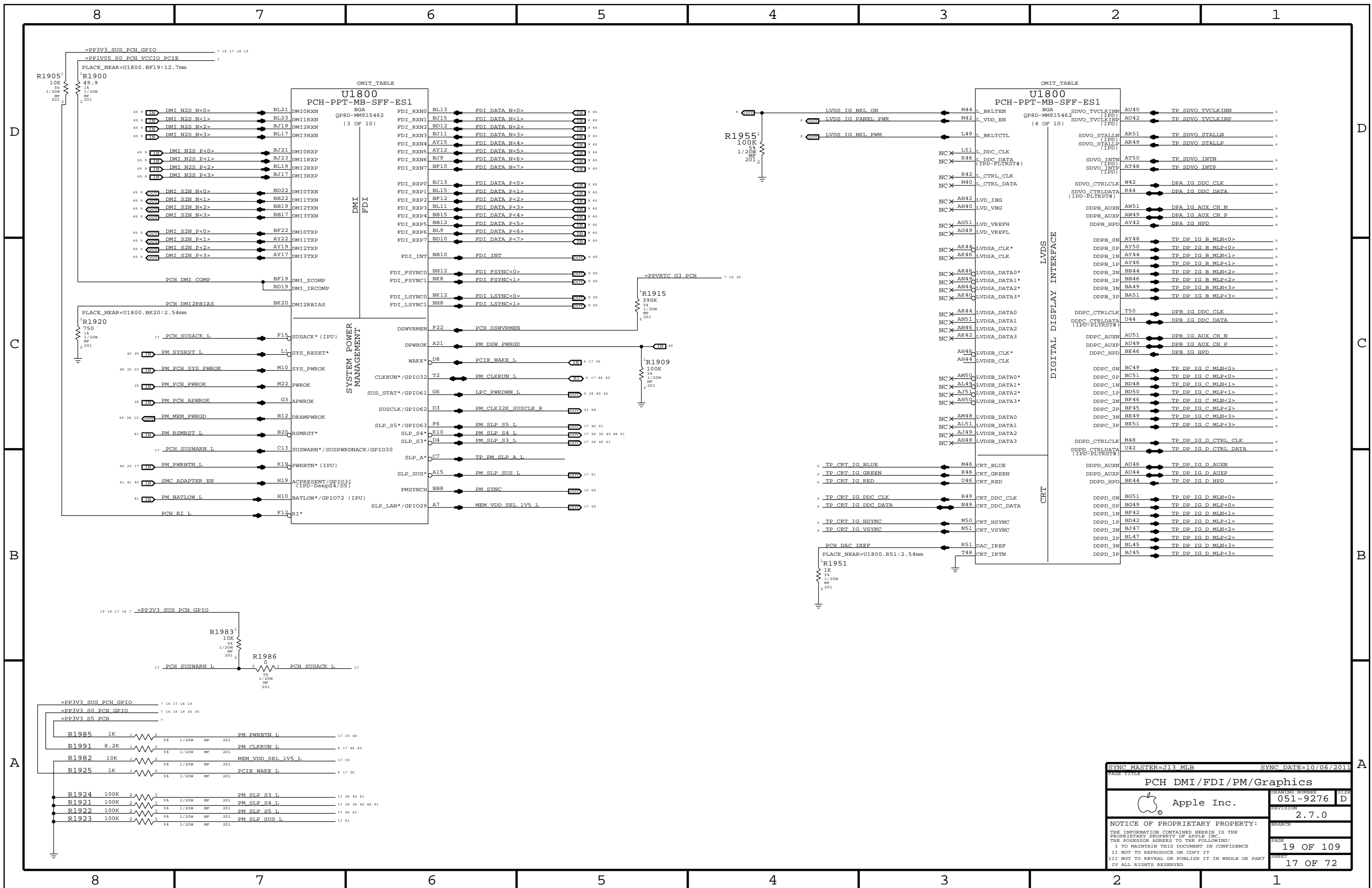
Intel recommendation (Section 6.6): 3x 1uF, 3x 10uF, 1x 330uF

PLACEMENT_NOTE (C1758-C1762):

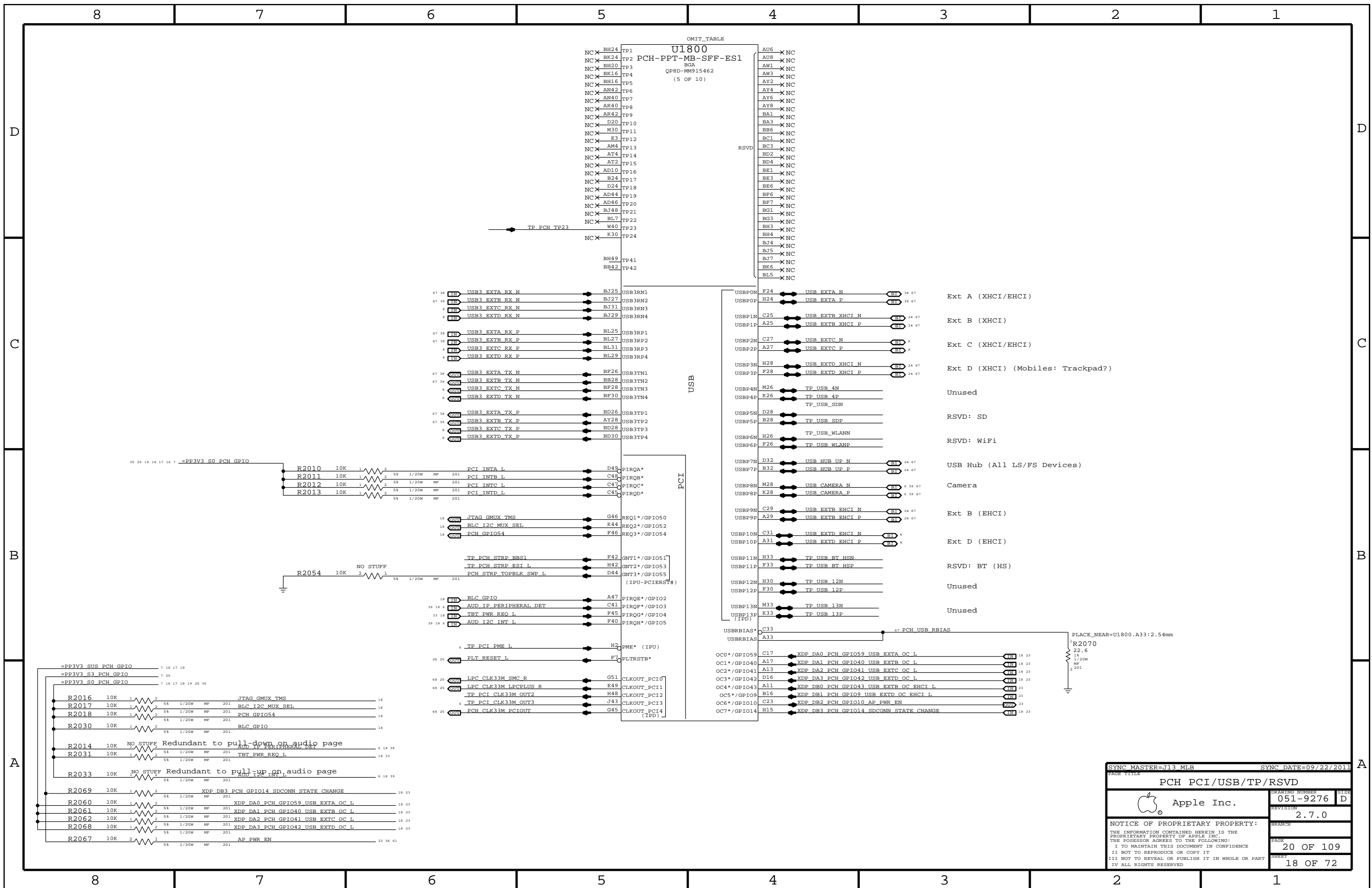


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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(5 OF 10)

NCX BH24	TP1	AU6	XNC
NCX BK24	TP2	AU8	XNC
NCX BH20	TP3	AW1	XNC
NCX BK16	TP4	AW3	XNC
NCX BH16	TP5	AY2	XNC
NCX AN42	TP6	AY4	XNC
NCX AN40	TP7	AY6	XNC
NCX AR40	TP8	AY8	XNC
NCX AR42	TP9	BA1	XNC
NCX D20	TP10	BA3	XNC
NCX M30	TP11	BB6	XNC
NCX E3	TP12	BC1	XNC
NCX AM4	TP13	BC3	XNC
NCX AT4	TP14	BD2	XNC
NCX AT2	TP15	BD4	XNC
NCX AD10	TP16	BE1	XNC
NCX B24	TP17	BE3	XNC
NCX D24	TP18	BE6	XNC
NCX AD44	TP19	BF6	XNC
NCX AD46	TP20	BF7	XNC
NCX BJ48	TP21	BG1	XNC
NCX BL7	TP22	BG3	XNC
W40	TP23	BH3	XNC
NCX K30	TP24	BH4	XNC
		BJ4	XNC
		BJ5	XNC
		BJ7	XNC
		BK6	XNC
		BL5	XNC

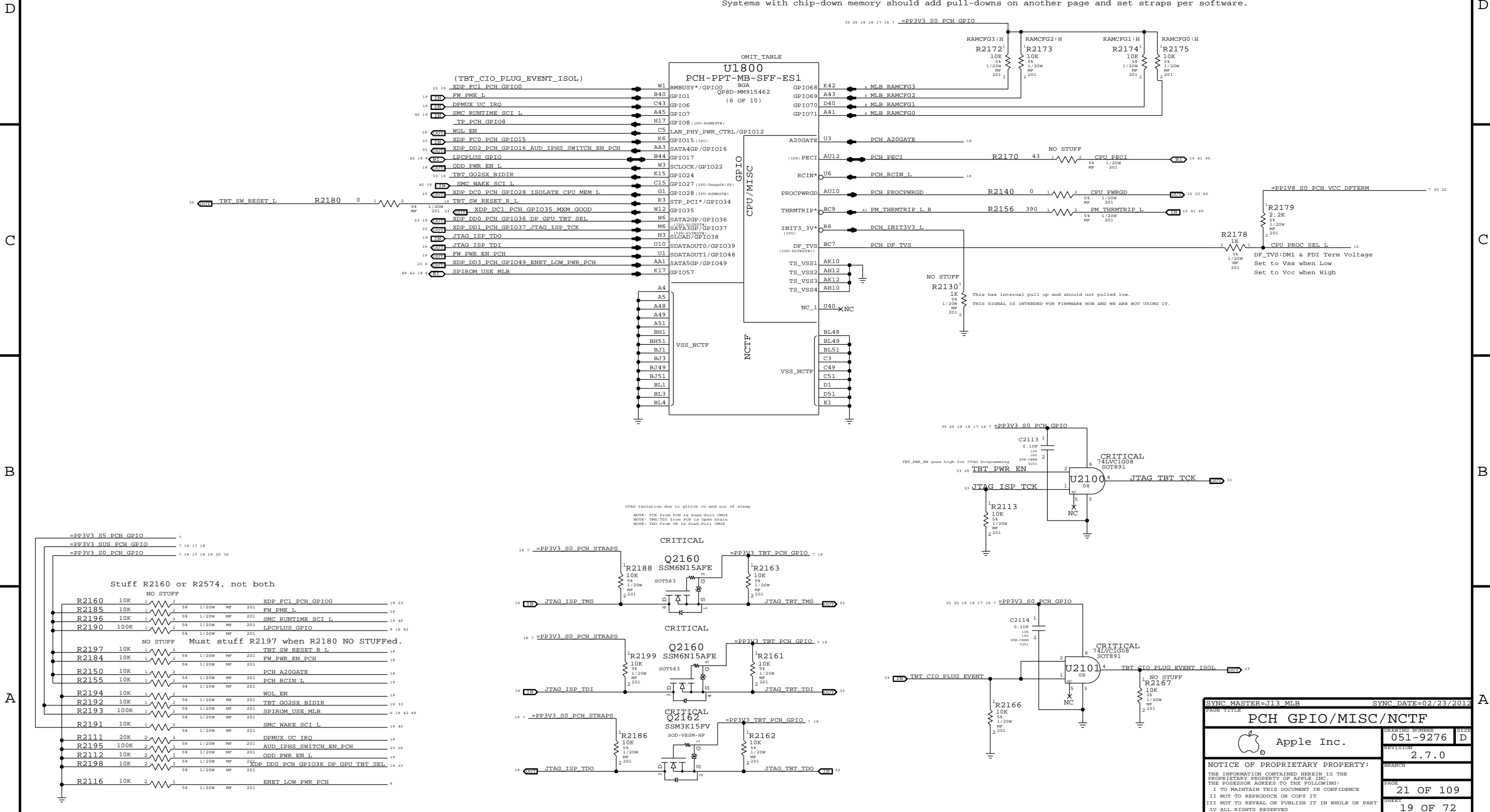
SYNC MASTER=J13 MLB SYNC DATE=09/22/2011

PCH PCI/USB/TP/RSVD

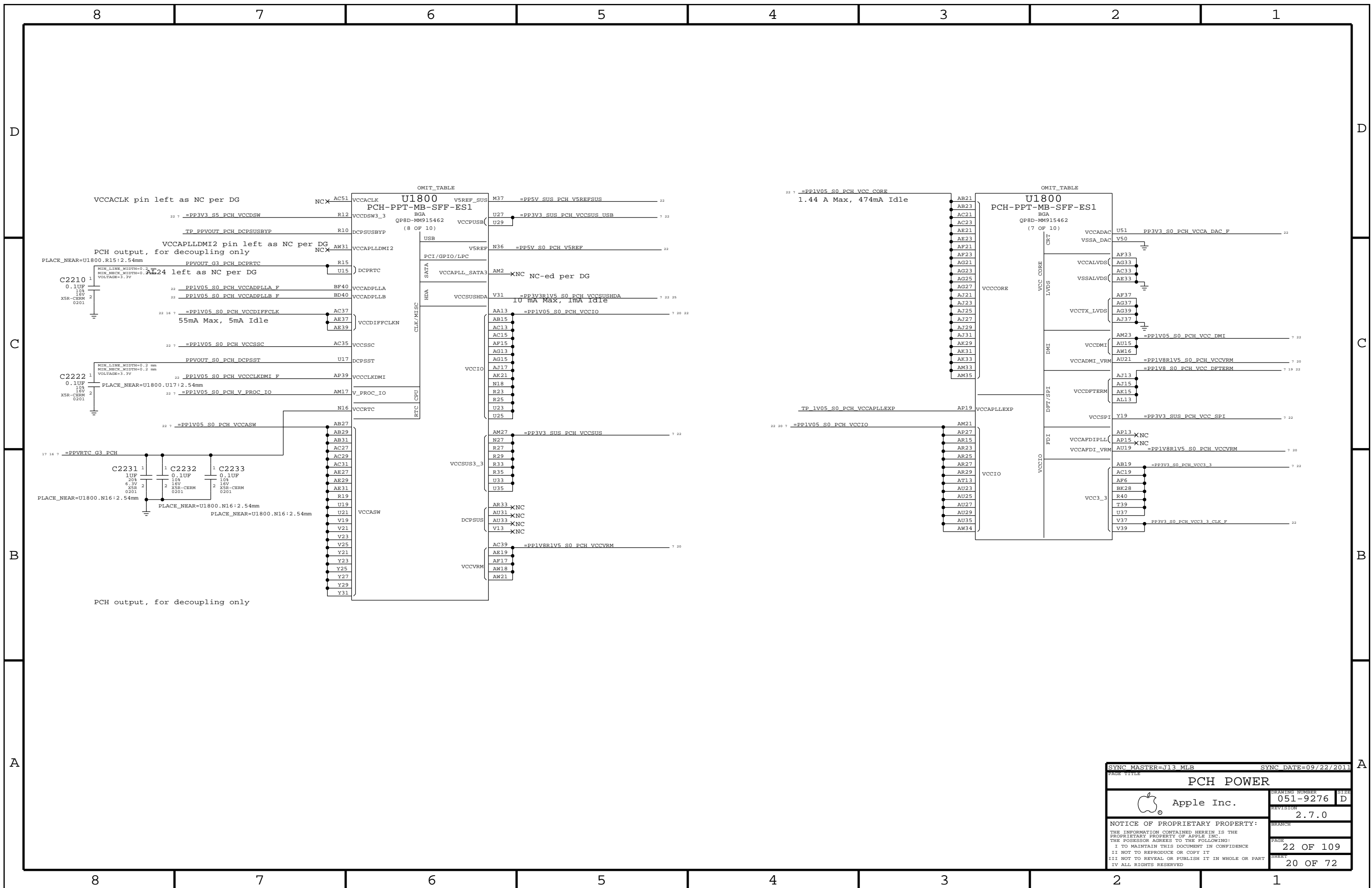
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

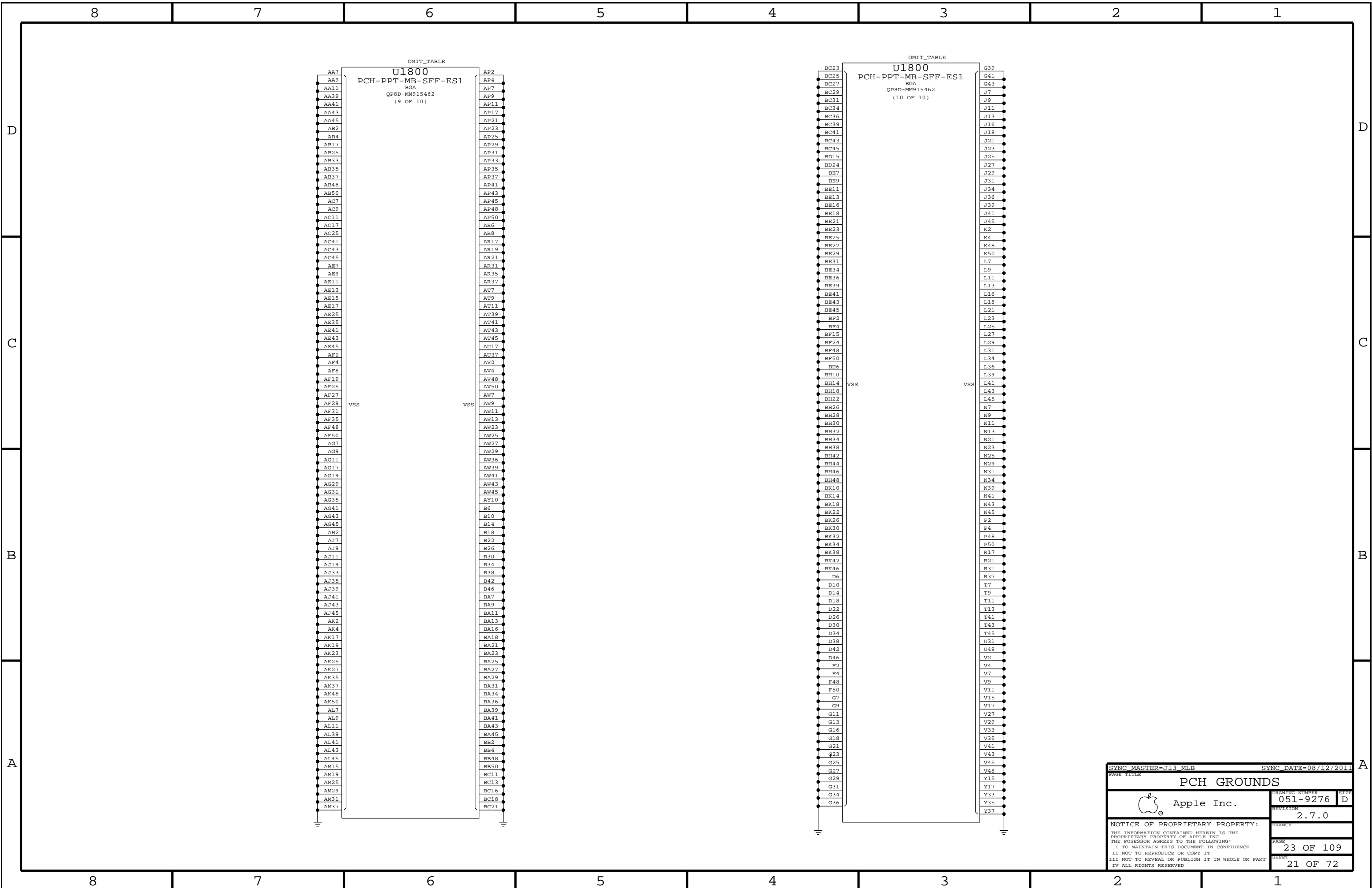
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.



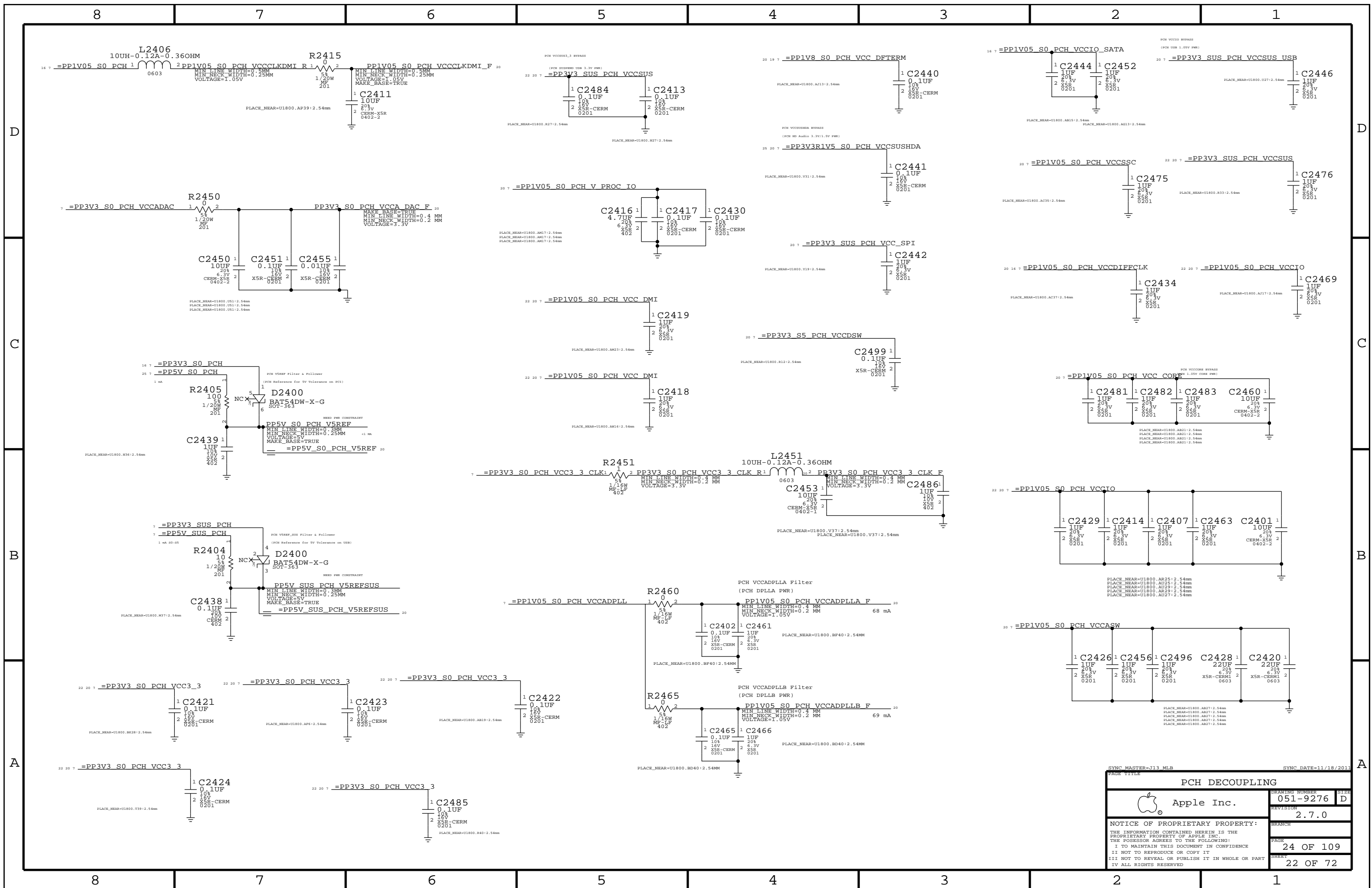
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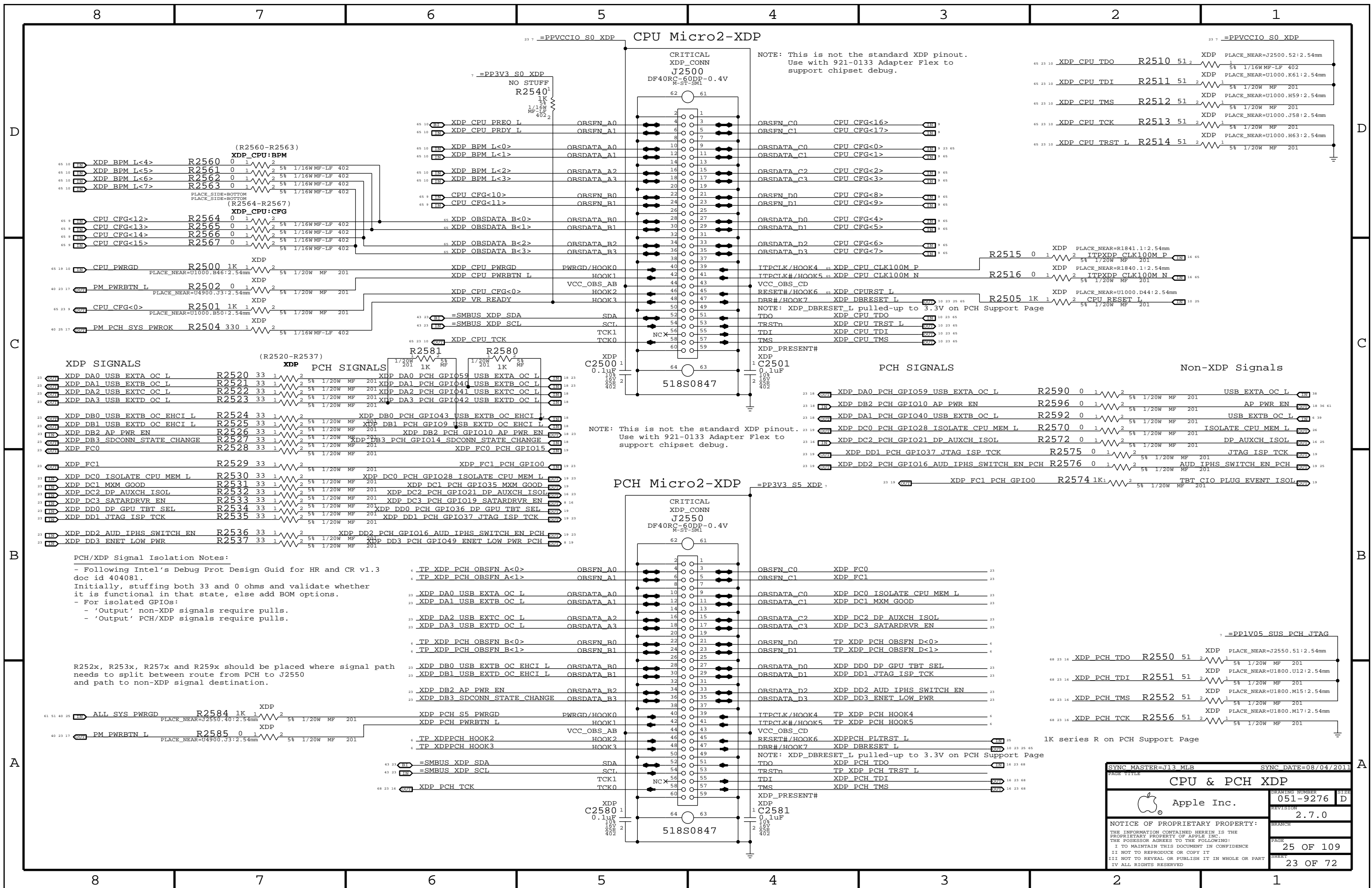
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PCH POWER			
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NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

(R2560-R2563)
XDP_CPU:BPM

XDP BPM L<4>	R2560	0	1	2	5%	1/16W	MF-LF	402
XDP BPM L<5>	R2561	0	1	2	5%	1/16W	MF-LF	402
XDP BPM L<6>	R2562	0	1	2	5%	1/16W	MF-LF	402
XDP BPM L<7>	R2563	0	1	2	5%	1/16W	MF-LF	402

PLACE_SIDE=BOTTOM
PLACE_SIDE=BOTTOM

(R2564-R2567)
XDP_CPU:CFG

CPU CFG<12>	R2564	0	1	2	5%	1/16W	MF-LF	402
CPU CFG<13>	R2565	0	1	2	5%	1/16W	MF-LF	402
CPU CFG<14>	R2566	0	1	2	5%	1/16W	MF-LF	402
CPU CFG<15>	R2567	0	1	2	5%	1/16W	MF-LF	402

XDP

CPU PWRGD	R2500	1K	1	2	5%	1/20W	MF	201
PM PWRBTN L	R2502	0	1	2	5%	1/20W	MF	201
CPU CFG<0>	R2501	1K	1	2	5%	1/20W	MF	201
PM PCH SYS PWROK	R2504	330	1	2	5%	1/16W	MF-LF	402

(R2520-R2537)
XDP PCH SIGNALS

XDP DA0 USB EXTA OC L	R2520	33	1	2	5%	1/20W	MF	201
XDP DA1 USB EXTB OC L	R2521	33	1	2	5%	1/20W	MF	201
XDP DA2 USB EXTC OC L	R2522	33	1	2	5%	1/20W	MF	201
XDP DA3 USB EXTD OC L	R2523	33	1	2	5%	1/20W	MF	201
XDP DB0 USB EXTB OC EHCI L	R2524	33	1	2	5%	1/20W	MF	201
XDP DB1 USB EXTD OC EHCI L	R2525	33	1	2	5%	1/20W	MF	201
XDP DB2 AP PWR EN	R2526	33	1	2	5%	1/20W	MF	201
XDP DB3 SDCONN STATE CHANGE	R2527	33	1	2	5%	1/20W	MF	201
XDP FC0	R2528	33	1	2	5%	1/20W	MF	201
XDP FC1	R2529	33	1	2	5%	1/20W	MF	201
XDP DC0 ISOLATE CPU MEM L	R2530	33	1	2	5%	1/20W	MF	201
XDP DC1 MXM GOOD	R2531	33	1	2	5%	1/20W	MF	201
XDP DC2 DP AUXCH ISOL	R2532	33	1	2	5%	1/20W	MF	201
XDP DC3 SATARDVR EN	R2533	33	1	2	5%	1/20W	MF	201
XDP DD0 DP GPU TBT SEL	R2534	33	1	2	5%	1/20W	MF	201
XDP DD1 JTAG ISP TCK	R2535	33	1	2	5%	1/20W	MF	201
XDP DD2 AUD IPHS SWITCH EN	R2536	33	1	2	5%	1/20W	MF	201
XDP DD3 ENET LOW PWR	R2537	33	1	2	5%	1/20W	MF	201

PCH/XDP Signal Isolation Notes:
- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
- 'Output' non-XDP signals require pulls.
- 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

XDP

ALL SYS PWRGD	R2584	1K	1	2	5%	1/20W	MF	201
PM PWRBTN L	R2585	0	1	2	5%	1/20W	MF	201

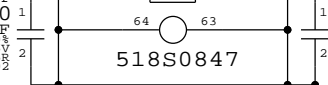
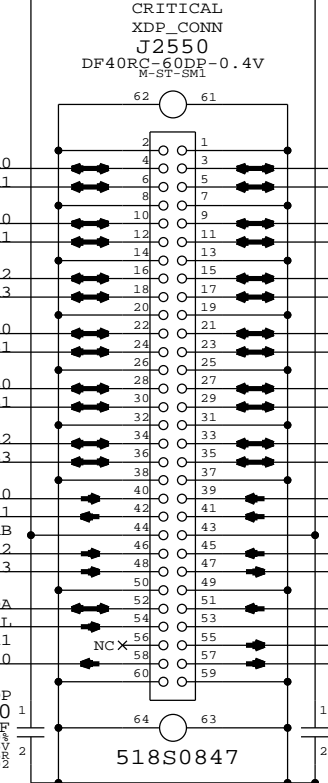
XDP

TP XDP PCH HOOK2								
TP XDP PCH HOOK3								

XDP

SMBUS XDP SDA								
SMBUS XDP SCL								
XDP PCH TCK								

PCH Micro2-XDP



(R2580-R2585)
XDP PCH SIGNALS

XDP DA0 PCH GPIO059 USB EXTA OC L	R2580	0	1	2	5%	1/20W	MF	201
XDP DA1 PCH GPIO040 USB EXTB OC L	R2581	0	1	2	5%	1/20W	MF	201
XDP DA2 PCH GPIO041 USB EXTC OC L	R2582	0	1	2	5%	1/20W	MF	201
XDP DA3 PCH GPIO042 USB EXTD OC L	R2583	0	1	2	5%	1/20W	MF	201
XDP DB0 PCH GPIO043 USB EXTB OC EHCI L	R2584	0	1	2	5%	1/20W	MF	201
XDP DB1 PCH GPIO09 USB EXTD OC EHCI L	R2585	0	1	2	5%	1/20W	MF	201
XDP DB2 PCH GPIO10 AP PWR EN								
XDP DB3 PCH GPIO14 SDCONN STATE CHANGE								
XDP FC0 PCH GPIO15								
XDP FC1 PCH GPIO0								
XDP DC0 PCH GPIO28 ISOLATE CPU MEM L								
XDP DC1 PCH GPIO35 MXM GOOD								
XDP DC2 PCH GPIO21 DP AUXCH ISOL								
XDP DC3 PCH GPIO19 SATARDVR EN								
XDP DD0 PCH GPIO36 DP GPU TBT SEL								
XDP DD1 PCH GPIO37 JTAG ISP TCK								
XDP DD2 PCH GPIO16 AUD IPHS SWITCH EN PCH								
XDP DD3 PCH GPIO49 ENET LOW PWR PCH								

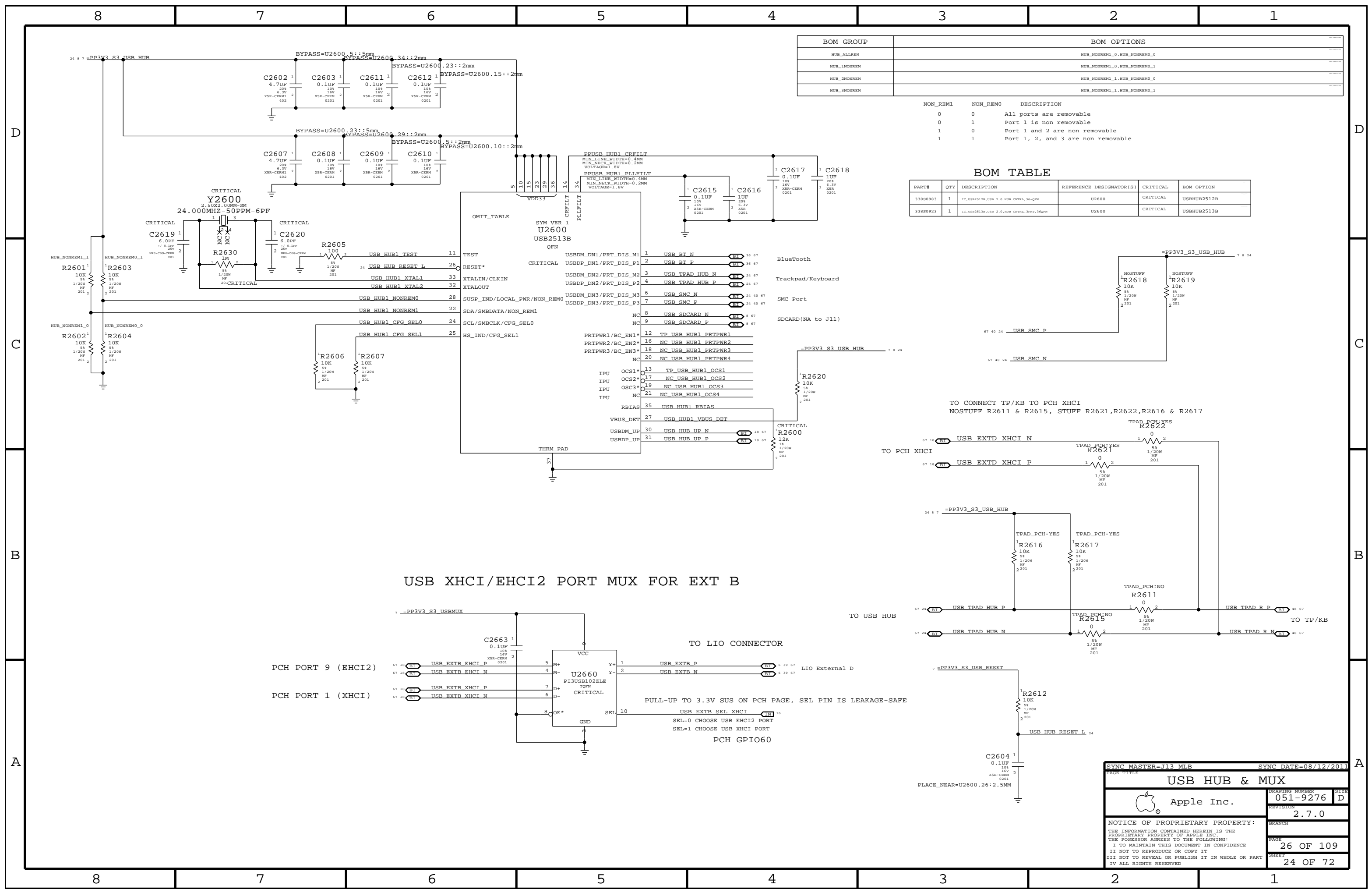
XDP

TP XDP PCH HOOK4								
TP XDP PCH HOOK5								
XDP PCH TDO								
TP XDP PCH TRST L								
XDP PCH TDI								
XDP PCH TMS								

XDP

XDP FC0								
XDP FC1								
XDP DC0 ISOLATE CPU MEM L								
XDP DC1 MXM GOOD								
XDP DC2 DP AUXCH ISOL								
XDP DC3 SATARDVR EN								
TP XDP PCH OBSFN D<0>								
TP XDP PCH OBSFN D<1>								
XDP DD0 DP GPU TBT SEL								
XDP DD1 JTAG ISP TCK								
XDP DD2 AUD IPHS SWITCH EN								
XDP DD3 ENET LOW PWR								
XDP PCH HOOK4								
XDP PCH HOOK5								
XDP PCH PLTRST L								
XDP PCH TDO								
XDP PCH TRST L								
XDP PCH TDI								
XDP PCH TMS								

PAGE TITLE		SYNC DATE=08/04/2011	
CPU & PCH XDP		DRAWING NUMBER	051-9276
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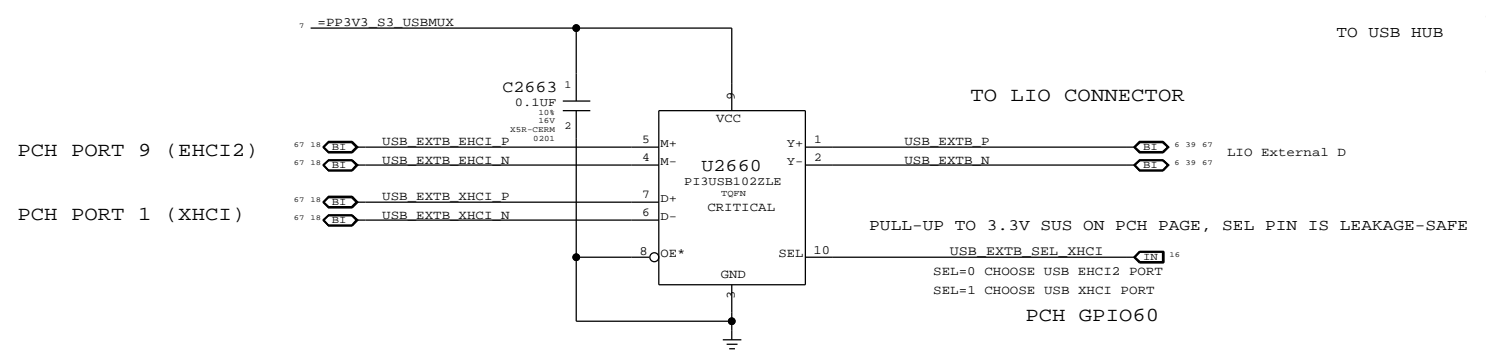
BOM GROUP		BOM OPTIONS	
HUB_ALLEEM		HUB_NONREM1_0, HUB_NONREM0_0	
HUB_1NONREM		HUB_NONREM1_0, HUB_NONREM0_1	
HUB_2NONREM		HUB_NONREM1_1, HUB_NONREM0_0	
HUB_3NONREM		HUB_NONREM1_1, HUB_NONREM0_1	

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

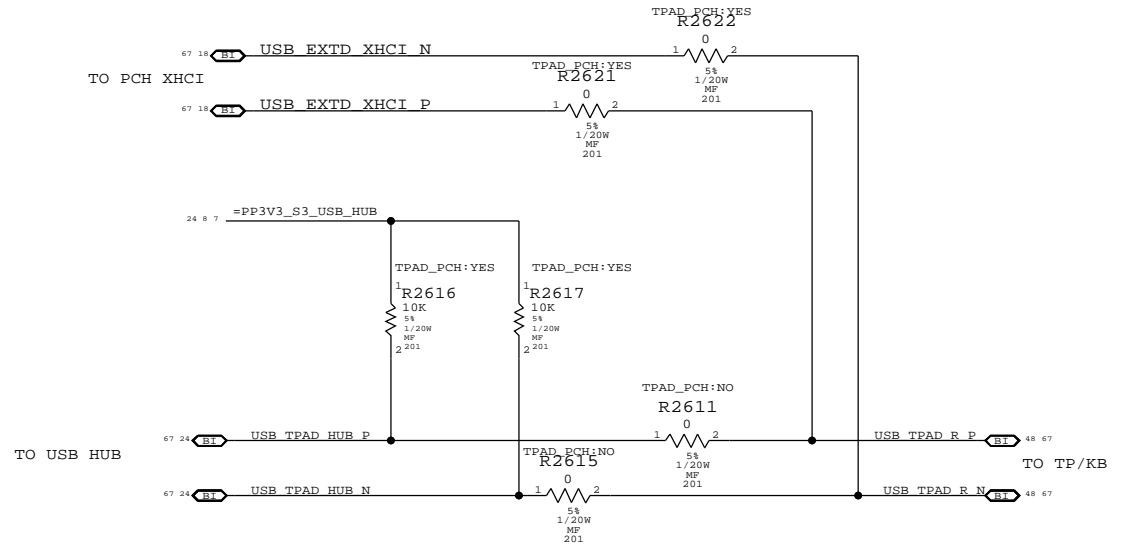
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880983	1	IC,USB2512B,USB 2.0 HUB CTRL,16-QFN	U2600	CRITICAL	USBHUB2512B
33880923	1	IC,USB2513B,USB 2.0 HUB CTRL,SPRT,34QFN	U2600	CRITICAL	USBHUB2513B

USB XHCI/EHCI2 PORT MUX FOR EXT B

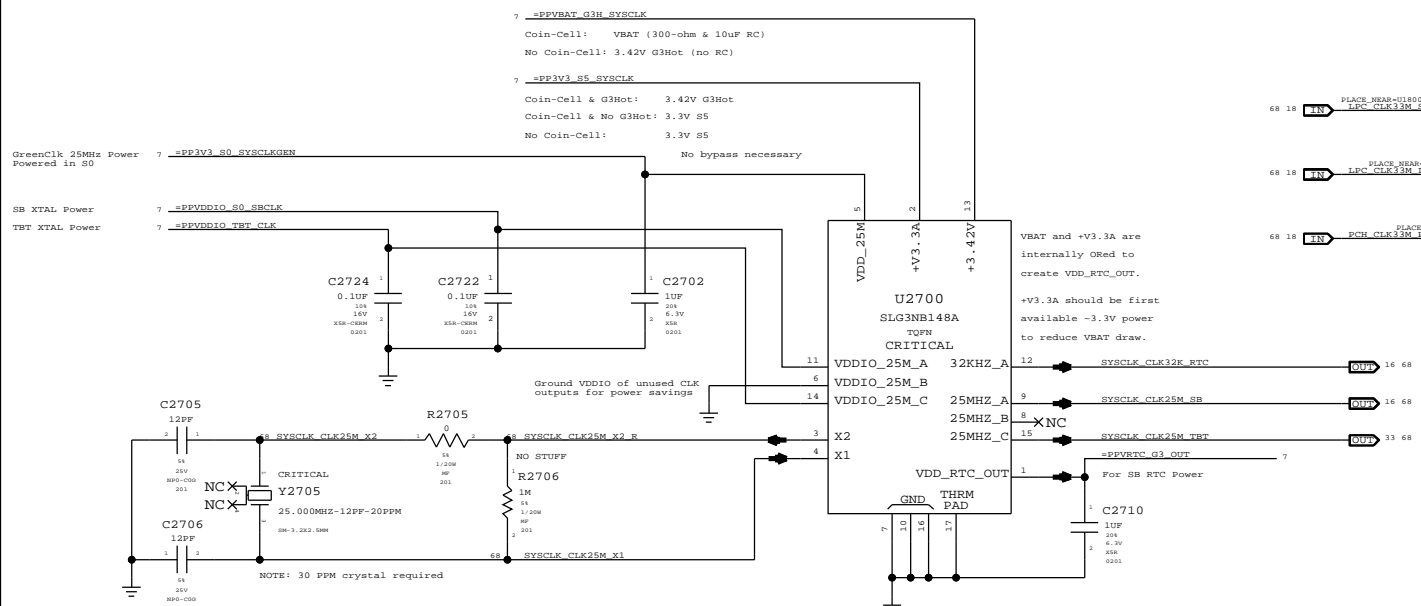


TO CONNECT TP/KB TO PCH XHCI
 NOSTUFF R2611 & R2615, STUFF R2621,R2622,R2616 & R2617

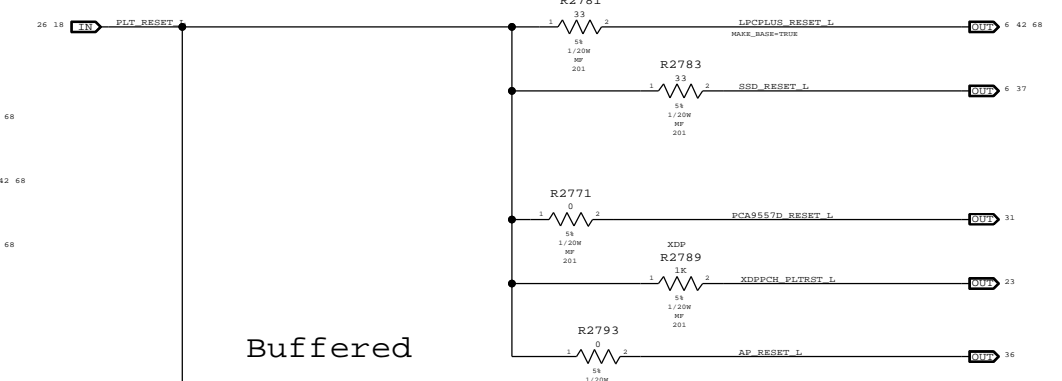


PAGE TITLE		SYNC DATE=08/12/2011	
USB HUB & MUX			
Apple Inc.	DRAWING NUMBER	051-9276	SIZE
	REVISION	2.7.0	
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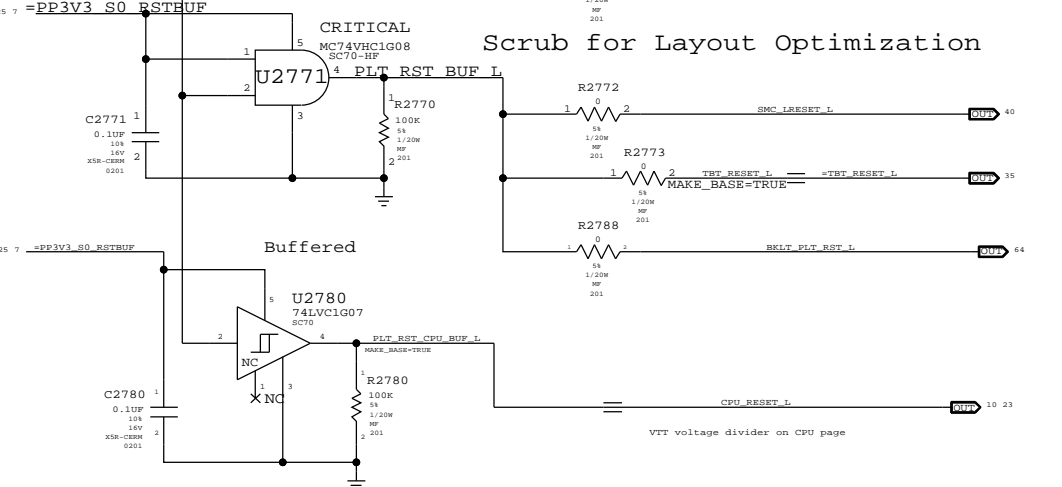
System RTC Power Source & 32kHz / 25MHz Clock Generator



Platform Reset Connections Unbuffered

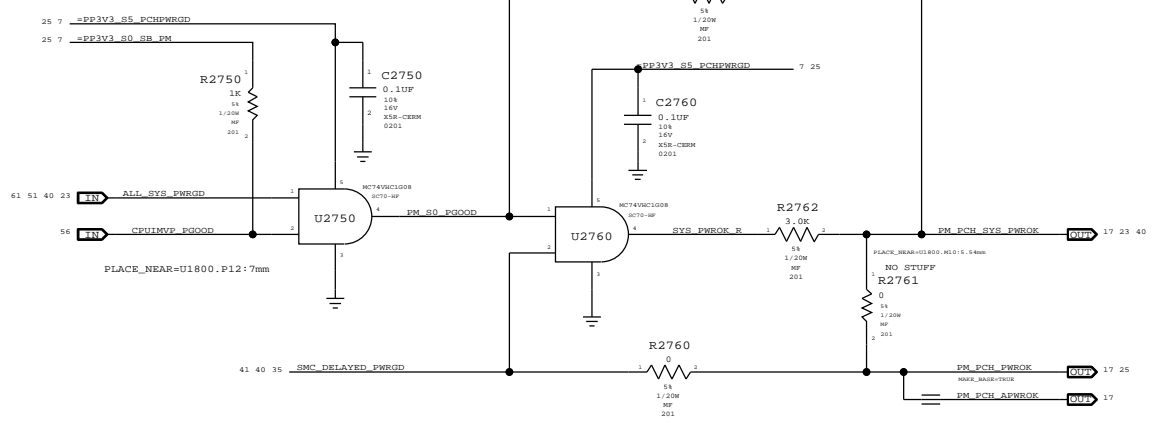


Buffered

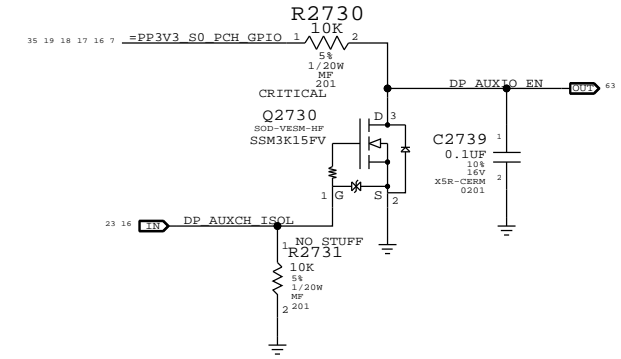


Scrub for Layout Optimization

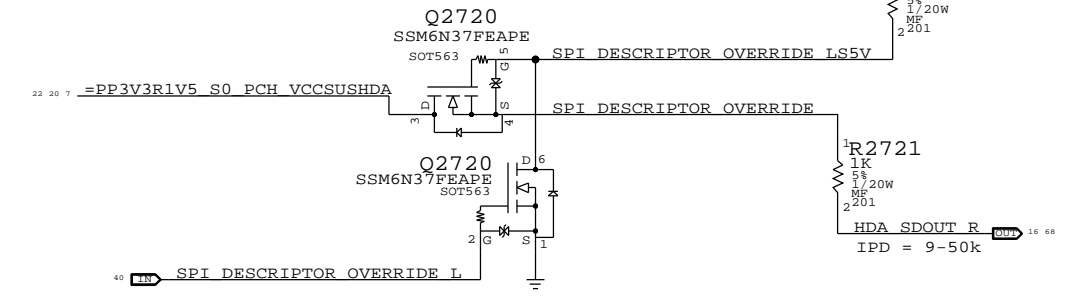
PCH S0 PWRGD



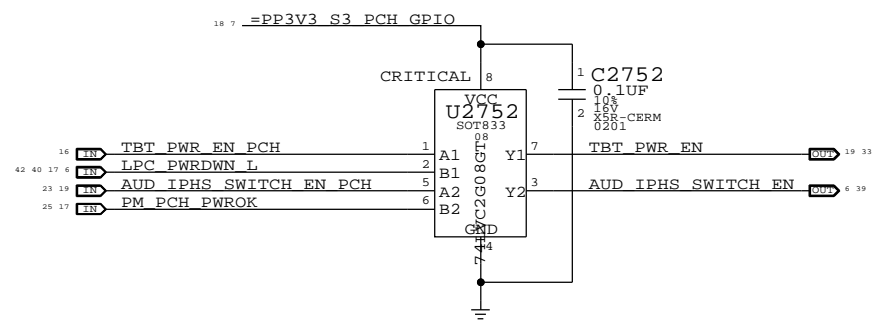
DP_AUXIO_EN Inversion



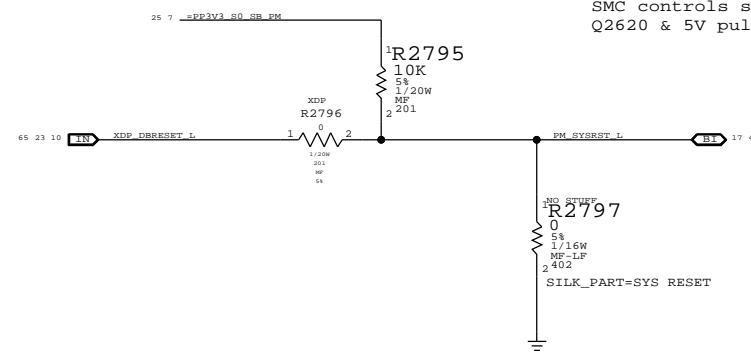
PCH ME Disable Strap



GPIO Glitch Prevention



PCH Reset Button



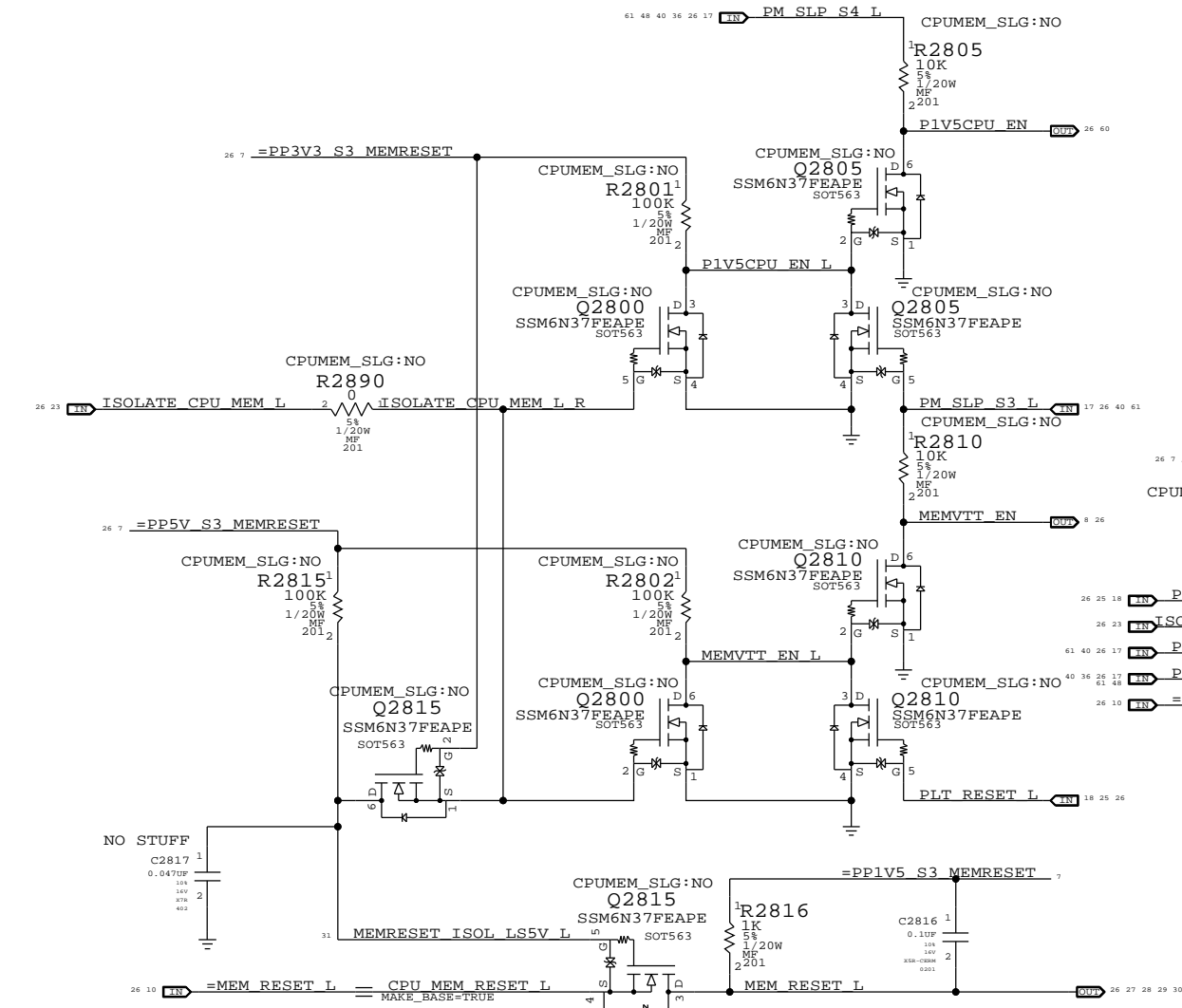
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

PAGE TITLE		DRAWING NUMBER		SIZE
Clock (CK505) and Chipset Support		051-9276		D
Apple Inc.		REVISION		2.7.0
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.
 WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
 WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
 MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
 MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

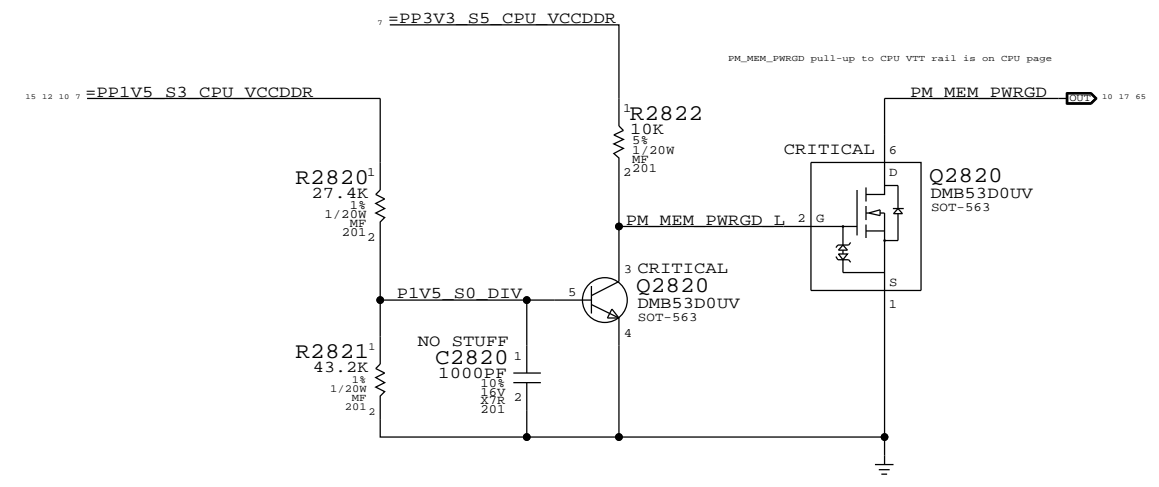


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1			
2	0	0		1	1		0	
3	0	0		1	X		0	
S3	4	0	0	1	X		0	
to	5	0	1	1	0 (*)		1	
6	0	1	1	1	1		1	
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

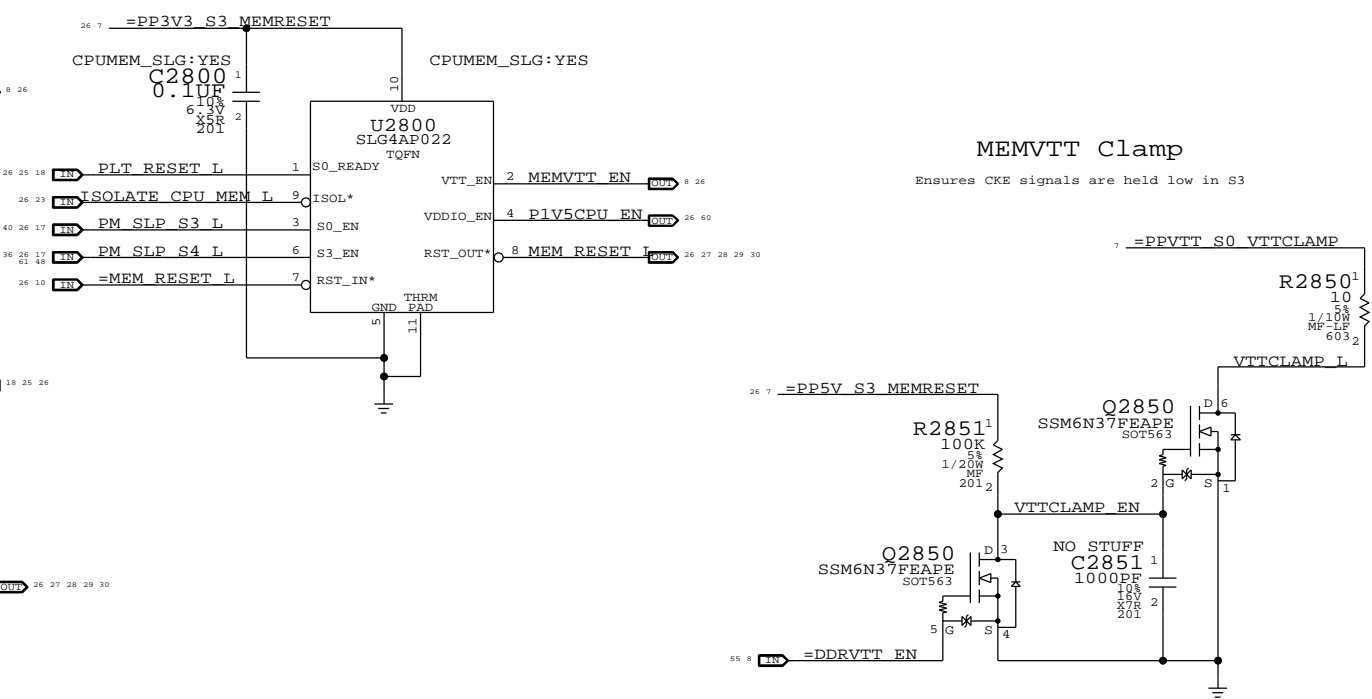
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU

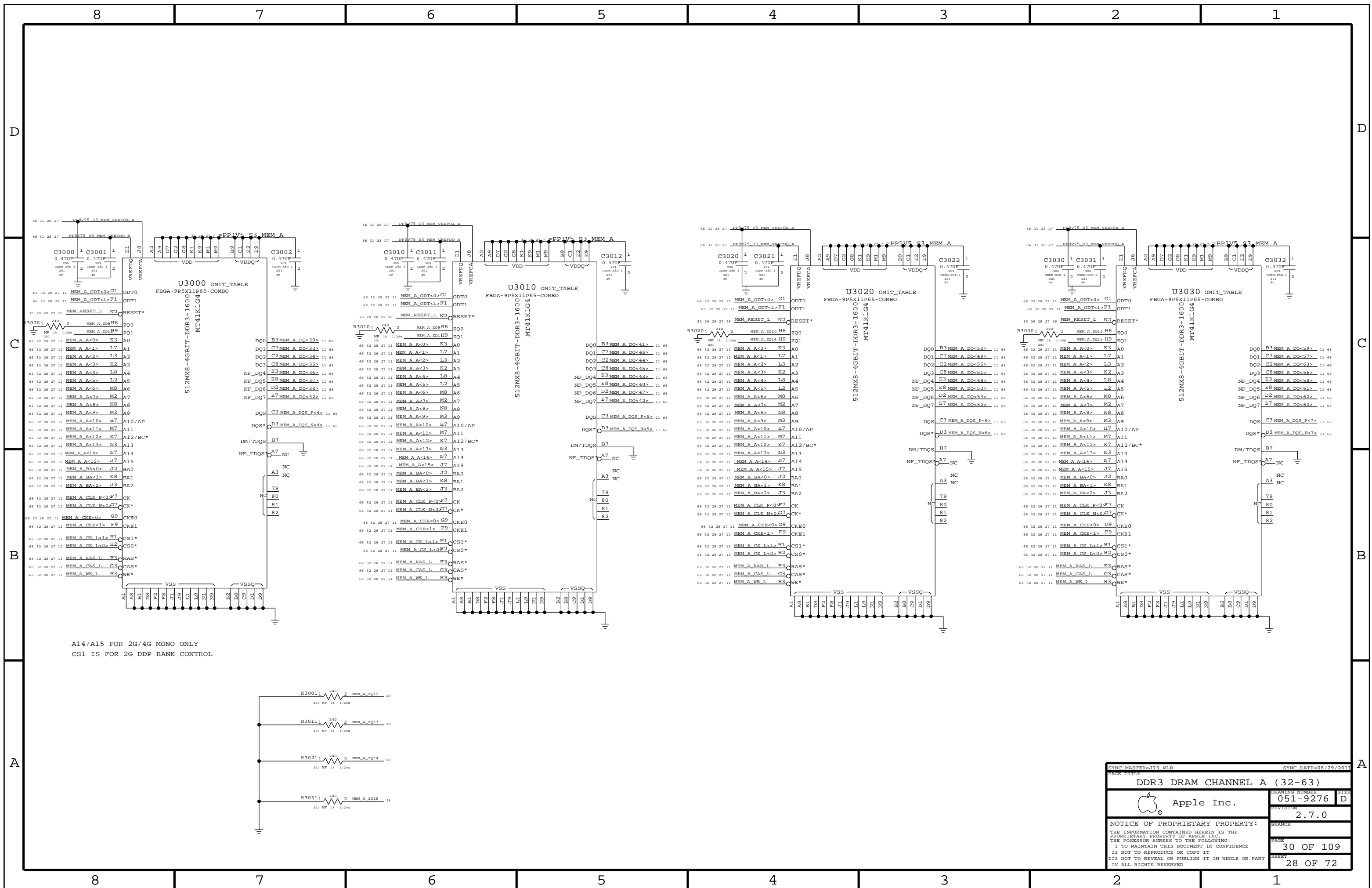


MEMVTT Clamp

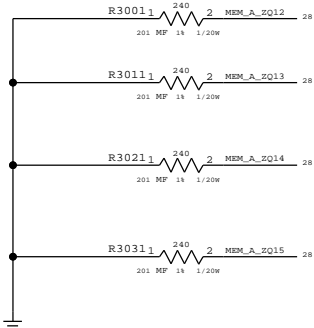
Ensures CKE signals are held low in S3



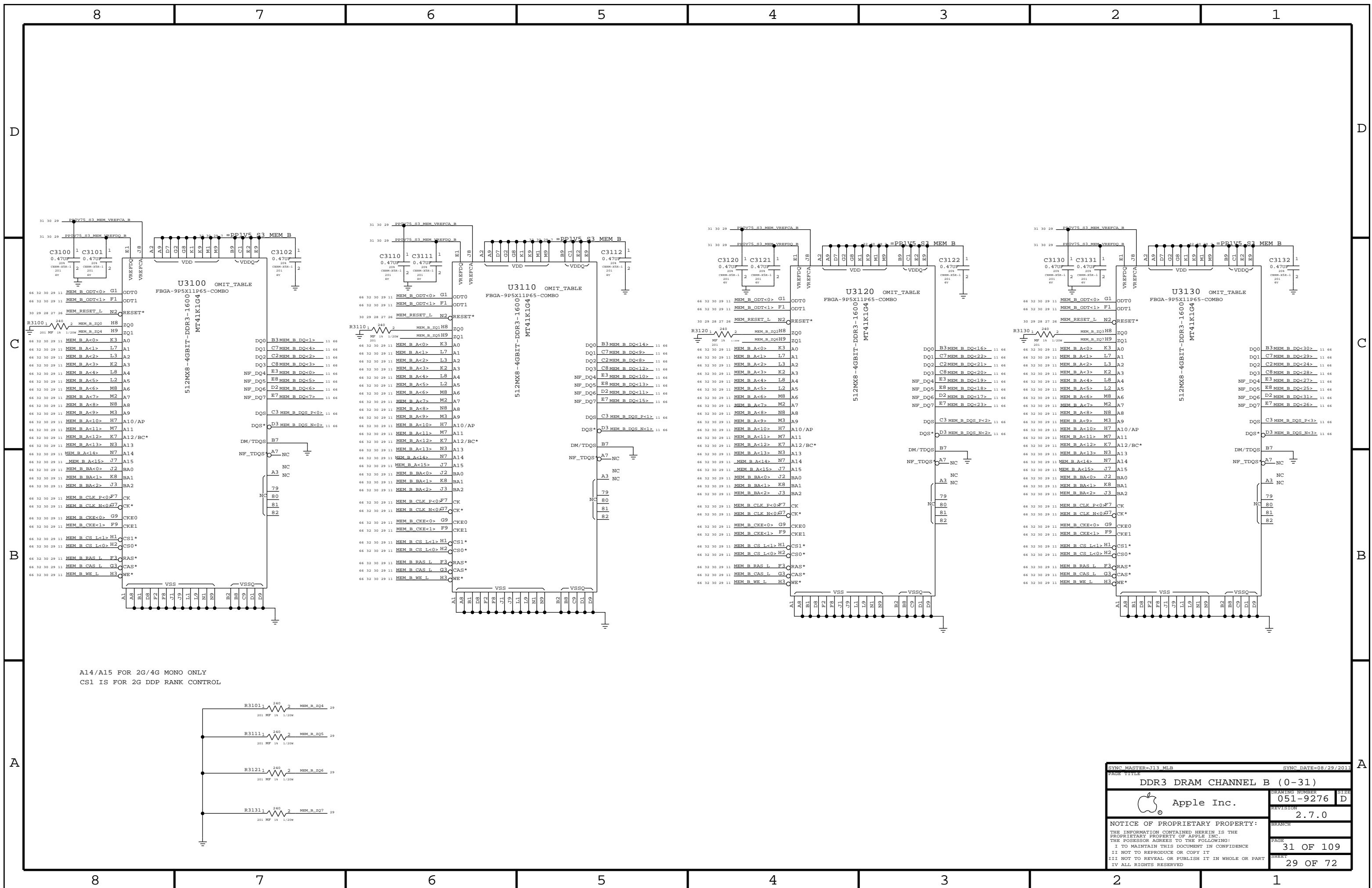
SYMC-WATER-013_MER		SYMC-DATA-11/18/2015	
CPU Memory S3 Support			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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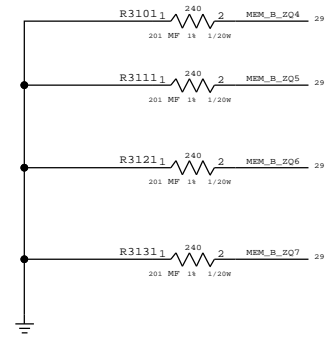
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



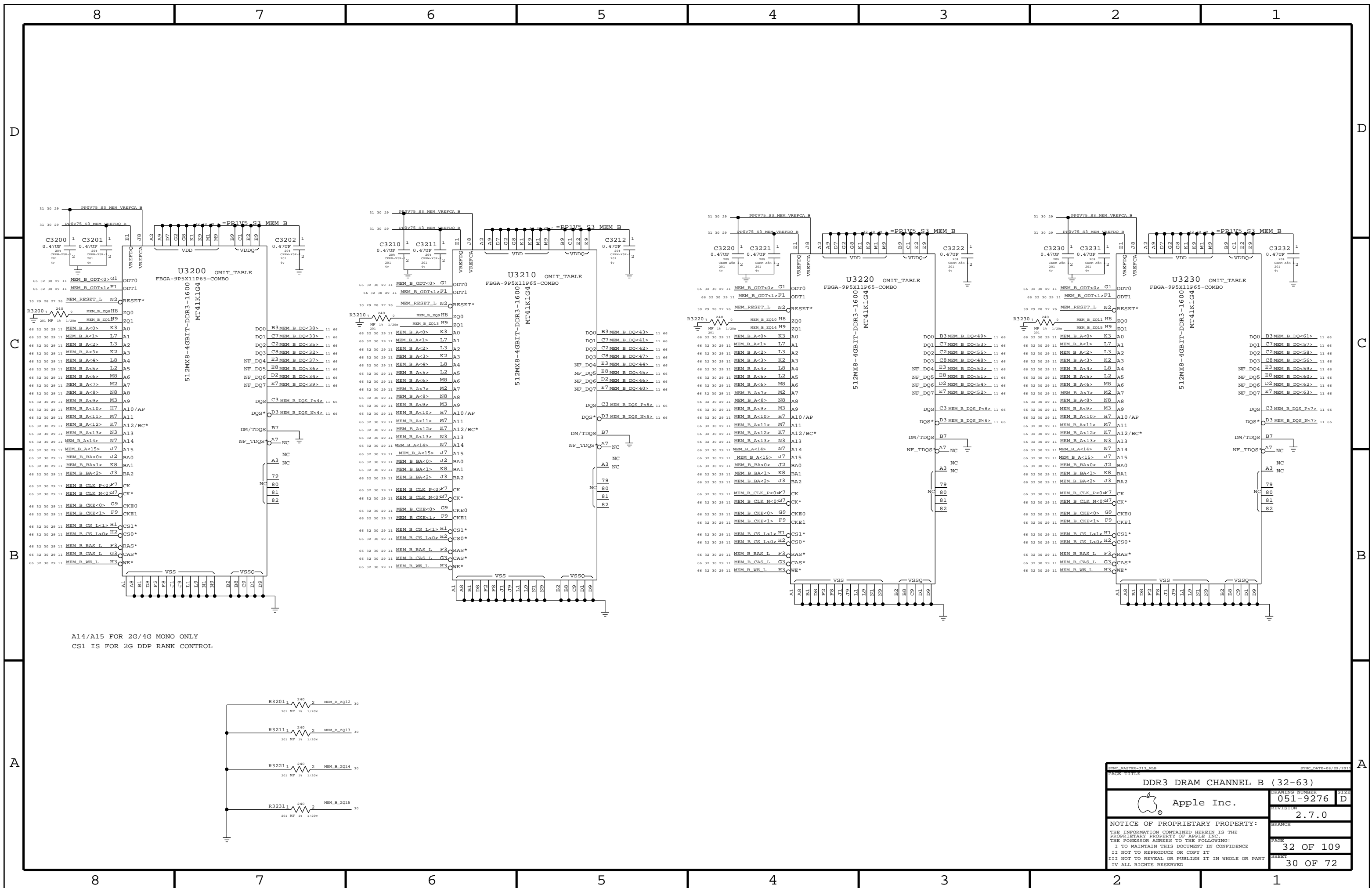
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DDR3 DRAM CHANNEL A (32-63)			
DRAWING NUMBER		SIZE	
051-9276		D	
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30 OF 109		28 OF 72	



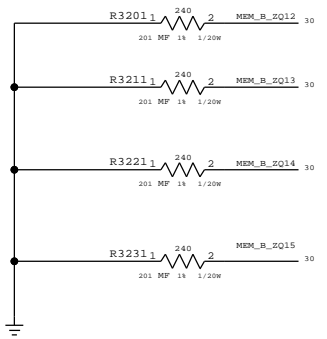
A14/A15 FOR 2G/4G MONO ONLY
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SYNC MASTER=113 MLB		SYNC DATE=08/29/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
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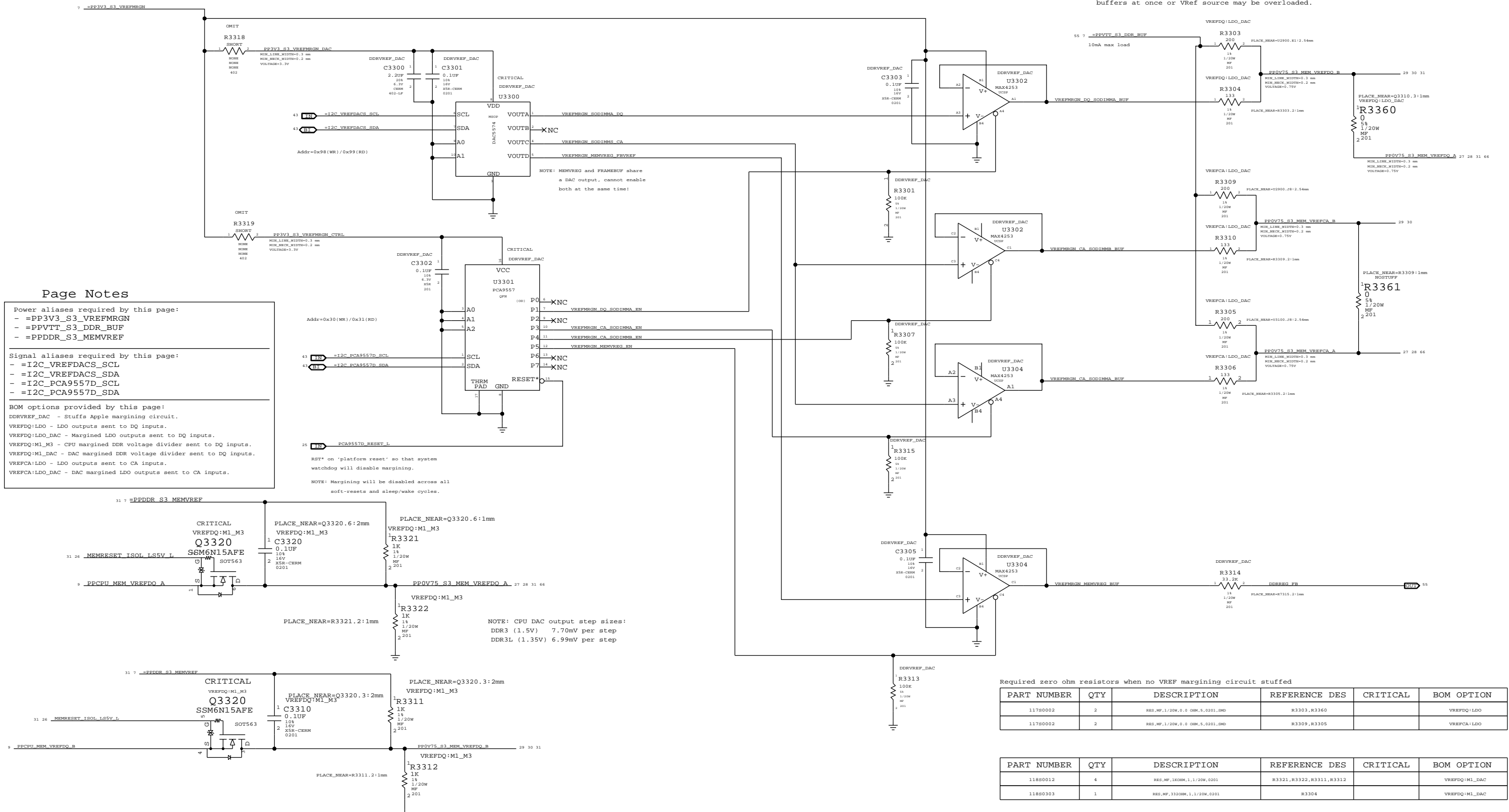


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PAGE TITLE			
DDR3 DRAM CHANNEL B (32-63)			
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or Vref source may be overloaded.



Page Notes

Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF
 - =PPDDR_S3_MEMVREF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 DDRVREF_DAC - Stuffs Apple margining circuit.
 VREFDQ:LDO - LDO outputs sent to DQ inputs.
 VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
 VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
 VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
 VREFCA:LDO - LDO outputs sent to CA inputs.
 VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
 DDR3 (1.5V) 7.70mV per step
 DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	2	RES,MP,1/20W,5.0 OHM,5,0201,080	R3303,R3360		VREFDQ:LDO
11780002	2	RES,MP,1/20W,5.0 OHM,5,0201,080	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880012	4	RES,MP,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
11880303	1	RES,MP,3320OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYMC: WATERS-113_MBR SYMC: DATE: 11/18/2011

051-9276

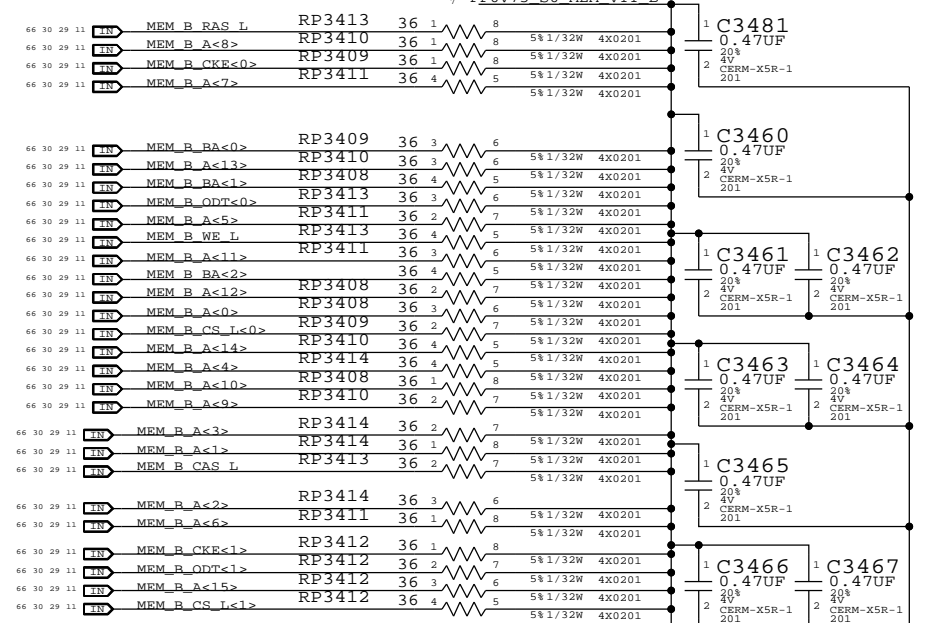
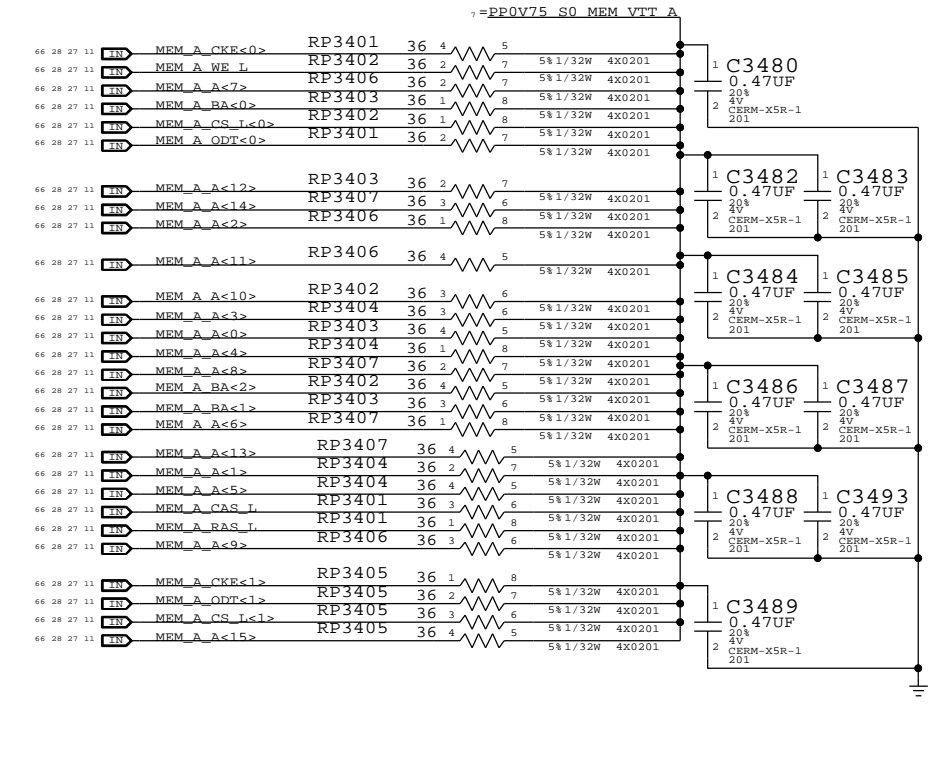
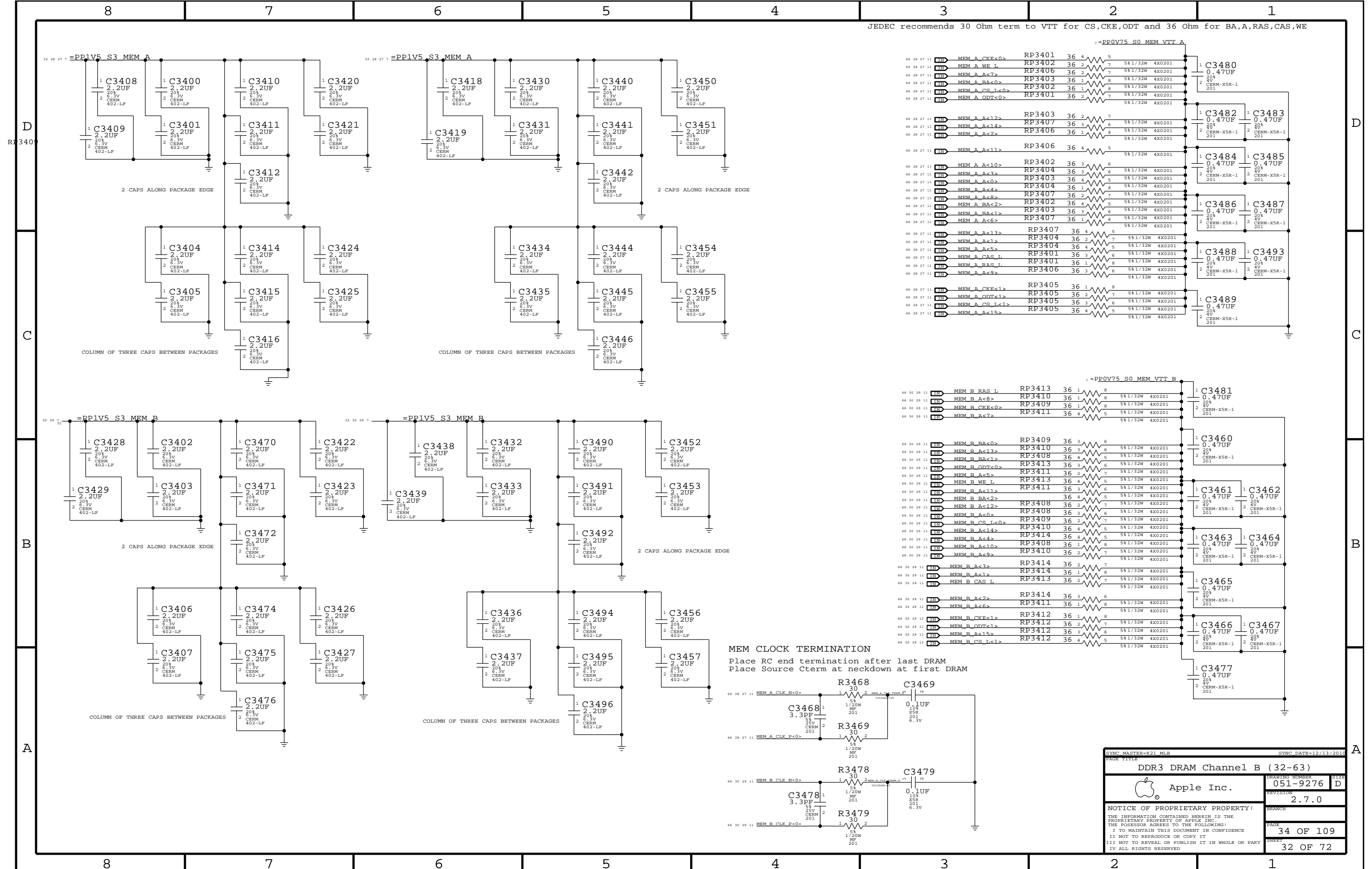
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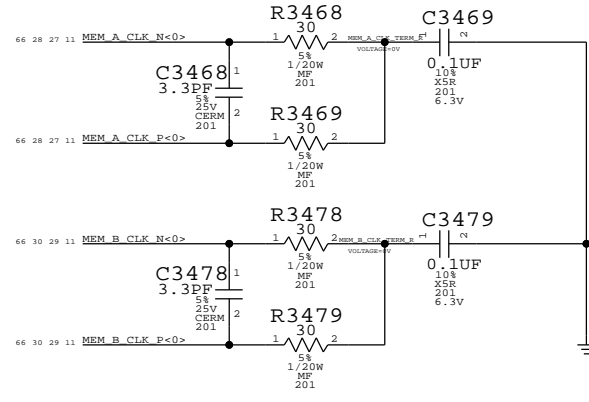
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JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=K21 MLB SYNC DATE=12/13/2014

DDR3 DRAM Channel B (32-63)

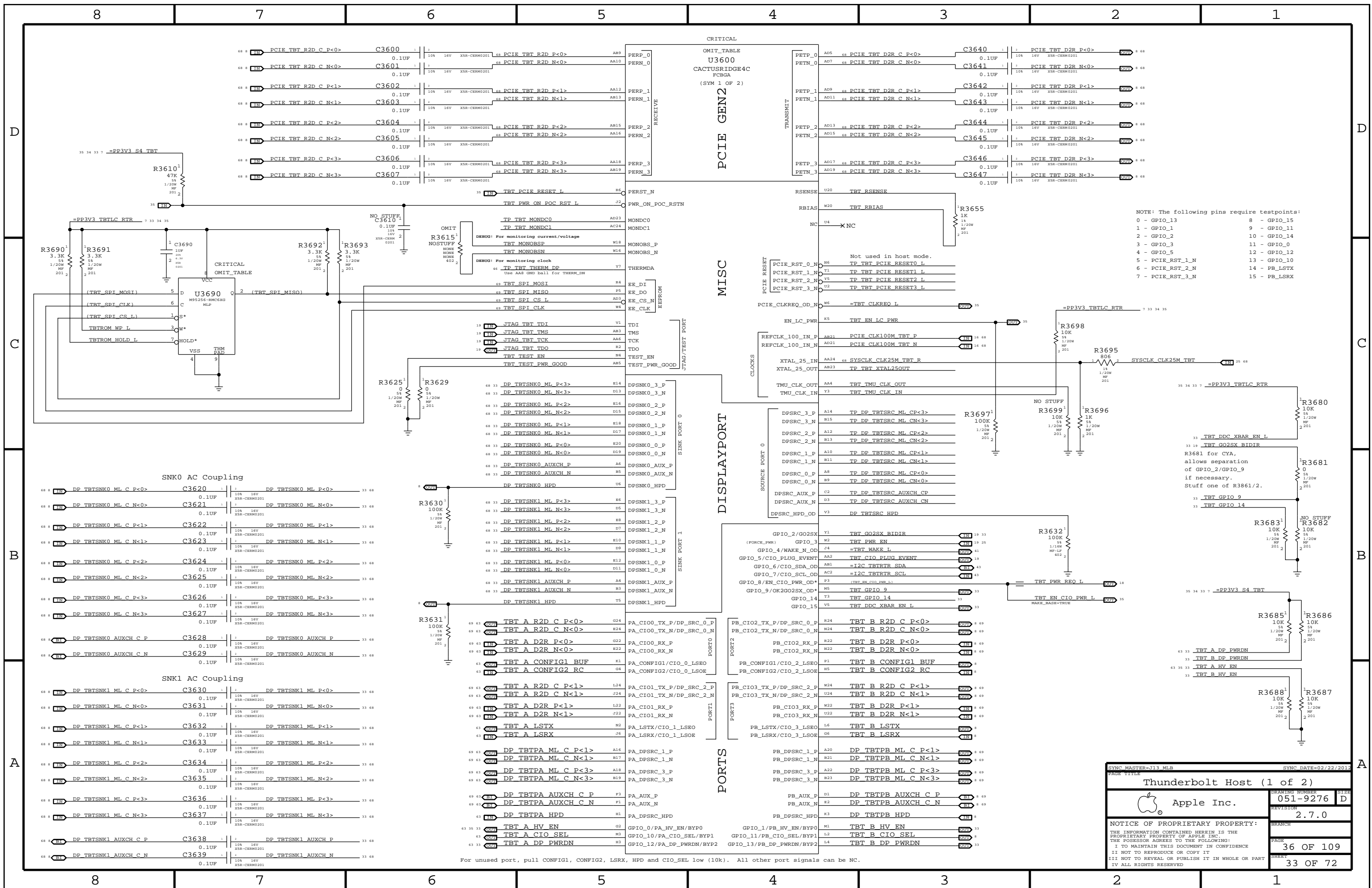
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Thunderbolt Host (1 of 2)

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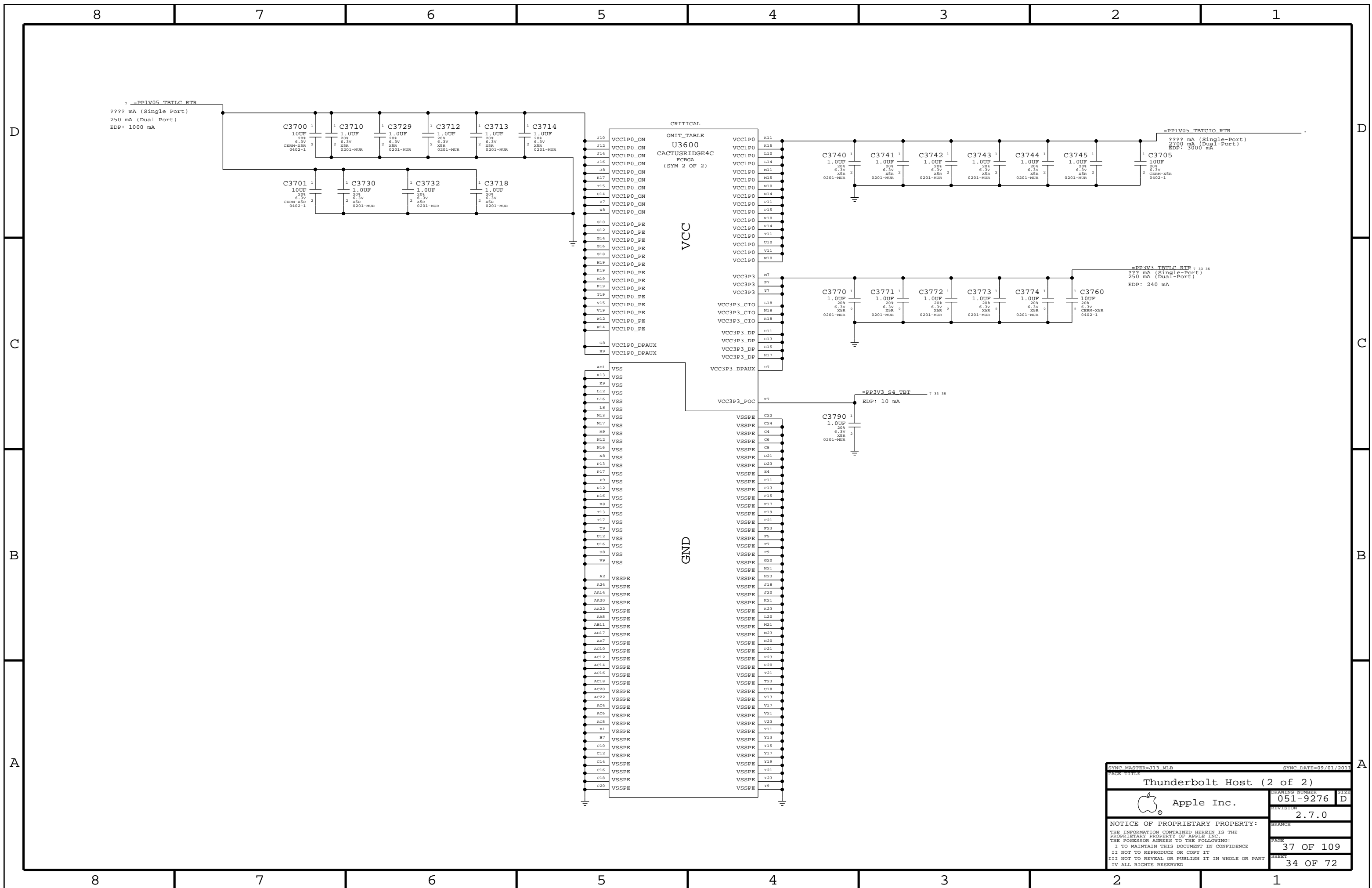
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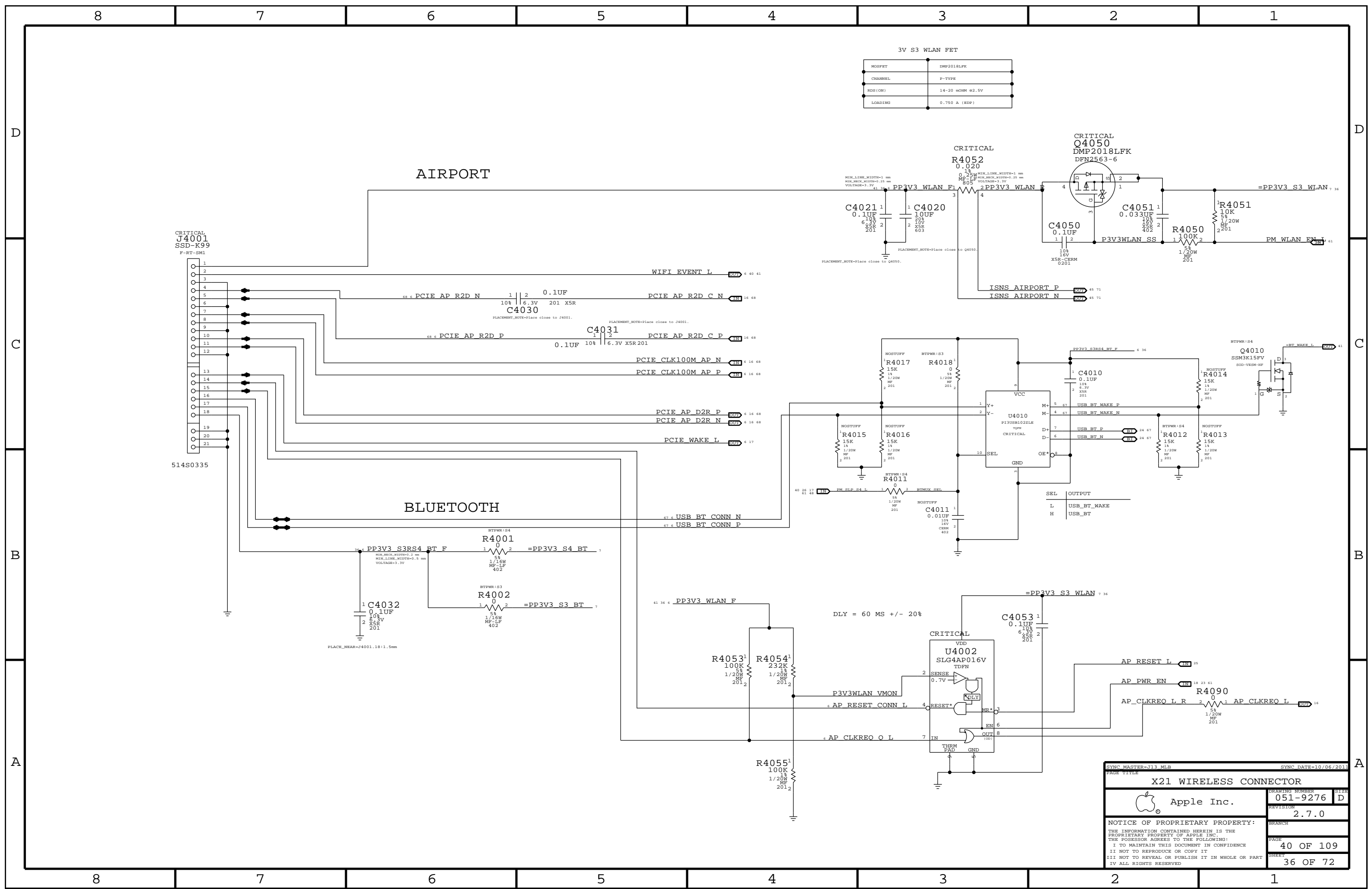
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Thunderbolt Host (2 of 2)			
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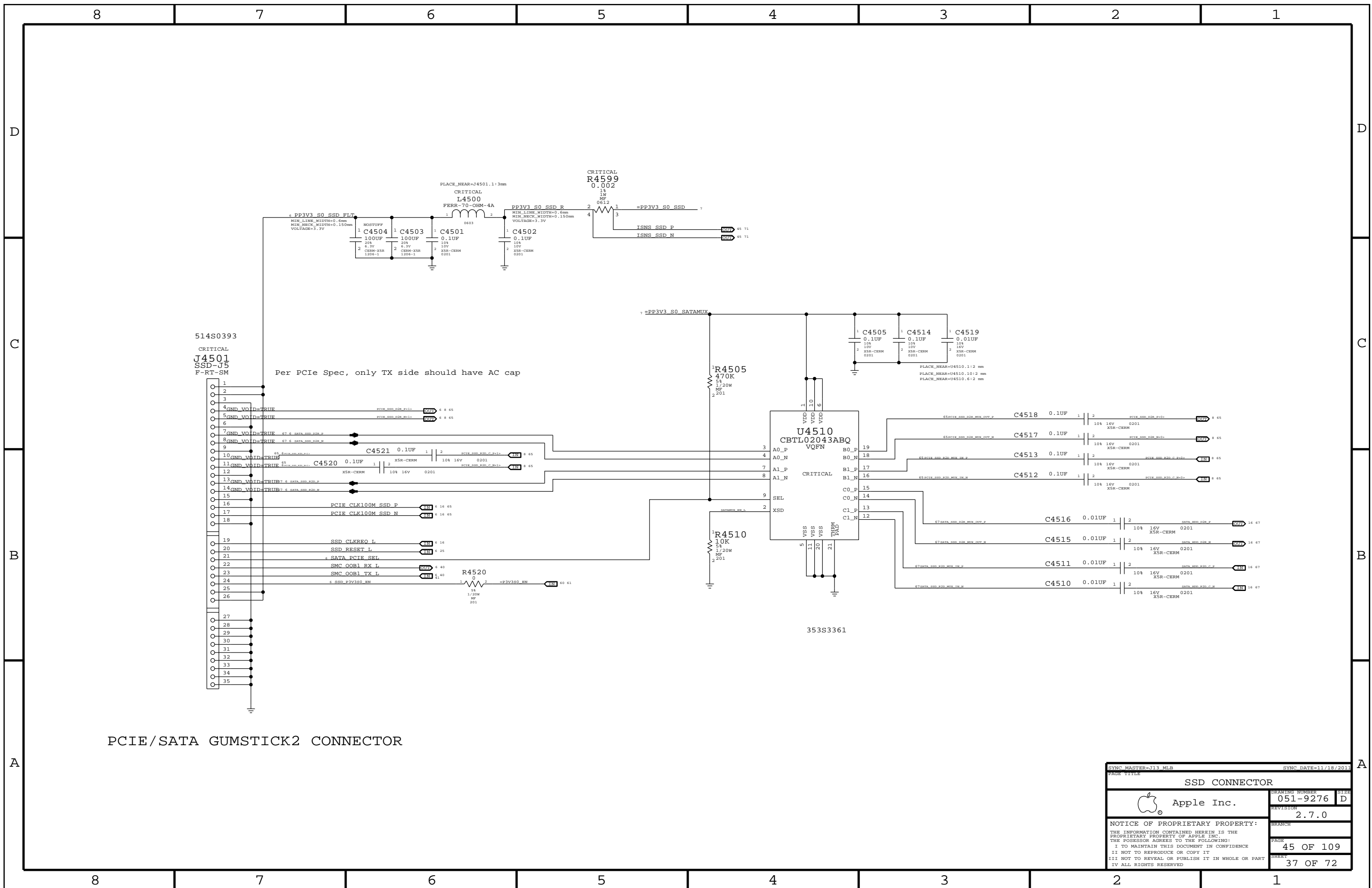


3V S3 WLAN FET	
MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON)	14-20 mOHM @2.5V
LOADING	0.750 A (RDP)

AIRPORT

BLUETOOTH

SYNC MASTER=113 MLB		SYNC DATE=10/06/2011	
X21 WIRELESS CONNECTOR			
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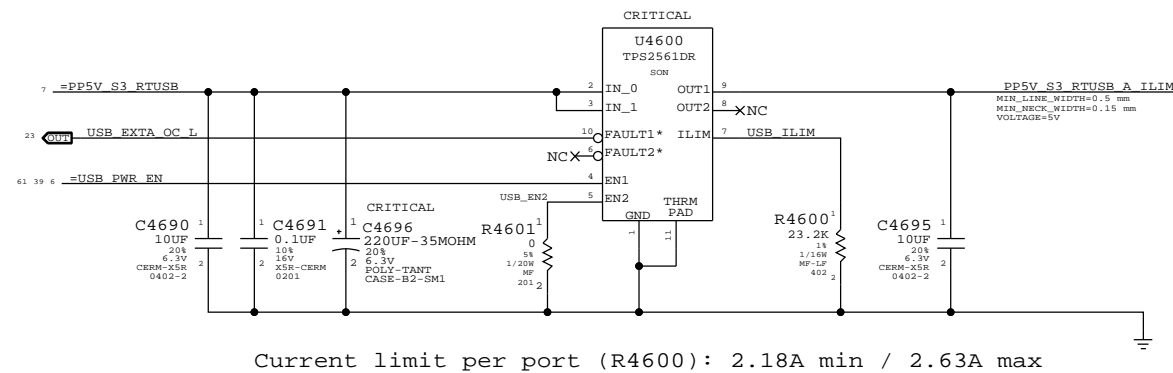


PCIE/SATA GUMSTICK2 CONNECTOR

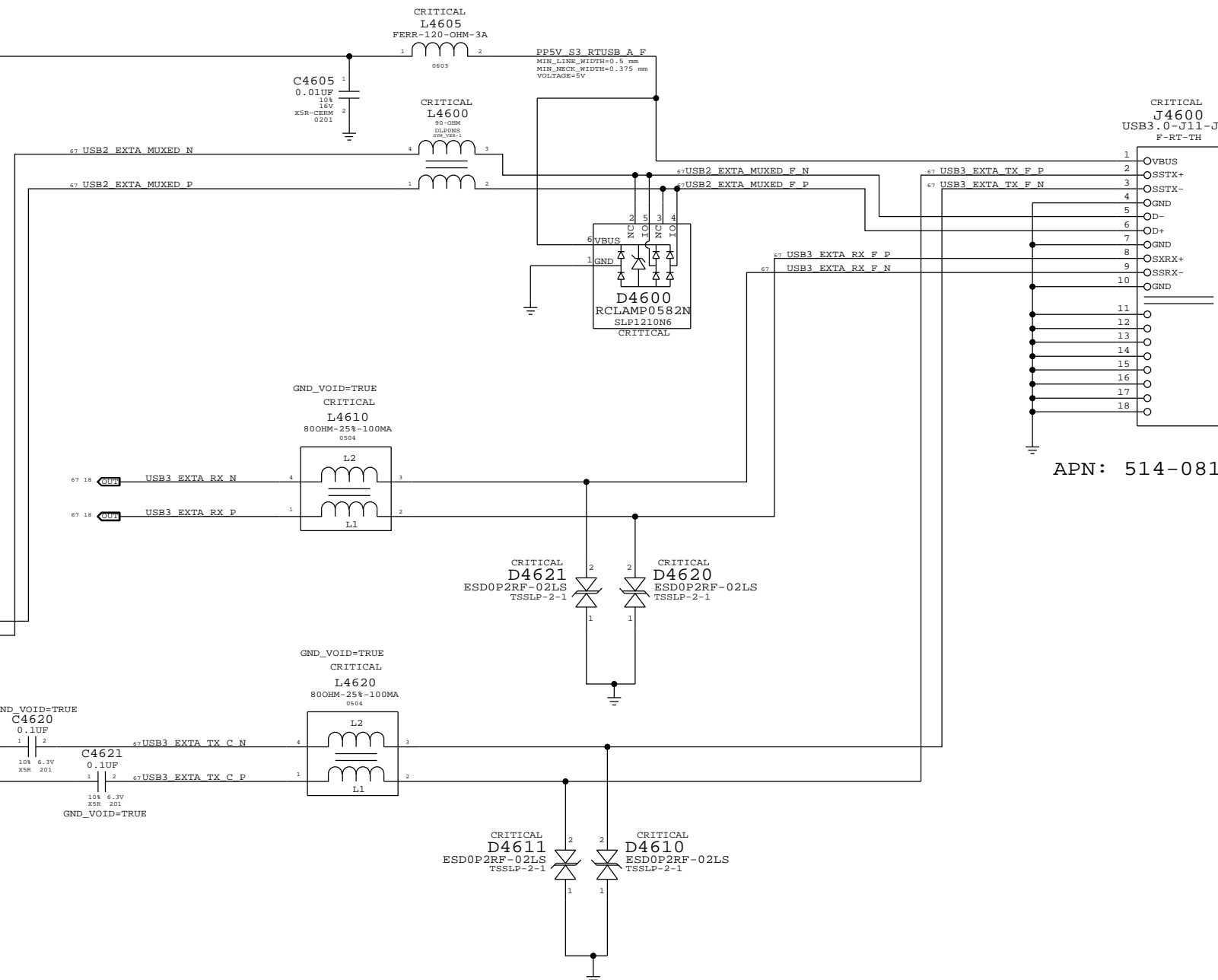
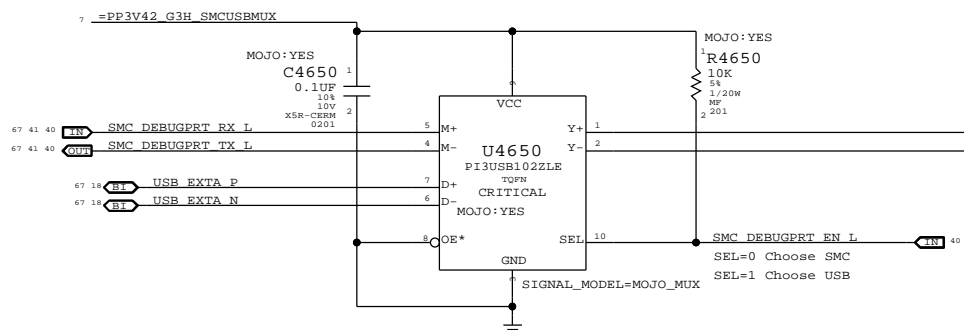
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SSD CONNECTOR			
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Right USB Port A

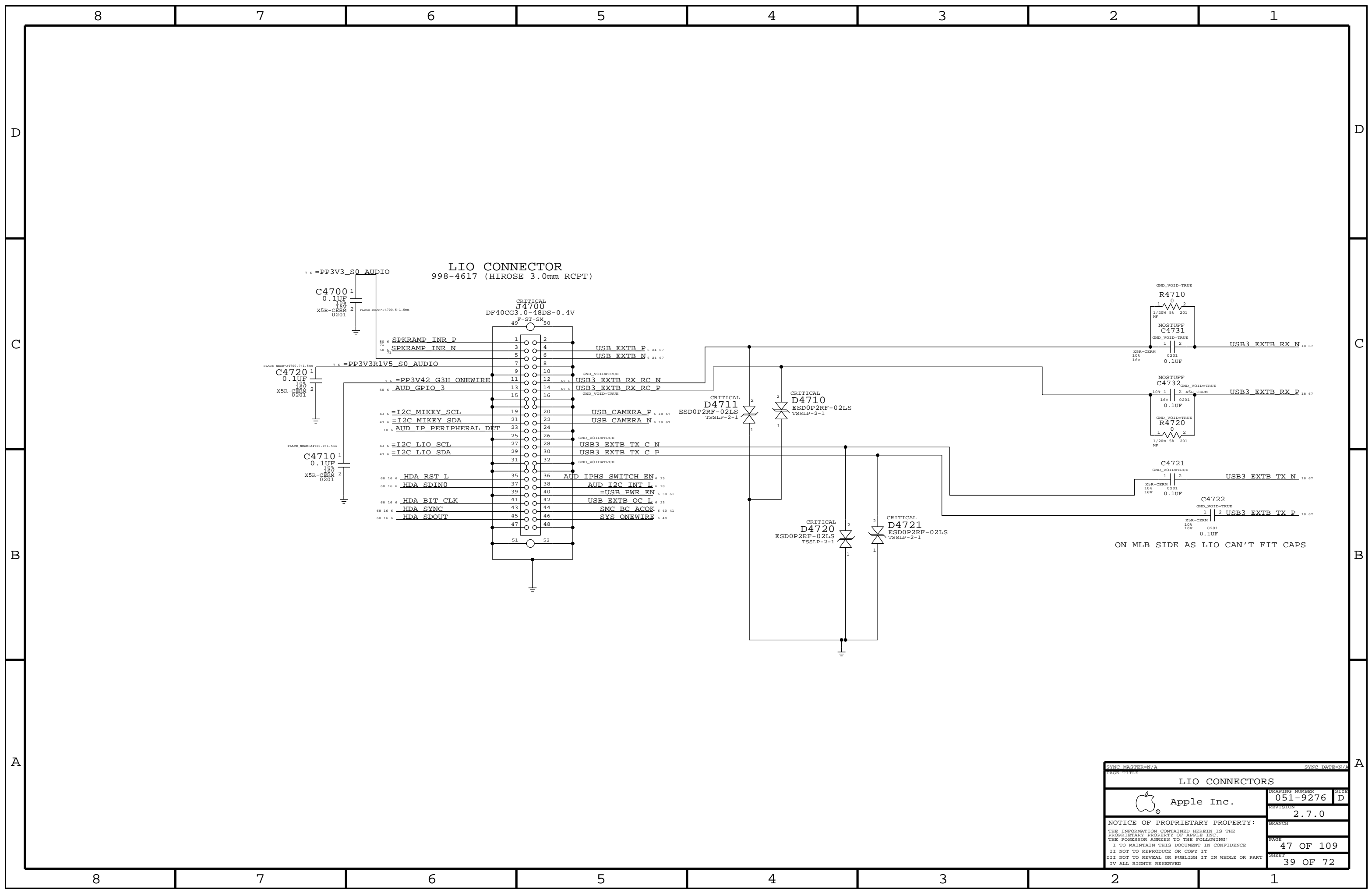
USB Port Power Switch



Mojo SMC Debug Mux

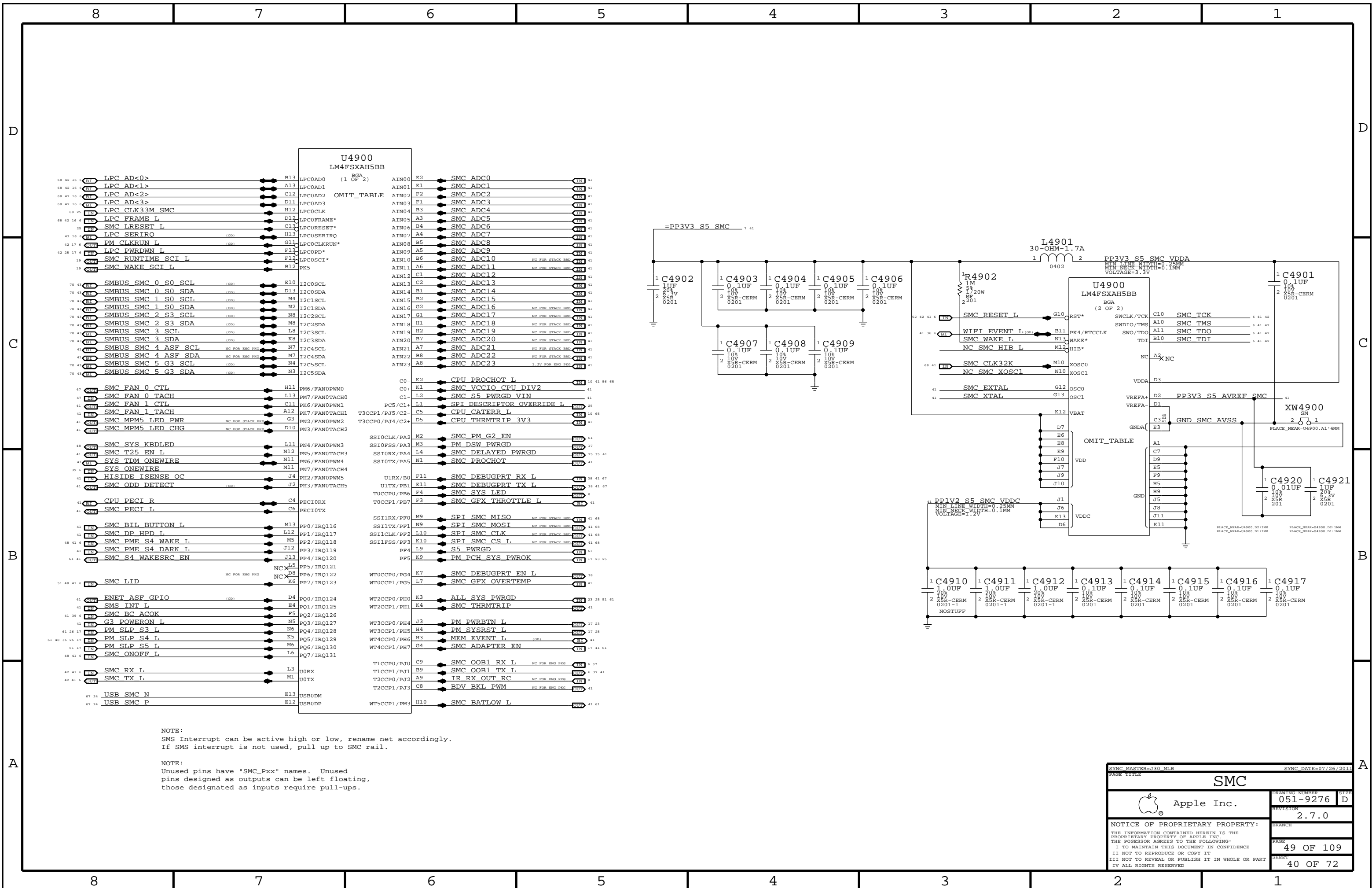


SYNC MASTER=J13_MLB		SYNC DATE=10/06/2011	
External A USB3 Connector			
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LIO CONNECTORS			
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ON MLB SIDE AS LIO CAN'T FIT CAPS

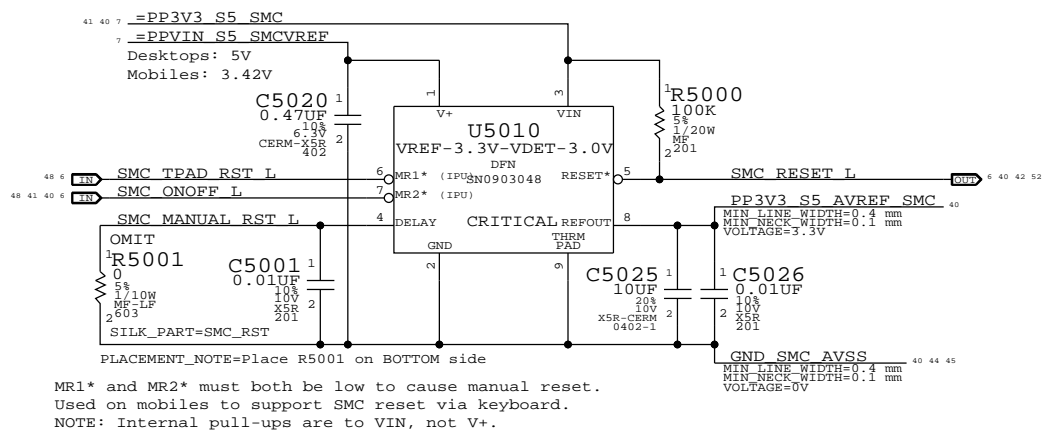


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

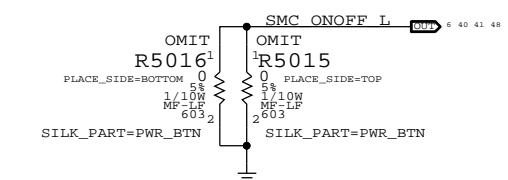
NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=J30_MLB		SYNC DATE=07/26/2011	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
		051-9276	D
		REVISION	
		2.7.0	
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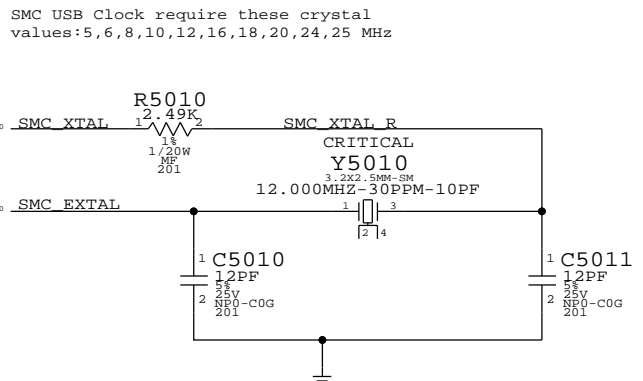
SMC Reset "Button", Supervisor & AVREF Supply



Debug Power "Buttons"



SMC Crystal Circuit

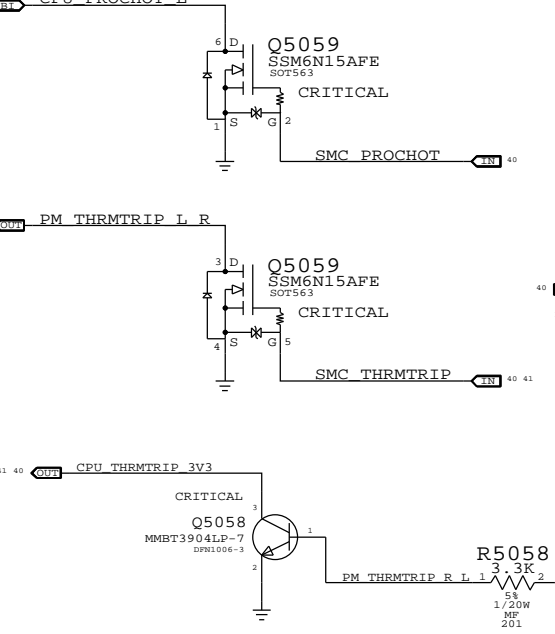
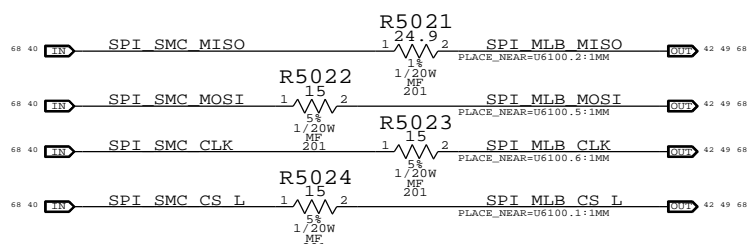


- SMC_ADC0 = SMC_CPU_VSENSE
- SMC_ADC1 = SMC_CPU_ISENSE
- SMC_ADC2 = MAKE_BASE=TRUE
- SMC_ADC3 = SMC_VCCSA_VSENSE
- SMC_ADC4 = SMC_DCIN_VSENSE
- SMC_ADC5 = SMC_DCIN_ISENSE
- SMC_ADC6 = SMC_HDD_ISENSE
- SMC_ADC7 = SMC_BMON_ISENSE
- SMC_ADC8 = SMC_HS_COMPUTING_ISENSE
- SMC_ADC9 = SMC_OTHER_HI_ISENSE
- SMC_ADC10 = SMC_1V5S3_ISENSE
- SMC_ADC11 = SMC_CPUVCCIO_ISENSE
- SMC_ADC12 = SMC_GFX_VSENSE
- SMC_ADC13 = SMC_CPU_SA_ISENSE
- SMC_ADC14 = SMC_3V3S0_ISENSE
- SMC_ADC15 = SMC_WLAN_ISENSE
- SMC_ADC16 = SMC_LCDBKLT_ISENSE
- SMC_ADC17 = NC_SMC_ADC17
- SMC_ADC18 = SMC_GFX_ISENSE
- SMC_ADC19 = SMC_GFX_ISENSE
- SMC_ADC20 = NC_SMC_ADC20
- SMC_ADC21 = NC_SMC_ADC21
- SMC_ADC22 = NC_SMC_ADC22
- SMC_ADC23 = SMC_ADC23
- SMC_GFX_OVERTEMP = NC_SMC_GFX_OVERTEMP
- SMC_GFX_THROTTLE L = NC_SMC_GFX_THROTTLE L
- SMC_FAN_1_CTL = NC_SMC_FAN_1_CTL
- SMC_FAN_1_TACH = NC_SMC_FAN_1_TACH
- ENET ASF GPIO = NC_ENET_ASF_GPIO
- SMC_MPM5_LED_PWR = NC_SMC_MPM5_LED_PWR
- SMC_MPM5_LED_CHG = NC_SMC_MPM5_LED_CHG
- SYS_TDM_ONEWIRE = NC_SYS_TDM_ONEWIRE

- SMC_DP_HPD L = NC_SMC_DP_HPD L
- CHGR_ACOK = MAKE_BASE=TRUE
- HISIDE_ISENSE_OC = NC_HISIDE_ISENSE_OC
- SMBUS_SMC_4_ASF_SCL = NC_SMBUS_SMC_4_ASF_SCL
- SMBUS_SMC_4_ASF_SDA = NC_SMBUS_SMC_4_ASF_SDA
- BDV_BKL_PWM = NC_BDV_BKL_PWM
- SMC_PME_S4_DARK L = =TBT_WAKE L
- SMC_T25_EN L = NC_SMC_T25_EN L
- PM_CLK32K_SUSCLK R1 = SMC_CLK32K

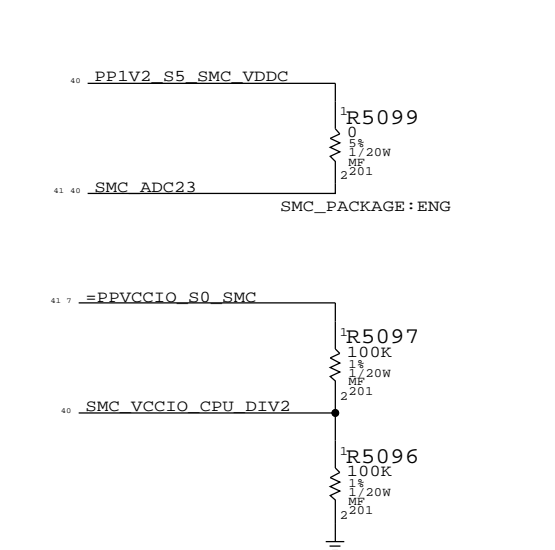
SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

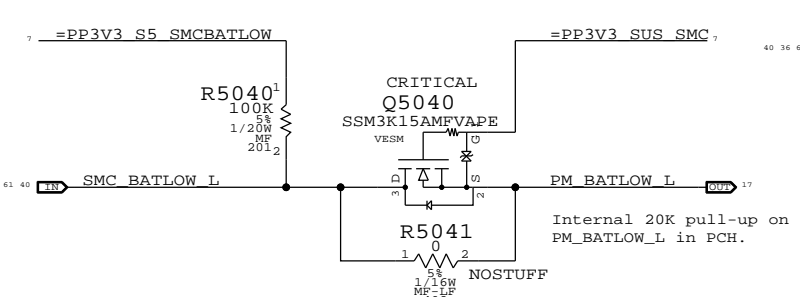


SMC12 Eng Pkg Support

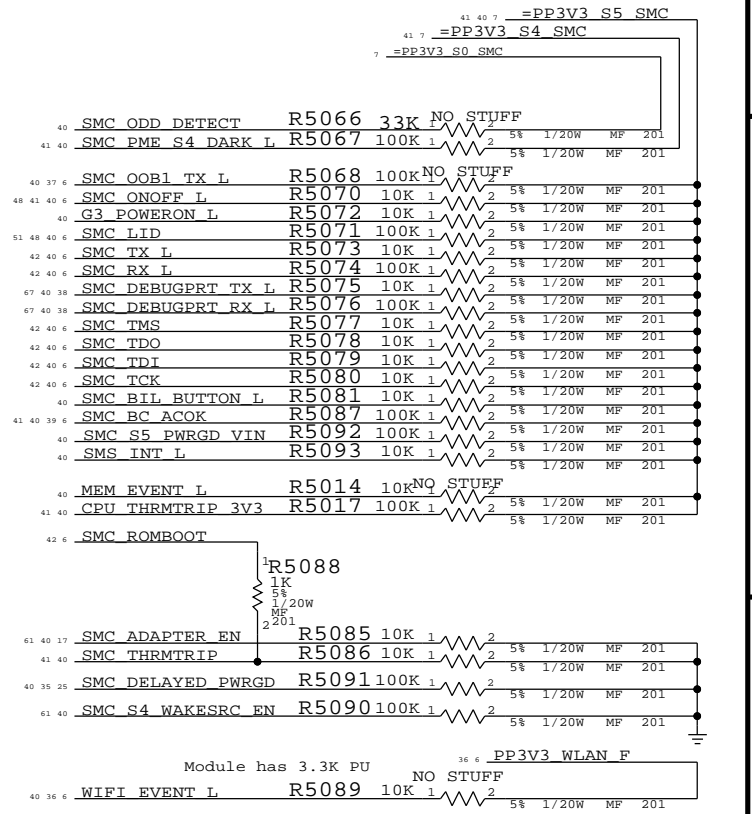
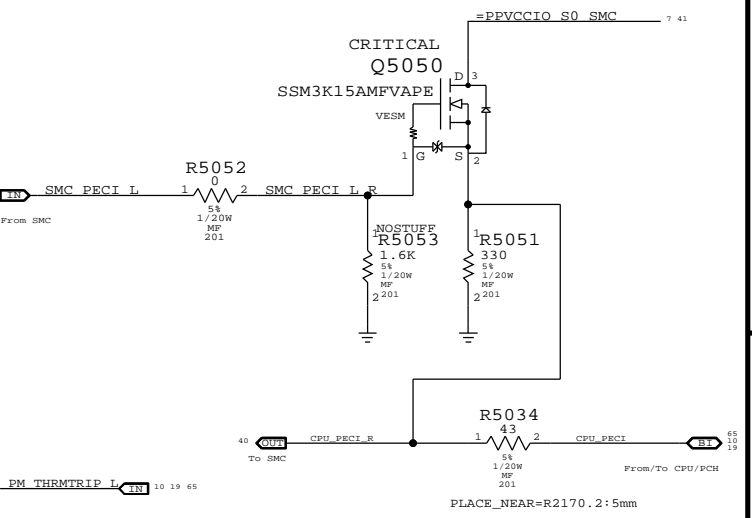
Eng Package requires 1.2V ON SMC_ADC23 pin.



BATLOW# Isolation



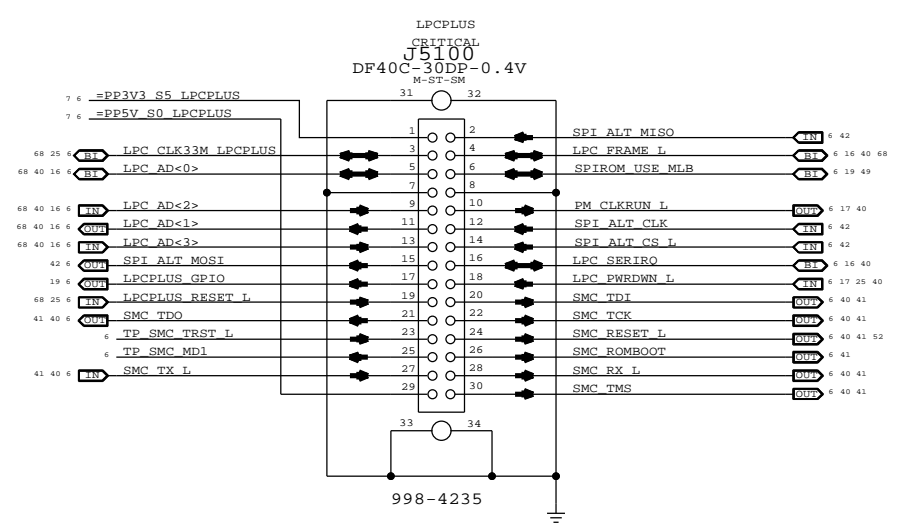
SMC12 PECEI Support



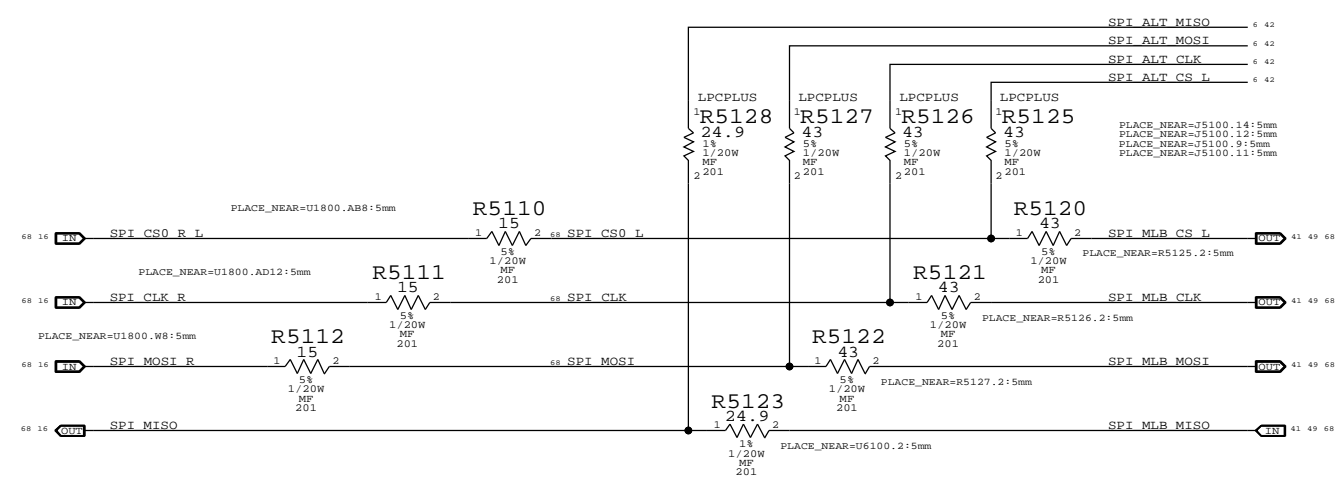
SYNC MASTER=J13_MLB		SYNC DATE=10/06/2011	
SMC Support			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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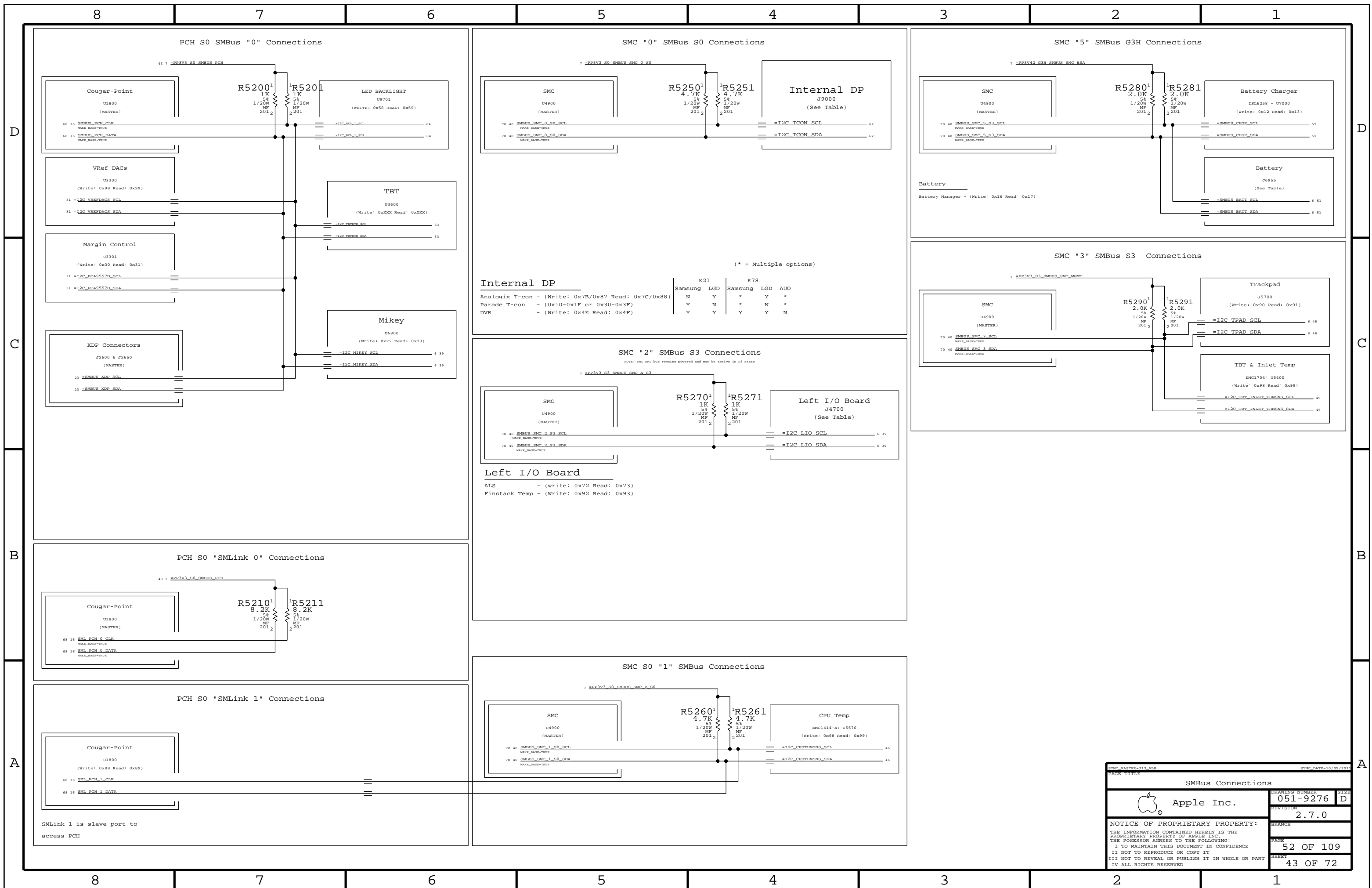
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
		051-9276	D
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Internal DP

Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)
 Parade T-con - (0x10-0x1F or 0x30-0x3F)
 DVR - (Write: 0x4E Read: 0x4F)

(* = Multiple options)

	K21		K78	
	Samsung	LGD	Samsung	LGD AUO
Analogix T-con	N	Y	*	Y *
Parade T-con	Y	N	*	N *
DVR	Y	Y	Y	Y N

Left I/O Board

ALS - (write: 0x72 Read: 0x73)
 Finstack Temp - (Write: 0x92 Read: 0x93)

SYMC MASTER=113_MCB SYMC DATE=10/05/2011

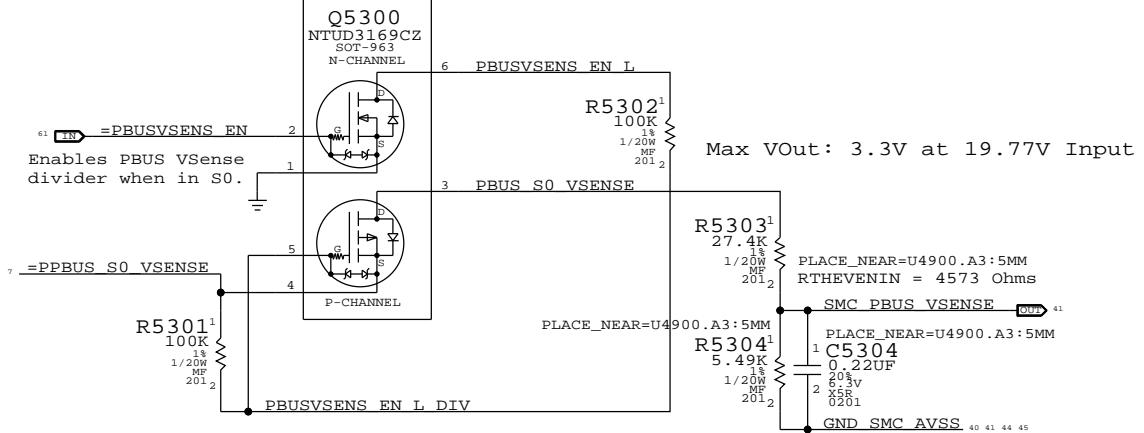
Apple Inc.

SMBus Connections

DRAWING NUMBER: 051-9276 SIZE: D
 REVISION: 2.7.0
 BRANCH:
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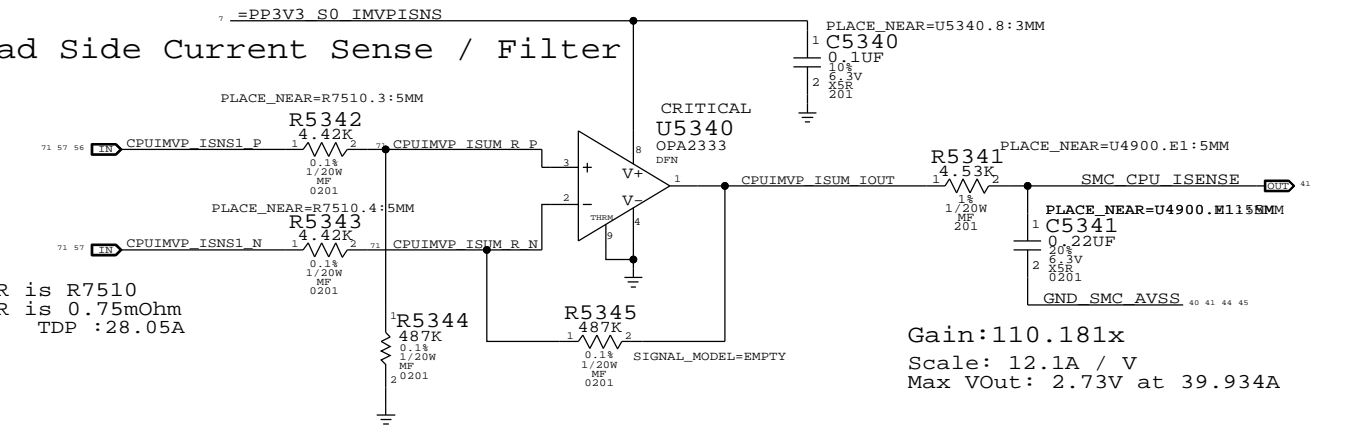
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PBUS Voltage Sense Enable & Filter



Max VOut: 3.3V at 19.77V Input

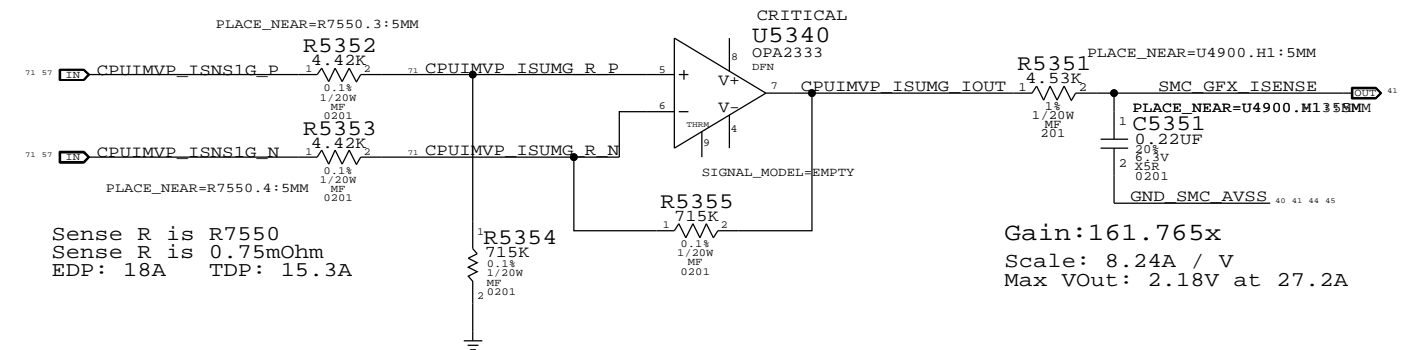
CPU VCore Load Side Current Sense / Filter



Sense R is R7510
Sense R is 0.75mOhm
EDP: 33A TDP :28.05A

Gain:110.18lx
Scale: 12.1A / V
Max VOut: 2.73V at 39.934A

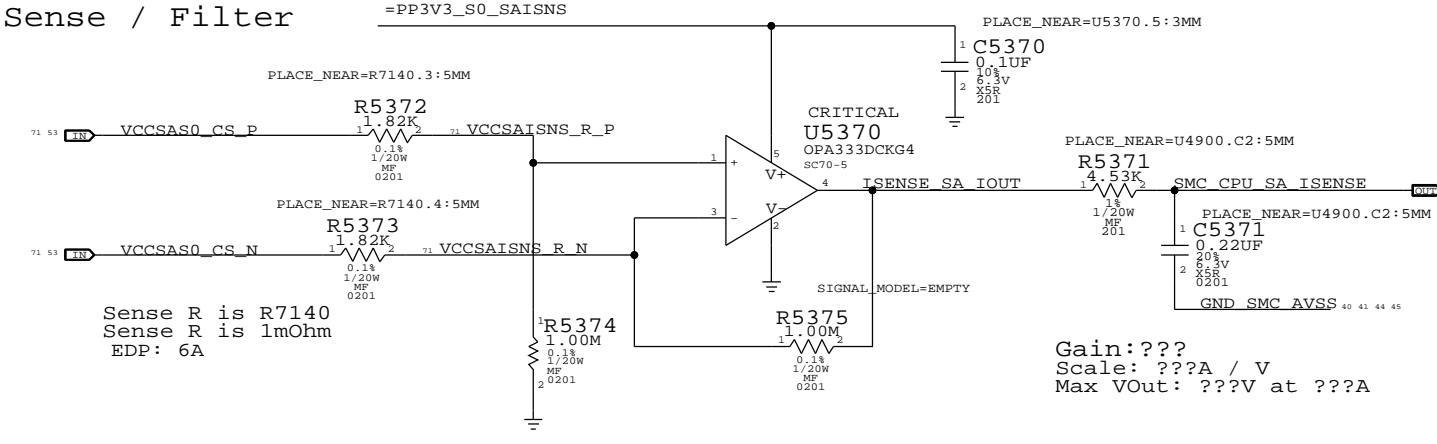
GFX/IG VCore Load Side Current Sense / Filter



Sense R is R7550
Sense R is 0.75mOhm
EDP: 18A TDP: 15.3A

Gain:161.765x
Scale: 8.24A / V
Max VOut: 2.18V at 27.2A

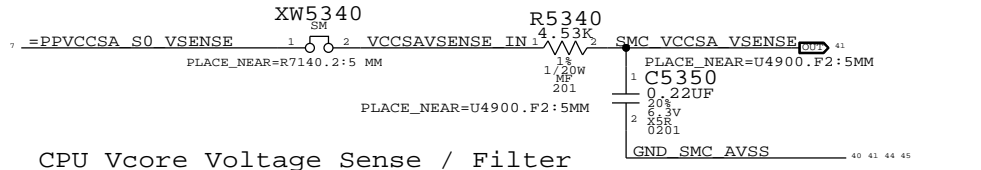
CPU SA Current Sense / Filter



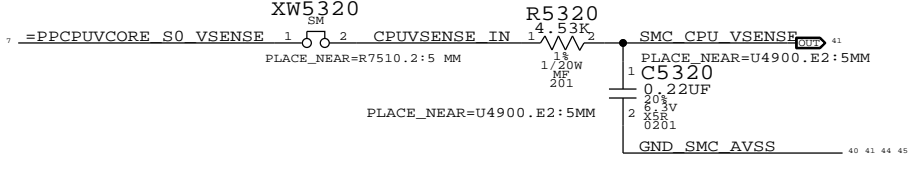
Sense R is R7140
Sense R is 1mOhm
EDP: 6A

Gain:???
Scale: ???A / V
Max VOut: ???V at ???A

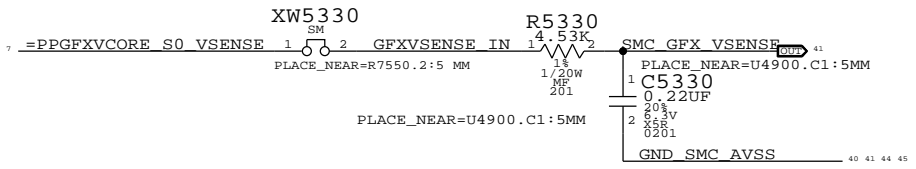
VCCSA Voltage Sense / Filter



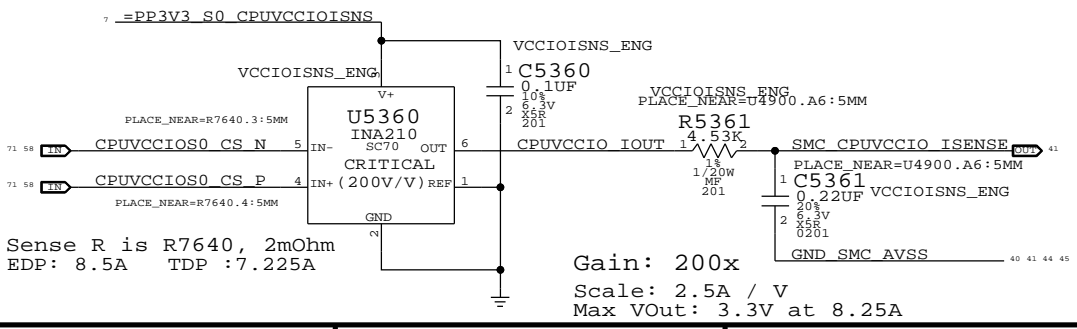
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



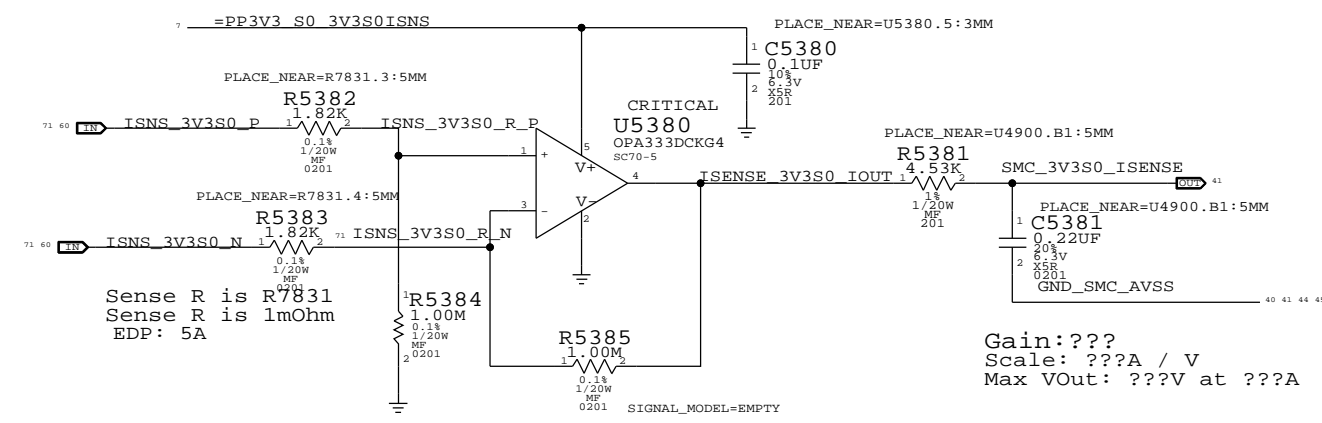
CPU 1.05V VCCIO Current Sense / Filter



Sense R is R7640, 2mOhm
EDP: 8.5A TDP :7.225A

Gain: 200x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

3.3V S0 FET Current Sense / Filter



Sense R is R7831
Sense R is 1mOhm
EDP: 5A

Gain:???
Scale: ???A / V
Max VOut: ???V at ???A

PAGE TITLE		SYNC DATE=09/15/2011	
Voltage & Load Side Current Sensing		DRAWING NUMBER	SIZE
Apple Inc.		051-9276	D
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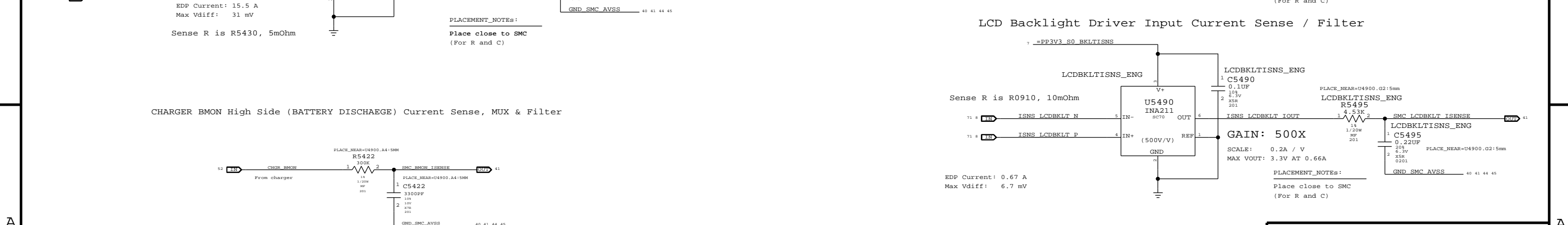
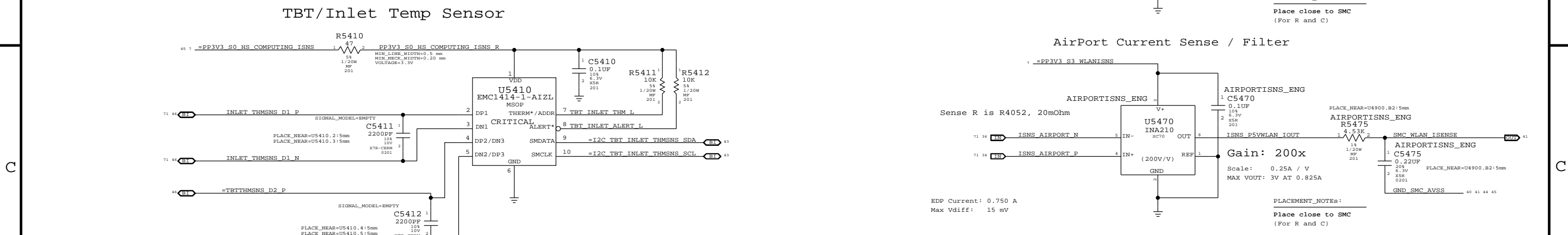
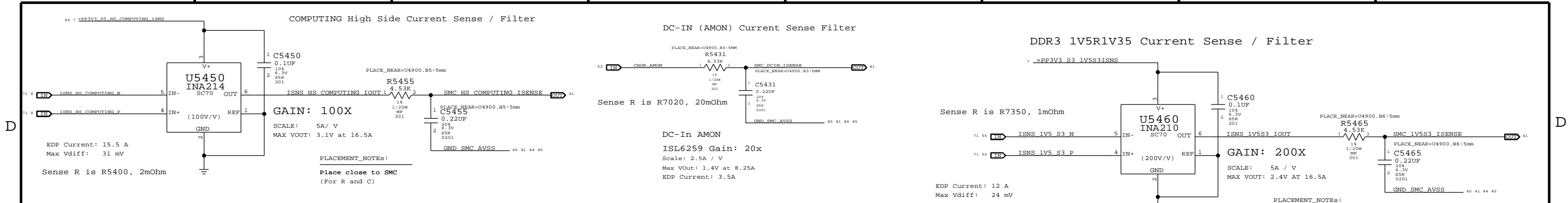
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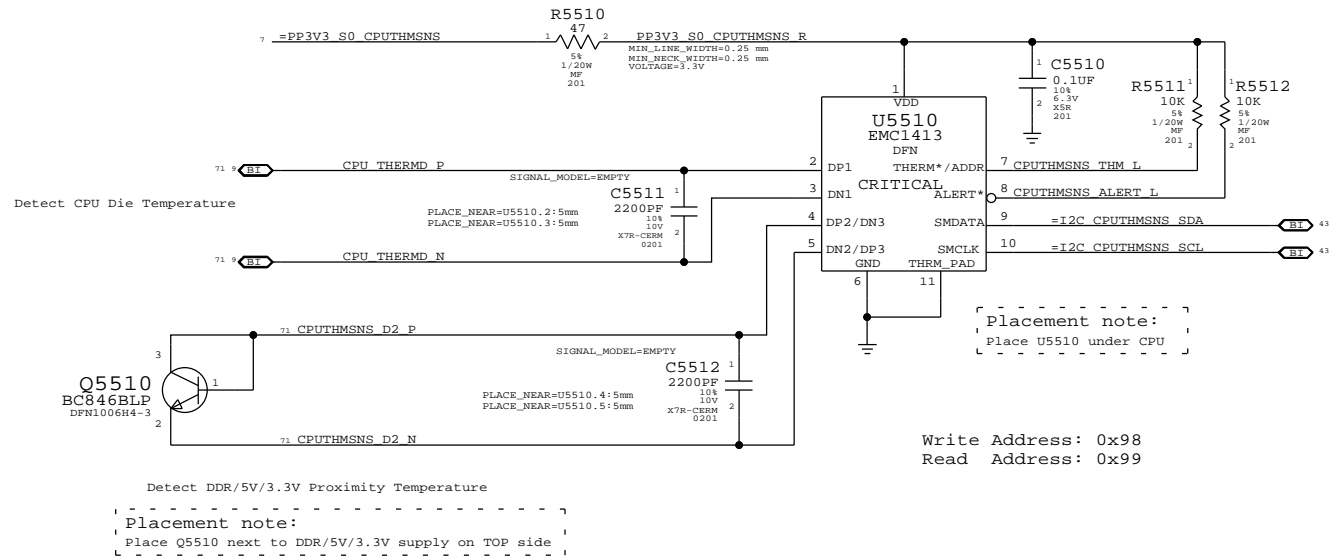
A

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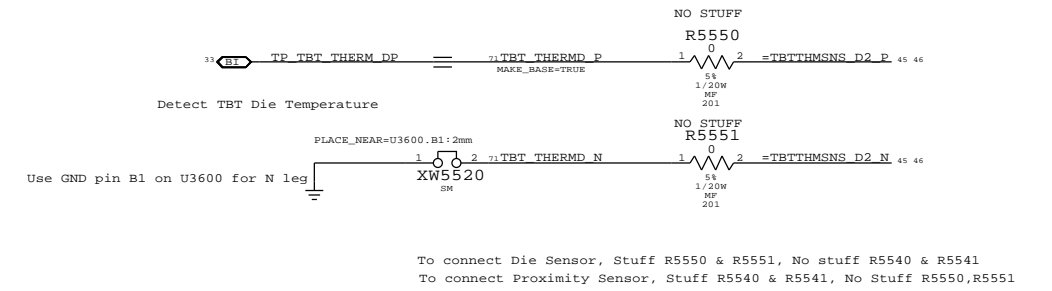


SMC PARTS=113.MBR		SYMC DATE=09/15/2011	
High Side Current Sensing			
Apple Inc.		DRAWING NUMBER	SIZE
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CPU Proximity Sensor



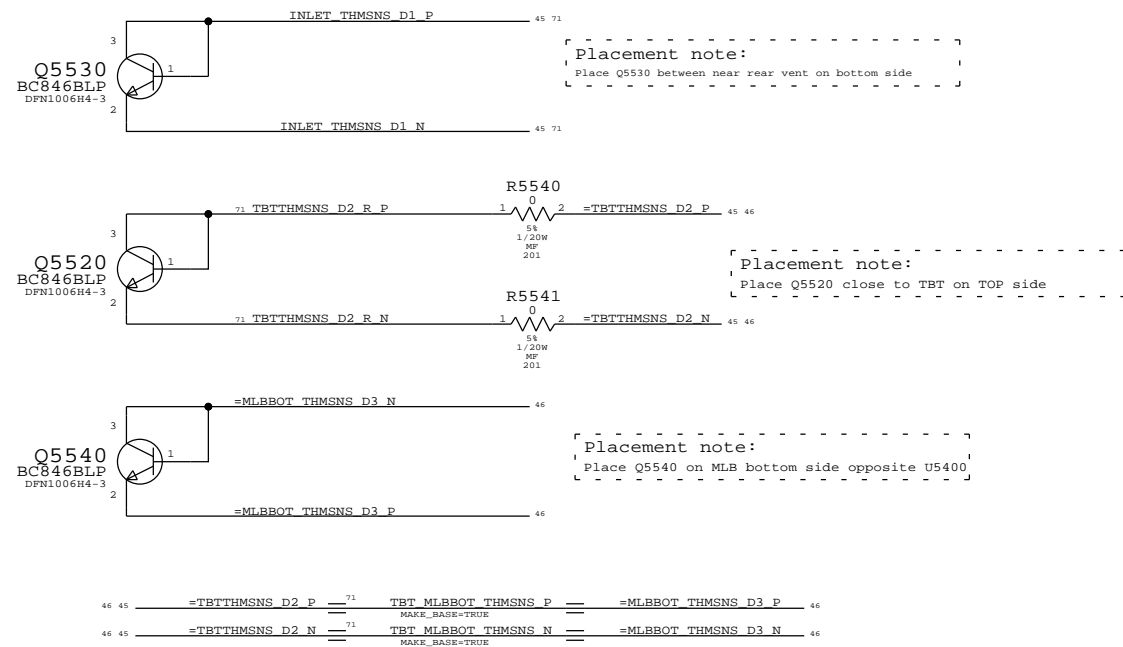
TBT Die



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5485		HDDISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5495		LCDBKLTISNS_PROD

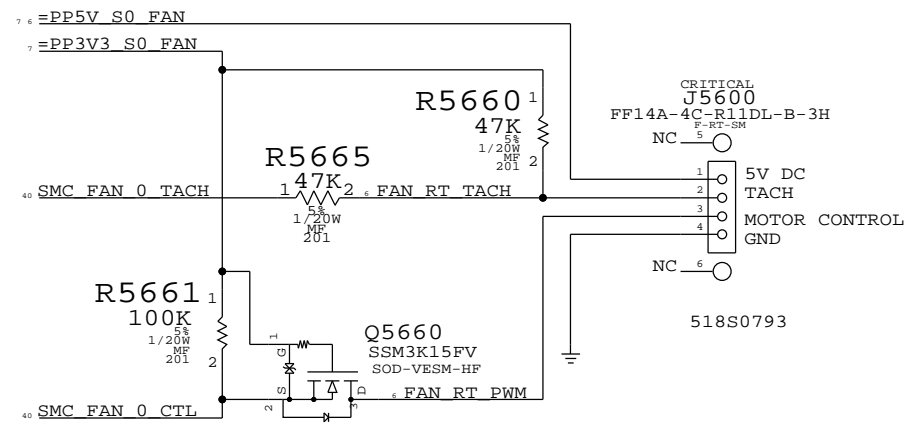
Replacing caps with 100K PD on ISENSE SMC inputs

TBT, MLB Bottom & Inlet Proximity Sensors



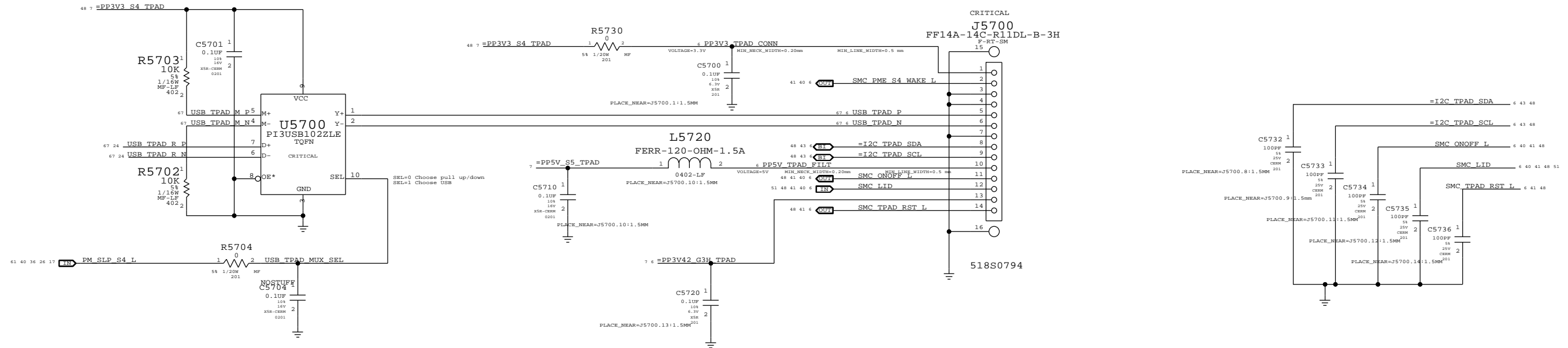
SYNC MASTER=113_MLB		SYNC DATE=08/30/2011	
PAGE TITLE Thermal Sensors			
DRAWING NUMBER 051-9276		SIZE D	
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FAN CONNECTOR

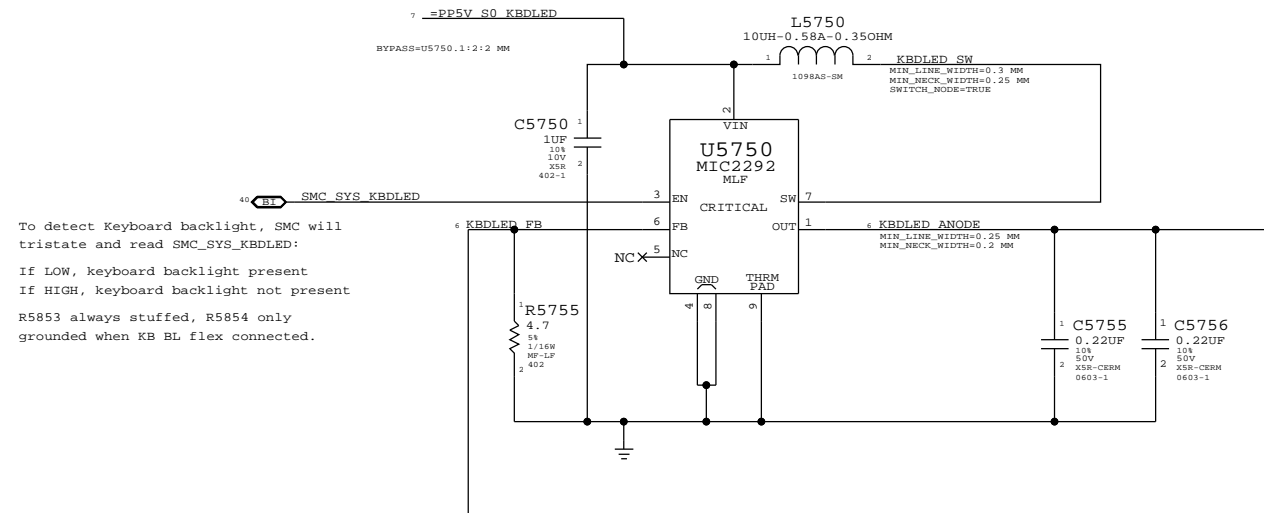


SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
Fan			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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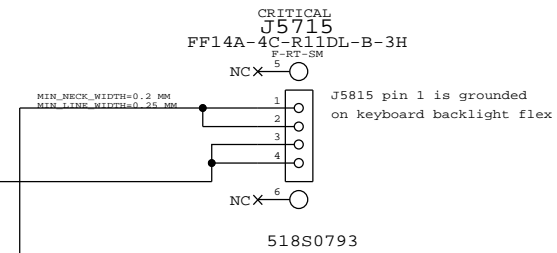
IPD Flex Connector



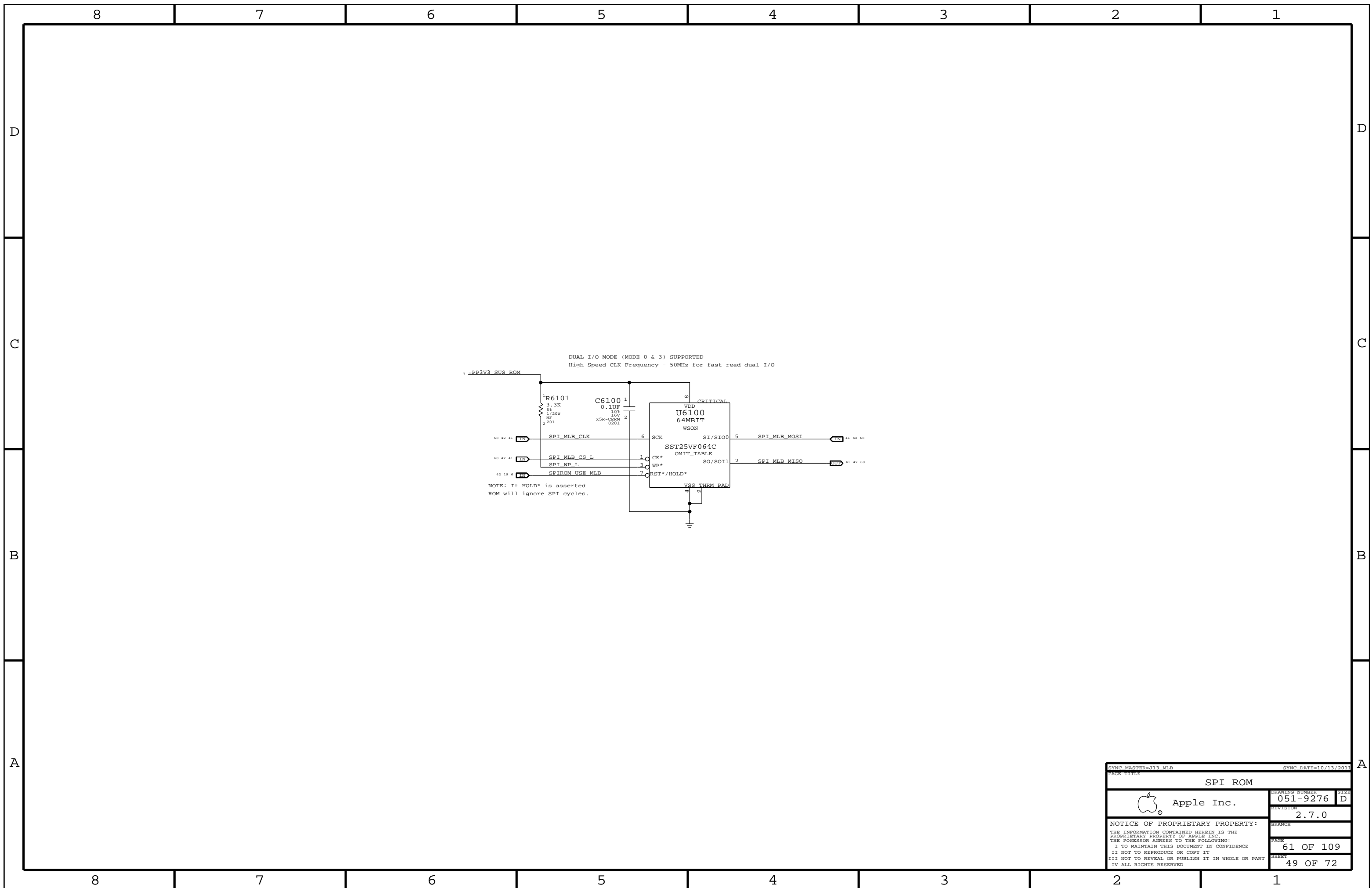
Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
IPD / KBD Backlight		DRAWING NUMBER	SIZE
Apple Inc.		051-9276	D
REVISION		2.7.0	
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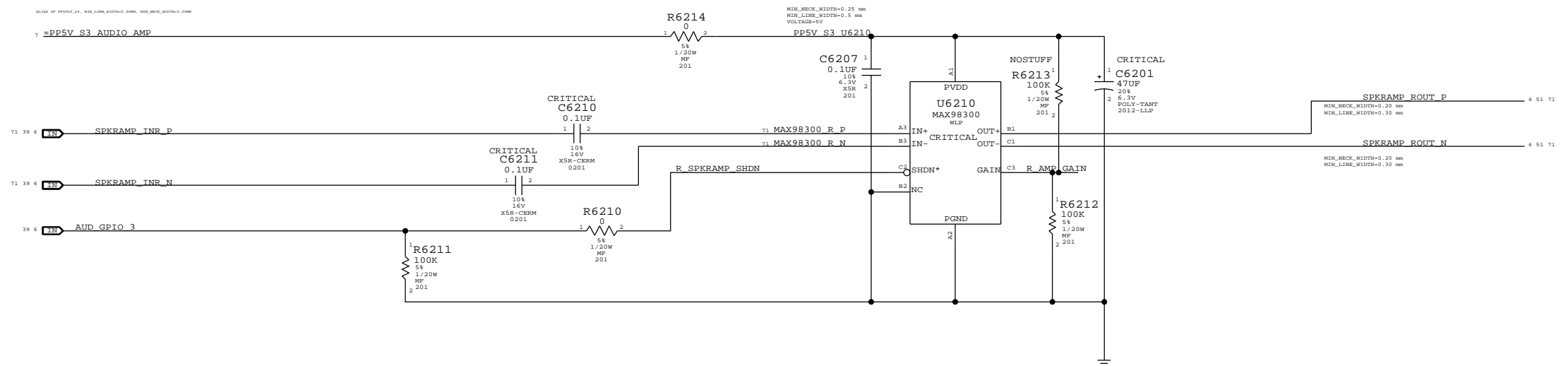
SYNC MASTER=113_MLB		SYNC DATE=10/13/2011	
PAGE TITLE SPI ROM			
DRAWING NUMBER 051-9276		SIZE D	
REVISION 2.7.0		BRANCH	
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8 7 6 5 4 3 2 1

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ
GAIN 6DB



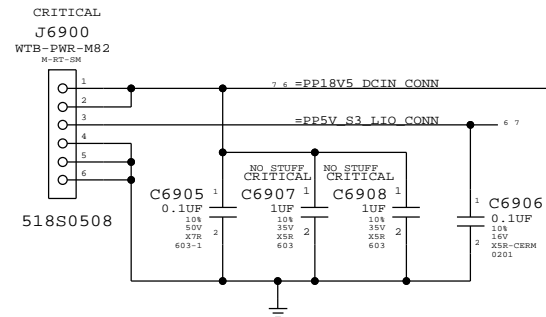
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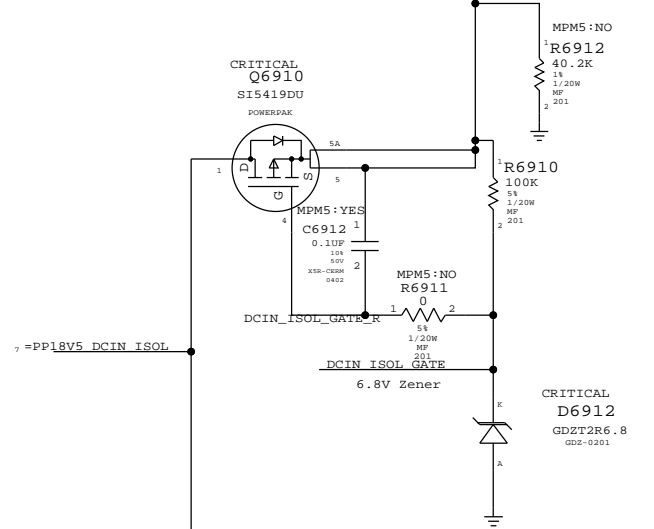
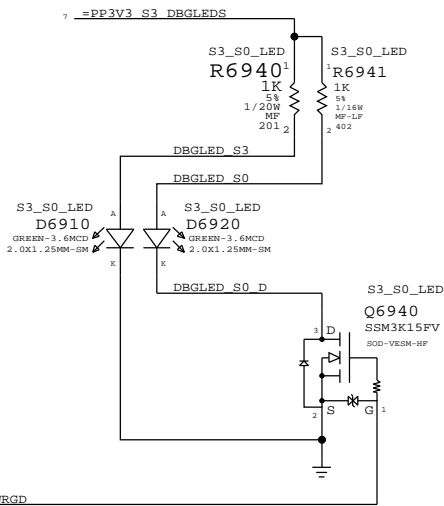
8 7 6 5 4 3 2 1

SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
PAGE TITLE AUDIO: SPEAKER AMP			
DRAWING NUMBER 051-9276		SIZE D	
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		SHEET 50 OF 72	

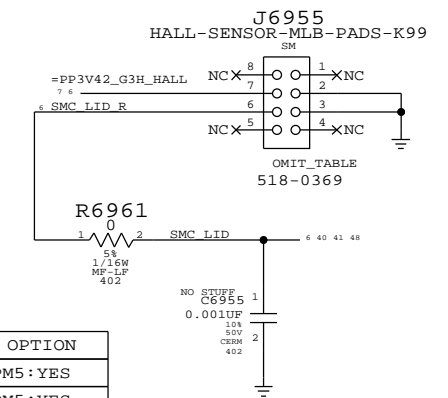
MLB to LIO Power Cable Connector



Debug LEDs
(For development only)

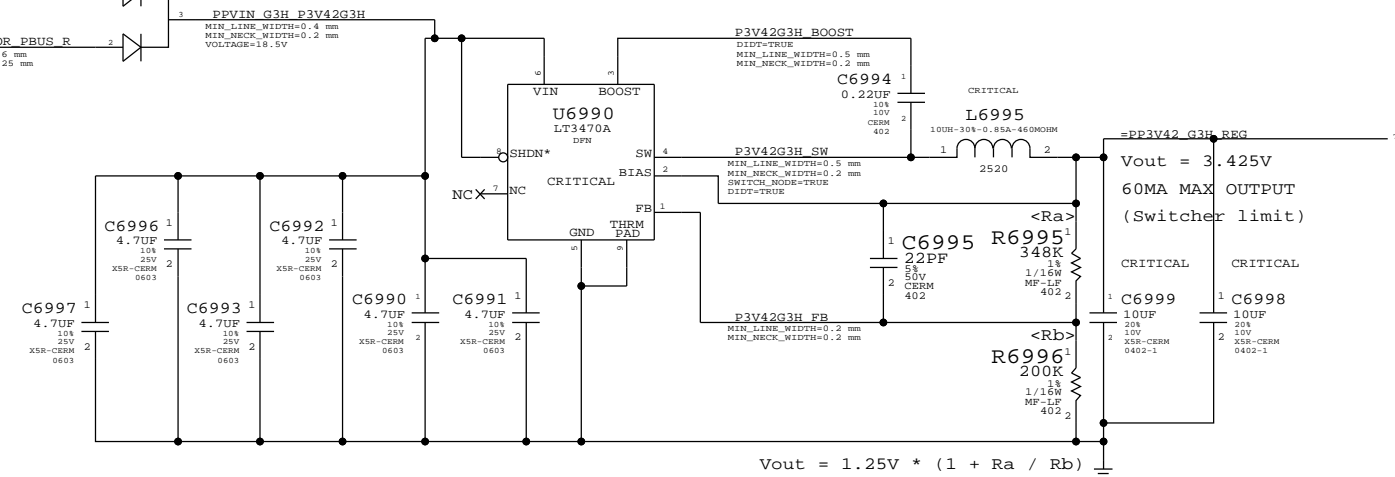


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES, MF, 90.9KOHM, 1, 1/20W, 0201	R6912	CRITICAL	MPM5: YES
117S0008	1	RES, MF, 100KOHM, 1, 1/20W, 0201	R6911	CRITICAL	MPM5: YES

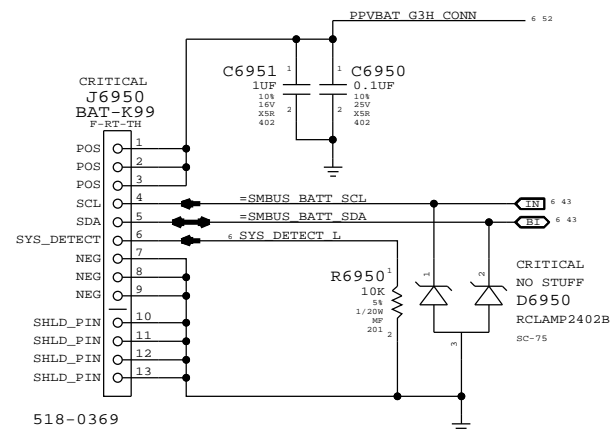


3.425V "G3Hot" Supply

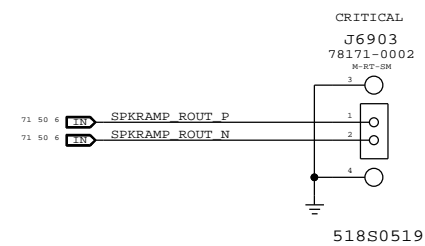
Supply needs to guarantee 3.31V delivered to SMC Vref generator



K99-Specific
Battery Connector



Right Speaker Connector



DC-In & Battery Connectors

Apple Inc.

051-9276

2.7.0

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Need to stuff R7092 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!

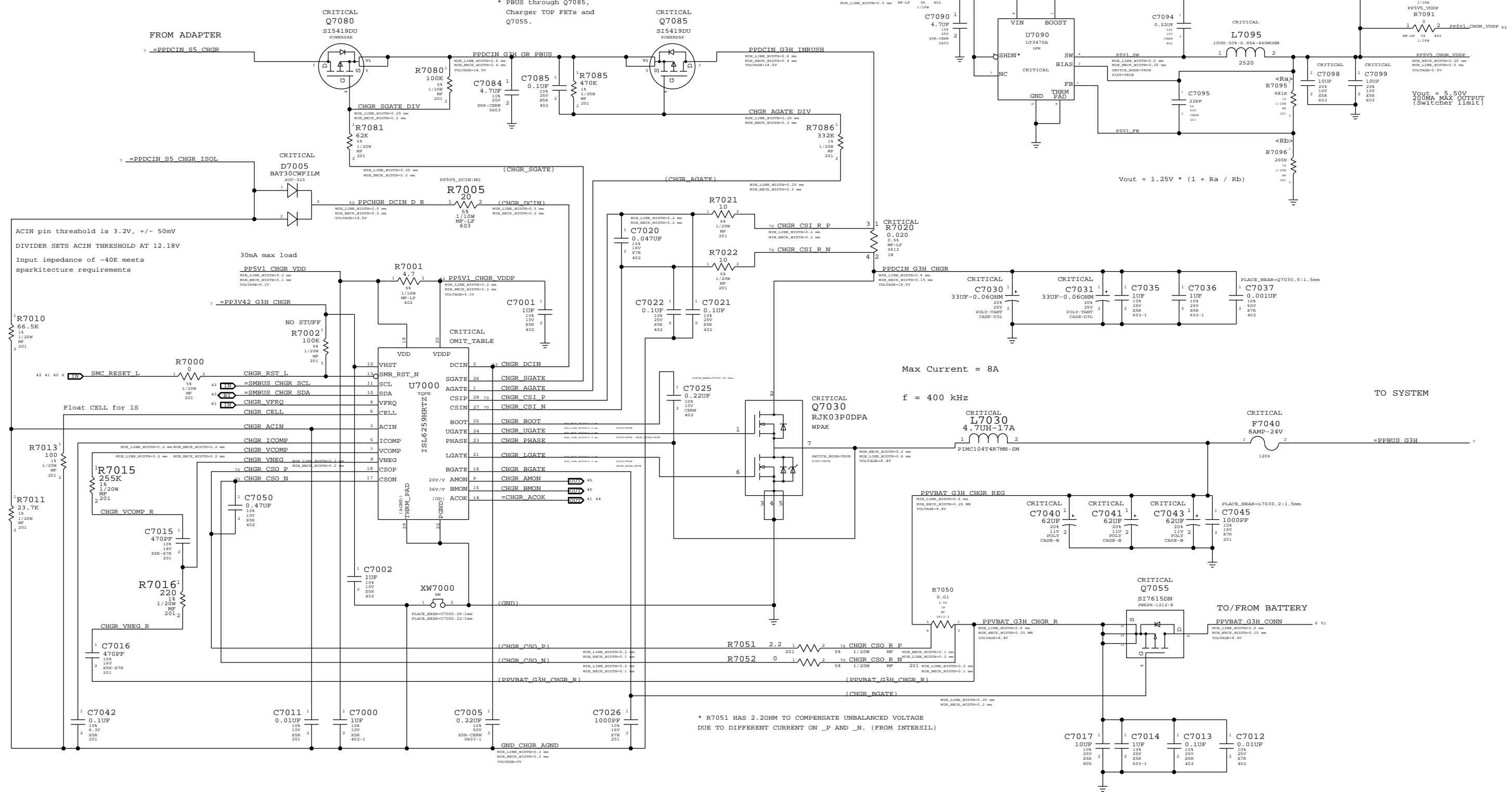
Reverse-Current Protection

This node is powered through body diodes:
 * DCIN through Q7080.
 * FBUS through Q7085,
 Charger TOP FETs and Q7055.

Inrush Limiter

5.5v "G3Hot" Supply
 For Exp Lot6 spec

PP5V5_DCIN:YES

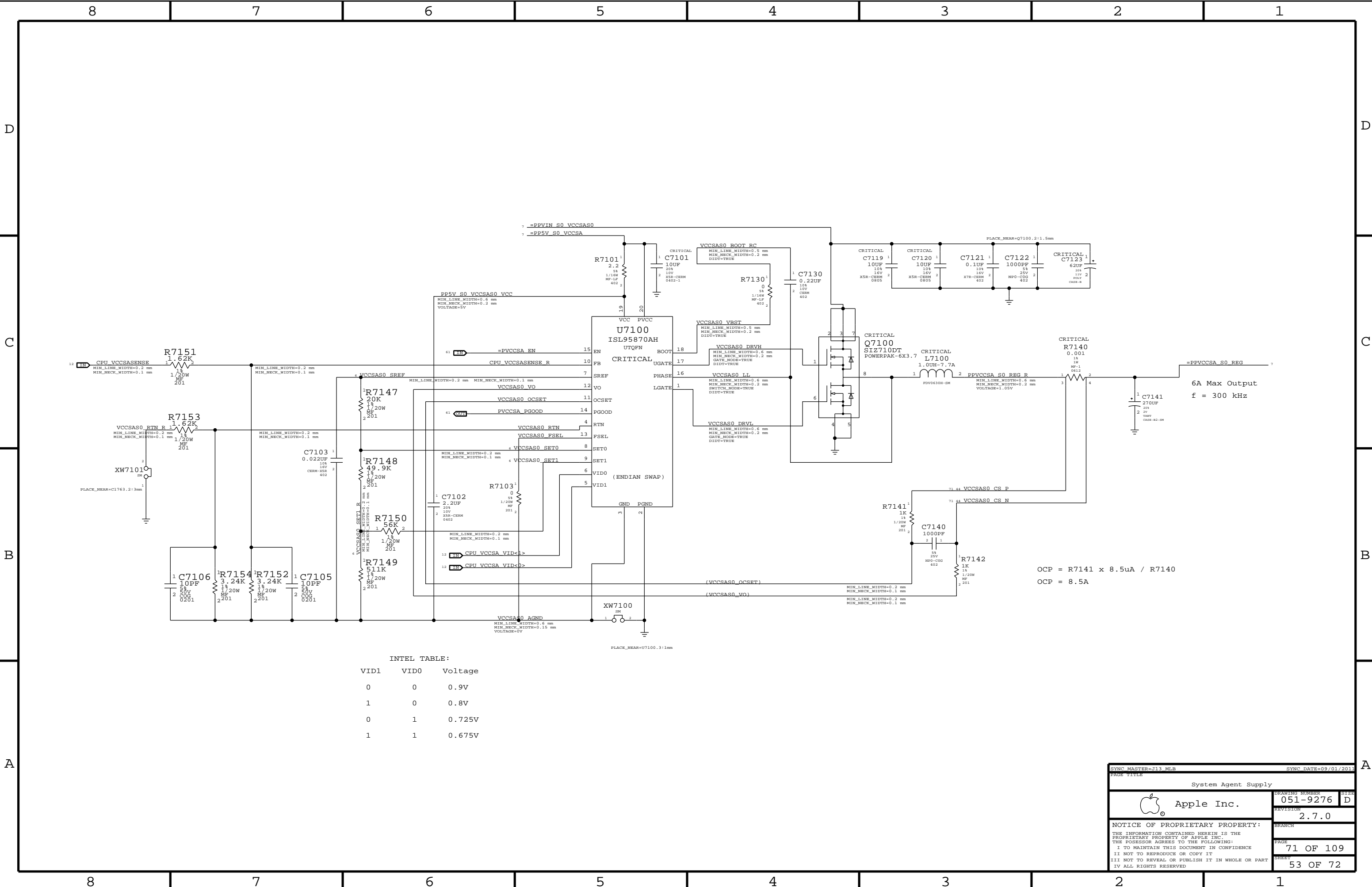


Max Current = 8A

f = 400 kHz

* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

SYNC MASTER=113 MLB		SYNC DATE=10/10/2011	
PAGE TITLE			
PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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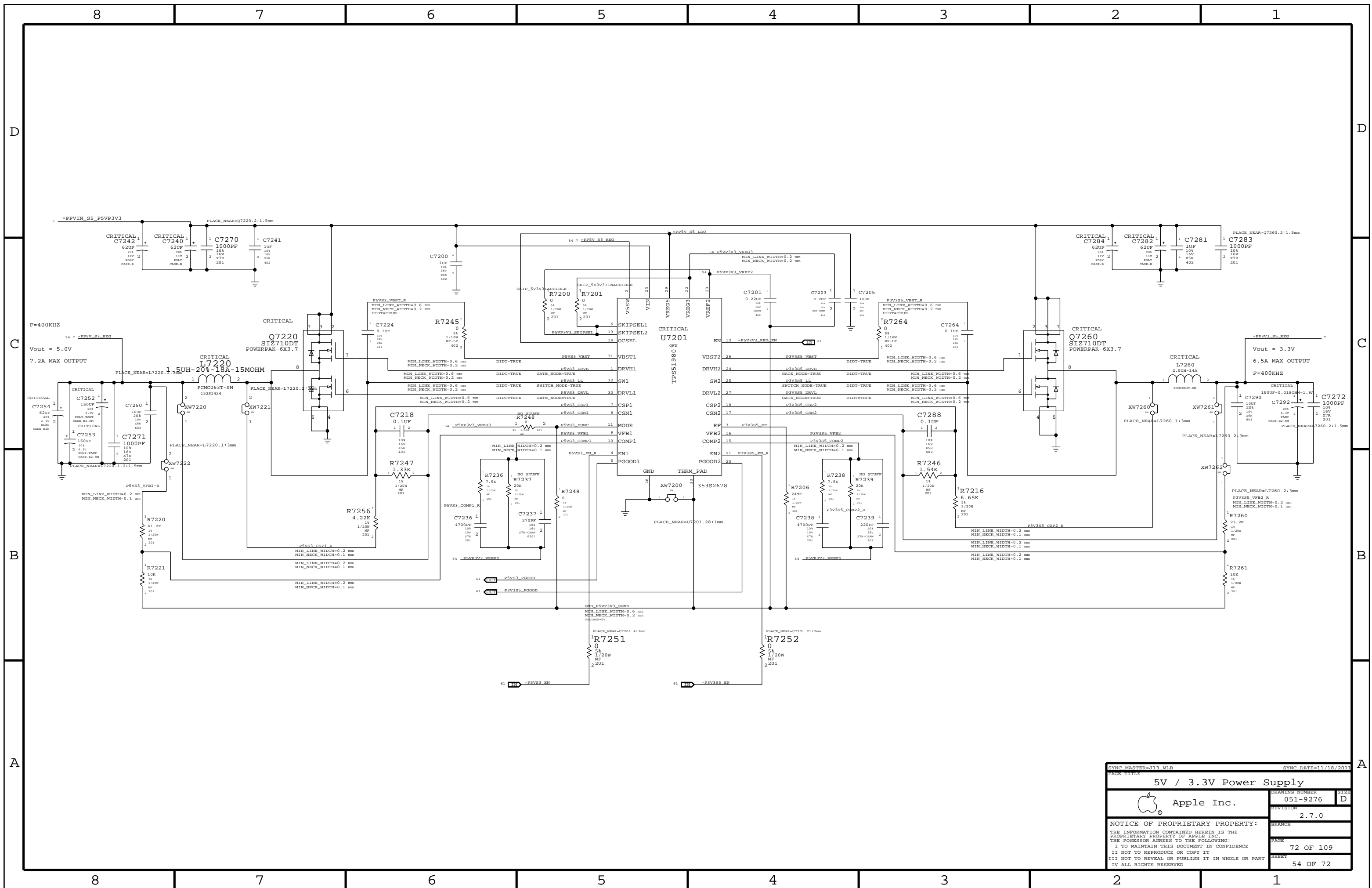


INTEL TABLE:

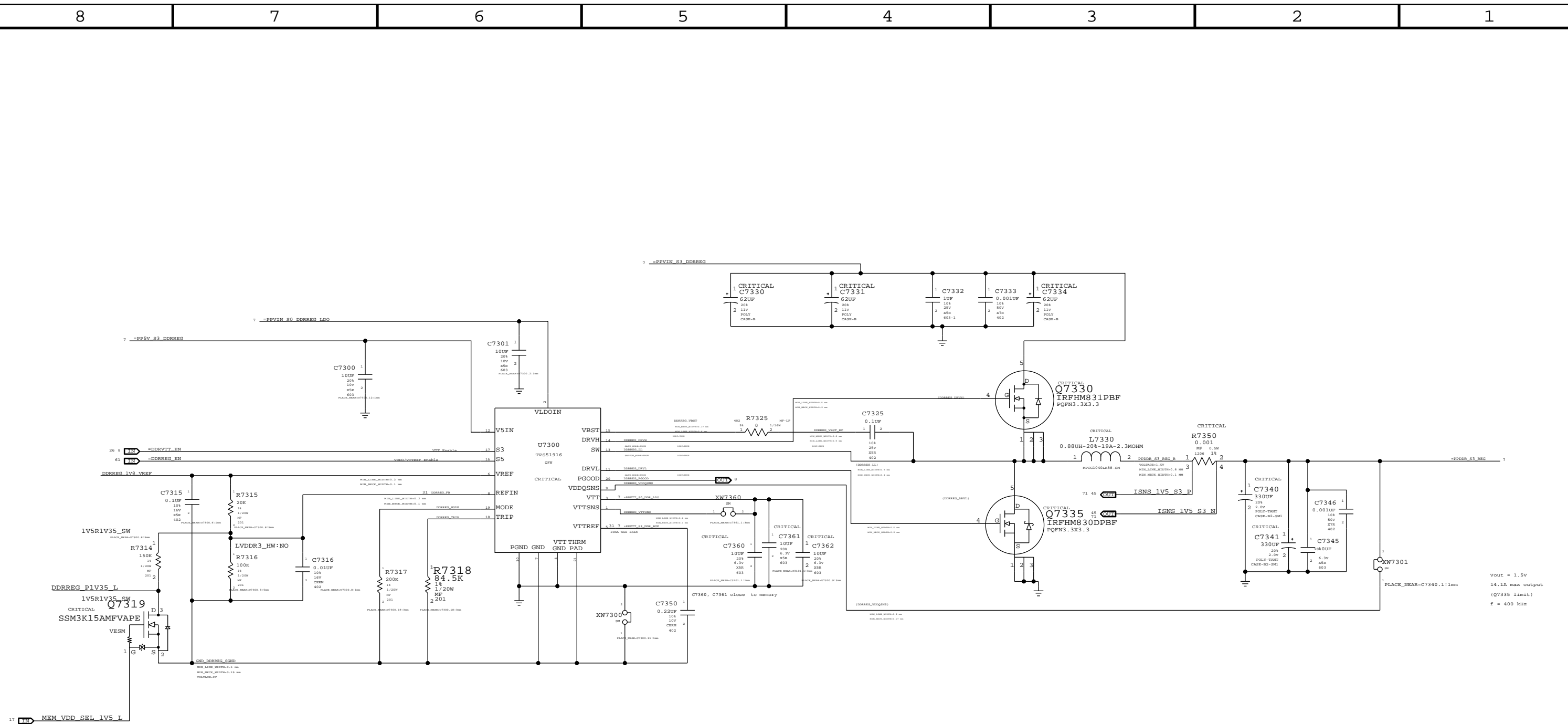
VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

$OCP = R7141 \times 8.5\mu A / R7140$
 $OCP = 8.5A$

SYNC MASTER=113 MLB		SYNC DATE=09/01/2011	
System Agent Supply			
Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
	REVISION	2.7.0	
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SYNC MASTER=113 MLB		SYNC DATE=11/18/2011	
PAGE TITLE			
5V / 3.3V Power Supply			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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		SHEET	54 OF 72
		SIZE	D



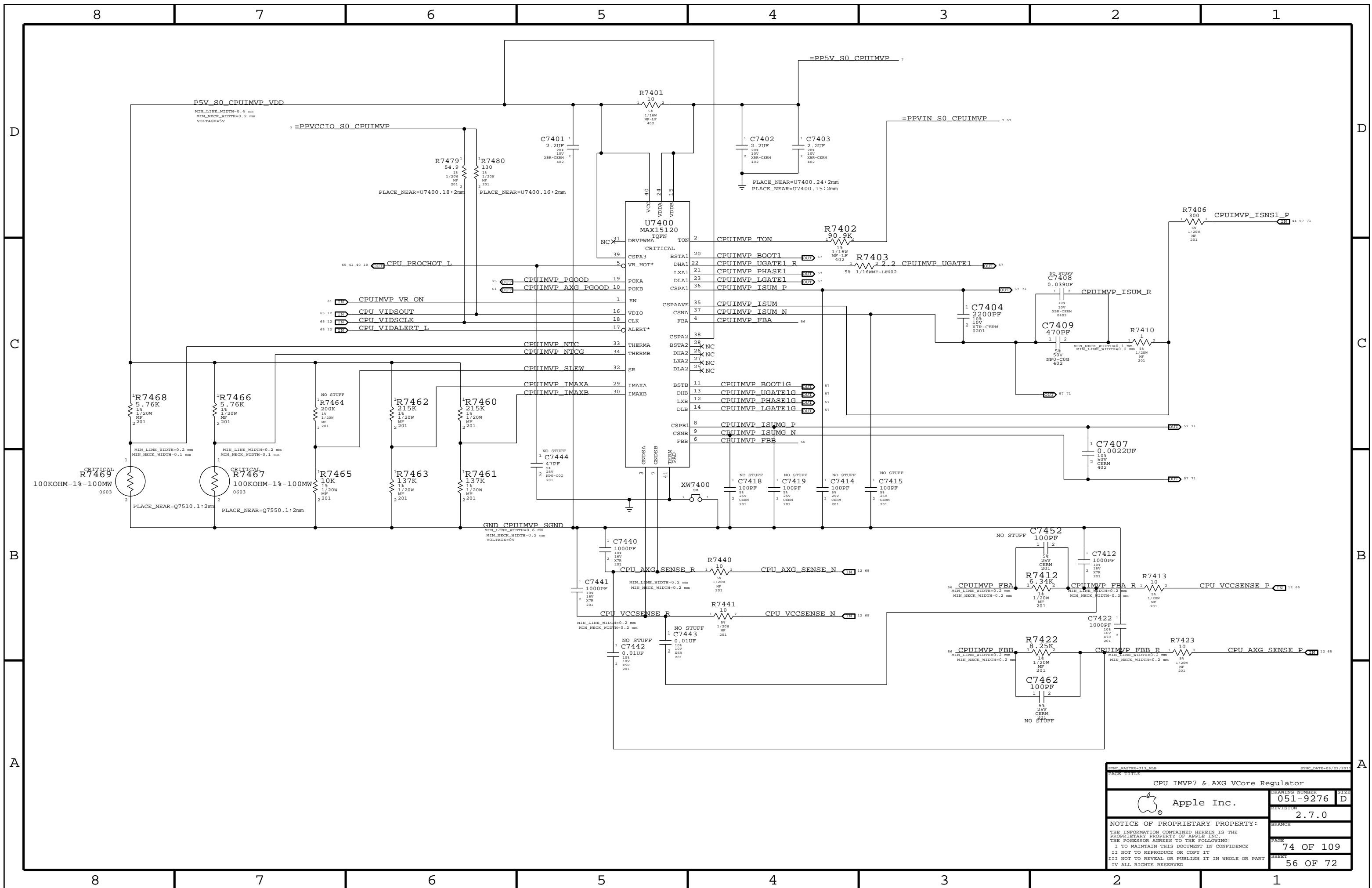
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES, MF, 60.4KOHM, 1.1/20W, 0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

DRAWING NUMBER		051-9276	SIZE	D
REVISION		2.7.0		
PAGE		73 OF 109		
SHEET		55 OF 72		

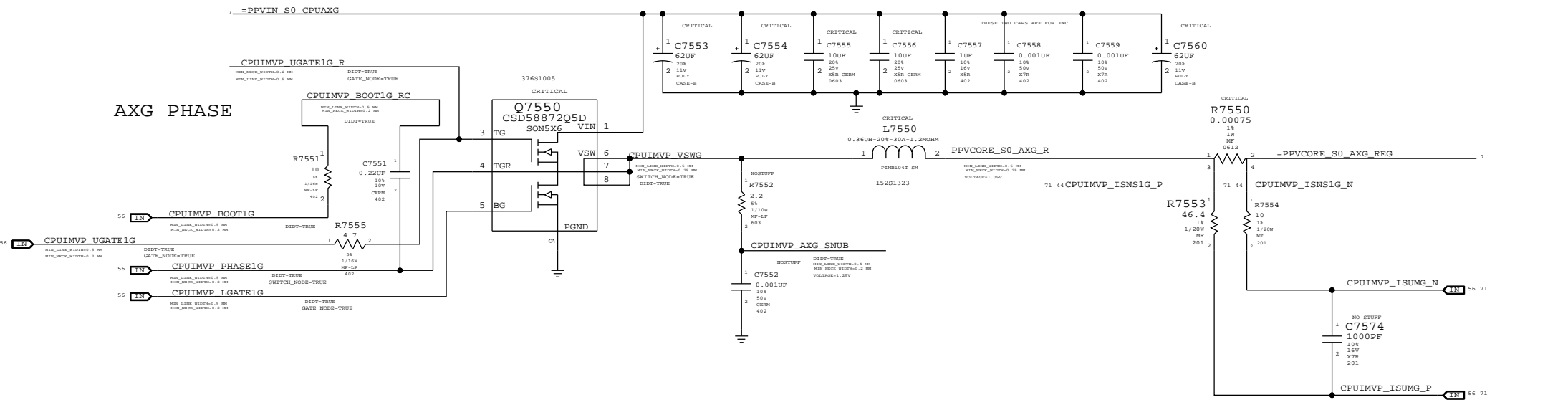
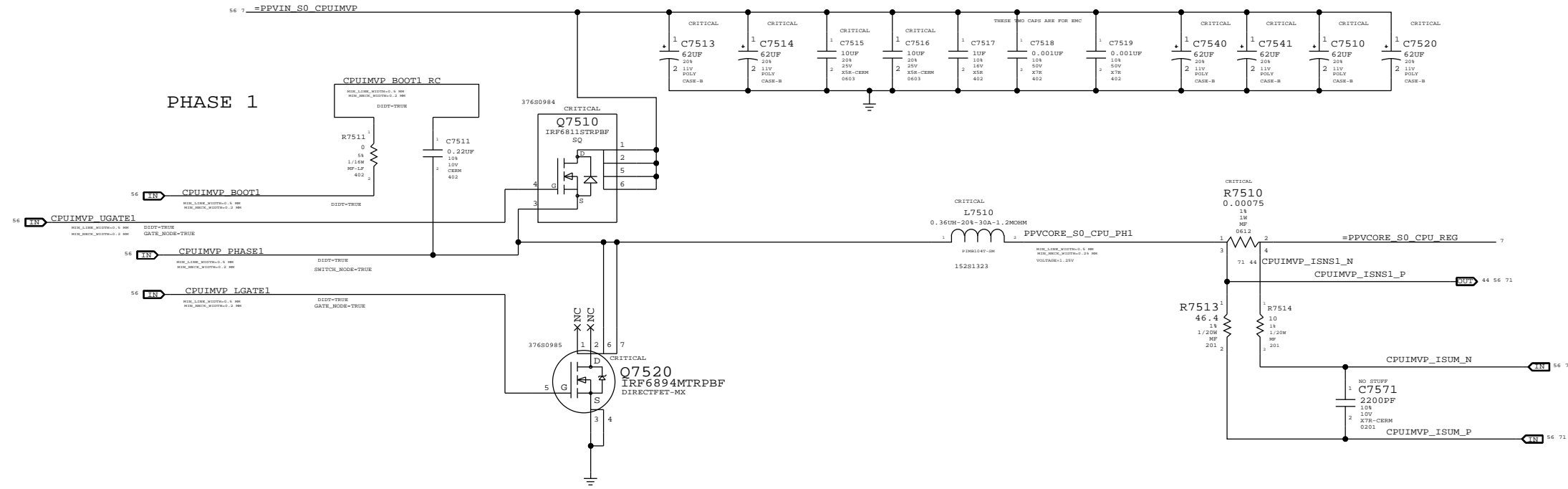
Apple Inc.

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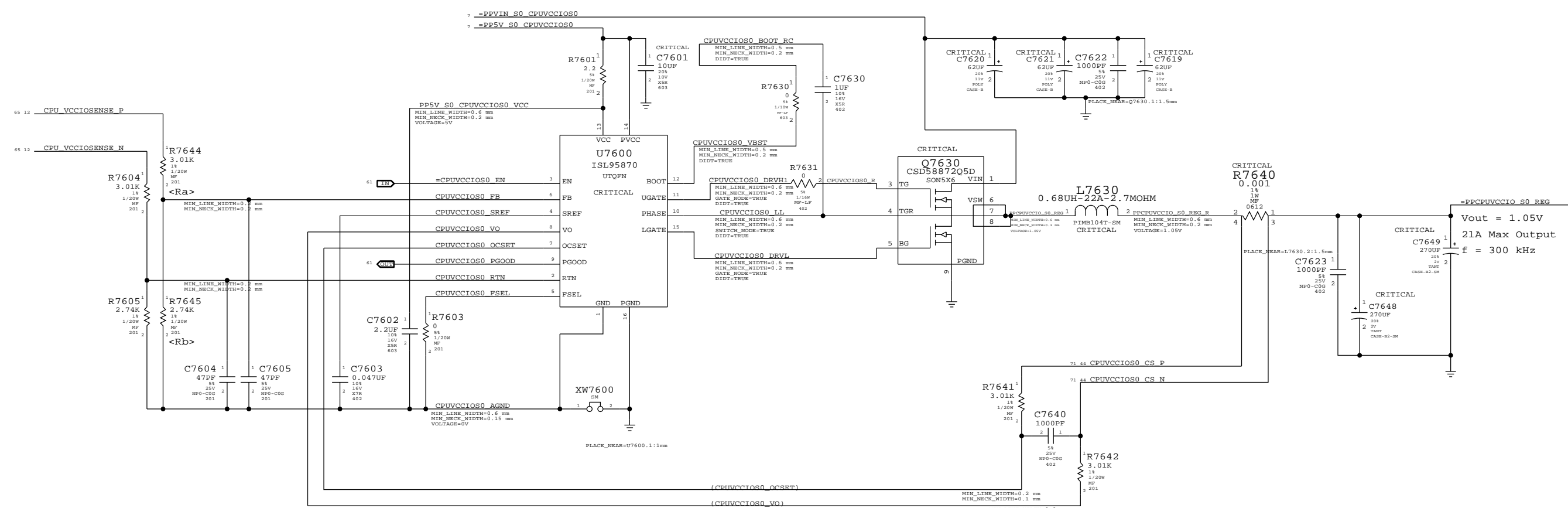
CPU IMVP7 & AXG VCore Regulator	
Apple Inc.	DRAWING NUMBER: 051-9276
REVISION: 2.7.0	SIZE: D
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CPU=IV Bridge ULV, AXG=GT2



CPU IMPV7 & AXG VCore Output		
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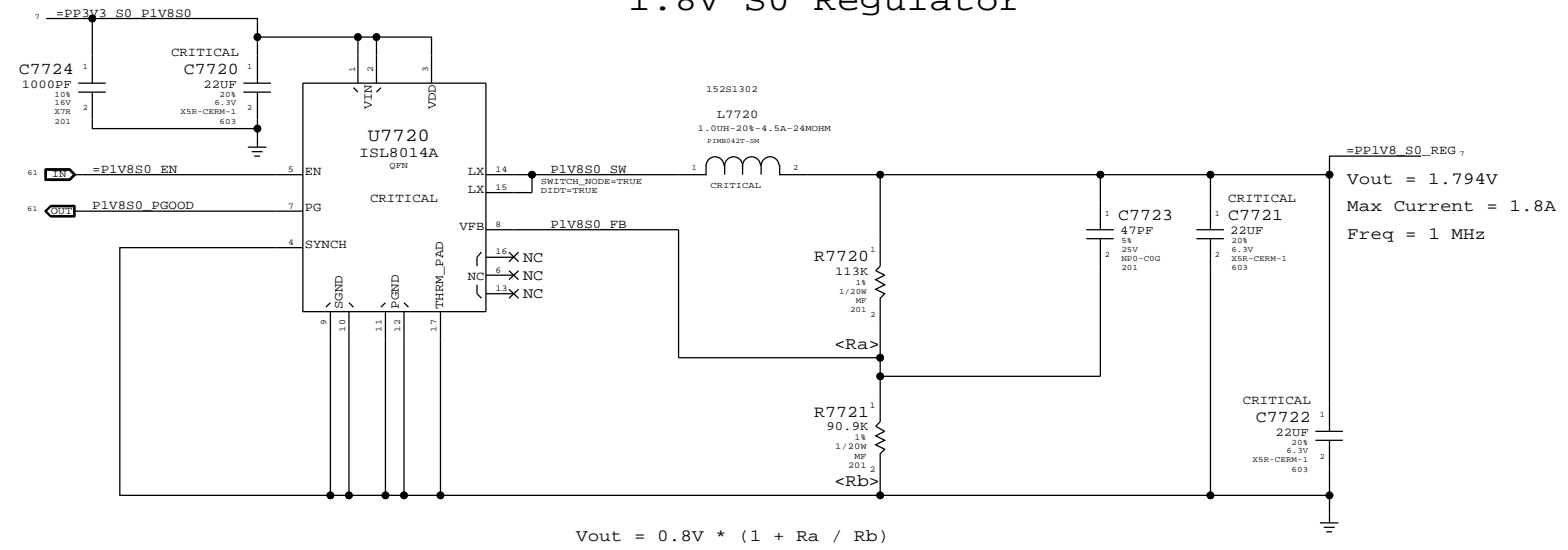
CPU VCCIO (1.05V S0) Regulator



$OCP = R7641 \times 8.5\mu A / R7640$
 $OCP = 25.6A$
 $V_{out} = 0.5V * (1 + R_a / R_b)$

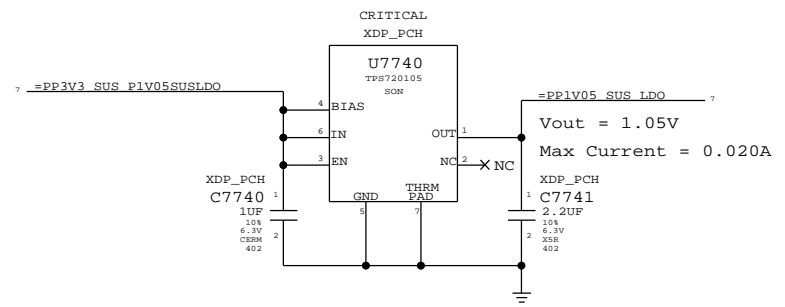
SYMC MASTER=113.MBR		SYMC_DATE=09/01/2015	
PAGE TITLE			
CPU VCCIO (1.05V) Power Supply			
Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
	REVISION	2.7.0	
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1.8V S0 Regulator

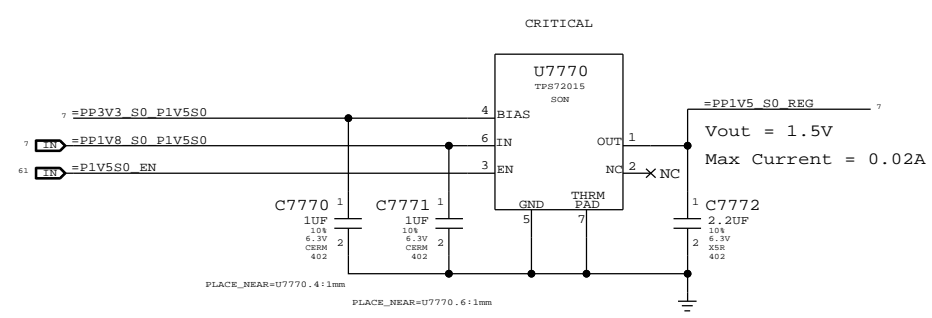


1.05V SUS LDO

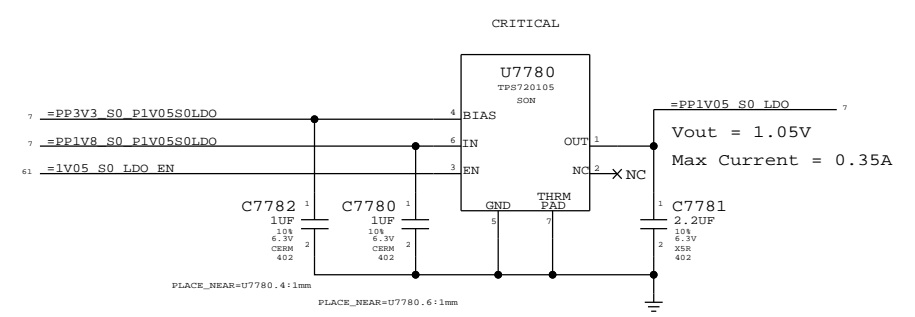
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



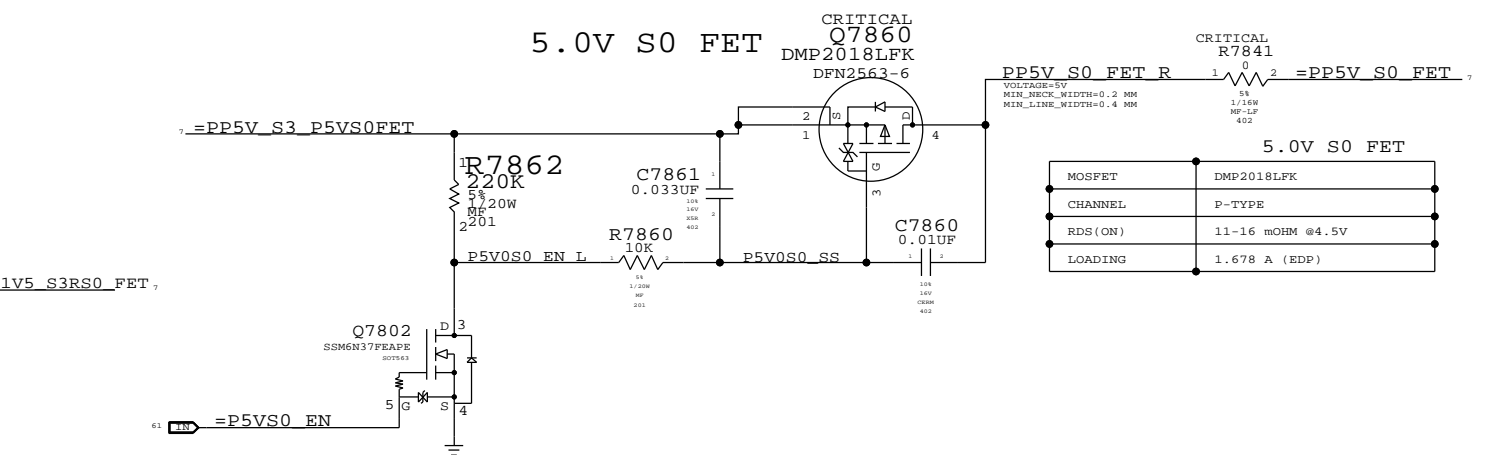
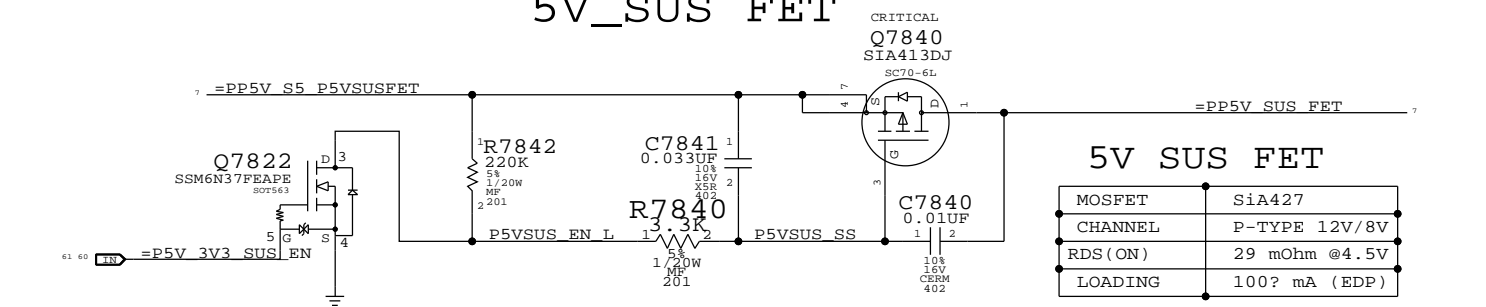
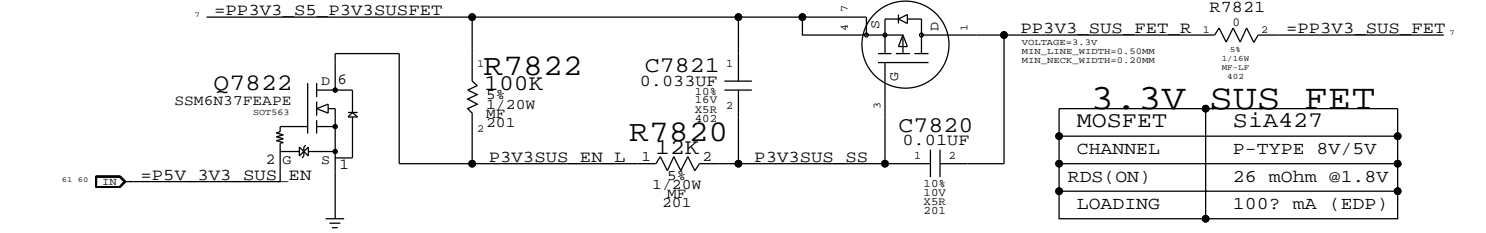
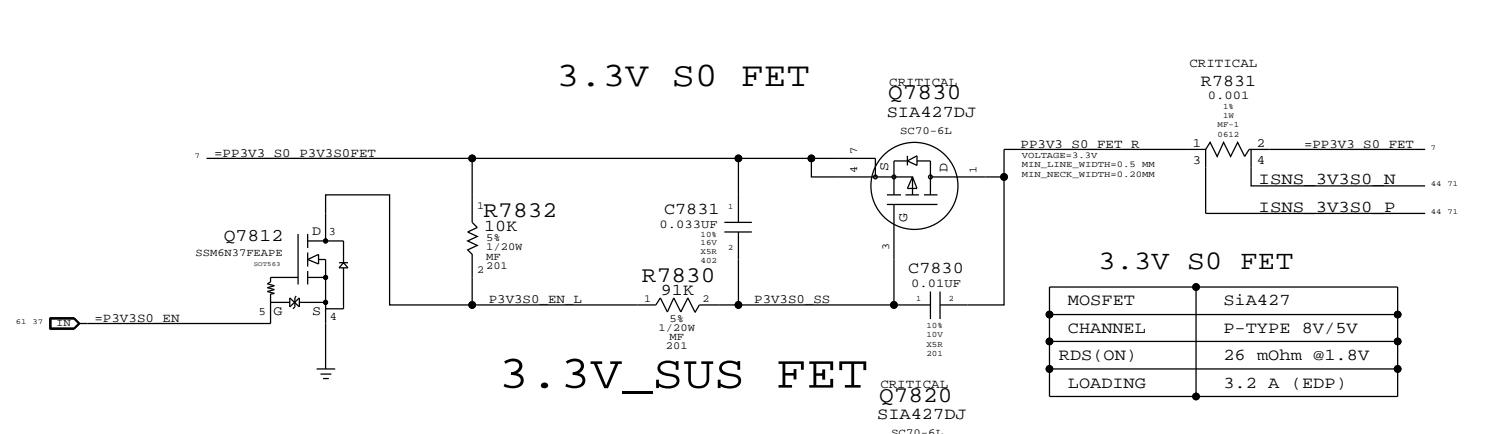
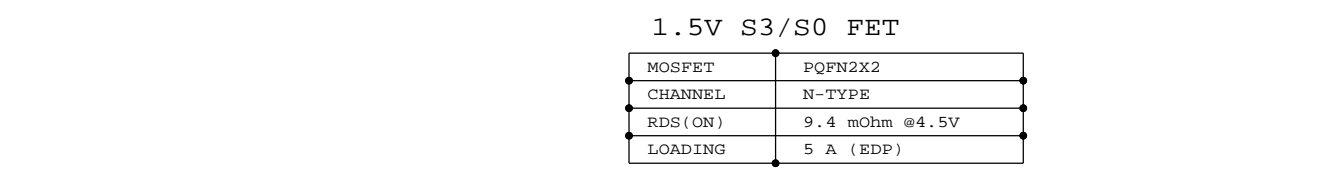
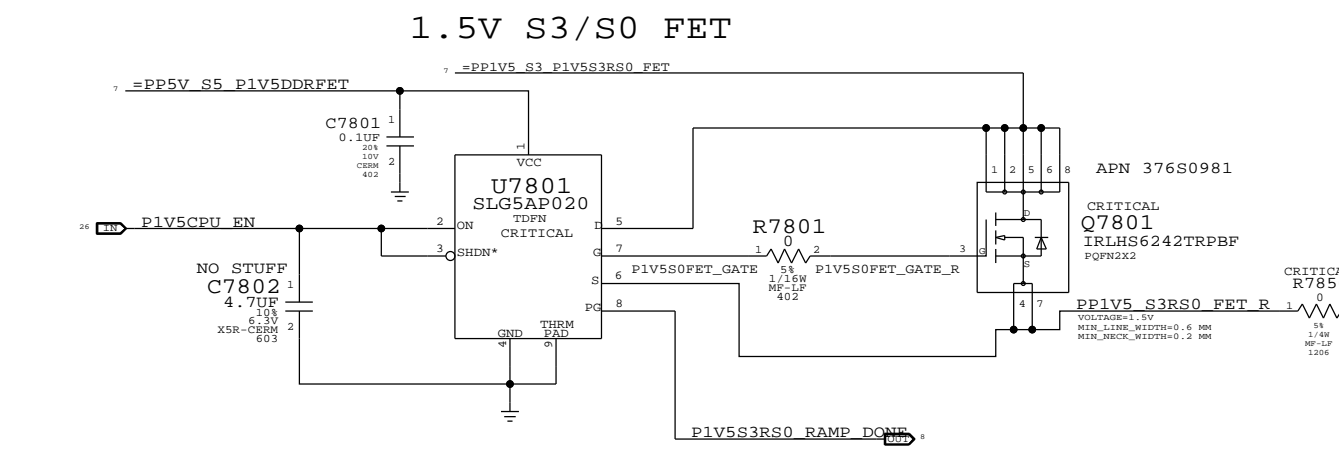
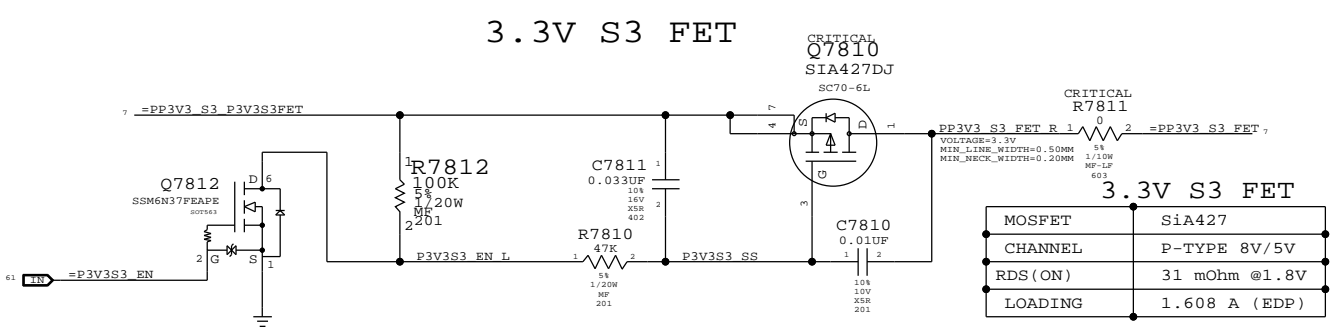
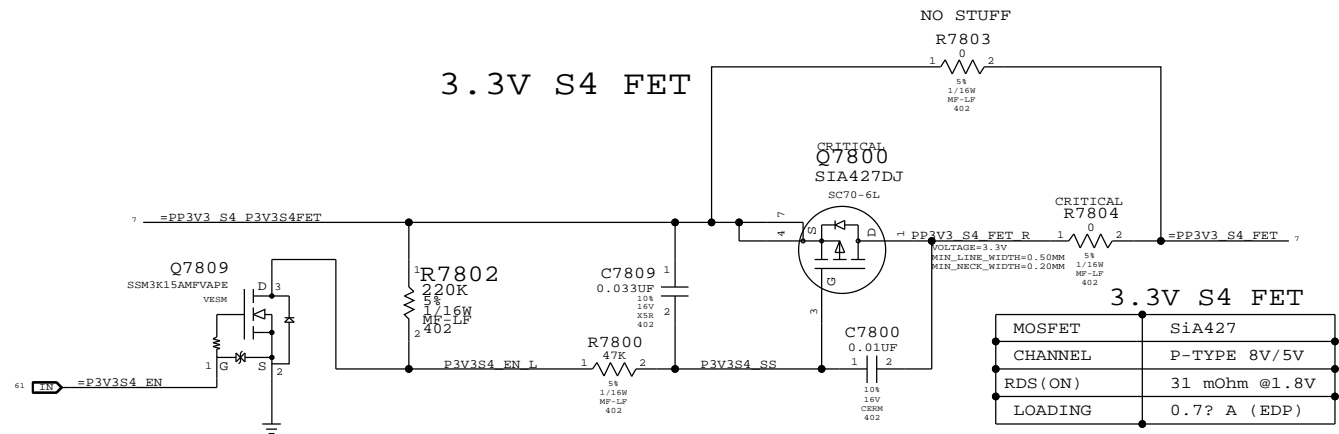
1.5V S0 LDO



1.05V S0 LDO



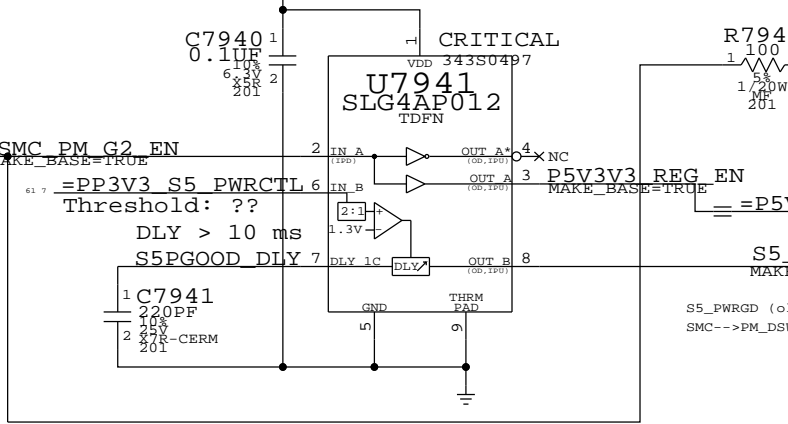
SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
PAGE TITLE			
Misc Power Supplies		DRAWING NUMBER	SIZE
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SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
Power FETs			
Apple Inc.		DRAWING NUMBER	051-9276
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S5 Rail Enables & PGOOD

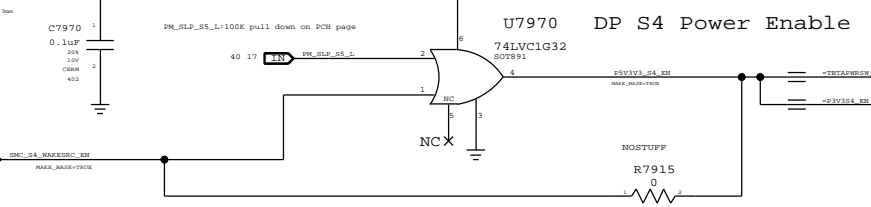
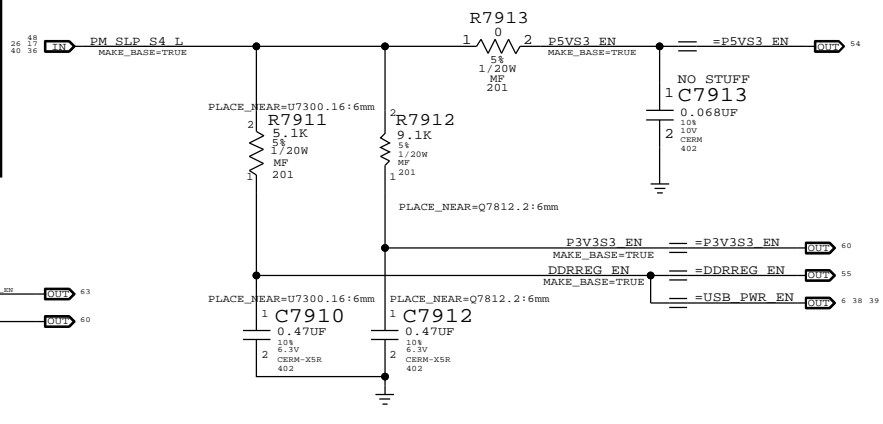
=PP3V42 G3H PWRCTL Internal pull-ups 100K +/- 20%



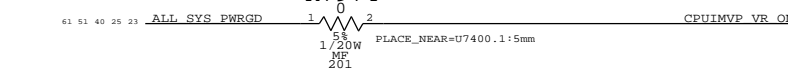
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKEG3C_EN	PM_S3S3_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S1_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Deep Sleep (S6)	0	1	0	0	0	0	0
Battery Off (S6Batt)	1	0	0	0	0	0	0
Battery Off (S6Batt)	1	0	0	0	0	0	0

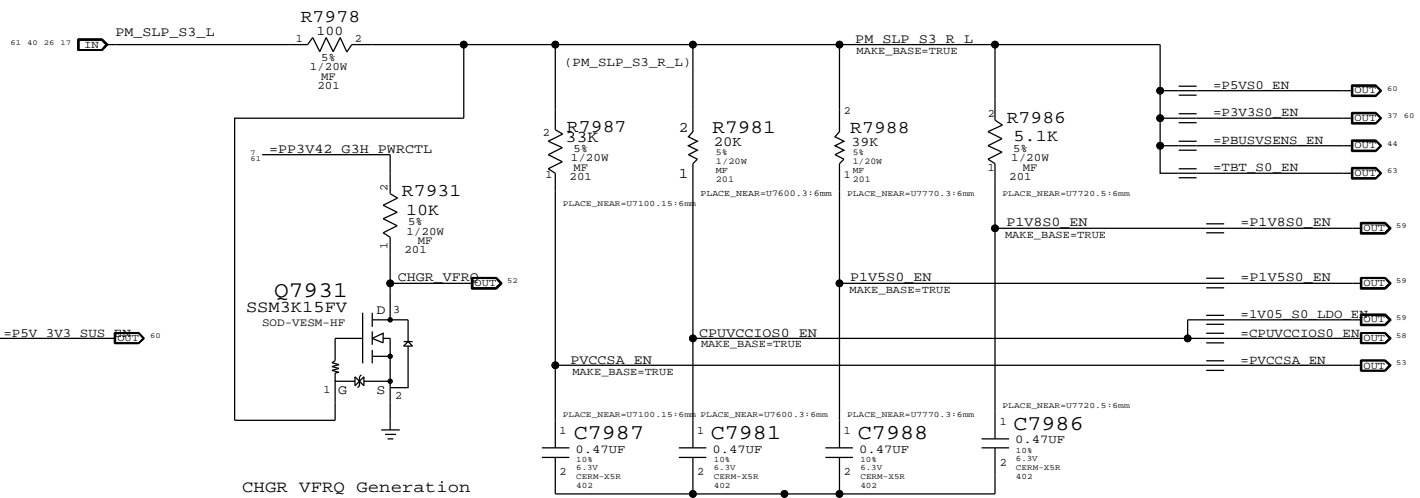
3.3V, 5V S3 ENABLE



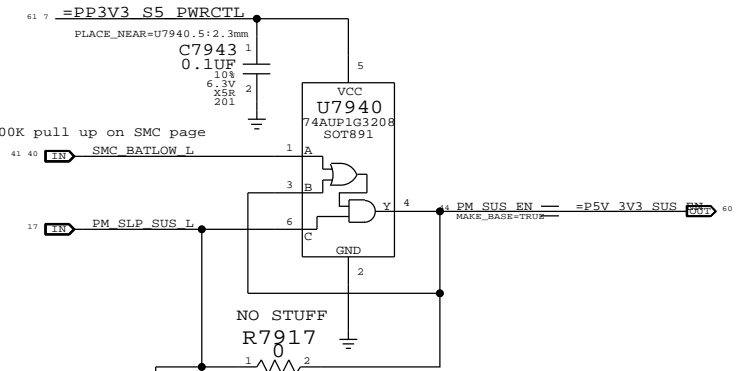
CPUVCORE ENABLE



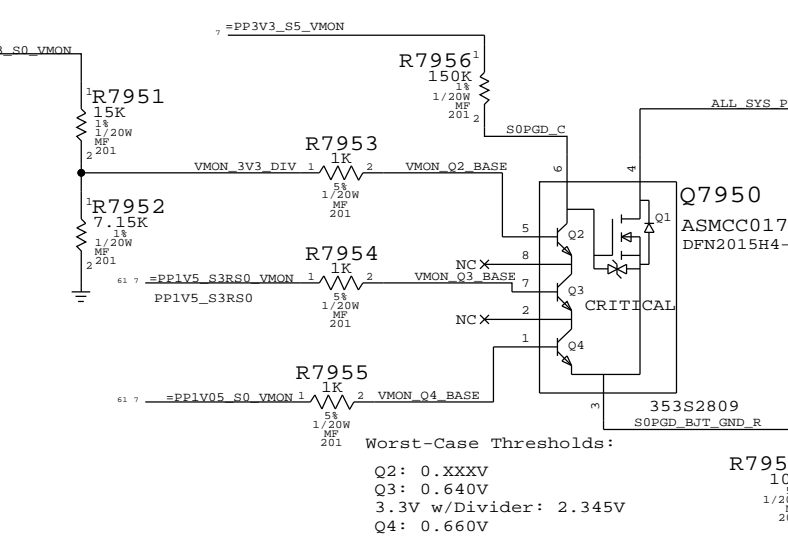
S0 ENABLE



3.3V/5.0V Sus ENABLE

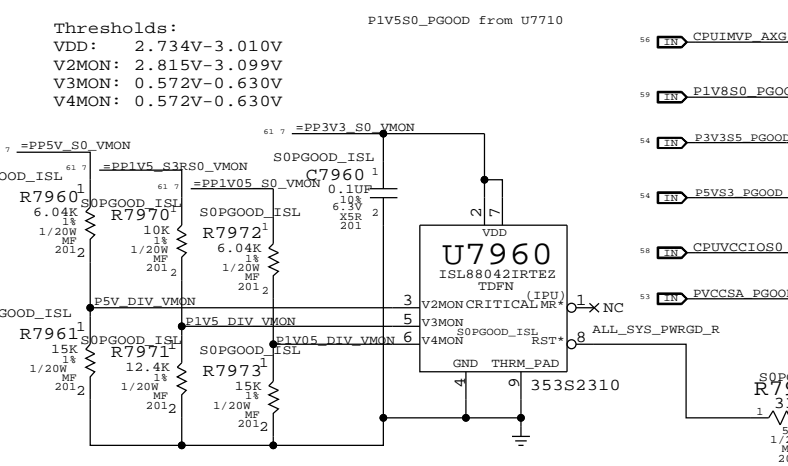


S0 Rail PGOOD (BJT Version)



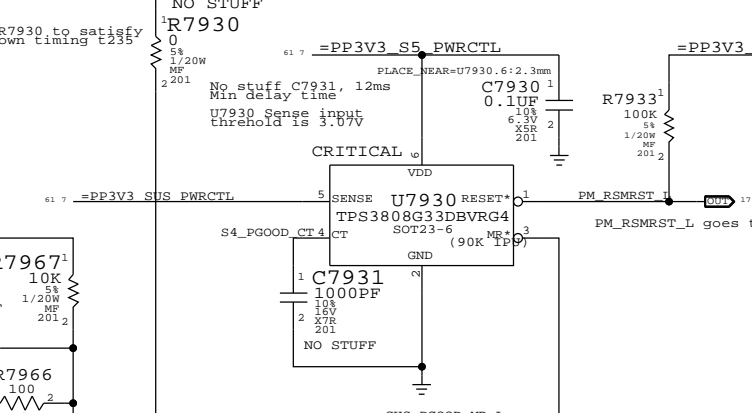
Worst-Case Thresholds:
 Q2: 0.XXXV
 Q3: 0.640V
 3.3V w/Divider: 2.345V
 Q4: 0.660V

S0 Rail PGOOD Circuitry (ISL Version in development)



Thresholds:
 VDD: 2.734V-3.010V
 V2MON: 2.815V-3.099V
 V3MON: 0.572V-0.630V
 V4MON: 0.572V-0.630V

3.3V SUS Detect



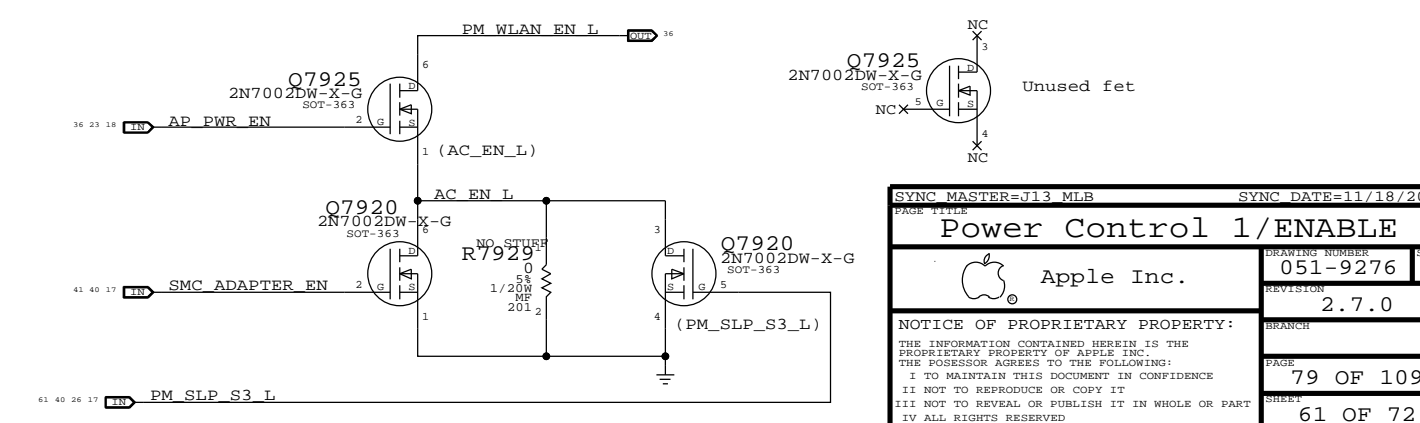
CHGR VFRQ Generation



VFRQ Low: Fix Frequency
 VFRQ High: Variable Frequency

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



SYNC MASTER=J13 MLB SYNC DATE=11/18/2011

Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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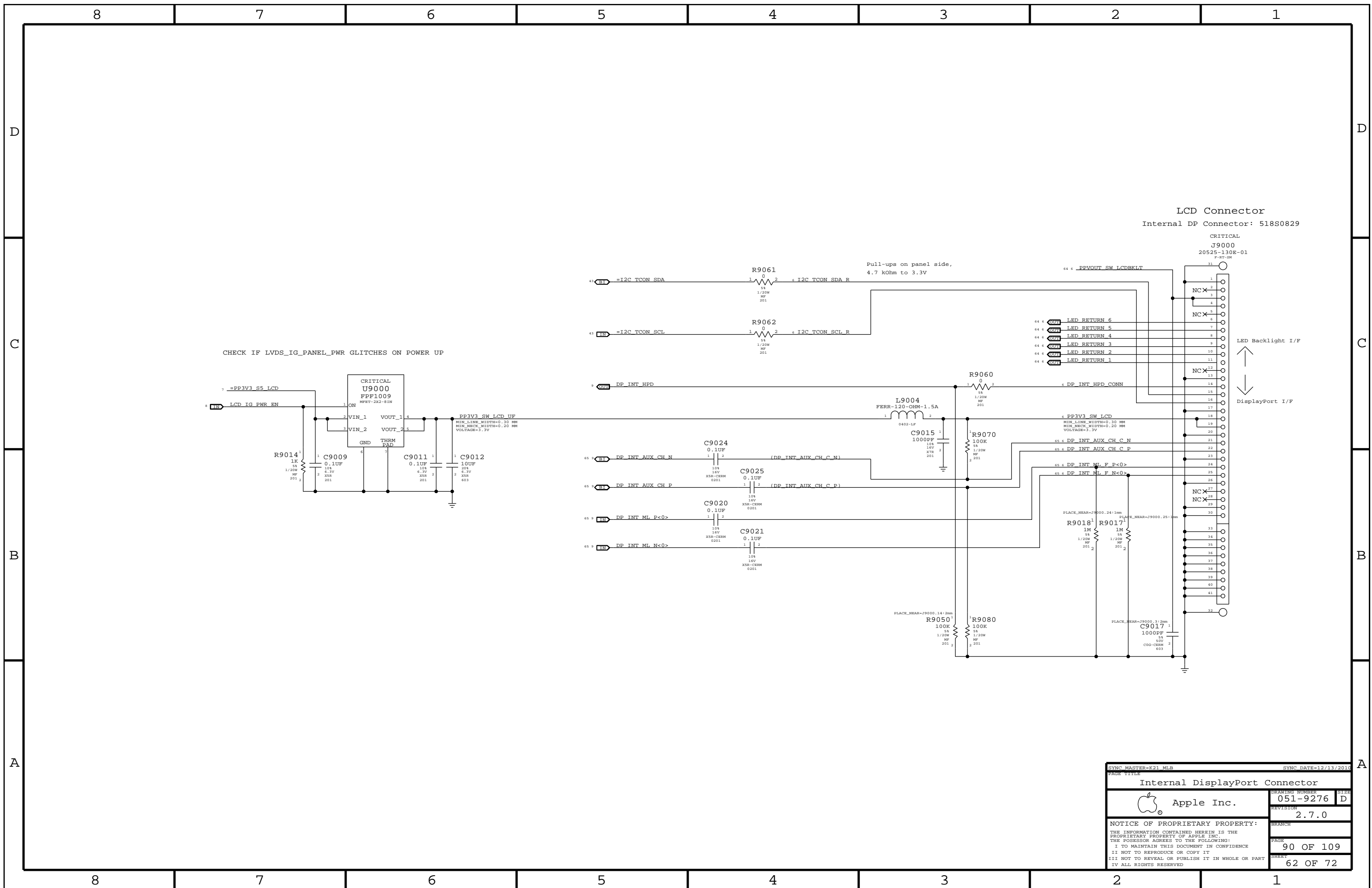
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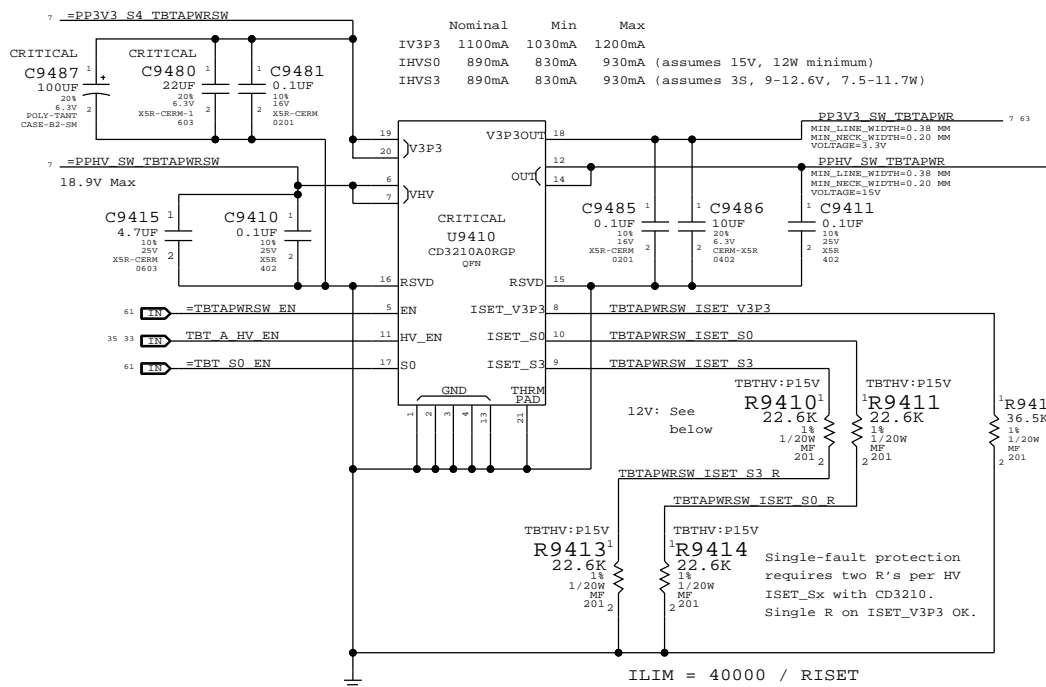
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SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
Internal DisplayPort Connector			
DRAWING NUMBER		051-9276	
REVISION		2.7.0	
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3.3V/HV Power MUX

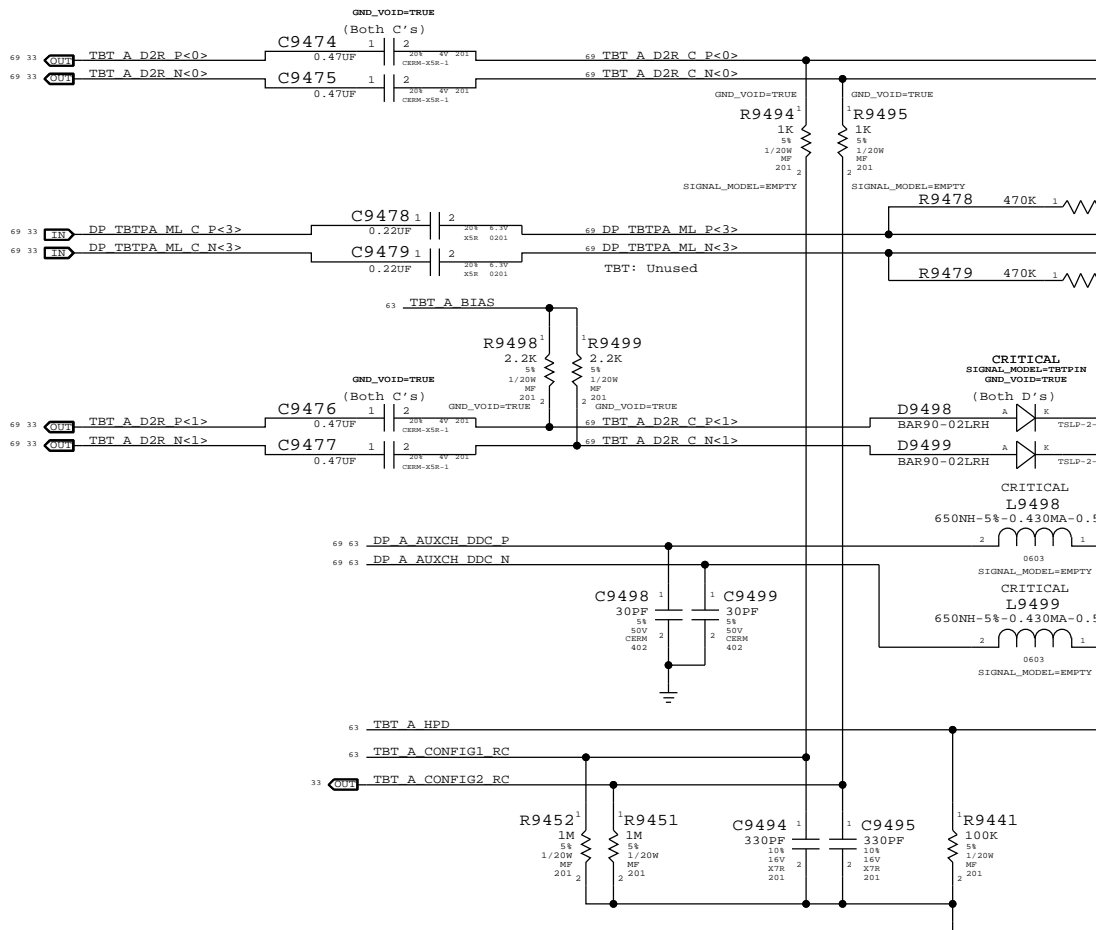
V3P3 must be S4 to support wake from Thunderbolt devices.



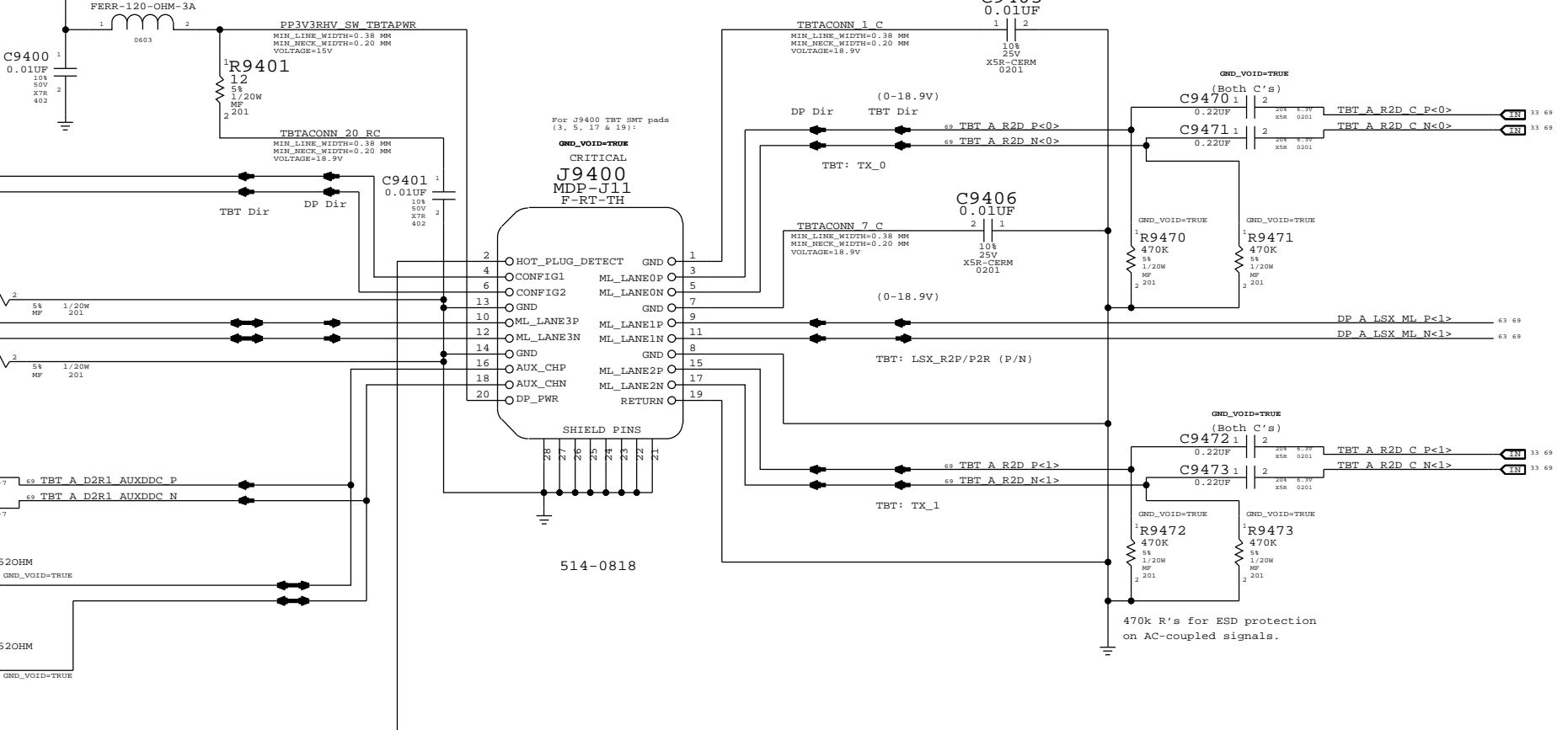
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	R9410, R9413	R9410, R9413		TBTHV:P12V
118S0145	2	R9411, R9414	R9411, R9414		TBTHV:P12V

	Nominal	Min	Max
IHV50/S3	1120mA	1090mA	1170mA (12W minimum)

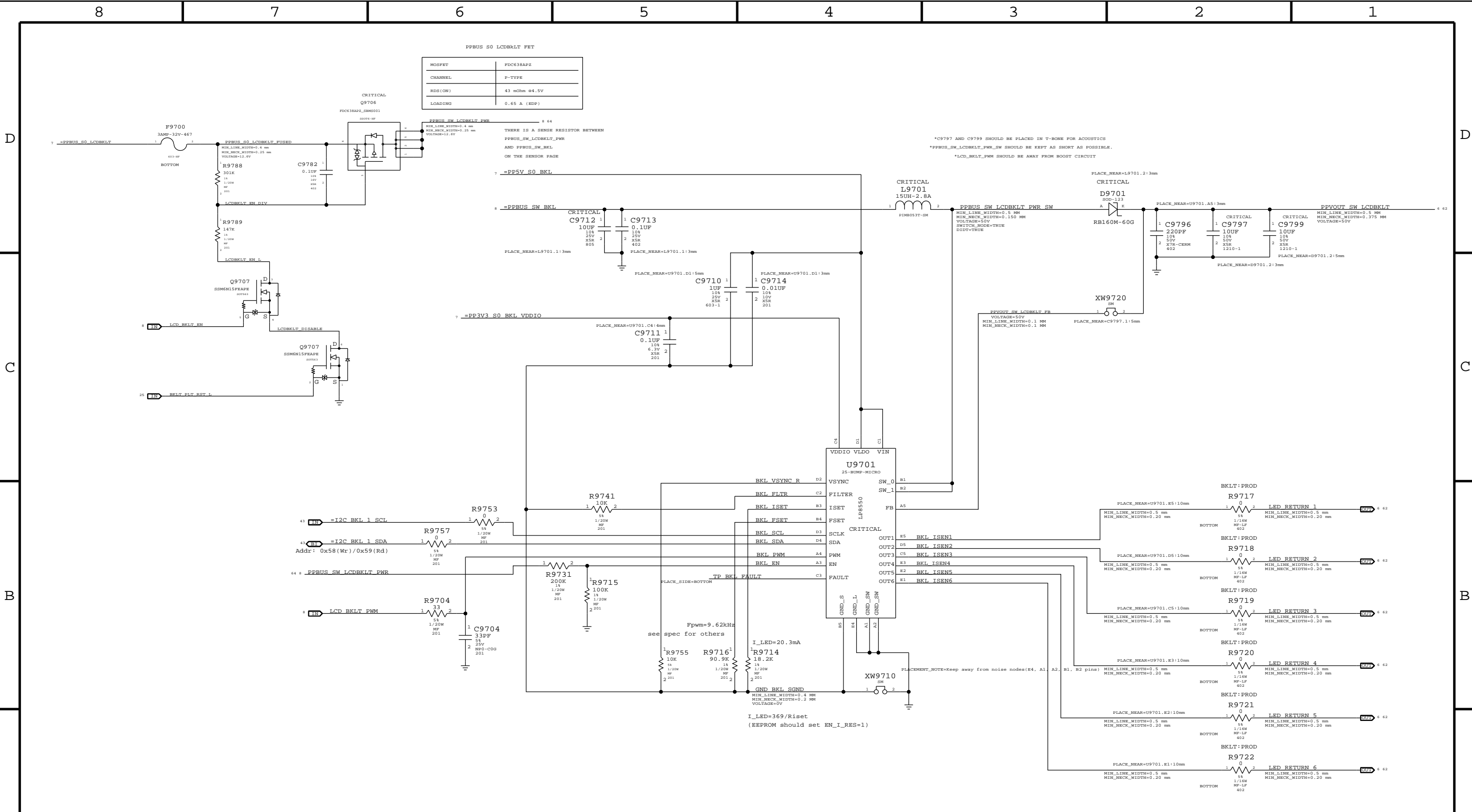


Thunderbolt Connector A



SYNC MASTER=113 MLB		SYNC DATE=11/18/2011	
Thunderbolt Connector A			
Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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PPBUS SW LCDBKLT FET	
MOSFET	FDC638APE
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EOP)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=113 MLEB SYNC DATE=10/13/2011

Apple Inc.

LCD Backlight Driver

DRAWING NUMBER: 051-9276
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIe Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

PCH PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

Note: DisplayPort tables are on Page 103

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N P<3:0>	9 17
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N N<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_EX	DMI_N2S P<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_EX	DMI_N2S N<3:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_EX	FDI_DATA P<7:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_EX	FDI_DATA N<7:0>	9 17
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_FSYN<1..0>	9 17
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_LSYN<1..0>	9 17
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_INT	9 17
CPU_PECT	CPU_45S	CPU_COMP	CPU PECT	10 19 41
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
CPU_45S	CPU_ITP	CPU_ITP	XDP DBRESET L	10 23 26
CPU_45S	CPU_ITP	CPU_ITP	XDP CPU PRDY L	10 23
CPU_45S	CPU_ITP	CPU_ITP	XDP CPU PREQ L	10 23
CPU_27P4S	CPU_COMP	CPU_COMP	EDP COMP	9
CPU_27P4S	CPU_COMP	CPU_COMP	CPU PEG COMP	9
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<2>	10
CPU_45S	CPU_ITP	CPU_ITP	CPU CFG<11..0>	9 23
CPU_CATERER_L	CPU_45S	CPU_AGTL	CPU CATERER L	10 40
CPU_VCCIO_SEL	CPU_45S	CPU_AGTL	CPU VCCIO_SEL	12
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU PROCHOT L	10 40 41 56
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU PWRGD	10 19 23
PM_THRMTRIP_L	CPU_45S	CPU_SMIL	PM THRMTRIP L	10 19 41
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M CPU P	10 16
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M CPU N	10 16
DPILL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPILL_REF_CLKP	8 10
DPILL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPILL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M P	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M N	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M P	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M N	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP CPU CLK100M P	23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP CPU CLK100M N	23
XDP_TDI	CPU_45S	CPU_ITP	XDP CPU TDI	10 23
XDP_TDO	CPU_45S	CPU_ITP	XDP CPU TDO	10 23
XDP_TMS	CPU_45S	CPU_ITP	XDP CPU TMS	10 23
XDP_TCK	CPU_45S	CPU_ITP	XDP CPU TCK	10 23
XDP_TRST_L	CPU_45S	CPU_ITP	XDP CPU TRST L	10 23
XDP_BPM_L	CPU_45S	CPU_ITP	XDP BPM L<3..0>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP BPM L<7..4>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP OBSDATA B<3..0>	9 23
(FSB_CHRST*_L)	CPU_45S	CPU_ITP	CPU CRG<15..12>	9 23
(FSB_CHRST*_L)	CPU_45S	CPU_ITP	XDP CPURST L	23
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU VCCSENSE P	12 56
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU VCCSENSE N	12 56
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU VCCIOSENSE P	12 56
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU VCCIOSENSE N	12 56
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU AXG SENSE P	12 56
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU AXG SENSE N	12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VDDO SENSE P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VDDO SENSE N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU AXG VALSENSE P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU AXG VALSENSE N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCC VALSENSE P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCC VALSENSE N	9
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU VIDALERT L	12 56
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU VIDCLK	12 56
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU VIDSOUT	12 56
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D C P<0>	6 37
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D C N<0>	6 37
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D MUX IN P	37
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D MUX IN N	37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R P<0>	6 37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R N<0>	6 37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R MUX OUT P	37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R MUX OUT N	37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_EX	PCIE SSD R2D C P<1>	6 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_EX	PCIE SSD R2D C N<1>	6 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D P<1>	6 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D N<1>	6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R P<1>	6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R N<1>	6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R C P<1>	6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_EX	PCIE SSD D2R C N<1>	6 37
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M SSD P	6 16 37
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M SSD N	6 16 37
DP_INT_ML	DP_80D	DP_TX	DP INT ML P<3..0>	6 62
DP_INT_ML	DP_80D	DP_TX	DP INT ML N<3..0>	6 62
DP_INT_ML	DP_80D	DP_TX	DP INT ML F P<3..0>	6 62
DP_INT_ML	DP_80D	DP_TX	DP INT ML F N<3..0>	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP INT AUX CH C P	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP INT AUX CH C N	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP INT AUX CH P	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP INT AUX CH N	6 62

DMI/FDI

PCIe SSD

DP

SYNC MASTER=CONSTRAINTS SYNC DATE=01/11/2012
PAGE TITLE

CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing

=2x_DIELECTRIC
=5.7x_DIELECTRIC
=4x_DIELECTRIC
=4x_DIELECTRIC
=4x_DIELECTRIC
=8.6x_DIELECTRIC
=5.7x_DIELECTRIC
=PWR_P2MM
=GND_P2MM
=8.6x_DIELECTRIC

"Real" Spacing

=2x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=6x_DIELECTRIC
=4x_DIELECTRIC
=PWR_P2MM
=GND_P2MM
=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE	ID
	PHYSICAL	SPACING			
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	5	11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	5	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CKE<3..0>	3	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CS L<3..0>	3	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A ODT<3..0>	3	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A A<15..0>	15	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A BA<2..0>	2	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A RAS L	1	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A CAS L	1	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A WE L	1	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM A DQ<7..0>	7	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM A DQ<15..8>	7	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM A DQ<23..16>	7	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM A DQ<31..24>	7	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM A DQ<39..32>	7	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM A DQ<47..40>	7	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM A DQ<55..48>	7	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM A DQ<63..56>	7	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	0	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS N<0>	0	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS P<1>	1	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<1>	1	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<2>	2	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS N<2>	2	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS P<3>	3	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<3>	3	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<4>	4	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS N<4>	4	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS P<5>	5	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<5>	5	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<6>	6	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS N<6>	6	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS P<7>	7	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<7>	7	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	5	11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	5	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CKE<3..0>	3	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CS L<3..0>	3	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B ODT<3..0>	3	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B A<15..0>	15	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B BA<2..0>	2	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B RAS L	1	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B CAS L	1	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B WE L	1	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM B DQ<7..0>	7	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM B DQ<15..8>	7	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM B DQ<23..16>	7	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM B DQ<31..24>	7	11 30
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM B DQ<39..32>	7	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM B DQ<47..40>	7	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM B DQ<55..48>	7	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM B DQ<63..56>	7	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	0	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS N<0>	0	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS P<1>	1	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<1>	1	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<2>	2	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS N<2>	2	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS P<3>	3	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<3>	3	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<4>	4	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS N<4>	4	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS P<5>	5	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<5>	5	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<6>	6	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS N<6>	6	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS P<7>	7	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<7>	7	11 30
MEM_PWR			PP1V5 S3RS0	6	7
MEM_PWR			PP1V5 S3	6	7
MEM_PWR			PP0V75 S3 MEM VREFCA A	27	28 31
MEM_PWR			PP0V75 S3 MEM VREFDO A	27	28 31

SYNC MASTER=CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
	REVISION	2.7.0	
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	PAGE
	PHYSICAL	SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA HDD R2D C P	16 37
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA HDD R2D C N	16 37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA SSD R2D MUX IN P	37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA SSD R2D MUX IN N	37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA SSD R2D P	6 37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA SSD R2D N	6 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_BX	SATA HDD D2R P	16 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_BX	SATA HDD D2R N	16 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_BX	SATA SSD D2R MUX OUT P	37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_BX	SATA SSD D2R MUX OUT N	37
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_BX	SATA SSD D2R P	6 37
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_BX	SATA SSD D2R N	6 37
PCH_SATA_ICOMP		SATA_ICOMP	PCH SATAICOMP	16
USB_HUB1_UP	USB_80D	USB	USB HUB UP P	18 24
USB_HUB1_UP	USB_80D	USB	USB HUB UP N	18 24
USB_BT	USB_80D	USB	USB BT P	24 36
USB_BT	USB_80D	USB	USB BT N	24 36
USB_BT	USB_80D	USB	USB BT CONN P	6 36
USB_BT	USB_80D	USB	USB BT CONN N	6 36
USB_BT	USB_80D	USB	USB BT WAKE P	36
USB_BT	USB_80D	USB	USB BT WAKE N	36
USB_TPAD	USB_80D	USB	USB TPAD P	6 48
USB_TPAD	USB_80D	USB	USB TPAD N	6 48
USB_TPAD	USB_80D	USB	USB TPAD CONN P	24
USB_TPAD	USB_80D	USB	USB TPAD CONN N	24
USB_TPAD_HUB	USB_80D	USB	USB TPAD HUB P	24 48
USB_TPAD_HUB	USB_80D	USB	USB TPAD HUB N	24 48
USB_TPAD_M	USB_80D	USB	USB TPAD R P	48
USB_TPAD_M	USB_80D	USB	USB TPAD R N	48
USB_TPAD_M	USB_80D	USB	USB TPAD M P	48
USB_TPAD_M	USB_80D	USB	USB TPAD M N	48
USB_SDCARD	USB_80D	USB	USB SDCARD P	8 24
USB_SDCARD	USB_80D	USB	USB SDCARD N	8 24
USB_SMC	USB_80D	USB	USB SMC P	24 40
USB_SMC	USB_80D	USB	USB SMC N	24 40
USB_CAMERA	USB_80D	USB	USB CAMERA P	6 18 39
USB_CAMERA	USB_80D	USB	USB CAMERA N	6 18 39
USB_EXT_A	USB_80D	USB	USB EXT_A P	18 38
USB_EXT_A	USB_80D	USB	USB EXT_A N	18 38
UART_45S	UART	UART	SMC DEBUGPRT TX L	38 40 41
UART_45S	UART	UART	SMC DEBUGPRT RX L	38 40 41
USB2_EXT_A_MUXED_P	USB_80D	USB	USB2_EXT_A MUXED P	38
USB2_EXT_A_MUXED_N	USB_80D	USB	USB2_EXT_A MUXED N	38
USB2_EXT_A_MUXED_F_P	USB_80D	USB	USB2_EXT_A MUXED F P	38
USB2_EXT_A_MUXED_F_N	USB_80D	USB	USB2_EXT_A MUXED F N	38
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A RX P	18 38
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A RX N	18 38
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A TX P	18 38
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A TX N	18 38
USB3_EXT_A_RX_F_P	USB_80D	USB3_PCH_RX	USB3_EXT_A RX F P	38
USB3_EXT_A_RX_F_N	USB_80D	USB3_PCH_RX	USB3_EXT_A RX F N	38
USB3_EXT_A_TX_F_P	USB_80D	USB3_PCH_TX	USB3_EXT_A TX F P	38
USB3_EXT_A_TX_F_N	USB_80D	USB3_PCH_TX	USB3_EXT_A TX F N	38
USB3_EXT_A_TX_C_P	USB_80D	USB3_PCH_TX	USB3_EXT_A TX C P	38
USB3_EXT_A_TX_C_N	USB_80D	USB3_PCH_TX	USB3_EXT_A TX C N	38
USB_EXTB_P	USB_80D	USB	USB_EXTB P	6 24 39
USB_EXTB_N	USB_80D	USB	USB_EXTB N	6 24 39
USB_EXTB_EHCI_P	USB_80D	USB	USB_EXTB EHCI P	18 24
USB_EXTB_EHCI_N	USB_80D	USB	USB_EXTB EHCI N	18 24
USB_EXTB_XHCI_P	USB_80D	USB	USB_EXTB XHCI P	18 24
USB_EXTB_XHCI_N	USB_80D	USB	USB_EXTB XHCI N	18 24
USB3_EXTB_RX_P	USB_80D	USB3_PCH_RX	USB3_EXTB RX P	18 39
USB3_EXTB_RX_N	USB_80D	USB3_PCH_RX	USB3_EXTB RX N	18 39
USB3_EXTB_RX_RC_P	USB_80D	USB3_PCH_RX	USB3_EXTB RX RC P	6 39
USB3_EXTB_RX_RC_N	USB_80D	USB3_PCH_RX	USB3_EXTB RX RC N	6 39
USB3_EXTB_RX_CONN_P	USB_80D	USB3_PCH_RX	USB3_EXTB RX CONN P	18 39
USB3_EXTB_RX_CONN_N	USB_80D	USB3_PCH_RX	USB3_EXTB RX CONN N	18 39
USB3_EXTB_TX_P	USB_80D	USB3_PCH_TX	USB3_EXTB TX P	18 39
USB3_EXTB_TX_N	USB_80D	USB3_PCH_TX	USB3_EXTB TX N	18 39
USB3_EXTB_TX_C_P	USB_80D	USB3_PCH_TX	USB3_EXTB TX C P	6 39
USB3_EXTB_TX_C_N	USB_80D	USB3_PCH_TX	USB3_EXTB TX C N	6 39
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI P	18 24
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI N	18 24
PCH_USB_RBBIAS	PCH_USB_RBBIAS		PCH_USB_RBBIAS	18
PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_PCH P	16
PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_PCH N	16
PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH CLK96M_DOT P	16
PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH CLK96M_DOT N	16
PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH CLK100M_SATA P	16
PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH CLK100M_SATA N	16
CPU_45S	CLK_PCIE	CLK_PCIE	PCH CLK14P3M_REFCLK	16

SATA SSD


USB Hub nets

USB Camera nets

USB EXT_A nets (Right USB port)

USB EXT_B nets (Left USB port)

Unused USB nets

SYNC MASTER=CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
PCH Constraints 1			
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?	DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?	DP_2OTHERHS	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?	DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	6 16 40 42
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME L	6 16 40 42
LPC_45S	LPC_45S	LPC	LPCPLUS RESET L	6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	25 40
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN	16 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIEOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	16 43
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	16 43
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	16 43
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	16 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK	16 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA	16 43
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	6 16 39
HDA_45S	HDA_45S	HDA	HDA BIT CLK R	16
HDA_SYNC	HDA_45S	HDA	HDA SYNC	6 16 39
HDA_45S	HDA_45S	HDA	HDA SYNC R	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
HDA_45S	HDA_45S	HDA	HDA_RST_L	6 16 39
HDA_SDINO	HDA_45S	HDA	HDA_SDINO	6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 39
HDA_45S	HDA_45S	HDA	HDA_SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 41
CLK_SLOW_45S	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	40 41
SPT_CLK	SPT_45S	SPT	SPI_CLK_R	16 42
SPT_45S	SPT_45S	SPT	SPI_CLK	42
SPT_45S	SPT_45S	SPT	SPI_MOST_R	16 42
SPT_45S	SPT_45S	SPT	SPI_MOST	42
SPT_45S	SPT_45S	SPT	SPI_MISO	16 42
SPT_45S	SPT_45S	SPT	SPI_CS0_R_L	16 42
SPT_45S	SPT_45S	SPT	SPI_CS0_L	42
SPT_45S	SPT_45S	SPT	SPI_SMC_CLK	40 41
SPT_45S	SPT_45S	SPT	SPI_SMC_MOST	40 41
SPT_45S	SPT_45S	SPT	SPI_SMC_MISO	40 41
SPT_45S	SPT_45S	SPT	SPI_SMC_CS_L	40 41
SPT_45S	SPT_45S	SPT	SPI_MLB_CLK	41 42 49
SPT_45S	SPT_45S	SPT	SPI_MLB_MOST	41 42 49
SPT_45S	SPT_45S	SPT	SPI_MLB_MISO	41 42 49
SPT_45S	SPT_45S	SPT	SPI_MLB_CS_L	41 42 49
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D P	6 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D N	6 36
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C P	16 36
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C N	16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R P	6 16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R N	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 36
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D P<3..0>	33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D N<3..0>	33
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C P<3..0>	6 33
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C N<3..0>	6 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R P<3..0>	6 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R N<3..0>	6 33
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C P<3..0>	6 33
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C N<3..0>	6 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 33
CLK_PCIE_80D	CLK_PCIE	CLK_PCIE	PEG_CLK100M_P	6 16
CLK_PCIE_80D	CLK_PCIE	CLK_PCIE	PEG_CLK100M_N	6 16
XDP_TDI	BCH_45S	BCH_ITP	XDP_PCH_TDI	16 23
XDP_TDO	BCH_45S	BCH_ITP	XDP_PCH_TDO	16 23
XDP_TMS	BCH_45S	BCH_ITP	XDP_PCH_TMS	16 23
XDP_TCK	BCH_45S	BCH_ITP	XDP_PCH_TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	33
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	33
DP_80D	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	6 33
DP_80D	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	6 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	33
DP_80D	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	6 33
DP_80D	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	6 33
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	33
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	33
DP_80D	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	6 33
DP_80D	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	6 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	33
DP_80D	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	6 33
DP_80D	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	6 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	33
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
CLK_25M_45S	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
CLK_25M_45S	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

SYSC_MASTER=CONSTRAINTS		SYSC_DATE=01/11/2012	
PAGE TITLE			
PCH Constraints 2			
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX	TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX	TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX	TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX	TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
TBT_A_R2D	TBTDE_80D	TBTDR_TX	TBT A R2D C P<1..0>	33 63
TBT_A_R2D	TBTDE_80D	TBTDR_TX	TBT A R2D C N<1..0>	33 63
TBT_A_R2D	TBTDE_80D	TBTDR_TX	TBT A R2D P<1..0>	63
TBT_A_R2D	TBTDE_80D	TBTDR_TX	TBT A R2D N<1..0>	63
DP_TBTPA_ML1	DP_80D	DP_TX	DP TBTPA ML C P<1>	33 63
DP_TBTPA_ML1	DP_80D	DP_TX	DP TBTPA ML C N<1>	33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP TBTPA ML C P<3>	33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP TBTPA ML C N<3>	33 63
	DP_80D	DP_TX	DP TBTPA ML P<3..1:2>	63
	DP_80D	DP_TX	DP TBTPA ML N<3..1:2>	63
	DP_80D	DP_TX	DP A LSX ML P<1>	63
	DP_80D	DP_TX	DP A LSX ML N<1>	63
	TBTDE_80D	TBTDR_BX	TBT A D2R C P<1..0>	63
	TBTDE_80D	TBTDR_BX	TBT A D2R C N<1..0>	63
	TBTDE_80D	TBTDR_BX	TBT A D2R P<1>	33 63
	TBTDE_80D	TBTDR_BX	TBT A D2R N<1>	33 63
	TBTDE_80D	TBTDR_BX	TBT A D2R P<0>	33 63
	TBTDE_80D	TBTDR_BX	TBT A D2R N<0>	33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP TBTPA AUXCH C P	33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP TBTPA AUXCH C N	33 63
	DP_80D	DP_AUX	DP TBTPA AUXCH P	63
	DP_80D	DP_AUX	DP TBTPA AUXCH N	63
	DP_80D	DP_AUX	DP A AUXCH DDC P	63
	DP_80D	DP_AUX	DP A AUXCH DDC N	63
	TBTDE_80D	TBTDR_BX	TBT A D2R1 AUXDDC P	63
	TBTDE_80D	TBTDR_BX	TBT A D2R1 AUXDDC N	63
TBT_B_R2D	TBTDE_80D	TBTDR_TX	TBT B R2D C P<1..0>	33 63
TBT_B_R2D	TBTDE_80D	TBTDR_TX	TBT B R2D C N<1..0>	33 63
	TBTDE_80D	TBTDR_TX	TBT B R2D P<1..0>	63
	TBTDE_80D	TBTDR_TX	TBT B R2D N<1..0>	63
DP_TBTPB_ML	DP_80D	DP_TX	DP TBTPB ML C P<3..1:2>	33 63
DP_TBTPB_ML	DP_80D	DP_TX	DP TBTPB ML C N<3..1:2>	33 63
	DP_80D	DP_TX	DP TBTPB ML P<3..1:2>	63
	DP_80D	DP_TX	DP TBTPB ML N<3..1:2>	63
	DP_80D	DP_TX	DP B LSX ML P<1>	63
	DP_80D	DP_TX	DP B LSX ML N<1>	63
	TBTDE_80D	TBTDR_BX	TBT B D2R C P<1..0>	63
	TBTDE_80D	TBTDR_BX	TBT B D2R C N<1..0>	63
	TBTDE_80D	TBTDR_BX	TBT B D2R P<1..0>	33 63
	TBTDE_80D	TBTDR_BX	TBT B D2R N<1..0>	33 63
TBT_B_D2R	DP_80D	DP_AUX	DP TBTPB AUXCH C P	33 63
TBT_B_D2R	DP_80D	DP_AUX	DP TBTPB AUXCH C N	33 63
	DP_80D	DP_AUX	DP TBTPB AUXCH P	63
	DP_80D	DP_AUX	DP TBTPB AUXCH N	63
	DP_80D	DP_AUX	DP B AUXCH DDC P	63
	DP_80D	DP_AUX	DP B AUXCH DDC N	63
	TBTDE_80D	TBTDR_BX	TBT B D2R1 AUXDDC P	63
	TBTDE_80D	TBTDR_BX	TBT B D2R1 AUXDDC N	63

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
	DP_80D	DP_TX	DP TBTSRC ML C P<3..0>	33
	DP_80D	DP_TX	DP TBTSRC ML C N<3..0>	33
	DP_80D	DP_AUX	DP TBTSRC AUXCH C P	33
	DP_80D	DP_AUX	DP TBTSRC AUXCH C N	33
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK	33
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI	33
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO	33
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS L	33

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=CONSTRAINTS		SYNC DATE=01/11/2012	
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Apple Inc.		DRAWING NUMBER	051-9276
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 40 43
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 40 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 40 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 40 43
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL 40 43
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA 40 43
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 40 43
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 40 43
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 40 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 40 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P 52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N 52
	1:1_DIFFPAIR		CHGR_CSI_R_P 52
	1:1_DIFFPAIR		CHGR_CSI_R_N 52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P 52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N 52
	1:1_DIFFPAIR		CHGR_CSO_R_P 52
	1:1_DIFFPAIR		CHGR_CSO_R_N 52

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SYNC MASTER=CONSTRAINTS		SYNC DATE=01/11/2012	
SMC Constraints			
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J11/J13 Specific Net Properties

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SENSE_1T01_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1T01_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET_THMSNS_D1_P	45 46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET_THMSNS_D1_N	45 46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_P	46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_N	46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_MLBBOT_THMSNS_P	46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_MLBBOT_THMSNS_N	46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS_D2_R_P	46
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS_D2_R_N	46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU_THERMD_P	9 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU_THERMD_N	9 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUTHMSNS_D2_P	46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUTHMSNS_D2_N	46
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0_CS_N	44 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0_CS_P	44 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1_P	44 56 57
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1_N	44 57
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUM_R_P	44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUM_R_N	44
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1G_P	44 57
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1G_N	44 57
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUMG_R_P	44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUMG_R_N	44
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	VCCSAS0_CS_P	44 53
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	VCCSAS0_CS_N	44 53
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	VCCSAISNS_R_P	44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	VCCSAISNS_R_N	44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_P	44 60
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_N	44 60
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_R_P	44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_R_N	44
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUMG_P	56 57
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUMG_N	56 57
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUM_P	56 57
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUM_N	56 57
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_N	8 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_P	8 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER_N	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER_P	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V5_S3_N	45 55
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V5_S3_P	45 55
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_N	36 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_P	36 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_SSD_N	37 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_SSD_P	37 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKIT_N	8 45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKIT_P	8 45
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	50
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 50 51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 50 51
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

SYNC MASTER=CONSTRAINTS SYNC DATE=01/11/2012

Project Specific Constraints

Apple Inc.

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS		BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM		NO_TYPE, BGA			MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3, ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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