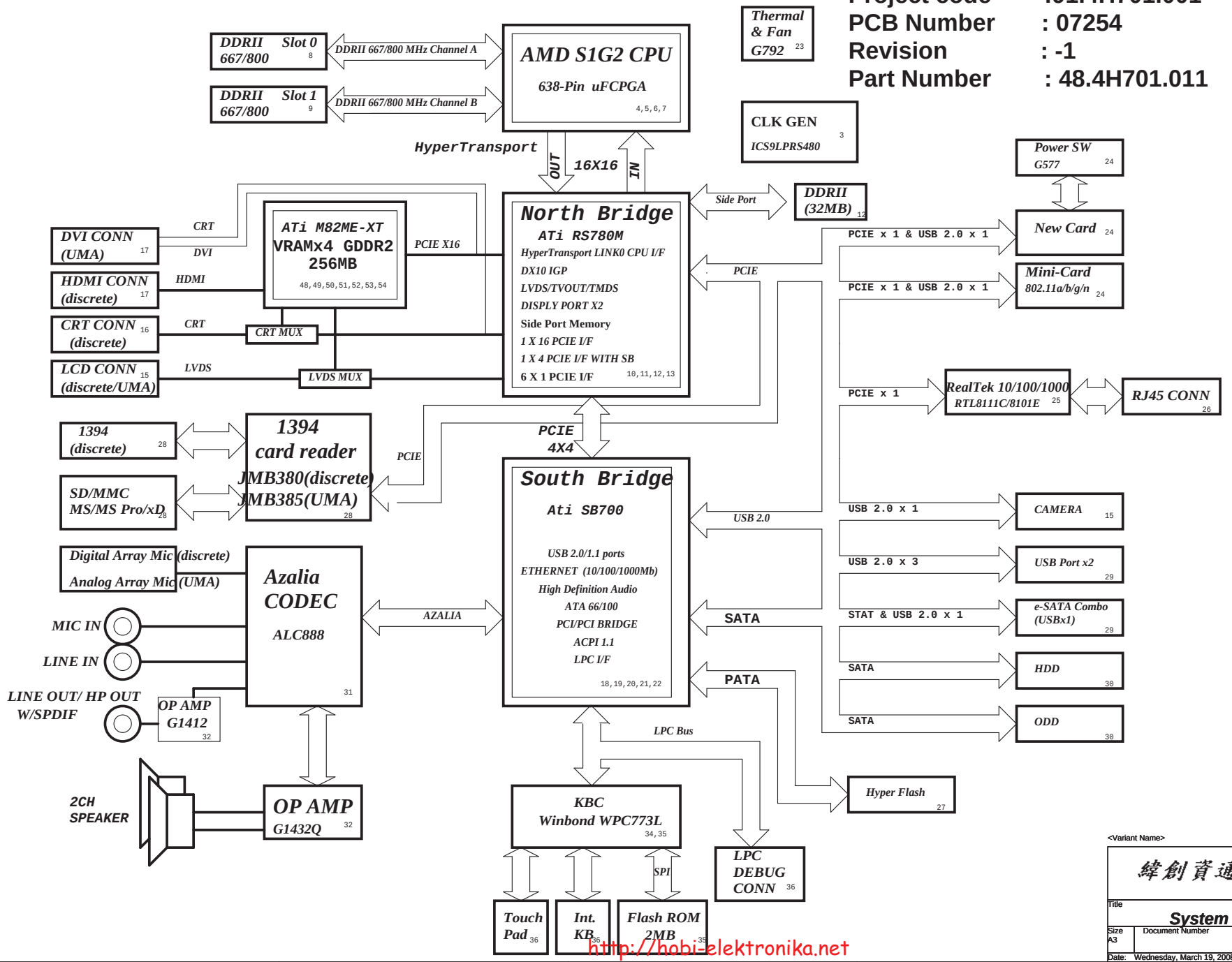
P1/P15 Block Diagram

Project code :91.4H701.001
PCB Number : 07254
Revision : -1
Part Number : 48.4H701.011



CPU V_CORE ISL6265 38,39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51124 41	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0

SYSTEM DC/DC TPS51125 40	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC LDO 44	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0

SYSTEM DC/DC LDO 44	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0

SYSTEM DC/DC TPS51125 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

MAXIM CHARGER BQ24745 46	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: System Block Diagram

Size	Document Number	Rev
A3	P1/P15	-1

Date: Wednesday, March 19, 2008 Sheet 1 of 56

SB700 Functional Strap Definitions

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X

		USB PORT#	DESTINATION
SB700	2.0	0	Combo(ESATA/USB)
		1	USB1
		2	USB2
		3	CAMERA
		4	NC
		5	NEW CARD
		6	NC
		7	WLAN
		8	NC
		9	NC
		10	NC
		11	NC
	1.1	12	NC
		13	NC

PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER &1394
Lane 4	NC
Lane 5	NC

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED (DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

	VGA	Display	Audio	LAN	1394a / Card Reader	BT	LED
P15	M82-ME XT	HDMI/CRT	Digital Array Mic	Giga LAN RTL 8111C	YES / JMB380	N/A	Power Button with white LED-Backlight
P1	RS780M	DVI-I	Analog Array Mic	LAN(10/100) RTL 8101E	N/A / JMB385	N/A	NO Backlight

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

<Variant Name>

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Title: Table of Content

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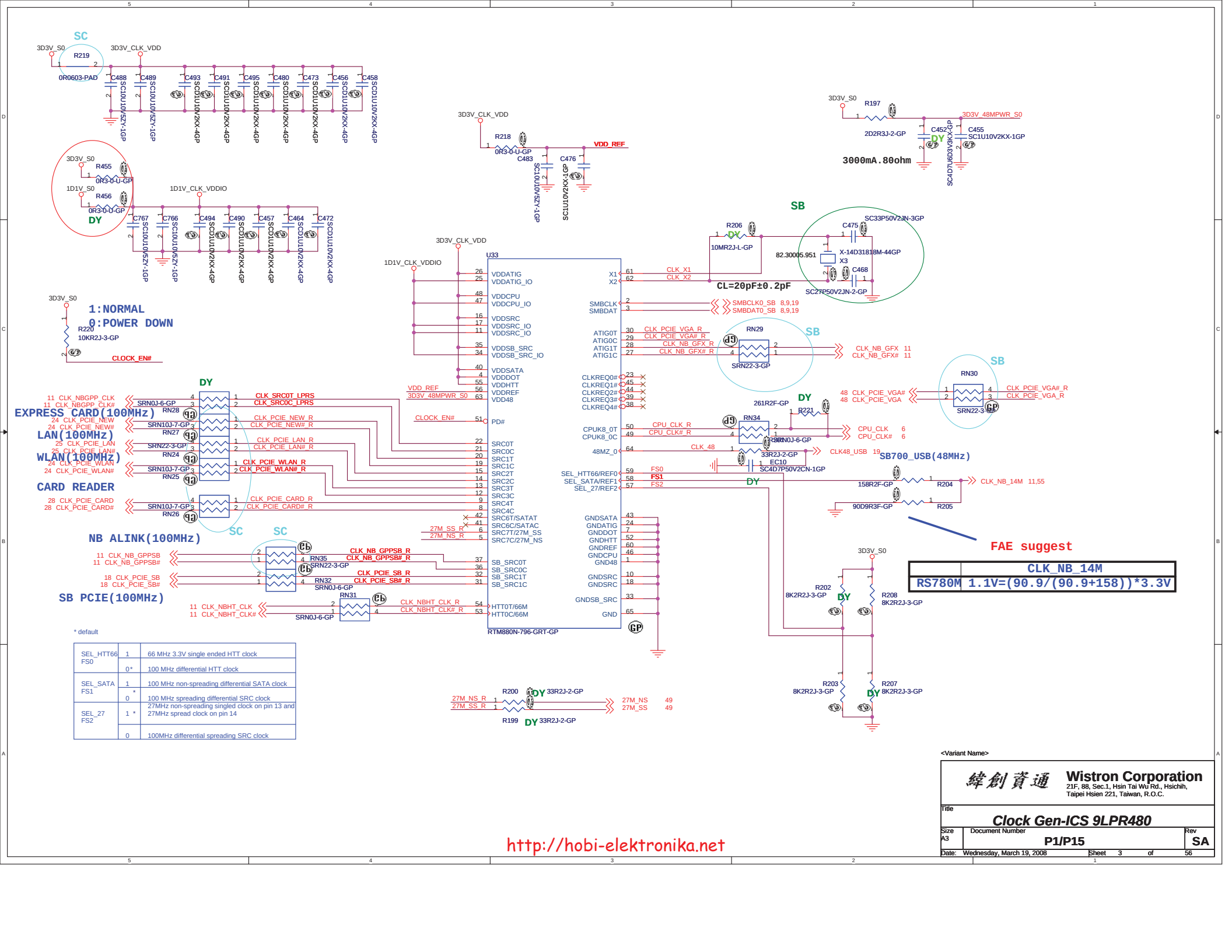
SC
3D3V_S0
3D3V_CLK_VDD
R219
0R0603-PAD
C488 C489 C493 C491 C495 C480 C473 C456 C458
SC10U10V5ZY-1GP
SC10U10V2KX-4GP
1D1V_S0
1D1V_CLK_VDDIO
R455
R456
0R3-0-U-GP
DY
C767 C766 C494 C490 C457 C464 C472
R218
VDD_REF
C483 C476
SC1U10V2KX-1GP
R197
2D2R3J-2-GP
3D3V_48MPWR_S0
C452
C455
SC1U10V2KX-1GP
SC47U6D3V3KX-GP
3000mA.80ohm
SB
SC33P50V2JN-3GP
R206
10MR2J-L-GP
C475
X-14D31818M-44GP
82.30005.951
X3
C468
SC27P50V2JN-2-GP
CL=20pF±0.2pF
U33
RTM880N-796-GRT-GP
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDDDOT
VDDHTT
VDDREF
VDD48
PD#
SRC0T
SRC0C
SRC1T
SRC1C
SRC2T
SRC2C
SRC3T
SRC3C
SRC4T
SRC4C
SRC6T/SATAT
SRC6C/SATAC
SRC7T/27M_SS
SRC7C/27M_NS
SB_SRC0T
SB_SRC0C
SB_SRC1T
SB_SRC1C
HTT0T/66M
HTT0C/66M
X1
X2
CLK_X1
CLK_X2
SMBCLK
SMBDAT
SMBCLK0_SB 8,9,19
SMBDAT0_SB 8,9,19
ATIG0T
ATIG0C
ATIG1T
ATIG1C
CLK_PCIE_VGA_R
CLK_PCIE_VGA#_R
CLK_NB_GFX_R
CLK_NB_GFX#_R
RN29
SRN22-3-GP
CLK_NB_GFX 11
CLK_NB_GFX# 11
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
RN30
48 CLK_PCIE_VGA#
48 CLK_PCIE_VGA
CLK_PCIE_VGA#_R
CLK_PCIE_VGA_R
CPUK8_0T
CPUK8_0C
CPU_CLK_R
CPU_CLK#_R
RN34
261R2F-GP
R221
SRN0J-6-GP
CPU_CLK 6
CPU_CLK# 6
48MZ_0
CLK_48
33R2J-2-GP
EC10
SC4D7P50V2CN-1GP
CLK48_USB 19
SB700_USB(48MHz)
SEL_HTT66/REF0
SEL_SATA/REF1
SEL_27/REF2
FS0
FS1
FS2
158R2F-GP
90D9R3F-GP
R204
R205
CLK_NB_14M 11,55
GNDSATA
GNDATIG
GNDDOT
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSB_SRC
GND
1:NORMAL
0:POWER DOWN
R220
10KR2J-3-GP
CLOCK_EN#
EXPRESS CARD(100MHz)
LAN(100MHz)
WLAN(100MHz)
CARD READER
11 CLK_NBGPP_CLK
11 CLK_NBGPP_CLK#
24 CLK_PCIE_NEW
24 CLK_PCIE_NEW#
25 CLK_PCIE_LAN
25 CLK_PCIE_LAN#
24 CLK_PCIE_WLAN
24 CLK_PCIE_WLAN#
28 CLK_PCIE_CARD
28 CLK_PCIE_CARD#
SRN0J-6-GP
SRN10J-7-GP
SRN22-3-GP
RN28
RN27
RN24
RN25
RN26
CLK_SRC0T_LPRS
CLK_SRC0C_LPRS
CLK_PCIE_NEW_R
CLK_PCIE_NEW#_R
CLK_PCIE_LAN_R
CLK_PCIE_LAN#_R
CLK_PCIE_WLAN_R
CLK_PCIE_WLAN#_R
CLK_PCIE_CARD_R
CLK_PCIE_CARD#_R
NB ALINK(100MHz)
SB PCIE(100MHz)
11 CLK_NB_GPPSB
11 CLK_NB_GPPSB#
18 CLK_PCIE_SB
18 CLK_PCIE_SB#
RN35
RN32
RN31
SRN22-3-GP
SRN0J-6-GP
CLK_NB_GPPSB_R
CLK_NB_GPPSB#_R
CLK_PCIE_SB_R
CLK_PCIE_SB#_R
11 CLK_NBHT_CLK
11 CLK_NBHT_CLK#
CLK_NBHT_CLK_R
CLK_NBHT_CLK#_R
27M_SS_R
27M_NS_R
R200
R199
33R2J-2-GP
27M_NS 49
27M_SS 49
R202
R208
R203
R207
8K2R2J-3-GP
FAE suggest
CLK_NB_14M
RS780M 1.1V=(90.9/(90.9+158))*3.3V
* default
SEL_HTT66 FS0 1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
SEL_SATA FS1 1 100 MHz non-spreading differential SATA clock
0 * 100 MHz spreading differential SRC clock
SEL_27 FS2 1 * 27MHz non-spreading singled clock on pin 13 and 27MHz spread clock on pin 14
0 100MHz differential spreading SRC clock
http://hobi-elektronika.net
<Variant Name>
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Gen-ICS 9LPR480
Size A3
Document Number
P1/P15
Rev SA
Date: Wednesday, March 19, 2008
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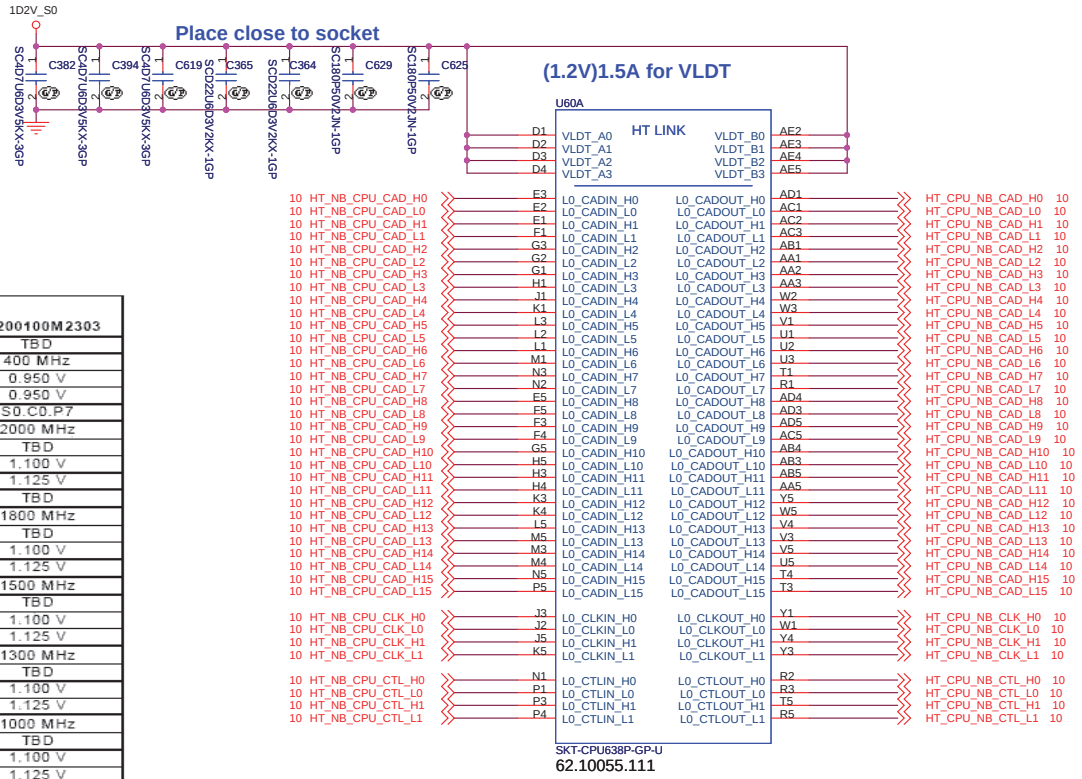
CPU / HT3.0

SSID = CPU



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Variant Name>

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Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

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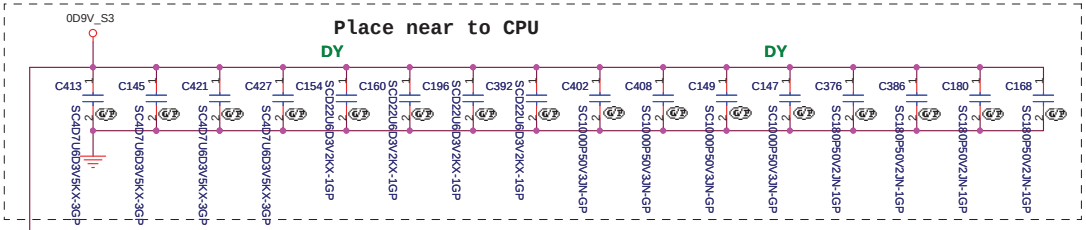
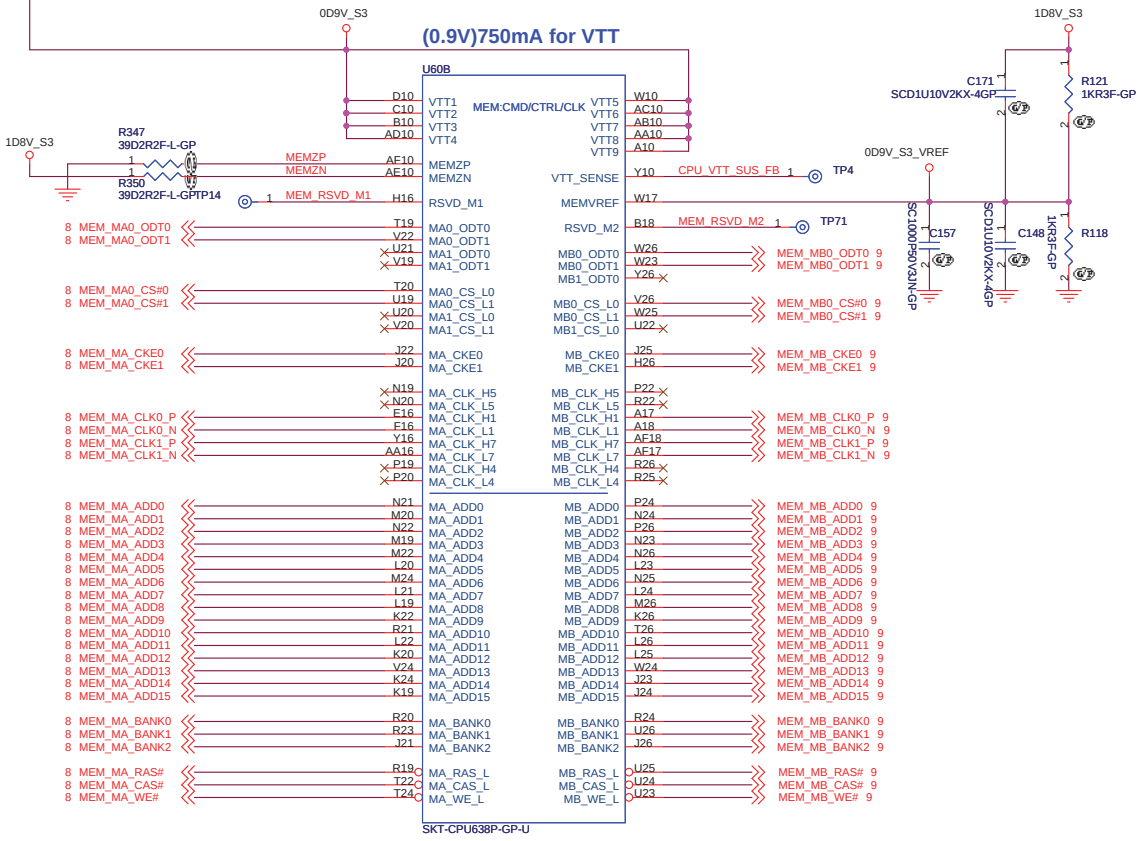
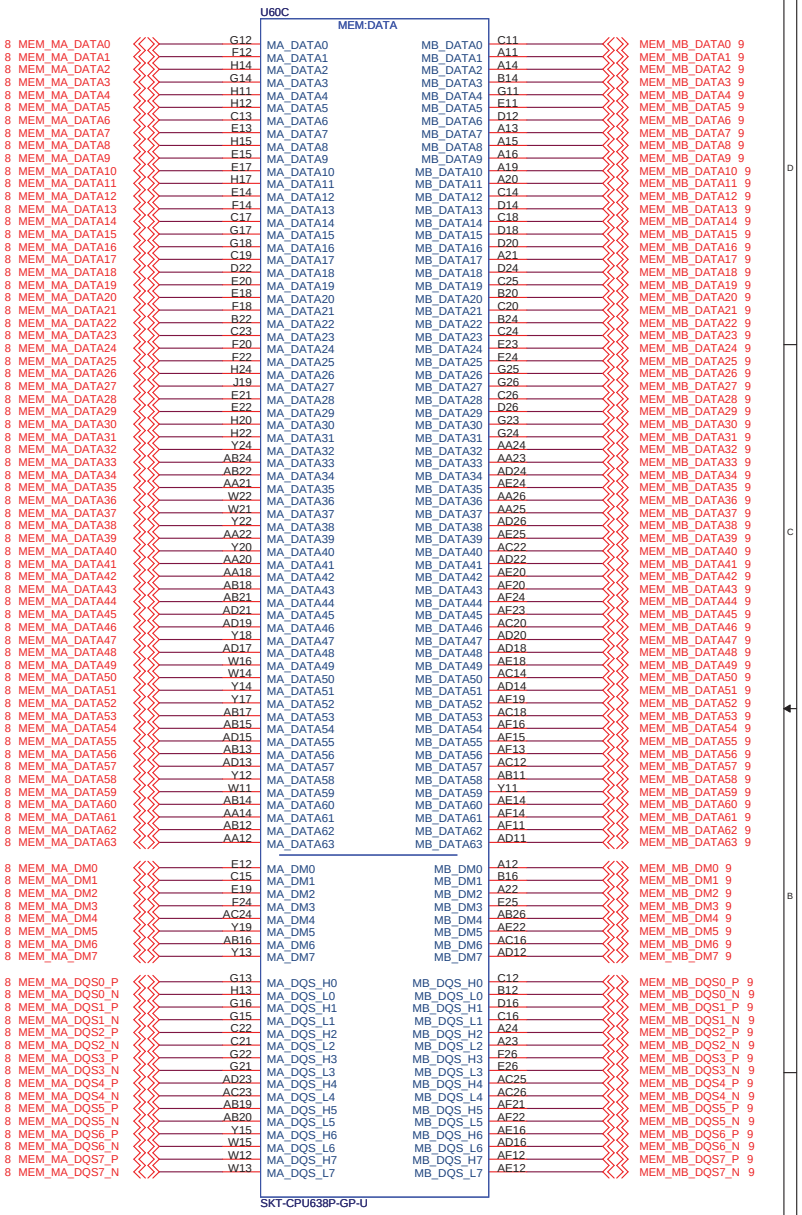
CPU / DDR2







<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_DDR_(2/4)**

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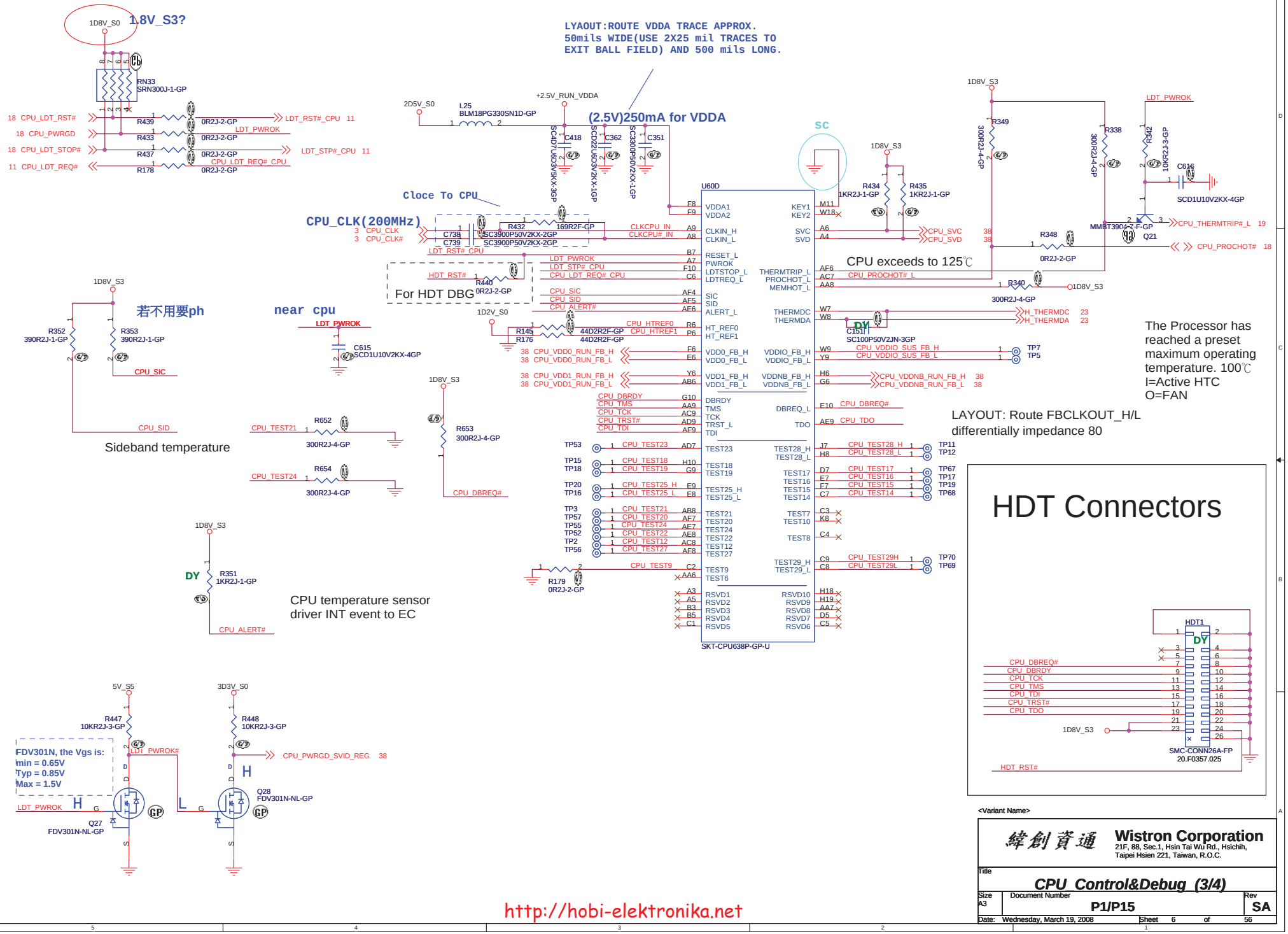
1.8V_S3?
1D8V_S0
RN33
SRN300J-1-GP
18 CPU_LDT_RST#
18 CPU_PWRGD
18 CPU_LDT_STOP#
11 CPU_LDT_REQ#
R439
R433
R437
R178
0R2J-2-GP
LDT_PWROK
CPU_LDT_REQ#_CPU
LDT_RST#_CPU 11
LDT_STP#_CPU 11
LAYOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
2D5V_S0
L25
BLM18PG330SN1D-GP
+2.5V_RUN_VDDA
(2.5V)250mA for VDDA
SC4D7U6D3V5KX-3GP
C418
SC22U6D3V2KX-1GP
C362
SC330P50V2KX-1GP
C351
Cloce To CPU
CPU_CLK(200MHz)
3 CPU_CLK
3 CPU_CLK#
C738
C739
SC3900P50V2KX-2GP
R432
169R2F-GP
CLKCPU_IN
CLKCPU#_IN
LDT_RST#_CPU
HDT_RST#
R440
0R2J-2-GP
For HDT DBG
LDT_PWROK
LDT_STP#_CPU
CPU_LDT_REQ#_CPU
CPU_SIC
CPU_SID
CPU_ALERT#
U60D
VDDA1
VDDA2
CLKIN_H
CLKIN_L
RESET_L
PWROK
LDTSTOP_L
LDTREQ_L
SIC
SID
ALERT_L
HT_REF0
HT_REF1
KEY1
KEY2
SVC
SVD
THERMTRIP_L
PROCHOT_L
MEMHOT_L
THERMDC
THERMDA
VDD0_FB_H
VDD0_FB_L
VDD1_FB_H
VDD1_FB_L
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
DBRDY
TMS
TCK
TRST_L
TDI
TDO
DBREQ_L
TEST23
TEST18
TEST19
TEST25_H
TEST25_L
TEST21
TEST20
TEST24
TEST22
TEST12
TEST27
TEST9
TEST6
TEST28_H
TEST28_L
TEST17
TEST16
TEST15
TEST14
TEST7
TEST10
TEST8
TEST29_H
TEST29_L
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD10
RSVD9
RSVD8
RSVD7
RSVD6
SKT-CPU638P-GP-U
CPU_HTREF0
CPU_HTREF1
R145
R176
44D2R2F-GP
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
CPU_VDD1_RUN_FB_H
CPU_VDD1_RUN_FB_L
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
CPU_TEST23
CPU_TEST18
CPU_TEST19
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST21
CPU_TEST20
CPU_TEST24
CPU_TEST22
CPU_TEST12
CPU_TEST27
CPU_TEST9
R179
0R2J-2-GP
CPU_TEST28_H
CPU_TEST28_L
CPU_TEST17
CPU_TEST16
CPU_TEST15
CPU_TEST14
CPU_TEST29H
CPU_TEST29L
CPU_DBREQ#
CPU_TDO
CPU_VDDIO_SUS_FB_H
CPU_VDDIO_SUS_FB_L
CPU_VDDNB_RUN_FB_H
CPU_VDDNB_RUN_FB_L
TP53
TP15
TP18
TP20
TP16
TP3
TP57
TP55
TP52
TP2
TP56
TP11
TP12
TP67
TP17
TP19
TP68
TP70
TP69
TP7
TP5
SC
1D8V_S3
R434
R435
1KR2J-1-GP
CPU_SVC
CPU_SVD
CPU exceeds to 125℃
CPU_PROCHOT# 18
R340
300R2J-4-GP
H_THERMDC 23
H_THERMDA 23
DY
C151
SC100P50V2JN-3GP
R349
R338
300R2J-4-GP
R342
10KR2J-3-GP
C616
SCD1U10V2KX-4GP
MMBT3904-7-F-GP
Q21
CPU_THERMTRIP#_L 19
R348
0R2J-2-GP
The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN
若不用要ph
R352
390R2J-1-GP
R353
390R2J-1-GP
CPU_SIC
CPU_SID
Sideband temperature
near cpu
LDT_PWROK
C615
SCD1U10V2KX-4GP
CPU_TEST21
CPU_TEST24
R652
R654
300R2J-4-GP
R653
300R2J-4-GP
CPU_DBREQ#
DY
R351
1KR2J-1-GP
CPU_ALERT#
CPU temperature sensor
driver INT event to EC
LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80
HDT Connectors
HDT1
DY
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
1D8V_S3
SMC-CONN26A-FP
20.F0357.025
HDT_RST#
5V_S5
3D3V_S0
R447
10KR2J-3-GP
R448
10KR2J-3-GP
LDT_PWROK#
CPU_PWRGD_SVID_REG 38
FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V
H
L
Q27
FDV301N-NL-GP
Q28
FDV301N-NL-GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_Control&Debug_(3/4)
Size A3
Document Number
P1/P15
Rev SA
Date: Wednesday, March 19, 2008
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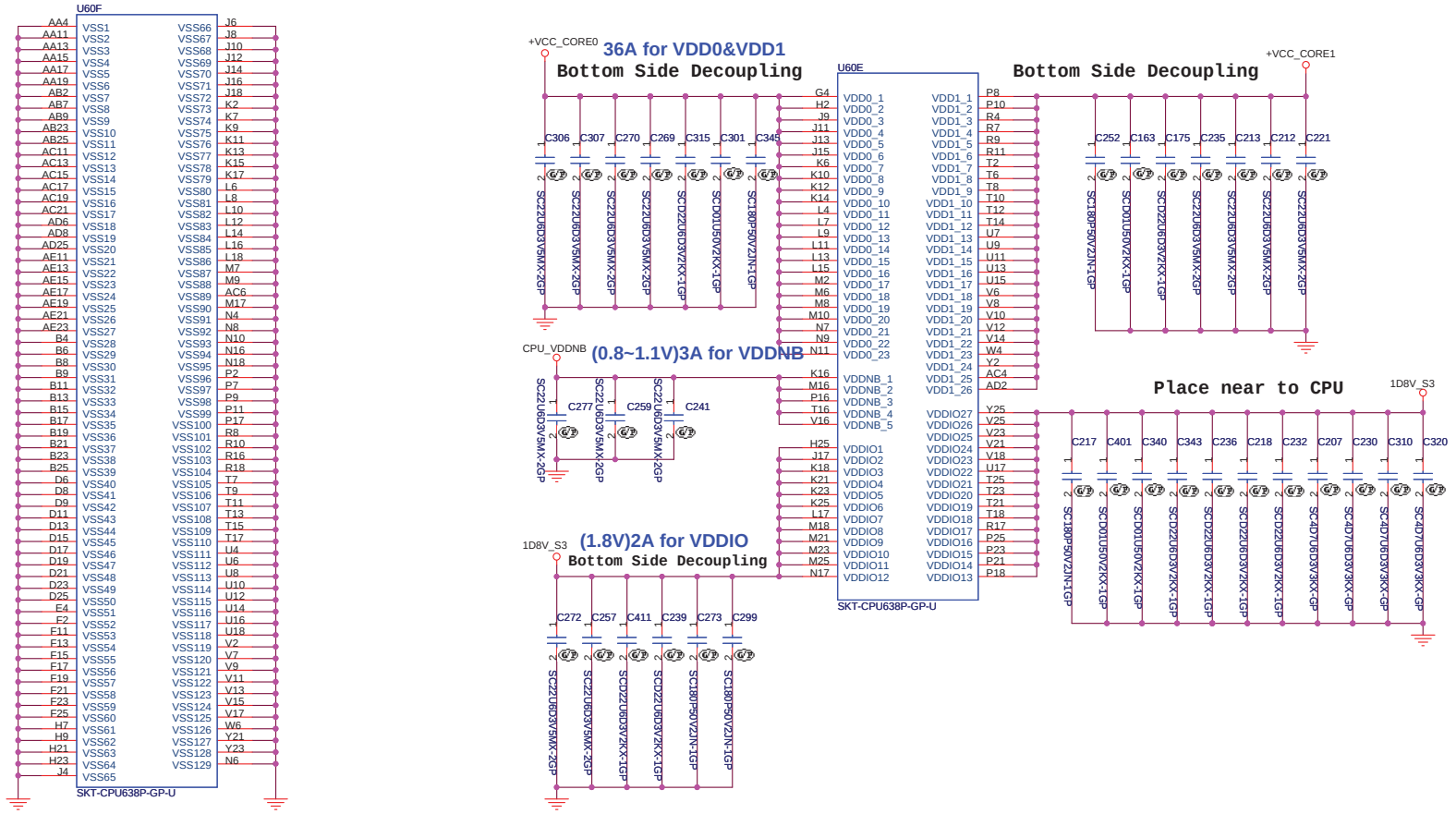
http://hobi-elektronika.net

SSID = CPU



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

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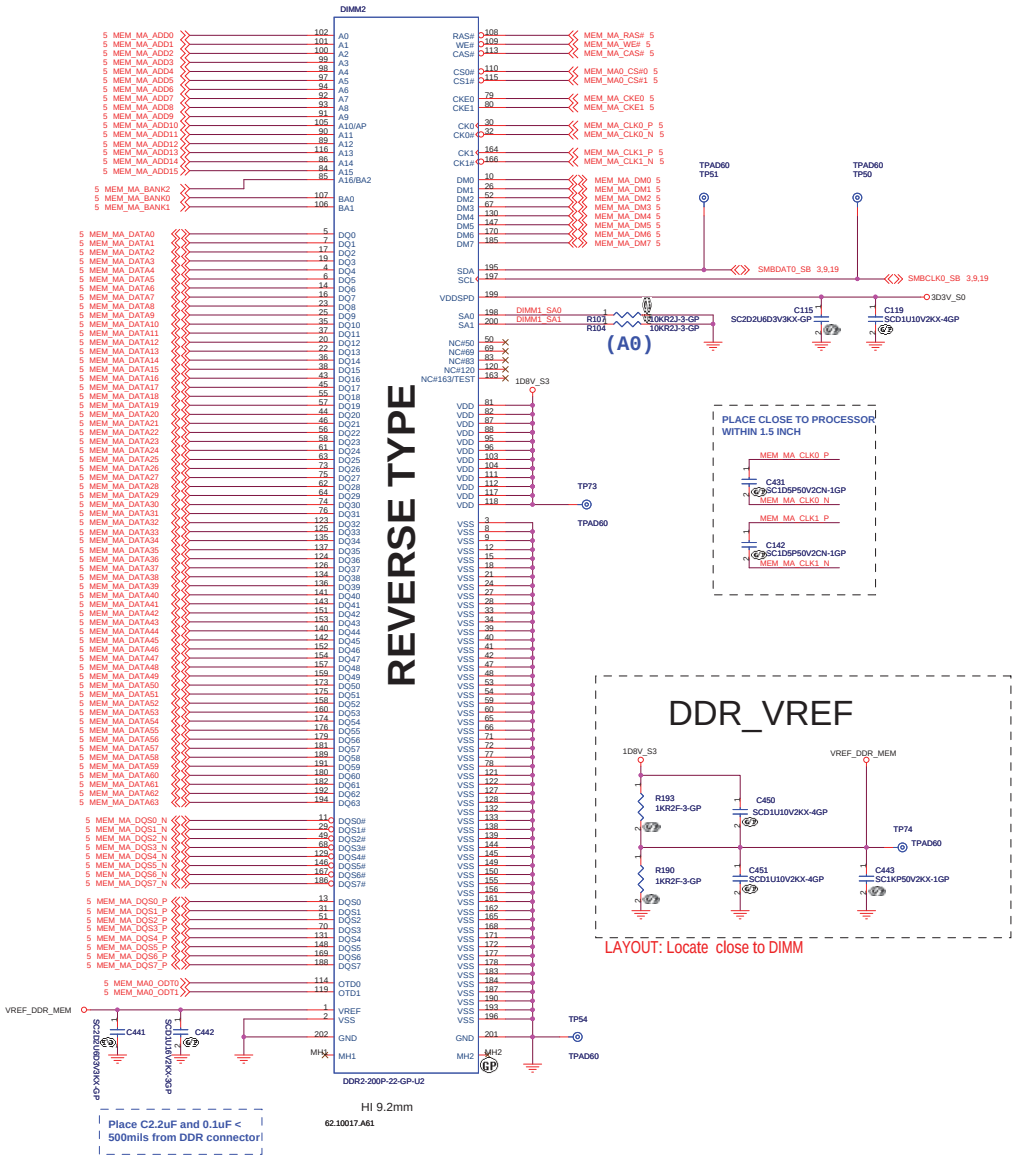
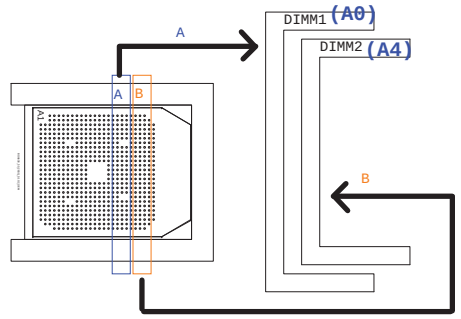
SSID = MEMORY

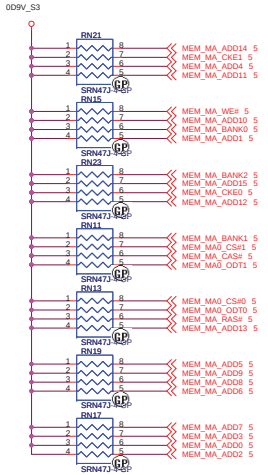




PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

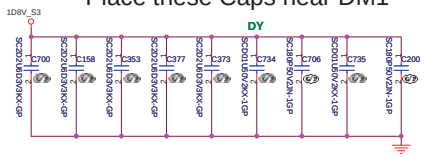
Do not share the Term resistor between the DDR addess and Control Signals.



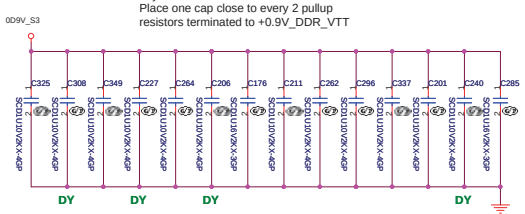
DDR_VREF

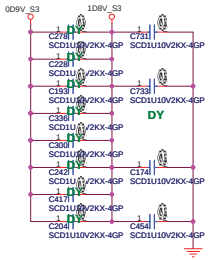
Decoupling Capacitor

Place these Caps near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





<Variant Name>

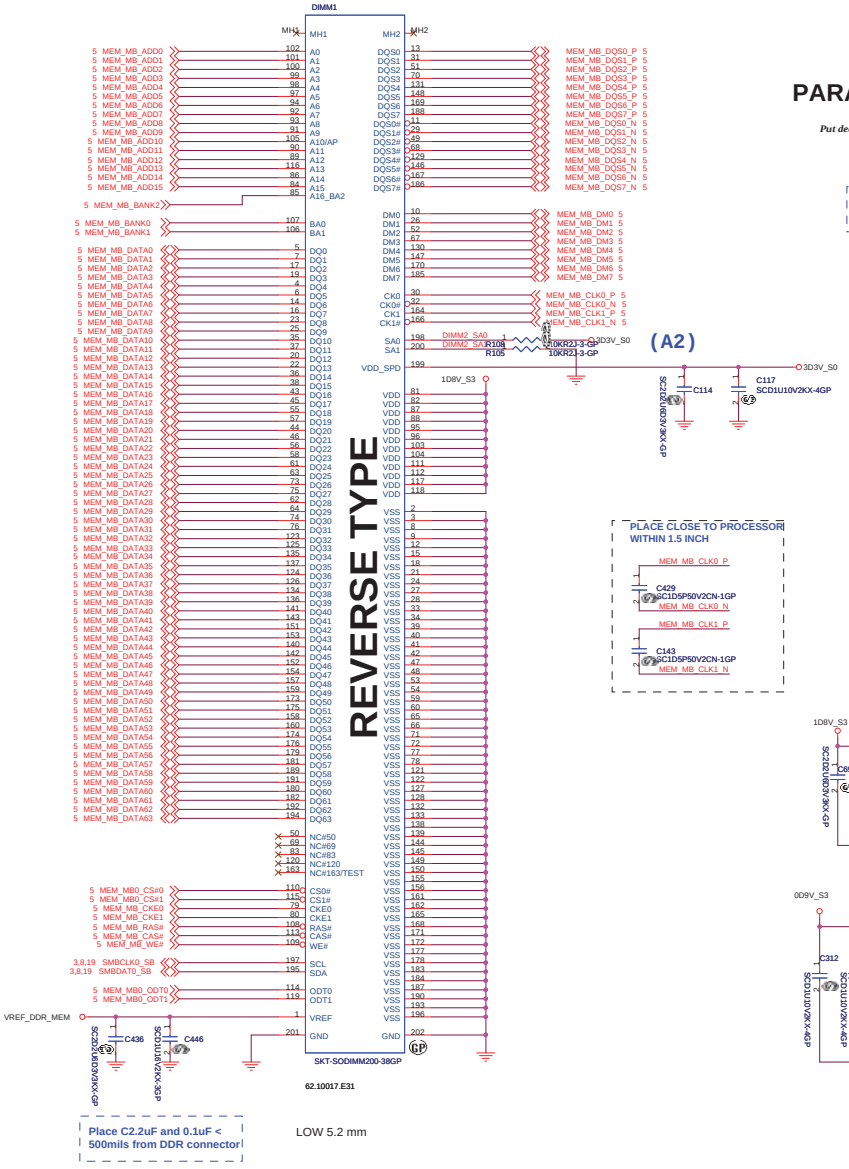
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DIMM1**

Size	Document Number	Rev
A2	P1/P15	SA

Date: Wednesday, March 19, 2008 Sheet 8 of 56

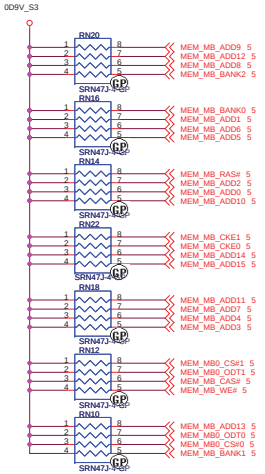
SSID = MEMORY



PARALLEL TERMINATION

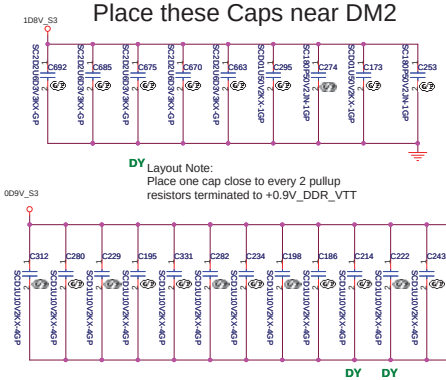
Put decap near power(0.9V) and pull-up resistor

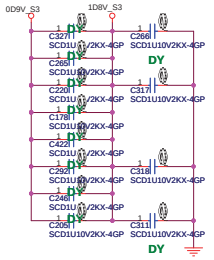
Do not share the Term resistor between the DDR addess and Control Signals.



Decoupling Capacitor

Place these Caps near DM2





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_DIMM2

Size	Document Number	Rev
A2	P1/P15	SA

Date: Wednesday, March 19, 2008 Sheet 9 of 56

SSID = N.B

U61A

PART 1 OF 6 — HYPER TRANSPORT CPU I/F

4 HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0 4
4 HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0 4
4 HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1 4
4 HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1 4
4 HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2 4
4 HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2 4
4 HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3 4
4 HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3 4
4 HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4 4
4 HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4 4
4 HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5 4
4 HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5 4
4 HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6 4
4 HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6 4
4 HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7 4
4 HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7 4
4 HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8 4
4 HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8 4
4 HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9 4
4 HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9 4
4 HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10 4
4 HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10 4
4 HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11 4
4 HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11 4
4 HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12 4
4 HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12 4
4 HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13 4
4 HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13 4
4 HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14 4
4 HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14 4
4 HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15 4
4 HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15 4
4 HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0 4
4 HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0 4
4 HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1 4
4 HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1 4
4 HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0 4
4 HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0 4
4 HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1 4
4 HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1 4
		HT_RXCALP	HT_TXCALP	B24	HT_NB_CPU_CLK_H0 4
		HT_RXCALN	HT_TXCALN	B25	HT_NB_CPU_CLK_L0 4

RS780M-GP-U1

1 R421 301R2F-GP HT_RXCALP C23 HT_RXCALN A24

Place < 100mils from pin C23 and A24

1 R419 301R2F-GP HT_TXCALP B24 HT_TXCALN B25

Place < 100mils from pin B25 and B24

Placement: close RS780

UMA DVI

GFX_TX15P_C	C405 1	UMA	SCD1U10V2KX-4GP	DVI_TXAOUT2+ 17
GFX_TX15N_C	C406 1	UMA	SCD1U10V2KX-4GP	DVI_TXAOUT2- 17
GFX_TX14P_C	C403 1	UMA	SCD1U10V2KX-4GP	DVI_TXAOUT1+ 17
GFX_TX14N_C	C404 1	UMA	SCD1U10V2KX-4GP	DVI_TXAOUT1- 17
GFX_TX13P_C	C400 1	UMA	SCD1U10V2KX-4GP	DVI_TXAOUT0+ 17
GFX_TX13N_C	C399 1	UMA	SCD1U10V2KX-4GP	DVI_TXAOUT0- 17
GFX_TX12P_C	C396 1	UMA	SCD1U10V2KX-4GP	DVI_TXACLK+ 17
GFX_TX12N_C	C397 1	UMA	SCD1U10V2KX-4GP	DVI_TXACLK- 17

Rx PCIE reversed

Tx PCIE reversed

U61B

PART 2 OF 6 — PCIE I/F GFX

48 PCIE_MXM_NB_RX15P	D4	GFX_RX0P	GFX_TX0P	A5	GFX_TX15P_C C729 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX15P 48
48 PCIE_MXM_NB_RX15N	C4	GFX_RX0N	GFX_TX0N	B5	GFX_TX15N_C C728 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX15N 48
48 PCIE_MXM_NB_RX14P	A3	GFX_RX1P	GFX_TX1P	A4	GFX_TX14P_C C727 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX14P 48
48 PCIE_MXM_NB_RX14N	B3	GFX_RX1N	GFX_TX1N	B4	GFX_TX14N_C C726 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX14N 48
48 PCIE_MXM_NB_RX13P	C2	GFX_RX2P	GFX_TX2P	C3	GFX_TX13P_C C724 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX13P 48
48 PCIE_MXM_NB_RX13N	C1	GFX_RX2N	GFX_TX2N	B2	GFX_TX13N_C C725 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX13N 48
48 PCIE_MXM_NB_RX12P	E3	GFX_RX3P	GFX_TX3P	D1	GFX_TX12P_C C721 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX12P 48
48 PCIE_MXM_NB_RX12N	F5	GFX_RX3N	GFX_TX3N	D2	GFX_TX12N_C C720 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX12N 48
48 PCIE_MXM_NB_RX11P	G5	GFX_RX4P	GFX_TX4P	E2	GFX_TX11P_C C718 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX11P 48
48 PCIE_MXM_NB_RX11N	G6	GFX_RX4N	GFX_TX4N	E1	GFX_TX11N_C C717 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX11N 48
48 PCIE_MXM_NB_RX10P	H5	GFX_RX5P	GFX_TX5P	F4	GFX_TX10P_C C361 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX10P 48
48 PCIE_MXM_NB_RX10N	H6	GFX_RX5N	GFX_TX5N	F3	GFX_TX10N_C C350 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX10N 48
48 PCIE_MXM_NB_RX9P	J6	GFX_RX6P	GFX_TX6P	F1	GFX_TX9P_C C712 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX9P 48
48 PCIE_MXM_NB_RX9N	J5	GFX_RX6N	GFX_TX6N	F2	GFX_TX9N_C C715 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX9N 48
48 PCIE_MXM_NB_RX8P	J7	GFX_RX7P	GFX_TX7P	H4	GFX_TX8P_C C338 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX8P 48
48 PCIE_MXM_NB_RX8N	J8	GFX_RX7N	GFX_TX7N	H3	GFX_TX8N_C C328 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX8N 48
48 PCIE_MXM_NB_RX7P	L5	GFX_RX8P	GFX_TX8P	H1	GFX_TX7P_C C705 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX7P 48
48 PCIE_MXM_NB_RX7N	L6	GFX_RX8N	GFX_TX8N	H2	GFX_TX7N_C C708 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX7N 48
48 PCIE_MXM_NB_RX6P	M8	GFX_RX9P	GFX_TX9P	J2	GFX_TX6P_C C704 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX6P 48
48 PCIE_MXM_NB_RX6N	L8	GFX_RX9N	GFX_TX9N	J1	GFX_TX6N_C C702 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX6N 48
48 PCIE_MXM_NB_RX5P	P7	GFX_RX10P	GFX_TX10P	K4	GFX_TX5P_C C298 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX5P 48
48 PCIE_MXM_NB_RX5N	M7	GFX_RX10N	GFX_TX10N	K3	GFX_TX5N_C C288 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX5N 48
48 PCIE_MXM_NB_RX4P	P5	GFX_RX11P	GFX_TX11P	K1	GFX_TX4P_C C695 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX4P 48
48 PCIE_MXM_NB_RX4N	M5	GFX_RX11N	GFX_TX11N	K2	GFX_TX4N_C C701 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX4N 48
48 PCIE_MXM_NB_RX3P	R8	GFX_RX12P	GFX_TX12P	M4	GFX_TX3P_C C694 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX3P 48
48 PCIE_MXM_NB_RX3N	P8	GFX_RX12N	GFX_TX12N	M3	GFX_TX3N_C C690 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX3N 48
48 PCIE_MXM_NB_RX2P	R6	GFX_RX13P	GFX_TX13P	M1	GFX_TX2P_C C268 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX2P 48
48 PCIE_MXM_NB_RX2N	R5	GFX_RX13N	GFX_TX13N	M2	GFX_TX2N_C C267 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX2N 48
48 PCIE_MXM_NB_RX1P	P4	GFX_RX14P	GFX_TX14P	N2	GFX_TX1P_C C682 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX1P 48
48 PCIE_MXM_NB_RX1N	P3	GFX_RX14N	GFX_TX14N	N1	GFX_TX1N_C C687 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX1N 48
48 PCIE_MXM_NB_RX0P	T4	GFX_RX15P	GFX_TX15P	P1	GFX_TX0P_C C679 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX0P 48
48 PCIE_MXM_NB_RX0N	T3	GFX_RX15N	GFX_TX15N	P2	GFX_TX0N_C C681 1 VGA SCD1U10V2KX-4GP PCIE_NB_MXM_TX0N 48

Placement: close RS780

PCIE I/F GPP

NEW / WLAN / LAN / CARD

24 PCIE_NBRX_NEWTX_P0	AE3	GPP_RX0P	GPP_TX0P	AC1	PCIE_NBTX_NEWRX_P0 C648 1 SCD1U10V2KX-4GP PCIE_NBTX_C_NEWRX_P0 24
24 PCIE_NBRX_NEWTX_N0	AD4	GPP_RX0N	GPP_TX0N	AC2	PCIE_NBTX_NEWRX_N0 C642 1 SCD1U10V2KX-4GP PCIE_NBTX_C_NEWRX_N0 24
24 PCIE_NBRX_WLANTX_P1	AE2	GPP_RX1P	GPP_TX1P	AB4	PCIE_NBTX_WLANRX_P1 C658 1 SCD1U10V2KX-4GP PCIE_NBTX_C_WLANRX_P1 24
24 PCIE_NBRX_WLANTX_N1	AD3	GPP_RX1N	GPP_TX1N	AB3	PCIE_NBTX_WLANRX_N1 C661 1 SCD1U10V2KX-4GP PCIE_NBTX_C_WLANRX_N1 24
25 PCIE_NBRX_LANTX_P2	AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_NBTX_LANRX_P2 C665 1 SCD1U10V2KX-4GP PCIE_NBTX_C_LANRX_P2 25
25 PCIE_NBRX_LANTX_N2	AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_NBTX_LANRX_N2 C660 1 SCD1U10V2KX-4GP PCIE_NBTX_C_LANRX_N2 25
28 PCIE_NBRX_CARDTX_P3	V5	GPP_RX3P	GPP_TX3P	Y1	PCIE_NBTX_CARDRX_P2 C669 1 SCD1U10V2KX-4GP PCIE_NBTX_C_CARDRX_P3 28
28 PCIE_NBRX_CARDTX_N3	W6	GPP_RX3N	GPP_TX3N	Y2	PCIE_NBTX_CARDRX_N2 C672 1 SCD1U10V2KX-4GP PCIE_NBTX_C_CARDRX_N3 28
	U5	GPP_RX4P	GPP_TX4P	Y4	
	U6	GPP_RX4N	GPP_TX4N	Y3	
	U8	GPP_RX5P	GPP_TX5P	V1	
	U7	GPP_RX5N	GPP_TX5N	V2	

A-LINK

PCIE I/F SB

18 ALINK_NBRX_SBTX_P0	AA8	SB_RX0P	SB_TX0P	AD7	ALINK_NBTX_SBRX_P0 C159 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_P0 18
18 ALINK_NBRX_SBTX_N0	Y8	SB_RX0N	SB_TX0N	AE7	ALINK_NBTX_SBRX_N0 C167 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_N0 18
18 ALINK_NBRX_SBTX_P1	AA7	SB_RX1P	SB_TX1P	AF6	ALINK_NBTX_SBRX_P1 C647 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_P1 18
18 ALINK_NBRX_SBTX_N1	Y7	SB_RX1N	SB_TX1N	AD6	ALINK_NBTX_SBRX_N1 C630 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_N1 18
18 ALINK_NBRX_SBTX_P2	AA5	SB_RX2P	SB_TX2P	AB6	ALINK_NBTX_SBRX_P2 C190 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_P2 18
18 ALINK_NBRX_SBTX_N2	AA6	SB_RX2N	SB_TX2N	AC6	ALINK_NBTX_SBRX_N2 C179 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_N2 18
18 ALINK_NBRX_SBTX_P3	W5	SB_RX3P	SB_TX3P	AD5	ALINK_NBTX_SBRX_P3 C656 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_P3 18
18 ALINK_NBRX_SBTX_N3	Y5	SB_RX3N	SB_TX3N	AE5	ALINK_NBTX_SBRX_N3 C654 1 SCD1U10V2KX-4GP ALINK_NBTX_C_SBRX_N3 18
			PCE_CALRP	AC8	PCE_PCAL
			PCE_CALRN	AB8	PCE_NCAL R126 1 1K27R2F-L-GP R139 2KR2F-3-GP 1D1V_S0

RS780M-GP-U1

Place < 100mils from pin AC8 and AB8

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M HT LINK&PCIE(1/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Wednesday, March 19, 2008 | Sheet 10 of 56

SSID = N.B

STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)

*0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

close NB within 1000 mil

Close to NB ball

ENABLE External CLK GEN

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

15mil width

15mil width

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_LVDS&CRT_(2/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Wednesday, March 19, 2008 | Sheet 11 of 56

SSID = N.B

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

1D8V_S0 — L5 BLM21PG221SN-1GP — 220 ohm @ 100MHz,2A — +1.8V_MEM_VDDQ

C102 SC22U6D3V5MX-2GP; C140 SCD1U10V2KX-4GP; C141 SCD1U10V2KX-4GP; C105 SC1U6D3V2KX-GP; C106 SC1U6D3V2KX-GP

U61D — PAR 4 OF 6 — SBD_MEM/DVO_I/F — RS780M-GP-U1

MEM_A0 AB12; MEM_A1 AE16; MEM_A2 V11; MEM_A3 AE15; MEM_A4 AA12; MEM_A5 AB16; MEM_A6 AB14; MEM_A7 AD14; MEM_A8 AD13; MEM_A9 AD15; MEM_A10 AC16; MEM_A11 AE13; MEM_A12 AC14; MEM_A13 Y14

TP8

MEM_BA0 AD16; MEM_BA1 AE17; MEM_BA2 AD17

RAS# W12; CAS# Y12; WE# AD18; CS# AB13; CKE AB18; ODT V14

MEM_CLKP V15; MEM_CLKN W14

MEM_COMPP AE12; MEM_COMPN AD12

MEM_DQ0/DVO_VSYNC AA18 MEM_DQ0; MEM_DQ1/DVO_HSYNC AA20 MEM_DQ1; MEM_DQ2/DVO_DE AA19 MEM_DQ2; MEM_DQ3/DVO_D0 Y19 MEM_DQ3; MEM_DQ4 V17 MEM_DQ4; MEM_DQ5/DVO_D1 AA17 MEM_DQ5; MEM_DQ6/DVO_D2 AA15 MEM_DQ6; MEM_DQ7/DVO_D4 Y15 MEM_DQ7; MEM_DQ8/DVO_D3 AC20 MEM_DQ8; MEM_DQ9/DVO_D5 AD19 MEM_DQ9; MEM_DQ10/DVO_D6 AE22 MEM_DQ10; MEM_DQ11/DVO_D7 AC18 MEM_DQ11; MEM_DQ12 AB20 MEM_DQ12; MEM_DQ13/DVO_D9 AD22 MEM_DQ13; MEM_DQ14/DVO_D10 AC22 MEM_DQ14; MEM_DQ15/DVO_D11 AD21 MEM_DQ15

MEM_DQS0P/DVO_IDCKP Y17 MEM_DQS0P; MEM_DQS0N/DVO_IDCKN W18 MEM_DQS0N; MEM_DQS1P AD20 MEM_DQS1P; MEM_DQS1N AE21 MEM_DQS1N

MEM_DM0 W17 MEM_DM0; MEM_DM1/DVO_D8 AE19 MEM_DM1

IOPLLVDD18 AE23 +1.8V_IOPLLVDD18; IOPLLVDD AE24 +1.1V_IOPLLVDD

IOPLLVSS AD23

MEM_VREF AE18 MEM_VREF_NB

+1.8V_MEM_VDDQ — 40D2R2F-GP R120 — R360 40D2R2F-GP

15mil width — L8 BLM15AG221SN-GP — 1D8V_S0 — C153 SC2D2U6D3V3KX-GP

15mil width — L15 BLM15AG221SN-GP — 1D1V_S0 — C187 SC2D2U6D3V3KX-GP; C182 SCD1U10V2KX-4GP

+1.8V_MEM_VDDQ — R119 1KR2F-3-GP — C152 SCD1U10V2KX-4GP; R122 1KR2F-3-GP — C188 SCD1U10V2KX-4GP

SC

U21

MEM_BA0 L2; MEM_BA1 L3

MEM_A12 R2; MEM_A11 P7; MEM_A10 M2; MEM_A9 P3; MEM_A8 P8; MEM_A7 P2; MEM_A6 N7; MEM_A5 N3; MEM_A4 N8; MEM_A3 N2; MEM_A2 M7; MEM_A1 M3; MEM_A0 M8

ATI DY — DY — R116 100R2F-L1-GP-U

MEM_CLKN K8; MEM_CLKP J8

CKE K2

CS# L8; WE# K3; RAS# K7; CAS# L7

MEM_DM0 F3; MEM_DM1 B3

ODT K9

MEM_DQS0P F7; MEM_DQS0N F8

MEM_DQS1P B7; MEM_DQS1N A8

MEM_VREF_CHIP J2

MEM_BA2 L1

DQ15 B9 MEM_DQ15; DQ14 B1 MEM_DQ14; DQ13 D9 MEM_DQ13; DQ12 D1 MEM_DQ12; DQ11 D3 MEM_DQ11; DQ10 D7 MEM_DQ10; DQ9 C2 MEM_DQ9; DQ8 C8 MEM_DQ8; DQ7 F9 MEM_DQ7; DQ6 F1 MEM_DQ6; DQ5 H9 MEM_DQ5; DQ4 H1 MEM_DQ4; DQ3 H3 MEM_DQ3; DQ2 H7 MEM_DQ2; DQ1 G2 MEM_DQ1; DQ0 G8 MEM_DQ0

+1.8V_MEM_VDDQ — VDDQ1 A9; VDDQ2 C1; VDDQ3 C3; VDDQ4 C7; VDDQ5 C9; VDDQ6 F9; VDDQ7 G1; VDDQ8 G3; VDDQ9 G7; VDDQ10 G9

VDD1 A1; VDD2 E1; VDD3 J9; VDD4 M9; VDD5 R1

L4 BLM18AG601SN-3GP — 600 ohm @ 100MHz,200mA

VDDL_VRAM — VDDL J1; VSSDL J7

Layout Note: 50 mil for VSSDL

C103 SC1U6D3V3KX-1GP

VSSQ1 A7; VSSQ2 B2; VSSQ3 B8; VSSQ4 D2; VSSQ5 D8; VSSQ6 E7; VSSQ7 F2; VSSQ8 F8; VSSQ9 H2; VSSQ10 H8

VSS1 A3; VSS2 E3; VSS3 J3; VSS4 N1; VSS5 P9

NC#A2 A2; NC#E2 E2; NC#L1 L1; NC#R3 R3; NC#R7 R7; NC#R8 R8

+1.8V_MEM_VDDQ — R93 1KR2F-3-GP — C100 SCD1U10V2KX-4GP — R100 1KR2F-3-GP — C104 SCD1U10V2KX-4GP

HYB18T512161B2F-25-GP

72.18512.M0U

<Variant Name>

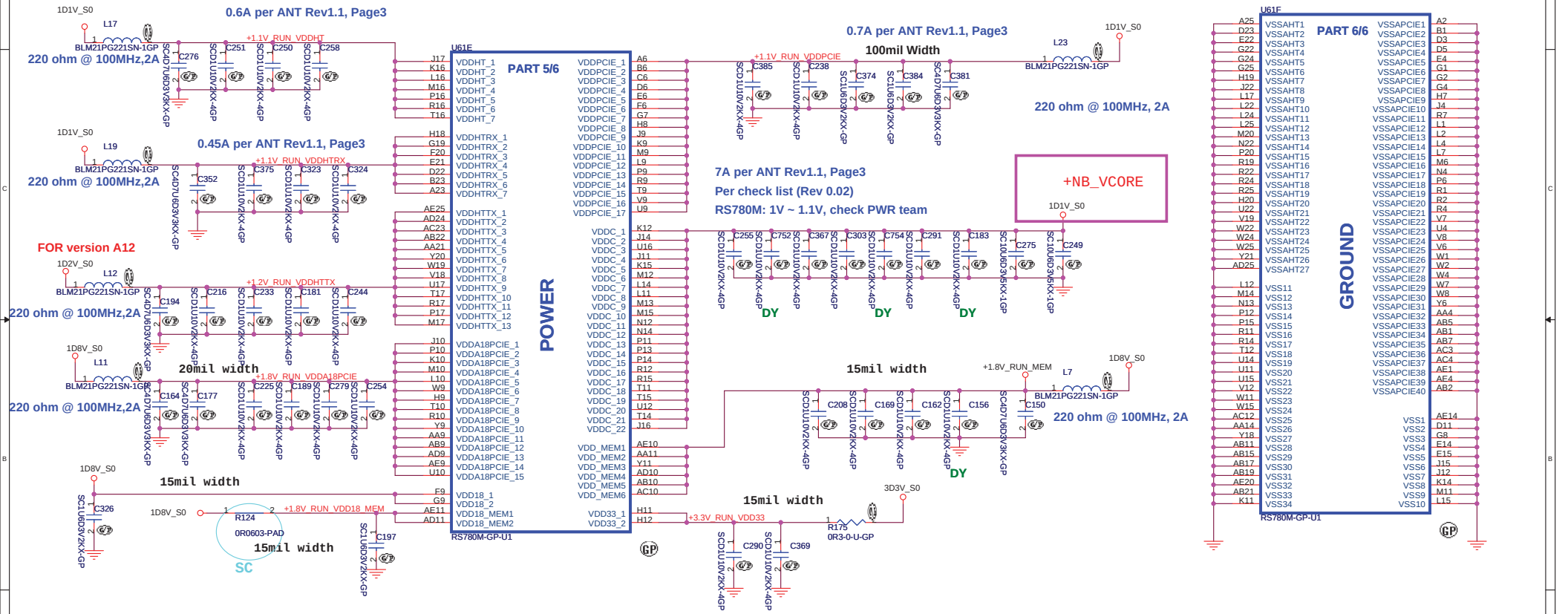
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_SidePort_(3/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Wednesday, March 19, 2008 | Sheet 12 of 56

SSID = N.B



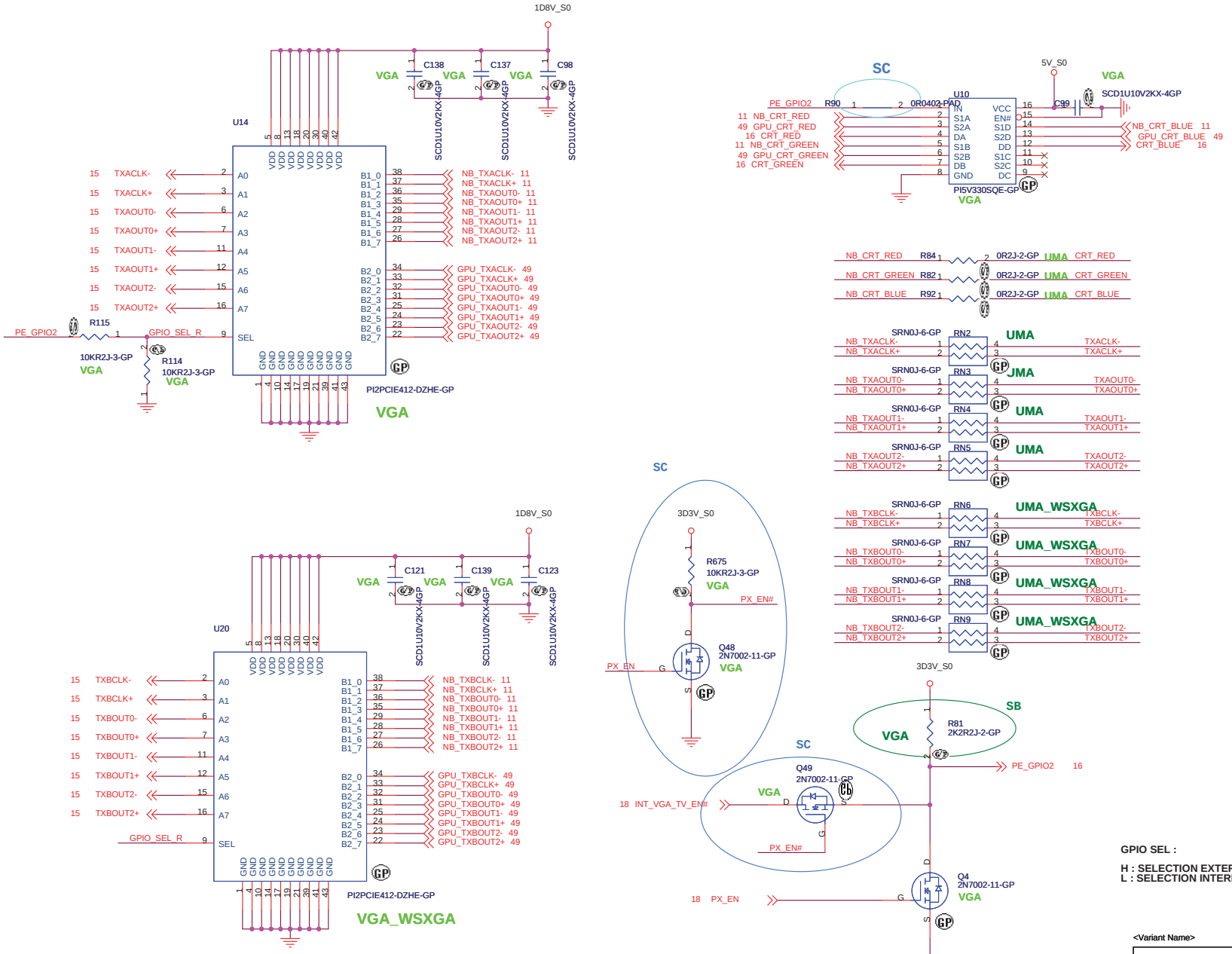
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

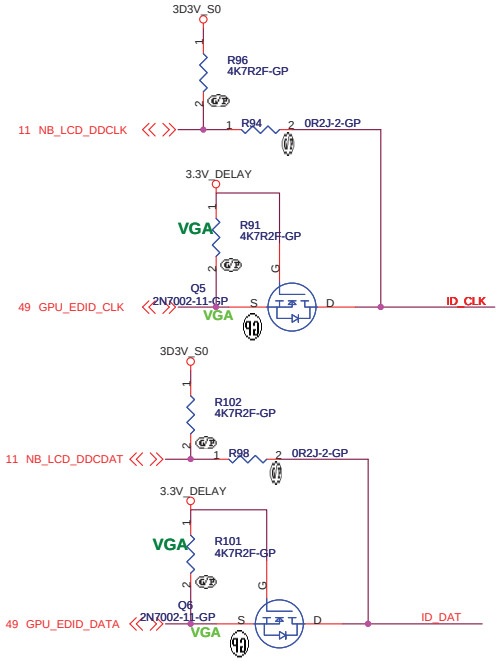
Title: **ATi-RS780M_PWR&GD_(4/4)**

Size	Document Number	Rev
A3	P1/P15	SA

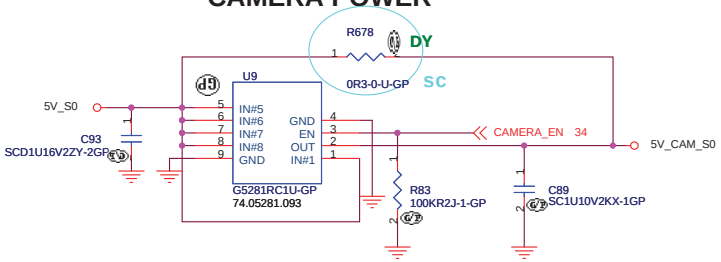
Date: Wednesday, March 19, 2008 Sheet 13 of 56

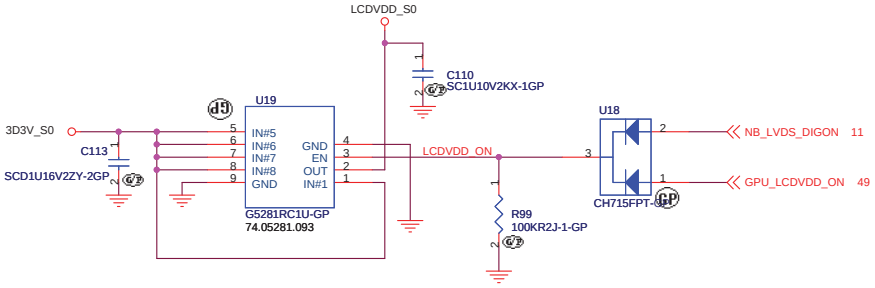


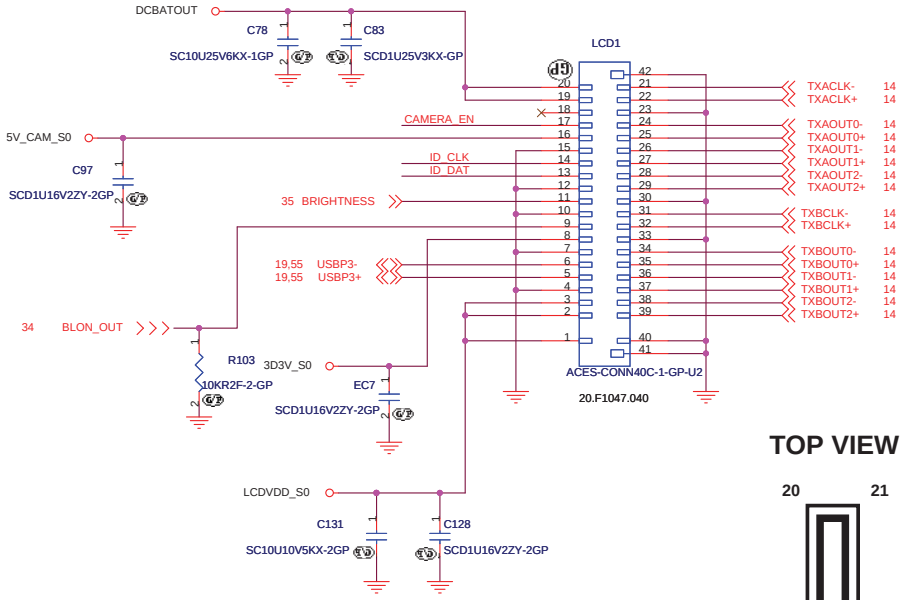
LCD CONNECTOR



CAMERA POWER







TOP VIEW

<Variant Name>

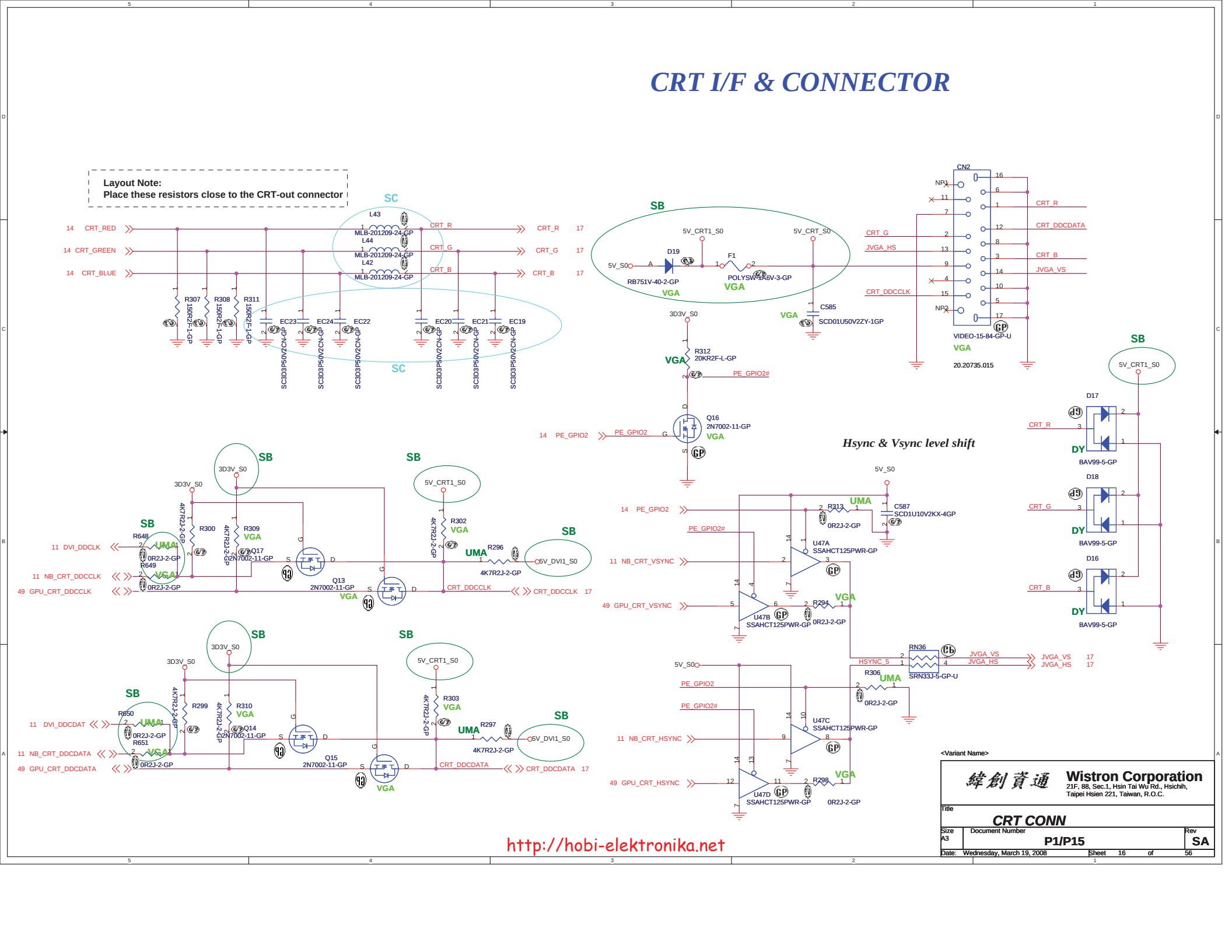
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN/CAMERA**

Size	Document Number	Rev
A3	P1/P15	SA

Date: Wednesday, March 19, 2008 Sheet 15 of 56

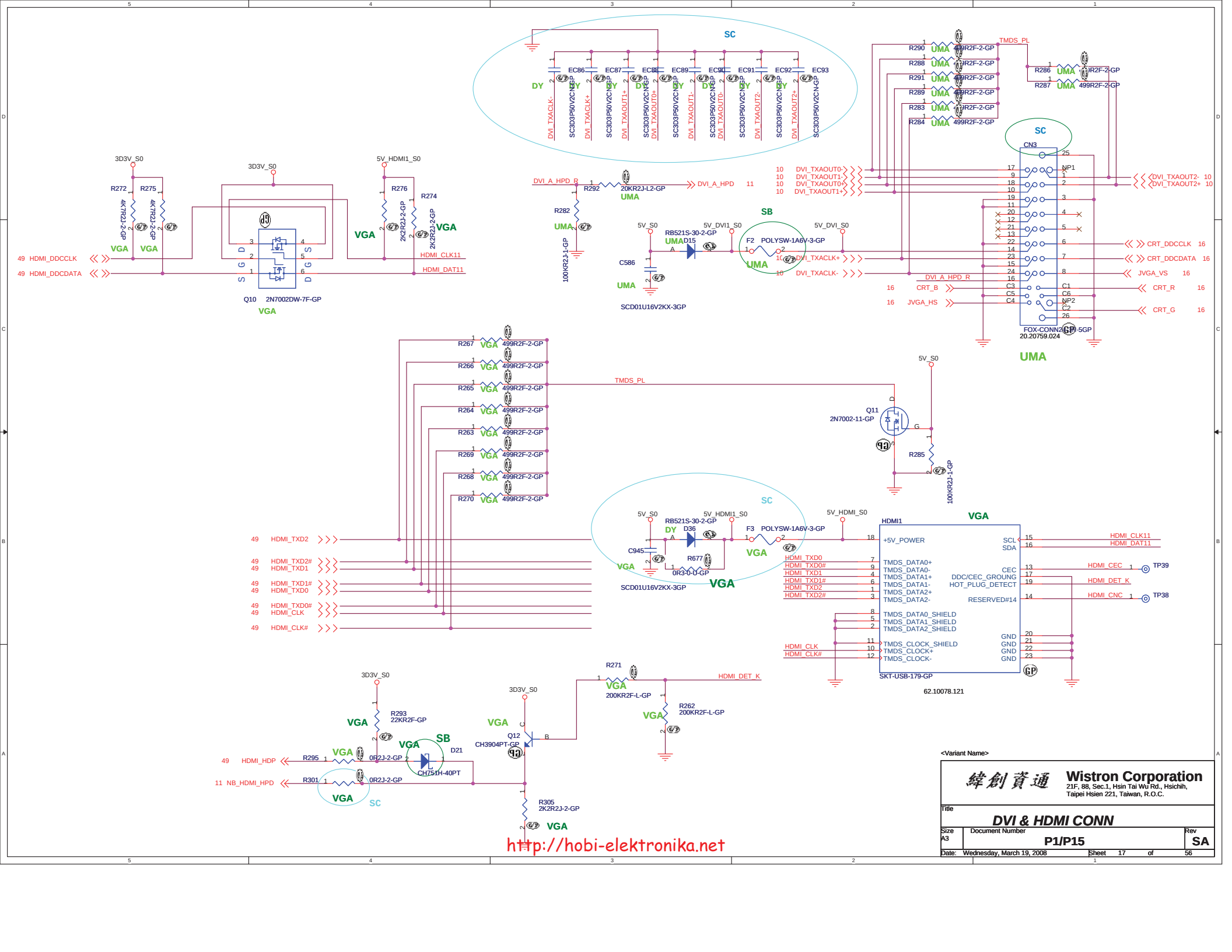
CRT I/F & CONNECTOR



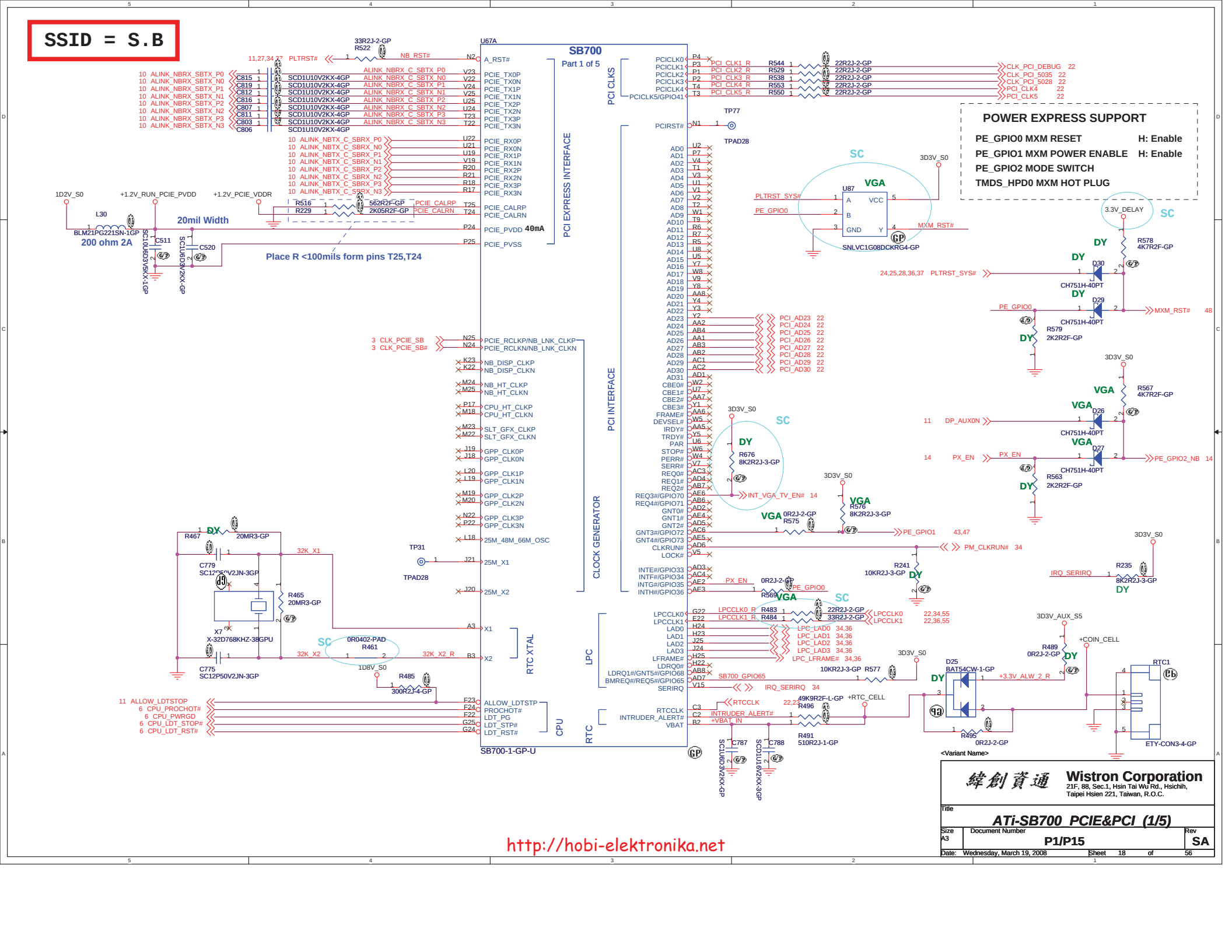
http://hobi-elektronika.net

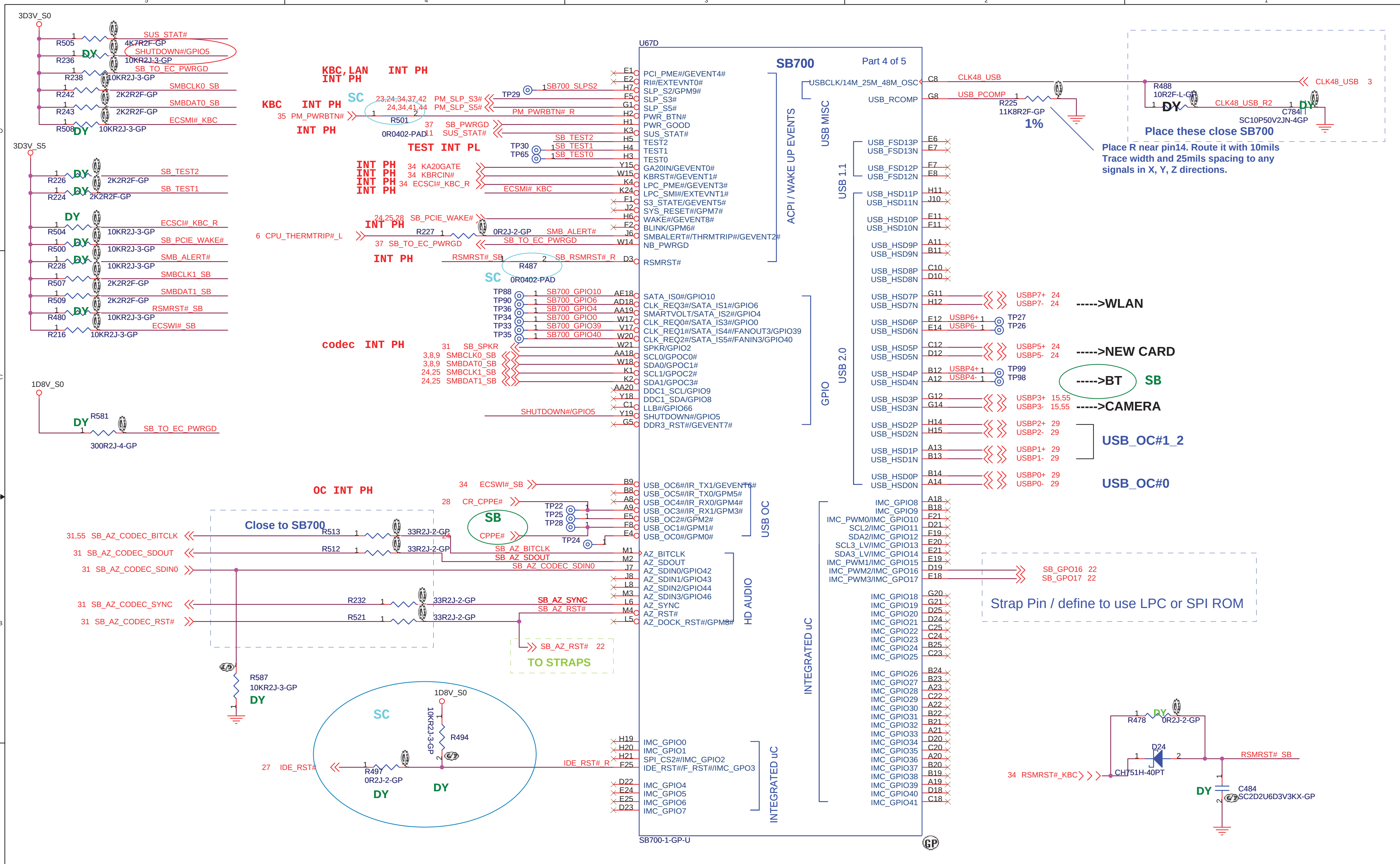
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CRT CONN		
Size: A3	Document Number: P1/P15	Rev: SA
Date: Wednesday, March 19, 2008	Sheet 16 of 56	


SC
DY
EC86
EC87
EC88
EC89
EC90
EC91
EC92
EC93
SC3303P50V2CN-GP
DVI_TXACLK-
DVI_TXACLK+
DVI_TXAOUT1+
DVI_TXAOUT0+
DVI_TXAOUT1-
DVI_TXAOUT0-
DVI_TXAOUT2-
DVI_TXAOUT2+
TMDS_PL
R290
R288
R291
R289
R283
R284
R286
R287
UMA
499R2F-2-GP
3D3V_S0
5V_HDMI1_S0
R272
R275
4K7R2J-2-GP
VGA
R276
R274
2K2R2J-2-GP
Q10
2N7002DW-7F-GP
HDMI_DDCCLK
HDMI_DDCDATA
HDMI_CLK11
HDMI_DAT11
DVI_A_HPD_B
R292
20KR2J-L2-GP
DVI_A_HPD
R282
100KR2J-1-GP
5V_S0
5V_DVI1_S0
5V_DVI_S0
RB521S-30-2-GP
D15
F2
POLYSW-1A6V-3-GP
SB
C586
SCD01U16V2KX-3GP
CN3
FOX-CONN2GP-5GP
20.20759.024
CRT_DDCCLK
CRT_DDCDATA
JVGA_VS
CRT_R
CRT_G
CRT_B
JVGA_HS
R267
R266
R265
R264
R263
R269
R268
R270
HDMI_TXD2
HDMI_TXD2#
HDMI_TXD1
HDMI_TXD1#
HDMI_TXD0
HDMI_TXD0#
HDMI_CLK
HDMI_CLK#
Q11
2N7002-11-GP
R285
100KR2J-1-GP
D36
F3
C945
R677
0R3-0-U-GP
HDMI1
+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND
SKT-USB-179-GP
62.10078.121
HDMI_CEC
HDMI_DET_K
HDMI_CNC
TP39
TP38
R293
22KR2F-GP
R295
0R2J-2-GP
HDMI_HDP
R301
NB_HDMI_HPD
D21
CH751H-40PT
Q12
CH3904PT-GP
R271
200KR2F-L-GP
R262
R305
2K2R2J-2-GP
http://hobi-elektronika.net
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DVI & HDMI CONN
Size
A3
Document Number
P1/P15
Rev
SA
Date: Wednesday, March 19, 2008
Sheet 17 of 56

SSID = S.B


SB700
Part 1 of 5
U67A
SB700-1-GP-U
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
Place R <100mils form pins T25,T24
20mil Width
200 ohm 2A
SNLVC1G08DCKRG4-GP
CH751H-40PT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_PCIE&PCI_(1/5)
P1/P15
SA
Wednesday, March 19, 2008
http://hobi-elektronika.net

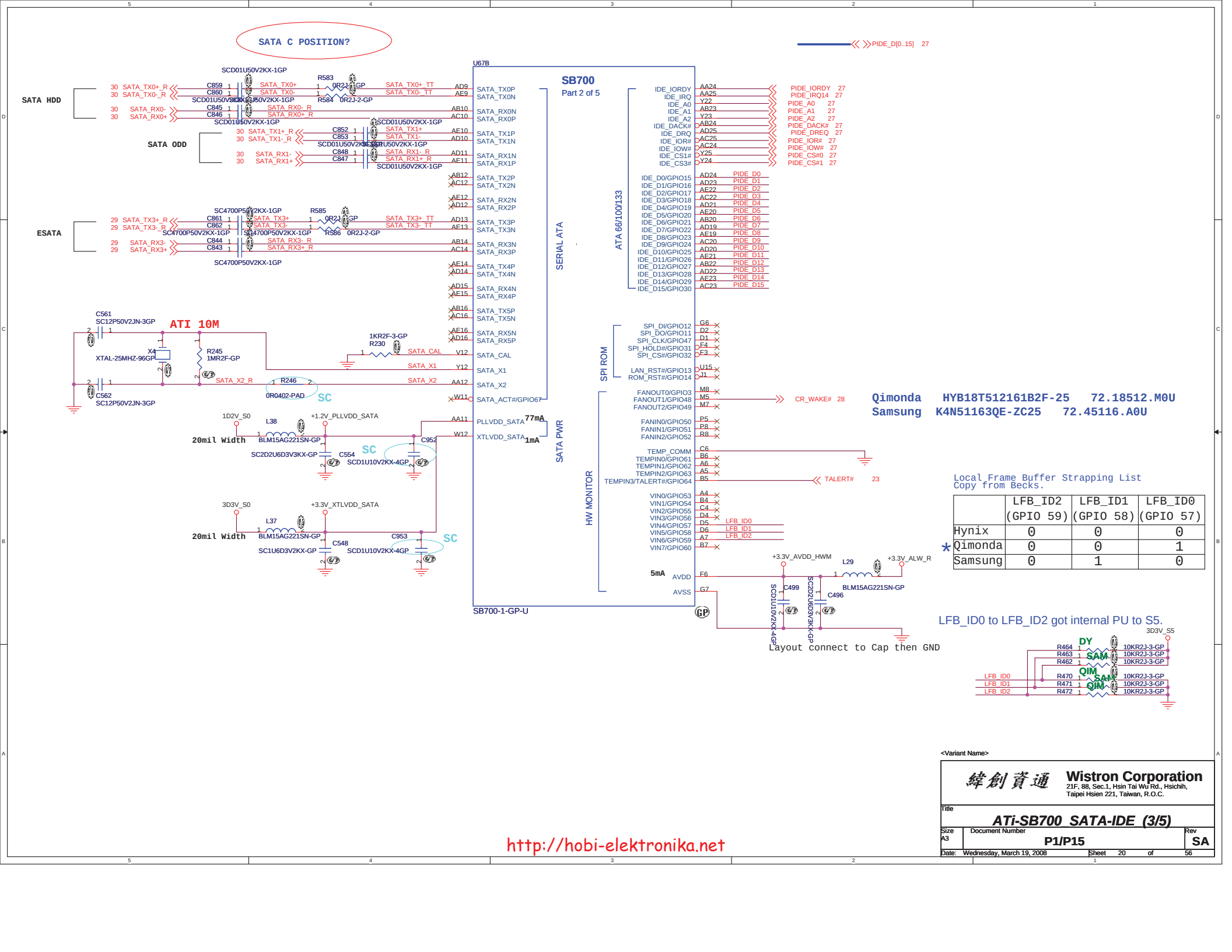


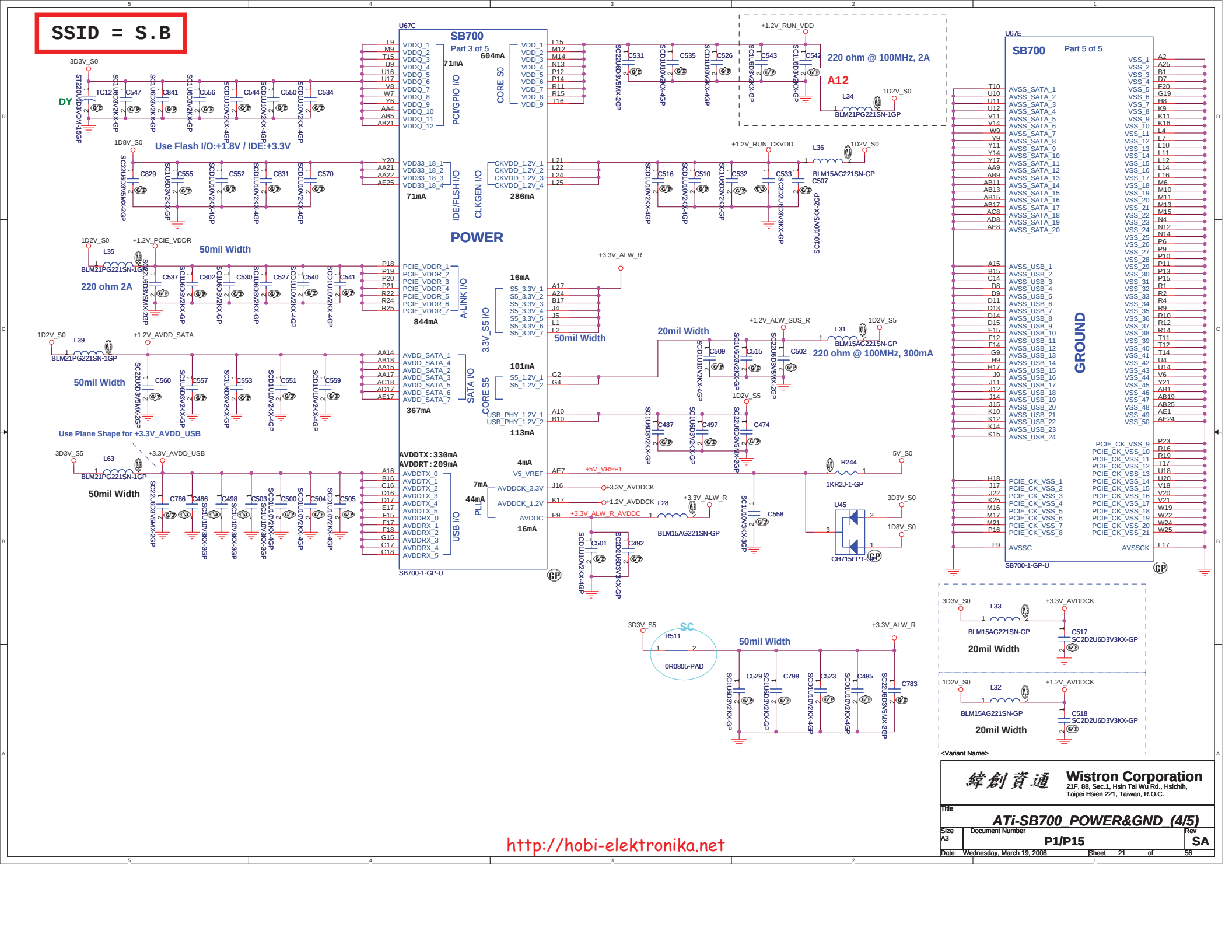
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATi-SB700_USB&GPIO_(2/5)	
Size A3	Document Number P1/P15	Rev SA
Date: Wednesday, March 19, 2008	Sheet 19 of 56	

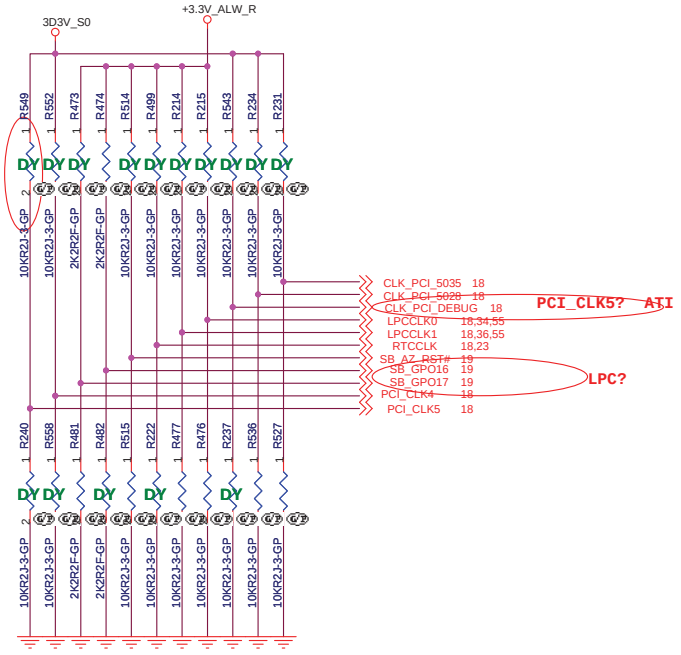
http://hobi-elektronika.net


SATA C POSITION?
SATA HDD
SATA ODD
ESATA
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
HW MONITOR
SATA PWR
ATI 10M
SB700-1-GP-U
Qimonda HYB18T512161B2F-25 72.18512.M0U
Samsung K4N51163QE-ZC25 72.45116.A0U
Local Frame Buffer Strapping List
Copy from Becks.
LFB_ID2 (GPIO 59) | LFB_ID1 (GPIO 58) | LFB_ID0 (GPIO 57)
Hynix 0 0 0
*Qimonda 0 0 1
Samsung 0 1 0
LFB_ID0 to LFB_ID2 got internal PU to S5.
Layout connect to Cap then GND
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_SATA-IDE_(3/5)
P1/P15
Wednesday, March 19, 2008


SSID = S.B
U67C
SB700
Part 3 of 5
SB700-1-GP-U
POWER
DY
Use Flash I/O:+1.8V / IDE:+3.3V
Use Plane Shape for +3.3V_AVDD_USB
50mil Width
220 ohm 2A
220 ohm @ 100MHz, 2A
220 ohm @ 100MHz, 300mA
A12
20mil Width
U67E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U
SC
0R0805-PAD
<Variant Name>
http://hobi-elektronika.net
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_POWER&GND_(4/5)
Size A3
Document Number
P1/P15
Rev SA
Date: Wednesday, March 19, 2008
Sheet 21 of 56

SSID = S.B

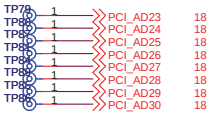
REQUIRED STRAPS



REQUIRED SYSTEM STRAPS

DEBUG STRAPS

NEED?



	CLK_PCI_5035	CLK_PCI_5028	CLK_PCI_DEBUG	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17 , SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

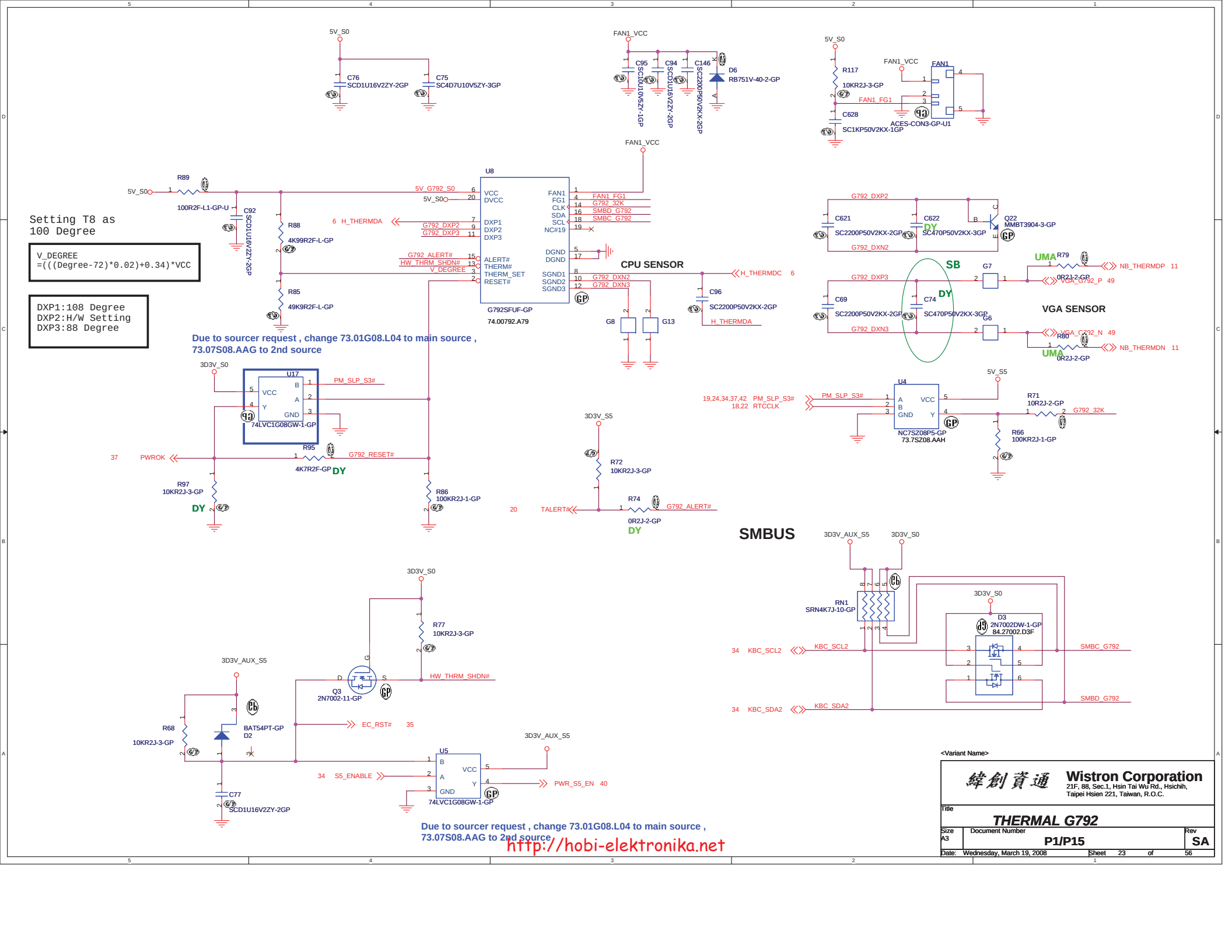
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

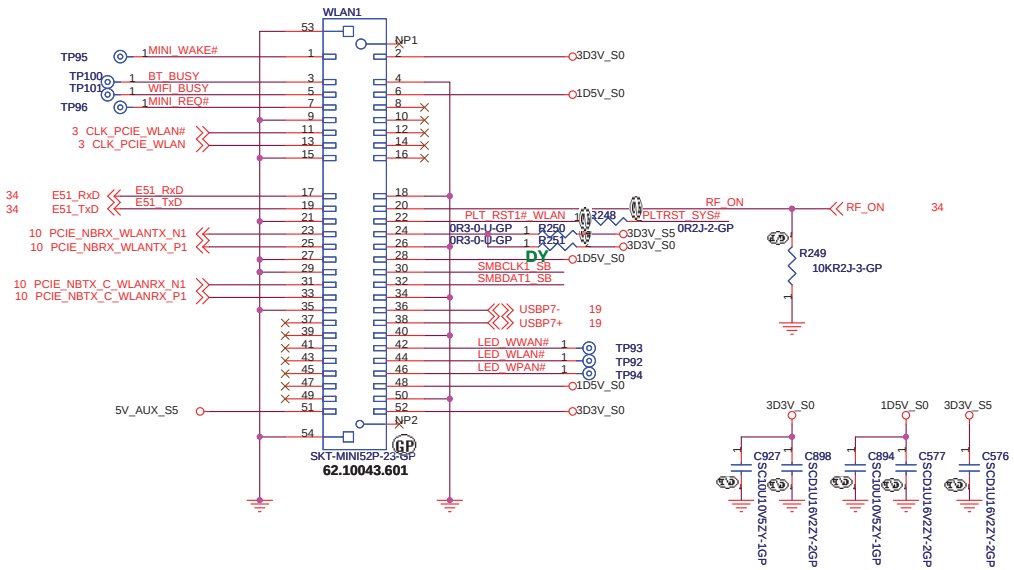
Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: P1/P15 | Rev: SA

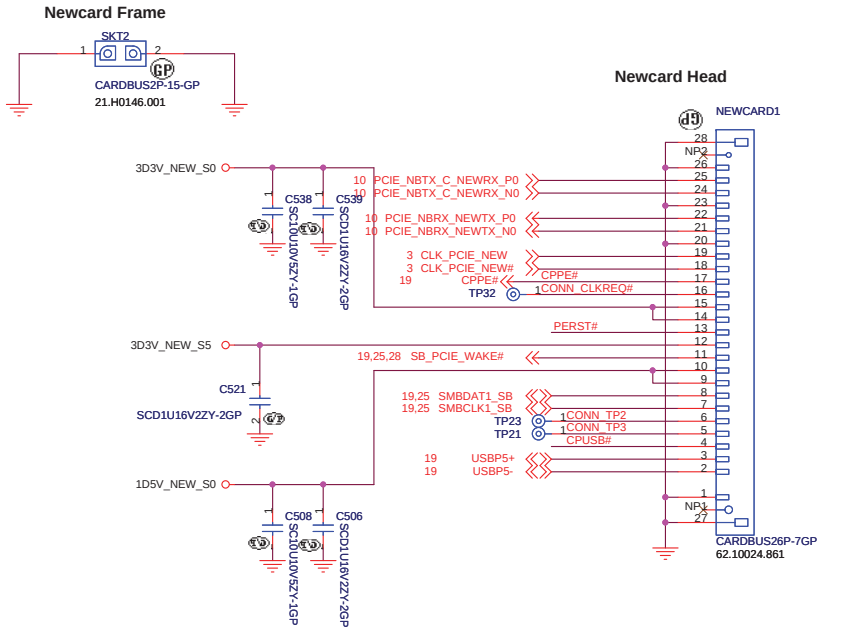
Date: Wednesday, March 19, 2008 | Sheet 22 of 56


Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
CPU SENSOR
VGA SENSOR
SMBUS
Due to sourcer request , change 73.01G08.L04 to main source ,
73.07S08.AAG to 2nd source
Due to sourcer request , change 73.01G08.L04 to main source ,
73.07S08.AAG to 2nd source
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
THERMAL G792
P1/P15
SA
Wednesday, March 19, 2008

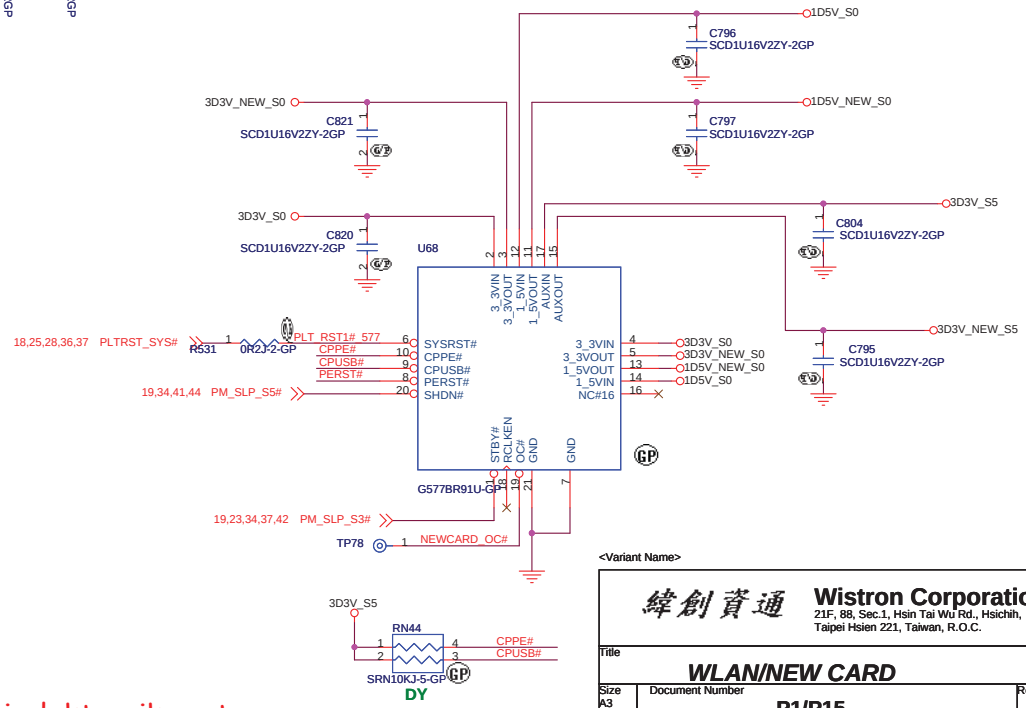
WLAN Connector



NEWCARD Connector



Place them Near to Chip



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WLAN/NEW CARD	
Size A3	Document Number P1/P15	Rev SA
Date: Wednesday, March 19, 2008	Sheet 24 of 56	

UMA 8101E 71.08101.B0G
DIS 8111C 71.08111.E03
8102E 71.08102.003

3D3V_S5 — 60 ~ 100 mils — G3 GAP-CLOSE-PWR — 60 ~ 100 mils — 3D3V_LAN_S5

Power domain chart

	RTL8111B / RTL8101E	RTL8111C/ RTL8102E
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

RTL8111B	Q3 Need	Q5 Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A
RTL8102E	N/A	N/A

EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)

Pin 63 should be near 0.1u F(C494) then 22u F(C493).

The trace width from VDD33 to pin63 should>40mils

The trace length between L39 and 8111C pin1 must be within 200mil.

C471,C472,C473, and C474 as close as possible to RTL8111C

C469 close L39 200mil.

Power plan for pin1

Pin1 should be near inductor(4.7u H,L39) then 22u F(C469) then 0.1u F(C470).

8101E REMOVE
8111B REMOVE
8111C STUFF

8111B STUFF CAP
8111C REMOVE CAP

8111C/8102E 2.49K 64.24915.6DL
8101E 2K 64.20015.6DL

They are for U49 AVDD33 pin-2 and 59

They are for U49 VDD33 pin-16,37,46 and 53

They are for U49 AVDD18 pin-5,8,11 and 14

They are for U49 EVDD18 pin-22 and 28

They are for U49 DVDD15 pin-15,21,32,33,38,41,43,49,52 and 58

8101E/8111B STUFF
8111C REMOVE

8111B STUFF
8111C REMOVE

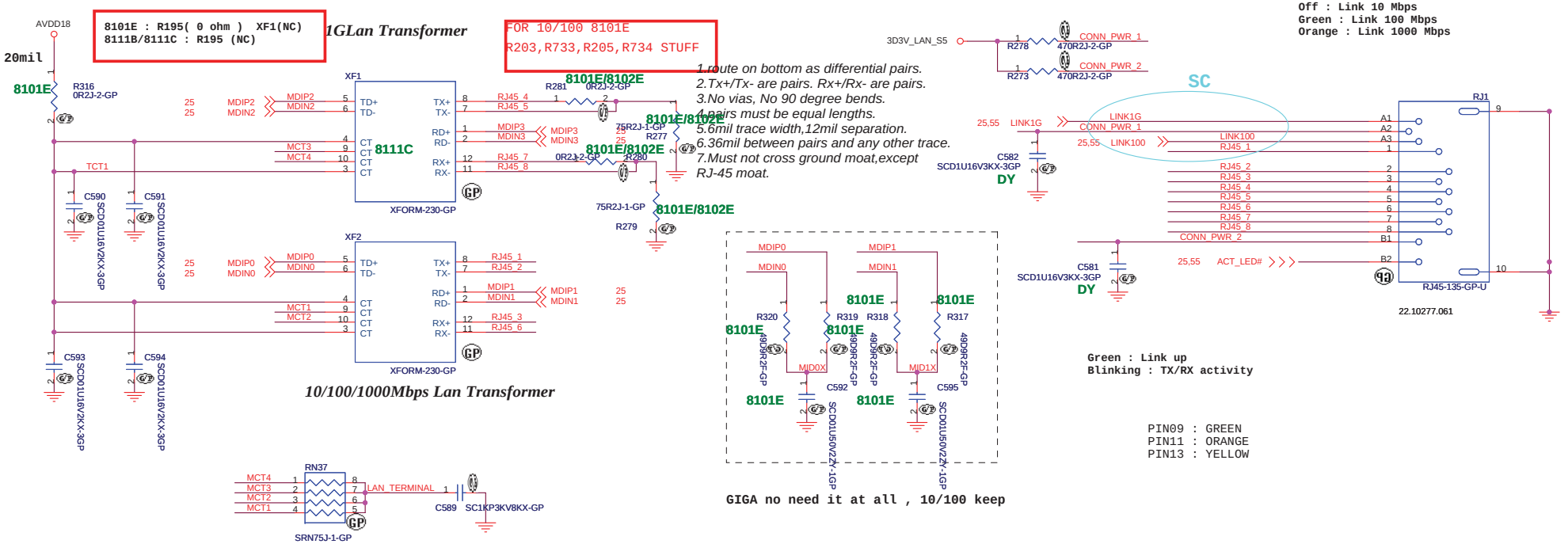
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN 8111C/8101E

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Wednesday, March 19, 2008 | Sheet 25 of 56



UMA 8101E 71.08101.B0G
DIS 8111C 71.08111.E03
8102E 71.08102.003

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	P1/P15	SA

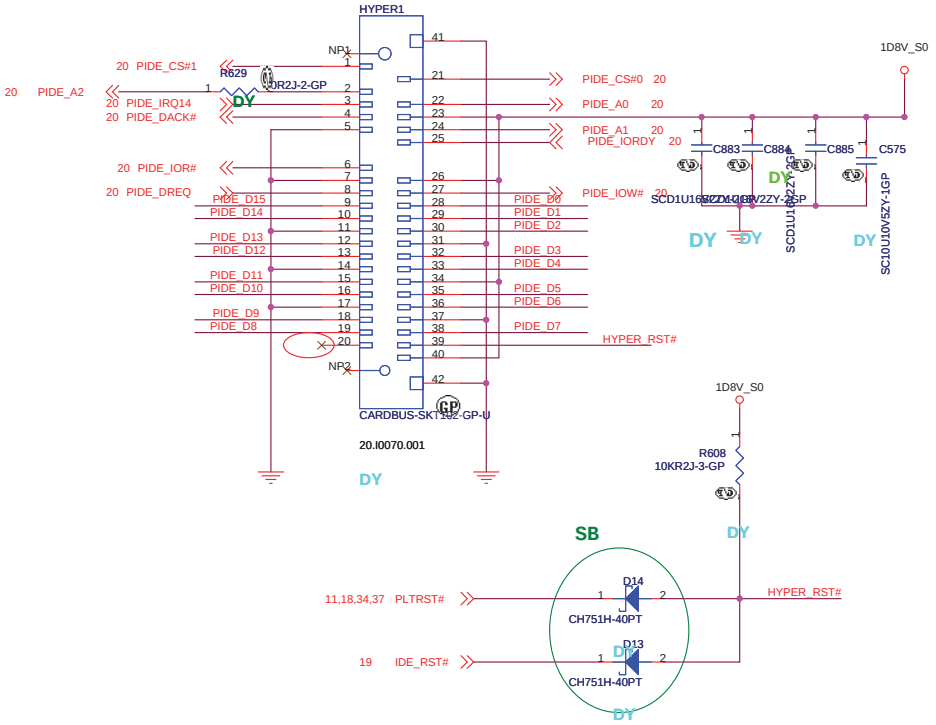
Date: Wednesday, March 19, 2008 Sheet 26 of 56

HYPER FLASH

SB DELETE Bluetooth

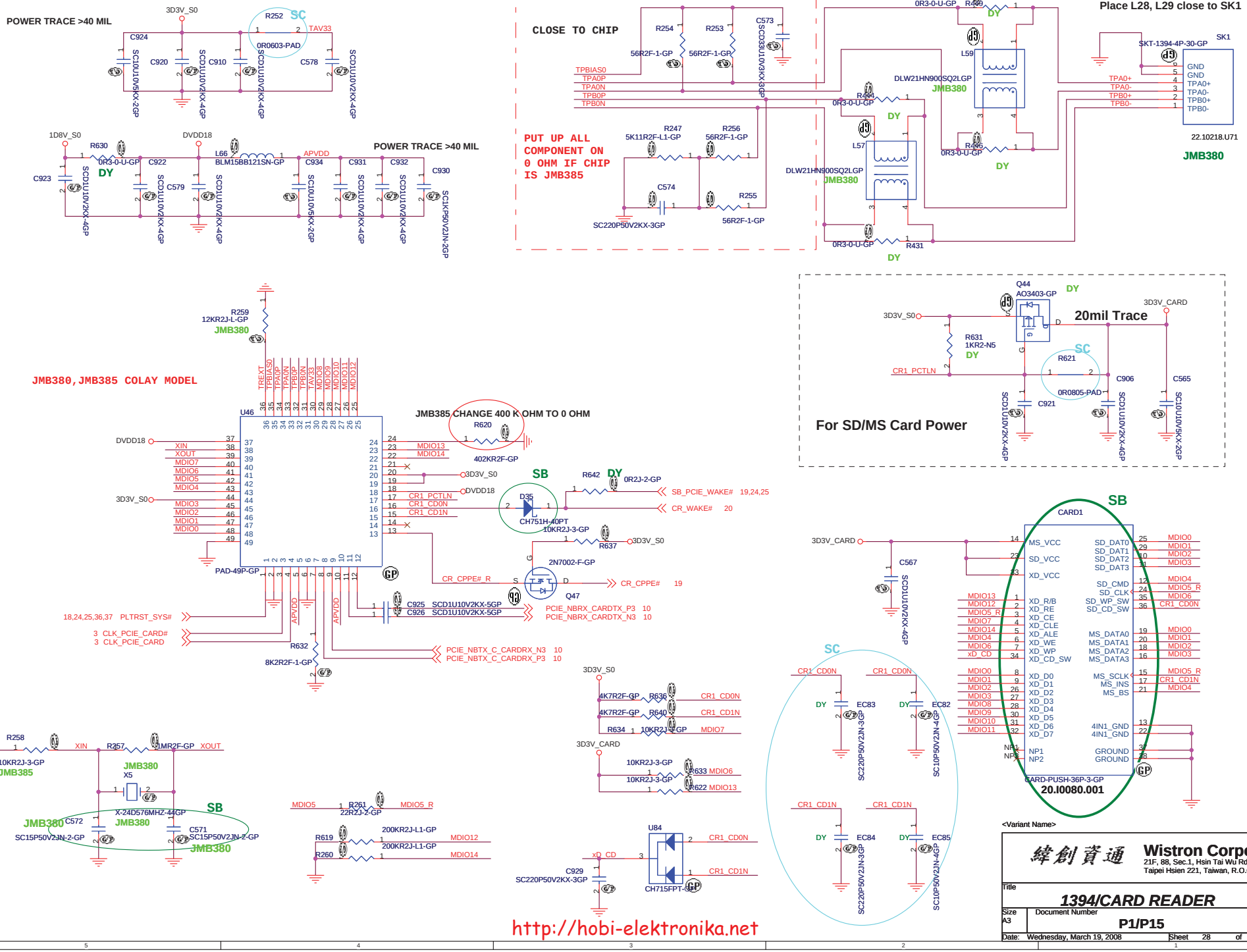
20 PIDE_D[0..15]

SC DY HYPERFLASH FUNCTION



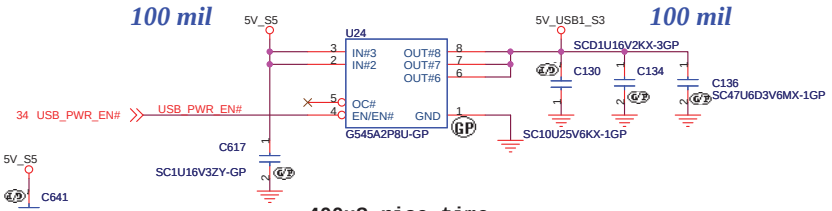
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HYPER FLASH/BT
Size A3 / Document Number	P1/P15 / Rev SA
Date: Wednesday, March 19, 2008	Sheet 27 of 56


POWER TRACE >40 MIL
3D3V_S0
R252
SC
TAV33
0R0603-PAD
C924
C920
C910
C578
SC10U10V5KX-2GP
SCD1U10V2KX-4GP
1D8V_S0
DVDD18
R630
0R3-0-U-GP
DY
L66
BLM15BB121SN-GP
APVDD
C923
C922
C579
C934
C931
C932
C930
SC1KP50V2JN-2GP
CLOSE TO CHIP
R254
R253
C573
56R2F-1-GP
SCD33U10V3KX-3GP
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
PUT UP ALL COMPONENT ON 0 OHM IF CHIP IS JMB385
R247
5K11R2F-L1-GP
R256
R255
C574
SC220P50V2KX-3GP
0R3-0-U-GP
R429
R430
R426
R431
L59
L57
DLW21HN900SQ2LGP
JMB380
Place L28, L29 close to SK1
SKT-1394-4P-30-GP
SK1
GND
TPA0+
TPA0-
TPB0+
TPB0-
22.10218.U71
JMB380
JMB380,JMB385 COLAY MODEL
R259
12KR2J-L-GP
TREXT
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
TAV33
MDIO8
MDIO9
MDIO10
MDIO11
MDIO12
U46
PAD-49P-GP
XIN
XOUT
MDIO7
MDIO6
MDIO5
MDIO4
MDIO3
MDIO2
MDIO1
MDIO0
MDIO13
MDIO14
JMB385 CHANGE 400 K OHM TO 0 OHM
R620
402KR2F-GP
SB
R642
0R2J-2-GP
SB_PCIE_WAKE#
CR_WAKE#
D35
CH751H-40PT
10KR2J-3-GP
R637
2N7002-F-GP
Q47
CR_CPPE#_R
CR_CPPE#
C925
C926
SCD1U10V2KX-5GP
PCIE_NBRX_CARDTX_P3
PCIE_NBRX_CARDTX_N3
PLTRST_SYS#
CLK_PCIE_CARD#
CLK_PCIE_CARD
R632
8K2R2F-1-GP
PCIE_NBTX_C_CARDRX_N3
PCIE_NBTX_C_CARDRX_P3
For SD/MS Card Power
Q44
AO3403-GP
20mil Trace
3D3V_CARD
R631
1KR2-N5
CR1_PCTLN
R621
C906
C565
C921
0R0805-PAD
SCD1U10V2KX-4GP
SC10U10V5KX-2GP
SB
CARD1
C567
MS_VCC
SD_VCC
XD_VCC
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_WP_SW
SD_CD_SW
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_CD_SW
MS_DATA0
MS_DATA1
MS_DATA2
MS_DATA3
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
MS_SCLK
MS_INS
MS_BS
4IN1_GND
GROUND
NP1
NP2
CARD-PUSH-36P-3-GP
20.I0080.001
SC
EC83
EC82
EC84
EC85
SC220P50V2JN-3GP
SC10P50V2JN-4GP
R258
10KR2J-3-GP
JMB385
R257
1MR2F-GP
X5
X-24D576MHZ-44GP
C572
C571
SC15P50V2JN-2-GP
R261
22R2J-2-GP
R619
R260
200KR2J-L1-GP
4K7R2F-GP
R636
R640
R634
R633
R622
MDIO7
MDIO6
MDIO13
U84
CH715FPT-GP
C929
SC220P50V2KX-3GP
http://hobi-elektronika.net
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1394/CARD READER
Size
A3
Document Number
P1/P15
Rev
SA
Date: Wednesday, March 19, 2008
Sheet 28 of 56

400uS rise time
Supply 2~1.5A

100 mil

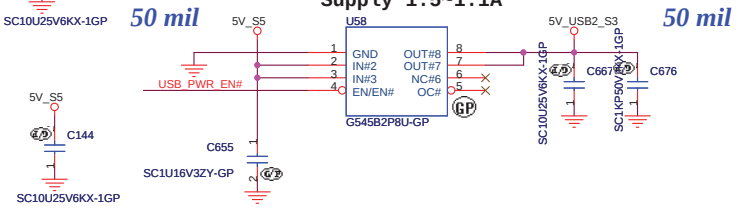


100 mil

5V_S5
C641
SC10U25V6KX-1GP

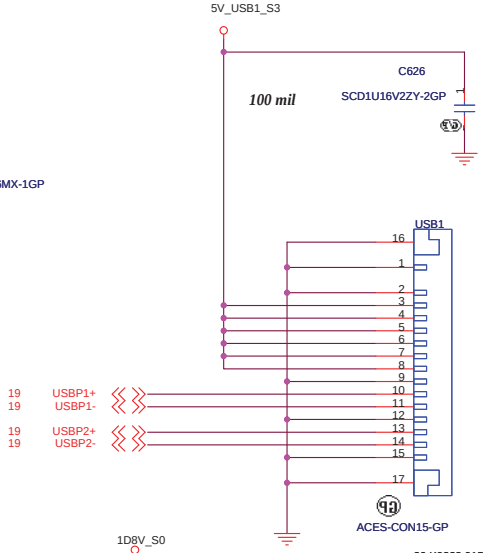
400uS rise time
Supply 1.5~1.1A

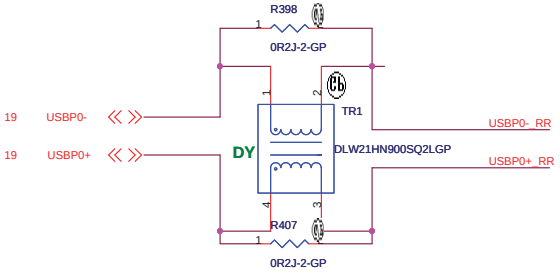
50 mil

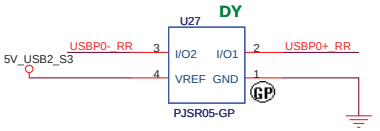


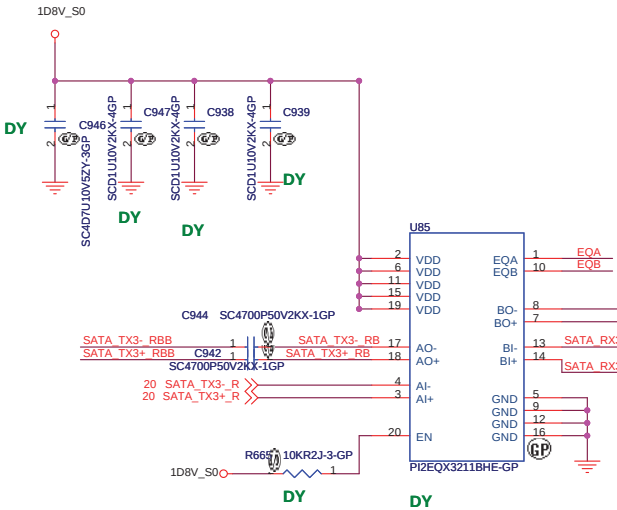
50 mil

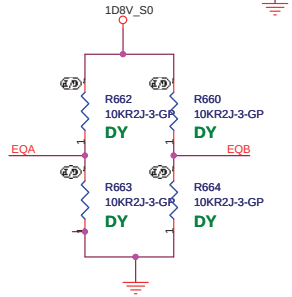
5V_S5
C144
SC10U25V6KX-1GP

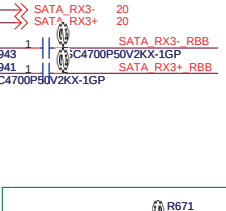


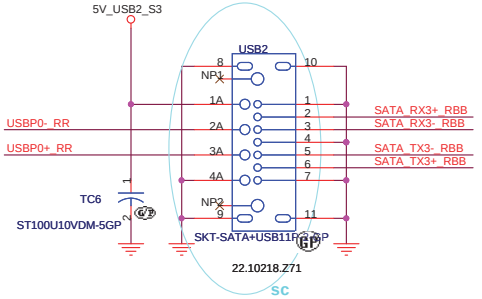


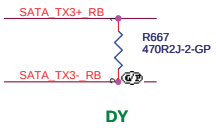




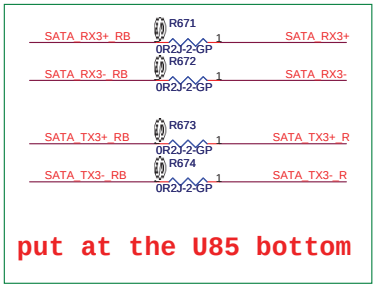








put close to connector



put at the U85 bottom

http://hobi-elektronika.net

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB/ESATA CONN

Size	Document Number	Rev
A3	P1/P15	SA

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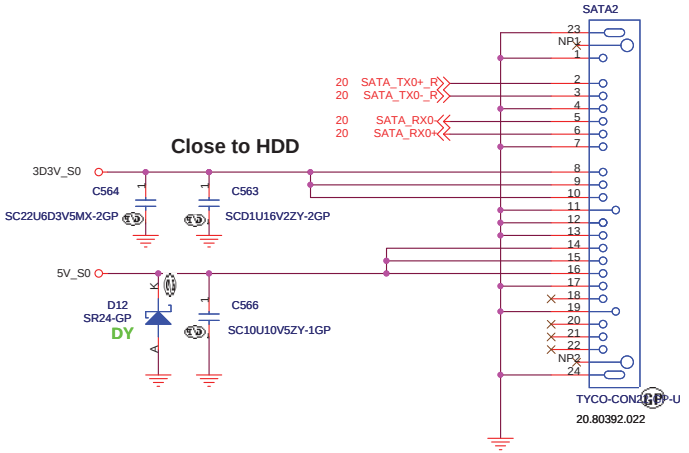
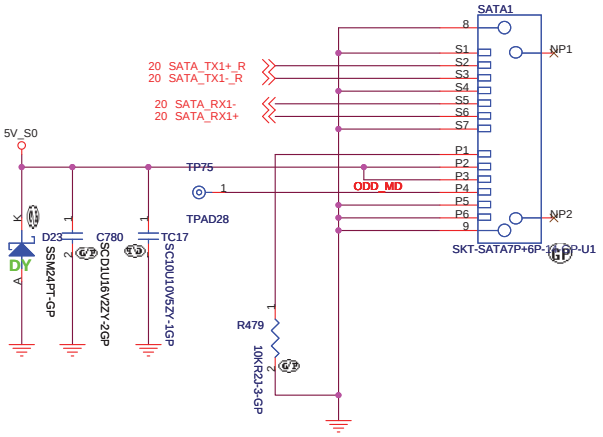
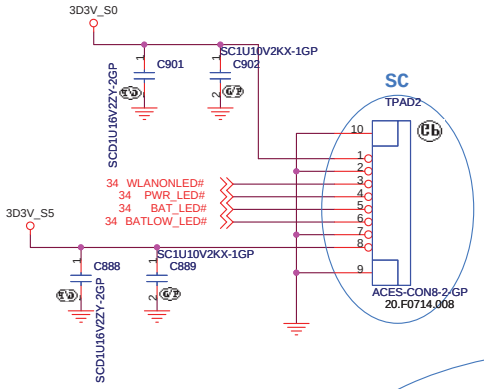
SATA HDD Connector



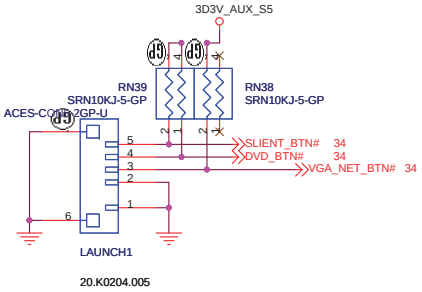
SATA ODD Connector

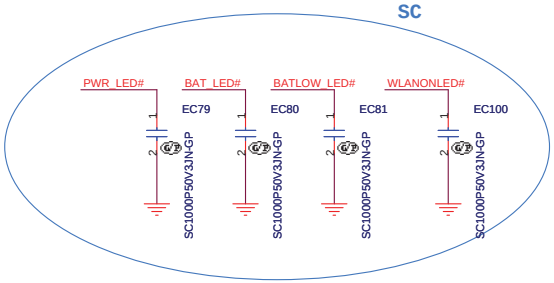


LED BD CONN

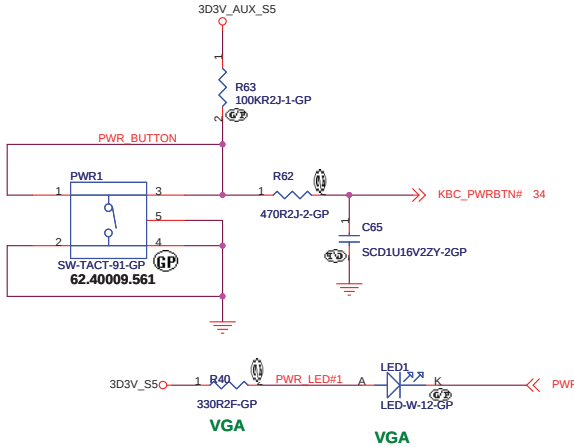


LAUNCH BD CONN



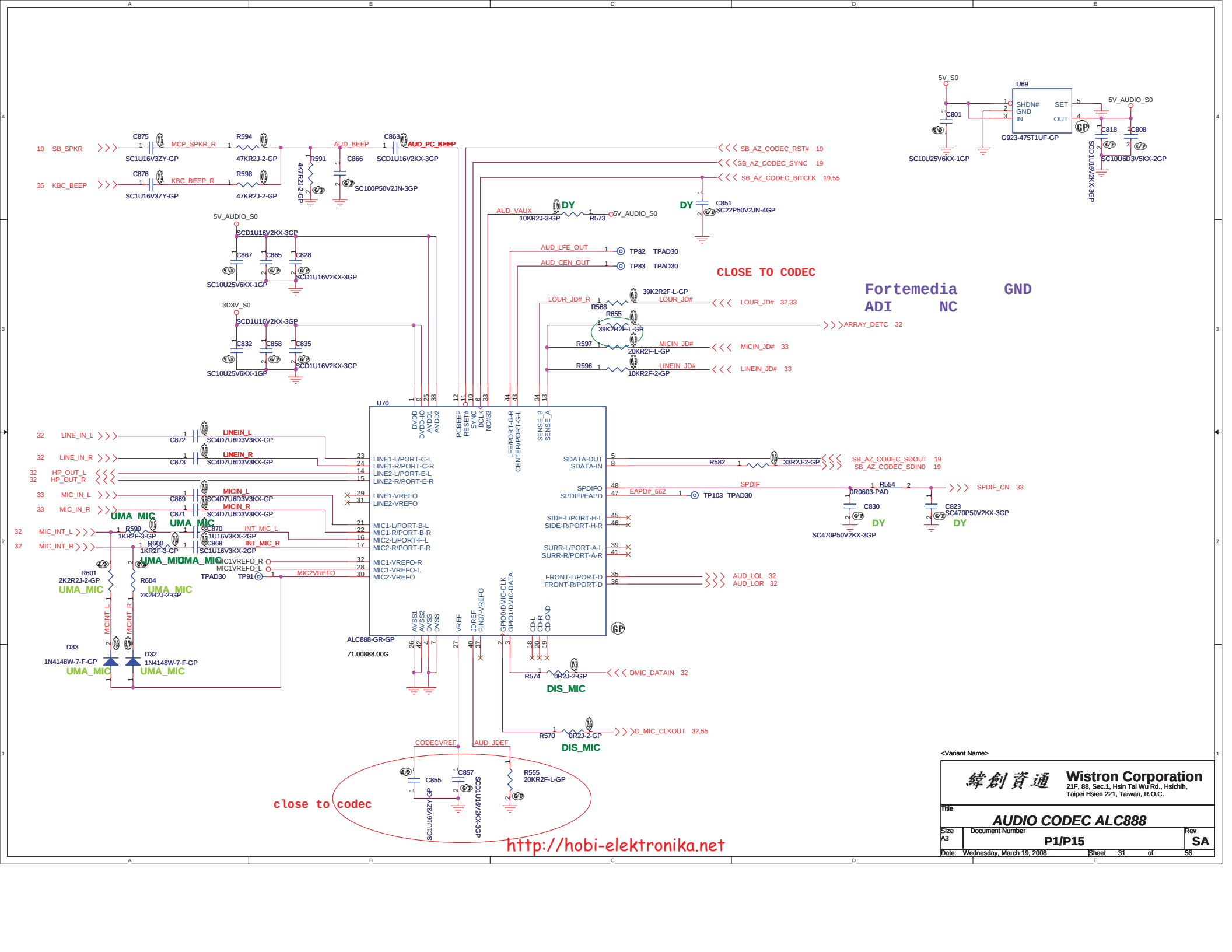


POWER BUTTON



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HDD/CDROM/LED/LAUNCH***
Size: A3	Document Number: **P1/P15** — Rev: **SA**
Date: Wednesday, March 19, 2008	Sheet 30 of 56



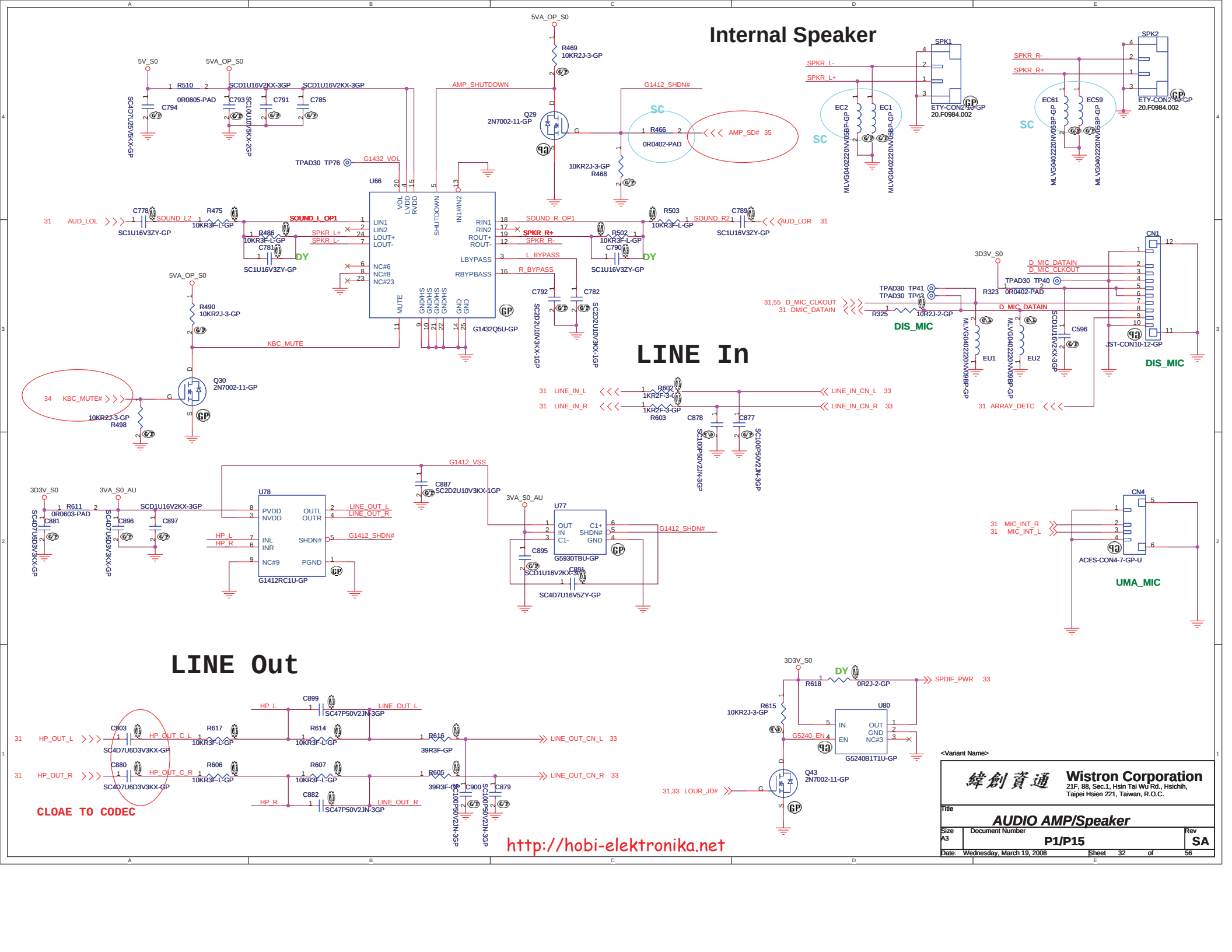
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

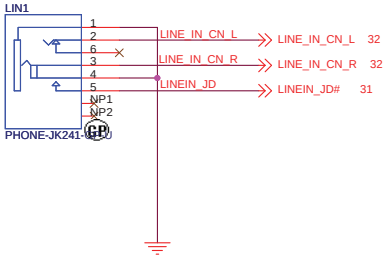
Title: AUDIO CODEC ALC888

Size	Document Number	Rev
A3	P1/P15	SA

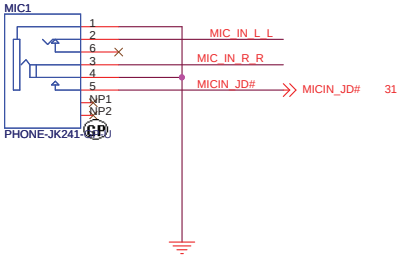
Date: Wednesday, March 19, 2008 Sheet 31 of 56

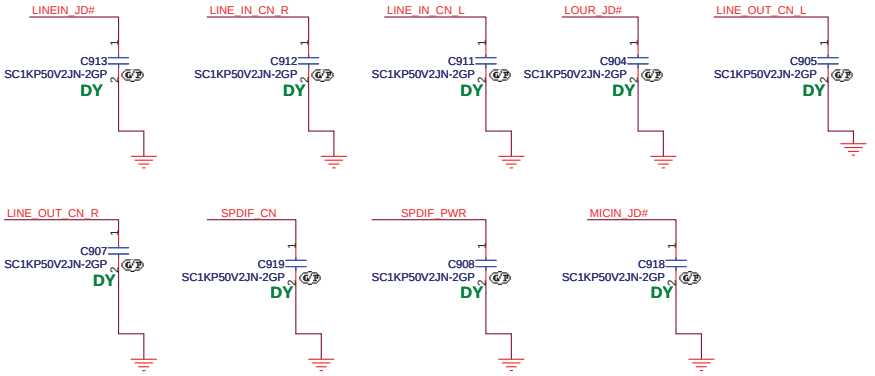

Internal Speaker
LINE In
LINE Out
U66
G1432Q5U-GP
U78
G1412RC1U-GP
U77
G5930TBU-GP
U80
G5240B1T1U-GP
SPK1
SPK2
ETY-CON2-20-GP
20.F0984.002
CN1
JST-CON10-12-GP
CN4
ACES-CON4-7-GP-U
DIS_MIC
UMA_MIC
Q29
2N7002-11-GP
Q30
2N7002-11-GP
Q43
2N7002-11-GP
AMP_SHUTDOWN
G1412_SHDN#
G1432_VOL
KBC_MUTE
SOUND_L_OP1
SOUND_R_OP1
SPKR_R+
SPKR_R-
L_BYPASS
R_BYPASS
G1412_VSS
LINE_OUT_L
LINE_OUT_R
HP_L
HP_R
D_MIC_DATAIN
D_MIC_CLKOUT
ARRAY_DETC
SPDIF_PWR
LOUR_JD#
CLOAE TO CODEC
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO AMP/Speaker
P1/P15
Wednesday, March 19, 2008

LINE IN

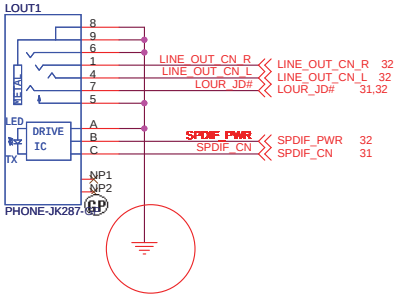


MIC IN



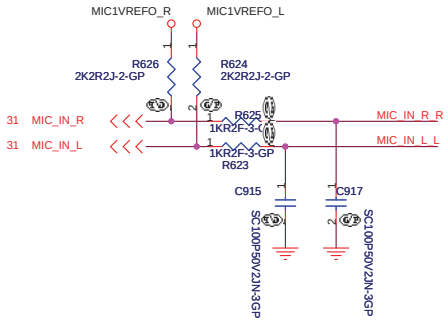


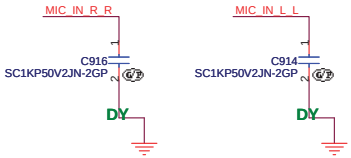
SPDIF / LINE OUT



ANALOG/GIGITAL GROUND SEPARATE

MIC In





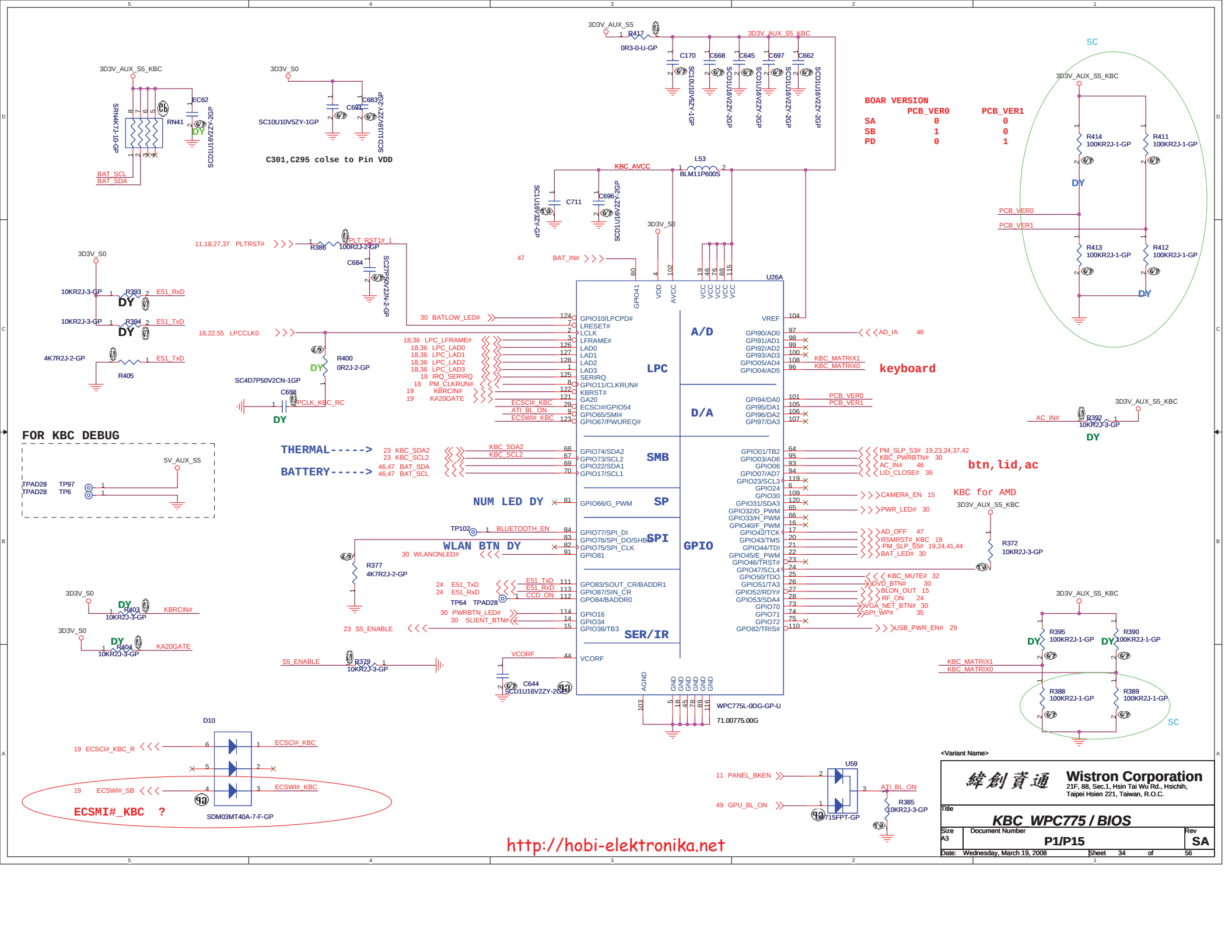
<Variant Name>

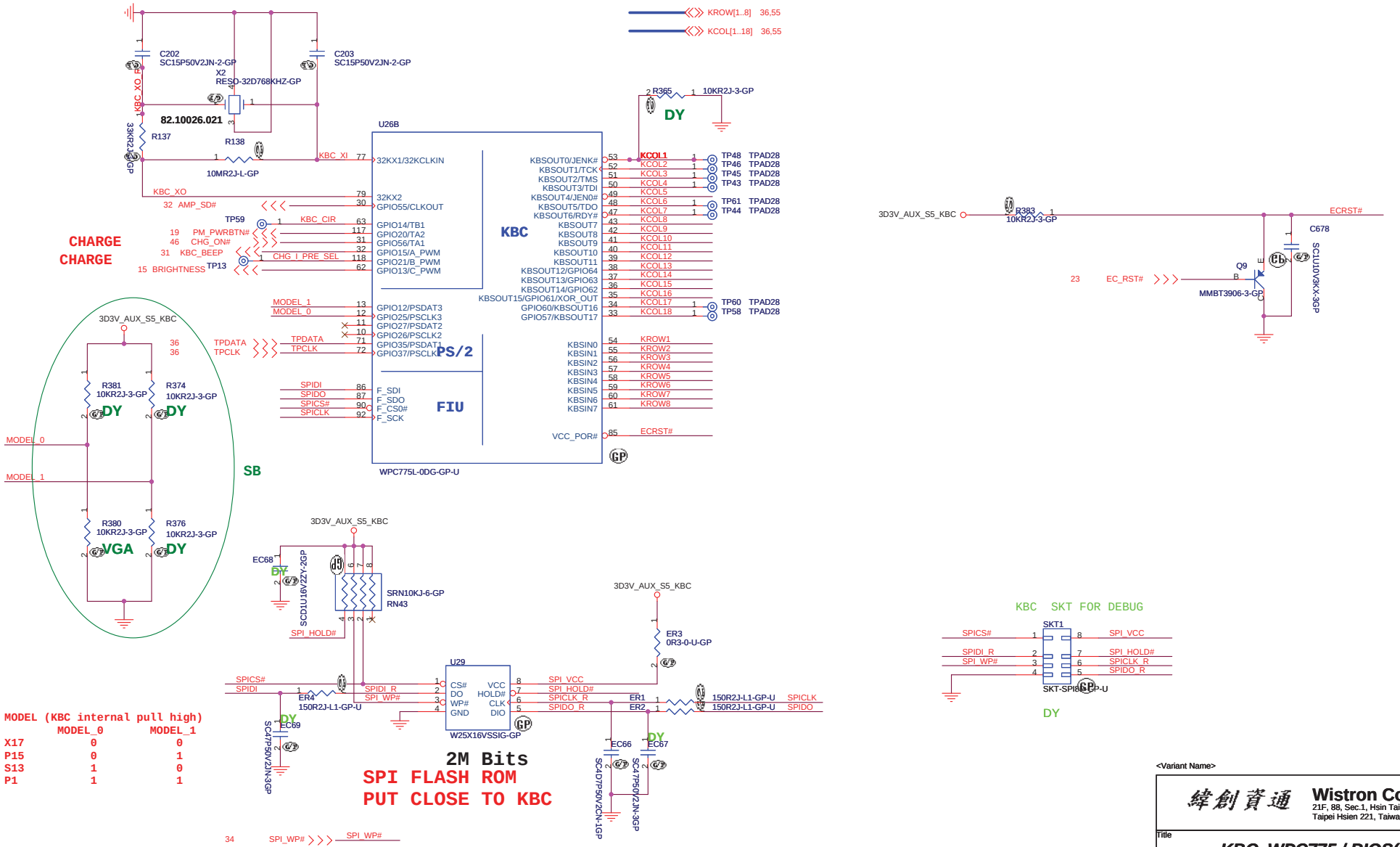
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CONN/SUBWOOFER

Size	Document Number	Rev
A3	P1/P15	SA

Date: Wednesday, March 19, 2008 Sheet 33 of 56


3D3V_AUX_S5
R417
0R3-0-U-GP
3D3V_AUX_S5_KBC
C170
C668
C645
C697
C662
SCD1U16V2ZY-2GP
3D3V_AUX_S5_KBC
SRN4K7J-10-GP
RN41
EC62
DY
SCD1U16V2ZY-2GP
BAT_SCL
BAT_SDA
3D3V_S0
SC10U10V5ZY-1GP
C691
C683
SC2Z2V0J1U-2GP
C301,C295 colse to Pin VDD
BOAR VERSION
PCB_VER0
PCB_VER1
SA 0 0
SB 1 0
PD 0 1
SC
3D3V_AUX_S5_KBC
R414 100KR2J-1-GP
R411 100KR2J-1-GP
DY
PCB_VER0
PCB_VER1
R413 100KR2J-1-GP
R412 100KR2J-1-GP
DY
KBC_AVCC
L53
BLM11P600S
SC1U16V2ZY-2GP
C711
C696
SCD1U16V2ZY-2GP
3D3V_S0
11,18,27,37 PLTRST#
R386
PLT_RST1#_1
100R2J-2-GP
C684
SC27P50V2JN-2GP
47 BAT_IN#
U26A
GPIO41
VDD
AVCC
VCC
3D3V_S0
10KR2J-3-GP
R393
E51_RxD
DY
10KR2J-3-GP
R394
E51_TxD
DY
4K7R2J-2-GP
R405
E51_TxD
18,22,55 LPCCLK0
R400
0R2J-2-GP
DY
SC4D7P50V2CN-1GP
C688
LPCCLK_KBC_RC
DY
30 BATLOW_LED#
18,36 LPC_LFRAME#
18,36 LPC_LAD0
18,36 LPC_LAD1
18,36 LPC_LAD2
18,36 LPC_LAD3
18 IRQ_SERIRQ
18 PM_CLKRUN#
19 KBRCIN#
19 KA20GATE
ECSCI# KBC
ATI_BL_ON
ECSWI# KBC
GPIO10/LPCPD#
LRESET#
LCLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
SERIRQ
GPIO11/CLKRUN#
KBRST#
GA20
ECSCI#/GPIO54
GPIO65/SMI#
GPIO67/PWUREQ#
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
VREF
GPI90/AD0
GPI91/AD1
GPI92/AD2
GPI93/AD3
GPIO05/AD4
GPIO04/AD5
AD_IA 46
KBC_MATRIX1
KBC_MATRIX0
keyboard
GPI94/DA0
GPI95/DA1
GPI96/DA2
GPI97/DA3
PCB_VER0
PCB_VER1
3D3V_AUX_S5_KBC
AC_IN#
R392
10KR2J-3-GP
DY
FOR KBC DEBUG
5V_AUX_S5
TPAD28 TP97
TPAD28 TP6
THERMAL-----> 23 KBC_SDA2 23 KBC_SCL2
BATTERY-----> 46,47 BAT_SDA 46,47 BAT_SCL
KBC_SDA2
KBC_SCL2
GPIO74/SDA2
GPIO73/SCL2
GPIO22/SDA1
GPIO17/SCL1
NUM LED DY
GPIO66/G_PWM
TP102
BLUETOOTH_EN
WLAN BTN DY
30 WLANONLED#
R377
4K7R2J-2-GP
GPIO77/SPI_DI
GPIO76/SPI_DO/SHBM
GPIO75/SPI_CLK
GPIO81
GPIO01/TB2
GPIO03/AD6
GPIO06
GPIO07/AD7
GPIO23/SCL3
GPIO24
GPIO30
GPIO31/SDA3
GPIO32/D_PWM
GPIO33/H_PWM
GPIO40/F_PWM
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45/E_PWM
GPIO46/TRST#
GPIO47/SCL4
GPIO50/TDO
GPIO51/TA3
GPIO52/RDY#
GPIO53/SDA4
GPIO70
GPIO71
GPIO72
GPO82/TRIS#
PM_SLP_S3# 19,23,24,37,42
KBC_PWRBTN# 30
AC_IN# 46
LID_CLOSE# 36
btn,lid,ac
KBC for AMD
CAMERA_EN 15
PWR_LED# 30
AD_OFF 47
RSMRST#_KBC 19
PM_SLP_S5# 19,24,41,44
BAT_LED# 30
KBC_MUTE# 32
DVD_BTN# 30
BLON_OUT 15
RF_ON 24
VGA_NET_BTN# 30
SPI_WP# 35
USB_PWR_EN# 29
3D3V_AUX_S5_KBC
R372
10KR2J-3-GP
24 E51_TxD
24 E51_RxD
TP64 TPAD28
E51_TxD
E51_RxD
CCD_ON
GPO83/SOUT_CR/BADDR1
GPO87/SIN_CR
GPO84/BADDR0
30 PWRBTN_LED#
30 SLIENT_BTN#
GPIO16
GPIO34
GPIO36/TB3
23 S5_ENABLE
3D3V_S0
R403
10KR2J-3-GP
KBRCIN#
3D3V_S0
R404
10KR2J-3-GP
KA20GATE
S5_ENABLE
R379
10KR2J-3-GP
VCORF
C644
SCD1U16V2ZY-2GP
VCORF
AGND
GND
WPC775L-0DG-GP-U
71.00775.00G
3D3V_AUX_S5_KBC
R395 100KR2J-1-GP
R390 100KR2J-1-GP
DY
DY
KBC_MATRIX1
KBC_MATRIX0
R388 100KR2J-1-GP
R389 100KR2J-1-GP
SC
D10
19 ECSCI#_KBC_R
ECSCI# KBC
19 ECSWI#_SB
ECSWI# KBC
ECSMI#_KBC ?
SDM03MT40A-7-F-GP
11 PANEL_BKEN
49 GPU_BL_ON
U59
ATI_BL_ON
R385
10KR2J-3-GP
UP715FPT-GP
http://hobi-elektronika.net
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC_WPC775 / BIOS
Size A3
Document Number
P1/P15
Rev SA
Date: Wednesday, March 19, 2008
Sheet 34 of 56



<variant_name>

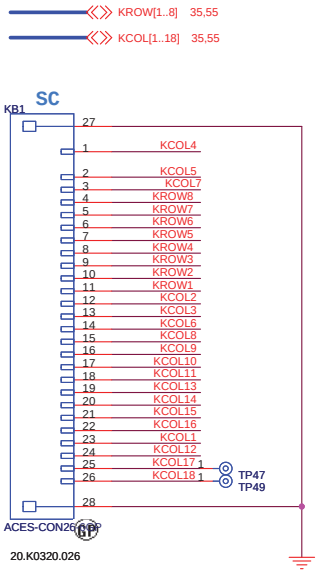
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

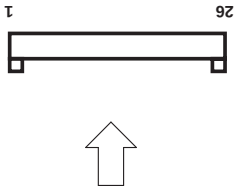
Title: KBC_WPC775 / BIOS(2/2)

Size: A3 | Document Number: P1/P15 | Rev: SA

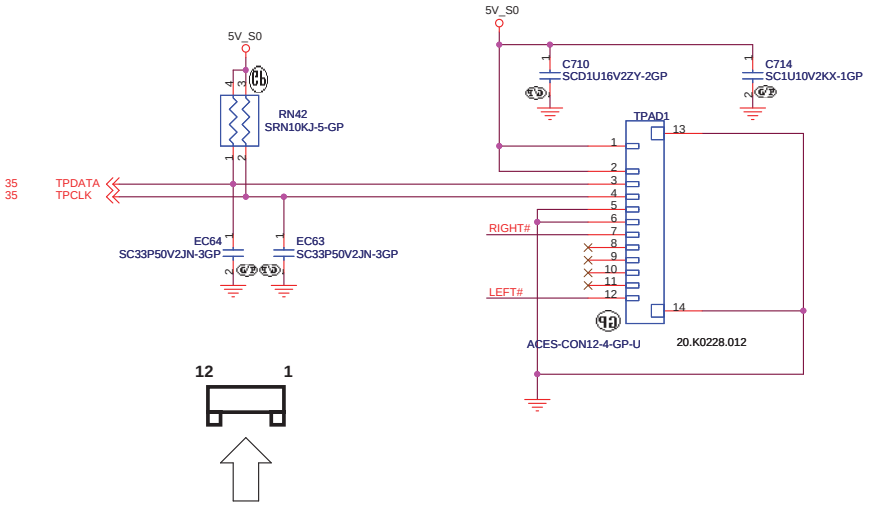
Date: Wednesday, March 19, 2008 | Sheet 35 of 56

Internal KeyBoard Connector

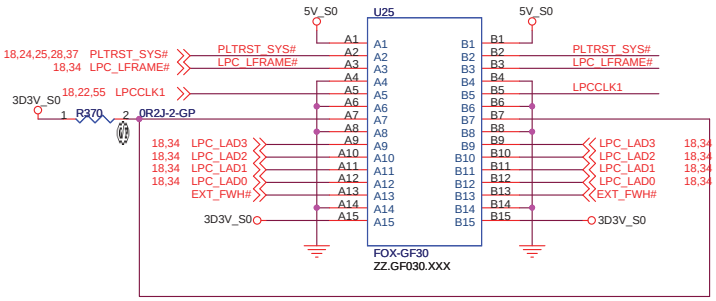




TouchPad Connector



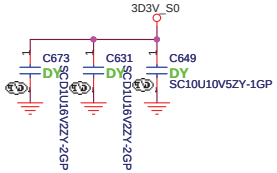
GOLDEN FINGER FOR DEBUG BOARD



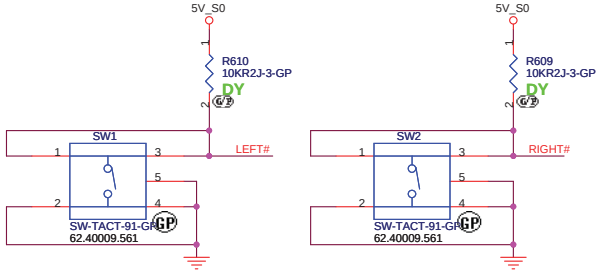
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

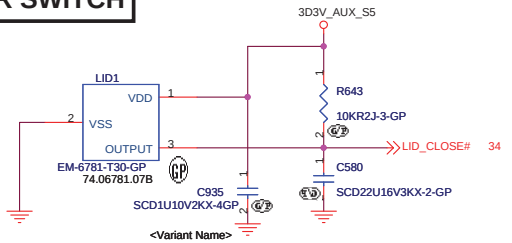
(BOTTOM VIEW)



15" TOUCHPAD BUTTON SWITCH



COVER SWITCH



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KEYBOARD/TPAD/DEBUG/LID**

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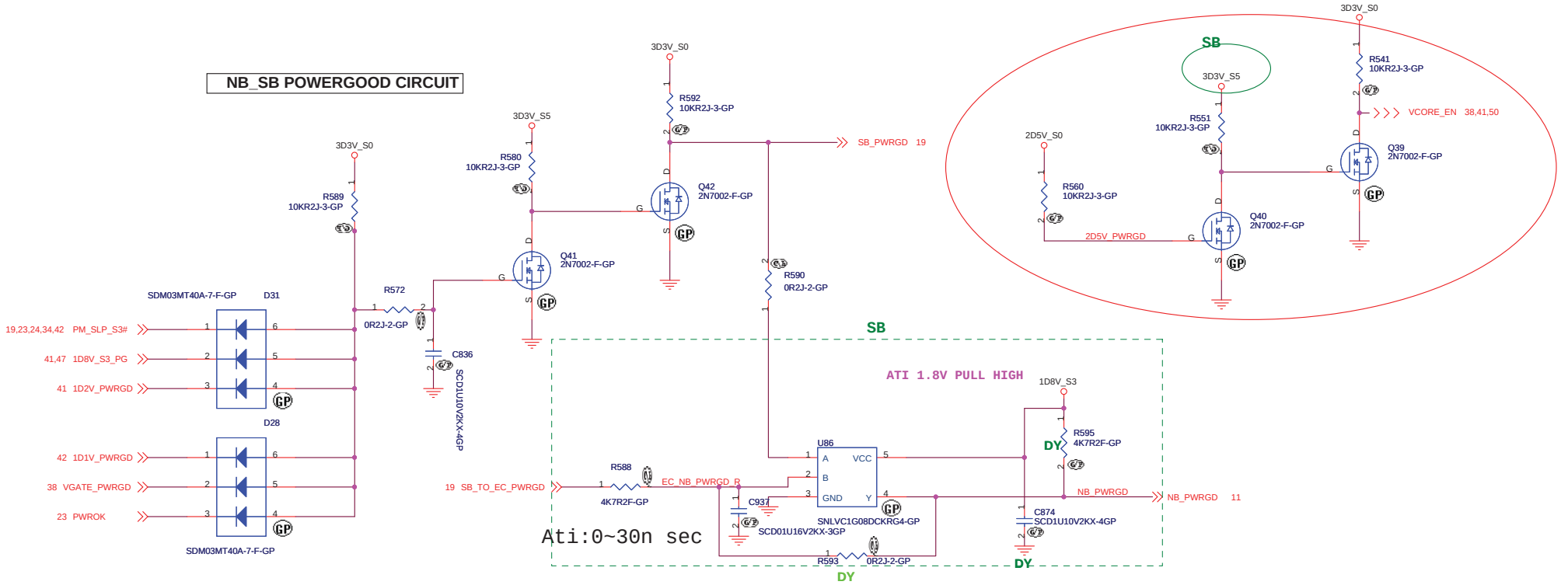
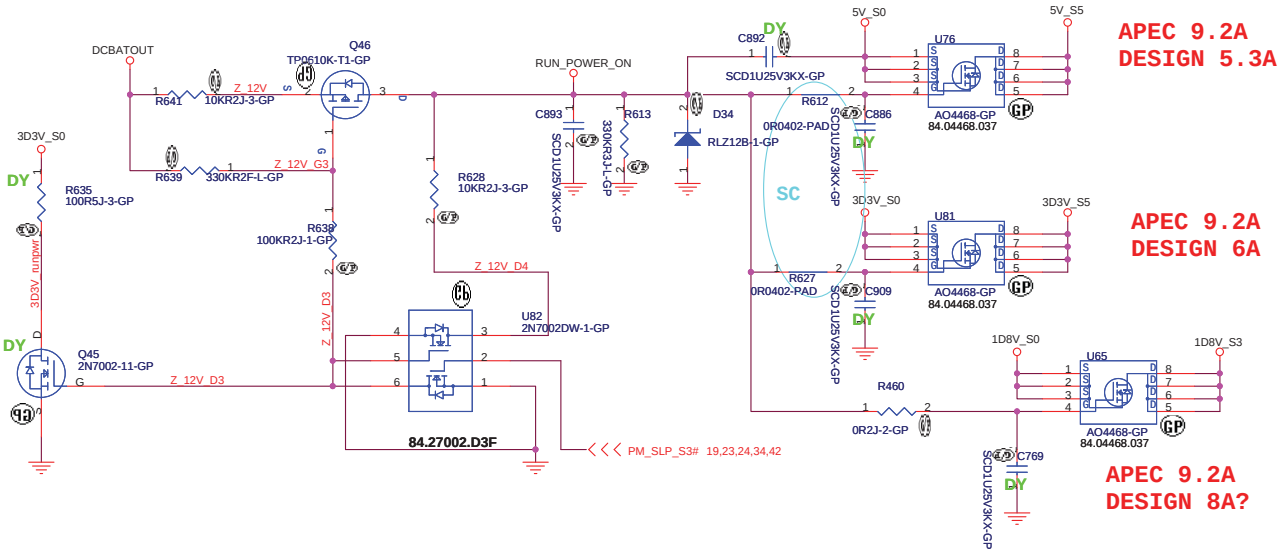
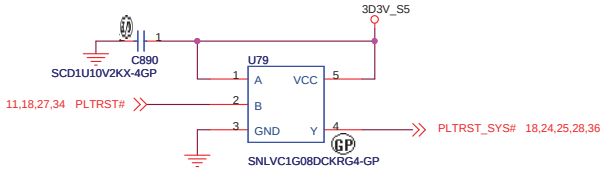
NB_SB POWERGOOD CIRCUIT



Run Power





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUNPOWER**

Size	Document Number	Rev
A3	P1/P15	SA

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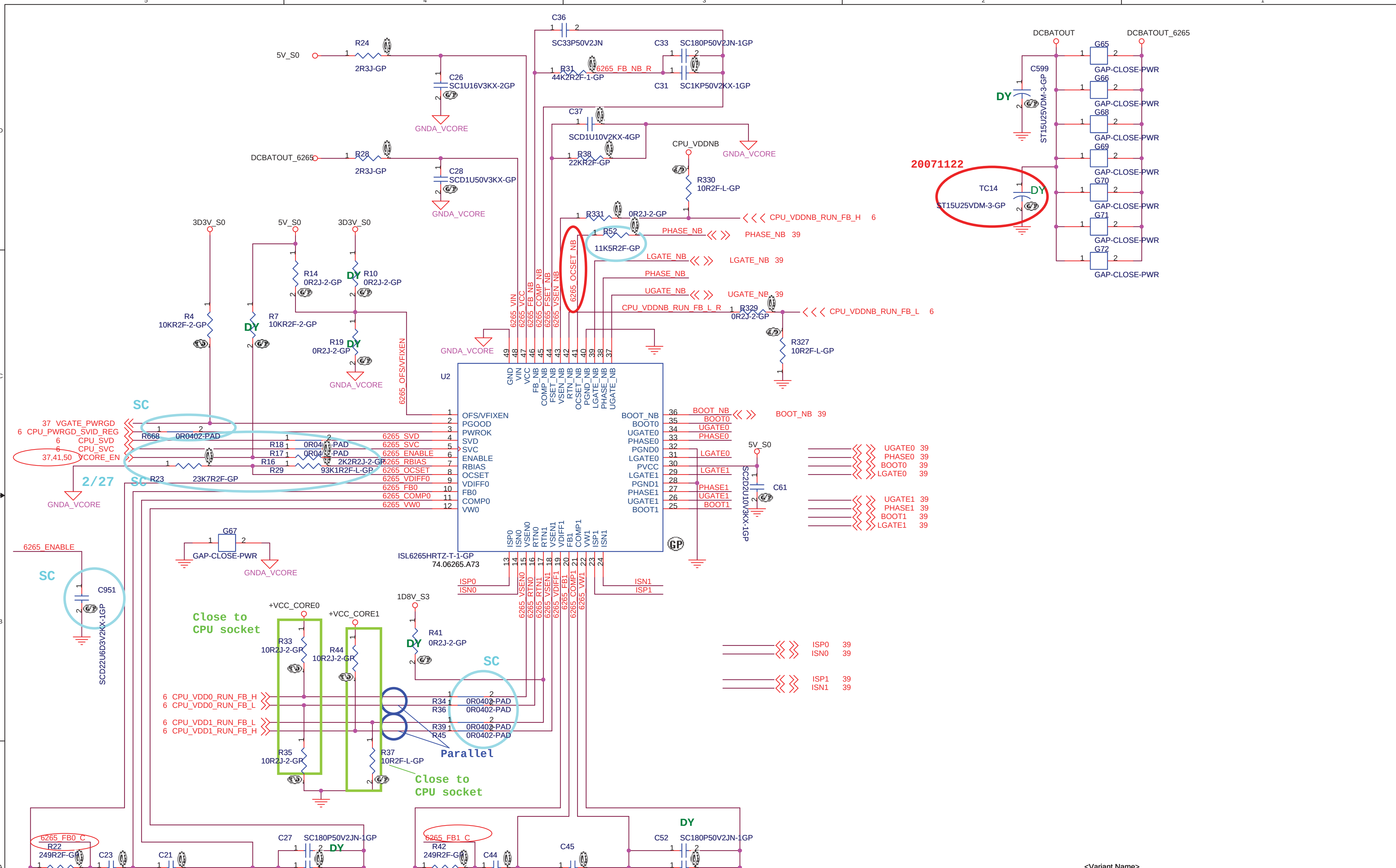
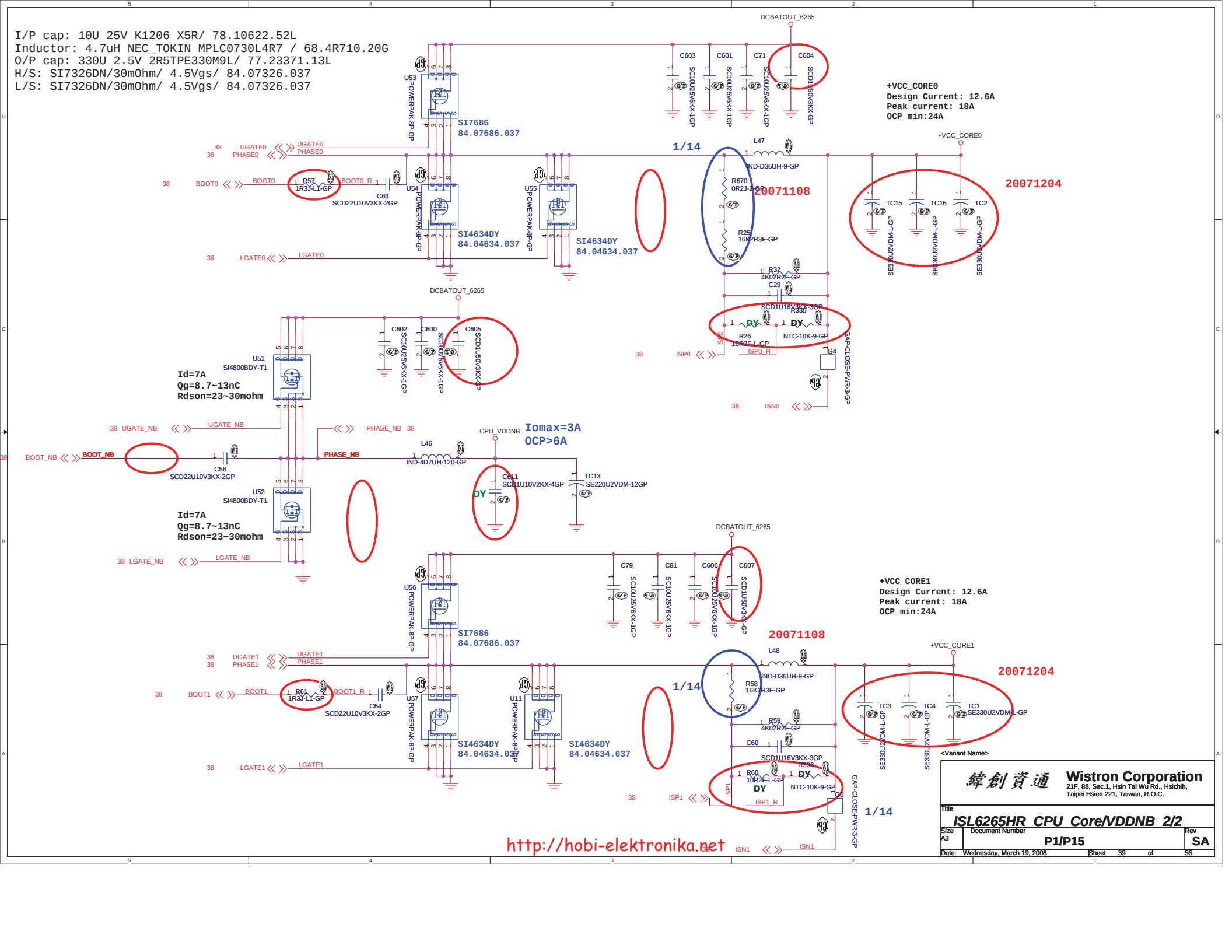


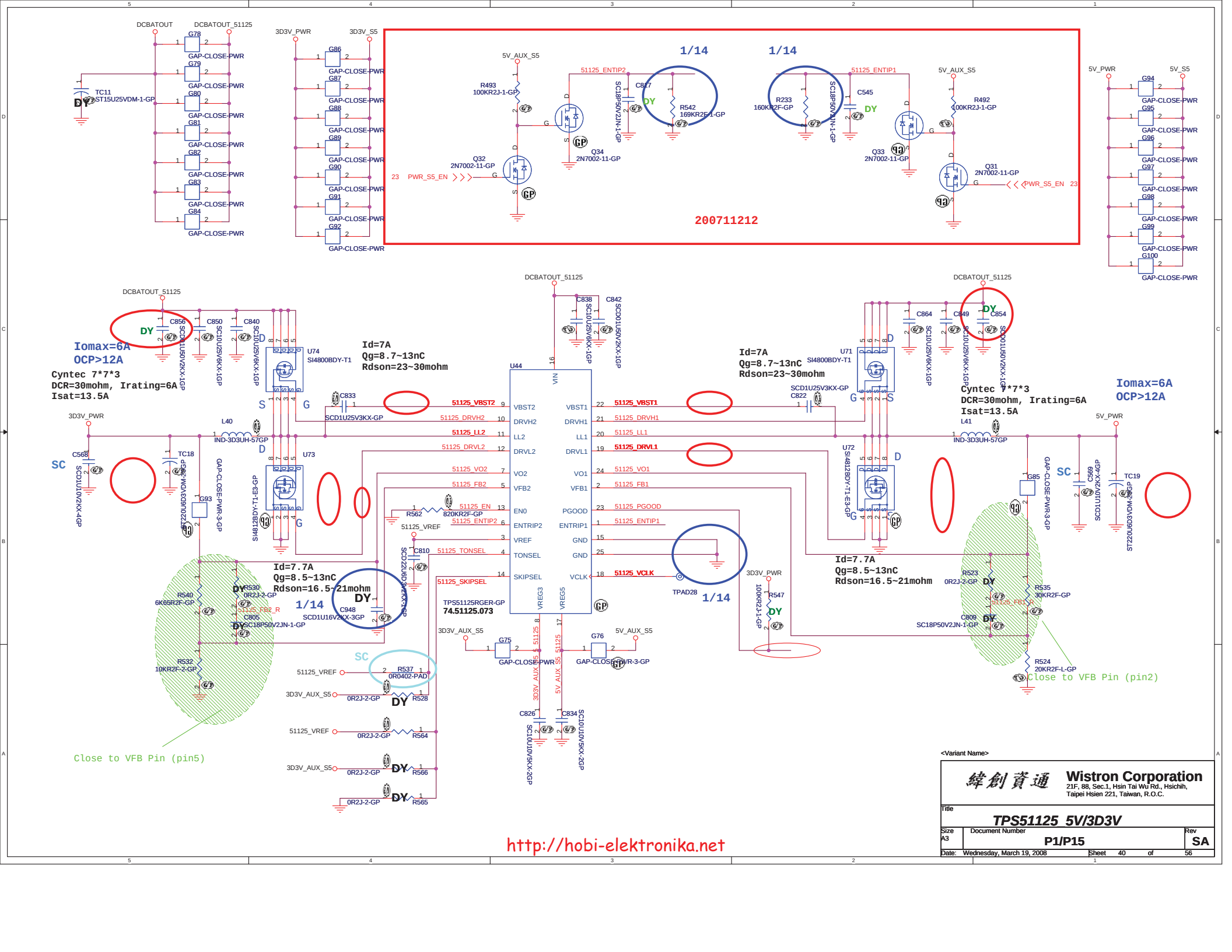
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ISL6265HR_CPU_Core/VDDNB_1/2		
Size A3	Document Number P1/P15	Rev SA
Date: Wednesday, March 19, 2008	Sheet 38 of 56	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20G
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037




DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
1/14
1/14
200711212
51125_ENTIP2
51125_ENTIP1
PWR_S5_EN
Iomax=6A
OCP>12A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51125 5V/3D3V
P1/P15
SA
Wednesday, March 19, 2008
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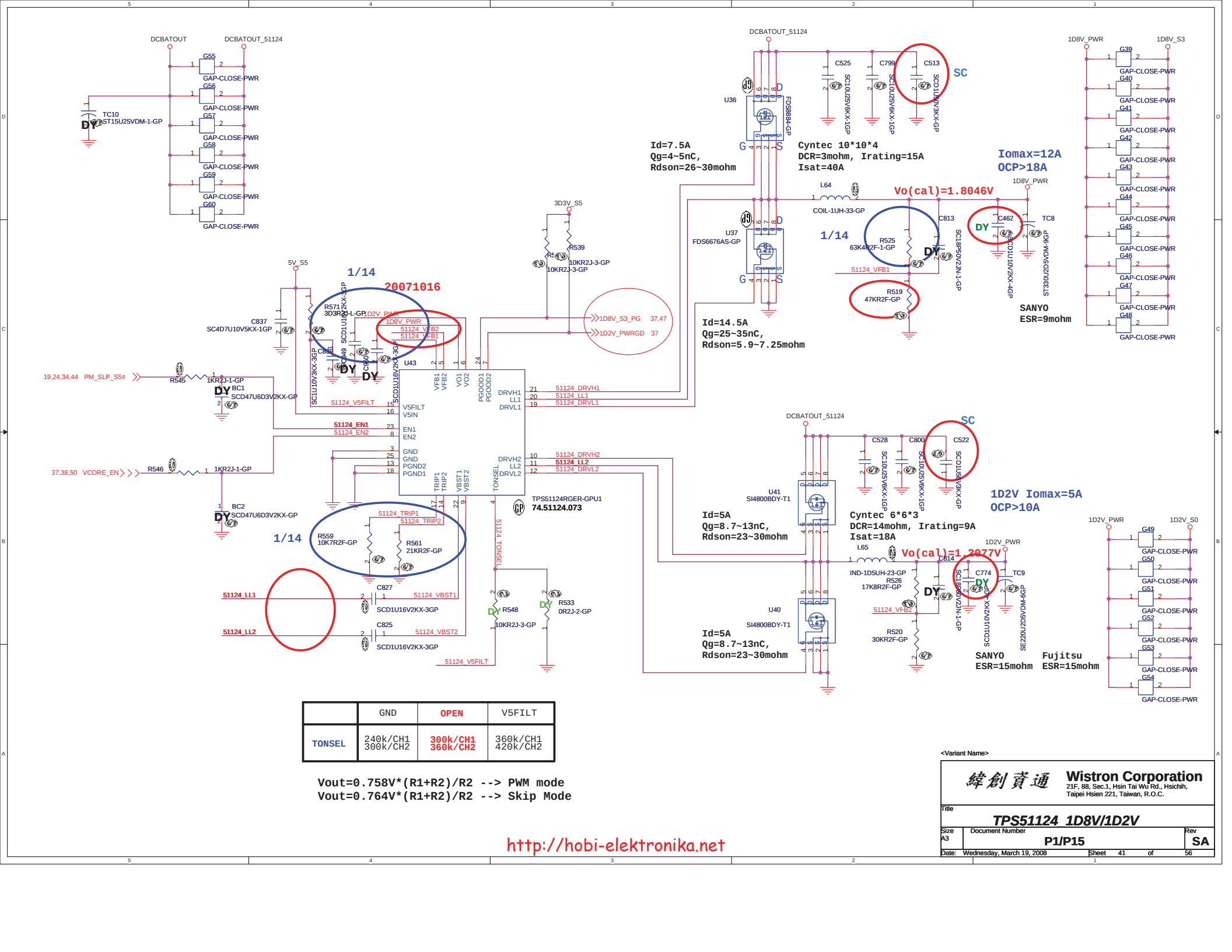

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

http://hobi-elektronika.net

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V/1D2V

Size	Document Number	Rev
A3	P1/P15	SA

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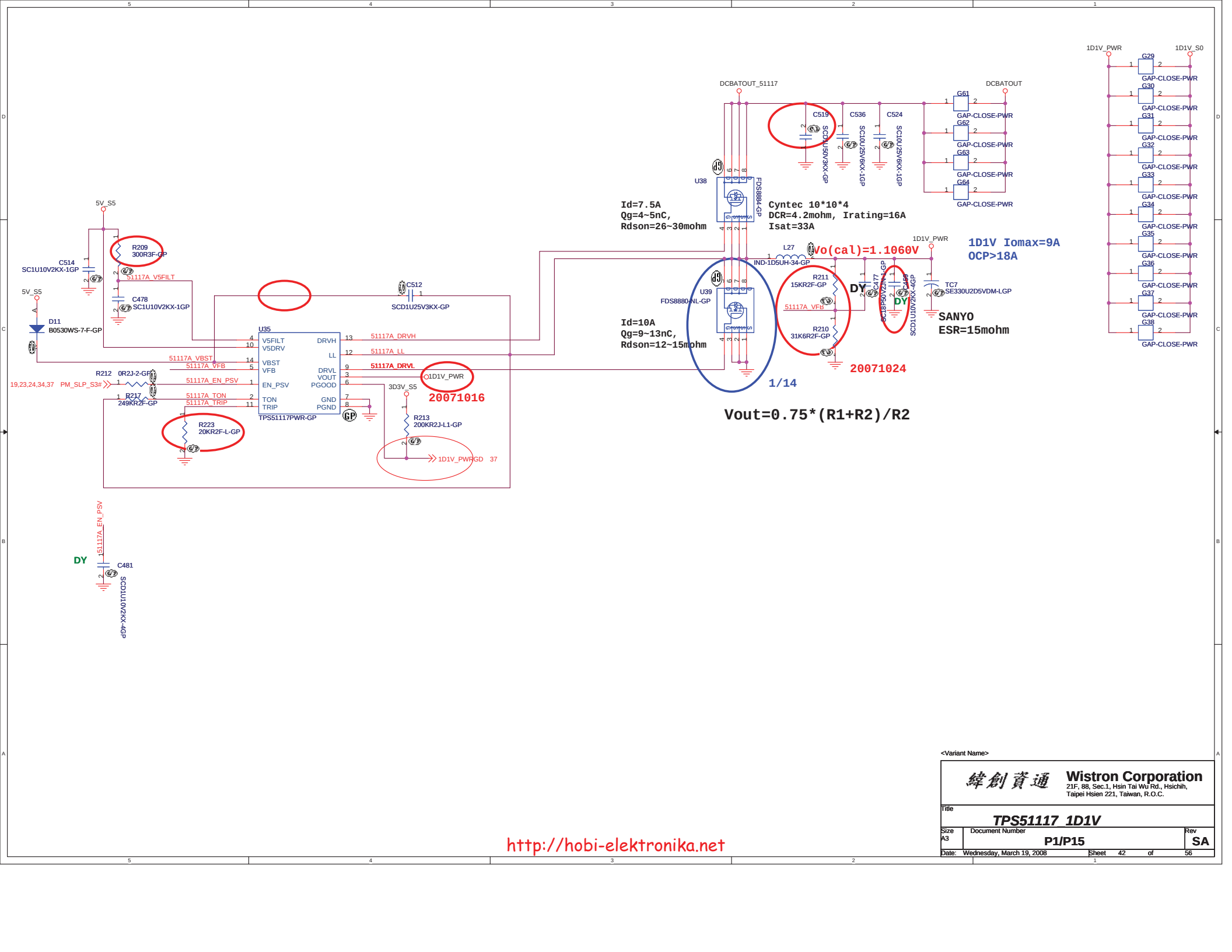
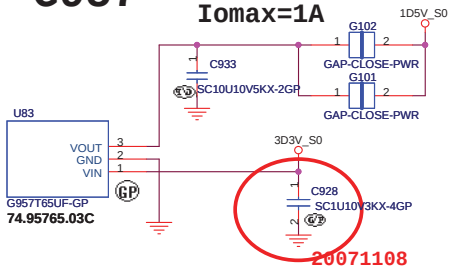


<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51117_1D1V		
Size: A3	Document Number: P1/P15	Rev: SA
Date: Wednesday, March 19, 2008	Sheet 42 of 56	

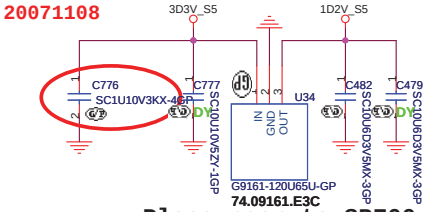
G957

1D5V_S0
Iomax=1A

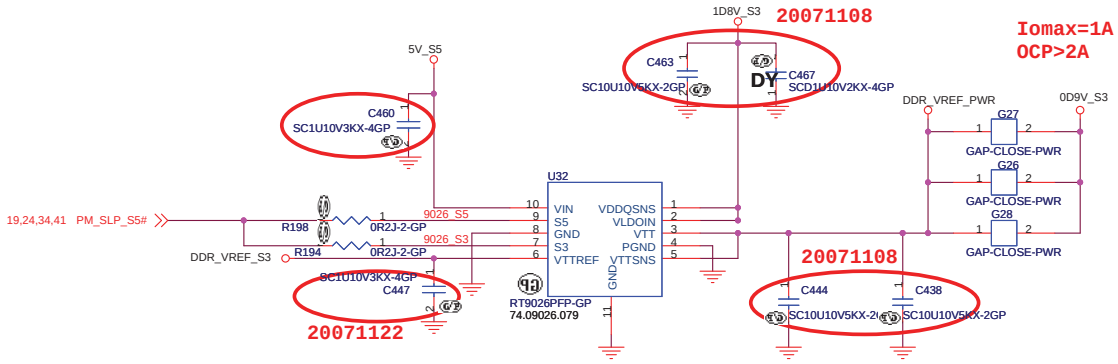


1D2V_S5
Iomax=400mA

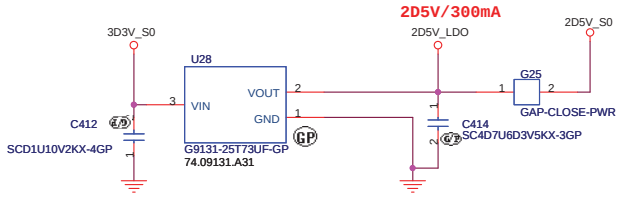
20071108



Place near to SB700



2D5V_S0
Iomax=0.3A



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V&2D5V&1D25V&1D5V

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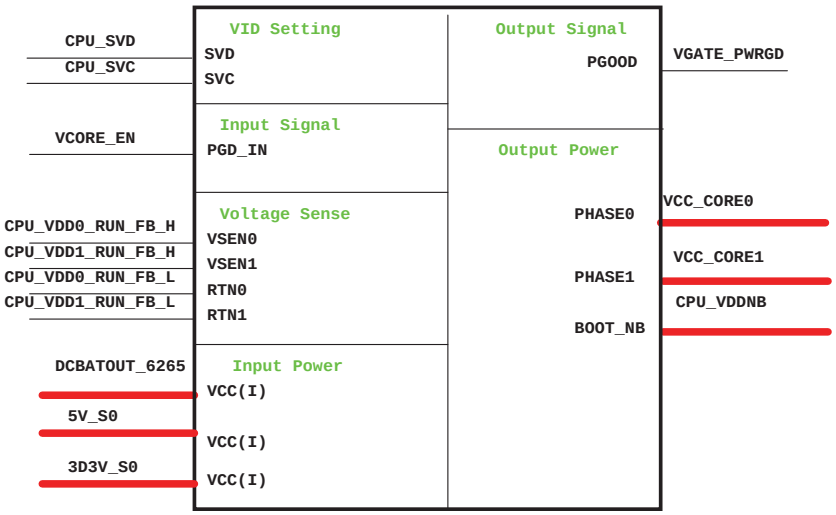
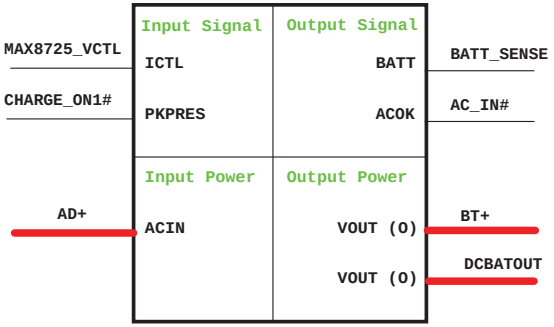
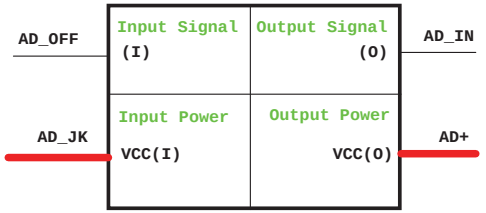
CPU_CORE
Intersil ISL6265



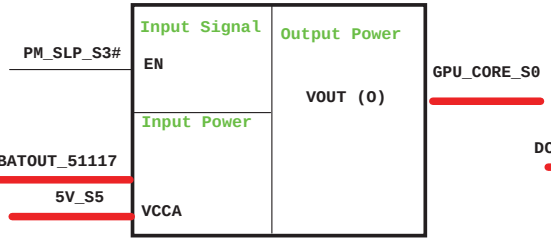
Charger Max8725



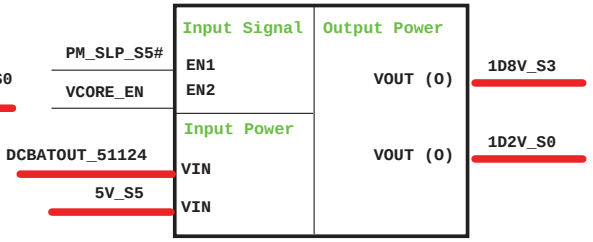
Adapter



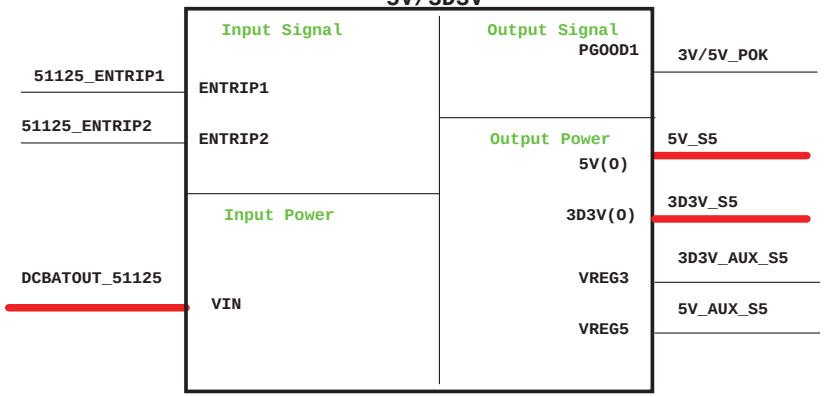
TPS51117
GPU_CORE



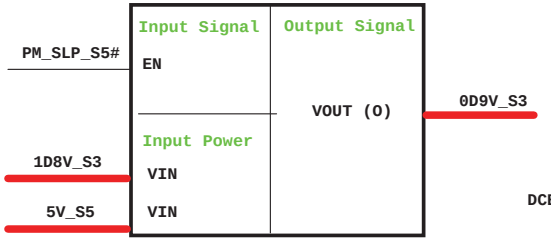
TPS51124
1D8V_S3
1D2V_S0



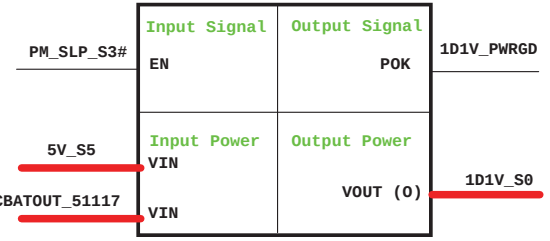
TPS51125
5V/3D3V



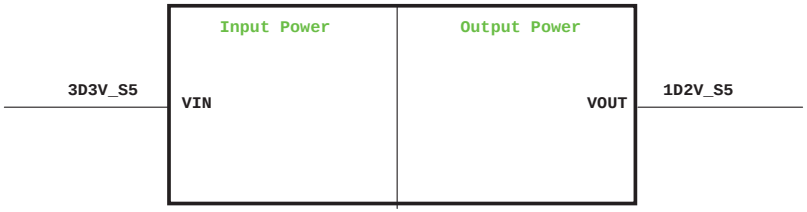
RT9026PFP
0D9V_S3



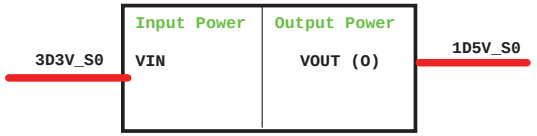
TPS51117
1D1V_S0



G9161
1D2V_S5



G957
1D5V_S0



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

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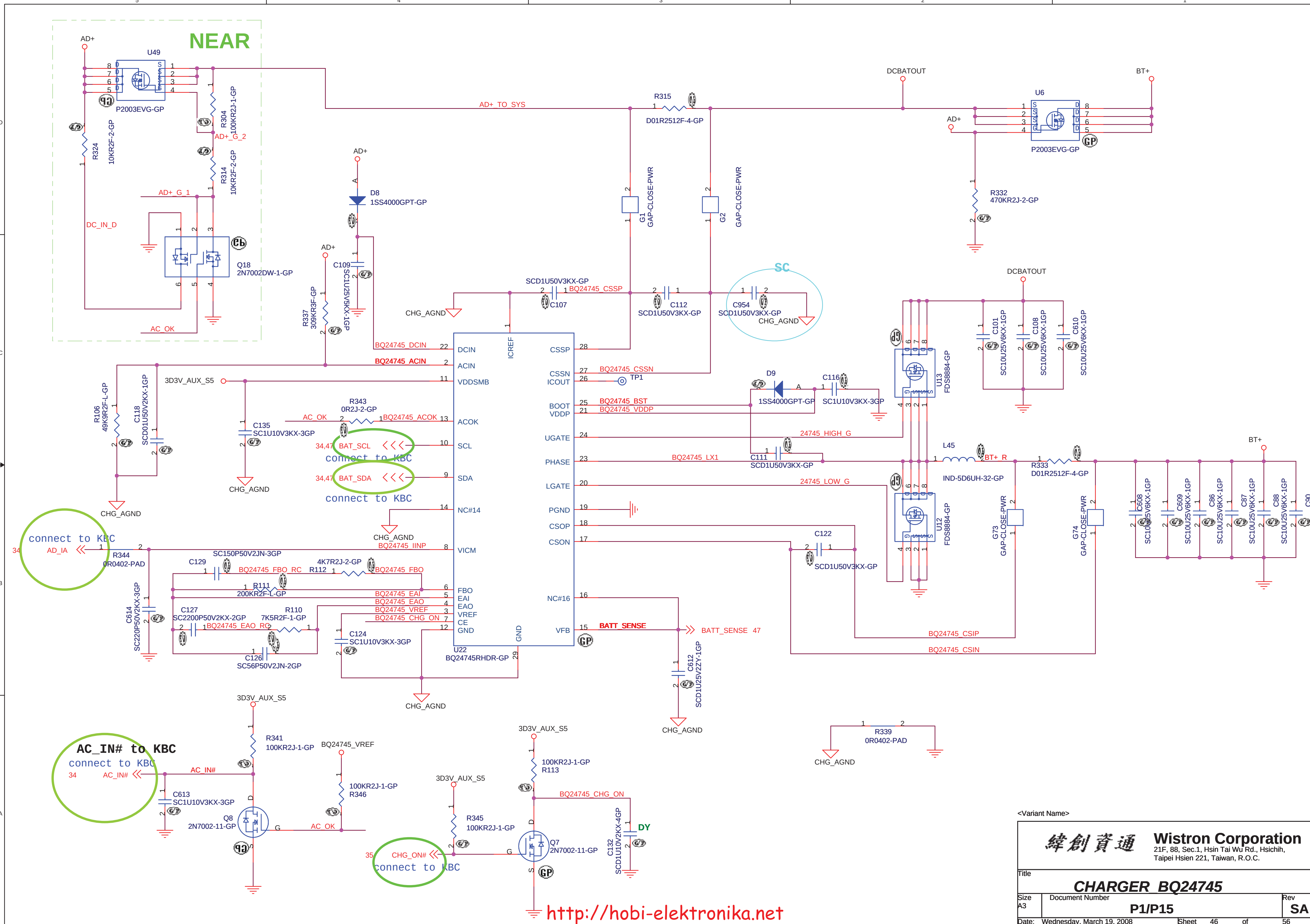
NEAR
AD+
U49
P2003EVG-GP
R324
10KR2F-2-GP
R304
100KR2J-1-GP
AD+_G_2
R314
10KR2F-2-GP
AD+_G_1
DC_IN_D
Q18
2N7002DW-1-GP
AC_OK
D8
1SS4000GPT-GP
C109
SC1U25V5KX-1GP
R337
309KR3F-GP
AD+_TO_SYS
R315
D01R2512F-4-GP
DCBATOUT
BT+
U6
P2003EVG-GP
R332
470KR2J-2-GP
G1
GAP-CLOSE-PWR
G2
GAP-CLOSE-PWR
SC
SCD1U50V3KX-GP
C107
BQ24745_CSSP
C112
SCD1U50V3KX-GP
C954
SCD1U50V3KX-GP
CHG_AGND
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R106
49K9R2F-L-GP
C118
SCD01U50V2KX-1GP
C135
SC1U10V3KX-3GP
R343
0R2J-2-GP
BQ24745_ACOK
BAT_SCL
BAT_SDA
connect to KBC
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U22
BQ24745RHDR-GP
BQ24745_CSSN
TP1
BQ24745_BST
BQ24745_VDDP
D9
1SS4000GPT-GP
C116
SC1U10V3KX-3GP
24745_HIGH_G
BQ24745_LX1
C111
SCD1U50V3KX-GP
24745_LOW_G
U13
FDS8884-GP
U12
FDS8884-GP
C101
C108
C610
SC10U25V6KX-1GP
L45
IND-5D6UH-32-GP
BT+_R
R333
D01R2512F-4-GP
G73
G74
GAP-CLOSE-PWR
C608
C609
C86
C87
C88
C90
C122
SCD1U50V3KX-GP
BQ24745_CSIP
BQ24745_CSIN
AD_IA
R344
0R0402-PAD
C129
SC150P50V2JN-3GP
BQ24745_FBO_RC
R112
4K7R2J-2-GP
BQ24745_FBO
R111
200KR2F-L-GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C127
SC2200P50V2KX-2GP
R110
7K5R2F-1-GP
BQ24745_EAO_RC
C126
SC56P50V2JN-2GP
C124
SC1U10V3KX-3GP
C614
SC220P50V2KX-3GP
BATT_SENSE
BATT_SENSE 47
C612
SCD1U25V2Y-1GP
R339
0R0402-PAD
AC_IN# to KBC
AC_IN#
R341
100KR2J-1-GP
C613
SC1U10V3KX-3GP
Q8
2N7002-11-GP
R346
100KR2J-1-GP
R345
100KR2J-1-GP
CHG_ON#
R113
100KR2J-1-GP
BQ24745_CHG_ON
Q7
2N7002-11-GP
C132
SCD1U10V2KX-4GP
DY
http://hobi-elektronika.net
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER_BQ24745
Size A3
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P1/P15
Rev SA
Date: Wednesday, March 19, 2008
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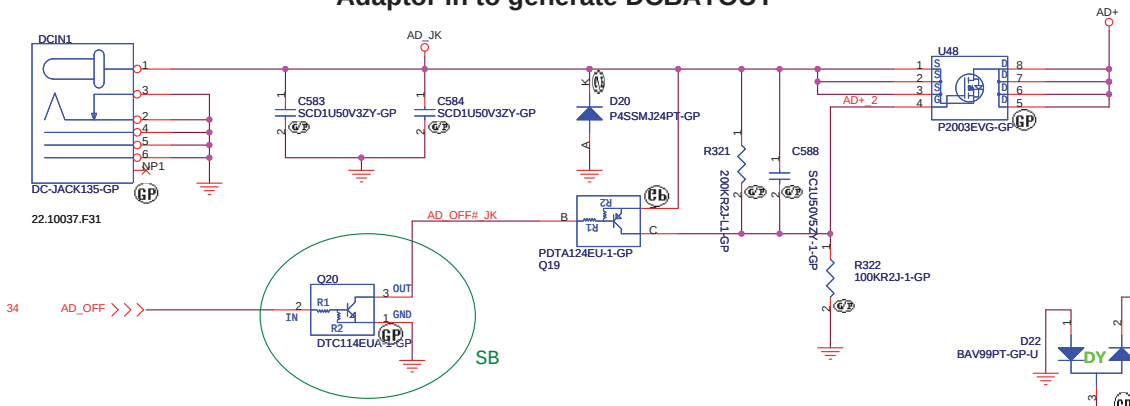
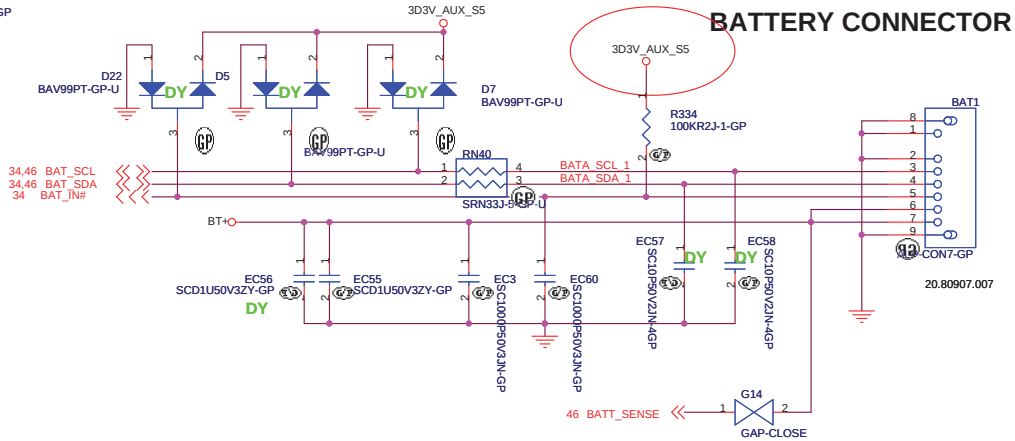
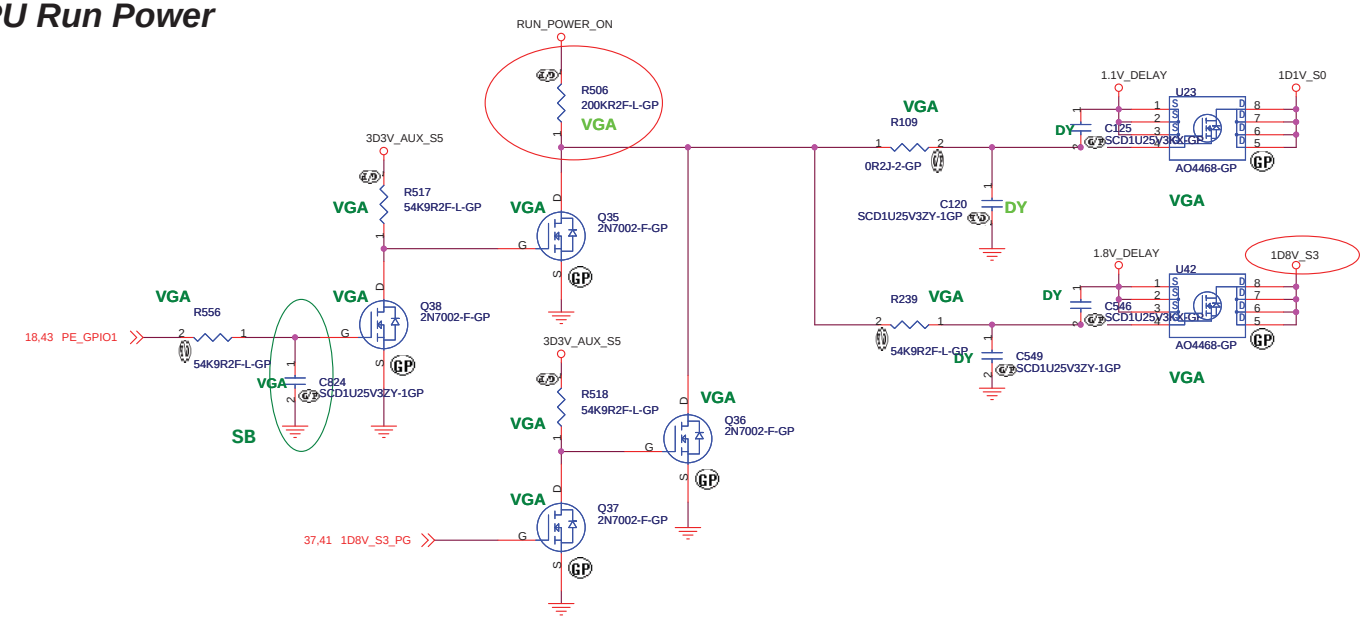
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



GPU Run Power



<Variant Name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AD_IN/ BTY SWITCH/GPURUN
Size A3 / Document Number	P1/P15
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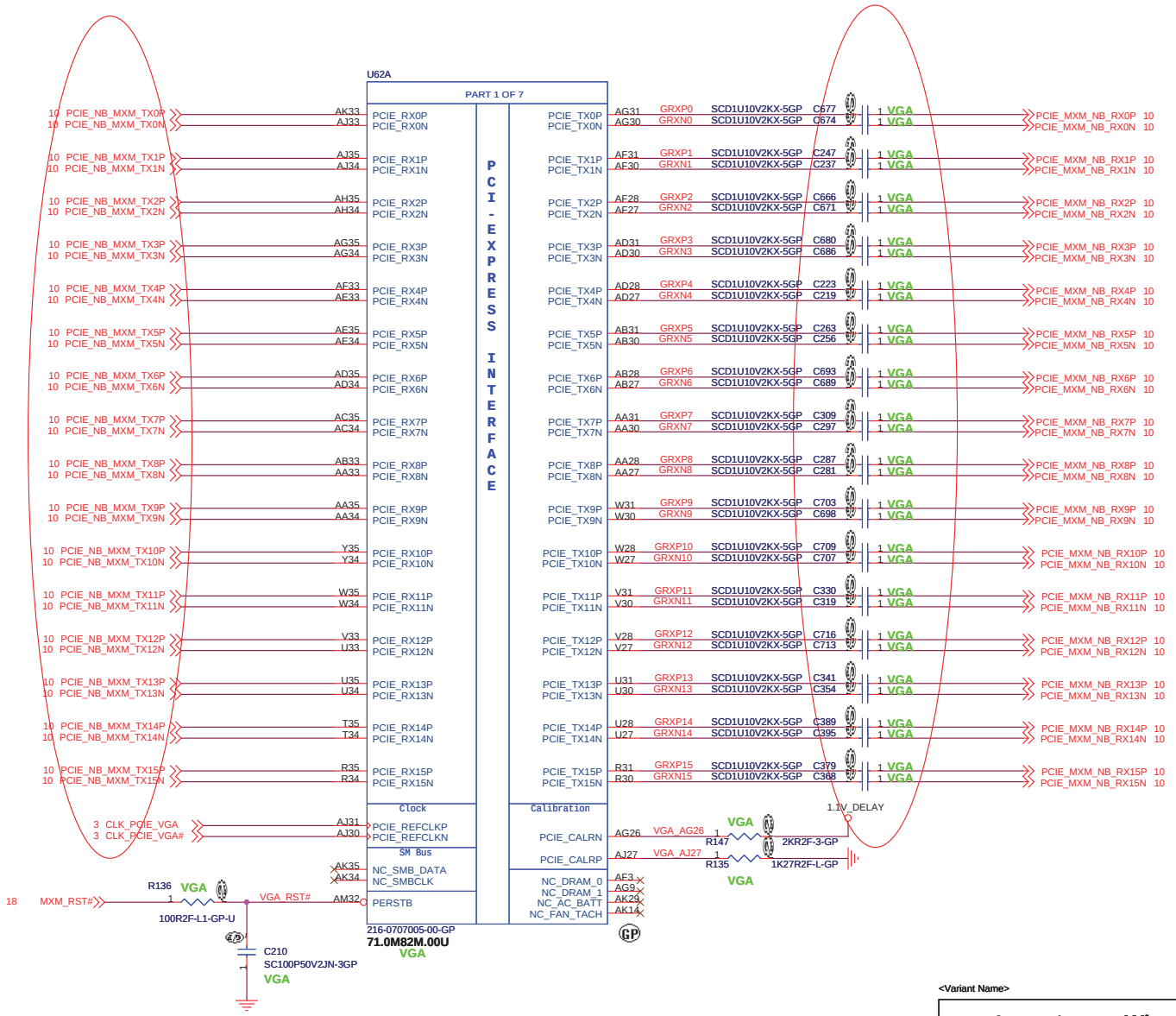

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<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: M8XM_PCIE

Size: A3 | Document Number: P1/P15 | Rev: SA

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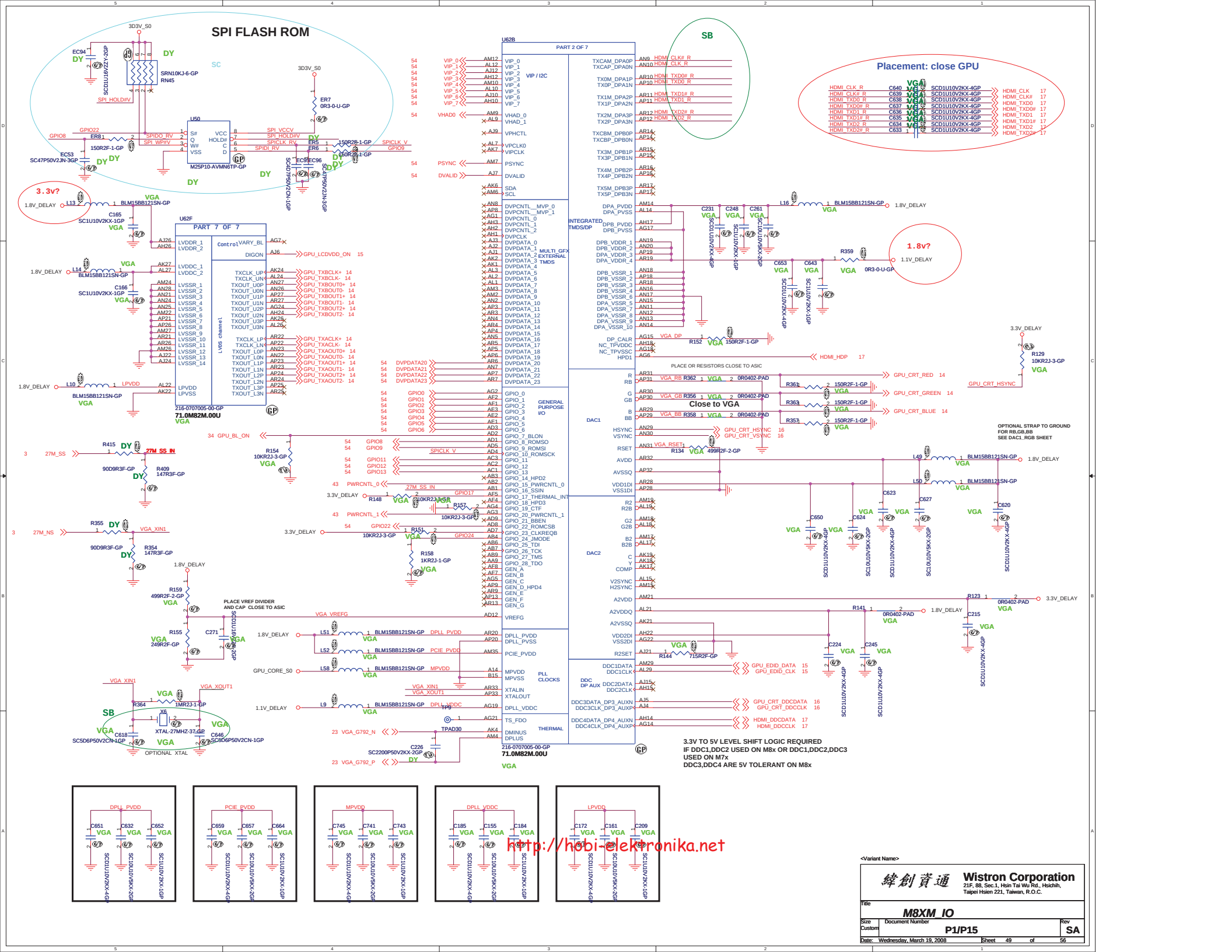
SPI FLASH ROM
SB
Placement: close GPU
U62B
PART 2 OF 7
U62F
PART 7 OF 7
U50
M25P10-AVMN6TP-GP
3.3v?
1.8v?
Close to VGA
PLACE OR RESISTORS CLOSE TO ASIC
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC
OPTIONAL STRAP TO GROUND FOR RB,GB,BB SEE DAC1_RGB SHEET
OPTIONAL XTAL
3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED IF DDC1,DDC2 USED ON M8x OR DDC1,DDC2,DDC3 USED ON M7x DDC3,DDC4 ARE 5V TOLERANT ON M8x
http://hobi-elektronika.net
Wistron Corporation
M8XM_IO
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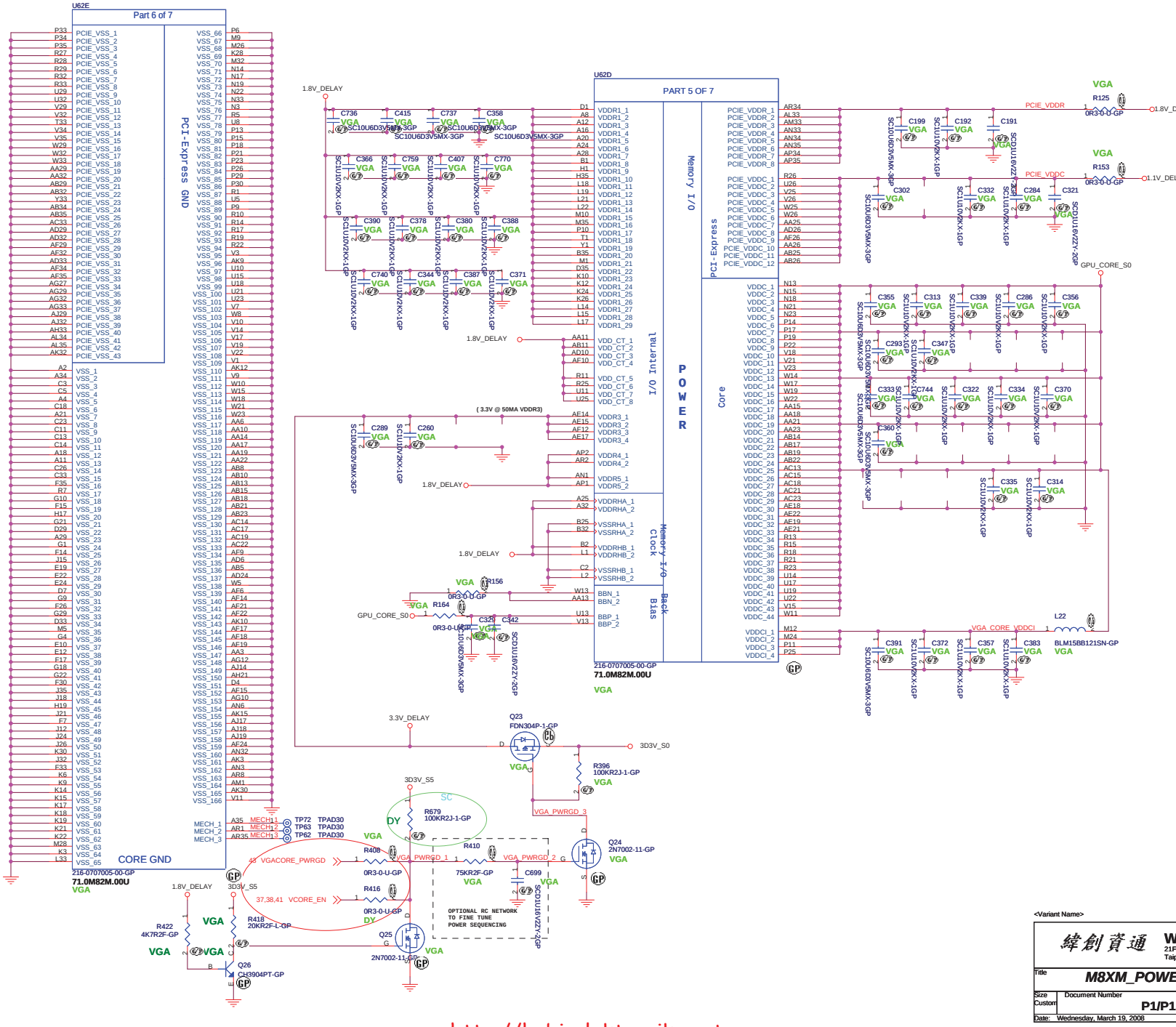
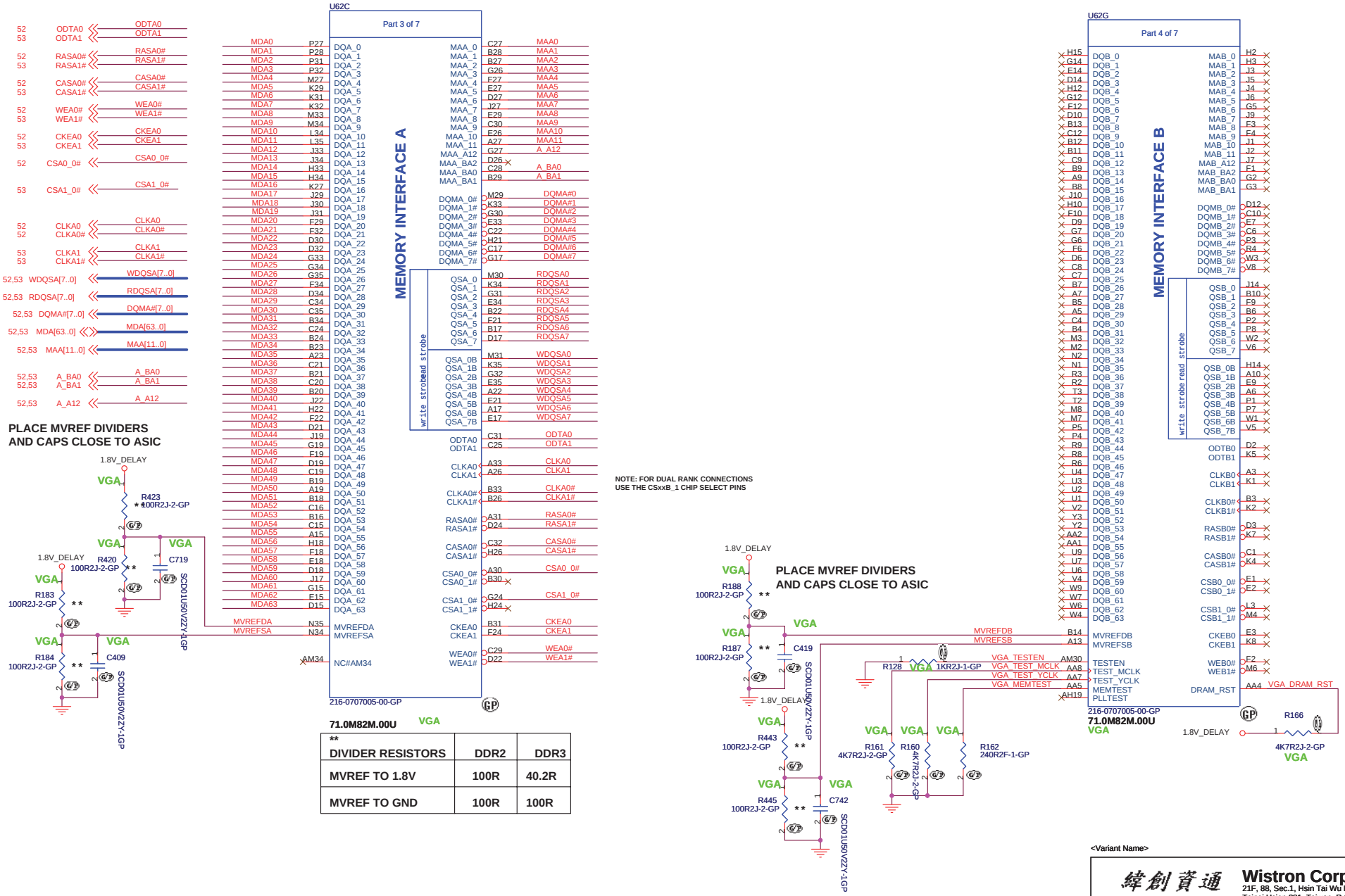
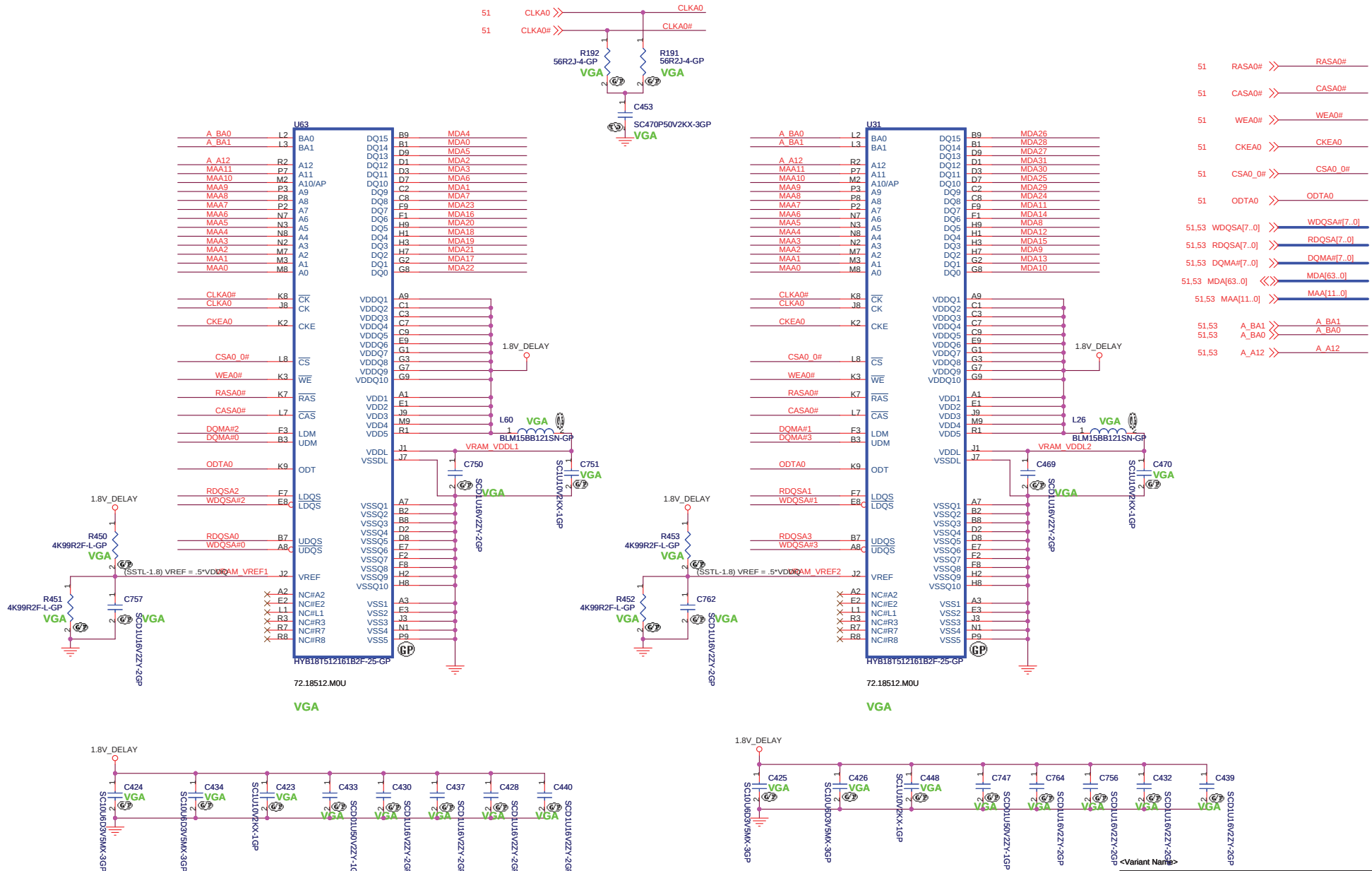
56







RASA0#
CASA0#
WEA0#
CKEA0
CSA0_0#
ODTA0
WDQSA#[7..0]
RDQSA[7..0]
DQMA#[7..0]
MDA[63..0]
MAA[11..0]
A_BA1
A_BA0
A_A12

緯創資通 **Wistron Corporation**
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Title: **VRAM DDR2 32MX16 A**

Size	Document Number	Rev
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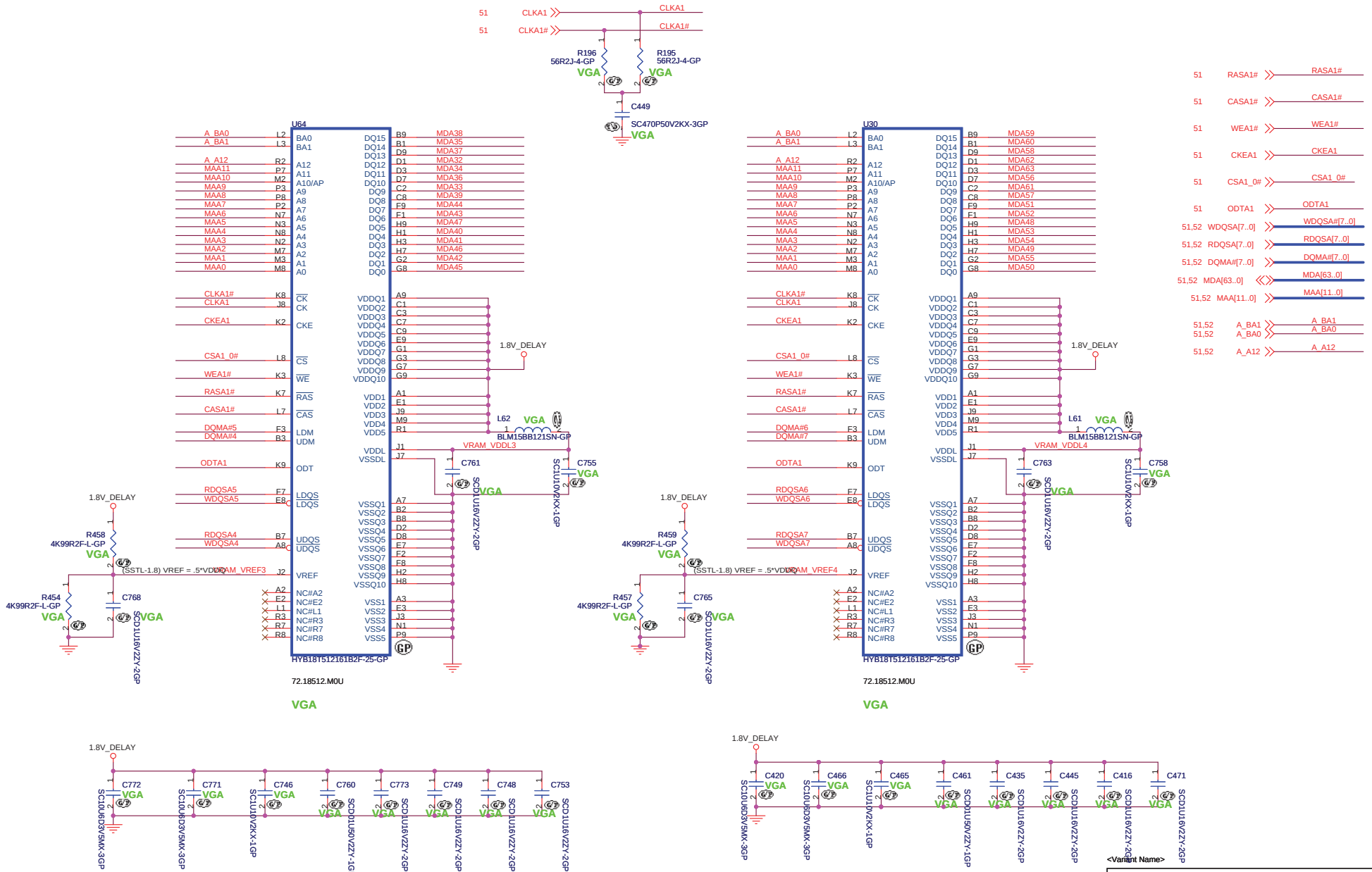
<Variant Name>



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM DDR2 32MX16 B**

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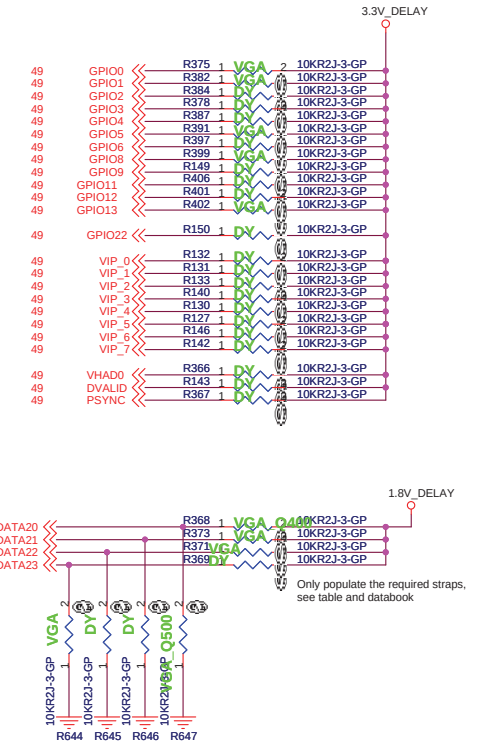
<Variant Name>

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

```
DVPDATA20 1
DVPDATA21 1   HY5PS121621CFP-25 Hynix
DVPDATA22 1      72.51216.F0U
DVPDATA23 1
```

```
DVPDATA20 1
DVPDATA21 1  HYB18T512161B2F-25  Qimonda 400MHz
DVPDATA22 1      72.18512.M0U
DVPDATA23 0
```

```
DVPDATA20 1
DVPDATA21 1  K4N51163QE-ZC25  Samsung
DVPDATA22 0      72.45116.A0U
DVPDATA23 1
```

```
DVPDATA20 0
DVPDATA21 1  HYB18T512161B2F-20  Qimonda 500MHz
DVPDATA22 1      72.18512.N0U
DVPDATA23 0
```


<Variant Name>

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Title: **STRAPS**

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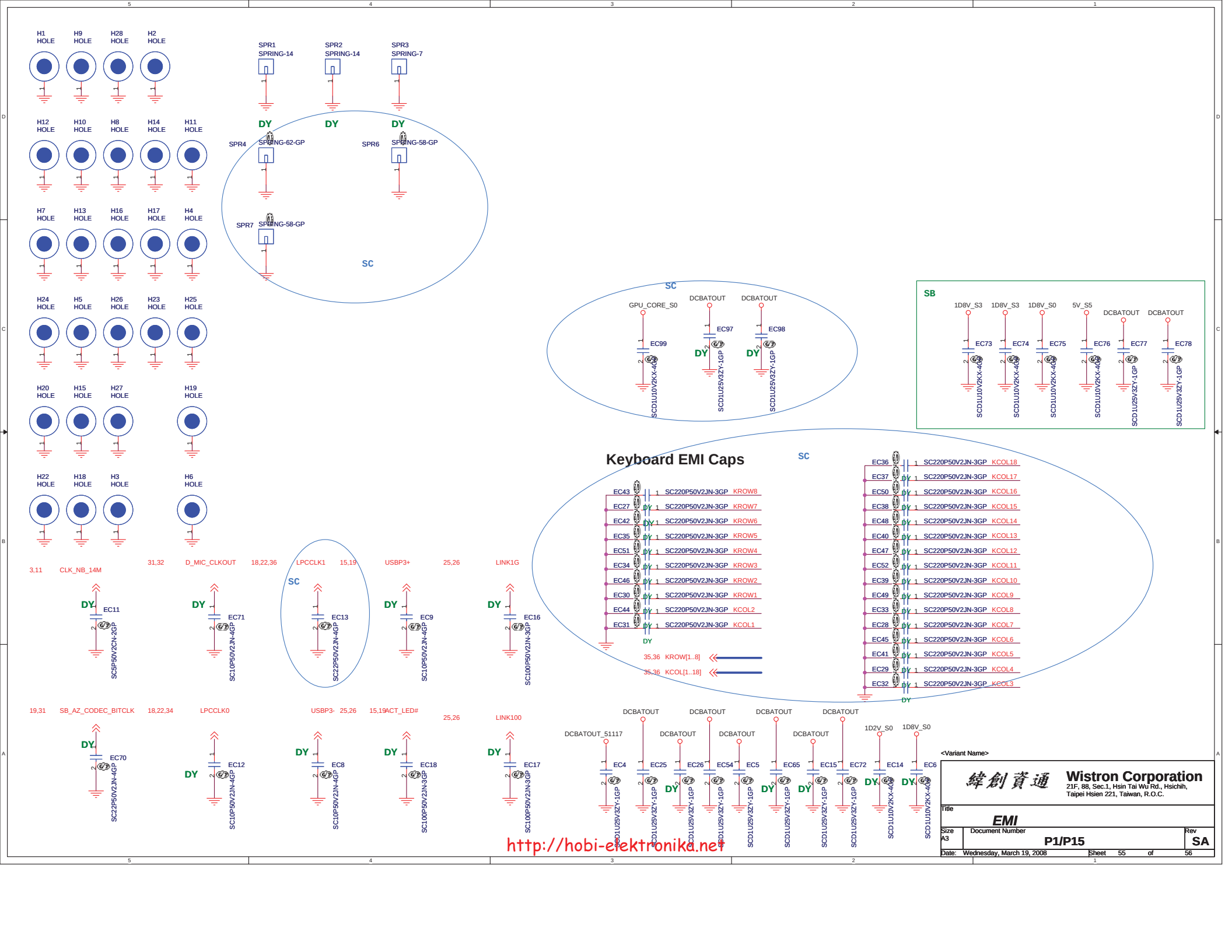
H1 HOLE
H9 HOLE
H28 HOLE
H2 HOLE
H12 HOLE
H10 HOLE
H8 HOLE
H14 HOLE
H11 HOLE
H7 HOLE
H13 HOLE
H16 HOLE
H17 HOLE
H4 HOLE
H24 HOLE
H5 HOLE
H26 HOLE
H23 HOLE
H25 HOLE
H20 HOLE
H15 HOLE
H27 HOLE
H19 HOLE
H22 HOLE
H18 HOLE
H3 HOLE
H6 HOLE
SPR1 SPRING-14
SPR2 SPRING-14
SPR3 SPRING-7
SPR4 SPRING-62-GP
SPR6 SPRING-58-GP
SPR7 SPRING-58-GP
DY
SC
GPU_CORE_S0
DCBATOUT
EC97
EC98
EC99
SCD1U25V3ZY-1GP
SB
1D8V_S3
1D8V_S0
5V_S5
EC73
EC74
EC75
EC76
EC77
EC78
SCD1U10V2KX-4GP
SCD1U25V3ZY-1GP
Keyboard EMI Caps
EC43
EC27
EC42
EC35
EC51
EC34
EC46
EC30
EC44
EC31
SC220P50V2JN-3GP
KROW8
KROW7
KROW6
KROW5
KROW4
KROW3
KROW2
KROW1
KCOL2
KCOL1
35,36 KROW[1..8]
35,36 KCOL[1..18]
EC36
EC37
EC50
EC38
EC48
EC40
EC47
EC52
EC39
EC49
EC33
EC28
EC45
EC41
EC29
EC32
KCOL18
KCOL17
KCOL16
KCOL15
KCOL14
KCOL13
KCOL12
KCOL11
KCOL10
KCOL9
KCOL8
KCOL7
KCOL6
KCOL5
KCOL4
KCOL3
3,11 CLK_NB_14M
31,32 D_MIC_CLKOUT
18,22,36 LPCCLK1
15,19 USBP3+
25,26 LINK1G
EC11
EC71
EC13
EC9
EC16
SC5P50V2CN-2GP
SC10P50V2JN-4GP
SC22P50V2JN-4GP
SC100P50V2JN-3GP
19,31 SB_AZ_CODEC_BITCLK
18,22,34 LPCCLK0
USBP3-
25,26
15,19 ACT_LED#
25,26 LINK100
EC70
EC12
EC8
EC18
EC17
DCBATOUT_51117
EC4
EC25
EC26
EC54
EC5
EC65
EC15
EC72
EC14
EC6
1D2V_S0
1D8V_S0
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI
Size A3
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NOTICE

1.VRAM and SIDE PORT GEOMETRY
2.digital array vendor

Change List

GEOMETRY

1.U60 62.10055.111 SKT-CPU638P-GP-U SKT-CPU638P-GP-U1 SKT-BGA638H176 SKT-BGA638H176

Common Part

1.RS780M_A13 U61 71.RS780.M12
2.SB700_A12 U67 71.SB700.M06
3.KBC U26 71.00773.00G
4.CLKGEN U33 71.09480.A03
5.SPDIF LOUT1 22.10270.031
6.MOSFET U53,U56 84.07686.037
7.MOSFET U11,U54,U55,U57 84.04634.037
8.H19,H20 34.4W601.001
9.U21 72.18512.M0U(QIMONDA)
10.card1 20.I0043.001
11.C861,C862,C941,C943 78.10324.2FL
12.C843,C844,C942,C944 63.R0034.1DL
13.USB2 22.10218.Z71
14.U70 71.00888.E0G
15.U32 74.51100.079
16.TC13 79.22719.2BL
17.ER1 63.15134.1DL
18.Add EC66 78.4R774.1FL
19.L42,L43,L44 68.00226.081

Common 2nd source

1.U21 72.45116.A0U
2.U58 74.09711.079

For P15

1.M82ME_A11 U62 71.M82ME.M01
2.8111C U1 71.08111.E03
3.JMB380 U46 71.00380.003
4.R12 64.24915.6DL
5.VRAM U30,U31,U63,U64 72.18512.M0U(QIMONDA400)

P15 2nd source

1.VRAM U30,U31,U63,U64 72.18512.N0U(QIMONDA500)

For P1

1.8101E U1 71.08101.B0G
2.JMB385 U46 71.JM385.A0G
3. R247,R253,R254,R255,R256,R620,C574 63.R0034.1DL
4. C573 63.00000.00L
5.R12 64.20015.6DL
6. R307,R163 64.14005.6DL
7.R316 68.00084.C71
8.C590,C591,C593,C594 78.10234.1FL
9.XF2 68.HD081.30A

<Variant Name>

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Title: CHANGE LIST
Size: A3
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